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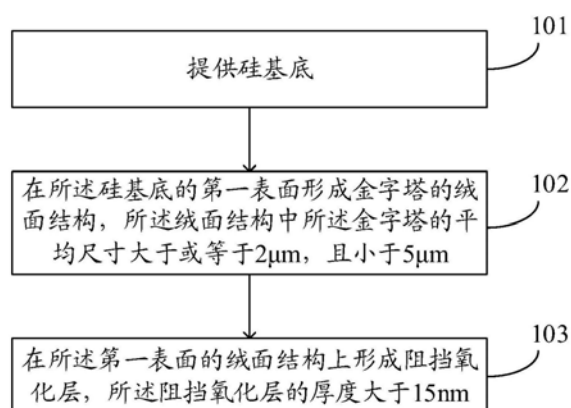
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(54) 发明名称

一种太阳能电池的制备方法以及太阳能电池

(57) 摘要

本发明提供了一种太阳能电池的制备方法，涉及太阳能光伏技术领域。其中，在制备太阳能电池的过程中，控制硅基底第一表面的绒面结构中金字塔的平均尺寸大于或等于 $2\mu\text{m}$ ，且小于 $5\mu\text{m}$ ，由于金字塔的平均尺寸较大，分布较为分散，因此，在通过金字塔结构保证硅基底反射率较低，光吸收较好的情况下，能够避免在绒面结构上形成厚度大于 15nm 的阻挡氧化层的过程中对绒面结构的破坏，此时，阻挡氧化层的厚度可以达到良好的掩膜作用，也同时避免了厚氧化层对太阳能电池性能的影响，显著提升太阳能电池的效率。



1. 一种太阳能电池的制备方法,其特征在于,所述方法包括:
提供硅基底;
在所述硅基底的第一表面形成金字塔的绒面结构,所述绒面结构中所述金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$;
在所述第一表面的绒面结构上形成阻挡氧化层,所述阻挡氧化层的厚度大于 15nm 。
2. 根据权利要求1所述的太阳能电池的制备方法,其特征在于,所述阻挡氧化层厚度大于 30nm 。
3. 根据权利要求1所述的太阳能电池的制备方法,其特征在于,所述绒面结构中所述金字塔的平均尺寸小于 $4\mu\text{m}$ 。
4. 根据权利要求1所述的太阳能电池的制备方法,其特征在于,所述在所述第一表面的绒面结构上形成阻挡氧化层,包括:
在 $600^{\circ}\text{C}\sim 1000^{\circ}\text{C}$ 的温度下,对所述第一表面进行热氧化形成阻挡氧化层。
5. 根据权利要求1所述的太阳能电池的制备方法,其特征在于,所述在所述第一表面的绒面结构上形成阻挡氧化层,包括:
对所述第一表面进行元素掺杂处理同步形成第一掺杂层和位于所述第一掺杂层上的阻挡氧化层,所述元素包括IIIA族元素、VA族元素中的至少一种。
6. 根据权利要求5所述的太阳能电池的制备方法,其特征在于,所述元素掺杂处理为热扩散工艺。
7. 根据权利要求1所述的太阳能电池的制备方法,其特征在于,所述在所述硅基底的第一表面形成金字塔的绒面结构的步骤之后,还包括:
对所述第一表面进行元素掺杂处理形成第一掺杂层,所述元素包括IIIA族元素、VA族元素中的至少一种;
所述在所述第一表面的绒面结构上形成阻挡氧化层,包括:
在所述第一表面的绒面结构上,对所述第一掺杂层热氧化形成阻挡氧化层。
8. 根据权利要求7所述的太阳能电池的制备方法,其特征在于,所述元素掺杂处理为热扩散工艺、离子注入或原位掺杂其中的一种。
9. 根据权利要求1~8任一项所述的太阳能电池的制作方法,其特征在于,所述基底的第二表面与第一表面相对,所述在所述第一表面的绒面结构上形成阻挡氧化层的步骤之后,还包括:
在所述基底的第二表面形成钝化接触结构,和/或,
在所述基底的第二表面形成钝化层。
10. 根据权利要求9所述的太阳能电池的制作方法,其特征在于,所述在所述基底的第二表面形成钝化接触结构,包括:
对基底第二表面进行刻蚀;
在基底的第二表面形成第一掺杂半导体层,同时在至少部分第一表面的阻挡氧化层上形成第一掺杂半导体层;
在第一表面阻挡氧化层对于硅基底第一表面的保护情况下,使用湿法处理过程去除第一表面的第一掺杂半导体层;
所述基底的第二表面和所述第一掺杂半导体层之间有隧穿钝化层,所述隧穿钝化层包

括:氧化硅。

11.一种太阳能电池,其特征在于,所述太阳能电池采用权利要求1~10任一项所述的太阳能电池的制作方法制作而成。

一种太阳能电池的制备方法以及太阳能电池

技术领域

[0001] 本发明涉及太阳能光伏技术领域,特别是涉及一种太阳能电池的制备方法以及太阳能电池。

背景技术

[0002] 在硅基太阳能电池的制备工艺中,为了降低硅片的表面反射率,增大对光的吸收,以提高太阳能电池的效率。通常,是采用化学腐蚀法在硅片的表面制备具备金字塔的绒面,金字塔的绒面可以对光线进行二次反射以及折射,从而增大对光的吸收,为了降低绒面的反射率,可以减小绒面中金字塔的尺寸,从而增强对光线的二次反射以及折射。

[0003] 在太阳能电池制备的过程中,为了避免绒面的金字塔结构在后续工艺中被破坏,通常需要在绒面上设置氧化层以隔离绒面与可能破坏绒面的环境,但是,制备氧化层也可能反而导致电池转化效率的降低。

发明内容

[0004] 本发明提供一种太阳能电池的制备方法以及太阳能电池,旨在避免太阳能电池的制备过程中制备保护作用的氧化层反而导致太阳能电池转化效率低的问题。

[0005] 第一方面,本发明实施例提供了一种太阳能电池的制备方法,该方法可以包括:

[0006] 提供硅基底;

[0007] 在所述硅基底的第一表面形成金字塔的绒面结构,所述绒面结构中所述金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$;

[0008] 在所述第一表面的绒面结构上形成阻挡氧化层,所述阻挡氧化层的厚度大于 15nm 。

[0009] 可选地,所述阻挡氧化层厚度大于 30nm 。

[0010] 可选地,所述绒面结构中所述金字塔的平均尺寸小于 $4\mu\text{m}$ 。

[0011] 可选地,所述在所述第一表面的绒面结构上形成阻挡氧化层,包括:

[0012] 在 $600^{\circ}\text{C}\sim 1000^{\circ}\text{C}$ 的温度下,对所述第一表面进行热氧化形成阻挡氧化层。

[0013] 可选地,所述在所述第一表面的绒面结构上形成阻挡氧化层,包括:

[0014] 对所述第一表面进行元素掺杂处理同步形成第一掺杂层和位于所述第一掺杂层上的阻挡氧化层,所述元素包括IIIA族元素、VA族元素中的至少一种。

[0015] 可选地,所述元素掺杂处理为热扩散工艺。

[0016] 可选地,所述在所述硅基底的第一表面形成金字塔的绒面结构的步骤之后,还包括:

[0017] 对所述第一表面进行元素掺杂处理形成第一掺杂层,所述元素包括IIIA族元素、VA族元素中的至少一种;

[0018] 可选地,所述在所述第一表面的绒面结构上形成阻挡氧化层,包括:

[0019] 在所述第一表面的绒面结构上,对所述第一掺杂层热氧化形成阻挡氧化层。

- [0020] 可选地,所述元素掺杂处理为热扩散工艺、离子注入或原位掺杂其中的一种。
- [0021] 可选地,所述基底的第二表面与第一表面相对,所述在所述第一表面的绒面结构上形成阻挡氧化层的步骤之后,还包括:
- [0022] 在所述基底的第二表面形成钝化接触结构,和/或,
- [0023] 在所述基底的第二表面形成钝化层。
- [0024] 可选地,所述在所述基底的第二表面形成钝化接触结构,包括:
- [0025] 对基底第二表面进行刻蚀;
- [0026] 在基底的第二表面形成第一掺杂半导体层,同时在至少部分第一表面的阻挡氧化层上形成第一掺杂半导体层;
- [0027] 在第一表面阻挡氧化层对于硅基底第一表面的保护情况下,使用湿法处理过程去除第一表面的第一掺杂半导体层;
- [0028] 所述基底的第二表面和所述第一掺杂半导体层之间有隧穿钝化层,所述隧穿钝化层包括:氧化硅。
- [0029] 第二方面,本发明实施例提供了一种太阳能电池,该太阳能电池由第一方面的太阳能电池的制备方法制备得到。
- [0030] 本发明实施例中,在制备太阳能电池的过程中,控制硅基底第一表面的绒面结构中金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$,由于金字塔的平均尺寸较大,分布较为分散,因此,在通过金字塔结构保证硅基底反射率较低,光吸收较好的情况下,能够在绒面结构上形成厚度大于 15nm 的阻挡氧化层的过程中对绒面结构的破坏,此时,阻挡氧化层的厚度可以达到良好的掩膜作用,也同时避免了厚氧化层对太阳能电池性能的影响,显著提升太阳能电池的效率。

附图说明

- [0031] 为了更清楚地说明本发明实施例的技术方案,下面将对本发明实施例的描述中所需要使用的附图作简单地介绍,显而易见地,下面描述中的附图仅仅是本发明的一些实施例,对于本领域普通技术人员来讲,在不付出创造性劳动性的前提下,还可以根据这些附图获得其他的附图。
- [0032] 图1示出了本发明实施例提供的第一种太阳能电池的制备方法的步骤流程图;
- [0033] 图2示出了本发明实施例提供的第二种太阳能电池的制备方法的步骤流程图;
- [0034] 图3示出了本发明实施例提供的一种电池基底结构示意图;
- [0035] 图4示出了本发明实施例提供的一种太阳能电池的结构示意图;
- [0036] 图5示出了本发明实施例提供的第三种太阳能电池的制备方法的步骤流程图;
- [0037] 图6示出了本发明实施例提供的另一种太阳能电池的结构示意图;
- [0038] 图7示出了本发明实施例提供的第四种太阳能电池的制备方法的步骤流程图;
- [0039] 图8示出了本发明实施例提供的又一种太阳能电池的结构示意图;
- [0040] 图9示出了本发明实施例提供的第五种太阳能电池的制备方法的步骤流程图;
- [0041] 图10示出了本发明实施例提供的第六种太阳能电池的制备方法的步骤流程图。
- [0042] 附图标记说明:
- [0043] 图4:301-硅基底;302-阻挡氧化层;

[0044] 图5:301-硅基底;303-第一钝化层;304-钝化隧穿层;305-第一掺杂半导体层;306-第二掺杂半导体层;307-第一电极;308-第二电极;309-第二钝化层;

[0045] 图6:501-硅基底;502-第一掺杂层;503-第一钝化层;504-第一电极;505-隧穿钝化层;506-第一掺杂半导体层;507-第二钝化层;508-第二电极;

[0046] 图7:701-硅基底;702-第一掺杂层;703-第一钝化层;704-第一电极;705-背面掺杂层;706-第二钝化层;707-第二电极。

具体实施方式

[0047] 下面将结合本发明实施例中的附图,对本发明实施例中的技术方案进行清楚、完整地描述,显然,所描述的实施例是本发明一部分实施例,而不是全部的实施例。基于本发明中的实施例,本领域普通技术人员在没有作出创造性劳动前提下所获得的所有其他实施例,都属于本发明保护的范围。

[0048] 图1示出了本发明实施例提供的第一种太阳能电池的制备方法的步骤流程图,如图1所示,该方法可以包括:

[0049] 步骤101、提供硅基底。

[0050] 本发明实施例中,硅基底可以是N型硅基底,也可以是P型硅基底,本发明实施例对此不作具体限制。

[0051] 步骤102、在所述硅基底的第一表面形成金字塔的绒面结构,所述绒面结构中所述金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$ 。

[0052] 本发明实施例中,在硅基底的第一表面形成金字塔的绒面结构前,可以对硅基底的第一表面进行清洗,以去除切片、研磨、倒角、抛光等工序中吸附在硅基底表面的杂质。

[0053] 本发明实施例中,可以对硅基底的第一表面进行“表面织构化”处理,如可以利用碱溶液对硅基底的第一表面进行各向异性腐蚀,从而在硅表面形成包含金字塔的绒面结构,包含金字塔的绒面结构可以对光线进行多次反射,降低了硅基底表面反射率,有效提高了入射太阳光的利用率,从而提高光生电流密度,提高了太阳能电池的转化效率。

[0054] 本发明实施例中,将绒面结构中金字塔的底边对边距离作为金字塔的尺寸,在对硅基底的第一表面制绒的过程中,可以控制绒面结构中金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$ 。可选地,可以通过调整制绒过程中反应的时间、溶液的配比,从而调整绒面结构中金字塔的平均尺寸,避免平均尺寸较小时金字塔密集分布,在后续形成阻挡氧化层时被破坏的问题,从而显著提升电池成品的转化效率;也避免金字塔的平均尺寸过大,导致降低反射率的效果较差,电池的转化效率较低。可选地,绒面结构中金字塔的平均尺寸可以是 $2\mu\text{m}$ 、 $3\mu\text{m}$ 、 $4\mu\text{m}$ 、 $4.5\mu\text{m}$ 等大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$ 的任意尺寸,本发明实施例对此不作具体限制。

[0055] 步骤103、在所述第一表面的绒面结构上形成阻挡氧化层,所述阻挡氧化层的厚度大于 15nm 。

[0056] 在现有的太阳能电池的制备工艺中,在硅基底表面形成金字塔的绒面后,通常需要制备较厚的氧化层作为阻挡层或保护层,以免后续工艺对绒面的破坏。但是,在实际制备中发现,为了保证阻挡层的保护效果需要氧化层的厚度较高,但是,氧化层在绒面上金字塔的塔尖处生长速率较快,从而使得氧化层的厚度较高时反而会破坏绒面的金字塔结构,如

金字塔的平均尺寸小于 $2\mu\text{m}$ 的绒面,使得电池性能严重下降,不利于提高电池转换效率,而氧化层厚度较低时保护效果较差,又可能导致金字塔的绒面在后续工艺中遭到破坏,影响电池转换效率。

[0057] 本发明实施例中,在硅基底第一表面为金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$ 的绒面结构的情况下,能够有效避免阻挡氧化层对绒面结构的破坏,因此,可以在第一表面的绒面结构上形成较厚的阻挡氧化层,其中,阻挡氧化层指太阳能电池工艺中用于保护硅基底的表面绒面结构的氧化层,通常来说,阻挡氧化层的厚度越厚对绒面结构的保护效果越好,从而能够保证电池性能,本发明在较厚的阻挡氧化层工艺中,能够显著提高电池的转换效率,可选地,阻挡氧化层的厚度可以大于 15nm ,如可以是 15.5nm 、 16nm 、 20nm 、 30nm 、 50nm 、 100nm 、 120nm 等 15nm 以上的厚度。

[0058] 本发明实施例中,可以根据电池具体的应用需求,对硅基底上除第一表面外的其他表面进行处理,或者在硅基底第一表面或其他表面上进一步形成其他功能层,可选地,可以是对硅基底上第一表面相对的第二表面进行抛光或刻蚀,本发明实施例对此不作具体限制。

[0059] 本发明实施例中,在制备太阳能电池的过程中,控制硅基底第一表面的绒面结构中金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$,由于金字塔的平均尺寸较大,分布较为分散,因此,在通过金字塔结构保证硅基底反射率较低,光吸收较好的情况下,能够避免在绒面结构上形成厚度大于 15nm 的阻挡氧化层的过程中对绒面结构的破坏,此时,阻挡氧化层的厚度可以达到良好的掩膜作用,也同时避免了厚氧化层对太阳能电池性能的影响,显著提升太阳能电池的效率。

[0060] 图2示出了本发明实施例提供的第二种太阳能电池的制备方法的步骤流程图,如图2所示,该方法包括:

[0061] 步骤201、提供硅基底。步骤202、在所述硅基底的第一表面形成金字塔的绒面结构,所述绒面结构中所述金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$ 。

[0062] 本发明实施例中,步骤201至步骤202可对应参照前述步骤101至步骤102的相关描述,为避免重复,在此不再赘述。可选地,在硅基底的第一表面形成金字塔的绒面结构后,可以调整硅基底第一表面的反射率小于 12% 。

[0063] 可选地,所述绒面结构中所述金字塔的平均尺寸小于 $4\mu\text{m}$ 。

[0064] 本发明实施例中,进一步的可以调整绒面结构中金字塔的平均尺寸小于 $4\mu\text{m}$,即使得绒面结构中金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $4\mu\text{m}$,从而在避免厚的阻挡氧化层影响绒面结构的同时,保证绒面结构对光反射率的较高效果。

[0065] 步骤203、在 $600^{\circ}\text{C}\sim 1000^{\circ}\text{C}$ 的温度下,对所述第一表面进行热氧化形成阻挡氧化层。

[0066] 本发明实施例中,步骤203可对应参照前述步骤103的相关描述,为避免重复,在此不再赘述。

[0067] 本发明实施例中,可以通过热氧化法在硅基底的第一表面制备阻挡氧化层,可选地,热氧化法可以是干氧热氧化法,也可以是湿氧热氧化法,其中,干氧热氧化法采用氧气实现,湿氧热氧化法采用氧气和水实现;可选地,在记性热氧化的过程中,可以将温度控制在 $600^{\circ}\text{C}\sim 1000^{\circ}\text{C}$,如可以是 600°C 、 650°C 、 700°C 、 800°C 、 900°C 、 1000°C 等 $600^{\circ}\text{C}\sim 1000^{\circ}\text{C}$ 的

任意温度。

[0068] 可选地,所述阻挡氧化层的厚度大于30nm。

[0069] 本发明实施例中,由于现有技术中氧化层的厚度越厚,对绒面的金字塔结构破坏越多,对绒面减反射的效果影响越大,因此,本发明实施例中在阻挡氧化层的厚度越厚时,相比于现有技术对绒面的金字塔结构的保存效果越好,有效提升电池转换效率,此时,在大于15nm的基础上,可以调整阻挡氧化层的厚度大于30nm,或大于70nm,本发明实施例对此不作具体限制。

[0070] 本发明实施例中,为了避免在对硅基底的第一表面形成阻挡氧化层的过程中,硅基底的其他表面也形成对应的氧化层,因此,可以在热氧化前对其他表面进行保护,以防止对应的氧化层的形成,或者,也可以在形成阻挡氧化层后,对其他表面上的氧化层进行去除,以避免对后续工艺的影响。

[0071] 图3示出了本发明实施例提供的一种电池基底结构示意图,如图3所示,该电池基底30包括硅基底301、阻挡氧化层302,其中,硅基底301与阻挡氧化层302之间还可以包括其他功能层,如掺杂层等,本发明实施例对此不作具体限制。

[0072] 如图3所示的电池基底结构中阻挡氧化层302的厚度为100nm,在900℃下在硅基底301的第一表面的绒面结构上通过干氧化法或湿氧化法形成。可选地,为了适应不同的应用需求,还可以对图3所示的电池基底结构的第二表面进行抛光处理,如将硅基301置于含有氢氧化钾或氢氧化钠的碱溶液中,在大于或等于60℃的温度下进行抛光处理,使得第二表面成为抛光面,获得电池基底结构,此时,阻挡氧化层302可起到保护第一表面上绒面结构的作用;再去除阻挡氧化层302,并在第一表面和第二表面上分别形成其他需求的功能层,以获得不同的太阳能电池。

[0073] 图4示出了本发明实施例提供的一种太阳能电池的结构示意图,在电池基底结构的基础上,可以制备IBC(Interdigitated back contact,背接触式)电池如图4所示,在图3的基础上,IBC电池包括硅基底301、第一钝化层303、钝化隧穿层304、第一掺杂半导体层305、第二掺杂半导体层306、第一电极307、第二电极308、第二钝化层309。

[0074] 本发明实施例中,在制备太阳能电池的过程中,控制硅基底第一表面的绒面结构中金字塔的平均尺寸大于或等于2 μm ,且小于5 μm ,由于金字塔的平均尺寸较大,分布较为分散,因此,在通过金字塔结构保证硅基底反射率较低,光吸收较好的情况下,能够在绒面结构上形成厚度大于15nm的阻挡氧化层的过程中对绒面结构的破坏,此时,阻挡氧化层的厚度可以达到良好的掩膜作用,也同时避免了厚氧化层对太阳能电池性能的影响,显著提升太阳能电池的效率。

[0075] 图5示出了本发明实施例提供的第三种太阳能电池的制备方法的步骤流程图,如图5所示,该方法包括:

[0076] 步骤401、提供硅基底。

[0077] 步骤402、在所述硅基底的第一表面形成金字塔的绒面结构,所述绒面结构中所述金字塔的平均尺寸大于或等于2 μm ,且小于5 μm 。

[0078] 本发明实施例中,步骤401至步骤402可对应参照前述步骤中101至步骤102的相关描述,为避免重复,在此不再赘述。

[0079] 步骤403、对所述第一表面进行元素掺杂处理同步形成第一掺杂层和位于所述第

一掺杂层上的阻挡氧化层,所述元素包括IIIA族元素、VA族元素中的至少一种,所述阻挡氧化层的厚度大于15nm。

[0080] 本发明实施例中,可以是对第一表面进行元素掺杂处理的同时,同步形成位于第一掺杂层上的阻挡氧化层,可选地,其中,掺杂的元素可以是IIIA族元素、VA族元素中的至少一种,即硼族元素、氮族元素中的至少一种,本发明实施例对此不作具体限制。

[0081] 可选地,所述步骤403中所述元素掺杂处理为热扩散工艺。

[0082] 本发明实施例中,可以采用整面形成掺杂源,采用热扩散工艺的元素驱入方式通过加热设备对第一表面进行元素掺杂,此时,可以将硅基底置于氧化气氛中,从而在元素掺杂的同时,基于热扩散工艺条件形成第一掺杂层上的阻挡氧化层。

[0083] 可选地,所述IIIA族元素可以为硼元素,所述步骤403具体包括:在850℃~1100℃的温度下,采用溴化硼或氯化硼对所述第一表面进行管式热扩散以同步形成硼元素掺杂的第一掺杂层,以及位于所述第一掺杂层上的阻挡氧化层。

[0084] 本发明实施例中,可以选择IIIA族元素的硼元素对硅基底的第一表面进行掺杂,此时,元素掺杂可以在850℃~1100℃的温度下进行,可选地,该温度可以是850℃、900℃、1000℃、1100℃等850℃~1100℃中的任意温度,本发明实施例对此不作具体限制。

[0085] 可选地,所述VA族元素为磷元素,所述步骤403具体包括在700℃~900℃的温度下,采用三氯氧磷对所述第一表面进行管式热扩散以同步形成磷元素掺杂的第一掺杂层,以及位于所述第一掺杂层上的阻挡氧化层。

[0086] 本发明实施例中,可以选择VA族元素为磷元素对硅基底的第一表面进行掺杂,此时,元素掺杂可以在700℃~900℃的温度下进行,可选地,该温度可以是700℃、750℃、800℃、900℃等700℃~900℃中的任意温度,本发明实施例对此不作具体限制。

[0087] 可选地,所述基底的第二表面与第一表面相对。

[0088] 步骤404、在所述基底的第二表面形成钝化接触结构。

[0089] 本发明实施例中,根据制备的太阳能电池的类型、应用领域等,可以在基底上与第一表面相对的第二表面形成不同的结构,如可以在基底的第二表面形成钝化接触结构,钝化接触结构是一种既能实现背面正面钝化,且无需开孔接触的制备工艺,避免了接触范围限制于开孔区域扩大了接触范围,并无需开孔简化了制备工艺。

[0090] 可选地,所述步骤404包括:

[0091] 步骤S11、对基底第二表面进行刻蚀。

[0092] 本发明实施例中,对硅基底的刻蚀可以通过链式酸溶液进行酸刻蚀,也可以通过碱溶液进行碱刻蚀,如在酸刻蚀的情况下,可以使用氢氟酸、硝酸的混合溶液,去除第二表面上部分的硅基底以进行刻蚀,可选地,混合溶液还可以包括硫酸溶液等,从而在提供酸性离子的同时,保证溶液密度与溶液表面张力;在碱刻蚀的情况下,可以使用氢氧化钾、氢氧化钠、三甲基氧化铵等,在对第二表面进行刻蚀的同时,避免对第一表面的阻挡氧化层、第一掺杂层等造成破坏。

[0093] 本发明实施例中,在对第二表面进行刻蚀前,可以去除第二表面的氧化层或绕扩散的第一掺杂层,从而避免电池完成制备后P和N共掺杂造成的漏电问题,提高产品的良率和可靠性。

[0094] 本发明实施例中,在刻蚀前还可以对第二表面进行清洗,如采用氢氟酸对第二表

面进行清洗,在清洗杂质后获得表现疏水状态的第二表面,不易于沾污,便于快速烘干,可选地,清洗还可以包括水洗、氯化氢酸洗、臭氧水洗等,本发明实施例对此不作具体限制。

[0095] 步骤S12、在基底的第二表面形成第一掺杂半导体层,同时在至少部分第一表面的阻挡氧化层上形成第一掺杂半导体层。

[0096] 本发明实施例中,在对第二表面进行刻蚀后,可以在第二表面上形成第一掺杂半导体层,其中,第一掺杂半导体层可以先沉积半导体层,再对半导体层进行元素掺杂得到,也可以在沉积半导体层的过程中原位掺杂得到,第一掺杂半导体层与第一掺杂层的导电类型不同,此时,可以采用三氯氧磷,通过磷离子注入退火、APCVD (Atmospheric Pressure Chemical Vapor Deposition,常压化学气相沉积) 磷硅玻璃加热推进等方式进行掺杂获得第一掺杂半导体层,具体可对应参照前述第一表面元素掺杂处理的相关描述,为避免重复,在此不再赘述。

[0097] 本发明实施例中,第一表面的阻挡氧化层在第二表面的掺杂处理过程中,会对第一表面的通过元素掺杂形成的发射极起到保护的作用,防止不同杂质元素的共掺杂和短路的问题,提高电池的良品率。

[0098] 可选地,所述半导体层的材料包括硅薄膜、碳化硅薄膜中的至少一种;

[0099] 可选地,所述半导体层的材料的晶体形貌包括多晶形貌、非晶形貌、微晶形貌、纳米形貌中的至少一种。

[0100] 本发明实施例中,半导体层的材料可以是硅薄膜、碳化硅薄膜中的至少一种,如半导体层可以是硅薄膜膜层、碳化硅薄膜膜层或硅薄膜和碳化硅薄膜的复合膜层;半导体层的材料的晶体形貌可以包括多晶形貌、非晶形貌、微晶形貌、纳米形貌中的至少一种,如半导体层的材料可以是多晶硅、非晶硅、微晶硅、纳米硅,或者多晶碳化硅、非晶碳化硅等,本发明实施例对此不作具体限制。

[0101] 可选地,所述步骤S12包括:

[0102] 步骤S121、在所述第二表面上沉积半导体层,并在沉积所述半导体层的过程中,同步对所述半导体层进行元素掺杂处理,获得所述第一掺杂半导体层。

[0103] 本发明实施例中,可以采用原位掺杂方法进行第一掺杂半导体层的制备,即在形成半导体层的过程中同时对半导体层进行元素掺杂,进一步的还可以在半导体层进行原位掺杂后,对其进行700℃~1000℃的退火处理,以获得更高质量的第一掺杂半导体层。

[0104] 本发明实施例中,在原位掺杂方法中退火时会通入一定量的氧气,从而导致第一掺杂半导体层上可能形成氧化层,该氧化层在后续工艺中可以对第一掺杂半导体层起阻挡作用,避免第一掺杂半导体层被碱溶液破坏。

[0105] 或,

[0106] 可选地,所述步骤S12,包括:

[0107] 步骤S122、在所述第二表面上沉积半导体层;

[0108] 步骤S123、对所述半导体层进行元素掺杂处理,获得所述第一掺杂半导体层。

[0109] 本发明实施例中还可以采用非原位掺杂方法,即先沉积本征类型的半导体层,在半导体层沉积完成后在对半导体层进行元素掺杂处理,以形成第一掺杂半导体层,可选地,对半导体层的掺杂方法包括管式热扩散方法、离子注入后退火方法、掺杂源涂布推进方法等,本发明实施例对此不作具体限制。

[0110] 本发明实施例中,半导体层的形成方法可以包括CVD (Chemical Vapour Deposition,气相沉积法方法)、PVD (Physical Vapor Deposition,物理气相沉积) 方法等,所述CVD方法包括LPCVD (Low Pressure Chemical Vapor Deposition,低压力化学气相沉积法)、PECVD、APCVD、HWCVD (Hot Wire Chemical Vapour Deposition,热丝气相沉积法方法) 中的至少一种;所述PVD方法包括磁控溅射,在原位掺杂方法、非原位掺杂方法中,均可以选用上述方式形成本征类型的半导体层或原位掺杂的第一掺杂半导体层。

[0111] 可选地,所述半导体层的厚度为20nm~500nm。

[0112] 本发明实施例中,半导体层的厚度可以为20nm~500nm间的任意数值,如20nm、50nm、100nm、300nm、500nm等。

[0113] 步骤S13、在第一表面阻挡氧化层对于硅基底第一表面的保护情况下,使用湿法处理过程去除第一表面的第一掺杂半导体层。

[0114] 本发明实施例中,在第二表面上制备第一掺杂半导体层,可能导致第一表面形成绕扩散的第一掺杂半导体层,此时,可以先保留第一表面的阻挡氧化层,对第一表面上绕扩散的第一掺杂半导体层进行去除,可选地,第一掺杂半导体层受限于工艺条件可能还会形成氧化层,在去除阻挡氧化层前也应对其进行去除。如,采用链式碱清洗工艺去除所述第一表面的绕镀的、主要为非晶形态或者多晶形态的第一掺杂半导体层,可选地,可以采用滚轮式或者履带式的链式单面去膜工艺去除,其中包括一个或者多个槽体,槽体中的液面与硅基底高度对应,将包括第一掺杂半导体层的硅基底的第一表面向下浸入液面从槽体中经过,槽体中可以包括氢氧化钾或者氢氧化钠溶液,则硅基底的第一表面上绕镀的第一掺杂半导体层被去除,第二表面的第一掺杂半导体层被完全保留或者部分保留。可选地,单面链式去膜工艺中还可以加入水膜装置,水膜装置在硅基底第一表面喷淋水,从而形成水膜,水膜可以防止在硅基底经过槽体时第二表面的第一掺杂半导体层被去除。

[0115] 本发明实施例中,可选地,当第一掺杂半导体层表面有氧化层时,也可以使用槽式碱清洗工艺,该氧化层可以在原位掺杂方法中经氧化或者由氧退火方法形成,也可以在非原位掺杂的掺杂过程、或者元素扩散等过程中形成,可以将硅基底浸入槽式清洗碱溶液中去除第一表面绕扩散的第一掺杂半导体层,利用链式单面去膜工艺去除了第一表面的氧化层,全部或部分保留了第二表面的氧化层,使得浸泡式的槽式碱清洗中,第一表面的绕镀的第一掺杂半导体层被去除,而第二表面的第一掺杂半导体层得到氧化层的保护不被破坏。

[0116] 本发明实施例中,单面链式去膜工艺中还可以加入去膜后的水洗程序,用来清洗残留的氢氟酸等去膜溶液,防止残留液体对后续工艺造成影响,可选地,在此水洗过程前,还可以增加含有盐酸溶液的清洗,以进一步降低基底表面的金属离子残留,氯离子的络合作用可以极大的降低金属离子含量,避免金属离子对太阳能电池的性能影响。可选地,还可以增加烘干步骤,使得硅基底表面干燥,防止沾染空气中或者工装夹具的灰尘、杂质。

[0117] 本发明实施例中,在对第一表面和第二表面分别进行元素掺杂处理获得第一掺杂层与第一掺杂半导体层后,可以去除第一掺杂层上的阻挡氧化层,可选地,可以采用链式、槽式的氢氟酸溶液进行清洗,进一步的,还可以包括其他清洗步骤,如采用盐酸、臭氧水、水洗等,保证清洁的效果,去除第一氧化层后,第一表面的反射率应小于14%,从而保留了第一表面低反射率的绒面结构,提高了电池的转换效率。另外,在第二表面的处理步骤中可能导致第二表面形成了其他氧化层,可选地,也可以对第二表面上的氧化层进行去除,本发明

实施例对此不作具体限制。

[0118] 可选地,所述基底的第二表面和所述第一掺杂半导体层之间有隧穿钝化层,所述隧穿钝化层包括:氧化硅。

[0119] 本发明实施例中,在基底的第二表面和第一掺杂半导体层之间还有隧穿钝化层,可选地,隧穿钝化层的材质可以是介电层,隧穿钝化层的材料可以选自氢化非晶硅、氮氧硅、碳化硅、氮化硅、氧化铝、氧化硅中的至少一种,本发明实施例对此不作具体限制。具体的,隧穿钝化层可以是氧化硅。

[0120] 可选地,隧穿钝化层的厚度为0.5nm~5nm。

[0121] 本发明实施例中,隧穿钝化层的厚度可以为0.5~5nm间的任意数值,如0.5nm、1nm、3nm、5nm等,本发明实施例对此不作具体限制。

[0122] 可选地,在通过原位掺杂方法制备第一掺杂半导体层时,可以对第一掺杂半导体层进行退火处理,从而将第二表面上主要为非晶形态的半导体层转为主要为多晶态的第一掺杂半导体层。在此过程中,隧穿钝化层中也会产生隧穿针孔,隧穿针孔有利于第二表面的隧穿钝化层在保证钝化效果的同时更好的进行载流子传输,提高电池的效率。

[0123] 本发明实施例中,还可以在所述第一掺杂层、钝化接触结构上形成其他功能层,如钝化层、电极等,从而得到太阳能电池。可选地,对第一掺杂层的硼掺杂工艺也可以替换为相应的磷掺杂工艺,例如溴化硼扩散或者氯化硼扩散可以替换为三氯氧磷热扩散,本领域技术人员可以根据工艺、应用需求调整各湿法清洗或者电极的形成过程,本发明实施例对此不做具体限制。

[0124] 图6示出了本发明实施例提供的另一种太阳能电池的结构示意图,如图6所示,该太阳能电池包括硅基底501、第一掺杂层502、第一钝化层503、第一电极504、隧穿钝化层505、第一掺杂半导体层506、第二钝化层507、第二电极508。具体的,通过步骤401至步骤404所述的太阳能电池的制备方法,图6所示的太阳能电池的制备过程如下所示:

[0125] 提供硅基底501;

[0126] 采用碱溶液对硅基底501的第一表面进行织构化处理获得金字塔的平均尺寸为2 μ m的绒面结构;

[0127] 在700℃~1100℃下,采用溴化硼或氯化硼管式热扩散对所述第一表面进行硼扩散处理形成硼掺杂的第一掺杂层502,并在第一掺杂层502上形成厚度为100nm的阻挡氧化层,第一掺杂层502的表面掺杂浓度为 $N_1=1\times 10^{17}\sim 5\times 10^{21}\text{cm}^{-3}$;

[0128] 对硅基底501的第二表面进行链式酸溶液或碱溶液的刻蚀,并除去在形成第一掺杂层502以及阻挡氧化层的过程中扩散至第二表面上的绕镀层;

[0129] 在第二表面上形成隧穿钝化层505,并在隧穿钝化层505上形成磷元素掺杂的第一掺杂半导体层506,其中,采用原位掺杂方法时使用磷化氢等气体作为掺杂源气体,非原位掺杂方法中则可以使用三氯氧磷等作为掺杂源;

[0130] 使用链式碱清洗或槽式碱清洗去除在制备第一掺杂半导体层506的过程中第一表面上形成的绕镀层;

[0131] 采用链式或槽式的氢氟酸溶液去除第一掺杂层502上的阻挡氧化层;

[0132] 在第一掺杂层502上形成第一钝化层503,在第一掺杂半导体层506上形成第二钝化层507;

[0133] 在第一钝化层502上形成第一电极504,在第一掺杂半导体层506上形成第二电极508。

[0134] 本发明实施例中,在制备太阳能电池的过程中,控制硅基底第一表面的绒面结构中金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$,由于金字塔的平均尺寸较大,分布较为分散,因此,在通过金字塔结构保证硅基底反射率较低,光吸收较好的情况下,能够避免形成厚度大于15nm的阻挡氧化层的过程中对绒面结构的破坏,此时,阻挡氧化层的厚度可以达到良好的掩膜作用,也同时避免了厚氧化层对太阳能电池性能的影响,显著提升太阳能电池的效率。

[0135] 图7示出了本发明实施例提供的第三种太阳能电池的制备方法的步骤流程图,如图7所示,该方法可以包括:

[0136] 步骤601、提供硅基底。

[0137] 步骤602、在所述硅基底的第一表面形成金字塔的绒面结构,所述绒面结构中所述金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$ 。

[0138] 本发明实施例中,步骤601至步骤602可对应参照前述步骤中101至步骤102的相关描述,为避免重复,在此不再赘述。

[0139] 步骤603、对所述第一表面进行元素掺杂处理同步形成第一掺杂层和位于所述第一掺杂层上的阻挡氧化层,所述元素包括IIIA族元素、VA族元素中的至少一种,所述阻挡氧化层的厚度大于15nm。

[0140] 本发明实施例中,步骤603可对应参照前述步骤403的相关描述,为避免重复,在此不做赘述。

[0141] 可选地,所述基底的第二表面与第一表面相对。

[0142] 步骤604、在所述基底的第二表面形成钝化层。

[0143] 本发明实施例中,除在第二表面上形成钝化接触结构外,也可以直接在基底的第二表面上形成钝化层,从而抑制第二表面上的不同缺陷,可选地,可以通过PECVD (Plasma Enhanced Chemical Vapor Deposition,等离子体增强化学气相沉积法)、原子层沉积等方法形成钝化层,本发明实施例对此不作具体限制。

[0144] 可选地,所述钝化层的材料包括氮化硅、氧化硅、氮氧化硅、氧化铝、碳化硅、非晶硅中的至少一种。

[0145] 本发明实施例中,还可以在第二表面上形成钝化层,不同钝化层的材料可以相同,也可以不同,且钝化层可以是单层也可以是两层以上,可以采用一种材料也可以采用两种以上的材料,如钝化层可以选择氮化硅、氧化硅、氮氧化硅、氧化铝、碳化硅、非晶硅中的至少一种材料,本发明实施例对此不作具体限制。

[0146] 本发明实施例中,还可以在钝化层上制备电极,电极的制备可以采用不同的金属化制备方法,如PVD (Physical Vapour Deposition,物理气相沉积) 方法、丝网印刷方法、电镀方法、无电镀方法、激光转印方法、喷涂方法中的一种或两种以上;可选地,在电极形成过程中,可以包括一个或两个以上温度处理过程,其中,温度的范围可以是 $100^{\circ}\text{C}\sim 900^{\circ}\text{C}$;可选地,不同钝化层分别对应的电极可以分别独立的选择银、铜、铝、镍、钛、钨、锡中的至少一种材料,本发明实施例对此不作具体限制。

[0147] 本发明实施例中,可以使用丝网印刷的方式印刷含银、铜的浆料,然后通过 500°C

~900℃的烧结工艺或退火工艺完成制备电极,或也可以先使用PVD方法制备种子层,再图形化该种子层,然后再利用电镀方法制备电极,最后辅助以退火形成电极,或也可以使用无电镀方法形成种子层,然后利用电镀方法加厚,最后使用退火完成电极制备,本发明实施例对电极制备的方法不作具体限制。

[0148] 图8示出了本发明实施例提供的又一种太阳能电池的结构示意图,如图8所示,该太阳能电池包括硅基底701、第一掺杂层702、第一钝化层703、第一电极704、背面掺杂层705、第二钝化层706、第二电极707。具体的,通过步骤601至步骤604所述的太阳能电池的制备方法,图8所示的太阳能电池的制备过程如下所示:

[0149] 提供硅基底701;

[0150] 采用碱溶液对硅基底701的第一表面进行织构化处理获得金字塔的平均尺寸为2.5μm的绒面结构;

[0151] 在700℃~1100℃下,采用溴化硼或氯化硼管式热扩散对所述第一表面进行硼扩散处理形成硼掺杂的第一掺杂层702,并在第一掺杂层702上形成厚度为70nm的阻挡氧化层,第一掺杂层702的表面掺杂浓度为 $N_1 = 1 \times 10^{17} \sim 5 \times 10^{21} \text{ cm}^{-3}$;

[0152] 对硅基底701的第二表面进行链式酸溶液或碱溶液的刻蚀;

[0153] 对第二表面进行磷掺杂处理获得背面掺杂层705;

[0154] 采用链式或槽式的氢氟酸溶液去除第一掺杂层702上的阻挡氧化层;

[0155] 在第一掺杂层702上形成第一钝化层703,在背面掺杂层705上形成第二钝化层706;

[0156] 在第一钝化层703上形成第一电极704,在第二钝化层706上形成第二电极707。

[0157] 本发明实施例中,可选地,对第一掺杂层的硼掺杂工艺可以替换为相应的磷掺杂工艺,例如溴化硼扩散或者氯化硼扩散可以替换为三氯氧磷热扩散,本领域技术人员可以根据工艺、应用需求调整各湿法清洗或者电极的形成过程,本发明实施例对此不做具体限制。

[0158] 本发明实施例中,在制备太阳能电池的过程中,控制硅基底第一表面的绒面结构中金字塔的平均尺寸大于或等于2μm,且小于5μm,由于金字塔的平均尺寸较大,分布较为分散,因此,在通过金字塔结构保证硅基底反射率较低,光吸收较好的情况下,能够避免在绒面结构上形成厚度大于15nm的阻挡氧化层的过程中对绒面结构的破坏,此时,阻挡氧化层的厚度可以达到良好的掩膜作用,也同时避免了厚氧化层对太阳能电池性能的影响,显著提升太阳能电池的效率。

[0159] 图9示出了本发明实施例提供的第四种太阳能电池的制备方法的步骤流程图,如图9所示,该方法可以包括:

[0160] 步骤801、提供硅基底。

[0161] 步骤802、在所述硅基底的第一表面形成金字塔的绒面结构,所述绒面结构中所述金字塔的平均尺寸大于或等于2μm,且小于5μm。

[0162] 本发明实施例中,步骤801至步骤802可对应参照前述步骤中101至步骤102的相关描述,为避免重复,在此不再赘述。

[0163] 步骤803、对所述第一表面进行元素掺杂处理形成第一掺杂层,所述元素包括IIIA族元素、VA族元素中的至少一种。

[0164] 本发明实施例中,也可以先对第一表面进行元素掺杂处理形成第一掺杂层,再将硅基底置于氧化气氛下在第一表面的绒面结构上进行热氧化以形成第一掺杂层上的阻挡氧化层,此时,可以采用更多种元素掺杂处理的方式对第一表面进行元素掺杂,本领域技术人员可以根据具体需求进行选择。

[0165] 可选地,所述步骤803中所述元素掺杂处理为热扩散工艺、离子注入或原位掺杂其中的一种。

[0166] 本发明实施例中,元素掺杂处理可以是热扩散工艺、离子注入或原位掺杂中的任一种,其中,热扩散工艺可对应参照前述步骤403的相关描述,为避免重复,在此不再赘述;离子注入可以是在低温下,对IIIA族元素或VA族元素的离子进行加速,以使IIIA族元素或VA族元素的离子进入第一表面中从而形成第一掺杂层;原位掺杂可以指形成第一表面的同时通入含有杂质元素的气体进行掺杂,从而提高了第一掺杂层的生产效率。

[0167] 步骤804、在所述第一表面的绒面结构上,对所述第一掺杂层热氧化形成阻挡氧化层。

[0168] 本发明实施例中,可以在形成第一掺杂层后,对所述第一掺杂层进行热氧化,以在第一掺杂层上形成阻挡氧化层,可选地。步骤804可对应参照前述步骤203的相关描述,为避免重复,在此不再赘述。

[0169] 可选地,所述基底的第二表面与第一表面相对。

[0170] 步骤805、在所述基底的第二表面形成钝化接触结构。

[0171] 本发明实施例中,步骤805可对应参照前述步骤404的相关描述,为避免重复,在此不再赘述。

[0172] 本发明实施例中,在制备太阳能电池的过程中,控制硅基底第一表面的绒面结构中金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$,由于金字塔的平均尺寸较大,分布较为分散,因此,在通过金字塔结构保证硅基底反射率较低,光吸收较好的情况下,能够避免在绒面结构上形成厚度大于 15nm 的阻挡氧化层的过程中对绒面结构的破坏,此时,阻挡氧化层的厚度可以达到良好的掩膜作用,也同时避免了厚氧化层对太阳能电池性能的影响,显著提升太阳能电池的效率。

[0173] 图10是本发明实施例提供的第五种太阳能电池的制备方法的步骤流程图,如图10所示,该方法可以包括:

[0174] 步骤901、提供硅基底。

[0175] 步骤902、在所述硅基底的第一表面形成金字塔的绒面结构,所述绒面结构中所述金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$ 。

[0176] 本发明实施例中,步骤901至步骤902可对应参照前述步骤中101至步骤102的相关描述,为避免重复,在此不再赘述。

[0177] 步骤903、对所述第一表面进行元素掺杂处理形成第一掺杂层,所述元素包括IIIA族元素、VA族元素中的至少一种。

[0178] 本发明实施例中,步骤903可对应参照前述步骤803的相关描述,为避免重复,在此不做赘述。

[0179] 步骤904、在所述第一表面的绒面结构上,对所述第一掺杂层热氧化形成阻挡氧化层。

[0180] 本发明实施例中,可以在形成第一掺杂层后,对所述第一掺杂层进行热氧化,以在第一掺杂层上形成阻挡氧化层,可选地。步骤904可对应参照前述步骤203的相关描述,为避免重复,在此不再赘述。

[0181] 可选地,所述基底的第二表面与第一表面相对。

[0182] 步骤905、在所述基底的第二表面形成钝化层。

[0183] 本发明实施例中,步骤905可对应参照前述步骤604的相关描述,为避免重复,在此不再赘述。

[0184] 本发明实施例中,在制备太阳能电池的过程中,控制硅基底第一表面的绒面结构中金字塔的平均尺寸大于或等于 $2\mu\text{m}$,且小于 $5\mu\text{m}$,由于金字塔的平均尺寸较大,分布较为分散,因此,在通过金字塔结构保证硅基底反射率较低,光吸收较好的情况下,能够在绒面结构上形成厚度大于 15nm 的阻挡氧化层的过程中对绒面结构的破坏,此时,阻挡氧化层的厚度可以达到良好的掩膜作用,也同时避免了厚氧化层对太阳能电池性能的影响,显著提升太阳能电池的效率。

[0185] 本发明实施例还提供了一种太阳能电池,该太阳能电池由图1至图8所述的太阳能电池的制备方法制备得到。

[0186] 参数对比示例

[0187] 本发明实施例还提供了太阳能电池参数对比实验,以厚度为 $180\mu\text{m}$,电阻率为 $1\Omega\cdot\text{cm}$ 的N型硅片为硅基底,分别制备绒面结构中金字塔的平均尺寸为 $1.5\mu\text{m}$ 的1号实验组、 $2.5\mu\text{m}$ 的2号实验组、 $3\mu\text{m}$ 的3号实验组、 $4\mu\text{m}$ 的4号实验组、 $5\mu\text{m}$ 的5号实验组以及 $6\mu\text{m}$ 的6号实验组。其中,各实验组太阳能电池的硼扩散峰值温度为 980°C ,在硼扩散过程中采用干氧化法,在 980°C 下对硅基底的第一表面进行氧化获得阻挡氧化层并同时进行的硼扩散PN结推进;然后对硅基底的第二表面采用氢氟酸清洗,再采用硝酸、氢氟酸、硫酸的混合溶液刻蚀,去除第二表面的PN结;采用三氯氧磷对第二表面的非晶硅进行磷掺杂,将其晶化为多晶硅;采用链式碱刻蚀去除第一表面绕镀的多晶硅,再用氢氟酸去除第一表面的阻挡氧化层和第二表面磷扩散中形成的氧化层;经过盐酸等清洗、烘干;采用ALD (Atomic layer deposition, 原子层沉积) 氧化铝对第一表面进行钝化,以及PECVD对各实验组的太阳能电池进行双面氮化硅钝化获得钝化层;使用银浆分别在第一表面和第二表面的钝化层上形成电极,获得各实验组的太阳能电池。

[0188] 本发明实施例对各实验组的太阳能电池进行电池性能测试,以1号实验组的测试参数作为对比,得到各组的测试参数如下表所示:

[0189] 实验组电池性能参数对照表

实验组编号	Uoc/mV	Isc/mA	FF/%	Eta/%	备注
1	0	0	0	0	
2	+1	+40	+0.20	+0.18	与 1 号实验组的相对值
3	+2	+27	+0.05	+0.14	与 1 号实验组的相对值
4	+2	+23	+0.01	+0.12	与 1 号实验组的相对值
5	+2	+10	-0.22	+0.02	与 1 号实
					验组的相
					对值
6	+3	-10	-0.56	-0.08	与 1 号实
					验组的相
					对值

[0192] 由上表内容可知,在绒面结构的金字塔的平均尺寸在 $2\mu\text{m}$ 到 $4\mu\text{m}$ 之间时,电池各参数相比于金字塔的平均尺寸为 $1.5\mu\text{m}$ 均有较为明显的提升,在金字塔的平均尺寸为 $5\mu\text{m}$ 时相比于 $1.5\mu\text{m}$ 各参数提升效果不明显,甚至FF (Fill Factor,填充因子)有所下降,在金字塔的平均尺寸为 $6\mu\text{m}$ 时相比于 $1.5\mu\text{m}$ 各参数提升效果进一步降低,FF和ISC (短路电流,Short Circuit Current)降低幅度明显。因此,本发明实施例的方案可以显著提升太阳能电池的效率。

[0193] 需要说明的是,对于方法实施例,为了简单描述,故将其都表述为一系列的动作组合,但是本领域技术人员应该知悉,本申请实施例并不受所描述的动作顺序的限制,因为依据本申请实施例,某些步骤可以采用其他顺序或者同时进行。其次,本领域技术人员也应该知悉,说明书中所描述的实施例均属于优选实施例,所涉及的动作并不一定都是本申请实施例所必须的。

[0194] 需要说明的是,在本文中,术语“包括”、“包含”或者其任何其他变体意在涵盖非排他性的包含,从而使得包括一系列要素的过程、方法、物品或者装置不仅包括那些要素,而且还包括没有明确列出的其他要素,或者是还包括为这种过程、方法、物品或者装置所固有的要素。在没有更多限制的情况下,由语句“包括一个……”限定的要素,并不排除在包括该要素的过程、方法、物品或者装置中还存在另外的相同要素。

[0195] 上面结合附图对本发明的实施例进行了描述,但是本发明并不局限于上述的具体

实施方式,上述的具体实施方式仅仅是示意性的,而不是限制性的,本领域的普通技术人员在本发明的启示下,在不脱离本发明宗旨和权利要求所保护的范围情况下,还可做出很多形式,这些均属于本发明的保护之内。

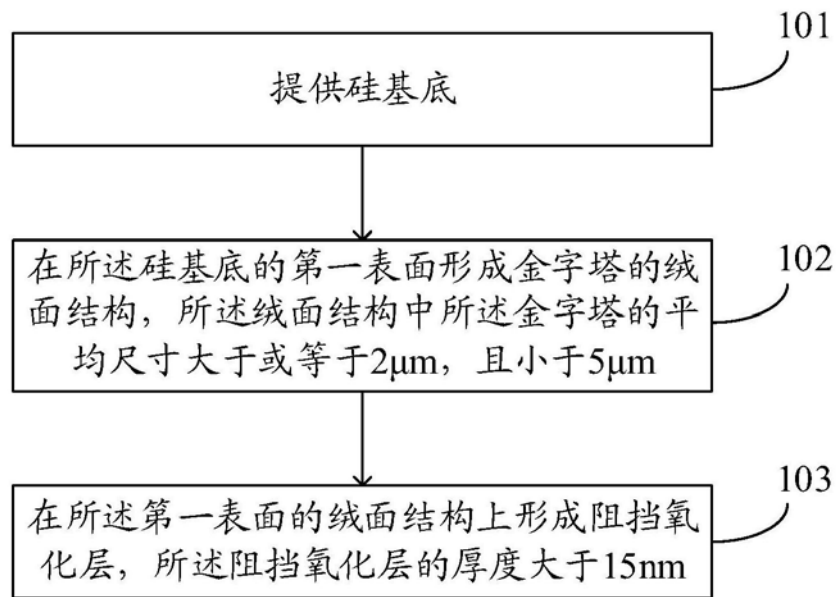


图1

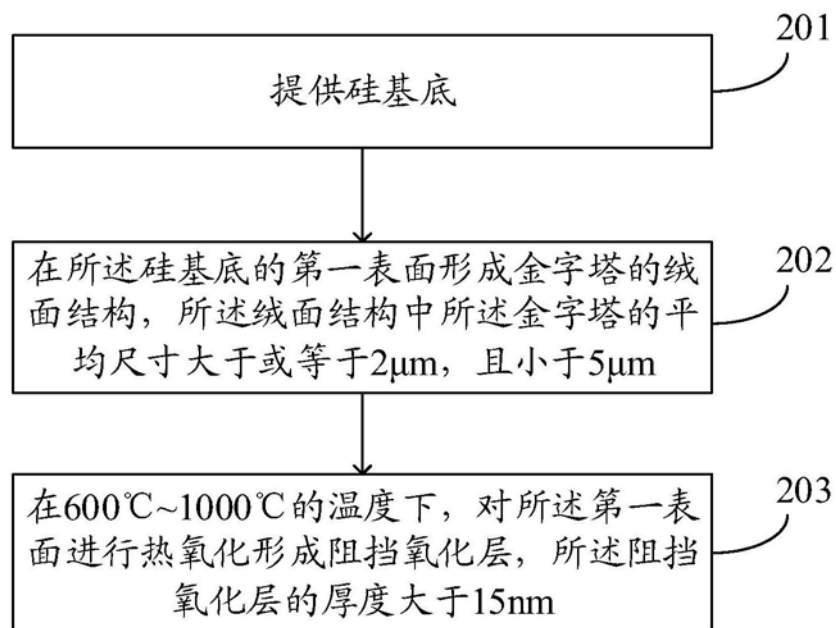


图2

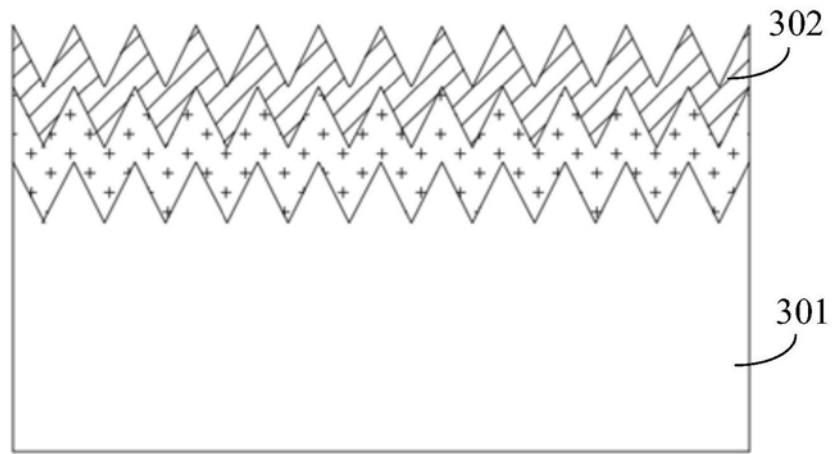


图3

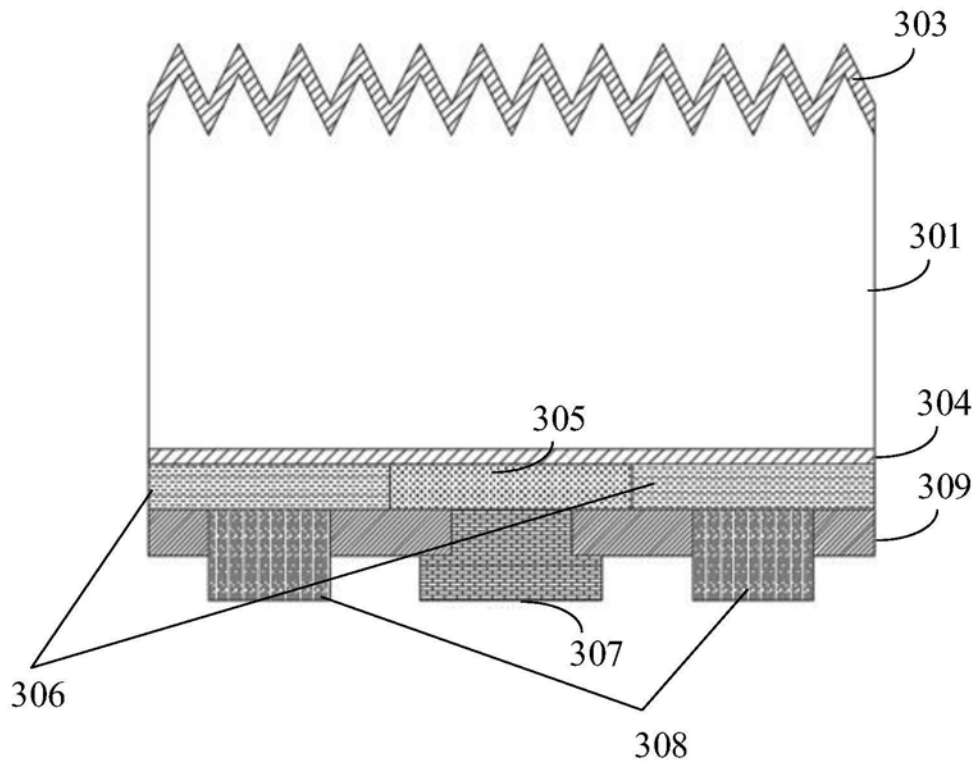


图4

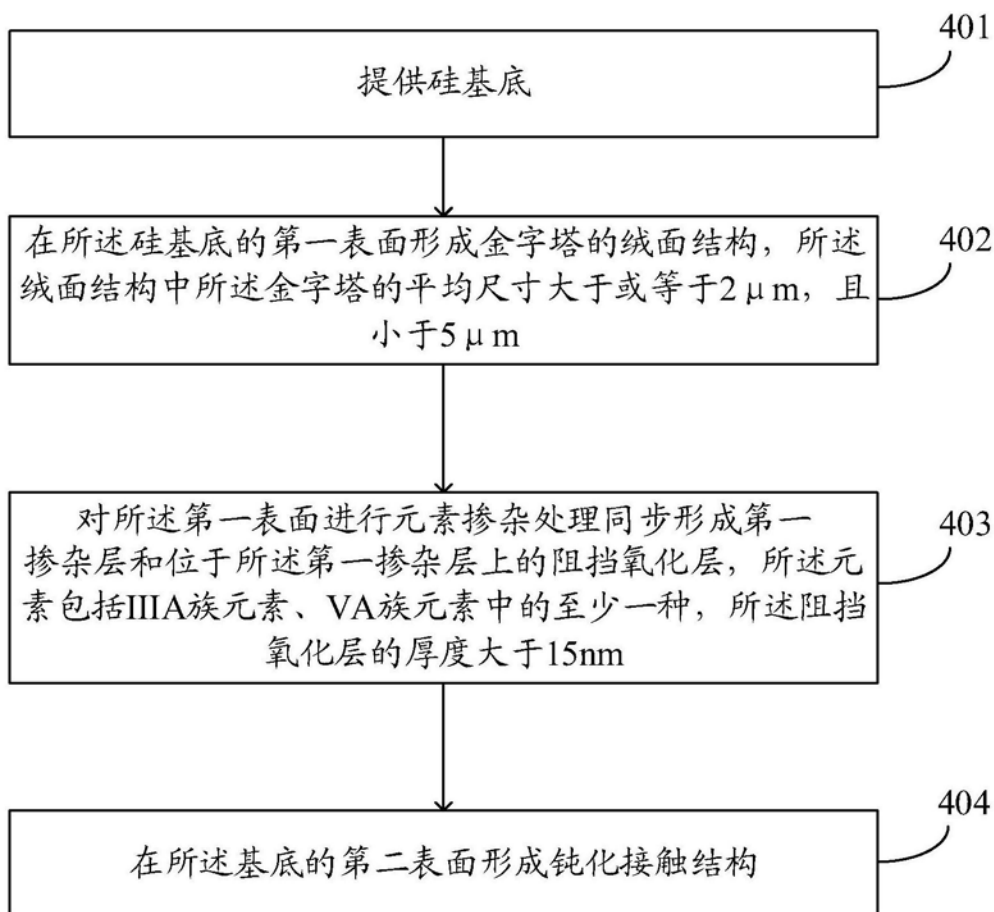


图5

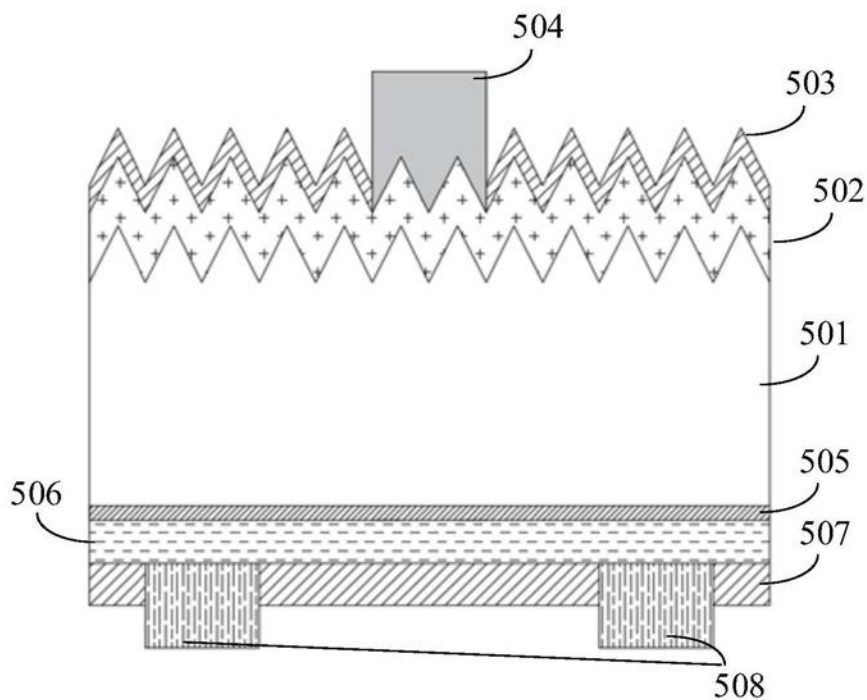


图6

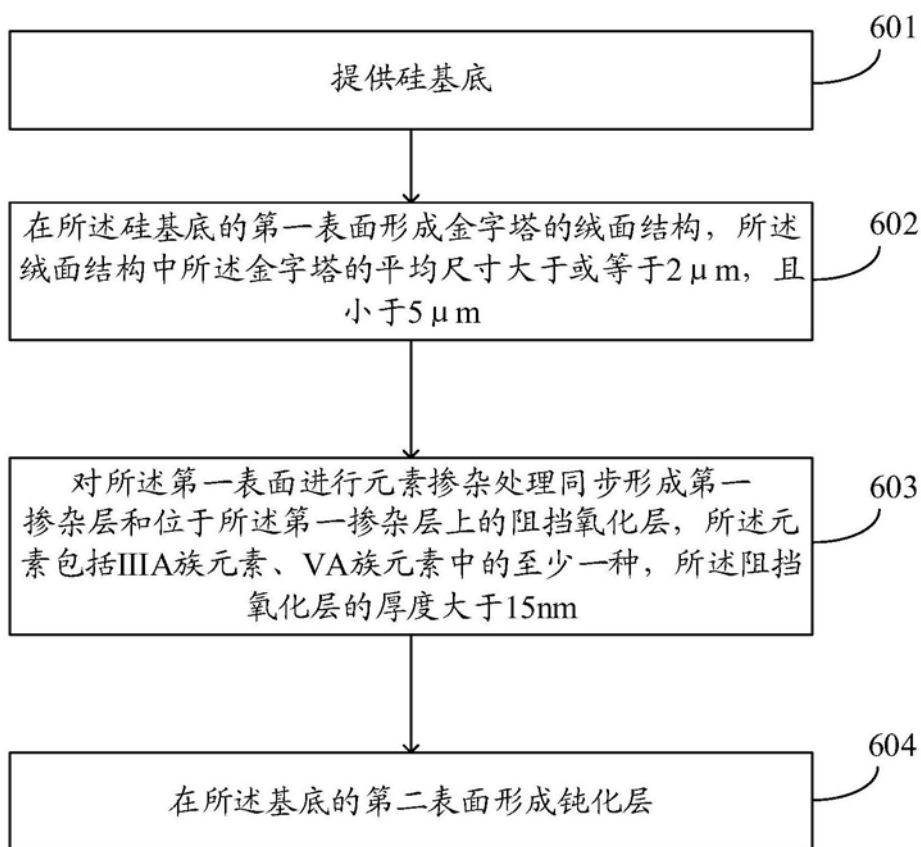


图7

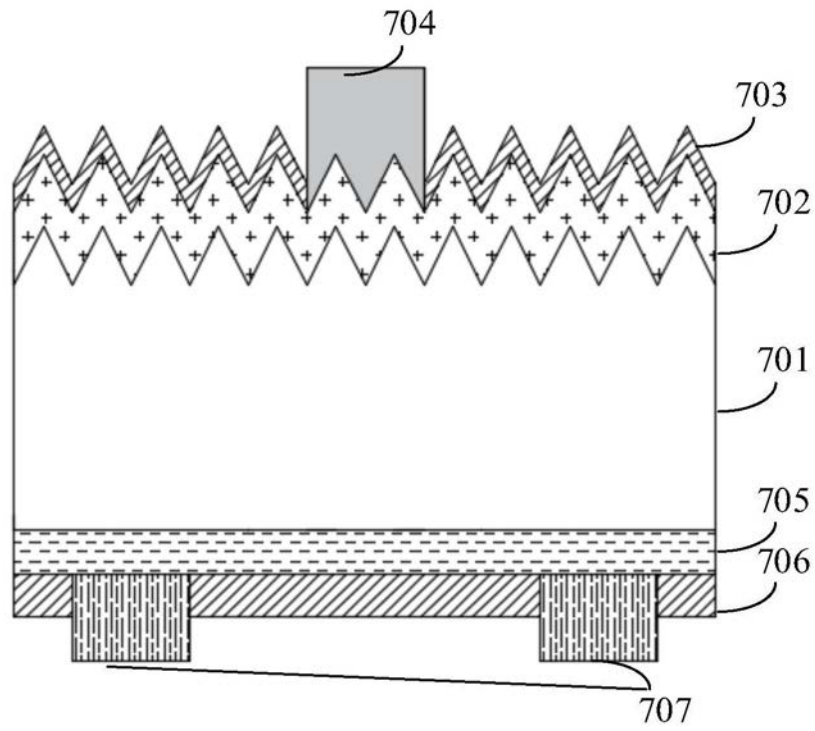


图8

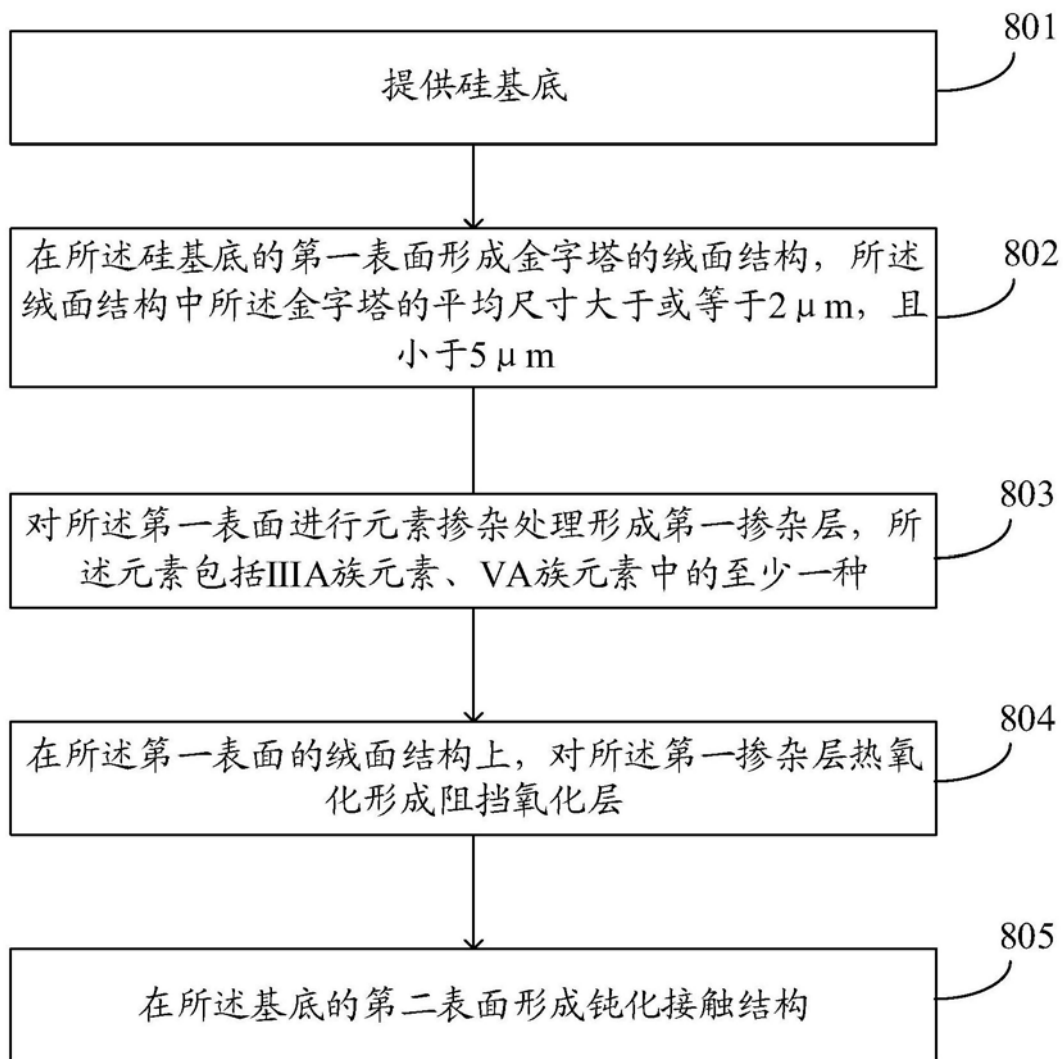


图9

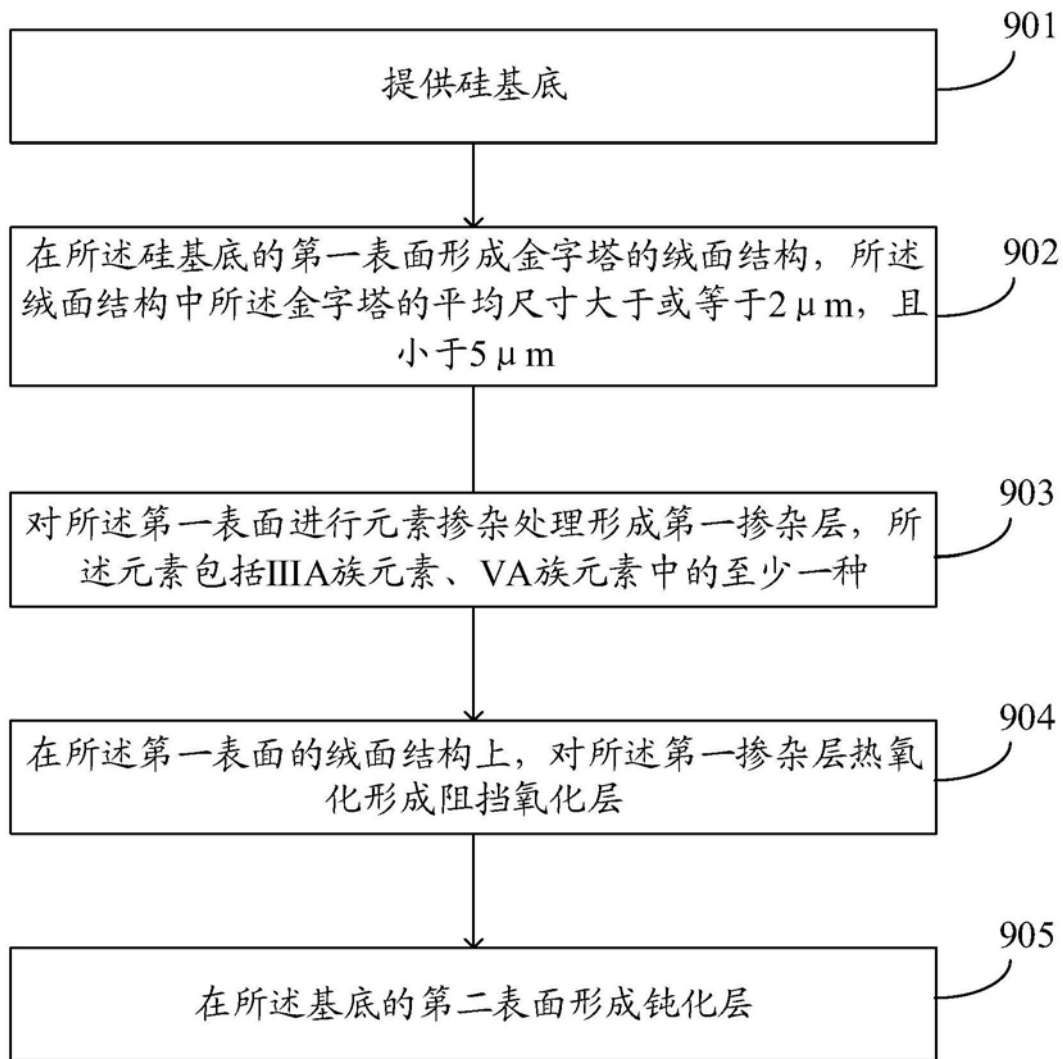


图10



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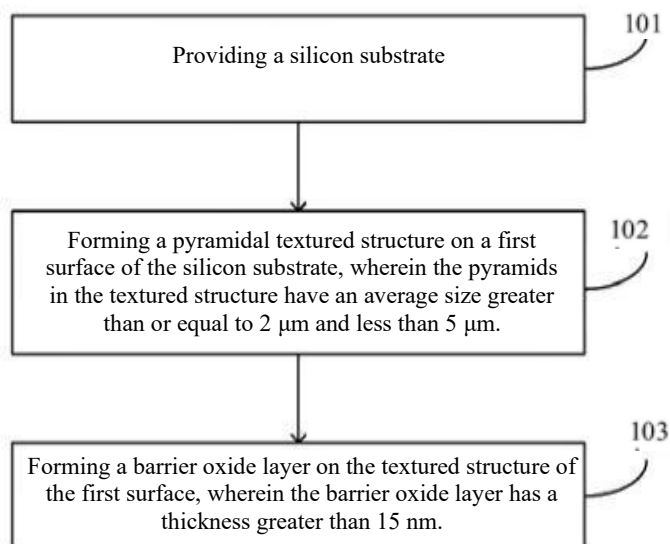
Claims (2 pages), Description (15 pages), Drawings (7 pages)

(54) Title of Invention

A method for preparing a solar cell and a type of solar cell

(57) Abstract

This invention provides a method for preparing a solar cell, relating to the field of solar photovoltaic technology. In the process of preparing the solar cell, the average size of the pyramids in the textured structure of the first surface of the silicon substrate is controlled to be greater than or equal to 2 μm and less than 5 μm . Because the average size of the pyramids is relatively large and their distribution is relatively dispersed, while ensuring low reflectivity and good light absorption of the silicon substrate through the pyramid structure, damage to the textured structure can be avoided during the formation of a barrier oxide layer with a thickness greater than 15 nm. At this point, the thickness of the barrier oxide layer can achieve a good masking effect, while also avoiding the impact of a thick oxide layer on the performance of the solar cell, significantly improving the efficiency of the solar cell.



CN 112635591 A

1. A method for preparing a solar cell, characterized in that the method comprises:

Provide silicon substrate;

A pyramidal textured structure is formed on the first surface of the silicon substrate, wherein the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 5 μm ;

A barrier oxide layer is formed on the textured surface of the first surface, the thickness of the barrier oxide layer being greater than 15 nm.

2. The method for preparing a solar cell according to claim 1, wherein the thickness of the barrier oxide layer is greater than 30 nm.

3. The method for preparing a solar cell according to claim 1, wherein the average size of the pyramids in the textured structure is less than 4 μm .

4. The method for preparing a solar cell according to claim 1, characterized in that forming a barrier oxide layer on the textured surface of the first surface comprises:

The first surface is thermally oxidized at a temperature of 600°C~1000°C to form a barrier oxide layer.

5. The method for preparing a solar cell according to claim 1, characterized in that forming a barrier oxide layer on the textured surface of the first surface comprises:

The first surface is subjected to elemental doping treatment to simultaneously form a first doped layer and a barrier oxide layer located on the first doped layer, wherein the elements include at least one of group IIIA elements and group VA elements.

6. The method for preparing a solar cell according to claim 5, wherein the element doping treatment is a thermal diffusion process.

7. The method for preparing a solar cell according to claim 1, characterized in that, after the step of forming a pyramidal textured structure on the first surface of the silicon substrate, it further includes:

The first surface is subjected to elemental doping treatment to form a first doped layer, wherein the element includes at least one of group IIIA elements and group VA elements;

The process of forming a barrier oxide layer on the textured surface of the first surface includes:

On the textured surface of the first surface, a barrier oxide layer is formed by thermal oxidation of the first doped layer.

8. The method for preparing a solar cell according to claim 7, wherein the element doping treatment is one of thermal diffusion process, ion implantation or in-situ doping.

9. A method for manufacturing a solar cell according to any one of claims 1 to 8, characterized in that the second surface of the substrate faces the first surface, and after the step of forming a barrier oxide layer on the textured surface of the first surface, the method further includes:

A passivated contact structure is formed on the second surface of the substrate, and/or,

A passivation layer is formed on the second surface of the substrate.

10. The method for manufacturing a solar cell according to claim 9, characterized in that forming a passivated contact structure on the second surface of the substrate comprises:

Etch the second surface of the substrate;

A first doped semiconductor layer is formed on the second surface of the substrate, and a first doped semiconductor layer is also formed on the barrier oxide layer on at least a portion of the first surface;

With the first surface barrier oxide layer protecting the first surface of the silicon substrate, the first doped semiconductor layer on the first surface is removed using a wet processing procedure;

A tunneling passivation layer is provided between the second surface of the substrate and the first doped semiconductor layer, the tunneling passivation layer comprising silicon oxide.

11. A solar cell, characterized in that the solar cell is manufactured using the method for manufacturing a solar cell according to any one of claims 1 to 10.

A method for preparing solar cell and a type of solar cell

Technical Field

[0001] This invention relates to the field of solar photovoltaic technology, and in particular to a method for preparing a solar cell and the solar cell itself.

Background Art

[0002] In the preparation process of silicon-based solar cells, in order to reduce the surface reflectivity of the silicon wafer and increase the absorption of light to improve the efficiency of the solar cell, a pyramidal textured surface is usually prepared on the surface of the silicon wafer using a chemical etching method. The pyramidal textured surface can perform secondary reflection and refraction of light, thereby increasing the absorption of light. In order to reduce the reflectivity of the textured surface, the size of the pyramids in the textured surface can be reduced, thereby enhancing the secondary reflection and refraction of light.

[0003] In the preparation process of solar cell, in order to avoid the pyramid structure of the textured surface being damaged in subsequent processes, it is usually necessary to set an oxide layer on the textured surface to isolate the textured surface from the environment that may damage it. However, the preparation of the oxide layer may also lead to a decrease in the cell conversion efficiency.

Summary of the Invention

[0004] The present invention provides a method for preparing a solar cell and a solar cell, which aims to avoid the problem that the preparation of a protective oxide layer during the preparation of a solar cell leads to low conversion efficiency of the solar cell.

[0005] In a first aspect, embodiments of the present invention provide a method for preparing a solar cell, the method comprising:

[0006] A silicon substrate is provided;

[0007] A pyramidal textured structure is formed on the first surface of the silicon substrate, wherein the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 5 μm ;

[0008] A barrier oxide layer is formed on the textured surface of the first surface, the thickness of the barrier oxide layer being greater than 15 nm.

[0009] Optionally, the thickness of the barrier oxide layer is greater than 30 nm.

[0010] Optionally, the average size of the pyramid in the textured structure is less than 4 μm .

[0011] Optionally, forming a barrier oxide layer on the textured surface of the first surface includes:

[0012] The first surface is thermally oxidized at a temperature of 600°C~1000°C to form a barrier oxide layer.

[0013] Optionally, forming a barrier oxide layer on the textured surface of the first surface includes:

[0014] The first surface is subjected to element doping treatment to simultaneously form a first doped layer and a barrier oxide layer located on the first doped layer, wherein the elements include at least one of group IIIA elements and group VA elements.

[0015] Optionally, the element doping treatment is a thermal diffusion process.

[0016] Optionally, after the step of forming the pyramidal textured structure on the first surface of the silicon substrate, the method further includes:

[0017] The first surface is subjected to elemental doping treatment to form a first doped layer, wherein the element includes at least one of group IIIA elements and group VA elements;

[0018] Optionally, forming a barrier oxide layer on the textured surface of the first surface includes:

[0019] On the textured surface of the first surface, the first doped layer is thermally oxidized to form a barrier oxide layer.

- [0020] Optionally, the element doping treatment is one of thermal diffusion process, ion implantation or in-situ doping.
- [0021] Optionally, the second surface of the substrate is opposite to the first surface, and after the step of forming a barrier oxide layer on the textured surface of the first surface, the method further includes:
- [0022] A passivated contact structure is formed on the second surface of the substrate, and/or ,
- [0023] A passivation layer is formed on the second surface of the substrate.
- [0024] Optionally, forming a passivated contact structure on the second surface of the substrate includes:
- [0025] The second surface of the substrate is etched;
- [0026] A first doped semiconductor layer is formed on the second surface of the substrate, and a first doped semiconductor layer is also formed on the barrier oxide layer on at least a portion of the first surface;
- [0027] With the first surface barrier oxide layer protecting the first surface of the silicon substrate, the first doped semiconductor layer on the first surface is removed using a wet processing procedure;
- [0028] A tunneling passivation layer is provided between the second surface of the substrate and the first doped semiconductor layer, the tunneling passivation layer comprising: silicon oxide.
- [0029] In a second aspect, embodiments of the present invention provide a solar cell, which is prepared by the method for preparing a solar cell in the first aspect.
- [0030] In this embodiment of the invention, during the preparation of the solar cell, the average size of the pyramids in the textured structure of the first surface of the silicon substrate is controlled to be greater than or equal to 2 μm and less than 5 μm . Since the average size of the pyramids is relatively large and the distribution is relatively dispersed, the damage to the textured structure can be avoided during the formation of a barrier oxide layer with a thickness greater than 15 nm on the textured structure while ensuring that the silicon substrate has low reflectivity and good light absorption through the pyramid structure. At this time, the thickness of the barrier oxide layer can achieve a good masking effect and at the same time avoid the influence of the thick oxide layer on the performance of the solar cell, significantly improving the efficiency of the solar cell.

Brief Description of the Drawings

- [0031] In order to more clearly illustrate the technical solutions of the embodiments of the present invention, the drawings used in the description of the embodiments of the present invention will be briefly introduced below. Obviously, the drawings described below are only some embodiments of the present invention. For those skilled in the art, other drawings can be obtained based on these drawings without creative effort.
- [0032] Figure 1 shows a flowchart of the steps of a method for preparing a first type of solar cell provided in an embodiment of the present invention;
- [0033] Figure 2 shows a flowchart of the steps of the second solar cell preparation method provided in the embodiment of the present invention;
- [0034] Figure 3 shows a schematic diagram of a battery substrate structure provided in an embodiment of the present invention;
- [0035] Figure 4 shows a schematic diagram of a solar cell provided in an embodiment of the present invention;
- [0036] Figure 5 shows a flowchart of the steps of the third method for preparing a solar cell provided in the embodiment of the present invention;
- [0037] Figure 6 shows a schematic diagram of another solar cell provided in an embodiment of the present invention;
- [0038] Figure 7 shows a flowchart of the steps of the fourth solar cell preparation method provided in the embodiment of the present invention.
- [0039] Figure 8 shows a schematic diagram of another solar cell provided in an embodiment of the present invention;
- [0040] Figure 9 shows a flowchart of the steps of the fifth solar cell preparation method provided in the embodiment of the present invention;
- [0041] Figure 10 shows a flowchart of the steps of the sixth solar cell preparation method provided in the embodiment of the present invention.
- [0042] Explanation of reference numerals in the drawings:
- [0043] Figure 4: 301 - Silicon substrate; 302 - Barrier oxide layer;

[0044] Figure 5: 301-Silicon substrate; 303-First passivation layer; 304-Passivation tunneling layer; 305-First doped semiconductor layer; 306-Second doped semiconductor layer; 307-First electrode; 308-Second electrode; 309-Second passivation layer;

[0045] Figure 6: 501-Silicon substrate; 502-First doped layer; 503-First passivation layer; 504-First electrode; 505-Tunneling passivation layer; 506-First doped semiconductor layer; 507-Second passivation layer; 508-Second electrode;

[0046] Figure 7: 701-Silicon substrate; 702-First doped layer; 703-First passivation layer; 704-First electrode; 705-Back doped layer; 706-Second passivation layer; 707-Second electrode.

Detailed Description of the Embodiments

[0047] The technical solutions of the embodiments of the present invention will be clearly and completely described below with reference to the accompanying drawings. Obviously, the described embodiments are only some embodiments of the present invention, and not all embodiments. Based on the embodiments of the present invention, all other embodiments obtained by those skilled in the art without creative effort are within the scope of protection of the present invention.

[0048] Figure 1 shows a flowchart of the steps of a first method for preparing a solar cell according to an embodiment of the present invention. As shown in Figure 1, the method may include:

[0049] Step 101: Provide a silicon substrate.

[0050] In this embodiment of the invention, the silicon substrate can be an N-type silicon substrate or a P-type silicon substrate, and this embodiment of the invention does not impose any specific restrictions on it.

[0051] Step 102: Form a pyramidal textured structure on the first surface of the silicon substrate, wherein the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 5 μm .

[0052] In this embodiment of the invention, before forming the pyramidal textured structure on the first surface of the silicon substrate, the first surface of the silicon substrate can be cleaned to remove impurities adsorbed on the surface of the silicon substrate during processes such as slicing, grinding, chamfering, and polishing.

[0053] In this embodiment of the invention, the first surface of the silicon substrate can be subjected to "surface texturing" treatment. For example, an alkaline solution can be used to anisotropically etch the first surface of the silicon substrate to form a pyramidal textured surface. The pyramidal textured surface can reflect light multiple times, reducing the surface reflectivity of the silicon substrate and effectively improving the utilization rate of incident sunlight, thereby increasing the photocurrent density and improving the conversion efficiency of the solar cell.

[0054] In this embodiment of the invention, the distance between the base sides of the pyramids in the textured structure is used as the size of the pyramids. During the texturing process on the first surface of the silicon substrate, the average size of the pyramids in the textured structure can be controlled to be greater than or equal to 2 μm and less than 5 μm . Optionally, the average size of the pyramids in the textured structure can be adjusted by adjusting the reaction time and solution ratio during the texturing process. This avoids the problem of densely distributed pyramids when the average size is small, which could be destroyed during the subsequent formation of the barrier oxide layer, thereby significantly improving the conversion efficiency of the finished battery. It also avoids the problem of excessively large average pyramid size, which would result in poor reflectivity reduction and low battery conversion efficiency. Optionally, the average size of the pyramids in the textured structure can be any size greater than or equal to 2 μm and less than 5 μm , such as 2 μm , 3 μm , 4 μm , 4.5 μm . This embodiment of the invention does not impose specific limitations on this.

[0055] Step 103: Form a barrier oxide layer on the textured surface of the first surface, wherein the thickness of the barrier oxide layer is greater than 15 nm.

[0056] In existing solar cell preparation processes, after forming a pyramidal textured surface on the silicon substrate, a relatively thick oxide layer is usually required as a barrier or protective layer to prevent damage to the textured surface in subsequent processes. However, in actual preparation, it has been found that a relatively high oxide layer thickness is required to ensure the protective effect of the barrier layer. However, the oxide layer grows rapidly at the apex of the pyramid on the textured surface, which means that a high oxide layer thickness can actually damage the pyramidal structure of the textured surface. For example, a textured surface with an average pyramid size of less than 2 μm will severely degrade the battery performance and is not conducive to improving the battery conversion efficiency. On the other hand, a low oxide layer thickness results in poor protection and may cause the textured surface of the pyramid to be damaged in subsequent processes, affecting the battery conversion efficiency.

[0057] In this embodiment of the invention, when the first surface of the silicon substrate has a textured structure with an average pyramidal size greater than or equal to 2 μm and less than 5 μm , the damage to the textured structure by the barrier oxide layer can be effectively avoided. Therefore, a thicker barrier oxide layer can be formed on the textured structure of the first surface. The barrier oxide layer refers to the oxide layer used in the solar cell process to protect the surface textured structure of the silicon substrate. Generally speaking, the thicker the barrier oxide layer, the better the protection effect on the textured structure, thereby ensuring the battery performance. In the process of a thicker barrier oxide layer, the present invention can significantly improve the conversion efficiency of the battery. Optionally, the thickness of the barrier oxide layer can be greater than 15nm, such as 15.5nm, 16nm, 20nm, 30nm, 50nm, 100nm, 120nm, etc., with a thickness of more than 15nm.

[0058] In this embodiment of the invention, other surfaces on the silicon substrate besides the first surface can be processed according to the specific application requirements of the battery, or other functional layers can be further formed on the first surface or other surfaces of the silicon substrate. Optionally, the second surface opposite to the first surface on the silicon substrate can be polished or etched. This embodiment of the invention does not impose specific limitations on this.

[0059] In this embodiment of the invention, during the preparation of the solar cell, the average size of the pyramids in the textured structure of the first surface of the silicon substrate is controlled to be greater than or equal to 2 μm and less than 5 μm . Since the average size of the pyramids is relatively large and the distribution is relatively dispersed, the damage to the textured structure can be avoided during the formation of a barrier oxide layer with a thickness greater than 15 nm on the textured structure while ensuring that the silicon substrate has low reflectivity and good light absorption through the pyramid structure. At this time, the thickness of the barrier oxide layer can achieve a good masking effect, and at the same time avoid the influence of the thick oxide layer on the performance of the solar cell, significantly improving the efficiency of the solar cell.

[0060] Figure 2 shows a flowchart of the steps of a second method for preparing a solar cell provided in an embodiment of the present invention. As shown in Figure 2, the method includes:

[0061] Step 201: Provide a silicon substrate. Step 202: Form a pyramidal textured structure on a first surface of the silicon substrate, wherein the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 5 μm .

[0062] In this embodiment of the invention, steps 201 to 202 can be referred to the relevant descriptions of steps 101 to 102 above. To avoid repetition, they will not be repeated here. Optionally, after forming a pyramidal textured structure on the first surface of the silicon substrate, the reflectivity of the first surface of the silicon substrate can be adjusted to be less than 12%.

[0063] Optionally, the average size of the pyramid in the textured structure is less than 4 μm .

[0064] In this embodiment of the invention, the average size of the pyramids in the textured structure can be further adjusted to be less than 4 μm , so that the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 4 μm , thereby ensuring the high or low light reflectivity of the textured structure while avoiding the influence of the thick barrier oxide layer on the textured structure.

[0065] Step 203: At a temperature of 600°C~1000°C, the first surface is thermally oxidized to form a barrier oxide layer.

[0066] In this embodiment of the invention, step 203 can be referred to the relevant description of step 103 above. To avoid repetition, it will not be repeated here.

[0067] In this embodiment of the invention, a barrier oxide layer can be prepared on the first surface of a silicon substrate by thermal oxidation. Optionally, the thermal oxidation method can be dry oxygen thermal oxidation or wet oxygen thermal oxidation. Dry oxygen thermal oxidation is achieved using oxygen, while wet oxygen thermal oxidation is achieved using oxygen and water. Optionally, during the thermal oxidation process, the temperature can be controlled at 600°C~1000°C, such as any temperature between 600°C and 1000°C, such as 600°C, 650°C, 700°C, 800°C, 900°C, 1000°C, etc.

[0068] Optionally, the thickness of the barrier oxide layer is greater than 30 nm.

[0069] In this embodiment of the invention, since the thicker the oxide layer in the prior art, the more damage is done to the pyramid structure of the textured surface, and the greater the impact on the anti-reflection effect of the textured surface, the thicker the barrier oxide layer in this embodiment of the invention, the better the preservation effect of the pyramid structure of the textured surface is compared with the prior art, and the battery conversion efficiency is effectively improved. At this time, based on 15nm, the thickness of the barrier oxide layer can be adjusted to be greater than 30nm or greater than 70nm. This embodiment of the invention does not make specific limitations on this.

[0070] In this embodiment of the invention, in order to avoid the formation of corresponding oxide layers on other surfaces of the silicon substrate during the formation of a barrier oxide layer on the first surface of the silicon substrate, the other surfaces can be protected before thermal oxidation to prevent the formation of corresponding oxide layers. Alternatively, the oxide layers on other surfaces can be removed after the barrier oxide layer is formed to avoid affecting subsequent processes.

[0071] Figure 3 shows a schematic diagram of a battery substrate structure provided in an embodiment of the present invention. As shown in Figure 3, the battery substrate 30 includes a silicon substrate 301 and a barrier oxide layer 302. Other functional layers, such as doped layers, may also be included between the silicon substrate 301 and the barrier oxide layer 302. The present invention does not impose specific limitations on this.

[0072] As shown in Figure 3, the thickness of the barrier oxide layer 302 in the battery substrate structure is 100 nm. It is formed on the textured structure of the first surface of the silicon substrate 301 by dry oxidation or wet oxidation at 900 °C. Optionally, in order to meet different application requirements, the second surface of the battery substrate structure shown in Figure 3 can also be polished. For example, the silicon substrate 301 can be placed in an alkaline solution containing potassium hydroxide or sodium hydroxide and polished at a temperature greater than or equal to 60 °C to make the second surface a polished surface, thus obtaining the battery substrate structure. At this time, the barrier oxide layer 302 can protect the textured structure on the first surface. Then, the barrier oxide layer 302 is removed, and other required functional layers are formed on the first and second surfaces respectively to obtain different solar cells.

[0073] Figure 4 shows a schematic diagram of the structure of a solar cell provided in an embodiment of the present invention. Based on the battery substrate structure, an IBC (Interdigitated back contact) battery can be fabricated as shown in Figure 4. Based on Figure 3, the IBC battery includes a silicon substrate 301, a first passivation layer 303, a passivation tunneling layer 304, a first doped semiconductor layer 305, a second doped semiconductor layer 306, a first electrode 307, a second electrode 308, and a second passivation layer 309.

[0074] In this embodiment of the invention, during the preparation of the solar cell, the average size of the pyramids in the textured structure of the first surface of the silicon substrate is controlled to be greater than or equal to 2 μm and less than 5 μm. Since the average size of the pyramids is relatively large and the distribution is relatively dispersed, the damage to the textured structure can be avoided during the formation of a barrier oxide layer with a thickness greater than 15 nm on the textured structure while ensuring that the silicon substrate has low reflectivity and good light absorption through the pyramid structure. At this time, the thickness of the barrier oxide layer can achieve a good masking effect and at the same time avoid the influence of the thick oxide layer on the performance of the solar cell, significantly improving the efficiency of the solar cell.

[0075] Figure 5 shows a flowchart of the steps of the third method for preparing a solar cell provided in the embodiment of the present invention. As shown in Figure 5, the method includes:

[0076] Step 401: Provide a silicon substrate.

[0077] Step 402: Form a pyramidal textured structure on the first surface of the silicon substrate, wherein the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 5 μm.

[0078] In this embodiment of the invention, steps 401 to 402 can be referred to the relevant descriptions of steps 101 to 102 in the foregoing steps. To avoid repetition, they will not be repeated here.

[0079] Step 403: Perform element doping treatment on the first surface to simultaneously form a first doped layer and a barrier oxide layer located on the first doped layer. The elements include at least one of group IIIA elements and group VA elements, and the thickness of the barrier oxide layer is greater than 15 nm.

[0080] In this embodiment of the invention, a barrier oxide layer may be formed simultaneously on the first doped layer while the first surface is subjected to element doping treatment. Optionally, the doped element may be at least one of group IIIA elements and group VA elements, that is, at least one of group boron elements and group nitrogen elements. This embodiment of the invention does not impose specific limitations on this.

[0081] Optionally, the element doping process in step 403 is a thermal diffusion process.

[0082] In this embodiment of the invention, the entire surface can be used to form the doping source, and the first surface can be doped with elements by means of element driving in the thermal diffusion process through a heating device. At this time, the silicon substrate can be placed in an oxidizing atmosphere, so that while the elements are being doped, a barrier oxide layer is formed on the first doped layer based on the thermal diffusion process conditions.

[0083] Optionally, the group IIIA element may be boron, and step 403 specifically includes: performing tubular thermal diffusion on the first surface at a temperature of 850°C~1100°C to simultaneously form a boron-doped first doped layer and a barrier oxide layer located on the first doped layer.

[0084] In this embodiment of the invention, boron, a group IIIA element, can be selected to dope the first surface of the silicon substrate. At this time, the element doping can be carried out at a temperature of 850°C to 1100°C. Optionally, the temperature can be any temperature in the range of 850°C to 1100°C, such as 850°C, 900°C, 1000°C, 1100°C, etc. This embodiment of the invention does not impose any specific restrictions on this.

[0085] Optionally, the VA group element is phosphorus, and step 403 specifically includes using phosphorus oxychloride to perform tubular thermal diffusion on the first surface at a temperature of 700°C~900°C to simultaneously form a first doped layer doped with phosphorus and a barrier oxide layer located on the first doped layer.

[0086] In this embodiment of the invention, phosphorus can be selected as a group VA element to dope the first surface of the silicon substrate. At this time, the element doping can be carried out at a temperature of 700°C~900°C. Optionally, the temperature can be any temperature in the range of 700°C~900°C, such as 700°C, 750°C, 800°C, 900°C, etc. This embodiment of the invention does not impose any specific restrictions on this.

[0087] Optionally, the second surface of the substrate is opposite to the first surface.

[0088] Step 404: Form a passivated contact structure on the second surface of the substrate.

[0089] In this embodiment of the invention, depending on the type of solar cell being prepared, the application field, etc., different structures can be formed on the second surface of the substrate opposite to the first surface. For example, a passivation contact structure can be formed on the second surface of the substrate. The passivation contact structure is a preparation process that can achieve passivation of both the back and front sides and does not require opening contact, thus avoiding the contact range being limited to the opening area and expanding the contact range. It also simplifies the preparation process by eliminating the need for opening.

[0090] Optionally, step 404 includes:

[0091] Step S11: Etch the second surface of the substrate.

[0092] In this embodiment of the invention, the etching of the silicon substrate can be performed by acid etching using a chain acid solution or by alkaline etching using an alkaline solution. For example, in the case of acid etching, a mixed solution of hydrofluoric acid and nitric acid can be used to remove part of the silicon substrate on the second surface for etching. Optionally, the mixed solution may also include sulfuric acid solution, etc., so as to provide acidic ions while ensuring solution density and solution surface tension. In the case of alkaline etching, potassium hydroxide, sodium hydroxide, trimethylammonium oxide, etc. can be used to etch the second surface while avoiding damage to the barrier oxide layer, the first doped layer, etc. on the first surface.

[0093] In this embodiment of the invention, before etching the second surface, the oxide layer or the first doped layer around the diffusion can be removed from the second surface, thereby avoiding leakage problems caused by P and N co-doping after the battery is fabricated, and improving the yield and reliability of the product.

[0094] In this embodiment of the invention, the second surface can be cleaned before etching, such as by using hydrofluoric acid to clean the second surface. After cleaning the impurities, a second surface with a hydrophobic state is obtained, which is not easy to get dirty and is easy to dry quickly. Optionally, the cleaning can also include water washing, hydrochloric acid washing, ozone water washing, etc. This embodiment of the invention does not make specific limitations on this.

[0095] Step S12: A first doped semiconductor layer is formed on the second surface of the substrate, and a first doped semiconductor layer is formed on the barrier oxide layer on at least a portion of the first surface.

[0096] In this embodiment of the invention, after etching the second surface, a first doped semiconductor layer can be formed on the second surface. The first doped semiconductor layer can be obtained by first depositing a semiconductor layer and then doping the semiconductor layer with elements, or it can be obtained by in-situ doping during the deposition of the semiconductor layer. The first doped semiconductor layer has a different conductivity type than the first doped layer. In this case, phosphorus oxychloride can be used to obtain the first doped semiconductor layer by phosphorus ion implantation annealing, APCVD (Atmospheric Pressure Chemical Vapor Deposition) phosphorus silicon glass heating and propulsion, etc. For details, please refer to the relevant description of the first surface element doping treatment mentioned above. To avoid repetition, it will not be repeated here.

[0097] In this embodiment of the invention, the barrier oxide layer on the first surface will protect the emitter formed by element doping on the first surface during the doping process of the second surface, preventing the co-doping of different impurity elements and short circuits, thereby improving the yield of the battery.

[0098] Optionally, the material of the semiconductor layer includes at least one of silicon thin film and silicon carbide thin film;

[0099] Optionally, the crystal morphology of the semiconductor layer material includes at least one of polycrystalline morphology, amorphous morphology, microcrystalline morphology, and nanocrystalline morphology.

[0100] In this embodiment of the invention, the material of the semiconductor layer can be at least one of silicon thin film and silicon carbide thin film. For example, the semiconductor layer can be a silicon thin film layer, a silicon carbide thin film layer, or a composite film layer of silicon thin film and silicon carbide thin film. The crystal morphology of the semiconductor layer material can include at least one of polycrystalline morphology, amorphous morphology, microcrystalline morphology, and nanomorphology. For example, the semiconductor layer material can be polycrystalline silicon, amorphous silicon, microcrystalline silicon, nanocrystalline silicon, or polycrystalline silicon carbide, amorphous silicon carbide, etc. This embodiment of the invention does not impose specific limitations on this.

[0101] Optionally, step S12 includes:

[0102] Step S121: Deposit a semiconductor layer on the second surface, and simultaneously perform element doping on the semiconductor layer during the deposition process to obtain the first doped semiconductor layer.

[0103] In this embodiment of the invention, the first doped semiconductor layer can be prepared by in-situ doping, that is, element doping is performed on the semiconductor layer during the process of forming the semiconductor layer. Furthermore, after in-situ doping of the semiconductor layer, it can be annealed at 700°C to 1000°C to obtain a higher quality first doped semiconductor layer.

[0104] In this embodiment of the invention, a certain amount of oxygen is introduced during annealing in the in-situ doping method, which may cause an oxide layer to form on the first doped semiconductor layer. This oxide layer can act as a barrier to the first doped semiconductor layer in subsequent processes, preventing the first doped semiconductor layer from being damaged by alkaline solution.

[0105] Or,

[0106] Optionally, step S12 includes:

[0107] Step S122: Deposit a semiconductor layer on the second surface;

[0108] Step S123: Perform element doping treatment on the semiconductor layer to obtain the first doped semiconductor layer.

[0109] In this embodiment of the invention, an in-situ doping method can also be used, that is, first depositing an intrinsic type semiconductor layer, and then performing element doping on the semiconductor layer after the semiconductor layer is deposited to form a first doped semiconductor layer. Optionally, the doping method for the semiconductor layer includes tubular thermal diffusion method, ion implantation followed by annealing method, doping source coating and advancement method, etc. This embodiment of the invention does not impose specific limitations on this.

[0110] In this embodiment of the invention, the method for forming the semiconductor layer may include CVD (Chemical Vapor Deposition), PVD (Physical Vapor Deposition), etc. The CVD method includes at least one of LPCVD (Low Pressure Chemical Vapor Deposition), PECVD, APCVD, and HWCVD (Hot Wire Chemical Vapor Deposition); the PVD method includes magnetron sputtering. In both in-situ doping and non-in-situ doping methods, the above-mentioned methods can be used to form the intrinsic type semiconductor layer or the in-situ doped first doped semiconductor layer.

[0111] Optionally, the thickness of the semiconductor layer is 20nm to 500nm.

[0112] In this embodiment of the invention, the thickness of the semiconductor layer can be any value between 20nm and 500nm, such as 20nm, 50nm, 100nm, 300nm, 500nm, etc.

[0113] Step S13: Under the protection of the first surface of the silicon substrate by the first surface barrier oxide layer, the first doped semiconductor layer on the first surface is removed by a wet process.

[0114] In this embodiment of the invention, the preparation of a first doped semiconductor layer on the second surface may result in the formation of a first doped semiconductor layer diffused around the first surface. In this case, the barrier oxide layer on the first surface can be retained first, and the first doped semiconductor layer diffused around the first surface can be removed. Optionally, the first doped semiconductor layer may also form an oxide layer due to process conditions, and this oxide layer should also be removed before removing the barrier oxide layer. For example, a chain alkaline cleaning process can be used to remove the first doped semiconductor layer, which is mainly amorphous or polycrystalline, deposited around the first surface. Optionally, a roller-type or conveyor-type chain single-sided film removal process can be used, which includes one or more tanks. The liquid level in the tank corresponds to the height of the silicon substrate. The first surface of the silicon substrate, including the first doped semiconductor layer, is immersed downwards through the liquid level in the tank. The tank may include potassium hydroxide or sodium hydroxide solution. Then, the first doped semiconductor layer deposited around the first surface of the silicon substrate is removed, and the first doped semiconductor layer on the second surface is completely or partially retained. Optionally, a water film device can be added to the single-sided chain stripping process. The water film device sprays water onto the first surface of the silicon substrate to form a water film. The water film can prevent the first doped semiconductor layer on the second surface from being removed when the silicon substrate passes through the tank.

[0115] In this embodiment of the invention, optionally, when there is an oxide layer on the surface of the first doped semiconductor layer, a tank alkaline cleaning process can also be used. The oxide layer can be formed by oxidation or oxygen annealing in an in-situ doping method, or it can be formed in a non-in-situ doping process or in a process such as element diffusion. The silicon substrate can be immersed in the tank cleaning alkaline solution to remove the first doped semiconductor layer diffused around the first surface. The oxide layer on the first surface is removed by a chain single-sided film removal process, and all or part of the oxide layer on the second surface is retained. In this way, in the immersion tank alkaline cleaning, the first doped semiconductor layer deposited around the first surface is removed, while the first doped semiconductor layer on the second surface is protected by the oxide layer and is not damaged.

[0116] In this embodiment of the invention, a water washing process can be added to the single-sided chain-type film removal process to clean the residual hydrofluoric acid and other film removal solutions, preventing the residual liquid from affecting subsequent processes. Optionally, before this water washing process, a cleaning process containing hydrochloric acid solution can be added to further reduce the residual metal ions on the substrate surface. The complexation effect of chloride ions can greatly reduce the metal ion content and avoid the impact of metal ions on the performance of solar cells. Optionally, a drying step can also be added to dry the silicon substrate surface and prevent it from being contaminated with dust or impurities from the air or tooling fixtures.

[0117] In this embodiment of the invention, after the first surface and the second surface are respectively subjected to elemental doping treatment to obtain the first doped layer and the first doped semiconductor layer, the barrier oxide layer on the first doped layer can be removed. Optionally, a chain-type or tank-type hydrofluoric acid solution can be used for cleaning. Further, other cleaning steps can be included, such as using hydrochloric acid, ozone water, water washing, etc., to ensure the cleaning effect. After removing the first oxide layer, the reflectivity of the first surface should be less than 14%, thereby retaining the textured structure of the low reflectivity of the first surface and improving the conversion efficiency of the battery. In addition, the treatment step of the second surface may cause other oxide layers to form on the second surface. Optionally, the oxide layer on the second surface can also be removed. This embodiment of the invention does not specifically limit this.

[0118] Optionally, a tunneling passivation layer is provided between the second surface of the substrate and the first doped semiconductor layer, the tunneling passivation layer comprising: silicon oxide.

[0119] In this embodiment of the invention, a tunneling passivation layer is further provided between the second surface of the substrate and the first doped semiconductor layer. Optionally, the material of the tunneling passivation layer can be a dielectric layer. The material of the tunneling passivation layer can be selected from at least one of hydrogenated amorphous silicon, silicon oxynitride, silicon carbide, silicon nitride, aluminum oxide, and silicon oxide. This embodiment of the invention does not impose specific limitations on this. Specifically, the tunneling passivation layer can be silicon oxide.

[0120] Optionally, the thickness of the tunneling passivation layer is 0.5 nm to 5 nm.

[0121] In this embodiment of the invention, the thickness of the tunneling passivation layer can be any value between 0.5 and 5 nm, such as 0.5 nm, 1 nm, 3 nm, 5 nm, etc. This embodiment of the invention does not impose any specific limitation on this.

[0122] Optionally, when preparing the first doped semiconductor layer by in-situ doping, the first doped semiconductor layer can be annealed to transform the semiconductor layer on the second surface, which is mainly amorphous, into the first doped semiconductor layer, which is mainly polycrystalline. During this process, tunneling pinholes will also be generated in the tunneling passivation layer. These tunneling pinholes are beneficial for the tunneling passivation layer on the second surface to better carry out carrier transport while ensuring the passivation effect, thereby improving the efficiency of the battery.

[0123] In this embodiment of the invention, other functional layers, such as passivation layers and electrodes, can also be formed on the first doped layer and the passivation contact structure to obtain a solar cell. Optionally, the boron doping process of the first doped layer can be replaced by a corresponding phosphorus doping process. For example, boron bromide diffusion or boron chloride diffusion can be replaced by phosphorus oxychloride thermal diffusion. Those skilled in the art can adjust the wet cleaning or electrode formation process according to the process and application requirements. This embodiment of the invention does not impose specific limitations on this.

[0124] Figure 6 shows a schematic diagram of another solar cell structure provided in an embodiment of the present invention. As shown in Figure 6, the solar cell includes a silicon substrate 501, a first doped layer 502, a first passivation layer 503, a first electrode 504, a tunneling passivation layer 505, a first doped semiconductor layer 506, a second passivation layer 507, and a second electrode 508. Specifically, the preparation process of the solar cell shown in Figure 6, through the solar cell preparation method described in steps 401 to 404, is as follows:

[0125] A silicon substrate 501 is provided;

[0126] The first surface of the silicon substrate 501 was textured using an alkaline solution to obtain a textured structure with an average pyramid size of 2 μm ;

[0127] At 700°C~1100°C, boron diffusion treatment is performed on the first surface using boron bromide or boron chloride tubular thermal diffusion to form a boron-doped first doped layer 502, and a barrier oxide layer with a thickness of 100nm is formed on the first doped layer 502. The surface doping concentration of the first doped layer 502 is $N_1=1\times 10^{17}\sim 5\times 10^{21}\text{cm}^{-3}$;

[0128] The second surface of the silicon substrate 501 is etched with a chain of acid or alkaline solutions to remove the coating that diffuses to the second surface during the formation of the first doped layer 502 and the barrier oxide layer.

[0129] A tunneling passivation layer 505 is formed on the second surface, and a first doped semiconductor layer 506 doped with phosphorus element is formed on the tunneling passivation layer 505. In the case of in-situ doping, a gas such as phosphine is used as the doping source gas, while in the case of non-in-situ doping, a gas such as phosphorus oxychloride can be used as the doping source.

[0130] The wrap-around coating formed on the first surface during the preparation of the first doped semiconductor layer 506 is removed by chain alkaline cleaning or tank alkaline cleaning.

[0131] The barrier oxide layer on the first doped layer 502 is removed by using a chain-type or tank-type hydrofluoric acid solution;

[0132] A first passivation layer 503 is formed on the first doped layer 502, and a second passivation layer 507 is formed on the first doped semiconductor layer 506;

[0133] A first electrode 504 is formed on the first passivation layer 502, and a second electrode 508 is formed on the first doped semiconductor layer 506.

[0134] In this embodiment of the invention, during the preparation of the solar cell, the average size of the pyramids in the textured structure of the first surface of the silicon substrate is controlled to be greater than or equal to 2 μm and less than 5 μm . Since the average size of the pyramids is relatively large and the distribution is relatively dispersed, the damage to the textured structure can be avoided during the formation of a barrier oxide layer with a thickness greater than 15 nm while ensuring that the silicon substrate has a low reflectivity and good light absorption through the pyramid structure. At this time, the thickness of the barrier oxide layer can achieve a good masking effect and at the same time avoid the influence of the thick oxide layer on the performance of the solar cell, thus significantly improving the efficiency of the solar cell.

[0135] Figure 7 shows a flowchart of the steps of a third method for preparing a solar cell provided in an embodiment of the present invention. As shown in Figure 7, the method may include:

[0136] Step 601: Provide a silicon substrate.

[0137] Step 602: Form a pyramidal textured structure on the first surface of the silicon substrate, wherein the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 5 μm .

[0138] In this embodiment of the invention, steps 601 to 602 can be referred to the relevant descriptions of steps 101 to 102 in the foregoing steps. To avoid repetition, they will not be repeated here.

[0139] Step 603: Perform element doping treatment on the first surface to simultaneously form a first doped layer and a barrier oxide layer located on the first doped layer. The elements include at least one of group IIIA elements and group VA elements, and the thickness of the barrier oxide layer is greater than 15 nm.

[0140] In this embodiment of the invention, step 603 can be referred to the relevant description of step 403 above. To avoid repetition, it will not be repeated here.

[0141] Optionally, the second surface of the substrate is opposite to the first surface.

[0142] Step 604: Form a passivation layer on the second surface of the substrate.

[0143] In this embodiment of the invention, in addition to forming a passivation contact structure on the second surface, a passivation layer can also be formed directly on the second surface of the substrate to suppress different defects on the second surface. Optionally, the passivation layer can be formed by PECVD (Plasma Enhanced Chemical Vapor Deposition), atomic layer deposition, or other methods. This embodiment of the invention does not impose specific limitations on this.

[0144] Optionally, the material of the passivation layer includes at least one of silicon nitride, silicon oxide, silicon oxynitride, aluminum oxide, silicon carbide, and amorphous silicon.

[0145] In this embodiment of the invention, a passivation layer may also be formed on the first surface. The materials of different passivation layers may be the same or different, and the passivation layer may be a single layer or two or more layers. One material or two or more materials may be used. For example, the passivation layer may be selected from at least one material among silicon nitride, silicon oxide, silicon oxynitride, aluminum oxide, silicon carbide, and amorphous silicon. This embodiment of the invention does not impose specific limitations on this.

[0146] In this embodiment of the invention, electrodes can also be prepared on the passivation layer. The preparation of the electrodes can be carried out using different metallization preparation methods, such as PVD (Physical Vapor Deposition), screen printing, electroplating, electroless plating, laser transfer, and spraying, or one or more of these methods. Optionally, the electrode formation process can include one or more temperature treatment processes, wherein the temperature range can be 100°C~900°C. Optionally, the electrodes corresponding to different passivation layers can be independently selected from at least one material among silver, copper, aluminum, nickel, titanium, tungsten, and tin. This embodiment of the invention does not impose specific limitations on this.

[0147] In this embodiment of the invention, a silver and copper-containing paste can be printed by screen printing, and then the electrode can be prepared by sintering or annealing at 500°C~900°C. Alternatively, a seed layer can be prepared first by PVD, then the seed layer can be patterned, and then the electrode can be prepared by electroplating. Finally, the electrode can be formed by annealing. Alternatively, a seed layer can be formed by electroless plating, then thickened by electroplating, and finally the electrode can be prepared by annealing. This embodiment of the invention does not impose specific limitations on the electrode preparation method.

[0148] Figure 8 shows a schematic diagram of another solar cell provided in an embodiment of the present invention. As shown in Figure 8, the solar cell includes a silicon substrate 701, a first doped layer 702, a first passivation layer 703, a first electrode 704, a back doped layer 705, a second passivation layer 706, and a second electrode 707. Specifically, the preparation process of the solar cell shown in Figure 8, through the solar cell preparation method described in steps 601 to 604, is as follows:

[0149] A silicon substrate 701 is provided;

[0150] The first surface of the silicon substrate 701 was textured using an alkaline solution to obtain a textured structure with an average pyramid size of 2.5 μm ;

[0151] At 700°C~1100°C, boron diffusion treatment is performed on the first surface using boron bromide or boron chloride tubular thermal diffusion to form a boron-doped first doped layer 702, and a barrier oxide layer with a thickness of 70nm is formed on the first doped layer 702. The surface doping concentration of the first doped layer 702 is $N_1=1\times 10^{17}\sim 5\times 10^{21}\text{cm}^{-3}$;

[0152] The second surface of the silicon substrate 701 is etched with a chain of acid or alkaline solutions;

[0153] The second surface is subjected to phosphorus doping treatment to obtain a back doped layer 705;

[0154] The barrier oxide layer on the first doped layer 702 is removed by using a chain-type or tank-type hydrofluoric acid solution;

[0155] A first passivation layer 703 is formed on the first doped layer 702, and a second passivation layer 706 is formed on the back doped layer 705;

[0156] A first electrode 704 is formed on the first passivation layer 703, and a second electrode 707 is formed on the second passivation layer 706.

[0157] In this embodiment of the invention, optionally, the boron doping process of the first doped layer can be replaced with the corresponding phosphorus doping process. For example, boron bromide diffusion or boron chloride diffusion can be replaced with phosphorus oxychloride thermal diffusion. Those skilled in the art can adjust the wet cleaning or electrode formation process according to the process and application requirements. This embodiment of the invention does not impose specific limitations on this.

[0158] In this embodiment of the invention, during the preparation of the solar cell, the average size of the pyramids in the textured structure of the first surface of the silicon substrate is controlled to be greater than or equal to 2 μm and less than 5 μm . Since the average size of the pyramids is relatively large and the distribution is relatively dispersed, the damage to the textured structure can be avoided during the formation of a barrier oxide layer with a thickness greater than 15 nm on the textured structure while ensuring that the silicon substrate has a low reflectivity and good light absorption through the pyramid structure. At this time, the thickness of the barrier oxide layer can achieve a good masking effect and at the same time avoid the influence of the thick oxide layer on the performance of the solar cell, thus significantly improving the efficiency of the solar cell.

[0159] Figure 9 shows a flowchart of the steps of the fourth method for preparing a solar cell provided in the embodiment of the present invention. As shown in Figure 9, the method may include:

[0160] Step 801: Provide a silicon substrate.

[0161] Step 802: Form a pyramidal textured structure on the first surface of the silicon substrate, wherein the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 5 μm .

[0162] In this embodiment of the invention, steps 801 to 802 can be referred to the relevant descriptions of steps 101 to 102 in the foregoing steps. To avoid repetition, they will not be repeated here.

[0163] Step 803: Perform element doping treatment on the first surface to form a first doped layer, wherein the element includes at least one of group IIIA elements and group VA elements.

[0164] In this embodiment of the invention, the first surface can be first subjected to element doping treatment to form a first doped layer, and then the silicon substrate can be placed in an oxidizing atmosphere on the textured structure of the first surface for thermal oxidation to form a barrier oxide layer on the first doped layer. At this time, more element doping treatment methods can be used to dope the first surface, and those skilled in the art can choose according to specific needs.

[0165] Optionally, the element doping treatment in step 803 is one of thermal diffusion process, ion implantation or in-situ doping.

[0166] In this embodiment of the invention, the element doping treatment can be any one of thermal diffusion process, ion implantation or in-situ doping. The thermal diffusion process can be referred to the relevant description of step 403 above, and will not be repeated here to avoid repetition. Ion implantation can be to accelerate the ions of group IIIA elements or group VA elements at low temperature so that the ions of group IIIA elements or group VA elements enter the first surface to form the first doped layer. In-situ doping can refer to the simultaneous introduction of a gas containing impurity elements for doping while forming the first surface, thereby improving the production efficiency of the first doped layer.

[0167] Step 804: On the textured surface of the first surface, the first doped layer is thermally oxidized to form a barrier oxide layer.

[0168] In this embodiment of the invention, after the first doped layer is formed, the first doped layer can be thermally oxidized to form a barrier oxide layer on the first doped layer. Optionally, step 804 can be referred to the relevant description of step 203 above, and will not be repeated here to avoid repetition.

[0169] Optionally, the second surface of the substrate is opposite to the first surface.

[0170] Step 805: Form a passivated contact structure on the second surface of the substrate.

[0171] In this embodiment of the invention, step 805 can be referred to the relevant description of step 404 above. To avoid repetition, it will not be repeated here.

[0172] In this embodiment of the invention, during the preparation of the solar cell, the average size of the pyramids in the textured structure of the first surface of the silicon substrate is controlled to be greater than or equal to 2 μm and less than 5 μm . Since the average size of the pyramids is relatively large and the distribution is relatively dispersed, the damage to the textured structure can be avoided during the formation of a barrier oxide layer with a thickness greater than 15 nm on the textured structure while ensuring that the silicon substrate has low reflectivity and good light absorption through the pyramid structure. At this time, the thickness of the barrier oxide layer can achieve a good masking effect and at the same time avoid the influence of the thick oxide layer on the performance of the solar cell, significantly improving the efficiency of the solar cell.

[0173] Figure 10 is a flowchart of the steps of the fifth method for preparing a solar cell provided in the embodiment of the present invention. As shown in Figure 10, the method may include:

[0174] Step 901: Provide a silicon substrate.

[0175] Step 902: Form a pyramidal textured structure on the first surface of the silicon substrate, wherein the average size of the pyramids in the textured structure is greater than or equal to 2 μm and less than 5 μm .

[0176] In this embodiment of the invention, steps 901 to 902 can be referred to the relevant descriptions of steps 101 to 102 in the foregoing steps. To avoid repetition, they will not be repeated here.

[0177] Step 903: Perform element doping treatment on the first surface to form a first doped layer, wherein the element includes at least one of group IIIA elements and group VA elements.

[0178] In this embodiment of the invention, step 903 can be referred to the relevant description of step 803 above. To avoid repetition, it will not be described again here.

[0179] Step 904: On the textured surface of the first surface, the first doped layer is thermally oxidized to form a barrier oxide layer.

[0180] In this embodiment of the invention, after the first doped layer is formed, the first doped layer can be thermally oxidized to form a barrier oxide layer on the first doped layer. Optionally, step 904 can be referred to the relevant description of step 203 above, and will not be repeated here to avoid repetition.

[0181] Optionally, the second surface of the substrate is opposite to the first surface.

[0182] Step 905: Form a passivation layer on the second surface of the substrate.

[0183] In this embodiment of the invention, step 905 can be referred to the relevant description of step 604 above. To avoid repetition, it will not be repeated here.

[0184] In this embodiment of the invention, during the preparation of the solar cell, the average size of the pyramids in the textured structure of the first surface of the silicon substrate is controlled to be greater than or equal to 2 μm and less than 5 μm . Since the average size of the pyramids is relatively large and the distribution is relatively dispersed, the damage to the textured structure can be avoided during the formation of a barrier oxide layer with a thickness greater than 15 nm on the textured structure while ensuring that the silicon substrate has low reflectivity and good light absorption through the pyramid structure. At this time, the thickness of the barrier oxide layer can achieve a good masking effect and at the same time avoid the influence of the thick oxide layer on the performance of the solar cell, significantly improving the efficiency of the solar cell.

[0185] This embodiment of the invention also provides a solar cell, which is prepared by the method for preparing solar cells described in Figures 1 to 8.

[0186] Parameter Comparison Example

[0187] The present invention also provides a solar cell parameter comparison experiment. Using an N-type silicon wafer with a thickness of 180 μm and a resistivity of 1 $\Omega\text{ cm}$ as the silicon substrate, experimental groups No. 1 with an average pyramid size of 1.5 μm , No. 2 with an average pyramid size of 2.5 μm , No. 3 with an average pyramid size of 3 μm , No. 4 with an average pyramid size of 4 μm , No. 5 with an average pyramid size of 5 μm , and No. 6 with an average pyramid size of 6 μm were prepared respectively. In this study, the peak boron diffusion temperature of the solar cells in each experimental group was 980°C. During the boron diffusion process, a dry oxygen oxidation method was used to oxidize the first surface of the silicon substrate at 980°C to obtain a barrier oxide layer while simultaneously advancing the boron diffusion PN junction. Then, the second surface of the silicon substrate was cleaned with hydrofluoric acid, followed by etching with a mixed solution of nitric acid, hydrofluoric acid, and sulfuric acid to remove the PN junction. Phosphorus doping was performed on the amorphous silicon of the second surface using phosphorus oxychloride to crystallize it into polycrystalline silicon. Chain-type alkaline etching was used to remove the polycrystalline silicon coated around the first surface, followed by the removal of the barrier oxide layer on the first surface and the oxide layer formed during phosphorus diffusion on the second surface using hydrofluoric acid. After cleaning with hydrochloric acid and drying, the first surface was passivated using ALD (Atomic Layer Deposition) aluminum oxide, and the solar cells in each experimental group underwent double-sided silicon nitride passivation using PECVD to obtain a passivation layer. Electrodes were formed on the passivation layers of the first and second surfaces using silver paste, respectively, to obtain the solar cells for each experimental group.

[0188] In this embodiment of the invention, the performance of the solar cells in each experimental group was tested. The test parameters of experimental group 1 were used as a comparison, and the test parameters of each group are shown in the table below:

[0189] Comparison table of battery performance parameters for the experimental group

[0190]

Experimental group number	Uoc/mV	Isc/mA	FF/%	Eta/%	Remark
1	0	0	0	0	
2	+1	+40	+0.20	+0.18	Relative value to experimental group 1
3	+2	+27	+0.05	+0.14	Relative value to experimental group 1
4	+2	+23	+0.01	+0.12	Relative value to experimental group 1
5	+2	+10	-0.22	+0.02	With No. 1

[0191]

					Relative value of the test group
6	+3	-10	-0.56	-0.08	Relative value to experimental group 1

[0192] As can be seen from the table above, when the average size of the pyramid with the textured surface is between 2 μm and 4 μm , the battery parameters show a significant improvement compared to when the average size of the pyramid is 1.5 μm . When the average size of the pyramid is 5 μm , the improvement in parameters is not significant compared to 1.5 μm , and even the fill factor (FF) decreases. When the average size of the pyramid is 6 μm , the improvement in parameters further decreases compared to 1.5 μm , with FF and ISC (short circuit current) showing the most significant decreases. The circuit current is significantly reduced. Therefore, the solution of this embodiment can significantly improve the efficiency of solar cells.

[0193] It should be noted that, for the sake of simplicity, the method embodiments are all described as a series of actions. However, those skilled in the art should understand that the embodiments of this application are not limited to the described order of actions, because according to the embodiments of this application, some steps can be performed in other orders or simultaneously. Secondly, those skilled in the art should also understand that the embodiments described in the specification are all preferred embodiments, and the actions involved are not necessarily necessary for the embodiments of this application.

[0194] It should be noted that, in this document, the terms "comprising," "including," or any other variations thereof are intended to cover non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements includes not only those elements but also other elements not expressly listed, or elements inherent to such a process, method, article, or apparatus. Without further limitation, an element defined by the phrase "comprising one..." does not exclude the presence of other identical elements in the process, method, article, or apparatus that includes that element.

[0195] The embodiments of the present invention have been described above with reference to the accompanying drawings. However, the present invention is not limited to the specific embodiments described above. The specific embodiments described above are merely illustrative and not restrictive. Those skilled in the art can make many other forms under the guidance of the present invention without departing from the spirit and scope of the claims. All of these are within the protection scope of the present invention.

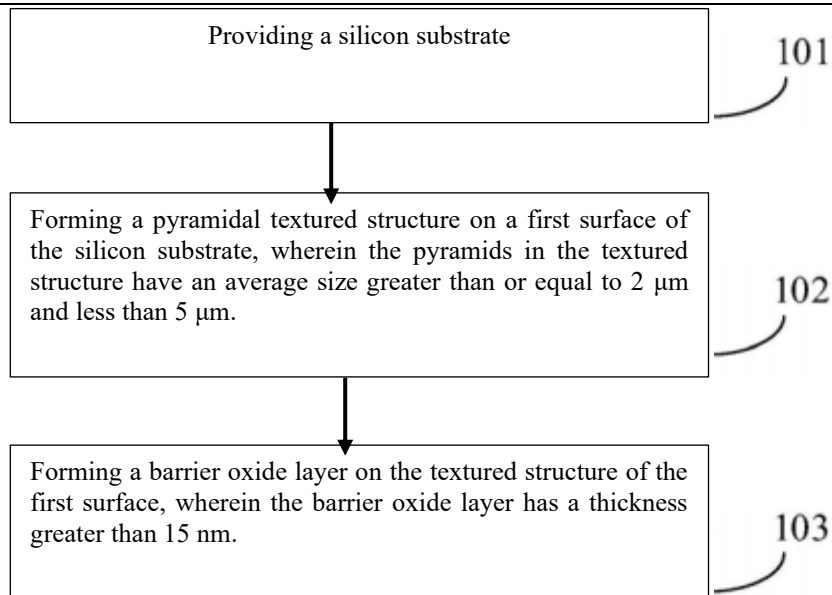


Figure 1

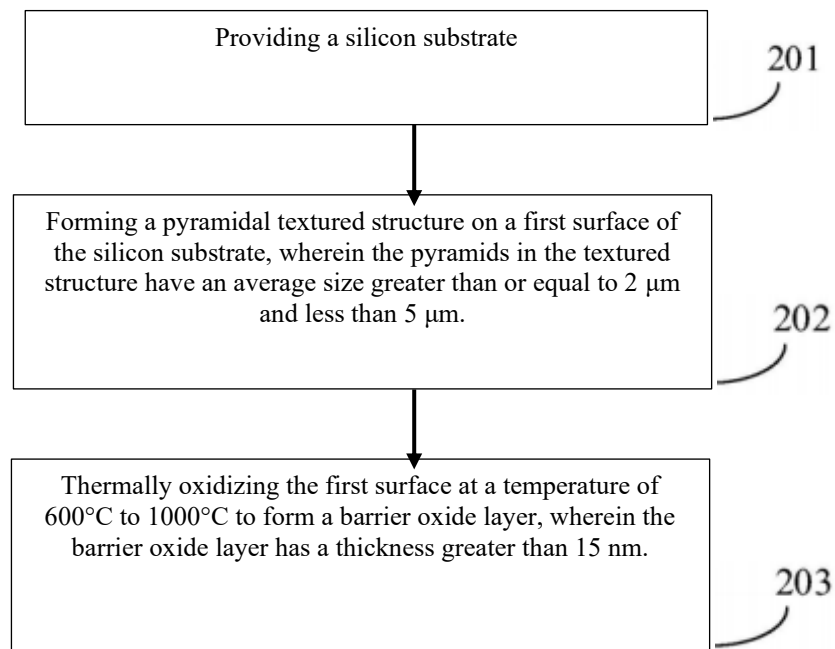


Figure 2

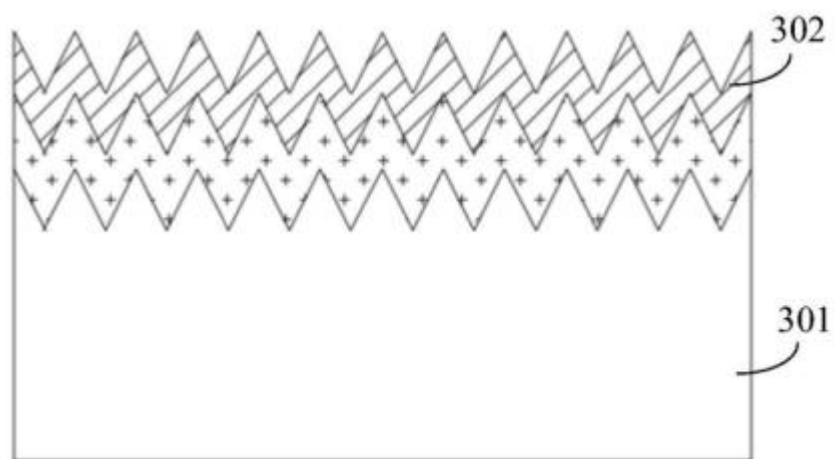


Figure 3

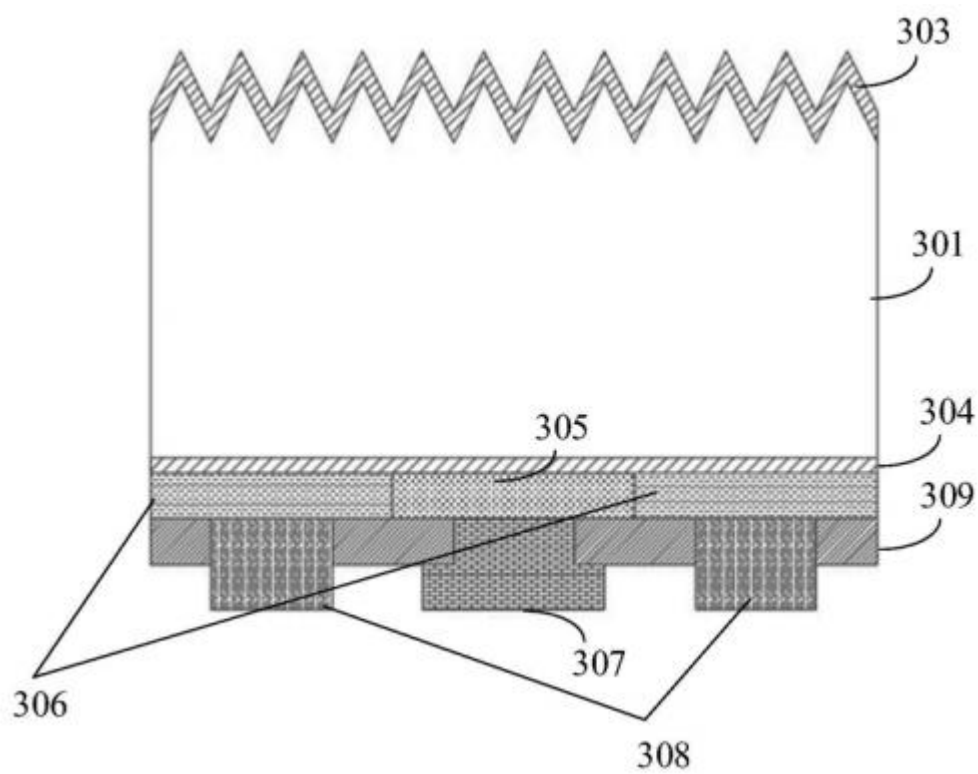


Figure 4

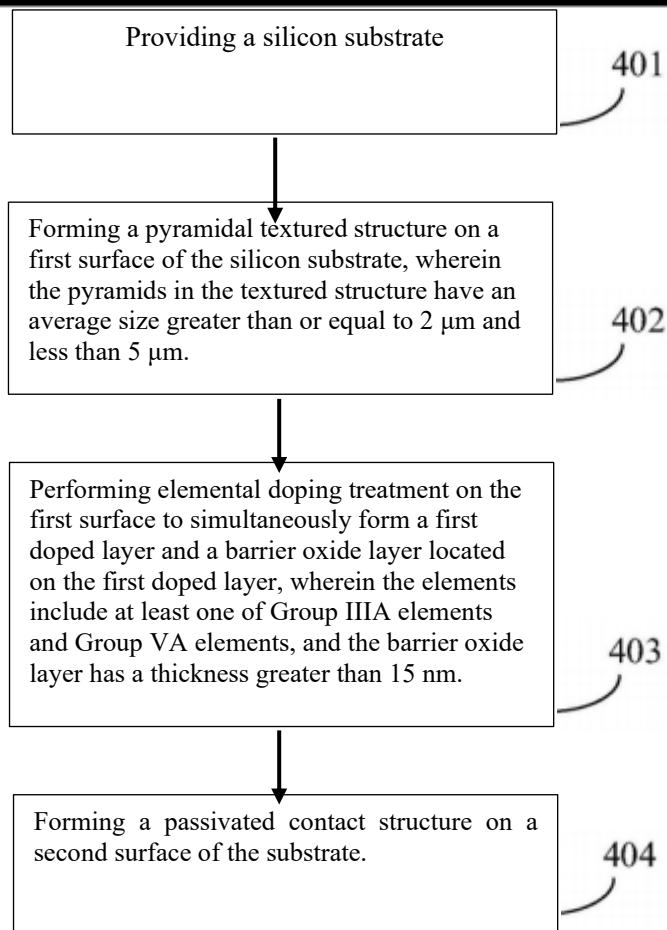


Figure 5

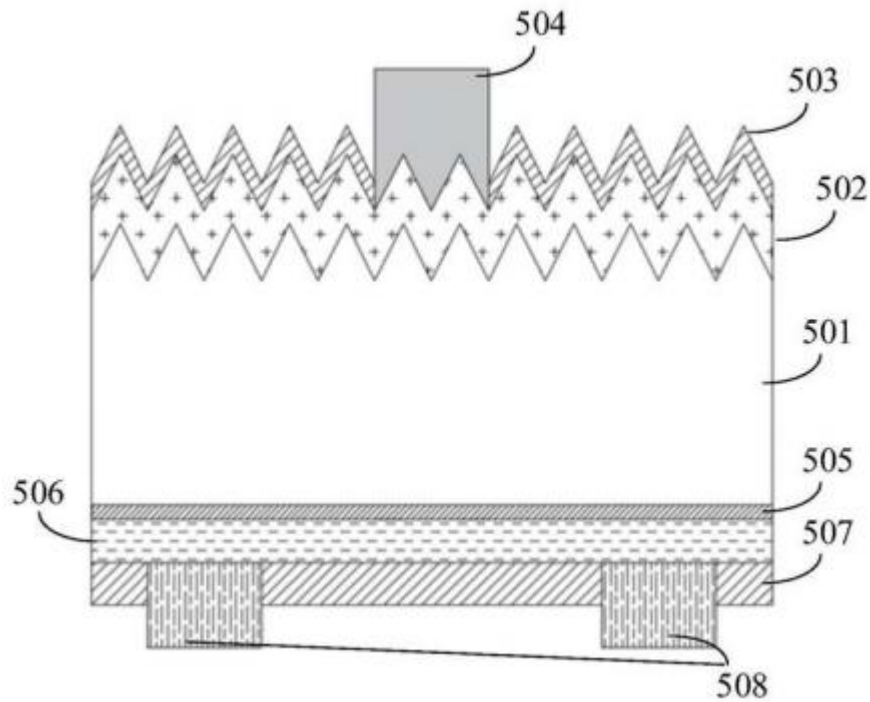


Figure 6

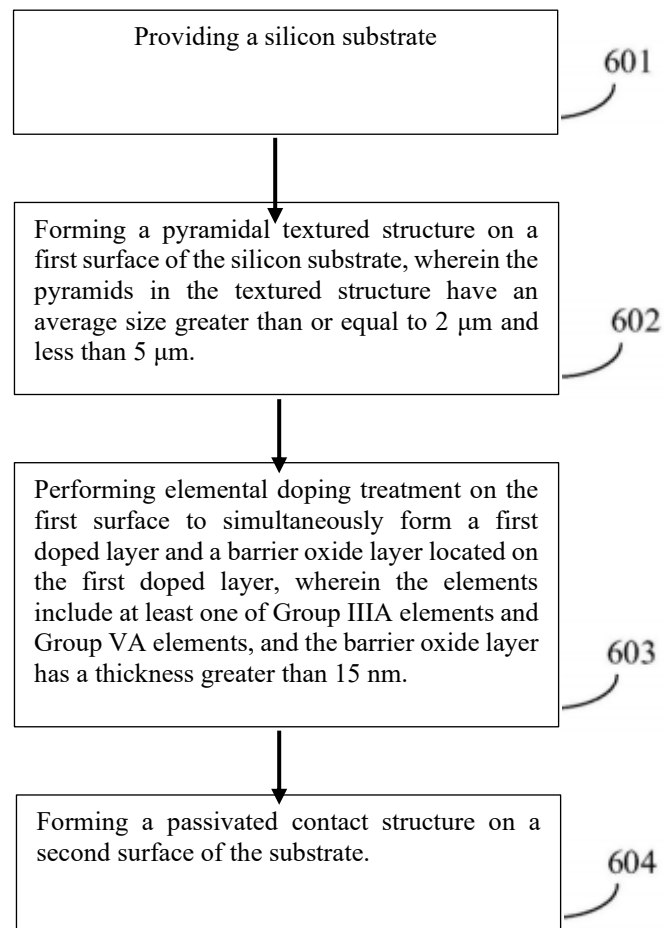


Figure 7

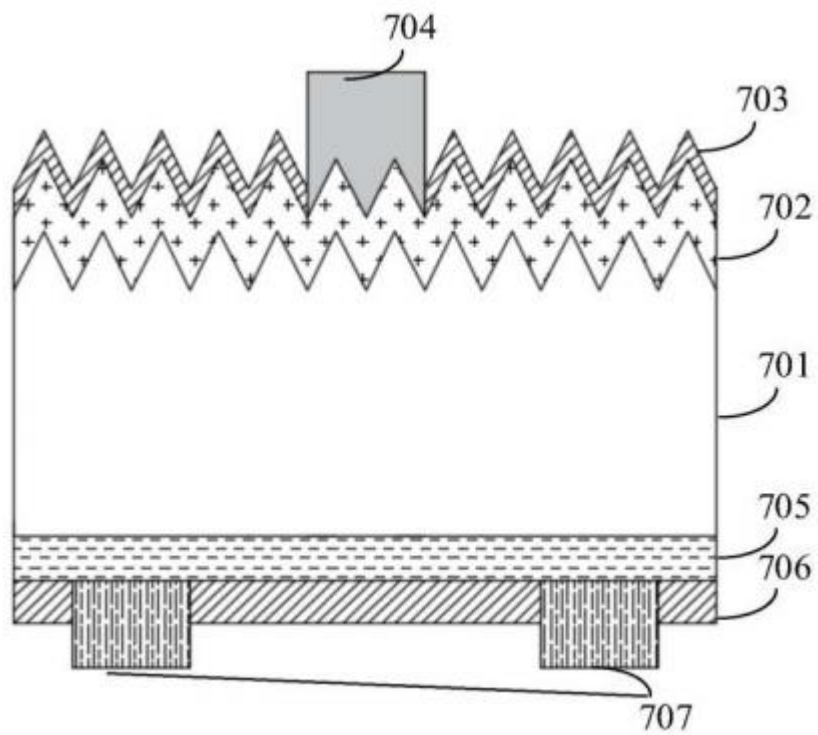


Figure 8

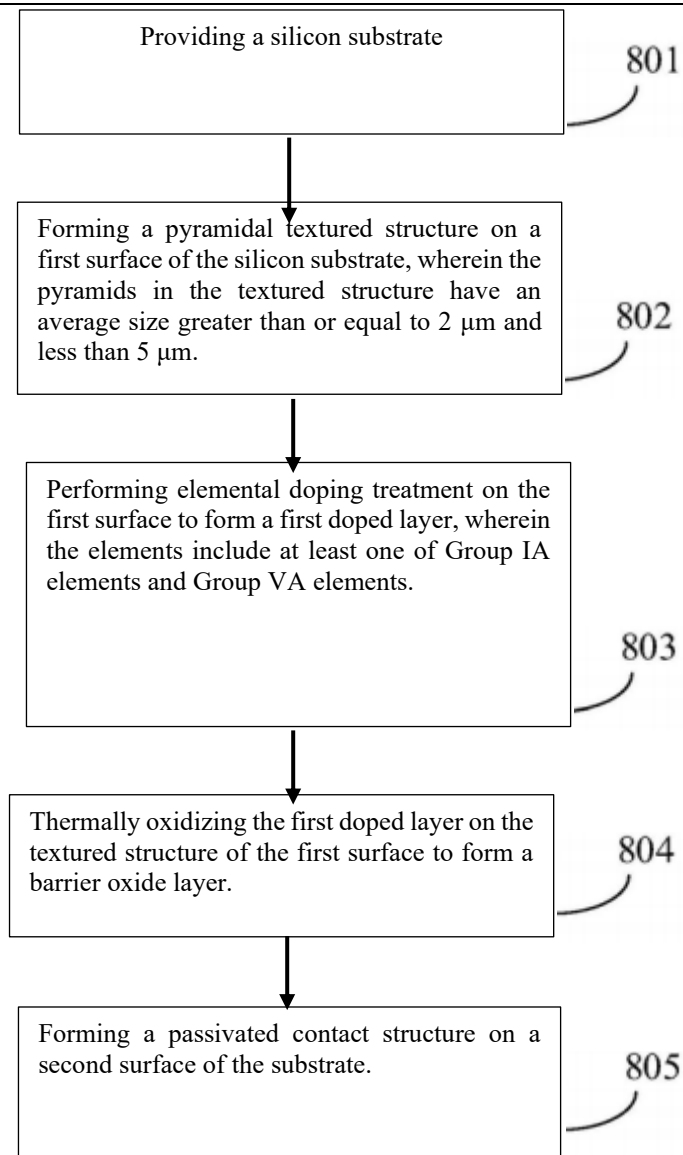


Figure 9

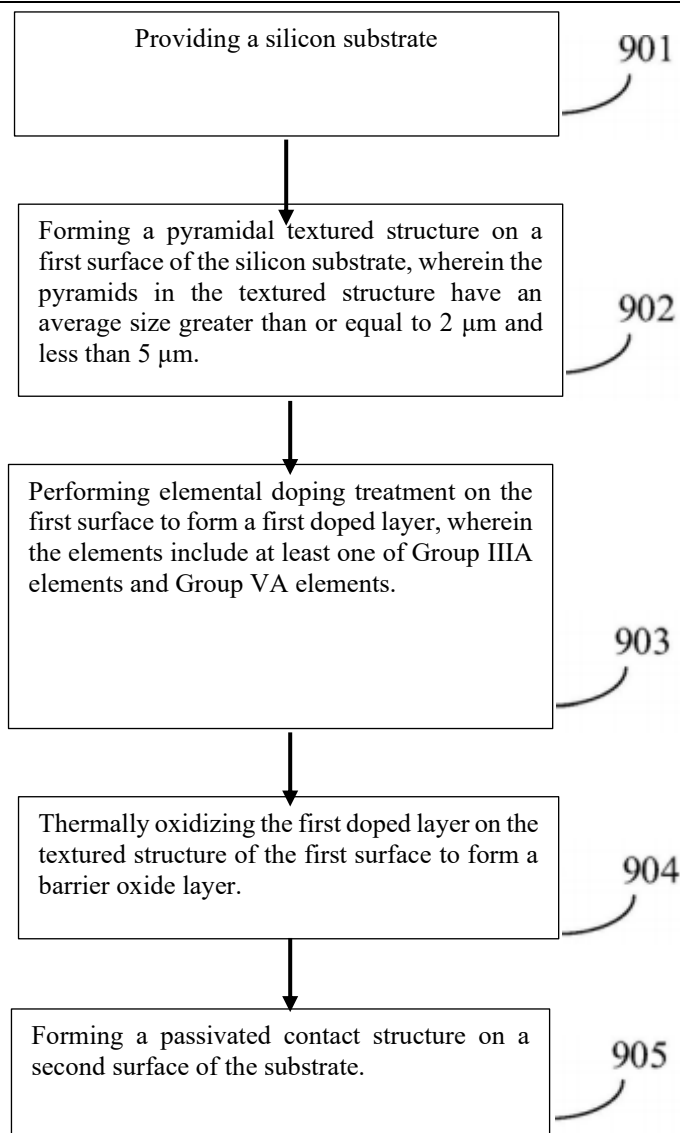


Figure 10

CERTIFICATE OF ACCURACY

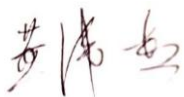
Attached as Ex A is the original document identified as patent application number CN112635591 A and attached as Ex B is the translation of the original document from Chinese to English.

This is to certify under penalty of perjury that I, Weijie Huang, translated the document attached as Exhibit B and it is a true, accurate, and complete translation of Exhibit A.

I am thoroughly familiar with and competent in both Chinese and English languages. I have over 15 years of experience in translating Chinese to English and hold a Bachelor's degree in Linguistics from Beijing Language and Culture University. Attached as Exhibit C is a copy of my current CV.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 01/19/2026



Weijie Huang
Chinese > English Linguist

Your
legal
translation
partner 

Weijie Huang

Highlights

15 years in translation between Chinese and English in multiple domains with a focus on litigation.

Experience

Translator | Mar 2008 – Present

- Extensive experience translating litigation and dispute-related documents, including court pleadings, judgments, affidavits, witness statements, evidentiary materials, and legal correspondence for use in cross-border litigation and arbitration.
- Proven expertise in financial and corporate translation, covering annual reports, audited financial statements, investment agreements, shareholder agreements, trust deeds, compliance materials, and internal governance documents.
- Specialized experience in patent and IP translation, including patent specifications, claims, abstracts, office actions, prosecution history, prior art references, and related technical-legal documentation, with strict adherence to jurisdiction-specific terminology and formatting requirements.

Partial list of subject matter experience:

Telecommunications

- 4G/LTE, 5G NR, and 6G Standards
- Network Architecture and Protocols (TCP/IP, RAN, NFV)
- Wireless and Mobile Communication
- Signal Processing and Data Encoding
- Internet of Things (IoT) and M2M
- Satellite and Microwave Communication
- Cybersecurity and Encryption Protocols

Mechanical Engineering

- Automotive Engineering (EV Drivetrains, Autonomous Systems)
- Robotics and Industrial Automation
- Thermodynamics and Heat Exchange Systems
- Fluid Dynamics and Hydraulic/Pneumatic Systems
- Aerospace and Aeronautical Engineering
- Manufacturing and Tooling (CNC, Additive Manufacturing)

Pharmaceuticals

- Drug Delivery
- Biologics and Monoclonal Antibodies (mAbs)
- Gene and Cell Therapy (CRISPR, mRNA)
- Small Molecule Synthesis and API Manufacturing
- Pharmacokinetics and Pharmacodynamics (ADME)
- Clinical Trial Protocols and Regulatory Documentation
- Immunology and Vaccine Development
- Medicinal Chemistry

Chemistry

- Polymer and Materials Science
- Organic and Inorganic Synthesis
- Electrochemistry (Batteries, Fuel Cells)
- Heterogeneous and Homogeneous Catalysis
- Nanotechnology and Nanomaterials
- Petrochemicals and Refining Processes
- Analytical Chemistry and Spectroscopic Methods
- Biochemistry and Enzymology

- Regularly handles high-stakes legal translations submitted to courts, regulators, arbitration panels, and government authorities, ensuring precision, consistency, and defensibility of terminology.
- Deep familiarity with common law and civil law systems, enabling accurate rendering of legal concepts across jurisdictions without distortion of legal effect or procedural meaning.
- Experienced in translating complex, multi-entity and multi-jurisdictional matters, including materials involving offshore structures, trusts, cross-border investments, and regulatory filings.
- Skilled in maintaining terminology consistency across large-volume projects through glossaries, style guides, and parallel reference materials, particularly in long-running litigation or patent portfolios.
- Experienced in producing certified and court-ready translations, including Certificates of Accuracy where required, and working under tight litigation and regulatory deadlines.
- Comfortable collaborating with law firms, in-house legal teams, IP professionals, financial advisors, and compliance teams, responding to revision requests and clarification queries with precision and professionalism.
- Strong attention to detail, formatting fidelity, and document structure, ensuring translated documents mirror the original legal and technical layout for seamless reference and submission.

Education and Training

Bachelor of English Language and Literature, Beijing Language & Culture University (BLCU) (2004-2008)
Master of Professional Studies, Informatics with Concentration in Data Analytics, Northeastern University, (2022-2024)

Skills & Language Abilities

Bilingual (English-Mandarin) with fluency in Cantonese and basic French