

EXHIBIT 2

EXHIBIT 2–Infringement Chart for U.S. Patent No. 11,824,136 (the “’136 Patent”)

The accused products may include, but not limited to, various module types (e.g., SEG’s Alpine N and Yukon N series of solar modules), including SEG-435-BTE-BG, SEG-440-BTE-BG, SEG-445-BTE-BG, SEG-450-BTE-BG, SEG-495-BTD-BG, SEG-500-BTD-BG, SEG-505-BTD-BG, SEG-510-BTD-BG, SEG-610-BTC-BG, SEG-615-BTC-BG, SEG-620-BTC-BG, SEG-625-BTC-BG, SEG-700-BTC-BG, SEG-705-BTC-BG, SEG-710-BTC-BG, SEG-715-BTC-BG, SEG-420-BTD-BG, SEG-425-BTD-BG, SEG-430-BTD-BG, SEG-435-BTD-BG, SEG-440-BTD-BG, SEG-445-BTD-BG, SEG-480-BTB-BG, SEG-485-BTB-BG, SEG-490-BTB-BG, SEG-495-BTB-BG, SEG-575-BTA-BG, SEG-580-BTA-BG, SEG-585-BTA-BG, SEG-590-BTA-BG, SEG-595-BTA-BG, SEG-625-BTZ-BG, SEG-630-BTZ-BG, SEG-635-BTZ-BG, SEG-640-BTZ-BG, and all substantially similar equivalents thereof. (*See generally* <https://www.segsolar.com/Public/Uploads/uploadfile/files/20250424/SEG435450BTEFullBlackBG210REN.pdf>, <https://www.segsolar.com/Public/Uploads/uploadfile/files/20250424/SEG495510BTDFullBlackBG210REN.pdf>, <https://www.segsolar.com/Public/Uploads/uploadfile/files/20241227/SEG700715BTCBG210EN.pdf>, <https://www.segsolar.com/Public/Uploads/uploadfile/files/20241227/SEG610625BTCBG210EN.pdf>, <https://www.segsolar.com/Public/Uploads/uploadfile/files/20250424/SEG430445BTDFullBlackBG182EN.pdf>, <https://www.segsolar.com/Public/Uploads/uploadfile/files/20250424/SEG480495BTBBG182EN.pdf>, <https://www.segsolar.com/Public/Uploads/uploadfile/files/20250424/SEG580595BTABG182EN.pdf>, <https://www.segsolar.com/Public/Uploads/uploadfile/files/20241227/SEG625640BTZBG182EN.pdf>, https://cdn.mycd.com/images/Products/ZZ0000/ZZ3098/00000/ZZ309800015_DS.pdf, https://cdn.mycd.com/images/Products/ZZ0000/ZZ3098/00000/ZZ309800017_DS.pdf.)

A chart of claim 1 against exemplary SEG-420-BTD-BG is provided below.

Annotations and identification of elements in this chart are preliminary, are not final, nor are they intended to limit Plaintiff’s identification of claim elements in Defendants’ infringing products. Furthermore, SEG-420-BTD-BG and the below claims have been provided as representative, and Plaintiff reserves the right to identify additional products and claims, and identify further representative products as discovery progresses. Plaintiff reserves the right to amend, supplement, expand, modify, or narrow its identifications in the accused products as it develops facts during discovery, based on the Court’s claim constructions, or for any other allowable purpose in this action.

’136 Patent Claim Limitation	SEG-420-BTD-BG
1[preamble] A solar cell, comprising:	The SEG-420-BTD-BG includes a solar cell.

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'136 Patent Claim Limitation	SEG-420-BTD-BG
	 The datasheet¹ of the SEG-420-BTD-BG (photovoltaic module), specifically as outlined in the red box, represents that the SEG-420-BTD-BG includes 108 N-type solar cells, which suggests each solar cell of the SEG-420-BTD-BG has an N-type silicon substrate.

¹ Available at https://cdn.mycad.com/images/Products/ZZ0000/ZZ3098/00000/ZZ309800015_DS.pdf.

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'136 Patent Claim Limitation	SEG-420-BTD-BG																								
	Mechanical Specifications <table border="1"> <tr> <td>External Dimension</td><td>1722 x 1134 x 30 mm</td></tr> <tr> <td>Weight</td><td>24.0 kg</td></tr> <tr> <td>Solar Cells</td><td>N-Type 182 x 91 mm(108 pcs)</td></tr> <tr> <td>Front Glass</td><td>2.0 mm AR coating semi-tempered glass</td></tr> <tr> <td>Back Glass</td><td>2.0 mm Semi-tempered glass</td></tr> <tr> <td>Frame</td><td>Black anodized aluminium alloy</td></tr> <tr> <td>Junction Box</td><td>IP68 / 3 diodes</td></tr> <tr> <td>Connector Type</td><td>MC4</td></tr> <tr> <td>Cable Type</td><td>12 AWG PV Wire(UL)</td></tr> <tr> <td>Cable Length</td><td>Portrait: 400 mm(+) / 200 mm(-) Landscape: 1200 mm(+) / 1200 mm(-) or customized length</td></tr> <tr> <td>Mechanical Load(Front)</td><td>5400 Pa / 113 psf*</td></tr> <tr> <td>Mechanical Load(Rear)</td><td>2400 Pa / 50 psf*</td></tr> </table> *Refer to SEG installation manual for details A front side photo of the SEG-420-BTD-BG is provided below. As shown, the SEG-420-BTD-BG includes 108 solar cells (with an example solar cell identified in a yellow box).	External Dimension	1722 x 1134 x 30 mm	Weight	24.0 kg	Solar Cells	N-Type 182 x 91 mm(108 pcs)	Front Glass	2.0 mm AR coating semi-tempered glass	Back Glass	2.0 mm Semi-tempered glass	Frame	Black anodized aluminium alloy	Junction Box	IP68 / 3 diodes	Connector Type	MC4	Cable Type	12 AWG PV Wire(UL)	Cable Length	Portrait: 400 mm(+) / 200 mm(-) Landscape: 1200 mm(+) / 1200 mm(-) or customized length	Mechanical Load(Front)	5400 Pa / 113 psf*	Mechanical Load(Rear)	2400 Pa / 50 psf*
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'136 Patent Claim Limitation	SEG-420-BTD-BG
	
1[a] a semiconductor substrate,	The SEG-420-BTD-BG includes a “semiconductor substrate.” The SEG-420-BTD-BG has an N-type silicon substrate. The datasheet² of the SEG-420-BTD-BG (photovoltaic module), specifically as outlined in the red box, indicates that the SEG-420-BTD-BG includes 108 N-type solar cells, which suggests each solar cell of the SEG-420-BTD-BG has an N-type silicon substrate.

² Available at https://cdn.myced.com/images/Products/ZZ0000/ZZ3098/00000/ZZ309800015_DS.pdf.

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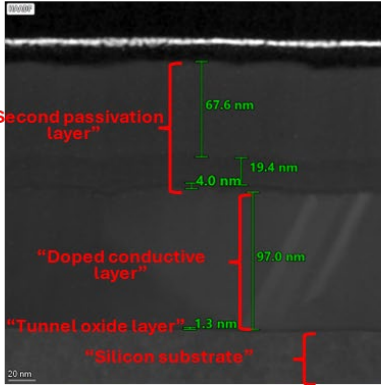
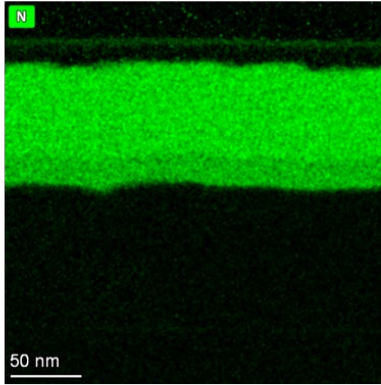
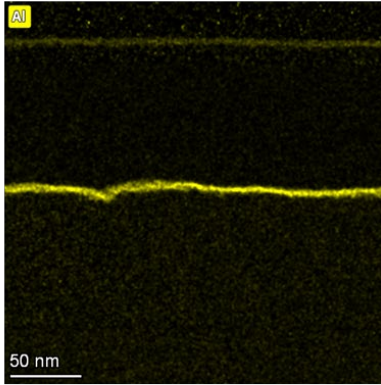
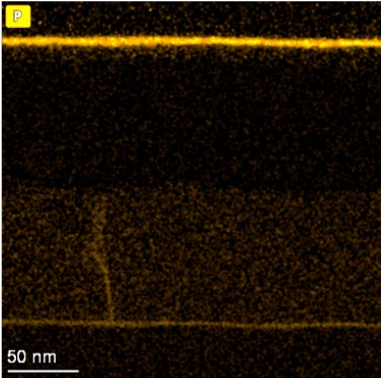
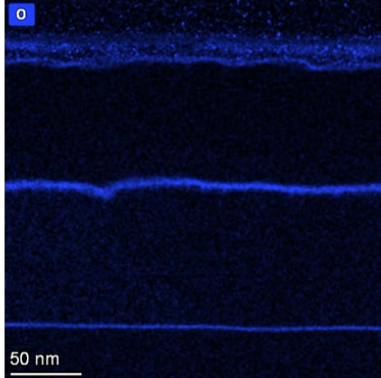
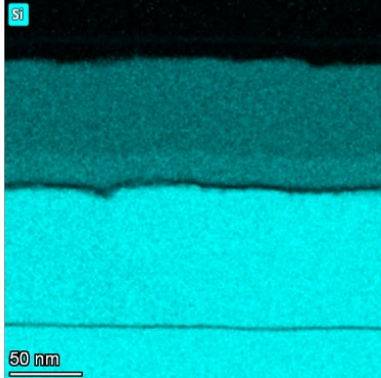
'136 Patent Claim Limitation	SEG-420-BTD-BG
	Rear side  “Second passivation layer” 67.6 nm 4.0 nm 19.4 nm “Doped conductive layer” 97.0 nm “Tunnel oxide layer” 1.3 nm “Silicon substrate” 20 nm  N 50 nm  Al 50 nm  P 50 nm  O 50 nm  Si 50 nm

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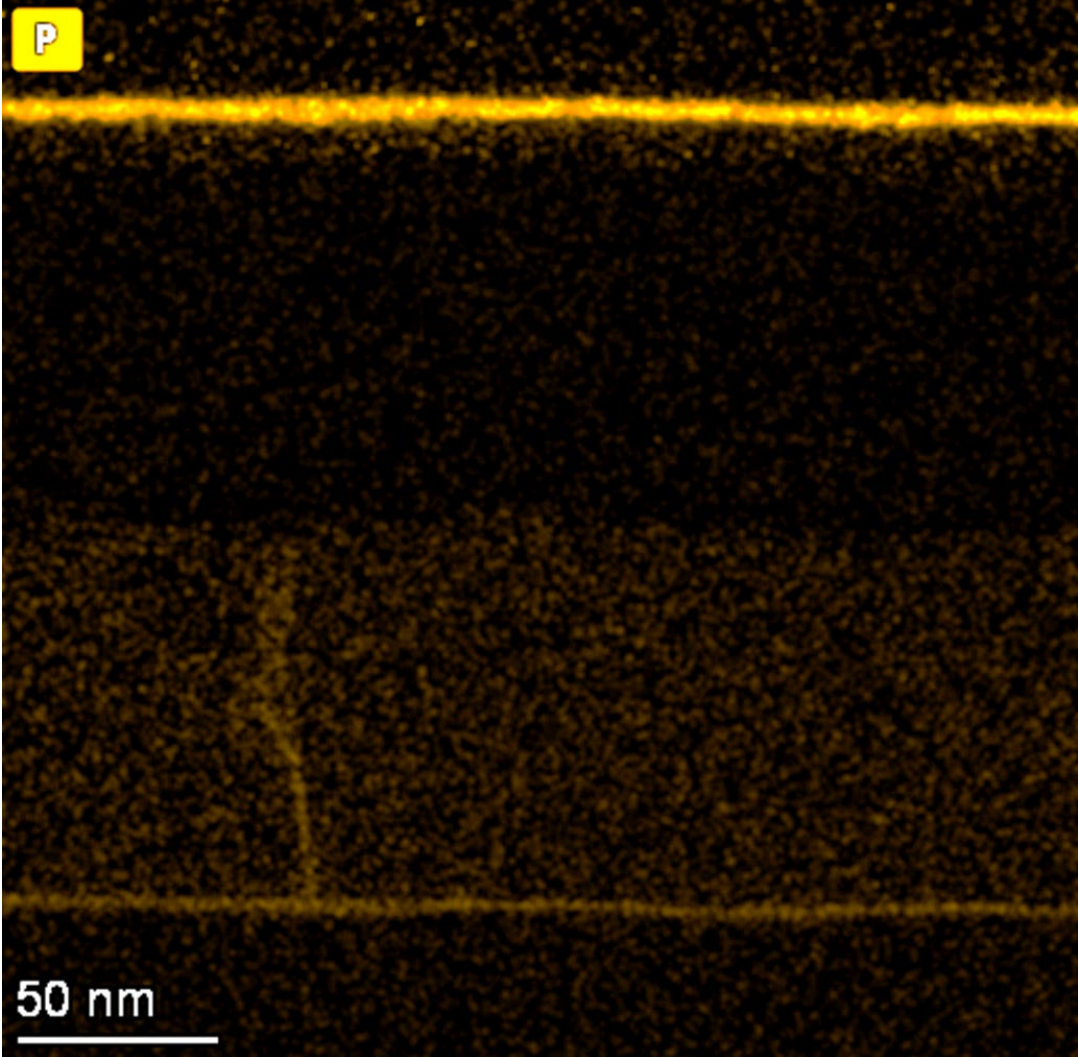
'136 Patent Claim Limitation	SEG-420-BTD-BG
	
1[b] wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture	The SEG-420-BTD-BG includes a rear surface of the semiconductor substrate having a first texture structure, where the first texture structure has a non-pyramid microstructure and includes two or more first substructures at least partially stacked on one another.

EXHIBIT 2–Infringement Chart for U.S. Patent No. 11,824,136 (the “’136 Patent”)

'136 Patent Claim Limitation	SEG-420-BTD-BG
structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another,	The below laser confocal microscopy images of the SEG-420-BTD-BG (with the main image on the right and the 3D image on the left) show that a rear surface of the semiconductor substrate in the SEG-420-BTD-BG has a first texture structure. For instance, the first texture includes two first substructures A and B partially stacked on one another (in the black oval), as shown in the main image (right), and are of different heights, as denoted in different colors in the 3D image (left), where blue represents the lowest height, red represents the highest height, and other colors represent heights in between.
1[c] a top surface of the first substructure is a polygonal plane,	The SEG-420-BTD-BG includes a top surface of the first substructure is a polygonal plane. The example laser confocal microscopy images above in limitation 1[b] demonstrate that a top surface of the first substructure (either first substructure A or first substructure B) is a polygonal plane.

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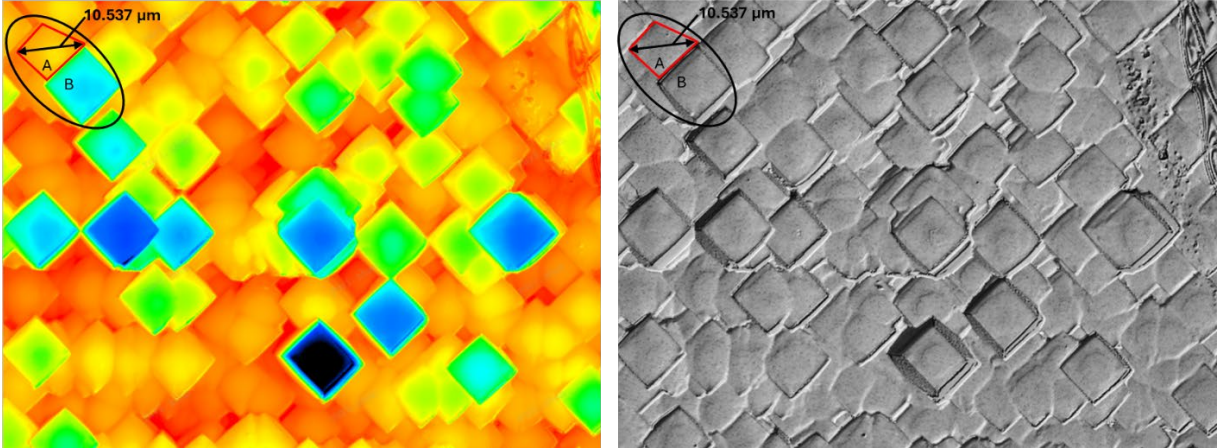
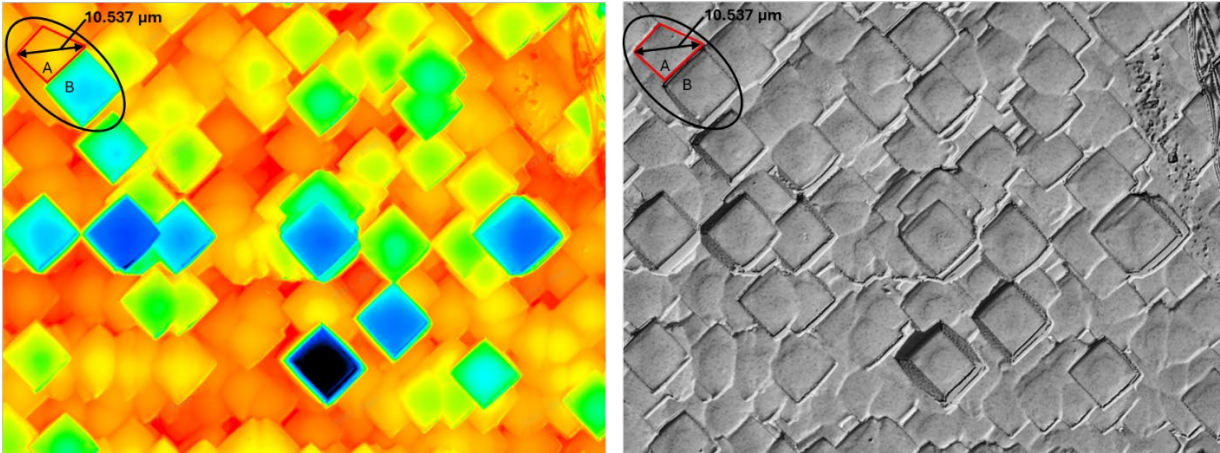
'136 Patent Claim Limitation	SEG-420-BTD-BG
	
1[d] and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm;	The SEG-420-BTD-BG includes a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm. As shown in the laser confocal microscopy images in limitation 1[b], the first substructure A is an example of the “outermost first substructure.” The maximum diagonal, representing an example of the “one-dimensional size” (denoted by the two-directional arrow), of the top surface of the first substructure A is 10.537 μm, thus satisfying the claim limitation. 

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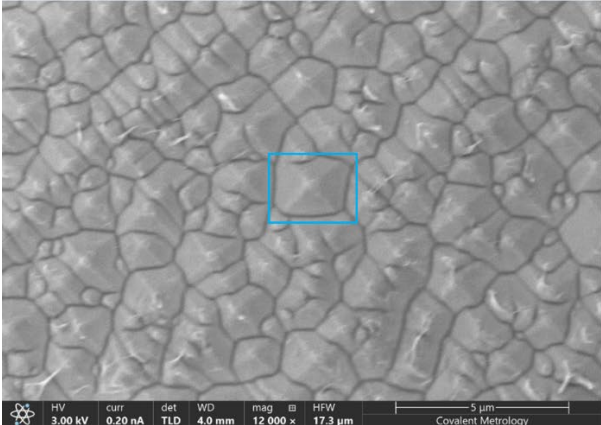
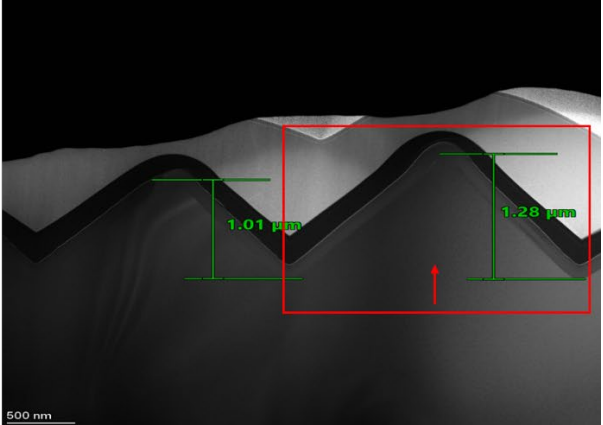
'136 Patent Claim Limitation	SEG-420-BTD-BG
1[e] and wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm;	The SEG-420-BTD-BG includes a front surface of the semiconductor substrate having a second texture structure, where the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm. By way of example, the SEM image on the left below displays the front side of the SEG-420-BTD-BG – indicating that it includes the front surface of the semiconductor substrate having a second textual structure including a plurality of pyramid-shaped microstructures. The TEM image on the right below shows an example pyramid-shaped microstructure (in the red box) corresponding to the pyramid-shaped microstructure in the blue box in the SEM image on the left below. The example pyramid-shaped microstructure has a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, where a distance between the top portion and the bottom portion of the pyramid-shaped microstructure in a direction (denoted by the red arrow) away from the front surface and perpendicular to the front surface is 1.28 μm (indicated by green lines), which is less than 5 μm and thus satisfies this claim limitation.  

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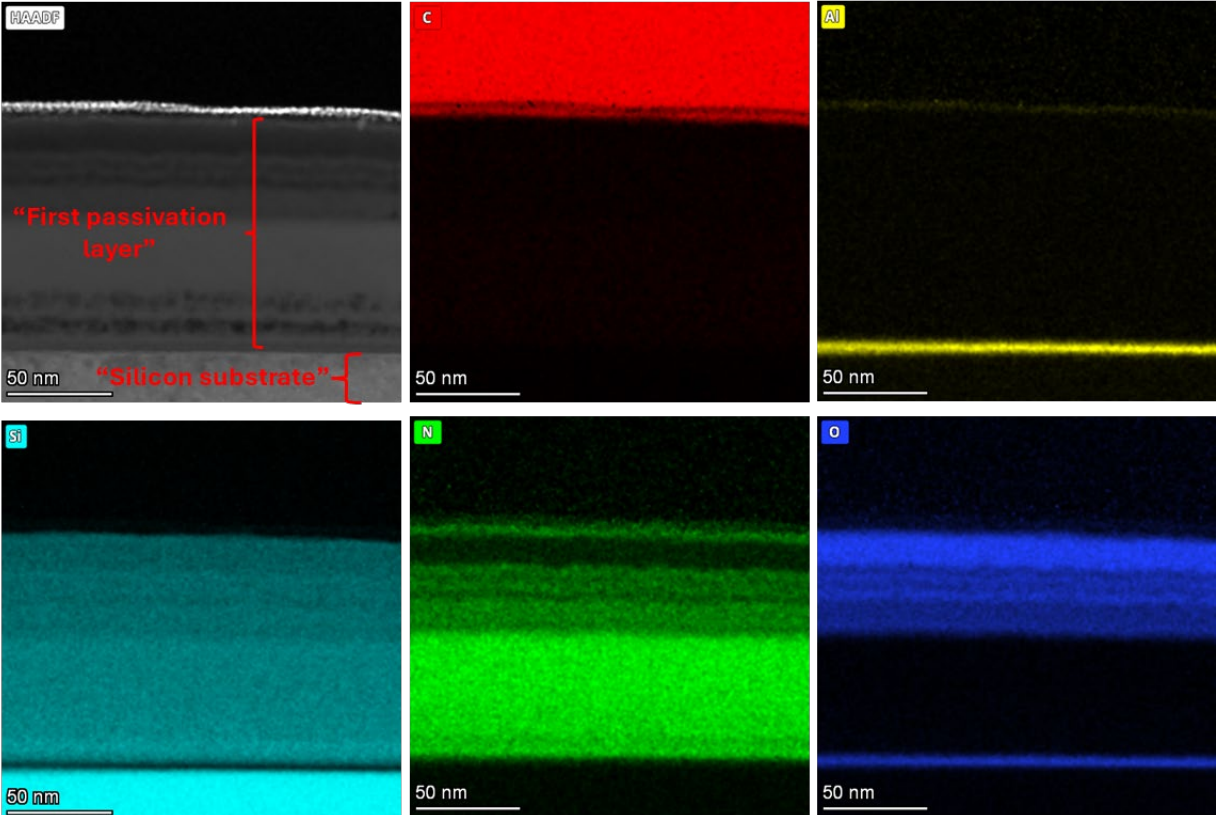
'136 Patent Claim Limitation	SEG-420-BTD-BG
1[f] a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate;	The SEG-420-BTD-BG includes a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate. The HAADF image of the front side of the SEG-420-BTD-BG and an element analysis of EDS maps confirm that the SEG-420-BTD-BG includes a first passivation layer located on the front surface of the semiconductor substrate. As discussed in limitation 1[e], the front surface of the semiconductor substrate has the second texture structure. Front side 

EXHIBIT 2–Infringement Chart for U.S. Patent No. 11,824,136 (the “’136 Patent”)

'136 Patent Claim Limitation	SEG-420-BTD-BG
1[g] a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;	The SEG-420-BTD-BG includes a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate. As shown in the HAADF image in limitation 1[a] and as described in limitations 1[a] and 1[b], the SEG-420-BTD-BG includes a tunnel oxide layer located on the rear surface of the semiconductor substrate having the first texture structure. Rear side The figure consists of six panels. The top-left panel is a HAADF cross-section image of the rear side of the device. It shows several layers with the following labels and thicknesses: 'Second passivation layer' (67.6 nm), 'Doped conductive layer' (97.0 nm), 'Tunnel oxide layer' (1.3 nm), and 'Silicon substrate'. A 20 nm scale bar is present at the bottom left. The other five panels are elemental maps for Nitrogen (N), Aluminum (Al), Phosphorus (P), Oxygen (O), and Silicon (Si), each with a 50 nm scale bar at the bottom left.

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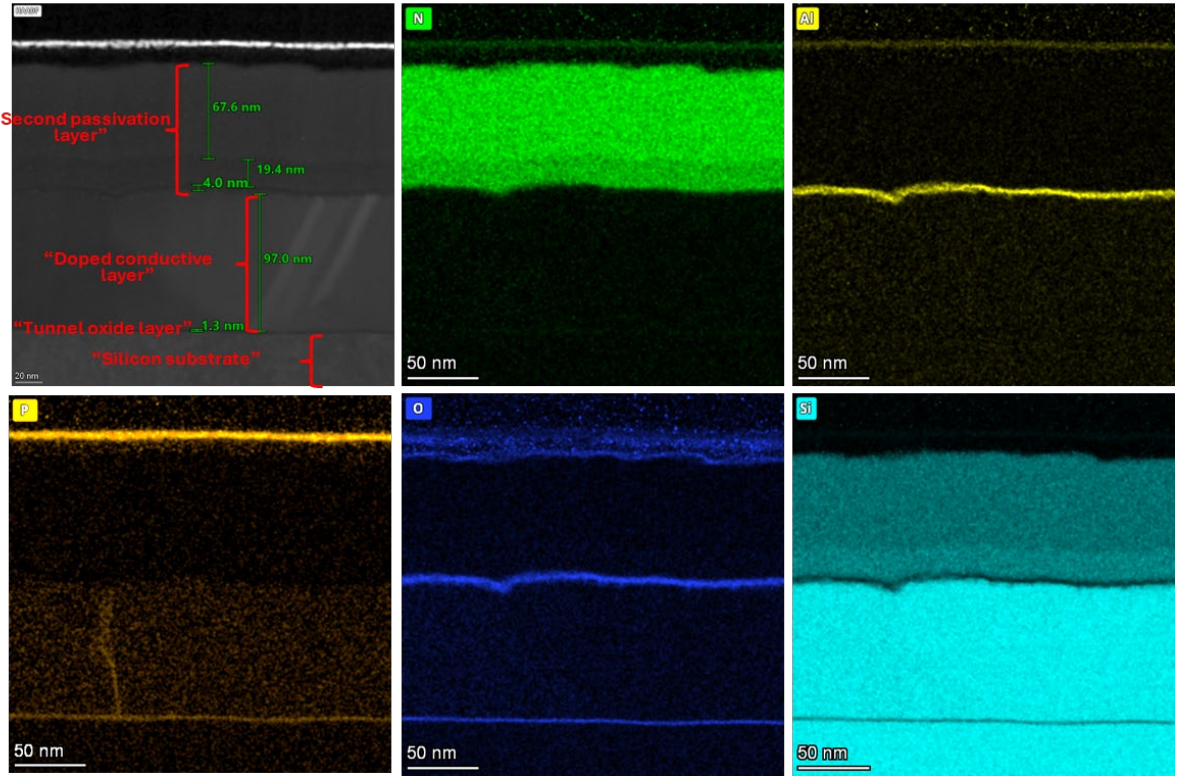
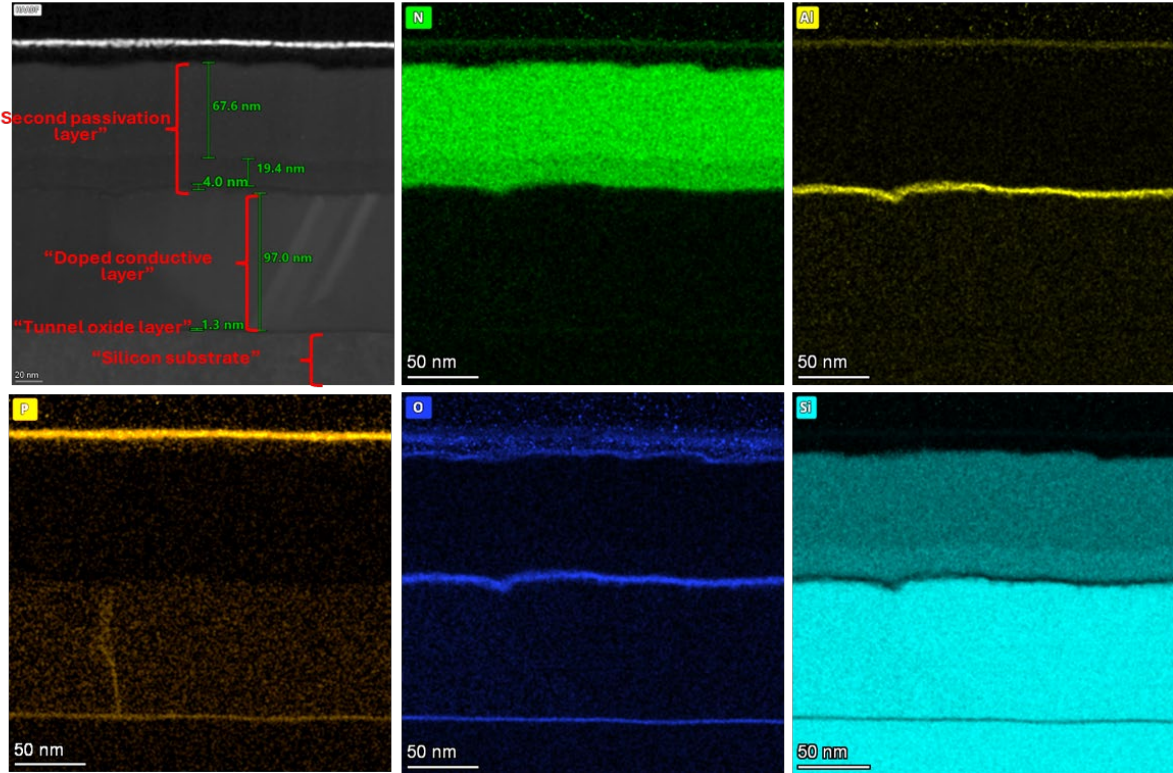
'136 Patent Claim Limitation	SEG-420-BTD-BG
1[h] a doped conductive layer located on a surface of the tunnel oxide layer; and	The SEG-420-BTD-BG includes a doped conductive layer located on a surface of the tunnel oxide layer. As shown in limitation 1[a], the SEG-420-BTD-BG includes a doped conductive layer located on a surface of the tunnel oxide layer. Rear side  Because the doped conductive layer is made of silicon and doped with P (shown in the element analysis in limitation 1[a] as reproduced below), the doped conductive layer of the SEG-420-BTD-BG is an N-type doped silicon layer.

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'136 Patent Claim Limitation	SEG-420-BTD-BG
1[i] a second passivation layer located on a surface of the doped conductive layer.	The SEG-420-BTD-BG provides a second passivation layer located on a surface of the doped conductive layer. As shown in limitation 1[a], the SEG-420-BTD-BG includes a second passivation layer located on a surface of the doped conductive layer. Rear side  The figure displays a cross-sectional SEM image and five corresponding elemental maps (N, S, P, O, Si) for the rear side of the SEG-420-BTD-BG. The SEM image shows the following layers and their thicknesses: "Second passivation layer" (67.6 nm), "Doped conductive layer" (97.0 nm), "Tunnel oxide layer" (1.3 nm), and "Silicon substrate". The elemental maps show the distribution of Nitrogen (N), Sulfur (S), Phosphorus (P), Oxygen (O), and Silicon (Si) across the device structure. Each map includes a 50 nm scale bar.