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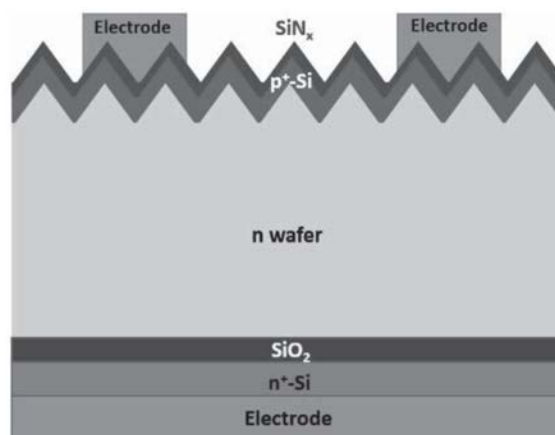
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(54) 发明名称

管式PECVD制备多晶硅钝化接触结构的方法

(57) 摘要

本发明公开了一种管式PECVD制备多晶硅钝化接触结构的方法,包括在硅的氧化物和/或硅的氮化物表面采用管式PECVD制备掺杂非晶硅薄膜,然后高温晶化退火得到多晶硅钝化接触结构;本发明不仅可以制备出高质量TOPCon结构,其钝化效率完全等同于LPCVD技术,具体体现在,采用n型TOPCon双面钝化的n型硅片的 iV_{oc} 可以达到720-750mV;同时还可以极大地简化生产流程。



1. 一种管式PECVD制备多晶硅钝化接触结构的方法,其特征在于,包括在硅的氧化物和/或硅的氮化物表面采用管式PECVD制备掺杂非晶硅薄膜,然后高温晶化退火得到多晶硅钝化接触结构;

包括以下具体步骤,采用管式PECVD设备按照以下步骤制备:

1) 硅片清洗后放入石墨舟;

2) 沉积氧化硅:衬底温度100-600°C,以笑气或二氧化碳或氧气为反应气体,流量1000sccm-5000sccm,气压为30-300Pa,沉积功率2000-8000W,射频通断比1:5-1:30,沉积时间为10-1000秒;

3) 在背面氧化硅上沉积I层掺磷非晶硅薄膜:为了降低界面轰击,I层掺磷非晶硅薄膜沉积功率较小,速率较低,厚度也较小;具体参数为:衬底温度100-700°C,以硅烷、氢气、磷烷为反应气体,每种气体的流量为1000sccm-5000sccm,三者的流量比 $\text{SiH}_4:\text{H}_2:\text{PH}_3=1:0-100:0.1-100$,气压为60-300Pa,沉积功率2000-8000W,射频通断比1:5-1:30,沉积时间为60-600秒;

4) 在I层掺磷非晶硅薄膜上沉积II层掺磷非晶硅薄膜:为了提高薄膜生长速率,II层掺磷非晶硅薄膜沉积功率增大;具体参数为:衬底温度100-700°C,以硅烷、氢气、磷烷为反应气体,三者的流量比 $\text{SiH}_4:\text{H}_2:\text{PH}_3=1:0-100:0.1-100$,气压为30-200Pa,沉积功率5000-15000W,射频通断比1:5-1:30,沉积时间为120-1200秒;

5) 晶化退火:将硅片放入管式退火炉,退火温度为760-1100°C,退火时间为10-240分钟。

2. 根据权利要求1所述的管式PECVD制备多晶硅钝化接触结构的方法,其特征在于,所述掺杂非晶硅薄膜的厚度为20-400nm。

3. 根据权利要求2所述的管式PECVD制备多晶硅钝化接触结构的方法,其特征在于,所述掺杂非晶硅薄膜的厚度为100-150nm。

4. 根据权利要求1所述的管式PECVD制备多晶硅钝化接触结构的方法,其特征在于,所述掺杂非晶硅薄膜为磷掺杂的非晶硅薄膜或硼掺杂的非晶硅薄膜。

管式PECVD制备多晶硅钝化接触结构的方法

技术领域

[0001] 本发明涉及太阳能电池技术领域,具体讲是一种管式PECVD制备多晶硅钝化接触(TOPCon)结构的方法。

背景技术

[0002] 隧穿氧/多晶硅钝化接触(TOPCon)太阳电池是2013年来由德国弗兰霍夫研究所提出的一种新型硅太阳电池。在电池片的背面上覆盖一层厚度在2nm以下的超薄氧化硅层,再覆盖一层掺杂的非晶硅层,然后经过高温退火形成重掺杂多晶硅。以n型磷掺杂TOPCon为例,电池的基本结构如图1所示,典型钝化片结构则如图2所示。电池的背面结构依次为n型硅片/超薄隧穿氧化层/n+多晶硅层/金属电极层。根据电池结构设计的不同,多晶硅也可以是硼掺杂的多晶硅。

[0003] 目前,采用TOPCon技术,背面钝化有了显著提高,n型TOPCon电池的效率比n-PERT电池效率有所提高。现有n-PERT电池的单面发电效率约为21.5%-22%,而双面n-TOPCon电池的单面发电效率约为22.5%-23.5%。

[0004] 产业上主要基于LPCVD技术制备TOPCon结构。以n型TOPCon电池为例,制备流程为:

[0005] 1) 硅片清洗,双面制绒;

[0006] 2) 正面扩硼;

[0007] 3) 背面化学抛光;

[0008] 4) 正面长氮化硅;

[0009] 5) 采用热氧化法在硅片背表面制备厚度低于3nm的氧化硅;时间通常需要30分钟;

[0010] 6) 采用低压化学气相沉积法(LPCVD)制备一层本征的多晶硅薄膜;制备100-150nm的多晶硅通常需要120-150分钟;

[0011] 7) 采用低压磷扩散法使本征多晶硅薄膜变成掺磷的多晶硅薄膜;扩散过程通常需要90-120分钟;

[0012] 8) 正面清洗,去除氮化硅;通常需要20分钟;

[0013] 9) 背面清洗去除磷硅玻璃层;

[0014] 10) 制备正面钝化减反膜及背面减反膜;

[0015] 11) 丝网印刷;

[0016] 12) 烧结;

[0017] 13) 测试分档。

[0018] 其中,步骤4-9,共六道步骤是制备磷掺杂TOPCon结构所必须的步骤。

[0019] 现有LPCVD法制备TOPCon结构的主要不足包括:

[0020] 1) 工艺步骤长:制备氧化硅/掺磷多晶硅需要六道工艺步骤,制作流程仍然比较复杂繁琐,需要增加额外的扩散工艺、清洗工艺,提高了生产复杂度,降低了电池成品率。

[0021] 2) 所需增加的专用设备一共是3种,具体包括:LPCVD炉、扩散炉、正面专用清洗机。同时,相关设备价格较高,增加了生产成本。

[0022] 3) 工艺时间长:制备氧化硅、本征多晶硅、磷扩散等步骤的总时间在280分钟以上,时间非常长,大大降低了电池产率。

发明内容

[0023] 针对上述问题,本发明开发一种基于管式PECVD的TOPCon结构制备技术。管式PECVD所用电源既可以是低频电源也可以是射频电源,管式PECVD技术不仅可以制备出高质量TOPCon结构,其钝化效率完全等同于LPCVD技术,具体体现在,采用n型TOPCon双面钝化的n型硅片的 iV_{oc} 可以达到720-750mV;同时还可以极大地简化生产流程。

[0024] 本发明提供一种管式PECVD制备多晶硅钝化接触结构的方法,包括在硅的氧化物和/或硅的氮化物表面采用管式PECVD制备掺杂非晶硅薄膜,然后高温晶化退火得到多晶硅钝化接触结构。硅的氧化物和/或硅的氮化物包括氧化硅层(SiO_x)、氮化硅层(SiN_x)、氮氧化硅层(SiO_xNy)及其不同叠层的组合。

[0025] 较佳地,所述掺杂非晶硅薄膜的厚度为20-400nm。

[0026] 更佳地,所述掺杂非晶硅薄膜的厚度为100-150nm。

[0027] 较佳地,所述掺杂非晶硅薄膜为磷掺杂的非晶硅薄膜或硼掺杂的非晶硅薄膜。

[0028] 作为优选,所述的管式PECVD制备多晶硅钝化接触结构的方法,包括以下具体步骤:

[0029] 1) 硅片清洗,双面制绒;

[0030] 2) 硅片正面扩硼;

[0031] 3) 硅片背面化学抛光;

[0032] 4) 在硅片背表面制备厚度低于3nm的氧化硅;

[0033] 5) 采用管式PECVD在氧化硅上制备20-400nm厚度的磷掺杂的非晶硅薄膜;

[0034] 6) 硅片正面清洗;

[0035] 7) 高温晶化退火;

[0036] 8) 制备正面钝化减反膜及背面减反膜;

[0037] 9) 丝网印刷;

[0038] 10) 烧结。

[0039] 作为最优选,采用管式PECVD设备按照以下步骤制备:

[0040] 1) 硅片清洗后放入石墨舟;

[0041] 2) 沉积氧化硅:衬底温度100-600°C,以笑气或二氧化碳或氧气为反应气体,流量1000sccm-5000sccm,气压为30-300Pa,沉积功率2000-8000W,射频通断比1:5-1:30,沉积时间为10-1000秒;

[0042] 3) 在背面氧化硅上沉积I层掺磷非晶硅薄膜:为了降低界面轰击,I层薄膜沉积功率较小,速率较低,厚度也较小;具体参数为:衬底温度100-700°C,以硅烷、氢气、磷烷为反应气体,每种气体的流量约为1000sccm-5000sccm,三者的流量比 $SiH_4:H_2:PH_3=1:0-100:0.1-100$,气压为60-300Pa,沉积功率2000-8000W,射频通断比1:5-1:30,沉积时间为60-600秒;

[0043] 4) 在I层掺磷非晶硅薄膜上沉积II层掺磷非晶硅薄膜:为了提高薄膜生长速率,II层薄膜沉积功率增大;具体参数为:衬底温度100-700°C,以硅烷、氢气、磷烷为反应气体,三

者的流量比 $\text{SiH}_4:\text{H}_2:\text{PH}_3=1:0-100:0.1-100$,气压为30-200Pa,沉积功率5000-15000W,射频通断比1:5-1:30,沉积时间为120-1200秒;

[0044] 5) 晶化退火:将硅片放入管式退火炉,退火温度为760-1100°C,退火时间为10-240分钟。

[0045] 本发明的有益效果是:归纳来说,采用管式PECVD具有如下优点:

[0046] 1) TOPCon的核心工艺步骤减少为四步,一共少了三步,大大减少了工艺数量,降低工艺复杂度。

[0047] 2) 所需增加的专用设备仅为两种:管式PECVD、高温退火炉。同时,设备价格较低,节约了成本。

[0048] 3) 显著缩短了工艺时间。一、管式PECVD绕镀小,因而不需要在硅片正面制备氮化硅掩膜层,同时也避免了后继繁琐的正面清洗刻蚀工作。二、管式PECVD可以在管内同时制备氧化硅和掺杂非晶硅薄膜。可以在PECVD管内直接制备氧化硅,无需采用其他方法制备氧化硅后并转移到炉子,减少了传送过程。三、管式PECVD制备非晶硅薄膜的速率很快,制备100nm的非晶硅薄膜,总时间通常在10分钟以内。四、非晶硅薄膜是原位掺杂的,无需再做扩散工艺。如果加上后继的晶化处理,采用管式PECVD法制备TOPCon结构所需的总时间在90-120分钟左右,显著低于LPCVD法所需的280分钟。

[0049] 4) 由于节省了工艺步骤,也大大降低了硅片的破碎率,提高了生产过程的良率。

[0050] 5) 另外,根据工艺需要,还可以额外通入甲烷(CH_4)制备掺杂碳化硅,通入氨气(CH_3)制备掺杂氮化硅、通入二氧化碳(CO_2)或笑气(N_2O)制备掺杂氧化硅。

附图说明

[0051] 图1为现有TOPCon结构太阳能电池结构示意图。

[0052] 图2为现有典型钝化片结构示意图。

具体实施方式

[0053] 下面用具体实施例对本发明做进一步详细说明,但本发明不仅局限于以下具体实施例。

[0054] 实施例中用到的n型硅片信息:(100)晶向,厚度为180微米,电阻率为1-7欧姆厘米。p型硅片信息:(100)晶向,厚度为180微米,电阻率为0.5-1.5欧姆厘米。下面为具体实施例。

[0055] 实施例1

[0056] 采用所述n型硅片,去表面损伤层,两面镀上同样的结构。具体处理如下:

[0057] 1. 硅片清洗后放入石墨舟;

[0058] 2. 沉积氧化硅:衬底温度400°C,以笑气(N_2O)为反应气体,流量3000sccm,气压为200Pa,沉积功率2000W,射频通断比2ms:10ms,沉积时间为120秒;

[0059] 3. 在氧化硅层上沉积I层掺磷非晶硅薄膜:衬底温度600°C, $\text{SiH}_4:\text{H}_2:\text{PH}_3=1500\text{sccm}:10000\text{sccm}:1500\text{sccm}$,气压为250Pa,沉积功率2000W,射频通断比3ms:45ms,沉积时间为600秒;

[0060] 4. 在I层掺磷非晶硅薄膜上沉积II层掺磷非晶硅薄膜:衬底温度600°C, $\text{SiH}_4:\text{H}_2:$

PH₃=1500sccm:10000sccm:1500sccm,气压为150Pa,沉积功率8000W,射频通断比3ms:45ms,沉积时间为180秒;

[0061] 5. 晶化退火:800°C退火时间约为40分钟。

[0062] 最后采用Sinton WCT-120测试样品的表面钝化效果。样品的平均隐含开路电压 $iV_{oc} \approx 725$ mV, iV_{oc} 分布为716~734 mV,对应的平均表面饱和电流 $J_0 \approx 8$ fA/cm²。

[0063] 实施例2

[0064] 采用所述n型硅片,去表面损伤层,两面镀上同样的结构。具体处理如下:

[0065] 1. 硅片清洗后放入石墨舟;

[0066] 2. 沉积氧化硅:衬底温度400°C,以二氧化碳(CO₂)为反应气体,流量5000sccm,气压为220Pa,沉积功率2500W,射频通断比2ms:30ms,沉积时间为120秒;

[0067] 3. 沉积I层掺磷非晶硅薄膜:衬底温度500°C, SiH₄:H₂:PH₃=1000sccm:10000sccm:1000sccm,气压为250Pa,沉积功率2000W,射频通断比3ms:75ms,沉积时间为500秒;

[0068] 4. 沉积II层掺磷非晶硅薄膜:衬底温度500°C, SiH₄:H₂:PH₃=1000sccm:10000sccm:1000sccm,气压为200Pa,沉积功率10000W,射频通断比3ms:75ms,沉积时间为200秒;

[0069] 5. 晶化退火:800°C退火时间约为40分钟。

[0070] 最后采用Sinton WCT-120测试样品的表面钝化效果。样品的平均隐含开路电压 $iV_{oc} \approx 723$ mV, iV_{oc} 分布为714~733 mV,对应的表面饱和电流 $J_0 \approx 8$ fA/cm²。

[0071] 实施例3

[0072] 采用所述n型硅片,去表面损伤层,两面镀上同样的结构。具体处理如下:

[0073] 1. 硅片清洗后放入石墨舟;

[0074] 2. 沉积氧化硅:衬底温度400°C,以笑气(N₂O)为反应气体,流量3000sccm,气压为200Pa,沉积功率2000W,射频通断比2ms:10ms,沉积时间为120秒;

[0075] 3. 沉积I层掺硼非晶硅薄膜:衬底温度600°C, SiH₄:H₂:B₂H₆=1500sccm:2000sccm:1500sccm,气压为250Pa,沉积功率1800W,射频通断比3ms:45ms,沉积时间为600秒;

[0076] 4. 沉积II层掺硼非晶硅薄膜:衬底温度600°C, SiH₄:H₂:B₂H₆=1600sccm:10000sccm:1600sccm,气压为150Pa,沉积功率10000W,射频通断比3ms:45ms,沉积时间为300秒;

[0077] 5. 晶化退火:780°C退火时间约为120分钟。

[0078] 最后采用Sinton WCT-120测试样品的表面钝化效果。样品的平均隐含开路电压 $iV_{oc} \approx 672$ mV, iV_{oc} 分布为668~679 mV,对应的表面饱和电流 $J_0 \approx 78$ fA/cm²。

[0079] 实施例4

[0080] 采用1欧姆厘米的p型硅片,去表面损伤层,两面镀上同样的结构。具体处理如下:

[0081] 1. 硅片清洗后放入石墨舟;

[0082] 2. 沉积氧化硅:衬底温度400°C,以笑气(N₂O)为反应气体,流量2000sccm,气压为240Pa,沉积功率2500W,射频通断比2ms:20ms,沉积时间为100秒;

[0083] 3. 沉积I层掺磷非晶硅薄膜:衬底温度600°C, SiH₄:H₂:PH₃=1500sccm:10000sccm:1500sccm,气压为250Pa,沉积功率2000W,射频通断比3ms:60ms,沉积时间为600秒;

[0084] 4. 沉积II层掺磷非晶硅薄膜:衬底温度600°C, SiH₄:H₂:PH₃=1500sccm:

10000sccm:1500sccm,气压为150Pa,沉积功率13000W,射频通断比3ms:60ms,沉积时间为240秒;

[0085] 5. 晶化退火:900°C退火时间约为30分钟。

[0086] 最后采用Sinton WCT-120测试样品的表面钝化效果。样品的平均隐含开路电压 $iV_{oc} \approx 716$ mV, iV_{oc} 分布为710~723 mV,对应的表面饱和电流 $J_0 \approx 11$ fA/cm²。

[0087] 实施例5

[0088] 采用n型硅片,TOPCon结构的制备具体如下所述:

[0089] 1. 硅片清洗后放入石墨舟;

[0090] 2. 沉积氧化硅:衬底温度400°C,以笑气(N₂O)为反应气体,流量3500sccm,气压为200Pa,沉积功率2000W,射频通断比2ms:15ms,沉积时间为200秒;

[0091] 3. 沉积I层掺磷非晶硅薄膜:衬底温度600°C, SiH₄:H₂:PH₃=1500sccm:8000sccm:1500sccm,气压为220Pa,沉积功率2000W,射频通断比3ms:55ms,沉积时间为600秒;

[0092] 4. 沉积II层掺磷非晶硅薄膜:衬底温度600°C, SiH₄:H₂:PH₃=1500sccm:8000sccm:1500sccm,气压为180Pa,沉积功率11000W,射频通断比3ms:55ms,沉积时间为300秒;

[0093] 5. 晶化退火:850°C退火时间约为30分钟。

[0094] 6. 最后制备成n型TOPCon电池效率为22.7%。

[0095] 实施例6

[0096] 采用n型硅片,TOPCon结构的制备具体如下所述:

[0097] 1. 硅片清洗后放入石墨舟;

[0098] 2. 制备氧化硅:采用热氧化法(600°C/20min)制备氧化硅;

[0099] 3. 沉积I层掺磷非晶硅薄膜:衬底温度400°C, SiH₄:H₂:PH₃=1500sccm:8000sccm:1500sccm,气压为220Pa,沉积功率2000W,射频通断比3ms:55ms,沉积时间为600秒;

[0100] 4. 沉积II层掺磷非晶硅薄膜:衬底温度400°C, SiH₄:H₂:PH₃=1500sccm:8000sccm:1500sccm,气压为180Pa,沉积功率11000W,射频通断比3ms:55ms,沉积时间为1000秒;

[0101] 5. 晶化退火:880°C退火时间约为30分钟。

[0102] 最后采用Sinton WCT-120测试样品的表面钝化效果。样品的平均隐含开路电压 $iV_{oc} \approx 733$ mV, iV_{oc} 分布为720~733 mV,对应的表面饱和电流 $J_0 \approx 4$ fA/cm²。

[0103] 以上仅是本发明的特征实施范例,对本发明保护范围不构成任何限制。凡采用同等交换或者等效替换而形成的技术方案,均落在本发明权利保护范围之内。

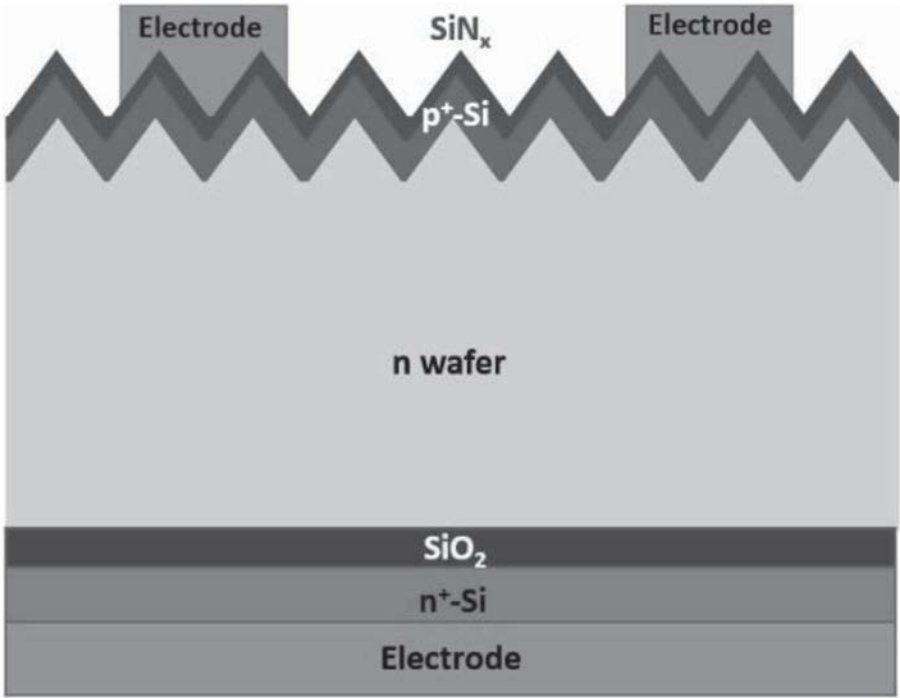


图1

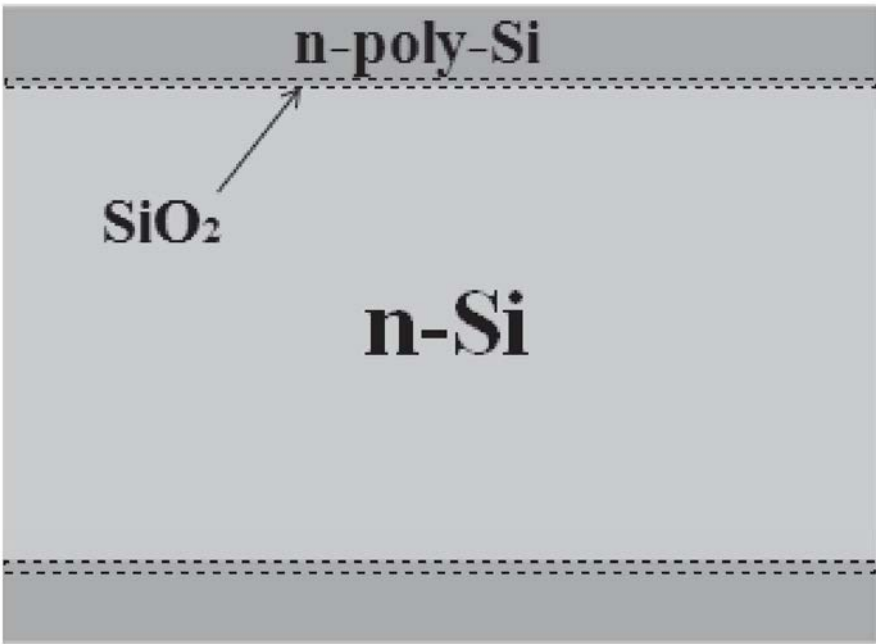


图2



(12) Invention Patent

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H 0 1 L 31/18 (January 2006)

Claims (1 page) Description (5 pages) Drawings (1 page)

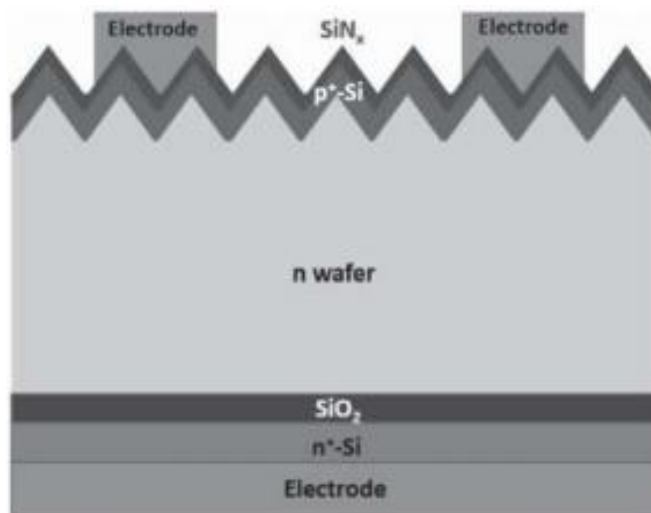
(54) Title of Invention

Method for preparing polycrystalline silicon passivated
contact structures by tubular PECVD

(57) Abstract

This invention discloses a method for preparing polycrystalline silicon passivated contact structures using tubular PECVD. The method includes preparing a doped amorphous silicon thin film on the surface of silicon oxide and/or silicon nitride using tubular PECVD, followed by high-temperature crystallization annealing to obtain the polycrystalline silicon passivated contact structure. This invention not only produces high-quality TOPCon structures with passivation efficiency completely equivalent to LPCVD technology—specifically, the iV_{OC} of n-type silicon wafers with double-sided passivation using n-type TOPCon can reach 720-750 mV—but also significantly simplifies the production process.

CN109802007B



1. A method for preparing polycrystalline silicon passivated contact structures by tubular PECVD, characterized in that it includes preparing a doped amorphous silicon thin film on the surface of silicon oxide and/or silicon nitride by tubular PECVD, and then obtaining the polycrystalline silicon passivated contact structure by high-temperature crystallization annealing.

The following specific steps are included in the preparation using a tubular PECVD device:

- 1) After cleaning, the silicon wafers are placed in a graphite boat;
- 2) Deposition of silicon oxide: substrate temperature 100-600°C, nitrous oxide, carbon dioxide or oxygen as reaction gas, flow rate 1000sccm-5000sccm, gas pressure 30-300Pa, deposition power 2000-8000W, RF on/off ratio 1:5-1:30, deposition time 10-1000 seconds.
- 3) Depositing a phosphorus-doped amorphous silicon film (I-layer) on the back silicon oxide: To reduce interface bombardment, the deposition power, deposition rate, and thickness of the phosphorus-doped amorphous silicon film (I-layer) are relatively low. Specific parameters are as follows: substrate temperature 100-700°C, silane, hydrogen, and phosphine as reactant gases, with a flow rate of 1000 sccm-5000 sccm for each gas, a flow rate ratio of $\text{SiH}_4:\text{H}_2:\text{PH}_3 = 1:0-100:0.1-100$, gas pressure 60-300 Pa, deposition power 2000-8000 W, RF on/off ratio 1:5-1:30, and deposition time 60-600 seconds.
- 4) Depositing a phosphorus-doped amorphous silicon film II on the phosphorus-doped amorphous silicon film I: In order to improve the film growth rate, the deposition power of the phosphorus-doped amorphous silicon film II is increased; the specific parameters are: substrate temperature 100-700°C, silane, hydrogen and phosphine as reaction gases, the flow ratio of the three $\text{SiH}_4:\text{H}_2:\text{PH}_3=1:0-100:0.1-100$, gas pressure 30-200Pa, deposition power 5000-15000W, RF on/off ratio 1:5-1:30, and deposition time 120-1200 seconds;
- 5) Crystallization annealing: Place the silicon wafer into a tube annealing furnace, anneal at a temperature of 760-1100°C, and anneal for 10-240 minutes.

2. The method for preparing polycrystalline silicon passivated contact structures by tubular PECVD according to claim 1, wherein the thickness of the doped amorphous silicon thin film is 20-400 nm.

3. The method for preparing polycrystalline silicon passivated contact structures by tubular PECVD according to claim 2, wherein the thickness of the doped amorphous silicon thin film is 100-150 nm.

4. The method for preparing polycrystalline silicon passivated contact structures by tubular PECVD according to claim 1, wherein the doped amorphous silicon thin film is a phosphorus-doped amorphous silicon thin film or a boron-doped amorphous silicon thin film.

Method for preparing polycrystalline silicon passivated contact structures by tubular PECVD

Technical Field

[0001] This invention relates to the field of solar cell technology, specifically to a method for preparing polycrystalline silicon passivated contact (TOPCon) structures using tubular PECVD.

Background Art

[0002] Tunneling oxygen/polycrystalline silicon passivated contact (TOPCon) solar cells are a novel type of silicon solar cell proposed by the Fraunhofer Institute in Germany in 2013. A thin layer of ultrathin silicon oxide (less than 2 nm thick) is coated on the back of the cell, followed by a layer of doped amorphous silicon, and then annealed at high temperature to form heavily doped polycrystalline silicon. Taking n-type phosphorus-doped TOPCon as an Embodiment, the basic structure of the cell is shown in Figure 1, and the typical passivation sheet structure is shown in Figure 2. The back structure of the cell is, in sequence, an n-type silicon wafer/ultrathin tunneling oxide layer/n⁺ polycrystalline silicon layer/metal electrode layer. Depending on the cell structure design, the polycrystalline silicon can also be boron-doped polycrystalline silicon.

[0003] Currently, with the adoption of TOPCon technology, back-side passivation has been significantly improved, and the efficiency of n-type TOPCon cells is higher than that of n-PERT cells. The single-sided power generation efficiency of existing n-PERT cells is about 21.5%-22%, while the single-sided power generation efficiency of bifacial n-TOPCon cells is about 22.5%-23.5%.

[0004] Industrially, TOPCon structures are mainly fabricated using LPCVD technology. Taking an n-type TOPCon battery as an Embodiment, the fabrication process is as follows:

[0005]1) Silicon wafer cleaning and double-sided texturing;

[0006]2) Front side boron expansion;

[0007]3) Back side chemical polishing;

[0008]4) Long silicon nitride on the front side;

[0009]5) Silicon oxide with a thickness of less than 3 nm is prepared on the back surface of the silicon wafer by thermal oxidation; the time usually takes 30 minutes;

[0010]6) An intrinsic polycrystalline silicon thin film is prepared by low-pressure chemical vapor deposition (LPCVD); it usually takes 120-150 minutes to prepare 100-150 nm polycrystalline silicon.

[0011]7) The intrinsic polycrystalline silicon film is transformed into a phosphorus-doped polycrystalline silicon film by low-pressure phosphorus diffusion method; the diffusion process usually takes 90-120 minutes.

[0012]8) Front side cleaning to remove silicon nitride; usually takes 20 minutes;

[0013]9) Clean the back side to remove the phosphosilicate glass layer;

[0014]10) Prepare a front passivation antireflection film and a back antireflection film;

[0015] 11) Screen printing;

[0016]12) Sintering;

[0017]13) Test grading.

[0018] Steps 4-9, a total of six steps, are necessary steps for preparing the phosphorus-doped TOPCon structure.

[0019] The main shortcomings of existing LPCVD methods for preparing TOPCon structures include:

[0020]1) Long process steps: The preparation of silicon oxide/phosphorus-doped polycrystalline silicon requires six process steps. The manufacturing process is still relatively complex and cumbersome. Additional diffusion and cleaning processes are required, which increases the production complexity and reduces the yield of battery products.

[0021]2) A total of three types of special equipment are required, including: LPCVD furnace, diffusion furnace, and front-side special cleaning machine. At the same time, the prices of the relevant equipment are high, which increases the production cost.

[0022]3) Long process time: The total time for steps such as preparing silicon oxide, intrinsic polycrystalline silicon, and phosphorus diffusion is more than 280 minutes, which is very long and greatly reduces the battery yield.

Summary of the Invention

[0023] To address the above problems, this invention develops a TOPCon structure fabrication technology based on tubular PECVD. The power supply used for tubular PECVD can be either a low-frequency power supply or a radio frequency power supply. Tubular PECVD technology can not only fabricate high-quality TOPCon structures, but its passivation efficiency is completely equivalent to that of LPCVD technology. Specifically, the iV_{oc} of n-type silicon wafers with double-sided passivation using n-type TOPCon can reach 720-750mV; at the same time, it can also greatly simplify the production process.

[0024] This invention provides a method for preparing polycrystalline silicon passivated contact structures using tubular PECVD, comprising preparing a doped amorphous silicon thin film on the surface of silicon oxide and/or silicon nitride using tubular PECVD, followed by high-temperature crystallization annealing to obtain the polycrystalline silicon passivated contact structure. The silicon oxide and/or silicon nitride include silicon oxide layers (SiO_x), silicon nitride layers (SiN_x), silicon oxynitride layers (SiO_xN_y), and combinations of different stacks thereof.

[0025] Preferably, the thickness of the doped amorphous silicon thin film is 20-400 nm.

[0026] More preferably, the thickness of the doped amorphous silicon thin film is 100-150 nm.

[0027] Preferably, the doped amorphous silicon film is a phosphorus-doped amorphous silicon film or a boron-doped amorphous silicon film.

[0028] Preferably, the method for preparing polycrystalline silicon passivated contact structures by tubular PECVD includes the following specific steps:

[0029]1) Silicon wafer cleaning and double-sided texturing;

[0030]2) Boron expansion on the front side of the silicon wafer;

[0031]3) Chemical polishing of the back side of the silicon wafer;

[0032]4) Prepare silicon oxide with a thickness of less than 3 nm on the back surface of the silicon wafer;

[0033]5) Phosphorus-doped amorphous silicon films with a thickness of 20-400 nm were prepared on silicon oxide using tubular PECVD;

[0034]6) Cleaning the front side of the silicon wafer;

[0035]7) High-temperature crystallization annealing;

[0036]8) Prepare a front passivation antireflection film and a back antireflection film;

[0037]9) Screen printing;

[0038]10) Sintering.

[0039] As the most preferred method, the preparation is carried out using a tubular PECVD equipment according to the following steps:

[0040]1) After cleaning, the silicon wafer is placed in a graphite boat;

[0041]2) Deposition of silicon oxide: substrate temperature 100-600°C, nitrous oxide, carbon dioxide or oxygen as reaction gas, flow rate 1000sccm-5000sccm, gas pressure 30-300Pa, deposition power 2000-8000W, RF on/off ratio 1:5-1:30, deposition time 10-1000 seconds;

[0042]3) Deposit a phosphorus-doped amorphous silicon thin film on the back silicon oxide: In order to reduce interface bombardment, the deposition power of the thin film is small, the rate is low, and the thickness is also small; the specific parameters are: substrate temperature 100-700°C, silane, hydrogen and phosphine are used as reaction gases, the flow rate of each gas is about 1000sccm-5000sccm, the flow rate ratio of the three is SiH₄:H₂:PH₃=1:0-100:0.1-100, the gas pressure is 60-300Pa, the deposition power is 2000-8000W, the RF on/off ratio is 1:5-1:30, and the deposition time is 60-600 seconds;

[0043]4) Deposit a phosphorus-doped amorphous silicon film on the phosphorus-doped amorphous silicon film: In order to improve the film growth rate, the deposition power of the second layer film is increased; the specific parameters are: substrate temperature 100-700°C, silane, hydrogen and phosphine as reaction gases, the flow ratio of the three SiH₄:H₂:PH₃=1:0-100:0.1-100, gas pressure 30-200Pa, deposition power 5000-15000W, RF on/off ratio 1:5-1:30, deposition time 120-1200 seconds;

[0044]5) Crystallization annealing: The silicon wafer is placed in a tube annealing furnace, the annealing temperature is 760-1100°C, and the annealing time is 10-240 minutes.

[0045] The beneficial effects of the present invention are as follows: In summary, using tubular PECVD has the following advantages:

[0046]1) The core process steps of TOPCon are reduced to four steps, a total of three steps are reduced, which greatly reduces the number of processes and reduces the complexity of the process.

[0047]2) Only two types of special equipment are required: tubular PECVD and high-temperature annealing furnace. At the same time, the equipment is inexpensive, saving costs.

[0048] 3) Significantly shortened process time. First, tubular PECVD has a small wafer diameter, thus eliminating the need to prepare a silicon nitride mask layer on the front side of the silicon wafer, and also avoiding the subsequent tedious front-side cleaning and etching work. Second, tubular PECVD can simultaneously prepare silicon oxide and doped amorphous silicon thin films within the tube. Silicon oxide can be prepared directly within the PECVD tube, eliminating the need for other methods to prepare silicon oxide and then transfer it to the furnace, reducing the transfer process. Third, tubular PECVD has a very fast rate for preparing amorphous silicon thin films; the total time for preparing a 100nm amorphous silicon thin film is typically less than 10 minutes. Fourth, the amorphous silicon thin film is in-situ doped, eliminating the need for further diffusion processes. Even with subsequent crystallization treatment, the total time required to prepare TOPCon structures using tubular PECVD is approximately 90-120 minutes, significantly lower than the 280 minutes required by LPCVD.

[0049]4) Because the process steps are saved, the breakage rate of silicon wafers is greatly reduced, and the yield of the production process is improved.

[0050]5) In addition, depending on the process requirements, methane (CH_4) can be introduced to prepare doped silicon carbide, ammonia (NH_3) can be introduced to prepare doped silicon nitride, and carbon dioxide (CO_2) or nitrous oxide (N_2O) can be introduced to prepare doped silicon oxide.

Brief Description of the Drawings

[0051] Figure 1 is a schematic diagram of the existing TOPCon solar cell structure.

[0052] Figure 2 is a schematic diagram of a typical existing passivation sheet structure.

Detailed Description of the Embodiments

[0053] The present invention will be further described in detail below with reference to specific embodiments, but the present invention is not limited to the following specific embodiments.

[0054] Information on the n-type silicon wafer used in the embodiments: (100) crystal orientation, thickness of 180 micrometers, resistivity of 1-7 ohm-cm. Information on the p-type silicon wafer: (100) crystal orientation, thickness of 180 micrometers, resistivity of 0.5-1.5 ohm-cm. The following are specific embodiments.

[0055] Embodiment 1

[0056] Using the n-type silicon wafer, the surface damage layer is removed, and the same structure is deposited on both sides. The specific processing is as follows:

[0057]1. After cleaning, the silicon wafer is placed in a graphite boat;

[0058]2. Deposition of silicon oxide: substrate temperature 400°C, nitrous oxide (N_2O) as reaction gas, flow rate 3000sccm, gas pressure 200Pa, deposition power 2000W, RF on/off ratio 2ms:10ms, deposition time 120 seconds.

[0059]3. Deposit a phosphorus-doped amorphous silicon thin film on the silicon oxide layer: substrate temperature 600°C, $\text{SiH}_4:\text{H}_2:\text{PH}_3=1500\text{sccm}:10000\text{sccm}:1500\text{sccm}$, gas pressure 250Pa, deposition power 2000W, RF on/off ratio 3ms:45ms, deposition time 600 seconds;

[0060] 4. Deposit a phosphorus-doped amorphous silicon film II on the phosphorus-doped amorphous silicon film I: substrate temperature 600°C, $\text{SiH}_4:\text{H}_2:\text{PH}_3=1500\text{sccm}:10000\text{sccm}:1500\text{sccm}$, gas pressure is 150Pa, deposition power is 8000W, RF on/off ratio is 3ms:45ms, deposition time is 180 seconds;

[0061] 5. Crystallization annealing: Annealing at 800°C for about 40 minutes.

[0062] Finally, the surface passivation effect of the sample was tested using a Sinton WCT-120. The average implied open-circuit voltage $iVoc \approx 725mV$, the $iVoc$ distribution was 716~734mV, and the corresponding average surface saturation current $Jo \approx 8fA/cm^2$.

[0063] Embodiment 2

[0064] Using the n-type silicon wafer, the surface damage layer is removed, and the same structure is deposited on both sides. The specific process is as follows:

[0065] 1. After cleaning, the silicon wafer is placed in a graphite boat;

[0066] 2. Deposition of silicon oxide: substrate temperature 400°C, carbon dioxide (CO₂) as reaction gas, flow rate 5000sccm, gas pressure 220Pa, deposition power 2500W, RF on/off ratio 2ms:30ms, deposition time 120 seconds.

[0067] 3. Deposition of phosphorus-doped amorphous silicon thin film I: substrate temperature 500°C, SiH₄:H₂:PH₃=1000sccm:10000sccm:1000sccm, gas pressure 250Pa, deposition power 2000W, RF on/off ratio 3ms:75ms, deposition time 500 seconds;

[0068] 4. Deposition of phosphorus-doped amorphous silicon thin film II: substrate temperature 500°C, SiH₄:H₂:PH₃ = 1000sccm:10000sccm:1000sccm, gas pressure is 200Pa, deposition power is 10000W, RF on/off ratio is 3ms:75ms, deposition time is 200 seconds;

[0069] 5. Crystallization annealing: Annealing at 800°C for about 40 minutes.

[0070] Finally, the surface passivation effect of the sample was tested using a Sinton WCT-120. The average implied open-circuit voltage $iVoc \approx 723mV$, the $iVoc$ distribution was 714~733mV, and the corresponding surface saturation current $Jo \approx 8fA/cm^2$.

[0071] Embodiment 3

[0072] Using the n-type silicon wafer, the surface damage layer is removed, and the same structure is deposited on both sides. The specific process is as follows:

[0073] 1. After cleaning, the silicon wafer is placed in a graphite boat;

[0074] 2. Deposition of silicon oxide: substrate temperature 400°C, nitrous oxide (N₂O) as reaction gas, flow rate 3000sccm, gas pressure 200Pa, deposition power 2000W, RF on/off ratio 2ms:10ms, deposition time 120 seconds.

[0075] 3. Deposition of boron-doped amorphous silicon thin film I: substrate temperature 600°C, SiH₄:H₂:B₂H₆=1500sccm:2000sccm:1500sccm, gas pressure 250Pa, deposition power 1800W, RF on/off ratio 3ms:45ms, deposition time 600 seconds;

[0076] 4. Deposition of boron-doped amorphous silicon thin film II: substrate temperature 600°C, SiH₄:H₂:B₂H₆=1600sccm:10000sccm:1600sccm, gas pressure is 150Pa, deposition power is 10000W, RF on/off ratio is 3ms:45ms, deposition time is 300 seconds;

[0077] 5. Crystallization annealing: Annealing at 780°C for about 120 minutes.

[0078] Finally, the surface passivation effect of the sample was tested using a Sinton WCT-120. The average implied open-circuit voltage $iVoc \approx 672mV$, the $iVoc$ distribution was 668~679mV, and the corresponding surface saturation current $Jo \approx 78fA/cm^2$.

[0079] Embodiment 4

[0080] A 1 ohm-centimeter p-type silicon wafer is used, the surface damage layer is removed, and the same structure is deposited on both sides. The specific processing is as follows:

[0081] 1. After cleaning, the silicon wafer is placed in a graphite boat;

[0082] 2. Deposition of silicon oxide: substrate temperature 400°C, nitrous oxide (N₂O) as reaction gas, flow rate 2000sccm, gas pressure 240Pa, deposition power 2500W, RF on/off ratio 2ms:20ms, deposition time 100 seconds.

[0083] 3. Deposition of phosphorus-doped amorphous silicon thin film I: substrate temperature 600°C, SiH₄:H₂:PH₃=1500sccm:10000sccm:1500sccm, gas pressure 250Pa, deposition power 2000W, RF on/off ratio 3ms:60ms, deposition time 600 seconds;

[0084] 4. Deposition of phosphorus-doped amorphous silicon thin film II: substrate temperature 600°C, SiH₄:H₂:PH₃=1500sccm:10000sccm:1500sccm, gas pressure 150Pa, deposition power 13000W, RF on/off ratio 3ms:60ms, deposition time 240 seconds;

[0085] 5. Crystallization annealing: Annealing at 900°C for about 30 minutes.

[0086] Finally, the surface passivation effect of the sample was tested using a Sinton WCT-120. The average implied open-circuit voltage $iVoc \approx 716$ mV, the $iVoc$ distribution was 710~723 mV, and the corresponding surface saturation current $Jo \approx 11$ fA/cm².

[0087] Embodiment 5

[0088] The fabrication of the TOPCon structure using an n-type silicon wafer is described in detail below:

[0089] 1. After cleaning, the silicon wafer is placed in a graphite boat;

[0090] 2. Deposition of silicon oxide: substrate temperature 400°C, nitrous oxide (N₂O) as reaction gas, flow rate 3500sccm, gas pressure 200Pa, deposition power 2000W, RF on/off ratio 2ms:15ms, deposition time 200 seconds.

[0091] 3. Deposition of phosphorus-doped amorphous silicon thin film I: substrate temperature 600°C, SiH₄:H₂:PH₃=1500sccm:8000sccm:1500sccm, gas pressure 220Pa, deposition power 2000W, RF on/off ratio 3ms:55ms, deposition time 600 seconds;

[0092] 4. Deposition of phosphorus-doped amorphous silicon thin film II: substrate temperature 600°C, SiH₄:H₂:PH₃=1500sccm:8000sccm:1500sccm, gas pressure 180Pa, deposition power 11000W, RF on/off ratio 3ms:55ms, deposition time 300 seconds;

[0093] 5. Crystallization annealing: Annealing at 850°C for about 30 minutes.

[0094] 6. Finally, an n-type TOPCon battery with an efficiency of 22.7% was prepared.

[0095] Embodiment 6

[0096] The fabrication of the TOPCon structure using an n-type silicon wafer is described in detail below:

[0097] 1. After cleaning, the silicon wafer is placed in a graphite boat;

[0098] 2. Preparation of silicon oxide: Silicon oxide was prepared by thermal oxidation (600°C/20min);

[0099] 3. Deposition of phosphorus-doped amorphous silicon thin film I: substrate temperature 400°C, SiH₄:H₂:PH₃=1500sccm:8000sccm:1500sccm, gas pressure 220Pa, deposition power 2000W, RF on/off ratio 3ms:55ms, deposition time 600 seconds;

[0100] 4. Deposition of phosphorus-doped amorphous silicon thin film II: substrate temperature 400°C, SiH₄:H₂:PH₃=1500sccm:8000sccm:1500sccm, gas pressure 180Pa, deposition power 11000W, RF on/off ratio 3ms:55ms, deposition time 1000 seconds;

[0101] 5. Crystallization annealing: Annealing at 880°C for about 30 minutes.

[0102] Finally, the surface passivation effect of the sample was tested using a SintonWCT-120. The average implied open-circuit voltage $iVoc \approx 733$ mV, the $iVoc$ distribution was 720~733 mV, and the corresponding surface saturation current $Jo \approx 4$ fA/cm².

[0103] The above are merely exemplary embodiments of the present invention and do not constitute any limitation on the scope of protection of the present invention. All technical solutions formed by equivalent exchange or equivalent substitution fall within the scope of protection of the present invention.

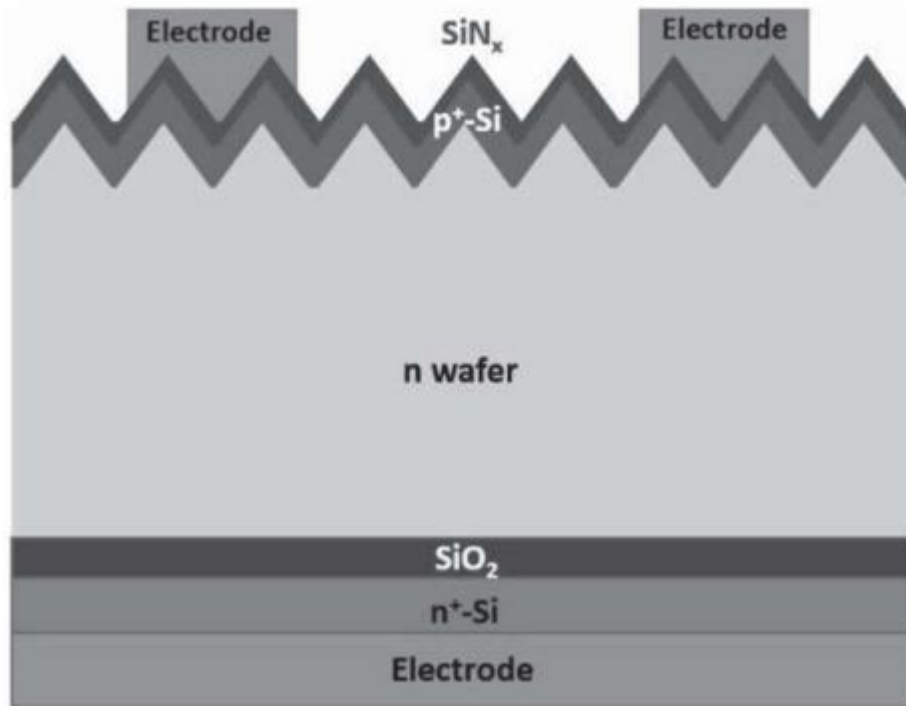


Figure 1

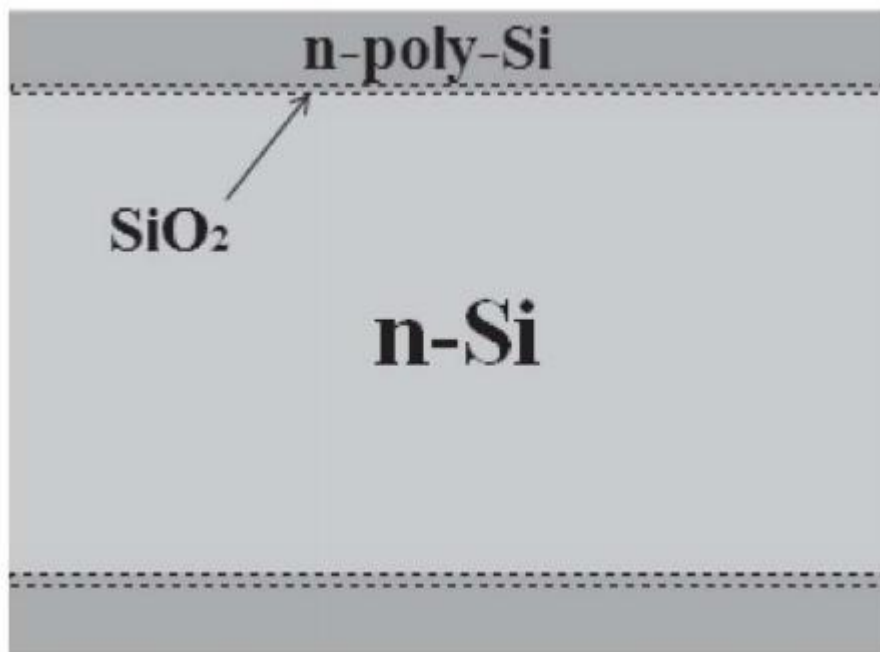


Figure 2

CERTIFICATE OF ACCURACY

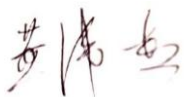
Attached as Ex A is the original document identified as patent application number CN109802007B and attached as Ex B is the translation of the original document from Chinese to English.

This is to certify under penalty of perjury that I, Weijie Huang, translated the document attached as Exhibit B and it is a true, accurate, and complete translation of Exhibit A.

I am thoroughly familiar with and competent in both Chinese and English languages. I have over 15 years of experience in translating Chinese to English and hold a Bachelor's degree in Linguistics from Beijing Language and Culture University. Attached as Exhibit C is a copy of my current CV.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 01/19/2026



Weijie Huang
Chinese > English Linguist

Your
legal
translation
partner 

Weijie Huang

Highlights

15 years in translation between Chinese and English in multiple domains with a focus on litigation.

Experience

Translator | Mar 2008 – Present

- Extensive experience translating litigation and dispute-related documents, including court pleadings, judgments, affidavits, witness statements, evidentiary materials, and legal correspondence for use in cross-border litigation and arbitration.
- Proven expertise in financial and corporate translation, covering annual reports, audited financial statements, investment agreements, shareholder agreements, trust deeds, compliance materials, and internal governance documents.
- Specialized experience in patent and IP translation, including patent specifications, claims, abstracts, office actions, prosecution history, prior art references, and related technical-legal documentation, with strict adherence to jurisdiction-specific terminology and formatting requirements.

Partial list of subject matter experience:

Telecommunications

- 4G/LTE, 5G NR, and 6G Standards
- Network Architecture and Protocols (TCP/IP, RAN, NFV)
- Wireless and Mobile Communication
- Signal Processing and Data Encoding
- Internet of Things (IoT) and M2M
- Satellite and Microwave Communication
- Cybersecurity and Encryption Protocols

Mechanical Engineering

- Automotive Engineering (EV Drivetrains, Autonomous Systems)
- Robotics and Industrial Automation
- Thermodynamics and Heat Exchange Systems
- Fluid Dynamics and Hydraulic/Pneumatic Systems
- Aerospace and Aeronautical Engineering
- Manufacturing and Tooling (CNC, Additive Manufacturing)

Pharmaceuticals

- Drug Delivery
- Biologics and Monoclonal Antibodies (mAbs)
- Gene and Cell Therapy (CRISPR, mRNA)
- Small Molecule Synthesis and API Manufacturing
- Pharmacokinetics and Pharmacodynamics (ADME)
- Clinical Trial Protocols and Regulatory Documentation
- Immunology and Vaccine Development
- Medicinal Chemistry

Chemistry

- Polymer and Materials Science
- Organic and Inorganic Synthesis
- Electrochemistry (Batteries, Fuel Cells)
- Heterogeneous and Homogeneous Catalysis
- Nanotechnology and Nanomaterials
- Petrochemicals and Refining Processes
- Analytical Chemistry and Spectroscopic Methods
- Biochemistry and Enzymology

- Regularly handles high-stakes legal translations submitted to courts, regulators, arbitration panels, and government authorities, ensuring precision, consistency, and defensibility of terminology.
- Deep familiarity with common law and civil law systems, enabling accurate rendering of legal concepts across jurisdictions without distortion of legal effect or procedural meaning.
- Experienced in translating complex, multi-entity and multi-jurisdictional matters, including materials involving offshore structures, trusts, cross-border investments, and regulatory filings.
- Skilled in maintaining terminology consistency across large-volume projects through glossaries, style guides, and parallel reference materials, particularly in long-running litigation or patent portfolios.
- Experienced in producing certified and court-ready translations, including Certificates of Accuracy where required, and working under tight litigation and regulatory deadlines.
- Comfortable collaborating with law firms, in-house legal teams, IP professionals, financial advisors, and compliance teams, responding to revision requests and clarification queries with precision and professionalism.
- Strong attention to detail, formatting fidelity, and document structure, ensuring translated documents mirror the original legal and technical layout for seamless reference and submission.

Education and Training

Bachelor of English Language and Literature, Beijing Language & Culture University (BLCU) (2004-2008)
Master of Professional Studies, Informatics with Concentration in Data Analytics, Northeastern University, (2022-2024)

Skills & Language Abilities

Bilingual (English-Mandarin) with fluency in Cantonese and basic French