



(12)发明专利申请

(10)申请公布号 CN 111640824 A

(43)申请公布日 2020.09.08

(21)申请号 202010528564.8

(22)申请日 2020.06.11

(71)申请人 常州时创能源股份有限公司

地址 213300 江苏省常州市溧阳市溧城镇
吴潭渡路8号

(72)发明人 沈梦超 张梦葛 黄海冰

(51)Int.Cl.

H01L 31/18(2006.01)

H01L 31/068(2012.01)

H01L 31/0288(2006.01)

权利要求书1页 说明书5页 附图2页

(54)发明名称

一种双面晶体硅太阳能电池及其制备方法

(57)摘要

本发明公开一种双面晶体硅太阳能电池制备方法,先在硅片上制备硼掺杂面所需表面形貌,然后进行硼掺杂,利用硼掺杂过程表面生成的氧化层作为掩膜制备磷掺杂面所需表面形貌并进行磷掺杂;通过氢氟酸水上漂去除硅片边沿的氧化层;通过边沿抛光对硅片进行边沿隔离,利用硼掺杂面和磷掺杂面的氧化层作为掩膜保护硅片两面掺杂层不被破坏;最后在硅片两面制作钝化层和金属电极。进一步,本发明还公开一种通过这种方法制得的双面晶体硅太阳能电池。该方法工艺过程简单,制作成本低,可以匹配不同类型的电池衬底和电池结构,并具有优良的边沿隔离效果,能大大降低双面晶体硅太阳能电池的边沿漏电。



CN 111640824 A

1. 一种双面晶体硅太阳能电池制备方法, 其特征在于, 包括以下步骤:
提供一种硅片, 选取硅片的一面作为硼掺杂面, 另一面作为磷掺杂面;
在硅片表面制备硼掺杂面所需表面形貌;
在硼掺杂面上进行硼掺杂, 制作硼掺杂层, 并在硼掺杂层表面生长一层硼氧化层;
通过氢氟酸水上漂的方法去除硼掺杂层制作过程中在磷掺杂面和边沿形成的绕扩硼氧化层;
在磷掺杂面制备磷掺杂面所需表面形貌, 同时去除硼掺杂层制作过程中在磷掺杂面和边沿形成的绕扩硼掺杂层, 所述硼氧化层被部分刻蚀或厚度保持不变;
在磷掺杂面上制作电池磷掺杂层, 并在磷掺杂面表面生长一层磷氧化层;
通过氢氟酸水上漂的方式去除磷掺杂层制作过程中在磷掺杂面的边沿形成的绕扩磷氧化层;
使用碱抛光的方式去除磷掺杂层制作过程中在磷掺杂面的边沿形成的绕扩磷掺杂层对硅片进行边沿隔离, 并同时去除磷掺杂制作过程中在硼氧化层表面附着的磷元素, 碱抛光后, 硼氧化层和磷氧化层未被完全刻蚀;
通过氢氟酸清洗的方式去除硼掺杂面剩余的硼氧化层和磷掺杂面剩余的磷氧化层;
对硼掺杂面和磷掺杂面进行表面钝化;
在硼掺杂面和磷掺杂面制备金属电极。
2. 如权利要求1所述的双面晶体硅太阳能电池制备方法, 其特征在于, 在硼掺杂层表面生长的硼氧化层的厚度为30-300nm。
3. 如权利要求1所述的双面晶体硅太阳能电池制备方法, 其特征在于, 在磷掺杂层表面生长的磷氧化层的厚度较制备完磷掺杂面所需表面形貌后的硼氧化层的厚度薄至少5nm。
4. 如权利要求3所述的双面晶体硅太阳能电池制备方法, 其特征在于, 在磷掺杂层表面生长的磷氧化层的厚度为3-20nm。
5. 如权利要求1所述的双面晶体硅太阳能电池制备方法, 其特征在于, 硼掺杂层方块电阻约为20-500 $\Omega/\square$, 磷掺杂层的方块电阻为20-500 $\Omega/\square$ 。
6. 如权利要求1所述的双面晶体硅太阳能电池制备方法, 其特征在于, 去除绕扩硼氧化层的氢氟酸水上漂的条件为: 氢氟酸溶液浓度为0.5-40%, 工艺时间为10-1200s。
7. 如权利要求1所述的双面晶体硅太阳能电池制备方法, 其特征在于, 去除绕扩磷氧化层的氢氟酸水上漂的条件为: 氢氟酸溶液浓度为0.5-10%, 工艺时间为5-300s。
8. 如权利要求1所述的双面晶体硅太阳能电池制备方法, 其特征在于, 所述碱抛光的条件是: 选用氢氧化钾或氢氧化钠的水溶液, 碱溶液浓度为0.5-20%, 抛光添加剂浓度为0.02-5%, 溶液温度为45-85 $^{\circ}\text{C}$, 抛光时间为10-300s; 所述抛光添加剂用于降低氧化层在碱溶液中的反应速率。
9. 如权利要求1所述的双面晶体硅太阳能电池制备方法, 其特征在于, 氢氟酸清洗硼氧化层和磷氧化层的条件为: 氢氟酸浓度为0.5-30%, 清洗时间为2-120min。
10. 一种双面晶体硅太阳能电池, 其特征在于, 采用权利要求1至9任意一项方法制备, 包括硅片基底; 依次形成于硅片基底一面的硼掺杂层、硼掺杂面钝化层、硼掺杂面金属电极; 依次形成于硅片基底另一面的磷掺杂层、磷掺杂面钝化层、磷掺杂面金属电极。

一种双面晶体硅太阳电池及其制备方法

[0001]

技术领域

[0002] 本发明属于晶体硅太阳电池制造技术领域,具体涉及一种双面晶体硅太阳电池制备方法及通过这种方法制得的双面晶体硅太阳电池。

背景技术

[0003] 太阳能是一种绿色环保的能源,太阳电池利用光生伏特效应将太阳能转换为电能,已经成为未来最有前景的能源解决方式。晶体硅太阳电池因其原料来源广,制作成本低等优势成为太阳电池的主要技术方案之一。在晶体硅太阳电池中,双面电池在电池两面进行了不同类型的掺杂在电池两面形成内建电场,具有优秀的载流子收集能力,并且能够双面受光提升发电能力。但是双面晶体硅太阳电池相比单面晶体硅太阳电池由于需要在电池两面进行不同类型的掺杂,为了避免两种掺杂相互之间的干扰,往往需要在电池的一面使用额外的掩膜来对另外一面的掺杂进行阻挡,工艺相对繁琐,也增加了制备成本,并且双面晶体硅太阳电池边沿处同时存在不同类型的掺杂,会增加电池边沿处的漏电,降低电池的性能。

发明内容

[0004] 有鉴于此,本发明提供一种双面晶体硅太阳电池制备方法,先在硅片上制备硼掺杂面所需表面形貌,然后进行硼掺杂,利用硼掺杂层表面生成的氧化层作为掩膜制备磷掺杂面所需表面形貌并进行磷掺杂;通过氢氟酸水上漂去除硅片边沿的磷氧化层;通过边沿抛光对硅片进行边沿隔离,利用硼掺杂面和磷掺杂面的氧化层作为掩膜保护硅片两面掺杂层不被破坏;最后在硅片两面制作钝化层和金属电极。进一步,本发明还公开一种通过这种方法制得的双面晶体硅太阳电池。本发明所述方法工艺过程简单,制作成本低,可以匹配不同类型的电池衬底和电池结构,且具有优良的边沿隔离效果,能大大降低双面晶体硅太阳电池的边沿漏电。

[0005] 结合图1所示,本发明公开的双面晶体硅太阳电池制备方法,主要包括以下步骤:

选取一种硅片。可以是n型单晶硅片、p型单晶硅片、n型多晶硅片或p型多晶硅片。

[0006] 选取硅片的一个面作为硼掺杂面,制备硼掺杂面所需表面形貌。具体可选择抛光或制绒的方法制备硼掺杂面所需表面形貌。另一个面即为磷掺杂面。

[0007] 在硼掺杂面上进行硼掺杂,制作电池硼掺杂层,并在硼掺杂面表面生长一层硼氧化层。硼掺杂可选择整面的均匀掺杂、局部掺杂或选择性掺杂。硼掺杂具体可选用管式硼扩散、硼浆掺杂、硼离子注入等方法中的一种或多种方法结合实现。硼氧化层是整面的,硼氧化层的生长通常在上述方法的杂质再分布阶段形成,也可以通过在硼掺杂之后再次对硅片进行氧化形成。硼氧化层形成后硼掺杂面的背面和边沿会因绕扩现象形成绕扩硼掺杂层和绕扩硼氧化层。硼掺杂层方块电阻约为 $20\sim 500\ \Omega/\square$,硼掺杂面上的硼氧化层厚度约为 $30\sim$

300nm。

[0008] 去除绕扩硼氧化层。具体可选用氢氟酸水上漂的方法去除硼掺杂面背面和边沿的绕扩硼氧化层。氢氟酸水上漂的工艺条件可以是：氢氟酸溶液浓度为0.5-40%，工艺时间为10-1200s。

[0009] 将硼掺杂面的背面作为磷掺杂面，制备磷掺杂面所需表面形貌，同时去除绕扩硼掺杂层。具体可选用碱制绒、碱抛光、酸刻蚀、酸制绒的方法制备磷掺杂面所需表面形貌。在此过程中，由于硼掺杂面具有硼氧化层，在制备磷掺杂面所需表面形貌过程中硼氧化层具有掩膜效果，能够保护硼掺杂面不被破坏。在制备磷掺杂面所需表面形貌完成后，硼氧化层厚度不变或有所减薄。

[0010] 在磷掺杂面上进行磷掺杂，制作电池磷掺杂层，并在磷掺杂面表面生长一层磷氧化层。磷掺杂可以选择整面的均匀掺杂、局部掺杂、选择性掺杂。磷掺杂具体可选用管式磷扩散、磷浆掺杂、磷离子注入等方法中的一种或多种方法结合实现。同样的，磷氧化层是整面的，磷氧化层的生长通常在上述方法的杂质再分布阶段形成，也可以通过在磷掺杂之后再次对硅片进行氧化形成。磷氧化层形成后硅片边沿会因绕扩现象形成绕扩磷掺杂层和绕扩磷氧化层，硼掺杂面的硼氧化层表面会因绕扩现象附着一层磷元素。磷掺杂层方块电阻约为20-500 $\Omega/\square$ ，磷掺杂面上的磷氧化层厚度约为3-20nm，磷氧化层的厚度比制备磷掺杂面所需表面形貌完成后硼氧化层剩余厚度薄5nm以上。

[0011] 去除绕扩磷氧化层。具体可使用氢氟酸水上漂的方法去除绕扩磷氧化层。在氢氟酸水上漂过程中，硼掺杂面朝下接触氢氟酸，由于氢氟酸溶液的表面张力作用，硅片边沿也会接触到氢氟酸，绕扩磷氧化层将被去除，磷掺杂面表面的磷氧化层厚度不变。由于硼掺杂面的硼氧化层厚度大于绕扩磷氧化层厚度，硼氧化层不会被完全去除。氢氟酸水上漂条件：氢氟酸溶液浓度为0.5-10%，工艺时间为5-300s。在氢氟酸水上漂之后，硼氧化层厚度减少约3-20nm，剩余厚度在5nm以上。去除绕扩磷氧化层之后，绕扩磷掺杂层裸露在硅片边沿。

[0012] 去除绕扩磷掺杂层，对硅片进行边沿隔离。使用碱抛光的方法去除绕扩磷掺杂层，由于硅片硼掺杂面表面具有硼氧化层，磷掺杂面表面具有磷氧化层，硼氧化层和磷氧化层在碱溶液中反应速率较慢，硼掺杂层和磷掺杂层不会被碱溶液腐蚀。硅片边沿具有绕扩磷掺杂层，绕扩磷掺杂层与碱溶液反应速率较快，将被碱溶液腐蚀，从而实现边沿隔离。碱抛光具体选用氢氧化钾或氢氧化钠的水溶液。碱抛光条件：选用氢氧化钠或氢氧化钾溶液，碱溶液浓度为0.5-20%，抛光添加剂浓度为0.02-5%，溶液温度为45-85℃，抛光时间为10-300s。抛光添加剂指含有脂肪醇聚氧乙烯醚等物质的化学品，具有降低氧化层在碱溶液中反应速率的功能。碱抛光之后，硼氧化层和磷氧化层厚度有所减少，但仍要有所保留，硼氧化层表面附着的一层磷元素被去除。

[0013] 去除硼氧化层和磷氧化层。使用氢氟酸清洗的方法去除硼氧化层和磷氧化层。氢氟酸清洗条件：氢氟酸浓度为0.5-30%，清洗时间为2-120min。

[0014] 对硅片进行表面钝化，具体可选择氧化铝、氮化硅、氧化硅、氮氧化硅、氟化镁、硫化锌中的一种或多种叠加对硅片表面进行钝化。钝化层制作方式不做限定。

[0015] 制备电池所需金属电极。金属电极制作方式可选择电镀、蒸镀、丝网印刷等方法实现。

[0016] 本发明具有以下有益效果：

本发明可通过简单的流程设置使硼掺杂面和磷掺杂面的表面形貌和掺杂浓度可以单独控制,不会相互影响,且具有较宽的工艺窗口。本发明能对硅片边沿进行有效隔离,降低的太阳电池边沿漏电问题,提升电池性能。

[0017] 本发明适用性广,可应用在不同类型的电池结构上,例如,p型双面电池、p型背结电池、n型双面电池、n型背结电池等。

附图说明

[0018] 图1 本发明所述的双面晶体硅太阳能电池制备流程图示意图;

图2为实施例1所述方法制备的n型正结双面电池,其中:11-n型单晶硅片,12-硼掺杂层,13-磷掺杂层,14-硼掺杂面钝化层,15-磷掺杂面钝化层,16-硼掺杂面金属电极,17-磷掺杂面金属电极;

图3为实施例2所述方法制备的n型正结双面电池,其中:21-p型单晶硅片,22-磷掺杂层,23-硼掺杂层,24-磷掺杂面钝化层,25-硼掺杂面钝化层,26-磷掺杂面金属电极,27-硼掺杂面金属电极。

具体实施方式

[0019] 下面结合具体实施例及附图进一步对本发明进行解释说明:

实施例1公开一种图2所示的n型正结双面电池(n型PERT)制备方法,主要包括以下步骤:

1.选取一种(100)晶向的n型单晶硅片,硅片电阻率为 $1.5\Omega\cdot\text{cm}$ 。

[0020] 2.选取硅片的一个面作为硼掺杂面,使用碱制绒的方法在硼掺杂面制备随机金字塔状绒面结构。使用业内常用的碱制绒方法即可。

[0021] 3.使用管式硼扩散的方法,在硼掺杂面上进行整面的均匀硼掺杂,制作电池硼掺杂层,并在硼掺杂面表面生长一层硼氧化层。硼掺杂后硼掺杂面的背面和边沿会因绕扩现象形成绕扩硼掺杂层和绕扩硼氧化层。硼掺杂层方块电阻约为 $100\Omega/\square$,硼掺杂面上的硼氧化层厚度约为80nm。

[0022] 4.将硼掺杂面的背面作为磷掺杂面,使用酸刻蚀的方法制备磷掺杂面所需表面形貌,同时去除绕扩硼氧化层和绕扩硼掺杂层,保留硼掺杂面上的硼氧化层。在酸刻蚀完成后,硼氧化层厚度基本不变。

[0023] 5.使用管式磷扩散的方法在磷掺杂面上进行整面的均匀磷掺杂,制作电池磷掺杂层,并在磷掺杂面表面生长一层磷氧化层。磷掺杂后硅片边沿会因绕扩现象形成绕扩磷掺杂层和绕扩磷氧化层,硼掺杂面的硼氧化层表面会因绕扩现象附着一层磷元素。磷掺杂层方块电阻约为 $50\Omega/\square$,磷掺杂面上的磷氧化层厚度约为10nm。

[0024] 6.使用氢氟酸水上漂的方法去除绕扩磷氧化层。氢氟酸水上漂条件:氢氟酸溶液浓度为3%,工艺时间为60s。在氢氟酸水上漂之后,硼氧化层厚度剩余约65nm。

[0025] 7.使用碱抛光的方法去除绕扩磷掺杂层,对硅片进行边沿隔离。碱抛光具体选用氢氧化钾的水溶液。碱抛光条件:碱溶液浓度为5%,抛光添加剂浓度为0.1%,溶液温度为 60°C ,抛光时间为300s。碱抛光之后,硼氧化层和磷氧化层厚度减少约5nm。

[0026] 8.去除硼氧化层和磷氧化层。使用氢氟酸清洗的方法去除硼氧化层和磷氧化层。

氢氟酸清洗条件:氢氟酸浓度为10%,清洗时间为30min。

[0027] 9.对硅片进行表面钝化。硼掺杂面钝化层使用氧化铝和氮化硅组成的叠层钝化层,其中氧化铝厚度约为5nm,氮化硅厚度约为75nm,氮化硅折射率为2.0。磷掺杂面使用氧化硅和氮化硅组成的叠层钝化层,其中氧化硅厚度约为2nm,氮化硅厚度约为80nm

10.使用丝网印刷的方法制备电池所需金属电极,硼掺杂面和磷掺杂面金属电极均为等间距分布的栅线状金属电极。至此,得到图2所示的n型PERT电池。

[0028] 实施例2公开一种图3所示的p型正结双面电池(p型PERT)制备方法,实施例1和实施例2主要不同之处在于硼掺杂面和磷掺杂面表面形貌不同并且可以单独控制,主要包括以下步骤:

1.选取一种(100)晶向的p型单晶硅片,硅片电阻率为 $0.8\ \Omega\cdot\text{cm}$ 。

[0029] 2.选取硅片的一个面作为硼掺杂面,使用碱抛光的方法制备硼掺杂面所需表面形貌。使用业内常用的碱抛光方法即可。

[0030] 3.使用管式硼扩散的方法,在硼掺杂面上进行整面的均匀硼掺杂,制作电池硼掺杂层,并在硼掺杂面表面生长一层硼氧化层。硼掺杂后硼掺杂面的背面和边沿会因绕扩现象形成绕扩硼掺杂层和绕扩硼氧化层。硼掺杂层方块电阻约为 $30\ \Omega/\square$,硼掺杂面上的硼氧化层厚度约为150nm。

[0031] 4.使用氢氟酸水上漂的方法去除硼掺杂面背面和边沿的绕扩硼氧化层。氢氟酸水上漂条件:氢氟酸溶液浓度为10%,工艺时间为360s。

[0032] 5.将硼掺杂面的背面作为磷掺杂面,使用碱制绒的方法在磷掺杂面制备随机金字塔状绒面结构,同时去除绕扩硼掺杂层,保留硼掺杂面上的硼氧化层。在碱制绒完成后,硼氧化层厚度减少约15nm。

[0033] 6.使用管式磷扩散的方法在磷掺杂面上进行整面的均匀磷掺杂,制作电池磷掺杂层,并在磷掺杂面表面生长一层磷氧化层。磷掺杂后硅片边沿会因绕扩现象形成绕扩磷掺杂层和绕扩磷氧化层,硼掺杂面的硼氧化层表面会因绕扩现象附着一层磷元素。磷掺杂层方块电阻约为 $120\ \Omega/\square$,磷掺杂面上的磷氧化层厚度约为15nm。

[0034] 7.使用氢氟酸水上漂的方法去除绕扩磷氧化层。氢氟酸水上漂条件:氢氟酸溶液浓度为3%,工艺时间为80s。在氢氟酸水上漂之后,硼氧化层厚度剩余约110 nm。

[0035] 8.使用碱抛光的方法去除绕扩磷掺杂层,对硅片进行边沿隔离。碱抛光具体选用氢氧化钾的水溶液。碱抛光条件:碱溶液浓度为20%,抛光添加剂浓度为5%,溶液温度为45℃,抛光时间为20s。碱抛光之后,硼氧化层和磷氧化层厚度减少约10nm。

[0036] 9.去除硼氧化层和磷氧化层。使用氢氟酸清洗的方法去除硼氧化层和磷氧化层。氢氟酸清洗条件:氢氟酸浓度为30%,清洗时间为20min。

[0037] 10.对硅片进行表面钝化。硼掺杂面钝化层使用氧化铝和氮化硅组成的叠层钝化层,其中氧化铝厚度约为15nm,氮化硅厚度约为70nm,氮化硅折射率为2.0。磷掺杂面使用氧化硅和氮化硅组成的叠层钝化层,其中氧化硅厚度约为2nm,氮化硅厚度约为80nm。

[0038] 11.使用丝网印刷的方法制备电池所需金属电极,硼掺杂面和磷掺杂面金属电极均为等间距分布的栅线状金属电极。至此,得到图3所示的p型PERT电池。

[0039] 最后需要说明的是,以上所述仅为本发明的优选实施例而已,并不用于限制本发明,对于本领域的技术人员来说,本发明可以有各种更改和变化。凡在本发明的精神和原则

之内,所作的任何修改、等同替换、改进等,均应包含在本发明的保护范围之内。

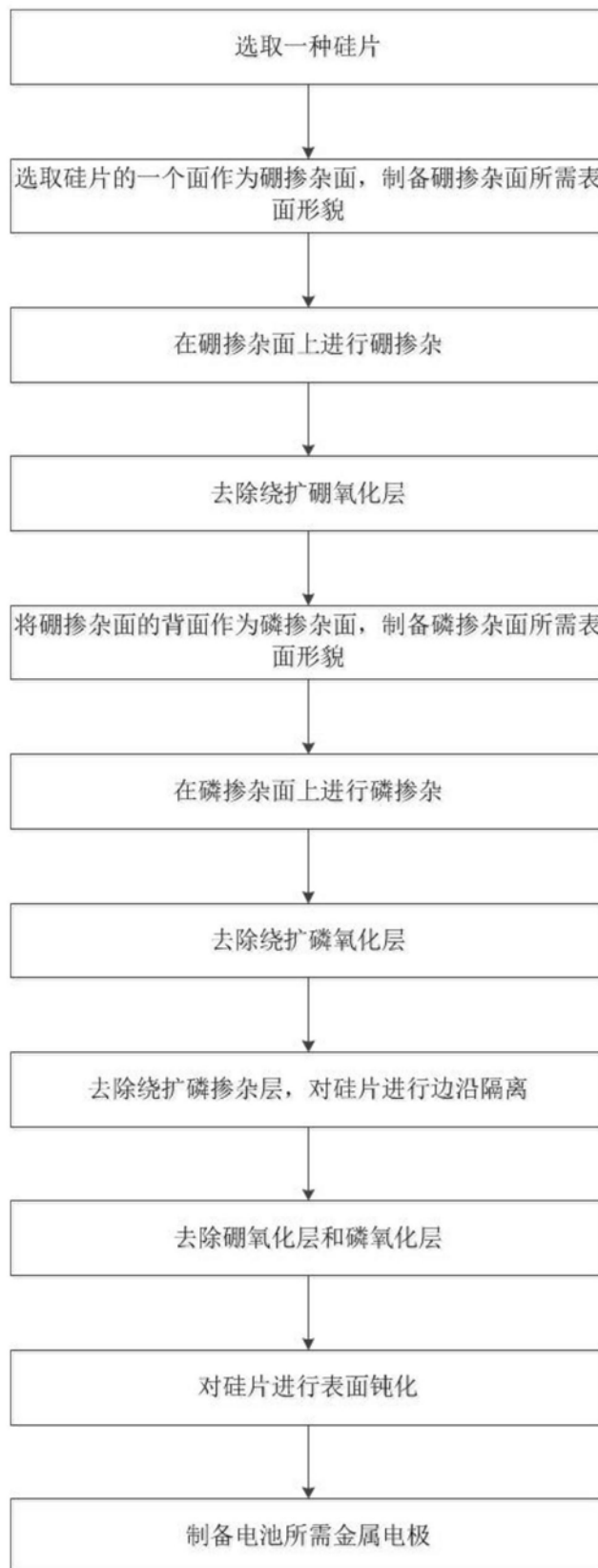


图1

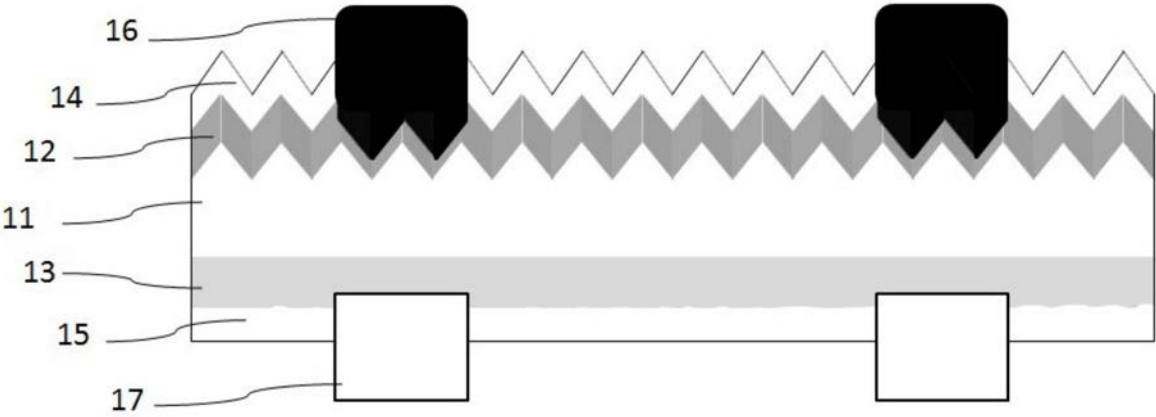


图2

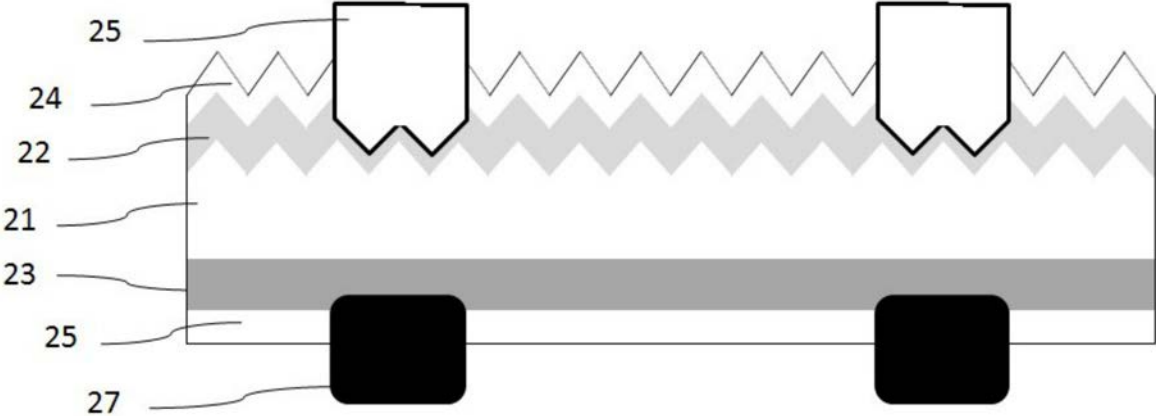


图3

1 Document

Publication numbers	Title	Current assignees
CN111640824B B	Double-sided crystalline silicon solar cell and preparation method thereof	CHANGZHOU SHICHUANG ENERGY

Family 1/1 - FAMPAT - ©Questel

Priority numbers

CN202010528564

Application number

CN202010528564

Publication numbers

CN111640824

CN111640824

Questel unique family ID (FAN)

90523532

Family publication details

CN111640824	B	2023-06-02	CN111640824B
CN111640824	A	2020-09-08	CN111640824

**Priority dates**

2020-06-11

Application dates

2020-06-11

Publication dates

2023-06-02

2020-09-08

Grant dates

(CN111640824B)

2023-06-02

Expected expiry dates

(CN111640824)

2040-06-11

Title

(CN111640824)

Double-sided crystalline silicon solar cell and preparation method thereof

Abstract

(CN111640824)

The invention discloses a preparation method of a double-sided crystalline silicon solar cell. The method comprises the following steps of: preparing surface morphology required by a boron-doped surface on a silicon wafer, then performing boron doping, preparing surface morphology required by a phosphorus-doped surface by using an oxide layer generated on the surface in the boron doping process as a mask, and performing phosphorus doping; removing the oxide layer on the edge of the silicon wafer through hydrofluoric acid water rinsing; performing edge isolation on the silicon wafer through edge polishing, and using oxide layers of the boron-doped surface and the phosphorus-doped surface as masks to protect doped layers on the two surfaces of the silicon wafer from being damaged; and finally, manufacturing a passivation layer and a metal electrode on two sides of the silicon wafer. Furthermore, the invention also discloses the double-sided crystalline silicon solar cell prepared by the method. The method is simple in technological process and low in manufacturing cost, can be matched with different types of cell substrates and cell structures, has an excellent edge isolation effect, and can greatly reduce edge electric leakage of the double-sided crystalline silicon solar cell.

Current assignees

CHANGZHOU SHICHUANG ENERGY

Assignee history

(CN111640824)

CHANGZHOU SHICHUANG ENERGY CO., LTD ([CN])

(CN111640824)

CHANGZHOU SHICHUANG ENERGY CO., LTD ([CN])

Inventors

SHEN MENGCHAO
ZHANG MENGGE
HUANG HAIBING

Inventors

(CN111640824)
SHEN MENGCHAO
ZHANG MENGGE
HUANG HAIBING
(CN111640824)
SHEN MENGCHAO
ZHANG MENGGE
HUANG HAIBING

Claims

(CN111640824)

1. The preparation method of the double-sided crystalline silicon solar cell is characterized by comprising the following steps of:

providing a silicon wafer, wherein one surface of the silicon wafer is selected as a boron doped surface, and the other surface of the silicon wafer is selected as a phosphorus doped surface;

preparing the surface morphology required by the boron doped surface on the surface of the silicon wafer;

boron doping is carried out on the boron doped surface, a boron doped layer is manufactured, and a boron oxide layer is grown on the surface of the boron doped layer; removing a winding boron oxide layer formed on the phosphorus doped surface and the edge in the manufacturing process of the boron doped layer by a hydrofluoric acid water floating method; preparing the surface morphology required by the phosphorus doped surface on the phosphorus doped surface, and simultaneously removing a winding boron doped layer formed on the phosphorus doped surface and the edge in the process of manufacturing the boron doped layer, wherein the boron oxide layer is partially etched or the thickness is kept unchanged;

manufacturing a battery phosphorus doping layer on the phosphorus doping surface, and growing a phosphorus oxide layer on the surface of the phosphorus doping surface;

removing a winding phosphorus oxide layer formed at the edge of the phosphorus doped surface in the process of manufacturing the phosphorus doped layer in a hydrofluoric acid water floating manner;

removing a surrounding phosphorus-expanding doped layer formed at the edge of a phosphorus doped surface in the process of manufacturing the phosphorus doped layer by using an alkali polishing mode to perform edge isolation on the silicon wafer, and simultaneously removing phosphorus elements attached to the surface of the boron oxide layer in the process of manufacturing the phosphorus doped layer, wherein the boron oxide layer and the phosphorus oxide layer are not completely etched after the alkali polishing;

removing the residual boron oxide layer on the boron doped surface and the residual phosphorus oxide layer on the phosphorus doped surface in a hydrofluoric acid cleaning mode;

surface passivation is carried out on the boron doped surface and the phosphorus doped surface;

preparing metal electrodes on the boron doped surface and the phosphorus doped surface;

the thickness of the boron oxide layer grown on the surface of the boron doped layer is 30-300nm;

the thickness of the phosphorus oxide layer grown on the surface of the phosphorus doped layer is 3-20nm;

the conditions for removing the hydrofluoric acid water bleaching around the boron expansion oxidation layer are as follows: the concentration of the hydrofluoric acid solution is 0.5-40%, and the process time is 10-1200s;

the conditions for removing the hydrofluoric acid water bleaching around the phosphorus-expanding oxide layer are as follows: the concentration of the hydrofluoric acid solution is 0.5-10%, and the process time is 5-300s;

the conditions of the alkali polishing are as follows: selecting aqueous solution of potassium hydroxide or sodium hydroxide, wherein the concentration of the aqueous solution is 0.5-20%, the concentration of the polishing additive is 0.02-5%, the temperature of the solution is 45-85 °C, and the polishing time is 10-300s; the polishing additive is used to reduce

the reaction rate of the oxide layer in the alkaline solution.

2. The method of claim 1, wherein the thickness of the phosphorus oxide layer grown on the surface of the phosphorus doped layer is at least 5nm thinner than the thickness of the boron oxide layer after the surface morphology required for the preparation of the phosphorus doped surface.

3. The method of claim 1, wherein the boron doped layer has a sheet resistance of about 20-500 $\Omega/\square$ and the phosphorus doped layer has a sheet resistance of about 20-500 $\Omega/\square$.

4. The method for preparing the double-sided crystalline silicon solar cell according to claim 1, wherein the conditions for cleaning the boron oxide layer and the phosphorus oxide layer by hydrofluoric acid are as follows: the concentration of hydrofluoric acid is 0.5-30%, and the cleaning time is 2-120min.

5. A double-sided crystalline silicon solar cell, characterized in that it is produced by the method according to any one of claims 1 to 4, comprising a silicon wafer substrate; the boron doped layer, the boron doped surface passivation layer and the boron doped surface metal electrode are sequentially formed on one surface of the silicon wafer substrate; the phosphorus doped layer, the phosphorus doped surface passivation layer and the phosphorus doped surface metal electrode are sequentially formed on the other surface of the silicon wafer substrate.

Description

(CN111640824)

TECHNICAL FIELD

[0001] The invention belongs to the technical field of crystalline silicon solar cell manufacturing, and particularly relates to a preparation method of a double-sided crystalline silicon solar cell and the double-sided crystalline silicon solar cell prepared by the method.

BACKGROUND ART

[0002] Solar energy is an environment-friendly energy source, and solar cells convert solar energy into electric energy by utilizing photovoltaic effect, so that the solar energy becomes the most promising energy source solution in the future. The crystalline silicon solar cell has the advantages of wide sources of raw materials, low manufacturing cost and the like, and becomes one of the main technical schemes of the solar cell. In the crystalline silicon solar cell, the double-sided cell is doped on two sides of the cell in different types to form a built-in electric field on two sides of the cell, so that the crystalline silicon solar cell has excellent carrier collection capability and can be subjected to double-sided light receiving to improve the power generation capability. However, compared with a single-sided crystalline silicon solar cell, the double-sided crystalline silicon solar cell has the advantages that different types of doping are required to be performed on two sides of the cell, so that in order to avoid mutual interference of the two types of doping, an additional mask is often required to be used on one side of the cell to block the doping on the other side, the process is relatively complicated, the preparation cost is increased, and different types of doping exist at the edge of the double-sided crystalline silicon solar cell at the same time, so that electric leakage at the edge of the cell is increased, and the performance of the cell is reduced.

DISCLOSURE

Disclosure of Invention

[0003] In view of the above, the present invention provides a method for preparing a double-sided crystalline silicon solar cell, which comprises the steps of preparing a surface morphology required by a boron doped surface on a silicon wafer, then performing boron doping, preparing a surface morphology required by a phosphorus doped surface by using an oxide layer generated on the surface of a boron doped layer as a mask, and performing phosphorus doping; removing a phosphorus oxide layer at the edge of the silicon wafer through hydrofluoric acid water rinsing; performing edge isolation on the silicon wafer by edge polishing, and protecting the two doped layers of the silicon wafer from being damaged by using the boron doped surface and the oxide layer of the phosphorus doped surface as masks; and finally, manufacturing passivation layers and metal electrodes on the two sides of the silicon wafer. Further, the invention also discloses a double-sided crystalline silicon solar cell manufactured by the method. The method has simple technical process and low manufacturing cost, can be matched with different types of battery substrates and battery structures, has excellent edge isolation effect, and can greatly reduce the edge leakage of the double-sided crystalline silicon solar battery.

[0004] Referring to fig. 1, the preparation method of the double-sided crystalline silicon solar cell disclosed by the invention mainly comprises the following steps:

[0005] a silicon wafer is selected. Can be an n-type monocrystalline silicon wafer, a p-type monocrystalline silicon wafer, an

n-type polycrystalline silicon wafer or a p-type polycrystalline silicon wafer.

[0006] One surface of the silicon wafer is selected as a boron doped surface, and the surface morphology required by the boron doped surface is prepared. Specifically, the surface morphology required by the boron doped surface can be prepared by selecting a polishing or texturing method. The other surface is the phosphorus doped surface.

[0007] And (3) carrying out boron doping on the boron doped surface, manufacturing a boron doped layer of the battery, and growing a boron oxide layer on the surface of the boron doped surface. The boron doping may be selected from the group consisting of uniform doping throughout, localized doping, and selective doping. The boron doping can be realized by combining one or more of the methods of tubular boron diffusion, boron slurry doping, boron ion implantation and the like. The boron oxide layer is integral and the growth of the boron oxide layer is usually formed at the impurity redistribution stage of the above method, or can be formed by oxidizing the silicon wafer again after boron doping. The back and edge of the boron doped surface after the boron oxide layer is formed can form a around-expansion boron doped layer and a around-expansion boron oxide layer due to the around-expansion phenomenon. The square resistance of the boron doped layer is about 20-500 $\Omega/\square$ and the thickness of the boron oxide layer on the boron doped surface is about 30-300nm.

[0008] And removing the around-expansion boron oxide layer. The method of hydrofluoric acid water floating is particularly selected to remove the around-expansion boron oxide layer on the back and the edge of the boron doped surface. The technological conditions of the hydrofluoric acid water bleaching can be as follows: the concentration of the hydrofluoric acid solution is 0.5-40%, and the process time is 10-1200s.

[0009] And taking the back surface of the boron doped surface as a phosphorus doped surface, preparing the surface morphology required by the phosphorus doped surface, and simultaneously removing the surrounding and expanding boron doped layer. Specifically, the surface morphology required by the phosphorus doped surface can be prepared by adopting the methods of alkali texturing, alkali polishing, acid etching and acid texturing. In the process, the boron doped surface is provided with the boron oxide layer, so that the boron oxide layer has a masking effect in the process of preparing the surface morphology required by the phosphorus doped surface, and the boron doped surface can be protected from being damaged. After the surface morphology required for preparing the phosphorus doped surface is finished, the thickness of the boron oxide layer is unchanged or thinned.

[0010] And (3) carrying out phosphorus doping on the phosphorus doped surface, manufacturing a phosphorus doped layer of the battery, and growing a phosphorus oxide layer on the surface of the phosphorus doped surface. The phosphorus doping can be selected from uniform doping, local doping and selective doping of the whole surface. The phosphorus doping can be realized by combining one or more of the methods of tubular phosphorus diffusion, phosphorus slurry doping, phosphorus ion implantation and the like. Similarly, the phosphorus oxide layer is integral and the growth of the phosphorus oxide layer is usually formed at the impurity redistribution stage of the above method, or may be formed by oxidizing the silicon wafer again after phosphorus doping. After the phosphorus oxide layer is formed, a phosphorus-doped layer and a phosphorus-doped layer are formed on the edge of the silicon wafer due to the phenomenon of coiling and expanding, and a layer of phosphorus element is attached to the surface of the boron oxide layer on the boron doped surface due to the phenomenon of coiling and expanding. The square resistance of the phosphorus doped layer is about 20-500 $\Omega/\square$, the thickness of the phosphorus oxide layer on the phosphorus doped surface is about 3-20nm, and the thickness of the phosphorus oxide layer is more than 5nm thinner than the residual thickness of the boron oxide layer after the surface morphology required by the preparation of the phosphorus doped surface is finished.

[0011] And removing the around-phosphorus-expansion oxide layer. Specifically, the method of hydrofluoric acid water bleaching can be used for removing the around-expansion phosphorus oxide layer. In the process of the hydrofluoric acid water floating, the boron doped surface is downward contacted with hydrofluoric acid, the edge of the silicon wafer is also contacted with hydrofluoric acid under the action of the surface tension of a hydrofluoric acid solution, the surrounding phosphorus oxide layer is removed, and the thickness of the phosphorus oxide layer on the surface of the phosphorus doped surface is unchanged. The thickness of the boron oxide layer of the boron doped surface is larger than that of the surrounding phosphorus oxide layer, so that the boron oxide layer cannot be completely removed. Hydrofluoric acid water bleaching conditions: the concentration of the hydrofluoric acid solution is 0.5-10%, and the process time is 5-300s. After the hydrofluoric acid water is rinsed, the thickness of the boron oxide layer is reduced by about 3-20nm, and the residual thickness is more than 5nm. And after the around-phosphorus-expanding oxide layer is removed, the around-phosphorus-expanding doped layer is exposed at the edge of the silicon wafer.

[0012] And removing the winding phosphorus-doped layer, and performing edge isolation on the silicon wafer. The around-expansion phosphorus doped layer is removed by an alkali polishing method, and as the boron oxide layer is arranged on the surface of the boron doped surface of the silicon wafer and the phosphorus oxide layer is arranged on the surface of the phosphorus doped surface, the reaction rate of the boron oxide layer and the phosphorus oxide layer in alkali solution is slower, and the boron doped layer and the phosphorus doped layer cannot be corroded by the alkali solution. The silicon wafer edge is provided with a phosphorus-surrounding and phosphorus-expanding doped layer, the reaction rate of the phosphorus-surrounding and phosphorus-expanding doped layer and the alkali solution is high, and the silicon wafer edge is corroded by the alkali solution, so that edge isolation is realized. The alkali polishing is specifically aqueous solution of potassium hydroxide or sodium hydroxide. Alkali polishing conditions: sodium hydroxide or potassium hydroxide solution is selected, the concentration of the alkali solution is 0.5-20%, the concentration of the polishing additive is 0.02-5%, the temperature of the solution is 45-85 °C, and the polishing time is 10-300s. The polishing additive refers to a chemical containing substances such as fatty alcohol polyoxyethylene ether and the like, and has the function of reducing the reaction rate of an oxide layer in an alkali solution. After the alkali polishing, the thickness of the boron oxide layer and the phosphorus oxide layer is reduced, but the thickness still remains, and a layer of phosphorus element attached to the surface of the boron oxide layer is removed.

[0013] And removing the boron oxide layer and the phosphorus oxide layer. And removing the boron oxide layer and the phosphorus oxide layer by using a hydrofluoric acid cleaning method. Hydrofluoric acid cleaning conditions: the concentration of hydrofluoric acid is 0.5-30%, and the cleaning time is 2-120min.

[0014] The surface passivation is carried out on the silicon wafer, and the surface of the silicon wafer can be passivated by superposing one or more of aluminum oxide, silicon nitride, silicon oxide, silicon oxynitride, magnesium fluoride and zinc sulfide. The passivation layer is not limited in its fabrication method.

[0015] And preparing a metal electrode required by the battery. The metal electrode can be manufactured by electroplating, vapor plating, screen printing and other methods.

[0016] The invention has the following beneficial effects:

[0017] the invention can enable the surface morphology and doping concentration of the boron doping surface and the phosphorus doping surface to be controlled independently through simple process setting, can not influence each other, and has a wider process window. The invention can effectively isolate the edge of the silicon wafer, reduce the problem of electric leakage at the edge of the solar cell and improve the performance of the cell.

[0018] The invention has wide applicability and can be applied to different types of battery structures, such as a p-type double-sided battery, a p-type back junction battery, an n-type double-sided battery, an n-type back junction battery and the like.

DRAWINGS DESCRIPTION

[0019] FIG. 1 is a schematic flow chart of a preparation method of a double-sided crystalline silicon solar cell according to the invention;

[0020] fig. 2 is an n-type positive junction double sided battery prepared as described in example 1, wherein: the device comprises an 11-n type monocrystalline silicon piece, a 12-boron doped layer, a 13-phosphorus doped layer, a 14-boron doped surface passivation layer, a 15-phosphorus doped surface passivation layer, a 16-boron doped surface metal electrode and a 17-phosphorus doped surface metal electrode;

[0021] fig. 3 is an n-type positive junction double sided battery prepared as described in example 2, wherein: the device comprises a 21-p type monocrystalline silicon wafer, a 22-phosphorus doped layer, a 23-boron doped layer, a 24-phosphorus doped surface passivation layer, a 25-boron doped surface passivation layer, a 26-phosphorus doped surface metal electrode and a 27-boron doped surface metal electrode.

INVENTION MODE

Detailed Description

[0022] The invention is further illustrated by the following examples and the accompanying drawings:

[0023] example 1 discloses a method for preparing an n-type positive junction double-sided battery (n-type PERT) shown in fig. 2, which mainly comprises the following steps:

[0024] 1. an n-type monocrystalline silicon wafer with a (100) crystal orientation is selected, and the resistivity of the silicon wafer is 1.5 ohm cm.

[0025] 2. One surface of the silicon wafer is selected as a boron doped surface, and a random pyramid-shaped suede structure is prepared on the boron doped surface by using an alkali suede method. The alkali texturing method commonly used in the industry is used.

[0026] 3. And (3) carrying out uniform boron doping on the whole surface of the boron doped surface by using a tubular boron diffusion method, manufacturing a boron doped layer of the battery, and growing a boron oxide layer on the surface of the boron doped surface. The back and edge of the boron doped surface after boron doping can form a around-expansion boron doped layer and a around-expansion boron oxide layer due to the around-expansion phenomenon. The sheet resistance of the boron doped layer was about $100 \Omega/\square$ and the thickness of the boron oxide layer on the boron doped surface was about 80nm.

[0027] 4. And taking the back surface of the boron doped surface as a phosphorus doped surface, preparing the surface morphology required by the phosphorus doped surface by using an acid etching method, simultaneously removing the around-expansion boron oxide layer and the around-expansion boron doped layer, and reserving the boron oxide layer on the boron doped surface. After the acid etching is completed, the thickness of the boron oxide layer is basically unchanged.

[0028] 5. And carrying out the whole-surface uniform phosphorus doping on the phosphorus doping surface by using a tubular phosphorus diffusion method, manufacturing a phosphorus doping layer of the battery, and growing a phosphorus oxide layer on the surface of the phosphorus doping surface. The edge of the silicon wafer after being doped with phosphorus can form a phosphorus-doped layer and a phosphorus-doped oxide layer by the surrounding and expanding phenomenon, and a layer of phosphorus element can be attached to the surface of the boron oxide layer on the boron doped surface by the surrounding and expanding phenomenon. The sheet resistance of the phosphorus doped layer was about $50 \Omega/\square$ and the thickness of the phosphorus oxide layer on the phosphorus doped surface was about 10nm.

[0029] 6. And removing the around-phosphorus-expansion oxide layer by using a hydrofluoric acid water bleaching method. Hydrofluoric acid water bleaching conditions: the concentration of the hydrofluoric acid solution is 3%, and the process time is 60s. After the hydrofluoric acid water rinse, the boron oxide layer remained at about 65nm thick.

[0030] 7. And removing the around-phosphorus-doped layer by using an alkali polishing method, and performing edge isolation on the silicon wafer. The alkali polishing is specifically performed by using an aqueous solution of potassium hydroxide. Alkali polishing conditions: the concentration of the alkali solution is 5%, the concentration of the polishing additive is 0.1%, the temperature of the solution is 60 °C, and the polishing time is 300s. After the alkali polishing, the boron oxide layer and the phosphorus oxide layer thickness were reduced by about 5nm.

[0031] 8. And removing the boron oxide layer and the phosphorus oxide layer. And removing the boron oxide layer and the phosphorus oxide layer by using a hydrofluoric acid cleaning method. Hydrofluoric acid cleaning conditions: the concentration of hydrofluoric acid is 10%, and the cleaning time is 30min.

[0032] 9. And carrying out surface passivation on the silicon wafer. The boron doped surface passivation layer is a laminated passivation layer composed of aluminum oxide and silicon nitride, wherein the thickness of the aluminum oxide is about 5nm, the thickness of the silicon nitride is about 75nm, and the refractive index of the silicon nitride is 2.0. The phosphorus doped surface uses a laminated passivation layer composed of silicon oxide and silicon nitride, wherein the thickness of the silicon oxide is about 2nm, and the thickness of the silicon nitride is about 80nm

[0033] 10. The metal electrodes required by the battery are prepared by using a screen printing method, and the metal electrodes of the boron doped surface and the phosphorus doped surface are all grid line metal electrodes distributed at equal intervals. Thus, an n-type PERT cell shown in FIG. 2 was obtained.

[0034] Example 2 discloses a method for preparing a p-type positive junction double-sided battery (p-type PERT) shown in fig. 3, and the main difference between example 1 and example 2 is that the surface morphology of the boron doped surface and the surface morphology of the phosphorus doped surface are different and can be controlled independently, and the method mainly comprises the following steps:

[0035] 1. and selecting a p-type monocrystalline silicon wafer with the crystal orientation of (100), wherein the resistivity of the silicon wafer is 0.8 $\Omega \cdot \text{cm}$.

[0036] 2. One surface of the silicon wafer is selected as a boron doped surface, and the surface morphology required by the boron doped surface is prepared by an alkali polishing method. The alkali polishing method commonly used in the industry is used.

[0037] 3. And (3) carrying out uniform boron doping on the whole surface of the boron doped surface by using a tubular

boron diffusion method, manufacturing a boron doped layer of the battery, and growing a boron oxide layer on the surface of the boron doped surface. The back and edge of the boron doped surface after boron doping can form a around-expansion boron doped layer and a around-expansion boron oxide layer due to the around-expansion phenomenon. The sheet resistance of the boron doped layer was about $30\Omega/\square$ and the thickness of the boron oxide layer on the boron doped surface was about 150nm.

[0038] 4. And removing the around-expansion boron oxide layer on the back and the edge of the boron doped surface by using a hydrofluoric acid water floating method. Hydrofluoric acid water bleaching conditions: the concentration of the hydrofluoric acid solution is 10 percent, and the process time is 360 seconds.

[0039] 5. And taking the back surface of the boron doped surface as a phosphorus doped surface, preparing a random pyramid-shaped suede structure on the phosphorus doped surface by using an alkali texturing method, removing the surrounding and expanding boron doped layer, and reserving the boron oxide layer on the boron doped surface. After alkali texturing is completed, the thickness of the boron oxide layer is reduced by about 15nm.

[0040] 6. And carrying out the whole-surface uniform phosphorus doping on the phosphorus doping surface by using a tubular phosphorus diffusion method, manufacturing a phosphorus doping layer of the battery, and growing a phosphorus oxide layer on the surface of the phosphorus doping surface. The edge of the silicon wafer after being doped with phosphorus can form a phosphorus-doped layer and a phosphorus-doped oxide layer by the surrounding and expanding phenomenon, and a layer of phosphorus element can be attached to the surface of the boron oxide layer on the boron doped surface by the surrounding and expanding phenomenon. The sheet resistance of the phosphorus doped layer is about $120\Omega/\square$ and the thickness of the phosphorus oxide layer on the phosphorus doped surface is about 15nm.

[0041] 7. And removing the around-phosphorus-expansion oxide layer by using a hydrofluoric acid water bleaching method. Hydrofluoric acid water bleaching conditions: the concentration of the hydrofluoric acid solution is 3 percent and the process time is 80 seconds. After the hydrofluoric acid water rinse, the boron oxide layer remained approximately 110 a nm a thick.

[0042] 8. And removing the around-phosphorus-doped layer by using an alkali polishing method, and performing edge isolation on the silicon wafer. The alkali polishing is specifically performed by using an aqueous solution of potassium hydroxide. Alkali polishing conditions: the concentration of the alkali solution is 20%, the concentration of the polishing additive is 5%, the temperature of the solution is 45 °C, and the polishing time is 20s. After the alkali polishing, the boron oxide layer and the phosphorus oxide layer thickness were reduced by about 10nm.

[0043] 9. And removing the boron oxide layer and the phosphorus oxide layer. And removing the boron oxide layer and the phosphorus oxide layer by using a hydrofluoric acid cleaning method. Hydrofluoric acid cleaning conditions: the concentration of hydrofluoric acid is 30%, and the cleaning time is 20min.

[0044] 10. And carrying out surface passivation on the silicon wafer. The boron doped surface passivation layer is a laminated passivation layer composed of aluminum oxide and silicon nitride, wherein the thickness of the aluminum oxide is about 15nm, the thickness of the silicon nitride is about 70nm, and the refractive index of the silicon nitride is 2.0. The phosphorus doped surface uses a stacked passivation layer of silicon oxide and silicon nitride, wherein the silicon oxide is about 2nm thick and the silicon nitride is about 80nm thick.

[0045] 11. The metal electrodes required by the battery are prepared by using a screen printing method, and the metal electrodes of the boron doped surface and the phosphorus doped surface are all grid line metal electrodes distributed at equal intervals. Thus, a p-type PERT cell shown in FIG. 3 was obtained.

[0046] Finally, it should be understood that the above description is only of the preferred embodiments of the present invention and is not intended to limit the invention, but rather that various modifications and changes will be apparent to those skilled in the art. Any modification, equivalent replacement, improvement, etc. made within the spirit and principle of the present invention should be included in the protection scope of the present invention.

English description

(CN111640824)

TECHNICAL FIELD

[0001] The invention belongs to the technical field of crystalline silicon solar cell manufacturing, and particularly relates to a preparation method of a double-sided crystalline silicon solar cell and the double-sided crystalline silicon solar cell prepared by the method.

BACKGROUND ART

[0002] Solar energy is an environment-friendly energy source, and solar cells convert solar energy into electric energy by utilizing photovoltaic effect, so that the solar energy becomes the most promising energy source solution in the future. The crystalline silicon solar cell has the advantages of wide sources of raw materials, low manufacturing cost and the like, and becomes one of the main technical schemes of the solar cell. In the crystalline silicon solar cell, the double-sided cell is doped on two sides of the cell in different types to form a built-in electric field on two sides of the cell, so that the crystalline silicon solar cell has excellent carrier collection capability and can be subjected to double-sided light receiving to improve the power generation capability. However, compared with a single-sided crystalline silicon solar cell, the double-sided crystalline silicon solar cell has the advantages that different types of doping are required to be performed on two sides of the cell, so that in order to avoid mutual interference of the two types of doping, an additional mask is often required to be used on one side of the cell to block the doping on the other side, the process is relatively complicated, the preparation cost is increased, and different types of doping exist at the edge of the double-sided crystalline silicon solar cell at the same time, so that electric leakage at the edge of the cell is increased, and the performance of the cell is reduced.

DISCLOSURE

Disclosure of Invention

[0003] In view of the above, the present invention provides a method for preparing a double-sided crystalline silicon solar cell, which comprises the steps of preparing a surface morphology required by a boron doped surface on a silicon wafer, then performing boron doping, preparing a surface morphology required by a phosphorus doped surface by using an oxide layer generated on the surface of a boron doped layer as a mask, and performing phosphorus doping; removing a phosphorus oxide layer at the edge of the silicon wafer through hydrofluoric acid water rinsing; performing edge isolation on the silicon wafer by edge polishing, and protecting the two doped layers of the silicon wafer from being damaged by using the boron doped surface and the oxide layer of the phosphorus doped surface as masks; and finally, manufacturing passivation layers and metal electrodes on the two sides of the silicon wafer. Further, the invention also discloses a double-sided crystalline silicon solar cell manufactured by the method. The method has simple technical process and low manufacturing cost, can be matched with different types of battery substrates and battery structures, has excellent edge isolation effect, and can greatly reduce the edge leakage of the double-sided crystalline silicon solar battery.

[0004] Referring to fig. 1, the preparation method of the double-sided crystalline silicon solar cell disclosed by the invention mainly comprises the following steps:

[0005] a silicon wafer is selected. Can be an n-type monocrystalline silicon wafer, a p-type monocrystalline silicon wafer, an n-type polycrystalline silicon wafer or a p-type polycrystalline silicon wafer.

[0006] One surface of the silicon wafer is selected as a boron doped surface, and the surface morphology required by the boron doped surface is prepared. Specifically, the surface morphology required by the boron doped surface can be prepared by selecting a polishing or texturing method. The other surface is the phosphorus doped surface.

[0007] And (3) carrying out boron doping on the boron doped surface, manufacturing a boron doped layer of the battery, and growing a boron oxide layer on the surface of the boron doped surface. The boron doping may be selected from the group consisting of uniform doping throughout, localized doping, and selective doping. The boron doping can be realized by combining one or more of the methods of tubular boron diffusion, boron slurry doping, boron ion implantation and the like. The boron oxide layer is integral and the growth of the boron oxide layer is usually formed at the impurity redistribution stage of the above method, or can be formed by oxidizing the silicon wafer again after boron doping. The back and edge of the boron doped surface after the boron oxide layer is formed can form a around-expansion boron doped layer and a around-expansion boron oxide layer due to the around-expansion phenomenon. The square resistance of the boron doped layer is about 20-500 $\Omega/\square$ and the thickness of the boron oxide layer on the boron doped surface is about 30-300nm.

[0008] And removing the around-expansion boron oxide layer. The method of hydrofluoric acid water floating is particularly selected to remove the around-expansion boron oxide layer on the back and the edge of the boron doped surface. The technological conditions of the hydrofluoric acid water bleaching can be as follows: the concentration of the hydrofluoric acid solution is 0.5-40%, and the process time is 10-1200s.

[0009] And taking the back surface of the boron doped surface as a phosphorus doped surface, preparing the surface morphology required by the phosphorus doped surface, and simultaneously removing the surrounding and expanding boron doped layer. Specifically, the surface morphology required by the phosphorus doped surface can be prepared by

adopting the methods of alkali texturing, alkali polishing, acid etching and acid texturing. In the process, the boron doped surface is provided with the boron oxide layer, so that the boron oxide layer has a masking effect in the process of preparing the surface morphology required by the phosphorus doped surface, and the boron doped surface can be protected from being damaged. After the surface morphology required for preparing the phosphorus doped surface is finished, the thickness of the boron oxide layer is unchanged or thinned.

[0010] And (3) carrying out phosphorus doping on the phosphorus doped surface, manufacturing a phosphorus doped layer of the battery, and growing a phosphorus oxide layer on the surface of the phosphorus doped surface. The phosphorus doping can be selected from uniform doping, local doping and selective doping of the whole surface. The phosphorus doping can be realized by combining one or more of the methods of tubular phosphorus diffusion, phosphorus slurry doping, phosphorus ion implantation and the like. Similarly, the phosphorus oxide layer is integral and the growth of the phosphorus oxide layer is usually formed at the impurity redistribution stage of the above method, or may be formed by oxidizing the silicon wafer again after phosphorus doping. After the phosphorus oxide layer is formed, a phosphorus-doped layer and a phosphorus-oxidized layer are formed on the edge of the silicon wafer due to the phenomenon of coiling and expanding, and a layer of phosphorus element is attached to the surface of the boron oxide layer on the boron doped surface due to the phenomenon of coiling and expanding. The square resistance of the phosphorus doped layer is about 20-500 $\Omega/\square$, the thickness of the phosphorus oxide layer on the phosphorus doped surface is about 3-20nm, and the thickness of the phosphorus oxide layer is more than 5nm thinner than the residual thickness of the boron oxide layer after the surface morphology required by the preparation of the phosphorus doped surface is finished.

[0011] And removing the around-phosphorus-expansion oxide layer. Specifically, the method of hydrofluoric acid water bleaching can be used for removing the around-expansion phosphorus oxide layer. In the process of the hydrofluoric acid water floating, the boron doped surface is downward contacted with hydrofluoric acid, the edge of the silicon wafer is also contacted with hydrofluoric acid under the action of the surface tension of a hydrofluoric acid solution, the surrounding phosphorus oxide layer is removed, and the thickness of the phosphorus oxide layer on the surface of the phosphorus doped surface is unchanged. The thickness of the boron oxide layer of the boron doped surface is larger than that of the surrounding phosphorus oxide layer, so that the boron oxide layer cannot be completely removed. Hydrofluoric acid water bleaching conditions: the concentration of the hydrofluoric acid solution is 0.5-10%, and the process time is 5-300s. After the hydrofluoric acid water is rinsed, the thickness of the boron oxide layer is reduced by about 3-20nm, and the residual thickness is more than 5nm. And after the around-phosphorus-expanding oxide layer is removed, the around-phosphorus-expanding doped layer is exposed at the edge of the silicon wafer.

[0012] And removing the winding phosphorus-doped layer, and performing edge isolation on the silicon wafer. The around-expansion phosphorus doped layer is removed by an alkali polishing method, and as the boron oxide layer is arranged on the surface of the boron doped surface of the silicon wafer and the phosphorus oxide layer is arranged on the surface of the phosphorus doped surface, the reaction rate of the boron oxide layer and the phosphorus oxide layer in alkali solution is slower, and the boron doped layer and the phosphorus doped layer cannot be corroded by the alkali solution. The silicon wafer edge is provided with a phosphorus-surrounding and phosphorus-expanding doped layer, the reaction rate of the phosphorus-surrounding and phosphorus-expanding doped layer and the alkali solution is high, and the silicon wafer edge is corroded by the alkali solution, so that edge isolation is realized. The alkali polishing is specifically aqueous solution of potassium hydroxide or sodium hydroxide. Alkali polishing conditions: sodium hydroxide or potassium hydroxide solution is selected, the concentration of the alkali solution is 0.5-20%, the concentration of the polishing additive is 0.02-5%, the temperature of the solution is 45-85 °C, and the polishing time is 10-300s. The polishing additive refers to a chemical containing substances such as fatty alcohol polyoxyethylene ether and the like, and has the function of reducing the reaction rate of an oxide layer in an alkali solution. After the alkali polishing, the thickness of the boron oxide layer and the phosphorus oxide layer is reduced, but the thickness still remains, and a layer of phosphorus element attached to the surface of the boron oxide layer is removed.

[0013] And removing the boron oxide layer and the phosphorus oxide layer. And removing the boron oxide layer and the phosphorus oxide layer by using a hydrofluoric acid cleaning method. Hydrofluoric acid cleaning conditions: the concentration of hydrofluoric acid is 0.5-30%, and the cleaning time is 2-120min.

[0014] The surface passivation is carried out on the silicon wafer, and the surface of the silicon wafer can be passivated by superposing one or more of aluminum oxide, silicon nitride, silicon oxide, silicon oxynitride, magnesium fluoride and zinc

sulfide. The passivation layer is not limited in its fabrication method.

[0015] And preparing a metal electrode required by the battery. The metal electrode can be manufactured by electroplating, vapor plating, screen printing and other methods.

[0016] The invention has the following beneficial effects:

[0017] the invention can enable the surface morphology and doping concentration of the boron doping surface and the phosphorus doping surface to be controlled independently through simple process setting, can not influence each other, and has a wider process window. The invention can effectively isolate the edge of the silicon wafer, reduce the problem of electric leakage at the edge of the solar cell and improve the performance of the cell.

[0018] The invention has wide applicability and can be applied to different types of battery structures, such as a p-type double-sided battery, a p-type back junction battery, an n-type double-sided battery, an n-type back junction battery and the like.

DRAWINGS DESCRIPTION

[0019] FIG. 1 is a schematic flow chart of a preparation method of a double-sided crystalline silicon solar cell according to the invention;

[0020] fig. 2 is an n-type positive junction double sided battery prepared as described in example 1, wherein: the device comprises an 11-n type monocrystalline silicon piece, a 12-boron doped layer, a 13-phosphorus doped layer, a 14-boron doped surface passivation layer, a 15-phosphorus doped surface passivation layer, a 16-boron doped surface metal electrode and a 17-phosphorus doped surface metal electrode;

[0021] fig. 3 is an n-type positive junction double sided battery prepared as described in example 2, wherein: the device comprises a 21-p type monocrystalline silicon wafer, a 22-phosphorus doped layer, a 23-boron doped layer, a 24-phosphorus doped surface passivation layer, a 25-boron doped surface passivation layer, a 26-phosphorus doped surface metal electrode and a 27-boron doped surface metal electrode.

INVENTION MODE

Detailed Description

[0022] The invention is further illustrated by the following examples and the accompanying drawings:

[0023] example 1 discloses a method for preparing an n-type positive junction double-sided battery (n-type PERT) shown in fig. 2, which mainly comprises the following steps:

[0024] 1. an n-type monocrystalline silicon wafer with a (100) crystal orientation is selected, and the resistivity of the silicon wafer is 1.5 $\Omega \cdot \text{cm}$.

[0025] 2. One surface of the silicon wafer is selected as a boron doped surface, and a random pyramid-shaped suede structure is prepared on the boron doped surface by using an alkali suede method. The alkali texturing method commonly used in the industry is used.

[0026] 3. And (3) carrying out uniform boron doping on the whole surface of the boron doped surface by using a tubular boron diffusion method, manufacturing a boron doped layer of the battery, and growing a boron oxide layer on the surface of the boron doped surface. The back and edge of the boron doped surface after boron doping can form a around-expansion boron doped layer and a around-expansion boron oxide layer due to the around-expansion phenomenon. The sheet resistance of the boron doped layer was about 100 $\Omega/\square$ and the thickness of the boron oxide layer on the boron doped surface was about 80nm.

[0027] 4. And taking the back surface of the boron doped surface as a phosphorus doped surface, preparing the surface morphology required by the phosphorus doped surface by using an acid etching method, simultaneously removing the around-expansion boron oxide layer and the around-expansion boron doped layer, and reserving the boron oxide layer on the boron doped surface. After the acid etching is completed, the thickness of the boron oxide layer is basically unchanged.

[0028] 5. And carrying out the whole-surface uniform phosphorus doping on the phosphorus doping surface by using a tubular phosphorus diffusion method, manufacturing a phosphorus doping layer of the battery, and growing a phosphorus oxide layer on the surface of the phosphorus doping surface. The edge of the silicon wafer after being doped with phosphorus can form a phosphorus-doped layer and a phosphorus-doped oxide layer by the surrounding and expanding phenomenon, and a layer of phosphorus element can be attached to the surface of the boron oxide layer on the boron doped surface by the surrounding and expanding phenomenon. The sheet resistance of the phosphorus doped layer was about 50 $\Omega/\square$ and the thickness of the phosphorus oxide layer on the phosphorus doped surface was about 10nm.

[0029] 6. And removing the around-phosphorus-expansion oxide layer by using a hydrofluoric acid water bleaching method. Hydrofluoric acid water bleaching conditions: the concentration of the hydrofluoric acid solution is 3%, and the process time is 60s. After the hydrofluoric acid water rinse, the boron oxide layer remained at about 65nm thick.

[0030] 7. And removing the around-phosphorus-doped layer by using an alkali polishing method, and performing edge isolation on the silicon wafer. The alkali polishing is specifically performed by using an aqueous solution of potassium hydroxide. Alkali polishing conditions: the concentration of the alkali solution is 5%, the concentration of the polishing additive is 0.1%, the temperature of the solution is 60 °C, and the polishing time is 300s. After the alkali polishing, the boron oxide layer and the phosphorus oxide layer thickness were reduced by about 5nm.

[0031] 8. And removing the boron oxide layer and the phosphorus oxide layer. And removing the boron oxide layer and the phosphorus oxide layer by using a hydrofluoric acid cleaning method. Hydrofluoric acid cleaning conditions: the concentration of hydrofluoric acid is 10%, and the cleaning time is 30min.

[0032] 9. And carrying out surface passivation on the silicon wafer. The boron doped surface passivation layer is a laminated passivation layer composed of aluminum oxide and silicon nitride, wherein the thickness of the aluminum oxide is about 5nm, the thickness of the silicon nitride is about 75nm, and the refractive index of the silicon nitride is 2.0. The phosphorus doped surface uses a laminated passivation layer composed of silicon oxide and silicon nitride, wherein the thickness of the silicon oxide is about 2nm, and the thickness of the silicon nitride is about 80nm

[0033] 10. The metal electrodes required by the battery are prepared by using a screen printing method, and the metal electrodes of the boron doped surface and the phosphorus doped surface are all grid line metal electrodes distributed at equal intervals. Thus, an n-type PERT cell shown in FIG. 2 was obtained.

[0034] Example 2 discloses a method for preparing a p-type positive junction double-sided battery (p-type PERT) shown in fig. 3, and the main difference between example 1 and example 2 is that the surface morphology of the boron doped surface and the surface morphology of the phosphorus doped surface are different and can be controlled independently, and the method mainly comprises the following steps:

[0035] 1. and selecting a p-type monocrystalline silicon wafer with the crystal orientation of (100), wherein the resistivity of the silicon wafer is 0.8 $\Omega \cdot \text{cm}$.

[0036] 2. One surface of the silicon wafer is selected as a boron doped surface, and the surface morphology required by the boron doped surface is prepared by an alkali polishing method. The alkali polishing method commonly used in the industry is used.

[0037] 3. And (3) carrying out uniform boron doping on the whole surface of the boron doped surface by using a tubular boron diffusion method, manufacturing a boron doped layer of the battery, and growing a boron oxide layer on the surface of the boron doped surface. The back and edge of the boron doped surface after boron doping can form a around-expansion boron doped layer and a around-expansion boron oxide layer due to the around-expansion phenomenon. The sheet resistance of the boron doped layer was about $30\Omega/\square$ and the thickness of the boron oxide layer on the boron doped surface was about 150nm.

[0038] 4. And removing the around-expansion boron oxide layer on the back and the edge of the boron doped surface by using a hydrofluoric acid water floating method. Hydrofluoric acid water bleaching conditions: the concentration of the hydrofluoric acid solution is 10 percent, and the process time is 360 seconds.

[0039] 5. And taking the back surface of the boron doped surface as a phosphorus doped surface, preparing a random pyramid-shaped suede structure on the phosphorus doped surface by using an alkali texturing method, removing the surrounding and expanding boron doped layer, and reserving the boron oxide layer on the boron doped surface. After alkali texturing is completed, the thickness of the boron oxide layer is reduced by about 15nm.

[0040] 6. And carrying out the whole-surface uniform phosphorus doping on the phosphorus doping surface by using a tubular phosphorus diffusion method, manufacturing a phosphorus doping layer of the battery, and growing a phosphorus oxide layer on the surface of the phosphorus doping surface. The edge of the silicon wafer after being doped with phosphorus can form a phosphorus-doped layer and a phosphorus-doped oxide layer by the surrounding and expanding phenomenon, and a layer of phosphorus element can be attached to the surface of the boron oxide layer on the boron doped surface by the surrounding and expanding phenomenon. The sheet resistance of the phosphorus doped layer is about $120 \Omega/\square$ and the thickness of the phosphorus oxide layer on the phosphorus doped surface is about 15nm.

[0041] 7. And removing the around-phosphorus-expansion oxide layer by using a hydrofluoric acid water bleaching method.

Hydrofluoric acid water bleaching conditions: the concentration of the hydrofluoric acid solution is 3 percent and the process time is 80 seconds. After the hydrofluoric acid water rinse, the boron oxide layer remained approximately 110 nm thick.

[0042] 8. And removing the around-phosphorus-doped layer by using an alkali polishing method, and performing edge isolation on the silicon wafer. The alkali polishing is specifically performed by using an aqueous solution of potassium hydroxide. Alkali polishing conditions: the concentration of the alkali solution is 20%, the concentration of the polishing additive is 5%, the temperature of the solution is 45 °C, and the polishing time is 20s. After the alkali polishing, the boron oxide layer and the phosphorus oxide layer thickness were reduced by about 10nm.

[0043] 9. And removing the boron oxide layer and the phosphorus oxide layer. And removing the boron oxide layer and the phosphorus oxide layer by using a hydrofluoric acid cleaning method. Hydrofluoric acid cleaning conditions: the concentration of hydrofluoric acid is 30%, and the cleaning time is 20min.

[0044] 10. And carrying out surface passivation on the silicon wafer. The boron doped surface passivation layer is a laminated passivation layer composed of aluminum oxide and silicon nitride, wherein the thickness of the aluminum oxide is about 15nm, the thickness of the silicon nitride is about 70nm, and the refractive index of the silicon nitride is 2.0. The phosphorus doped surface uses a stacked passivation layer of silicon oxide and silicon nitride, wherein the silicon oxide is about 2nm thick and the silicon nitride is about 80nm thick.

[0045] 11. The metal electrodes required by the battery are prepared by using a screen printing method, and the metal electrodes of the boron doped surface and the phosphorus doped surface are all grid line metal electrodes distributed at equal intervals. Thus, a p-type PERT cell shown in FIG. 3 was obtained.

[0046] Finally, it should be understood that the above description is only of the preferred embodiments of the present invention and is not intended to limit the invention, but rather that various modifications and changes will be apparent to those skilled in the art. Any modification, equivalent replacement, improvement, etc. made within the spirit and principle of the present invention should be included in the protection scope of the present invention.

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