

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT TRIAL AND APPEAL BOARD

SEG MANUFACTURING INC., NEW ENERGY IMPORTS INC.,
SEG SOLAR INC., PT. SEG SOLAR MANUFAKTUR INDONESIA, and
SEG ENERGY SINGAPORE PTE. LTD.,

Petitioners

v.

SHANGHAI JINKO GREEN ENERGY ENTERPRISE MANAGEMENT CO.,
LTD. AND ZHEJIANG JINKO SOLAR CO., LTD.,

Patent Owners

Case No. IPR2026-00230
Patent 11,824,136

**DECLARATION OF E. FRED SCHUBERT, PH.D. IN SUPPORT OF PETITION FOR *INTER*
PARTES REVIEW**

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I. INTRODUCTION

1. My name is E. Fred Schubert, Ph.D. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

2. I have been asked to provide technical assistance in the inter partes review of U.S. Patent No. 11,824,136, which I may abbreviate as “the ’136 Patent” or refer to as the “Challenged Patent.” This declaration is a statement of my opinions on issues related to the unpatentability of claims of the ’136 Patent. I am being compensated at an hourly rate of \$600/hour for my analysis, plus reimbursement for expenses. My compensation does not depend on the content of my opinions or the outcome of this proceeding.

3. I am not employed by Petitioners or any affiliate or subsidiary thereof. I do not have a financial interest in Petitioners.

II. SUMMARY OF OPINIONS

4. As set forth in detail below, in my opinion, claims 1-20 of the ’136 patent are unpatentable in view of the grounds set forth below and in the Petition.

III. EXPERIENCE AND QUALIFICATIONS

5. A true and correct copy of my *curriculum vitae* (CV) is included as Ex. 2029. The following is a brief summary of my relevant qualifications and professional experience.

6. I am currently an active tenured full Professor in the Department for Electrical, Computer, and Systems Engineering at the Rensselaer Polytechnic Institute (RPI) located in Troy, New York. My major faculty activities are teaching, research, intramural and extramural service, and consulting.

7. I received a Bachelor's Degree in Electrical Engineering from the University of Stuttgart, Germany, in 1978. I received a Master's Degree in Electrical Engineering from the University of Stuttgart in 1981. I then joined the Max Planck Institute for Solid-State Research, Stuttgart, as a Member of the Scientific Staff, and, from 1981 to 1985, conducted research for which I received a Ph.D. degree in Electrical Engineering from the University of Stuttgart.

8. In 1985, subsequent to my tenure at the Max Planck Institute, I joined AT&T Bell Laboratories in Holmdel and Murray Hill, New Jersey, initially as a post-doctoral Member of Technical Staff. About two years later, in 1988, I became a Member of Technical Staff, Principal Investigator, and Member of Management. I worked at AT&T Bell Laboratories for 10 years, until 1995.

9. In 1995, I joined academia. My first position was at Boston University (Boston, MA), where I worked as a full professor for seven years. At Boston University, I directed the Semiconductor Devices Research Laboratory and co-directed (with Professor Jan G. Smits) the Silicon Integrated Circuit Processing Facility.

10. In 2002, I joined Rensselaer Polytechnic Institute (RPI) as a distinguished professor, the Wellfleet Senior Constellation Professor with appointments in the Department for Electrical, Computer, and Systems Engineering and the Department for Physics, Applied Physics and Astronomy. During my tenure at RPI, I held various leadership positions, including Head of the Future Chips Constellation and Director of the Smart Lighting Engineering Research Center (Smart Lighting ERC) that was funded by the U.S. National Science Foundation at a volume of \$40 million for over 10 years.

11. I am named as inventor or co-inventor of 39 U.S. patents and have co-authored more than 300 publications. I authored the books “Doping in III-V Semiconductors” (1993), “Delta Doping of Semiconductors” (1996), “Physical Foundations of Solid-State Devices” (2015 and 2022) and the first, second and third editions of “Light-Emitting Diodes” (2003, 2006 and 2018); the latter book is known as a standard textbook in the field of LEDs, and the book has been translated into Russian, Japanese and Korean. My publications have been well recognized by the technical community as illustrated by the more than 45,000 citations that my publications have received.

12. I received several awards for my technical contributions. They include: Senior Member IEEE (1993); Literature Prize of Verein Deutscher Elektrotechniker for my book “Doping in III-V Semiconductors” (1994); Fellow SPIE (1999);

Alexander von Humboldt Senior Research Award (1999); Fellow IEEE (1999); Fellow OSA (2000); Boston University Provost Innovation Award (2000); Discover Magazine Award for Technological Innovation (2000); R&D 100 Award for RCLED (2001); Fellow APS (2001); RPI Trustees Award for Faculty Achievement (2002 and 2008); Honorary Membership in Eta Kappa Nu (2004); 25 Most Innovative Micro- and Nano-Products of the Year Award of R&D Magazine (2007); and Scientific American 50 Award (2007).

13. My general expertise is in the field of electrical engineering and applied physics including semiconductor materials, semiconductor physics, processing, and devices.

14. I have worked on multiple aspects of solar cell technology. My research, teaching, and consulting activities included electrical aspects of solar cells, optical aspects of solar cells, as well as manufacturing aspects of solar cells. My work activities in solar cells are reflected in my publication activities that include multiple publications on anti-reflection coatings.

15. My work activities on the electrical aspects of solar cells focused on the doping of solar cells including the employment of highly doped regions and doping with a concentration gradient to promote carrier transport over the PN-junction barrier and over the contact barriers to demonstrate solar cells with a high efficiency. The base materials of solar cell materials I developed included single-crystal silicon,

poly-crystalline silicon, as well as III-V semiconductors. I have conducted research on ohmic metal-to-semiconductor contacts having an insulating interface layer (such as TiO_2 , SiO_2 and Si_3N_4) that de-pins the Fermi level, passivates the semiconductor surface, and allows for the tuning of the Schottky barrier height by selection of metals with suitable metal work functions.

16. My work activities on the optical aspects of solar cells included the design and fabrication of low-reflectivity optical coatings that minimize Fresnel reflection losses. The anti-reflection coatings included multiple layers having a carefully designed refractive index sequence, so as to minimize optical reflections over a broad wavelength range, as is desirable for the broad spectral band of solar radiation (ranging from the infrared to the ultraviolet).

17. My work activities on the manufacturing aspects of solar cells included ohmic contacts made by diffusion rather than implantation processes. Furthermore, my activities included manufacturing feasibility studies for graded-index optical coatings that possess a high degree of porosity, which may reduce the mechanical strength of the coatings. Finally, my activities included manufacturing efficiency considerations, such as throughput considerations as well as reliability considerations.

18. As Director and Principal Investigator of the Smart Lighting Engineering Research Centre, funded by the US National Science Foundation, I have directed

research on LEDs for use in intelligent or “smart” lighting systems. Such smart lighting systems have functionalities that go beyond lighting and include, for example, the tuning of the color temperature, as well as communication with lighting sources.

IV. TASK SUMMARY AND MATERIALS REVIEWED

19. I have been asked to review the Challenged Patent and its prosecution history, to provide an understanding of the technology relevant to the Challenged Patent, to review certain prior-art references, and to analyze whether or not those references disclose or teach limitations of claims from the Challenged Patent. The opinions stated in this declaration are from the perspective of a person of ordinary skill in the art (POSITA).

V. LIST OF EXHIBITS

20. In forming my opinions, I have reviewed the Challenged Patent, its prosecution history and references cited by the Examiner, the materials cited in the List of Exhibits, and the materials cited throughout my declaration.

Exhibit Number	Description
EX1001	U.S. Patent No. 11,824,136 to Yu et al. (“the ’136 Patent”)
EX1002	CV of Petitioners’ Expert Dr. Fred Shubert

EX1003	Expert Declaration of Petitioners' Expert Dr. Fred Shubert
EX1004	Chinese Patent No. CN112259614A to Ye et al. ("Ye")
EX1005	Chinese Patent No. CN105826411B to Yun et al. ("Yun")
EX1006	Chinese Patent No. CN111690987A to Xia et al. ("Xia")
EX1007	File History of the '454 Patent (Parent of the '136 Patent)
EX1008	Reserved
EX1009	PCT International Publication No. WO2016/129481 to Sakai ("Sakai")
EX1010	Chinese Patent No. CN112635591A to Tong et al. ("Tong")
EX1011	Taiwan Patent No. TWI589655B to Zhang et al. ("Zhang")
EX1012	Basu, P.K. et al. (2015), The effect of front pyramid heights on the efficiency of homogeneously textured inline-diffused screen-printed monocrystalline silicon wafer solar cells, <i>Renewable Energy</i> , 78, (590-598). http://dx.doi.org/10.1016/j.renene.2015.01.058 ("Basu Paper")
EX1013	Guan, L. et al. (2019), Double-sided pyramid texturing design to reduce the light escape of ultrathin crystalline silicon solar cells, <i>Optics and Laser Technology</i> , 120, (1-7). https://doi.org/10.1016/j.optlastec.2019.105700 ("Guan Paper")
EX1014	Lozach M. et al. (2020), Role of silicon surface polished <100> and <111> or textured on the efficiency of double-sided TOPCon solar

	cells, <i>Progress in Photovoltaics</i> 28, (1001-1011). https://onlinelibrary.wiley.com/doi/abs/10.1002/pip.3304 (“Lozach Book”)
EX1015	Arvind Shah, Solar Cells and Modules, Spring Series in Materials Science Vol. 301 (2020) (“Shah Book”)
EX1016	Yu, et al. (2021). Selective tunnel oxide passivated contact on the emitter of large-size N-type TOPCon bifacial solar cells. <i>Journal of Alloys and Compounds</i> , 870, 159679-686. (“Yu”)
EX1017	Chinese Patent No. CN113193074A to Du et al. (“Du”)
EX1018	File History of ’136 Patent
EX1019	Claim listing for 136 Patent
EX1020	Librarian Declaration
EX1021	Exhibit 2 of Patent Owner’s Complaint in SDTX-4:25-cv-05226
EX1022	U.S. Patent No. US20180277701A1 to Lenes et al. (“Lenes”)
EX1023	U.S. Patent No. US11456391B2 to Chang et at. (“Chang”)
EX1024	Kim, Y., Lee, H., & Park, J. (2008). Texturing of large area multi-crystalline silicon wafers through different chemical approaches for solar cell fabrication. <i>Solar Energy Materials & Solar Cells</i> , 92(9), 960-964. (“Kim-1 Paper”)
EX1025	Papet, P., et al. (2006). Pyramidal texturing of silicon solar cell with TMAH chemical anisotropic etching. <i>Solar Energy Materials and Solar Cells</i> , 90, 2319-2325. (“Papet Paper”).

EX1026	Kim, H., et al. "Effect of Surface Treatment by Chemical-Mechanical Polishing for Transparent Electrode of Perovskite Solar Cells." <i>Energies</i> , vol. 13, no. 585, 2020. ("Kim-2 Paper")
EX1027	Le, Jianbo, et al. "Mechanisms of Surface and Subsurface Damage of Silicon Wafers Induced by External Stress During Nano-Polishing" <i>Ceramics International</i> , 2025. ("Le Paper")
EX1028	Li, Yiwei, et al. "The Effect of Chemical Polishing Treatment on the Microstructure and Photoelectric Properties of CdZnTe Polycrystalline Films." 2021. ("Li Paper")
EX1029	Chinese Patent No. CN109802007B to Zeng et al. ("Zeng")
EX1030	K. A.W. Horowitz et al., <i>A Techno-Economic Analysis and Cost Reduction Roadmap for III-V Solar Cells</i> , NREL/TP-6A20-72103 (Nat'l Renewable Energy Lab'y, Nov. 2018) ("Horowitz Report")
EX1031	B. G. Priyadarshini et al., <i>Design of Multi-Layer Anti-Reflection Coating for Terrestrial Solar Panel Glass</i> , 39 Bull. Mater. Sci. 683 (June 2016) (Priyadarshini Paper)
EX1032	J.-Q. Xi et al., <i>Optical Thin-Film Materials with Low Refractive Index for Broadband Elimination of Fresnel Reflection</i> , 1 Nature Photonics 176 (Mar. 1, 2007) ("Xi Paper")
EX1033	Panadyne, <i>Silicon Nitride Technical Data</i> (2026), https://panadyne.com/silicon-nitride-technical-data/ .
EX1034	U.S. Patent Publication No. 20200212242A1 to Fang et al. ("Fang")
EX1035	Richter, et al (2017). n-Type Si solar cells with passivating electron contact: Identifying sources for efficiency limitations by wafer

	thickness and resistivity variation. <i>Solar Energy Materials and Solar Cells</i> , 173, 96-105. (“Richter”)
EX1036	Chinese Patent No. 111640824_MT to Shen et al., (from Orbit) (“Shen”)
EX1037	T. S. Eriksson et al., <i>Infrared optical properties of evaporated alumina films</i> , 20 Appl. Opt. 2742 (1981). (“Ericksson Paper”)
EX1038	F. Rebib et al., <i>Determination of Optical Properties of a-SiOxNy Thin Films by Ellipsometric and UV-Visible Spectroscopies</i> , 100 J. Physics: Conf. Series 082033 (2008). (“Rebib Paper”)
EX1040	Xie et al., <i>High Efficiency Chemical Mechanical Polishing for Silicon Wafers Using a Developed Slurry</i> , 38 Surfaces & Interfaces 102833 (2023) (“Xie Paper”)

All citations to exhibits reference original page numbers found in the underlying document, and all emphases are added.

VI. SUMMARY OF CONCLUSIONS AND GROUNDS FOR CHALLENGE

21. After reviewing the materials identified in the List of Exhibits, I have concluded that each of the Challenged Claims of the ’136 Patent would have been obvious to a person of ordinary skill in the art, based on the following grounds.

Ground	Type	Summary
1	§103	Claims 1, 3, 5-7, 9, 12, 13, 15, and 17-19 are rendered obvious by Ye in view of <i>Basu</i>
1A	§103	Claims 1-3, 5-9, 12-15, and 17-20 are rendered obvious by Ye in view of <i>Basu</i> and <i>Yun</i>

2	§103	Claims 2, 5, 6, 14, 17, and 18 are rendered obvious by <i>Ye</i> in view of <i>Basu</i> and <i>Xia</i>
3	§103	Claims 7, 9, and 19 are rendered obvious by <i>Ye</i> in view of <i>Basu</i> and <i>Chang</i>
3A	§103	Claims 7, 9, and 19 are rendered obvious by <i>Ye</i> in view of <i>Basu</i> , <i>Yun</i> , and <i>Chang</i>
4	§103	Claim 10 is rendered obvious by <i>Ye</i> in view of <i>Basu</i> and <i>Yu</i>
4A	§103	Claim 10 is rendered obvious by <i>Ye</i> in view of <i>Basu</i> , <i>Yun</i> , and <i>Yu</i>
5	§103	Claim 11 is rendered obvious by <i>Ye</i> in view of <i>Basu</i> and <i>Fang</i>
5A	§103	Claim 11 is rendered obvious by <i>Ye</i> in view of <i>Basu</i> , <i>Yun</i> , and <i>Fang</i>
6	§§ 102 / 103	Claims 1, 3, 5-9, 12, 13, and 17-20 are anticipated and/or rendered obvious by <i>Sakai</i>
6A	§103	Claims 1-3, 5-9, 12-15, and 17-20 are rendered obvious by <i>Sakai</i> in view of <i>Yun</i>
7	§103	Claim 10 is rendered obvious by <i>Sakai</i> in view of <i>Yu</i>
7A	§103	Claim 10 is rendered obvious by <i>Sakai</i> in view of <i>Yun</i> and <i>Yu</i>
8	§103	Claim 11 is rendered obvious by <i>Sakai</i> in view of <i>Fang</i>
8A	§103	Claim 11 is rendered obvious by <i>Sakai</i> in view of <i>Yun</i> and <i>Fang</i>

VII. LEGAL STANDARDS

A. LEVEL OF ORDINARY SKILL IN THE ART

22. When interpreting a patent, I understand that it is important to identify the relevant art pertaining to the patent-in-suit as well as the level of ordinary skill in that art at the time of the claimed invention. The “art” is the field of technology to which the patent is related.

23. I have been instructed by counsel that the person of ordinary skill in the art is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor’s skill is not determinative of the level of ordinary skill. I further understand that the factors that may be considered in determining the level of skill include: the types of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or more of them may predominate.

B. LEGAL STANDARD FOR CLAIM CONSTRUCTION

24. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a POSITA would have understood the claim terms.

25. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim. I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

26. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the “Phillips standard.” I understand that this means that claim terms of a patent are given the meaning the terms would have to a POSITA, in view of the description provided in the patent itself and the patent’s file history.

27. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent, and the patent’s prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution

history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

28. I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the patent and its prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

29. In comparing the claims of the Challenged Patent to the prior art, I have considered the Challenged Patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

C. ANTICIPATION AND DISCLOSURE

30. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in a single prior art reference or system. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference, and that it would have been so recognized by a POSITA. In addition, I understand that an enabling disclosure is

a disclosure that allows a POSITA to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

31. I understand that U.S. patent law provides that a claimed numerical range may be anticipated or disclosed by a prior art reference in several circumstances. In particular, it is my understanding that:

- a. A prior art reference expressly discloses a range that overlaps or touches the claimed range may anticipate the claimed range. When a reference describes a numerical range that overlaps with, fully encompasses, or even meets the boundaries of a claimed range, the law treats that disclosure as anticipating the claimed range unless the patentee demonstrates that the claimed portion of the range is critical or yields unexpected results.
- b. A prior art reference disclosing a point within the claimed range or a range that is fully within the claimed range also anticipates the entire claimed range. A single embodiment or value falling inside the claimed range constitutes a disclosure of that range for purposes of anticipation.

- c. An overlapping prior art range creates a presumption of anticipation, and it is my understanding that the burden rests on the patentee to rebut that presumption by showing that the subset of the range claimed in the patent is critical to achieving a particular result, or that the prior art teaches away from operating in the claimed portion of the range.

32. It is further my understanding that the law does not require the prior art to recognize or explain the significance of the disclosed range. A reference may anticipate even if it does not identify the criticality or advantage of the disclosed values.

D. OBVIOUSNESS

33. I understand that the prior art may render a patent claim “obvious.” I understand that two or more prior art references (e.g., prior art articles, patents, or publications) that each disclose fewer than all elements of a patent claim may nevertheless be combined to render a patent claim obvious if the combination of the prior art collectively discloses all elements of the claim and one of ordinary skill in the art at the time would have been motivated to combine the prior art in such a way. I understand that this motivation to combine need not be explicit in any of the prior art but may be inferred from the knowledge of one of ordinary skill in the art at the time the patent was filed. I also understand that one of ordinary skill in the art is not an automaton but is a person having ordinary creativity. I further understand that one

or more prior art references, articles, patents or publications that disclose fewer than all of the elements of a patent claim may render a patent claim obvious if including the missing element would have been obvious to one of skill in the art (e.g., the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system).

34. I understand that under the doctrine of obviousness, a claim may be invalid if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA to which the subject matter pertains.

35. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any secondary considerations to the extent they exist.

36. I understand that any evidence of secondary indicia of non-obviousness should be considered when evaluating whether a claimed invention would have been obvious to one of ordinary skill at the time of invention. These secondary indicia of non-obviousness may include, for example:

- a long felt but unmet need in the prior art that was satisfied by the claimed invention;
- commercial success of processes claimed by the patent;
- unexpected results achieved by the invention;
- praise of the invention by others skilled in the art;

- the taking of licenses under the patent by others; and
- deliberate copying of the invention.

37. I understand that there must be a nexus between any such secondary indicia and the claimed invention.

38. It is also my understanding that there are additional considerations that may be used as further guidance as to when the above factors will result in a finding that a claim is obvious, including the following:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;
- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;
- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;
- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a POSITA;
- there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent’s claims; and

- there is some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed subject matter.

39. I further understand that optimizing known, result-effective variables is ordinarily considered routine experimentation. Where the prior art identifies a parameter, variable, or quantitative range as affecting the outcome of a system, adjusting that parameter to achieve improved or desired performance is considered within the predictable skill of a POSITA.

40. I also understand that a POSITA is not an automaton but rather someone with ordinary creativity, capable of applying routine engineering judgment. Thus, where the prior art teaches (1) the variable, (2) that the variable affects system performance, and (3) a finite and predictable set of options for adjustment, the optimization of the numerical value or range would have been obvious to a POSITA through routine experimentation.

41. Further, selecting narrower or preferred values within a disclosed range, including adjusting parameters such as thickness, size, or other scalar process variables is typically considered obvious when the prior art teaches workable broader ranges and identifies the variable as influencing results.

42. Yet further, I understand that obviousness may be established based on a single prior art reference where any missing claim elements would have been

supplied by the general knowledge or common sense of a POSITA, including the routine ability to optimize a known result-effective variable.

43. Finally, I understand that a claim may be deemed invalid for obviousness in light of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art.

VIII. OVERVIEW OF THE CHALLENGED PATENT

44. I have reviewed U.S. Patent No. 11,824,136 (“the ’136 Patent”), which is entitled “Solar Cell Manufacturing Method Thereof, and Photovoltaic Module.” Ex. 1001. I understand that the ’136 Patent was filed on October 12, 2022, and that it was issued on November 21, 2023. The application that issued as the ’136 Patent issued from a divisional application of U.S. Patent App. No. 17/459,689, filed on August 27, 2021, which claims priority to a Chinese patent application 202110895225.8 filed on August 4, 2021. Accordingly, I have been asked to assume that the ’136 Patent has a priority date no earlier than August 4, 2021.

A. THE SUBJECT MATTER OF THE CHALLENGED PATENT

45. The ’136 Patent relates to solar cells used for converting light to electricity. EX1001, 1:15-17. As the ’136 Patent describes, solar cells are a type of semiconductor device that are manufactured by forming PN junctions and other functional layers through dopant diffusion in silicon, and etching the silicon wafer

to create surface textures. *Id.*, 5:54-60; 6:4-14. One or both surfaces of the solar cell can be textured in order to reduce light reflection and improve light-conversion efficiency. *Id.*, 6:29-34.

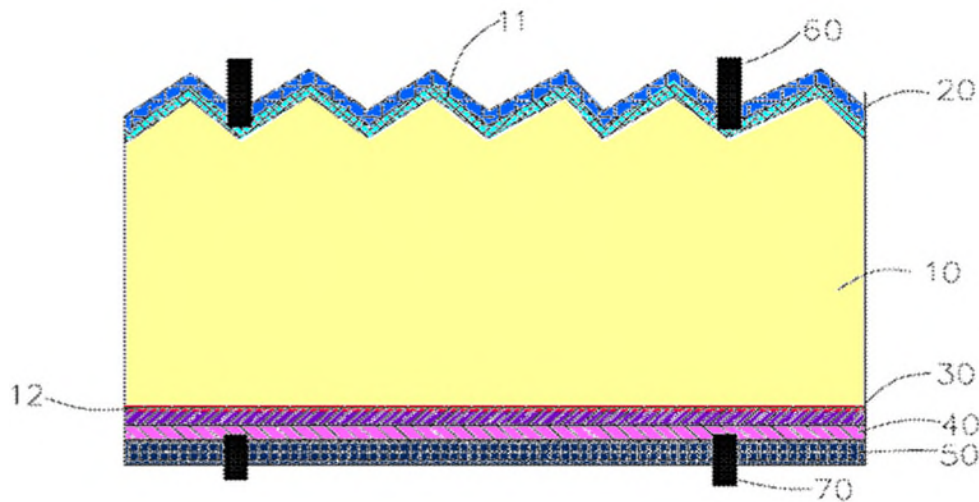
46. The claimed solar cells have textures on both front and rear surfaces of the substrate. *Id.*, Claim 1; FIGS. 1-2. The rear surface has non-pyramid texture structures with a maximum one-dimensional size of the first substructure of 45 μm . *Id.* The front surface of the substrate has pyramid-shaped texture structures with a maximum pyramid height of 5 μm . *Id.* The solar cell further has a passivation layer on the pyramid-shaped texture structures of the substrate. *Id.* The rear surface has a tunnel oxide layer (on the non-pyramid texture structures), a doped conductive layer (on the tunnel oxide layer), and a passivation layer (on the doped conductive layer). *Id.*

47. Surfaces and layers of the claimed solar cells are listed below and colored in Figure 1:

- a semiconductor silicon substrate 10 (yellow) (claim 1[a])
- a rear substrate surface 12 with non-pyramid texture structures (red) (claim 1[b])
- a front substrate surface 11 with pyramid texture structures (light blue) (claim 1[c])
- a passivation layer 20 (blue) on the pyramid texture structures of the

front substrate surface (claim 1[e])

- a tunnel oxide layer 30 (purple) on the non-pyramid texture structures of the rear substrate surface (claim 1[f])
- a doped conductive layer 40 (pink) on the tunnel oxide layer of the rear surface (claim 1[g])
- a passivation layer 50 (dark blue) on the doped conductive layer of the rear surface (claim 1[h])



Id., 5:20-6:3 and FIG. 1 (annotated). As discussed in the '136 Patent's background section, the tunnel oxide layer is a feature of an "N-type tunnel oxide passivated contact (TOPCon) solar cell," which was known in the art before the '136 Patent. *Id.*, 1:21-24.

48. Figure 2 is an image looking downward on the front-side pyramid texture structures, and Figure 3 is an image looking downward on the rear-side non-pyramid texture structure. The '136 Patent specification describes that the non-pyramid

texture structures are made by polishing the rear surface with an alkali solution. *Id.*, 7:38-40. It states that the non-pyramid texture structures have “polygonal” top surfaces with a maximum size of 45 μm and some of the non-pyramid structures are at least partially “stacked” on one another. *Id.*, 1:50-59; FIG. 3.

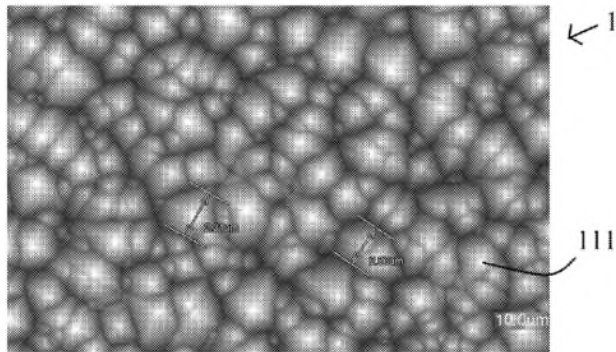


FIG. 2

Front Side

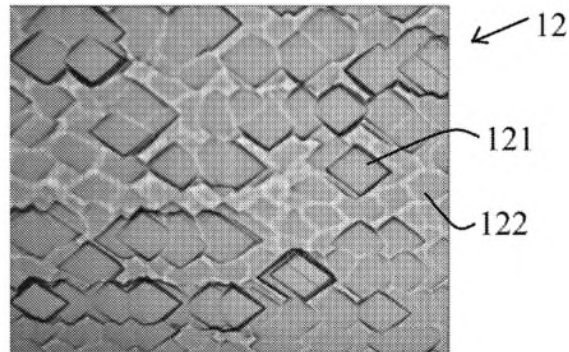


FIG. 3

Rear Side

49. The independent Claims of the '136 Patent recite a single solar cell (Claim 1) and a photovoltaic module with two or more solar cells (Claim 13), but both recite the same layer-structure illustrated in FIG. 1. *Id.* Dependent claims 2-12 and 14-20 each specify details of one or more layers of the solar cell. *Id.*

50. As demonstrated herein, all features of the Challenged Claims, including the design considerations and purported advantages described in the '136 Patent, were well known at the time the application leading to the '136 Patent was filed.

B. LEVEL OF ORDINARY SKILL IN THE ART

51. As of the earliest claimed priority date, it is my opinion that a person of ordinary skill in the art (“POSITA”) relating to the ’136 Patent would have at least a person of ordinary skill in the art (“POSITA”) would have at least bachelor's degree in electrical engineering, applied physics, materials science, or a related discipline and at least two years of experience designing, developing, or researching the design and/or manufacture of solar cells or related technologies. This definition is approximate, and more education may substitute for industry experience or vice versa. As of the priority date of the ’136 Patent, I possessed at least the level of skill of a POSITA under this definition.

52. As discussed below, it is my opinion that a POSITA as defined above would have deemed the subject matter of the ’136 Patent’s claims obvious in light of the prior art and a POSITA’s knowledge at the time of the ’136 Patent’s priority date. It may be that persons having different levels or types of education, skill, and/or experience in the relevant art at that time also may have found the subject matter of the ’136 Patent’s claims obvious. I reserve the right to amend or supplement my opinions if Patent Owner disputes the qualifications of a POSITA stated above or presents different qualifications for a POSITA in this matter.

C. PROSECUTION HISTORY

53. The application that issued as the '136 Patent was filed on October 12, 2022, as a divisional application of U.S. Patent Application No. 17,459,689, filed on August 27, 2021 and claiming priority to a Chinese Patent Application No. 20211089522.8, filed on August 4, 2021. EX1001. The '136 Patent's prosecution was short. *See generally* EX1018. In the two non-final Office Actions, the only rejections were based on double-patenting and there was no prior-art-based rejection. *See* EX1018; EX1019.

54. The Examiner issued a Notice of Allowance on August 30, 2023, citing WO2016/129481A1 to *Sakai* as the closest prior art in the reasons for allowance. In particular, the Examiner found that *Sakai* disclosed a solar cell (claim 1[p]) with a substrate (claim 1[a]) having the claimed tunnel oxide layer (claim 1[f]), passivation layers (claim 1[e] and 1[h]), and doped semiconductor layer (claim 1[g]). EX1018, 12-17. The Examiner also noted that *Sakai* disclosed textured structures on the rear and light receiving surfaces, including pyramid and "truncated four-sided pyramidal" texture structures with a size of less than 15 micrometers," as recited in claims 1[b] and 1[c]. However, the Examiner asserted that *Sakai* "does not clearly show among the overlapping unevenness about the distance of the top face of an outermost protruding part, and the top face of the protruding part which adjoins it." EX1018, 15-16. The '136 Patent issued on November 21, 2023.

**D. COMPARISON OF ASSERTED REFERENCES TO PRIOR ART DISCUSSED
DURING PROSECUTION**

55. I have been asked to review the examination history of the '136 Patent, and to compare the prior art grounds presented herein to those considered in rejections by the Examiner during the examination of the '136 Patent. As I describe below, my opinion is that the Grounds of invalidity considered herein are not cumulative of the prior art considered by the Examiner during examination.

E. CLAIM CONSTRUCTION OF THE '136 PATENT

56. For purposes of my analysis of the '136 Patent claims, I have applied the ordinary and accepted meaning of the claim language as a POSITA would have understood the claim language. However, I understand that certain terms in those claims may require construction under the applicable law.

IX. TECHNOLOGY BACKGROUND AND STATE OF THE ART

57. In the subsections below, I describe some of the basic principles of engineering that would be used, or at least considered for use, in the field of design and manufacturing of solar cells. The principles discussed in the subsections below would have been well-known to a POSITA in the August 2021 timeframe, and many of them long before that.

A. SOLAR CELLS GENERALLY

58. Solar cells capture the energy of sunlight. When a photon impinges upon a solar cell, it may separate an electron from the remainder of an atom. This creates a floating electron (negatively charged) and a floating hole (positively charged). If the electron and hole are collected by emitters before combining, a voltage difference can be achieved, thereby permitting electric current flow.

59. In order to capture significant amounts of sunlight, typical solar installations cover many square feet, such as 100 or 1,000 square feet. Since the silicon wafer sizes are significantly less than a square foot, multiple solar cells are electrically connected into strings, which are then assembled into array-shaped modules. *See, e.g.*, EX1015 at 115, 219-223.



Fig. 9.1 c-Si solar cells with (from the top left) two (2BB), three (3BB), five (5BB) busbar and cell without busbars (below right). Current-collecting fingers are placed perpendicular to the busbars

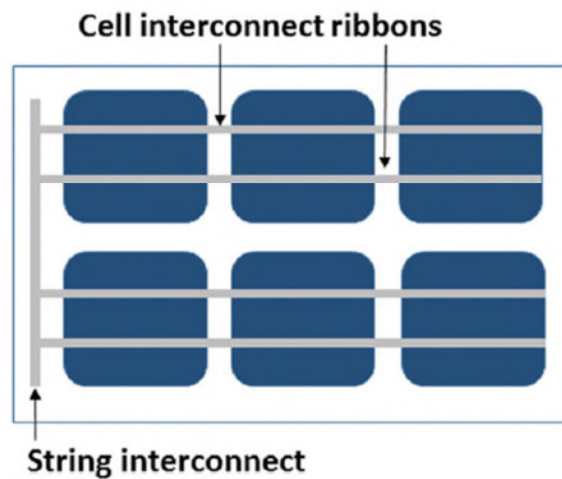


Fig. 9.2 Simplified sketch of a solar module with two-busbar (2BB) cells. *Cell interconnect ribbons* and *string interconnects* are shown. *Busbars* are hidden below the ribbons

One example of a module may consist of 8×8 silicon solar cells, each cell having a diameter of 200 mm. Modules, which are designed to include a mechanical support frame for structural integrity, can be mounted in appropriate locations such as the roofs of residential buildings.

60. There are multiple types of solar cell architectures. One of them is the PERC solar cell or Passivated Emitter and Rear Contact (PERC) solar cell. A PERC (Passivated Emitter and Rear Contact) solar cell is an advanced silicon solar cell that adds a transparent dielectric passivation layer and local small-area ohmic contacts to the back side of the solar cell. The dielectric is covered by a blanket metal layer acting like a mirror to reflect unabsorbed sunlight back into the silicon wafer for a second absorption chance, significantly boosting efficiency, reducing electron loss, and improving performance, making it an industry standard for solar cells with a higher energy yield.

61. Another advanced solar cell architecture is the TOPCon architecture. Tunneling oxide passivation contact (TOPCon) solar cells employ an ohmic contact structure that is characterized by a thin oxide layer (e.g., an SiO₂ layer) that is thin enough to be tunneled through by charge carriers (electrons and holes), so that an ohmic contact is achieved, yet thick enough to passivate the silicon surface so as to reduce unwanted electron-hole surface re-combination. EX1015 at 130-136, 167-168. A typical thickness for a tunneling oxide passivation (TOP) layer is about 1 to 2 nm thick. See EX1015 at 134 (“One uses a 'sandwich structure' consisting of a SiO₂ layer of approximately 2 nm thickness and a strongly n-doped polycrystalline layer (n⁺-poly-Si) to form the contact... The additional tunnel oxide, with a thickness of approximately 2 nm, takes over the high charge carrier-selective current

conduction via the tunnel effect.”); *See also*, Sakai at 0041-0042 (“the passivation film 3 has a film thickness that allows carriers (electrons and holes) to tunnel ... the film thickness of the passivation film 3 is set to 2 nm.”) The TOP layer is covered by a conductive semiconductor layer, typically N-type or P-type polycrystalline silicon. The TOPCon solar cell architecture is characterized by high efficiencies, for example, 25% as compared to typical PERC solar cells.

B. MANUFACTURING OF SOLAR CELLS

62. The base material for the substrate of a high-quality solar cells is single-crystal silicon with silicon wafers sizes of about 200 mm (e.g. the 182 mm (M10) and 210 mm (G12) format). Polycrystalline silicon solar cells feature much shorter minority carrier lifetimes and lower efficiencies, and for this reason are only rarely used for solar cell applications. Furthermore, whereas other solar cell materials, such as GaAs or CdZnTe, are available, their efficiencies are significantly lower than those of single-crystal silicon solar cells. Accordingly, single-crystal silicon wafers are a viable and preferred choice for substrates for efficient solar cells.

63. During solar cell manufacturing, various thin films are deposited on the silicon wafer. This includes passivation layers, tunnel oxide layers, and conductive layers.

64. Passivation layers are used in both PERC and TOPCon solar cells, and can perform several different functions in the solar cell. Passivation layers can

chemically passivate the solar cell surface so that it resists oxidation and corrosion for years. Passivation layers can also electrically de-activate (passivate) electronic surface states through which undesired electron-hole recombination occurs. Finally, passivation layers can serve as optical anti-reflection layers (and are sometimes interchangeably referred to as anti-reflective coatings or “ARCs”) that make incident light enter the silicon solar cell rather than being reflected. Dielectric optically transparent layers such as SiO₂, Al₂O₃, MgF₂, Si₃N₄, and SiON are common passivation layers and ARCs. *See* EX1024 at 967 (“SiN_x film as AR coating as well as a surface passivation layer plays an important role in commercial mc-Si solar cells”); EX1025 at 2326 (“In photovoltaic industries, SiN_x:H ARC is often deposited after texturing in order to increase light collection and to passivate silicon surface”); Shah at 78-82 (discussing silicon nitride) and 166-167 (discussing aluminum oxide). They can be deposited by chemical vapor deposition (CVD) which is a typical method of deposition.

65. Tunnel oxide passivation (TOP) layers are part of the advanced electrical contact structure of a TOPCon cell with the TOP layer being located between the silicon semiconductor and a conductive contact layer. The TOP layer has the purpose of electronically passivating interface states that naturally occur at a conventional metal-semiconductor interface. Inserting a thin TOP layer passivates (de-activates) these interface states so that detrimental electron-hole interface recombination is

avoided. However, if the TOP layer is too thick, the contact resistance increases. Therefore, a well-accepted thickness range for the TOP layer is 1 to 2 nm. SiO₂ is a preferred material for the TOP layer because of its favorable passivation characteristics for silicon surfaces. Other materials, such as Al₂O₃ can be suitable as well. Native oxide (SiO₂) TOP layers can be grown by exposing the silicon surface to an oxidizing ambient, such as air or oxygen (e.g. in a furnace). Alternatively, top layers can be deposited by a thin-film deposition technique such as CVD.

66. Conductive layers are used in both PERC and TOPCon solar cells to complete the electrical contact of the solar cell. In a TOPCon cell, a conductive layer is deposited onto the TOP layer. To promote low resistivity contacts, an n-type and p-type conductive layer is deposited for n-type and p-type contacts, respectively. Doped poly-silicon (n-type or p-type) is the material of choice for these conductive layers. A common deposition technique for these conductive layers is CVD.

67. One or more surfaces of the substrate wafer are typically processed to form a texture on the surface, among other reasons, to improve the amount of light trapped by the solar cell. Various techniques for forming textured surfaces were known to POSITAs and routinely used in solar cell manufacturing, including chemical mechanical polishing techniques and chemical etching techniques. Wet chemically etching of (001) silicon surfaces in an alkaline solution containing KOH

or NaOH is a known method for creating textured silicon surfaces whose microstructure consists of micro-pyramids. The pyramids typically have a tetragonal (square) base and four slanted sidewalls forming a tip at the top. The base angles have been established to be close to 55° and about 70° at the top (when measured along the middle symmetry line of the pyramid), as determined by crystal symmetry. The sum of the two base angles plus the top angle is $55^\circ + 55^\circ + 70^\circ = 180^\circ$ as required for the cross-sectional triangle of the pyramid. Calling the half-diameter of the pyramid its radius r , and denoting its height by h , the following trigonometric relation can be written: $h / r = \tan 55^\circ$. For example, a pyramid with a radius of $4 \mu\text{m}$ has a height of $h = 4 \mu\text{m} \times \tan 55^\circ = 5.7 \mu\text{m}$.

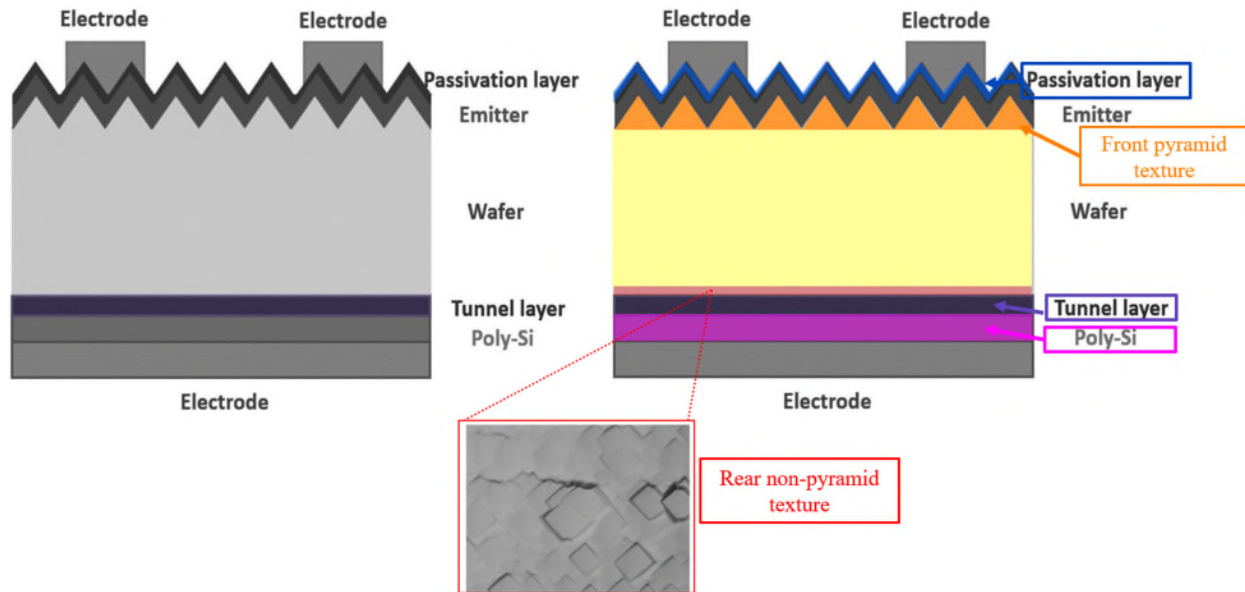
68. Whereas KOH and NaOH solutions are known as anisotropic etching solutions (driven by crystal symmetry), other wet chemistries result in isotropic material removal that do not result in textured surfaces. In addition, polishing interactions using a slurry can result on a variety of surfaces that range from textured (pyramidal) to flat (non-pyramidal) as well as anything in between.

X. OVERVIEW OF THE PRIOR ART¹

A. YE (EX1004)

69. Ye relates to a method of manufacturing TOPCon solar cells. EX1004 ¶¶0003-0004, 0018. Ye's solar cells have texture surfaces on both the front and rear sides of a silicon wafer. *Id.* The front side includes a textured surface with pyramid-shaped substructures (in orange below) and a passivation layer (in blue below). *Id.*, Figure 1. The rear surface of the substrate (in red below) has non-pyramid-shaped textures. *Id.*, Figure 3. The rear side further has the following series of layers: a tunnel oxide layer ("tunnel layer") on the non-pyramid textured surface, a doped conductive layer ("Poly-Si") on the tunnel oxide layer, and another passivation layer on the doped conductive layer. *See e.g., Id.* ¶0038; Figure 1; Claim 1.

¹ Original references for EX1004, EX1005, EX1006 and EX1009 are in Chinese or Japanese; certified English translations are appended thereto.



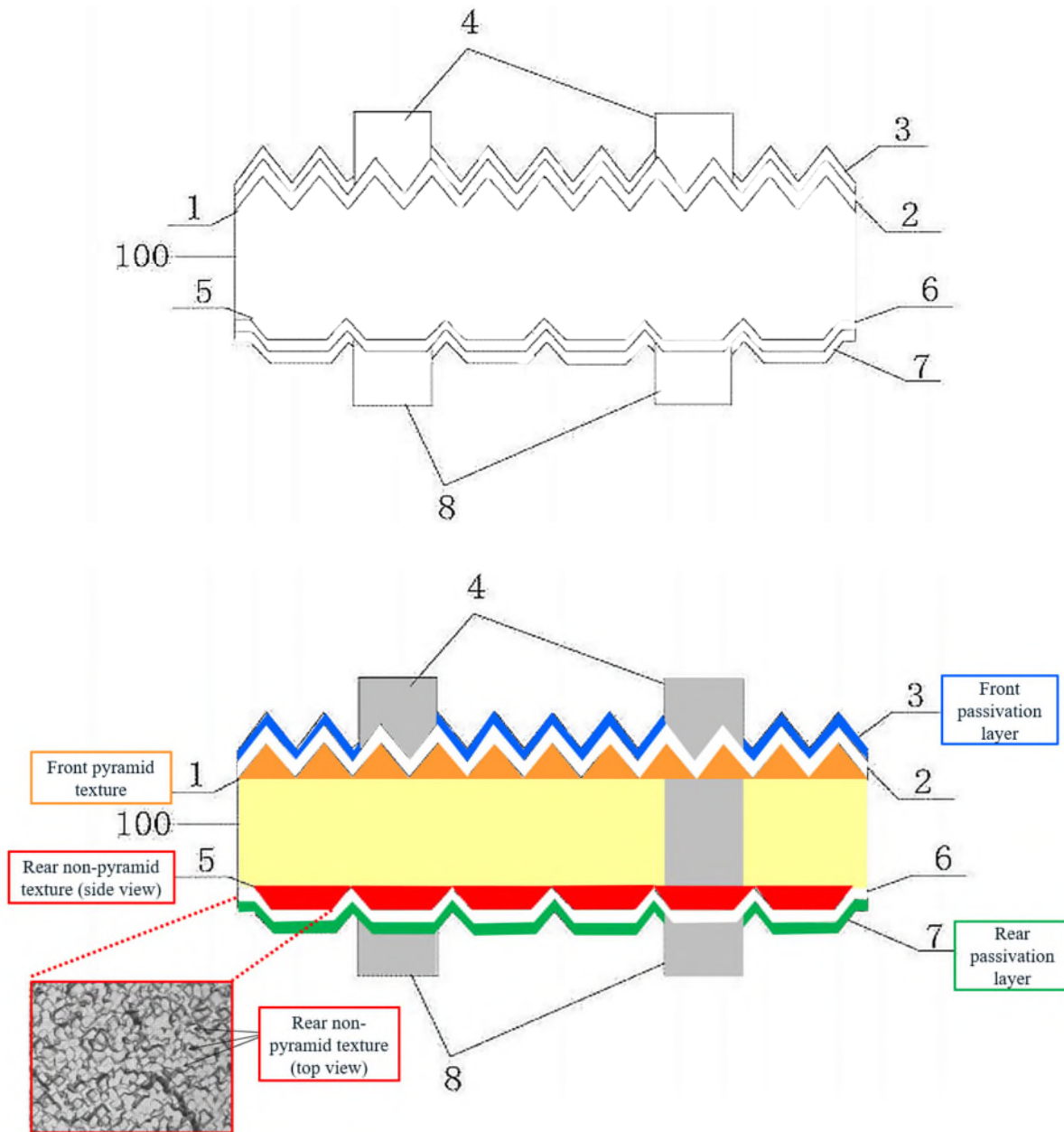
EX1004 (annotated).

70. Figure 3 shows the non-pyramid texture of the rear surface next to the tunnel oxide layer. The non-pyramid structures have polygonal top surfaces. *Id. Ye* was not of record during the '136 Patent's prosecution.

B. YUN (EX1005)

71. *Yun* relates to a bifacial solar cell made of monocrystalline silicon. EX1005, Abstract; Claim 1; Figure 1. *Yun*'s solar cells use both front and back surfaces of a substrate 100 to receive light and both surfaces are textured. *Id.* ¶0002. As shown in Figure 1, the front side has pyramid-shaped textures 1 on the substrate surface (in dark yellow below) and a front passivation layer 3 (in blue below). *Id.* ¶0029, 0034. The rear side has non-pyramid "platform-shaped" shaped surface textures (in orange below) that have an upper planar surface with a maximum side

length of 10 μm . *Id.* ¶¶0029, 0032; Abstract; Figure 1. The rear side further has a passivation layer 7 (in dark blue below) on the non-pyramid texture. *Id.*, Figure 1.



EX1005, Figure 1 (annotated) and 2.

72. Figure 2 shows that the “platform-shaped” structures (i.e., non-pyramid textures) have polygonal top surfaces, which have a maximum side length of 10 μm .

Id., Figure 2, Claim 1. The platform-shaped structures can be dispersed or partially overlapping. *Id. Yun* was not of record during the '136 Patent's prosecution.

C. BASU PAPER (EX1012)

73. *Basu Paper* is a published scientific paper that relates to optimizing pyramid structures formed on the surfaces of monocrystalline silicon wafer solar cells. EX1012, 590. *Basu Paper* describes the effect of pyramid heights on the efficiency of the solar cells. *Id. Basu Paper* studies various ranges of pyramid heights of the surface textures formed using alkaline texture processes, and concludes that the smaller pyramids (i.e., $\sim 5\ \mu\text{m}$ maximum among the ranges studied) give the highest fill factor and hence efficiency. *Id.*, 597.

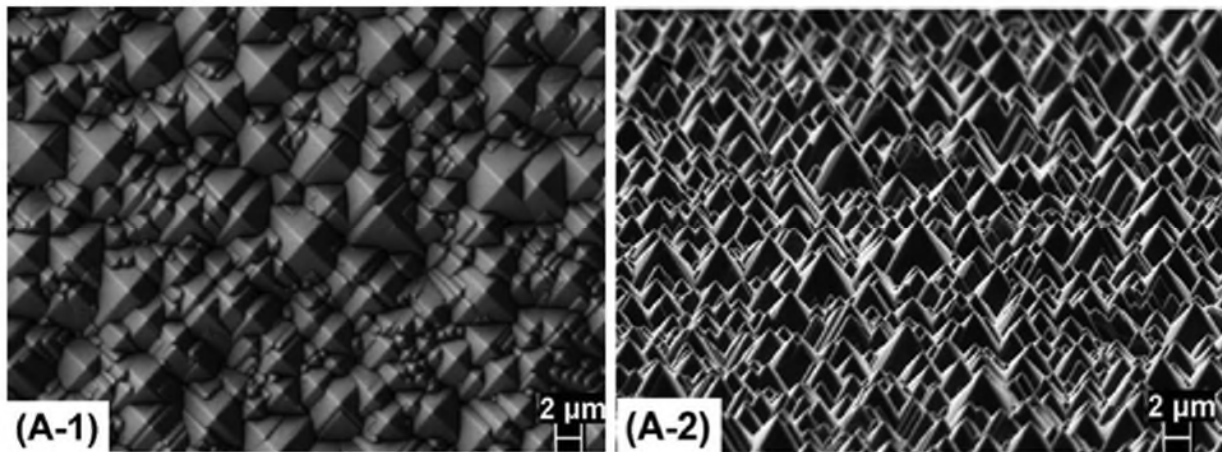


Fig. 4 (A-1) (top view)

Fig. 4 (A-2) (angular view)

EX1012, Fig. 4.

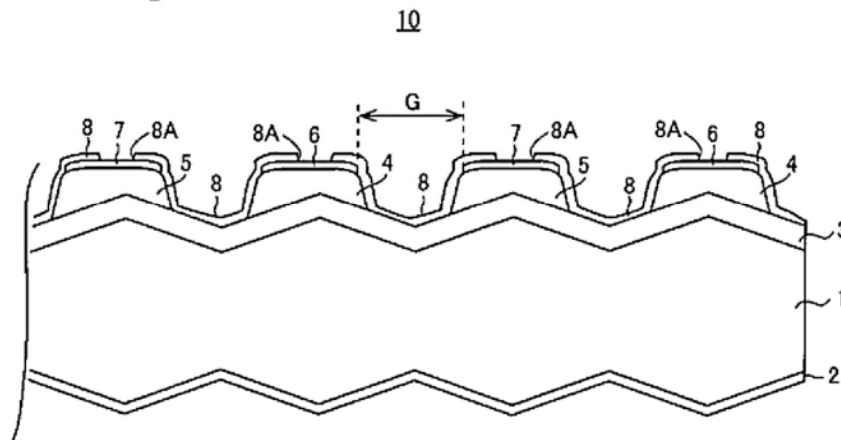
74. Figure 4 (A-1) shows a top view SEM micrographs of pyramid textures with a maximum height of $5\ \mu\text{m}$; Figure 4 (A-2) shows an angular view of the

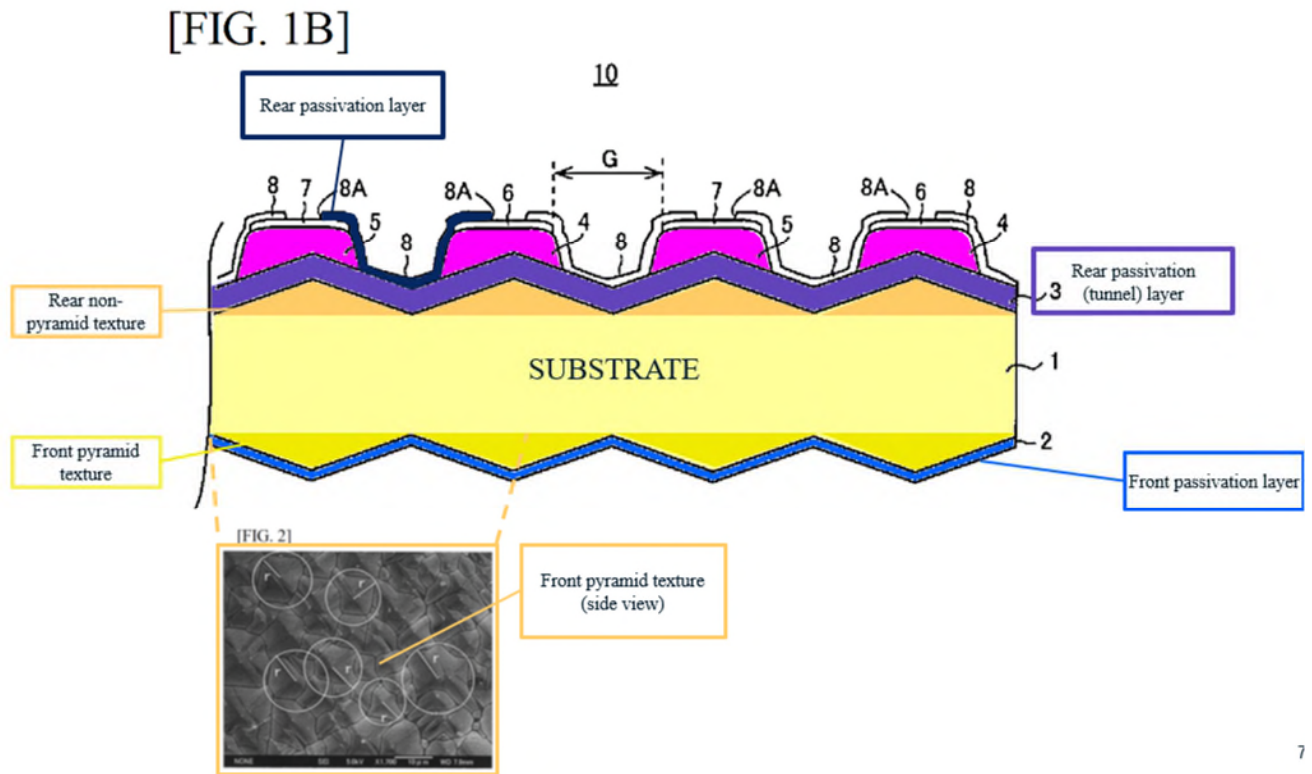
pyramid textures. *Id.*, Fig. 4. *Basu* Paper was not of record during the '136 Patent's prosecution.

D. SAKAI (EX1009)

75. *Sakai* relates to a TOPCon solar cell (*i.e.*, photoelectric conversion element) with textured front and rear substrate surfaces. EX1009. As shown in Figure 1B, the front texture (in dark yellow below) and rear texture (in orange below) of the substrate are made by etching on a silicon substrate and can be pyramid-shaped (FIG. 2) or truncated pyramid-shaped (not shown). *Id.*, ¶0045.

[FIG. 1B]





7

EX1012, FIGS. 1B (annotated) and 2; see *id.* [0042].

76. The texture structure has a convex portion with a size equivalent to a circumscribed circle with a diameter of less than 15 μm . *Id.*, Claim 5. The textures have unevenness including overlapping portions. *Id.*, ¶0042. The pyramid heights are 1 μm or less. *Id.*, ¶0120. The front side of the solar cell has an antireflective passivating film 2 (in light blue above) on the front substrate texture. *Id.*, FIG. 1B. The back side of the solar cell has an oxide film 3 (in purple above) of a thickness that “allows carriers (electrons and holes) to tunnel.” *Id.*, [0042]; see also *id.*, [0159]. On top of film 3 are doped semiconductor layers 4 and 5 (in pink above) (*id.*, [0147])-

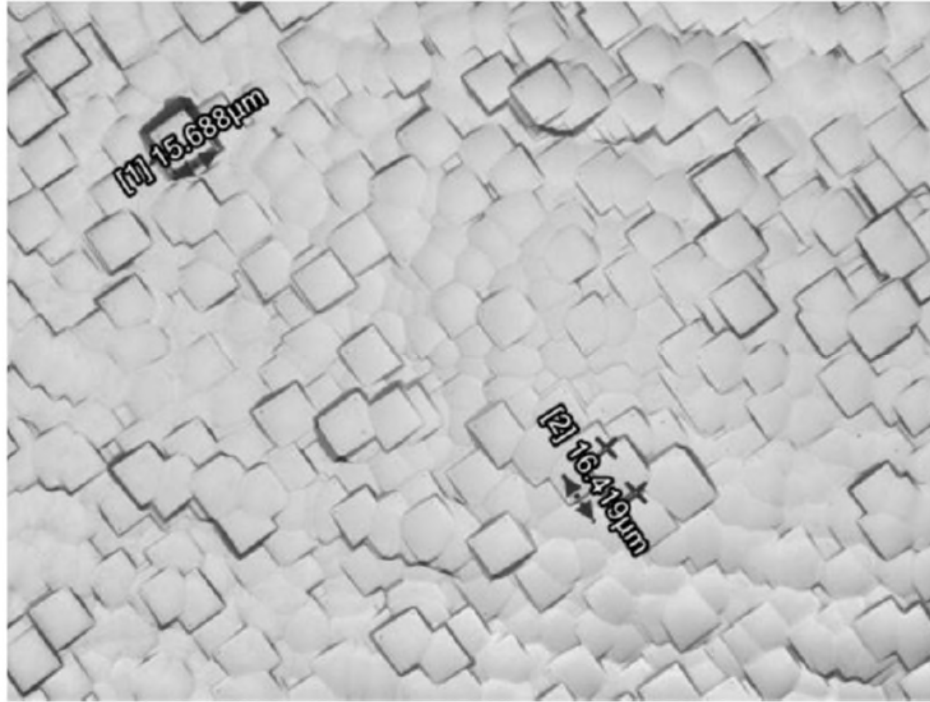
[0148]), followed by a protective film 8 (in dark blue above) that passivates the semiconductor layer 4 (*id.*, [0053], [0078]).

77. *Sakai* was mentioned in the Notice of Allowance of the '136 Patent as the closest prior art. EX1018, 16-17. However, the Examiner erred in distinguishing *Sakai* from the '136 Patent claims. The Examiner asserted that “*Sakai* does not clearly show among the overlapping unevenness about the distance of the top face of an outermost protruding part, and the top face of the protruding part which adjoins it.” *Id.* But the '136 Patent's independent claims do not recite any “distance of the top face of an outermost protruding part, and the top face of the protruding part which adjoins it.” It also is unclear whether the Examiner fully considered *Sakai*'s complete disclosure. *Sakai* was filed and published in Japanese and has no counterpart in any other country. The copy of *Sakai* in the '136 prosecution history only contains an English translation of its Abstract (EX1018, 302-391), which does not cover all of the disclosures of *Sakai* relied upon in this Petition, as noted throughout Sections 6, 6A, 7, 7A, 8, and 8A, *infra*. Nor is there any indication that the Examiner could read or comprehend *Sakai*'s technical subject matter in Japanese.

E. XIA (EX1006)

78. *Xia* relates to a method of polishing crystalline silicon surfaces for TOPCon solar cells. EX1006, ¶¶0001-0002. *Xia* discloses that the silicon wafers

typically have a surface roughness of about 10-20 μm and a pre-polishing step can reduce it to 1-3 μm . *Id.* ¶0007.



EX1006, Figure 1.

79. Figure 1 shows a microscopy image of the polished crystalline silicon surface on the rear side of the solar cell wafer, resulting from the polishing method in *Xia. Id.*, Figure 1. The polished surface has “uniform and smooth square structures” with approximately the same size of about 15 to 16 μm . *Id.* ¶0033.

F. CHANG (EX1023)

80. *Chang* teaches a solar cell having rear tunneling layers on a silicon substrate to enable passivation and carrier tunneling, specifying materials including silicon oxide, silicon nitride, and silicon oxynitride with a tunneling layer thickness

of about 0.5–2 nm. EX1023, 5:21-27, 5:30-34, 7:8-15. A rear polySi back surface field is formed on the tunneling layer. *Id.* The passivation/antireflective films may include dielectrics such as Al₂O₃, HfO₂, SiO_x, SiN_x, and SiON, and the tunneling layers can be formed by thermal growth, PECVD, or ALD. *Id.*, 5:21-27, 5:30-34, 6:30-37, 7:8-15.

G. YU PAPER (EX1016)

81. *Yu* is a published scientific paper that relates to improving tunnel oxide passivated contacts (TOPCon) in bifacial solar cells, and describes optimized designs for their front surfaces. EX1016 at 1. Figure 4 of *Yu Paper* is a diagram of the solar cells fabricated in its experiments.

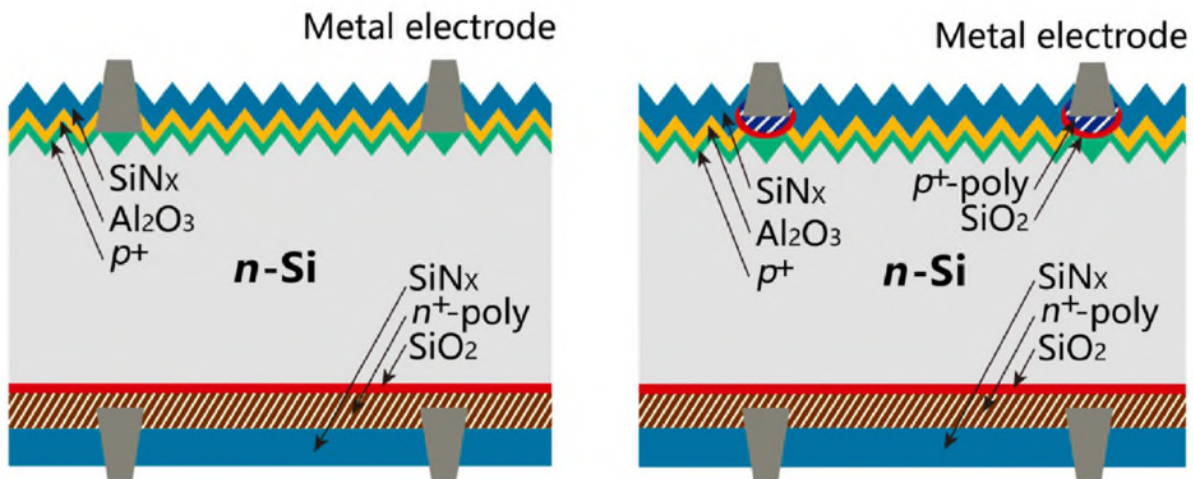


Fig. 4. Solar cell construction diagram.

EX1016, Figure 4.

Those cells include 5-nm aluminum oxide and a 75-nm silicon nitride passivation layers on the boron emitter on the substrate's front surface. *Id.*, 3.

H. FANG (EX1034)

82. *Fang* relates to PERC-type solar cells prepared using plasma enhanced chemical vapor deposition techniques to deposit composite passivation films on silicon wafers. EX1034, Abstract, [0068]. *Fang* describes various embodiments of composite passivation films 3 formed using its methods, which include 2-6 films or sublayers. *Id.*, Figs. 3-8, [0077]-[0084]. Each sublayer can be made of various materials, including aluminum oxide, silicon nitride, and silicon oxynitride, and *Fang* discloses thickness ranges for those sub-layers. *Id.*, [0085].

XI. GROUND 1: CLAIMS 1, 3, 5-7, 9, 12, 13, 15, AND 17-19 ARE RENDERED OBVIOUS BY YE IN VIEW OF BASU PAPER

A. RATIONALE FOR COMBINING YE AND BASU PAPER

83. The '136 Patent relates to the field of solar cells generally, and more specifically to optimizing solar cell design (*e.g.*, of TOPCon solar cells) to improve efficiency (*e.g.*, by using textured front and back surfaces). EX1001, 1:15-18, 1:41-46. *Ye* also relates to the field of solar cells, and more specifically to preparing a laminated thin-film tunneling oxide passivated (TOP) contact structure in a way that optimizes a solar cell's design and improves its quality (*e.g.*, by avoiding delamination). EX1004, ¶¶ 0001, 0008-0009. *Ye* specifically refers to TOPCon solar cells as an example of the type of solar cells improved by these optimizations.

EX1004, ¶ 0003-0008. Basu Paper also relates to the field of solar cells made from monocrystalline silicon wafers, and is directed to optimizing solar cell structure (e.g., pyramid height) to maximize the efficiency. EX1012 at 590. As such, *Ye* and Basu Paper both relate to the same field as the '136 Patent, and are therefore analogous art to each other and to the '136 Patent. EX1001, 1:41-46; 4:13-17; 5:44-55; EX1004, ¶¶ 0008-0009; EX1012 at 590.

84. Alternatively, the '136 Patent is concerned with the problem of optimizing the textured surfaces and other layers of solar cells to improve the cell's open-circuit voltage, reduce contact resistance of the cell's electrodes, and improve the cells' efficiency. EX1001, 1:40-47, 5:29-38. *Ye* and Basu Paper each teaches how to optimize the cell's textured surfaces and/or their adjacent layers to improve the efficiency, quality or reduce cost. EX1004, Abstract & [0022] (laminated thin film "maintains a relatively low sheet resistance, which is beneficial for metal contacting..." and "achieve[s] high open-circuit voltage"); EX1004 at 597. As such, *Ye* and Basu Paper both relate to problems with which the '136 Patent would have been concerned. Therefore, *Ye* and Basu Paper are analogous art to each other and to the '136 Patent.

85. *Ye* describes solar cells that have texture surfaces on both the front and rear sides. EX1004, Figure 1; Figure 3. The front surface texture has a pyramid shape, and the rear surface has a non-pyramid shape. *Id.* Basu Paper teaches that

solar cell efficiency can be maximized by choosing optimal pyramid heights for the front surface textures. EX1006 at 597. Basu Paper studies three ranges of pyramid heights (small: $\sim 5\ \mu\text{m}$, medium: $\sim 6\ \mu\text{m}$, and large $\sim 8\ \mu\text{m}$) of the surface textures, and concludes that the smaller pyramids (i.e., $\sim 5\ \mu\text{m}$ among the three ranges) give the highest fill factor and hence highest efficiency. *Id.* at 594, 597 (“The FF was found to decrease with increasing maximum pyramid heights within the variation studied here and smaller pyramids were found to give the highest FF and hence efficiency.”). A POSITA would have been motivated to use pyramids of the height range disclosed in Basu Paper as being most efficient (i.e., $\sim 5\ \mu\text{m}$ maximum, or 2-5 μm) for the front surface texture in *Ye* to further improve the solar cell efficiency. A POSITA would have had a reasonable expectation of success in adopting the pyramid heights disclosed in Basu Paper for the solar cells in *Ye*, because it merely optimizes the size of a known texture structure and shape (i.e., pyramids) of the solar cell within a known range of pyramid heights using a known method (Basu Paper’s optimal height of $\sim 5\ \mu\text{m}$) to obtain predictable results (improved efficiency). EX1006 at 597.

B. DISCLOSURE OF YE IN VIEW OF BASU PAPER

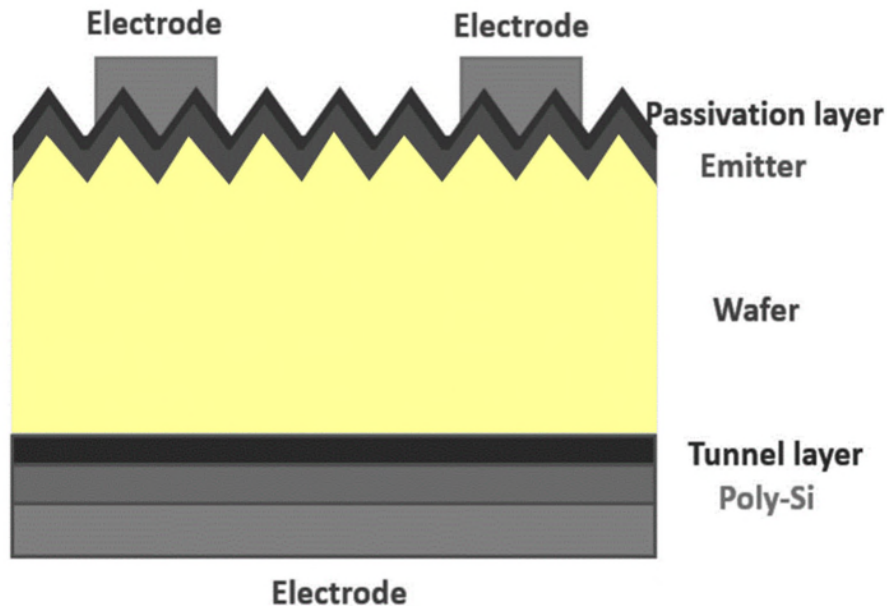
a. Claim 1

i. Claim 1[p]: “A solar cell, comprising:”

86. To the extent the preamble is limiting, Ye discloses various embodiments of “solar cells” with TOPCon structures. EX1004, ¶¶ 0001-0002; Figures 1; *see also id.*, 0018, 0020-0024, 0037-0038 (“The present invention relates to the technical fields of solar cells ...). Basu Paper also discloses the effect of the front pyramid height on the performance of “industrial monocrystalline silicon (c-Si) wafer solar cells.” EX1006 at 590, 597 (“In this work we report the impact of pyramid height on the performance of inline-diffused c-Si solar cell”).

ii. Claim 1[a]: “a semiconductor substrate,”

87. A POSITA would have understood that the “n-type silicon wafer” in Ye (e.g., illustrated in Figure 1) on which the silicon oxide layer grows is a semiconductor substrate. EX1004, Abstract, ¶¶ 0007, 0011, 0030-0032, 0038; Figure 1.



EX1004, Figure 1 (annotated).

88. Basu Paper also discloses solar cells formed from an “industrial monocrystalline silicon (c-Si) wafer”. POSITA would have understood that the monocrystalline silicon wafer is a semiconductor substrate. EX1006 at 590, 592.

- iii. **Claim 1[b]: “wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another, a top surface of the first substructure is a polygonal plane, and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ;**”

89. Ye discloses that the solar cell has a textured rear surface with non-pyramid-shaped substructures. EX1004, Figures 1, 2 and 3. Figure 3 shows a top

view of the top surface of those substructures, which appear as four-sided polygonal planar surfaces located on the rear surface of the solar cell. As shown in Figure 3, at least some adjacent texture substructures do not stack on one another. *Id.*

90. I assume for purposes of this proceeding that the claimed size limitation of “less than or equal to 45 μm ” refers to a non-zero size. Various prior art references, such as Basu Paper and Shah Book, show that this range of size was well known to a POSITA before the effective filing date of the ’136 Patent. For example, Basu Paper discloses that the front-side pyramid base dimension is less than 10 μm (see the microscopy images in Figures 4 and 5 of Basu Paper). Since the silicon front surface and back surface are crystallographically equivalent and indistinguishable (due to the well-known inversion symmetry of silicon), the rear-side polygons have approximately the same dimensions as the bases of the pyramids on the front side. As such, the rear-side polygonal substructures have about the same dimension of less than 10 μm , that is, less than 45 μm . Furthermore, Shah Book discloses a pyramid height of up to 7 μm (EX1015 at 85). With a typical pyramid apex angle of approximately 70.5° (*id.* at 86) and pyramid height of 7 μm , the pyramid base dimension, which is the maximum possible size of the polished top surface, is about 10 μm , which is less than 45 μm . As such, based on the typical size and scale of most TOPCon solar cells and the textured substructures formed on the substrates for

those solar cells, a POSITA would have recognized that the top surfaces of these substructures in Ye are smaller than 45 μm in any dimensional size.

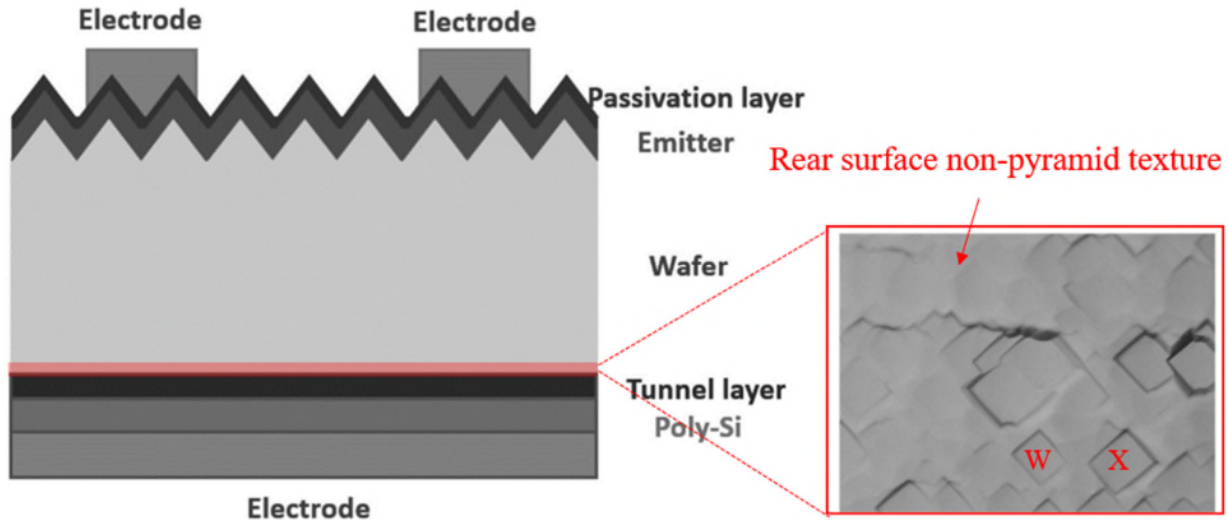


Figure 1 (solar cell side view)

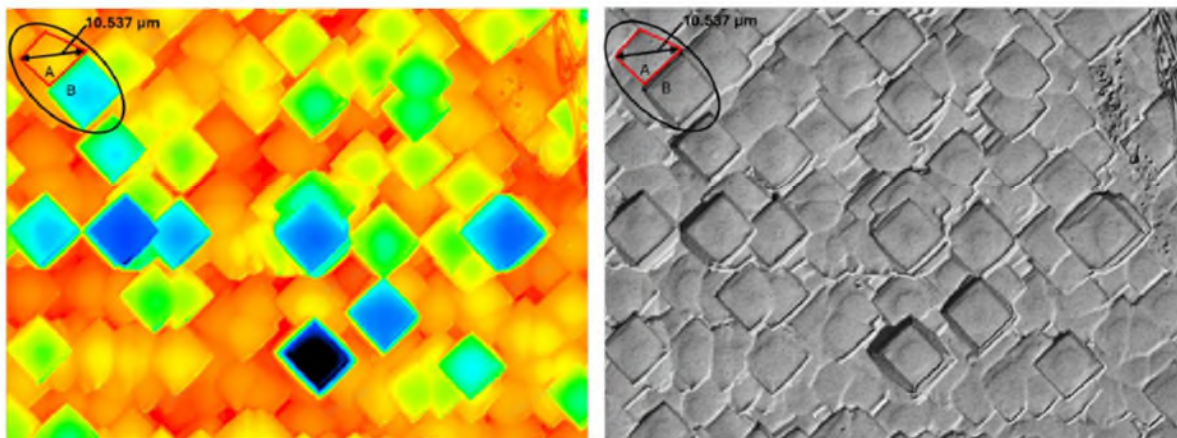
Figure 3 (rear surface texture top view)

EX1004, Figures 1 and 3 (annotated).

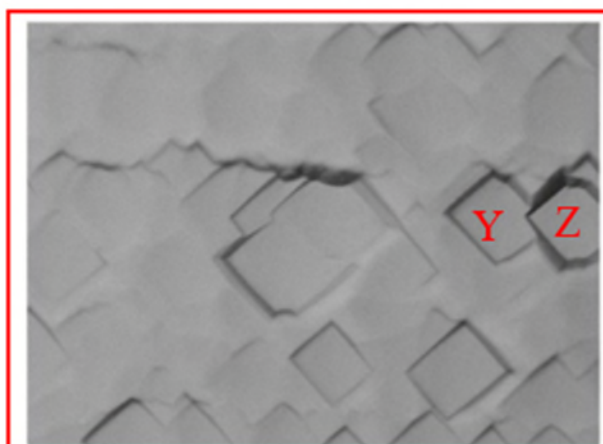
91. In their complaint for patent infringement against Petitioners, Patent Owner has interpreted “two or more first substructures at least partially stacked on one another” in claim 1[b] to read on polygonal shaped structures labeled A and B below. EX1021 at page 10.

SEG-420-BTD-BG

The below laser confocal microscopy images of the SEG-420-BTD-BG (with the main image on the right and the 3D image on the left) show that a rear surface of the semiconductor substrate in the SEG-420-BTD-BG has a first texture structure. For instance, the first texture includes two first substructures A and B partially stacked on one another (in the black oval), as shown in the main image (right), and are of different heights, as denoted in different colors in the 3D image (left), where blue represents the lowest height, red represents the highest height, and other colors represent heights in between.



92. To the extent the structures labeled A and B in Patent Owner’s complaint are “at least partially stacked on one another”, then structures in Figure 3 of Ye labeled as Y and Z below also would be “at least partially stacked on one another”.

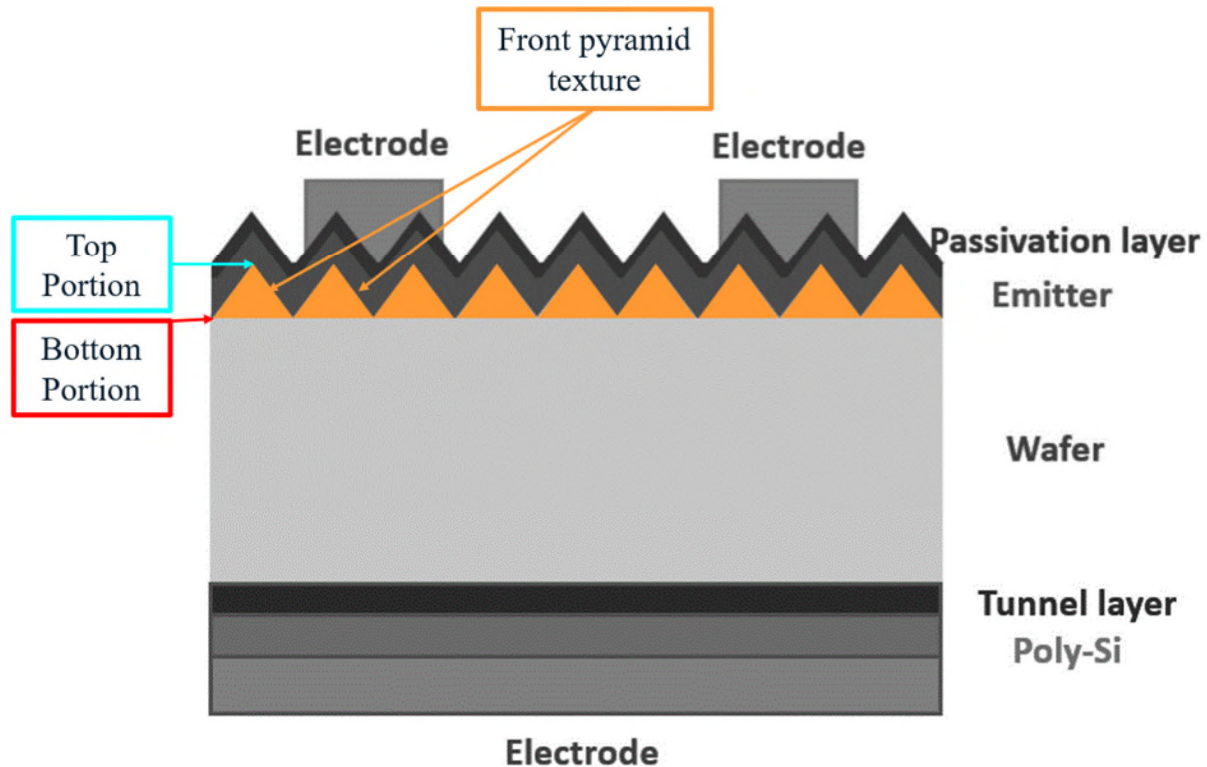


93. Therefore, based on Patent Owner's interpretation, Ye discloses this requirement of claim 1[b].²

- iv. **Claim 1[c]: “wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and”**

94. A POSITA would have understood that Ye discloses that the front surface of the solar cell substrate has a textured structure including pyramid-shaped microstructures. EX1004, Figure 1. As illustrated in Figure 1, the pyramid-shaped microstructure includes a top portion away from the substrate and a bottom portion close to the substrate. *Id.*

² If the Board does not adopt Patent Owner's interpretation, as discussed in Ground 1A, *Yun* discloses this requirement under its plain meaning.



EX1004, Figure 1 (annotated).

- v. **Claim 1[d]: “in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm ,”**

95. A POSITA would have understood that “a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure” corresponds to the pyramid heights of the front surface texture. EX1004, Figure 1; EX1006, Fig. 4. Ye does not specify the height of the pyramid-shaped texture structures on the front surfaces of the solar cells.

96. Basu Paper studies “[t]he effect of the front pyramid heights on the efficiency of ... solar cells” and discloses three ranges of pyramid heights (small: $\sim 5\ \mu\text{m}$, medium: $\sim 6\ \mu\text{m}$, and large $\sim 8\ \mu\text{m}$) of the front surface textures, concluding that the smaller pyramid heights (i.e., $\sim 5\ \mu\text{m}$ maximum), as shown in Fig. 4, give the highest fill factor and hence solar cell efficiency. EX1006 at 590, 597.

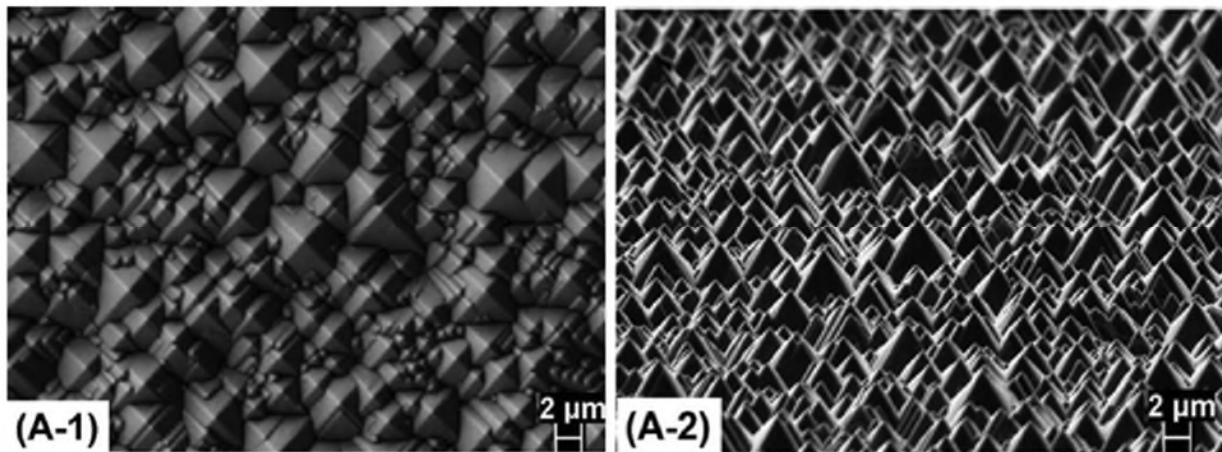


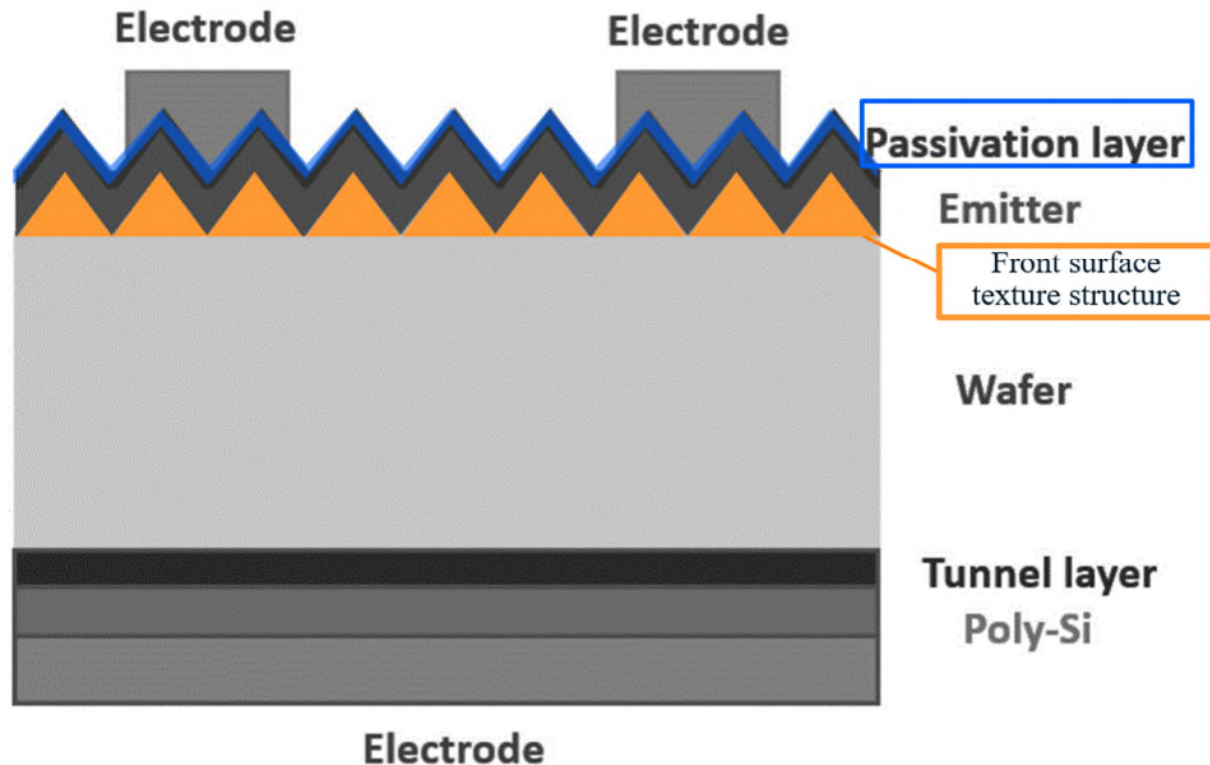
Fig. 4 (A-1) (top view)

Fig. 4 (A-2) (angular view)

EX1006, Fig. 4. Therefore, in light of Basu Paper’s teachings, a POSITA would have found it obvious to design a solar cell as disclosed in Ye to have pyramid texture structures on the front surface having a height of less than $5\ \mu\text{m}$. .

vi. Claim 1[e]: “a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate;”

97. Ye discloses that the front side of the solar cell has a passivation layer located on top of an emitter layer, which is located on top of the front surface texture structure. EX1004, ¶¶ 0019, 0022, 0031-0034, 0038; Figure 1.

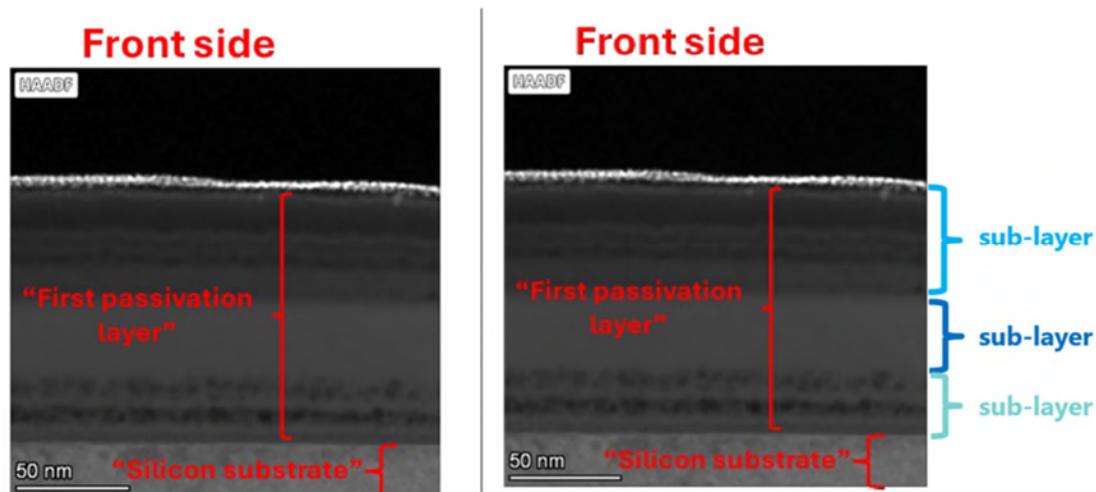


EX1004, Fig. 1 (annotated).

98. Basu Paper also discloses an amorphous SiNx antireflection coating that is “deposited onto the front surface,” and that an emitter is formed on the front side of the substrate. A POSITA would have understood that this antireflection (AR) coating is a standard passivation layer in solar cells. EX1012 at 591; *see also*, EX1024 at 967 (“SiNx film as AR coating as well as a surface passivation layer plays an important role in commercial mc-Si solar cells”); EX1025 at 2326 (“In photovoltaic industries, SiNx:H ARC is often deposited after texturing in order to increase light collection and to passivate silicon surface”). Basu Paper also discloses an amorphous SiNx antireflection coating that is “deposited onto the front surface,”

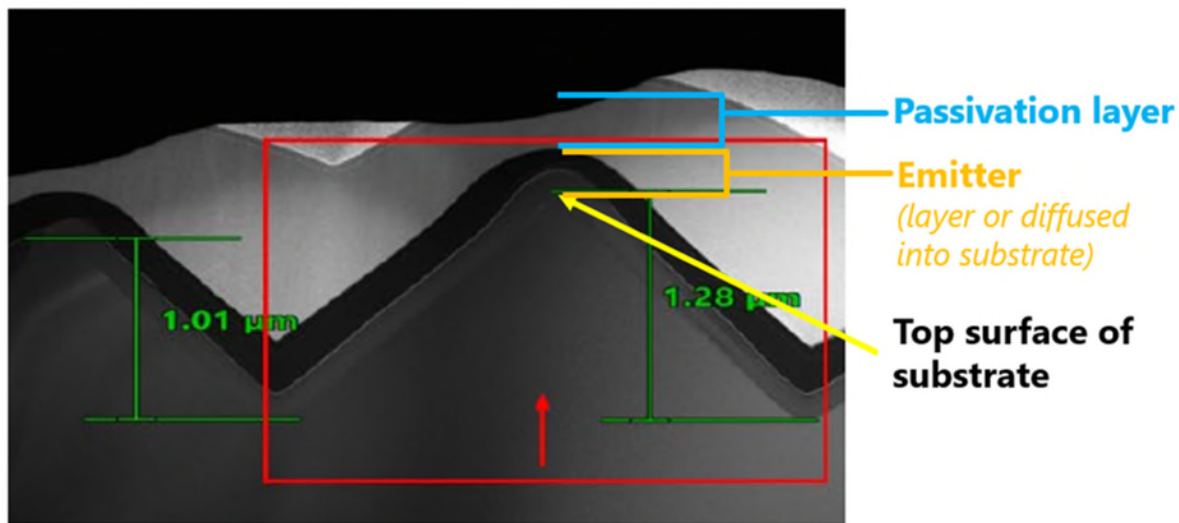
and that an emitter is formed on the front side of the substrate. A POSITA would have understood that this antireflection coating is a standard passivation layer in solar cells. EX1012 at 591; *see also, id.* at 594-95 (“Emitter was formed, on both sides of wafers.... The process was completed by deposition of a 70 nm thickness ARC SiN_x layer on both surfaces....”).

99. In their complaint for patent infringement against Petitioners, Patent Owner has interpreted “a first passivation layer located on the second texture structure” in claim 1[e] to require a layer in the accused products that contacts what Patent Owner labels as the substrate. See below at left from EX1021, page 12 (Patent Owner’s annotation).



However, as shown in the same figure relied upon by Patent Owner, Patent Owner is relying upon multiple distinct layers as the alleged “passivation layer,” including an emitter layer that resides between the front substrate surface and the passivation layer. (see above multiple distinct layers identified in Petitioner’s annotations). The

following figure from Patent Owner's Complaint more clearly illustrates what the Patent Owner regards as the top of the front surface of the substrate (see top end of 1.28 μm measurement in green below), as well as the emitter layer residing on that substrate surface and a passivation layer residing on the emitter layer. For example, I understand that those additional layers include a doped emitter layer between the silicon substrate and the passivation layer.



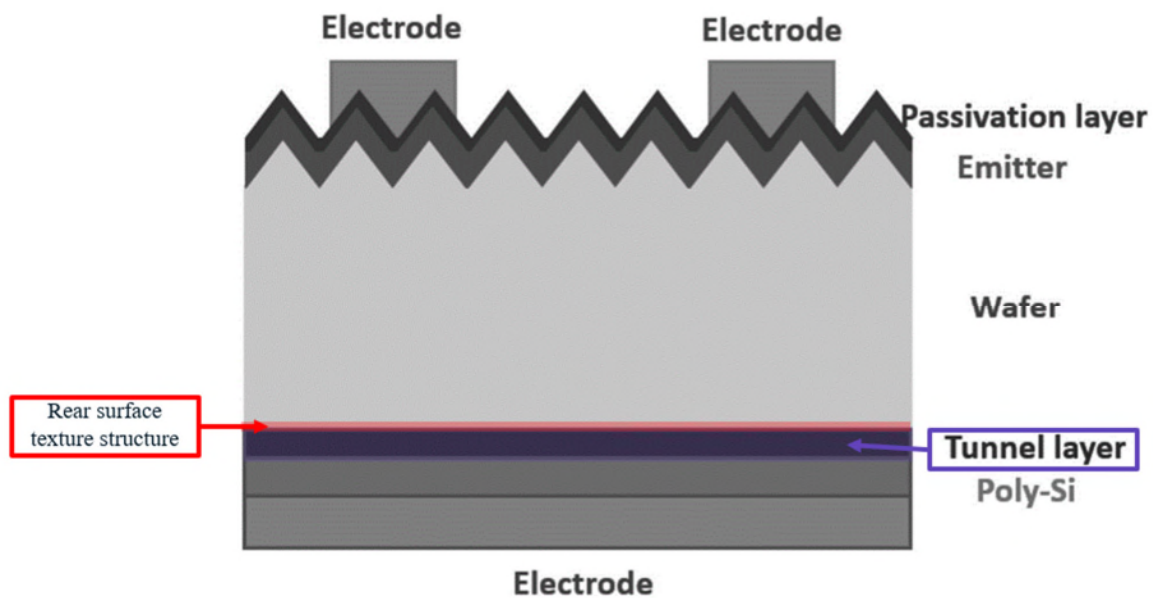
EX1021, page 11 (annotated). Therefore, to the extent the Patent Owner's identification of a passivation layer located on an emitter layer, which in turn is located on a front substrate surface is "a first passivation layer located on the second texture structure" of the front substrate surface, then each of the following also would be "a first passivation layer located on the second texture structure": (1) the passivation layer of Ye, either alone or in combination with the emitter layer; and/or (2) the amorphous SiNx antireflection coating of Basu Paper, either alone or in

combination with the front side emitter. Therefore, based on Patent Owner's interpretation, each of Ye and Basu Paper disclose this requirement of claim 1[e].³

vii. Claim 1[f]: “a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;”

100. Ye discloses “growing a silicon oxide layer ... to form a tunnel-oxide passivated contact structure,” which results in a silicon oxide layer as the tunnel oxide layer. Ye also discloses “TOPCon crystalline silicon solar cell consist of ... a silicon oxide passivating tunneling layer,” which is a tunnel oxide passivation (TOP) layer located on the rear texture structure of the solar cell, as shown in Figure 1 (“Tunnel layer”). *Id.*, ¶ 0004; Figure 1.

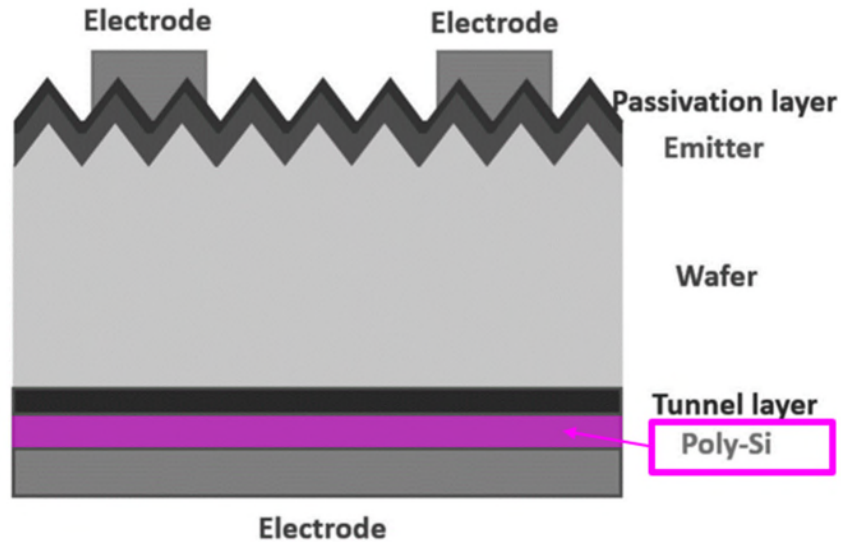
³ If the Board does not adopt Patent Owner's interpretation, as discussed in Ground 6, *Sakai* discloses this requirement under its plain meaning.



EX1004, 11:64-12:1.

viii. Claim 1[g]: “a doped conductive layer located on a surface of the tunnel oxide layer; and

101. Ye discloses “[a] heavily doped polysilicon thin film” formed on top of the underlying silicon-carbon thin film on the rear side of the solar cell. EX1004, ¶ 0023. A POSITA would have recognized from Ye that this layer is “a doped conductive layer” located on the tunnel oxide layer. EX1004, Figure 1; ¶¶ 0023, 0035, 0039.



EX1004, Figure 1.

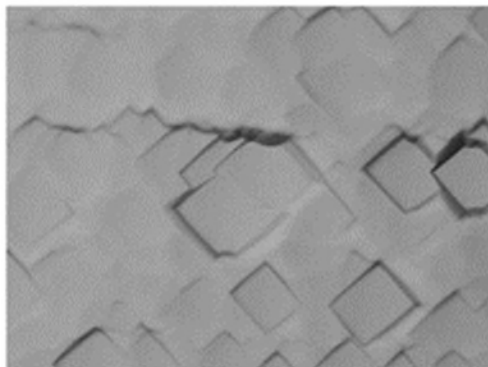
ix. Claim 1[h]: “a second passivation layer located on a surface of the doped conductive layer.”

102. Ye discloses a second passivation layer on the rear side of the solar cell. EX1004, ¶ 0038 (“a SiN passivation layer is formed on the rear surface”); *see also*, Figure 1. Furthermore, Ye discloses the manufacturing process of the rear passivation layer: “[f]irst, boron diffusion is performed on the front surface ... then backside alkaline polishing is carried out ... a silicon oxide layer is formed on the rear surface by thermal oxidation ... a SiN passivation layer is formed on the rear surface”). A POSITA would have understood that the rear passivation layer is located on the surface of the “heavily doped polysilicon thin film”, *i.e.*, the doped conductive layer. *Id.*

103. Basu Paper also discloses that the solar cell manufacturing process “was completed by deposition of a 70 nm thickness ARC SiNx layer on both surfaces.” A POSITA would have understood that these ARC SiNx layers are passivation layers and the rear passivation layer is located on the doped conductive layer of the rear side. EX1006 at 595.

- b. **Claim 3: “a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a substantially trapezoid.”**

104. Ye discloses that the rear surface of the solar cell is textured by non-pyramid-shaped structures which have polygonal top planes. EX1004, Figure 3. A POSITA would have recognized that the polygonal plane can be a diamond, a square, a trapezoid or a substantial diamond/square/trapezoid. Moreover, at least a number of the polygonal surfaces in Figure 3 are diamonds, squares, trapezoids, or substantially one of those shapes.

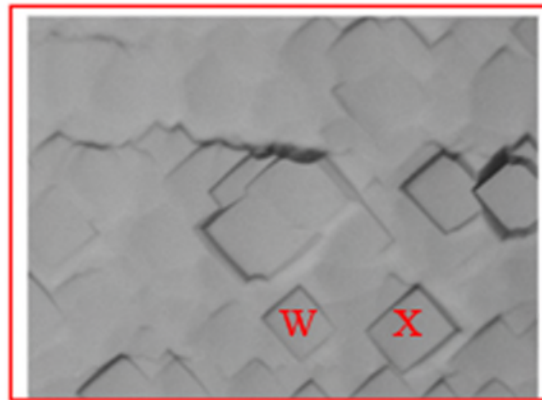


EX1004, Figure 3.

- c. **Claim 5: “the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm .”**

105. Ye discloses that the rear surface of the solar cell is textured by non-pyramid-shaped structures. EX1004, Figure 3. As shown in Figure 3, at least the highlighted adjacent texture structures are not stacked on one another. *Id.* The substructures on the back side of the solar cell in Ye are approximately square-shaped. A square is a polygonal shape. I assume for purposes of this proceeding that the size limitation of “less than or equal to 45 μm ” refers to a non-zero size. With that assumption, various prior art references, such as Basu Paper and Shah Book, show that this range of size was well known to a POSITA before the effective filing date of the '136 Patent. For example, Basu Paper discloses that the front-side pyramid base dimension is less than 10 μm (see the microscopy images in Figures 4 and 5 of Basu Paper). Since the silicon front surface and back surface are crystallographically equivalent and indistinguishable (due to the well-known inversion symmetry of silicon), the rear-side polygons have approximately the same dimensions as the bases of the pyramids on the front side. As such, the rear-side polygonal substructures have about the same dimension of less than 10 μm , that is, less than 45 μm . Furthermore, Shan Book discloses a pyramid height of up to 7 μm (EX1015 at 85). With a typical pyramid apex angle of approximately 70.5° (*id.* at

86) and pyramid height of 7 μm , the pyramid base dimension, which is the maximum possible size of the polished top surface, is about 10 μm , which is less than 45 μm . As such, based on the typical size and scale of most TOPCon solar cells and the textured substructures formed on the substrates for those solar cells, a POSITA would have recognized that these top surfaces are smaller than 45 μm in any dimensional size.



EX1004, Figure 3 (annotated).

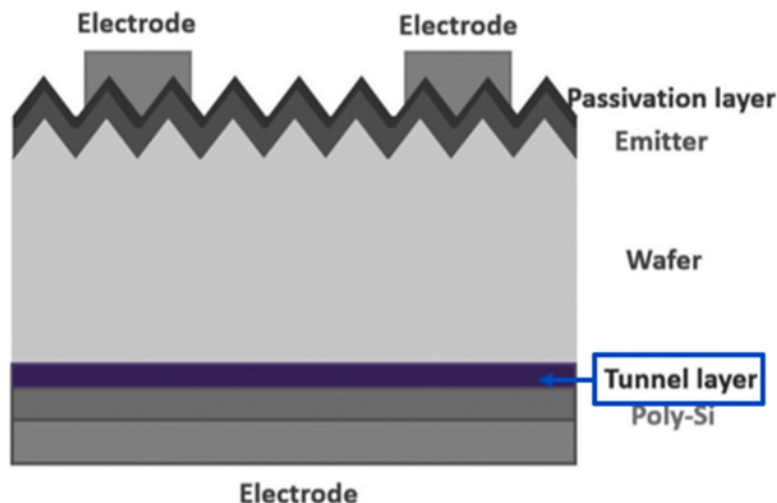
d. **Claim 6: “the top surface of the second substructure is a polygonal plane.”**

106. This claim depends from claim 5, which is discussed above. Under Patent Owner’s interpretation of the claims, Ye discloses the marked top surfaces of the non-pyramid substructures is a polygonal plane.

e. **Claim 7**

- i. **Claim 7[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

107. See discussion of claim 1[f]. Ye discloses “growing a silicon oxide layer ... to form a tunnel-oxide passivated contact structure,” which results in a silicon oxide layer as the tunnel oxide layer. EX1004, Claim 1. Ye also discloses “TOPCon crystalline silicon solar cell consist of ... a silicon oxide passivating tunneling layer,” which is a tunnel oxide layer located on the rear texture structure of the solar cell, as shown in Figure 1 (“Tunnel layer”). *Id.*, ¶ 0004; Figure 1.



EX1004, 11:64-12:1.

ii. Claim 7[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”

108. See discussion of claim 1[f]. *Ye* discloses “thickness of the silicon oxide layer is 1.0–3.5 nm,” which overlaps a significant portion (more than 83%) of the claimed thickness range from 0.8 nm to 2 nm. *Id.*, Claim 3. That overlap discloses a tunnel oxide layer having a thickness in the claimed range. Alternatively, based on these teachings, it would have been obvious to a POSITA to make the tunnel oxide layer of *Ye* with a thickness ranging from 1.0 nm to 2 nm. *Ye* does not suggest any particular benefit of the thickness range above the range claimed in the ’136 patent.

109. As noted in my discussion of the technology background in Section IX above, a POSITA would be aware that a tunnel oxide passivation (TOP) layer must be thin enough to be tunneled through but should also passivate the semiconductor surface. Therefore, a POSITA would have recognized that thickness as a result-effective variable. For example, a tunneling layer much thicker than 2 nm, e.g. 20 nm, would be too thick for an efficient quantum-mechanical tunneling process. On the other hand, to effectively passivate the semiconductor surface, a tunnel oxide passivation (TOP) layer should be at least 0.5 nm thick. This puts the preferable range of the TOP layer between 0.5 nm and a few nm. In addition, the contact area also plays a role, with larger contact areas allowing for thicker TOP layers, and smaller contact areas requiring thinner TOP layers, to keep the contact resistance

low. A POSITA would understand that any of the ranges, such as 0.5 to 2.0 nm, 1.0 to 2.0 nm, or 1.0 to 3.0 nm, would be a preferred TOP layer thickness range. Given the finite range of thicknesses disclosed in Ye, a POSITA would have found it obvious to select a tunnel oxide layer with a thickness of 1.0 nm – 2.0 nm, which is within the claimed range. A POSITA also would have recognized that selecting an appropriate thickness was a routine engineering problem in solar cell design.

f. **Claim 9: “the first passivation layer includes at least one of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer or a silicon oxynitride layer.”**

110. See claim 1[e]. Ye discloses that “Al₂O₃/SiN passivation layers are formed on the front surface,” which indicates that the front passivation layer can include silicon nitride (SiN) and an aluminum oxide layer. EX1004, ¶ 0038.

1. Claim 12

i. **Claim 12[a]: “the semiconductor substrate is an N-type monocrystalline silicon substrate,”**

111. Ye discloses that the semiconductor substrate is an N-type monocrystalline silicon wafer (substrate). EX1004, ¶ 0030 (“The n-type silicon wafers used in the present invention are 180 μm-thick solar-grade Czochralski-grown monocrystalline silicon wafers ...”).

- ii. **Claim 12[b]: “the doped conductive layer is an N-type doped polycrystalline silicon layer, an N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer, and”**

112. See discussion of claim 1[g]. Ye discloses the doped conductive layer is an N-type doped amorphous silicon layer or an N-type doped polycrystalline conductive layer (after crystallization). EX1004, ¶ 0007 (“a doped amorphous silicon layer is deposited by PECVD; subsequently, a high-temperature crystallization process is performed to convert the amorphous silicon into polysilicon, thereby forming a TOPCon structure”); *see also, id.*, ¶ 0031 (“one or more phosphorus-doped amorphous silicon thin-film layers with a thickness of 80–200 nm are deposited”).

- iii. **Claim 12[c]: “the doped conductive layer has a thickness ranging from 60 nm to 200 nm.”**

113. Ye discloses phosphorus-doped amorphous silicon thin-film layers with a thickness of 80–200 nm, which falls within the claimed range of 60 nm to 200 nm. EX1004, ¶ 0031. Furthermore, Ye discloses an embodiment having a doped conductive layer with a thickness of 120 nm, which falls within the claimed range of 60 nm to 200 nm. *Id.*, ¶ 0039 (“n⁺ poly-Si (120 nm)”). A POSITA would have understood that the “n⁺ poly-Si” is n-type doped polycrystalline silicon layer.

g. **Claim 13**

- i. **Claim 13[p]: “A photovoltaic module, comprising a plurality of solar cell strings, wherein each of the plurality of solar cell strings comprises solar cells, and at least one of the solar cells comprise:”**

114. See claim 1[p] in this Ground. EX1004, ¶¶ 0001-0002; Figures 1; *see also id.*, 0018, 0020-0024, 0037-0038. Moreover, as noted in my discussion of the technology background in Section IX above, in order to capture significant amounts of sunlight, typical solar installations cover many square feet, such as 100 or 1,000 square feet. Since the silicon wafer sizes are significantly less than a square foot, in order to generate a sufficient amount of electricity for most applications, a POSITA would understand that any solar cell must be used together with a plurality of solar cells assembled into one or more strings to form a photovoltaic module or solar panel. Such strings and modules were well known in the art before the '136 Patent. *See* EX1015 at 115 (“For the construction of a whole module, the copper ribbons are used to connect the front of the first cell to the back of the second cell, etc. This corresponds to a series connection of the solar cells and leads to an addition of the individual voltages, whilst the current remains constant. Typically, 1–12 cells are processed into a so-called ‘string’. Six strings are then connected in series to finally make up a whole module.”) and 219-223.



Fig. 9.1 c-Si solar cells with (from the top left) two (2BB), three (3BB), five (5BB) busbar and cell without busbars (below right). Current-collecting fingers are placed perpendicular to the busbars

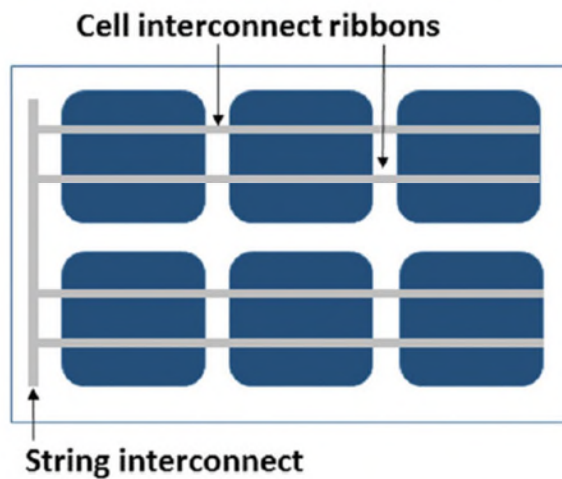


Fig. 9.2 Simplified sketch of a solar module with two-busbar (2BB) cells. *Cell interconnect ribbons* and *string interconnects* are shown. *Busbars* are hidden below the ribbons

115. Therefore, a POSITA would have found it obvious to assemble a plurality of the solar cells of Ye and/or Basu Paper into a plurality of strings that form a photovoltaic module, and claim 13[p] is taught or rendered obvious by each of Ye and Basu Paper.

ii. Claim 13[a] “a semiconductor substrate,”

116. See claim 1[a] in this ground. For the same reasons discussed with regard to claim 1[a] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 13[a].

iii. Claim 13[b] “wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another, a top surface of the first substructure is a polygonal plane, and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ; and”

117. See claim 1[b] in this ground. For the same reasons discussed with regard to claim 1[b] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 13[b].

- iv. **Claim 13[c] “wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and”**

118. See claim 1[c] in this ground. For the same reasons discussed with regard to claim 1[c] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 13[c].

- v. **Claim 13[d] “in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm ,”**

119. See claim 1[d] in this ground. For the same reasons discussed with regard to claim 1[d] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 13[d].

- vi. **Claim 13[e] “a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate;”**

120. See claim 1[e] in this ground. For the same reasons discussed with regard to claim 1[e] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 13[e].

vii. Claim 13[f] “a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;”

121. See claim 1[f] in this ground. For the same reasons discussed with regard to claim 1[f] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 13[e].

viii. Claim 13[g] “a doped conductive layer located on a surface of the tunnel oxide layer; and”

122. See claim 1[g] in this ground. For the same reasons discussed with regard to claim 1[g] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 13[g].

ix. Claim 13[h] “a second passivation layer located on a surface of the doped conductive layer.”

123. See claim 1[h] in this ground. For the same reasons discussed with regard to claim 1[h] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 13[h].

h. Claim 14 “The photovoltaic module according to claim 13, wherein for the two or more first substructures at least partially stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, a distance between the top surface of the outermost first substructure and the top surface of the adjacent first substructure is equal to or less than 2 μm .”

124. [Reserved].

- i. **Claim 15 “The photovoltaic module according to claim 13, wherein a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a substantially trapezoid.”**

125. See claim 3 in this ground. For the same reasons discussed with regard to claim 3 in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 14.

- j. **Claim 17 “The photovoltaic module according to claim 13, wherein the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm .”**

126. See claim 5 in this ground. For the same reasons discussed with regard to claim 5 in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 17.

- k. **Claim 18 “The photovoltaic module according to claim 17, wherein the top surface of the second substructure is a polygonal plane.”**

127. See claim 6 in this ground. For the same reasons discussed with regard to claim 6 in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 18.

I. Claim 19

- i. Claim 19[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

128. See claim 7[a] in this ground. For the same reasons discussed with regard to claim 7[a] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 19[a].

- ii. Claim 19[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”**

129. See claim 7[b] in this ground. For the same reasons discussed with regard to claim 7[b] in this ground, the combination of Ye and Basu Paper discloses or renders obvious claim 19[b].

m. Claim 20

- i. Claim 20[a]: “the second passivation layer includes at least one of a silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and”**

130. [Reserved]

- ii. Claim 20[b]: “the second passivation layer has a thickness ranging from 70 nm to 120 nm.”**

131. [Reserved]

XII. GROUND 1A: CLAIMS 1-3, 5-15, AND 17-20 ARE RENDERED OBVIOUS BY YE IN VIEW OF BASU PAPER AND YUN

A. RATIONALE FOR COMBINING YE, YUN, AND BASU PAPER

132. The '136 Patent relates to the field of solar cells generally, and more specifically to optimizing solar cell design (*e.g.*, of TOPCon solar cells) to improve efficiency (*e.g.*, by using textured front and back surfaces). EX1001, 1:15-18, 1:41-46. *Ye* also relates to the field of solar cells, and more specifically to preparing a laminated thin-film tunneling oxide passivated (TOP) contact structure in a way that optimizes a solar cell's design and improves its quality (*e.g.*, by avoiding delamination). EX1004, ¶¶ 0001, 0008-0009. *Ye* specifically refers to TOPCon solar cells as an example of the type of solar cells improved by these optimizations. EX1004, ¶ 0003-0008. *Yun* also relates to the field of solar cells, and is directed to optimizing solar cell structures by surface texturing to improve efficiency and reduce cost (*e.g.*, by using textured surface structures on the solar cell). EX1005, ¶ 0001 - 0003. Basu Paper also relates to the field of solar cells made from monocrystalline silicon wafers, and is directed to optimizing solar cell structures (*e.g.*, by optimizing the pyramid height) to maximize the efficiency. EX1012 at 590. As such, *Ye*, *Yun* and Basu Paper all relate to the same field as the '136 Patent, and are therefore analogous art to each other and to the '136 Patent. EX1001, 1:41-46; 4:13-17; 5:44-55; EX1004, ¶¶ 0008-0009; EX1005, ¶ 0002; EX1012 at 590.

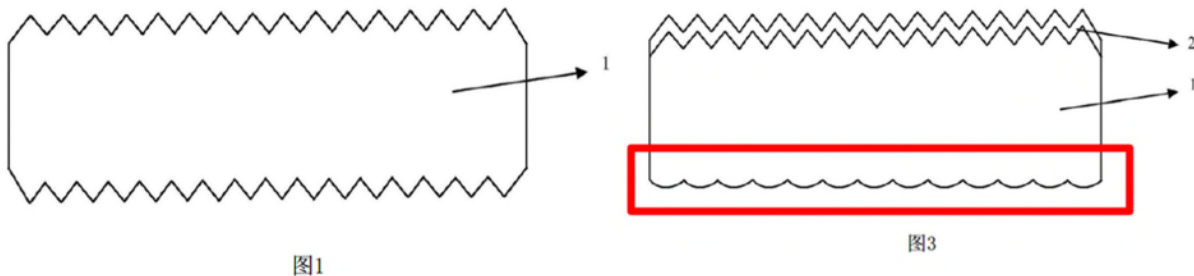
133. Alternatively, the '136 Patent is concerned with the problem of solar cells having non-optimal back surfaces that adversely affect other layers and lower the efficiency. EX1001, 5:29-38. *Ye, Yun* and Basu Paper each teaches how to optimize the textured front/back surfaces and their adjacent layers to improve the efficiency, quality or reduce cost. EX1004, ¶¶ 0020, 0022; EX1005, ¶ 0022; EX1012 at 597. As such, *Ye, Yun* and Basu Paper all relate to problems with which the '136 Patent is concerned. Therefore, *Ye, Yun* and Basu Paper are analogous art to each other and to the '136 Patent.

134. *Ye* describes solar cells that have texture surfaces on both the front and rear sides. EX1004, Figure 1; Figure 3. The front surface texture has a pyramid shape, and the rear surface has a non-pyramid shape. *Id.* *Ye* states that, to create non-pyramid texture on the rear surface, the “backside alkaline polishing is carried out” after “boron diffusion is performed on the front surface.” *Id.*, ¶ 0038. In other words, *Ye* teaches removal of texture material on the rear side of a TOPCon cell with polishing, for example, using chemical mechanical polishing (CMP) as an additional polishing step. *Id.* The use of similar chemical mechanical polishing techniques with alkaline solutions to remove texture material from a silicon surface was well known to POSITAs before the '136 Patent. *See e.g.*, EX1026 at 2 (“Due to these merits, the manufacturing industry of semiconductor production processes ... have been using CMP for decades”). However, these methods are known to make the manufacturing

process more complex and costly. *Id.* As an example, Horowitz Report finds that CMP is a high-cost fabrication process in the context of solar cell manufacturing. EX1030 at 11 (“the CMP costs are similar to the total cost of the substrate in this case, because the substrate cost is amortized over five reuses. The substrate and costs associated with reuses—CMP and ELO—are the largest contributor to overall cell costs.”); *id.* at 13 (“The cost of CMP used to re-prepare the surface after lift-off, is another major cost driver”). Furthermore, the mechanical component during polishing is known to create damage on the rear side that can be detrimental. *Id.* EX1027 at 1 (“Mechanical polishing... is prone to introducing scratches and residual stress... CMP... may still induce structural defects, such as silicon wafer warping and subsurface cracks... These defects are challenging to detect ...”); EX1028 at 1 (“The surface of the mechanically polished CZT film has a damage layer composed of stress concentration, electroactive defects, impurities and micro-scratches, dimpled surface, etc., which will cause periodic damage to the crystal lattice in the surface damage layer...”).

135. *Yun* teaches using wet chemical methods (which do not require mechanical polishing) to remove texture material on the rear side of a double-sided solar cell to form platform-shaped structures of certain sizes. EX1005, ¶¶ 0019, 0043, 0056. The use of wet chemical techniques to remove texture material from a silicon surface was well known to POSITAs before the '136 Patent. *See e.g.,*

EX1040 (Xie Paper) at 1-2 (“During the CMP process, Si atoms on the surface of the silicon wafers react with OH^- and H_2O in the polishing slurry to form a layer of silicates [] in an alkaline environment[] ... This generated layer is subsequently removed by the abrasive particles under the action of pressure and rotational speed []. This is the typical mechanism of material removal during the polishing process.”). As another example, *Du* discloses a process for manufacturing an N-type TOPCon solar cell that includes “double-sided texturing” of the silicon substrate to form pyramid-shaped texture structures on both sides as shown in Figure 1 below, and then exposing the back side of the substrate to “a mixed solution of HF, HNO_3 , and H_2SO_4 for etching treatment” that “obtain[s] a smooth pyramid surface,” as shown in Figure 3 below. EX1017.



EX1017, Figure 1; Figure 3.

136. Therefore, a POSITA would have been motivated to adopt the wet chemical methods of removing material disclosed by *Yun* to remove material from the rear side of the TOPCon cell in *Ye* instead of mechanical polishing, for example, to reduce the risk of damage to the rear side of the solar cell. This advantage of

using wet chemical techniques over mechanical polishing would have been well known to a POSITA. *See e.g.*, EX1017, Figure 1, Figure 3; EX1029 at 2. That would result in the formation of overlapping platform-shaped (non-pyramid) structures of the sizes claimed in the '136 patent. A POSITA would have had a reasonable expectation of success in applying the wet chemical method disclosed in *Yun* to the solar cells in *Ye* because it uses a known method (*Yun*'s wet chemical method) to obtain predictable results (i.e., forming non-pyramid textures in a manner that is less likely to cause damage to the silicon surface). EX1005, ¶¶ 0019, 0043, 0056.

137. Basu Paper teaches that solar cell efficiency can be maximized by choosing optimal pyramid heights for the front surface textures. EX1013 at 597. Basu Paper studies three ranges of pyramid heights (small: ~5 μm , medium: ~6 μm , and large ~8 μm) of the surface textures, and concludes that the smaller pyramids (i.e., ~5 μm among the three ranges) give the highest fill factor and hence most efficiency. *Id.* at 594, 597 ("The FF was found to decrease with increasing maximum pyramid heights within the variation studied here and smaller pyramids were found to give the highest FF and hence efficiency."). A POSITA would have been motivated to use pyramids of the height range disclosed in Basu Paper as being most efficient (i.e., ~5 μm maximum, or 2-5 μm) for the front surface texture in *Ye* and *Yun* to further improve the solar cell efficiency. A POSITA would have had a

reasonable expectation of success in adopting the pyramid heights disclosed in Basu Paper for the solar cells in *Ye* and *Yun*, because it merely optimizes the size of a known texture structure and shape (i.e., pyramids) of the solar cell within a known range of pyramid heights using a known method (Basu Paper's optimal height of ~ 5 μm) to obtain predictable results (improved efficiency). EX1012 at 597.

138. Based on the above, a POSITA would have been motivated to combine the teachings of *Ye*, *Yun*, and Basu Paper to manufacture solar cells with improved efficiency and quality, as claimed in the '136 Patent. EX1004, Figure 1, Figure 3; EX1005, ¶¶ 0019, 0043, 0056; EX1012 at 597. A POSITA would have had a reasonable expectation of success in combining *Ye*, *Yun*, and Basu Paper to reach the invention claimed in the '136 Patent because combining these three references is merely optimization of different aspects of solar cells to improve the solar cell efficiency and quality, falling within routine engineering problems that a POSITA would have been able to solve. EX1004, Figure 1, Figure 3; EX1005, ¶¶ 0019, 0043, 0056; EX1012 at 597.

139. Additionally, a POSITA would have deemed it obvious to: (1) apply the wet chemical method based on *Yun*'s teaching to create non-pyramid-shaped texture for the rear surface of the solar cell in *Ye*, and (2) further optimize the front texture pyramid height by adopting the optimal height range (~ 5 μm) based on Basu Paper's teaching. EX1004, Figure 1; EX1005, ¶¶ 0019, 0043, 0056; EX1012 at 597.

A POSITA would have motivated to make these optimizations to *Ye*'s solar cells to (1) improve the light-conversion efficiency, (2) improve the solar cell quality and yield, and (3) reduce the manufacturing cost of *Ye*'s solar cells. *Id.* A POSITA would have had a reasonable expectation of success in these optimizations since they would have involved using known methods (the wet chemical method such as that disclosed in *Yun*; the optimization of texture sizes and shapes) to obtain known results (improved efficiency, quality and reduced cost). EX1004, Figure 1; EX1005, ¶¶ 0019, 0043, 0056; EX1012 at 597. *see also* §X.A, X.B, and X.C, *supra*.

B. DISCLOSURE OF YE IN VIEW OF BASU PAPER AND YUN

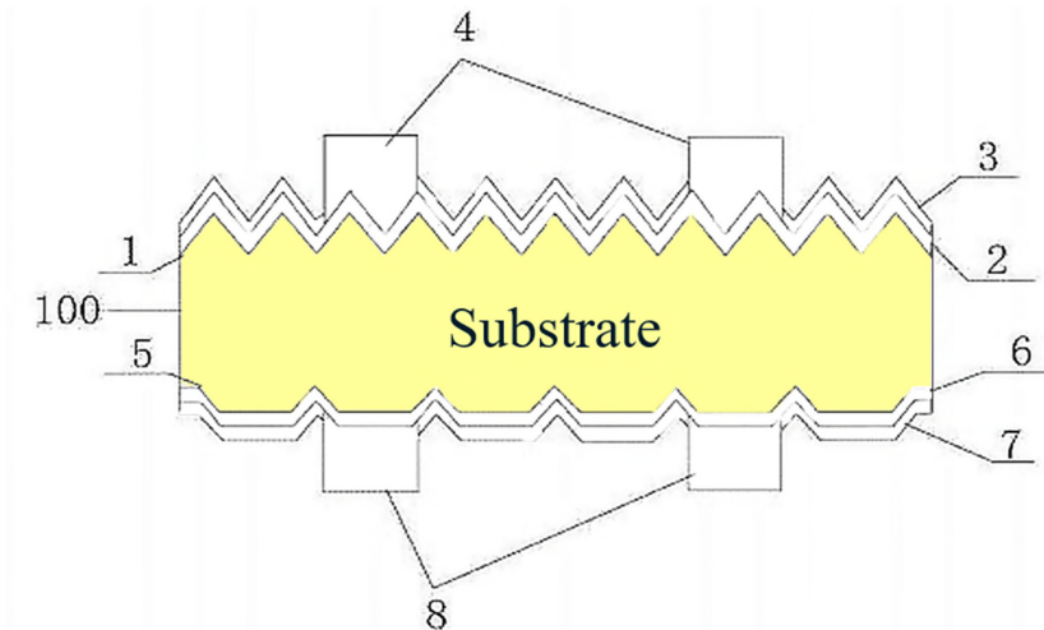
a. Claim 1

i. Claim 1[p]: “A solar cell, comprising:”

140. See claim 1[p] in Ground 1. *Yun* also discloses various embodiments of “solar cells” with textured surfaces. EX1005, Abstract, ¶¶ 0001, 0004-0007, 0020-0023, 0038, 0051 (“This invention relates to a solar cell and its preparation method ..., belonging to the field of solar cell technology”); *see also*, Figure 1.

ii. Claim 1[a]: “a semiconductor substrate,”

141. See claim 1[a] in Ground 1. *Yun* also discloses a monocrystalline silicon substrate (100 in Figure 1) that is a semiconductor substrate. EX1005, Claim 1; ¶¶ 0007, 0026, 0029, 0030, 0034, 0039, 0052.

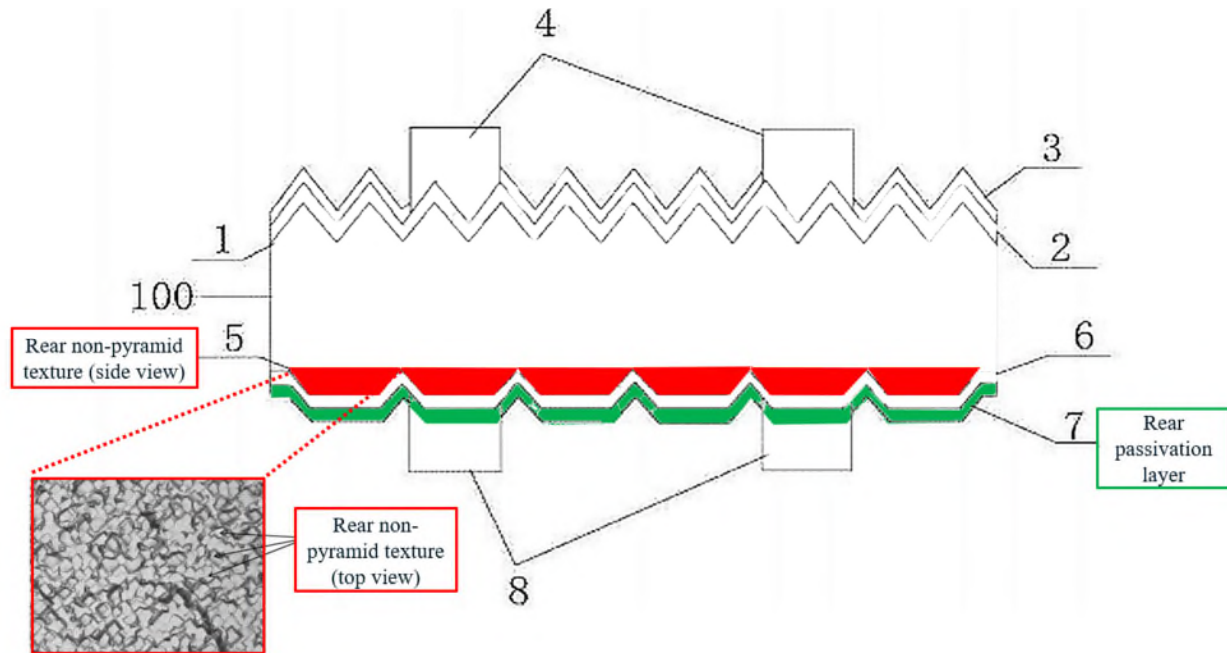


EX1005, Figure 1 (annotated).

- iii. **Claim 1[b]: “wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another, a top surface of the first substructure is a polygonal plane, and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ;**”

142. See claim 1[b] in Ground 1. *Yun* discloses solar cells having a textured rear surface with “platform-shaped substructures,” which a POSITA would have understood to be “non-pyramid-shaped substructures”. EX1005, Abstract; Claim 1; ¶¶ 0007, 0010, 0019, 0022-0023, 0030, 0034, 0036, 0048 (“The back textured surface is characterized by being a platform-shaped texture surface”); *see also*,

Figures 1-2. Figure 2 shows a top view of the top surface of those platform shaped structures, which appear as four-sided polygonal planar surfaces located on the rear surface of the solar cell.

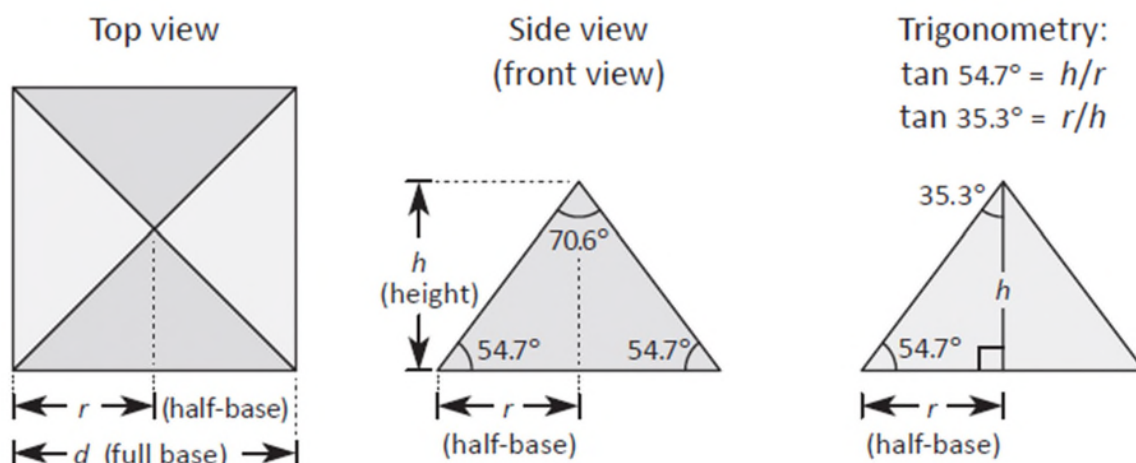


EX1005, Figure 1; Figure 2 (annotated).

143. *Yun* further discloses “[t]he platform structures are ... partially overlapping ...,” which a POSITA would have understood to mean that the platform structures (i.e., non-pyramid substructures) are at least partially stacked on one another. Furthermore, *Yun* discloses “[e]ach platform structure has a lower plane connected to the silicon substrate and an upper plane opposite to the lower plane,” and “the side length of the upper plane is 2 to 10 μm ,” which means the top surface of each platform-shaped substructures has a one-dimensional size less than 45 μm . *Id.*, Abstract. Furthermore, given that the top angle of the front-side pyramids is

crystallographically determined and well-known to be 70.6° , the base half-dimension (half-base) is given by the pyramid height times tangent ($70.6^\circ / 2$). That is, the base dimension (full base) is given by the equation and illustrated in the figure below:

$$\text{Base dimension} = 2 \times \text{Pyramid height} \times \tan (70.6^\circ / 2)$$

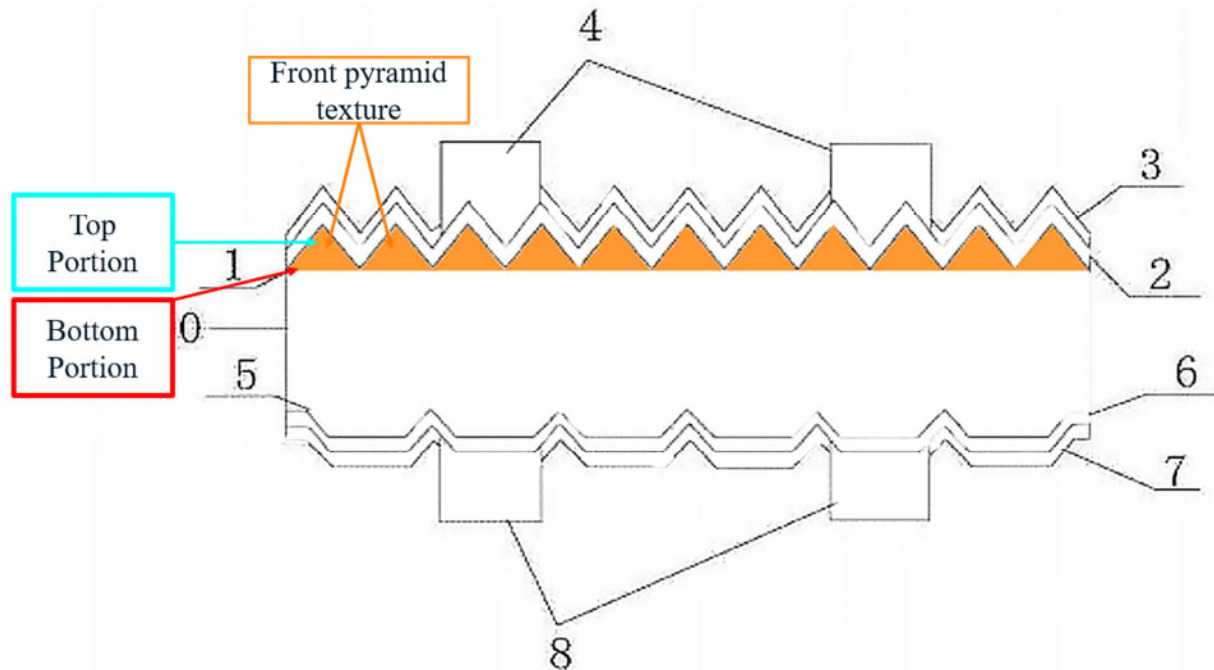


144. Based on the above equation and assuming a pyramid height of $5\ \mu\text{m}$ (as disclosed in Basu paper and discussed in claim 1[d] below), the base dimension can be calculated to be $7.08\ \mu\text{m}$ ($2 \times 5\ \mu\text{m} \times \tan (70.6^\circ / 2) = 7.08\ \mu\text{m}$), that is, less than $45\ \mu\text{m}$. Therefore, the combination of *Ye* and *Yun* discloses claim 1[b]. The calculation is based on the use of elementary trigonometric functions such as the tangent function. The trigonometric relationships invoked here apply to triangles with one of the three angles being a 90° angle. For such right-angled triangles, trigonometric functions such as the sine, cosine and tangent function apply. The

cross-sectional shape of the textured pyramids are right-angled triangles so that trigonometric functions, such as the sine, cosine, and tangent functions, can be applied. The equations written above are based on elementary trigonometry applicable to right-angled triangles.

- iv. **Claim 1[c]: “wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and”**

145. See claim 1[b] in Ground 1. *Yun* also discloses that the front surface of the solar cell substrate has pyramid-shaped texture structures. EX1005, Figure 1; ¶¶ 0003, 0029 (“In this embodiment, it consists of a front-side pyramidal texturing surface”); *see also id.*, 0034 (“As shown in FIG. 1, a front pyramid-shaped texture surface 1 ...”). A POSITA would have understood that the pyramid-shaped texture structure of the front surface has a top portion away from the substrate, and a bottom close to the substrate. *Id.* Figure 1.



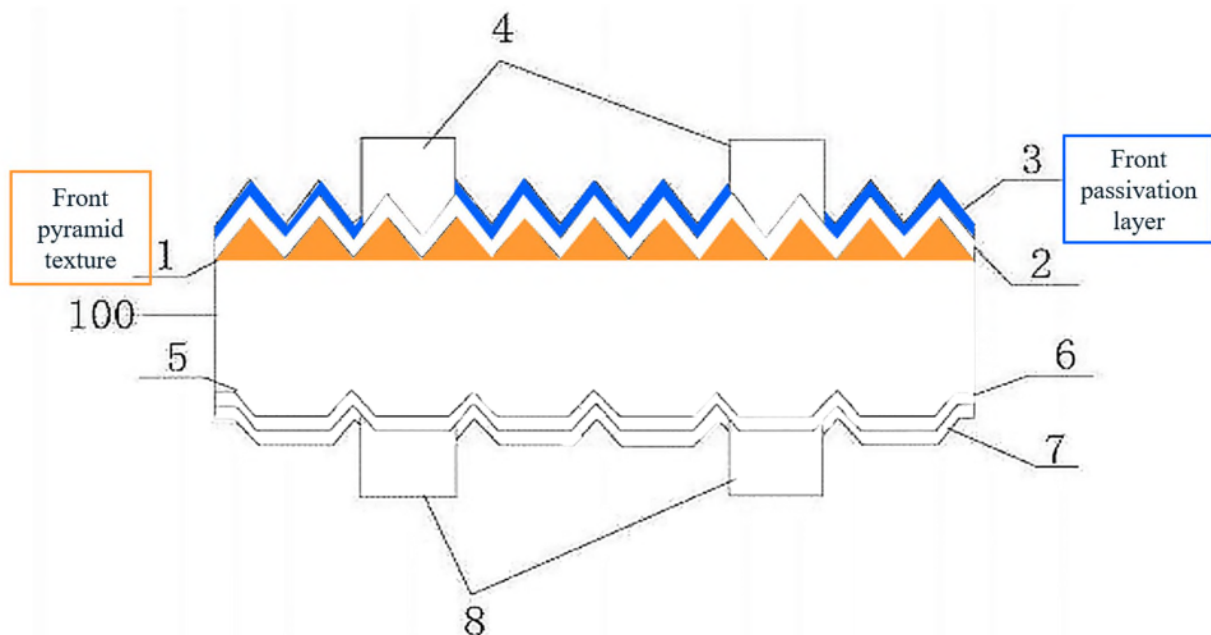
EX1005, Figure 1 (annotated).

- v. **Claim 1[d]: “in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm ,”**

146. See claim 1[e] in Ground 1. *Yun* also does not specify the height of the pyramid-shaped texture structures on the front surfaces of its solar cells. *Yun* gives examples of heights of the non-pyramid platform structures on the back surface of its solar cells that range from 1 μm to 8 μm , which overlaps the claimed range and the range taught by Basu Paper. EX1005, ¶¶0007, 0030 (1 μm), 0032 (8 μm), 0034 (3 μm), 0036 (6 μm), & Abstract.

vi. **Claim 1[e]: “a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate;”**

147. See claim 1[e] in Ground 1. *Yun* also discloses that the solar cell has “a front passivation antireflection dielectric layer” on the front surface texture structure. EX1005, Abstract; Claims 1-2; ¶¶ 0007-0008, 0026, 0029-0036.



EX1005, Figure 1 (annotated).

148. As discussed in Ground 1, based on Patent Owner’s interpretation applied in its patent infringement complaint the front passivation antireflection

dielectric layer 3 of *Yun*, either alone or in combination with the front PN emitter junction 2 discloses this requirement of claim 1[e].⁴

vii. Claim 1[f]: “a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;”

149. See claim 1[f] in Ground 1. For the same reasons discussed with regard to claim 1[f] in Ground 1, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious Claim 1[f].

viii. Claim 1[g]: “a doped conductive layer located on a surface of the tunnel oxide layer; and

150. See claim 1[g] in Ground 1. *Yun* also discloses that the rear side of the solar cell includes a phosphorus-doped back surface field, which corresponds to a doped conductive layer. EX1005, ¶ 0034 (“On the back side of the N-type single-crystal silicon substrate ... a phosphorus-doped back surface field 6 formed by back phosphorus doping ...”).

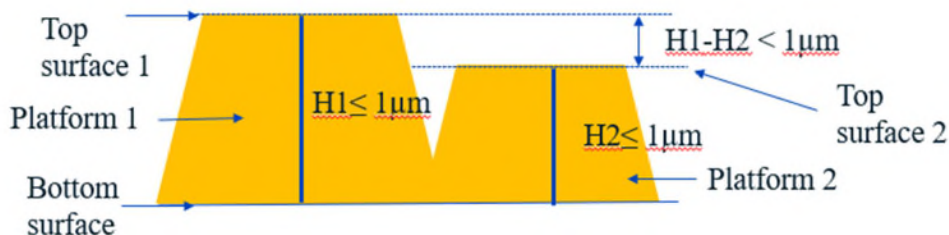
⁴ If the Board does not adopt Patent Owner’s interpretation, as discussed in Ground 6, *Sakai* discloses this requirement under any plausible construction.

ix. **Claim 1[h]: “a second passivation layer located on a surface of the doped conductive layer.”**

151. See claim 1[h] in Ground 1. For the same reasons discussed with regard to Claim 1[h] in Ground 1, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious Claim 1[h].

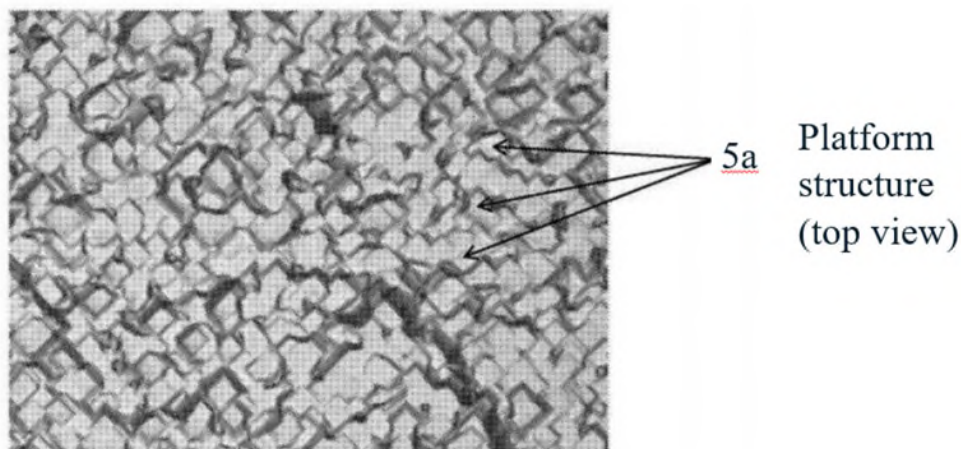
b. **Claim 2: “for the two or more first substructures at least partially stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, a distance between the top surface of the outermost first substructure and the top surface of the adjacent first substructure is equal to or less than 2 μm .”**

152. *Yun* discloses the rear surface of the solar cell has a platform-shaped texture and “the height of the platform structure 5a is 1 μm .” EX1005, ¶ 0030. A POSITA would have understood that when all platform-shaped structures have heights (H_1 , H_2 in the illustrative figure below) less than 1 μm with respect to the same surface of the solar cell, the distance between top surfaces (i.e., $H_1 - H_2$) of any two platform-shaped structures would be equal to or less than 1 μm (thus, less than 2 μm).



- c. **Claim 3: “a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a substantially trapezoid.”**

153. See claim 3 in Ground 1. *Yun* discloses that the rear surface of the solar cell is textured by platform-shaped (i.e., non-pyramid-shaped) structures which have polygonal planes. EX1005, Figure 2. A POSITA would have recognized that the polygonal plane can be a diamond, a square, a trapezoid or a substantial diamond/square/trapezoid. Moreover, at least a number of the polygonal surfaces in Figure 2 are diamonds, squares, trapezoids, or substantially one of those shapes.

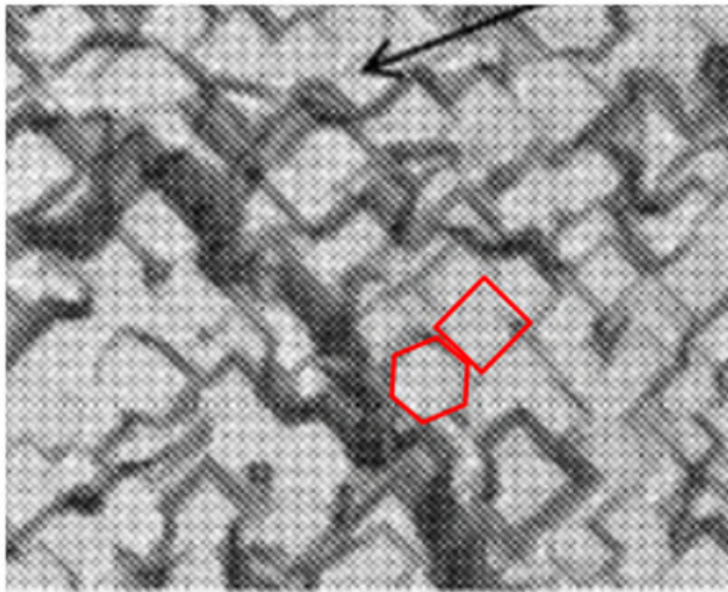


EX1005, Figure 2.

- d. **Claim 5: “the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm .”**

154. See claim 5 in Ground 1. *Yun* discloses the solar cell has a textured rear surface with “platform-shaped substructures,” which a POSITA would have

understood that it is “non-pyramid-shaped substructures” for the rear surface texture. EX1005, Abstract; Claim 1; *see also*, Figures 1-2. As shown in Figure 2, the highlighted platform-shaped substructures do not stack on one another. *Id.* [0007]. *Yun* discloses that each of these terms indicates that the bottoms of adjacent platform structures do not overlap each other. *Id.*, [0010]. A POSITA would understand this disclosure as describing platform structures that are not stacked on one another. Moreover, as shown in Figure 2, the highlighted platform-shaped substructures do not stack on one another. *Id.*



EX1005, Figure 2 (annotated).

155. Furthermore, *Yun* discloses “[e]ach platform structure has a lower plane connected to the silicon substrate and an upper plane opposite to the lower plane.” The upper plane of the platform corresponds to the top surface of the non-pyramid

substructure on the rear side of the solar cell as claimed in the '136 Patent. *Yun* further discloses “the side length of the upper plane is 2 to 10 μm ,” referring to the upper plane of each platform structure. That means that the top surface of each platform-shaped substructures (i.e., the top surface of the non-pyramid substructure) have a one-dimensional size less than 45 μm . *Id.*, Abstract.

e. **Claim 6: “the top surface of the second substructure is a polygonal plane.”**

156. See claim 6 in Ground 1 and claim 5 in this ground. This claim depends from claim 5, which is discussed above. *Yun* discloses the marked top surfaces of the non-pyramid substructures is a polygonal plane. Ex1005, Figure 2.

f. **Claim 7**

i. **Claim 7[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

157. See claim 7[a] in Ground 1 and claim 1[f], this ground. For the same reasons discussed with regard to claim 7[a] in Ground 1 and claim 1[f] in this ground, the combination of *Ye*, *Basu Paper*, and *Yun* discloses or renders obvious claim 7[a].

ii. **Claim 7[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”**

158. See claim 7[b] in Ground 1 and claim 1[f], this ground. For the same reasons discussed with regard to claim 7[b] in Ground 1 and claim 1[f] in this

ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 7[b].

g. Claim 8

i. Claim 8[a]: “the second passivation layer includes at least one of a silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and”

159. See claim 1[h], this ground. *Ye* discloses that the passivation layer on the rear surface is “a SiN passivation layer.” EX1005, ¶¶ 0030, 0034. *Yun* discloses that the front passivation antireflection dielectric layer (3) and the back passivation antireflection dielectric layer 7 are respectively composed of single-layer film or multi-layer film, which can be “made of silicon oxide, silicon nitride, silicon oxynitride ...,” amongst other things EX1005, Claim 2.

ii. Claim 8[b]: “the second passivation layer has a thickness ranging from 70 nm to 120 nm.”

160. *Ye* is silent on the thickness of the passivation layer on the rear surface. However, *Yun* discloses that “the back passivation antireflection dielectric layer 7 is a single layer film made of silicon nitride, with a film thickness of 70 to 80 nm,” which falls within the claimed range. EX1004, ¶ 0034; *see also id.* ¶¶ 0030, 0046 (“[t]he front passivation antireflection dielectric layer 3 is a single-layer film made of silicon nitride with a thickness of 70 to 80 nm.”). The back passivation antireflection dielectric layer 7 of *Yun* performs a very similar function to the rear

surface passivation layer in *Ye* and is made of the same silicon nitride material. As noted in my discussion of the technology background in Section IX above, POSITAs recognized that passivation layers and antireflective coatings perform similar functions. See EX1024 at 967 (“SiNx film as AR coating as well as a surface passivation layer plays an important role in commercial mc-Si solar cells”); EX1025 at 2326 (“In photovoltaic industries, SiNx:H ARC is often deposited after texturing in order to increase light collection and to passivate silicon surface”). This is true of passivation layers and ARCs on the front or rear side of a solar cell. Therefore, a POSITA would have found it obvious to make the passivation layer on the rear surface of the cell in *Ye* to have a thickness in the range disclosed for the passivation layer on the rear surface of the cell in *Yun*.

h. Claim 9: “the first passivation layer includes at least one of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer or a silicon oxynitride layer.”

161. See claim 9 in Ground 1 and discussion of claim 1[e] in this ground. For the same reasons discussed with regard to claim 9 in Ground 1 and claim 1[e] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 9.

i. **Claim 12**

i. **Claim 12[a]: “the semiconductor substrate is an N-type monocrystalline silicon substrate,”**

162. See claim 12[a] in Ground 1. *Yun* also discloses that the semiconductor wafer (substrate) is an N-type single-crystal silicon. EX1005, ¶ 0034 (“This embodiment describes the application of the present invention to N-type single-crystal silicon. As shown in FIG1, a front pyramid-shaped textured surface 1, ... a front electrode 4 are sequentially formed on the front side of the N-type single-crystal silicon substrate 100). A POSITA would have understood that the “N-type single-crystal silicon substrate” is “an N-type monocrystalline silicon substrate.”

ii. **Claim 12[b]: “the doped conductive layer is an N-type doped polycrystalline silicon layer, an N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer, and”**

163. See claim 12[a] in Ground 1 and discussion of claim 1[g], this ground. *Yun* also discloses that the rear surface includes a phosphorus-doped back surface field, which corresponds to a doped conductive layer. EX1005, ¶ 0034 (“This embodiment describes the application of the present invention to N-type single-crystal silicon. As shown in FIG. 1, a front pyramid-shaped textured surface 1, ... a front electrode 4 are sequentially formed on the front side of the N-type single-crystal silicon substrate 100). A POSITA would have understood that the doped

conductive layer of the rear surface can be N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer.

iii. Claim 12[c]: “the doped conductive layer has a thickness ranging from 60 nm to 200 nm.”

164. See claim 12[c] in Ground 1 and discussion of claim 1[g], this ground. For the same reasons discussed with regard to claim 12[c] in Ground 1 and claim 1[g] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 9.

j. Claim 13

i. Claim 13[p]: “A photovoltaic module, comprising a plurality of solar cell strings, wherein each of the plurality of solar cell strings comprises solar cells, and at least one of the solar cells comprise:”

165. See claim 1[p] in this ground. *Yun* also discloses a “photovoltaic power generation system based on bifacial solar cells.” EX1005, ¶ 0002. A POSITA would have understood that the “photovoltaic power generation system based on bifacial solar cells” would correspond to a module with a plurality of solar cells or solar cell strings. Moreover, in order to generate a sufficient amount of electricity for most applications, a POSITA would understand that any solar cell must be used together with a plurality of solar cells assembled into one or more strings to form a photovoltaic module or solar panel. Therefore, claim 13[p] is taught or rendered obvious by each of *Ye*, *Yun*, and Basu Paper.

ii. Claim 13[a] “a semiconductor substrate,”

166. See claim 1[a] in this ground. For the same reasons discussed with regard to claim 1[a] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 13[a].

iii. Claim 13[b] “wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another, a top surface of the first substructure is a polygonal plane, and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ; and”

167. See claim 1[b] in this ground. For the same reasons discussed with regard to claim 1[b] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 13[b].

- iv. **Claim 13[c] “wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and”**

168. See claim 1[c] in this ground. For the same reasons discussed with regard to claim 1[c] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 13[c].

- v. **Claim 13[d] “in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm ,”**

169. See claim 1[d] in this ground. For the same reasons discussed with regard to claim 1[d] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 13[d].

- vi. **Claim 13[e] “a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate;”**

170. See claim 1[e] in this ground. For the same reasons discussed with regard to claim 1[e] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 13[e].

vii. Claim 13[f] “a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;”

171. See claim 1[f] in this ground. For the same reasons discussed with regard to claim 1[f] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 13[f].

viii. Claim 13[g] “a doped conductive layer located on a surface of the tunnel oxide layer; and”

172. See claim 1[g] in this ground. For the same reasons discussed with regard to claim 1[g] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 13[g].

ix. Claim 13[h] “a second passivation layer located on a surface of the doped conductive layer.”

173. See claim 1[h] in this ground. For the same reasons discussed with regard to claim 1[h] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 13[h].

- k. **Claim 14 “The photovoltaic module according to claim 13, wherein for the two or more first substructures at least partially stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, a distance between the top surface of the outermost first substructure and the top surface of the adjacent first substructure is equal to or less than 2 μm .”**

174. See claim 2 in this ground. For the same reasons discussed with regard to claim 2 in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 14.

- l. **Claim 15 “The photovoltaic module according to claim 13, wherein a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a substantially trapezoid”**

175. See claim 3 in this ground. For the same reasons discussed with regard to claim 3 in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 15.

- m. **Claim 17 “The photovoltaic module according to claim 13, wherein the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm .”**

176. See claim 5 in this ground. For the same reasons discussed with regard to claim 5 in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 17.

- n. **Claim 18 “The photovoltaic module according to claim 17, wherein the top surface of the second substructure is a polygonal plane.”**

177. See claim 6 in this ground. For the same reasons discussed with regard to claim 6 in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 18.

- o. **Claim 19**

- i. **Claim 19[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

178. See claim 7[a] in this ground. For the same reasons discussed with regard to claim 7[a] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 19[a].

- ii. **Claim 19[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”**

179. See claim 7[b] in this ground. For the same reasons discussed with regard to claim 7[b] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 19[b].

p. **Claim 20**

- i. **Claim 20[a]: “the second passivation layer includes at least one of a silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and”**

180. See claim 8[a] in this ground. For the same reasons discussed with regard to claim 8[a] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 20[a].

- ii. **Claim 20[b]: “the second passivation layer has a thickness ranging from 70 nm to 120 nm.”**

181. See claim 8[b] in this ground. For the same reasons discussed with regard to claim 8[b] in this ground, the combination of *Ye*, Basu Paper, and *Yun* discloses or renders obvious claim 20[b].

XIII. GROUND 2: CLAIMS 2, 5, 14, AND 17 ARE RENDERED OBVIOUS BY YE IN VIEW OF BASU PAPER AND XIA.

A. RATIONALE FOR COMBINING YE, BASU PAPER, AND XIA

182. For the same reasons in Ground 1, a POSITA would be motivated to combine *Ye* and Basu Paper. *Xia* also relates to optimizing solar cell design, and specifically is concerned with the problem of improving existing alkaline-based methods for polishing crystalline silicon surfaces of solar cells (including TOPCon cells), which improves the cell’s conversion efficiency. EX1006, ¶¶ 0001-0002, 0055. Therefore, *Xia* is not only in the same field of solar cell design as the ’136 Patent, but also concerns the same problem of optimizing the cell’s texture surfaces

to improve its efficiency as the '136 Patent. EX1006, ¶¶ 0001-0002. Therefore, *Xia* is analogous art to the '136 Patent.

183. *Ye* describes that one issue with PECVD techniques used in manufacturing TOPcon solar cells. Is that, to reduce the sheet resistance of the polysilicon thin-film layer, the thickness of the amorphous silicon films must be increased. However, excessively thick amorphous silicon films are prone to delaminate during high-temperature crystallization, which leads to deterioration in the passivation performance. EX1004, [0008]. *Ye* addresses this problem by providing a specific process for preparing the laminated thin-film passivated contact structure with optimized layer thickness and improved adhesion and mechanical strength. *Id.* [0011]-[0015], [0020]. *Xia* describes a method of polishing the silicon wafer surface, which is an upstream step to *Ye*'s process on preparing the TOPCon structure. EX1006, [0002]. *Xia* states that a polished, flat back surface "can effectively improve the uniformity of the back passivation coating and improve the passivation effect." *Id.* As discussed earlier, *Ye* teaches the importance of good adhesion between the silicon oxide layer and subsequent thin films to prevent delamination. EX1004, [0020]. As such, a POSITA would recognize that a smoother, more uniform substrate (achieved by *Xia*) would provide a better foundation for *Ye*'s laminated film structure and would have been motivated to combine *Xia* and *Ye* to further improve the quality of solar cells.

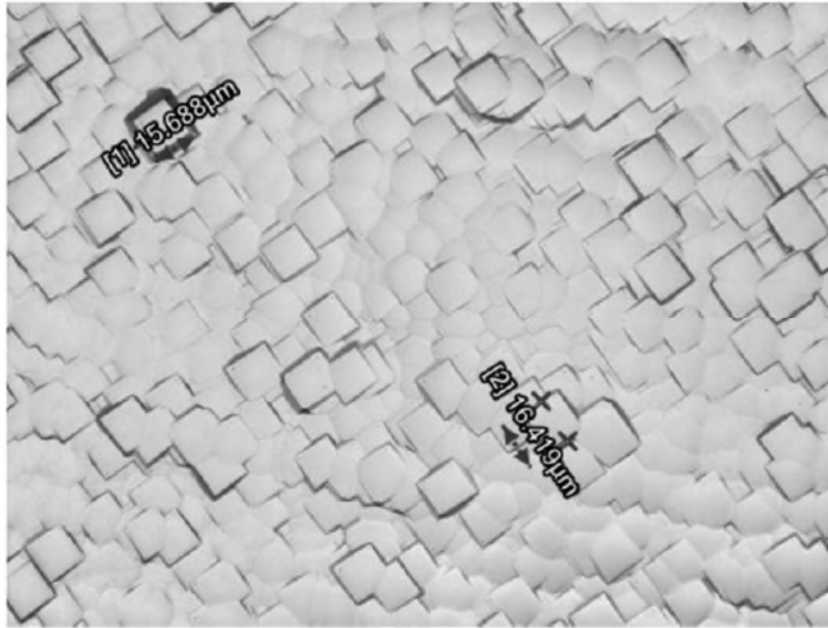
184. Furthermore, since *Xia* and *Ye* address an upstream step and downstream step of the same manufacturing process of TOPCon solar cells (EX1006, [0002]), a POSITA would naturally consider combining these sequential process steps by using the polishing method in *Xia* to further improve the adhesion and mechanical strength of the TOPCon structures in *Ye*. In other words, *Xia* solves surface roughness and defect problem at the silicon wafer level; *Ye* solves delimitation problems at the passivation film level. EX1006, [0002]; EX1004, [0008], and a POSITA would understand that solving problems at both levels would yield cumulative improvement in solar cells. As such, POSITAs would be motivated to combine *Xia* and *Ye* to optimize the manufacturing process and improve the quality of solar cells.

185. As discussed earlier, because *Xia* and *Ye* address different steps of the same process for manufacturing TOPCon solar cells, a POSITA would have no problem to first use *Xia*'s method in polishing the silicon wafer, then to use *Ye*'s method in preparing the TOPCon structures. Since *Xia* and *Ye*'s methods generally use similar types of processes for manufacturing TOPCon solar cells, a POSITA would have reasonable expectation the combination of *Xia* and *Ye* would succeed. Based on the above, POSITAs would have been motivated to combine the teachings of *Ye*, Basu Paper, and *Xia* to manufacture solar cells with improved quality, as claimed in the '136 Patent. POSITAs would have reasonable expectation of success

in combining *Ye*, Basu Paper, and *Xia*, to reach the invention claimed in the '136 Patent because inventions in *Ye* and *Xia* use compatible N-type monocrystalline silicon wafers and target similar solar cell architecture (i.e., the combination involves no incompatible materials or processes) and Basu Paper is merely optimization of another aspect of the solar cell (i.e., the pyramid height).

- a. **Claims 2 and 14 “wherein for the two or more first substructures at least partially stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, a distance between the top surface of the outermost first substructure and the top surface of the adjacent first substructure is equal to or less than 2 μm .”**

186. *Xia* discloses that the silicon wafers typically have a surface roughness of about 10-20 μm and a pre-polishing step can reduce it to 1-3 μm . *Id.* ¶ 0007. Figure 1 shows a microscopy image of the polished surface on the rear side of the solar cell wafer resulting from the polishing method in *Xia*. *Id.*, Figure 1. The rear-side polished surface has at least some non-pyramid substructures that, at least based on Patent Owner’s interpretation of the '136 Patent claims, are stacked on one another. *Id.*

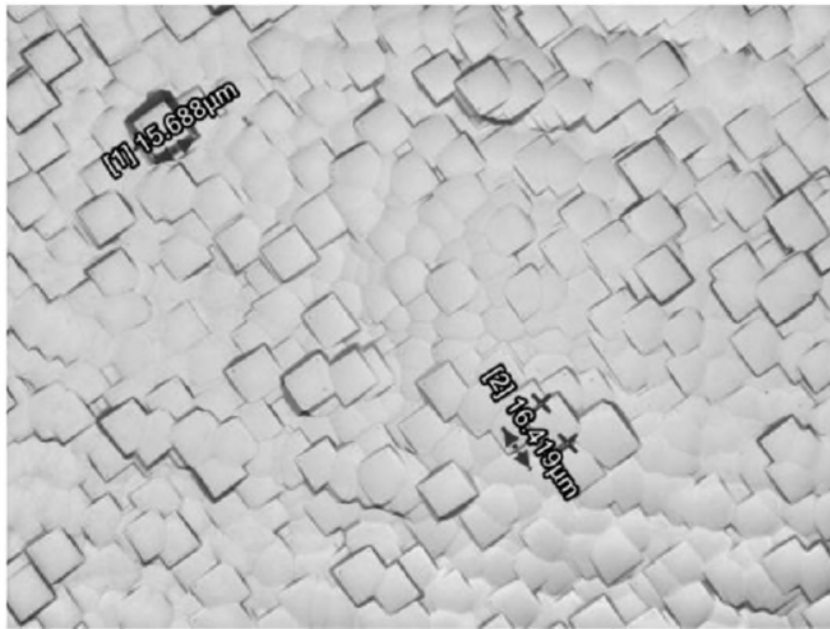


EX1006, Figure 1. *Xia* discloses that “[t]he silicon wafer obtained after polishing has high surface flatness and few surface defects.” *Id.* ¶ 0024. A POSITA would have understood these teachings to disclose or suggest polishing the rear wafer surface such that the distance away from and perpendicular to the rear substrate surface between the top surface of the outermost first substructure and the top surface of the adjacent first substructure would be equal to or less than 2 μm. *Id.*

- b. **Claims 5 and 17 “wherein the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm.”**

187. Figure 1 shows a microscopy image of the polished crystalline silicon that resulted from the polishing method in *Xia*. *Id.*, Figure 1. The polished surface has “uniform and smooth square structures” with approximately the same size of

about 15 to 16 μm . *Id.* ¶ 0033. Figure 1 of *Xia* shows a microscopy image of the polished crystalline silicon resulted from the polishing method in *Xia. Id.*, Figure 1. As shown in Figure 1, the polished surface on the rear-side wafer of the solar cell further has two or more adjacent second substructures that do not stack on one another. *Id.*, Figure 1. *Xia* discloses that the polished surface has “uniform and smooth square structures” with approximately the same size of about 15 to 16 μm , which is less than 45 μm . *Id.* ¶ 0033. Figure 1 also shows that the one-dimensional size of a top surface of the substructure away from the rear-side wafer surface is less than 45 μm . *Id.*



EX1006, Figure 1.

c. **Claims 6 and 18 “wherein the top surface of the second substructure is a polygonal plane.”**

188. See claims 5 and 17 in this ground. This claim depends from claim 5, which is discussed above. Figure 1 of *Xia* shows the polished rear-side surface of the solar cell wafer, which, according to *Xia*, has “uniform and smooth square structures.” *Id.* ¶ 0033. Figure 1 also shows the rear-side wafer surface has substructures with their top surfaces being substantially square, which is a type of polygonal shape. *Id.*, Figure 1. Figure 1 also shows the rear-side wafer surface has at least some substructures having their top surfaces in non-square polygonal shapes. *Id.*



EX1006, Figure 1.

XIV. GROUND 3: CLAIMS 7, 9, AND 19 ARE RENDERED OBVIOUS BY YE IN VIEW OF BASU PAPER, AND CHANG

A. RATIONALE FOR COMBINING YE, BASU PAPER, AND CHANG

189. For the same reasons discussed in Ground 1, a POSITA would be motivated to combine *Ye* and Basu Paper. *Chang* also relates to the fields of solar cells and specifically a TOPCon solar cell (*i.e.*, cell having a tunneling layer) with optimized and improved efficiency. EX1023, Abstract, 1:16-20. Chang is also specifically concerned with the problem of avoiding defects and damage on the back surface of the semiconductor substrate (*i.e.*, by optimizing the tunnel oxide layer on the back surface) to improve the cell's efficiency. EX1023 at 1:45-2:3. Therefore, *Chang* is not only in the same field of manufacturing solar cells as the '136 Patent, but also concerns the same problem of surface defects and recombination sites on semiconductor substrates that reduce solar cell efficiency, as the '136 Patent. Therefore, *Chang* is analogous art to the '136 Patent.

190. Like *Ye*, *Chang* teaches a TOPCon solar cell having rear tunneling layers on a silicon substrate to enable passivation and carrier tunneling, specifying materials including silicon oxide, silicon nitride, and silicon oxynitride with a tunneling layer thickness of about 0.5–2 nm. EX1004, Abstract, [0002], [0004], [0013]; EX1023, 5:21-27, 5:30-34, 7:8-15. In both references, a rear polySi back surface field is formed on the tunneling layer. *Id.* And in both references, the passivation/antireflective films may include dielectrics such as Al₂O₃, HfO₂, SiO_x,

SiNx, and SiON, and the tunneling layers can be formed by thermal growth, PECVD, or ALD. EX1004, [0031], [0038]; EX1023, 5:21-27, 5:30-34, 6:30-37, 7:8-15. As noted in my discussion of the technology background in Section IX above, a POSITA would be aware that a tunnel oxide passivation (TOP) layer must be thin enough to be tunneled through but should also passivate the semiconductor surface. Therefore, a POSITA would have recognized that thickness as a result-effective variable. Because layer thickness optimization is a routine engineering problem in solar cell design and manufacturing, POSITAs would have found it obvious to consider *Chang's* teachings regarding the tunnel layer thickness and apply them to the tunnel oxide layer of *Ye* to modify its thickness.

191. Furthermore, the solar cells in *Chang* and *Ye* share the same structural features and manufacturing methods where delimitation may occur. For example, *Chang* and *Ye* have silicon oxide layers within the similar thickness range (*Chang* has a silicon oxide layer of 0.5-5 nm (preferably 0.5-2 nm); *Ye* has a silicon oxide layer of 1.0-3.5 nm). EX1023, 7:10-20; EX1004, [0013]. Both *Chang* and *Ye* have polycrystalline silicon back surface after crystallization. EX1004, [0011]; EX1023, 1:60-65. Both *Chang* and *Ye* use the same PECVD-based deposition method. EX1004, [0006]; EX1023, 20:26-31. A POSITA would be motivated to combine *Chang* with *Ye* to create solar cells with improved quality and mechanical strength.

Because they concern the same PECVD method, a POSITA would have reasonable expectation of success in combining *Chang* with *Ye*.

192. Based on the above, POSITAs would have been motivated to combine the teachings of *Ye*, Basu Paper, and *Chang* to manufacture solar cells with improved quality, as claimed in the '136 Patent. POSITAs would have reasonable expectation of success in combining *Ye*, Basu Paper, and *Chang*, to reach the invention claimed in the '136 Patent because both *Ye* and *Chang* use the PECVD-based methods in manufacturing solar cells and the resulting solar cells have similar structural features where delamination could occur, and Basu Paper is merely optimization of another aspect of the solar cell (i.e., the pyramid height). A POSITA would be motivated to combine *Chang* with *Ye* and Basu Paper to create solar cells with improved efficiency using a cleaner and simpler manufacturing method.

a. **Claims 7 and 19**

- i. **Claim 7[a] and 19[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

193. See claims 7[a] and 19[a] in Ground 1. *Chang* also teaches rear tunneling layers on a silicon substrate to enable passivation and carrier tunneling, specifying materials including silicon oxide, silicon nitride, and silicon oxynitride with a tunneling layer thickness of about 0.5–2 nm (more generally 0.5–5 nm).

EX1023, 5:21-27; 5:30-34; 7:8-15. A rear polySi back surface field is formed on the tunneling layer, while passivation/antireflective films may include dielectrics such as Al₂O₃, HfO₂, SiO_x, SiN_x, and SiON, and the tunneling layers can be formed by thermal growth, PECVD, or ALD. *Id.* As such, *Chang* discloses the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer.

ii. Claim 7[b] and 19[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”

194. See claim 7[b] and 19[b] in Ground 1. *Chang* teaches rear tunneling layers including silicon oxide, silicon nitride, and silicon oxynitride with a tunneling layer thickness of 0.5–2 nm, which encompasses the claimed range of 0.8 nm to 2 nm. EX1023, 5:21-27; 5:30-34; 7:8-15.

195. Alternatively, based on *Chang*’s teaching, it would have been obvious for a POSITA to make the tunnel oxide layer of *Ye* with a thickness within the claimed range. As noted in my discussion of the technology background in Section IX above, a POSITA would be aware that a tunnel oxide passivation (TOP) layer must be thin enough to be tunneled through but should also passivate the semiconductor surface. Therefore, a POSITA would have recognized that thickness as a result-effective variable. For example, a tunneling layer much thicker than 2 nm, e.g. 20 nm, would be too thick for an efficient quantum-mechanical tunneling

process. On the other hand, to effectively passivate the semiconductor surface, a tunnel oxide passivation (TOP) layer should be at least 0.5 nm thick. This puts the preferable range of the TOP layer between 0.5 nm and a few nm. In addition, the contact area also plays a role, with larger contact areas allowing for thicker TOP layers, and smaller contact areas requiring thinner TOP layers, to keep the contact resistance low. A POSITA would understand that any of the ranges, such as 0.5 to 2.0 nm, 1.0 to 2.0 nm, or 1.0 to 3.0 nm, would be a preferred TOP layer thickness range. Moreover, selecting a thickness within this range would have been a routine engineering task for a POSITA. Given the finite range of thicknesses disclosed in *Chang*, and that only a small portion of *Chang*'s disclosed thickness range falls below the claimed range, a POSITA would have found it obvious to select a tunnel oxide layer with a thickness of 0.8 nm - 2 nm.

b. **Claim 9: “the first passivation layer includes at least one of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer or a silicon oxynitride layer.”**

196. See claim 9 in Ground 1. *Chang* discloses the “first passivation film 21” as including any of SiNx, hydrogenated SiNx, SiOx, SiON, Al2O3. EX1023, 6:30-37. Thus, *Chang* discloses that supporting that the passivation layer includes at least one of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer or a silicon oxynitride layer. *Id.*

XV. GROUND 3A: CLAIMS 7, 9, AND 19 ARE RENDERED OBVIOUS BY YE IN VIEW OF BASU PAPER, YUN, AND CHANG

197. For the same reasons discussed in Grounds 1A and 3, POSITAs would have found it obvious to combine *Ye*, *Basu*, *Yun*, and *Chang*. There is nothing about the teachings of *Yun* discussed in Ground 1A that would change the reasons for a POSITA to combine *Chang* with *Ye* and *Basu* as discussed in Ground 3.

198. Moreover, as discussed in Grounds 1A and 2, *Ye* in view of *Basu*, *Yun*, and *Chang* renders Claims 7, 9, and 19 obvious.

XVI. GROUND 4: CLAIM 10 IS RENDERED OBVIOUS BY YE IN VIEW OF BASU PAPER AND YU

A. RATIONALE FOR COMBINING YE, BASU PAPER, AND YU PAPER

199. As discussed above, the '136 Patent, *Ye* and *Basu* Paper both relate to the field of solar cells generally, and more specifically to optimizing solar cell design (e.g., of TOPCon solar cells) to improve efficiency (e.g., by using textured front and back surfaces). *Ye* specifically refers to TOPCon solar cells as an example of the type of solar cells improved by these optimizations. EX1004, ¶ 0003-0008. *Yu* Paper also relates to the field of solar cells, and more specifically to optimizing the design of a TOPCon solar cell. EX1016, Abstract. As such, *Ye*, *Basu* Paper, and *Yu* Paper all relate to the same field as the '136 Patent, and are therefore analogous art to each other and to the '136 Patent. EX1001, 1:41-46; 4:13-17; 5:44-55; EX1004, ¶¶ 0008-0009; EX1012, at 590; EX1016, Abstract.

200. *Ye* describes TOPCon solar cells having a textured front side that is passivated with $\text{Al}_2\text{O}_3/\text{SiN}$ passivation layers formed on the front surface, but is silent on the thicknesses of those layers. *Yu Paper* states that it “focuses on the optimized design of the front surface TOPCon layer” of a bifacial TOPCon solar cell and the performance of the solar cell based on that optimization. Part of that optimization of the front surface includes the use of a front side passivation layer. *Yu Paper*’s front side passivation layer is also a bilayer film made of the same sublayers and materials disclosed in *Ye*. Such sequential stacks were also well known in passivation layers in solar cells before the ’136 Patent. Therefore, a POSITA would have considered *Yu Paper*’s front side passivation layer to be substantially similar to *Ye*’s and thus would have considered *Yu Paper*’s teachings regarding the structure and thickness of the $\text{Al}_2\text{O}_3/\text{SiN}$ sublayers in designing *Ye*’s front passivation layer.

201. Moreover, a POSITA would be motivated to make the aluminum oxide layer of *Ye* or *Yun* as thin as possible while still providing effective passivation, for example, in order to reduce the amount of materials needed for manufacturing and minimize the size and weight of the solar cell. And *Yu Paper* teaches that an aluminum oxide layer as thin as 5 nm was effective to passivate the front side of the solar cell. Passivation layers composed of bilayer films with aluminum oxide layers of this thickness also would have been well known to POSITAs. See, e.g., EX1034, [0085] (disclosing composite passivation films that include aluminum oxide sub-

layers that are 5-15 nm thick); EX1039, 10:22-31 (disclosing a passivation layer that includes an aluminum oxide layer 17 “in a range of 4 nm to 20 nm”, specifying 5 nm and 10 nm as examples); EX1036, [0032] & Figure 2 (disclosing an n-type PERT solar cell having a “boron doped surface passivation layer” 14 that “is a laminated passivation layer consisting of aluminum oxide and silicon nitride, wherein the thickness of the aluminum oxide is about 5nm, the thickness of the silicon nitride is about 75nm”).

202. A POSITA would have had a reasonable expectation of success in using the thicknesses of the front passivation sub-layers disclosed in Yu Paper to the solar cells in Ye because it uses a known method (thicknesses of Yu Paper’s Al₂O₃/SiN bilayer film) to obtain predictable results (i.e., forming a passivation layer for the front surface of a TOPCon solar cell).

a. **Claim 10**

i. **Claim 10[a]: “the first passivation layer is a stacked passivation structure of an aluminum oxide layer and a silicon nitride layer,”**

203. See discussion of claim 1[e] in Ground 1. Yu Paper describes fabricating TOPCon solar cells in which the front side of the cell “was passivated by 5 nm AlO_x and 75 nm SiN_x.” EX1016 at 3 (Section 2.2.1 (describing solar cell “with front conventional n-PERT structure and rear TOPCon structure); *see also id.*, 4 (Section 2.2.2, describing solar cell with front selective and rear total TOPCon

structure and that “[t]he subsequent steps, including AlO_x and SiN_x layers deposition, as well as metallization are the same with the upper cells.”). As shown in Figure 4, the silicon nitride sub-layer (SiN_x, blue below) is stacked on top of the aluminum oxide sub-layer (Al₂O₃, in yellow below).

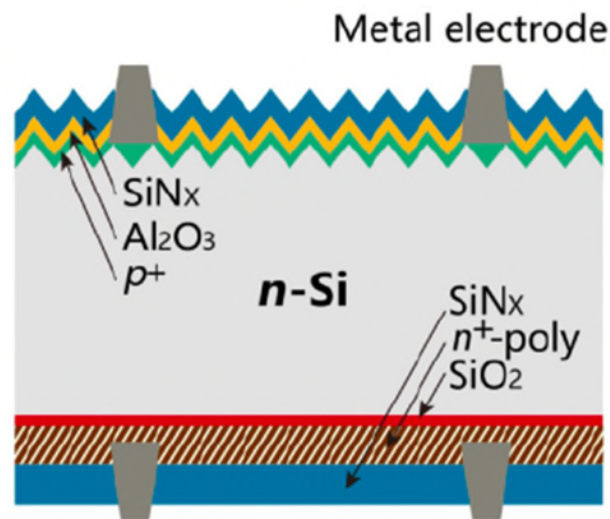


Fig. 4. Solar cell con

204. Therefore, Yu Paper discloses a stacked passivation structure of an aluminum oxide layer and a silicon nitride layer. A POSITA would have found it obvious to use a similar stack of aluminum oxide and silicon nitride sublayers in the front passivation layer of Ye.

ii. Claim 10[b]: “the aluminum oxide layer has a thickness ranging from 2 nm to 10 nm, and”

205. The AlO_x sublayer of Yu Paper’s passivation layer has a thickness of 5 nm, which falls within the range claimed in claim 10[b]. In view of Yu Paper’s

teachings, a POSITA would have found it obvious to make the aluminum oxide layer in the front passivation layer of *Ye* of the same or similar thickness as Yu Paper within the claimed range.

iii. Claim 10[c]: “the silicon nitride layer has a thickness ranging from 50 nm to 110 nm.”

206. The SiN_x sublayer of Yu Paper’s passivation layer has a thickness of 75 nm, which falls within the range claimed in claim 10[c]. In view of Yu Paper’s teachings, a POSITA would have found it obvious to make the silicon nitride layer in the front passivation layer of *Ye* of the same or similar thickness as Yu Paper within the claimed range.

XVII. GROUND 4A: CLAIM 10 IS RENDERED OBVIOUS BY YE IN VIEW OF BASU PAPER, YUN, AND YUN PAPER

A. RATIONALE FOR COMBINING YE, BASU PAPER, YUN, AND YU PAPER

207. As discussed in Ground 4 above, *Ye*, Basu Paper, and *Yun* are analogous art to the ’136 patent. As discussed in Section VIII above, Yu Paper is also analogous art to the ’136 Patent.

208. Similar to *Ye*, *Yun* describes solar cells having a front passivation layer that may be, for example, a bilayer film made of aluminum oxide and silicon nitride. EX1005, [0034]. *Yun* gives ranges of thicknesses for the aluminum oxide and silicon nitride sub-sublayers, and the ranges for the aluminum oxide sublayer are slightly thicker than the thickness recited in claim 10.

209. Yu Paper states that it “focuses on the optimized design of the front surface TOPCon layer” of a bifacial TOPCon solar cell and the performance of the solar cell based on that optimization. Part of that optimization of the front surface includes the use of a front side passivation layer. Yu Paper’s front side passivation layer is also a bilayer film made of the same sub-layers and materials disclosed in *Ye* and *Yun*. Such sequential stacks were also well known in passivation layers in solar cells before the ’136 Patent. Therefore, a POSITA would have considered Yu Paper’s front side passivation layer to be substantially similar to *Ye*’s and *Yun*’s and thus would have considered Yu Paper’s teachings regarding the structure and thickness of the $\text{Al}_2\text{O}_3/\text{SiN}$ sublayers in designing *Ye*’s or *Yun*’s front passivation layer. Moreover, a POSITA would be motivated to make the aluminum oxide layer of *Ye* or *Yun* as thin as possible while still providing effective passivation, for example, in order to reduce the amount of materials needed for manufacturing and minimize the size and weight of the solar cell. And Yu Paper teaches that an aluminum oxide layer as thin as 5 nm was effective to passivate the front side of the solar cell.

210. Passivation layers composed of bilayer films with aluminum oxide layers of this thickness also would have been well known to POSITAs. *See, e.g.*, EX1034, [0085] (disclosing composite passivation films that include aluminum oxide sub-layers that are 5-15 nm thick); EX1039, 10:22-31 (disclosing a passivation

layer that includes an aluminum oxide layer 17 “in a range of 4 nm to 20 nm”, specifying 5 nm and 10 nm as examples); EX1036, [0032], Figure 2 (disclosing an n-type PERT solar cell having a “boron doped surface passivation layer” 14 that “is a laminated passivation layer consisting of aluminum oxide and silicon nitride, wherein the thickness of the aluminum oxide is about 5nm, the thickness of the silicon nitride is about 75nm”). *see also* EX1015, 96-100.

211. A POSITA would have had a reasonable expectation of success in using the thicknesses of the front passivation sub-layers disclosed in Yu Paper to the solar cells in *Ye* and *Yun* because it uses a known method (thicknesses of Yu Paper’s Al₂O₃/SiN bilayer film) to obtain predictable results (i.e., forming a passivation layer for the front surface of a TOPCon solar cell).

a. Claim 10

i. Claim 10[a]: “the first passivation layer is a stacked passivation structure of an aluminum oxide layer and a silicon nitride layer,”

212. See discussion of claim 1[e] in Ground 1A. Yu Paper describes fabricating TOPCon solar cells in which the front side of the cell “was passivated by 5 nm AlO_x and 75 nm SiN_x.” EX1016 at 3 (Section 2.2.1 (describing solar cell “with front conventional n-PERT structure and rear TOPCon structure); *see also id.*, 4 (Section 2.2.2, describing solar cell with front selective and rear total TOPCon structure and that “[t]he subsequent steps, including AlO_x and SiN_x layers

deposition, as well as metallization are the same with the upper cells.”). As shown in Figure 4, the silicon nitride sub-layer (SiN_x , blue below) is stacked on top of the aluminum oxide sub-layer (Al_2O_3 , in yellow below).

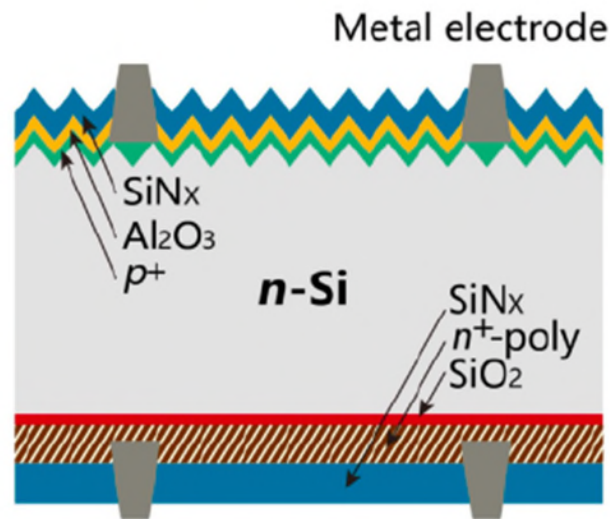


Fig. 4. Solar cell con

213. Therefore, Yu Paper discloses a stacked passivation structure of an aluminum oxide layer and a silicon nitride layer. A POSITA would have found it obvious to use that stack of aluminum oxide and silicon nitride sublayers in the front passivation layer of Ye and/or Yun.

214. Ye also discloses a stacked $\text{Al}_2\text{O}_3/\text{SiN}$ passivation structure on the front side. EX1004, ¶ 0038 (“ $\text{Al}_2\text{O}_3/\text{SiN}$ passivation layers are formed on the front surface, and a SiN passivation layer is formed on the rear surface”). A POSITA would have understood that Al_2O_3 means an aluminum oxide layer, and SiN means a silicon nitride layer, and thus the front passivation layer has a stacked structure of

an aluminum oxide layer and a silicon nitride layer on top of that. To the extent the claim so requires, a POSITA would have found it obvious to provide the stacked layers of Ye's passivation layer with aluminum oxide layer on top of and in contact with the substrate surface, and the silicon nitride layer. That is only one of two possible sequences for the two layers, and so at least would have been obvious to try.

215. Such sequential stacks were also well known in passivation layers in solar cells before the '136 Patent. *See, e.g.*, EX1034 at [0077]-[0084] ("The rear composite film 3 has various embodiments. Referring to FIGS. 3, 4 and 5, the bottom layer of the rear composite film is an aluminum oxide film, and the top layer is composed of one or more of a silicon dioxide film, a silicon oxynitride film, and a silicon nitride film. ... Referring to FIGS. 6, 7 and 8, the bottom layer 31 of the rear composite film is a silicon dioxide film; the middle layer 32 of the rear composite film is an aluminum oxide film; and the top layer 33 is composed of one or more of a silicon dioxide film, a silicon oxynitride film, and a silicon nitride film.), EX1035 at 97 ("The emitter was passivated with a 10 nm thick Al₂O₃ layer deposited with plasma-assisted atomic layer deposition. The front side was additionally coated with a double-layer antireflection coating (DARC) consisting of 50 nm SiN_x grown by plasma-enhanced chemical vapor deposition (PECVD) and 90 nm thermally evaporated MgF₂.").

216. *Yun* also teaches a front passivation layer that is a bilayer film made of aluminum oxide and silicon nitride. EX1005, [0034]. To the extent the claim so requires, a POSITA would have found it obvious to provide the stacked layers of *Yun*'s front passivation layer with aluminum oxide layer on top of and in contact with the substrate surface, and the silicon nitride layer on top of that. That is only one of two possible sequences for the two layers, and so at least would have been obvious to try. Such sequential stacks were also well known in passivation layers in solar cells before the '136 Patent.

217. For example, *See, e.g.*, EX1034 at [0077]-[0084] ("The rear composite film 3 has various embodiments. Referring to FIGS. 3, 4 and 5, the bottom layer of the rear composite film is an aluminum oxide film, and the top layer is composed of one or more of a silicon dioxide film, a silicon oxynitride film, and a silicon nitride film. ... Referring to FIGS. 6, 7 and 8, the bottom layer 31 of the rear composite film is a silicon dioxide film; the middle layer 32 of the rear composite film is an aluminum oxide film; and the top layer 33 is composed of one or more of a silicon dioxide film, a silicon oxynitride film, and a silicon nitride film.), EX1035 at 97 ("The emitter was passivated with a 10 nm thick Al₂O₃ layer deposited with plasma-assisted atomic layer deposition. The front side was additionally coated with a double-layer antireflection coating (DARC) consisting of 50 nm SiN_x grown by

plasma-enhanced chemical vapor deposition (PECVD) and 90 nm thermally evaporated MgF₂.”).

218. *Yun* also teaches a back passivation layer that is a stacked passivation structure of an aluminum oxide layer and a silicon nitride layer. EX1005, ¶¶ 0030, 0034, 0046 (“the back passivation antireflection dielectric layer 7 is a double-layer film made of aluminum oxide and silicon nitride”); *see also id.*, [0032]. The rear passivation layer of *Yun* and front passivation layers of *Ye* and *Yun* are all made of the same materials (silicon nitride and aluminum oxide) and perform the same function (passivating a surface of a cell). Therefore, for the reasons similar to those discussed above with regard to claim 8[b], a POSITA would have found it obvious to apply *Yun*’s teachings regarding the passivation layer on the rear surface to *Ye*’s passivation structure on the front side.

ii. Claim 10[b]: “the aluminum oxide layer has a thickness ranging from 2 nm to 10 nm, and”

219. The AlO_x sublayer of Yu Paper’s passivation layer has a thickness of 5 nm, which falls within the range claimed in claim 10[b]. In view of *Yun*’s teachings, a POSITA would have found it obvious to make the aluminum oxide layer in the front passivation layer of *Ye* and/or *Yun* of the same or similar thickness as Yu Paper within the claimed range.

220. To the extent that making the aluminum oxide layer of *Yun* thinner might have made the overall front passivation layer of *Yun* approximately 10-15 nm thinner than the lower end of the range disclosed in *Yun*, a POSITA would have been able to make any adjustments appropriate in light of that change. For example, if a POSITA wanted to maintain the same total thickness of the passivation layer, a POSITA would have increased the thickness of the silicon nitride sub-layer in *Yun*'s front passivation layer by a similar amount. That would have made *Yun*'s silicon nitride sub-layer approximately 55-85 nm thick, which still would fall within the range recited in claim 10[c].

221. Furthermore, *Yun* discloses that the aluminum oxide layer has a thickness of 20 to 30 nm. EX1004, ¶ 0034; *see also, id.*, ¶¶ 0030, 0059. A POSITA would have found it obvious to modify the aluminum oxide layer thickness disclosed in *Yun* to be in the range of 2-10 nm because, as discussed below, passivation layer thickness optimization was recognized as a result-effective variable and selecting an appropriate thickness was a routine engineering problem in solar cell design.

222. Al_2O_3 , also denoted as alumina, when used in a solar cell may have multiple functions. EX1037, 2742-43. First, alumina can serve as a chemical passivation layer that protects a silicon surface and makes it resistant to chemical reactions such as oxidation and corrosion. EX1037, 2742. Second, alumina can serve as an anti-reflection coating (ARC), so that the incident sunlight enters the silicon

solar cell rather than being reflected by the silicon solar cell. The thickness of an ARC is guided by theory and well accepted to be $\lambda / (4 n)$, where λ is the wavelength of interest and n is the refractive index of the ARC material. EX1037, 2742–43. Third, alumina can serve as an electronic passivation layer that de-activates the electronic states associated with a silicon surface (dangling-bond states). By de-activating the silicon surface electronic states, electron-hole surface recombination can be reduced or suppressed. Since the electronic passivation concerns surface dangling bonds, a relatively thin electronic passivation layer, such as 10 nm to 20 nm, may be sufficient. *Id.*

223. Anti-reflection coatings typically have layer thicknesses of $\lambda/(4n)$ where λ is the light's wavelength of interest and n is the refractive index of the ARC. EX1021 at 684 (“However, the region of low reflectivity for a single-layer optical coating occurs at thickness of $\lambda/4n_1$ which cannot cover the entire absorption width over a 400–700 nm visible range.”). Therefore, a POSITA would have recognized the thickness of a passivation layer such as aluminum oxide layer as a result-effective variable. The refractive index of aluminum oxide is approximately 1.6~1.8. EX1037, Figure 1. For certain light wavelengths of interest (which typically ranges from 400 nm to 700 nm) and thicknesses of silicon nitride layers combined with the aluminum oxide layer, a thickness of 2-10 nm would be appropriate.

224. Therefore, such optimizations would have been routine engineering tasks for a POSITA designing a solar cell. *See also* EX1015 at 78-82 (describing examples of how to select materials and thicknesses for an ARC layer). And, several references teach passivation layers that include an aluminum oxide sublayer of a thickness in this range. *See* EX1016 at 3 (“The front boron emitter of the samples was passivated **by 5 nm AlO_x** and 75 nm SiN_x”); EX1035 at 97 (“The emitter was passivated with **a 10 nm thick Al₂O₃ layer** deposited with plasma-assisted atomic layer deposition.”); EX1034 at [0020] (“the thickness of the aluminum oxide film is 5-15 nm”); EX1030, 6:27-34 (“The second passivation layer 20 includes at least one aluminum oxide layer Al_xO_y When the at least one aluminum oxide layer is provided with a single layer (i.e., an aluminum oxide layer 17 shown in FIG. 1), a thickness of the aluminum oxide layer 17 is in a range of 4 nm to 20 nm. Particularly, the thickness of the aluminum oxide layer 17 is 5 nm, 10 nm, 15 nm or 20 nm”). Therefore, a POSITA would have found it obvious to modify the aluminum oxide layer thickness disclosed in *Yun* to fall within the claimed range.

iii. Claim 10[c]: “the silicon nitride layer has a thickness ranging from 50 nm to 110 nm.”

225. The SiN_x sublayer of Yu Paper’s passivation layer has a thickness of 75 nm, which falls within the range claimed in claim 10[c] and the range described in Yu Paper. In view of Yu Paper’s teachings, a POSITA would have found it

obvious to make the silicon nitride layer in the front passivation layer of *Ye* and/or *Yun* of the same or similar thickness as *Yu* Paper within the claimed range.

226. Furthermore, *Yun* discloses that the silicon nitride layer has a thickness of 50 to 70 nm, which falls within the claimed thickness range of 50 nm to 110 nm. EX1004, ¶ 0034; *see also, id.*, ¶¶ 0030, 0059. Basu Paper also discloses an amorphous SiN_x film with a thickness of 70 nm on the front surface, which falls within the claimed range. EX1006 at 591 (“Amorphous silicon nitride (SiN_x) ... deposited onto the front surface ... The film thickness ... 70 nm”). A POSITA would have understood that the thickness of the silicon nitride layer can be in the range of 50 nm to 100 nm.⁵

XVIII. GROUND 5: CLAIM 11 IS RENDERED OBVIOUS BY YE IN VIEW OF BASU PAPER AND FANG

A. RATIONALE FOR COMBINING YE, BASU PAPER, AND FANG

227. *Fang* also relates to the field of solar cells, and more specifically to solar cells that have a high photoelectric conversion efficiency, high appearance quality, and are simple to manufacture. EX1034, [0010]-[0011]. Therefore, *Fang* relates to the same field as the '136 Patent, and is therefore analogous art.

⁵ Regarding claim 10[b], to the extent making the aluminum oxide layer of *Yun* thinner might make the overall front passivation layer of *Yun* thinner than the lower end of *Yun*'s range, POSITAs would have made any appropriate adjustments.

228. As discussed above, the '136 Patent, *Ye* and Basu Paper both relate to the field of solar cells generally, and more specifically to optimizing solar cell design (e.g., of TOPCon solar cells) to improve efficiency. *Fang* also relates to the field of solar cells, and more specifically to provide solar cells that have a high photoelectric conversion efficiency, high appearance quality, and are simple to manufacture. EX1034, [0010]-[0011]. As such, *Ye*, Basu Paper, and *Fang* all relate to the same field as the '136 Patent, and are therefore analogous art to each other and to the '136 Patent. EX1001, 1:41-46; 4:13-17; 5:44-55; EX1004, ¶¶ 0008-0009; EX1012, at 590; EX1034, at Abstract, [0001].

229. *Ye* describes TOPCon solar cells having a textured front side that is passivated with $\text{Al}_2\text{O}_3/\text{SiN}$ passivation layers formed on the front surface, but is silent on the thicknesses of those layers or whether it may include additional passivating layers on the front surface. Passivation layers comprised of stacks of sublayers were well known to POSITAs, and it was well known that the performance of such passivation layers could be enhanced by adjusting the composition, thickness, and other properties of the sublayers. EX1034, [0085]; EX1039, 10:22-31; EX1036, Figure 2, [0032]; EX1015, 96-100. *Fang* describes a PECVD device and process that uses different gas combinations, flow rates, and deposition times to form composite passivation films on a solar cell having sublayers of different compositions and thicknesses. *Id.*, [0148]. *Fang* teaches that its preparation method

is simple, flexible, controllable, and compatible with existing production lines. *Id.* *Fang* teaches that, using these methods and devices, “the rear composite film is optimized to match the all-aluminum rear electric field at the rear surface, which gives the best passivation effect and significantly increases the photoelectric conversion efficiency of the PERC cell.” *Id.*

230. *Fang* further discloses various examples of rear passivation films formed with its methods that include a composite film of 2-6 sub-layers. EX1034, [0077]-[0084], Figs. 3-8. *Fang* also discloses that the sublayers can be made of some of the same materials as the passivation layer of *Ye*, including aluminum oxide and silicon nitride. EX1034, [0077], [0081]. A POSITA also would have understood that the rear composite film of *Fang* and the front passivation layer of *Ye* perform similar functions, i.e., passivation of the substrate surface. Therefore, a POSITA would be motivated to use *Fang*’s methods and teachings regarding its rear composite films and the methods for forming them in order to optimize the passivation effect of the front passivation layers on the solar cells of *Ye*.

231. A POSITA would have had a reasonable expectation of success in applying *Fang*’s teachings regarding the sublayers and thicknesses of the rear composite film disclosed to the front passivation layer of the solar cells in *Ye* because it uses a known method (forming a composite passivation film as described

in Fang) to obtain predictable results (i.e., forming a passivation layer on a solar cell).

a. **Claim 11**

- i. **Claim 11[a]: “the first passivation layer is a stacked passivation structure of an aluminum oxide layer, a silicon nitride layer and a silicon oxynitride layer sequentially stacked,”**

232. See discussion of claim 1[e] in Ground 1. *Fang* discloses that the rear passivation film in Figure 3 includes a bottom layer 31 that is an aluminum oxide layer, and a “top layer 32 [that] is composed of a silicon oxynitride film and a silicon nitride film.” EX1034, [0078], Fig. 3.

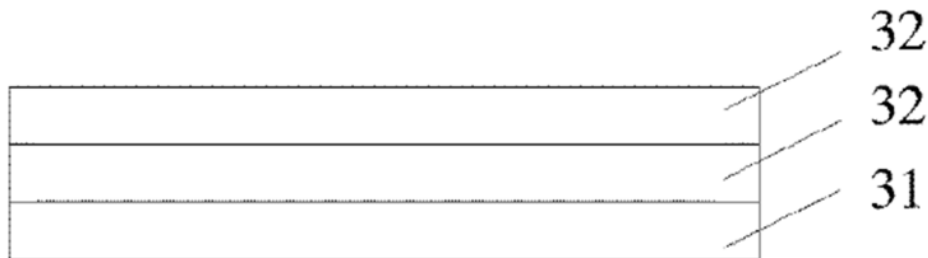


FIG. 3

Although Fang does not expressly specify the order of the silicon nitride and silicon oxynitride films in the top layers 32, Fang does state that “[t]he combination order, thickness, and composition of the composite film *can be flexibly adjusted*.” *Id.*, [0134]. Therefore a POSITA would have understood *Fang* to teach providing the silicon nitride layer on top of the aluminum oxide layer and the silicon oxynitride

layer on top of that. That is one of only two possible sequences for those layers in Figure 3, and so at least would have been obvious to try.

233. A POSITA would have found it obvious to use *Fang*'s rear composite film of Figure 3 in place of Ye's or Basu Paper's front passivation layers, or to modify Ye's or Basu Paper's passivation layers to include the sublayers noted above sequentially stacked as disclosed in *Fang*.

ii. Claim 11[b]: "the aluminum oxide layer has a thickness ranging from 2 nm to 10 nm,"

234. *Fang* discloses that the aluminum oxide layer has a thickness of 5 nm to 15 nm, which overlaps more than 62% of the claimed range and therefore presumptively discloses it and renders it obvious. EX1034, [0085]. Moreover, as discussed in Section II, *supra*, several references taught composite passivation layers that include an aluminum oxide sublayer of a thickness in the claimed range, and therefore it would have been within the level of skill of a POSITA to select a thickness within the claimed range. Finally, a POSITA would have found it obvious to select a thickness within the claimed range because passivation layer thickness optimization was recognized as a result-effective variable and selecting an appropriate thickness was a routine engineering problem in solar cell design. Aluminum oxide (Al_2O_3) is known as a material with good electronic passivation and anti-reflection characteristics. A POSITA would recognize that the thickness of

the aluminum oxide layer may be optimized in order to achieve benefits such as optimized electronic surface-state passivation as well as optimized anti-reflection characteristics, surface chemical passivation (to reduce oxidation and corrosion), favorable optical anti-reflection characteristics (to reduce the reflection of incoming sunlight), and electronic passivation (so as to reduce unwanted electron-hole recombination at the semiconductor surface).

235. Such optimizations would have been routine engineering tasks for a POSITA designing a solar cell. Al_2O_3 , also denoted as alumina, when used in a solar cell may have multiple functions. EX1037 at 2742-43. First, alumina can serve as a chemical passivation layer that protects a silicon surface and makes it resistant to chemical reactions such as oxidation and corrosion. EX1037 at 2742. Second, alumina can serve as an anti-reflection coating (ARC), so that the incident sunlight enters the silicon solar cell rather than being reflected by the silicon solar cell. The thickness of an ARC is guided by theory and well accepted to be $\lambda / (4 n)$, where λ is the wavelength of interest and n is the refractive index of the ARC material. EX1037, 2742–43. Third, alumina can serve as an electronic passivation layer that de-activates the electronic states associated with a silicon surface (dangling-bond states). By de-activating the silicon surface electronic states, electron-hole surface recombination can be reduced or suppressed. Since the electronic passivation

concerns surface dangling bonds, a relatively thin electronic passivation layer, such as 10 nm to 20 nm, may be sufficient. *Id.*

236. Anti-reflection coatings typically have layer thicknesses of $\lambda/(4n)$ where λ is the light's wavelength of interest and n is the refractive index of the ARC. EX1021 at 684 (“However, the region of low reflectivity for a single-layer optical coating occurs at thickness of $\lambda/4n_1$ which cannot cover the entire absorption width over a 400–700 nm visible range.”). Therefore, a POSITA would have recognized the thickness of a passivation layer such as aluminum oxide layer as a result-effective variable. The refractive index of aluminum oxide is approximately 1.6~1.8. EX1037, Figure 1. For certain light wavelengths of interest (which typically ranges from 400 nm to 700 nm) and thicknesses of silicon nitride layers combined with the aluminum oxide layer, a thickness of 2-10 nm would be appropriate. Therefore, such optimizations would have been routine engineering tasks for a POSITA designing a solar cell. *See also* EX1015 at 78-82 (describing examples of how to select materials and thicknesses for an ARC layer).

237. Furthermore, several references teach passivation layers that include an aluminum oxide sublayer of a thickness in this range. *See* EX1016 at 3 (“The front boron emitter of the samples was passivated **by 5 nm AlO_x** and 75 nm SiN_x”); EX1035 at 97 (“The emitter was passivated with **a 10 nm thick Al₂O₃ layer** deposited with plasma-assisted atomic layer deposition.”); EX1039, 6:27-34 (“The

second passivation layer 20 includes at least one aluminum oxide layer Al_xO_y

When the at least one aluminum oxide layer is provided with a single layer (i.e., an aluminum oxide layer 17 shown in FIG. 1), a thickness of the aluminum oxide layer 17 is in a range of 4 nm to 20 nm. Particularly, the thickness of the aluminum oxide layer 17 is 5 nm, 10 nm, 15 nm or 20 nm”).

238. Therefore, a POSITA would have found it obvious to choose a thickness for the aluminum oxide layer of *Fang* (and, similarly, for the aluminum oxide layer in the front passivation layer of *Ye*) within the claimed range because layer thickness optimization is a routine engineering problem in solar cell design.

iii. Claim 11[c]: “the silicon nitride layer has a thickness ranging from 40 nm to 80 nm, and”

239. *Fang* discloses that the silicon nitride layer has a thickness of 50 nm to 150 nm, which overlaps more than 75% of the claimed range and therefore presumptively discloses it and renders it obvious. EX1034, [0085]. Moreover, as discussed in Section II, *supra*, several references taught composite passivation layers that include a silicon nitride sublayer of a thickness in the claimed range, and therefore it would have been within the level of skill a POSITA to select a thickness within the claimed range. Finally, a POSITA would have found it obvious to select a thickness within the claimed range because passivation layer thickness optimization was recognized as a result-effective variable and selecting an

appropriate thickness was a routine engineering problem in solar cell design. Silicon nitride (Si_3N_4) is known as a material with excellent mechanical strength (having a Mohs hardness of 9.0) and serving as a diffusion barrier that keeps reactive chemical species (such as oxygen and chlorine) away from the silicon surface. A POSITA would recognize that the thickness of the silicon nitride layer may be optimized in order to achieve benefits such as surface low optical reflectivity, high scratch resistance, and protection from oxidation and corrosion, mechanical protection (to reduce surface damage by, for example, scratches), surface chemical passivation (to reduce oxidation and corrosion), favorable optical anti-reflection characteristics (to reduce the reflection of incoming sunlight), and electronic passivation (so as to reduce unwanted electron-hole recombination at the semiconductor surface).

240. Such optimizations would have been routine engineering tasks for a POSITA designing a solar cell. Anti-reflection coatings typically have layer thicknesses of $\lambda/(4n)$ where λ is the light's wavelength of interest and n is the refractive index of the ARC. EX1021 at 684 (“However, the region of low reflectivity for a single-layer optical coating occurs at thickness of $\lambda/4n_1$ which cannot cover the entire absorption width over a 400–700 nm visible range.”). Therefore, a POSITA would have recognized the thickness of a passivation layer such as silicon nitride layer as a result-effective variable. The refractive index of silicon nitride is approximately 2.0. EX1038 at 1 (“Indeed, these materials are

transparent in the visible range, and their refractive index can be varied from one of silicon oxide (1.46) to that of silicon nitride (2.02) by only acting on the oxygen and nitrogen concentrations [1]. Their optical band gap could also be increased by increasing the oxygen amount [2]”). For certain light wavelengths of interest (which typically ranges from 400 nm to 700 nm) and thicknesses of silicon nitride layers combined with the aluminum oxide layer, a thickness of 2-10 nm would be appropriate. Therefore, such optimizations would have been routine engineering tasks for a POSITA designing a solar cell. *See also* EX1015 at 78-82 (describing examples of how to select materials and thicknesses for an ARC layer).

241. Therefore, a POSITA would have found it obvious to choose a thickness for the silicon nitride layer of Fang (and, similarly, for the silicon nitride layer in the front passivation layer of Ye) within the claimed range because layer thickness optimization is a routine engineering problem in solar cell design.

iv. Claim 11[d]: “the silicon oxynitride layer has a thickness ranging from 10 nm to 60 nm.”

242. *Fang* discloses that the silicon oxynitride layer has a thickness of 5 nm to 20 nm, which overlaps claimed range and therefore presumptively discloses it and renders it obvious. EX1034, [0085]. More than 66% of *Fang*’s disclosed range falls within the claimed range. A POSITA also would have found it obvious to select a thickness within the claimed range because passivation layer thickness optimization

was recognized as a result-effective variable and selecting an appropriate thickness was a routine engineering problem in solar cell design. A POSITA would recognize that the thickness of the silicon oxynitride layer may be optimized in order to achieve benefits such as low optical reflectivity, high scratch resistance, protection from oxidation and corrosion, improved electronic passivation (compared to Si_3N_4), improved (higher) refractive index (compared to SiO_2), and improved diffusion barrier properties (compared to SiO_2). SiON is a mixture of SiO_2 and Si_3N_4 with each of these two constituent materials having distinct properties and advantages: For example, SiO_2 allows for an excellent electronic passivation of silicon surfaces. Si_3N_4 is known as a highly effective diffusion barrier that prevents oxidizing and corrosive gases, such as O_2 and Cl_2 , from reaching the silicon surface. Furthermore, Si_3N_4 is a mechanically hard material (with a 9.0 hardness on the Mogs scale) that protects the silicon surface from mechanical damage such as scratches. By using SiON as a surface coating, the favorable characteristics of SiO_2 and Si_3N_4 are combined, thereby improving the quality of the surface passivation.

243. Such optimizations would have been routine engineering tasks for a POSITA designing a solar cell. In selecting the appropriate thickness, anti-reflection coatings typically have layer thicknesses of $\lambda/(4n)$ where λ is the wavelength of interest and n is the refractive index of the ARC. EX1021 at 684 (“However, the region of low reflectivity for a single-layer optical coating occurs at thickness of

$\lambda/4n_1$ which cannot cover the entire absorption width over a 400–700 nm visible range.”). Therefore, a POSITA would have recognized the thickness of a passivation layer such as a silicon oxynitride layer as a result-effective variable. The refractive index of silicon oxynitride varies between 1.46 and 1.94 depending on the relative amounts of silicon oxide and silicon nitride therein. EX1038, Abstract. For certain light wavelengths of interest (which typically ranges from 400 nm to 700 nm) and thicknesses of aluminum oxide and silicon nitride layers combined with the silicon oxynitride layer, a thickness of 10-60 nm would be appropriate. It would be within the skill of a POSITA to design such anti-reflection coatings. For example, a SiO₂ ARC for the solar spectrum (500 nm) would have a calculated thickness of $500 \text{ nm} / (4 \times 1.5) = 83 \text{ nm}$. *See also* EX1015 at 78-82 (describing examples of how to select materials and thicknesses for an ARC layer).

244. Moreover, silicon oxynitride passivation layers with thicknesses within the claimed range were well known in the art. *See* EX1034 at [0085] (“Specifically, ... the thickness of the silicon oxynitride film is 5-20 nm.... The actual thickness of the aluminum oxide film, the silicon nitride film, the silicon oxynitride film, and the silicon dioxide film may be adjusted according to actual needs”); EX1039, 6:65-7:8 (“The polarization phenomenon weakening layer 18 includes at least one silicon oxynitride layer SirOsNt, In some embodiments, a thickness of the at least one silicon oxynitride layer in the PPW layer 18 is in a range of 1 nm to

30 nm. Particularly, the thickness of the at least one silicon oxynitride layer is 6 nm, 11 nm, 16 nm, 21 nm, 25 nm or 30 nm”).

245. A POSITA would have found it obvious to use in *Ye* a front passivation stack like Fang’s rear composite film that includes an oxynitride layer of the disclosed thickness, or to add a silicon oxynitride layer of that thickness on top of *Ye*’s existing Al₂O₃/SiN front passivation layers, in order to optimize the passivation effect.

XIX. GROUND 5A: CLAIM 11 IS RENDERED OBVIOUS BY YE IN VIEW OF BASU, YUN AND FANG

A. RATIONALE FOR COMBINING YE, BASU PAPER, YUN, AND FANG

As discussed in Grounds 1, 1A, and 5 above, *Ye*, *Basu*, *Fang*, and *Yun* are analogous art to the ’136 patent.

Yun describes solar cells having a front passivation layer that is “composed of single layer film or multilayer film made of silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide” EX1005, Claim 2. For examples of passivation layers comprising a bilayer of silicon nitride and aluminum oxide, *Yun* also gives ranges of thicknesses for those sub-sublayers, although *Yun* does not give ranges of thicknesses where the passivation layer comprises more than 2 sub-layers.

As noted above, Fang discloses various examples of multi-layer rear passivation films that are made of some of the same materials as *Ye*’s and *Yun*’s passivation layers, including aluminum oxide, silicon nitride, and silicon oxynitride.

EX1005, [0077]-[0084]. POSITAs also would have understood that the rear composite film of *Fang* and *Ye*'s and *Yun*'s front passivation layers perform similar functions, i.e., passivation of the substrate surface. And passivation layers comprised of stacks of sublayers were well known to POSITAs, and it was well known that the performance of such passivation layers could be enhanced by adjusting the composition and other properties of the sublayers. Therefore, POSITAs would be motivated to use *Fang*'s methods and teachings regarding its rear composite films and the methods for forming them in order to optimize the passivation effect of the front passivation layers on *Ye*'s and *Yun*'s solar cells.

POSITAs would have had a reasonable expectation of success in applying *Fang*'s teachings regarding the sublayers and thicknesses of the rear composite film disclosed to the front passivation layer of the solar cells in *Ye* and *Yun* because it uses a known method (forming a composite passivation film as described in *Fang*) to obtain predictable results (i.e., forming a passivation layer on a solar cell).

a. **Claim 11**

- i. **Claim 11[a]: “the first passivation layer is a stacked passivation structure of an aluminum oxide layer, a silicon nitride layer and a silicon oxynitride layer sequentially stacked,”**

246. For the same reasons discussed in Ground 5, *Fang* discloses claim 11[a].

247. Moreover, See discussion of claim 10(a) in Ground 4A. *Yun* discloses “the front passivation antireflection dielectric layer ... [is] composed of single layer film or multilayer film made of silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, silicon carbide, amorphous silicon, microcrystalline silicon, indium tin oxide or titanium oxide.” EX1004, Claim 2. In light of these teachings, a POSITA would have found it obvious to build a multilayer antireflection dielectric layer that also includes a silicon oxynitride layer stacked on top of a silicon nitride layer that is stacked on top of an aluminum oxide layer. Those materials are 3 of only 9 options for materials disclosed for the multilayer film of *Yun*, and as noted in my discussion of the technology background in Section IX above, those materials were well known options for passivating in this field. So, a POSITA would have found that combination of 3 materials obvious to try. It was also well known in the art that passivation layers with more than 2 sublayers could provide benefits such as a lower optical reflectivity over a broad spectral range. A POSITA would have known that multi-layer anti-reflection coatings (ARCs) have a lower reflectivity than single-layer ARCs. In particular, multi-layer ARCs allow for a broadband low reflectivity that single-layer ARCs cannot provide. See EX1032.

248. To the extent the claim so requires, a POSITA would have found it obvious to provide the stacked layers of *Yun*’s front passivation layer with aluminum oxide layer on top of and in contact with the substrate surface, the silicon nitride

layer on top of that, and the silicon oxynitride layer on top of that. That is only one of a limited number of possible sequences for the two layers, and so at least would have been obvious to try. Similar sequential stacks were also well known in passivation layers in solar cells before the '136 Patent. *See, e.g.*, EX1034 at [0077-0084] (“The rear composite film 3 has various embodiments. Referring to FIGS. 3, 4 and 5, the bottom layer of the rear composite film is an aluminum oxide film, and the top layer is composed of one or more of a silicon dioxide film, a silicon oxynitride film, and a silicon nitride film. ... Referring to FIGS. 6, 7 and 8, the bottom layer 31 of the rear composite film is a silicon dioxide film; the middle layer 32 of the rear composite film is an aluminum oxide film; and the top layer 33 is composed of one or more of a silicon dioxide film, a silicon oxynitride film, and a silicon nitride film.”), EX1035 at 97 (“The emitter was passivated with a 10 nm thick Al₂O₃ layer deposited with plasma-assisted atomic layer deposition. The front side was additionally coated with a double-layer antireflection coating (DARC) consisting of 50 nm SiN_x grown by plasma-enhanced chemical vapor deposition (PECVD) and 90 nm thermally evaporated MgF₂.”).

ii. Claim 11[b] “the aluminum oxide layer has a thickness ranging from 2 nm to 10 nm,”

249. For the same reasons discussed in Ground 5, Fang discloses claim 11[b].

250. Moreover, *Yun* discloses that the aluminum oxide layer has a thickness of 20 to 30 nm. EX1005, ¶ 0034 (“the aluminum oxide film is 20 to 30 nm thick”). *See also, id.*, ¶ 0059. As discussed with regard to claim 10[a] above, a POSITA would have found it obvious to modify the aluminum oxide layer thickness disclosed in *Yun* to be in the range of 2-10 nm because passivation layer thickness optimization was recognized as a result-effective variable and selecting an appropriate thickness was a routine engineering problem in solar cell design. *See also* EX1015 at 78-82 (describing examples of how to select materials and thicknesses for an ARC layer). In particular, the addition of a silicon oxynitride layer as discussed above would have caused a POSITA to recalculate the appropriate thickness of the other 2 layers. And, as noted in the section discussing claim 10[a] above, several references teach passivation layers that include an aluminum oxide sublayer of a thickness in this range. Therefore, a POSITA would modify the aluminum oxide layer thickness disclosed in *Yun* to fall within the claimed range.

iii. Claim 11[c]: “the silicon nitride layer has a thickness ranging from 40 nm to 80 nm, and”

251. For the same reasons discussed in Ground 5, Fang discloses claim 11[c].

252. Moreover, *Yun* discloses that the silicon nitride layer has a thickness of 50 to 70 nm, which falls within the claimed thickness range of 40 nm to 80 nm.

EX1005, ¶ 0034 (“the aluminum oxide film is 20 to 30 nm thick and the silicon nitride film is 50 to 70 nm thick”). *See also, id.*, ¶ 0059. Basu Paper also discloses an amorphous SiN_x film with a thickness of 70 nm on the front surface, which falls in the thickness range of 40 nm to 80 nm. EX1012 at 591 (“Amorphous silicon nitride (SiN_x) ... deposited onto the front surface ... The film thickness ... 70 nm”). A POSITA would have understood that the SiN_x film is a silicon nitride layer, and its thickness can be in the range of 40 nm to 80 nm.

iv. Claim 11[d]: “the silicon oxynitride layer has a thickness ranging from 10 nm to 60 nm.”

253. For the same reasons discussed in Ground 5, Fang discloses claim 11[d].

254. Moreover, as discussed above, *Yun* discloses an example of a front passivation as a bilayer film made of aluminum oxide and silicon nitride. However, *Yun* also teaches that the passivation layer can be a “multilayer film” that includes additional layers. EX1005, Claim 2. *Yun* also teaches silicon oxynitride as one of a finite set of suitable materials for those layers. *Id.* Therefore, adding a silicon oxynitride layer to *Yun*’s disclosed example of a bilayer film would have been obvious to a POSITA.

255. Based on the disclosed thicknesses of the aluminum oxide and silicon nitride layers in *Yun*’s bilayer, the total thickness of the bilayer may range from 70

nm to 100 nm. EX1005, ¶ 0034. A POSITA would have found it obvious to add a silicon oxynitride layer having a thickness within the claimed range because layer thickness optimization is a routine engineering problem in solar cell design. For example, if a POSITA selected an Al_2O_3 layer that is 20 nm thick and a silicon nitride layer that is 50 nm thick (as taught in *Yun*), the POSITA could add a silicon oxynitride sublayer that is up to 30 nm thick and the overall thickness of the front passivation layer would not exceed the total thickness of the bilayer film expressly described in *Yun*. In selecting the appropriate thickness, anti-reflection coatings typically have layer thicknesses of $\lambda/(4n)$ where λ is the wavelength of interest and n is the refractive index of the ARC. EX1021 at 684 (“However, the region of low reflectivity for a single-layer optical coating occurs at thickness of $\lambda/4n_1$ which cannot cover the entire absorption width over a 400–700 nm visible range.”). Therefore, a POSITA would have recognized the thickness of a passivation layer such as a silicon oxynitride layer as a result-effective variable.

256. The refractive index of silicon oxynitride varies between 1.46 and 1.94 depending on the relative amounts of silicon oxide and silicon nitride therein. EX1038, Abstract. For certain light wavelengths of interest (which typically ranges from 400 nm to 700 nm) and thicknesses of aluminum oxide and silicon nitride layers combined with the silicon oxynitride layer, a thickness of 10-60 nm would be appropriate. It would be within the skill of a POSITA to design such anti-reflection

coatings. For example, a SiO₂ ARC for the solar spectrum (500 nm) would have a calculated thickness of $500 \text{ nm} / (4 \times 1.5) = 83 \text{ nm}$. *See also* EX1015 at 78-82 (describing examples of how to select materials and thicknesses for an ARC layer).

257. Moreover, silicon oxynitride passivation layers with thicknesses within the claimed range were well known in the art. *See* EX1034 at [0085] (“Specifically, ... the thickness of the silicon oxynitride film is 5-20 nm.... The actual thickness of the aluminum oxide film, the silicon nitride film, the silicon oxynitride film, and the silicon dioxide film may be adjusted according to actual needs”); EX1039, 6:65-7:8 (“The polarization phenomenon weakening layer 18 includes at least one silicon oxynitride layer SirOsNt, In some embodiments, a thickness of the at least one silicon oxynitride layer in the PPW layer 18 is in a range of 1 nm to 30 nm. Particularly, the thickness of the at least one silicon oxynitride layer is 6 nm, 11 nm, 16 nm, 21 nm, 25 nm or 30 nm”). Therefore, a POSITA would have found it obvious to include in Ye’s front passivation layer a silicon oxynitride layer having a thickness within the claimed range.

XX. GROUND 6: CLAIMS 1, 3, 5-9, 12, 13, AND 17-20 ARE ANTICIPATED AND/OR RENDERED OBVIOUS BY SAKAI

258. It is my opinion that *Sakai*, discloses and/or suggests all limitations of Claims 1, 5-9, 12, 13, and 17-20 and thus anticipated and/or rendered those claims obvious.

a. Claim 1

259. It is my opinion that *Sakai* discloses and/or suggests each and every limitation of Claim 1, and a POSITA would have found Claim 1 to be obvious based on *Sakai*.

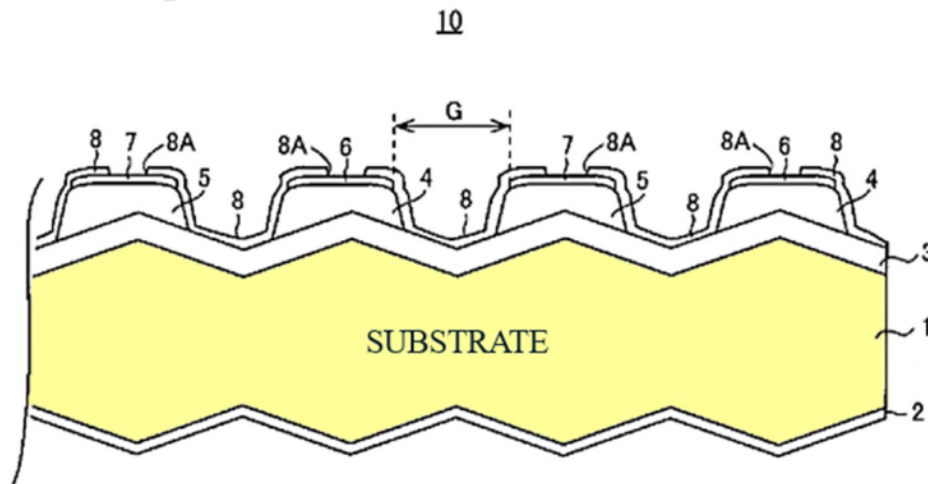
i. Claim 1[p]: “A solar cell, comprising:”

260. *Sakai* discloses various embodiments of “photoelectric conversion elements”, which are also known as solar cells. EX1009, [0006], [0008]-[0009], Figs. 1A & 1B (element 10); *see also id.*, [0172] (reference to “heterojunction solar cell”), [0038] (“The present invention applies to a photoelectric conversion element, a solar cell module provided therewith...”); Figs. 2-21.

ii. Claim 1[a]: “a semiconductor substrate,”

261. All of the photoelectric conversion elements in *Sakai* include a planar “semiconductor substrate” (element 1 in Figure 1A below) that is “composed of, for example, an n-type single crystal silicon substrate” onto which several layers are deposited. EX1009, [0025]-[0026], [0028]; Figs. 1A & 1B.

[FIG. 1B]



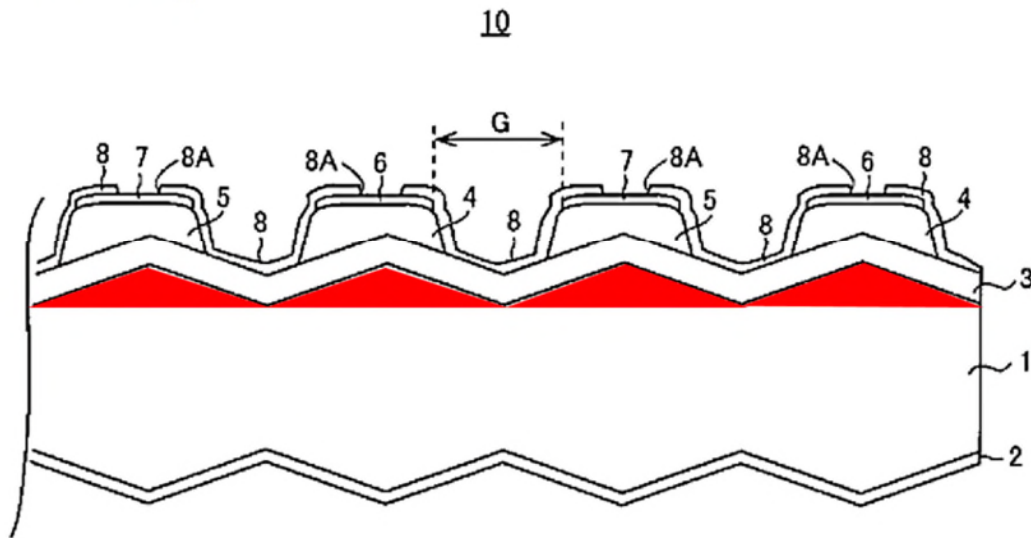
EX1009, Figure 1 (annotated).

- iii. **Claim 1[b]: “wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another, a top surface of the first substructure is a polygonal plane, and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ,”**

262. *Sakai* refers to the surface of the semiconductor substrate 1 on which layers 4 and 5 are formed as the “back surface” of the substrate. EX1009, [0027]. *Sakai* states that semiconductor substrate 1 has texture structures or “unevenness” on both surfaces of substrate 1 (including the back surface) that include multiple substructures across the surface, as shown in Figure 1B. *Id.* [0028] & [0045] (texture

has "unevenness of various sizes and shapes formed in plurality"). Figure 1B shows such texture substructures on the back surface.

[FIG. 1B]



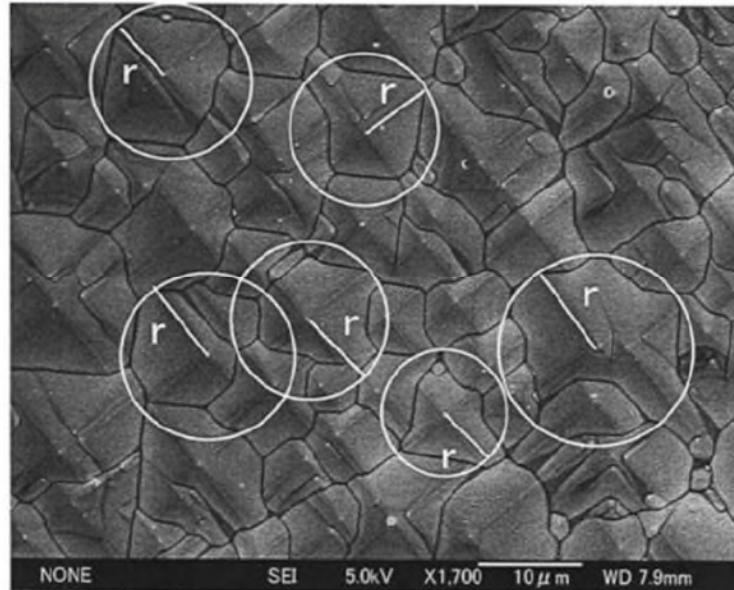
EX1009, Figure 1B (annotated).

263. *Sakai* discloses that the textured structures may be “quadrangle pyramid-shaped or **truncated** quadrangular pyramid-shaped”, the latter of which is a frustum or non-pyramid-shaped microstructure having planar top surface in the shape of a polygon with at least four sides. *Id.* [0045]. Thus, a POSITA would understand *Sakai* to disclose non-pyramid-shaped texture structures on the back surface of the substrate. Additionally, it would have been obvious for a POSITA to choose that shape as one of only two types of shapes that *Sakai* discloses. *Sakai* also states that the “unevenness includes overlapping portions and deformed portions,”

id. [0045], which discloses that at least a portion of the non-pyramid substructures may be at least partially stacked on one another.

264. *Sakai* states that the size of the texture substructures on the back surface of the substrate is less than 15 μm . *Id.* [0028], [0120], [0135]. For example, *Sakai* explains that, when the textured surface is viewed in a plan (top-down) view, “an average value of a diameter of a circumscribed circle of a convex portion of the texture structure is less than 15 μm .” *Id.* [0021], [0046]-[0047], Fig. 2 (image of substructures with a radius r of approximately 7.6 μm); *see also id.*, [0121] (“the size of the texture may be controlled by changing various conditions such as the temperature of the etching solution, the processing time, the type of etching inhibitor, the etching rate, the type of substrate, and the like”). Therefore, the top surface of truncated quadrangle pyramid-shaped substructures in *Sakai* must have a one-dimensional size of less than 45 μm .

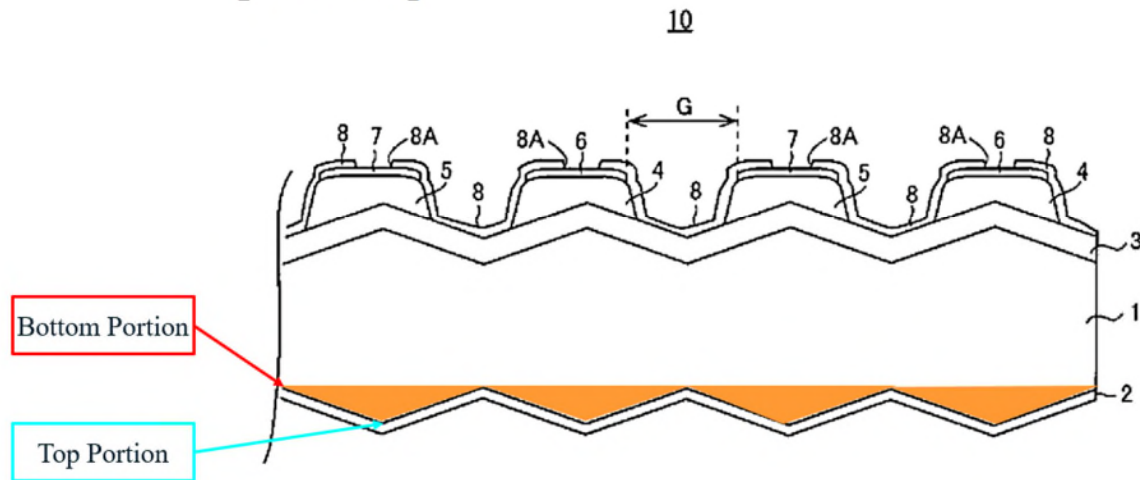
[FIG. 2]



- iv. **Claim 1[c]: “wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and”**

265. *Sakai* refers to the surface of the semiconductor substrate 1 on which film 2 is formed as the “light-receiving surface” of the substrate, which is opposite the “back surface”. EX1009, [0027].

[FIG. 1B]



EX1009, Figure 1B (annotated).

266. *Sakai* states that semiconductor substrate 1 has texture structures or “unevenness” on both surfaces of substrate 1 (including the “light-receiving surface”) that include multiple substructures across the surface, as shown in Figure 1B. *Id.* [0028] & [0045] (texture has “unevenness of various sizes and shapes formed in plurality”). *Sakai* discloses that the textured structure may be “quadrangular pyramid-shaped”. *Id.* [0045]; see also *id.*, Fig. 1B and Fig. 2 (depicting pyramid structures). Additionally, it would have been obvious for a POSITA to choose that shape as one of only two types of shapes that *Sakai* discloses.

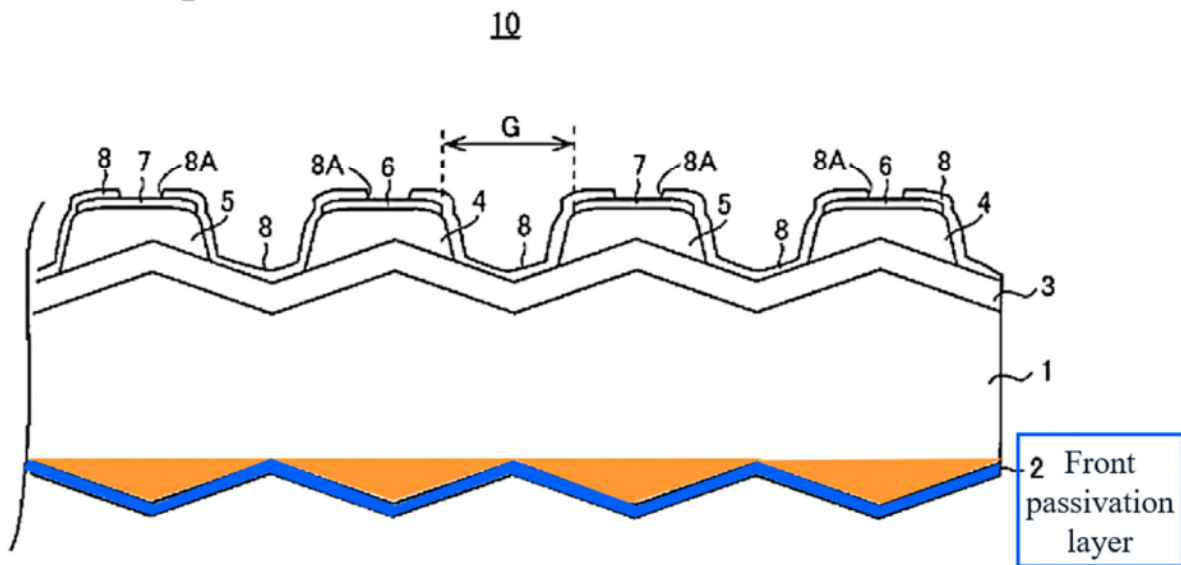
- v. **Claim 1[d]: “in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm ;**”

267. *Sakai* discloses that the “fine pyramid-shaped” texture structure on the surface of the substrate may have a “height from the bottom surface of a concave portion to the top of the convex portion [that] is 1 μm or less”, which is less than 5 μm . *Id.*, [0120]. Furthermore, in describing the size of the pyramid-shaped texture structures, *Sakai* notes that “when an angle θ formed by the bottom surface and an hypotenuse side surface is defined as an inclination angle of the texture, a height b has a relationship of $b = r \times \tan \theta$.” *Id.*, [0048]. As discussed above, Figure 2 shows pyramids with a dimension r ranging from 4 μm to 10 μm , and *Sakai* also states that the inclination angle θ of the texture may be defined as 40° or more, and in some cases may be between 40° and 54° . *Id.*, [0117]-[0118], [0168]. Assuming $\theta = 40^\circ$ and $r = 4 \mu\text{m}$, the height b would be 3.35, which is also less than 5 μm . As another example, assuming $\theta = 40^\circ$ and $r = 5 \mu\text{m}$, the height b would be 2.97 μm , which is also less than 5 μm .

- vi. **Claim 1[e]: “a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate;”**

268. *Sakai* describes an antireflective film 2 located on the textured light-receiving surface of the substrate 1 composed of a silicon nitride film and optionally an oxide film. *Id.*, [0029], [0039]; [0122]-[0124] (discussing formation of silicon nitride film 12 and oxide film 11 in Figures 6 & 7, collectively labeled as film 2 in Figures 7-10).

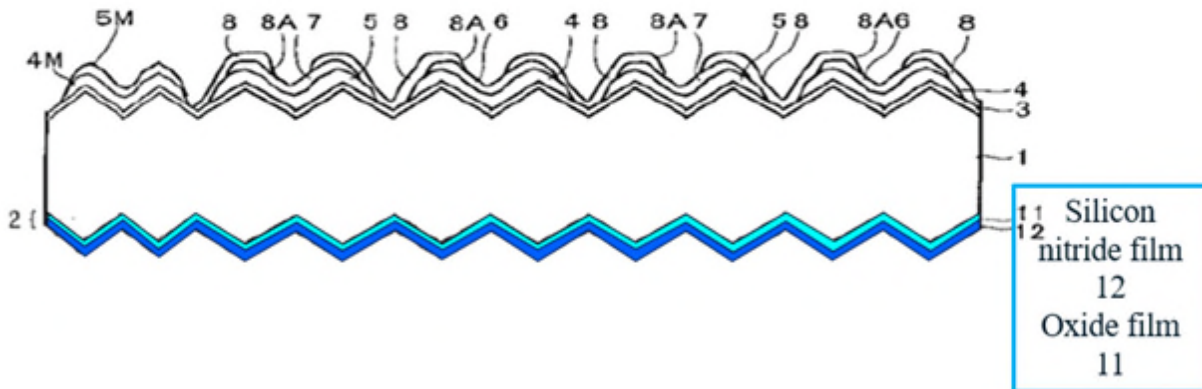
[FIG. 1B]



EX1009, Figure 1B (annotated).

[FIG. 10]

(m)



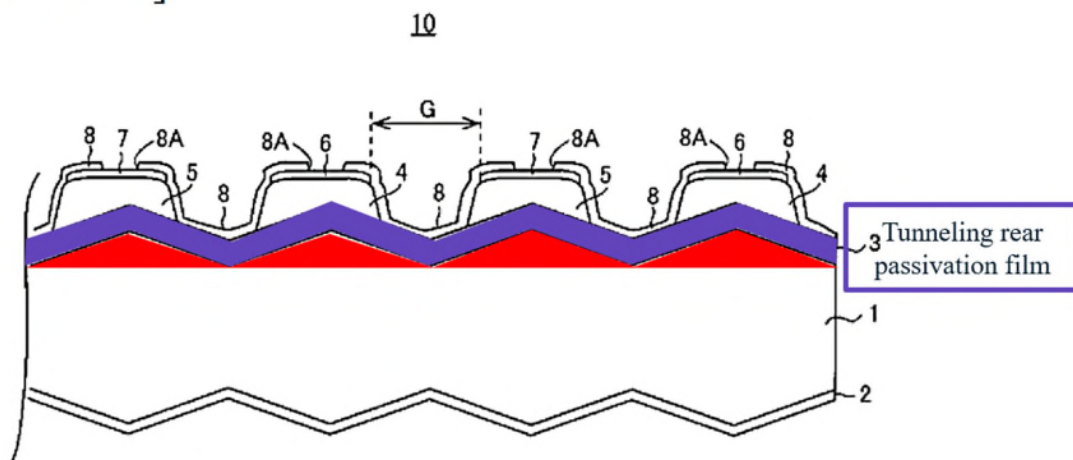
EX1009, Figure 10 (annotated). As noted in my discussion of the technology background in Section IX above, a POSITA would understand that antireflective film 2 is a passivation layer as depicted in Figures 1B and 10.

269. Alternatively, *Sakai* discloses optional embodiments in which “an intrinsic amorphous semiconductor layer or an n-type or p-type conductive amorphous semiconductor layer may be inserted between the antireflective layer 2 and the light-receiving surface” of the substrate, and that “[i]n this case, the passivation property of the light-receiving surface may be improved, which is preferable.” *Id.*, [0039]. As discussed above in Ground 1, this embodiment is consistent with the way Patent Owner is applying the claims against the accused products in the district court. Therefore, *Sakai* discloses a first passivation layer on the second texture structure of the substrate’s front surface under any plausible construction.

vii. Claim 1[f]: “a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;”

270. *Sakai* describes a passivation film 3 on the textured back surface of the substrate that “is composed of, for example, any of amorphous silicon, an oxide of amorphous silicon, a nitride of amorphous silicon, an oxynitride of amorphous silicon, and polycrystalline silicon.” *Id.*, [0040]; *see also id.*, [0260] (describing passivation film 301 as being composed of an “i-type amorphous silicon”).

[FIG. 1B]



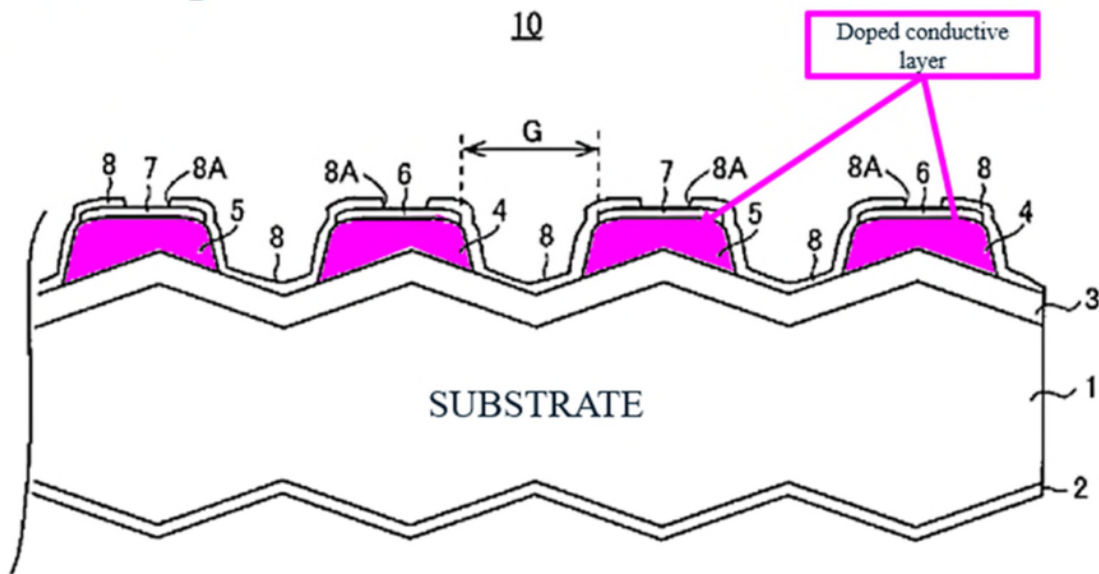
EX1009, Figure 1B (annotated).

271. *Sakai* states that “when the passivation film 3 is composed of a silicon insulating film, the passivation film 3 has a film thickness that allows carriers (electrons and holes) to tunnel.” *Id.*, [0042] (disclosing a thickness of 1 to 20 nm, or preferably 3 to 8 nm); *see also id.*, [0159]. Therefore, a POSITA would understand passivation film 3 to be a tunnel oxide layer.

viii. Claim 1[g]: “a doped conductive layer located on a surface of the tunnel oxide layer; and”

272. *Sakai* describes an n-type amorphous semiconductor layer 4 deposited in contact with passivation film 3 that includes phosphorus as an n-type dopant. *Id.*, [0031], [0043]. *Sakai* also describes that a p-type amorphous semiconductor layer 5 is deposited in contact with the n-type amorphous semiconductor layer 4 that includes boron as a p-type dopant. *Id.*, [0032], [0044].

[FIG. 1B]

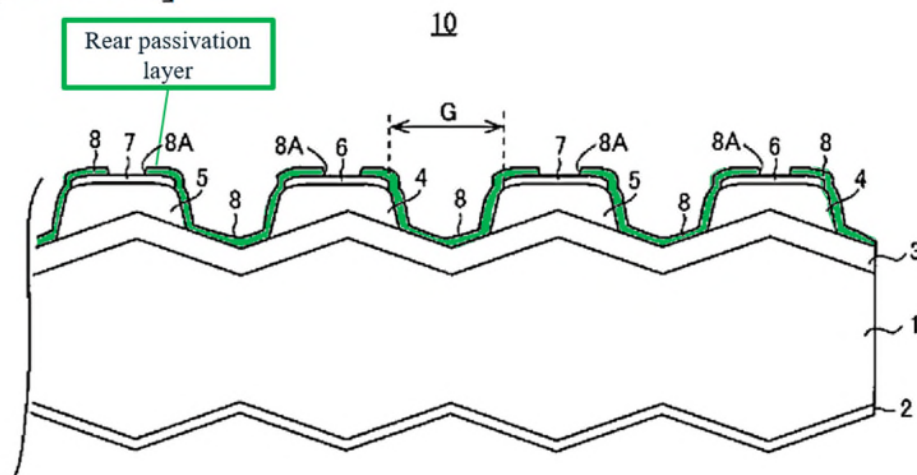


EX1009, Figure 1B (annotated). A POSITA would have understood that either of layers 4 or 5 or the combination thereof is a “doped conductive layer”.

ix. Claim 1[h]: “a second passivation layer located on a surface of the doped conductive layer.”

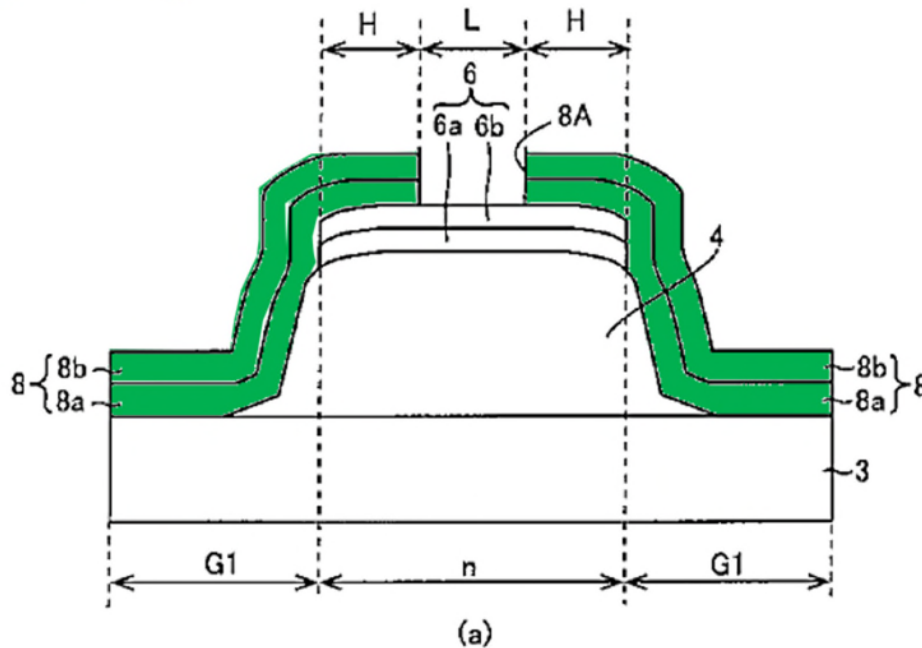
273. *Sakai* describes a protective dielectric film 8 deposited on the n-type and p-type amorphous semiconductor layers that includes “an inorganic insulating material” such as “an oxide film, a nitride film, an oxynitride film, or the like.” *Id.*, [0038], [0065]-[0068], [0073]. Film 8 may be composed of a single layer or multiple sub-layers (*e.g.*, layers 8a and 8b as shown, for example in Figure 3), and some of the sub-layers may be an amorphous semiconductor layer composed of materials such as amorphous silicon, amorphous silicon germanium, amorphous germanium, amorphous silicon carbide, amorphous silicon nitride, amorphous silicon oxide, amorphous silicon oxynitride, amorphous silicon carbon oxide, or the like. *Id.* [0070]-[0072].

[FIG. 1B]



EX1009, Figure 1B (annotated).

[FIG. 3]



EX1009, Figure 3 (annotated).

274. When the protective film 8 is composed of a multi-layer structure that includes an amorphous semiconductor layer (*e.g.*, 8a), “it possible to achieve both passivation of the n-type amorphous semiconductor layer 4 and the p-type amorphous semiconductor layer 5, and insulation between electrodes 6 and 7, which is preferable.” *Id.*, [0078]. Therefore, *Sakai* discloses a second passivation layer on the surface of the doped conductive layer(s).

- b. **Claim 3: “a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a substantially trapezoid.”**

275. As noted above for claim 1[b] in this ground, *Sakai* discloses or teaches that the textured structures on the back surface of the substrate may be “truncated quadrangular pyramid-shaped”, which is a frustum or non-pyramid-shaped structure having a planar top surface with four sides. *Id.* [0045]. A POSITA would understand from this disclosure that the top surface of each such truncated quadrangular pyramid is in the shape of a square, a trapezoid, a diamond, or substantially one of those shapes.

- c. **Claim 5: “the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm .”**

276. As discussed above for claim 1[b] in this ground, *Sakai* discloses or teaches that the back surface of the semiconductor substrate includes textured microstructures that have a truncated quadrangle pyramid shape with a top surface with a one-dimensional size of less than 45 μm . *Sakai* states that the textured microstructures or unevenness on the substrate, including those on the back surface, “includes overlapping portions”. *Id.* [0045]. POSITA would understand from this disclosure that at least some of the truncated pyramid-shaped microstructures include portions that are not overlapped or stacked on one another.

d. **Claim 6: “the top surface of the second substructure is a polygonal plane.”**

277. See discussion of claim 5, this ground. This claim depends from claim 5, which is discussed above. As noted above for claim 1[b], *Sakai* discloses or teaches that the back surface of the semiconductor substrate includes textured microstructures that have a truncated quadrangle pyramid shape with a top surface, which is a frustum or non-pyramid-shaped microstructure having planar top surface in the shape of a polygon with at least four sides. *Id.* [0045]. A POSITA would understand that this teaching applies to all of the microstructures of that shape, including those that are not overlapped or stacked on one another.

e. **Claim 7**

i. **Claim 7[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

278. See discussion of claim 1[f] in this ground. *Sakai* states that passivation film 3 may be composed of various materials, including an oxide of an amorphous silicon or an oxynitride of an amorphous silicon. *Id.* [0040]; *see id.* [0042] (film 3 in embodiment 1 is composed of “a thermal oxide film of silicon”). These options read on the claimed elements of a silicon oxide layer or a silicon oxynitride layer.

ii. Claim 7[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”

279. *Sakai* states that film 3 has a thickness of 1 to 20 nm, and in embodiment 1 its thickness is set to 2 nm. *Id.*, [0042]. These disclosures overlap or fall within the claimed range of 0.8 nm to 2 nm.

280. Moreover, selecting a thickness for *Sakai*'s film 3 within the range recited in claim 7[b] would have been obvious to a POSITA. As noted in my discussion of the technology background in Section IX above, a POSITA would be aware that a tunnel oxide passivation (TOP) layer must be thin enough to be tunneled through but should also passivate the semiconductor surface. Therefore, a POSITA would have recognized that thickness as a result-effective variable. For example, a tunneling layer much thicker than 2 nm, e.g. 20 nm, would be too thick for an efficient quantum-mechanical tunneling process. On the other hand, to effectively passivate the semiconductor surface, a tunnel oxide passivation (TOP) layer should be at least 0.5 nm thick. This puts the preferable range of the TOP layer between 0.5 nm and a few nm. In addition, the contact area also plays a role, with larger contact areas allowing for thicker TOP layers, and smaller contact areas requiring thinner TOP layers, to keep the contact resistance low. A POSITA would understand that any of the ranges, such as 0.5 to 2.0 nm, 1.0 to 2.0 nm, or 1.0 to 3.0 nm, would be a preferred TOP layer thickness range. Given the finite range of thicknesses disclosed

in *Sakai*, a POSITA would have found it obvious to select a tunnel oxide layer with a thickness of 1.0 nm - 2 nm, which is within the claimed range.

f. Claim 8

i. Claim 8[a]: “the second passivation layer includes at least one of a silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and”

281. See discussion of claim 1[h] in this ground. *Sakai* states that protective dielectric film 8 may be composed of “an oxide film, a nitride film, an oxynitride film, or the like” (*id.*, [0038], [0065]-[0068], [0073]), and that one of more of its sublayers may be composed of amorphous silicon nitride, amorphous silicon oxide, amorphous silicon oxynitride, amorphous silicon carbon oxide, or the like. *Id.* [0070]-[0072]. These options read on the claimed elements of a silicon nitride layer, a silicon oxide layer, or a silicon oxynitride layer.

ii. Claim 8[b]: “the second passivation layer has a thickness ranging from 70 nm to 120 nm.”

282. In one example, *Sakai* describes forming protective film 8 by sequentially depositing (i) “an intrinsic amorphous semiconductor film” having a thickness of, for example, 10 nm, followed by (ii) a silicon nitride film having a thickness of, for example, 120 nm. *Id.*, [0153]. The total thickness of those films would be 130 nm, which a POSITA would recognize is close to the upper end of the claimed range and therefore either discloses or teaches that thickness to a POSITA,

and presumptively renders obvious the claimed range of 70-120 nm. To the extent that total thickness falls above the claimed range of 70 nm to 120 nm, a POSITA would understand that the thicknesses of one or both of those films may be adjusted depending on numerous factors, and might make one or both of those films slightly thinner. A POSITA would expect a protective film 8 of 130 nm to have substantially the same properties as one having a thickness of 120 nm.

283. Anti-reflection coatings typically have layer thicknesses of $\lambda/(4n)$ where λ is the wavelength of interest and n is the refractive index of the ARC. EX1021 at 684 (“However, the region of low reflectivity for a single-layer optical coating occurs at thickness of $\lambda/4n_1$ which cannot cover the entire absorption width over a 400–700 nm visible range.”). Therefore, a POSITA would have recognized the thickness of a passivation layer such as protective film 8 as a result-effective variable. For certain light wavelengths of interest (which typically ranges from 400 nm to 700 nm) and materials disclosed in Sakai for protective film 8, a total thickness of 70-120 nm would be appropriate. It would be within the skill of a POSITA to design such anti-reflection coatings. *See also* EX1015 at 78-82 (describing examples of how to select materials and thicknesses for an ARC layer). Moreover, a POSITA would have been motivated to make the component layers of protective film 8 of *Sakai* as thin as possible while still providing effective passivation, for example, in order to reduce the amount of materials needed for manufacturing and minimize the

size and weight of the solar cell. A POSITA also would have recognized that selecting an appropriate thickness was a routine engineering problem in solar cell design. Therefore, it would be obvious for a POSITA to form protective film 8 (i.e., the passivation layer) of *Sakai* to have a thickness of 70 nm to 120 nm.

g. **Claim 9: “the first passivation layer includes at least one of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer or a silicon oxynitride layer.”**

284. See discussion of claim 1[e] in this ground. *Sakai* states antireflective film 2 includes a silicon nitride film. *Id.*, [0029] [0039]; [0122]-[0124] (discussing formation of silicon nitride film 12, which is a part of film 2).

h. **Claim 12**

i. **Claim 12[a]: “the semiconductor substrate is an N-type monocrystalline silicon substrate,”**

285. See discussion of claim 1[a] in this ground. A POSITA would understand that a "single crystal" silicon is a monocrystalline silicon.

ii. **Claim 12[b]: “the doped conductive layer is an N-type doped polycrystalline silicon layer, an N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer, and”**

286. See discussion of claim 1[g] in this ground, i.e., the n-type amorphous semiconductor layer 4 deposited in contact with passivation film 3 that includes phosphorus as an n-type dopant. *Id.*, [0031], [0043]. *Sakai* states that layer 4 may be composed of, for example, n-type amorphous silicon. *Id.*, [0043].

iii. Claim 12[c]: “the doped conductive layer has a thickness ranging from 60 nm to 200 nm.”

287. See discussion of claim 1[g] in this ground. *Sakai* states that layer 4 has a film thickness of, for example, 5 nm to 50 nm, (*id.*, [0043]), which presumptively renders obvious the claimed range of 60-200 nm. A POSITA would expect a layer 4 of 50 nm to have the substantially same properties as one having a thickness of 60 nm. To the extent that the upper end of that range of thicknesses falls below the lower end of the claimed range of 60 nm to 200 nm, a POSITA would understand that the thickness of layer 4 may be adjusted depending on numerous factors, and might make that layer a bit thicker, e.g., by 10 nm. For example, *Sakai* discloses an N-type amorphous semiconductor layer 4, such as N-type amorphous Si, SiGe, or Ge. EX1009, [0043]. The N-type amorphous semiconductor layer 4 is located above the passivation film 3 (a tunnel oxide passivation film, or TOP film) that has a film thickness of a few nm so that carriers (electrons and holes) can tunnel through it. *Id.* *Sakai* suggests that n-type amorphous semiconductor layer 4 has a thickness “of, for example, 5 to 50 nm.” *Id.* The fact that *Sakai* discloses the thickness range of “5 to 50 nm” as an “example,” conveys to a POSITA that the thickness is not critical and that greater thickness ranges, for example 25 to 75 nm, are equally acceptable. Indeed, whereas AR coatings have a theoretical target thickness (given by $\lambda / (4 n)$), *Sakai*’s n-type amorphous semiconductor layer 4 does

not have such theoretical target thickness. This further supports the understanding of a POSITA that Sakai's "example" thickness range ("5 to 50 nm") is indeed an example and should not be understood as a strict limitation. POSITAs would understand that a thicker layer may provide greater manufacturing tolerances thereby reducing cost. Therefore, it would be obvious for a POSITA to form layer 4 of *Sakai* to have a thickness of 60 nm to 200 nm.

i. Claim 13

288. See claim 1[p] this ground; EX1009, [0006], [0008]-[0009], Figs. 1A & 1B (element 10); *see also id.*, [0172] (reference to "heterojunction solar cell"), [0038] ("The present invention applies to a photoelectric conversion element, a solar cell module provided therewith..."); Figs. 2-21. Moreover, as noted in my discussion of the technology background in Section IX above, in order to capture significant amounts of sunlight, typical solar installations cover many square feet, such as 100 or 1,000 square feet. Since the silicon wafer sizes are significantly less than a square foot, in order to generate a sufficient amount of electricity for most applications, a POSITA would understand that any solar cell must be used together with a plurality of solar cells assembled into one or more strings to form a photovoltaic module or solar panel. Such strings and modules were well known in the art before the '136 Patent. See EX1015 at 115 ("For the construction of a whole module, the copper ribbons are used to connect the front of the first cell to the back of the second cell,

etc. This corresponds to a series connection of the solar cells and leads to an addition of the individual voltages, whilst the current remains constant. Typically, 1–12 cells are processed into a so-called ‘string’. Six strings are then connected in series to finally make up a whole module.”) and 219-223.



Fig. 9.1 c-Si solar cells with (from the top left) two (2BB), three (3BB), five (5BB) busbar and cell without busbars (below right). Current-collecting fingers are placed perpendicular to the busbars

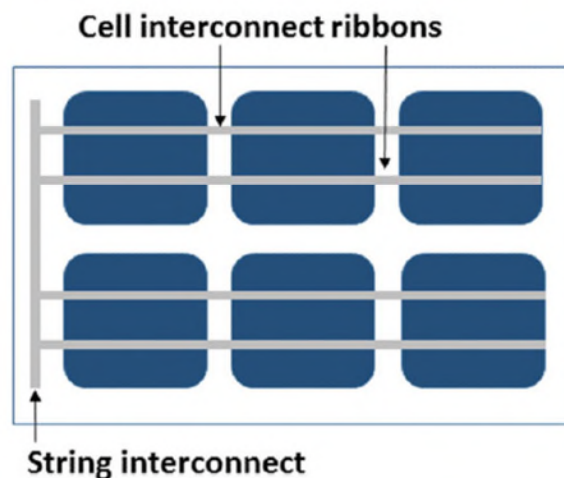


Fig. 9.2 Simplified sketch of a solar module with two-busbar (2BB) cells. *Cell interconnect ribbons* and *string interconnects* are shown. *Busbars* are hidden below the ribbons

289. Therefore, a POSITA would have found it obvious to assemble a plurality of the solar cells of *Sakai* into a plurality of strings that form a photovoltaic module, and claim 13[p] is taught or rendered obvious by *Sakai*.

i. Claim 13[a] “a semiconductor substrate,”

290. See claim 1[a] in this ground. For the same reasons discussed with regard to claim 1[a] in this ground, *Sakai* discloses or renders obvious claim 13[a].

ii. Claim 13[b] “wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another, a top surface of the first substructure is a polygonal plane, and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ; and”

291. See claim 1[b] in this ground. For the same reasons discussed with regard to claim 1[b] in this ground, *Sakai* discloses or renders obvious claim 13[b].

- iii. **Claim 13[c] “wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and”**

292. See claim 1[c] in this ground. For the same reasons discussed with regard to claim 1[c] in this ground, *Sakai* discloses or renders obvious claim 13[c].

- iv. **Claim 13[d] “in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm ,”**

293. See claim 1[d] in this ground. For the same reasons discussed with regard to claim 1[d] in this ground, *Sakai* discloses or renders obvious claim 13[d].

- v. **Claim 13[e] “a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate,”**

294. See claim 1[e] in this ground. For the same reasons discussed with regard to claim 1[e] in this ground, *Sakai* discloses or renders obvious claim 13[e].

- vi. **Claim 13[f] “a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;”**

295. See claim 1[f] in this ground. For the same reasons discussed with regard to claim 1[f] in this ground, *Sakai* discloses or renders obvious claim 13[f].

- vii. **Claim 13[g] “a doped conductive layer located on a surface of the tunnel oxide layer; and”**

296. See claim 1[g] in this ground. For the same reasons discussed with regard to claim 1[g] in this ground, *Sakai* discloses or renders obvious claim 13[g].

- viii. **Claim 13[h] “a second passivation layer located on a surface of the doped conductive layer.”**

297. See claim 1[h] in this ground. For the same reasons discussed with regard to claim 1[h] in this ground, *Sakai* discloses or renders obvious claim 13[h].

- j. **Claim 17 “The photovoltaic module according to claim 13, wherein the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm .”**

298. See claim 5 in this ground. For the same reasons discussed with regard to claim 5 in this ground, *Sakai* discloses or renders obvious claim 17.

- k. **Claim 18 “The photovoltaic module according to claim 17, wherein the top surface of the second substructure is a polygonal plane.”**

299. See claim 6 in this ground. For the same reasons discussed with regard to claim 6 in this ground, *Sakai* discloses or renders obvious claim 18.

l. **Claim 19**

- i. **Claim 19[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

300. See claim 7[a] in this ground. For the same reasons discussed with regard to claim 7[a] in this ground, *Sakai* discloses or renders obvious claim 19[a].

- ii. **Claim 19[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”**

301. See claim 7[b] in this ground. For the same reasons discussed with regard to claim 7[b] in this ground, *Sakai* discloses or renders obvious claim 19[b].

m. **Claim 20**

- i. **Claim 20[a]: “the second passivation layer includes at least one of a silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and”**

302. See claim 8[a] in this ground. For the same reasons discussed with regard to claim 8[a] in this ground, *Sakai* discloses or renders obvious claim 20[a].

ii. Claim 20[b]: “the second passivation layer has a thickness ranging from 70 nm to 120 nm.”

303. See claim 8[b] in this ground. For the same reasons discussed with regard to claim 8[b] in this ground, *Sakai* discloses or renders obvious claim 20[b].

XXI. GROUND 6A: CLAIMS 1-3, 5-9, 12-15, AND 17-20 ARE RENDERED OBVIOUS BY SAKAI IN VIEW OF YUN.

A. RATIONALE TO COMBINE SAKAI AND YUN

304. The '136 Patent relates to the field of solar cells generally, and more specifically to optimizing solar cell design (*e.g.*, of TOPCon solar cells) to improve efficiency (*e.g.*, by using textured front and back surfaces). EX1001, 1:15-18, 1:41-46. *Sakai* also relates to the field of solar cells, and more specifically to preparing a cell that reduces photoelectric conversion inefficiencies due to overlapping of n-type and p-type semiconductor layers. EX1009, [0005]. *Yun* also relates to the field of solar cells and is directed to optimizing solar cell structure to improve efficiency and reduce cost (*e.g.*, by using textured surface structures on the solar cell). EX1005, ¶ 0001 - 0003. As such, *Sakai* and *Yun* both relate to the same field as the '136 Patent, and are therefore analogous art to each other and to the '136 Patent. EX1001, 1:41-46; 4:13-17; 5:44-55; EX1009, [0005]; EX1005, ¶ 0002.

305. Alternatively, the '136 Patent is concerned with the problem of solar cells having non-optimal back surfaces that adversely affect other layers and lower the efficiency. EX1001, 5:29-38. *Sakai* and *Yun* each teach how to optimize the

textured front/back surfaces or their adjacent layers to improve the efficiency, quality or reduce cost. EX1009, [0274]; EX1005, ¶ 0022. As such, *Sakai* and *Yun* both relate to problems with which the inventors of the '136 Patent would have been concerned. Therefore, *Sakai* and *Yun* are analogous art to each other and to the '136 Patent. Finally, the '136 Patent Examiner cited *Sakai* as the closest prior art to the '136 Patent. EX1018, 15-16. This confirms that *Sakai* is analogous art to the '136 Patent.

306. *Sakai* relates to the field of solar cells, and more specifically to preparing a cell that reduces photoelectric conversion inefficiencies due to overlapping of n-type and p-type semiconductor layers. EX1009, [0005]. As such, *Sakai* relates to the same field as the '136 Patent, and is therefore analogous art to the '136 Patent.⁶

307. *Sakai* describes solar cells that have texture surfaces on both the front and rear sides, with at least the front side texture having a pyramid shape. EX1009. *Sakai* describes forming the texture surfaces with “wet etching using an alkaline etching solution” such as a sodium hydroxide solution optionally with an isopropyl alcohol etching inhibitor. *Id.*, [0116]. *Sakai* further teaches that the size of texture

⁶ The '136 Patent Examiner cited *Sakai* as the closest prior art, confirming that *Sakai* is analogous art. EX1018, 15-16.

structures may be controlled by changing various conditions of the etching solution, including the type of etching inhibitor. *Id.*, [0120-0121]. Sakai then describes varying the size of the texture structure on the back surface of the substrate in order to reduce the amount of light reflected from the back surface of the substrate, facilitating the reliable determination of alignment marks during manufacture of the cell. *Id.*, [0160-0168].

308. *Yun* teaches using similar wet chemical methods (i.e., an alkaline solution with an alcohol additive (isopropanol)) to create textured structures on the rear side of a double-sided solar cell that include platform-shaped structures of certain sizes. EX1005, ¶¶ 0019, 0043, 0056. A POSITA would have been motivated to use the wet chemical methods disclosed by *Yun* to form the textured structures on the rear side of the TOPCon cell in *Sakai*, for example, to control the size and shape of the textured structures as expressly suggested in *Sakai*, in order to facilitate recognition of alignment marks on the cell. That would result in the formation of overlapping platform-shaped (non-pyramid) structures of the sizes claimed in the '136 patent. A POSITA would have had a reasonable expectation of success in applying the wet chemical method disclosed in *Yun* to the solar cells in *Sakai* because it uses a known method (*Yun*'s wet chemical method) to obtain predictable results (i.e., forming non-pyramid textures of different shapes and sizes). EX1005, ¶¶ 0019, 0043, 0056; see *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740 (2007).

a. **Claims 1**

i. **Claim 1[p]: “A solar cell, comprising:”**

309. See claim 1[p] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[p] in Ground 1A, *Yun* also discloses or renders obvious claim 1[p]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 1[p].

ii. **Claim 1[a] “a semiconductor substrate,”**

310. See claim 1[a] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[a] in Ground 1A, *Yun* also discloses or renders obvious claim 1[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 1[a].

iii. **Claim 1[b] “wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another, a top surface of the first substructure is a polygonal plane, and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ; and”**

311. See claim 1[b] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[b] in Ground 1A, *Yun* also discloses or renders obvious claim 1[b]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 1[b].

- iv. **Claim 1[c] “wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and”**

312. See claim 1[c] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[c] in Ground 1A, *Yun* also discloses or renders obvious claim 1[c]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 1[c].

- v. **Claim 1[d] “in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm ,”**

313. See claim 1[d] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[d] in Ground 1A, *Yun* also discloses or renders obvious claim 1[d]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 1[d].

vi. Claim 1[e] “a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate;”

314. See claim 1[e] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[e] in Ground 1A, *Yun* also discloses or renders obvious claim 1[e]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 1[e].

vii. Claim 1[f] “a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;”

315. See claim 1[f] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[f] in Ground 1A, *Yun* also discloses or renders obvious claim 1[f]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 1[f].

viii. Claim 1[g] “a doped conductive layer located on a surface of the tunnel oxide layer; and”

316. See claim 1[g] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[g] in Ground 1A, *Yun* also discloses or renders obvious claim 1[g]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 1[g].

ix. Claim 1[h] “a second passivation layer located on a surface of the doped conductive layer.”

317. See claim 1[h] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 1[h] in Ground 1A, *Yun* also discloses or renders obvious claim 1[h]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 1[h].

b. Claim 2: “for the two or more first substructures at least partially stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, a distance between the top surface of the outermost first substructure and the top surface of the adjacent first substructure is equal to or less than 2 μm .”

318. As discussed in claim 2 in Ground 1A, *Yun* discloses or renders obvious claim 2. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 2.

c. Claim 3: “a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a substantially trapezoid.”

319. See claim 3 in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 3 in Ground 1A, *Yun* also discloses or renders obvious claim 3. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 3.

- d. **Claim 5: “the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm .”**

320. See claim 5 in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 5 in Ground 1A, *Yun* also discloses or renders obvious claim 5. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 5.

- e. **Claim 6: “the top surface of the second substructure is a polygonal plane.”**

321. See claim 6 in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 6 in Ground 1A, *Yun* also discloses or renders obvious claim 6. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 6.

- f. **Claim 7**

- i. **Claim 7[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

322. See claim 7[a] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 7[a] in Ground 1A, *Yun* also discloses or renders obvious claim 7[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 7[a].

ii. Claim 7[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”

323. See claim 7[b] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 7[b] in Ground 1A, *Yun* also discloses or renders obvious claim 7[b]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 7[b].

g. Claim 8

i. Claim 8[a]: “the second passivation layer includes at least one of a silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and”

324. See claim 8[a] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 8[a] in Ground 1A, *Yun* also discloses or renders obvious claim 8[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 8[a].

ii. Claim 8[b]: “the second passivation layer has a thickness ranging from 70 nm to 120 nm.”

325. See claim 8[b] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 8[b] in Ground 1A, *Yun* also discloses or renders obvious claim 8[b]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 8[b].

h. **Claim 9: “the first passivation layer includes at least one of a silicon oxide layer, a silicon nitride layer, an aluminum oxide layer or a silicon oxynitride layer.”**

326. See claim 9 in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 9 in Ground 1A, *Yun* also discloses or renders obvious claim 9. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 9.

i. **Claim 12**

i. **Claim 12[a]: “the semiconductor substrate is an N-type monocrystalline silicon substrate,”**

327. See claim 12[a] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 12[a] in Ground 1A, *Yun* also discloses or renders obvious claim 12[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 12[a].

ii. **Claim 12[b]: “the doped conductive layer is an N-type doped polycrystalline silicon layer, an N-type doped microcrystalline silicon layer or an N-type doped amorphous silicon layer, and”**

328. See claim 12[b] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 12[b] in Ground 1A, *Yun* also discloses or renders obvious claim 12[b]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 12[b].

iii. Claim 12[c]: “the doped conductive layer has a thickness ranging from 60 nm to 200 nm.”

329. See claim 12[c] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 12[c] in Ground 1A, *Yun* also discloses or renders obvious claim 12[c]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 12[c].

j. Claim 13

i. Claim 13[p]: “A photovoltaic module, comprising a plurality of solar cell strings, wherein each of the plurality of solar cell strings comprises solar cells, and at least one of the solar cells comprise:”

330. See claim 13[p] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[p] in Ground 1A, *Yun* also discloses or renders obvious claim 13[p]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 13[p].

ii. Claim 13[a] “a semiconductor substrate,”

331. See claim 13[p] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[a] in Ground 1A, *Yun* also discloses or renders obvious 13[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 13[a].

- iii. **Claim 13[b] “wherein a rear surface of the semiconductor substrate has a first texture structure, the first texture structure has a non-pyramid-shaped microstructure and includes two or more first substructures at least partially stacked on one another, a top surface of the first substructure is a polygonal plane, and a one-dimensional size of the top surface of the outermost first substructure is less than or equal to 45 μm ; and”**

332. See claim 13[b] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[b] in Ground 1A, *Yun* also discloses or renders obvious claim 13[b]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 13[b].

- iv. **Claim 13[c] “wherein a front surface of the semiconductor substrate has a second texture structure, the second texture structure includes a pyramid-shaped microstructure, the pyramid-shaped microstructure includes a top portion away from the front surface of the semiconductor substrate and a bottom portion close to the front surface of the semiconductor substrate, and”**

333. See claim 13[c] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[c] in Ground 1A, *Yun* also discloses or renders obvious 13[c]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 13[c].

- v. **Claim 13[d] “in a direction away from the front surface and perpendicular to the front surface, a distance between the top portion and the bottom portion of the pyramid-shaped microstructure is less than or equal to 5 μm ,”**

334. See claim 13[d] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[d] in Ground 1A, *Yun* also discloses or renders obvious claim 13[d]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 13[d].

- vi. **Claim 13[e] “a first passivation layer located on the second texture structure of the front surface of the semiconductor substrate;”**

335. See claim 13[e] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[e] in Ground 1A, *Yun* also discloses or renders obvious claim 13[e]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 13[e].

- vii. **Claim 13[f] “a tunnel oxide layer located on the first texture structure of the rear surface of the semiconductor substrate;”**

336. See claim 13[f] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[d] in Ground 1A, *Yun* also discloses or renders obvious claim 13[f]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 13[f].

viii. Claim 13[g] “a doped conductive layer located on a surface of the tunnel oxide layer; and”

337. See claim 13[g] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[g] in Ground 1A, *Yun* also discloses or renders obvious claim 13[g]. Therefore, for the same reasons discussed in those sections and this ground, the combination of Sakai and Yun disclose or renders obvious claim 13[g].

ix. Claim 13[h] “a second passivation layer located on a surface of the doped conductive layer.”

338. See claim 13[j] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 13[h] in Ground 1A, *Yun* also discloses or renders obvious claim 13[h]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 13[h].

k. Claim 14 “The photovoltaic module according to claim 13, wherein for the two or more first substructures at least partially stacked on one another, in the direction away from the rear surface and perpendicular to the rear surface, a distance between the top surface of the outermost first substructure and the top surface of the adjacent first substructure is equal to or less than 2 μm .”

339. As discussed in claim 14 in Ground 1A, *Yun* discloses or renders obvious claim 14. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 14.

- l. **Claim 15 “The photovoltaic module according to claim 13, wherein a shape of the polygonal plane includes at least one of a diamond, a square, a trapezoid, a substantially diamond, a substantially square or a substantially trapezoid”**

340. See claim 15 in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 15 in Ground 1A, *Yun* also discloses or renders obvious claim 15. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 15.

- m. **Claim 17 “The photovoltaic module according to claim 13, wherein the first texture structure further includes two or more adjacent second substructures that do not stacked on one another, and a one-dimensional size of a top surface of the second substructure away from the rear surface is less than or equal to 45 μm .”**

341. See claim 17 in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 17 in Ground 1A, *Yun* also discloses or renders obvious claim 17. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 17.

- n. **Claim 18 “The photovoltaic module according to claim 17, wherein the top surface of the second substructure is a polygonal plane.”**

342. See claim 18 in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 18 in Ground 1A, *Yun* also discloses or renders obvious claim

18. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 18.

o. Claim 19

- i. Claim 19[a]: “the tunnel oxide layer includes at least one of a silicon oxide layer, an aluminum oxide layer, a silicon oxynitride layer, a molybdenum oxide layer or a hafnium oxide layer, and”**

343. See claim 19[a] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 19[a] in Ground 1A, *Yun* also discloses or renders obvious claim 19[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 19[a].

- ii. Claim 19[b]: “the tunnel oxide layer has a thickness ranging from 0.8 nm to 2 nm.”**

344. See claim 19[b] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 19[b] in Ground 1A, *Yun* also discloses or renders obvious claim 19[b]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 19[b].

p. **Claim 20**

- i. **Claim 20[a]: “the second passivation layer includes at least one of a silicon nitride layer, a silicon oxide layer or a silicon oxynitride layer, and”**

345. See claim 20[a] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 20[a] in Ground 1A, *Yun* also discloses or renders obvious claim 20[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 20[a].

- ii. **Claim 20[b]: “the second passivation layer has a thickness ranging from 70 nm to 120 nm.”**

346. See claim 20[b] in Ground 6 regarding Sakai’s disclosure. Moreover, as discussed in claim 20[b] in Ground 1A, *Yun* also discloses or renders obvious claim 20[b]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* and *Yun* disclose or renders obvious claim 20[a].

XXII. GROUNDS 7 AND 7A: CLAIM 10 IS RENDERED OBVIOUS BY SAKAI (AND OPTIONALLY YUN) IN VIEW OF YU

A. RATIONALE TO COMBINE SAKAI AND YU (AND OPTIONALLY YUN)

347. As discussed in Grounds 1A, 4, and 6, Sakai, Yu, and Yun are analogous art to the ’136 Patent.

348. See discussions of rationales to combine in Grounds 6A, 4 and 4A . *Sakai* discloses TOPCon solar cells having a textured front side that is passivated with a silicon nitride film and optionally an oxide film (see claim 1[e], Ground 6)

but is silent on the specific oxide used and on the thickness of those layers when an oxide film is used. Therefore, POSITAs would have found it obvious to make the front side passivation films in *Sakai* or *Yun* of the compositions and thicknesses described in *Yu* for the same reasons discussed in Grounds 4 and 4A.

a. **Claim 10**

i. **Claim 10[a]: “the first passivation layer is a stacked passivation structure of an aluminum oxide layer and a silicon nitride layer,”**

349. See claim 10[a] in Ground 4 and 4A. As discussed in claim 10[a] in Ground 4, *Yu* discloses or renders obvious claim 10[a]. Moreover, as discussed in claim 10[a] in Ground 4A, *Yun* also discloses or renders obvious claim 10[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* (and optionally *Yun*) and *Yu* disclose or renders obvious claim 10[a].

ii. **Claim 10[b]: “the aluminum oxide layer has a thickness ranging from 2 nm to 10 nm, and”**

350. See claim 10[b] in Ground 4 and 4A. As discussed in claim 10[b] in Ground 4, *Yu* discloses or renders obvious claim 10[b]. Moreover, as discussed in claim 10[b] in Ground 4A, *Yun* also discloses or renders obvious claim 10[b]. Therefore, for the same reasons discussed in those sections and this ground,

the combination of *Sakai* (and optionally *Yun*) and *Yu* disclose or renders obvious claim 10[b].

iii. Claim 10[c]: “the silicon nitride layer has a thickness ranging from 50 nm to 110 nm.”

351. See claim 10[c] in Ground 4 and 4A. As discussed in claim 10[c] in Ground 4, *Yu* discloses or renders obvious claim 10[c]. Moreover, as discussed in claim 10[c] in Ground 4A, *Yun* also discloses or renders obvious claim 10[c]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* (and optionally *Yun*) and *Yu* disclose or renders obvious claim 10[c].

XXIII. GROUND 8 AND 8A: CLAIM 11 IS RENDERED OBVIOUS BY SAKAI (AND OPTIONALLY YUN) IN VIEW OF FANG

A. RATIONALE TO COMBINE SAKAI AND FANG (AND OPTIONALLY YUN)

352. As discussed in Grounds 1A, 5, and 6, *Sakai*, *Fang*, and *Yun* are analogous art to the '136 Patent.

353. See Grounds 5 and 5A rationale to combine. *Sakai* discloses TOPCon solar cells having a textured front side that is passivated with a silicon nitride film and optionally an oxide film (see claim 1[e], Ground 6) but is silent on the specific oxide used, the thickness of those layers when an oxide film is used, or whether it may include additional passivating layers on the front surface. Therefore, POSITAs would have found it obvious to make the front side passivation films in *Sakai* or *Yun*

of the sublayers and thicknesses described in *Fang* for the same reasons discussed in Grounds 5 and 5A.

a. **Claim 11**

- i. **Claim 11[a]: “the first passivation layer is a stacked passivation structure of an aluminum oxide layer, a silicon nitride layer and a silicon oxynitride layer sequentially stacked,”**

354. See claim 11[a] in Ground 5 and 5A. As discussed in claim 11[a] in Ground 5, *Fang* discloses or renders obvious claim 11[a]. Moreover, as discussed in claim 11[a] in Ground 5A, *Yun* also discloses or renders obvious claim 11[a]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* (and optionally *Yun*) and *Fang* disclose or renders obvious claim 11[a].

- ii. **Claim 11[b]: “the aluminum oxide layer has a thickness ranging from 2 nm to 10 nm,”**

355. See claim 11[b] in Ground 5 and 5A. As discussed in claim 11[b] in Ground 5, *Fang* discloses or renders obvious claim 11[b]. Moreover, as discussed in claim 11[b] in Ground 5A, *Yun* also discloses or renders obvious claim 11[b]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* (and optionally *Yun*) and *Fang* disclose or renders obvious claim 11[b].

iii. Claim 11[c]: “the silicon nitride layer has a thickness ranging from 40 nm to 80 nm, and”

356. See claim 11[c] in Ground 5 and 5A. As discussed in claim 11[c] in Ground 5, *Fang* discloses or renders obvious claim 11[c]. Moreover, as discussed in claim 11[c] in Ground 5A, *Yun* also discloses or renders obvious claim 11[c]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* (and optionally *Yun*) and *Fang* disclose or renders obvious claim 11[c].

iv. Claim 11[d]: “the silicon oxynitride layer has a thickness ranging from 10 nm to 60 nm.”

357. See claim 11[d] in Ground 5 and 5A. As discussed in claim 11[d] in Ground 5, *Fang* discloses or renders obvious claim 11[d]. Moreover, as discussed in claim 11[d] in Ground 5A, *Yun* also discloses or renders obvious claim 11[d]. Therefore, for the same reasons discussed in those sections and this ground, the combination of *Sakai* (and optionally *Yun*) and *Fang* disclose or renders obvious claim 11[d].

XXIV. SECONDARY CONSIDERATIONS

358. Should the Patent Owner put forth any alleged evidence of secondary considerations in this proceeding or the related litigation, I reserve the right to

consider such evidence, to consider whether any such evidence has a nexus to any claims of the Challenged Patent, and to update my analysis.

XXV. CONCLUSION

359. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. I further understand that willful false statements and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Executed on February 18, 2026



E. Fred Schubert, Ph.D.