

**UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

SEG MANUFACTURING INC., NEW ENERGY
IMPORTS INC., SEG SOLAR INC., PT. SEG SOLAR
MANUFAKTUR INDONESIA, and SEG ENERGY
SINGAPORE PTE. LTD.,

Petitioners,

v.

SHANGHAI JINKO GREEN ENERGY ENTERPRISE
MANAGEMENT CO., LTD. and ZHEJIANG JINKO
SOLAR CO., LTD.,

Patent Owner.

Case No. IPR2026-00230

U.S. Patent No. 11,824,136

**DECLARATION OF DR. MILTIADIS HATALIS
IN SUPPORT OF PATENT OWNER'S PRELIMINARY RESPONSE**

I. INTRODUCTION

1. I, Dr. Miltiadis Hatalis, declare as follows. I am over 18 and competent to make this declaration. My statements are based on my personal knowledge, education, professional experience, and the materials identified in Section III.

2. I have been retained as an independent technical consultant by counsel for Shanghai Jinko Green Energy Enterprise Management Co., Ltd. and Zhejiang Jinko Solar Co., Ltd. (“Jinko” or “Patent Owner”) to support Patent Owner’s Preliminary Response in IPR2026-00230, addressing U.S. Patent No. 11,824,136 (the ’136 Patent) (EX1001).

3. I have been asked to provide technical opinions on the ’136 Patent (U.S. Patent No. 11,824,136 (EX1001)); the prior art cited in the Petition (including Ye, Yun, Sakai, and Basu, and additional references); the level of ordinary skill; how a POSITA would have understood the ’136 Patent and the asserted prior art; and whether the Petition shows a reasonable likelihood that any challenged claim is unpatentable.

4. I am compensated at my standard consulting rate. My compensation is not contingent on the substance of my opinions or any outcome; I have no financial interest in any party.

5. My qualifications are summarized in Section II and detailed in my CV. My opinions are based on my knowledge, training, experience, the Section III materials, and the Section IV legal standards.

II. BACKGROUND AND QUALIFICATIONS

6. My complete qualifications appear in my curriculum vitae; what follows summarizes those most relevant here.

7. I am a Professor of Electrical and Computer Engineering at Lehigh University, where I have held a full-time faculty appointment since 1987.

8. I received a B.S. in Physics from Aristotle University, Greece; an M.S. in Electrical Engineering from SUNY Buffalo; and a Ph.D. in Electrical Engineering from Carnegie Mellon (1987). I joined Lehigh's Department of Electrical and Computer Engineering that year as Assistant Professor, was Associate Professor from 1991 to 1995, and have been a full Professor since 1995.

9. At Lehigh I served as Associate Director of the Microelectronics Research Laboratory (1988-1993), Director of the Display Research Laboratory (1992-2018), and Interim Director of the Sherman Fairchild Center for Solid State Studies (2010-2013). From 2003 to 2008 I concurrently served as Professor of Computer Science at Aristotle University, Greece.

10. From 1987 to 2015 I consulted for several companies including IBM, Kodak, Sharp, Air Products, and Motorola Solutions on electronic materials,

semiconductor devices, and microelectronic systems. In 1992 I was a visiting scientist at XEROX PARC.

11. In 1992 I established and directed a Lehigh cleanroom for research on thin-film materials and devices for flat-panel displays, flexible electronics, photovoltaics, and large-area microelectronic systems. I have raised over \$13 million in research funding from DARPA, ARL, NSF, NASA, the Commonwealth of Pennsylvania, and industrial sponsors including Corning, IBM, Kodak, Sharp, and Northrop Grumman.

12. Since 1984 my research has focused on thin-film electronic materials and devices, microfabrication, novel circuits, and integrated microsystems. My Lehigh group pioneered devices and circuits on flexible substrates, AMOLED displays, and addressable sensor arrays.

13. During my Ph.D. (1984-1987) and later as a Lehigh faculty member I pioneered low-temperature solid-phase crystallization of amorphous silicon, a technique used in manufacturing ICs, solar cells, and flat-panel displays. I routinely use the same microfabrication equipment as the semiconductor, PV, and FPD industries, including PECVD, LPCVD, sputter and e-beam deposition, photolithography, RIE and wet etching, and characterization tools including optical microscopy, SEM, TEM, AFM, and electrical characterization.

14. I have authored or co-authored about 180 publications, including peer-reviewed articles, conference proceedings, three issued U.S. patents, and two book chapters on polysilicon TFT technology and on polysilicon TFTs in AMOLED displays. Google Scholar shows ~5,020 citations and an h-index of ~30.

15. My papers have appeared in Thin Solid Films, J. Electrochem. Soc., Solid-State Electronics, J. Appl. Phys., J. SID, J. Materials Science, and IEEE publications (J. Display Technology, Trans. Electron Devices, J. Solid-State Circuits, Electron Device Letters); my conference papers at SID, MRS, ECS, and IEEE.

16. At Lehigh I have supervised twenty Ph.D. dissertations in semiconductors and microelectronics (1989-2016); my graduates have taken positions at Apple, IBM, Intel, Sharp, TSMC, and Motorola, and in academia in the U.S. and abroad. I have also supervised post-docs, Master's theses, and undergraduate projects, and lectured worldwide.

17. I have taught Lehigh undergraduate and graduate courses on the physics, technology, design, and fabrication of solid-state devices and ICs, including courses I introduced, "Introduction to VLSI Design," "Semiconductor Material and Device Characterization," and "Introduction to Photovoltaic Energy Systems", as well as "Principles of Electrical Engineering," "Introduction to Computer Engineering," "Electronic Circuits," and "Introduction to VLSI Circuits." Regularly

teaching photovoltaics for over 15 years has required me to remain current with modern industrial crystalline-silicon cells.

18. My research and teaching on photovoltaic devices have addressed the device physics and fabrication of crystalline-silicon solar cells across the principal industrial architectures, Al-BSF, PERC, TOPCon, SHJ, and IBC variants. I am very familiar with all of these technologies and I apply this understanding throughout.

19. I am a member of the IEEE Electron Devices Society and SID, have chaired SID-sponsored AMLCD workshops and an MRS Flat Panel Displays symposium, have peer-reviewed for scientific journals, and have served as an NSF SBIR program reviewer.

20. My microfabrication work on crystalline and thin-film silicon includes extensive alkaline and acidic wet etching of monocrystalline Si substrates. I am familiar with the crystallographic basis of the resulting pyramidal morphology and with concentrated alkaline solutions used for “alkaline polishing” or saw-damage removal, a mass-removal step that planarizes rather than textures. I am separately familiar with CMP, a distinct unit operation using slurry, pad, and mechanical pressure, and with growth of ultra-thin SiO₂ in the 1- to several-nm range, conformality, step coverage, and the role of pinhole density and local thinning in degrading device performance.

21. Through my research and teaching experience I am familiar with variety of wet and dry chemistries for cleaning, etching, and polishing applications. I am also familiar with the effect of certain additives on the behavior of certain chemistries and based on my experience I understand that two superficially similar wet chemistry steps must be kept mechanistically distinct. For example, the same wafer can be driven to polished, partially-textured, or fully-textured end points depending in small changes in chemistries.

22. A complete list of my publications, professional experience, research grants, advised dissertations, and expert-witness matters appears in my curriculum vitae.

III. MATERIALS REVIEWED

23. I am not an attorney and offer no legal opinions, but have substantial experience analyzing patents from the POSITA perspective, applied here using the Section VI.C definition.

24. I reviewed the '136 Patent (U.S. Patent No. 11,824,136 (EX1001)) and its claims in light of the specification; the prosecution histories of the '136 Patent and related applications; the Petition and supporting declaration; the cited prior art; and additional publications and references reflecting the state of the art before, at, and after the claimed invention.

25. I also relied on my education, training, and experience in semiconductor processing, thin-film device fabrication, amorphous and polycrystalline silicon thin film material, and photovoltaic device physics. Additional materials are identified at the point of reliance.

26. I considered these materials from the POSITA perspective as of the priority date in Section VI.C, informed by the Section IV legal standards.

IV. RELEVANT LEGAL STANDARDS

27. I am not an attorney and offer no legal opinions. Counsel has informed me of the standards below, which I have applied. If any standard is later determined to differ, I reserve the right to consider the effect on my opinions.

28. I have applied the priority date addressed in Section VI.C; my analyses of the state of the art and POSITA knowledge are made as of that date.

29. Claim terms are given their ordinary and customary meaning to a POSITA at the time of invention, in light of the specification and prosecution history, the same standard as district court. Intrinsic evidence controls; extrinsic evidence is less reliable and may not contradict the intrinsic record. Terms generally have the same meaning throughout the claims and specification; a patentee may be its own lexicographer.

30. Patent drawings (including prior-art figures) are not to scale unless the specification so states, and cannot alone establish a particular dimension,

dimensional relationship, or height difference. Geometric inferences from a figure must be supported by corresponding text. I apply this when evaluating Petitioner's reliance on figures.

31. Petitioner bears the burden of proving unpatentability by a preponderance, and that burden never shifts. At institution, the question is whether the petition demonstrates a reasonable likelihood that the petitioner would prevail on at least one challenged claim. Mere identification of a possibility is insufficient; the petition must, on its four corners, articulate sufficient evidence and reasoning for each element of each ground.

32. A claim is anticipated under § 102 only if every element, arranged as recited, is disclosed expressly or inherently in a single reference. Inherent disclosure requires that the missing element necessarily be present or necessarily result; mere possibility is insufficient. Anticipation cannot be established by combining references or disconnected embodiments.

33. A claim is obvious under § 103 if the differences between the claimed invention and the prior art would have been obvious to a POSITA at filing. The analysis rests on (i) scope/content of the prior art, (ii) ordinary skill, (iii) differences, and (iv) objective indicia.

34. For a combination, the proponent must show a POSITA reason to combine and a reasonable expectation of success, articulated with particularity,

supported by evidence, and grounded in the actual teachings of the prior art and POSITA knowledge as of the relevant date.

35. Relevant considerations include whether the prior art combines to yield predictable results; whether a POSITA could implement a predictable variation; whether a finite set of identified, predictable solutions was available; whether the claimed elements are one of a limited set of known design choices; whether the prior art teaches or suggests the modification; and whether a known technique is applied to improve a similar device in a similar way.

36. A POSITA possesses ordinary creativity and is not an automaton. Obviousness requires articulated reasoning with rational underpinnings, not conclusory statements.

37. Obviousness cannot rest on hindsight. The analysis must be conducted from the POSITA perspective at the time of invention, without using the patent's teachings as a roadmap.

38. A teaching-away reference, one that criticizes, discredits, or discourages the path to the invention, weighs against obviousness, as does a combination that would change the principle of operation of a primary reference or render it unsatisfactory for its intended purpose.

39. Objective indicia include commercial success, long-felt need, failure of others, copying, unexpected results, industry praise, and licensing on merit, provided a nexus to the claimed invention exists.

40. The POSITA is presumed aware of all pertinent prior art, of ordinary creativity, and with appropriate education and experience. My analyses use the Section VI.C definition as of the priority date.

41. I reserve the right to supplement or modify my opinions based on additional information, including positions taken by Petitioner or its declarant in subsequent submissions.

V. TECHNOLOGY BACKGROUND

A. Crystalline Silicon Solar Cells: General Principles

42. A crystalline-silicon solar cell converts photons into electrical power through three steps: optical absorption that generates (or creates) positively (*holes*) and negatively (*electrons*) charged carriers, carrier separation by a built-in carrier-selective driving force (*otherwise holes and electrons will recombine and disappear*), and extraction of the carriers by metal electrodes (*so carriers will result in flow of current to produce electric power*). In a conventional homojunction solar cell, the driving force is a p-n junction formed by diffusing one dopant species (typically phosphorus) into a wafer of the opposite type (typically boron-doped p-Si, though n-type wafers with diffused boron emitters are increasingly common).

The junction's built-in field sweeps minority carriers across the depletion region so that electrons generated in the p-region reach the n-region and holes generated in the n-region reach the p-region. The accumulation of extra holes (i.e., positive charge) in the p-region and of electrons (i.e., negative charge) in the n-region, results in a voltage difference between the p- and the n- regions of the p-n junction; this voltage difference can drive an electrical current through an external "load" when such load is connected to a solar cell via wires and result in the delivery of electrical power to the "load."

43. Crystalline silicon has an indirect ~ 1.12 eV bandgap. Due to the indirect nature of the energy bandgap in silicon, the photon absorption is weak, so the useful thickness of silicon in order to absorb photons at red and near-infrared wavelengths is tens to hundreds of micrometers. Modern wafers are relatively thin 140-180 μm thick; thus, front-side substrate texturing combined with a rear reflector is essential for capturing the long-wavelength portion of the solar spectrum known as AM1.5G.

44. Cell performance is summarized by four parameters: 1) the short circuit current density $J_{sc}(\text{mA}/\text{cm}^2)$ depends on optical coupling and internal collection; 2) the open circuit voltage V_{oc} (mV) measures quasi-Fermi-level splitting and is limited by the minority carrier lifetime which in turn depends upon the various prevalent (e.g., bulk Auger, SRH, surface, and contact) recombination mechanisms; 3) the fill factor FF which measures J-V rectangularity and is degraded by series

resistance, shunt conductance, and non-ideal recombination; and 4) the solar cell efficiency $\eta = J_{sc} \cdot V_{oc} \cdot FF / P_{in}$ where P_{in} is the incident optical power. Shah at §§ 3.4-3.5 (2020) (EX1015).

45. Modern c-Si devices are dominated by two loss categories: recombination (principally surface and contact) which depress V_{oc} and FF , and the optical losses (front reflection, shading, parasitic absorption) which depress J_{sc} . The various solar cell technologies (discussed in detail below) such as the PERC, PERT, TOPCon, and heterojunction advances have primarily attacked surface and contact recombination, because bulk Auger recombination in well-passivated material is near its physical limit. Glunz et al., Silicon-based passivating contacts: The TOPCon route*, *Prog. Photovolt. Res. Appl.* 31:341-359, at 341-342 (2023).

B. Surface Passivation in Silicon Solar Cells

46. Surface recombination at a bare silicon surface is a defect process: lattice termination creates dangling bonds whose mid-gap states cause electrons and holes to recombine within nanoseconds. The corresponding figure of merit is called the surface recombination velocity, S (cm/s) or $J_{0,s}$ (fA/cm²). Bare silicon shows $S > 10^6$ cm/s; a well-passivated silicon surface can suppress S at the dielectric-silicon interface to below ~ 10 cm/s, improving implied V_{oc} by 100-150 mV.

47. Dielectric passivation works via two mechanisms. Chemical passivation reduces interface-state density D_{it} , typically by hydrogen termination of

dangling bonds (PECVD SiNx:H is the classical example). Field-effect passivation relies on the fixed dielectric charge that causes band-bending in silicon that repels minority carriers from the surface region and thus further reduces the surface recombination. SiNx carries positive fixed charge ($Q_f \approx +10^{12}$ - 10^{13} cm⁻²), ideal for n-type surfaces such as phosphorus-diffused emitters as it repels the holes from the surface region. Al₂O₃ carries negative fixed charge ($\sim 10^{12}$ - 10^{13} cm⁻²), ideal for boron-diffused p-type emitters and high-resistivity p-type surfaces as it repels the electrons from the surface region.

48. Dielectric-to-surface pairing is not arbitrary. SiNx on a phosphorus emitter (Al-BSF/PERC front) and Al₂O₃ on a boron emitter or boron-doped surface (TOPCon front, PERC rear) are the dominant industrial schemes. The AlO_x/SiNx stack (5-30 nm Al₂O₃ capped by thicker SiNx) combines Al₂O₃ field-effect passivation with SiNx chemical passivation, due to hydrogen, and the SiNx antireflective coating property (ARC). The front passivation constrains the front metallization, as discussed in V.F.

C. The Four Cell-Architecture Classes Relevant to the Petition

49. Shah (EX1015) organizes industrial c-Si cell architectures into four classes: Al-BSF (§ 5.3), PERC (§ 5.4)/PERT (§ 5.5.1), TOPCon (§ 5.5.2), and silicon heterojunction (Ch. 7), with heterojunction-IBC as a back-contact variant. These are not interchangeable; they differ in carrier-selectivity mechanism, rear-stack

chemistry, passivation, metallization, and rear-surface preparation. The disputes in this proceeding hinge on these differences.

1. Al-BSF (Aluminum Back-Surface-Field) Cells

50. Al-BSF, dominant ~2005-2018, uses a p-type wafer with an n⁺ phosphorus front emitter, SiN_x front passivation/ARC, fire-through screen-printed Ag front contacts, and a full-area screen-printed Al rear paste that alloys during co-firing into a heavily p⁺ “back-surface field.” Shah (EX1015). The Al-alloyed p⁺ provides rear selectivity without dielectric passivation. This simple structure requires no tunnel oxide, no rear doped poly-Si, and no rear dielectric passivation; the dominant losses in this structure are recombination at the Al-alloyed rear metal contact ($J_{0,\text{rear}} \sim 200\text{-}600 \text{ fA/cm}^2$) and rear absorption in the full-area Al, capping efficiencies near ~20%.

2. PERC and PERT (Passivated Emitter / Rear-Diffused) Cells

51. PERC replaces most of the full-area rear Al with an AlO_x/SiN_x dielectric stack, and enables rear metal contact only at localized points formed by laser-ablation. Shah (EX1015). Rear J_0 drops an order of magnitude, internal back reflection improves, and industrial efficiencies reach 22-23%. PERC retains the Ag-on-SiN_x-passivated phosphorus-emitter front of Al-BSF. PERT retains a full-area rear diffusion under the dielectric, enabling bifaciality. Bifacial PERC and PERT rears are typically textured to collect rear-incident light.

3. TOPCon (Tunnel-Oxide Passivated Contact) Cells

52. TOPCon, the '136's architecture, differs fundamentally at the rear. The rear stack is (i) an ultra-thin SiO_x tunnel layer (typically 1.2-1.5 nm), (ii) a heavily doped poly-Si layer (60-150 nm; n⁺ on n-type wafers, p⁺ on p-type), and (iii) a SiN_x:H cap. Glunz at 341-343; Shah § 5.5.2 (EX1015). The SiO_x chemically passivates the c-Si surface; the doped poly-Si band-bends the underlying c-Si and, with asymmetric tunneling, yields strongly asymmetric conductivity ($\sigma_n \gg \sigma_p$ for the n⁺ case). Glunz at 341-342.

53. Modern n-type industrial TOPCon cells have a boron-diffused p⁺ front emitter passivated by AlO_x/SiN_x with screen-printed Ag/Al hybrid contact, and the n⁺ poly-Si/SiO_x/c-Si TOPCon stack on the rear. U.S. Patent No. 11,824,136 (the '136 Patent) at 1:21-37 (EX1001); Glunz at 343-345, Table 1.

54. Central to the disputes: the sub-2-nm tunnel oxide's passivation and carrier-selectivity functions are exquisitely sensitive to thickness uniformity and underlying silicon topography (see V.G). That sensitivity is absent in PERC, PERT, Al-BSF, and heterojunction cells, none of which uses a sub-2 nm tunneling oxide.

4. Silicon Heterojunction and Heterojunction-IBC Cells

55. Silicon heterojunction (SHJ) forms carrier-selective contacts using hydrogenated amorphous-silicon stacks, no poly-Si, no tunnel oxide. Each face has a thin (~5 nm) intrinsic a-Si:H(i) buffer (chemical passivation by H-termination),

followed by a doped a-Si:H(n or p) providing selectivity through band offsets. Glunz at 342 (2023); Shah (EX1015). Transport is governed by band-edge alignment and defect-mediated transport, not tunneling. SHJ processing is restricted below ~200 °C, precluding co-fired screen-printed contacts and requiring TCOs with low-temperature metallization.

56. A heterojunction interdigitated-back-contact (HJ-IBC) cell moves both polarities to the rear, with n-type and p-type a-Si:H stripes patterned by shadow masks or laser/photolithography. The front carries only passivation and ARC. Because rear patterning relies on alignment fiducials, rear features in HJ-IBC are often deliberately introduced for alignment-mark visibility, an entirely different function from rear topography in TOPCon.

D. Front-Side Texturing of Crystalline Silicon Cells

57. The front face of a monocrystalline cell is textured.

58. Pyramidal texture serves two beneficial functions. First, it reduces specular reflectance and second, refracted rays enter silicon at oblique angles, lengthening the optical path. However, the increased surface area raises surface recombination.

59. Front-face morphology does not predict rear-face morphology when the two faces undergo different processing. The lattice is centrosymmetric, but anisotropic etching exploits lattice anisotropy to create topography; morphology is

set by etch chemistry, time, temperature, and subsequent processing, not by the underlying lattice.

60. Pyramid morphology is intrinsically non-uniform: a typical textured front shows distributed heights and base widths, with truncated and partially-merged pyramids interspersed. Pyramid-tip density (apices/area) is a derived statistical property that plays a role in Ag-on-SiN_x contact formation on phosphorus-emitter fronts (V.F). Front-face texturing is governed by optical coupling, conformal passivation, and fire-through contact statistics on a phosphorus emitter; rear optimization endpoints differ by architecture.

E. Rear-Side Preparation Strategies and Their Architecture Dependence

61. Rear-side preparation is architecture-specific, driven by the rear carrier-selective structure, passivation chemistry, bifacial vs. monofacial operation, and rear metallization. It is not a single “polish the rear” step.

62. The Al-BSF rear is contacted with full-area Al paste that alloys into the silicon. The rear is typically as-sawn or lightly etched; texture is neither required nor avoided, because the dominant carrier-selective effect is the Al-alloyed p⁺ region.

63. The PERC monofacial rear is dielectric-passivated (AlO_x/SiN_x) with local laser-opened contacts.

64. Bifacial PERT rears are usually textured, for the same optical reasons that texturing helps on the front; a polished bifacial rear gives up rear-incident J_{sc}.

65. The heterojunction rear is conformally coated with a-Si:H stacks and a transparent conductive oxide TCO. Texture on both faces is the standard SHJ practice.

66. Alkaline-polishing the TOPCon rear before tunnel-oxide growth is what the '136 identifies as imperfect: a polished rear leaves residual roughness translating into oxide nonuniformity '136 Patent at 1:21-37, 5:1-19 (EX1001), while a pyramid-textured rear leaves apices and (111) facets that perturb oxide thickness. The '136's controlled polygonal-topped microstructure (top-surface $\leq 45 \mu\text{m}$) sits between the extremes because the tunnel-oxide function imposes a different optimum from PERC (polished) or bifacial PERT (textured).

67. One prior-art bifacial morphology is the truncated-pyramid or platform rear: upper pyramid portions are etched away, leaving flat-topped frusta with sloped sidewalls. Truncation reduces rear surface area for recombination while preserving some rear-incident light trapping. In bifacial PERT or Al-BSF the goal is an optimum between optical gain and recombination loss on the dielectric-passivated rear, fundamentally different from a TOPCon rear, which must support uniform tunnel-oxide growth and where rear light coupling is secondary because the rear is full-area-coated. Importing a bifacial rear onto a TOPCon stack imports a feature optimized for an incompatible function.

68. The four prior-art references map onto the four architectural classes: Ye, a TOPCon cell (n-type wafer, boron p+ front, AlOx/SiNx front, alkaline-polished rear, SiOx/n+-poly-Si rear); Yun, a bifacial PERT cell with platform-shaped truncated-pyramid rear and dielectric passivation on both faces; Basu, an Al-BSF cell (n+ phosphorus front, fire-through pure-Ag on SiNx, full-area Al rear); and Sakai, a heterojunction-IBC cell (interdigitated n- and p-type a-Si stripes on the rear). The mismatches, different front chemistries, paste systems, rear-stack architectures, and rear-topography optima, are the architectural-incompatibility issues addressed ground-by-ground below.

F. Screen-Printed Front Contact Formation and Its Architecture Dependence

69. The screen-printed Ag front-contact paste consists of micron-scale Ag particles, an organic binder that burns out during firing, and a few wt% lead-based borosilicate “glass frit” (PbO + B₂O₃ + SiO₂ + minor oxides). Fields et al., The formation mechanism for printed silver-contacts for silicon solar cells*, Nat. Commun. 7:11143 at 2 (2016). The wafer is screen-printed, dried, and rapidly fired in a belt furnace peaking near 750-800 °C for a few seconds.

70. The mechanism elucidated by in-situ XRD (Fields) proceeds in stages. Between ~500 and 650 °C, PbO in the molten frit etches the SiNx, exposing the silicon emitter (consistent with $2 \text{ PbO} + \text{SiNx} \rightarrow 2 \text{ Pb} + \text{SiO}_2 + (\text{x}/2) \text{ N}_2$). Fields at 2-3. Above ~650 °C, Ag dissolves into the molten glass as Ag⁺; on cooling, Ag

precipitates as nanocrystals in the resolidified glass intermediate layer, with some direct Ag deposition on the exposed emitter. Fields at 1. Conduction is dominated by tunneling between the bulk Ag finger and the c-Si emitter through the Ag-nanocrystal-decorated glass.

71. Two corollaries are central. First, the fire-through contact reaches silicon only where PbO has locally etched through the SiN_x. Pyramid tips, sharp apices where SiN_x is locally thinned and curvature concentrates stress, are statistically the most favorable burn-through sites and the most favorable sites for Ag/c-Si contact formation. Pyramid-tip density correlates with available contact sites under each Ag finger; reducing average pyramid height while holding finger area constant reduces tip density and contact sites, increasing contact resistance and degrading FF. This is the mechanism Basu measures on Al-BSF cells (sharing Ag/SiN_x/n⁺ chemistry with PERC). Basu at § 3.

72. Second, this mechanism is specific to its front chemistry: a SiN_x-passivated phosphorus n⁺ emitter with pure-Ag paste co-fired in one step. It does not directly transfer to TOPCon, whose front is a boron p⁺ emitter passivated by AlO_x/SiN_x. A low-resistance contact to p⁺ boron requires an Ag/Al paste, and fire-through must traverse both SiN_x and AlO_x. Pyramid-tip statistics governing Ag/SiN_x/n⁺ on Al-BSF or PERC do not govern Ag-Al/SiN_x/AlO_x/p⁺ on TOPCon.

Treating an improvement in the fill factor (FF) reported on a PERC/Al-BSF front as if it transfers to TOPCon is an error.

G. Tunnel-Oxide Physics in TOPCon

73. The tunnel oxide is the defining technological feature of TOPCon. Three properties of the tunnel oxide bear directly on the disputes.

74. The TOPCon tunnel oxide is sub-2 nm; industrial values are typically 1.2-1.5 nm and rarely outside 1.0-2.0 nm. Glunz, Choi et al., Structural evolution of tunneling oxide passivating contact upon thermal annealing, Sci. Rep. 7:12853 at 1 (2017). Transport is direct quantum tunneling, $T \propto \exp(-2\kappa d)$. For a 3 eV SiO₂ barrier and electron effective mass $\sim 0.3 m_e$, $\kappa^{-1} \sim 1 \text{ \AA}$, so a 1-3 Å thickness change changes the tunneling current by an order of magnitude. The electron/hole tunneling asymmetry is what makes the contact carrier-selective. Thinning the oxide to direct band-to-band conduction through pinholes destroys that asymmetry.

75. Above a thermal-budget threshold, the tunnel oxide develops pinholes, sub-10 nm discontinuities where doped poly-Si directly contacts c-Si. Glunz at 343-344 (2023). At controlled density, pinholes can be a desirable conduction pathway and form the basis of the POLO route, which uses a thicker oxide ($\sim 2\text{-}3 \text{ nm}$) with deliberate pinholes. Glunz at 343. In the direct-tunneling TOPCon regime, uncontrolled thinning or pinholes create short-circuit paths that destroy carrier selectivity and raise J_0,c . As Choi concluded, “[t]he locally reduced tunnel oxide

introduces direct contact between the c-Si wafer substrate and n⁺ poly-Si, transporting both electrons and holes that deteriorates the carrier selectivity of the TOPCon passivating contact.” Choi at 8.

76. The tunnel oxide is grown or deposited as a conformal film tracking the silicon surface at sub-nanometer fidelity. Whatever rear topography exists is reproduced in the oxide thickness profile, because oxide-growth chemistry is rate-limited at the Si/oxide interface and sensitive to curvature, orientation, and local field. A rear planarized to angstrom-scale flatness offers no consistent nucleation template for sub-2 nm growth at industrial throughputs; the oxide grows non-uniformly. Rear topography is therefore the upstream variable setting oxide uniformity, and thus carrier selectivity, contact resistivity, and Voc/FF.

77. Because the oxide is 1-2 nm, the underlying silicon topography propagates almost entirely into oxide geometry. Sharp convex features (pyramid apices) and sharp concave features (pyramid valleys) both perturb local oxide thickness, because growth rate varies with orientation, curvature-induced stress locally accelerates or retards growth and can drive thinning during the poly-Si anneal, and for chemically grown oxides, mass transport into concave features differs from transport over convex apices. On pyramidal-textured surfaces the tunnel oxide cannot be simultaneously uniform and ultra-thin.

78. This conformality requirement is why ALD has gained traction for tunnel oxides on non-polished rears: ALD's self-limiting half-reactions deposit one atomic layer at a time, achieving near-perfect conformality on textured topography in a way thermal or chemical oxidation cannot. The conformality penalty for textured-rear TOPCon motivates the deposition-method choice.

79. Conformality has a hard geometric floor. A 1.2-1.5 nm oxide is only a few silicon lattice constants thick; wrapping rear features microns in height gives feature-to-oxide ratios of 10^3 - 10^4 . No deposition method, thermal, chemical, ozone, plasma, or ALD, can simultaneously deliver 1-2 nm thickness across the entire rear, freedom from pinholes in concave valleys, and wafer-to-wafer reproducibility when the rear presents micron-scale convex platforms with sharp sidewalls. Exponential thickness dependence converts modest excursions into order-of-magnitude swings in local current density; a single sub-10 nm pinhole short-circuits selectivity over many times its footprint. The sub-2 nm-oxide/multi-micron-topography incompatibility is a device-physics constraint, not an engineering preference.

80. Together these three properties, exponential thickness sensitivity, pinhole formation under thermal stress, and the conformality penalty, explain why the '136 Patent treats controlled rear roughness as a manufacturing variable. The claimed non-pyramid first substructures with polygonal tops, partially stacked, top-

surface size $\leq 45 \mu\text{m}$ produce a rear topography on which the tunnel oxide can be grown uniformly enough to preserve carrier selectivity. '136 Patent at 7:15-29, 7:62-8:9, 8:41-50, 8:62-9:1, 9:30-40. Polished rears leave residual non-uniformity that sub-2 nm oxide growth amplifies; pyramidal-textured rears introduce sharp apices and (111) facets that perturb oxide thickness. The '136 Patent's polygonal-topped, stacked rear presents controlled flat tops separated by controlled vertical steps, supporting uniform oxide growth with optical and surface-area properties intermediate between polished and textured.

H. Synthesis: Why Architecture Matters to the Petition

81. The Petition's cross-architecture mappings are problematic on every axis. Front passivation: SiN_x on n^+ phosphorus (Al-BSF/PERC); $\text{AlO}_x/\text{SiN}_x$ on p^+ boron (TOPCon/PERT-boron); a-Si:H(i)/(p) (SHJ). Front paste: pure Ag (SiN_x/n^+); Ag/Al ($\text{SiN}_x/\text{AlO}_x/p^+$); low-T Ag (SHJ). Rear carrier-selectivity: Al-alloyed p^+ BSF; dielectric-passivated local contacts (PERC); $\text{SiO}_x/\text{poly-Si}$ (TOPCon); a-Si:H(i)/(n or p) (SHJ); alternating a-Si:H stripes (HJ-IBC). Rear topography optimum: as-sawn/lightly etched (Al-BSF); polished (monofacial PERC); textured (bifacial PERT); conformally textured (SHJ); controlled, uniform (TOPCon).

82. A feature that helps one architecture often has no operative mechanism, or an actively detrimental effect, in another. Reduced pyramid-tip density that raises FF on an Al-BSF front has no analog on a TOPCon front, which contacts a boron p^+

emitter through AlOx. Rear texture for HJ-IBC alignment-mark visibility has no analog on TOPCon, whose rear is full-area-coated. Rear texture for rear-incident light capture on a bifacial Al-BSF is the opposite of the controlled, uniform topography a TOPCon rear requires. These architecture-specific mechanisms are why the Petition's cross-architecture borrowings require, at minimum, an explanation of how the borrowed feature could operate in its new home.

83. With that technology background in place, I now turn to the level of ordinary skill in the art, claim construction, and the specific grounds of the Petition.

VI. THE '136 PATENT

A. Overview of the '136 Patent's Technology

84. I have studied the '136 Patent (EX1001), including its specification, drawings, and claims. The '136 Patent is directed to a TOPCon solar cell, a photovoltaic module using such cells, and a manufacturing method. (EX1001 at 1:21-25; claim 1; claim 13.) It provides a surface-engineering scheme in which the front and rear faces of an n-type monocrystalline silicon wafer are given different, asymmetric micro topographies tuned to the optical and electrical job each face must do.

85. The front ("second texture structure 11") is a conventional anisotropically-etched random upright pyramid array. EX1001 at 5:21-35; FIG. 2 (EX1001). The pyramids are substantially tetrahedra or pentahedra, height $\leq 5 \mu\text{m}$

(preferably 2-5 μm). (EX1001 at 7:28-43.) The $\{111\}$ -bounded pyramidal front suppresses Fresnel reflection via double-bounce geometry and lengthens the path of weakly-absorbed near-infrared photons. (EX1001 at 5:27-35; 19:1-18.) A first passivation layer 20 (typically $\text{Al}_2\text{O}_3/\text{SiN}_x$) is deposited on the pyramidal front, with no diffused emitter interposed. (EX1001 at FIG. 1; 5:43-6:13; 8:13-9:7.)

86. The rear (“first texture structure 12”) is deliberately not pyramidal. The patent calls it a “non-pyramid-shaped microstructure” with a “substantially ‘step’ profile” formed by two or more “first substructures 121” “at least partially stacked.” (EX1001 at 9:35-50; FIGs.3, 4a, 4b.) Substructure top surfaces are flat polygonal planes (diamonds, squares, trapezoids), one-dimensional top-surface size $L \leq 45 \mu\text{m}$ (preferably 10-15 μm), vertical step $H \leq 2 \mu\text{m}$ (preferably 0.3-1.2 μm). (EX1001 at 10:1-35.) On this rear the patent forms the TOPCon stack: ≈ 0.8 -2 nm tunnel oxide, 60-200 nm doped poly-Si, and a 70-120 nm SiN_x -based second passivation. (EX1001 at 11:10-13:25.)

87. The result is a bifacially-engineered TOPCon cell: the front is optimized for optical capture and front passivation directly against textured silicon, while the rear is given just enough controlled vertical relief, not pyramidal relief, to host a uniform tunnel-oxide/poly-Si stack without the parasitic problems historically plaguing TOPCon manufacturing.

B. The Problem the '136 Patent Solves

88. The patent responds to a rear-side process problem in n-type TOPCon. The flow includes boron diffusion on the front, which leaves borosilicate-glass (“BSG”) wrap-around on the rear; this is removed by an oxidizing acid and “cleaned” by alkaline polishing of the rear. (EX1001 at 1:30-55; 2:1-25.) Industrial practice has been to polish the rear as flat as throughput allows before depositing the tunnel oxide. (Id.)

89. A too-flat rear is, counterintuitively, a poor surface on which to grow a uniform 1-2 nm tunnel oxide at production speeds. The oxide is load-bearing at the sub-nanometer scale: its thickness and uniformity govern carrier-selective tunneling, suppress recombination, and set rear contact resistivity. (Choi at 1, 8 (2017) ($\approx$ 1.2-1.5 nm optimum; localized thinning “deteriorates the carrier selectivity”).) On an over-planarized rear, the oxide grows non-uniformly, producing thin-spots and pinholes. Phosphorus from the doped poly-Si then diffuses through those thin-spots in localized “spikes,” raising parasitic recombination and contact resistivity and, under firing, promoting blistering and delamination. (EX1001 at 2:1-35; 10:35-60.) These failure modes degrade Voc, FF, and η .

90. The '136 solution is a controlled, non-pyramidal, polygonal-step rear small enough to avoid high-recombination pyramidal texture but rough enough to provide stable nucleation sites for uniform oxide growth. The $\leq 2 \mu\text{m}$ vertical step

and $\leq 45\ \mu\text{m}$ polygonal top define the window in which the rear presents sufficient step-riser density to seed uniform oxide growth, lacks sharp apices that concentrate field or interface recombination, and keeps rear area enhancement low enough to manage surface recombination. (EX1001 at 10:35-11:8; 14:1-18.) Table 3 and the Comparative Examples confirm that excursions above the $\leq 2\ \mu\text{m}$ bound of dependent claim 2, or to a fully pyramidal rear, degrade tunnel-oxide uniformity, contact resistivity, FF, and Voc. (EX1001 at 22:5-24:5.)

91. The '136 solves a throughput-vs-uniformity problem at the rear of an n-type TOPCon cell, replacing “polish-it-flat” with a controlled, sub-45 μm , partially-stacked polygonal microstructure on which a sub-2 nm tunnel oxide grows uniformly at production speed. The front pyramidal texture is preserved for optics; the two textures are deliberately asymmetric, pyramids on front, stepped polygons on rear. That asymmetry is a structural attribute of the claim.

C. Level of Ordinary Skill in the Art (POSITA)

92. Based on my work with engineers in crystalline-silicon PV and my reading of the '136 Patent and surrounding prior art, a POSITA as of the August 4, 2021 priority date would have had (a) a B.S. in materials science, electrical engineering, physics, chemical engineering, or a closely related discipline with three to five years of practical experience in crystalline-silicon solar-cell design,

fabrication, or process development; or (b) an M.S. or Ph.D. in one of those disciplines with one to two years of equivalent experience.

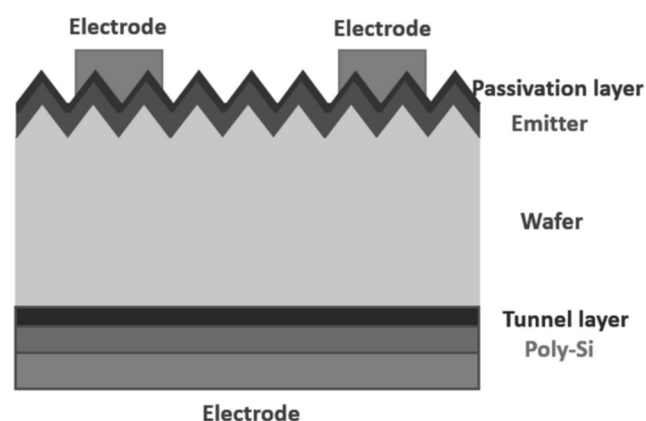
93. My qualifications exceed this level. I hold a Ph.D. in the relevant disciplines and have decades of research and teaching experience in semiconductor processing, thin-film transistor and PV device design, and silicon surface chemistry, with hands-on experience in the process steps at issue. My opinions are offered from the POSITA perspective described.

VII. ANALYSIS OF GROUND 1 (YE + BASU)

A. Ye or the Ye+Basu Combination Do Not Teach Several Claim Limitations

94. Ye is a Chinese invention patent application directed to “a method for preparing a laminated thin-film passivated-contact structure” for TOPCon solar cells on n-type crystalline silicon substrates. (Ye at Absract, [0030]). Ye’s invention addresses a silicon thin film delamination problem present in TOPCon solar cells during the high temperature crystallization of the doped amorphous silicon thin film formed on the tunnel oxide via the Plasma Enhanced Chemical Vapor Deposition (PECVD) method. (Ye at [0008]). Ye explains that “PECVD-grown amorphous silicon films contain a high hydrogen content” and that during annealing “hydrogen out-diffusion may occur, which damages the adhesion between the silicon film and the silicon oxide interface, causing film delamination.” (Ye at [0008]). Ye provides a materials solution to this PECVD amorphous silicon delamination problem.

Specifically, Ye inserts “an intrinsic or doped silicon-carbon thin film” interlayer between the tunnel oxide and the doped amorphous silicon thin film. (Ye at [0011]). Ye teaches that “the silicon-carbon thin film has good adhesion to silicon oxide and also exhibits high mechanical strength. Therefore, during the high-temperature crystallization, the silicon-carbon film is less prone to delamination.” (Ye at [0020]). The embodiment 2 described by Ye uses a TOPCon device structure known in the prior art and depicted in FIG. 1. (Ye at [0025], FIG. 1). Ye discloses that the wafers were 180 μm thick, n-type Czochralski-grown monocrystalline silicon wafers “subjected to double-sided alkaline polishing” (Ye at [0030]). With respect to the other layers shown in Figure 1, Ye discloses that the P+ front emitter was formed by boron-diffusion, the front passivation layer comprised of $\text{Al}_2\text{O}_3/\text{SiN}$ layers, and that the front and rear electrodes were formed by screen-printing followed by firing. (Ye at [0038].)



95. With that as the architectural backdrop, I take the three claim-limitation gaps in turn.

1. Ye is silent on rear-substructure size

96. Claim 1[b] requires “a one-dimensional size of the top surface of the outermost first substructure” $\leq 45 \mu\text{m}$. Ye is silent on rear-substructure size. According to Ye’s disclosures, the rear of the substrate was exposed to an “alkaline polishing” twice, first during the wafer preparation when the wafers were “subjected to double-sided alkaline polishing” (Ye at [0030]), and a second time after the boron diffusion for forming a p⁺ emitter on the front “then backside alkaline polishing is carried out.” (Ye at [0038]). However, Ye gives no numerical dimension for any rear feature, no top-surface size, no diagonal, no pitch, no step height. Figures 2 and 3 of Ye contain no dimensional scale marker and no indication regarding the optical imaging magnification factor. Thus, it is not possible to extract quantitative information regarding the size of any substructure that might have been formed on the rear surface. As I explained above a POSITA would understand that the two processing steps disclosed explicitly by Ye, i.e.,: 1) a “double-sided alkaline polishing” prior to forming the front emitter and 2) a “backside alkaline polishing” prior to forming the tunnel oxide, are intended for specific purposes with the former aiming to remove the wafer saw damage and providing the front texture depicted in Figure 1 and for the latter to remove the boron doped rear surface layer and polish the rear surface to remove any texture formed on the rear during the initial “double-sided alkaline polishing.” A POSITA would understand that Ye’s solar cell structure

will not function properly without removing both the saw damage from the front and rear substrate surfaces and the boron doped layer from the rear surface of the substrate after forming the p⁺ emitter on the front surface. A POSITA would further understand that neither of these removal steps are designed or intended to leave controlled polygonal stepped substructures on the rear surface of the semiconductor substrate.

97. Reading “ $\leq 45 \mu\text{m}$ ” as satisfied by any “non-zero” rear feature, as Petitioner’s declarant assumes (Schubert Decl. at ¶ 90 (EX1003)), is technically meaningless. Every silicon wafer surface has features of some non-zero size, from atomic steps (sub-nm) to saw-mark roughness (μm) to wafer-bow (mm). Moreover, the two alkaline polishing steps disclosed by Ye could leave a surface with “non-zero” features but such a surface would lack the claimed first substructures entirely. A POSITA would also know that even an atomically flat surface would reconstruct forming “non-zero” surface features which could be exaggerated by the growth of a silicon oxide layer (e.g., the tunnel oxide) or the deposition of thin films (e.g., the silicon carbon layer). Thus, a “non-zero” reading is silent on whether the wafer has the controlled, polygonal-topped, partially-stacked topography the patent claims, and is incompatible with the specification’s enumerated embodiments (2 μm , 5 μm , 8 μm , ..., 45 μm). (EX1001 at 10:15-34 .) .

98. Petitioner’s cross-reference importing a 45 μm -or-smaller dimension into Ye, via crystallographic equivalence of (100) silicon, does not survive scrutiny. The lattice is the same on both (100) faces, but the processing history is different: front anisotropically textured (upright $\{111\}$ -bounded pyramidal facets), rear alkaline-polished (which removes a doped layer and surface texture). A POSITA would not expect that rear topography mirror front topography after different processing; the dimensions of an anisotropically-etched (100) surface and an alkaline-polished surface are determined by wet-chemistry kinetics, not lattice symmetry. Moreover, the wet-chemistry kinetics are affected by the doping of the substrate. The front surface texturing occurs before the boron diffusion while the “backside alkaline polishing” occurs after the boron diffusion step.

99. Importing Basu’s front-pyramid dimensions (5-8 μm) into Ye’s rear likewise fails. Basu reports no rear-side dimensions. As I explained above, Basu’s rear is an Al-BSF screen-printed Al contact with no rear topography characterization. (Basu at §§ 2.1-2.2.) Basu measures pyramid height on the front; the ’136 claim recites a top-surface size of a flat polygonal step on the rear, different geometric quantities on different surfaces of different architectures.

2. Ye does not depict or describe “partially stacked” first substructures

100. Claim 1[b] further requires “two or more first substructures at least partially stacked on one another.” Ye discloses no such structure, textual or pictorial.

Ye's text says only that the rear was "alkaline polished" (Ye at [0030], [0038]); the words "stack," "stacked," "polygon," and "step" do not appear in connection with Ye's rear texture.

101. Petitioner relies on Ye's Figure 3 for partial stacking. That misreads the figure. Ye identifies Figure 3 as "an optical microscope image showing a silicon-carbon thin film / silicon thin-film laminated structure without film blistering or delamination." (Ye at [0027]; *see also* Ye at [0026] (FIG. 2 is the delamination comparison case).) Figures 2 and 3 are paired blistering visualizations; Figure 3 is an optical micrograph of the thin-film top surface, not of the underlying silicon substrate.

102. A POSITA reading Figure 3 in context could understand the visible features as morphological artifacts of the deposited a-Si/SiC_x laminate post-crystallization-anneal, photographed to show absence of blistering. The contrast reports on the morphology of a composite film stack on a polished monocrystalline silicon wafer. A POSITA would understand that Ye's Figure 3 could include a stack of as many as three different layers of polycrystalline silicon and silicon-carbon thin films, e.g., "c-Si / SiO_x / i-poly-SiC_x (5 nm) / n⁺poly-SiC_x (15 nm) / n⁺poly-Si (150 nm)." (Ye at [0040]). Ye's specification and figure caption contain no dimensional callout connecting any Figure 3 feature to any substrate-level "first substructures." Moreover, Ye discloses no images of the silicon wafer surface alone, i.e., prior to

depositing the composite film stack, and no cross sectional images of the silicon wafer with the composite film stack.

103. Schubert Decl. at ¶ 89 (EX1003) asserts Ye's Figure 3 shows partially-stacked substructure tops. As shown, Figure 3 is, per Ye's own caption (Ye at [0027]), an optical micrograph of the deposited SiCx/Si laminate documenting absence of blistering, not a depiction of the c-Si rear topography. His ¶ 92 is a conditional: "to the extent" the A/B structures Patent Owner annotated in its litigation complaint are partially stacked, then Y/Z in Ye's Figure 3 would also be. Figure 3 has no dimensional callout, no height data, no SEM cross-section, no profilometry, the conditional is not a technical disclosure of partial stacking.

104. The A/B structures depicted in Schubert Decl. at ¶ 91 (EX1003) are different regions within a laser confocal microscopy image; such an image can accurately depict the height difference between different surface regions, and such 3D information can be visualized in a variety of ways, including a color-coded scheme. In contrast, Ye's Figure 3 lacks teachings on height differences in structures.

105. The Petition's identification of "Y" and "Z" in Ye's Figure 3 as analogous to "A" and "B" annotated by Patent Owner on a litigation exhibit (from 3D measurements of accused products) does not show that Ye discloses anything about stacked substrate substructures. Ye contains no height data, no dimensional

data, no SEM cross-section, and no AFM profile permitting a POSITA to say Figure 3 features are partially-stacked first substructures of the '136 dimensions. The Ye+Basu combination fails to disclose this limitation as Basu reports no rear-side substructures and no dimensions associated with them. As I explained above, Basu's rear surface is an Al-BSF screen-printed Al contact with no rear topography characterization. (Basu at §§ 2.1-2.2.).

B. Basu Studies a Different Cell Architecture

106. Basu is a 2015 Renewable Energy paper by Basu, Khanna, and Hameiri. Basu's is disclosing a solar cell structure that is not the same as Ye's TOPCon structure. Basu instead uses a "Back-Surface Field" (BSD) formed by alloying silicon with aluminum during an annealing step ("co-firing") of the screen-printed Al contact to push minority carriers away from the rear electrode which is a very different approach than the oxide passivation approach used in Ye's TOPCon structure. (Basu at §§ 2.1-2.2.) Moreover, the silicon substrates disclosed by Basu are p-type boron-doped compared to the n-type silicon wafers disclosed by Ye. Due to the difference in substrate type, Basu's p-type vs Ye's n-type, there are significant differences in the emitter layer formed by doping on the front surface. Basu is disclosing an N⁺ emitter formed by phosphorus diffusion while Ye is disclosing a P⁺ emitter formed by boron diffusion. Since the "TOPCon" does not appear in Basu; no tunnel oxide and no doped polysilicon is present.

107. Al-BSF was the c-Si workhorse from the 1980s through the early 2010s. Rear carrier selectivity is achieved by aluminum alloying: screen-printed Al paste reacts with silicon during co-firing to form a heavily p⁺ Al-alloyed rear layer that reflects minority electrons back to the junction. No tunnel oxide, no doped polysilicon, no carrier-selective dielectric stack on the rear. Al-BSF and TOPCon share only generic features (c-Si wafer, front diffused emitter, SiN_x ARC, screen-printed metallization). They differ in carrier-selectivity mechanism, rear passivation, rear contact scheme, dopant polarities, and dominant loss pathways. The physics mechanisms that govern the transport of minority and majority carriers (i.e., the movement of the electrons and holes), and which in turn affect the solar cell efficiency, fill-factor (FF), and contact resistivity in an Al-BSF solar cell differ to those in a TOPCon solar cell. For example, Ye's TOPCon structure relies on the tunnel oxide to: a) passivate the silicon wafer surface and thus reduce electron-hole recombination (this improves efficiency), and b) favor the tunnelling of electrons (majority carriers) through it while blocking the holes (minority carriers) from reaching the rear contact (this improves efficiency, reduces contact resistance and increases fill-factor and efficiency).

C. Basu's Pyramid-Height Findings Are Architecture-Specific

1. Basu reports no significant variation in τ_{eff} , iV_{oc} , J_{sc} ,

reflectance, Jsc, or Voc across the pyramid-height range studied

108. Basu’s actual result is more limited than the Petition suggests. Across three texture groups (A $\sim 5\ \mu\text{m}$, B $\sim 6\ \mu\text{m}$, C $\sim 8\ \mu\text{m}$), Basu found “the investigated homogeneous pyramidal surfaces are optically similar, irrespective of the pyramid heights”: the weighted average reflectance (WAR) for all was 11.6%/11.6%/11.7% before and 1.9% after forming a SiNx antireflection (ARC) layer; prompting Basu to conclude that “the investigated homogeneous pyramidal surfaces are optically similar, irrespective of the pyramid heights.” (Basu at § 3.1.2.). Basu further discloses that with respect to various important electrical parameters, including the carrier effective lifetime (τ_{eff}), the implied open circuit voltage (iVoc), and emitter saturation current density (J_0), “[n]o significant variation is observed in these three parameters for the different texture processes.” (id. at § 3.1.3). Moreover, Basu discloses that “Fig. 8 clearly indicates negligible variation of Jsc and Voc between the groups” (id. at § 3.2.1).

109. Of Basu’s measured figures of merit, only the fill factor FF (and in turn the solar cell efficiency, as the algebraic consequence) varied somewhat meaningfully with pyramid height over the range between 5 to 8 μm . (Basu at § 3.2.1.) It is important to note that even the improvement in the fill factor was very small, “a FF gain of up to 1% absolute” corresponding to “an efficiency gain of 0.4%

absolute,” (Basu at § 4.) That single finding is the entire empirical basis for Petitioner’s motivation.

2. Basu identifies the FF mechanism as Ag/glass-frit contact formation at pyramid tips on a phosphorus-doped n+ emitter

110. After ruling out sheet-resistance and finger contributions (comparable across groups), Basu performed TLM measurements and reported specific front-contact resistivities of 2.9, 3.4, and 5.3 mΩ·cm² for Groups A, B, C. (Basu at § 3.2.3.) Basu identifies the cause:

111. “[T]he difference in contact resistance for the three pyramid groups is linked to the difference in the pyramid count density (number of pyramids per unit area). Pyramid tips represent favorable sites for screen printed silver--silicon contact formation, and increasing average pyramid height reduces the pyramid count density and hence the number of potential sites for contact formation.” (Basu at § 3.2.3.)

112. Basu’s causal chain: pyramid height → count density → Ag-on-c-Si nucleation sites at tips → ρ_c → FF → efficiency. Height is result-effective in Basu only because Ag-on-phosphorus-n+ contact chemistry exists at the tips to translate density into resistance.

3. The Ag-on-pyramid-tip contact mechanism requires PbO-bearing glass-frit etching of SiN_x and Ag deposition on phosphorus-doped n+ silicon; neither chemical input exists at

Ye's front

113. The Ag-paste-on-pyramid-tip mechanism Basu invokes has been studied in detail. The most thorough mechanistic study is Fields, using in situ XRD during RTP firing; Basu cites Khanna 2015 [23] and Cabrera 2011, 2013 [24], [7].

114. The mechanism, as documented in Fields has two essential chemical inputs:

115. (a) PbO in the glass frit must etch through the SiN_x ARC to expose silicon at the pyramid tip. Molten PbO dissolves SiN_x and exposes silicon at the high-curvature apex first. Without PbO-bearing frit and an etchable SiN_x between Ag and silicon, no Ag/Si contact forms.

116. (b) The exposed silicon must be heavily phosphorus-doped n-type for Ag to form a low-resistance ohmic contact. Work-function alignment plus field emission through the n⁺ surface make the contact ohmic with low pc. Pure-Ag pastes show elevated resistance on boron p⁺ silicon, which is why industry uses Ag/Al hybrid pastes for boron-p⁺ emitters.

117. Neither input exists at Ye's front. Ye's front is a boron-diffused P⁺ emitter on n-type silicon, passivated by Al₂O₃/SiN. (Ye at [0038].) The silicon is boron p⁺, not phosphorus n⁺; the Al₂O₃ further alters dielectric-removal chemistry. The Basu Ag-on-n⁺-pyramid-tip mechanism has no analog at Ye's front.

4. N-type TOPCon front contacts use Ag/Al hybrid pastes precisely because pure-Ag pastes do not form satisfactory contacts

on boron-p⁺ emitters

118. This mismatch is documented in contemporary TOPCon literature. Glunz, Feldmann et al. (Glunz at 341-359 (2023)) identify “silver or aluminum-silver pastes” as the screen-printing technology of choice for i-TOPCon metallization. Glunz at 345 (2023). The industry uses Ag/Al hybrid pastes on n-type TOPCon p⁺ boron emitters because pure-Ag shows elevated resistance on boron-p⁺ silicon; the Al fraction alloys via an Al-Si liquid-phase reaction. The contact chemistry is fundamentally different from Basu’s Ag-on-n⁺ Al-BSF cells.

119. A POSITA optimizing n-type TOPCon front metallization does not reach for the same toolkit as one optimizing a phosphorus-emitter Al-BSF front. The two systems differ in paste chemistry, glass-frit formulation, firing window, and sensitivity to morphology. Pyramid-tip count density does not carry the same FF significance on an Ag/Al/boron-p⁺/Al₂O₃-SiN system as on a pure-Ag/phosphorus-n⁺/SiN_x system.

5. A POSITA designing a TOPCon cell would not have looked to Basu for guidance on TOPCon rear texture optimization

120. The ’136 problem is rear-side tunnel-oxide uniformity in an n-type TOPCon cell; Basu’s data address front-side Ag contact resistance in an Al-BSF cell with n

121. + phosphorus emitter. The two studies sit on opposite faces of architecturally different cells, address different loss mechanisms, and obey different

surface chemistries. A POSITA working on TOPCon rear topography would not look to an Al-BSF front-pyramid/Ag-contact paper for guidance.

122. The mismatch is also asymmetric. Basu's FF/efficiency finding is a front-contact finding tied to front-pyramid count density. Basu's rear is screen-printed Al-BSF; Basu reports no rear-side dimensions and makes no claim about the rear at all. Using Basu to fill Ye's rear-side gap asks Basu to supply a teaching it does not contain.

123. Further, a POSITA would understand that Ye directs away from a doped conductive layer located on the tunnel oxide layer. According to Ye's disclosures, a POSITA would be motivated to form a structure that includes an undoped polycrystalline silicon carbon layer "i-poly-SiCx (5 nm)" in direct contact with the tunnel silicon oxide. Ye is disclosing that when such a layer is included, (see Ye at [0039]: "c-Si / SiO_x / i-poly-SiCx (5 nm) / n⁺poly-SiCx (5 nm) / n⁺ poly-Si(120nm)," and Ye at [0040]: "c-Si / SiO_x / i-poly-SiCx (5 nm) / n⁺poly-SiCx (15 nm) / n⁺poly-Si (150 nm)") the solar cell electrical characteristics are far superior compared to solar cells when a doped conductive layer (i.e., n⁺ poly-Si (120 nm)) is in direct contact with the tunnel silicon oxide. As it is disclosed in Ye's tables shown in [0039]-[0040] the presence of an "i-poly-SiCx," (a POSITA would understand that "i-poly" stands for an "intrinsic-polycrystalline," i.e., "undoped-polycrystalline") results in higher open circuit voltage (Voc), higher short circuit

current (J_{sc}), higher fill factor (FF) and higher solar cell power conversion efficiency (Eff.). Compared to “c-Si / SiO_x / n^+ poly-Si (120 nm)” having an efficiency of around 17.5% (No.1 17.36%, No.2 17.72), Ye is disclosing that incorporating an undoped polycrystalline silicon carbon layer in direct contact with the tunnel oxide the solar cell efficiency becomes greater than 22%. (Ye at [0039]-[0040]). In the field of solar cells improving the efficiency from ~17.5% to more than 22%, i.e., an improvement of more than 4% absolute, is considered a major improvement. Note that Dr. Schubert provides as motivation to combine Ye and Basu, the improvement of 0.4% absolute in efficiency that Basu discloses; albeit the fact that this small improvement cannot be realized in Ye’s structure as I explain above. Therefore, a POSITA would understand that Ye is teaching the use of an undoped polycrystalline silicon carbon layer “i-poly-SiC_x (5 nm)” on the surface of the tunnel oxide and is teaching away from the use of a doped conductive layer.

D. No Reasonable Expectation of Success in the Proposed Combination

124. Setting motivation aside, the combination would not function. Petitioner’s theory: a POSITA adopts Basu’s “optimal” 2--5 μm range at Ye’s front and obtains Basu’s FF improvement. That improvement cannot be obtained, the mechanism producing it in Basu is absent at Ye’s front.

125. In Basu: smaller pyramids $\rightarrow$ higher count density $\rightarrow$ more Ag/frit nucleation sites on phosphorus n^+ silicon $\rightarrow$ lower $\rho_c \rightarrow$ higher FF. (Basu at § 3.2.3.)

At Ye's front, the silicon is boron p+; the dielectric is Al₂O₃/SiN; the paste is Ag/Al. The pyramid-tip Ag-nucleation events driving Basu's count-density-vs-pc relationship do not occur. A POSITA transferring Basu's pyramid-height number to Ye would have no rational basis to expect Basu's FF improvement.

126. Basu's measurements rule out alternative pathways. Reflectance, lifetime, iVoc, Joe, Jsc, and Voc do not change significantly with pyramid height across the range of 5 to 8 μm. (Basu at §§ 3.1-3.2, § 4.) Only FF moved; only Ag/n+ tip contact formation was identified as the cause. No second mechanism survives translation to Ye's chemistry.

127. The combination does not remedy the rear-side problem '136 solves. Even with Basu's 2--5 μm front-pyramid range imported into Ye, Ye's rear has been "alkaline polished" twice (Ye at [0030], [0038]), and thus remains a flat, planarized rear as depicted in Ye's Figure 1. This is opposite to the controlled, sub-45 μm, polygonal-topped, partially-stacked, non-pyramid structure claim 1[b] requires and that '136 identifies as essential to tunnel-oxide uniformity. ('136 Patent at 9:35-10:35; 22:5-24:5.) Ye + Basu leaves 1[b] unmet with no mechanism to satisfy it.

128. In sum: (a) Ye does not teach 1[b]'s rear-substructure size or partial-stacking; (b) Basu is a different architecture and problem; (c) Basu's relied-upon finding flows from contact chemistry absent at Ye's front; (d) a POSITA on TOPCon would not consult Basu's Al-BSF study; and (e) even performing the combination,

no FF improvement materializes at Ye's boron-p⁺ front, and claim 1's rear limitations remain unmet. Moreover, Ye teaches away from the 1[g] limitation as it finds that the use of an undoped polycrystalline silicon-carbon layer on the surface of the tunnel oxide layer yields to an efficiency improvement of more than 4% absolute from ~17.5% with a doped layer to over 22% with an undoped conductive layer.

129. Claim 13 re-recites claim 1's cell-level limitations and adds a solar-cell-string preamble. ('136 Patent at claim 13.) Those limitations are unmet by Ye + Basu for the same reasons as claim 1. Assembling Ye-style cells (alkaline-polished rear, no partially-stacked sub-45 μm polygonal first substructures) into strings does not produce the rear topography claim 13 requires. Petitioner's module-level testimony (Schubert Decl. at ¶¶ 114-115 (EX1003)) addresses string assembly generally; it does not supply the cell-level limitation claim 13 inherits.

VIII. ANALYSIS OF GROUND 1A (YE + YUN + BASU)

A. Overview of Ground 1A and Yun's Architecture

130. I address Ground 1A, in which Petitioner adds Yun to the Ye/Basu combination. I evaluate whether building blocks drawn from three different cell architectures fit together as Petitioner suggests. They do not.

131. Yun is a (100) monocrystalline silicon bifacial PERT-style cell with diffused front emitter and diffused BSF. Yun at [0007]; claim 1. P-type embodiment:

phosphorus N⁺ front emitter, boron P⁺ rear BSF (Yun at [0029], [0040], [0044]). N-type embodiment: boron P⁺ front emitter, phosphorus N⁺ rear BSF (Yun at [0034], [0053], [0057]). Both surfaces are passivated by SiN/Al₂O₃/SiON dielectric stacks, with screen-printed silver gridlines co-fired at 850--900 °C to make ohmic contact with the diffused silicon. Yun at [0030], [0046]-[0047].

132. The architectural distinction lies in rear-side carrier-selectivity. In Yun's PERT, selectivity comes from diffusing dopants directly into silicon to form a BSF, with rear metal fired through the dielectric for direct ohmic contact. (Yun at [0029]-[0030], [0040], [0044], [0046]-[0047].) No tunnel oxide, no polysilicon. In Ye's TOPCon cell (and the '136), selectivity uses an ultra-thin tunnel oxide (sub-2 nm SiO_x) on polished silicon with a doped polysilicon layer on top.

133. These are two different rear-side device physics. Yun was engineered for a diffused-junction bifacial cell where metal contacts silicon; Ye for TOPCon tunneling where the rear metal electrode never touches the monocrystalline silicon wafer and the dominant figure of merit is nanometer-scale tunnel-oxide uniformity. Any combination must reckon with that divergence.

B. Petitioner's Recast of Ye's Polishing as "CMP" Is Technically Wrong

134. Petitioner's combination is premised on the assertion that Ye uses "mechanical polishing," specifically CMP, and that a POSITA would have looked

to Yun's wet chemistry to reduce mechanical-damage risk. Pet. 39-40. Ye's text does not support that.

135. Ye describes two polishing steps. The starting wafer is "subjected to double-sided alkaline polishing." Ye at [0030]. In Embodiment 2, after front boron diffusion, "backside alkaline polishing is carried out." Ye at [0038]. Both name the chemistry as alkaline and the process as polishing. "Alkaline polishing" in the silicon-PV community refers to a wet chemical bath etch, not a mechanical or chemical-mechanical process.

136. CMP is a distinct industrial process. A wafer is held face-down against a rotating polishing pad while a slurry of abrasive particles (silica, alumina, or ceria) and chemical etchant is delivered under controlled pressure. Material removal combines mechanical abrasion with chemical reaction. CMP requires dedicated tooling (platen, slurry delivery, pad conditioning, end-point detection); signatures include down-force-controlled removal, near-global planarity, micro-scratches, slurry-particle embedment, and pad debris.

137. Ye discloses none of CMP's indicia: no pad, slurry, abrasive, pressure, rotational speed, end-point detection, CMP tool, or surface-finish data. What Ye describes is conventional alkaline wet polishing in a bath, embedded in an otherwise wet-chemical sequence (HF borosilicate-glass removal before, thermal oxidation after). Petitioner's CMP reading is recharacterization, not reading.

138. Petitioner's motivation premise, Yun's wet chemistry substituting for Ye's "mechanical polishing" to reduce damage risk, fails. There is no disclosed mechanical polishing in Ye and no damage risk to eliminate. Ye is wet chemistry; Yun is wet chemistry. The proposed improvement solves no problem in Ye.

139. The CMP recharacterization is inconsistent with the Petition's own usage. The Petition describes Xia as improving alkaline polishing (Pet. 54) and Sakai as forming texture by wet alkaline etching (Pet. 75), both correct. Only in Ground 1A does the Petition rename alkaline polishing as CMP, in the same paragraph proposing Yun's substitution. The renaming serves the combination argument, not the field's usage.

C. Petitioner Does Not Articulate the Combined Device

140. Setting aside CMP, Ground 1A does not specify what device results. Transplanting features across three architectures (Ye's TOPCon, Basu's PERC/Al-BSF, Yun's PERT) requires identifying which features come from which reference, how they sit, and how they couple. The Petition does not.

141. A cell has one front emitter. The Petition does not state whether the combined device uses Ye's P⁺ boron emitter (Ye at [0038]) or Basu's N⁺ phosphorus emitter (Basu at § 2.2). These are mutually exclusive, different substrate polarities, doping chemistries, passivation, and front-contact metallurgies. Ye's P⁺

boron uses $\text{Al}_2\text{O}_3/\text{SiN}$ front passivation; Basu's N^+ phosphorus uses single-layer SiN_x . One cannot run both.

142. The front metallization presents the same problem. Basu's pyramid-height effect on FF is mediated by Ag-paste contact formation at pyramid tips on the N^+ phosphorus emitter. Basu at § 3. That chemistry, Ag paste fired through SiN_x into phosphorus N^+ , is not the same as forming a contact through $\text{Al}_2\text{O}_3/\text{SiN}$ into boron P^+ , which uses different paste compositions (Ag/Al hybrids), firing profiles, and dielectric-etching. The Petition does not specify which contact system is used, and Basu's pyramid-height effect does not carry over.

143. The rear cannot simultaneously be Yun's bifacial PERT (diffused BSF, metal-to-silicon through dielectric openings) and Ye's TOPCon (tunnel oxide, doped polysilicon, metal-to-polysilicon). The Petition does not say whether the cell retains Ye's TOPCon stack over Yun's platforms, replaces it with Yun's BSF, or hybridizes. None is self-evident; each has different consequences; the Petition leaves a process engineer no way to determine which device is proposed.

144. The Petition assembles features without committing to a device. A POSITA reading Ground 1A would not have understood what device was being proposed, much less whether it would function.

D. Importing Yun's Platform Geometry into Ye's TOPCon Stack

Destroys Ye's Principle of Operation

145. Even crediting Petitioner's framing, Ye's TOPCon rear stack retained with Yun's platforms substituted for Ye's polished rear, the combination would not function as TOPCon. Yun's platforms are micrometers tall; Ye's tunnel oxide is nanometers thin, three orders of magnitude apart.

146. Yun's claim 1 specifies 2--10 μm upper-plane side length and 1--8 μm platform height, with upper plane parallel to (100) and {111}-bounded sidewalls. Yun at claim 1. Heights are 1 μm (Embod 1, Yun at [0030]), 8 μm (Embod 2, Yun at [0032]), 3 μm (Embod 3, Yun at [0034]), 6 μm (Embod 4, Yun at [0036]), i.e., 1,000--8,000 nm tall with 2,000--10,000 nm lateral footprint. These are macroscopic features at the carrier-diffusion-length scale, larger than visible-light wavelengths and many times the depth of a diffused emitter.

147. Ye's tunnel oxide, by contrast, is ultra-thin: Ye's claim 3 specifies 1.0--3.5 nm (Ye at claim 3; Ye at [0013]), and the '136 Patent specifies 0.8--2.0 nm (EX1001) at 8:43-46, claim 7). Tunneling physics dictates these thicknesses: the dielectric must be thin enough for adequate tunneling probability yet thick enough to maintain passivation and selectivity. The TOPCon literature converges on an optimum near 1.4--1.6 nm, with iVoc falling sharply on either side Choi, reporting 1.2--1.5 nm, at 1, 8.

148. A sub-2-nm dielectric cannot conformally cover a 1,000--8,000 nm topographic step without local thinning: deposited-film thickness varies with local angle, species flux, and precursor diffusion length. For a ~1.5 nm target, the permissible variation is a few Ångstroms before exiting the tunneling-optimum window. No realistic deposition process holds that tolerance over micrometer-tall sidewalls, corners, and re-entrant overlap geometries Yun expressly contemplates (Yun at [0010], [0029]).

149. Local thinning below the tunneling-optimum window produces two failure modes. First, thinned regions lose chemical passivation (fixed-charge and hydrogen), raising interface recombination. Second, where thinning reaches pinholes, doped polysilicon contacts the substrate directly, destroying selectivity. Choi describes exactly this: “[t]he locally reduced tunnel oxide introduces direct contact between the c-Si wafer substrate and n+ poly-Si, transporting both electrons and holes that deteriorates the carrier selectivity of the TOPCon passivating contact.” Choi at 8.

150. The architectural objectives point in opposite directions. Yun’s platforms reduce rear silicon-to-cell area to suppress recombination at metal-silicon contacts through dielectric openings. Yun at [0022]. Ye’s polished rear supports uniform sub-2 nm tunnel-oxide growth. Ye at [0030], [0038]; EX1001 at 7:62-8:18. The references are not solving the same problem.

151. A POSITA who understood TOPCon physics would have recognized that imposing Yun's micrometer platforms under Ye's nanometer tunnel oxide would not yield a functioning device. Each failure mode, local oxide thinning at edges and overlaps, pinhole-mediated polysilicon-on-silicon shorts, loss of uniformity-dependent passivation, degraded polysilicon conformality, is documented and follows from putting micrometer topography under a sub-2 nm dielectric.

152. Petitioner addresses none of these failure modes. The Petition analyzes no tunnel-oxide thickness budget over Yun's platforms, no polysilicon conformality, no TOPCon literature on uniformity-driven losses, and no mechanism by which the device retains TOPCon selectivity. The combination is treated as a parts-list, not a device-design exercise.

E. Reasonable Expectation of Success

153. Petitioner frames the combination as "known method, predictable results." That rubric does not apply where the geometric and chemical inputs are absent from the host. Yun's chemistry produces Yun's platforms on a bare (100) PERT wafer, without a tunnel oxide. Whether the same chemistry in Ye's TOPCon flow produces those platforms, and whether platforms under Ye's tunnel oxide yield a working device, is not answered by transferring chemistry across architectures.

154. “Known method, predictable results” applies when a step has been characterized on a similar substrate and downstream steps don’t depend on properties the substitution changes. Neither condition is met. Yun’s chemistry was characterized on bare (100) silicon for a diffused emitter, not for sub-2 nm tunnel oxide. Ye’s downstream tunnel-oxide growth depends on angstrom-scale morphology that Yun’s chemistry changes in unmeasured ways. Calling it “known” and “predictable” restates the conclusion.

155. The Petition supplies no analysis of how Yun’s TMAH/IPA etch (Yun at [0043], [0056]) would behave at Ye’s backside-polishing stage, after front boron diffusion, with borosilicate glass on the rear, with the wafer destined for thermal oxidation; no analysis of platform/tunnel-oxide interaction; no analysis of contact chemistry at Ye’s boron-P+ front (which Basu’s finding does not address).

156. A POSITA reading Ground 1A would not have expected the combination to function as TOPCon. The geometric mismatch is a barrier, not routine integration; the references address different problems; and the Petition supplies no thickness budget, conformality analysis, or contact-system specification.

157. Ground 1A does not establish that the claimed device was within routine engineering reach, and a POSITA would not have expected the Ye/Yun/Basu combination to succeed in producing a functional TOPCon cell of the type the ’136 Patent claims.

IX. ANALYSIS OF GROUND 6 (SAKAI)

A. Sakai's Architecture: A Back-Contact Heterojunction (Heterojunction-IBC) Cell

158. I have read Sakai (certified English translation). Sakai discloses a back-contact heterojunction (“HJ-IBC”) cell with four defining features.

159. First, the absorber is an n-type single-crystal silicon wafer (100--150 μm thick), anisotropically etched on both faces (Sakai at ¶ 28); the light-receiving face has a ~60 nm SiN antireflection film (Sakai at ¶ 39). Second, carrier-collecting junctions are on the rear only; no front emitter. Third, alternating n- and p-type a-Si:H stripes are formed on the rear side of the substrate on the surface of a 1-20 nm passivation film that covers the entire rear side of the substrate (Sakai at ¶¶ 32-33, 40-42). Fourth, each stripe is contacted by its own metal-on-TCO electrode (e.g., ITO/Ag), with protective dielectric in the gap (Sakai at ¶¶ 36-38, 53-55, 57-58, 65-68).

160. The defining step is shadow-mask patterning of the doped a-Si:H regions. N-type stripes are deposited through mask 30; mask 40 aligns to those via an alignment mark, then deposits p-type stripes. (Sakai at ¶¶ 125-142.) Sakai exists to solve n/p overlap when mask 40 is misregistered. (Sakai at ¶¶ 4-5.) Every other element, including rear texture, is calibrated to support that alignment.

161. The dispute over Ground 6 turns on what kind of cell Sakai is and what its rear texture does. Sakai is not a front-junction cell with a polysilicon-on-oxide

rear contact; it is a back-contact heterojunction cell with two laterally separated a-Si:H polarities and no blanket rear contact stack.

B. Sakai Is Not a TOPCon Cell

162. Petitioner and Dr. Schubert repeatedly characterize Sakai as a “TOPCon” cell. (*See, e.g.*, Schubert Decl. ¶¶ 75, 308, 348, 353 (EX1003); Pet. at 15, 70, 86.) That is technically incorrect. TOPCon and heterojunction-IBC are distinct carrier-selective contact architectures using different materials, patterning, and transport physics.

163. A TOPCon cell, as used in the field and in Petitioner’s textbook (Shah (ed.), *Solar Cells and Modules*, Springer (2020) (“Shah”), at § 5.5.2 (EX1015)), collects selectively the substrate majority carriers vertically through a blanket rear stack comprising of an ultrathin (~1--2 nm) tunnel SiO_x that covers the entire rear side of the substrate and a continuous doped poly-Si (doped same type as the substrate) on top of the tunnel oxide, the carriers are then collected by a continuous metal grid. Both the tunnel SiO_x and the doped poly-Si layers are blanket; neither the doped poly-Si nor the metal is patterned into opposite-polarity stripes. In general, the operation of the TOPCon cell relies on the difference between the tunnelling of the electrons and holes through the tunnel oxide in order to ensure that most of the carriers that tunnel and collected by the metal electrodes are the substrate majority carriers; typically, such carriers are the electrons.

164. A heterojunction-IBC cell (Shah (ed.), Solar Cells and Modules, Springer (2020) (“Shah”), at § 5.5.3 and Ch. 7 (EX1015)) works differently. Collection is lateral: n-type stripes collect electrons, p-type stripes collect holes, on an interdigitated comb. There is no blanket tunnel oxide; current flows laterally to the nearest correct-polarity stripe, tunneling through a thin passivation film into the a-Si:H above.

165. Sakai has no polysilicon contact in the TOPCon sense. Its emitter and BSF layers are a-Si:H (or alloys), not polysilicon (Sakai at ¶¶ 43-44); its passivation film is a heterojunction interface, not a polysilicon-on-oxide contact. There is no blanket doped layer on the rear; just alternating oppositely-doped a-Si:H regions forming stripes that are separated by a gap. (Sakai at ¶¶ 32-33, 54-55.) Even though in some embodiments, Sakai discloses a thin insulating layer as the passivation layer 3 between the substrate and the n- and p- doped amorphous silicon regions elements 4 and 5 respectively, Sakai requires that this passivation layer “allows carriers (electrons and holes) to tunnel.” (Sakai at ¶¶ 38-41, 42.) In view of Sakai’s disclosures a POSITA would understand that the purpose of Sakai’s passivation layer 3 is to passivate the surface of the substrate and thus reduce carrier recombination, particularly in the gaps between the doped n- and p- amorphous silicon regions. Sakai does not disclose that this layer selectively allows only one type of carrier to tunnel as it is the case in a TOPCon structure.

166. The misidentification supplies the architectural premise for Petitioner’s mapping of claim 1’s tunnel-oxide / doped-conductive-layer rear stack onto Sakai. There is no such stack. Sakai describes a “back surface heterojunction solar cell” (Sakai at ¶ 172) and contrasts the “conventional heterojunction” in which the doped a-Si layer and TCO are “formed on substantially the entire surface” (Sakai at ¶ 171). Sakai is squarely in the heterojunction-IBC class.

C. Sakai’s Rear Texture is Described as Pyramid Shaped

167. Claim 1[b] requires “a non-pyramid-shaped microstructure” on the rear. Sakai describes the opposite. The passage Petitioner relies upon, ¶ 45, reads in full: “A specific example of the texture is a pyramid-shaped (quadrangular pyramid-shaped or truncated quadrangular pyramid-shaped) uneven structure obtained by performing anisotropic etching on an n-type single crystal silicon substrate whose main surface is a (100) surface.” (Sakai at ¶ 45.) Sakai describes this shape as a pyramid.

168. The subject is “a specific example of the texture”; the predicate is “pyramid-shaped ... uneven structure.” The parenthetical lists complete and truncated quadrangular pyramid as subspecies of “pyramid-shaped.” The next sentence confirms: “the actual texture has pyramid-shaped unevenness of various sizes and shapes formed in plurality.” (*Id.*) Sakai’s pyramid is described as a genus; quadrangular and truncated quadrangular are species.

169. The USPTO Examiner reached the same conclusion twice on the same disclosure. In '136 prosecution, the Examiner described Sakai's rear textures as "pyramid form and truncated four-sided pyramidal rugged structure" and identified missing limitations. ('136 Patent File History, at 15-16 (EX1018).) In continuation application 18/888,868, the same Examiner repeated that characterization and stated "[Sakai] does not clearly show non-pyramid-shaped microstructures." (Non-Final Office Action mailed Aug. 19, 2025 in U.S. App. No. 18/888,868, at 5 (EX2001).)

D. Sakai Cannot Supply Both 1[b] (Non-Pyramid Rear) and 1[c] (Pyramid Front) From the Same Disclosure

170. Claim 1 requires two different microstructures on the same wafer: non-pyramid rear (1[b]) and pyramid front (1[c]). A single reference must describe a cell whose two faces carry different morphologies. Sakai does not.

171. Sakai applies a single anisotropic etch to both surfaces. Sakai at ¶ 28: "texture structure formed on both surfaces of the substrate." Sakai at ¶ 121: "Both surfaces ... are thus anisotropically etched to form a texture structure where the size of the texture is 15 μm or less." A single bath, KOH (1--5 wt%) + IPA (1-10 wt%), 60-80°C, 10-30 min, both faces same etchant, same duration, same morphology.

172. Paragraph 45, which Petitioner cites for both rear and front, describes that one common morphology. It does not partition the morphology between front and rear. It does not say "the rear is truncated" and "the front is non-truncated," and

no other Sakai passage makes that assignment. Petitioner's mapping reads a single sentence, one both producing one family of pyramids, as two different morphologies on two faces. That is relabeling, not reading.

173. Sakai's figures confirm symmetry. In Figs. 1B, 6-10, 14, and 17-21, front and rear are drawn with the same triangular profile of comparable size. No figure depicts a pyramid on one face and a stepped, polygonal-topped non-pyramid on the other.

174. Even if ¶ 45 could be parsed as "truncated quadrangular pyramid" on the rear, it would still need to supply "quadrangular pyramid" on the front for 1[c]. A single sentence describing one etch on both faces cannot disclose two morphologies.

175. Sakai discloses one texture morphology applied symmetrically to both faces by a single etch. Sakai does not disclose the asymmetric architecture of claim 1.

E. Petitioner's Textbook Reinforces This Reading

176. Petitioner's textbook (Shah (ed.), Solar Cells and Modules, Springer (2020) ("Shah") (EX1015)) treats TOPCon and heterojunction-IBC as distinct device classes in separate sections (§§ 5.5.2 and 5.5.3, IBC also Ch. 7). It supplies no basis to recharacterize Sakai's a-Si:H interdigitated rear contact as TOPCon, or its symmetric pyramidal texture as non-pyramid.

X. ANALYSIS OF GROUND 6A (SAKAI + YUN)

A. Overview of the Combination

177. Ground 6A adds Yun (Yun) to supply 1[b]'s partial-stacking and polygonal-top features. The combination does not address the asymmetric-texture problem (Section IX.D): even with Yun's platforms on the rear, the front must still be pyramid under 1[c], and Sakai's single-bath etch produces only one morphology on both faces.

178. Even setting that defect aside, a POSITA designing a back-contact heterojunction cell would not have made the combination. Sakai's rear texture has a specific functional purpose that Yun's platform geometry would defeat.

B. Sakai's Rear Texture Exists to Enable Shadow-Mask Alignment

179. The rear is patterned in two sequential shadow-mask steps: mask 30 deposits n-type stripes plus alignment mark; mask 40 aligns to that mark and deposits p-type stripes. Misregistration causes n/p overlap, the failure Sakai exists to fix. (Sakai at ¶¶ 4-5.) Alignment is performed under an optical microscope through openings in the second mask. (Sakai at ¶¶ 135, 160.)

180. For alignment to work, the rear-face reflectance must be substantially uniform. Non-uniform reflected light (bright facets at random orientations) prevents reliable mark distinction. Sakai addresses this by keeping the rear texture small enough that reflectance averages to a uniform field. (Sakai at ¶¶ 10, 160, 162.)

181. Sakai is quantitative. Sakai at ¶ 167 reports that at “15 μm or larger,” “the boundary portion of the alignment mark is difficult to recognize.” Sakai at ¶ 162: “as the texture size increases, the amount of film entered into the back surface of the shadow mask increases.” Sakai gives 1 μm as an easy-recognition example (Sakai at ¶ 163, Fig. 12(c)); embodiments stay below 15 μm .

182. The rear texture in Sakai is not a free design parameter; it is a calibrated input to the shadow-mask alignment process. Both its size and uniformity are set by the alignment-mark recognition requirement.

C. Yun’s Platform Dimensions Would Defeat Sakai’s Alignment Function

183. Yun’s rear is a “platform-shaped textured surface”: “the side length of the upper plane is 2 to 10 μm , and the height of the platform structure is 1 to 8 μm .” (Yun at claim 1; see also Yun at ¶ 7.) The four embodiments report 2/1 μm (Embod 1, Yun at ¶ 30); 10/8 μm (Embod 2, Yun at ¶ 32); 4/3 μm (Embod 3, Yun at ¶ 34); 7/6 μm (Embod 4, Yun at ¶ 36).

184. Two observations follow if Yun’s platforms are installed on Sakai’s rear.

185. First, upper-plane side length is only part of the relevant dimension. The lower plane is “larger than” the upper (Yun at claim 1); adjacent platforms can be “partially overlapping” or “partially connected” (Yun at ¶¶ 10, 30, 36). The microscope footprint is the lower-plane size, which exceeds 2--10 μm ; as upper side

length approaches 10 μm with overlap, the footprint pushes into Sakai's 15 μm failure threshold.

186. Second, Yun's 1-8 μm relief with steep facets produces specular reflections, exactly the "non-uniform reflected light" Sakai's small-texture rule suppresses. A 7--8 μm platform with 10 μm footprint is in the geometric-optics regime where individual facets act as specular reflectors. Sakai's rear is small enough that individual facets do not produce distinguishable reflectance. Grafting Yun's platforms replaces a reflectance-averaging texture with one engineered for the opposite purpose (bifacial light trapping).

187. A POSITA would not import Yun's platform morphology onto Sakai's rear because doing so would compromise the alignment-mark recognition that Sakai's two-mask patterning depends on. The very rationale Sakai gives for its rear texture is what Yun's morphology defeats.

D. Method vs. Morphology, A POSITA Would Adjust Sakai's Own Process, Not Import Yun's Geometry

188. Petitioner conflates etch method with resulting morphology. Sakai already teaches alkaline texturing (NaOH/KOH + IPA inhibitor, 60--80°C, 10--30 min) and how to control texture size by varying solution temperature, processing time, inhibitor type, etching rate, and substrate so that "the size of the texture is 15 μm or less." (Sakai at ¶¶ 116, 119-121.) Sakai also identifies lignin and bicarbonate additives that produce fine ($\leq 1 \mu\text{m}$) pyramids. (Sakai at ¶¶ 116, 119-121.)

189. Yun's chemistry (NaOH/KOH/TMAH/HF-HNO₃ with IPA or ethylene glycol, 60--80°C, 10--900 s; Yun at claim 5) adds no capability Sakai lacks. Both draw from the standard alkaline/acidic texturing repertoire. What differentiates Yun is morphology, not chemistry, flat upper plane on a wider lower plane, in dispersed, overlapping, or connected distributions.

190. A POSITA fine-tuning Sakai's rear texture would adjust Sakai's etch parameters, not import a morphology from a different architecture. And tuning would target Sakai's sub-15 µm alignment threshold (1 µm preferred), not Yun's 2--10 µm platforms with 1--8 µm relief, the wrong direction.

191. Petitioner's mapping demands Yun's platform geometry, polygonal upper planes, partial overlap, 2-10 µm side length, 1-8 µm height. A "same chemistry as Sakai" rationale carries only the etchant choice, not the geometry. The morphological piece, what 1[b] recites, is unsupported.

E. Architectural Mismatch Between Sakai and Yun

192. Sakai and Yun solve different problems with different rear-side architectures.

193. Sakai's rear is the active carrier-collecting face of a back-contact heterojunction cell, covered by a-Si:H/TCO/metal stacks with dielectric in the gaps. (Sakai at ¶¶ 4-6, 33, 36-37, 53-55.) It is operationally opaque; its texture exists for in-process optical recognition, not light management.

194. Yun’s rear is that of a bifacial PERT cell with diffused BSF, exposed to ambient and ground-reflected light. (Yun at claim 1, ¶¶ 3, 22.) Its platform morphology serves two purposes unrelated to alignment: reducing rear-surface area to suppress recombination (Yun at ¶¶ 4, 22), and increasing internal reflectance of long-wavelength light (Yun at ¶ 22).

195. Yun’s rationale has no purchase on Sakai. Sakai’s rear is covered by a-Si:H/TCO/metal, not exposed for bifacial capture. Rear recombination is handled by a-Si:H/c-Si heterojunction passivation. Internal long-wave reflectance is supplied by Sakai’s rear electrodes, which reflect “90% or more” of long-wavelength light (Sakai at ¶ 56). Yun’s morphology buys Sakai nothing functionally and costs it the alignment scheme.

196. A POSITA in 2019-2020 designing a back-contact heterojunction cell would not select a rear morphology engineered for a bifacial diffused-BSF cell. Yun’s platforms optimize a free, optically exposed rear; Sakai’s rear is neither.

F. No Reasonable Expectation of Success

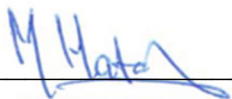
197. Petitioner offers a conclusory “known method / predictable results” rationale. (Pet. at 86.) It does not analyze the alignment-mark constraint (Section X.B), the architectural-cover difference (Section X.E), or the method-vs-morphology distinction (Section X.D).

198. A POSITA would not have expected Sakai+Yun to function. First, the second shadow-mask deposition would fail because alignment-mark recognition would degrade (Sakai's 15 μm threshold). Second, a-Si:H pattern fidelity would degrade because larger rear texture allows more film entry behind the mask, degrading n/p separation (Sakai at ¶ 162). Third, Yun's rationale (bifacial absorption, recombination reduction) does not exist in Sakai's architecture; the substitution buys nothing operationally to offset its manufacturing cost.

199. The combination would graft a bifacial-PERT rear morphology onto the shadow-mask-aligned, electrode-covered rear of a heterojunction-IBC cell, with a high likelihood of compromising the patterning step the cell depends on. A POSITA would not have expected it to function.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that this declaration was executed on the date set forth below.

Date: May 26, 2026



Dr. Miltiadis Hatalis