

Etron 鈺創科技
Etron Technology, Inc.

No.6 Technology Road 5,
Hsinchu Science Park,
Hsinchu, Taiwan 30078, R.O.C.
Tel: 886-3-578-2345
Fax: 886-3-563-2397

Maintenance Fee Branch
USPTO
FAX: 571-273-6500

Re: Entity Status Change Request

Dear Sir:

The patentee would like to **change to regular undiscounted entity status** for Patent No. 9,164,942 having application No. 13/649,131.

The patentee noticed that the automatically calculated amount for the above-mentioned patent is incorrect when attempting to pay the maintenance fee online, since the current entity status on the USPTO record for this patent is still small entity, rather than regular undiscounted entity. As such, the patentee respectfully requests the entity status change, for Patent No. 9,164,942 having application No. 13/649,131, to regular undiscounted entity status, and after that the maintenance fee could be paid online.

Best Regards,
Tony Wang


Legal and IP department
Etron Technology Inc.

2 / 8

#02- ET2011.022US



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/649,131	10/20/2015	9164942	ETRP0133USA	1078

27765

7590

09/30/2015

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 624 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Weng-Dah Ken, Hsinchu City, TAIWAN;
Nicky Lu, Taipei City, TAIWAN;
ETRON TECHNOLOGY, INC., Hsinchu, TAIWAN

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/649,131	10/11/2012	Weng-Dah Ken	ETRP0133USA	1078
27765 7590 09/14/2015 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER BYRNE, HARRY W	
			ART UNIT 2824	PAPER NUMBER
			NOTIFICATION DATE 09/14/2015	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Supplemental Notice of Allowability	Application No. 13/649,131	Applicant(s) KEN ET AL.	
	Examiner HARRY W. BYRNE	Art Unit 2824	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Application filed 10/11/2012.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-31. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☐ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/HARRY W BYRNE/
Primary Examiner, Art Unit 2824

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 08/18/2015

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Eve Hsieh	(Depositor's name)
/Eve Hsieh/	(Signature)
09/10/2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/649,131	10/11/2012	Weng-Dah Ken	ETRP0133USA	1078

TITLE OF INVENTION:

HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	Yes	\$480	\$0	\$0	\$480	11/18/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BYRNE, HARRY W	2824	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Winston Hsu

2 Scott Margo

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Etron Technology, Inc.

No. 6, Technology Road 5, Hsinchu, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3105 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Winston Hsu/

Date 09/09/2015

Typed or printed name Winston Hsu

Registration No. 41,526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		13649131		
Filing Date:		11-Oct-2012		
Title of Invention:		HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE		
First Named Inventor/Applicant Name:		Weng-Dah Ken		
Filer:		Winston Hsu/Eve Hsieh		
Attorney Docket Number:		ETRP0133USA		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				480

Electronic Acknowledgement Receipt

EFS ID:	23435055
Application Number:	13649131
International Application Number:	
Confirmation Number:	1078
Title of Invention:	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE
First Named Inventor/Applicant Name:	Weng-Dah Ken
Customer Number:	27765
Filer:	Winston Hsu/Eve Hsieh
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	ETRP0133USA
Receipt Date:	10-SEP-2015
Filing Date:	11-OCT-2012
Time Stamp:	02:18:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$480
RAM confirmation Number	10822
Deposit Account	503105
Authorized User	HSU, WINSTON

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	ETRP0133USA0_AN_1_NP072.pdf	238886 39b8fb26f56d1d86ed055be4bad4a8619e877a66	no	1

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30721 8a76991f07537d944ed7c1ef7498703d060eac6e	no	2
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Warnings:

Information:

Total Files Size (in bytes):			269607
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 08/18/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

BYRNE, HARRY W

ART UNIT

PAPER NUMBER

2824

DATE MAILED: 08/18/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/649,131	10/11/2012	Weng-Dah Ken	ETRP0133USA	1078

TITLE OF INVENTION: HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	11/18/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

27765 7590 08/18/2015

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/649,131	10/11/2012	Weng-Dah Ken	ETRP0133USA	1078

TITLE OF INVENTION: HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	11/18/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BYRNE, HARRY W	2824	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/649,131	10/11/2012	Weng-Dah Ken	ETRP0133USA	1078
27765 7590 08/18/2015 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER BYRNE, HARRY W	
			ART UNIT	PAPER NUMBER
			2824	

DATE MAILED: 08/18/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/649,131	Applicant(s) KEN ET AL.	
	Examiner HARRY W. BYRNE	Art Unit 2824	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Application filed 10/11/2012.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-25. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/HARRY W BYRNE/
Primary Examiner, Art Unit 2824

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. This action is responsive to an **Application** filed 10/11/2012. Claims 1-31 are pending. This **Application** claims benefit of 61/555,468 filed 11/03/2011 and is a CIP of 13/649,131 filed 10/11/2012 which claims benefit of 61/546,039 filed 10/11/2011.

ALLOWABLE SUBJECT MATTER

3. **Claims 1 – 31 are allowed.**

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance:

With respect to **independent claims 1** (and claims 2–18 which further depend), **claim 19** (and claims 20–31 which further depend), there is no teaching, suggestion, or motivation for combination in the prior art to a high speed memory including where the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus.

The prior art made of record and considered pertinent to applicant's disclosure: U.S. PG Pub US 2007/0005831 A1 to *Gregorius*.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be labeled "Comments on Statement of Reasons for Allowance."
6. When responding to this office action, applicants are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner.

Conclusion

7. A shortened statutory period for response to this action is set to expire **three months and zero days** from the mailing date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HARRY W. BYRNE whose telephone number is (571) 270-3308. The examiner can normally be reached on M-F 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

	/Harry W. Byrne/ Primary Examiner, Art Unit 2824
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Notice of References Cited	Application/Control No. 13/649,131	Applicant(s)/Patent Under Reexamination KEN ET AL.	
	Examiner HARRY W. BYRNE	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0246801 A1	12-2004	Lee et al.	365/221
*	B	US-2004/0260864 A1	12-2004	Lee et al.	711/101
*	C	US-7,013,359 B1	03-2006	Li, Gabriel	710/305
*	D	US-2007/0005831 A1	01-2007	Gregorius, Peter	710/052
*	E	US-7,206,876 B2	04-2007	Jang, Seong-jin	710/66
*	F	US-7,546,497 B2	06-2009	Jang, Seong-Jin	714/718
*	G	US-7,680,966 B1	03-2010	Falik et al.	710/45
*	H	US-2010/0235554 A1	09-2010	Chang et al.	710/104
*	I	US-7,810,017 B2	10-2010	Radke, William H.	714/769
*	J	US-7,903,685 B2	03-2011	Eshraghian, Hamed	370/466
*	K	US-8,036,052 B2	10-2011	Lee et al.	365/201
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 1078

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
13/649,131	10/11/2012	365	2824	ETRP0133USA		
APPLICANTS ETRON TECHNOLOGY, INC., Hsinchu, TAIWAN INVENTORS Weng-Dah Ken, Hsinchu City, TAIWAN; Nicky Lu, Taipei City, TAIWAN; ** CONTINUING DATA ***** This appln claims benefit of 61/546,039 10/11/2011 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED *** SMALL ENTITY ** 10/25/2012						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/HARRY W BYRNE/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 13	TOTAL CLAIMS 31	INDEPENDENT CLAIMS 2
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE						
FILING FEE RECEIVED 874	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13649131
Filing Date	2012-10-11
First Named Inventor	Weng-Dah Ken
Art Unit	2824
Examiner Name	ELMS, RICHARD T
Attorney Docket Number	ETRP0133USA

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8036052	B2	2011-10-11	Lee	
	2	8473653	B2	2013-06-25	Kondo	
	3	7680966	B1	2010-03-16	Falik	
	4	7903685	B2	2011-03-08	Eshraghian	
	5	7206876	B2	2007-04-17	Jang	
	6	7013359	B1	2006-03-14	Li	
	7	7810017	B2	2010-10-05	Radke	
	8	8803545	B2	2014-08-12	Yoko	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.B./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13649131
	Filing Date	2012-10-11
	First Named Inventor	Weng-Dah Ken
	Art Unit	2824
	Examiner Name	ELMS, RICHARD T
	Attorney Docket Number	ETRP0133USA

	9	7546497	B2	2009-06-09	Jang	
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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040246801	A1	2004-12-09	Lee	
	2	20040260864	A1	2004-12-23	Lee	
	3	20100235554	A1	2010-09-16	Chang	
	4	20070005831	A1	2007-01-04	Gregorius	

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1						

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.B./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13649131
	Filing Date	2012-10-11
	First Named Inventor	Weng-Dah Ken
	Art Unit	2824
	Examiner Name	ELMS, RICHARD T
	Attorney Docket Number	ETRP0133USA

	1		
EXAMINER SIGNATURE			
Examiner Signature	/Harry Byrne/ (08/02/2015)		Date Considered
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.B./

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Weng-Dah Ken
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	ETRP0133USA

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7385281		2008-06-10	Nishio	
	2	7245239		2007-07-17	Wallner	
	3	6317377		2001-11-13	Kobayashi	

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090024790		2009-01-22	Rajan	
	2	20090039492		2009-02-12	KANG	

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.B./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Weng-Dah Ken
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	ETRP0133USA

	1							
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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.
	1	

EXAMINER SIGNATURE

Examiner Signature	/Harry Byrne/ (08/02/2015)	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

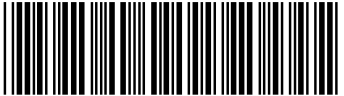
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.B./

Issue Classification 	Application/Control No. 13649131	Applicant(s)/Patent Under Reexamination KEN ET AL.	
	Examiner HARRY W BYRNE	Art Unit 2824	

CPC					
Symbol				Type	Version
G06F	13	/	40	F	2013-01-01
G11C	7	/	10	I	2013-01-01
H01L	2224	/	16145	A	2013-01-01
H01L	2224	/	16225	A	2013-01-01
H01L	2224	/	48227	A	2013-01-01
H01L	2225	/	0651	A	2013-01-01
H01L	2924	/	1431	A	2013-01-01
H01L	2924	/	1434	A	2013-01-01
H01L	2924	/	15311	A	2013-01-01
H01L	2225	/	06513	A	2013-01-01
H01L	2225	/	06541	A	2013-01-01
H01L	2225	/	06568	A	2013-01-01
H01L	2924	/	13091	A	2013-01-01
H01L	2224	/	32225	A	2013-01-01
H01L	2224	/	73265	A	2013-01-01
H01L	2924	/	3025	A	2013-01-01

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
H01L		2224	/	73265	A	1	1	2013-01-01
H01L		2224	/	32225	A	1	2	2013-01-01
H01L		2224	/	48227	A	1	3	2013-01-01
H01L		2924	/	00012	A	1	4	2013-01-01
H01L		2924	/	15311	A	2	1	2013-01-01
H01L		2224	/	73265	A	2	2	2013-01-01
H01L		2224	/	32225	A	2	3	2013-01-01
H01L		2224	/	48227	A	2	4	2013-01-01
H01L		2924	/	00	A	2	5	2013-01-01
H01L		2924	/	3025	A	3	1	2013-01-01
H01L		2924	/	00	A	3	2	2013-01-01

NONE		Total Claims Allowed: 31	
(Assistant Examiner)	(Date)		
/HARRY W BYRNE/ Primary Examiner. Art Unit 2824	08/03/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5 & 10

Issue Classification 	Application/Control No. 13649131	Applicant(s)/Patent Under Reexamination KEN ET AL.	
	Examiner HARRY W BYRNE	Art Unit 2824	

NONE (Assistant Examiner) (Date)		Total Claims Allowed: 31	
/HARRY W BYRNE/ Primary Examiner.Art Unit 2824 (Primary Examiner) (Date)		08/03/2015 O.G. Print Claim(s) 1	O.G. Print Figure 5 & 10

Issue Classification 	Application/Control No. 13649131	Applicant(s)/Patent Under Reexamination KEN ET AL.
	Examiner HARRY W BYRNE	Art Unit 2824

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION										
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED					
365			63			G	1	1	C	5 / 06 (2006.0)						
CROSS REFERENCE(S)																
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)															

NONE (Assistant Examiner) (Date)		Total Claims Allowed: 31	
/HARRY W BYRNE/ Primary Examiner. Art Unit 2824 (Primary Examiner) (Date)		08/03/2015 O.G. Print Claim(s) 1	O.G. Print Figure 5 & 10

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1	(memory WITH (IC OR (integrated ADJ circuit) OR chip OR module)) AND (memory WITH array) AND (("input/output" OR "I/O") WITH data WITH bus) AND (first WITH ((metal\$1oxide\$1semiconductor WITH field\$1effect WITH transistor) OR MOSFET)) AND (first WITH MOSFET WITH gate WITH length) AND (logic WITH unit) AND (first WITH transmission WITH bus) AND (first WITH parallel WITH data) AND (bus WITH width) AND (second WITH MOSFET WITH gate WITH length)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/02 23:25
L4	72	("7206876" "7680966" "20100235554" "20040260864" "7546497" "8473653" "20090039492" "6317377" "7245239" "7385281" "20040246801" "20070005831" "7013359" "20090024790" "7810017" "8036052" "8803545" "7903685").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/02 23:25
L5	6	((Weng-Dah) near2 (Ken)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/02 23:25
L6	27	((Nicky) near2 (Lu)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/02 23:25
L7	2	I5 and I6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/02 23:26
L10	12125	(365/63,185.05,185.06,185.11,214).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L11	8719	sandisk.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L12	497	L10 AND L11	US-PGPUB;	OR	OFF	2015/08/02

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			23:40
L13	269	((bit or column) adj line) or bit\$line\$1 or column\$1line) with different with (layer or level) with adjacent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L14	8	L13 and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L15	1540	((bit adj line) or (bit\$1line) adj pair) with (first adj (level or layer)) and (second adj (level or layer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L16	1506	L15 AND Memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L17	141	L15 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L18	71	L17 and "NAND"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L19	2	L18 and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L20	5015	(365/185.17).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2015/08/02 23:40

			IBM_TDB			
L21	8841	(365/185.18).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L22	2094	(365/185.25).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L23	3520	(365/185.33).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L24	40581	"NAND Flash"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L25	15892	L20 OR L21 OR L22 OR L23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L26	5355	L24 AND L25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L27	20	("20040051133" "20040208037" "5317535" "5337281" "6084820" "6377504" "6947324").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L28	24	("20050265079" "20060023497" "5659505" "5677875" "6191445" "6327182" "6477089" "6872614" "6873561" "6996024").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L29	377	L20 AND L22	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2015/08/02 23:40

			EPO; JPO; DERWENT; IBM_TDB			
L30	6500	(365/203).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L31	404	(L22 OR L30) AND L20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L32	1973	(pre\$charg\$3 WITH (source ADJ line))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/02 23:40
L33	75	L31 AND L32	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L34	40	L33 and potential	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L35	40	L34 and second	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L36	40	L35 and first	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L37	38	L36 and third	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L38	55	L32 and "third potential"	US-PGPUB; USPAT;	OR	OFF	2015/08/02 23:40

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L39	25	L38 and Flash	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L40	75	("6011287").PN. OR ("6859394").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/02 23:40
L41	3548	L11 AND NAND	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L42	35	L41 AND L32	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L43	786	(Aritome with Seichi).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L44	302	(Goda with Akira).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L45	49	L43 AND L44	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L46	44	L45 AND "NAND"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L47	905	L11 AND pre\$charg\$3	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2015/08/02 23:40

			EPO; JPO; DERWENT; IBM_TDB			
L48	775	L47 AND NAND	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L49	39	L48 AND (pre\$charg\$3 WITH ((source ADJ line) OR (common ADJ source) OR ("C-source")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L50	751	L48 AND READ	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L51	752	L48 AND READ\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L52	613	L51 AND ((select\$3 OR target\$3) WITH ("SL" OR (source ADJ Line) OR (common ADJ source) OR ("C-source")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L53	293	L52 AND ((unselect\$3 OR target\$3) WITH ("SL" OR (source ADJ Line) OR (common ADJ source) OR ("C-source")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L54	4	("5570315").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L55	0	L54 AND ("source line" NEAR float\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L56	1	L54 AND ("source line" SAME float\$3)	US-PGPUB; USPAT;	OR	OFF	2015/08/02 23:40

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L57	786	(Seiichi with Aritome).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L58	514	L57 AND "NAND"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L59	124	L58 AND (alternate or interposing)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L60	25	L58 AND ((alternate or interposing) with ((bit adj line\$1) OR (bit\$1line\$1)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L61	22	2004/0051133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L62	35	("20010005620" "20020100930" "20020190306" "20040051133" "4939690" "5432106" "5638327" "5712814" "5770502" "5783457" "5830788" "5837584" "5891774" "5896314" "5963808" "6008094" "6030869" "6066531" "6101128" "6130134" "6265292" "6300656" "6320236" "6384457" "6534787" "6620682" "6632686" "6689658" "6703659" "6724035" "6744668").PN. OR ("7294882").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/02 23:40
L63	4	"20040051133"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(memory WITH (IC OR (integrated ADJ circuit) OR chip OR module)) AND (memory WITH array) AND (("input/output" OR "I/O") WITH data WITH bus) AND (first WITH ((metal\$1oxide\$1semiconductor WITH field\$1effect WITH transistor) OR MOSFET)) AND (first WITH MOSFET WITH gate WITH length) AND (logic WITH unit) AND (first WITH transmission WITH bus) AND (first WITH parallel WITH data) AND (bus WITH width) AND (second WITH MOSFET WITH gate WITH length)	US-PGPUB; USPAT; UPAD	OR	ON	2015/08/02 23:25
L3	18	("7206876" "7680966" "20100235554" "20040260864" "7546497" "8473653" "20090039492" "6317377" "7245239" "7385281" "20040246801" "20070005831" "7013359" "20090024790" "7810017" "8036052" "8803545" "7903685").PN.	US-PGPUB; USPAT; UPAD	OR	ON	2015/08/02 23:25
L8	18	("7206876" "7680966" "20100235554" "20040260864" "7546497" "8473653" "20090039492" "6317377" "7245239" "7385281" "20040246801" "20070005831" "7013359" "20090024790" "7810017" "8036052" "8803545" "7903685").PN.	US-PGPUB; USPAT; UPAD	OR	ON	2015/08/02 23:27
L9	13	("20040246801" "20040260864" "20070005831" "20100235554" "7013359" "7206876" "7546497" "7680966" "7810017" "7903685" "8036052" "8473653" "8803545").PN.	US-PGPUB; USPAT; UPAD	OR	ON	2015/08/02 23:28

8/ 2/ 2015 11:45:34 PM

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1	(memory WITH (IC OR (integrated ADJ circuit) OR chip OR module)) AND (memory WITH array) AND (("input/output" OR "I/O") WITH data WITH bus) AND (first WITH ((metal\$1oxide\$1semiconductor WITH field\$1effect WITH transistor) OR MOSFET)) AND (first WITH MOSFET WITH gate WITH length) AND (logic WITH unit) AND (first WITH transmission WITH bus) AND (first WITH parallel WITH data) AND (bus WITH width) AND (second WITH MOSFET WITH gate WITH length)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/02 23:25
L4	72	("7206876" "7680966" "20100235554" "20040260864" "7546497" "8473653" "20090039492" "6317377" "7245239" "7385281" "20040246801" "20070005831" "7013359" "20090024790" "7810017" "8036052" "8803545" "7903685").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/02 23:25
L5	6	((Weng-Dah) near2 (Ken)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/02 23:25
L6	27	((Nicky) near2 (Lu)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/02 23:25
L7	2	I5 and I6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/02 23:26
L10	12125	(365/63,185.05,185.06,185.11,214).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L11	8719	sandisk.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L12	497	L10 AND L11	US-PGPUB;	OR	OFF	2015/08/02

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			23:40
L13	269	((bit or column) adj line) or bit\$line\$1 or column\$1line) with different with (layer or level) with adjacent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L14	8	L13 and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L15	1540	((bit adj line) or (bit\$1line) adj pair) with (first adj (level or layer)) and (second adj (level or layer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L16	1506	L15 AND Memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L17	141	L15 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L18	71	L17 and "NAND"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L19	2	L18 and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L20	5015	(365/185.17).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2015/08/02 23:40

			IBM_TDB			
L21	8841	(365/185.18).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L22	2094	(365/185.25).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L23	3520	(365/185.33).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L24	40581	"NAND Flash"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L25	15892	L20 OR L21 OR L22 OR L23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L26	5355	L24 AND L25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L27	20	("20040051133" "20040208037" "5317535" "5337281" "6084820" "6377504" "6947324").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L28	24	("20050265079" "20060023497" "5659505" "5677875" "6191445" "6327182" "6477089" "6872614" "6873561" "6996024").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L29	377	L20 AND L22	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2015/08/02 23:40

			EPO; JPO; DERWENT; IBM_TDB			
L30	6500	(365/203).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L31	404	(L22 OR L30) AND L20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L32	1973	(pre\$charg\$3 WITH (source ADJ line))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/02 23:40
L33	75	L31 AND L32	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L34	40	L33 and potential	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L35	40	L34 and second	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L36	40	L35 and first	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L37	38	L36 and third	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L38	55	L32 and "third potential"	US-PGPUB; USPAT;	OR	OFF	2015/08/02 23:40

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L39	25	L38 and Flash	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L40	75	("6011287").PN. OR ("6859394").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/02 23:40
L41	3548	L11 AND NAND	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L42	35	L41 AND L32	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L43	786	(Aritome with Seichi).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L44	302	(Goda with Akira).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L45	49	L43 AND L44	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L46	44	L45 AND "NAND"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L47	905	L11 AND pre\$charg\$3	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2015/08/02 23:40

			EPO; JPO; DERWENT; IBM_TDB			
L48	775	L47 AND NAND	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L49	39	L48 AND (pre\$charg\$3 WITH ((source ADJ line) OR (common ADJ source) OR ("C-source")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L50	751	L48 AND READ	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L51	752	L48 AND READ\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L52	613	L51 AND ((select\$3 OR target\$3) WITH ("SL" OR (source ADJ Line) OR (common ADJ source) OR ("C-source")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L53	293	L52 AND ((unselect\$3 OR target\$3) WITH ("SL" OR (source ADJ Line) OR (common ADJ source) OR ("C-source")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L54	4	("5570315").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L55	0	L54 AND ("source line" NEAR float\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L56	1	L54 AND ("source line" SAME float\$3)	US-PGPUB; USPAT;	OR	OFF	2015/08/02 23:40

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L57	786	(Seiichi with Aritome).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L58	514	L57 AND "NAND"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L59	124	L58 AND (alternate or interposing)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L60	25	L58 AND ((alternate or interposing) with ((bit adj line\$1) OR (bit\$1line\$1)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L61	22	2004/0051133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40
L62	35	("20010005620" "20020100930" "20020190306" "20040051133" "4939690" "5432106" "5638327" "5712814" "5770502" "5783457" "5830788" "5837584" "5891774" "5896314" "5963808" "6008094" "6030869" "6066531" "6101128" "6130134" "6265292" "6300656" "6320236" "6384457" "6534787" "6620682" "6632686" "6689658" "6703659" "6724035" "6744668").PN. OR ("7294882").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/02 23:40
L63	4	"20040051133"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/08/02 23:40

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(memory WITH (IC OR (integrated ADJ circuit) OR chip OR module)) AND (memory WITH array) AND (("input/output" OR "I/O") WITH data WITH bus) AND (first WITH ((metal\$1oxide\$1semiconductor WITH field\$1effect WITH transistor) OR MOSFET)) AND (first WITH MOSFET WITH gate WITH length) AND (logic WITH unit) AND (first WITH transmission WITH bus) AND (first WITH parallel WITH data) AND (bus WITH width) AND (second WITH MOSFET WITH gate WITH length)	US-PGPUB; USPAT; UPAD	OR	ON	2015/08/02 23:25
L3	18	("7206876" "7680966" "20100235554" "20040260864" "7546497" "8473653" "20090039492" "6317377" "7245239" "7385281" "20040246801" "20070005831" "7013359" "20090024790" "7810017" "8036052" "8803545" "7903685").PN.	US-PGPUB; USPAT; UPAD	OR	ON	2015/08/02 23:25
L8	18	("7206876" "7680966" "20100235554" "20040260864" "7546497" "8473653" "20090039492" "6317377" "7245239" "7385281" "20040246801" "20070005831" "7013359" "20090024790" "7810017" "8036052" "8803545" "7903685").PN.	US-PGPUB; USPAT; UPAD	OR	ON	2015/08/02 23:27
L9	13	("20040246801" "20040260864" "20070005831" "20100235554" "7013359" "7206876" "7546497" "7680966" "7810017" "7903685" "8036052" "8473653" "8803545").PN.	US-PGPUB; USPAT; UPAD	OR	ON	2015/08/02 23:28

8/ 2/ 2015 11:45:00 PM

C:\ Users\ hbyrne\ Documents\ EAST\ Workspaces\ 13649131.wsp

Search Notes 	Application/Control No. 13649131	Applicant(s)/Patent Under Reexamination KEN ET AL.
	Examiner HARRY W BYRNE	Art Unit 2824

CPC- SEARCHED		
Symbol	Date	Examiner
G11C5/00	8/2/2015	HWB

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
365	63,185.05,185.06,185.11,214	8/2/2015	HWB

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor Name Search	8/2/2015	HWB
EAST Search History	8/2/2015	HWB

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
365	63	8/2/2015	HWB
USPatent & PGPub	Text Search on Claim Language	8/2/2015	HWB

	/HARRY W BYRNE/ Primary Examiner.Art Unit 2824
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13649131
Filing Date	2012-10-11
First Named Inventor	Weng-Dah Ken
Art Unit	2824
Examiner Name	ELMS, RICHARD T
Attorney Docket Number	ETRP0133USA

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	8036052	B2	2011-10-11	Lee	
	2	8473653	B2	2013-06-25	Kondo	
	3	7680966	B1	2010-03-16	Falik	
	4	7903685	B2	2011-03-08	Eshraghian	
	5	7206876	B2	2007-04-17	Jang	
	6	7013359	B1	2006-03-14	Li	
	7	7810017	B2	2010-10-05	Radke	
	8	8803545	B2	2014-08-12	Yoko	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13649131
	Filing Date	2012-10-11
	First Named Inventor	Weng-Dah Ken
	Art Unit	2824
	Examiner Name	ELMS, RICHARD T
	Attorney Docket Number	ETRP0133USA

	9	7546497	B2	2009-06-09	Jang	
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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040246801	A1	2004-12-09	Lee	
	2	20040260864	A1	2004-12-23	Lee	
	3	20100235554	A1	2010-09-16	Chang	
	4	20070005831	A1	2007-01-04	Gregorius	

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1						

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.
--------------------	---------	---

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13649131
	Filing Date	2012-10-11
	First Named Inventor	Weng-Dah Ken
	Art Unit	2824
	Examiner Name	ELMS, RICHARD T
	Attorney Docket Number	ETRP0133USA

	1		
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13649131
Filing Date	2012-10-11
First Named Inventor	Weng-Dah Ken
Art Unit	2824
Examiner Name	ELMS, RICHARD T
Attorney Docket Number	ETRP0133USA

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

- ☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

- ☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

- ☐ See attached certification statement.
- ☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
- ☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott Margo/	Date (YYYY-MM-DD)	2015-06-21
Name/Print	Scott Margo	Registration Number	56277

Electronic Acknowledgement Receipt

EFS ID:	22692877
Application Number:	13649131
International Application Number:	
Confirmation Number:	1078
Title of Invention:	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE
First Named Inventor/Applicant Name:	Weng-Dah Ken
Customer Number:	27765
Filer:	Winston Hsu/Anna Lu
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	ETRP0133USA
Receipt Date:	23-JUN-2015
Filing Date:	11-OCT-2012
Time Stamp:	03:20:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2281676.PDF	32396 998dbcdf56af3be30352d879293cdd1885410cc7	no	4

Warnings:

Information:

This is not an USPTO supplied IDS fillable form	
Total Files Size (in bytes):	32396
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/649,131	10/11/2012	Weng-Dah Ken	ETRP0133USA

CONFIRMATION NO. 1078

27765

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

PUBLICATION NOTICE



Title:HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE

Publication No.US-2013-0091315-A1

Publication Date:04/11/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/649,131	10/11/2012	2827	874	ETRP0133USA	31	2

CONFIRMATION NO. 1078

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

FILING RECEIPT



OC000000057300183

Date Mailed: 11/01/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Weng-Dah Ken, Hsinchu City, TAIWAN;
Nicky Lu, Taipei City, TAIWAN;

Applicant(s)

Etron Technology, Inc., Hsinchu, TAIWAN

Assignment For Published Patent Application

Etron Technology, Inc., Hsinchu, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/546,039 10/11/2011

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 10/25/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/649,131**

Projected Publication Date: 04/11/2013

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/649,131			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	98		N/A			
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	310		N/A			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	125		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))	31	minus 20 = * 11	x 31 =	341	OR				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x 125 =	0.00					
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00					
				TOTAL		TOTAL			
				874					
* If the difference in column 1 is less than zero, enter "0" in column 2.									
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =		
	Application Size Fee (37 CFR 1.16(s))					OR			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR			
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =		
	Application Size Fee (37 CFR 1.16(s))					OR			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR			
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/649,131	10/11/2012	Weng-Dah Ken	ETRP0133USA

CONFIRMATION NO. 1078

POA ACCEPTANCE LETTER

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116



Date Mailed: 11/01/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/11/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hkquach/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Weng-Dah Ken
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	ETRP0133USA

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7385281		2008-06-10	Nishio	
	2	7245239		2007-07-17	Wallner	
	3	6317377		2001-11-13	Kobayashi	

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090024790		2009-01-22	Rajan	
	2	20090039492		2009-02-12	KANG	

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Weng-Dah Ken
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	ETRP0133USA

	1							
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NON-PATENT LITERATURE DOCUMENTS								
--	--	--	--	--	--	--	--	--

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE			
---------------------------	--	--	--

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Weng-Dah Ken
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	ETRP0133USA

CERTIFICATION STATEMENT

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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott Margo/	Date (YYYY-MM-DD)	2012-10-11
Name/Print	Scott Margo	Registration Number	56277

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	ETRP0133USA
		Application Number	
Title of Invention	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Weng-Dah		Ken		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Hsinchu City	Country Of Residence¹	TW		
Mailing Address of Inventor:					
Address 1		No.41, Zhiping Rd.			
Address 2					
City	Hsinchu City	State/Province			
Postal Code			Country¹	TW	
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Nicky		Lu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Taipei City	Country Of Residence¹	TW		
Mailing Address of Inventor:					
Address 1		8F., No.5, Ln. 63, Sec. 2, Dunhua S. Rd., Da'an Dist.			
Address 2					
City	Taipei City	State/Province			
Postal Code			Country¹	TW	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	ETRP0133USA
		Application Number	
Title of Invention	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE		

☐ An Address is being provided for the correspondence information of this application.

Customer Number	27765		
Email Address	scottmargo@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE		
Attorney Docket Number	ETRP0133USA	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	13	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

Request Not to Publish. I hereby request that the attached application not be published under

☐ 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	non provisional of	61546039	2011-10-11

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	ETRP0133USA
		Application Number	
Title of Invention	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☐ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	ETRP0133USA
		Application Number	
Title of Invention	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE		

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Remove

☒ Assignee	☐ Legal Representative under 35 U.S.C. 117
☐ Person to whom the inventor is obligated to assign.	☐ Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Assignee is an Organization check here. ☒

Organization Name Etron Technology, Inc.

Mailing Address Information:

Address 1		No. 6, Technology Road 5	
Address 2			
City	Hsinchu	State/Province	
Country ⁱ	TW	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Scott Margo/		Date (YYYY-MM-DD)	2012-10-11
First Name	Scott	Last Name	Margo	Registration Number
				56277

Additional Signature may be generated within this form by selecting the Add button.

Add

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	ETRP0133USA
		Application Number	
Title of Invention	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE
-------------------------------	---

As the below named inventor, I hereby declare that:

This declaration is directed to: ☒ The attached application, or
☐ United States application or PCT international application number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Weng-Dah Ken Date (Optional): _____

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office; U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

**Title of
Invention**

HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE
WITH A HIGH SPEED MEMORY CHIP MODULE

As the below named inventor, I hereby declare that:

This declaration is directed to: ☒ The attached application, or
☐ United States application or PCT international application number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Nicky Lu Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:



Practitioners associated with Customer Number:

27765

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:



The address associated with Customer Number:

27765

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address:

Etron Technology, Inc.
No. 6, Technology Road 5, Hsinchu, Taiwan, R.O.C.

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	OCT 03 2012
Name	Sung, Janmye	Telephone	+886-3-5782345
Title	President		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Etron Technology, Inc.Application No./Patent No.: N/AFiled/Issue Date: N/ATitled: HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULEEtron Technology, Inc., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Scott Margo/

Signature

Scott Margo

Printed or Typed Name

10/11/2012

Date

56277

Title or Registration Number

ASSIGNMENT OF INVENTION

In consideration of the payment by ASSIGNEE to ASSIGNOR of the sum of One Dollar (\$1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

ASSIGNOR(S) (Inventors):

Name: Weng-Dah Ken Nationality: TW

Name: Nicky Lu Nationality: US

Hereby sells, assigns and transfers to

ASSIGNEE(S):

Name: Etron Technology, Inc.

Address: No. 6, Technology Road 5, Hsinchu 30078, Taiwan, R.O.C.

and the successors and assignees of the ASSIGNEE the entire right, title, and interest in and to any and all improvements which are disclosed in the invention entitled:

"HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH
A HIGH SPEED MEMORY CHIP MODULE"

Which is found in :

- (a) + U.S. patent application executed on even date
(b) _____ U.S. patent application executed on _____
(c) _____ U.S. application serial no. _____
(d) _____ patent no. _____ issued _____
(e) _____ International application no. _____

and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof

ASSIGNOR hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

ASSIGNOR further covenants that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to ASSIGNOR and will testify as to the same in any interference, litigation or proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.

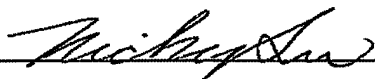
IN WITNESS WHEREOF, We have hereunto set hand and seal this 10-09-2012 (Date of signing). (請發明人務必簽署上列日期。)

(Type name of inventor)

Weng-Dah Ken

Nicky Lu

Signature of INVENTOR

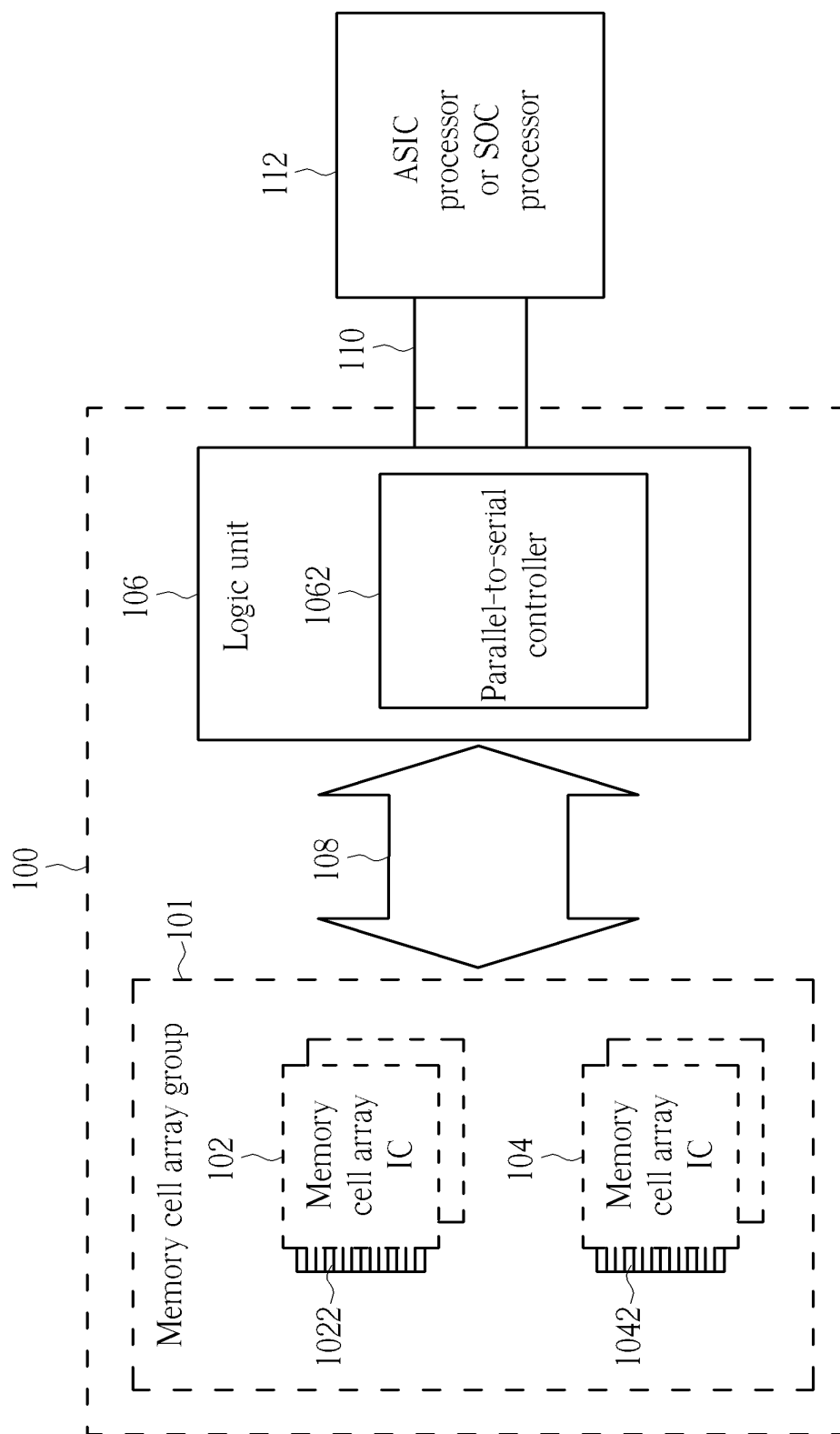


FIG. 1

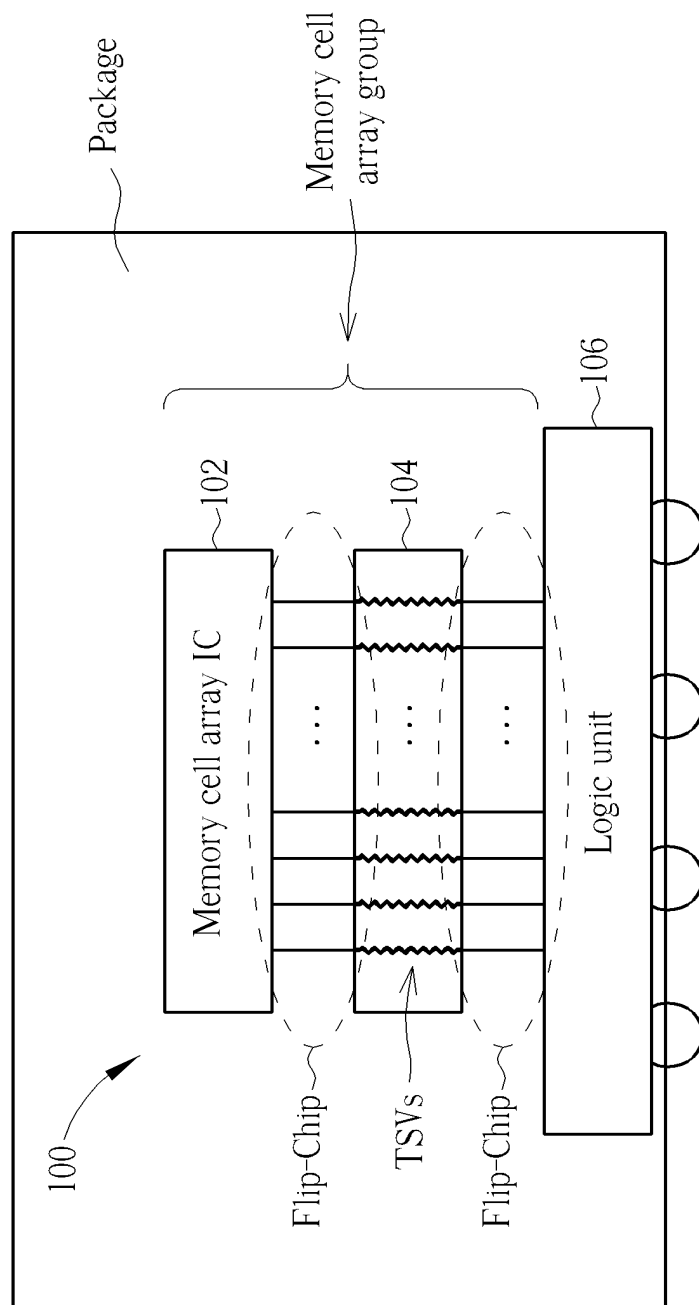


FIG. 2

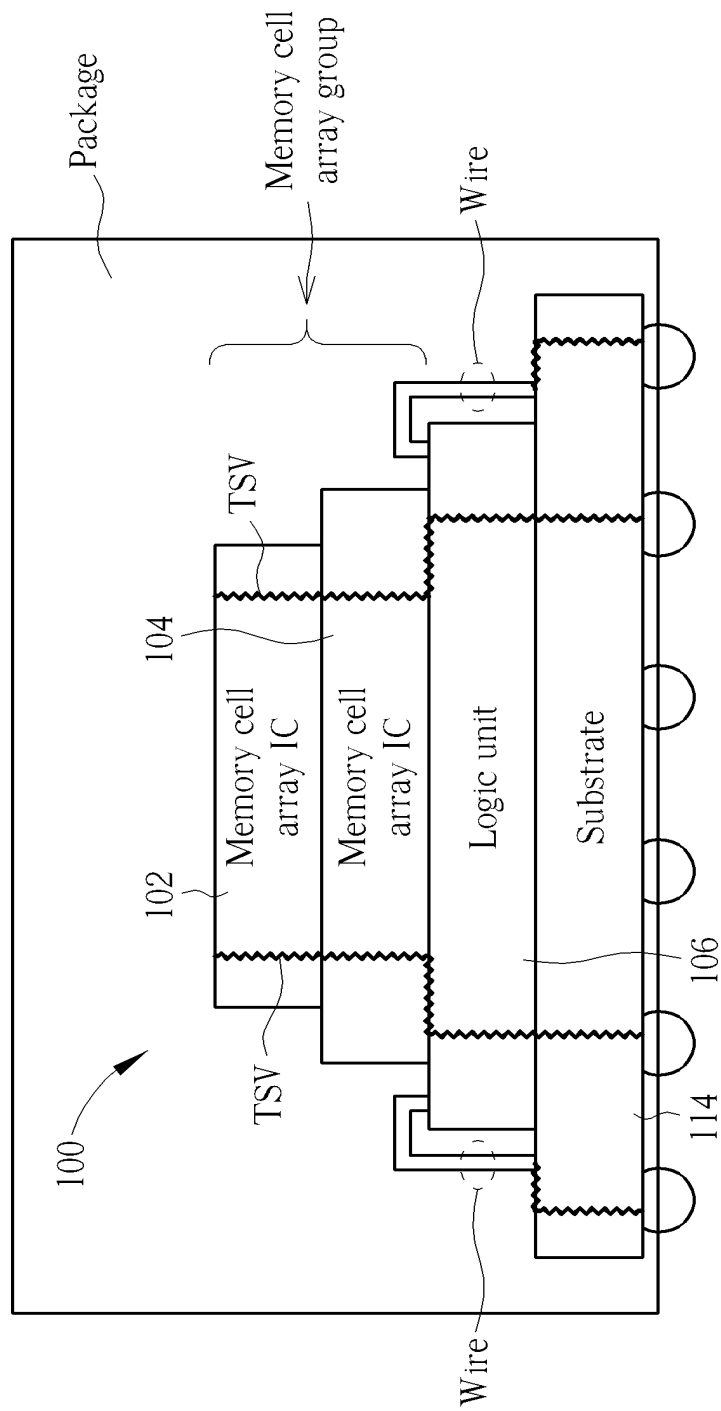


FIG. 3

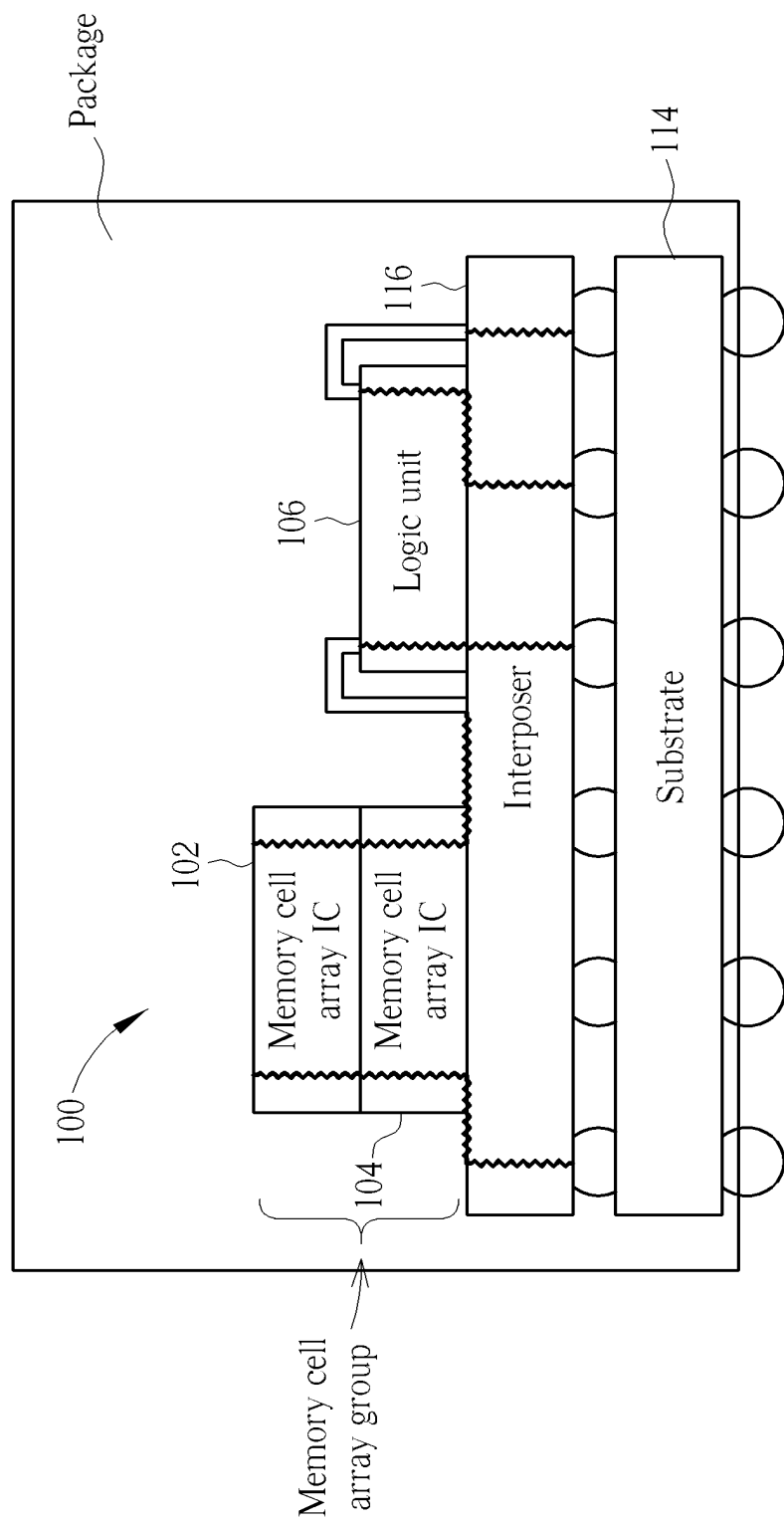


FIG. 4

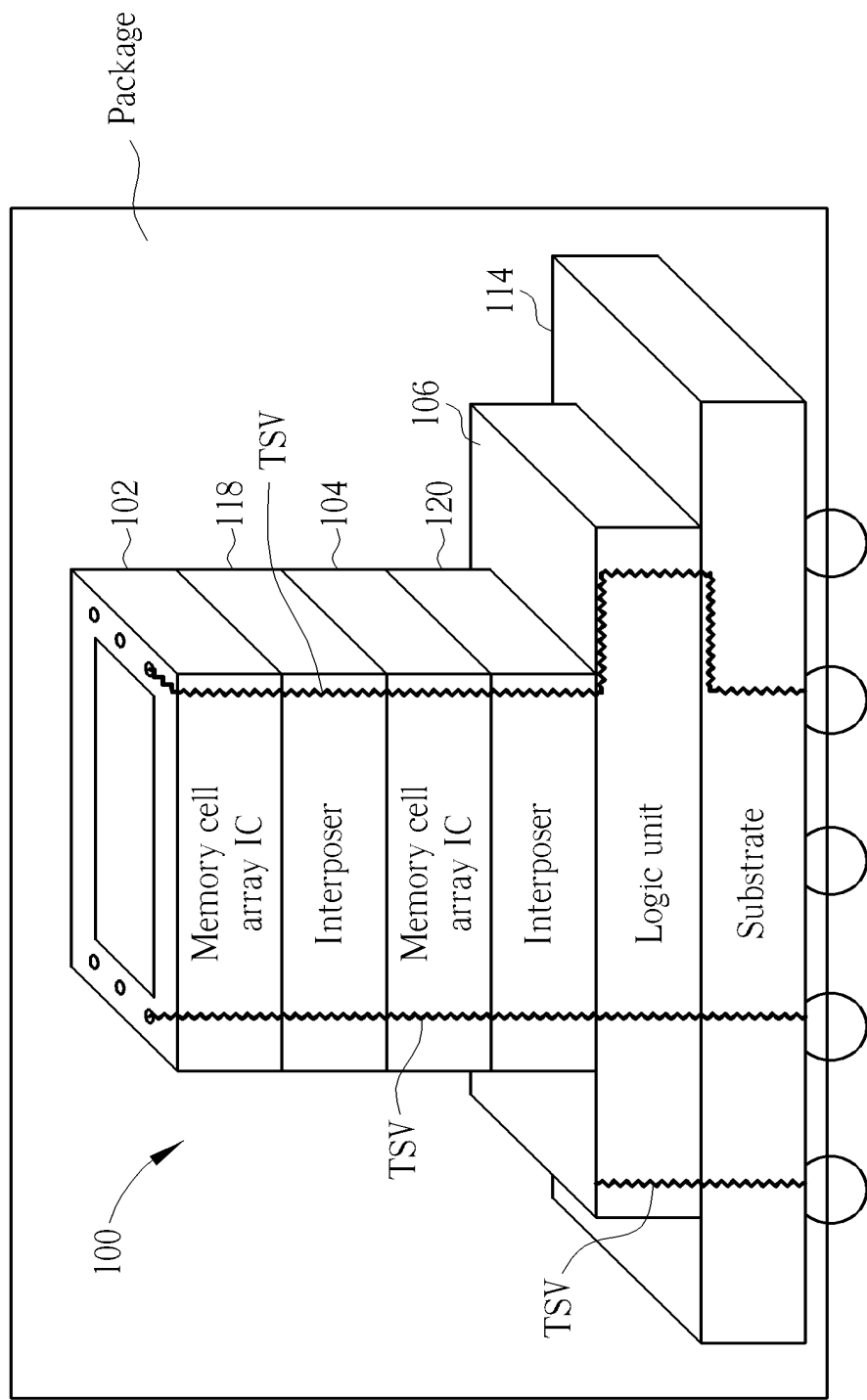


FIG. 5

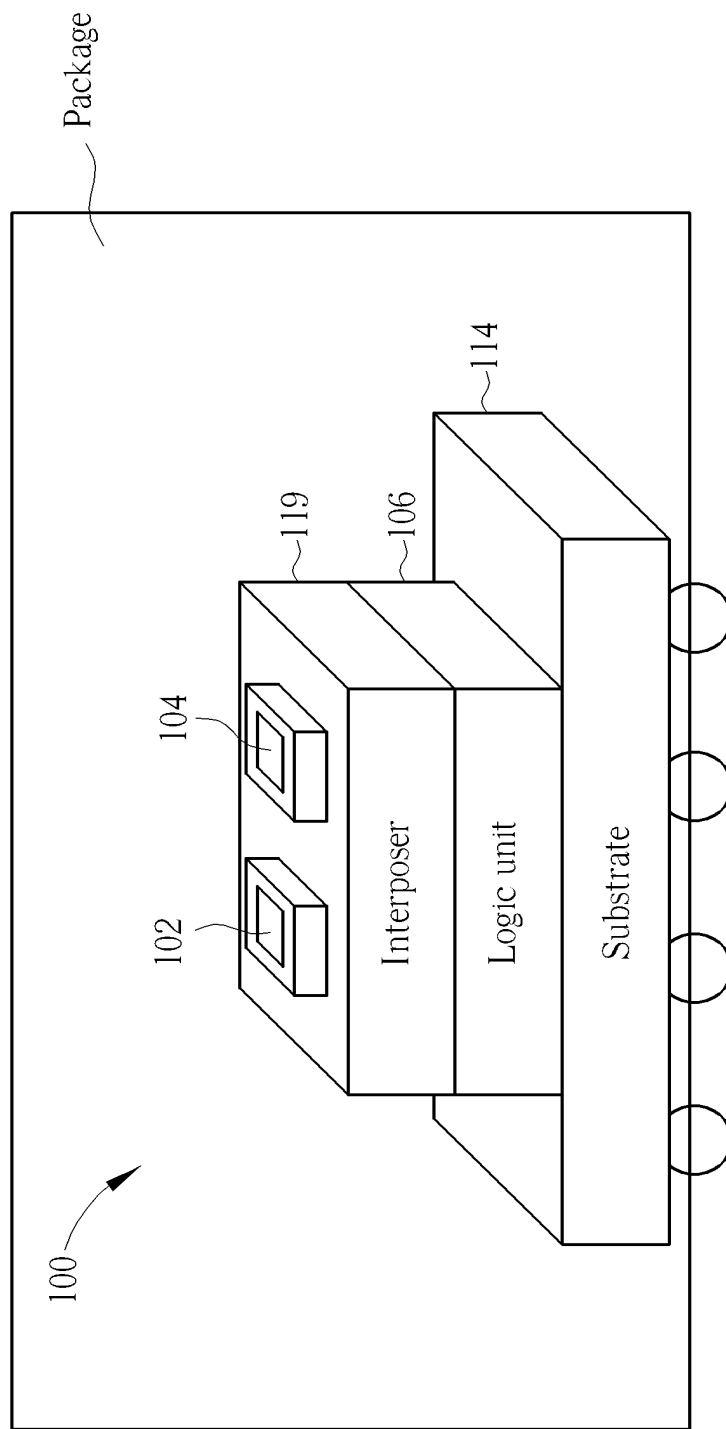


FIG. 6

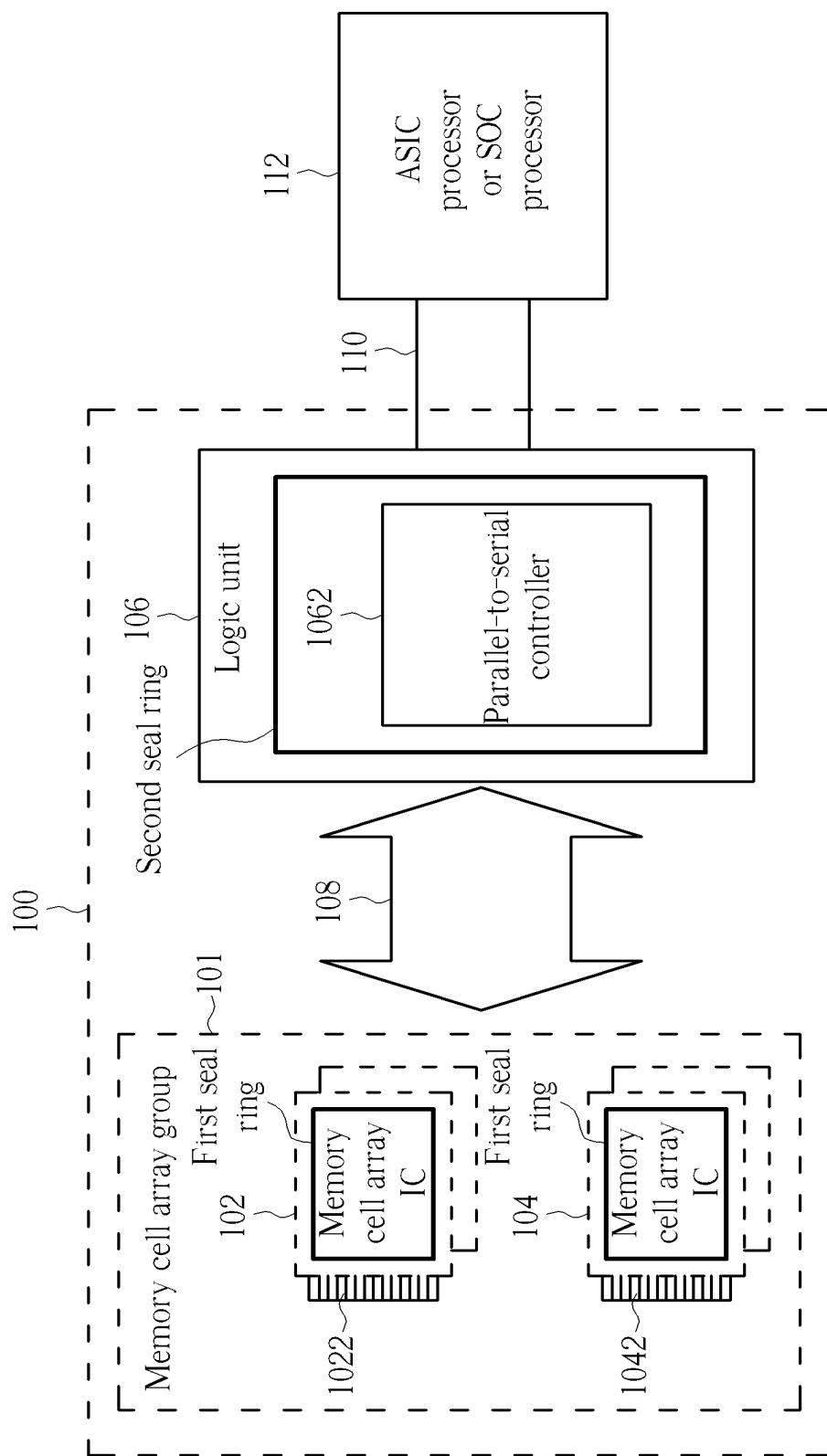


FIG. 7

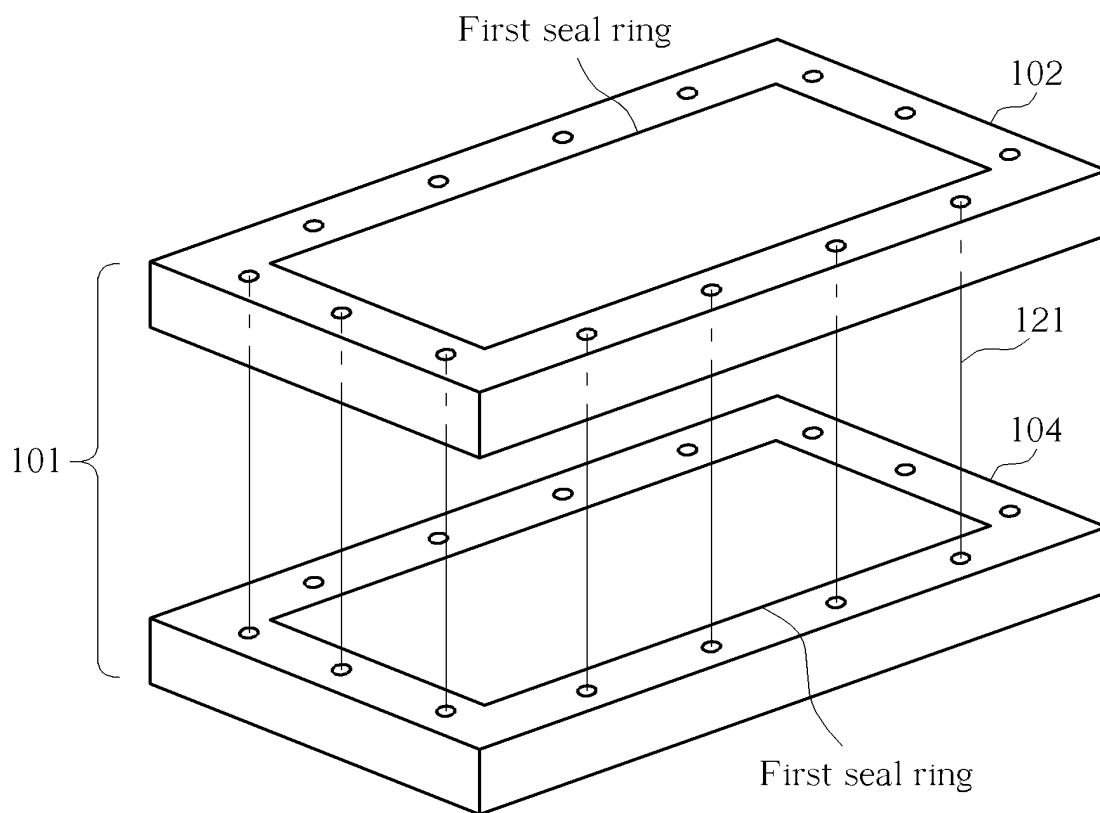


FIG. 8

Cover $\geq 50\%$ area of the topmost
memory cell array of the memory
cell array IC 102

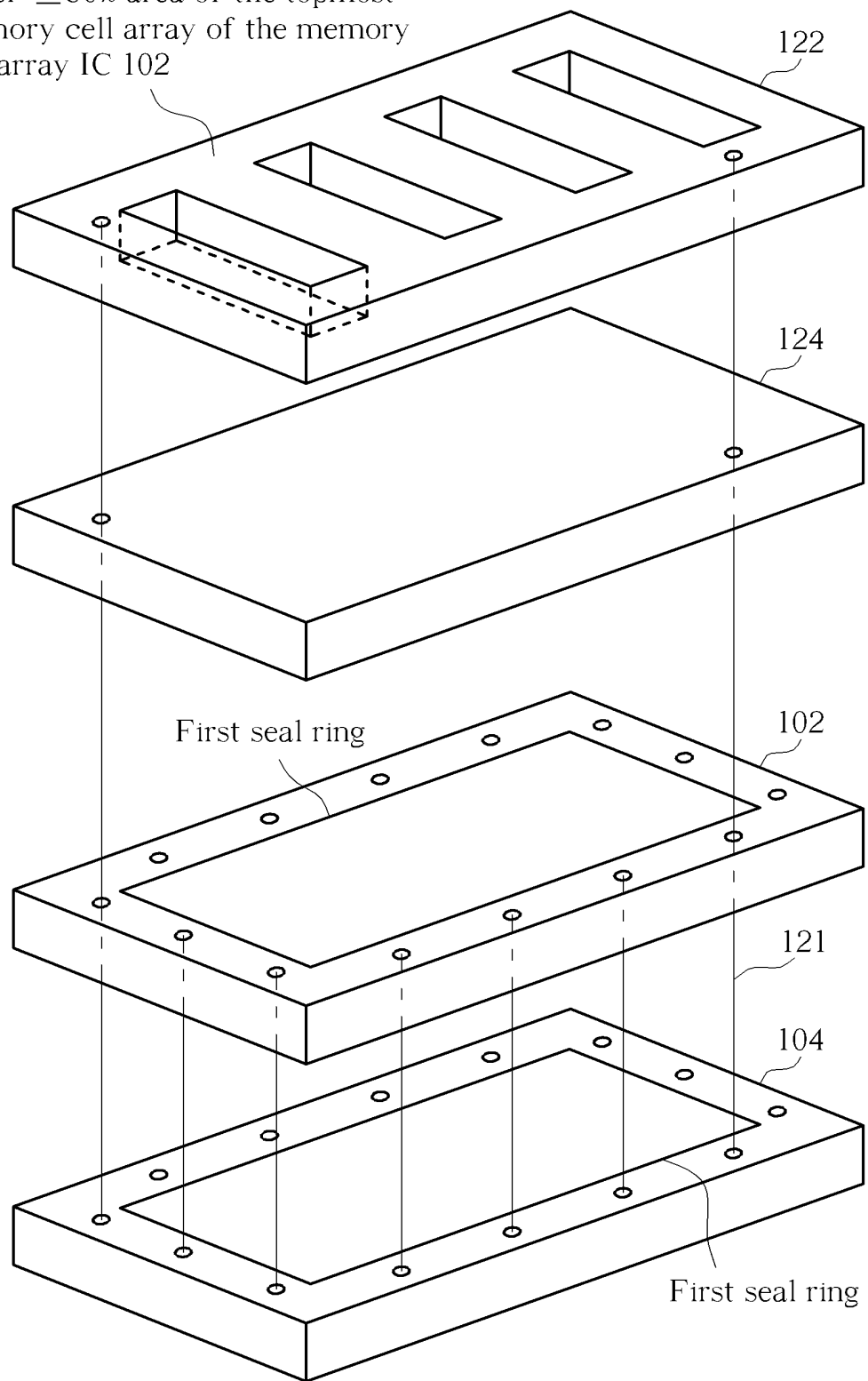


FIG. 9

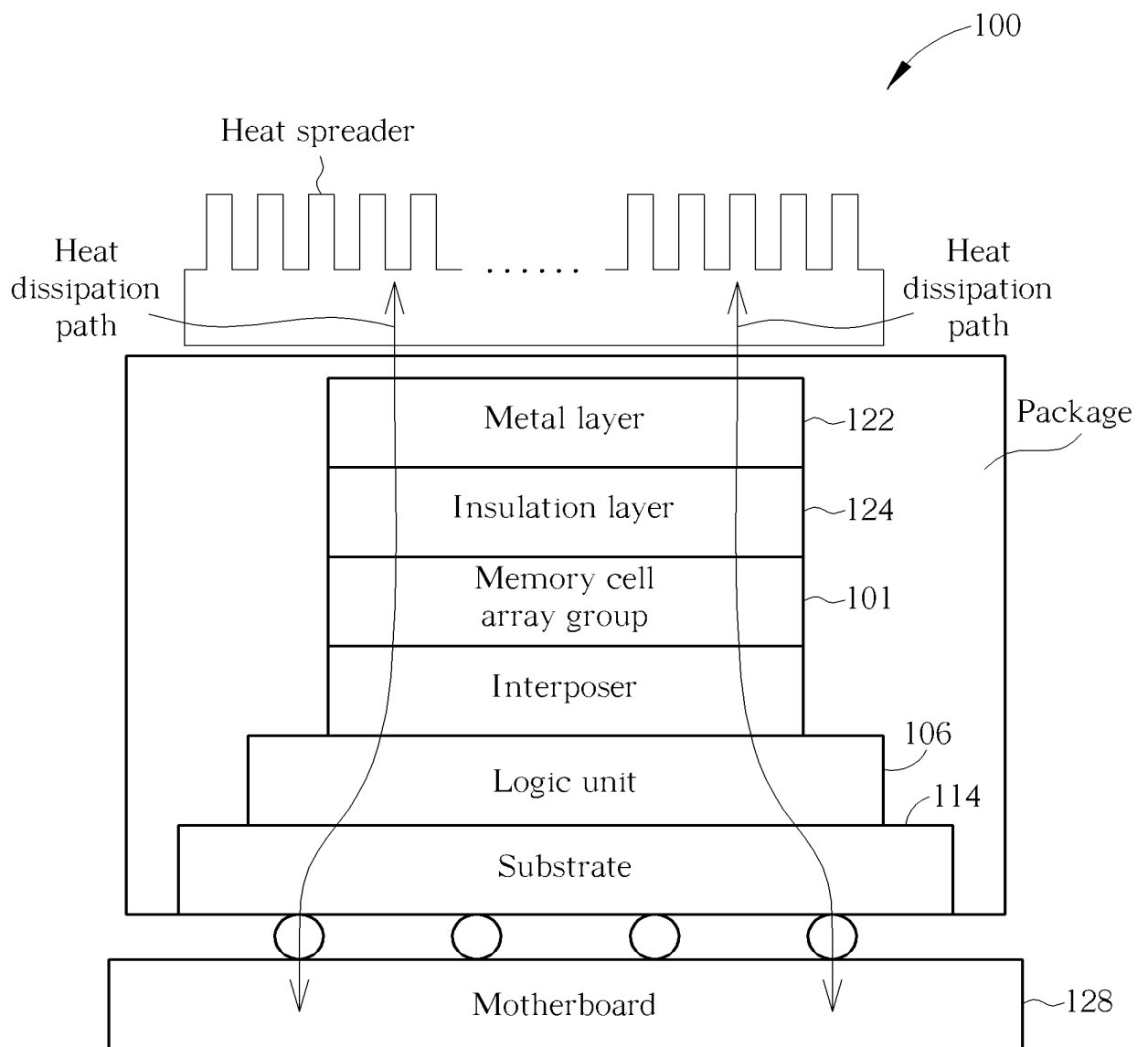


FIG. 10

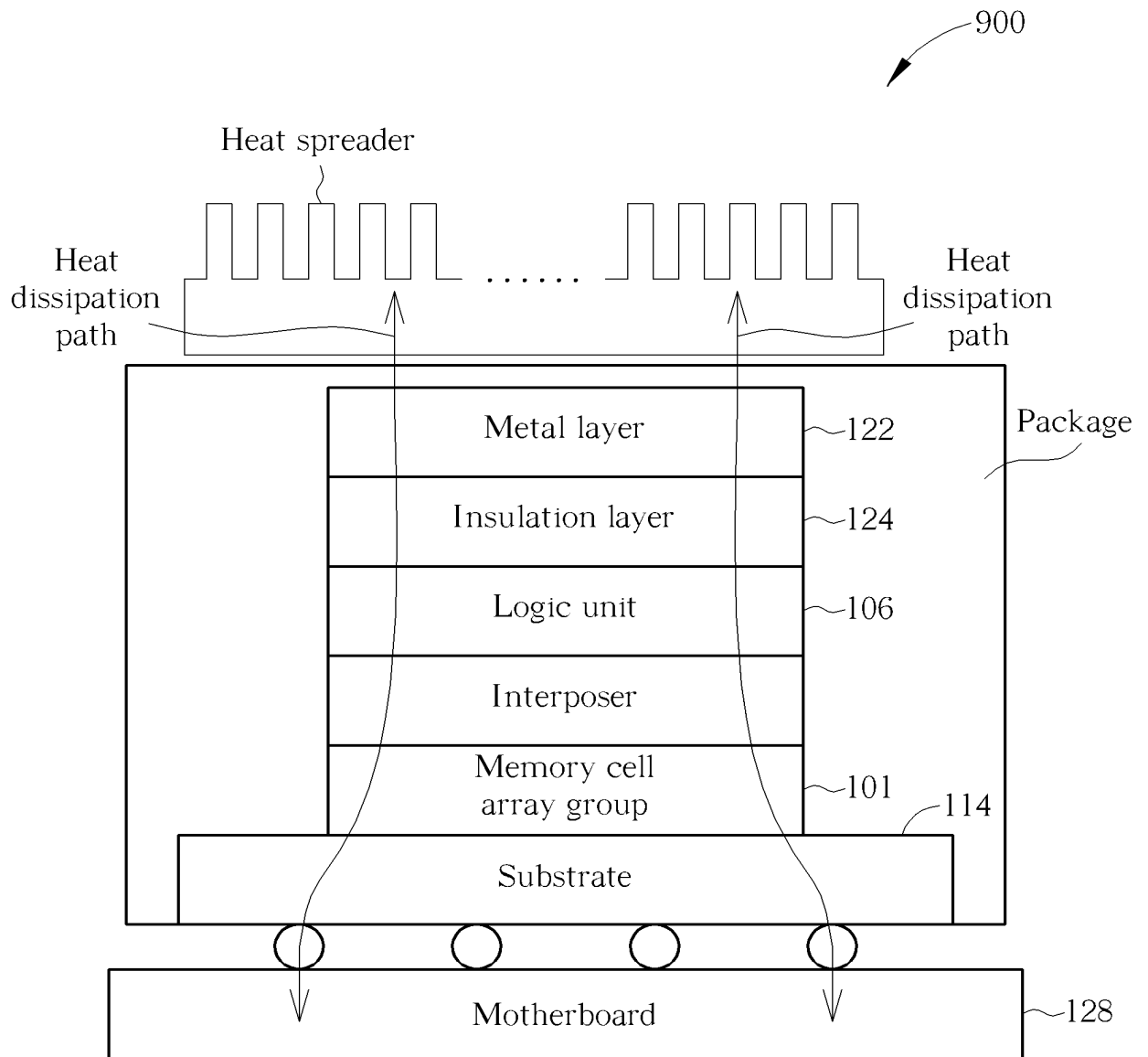


FIG. 11

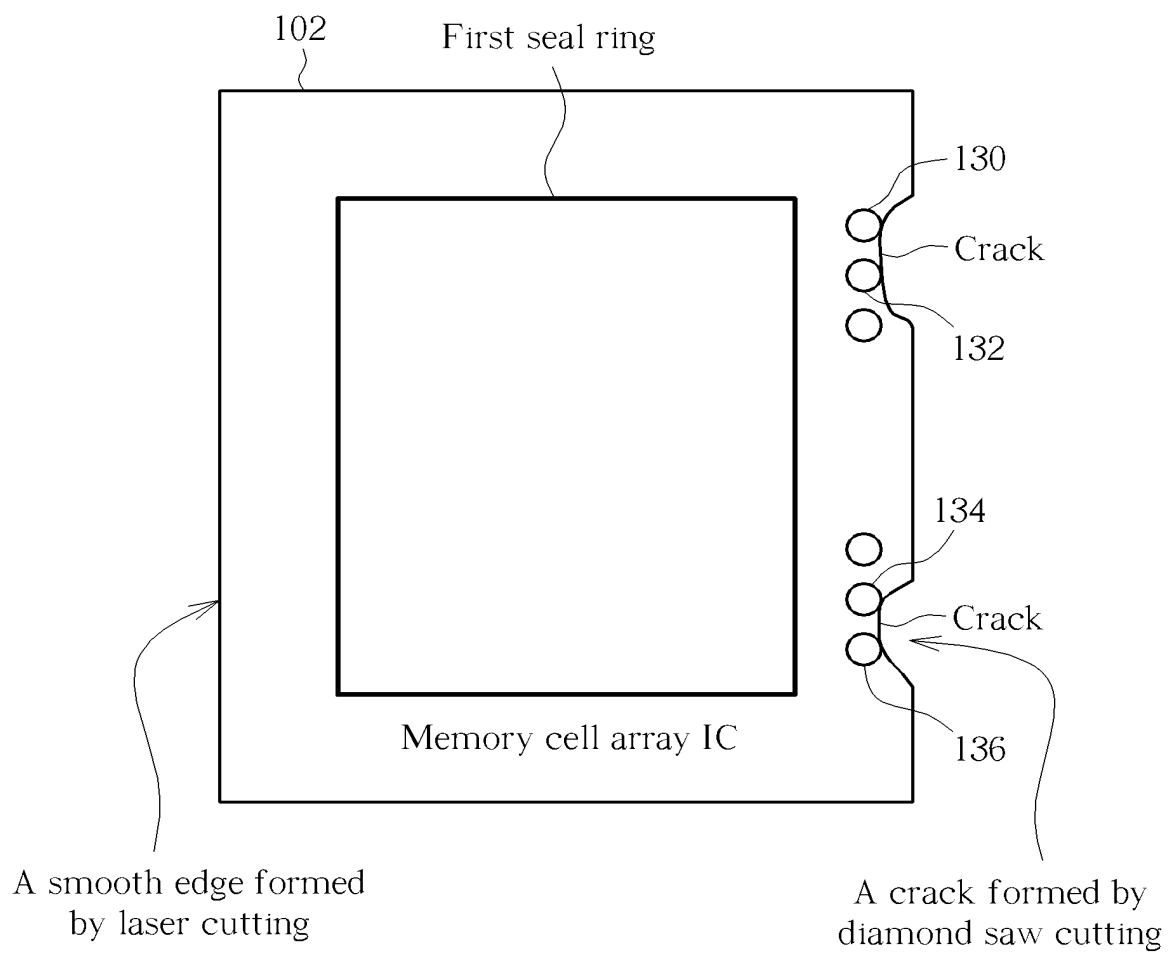


FIG. 12

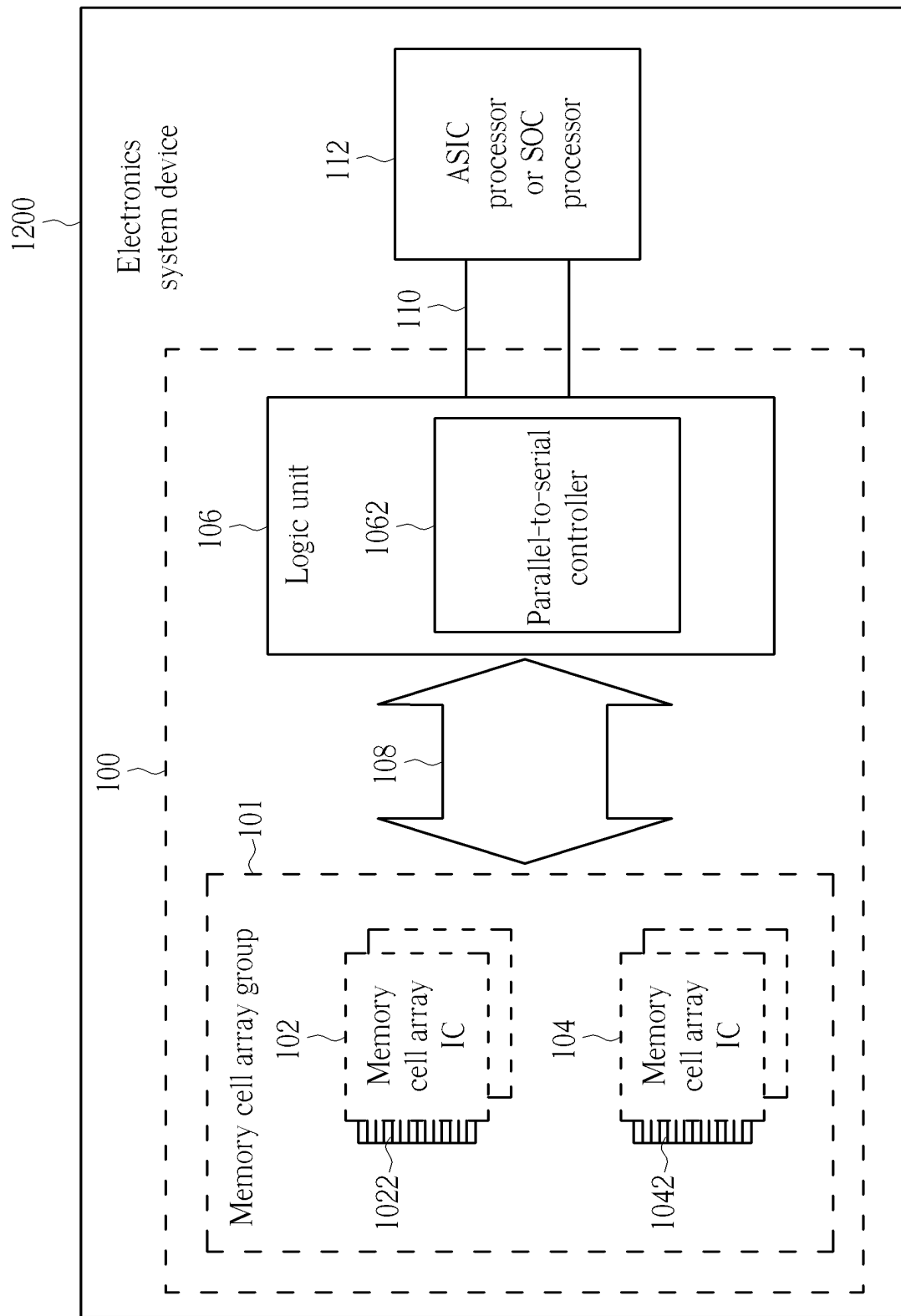


FIG. 13

Abstract of Disclosure

A high speed memory chip module includes a type of memory cell array group and a logic unit. The type memory cell array group includes multiple memory cell array integrated circuits (ICs), and each of the memory cell array ICs has a data bus and at least one memory cell array, and corresponds to first metal-oxide-semiconductor field-effect transistor (MOSFET) gate length corresponding to a first MOSFET process. The logic unit accesses the type of memory cell array group through a first transmission bus, where bus width of the first transmission bus is wider than bus width of the data bus of each of the memory cell array ICs. Corresponding to a second MOSFET process, the logic unit has a second MOSFET gate length which is shorter than the first MOSFET gate length.

Claims

What is claimed is:

1. A high speed memory chip module, comprising:
 - a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array integrated circuits (ICs), each of the memory cell array ICs has an input/output (I/O) data bus and at least one memory cell array corresponding to a first metal-oxide-semiconductor field-effect transistor (MOSFET) process, wherein the first MOSFET process corresponding to a first MOSFET gate length; and
 - a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an I/O data bus of each of the memory cell array ICs, wherein the logic unit corresponds to a second MOSFET process, the second MOSFET process corresponds to a second MOSFET gate length, and the first MOSFET gate length is longer than the second MOSFET gate length; wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus.
2. The high speed memory chip module of claim 1, wherein the multiple memory cell array ICs of the type of memory cell array group comprise a flash IC or a Dynamic Random Access Memory (DRAM) IC, wherein a dicing method for at least one memory cell array IC comprises a Laser cutting process.
3. The high speed memory chip module of claim 1, further comprising: an interposer, wherein at least one memory cell array IC of the memory cell array group and the logic unit are disposed over two opposite sides of the interposer, respectively, wherein

the interposer comprises silicon or oxide glass material.

4. The high speed memory chip module of claim 1, further comprising:
an interposer, wherein the multiple memory cell array ICs are disposed over the interposer respectively, and the interposer is disposed over the logic unit, wherein the interposer comprises silicon or oxide glass material, wherein a dicing method for at least one memory cell array IC comprises a Laser cutting process.
5. The high speed memory chip module of claim 1, wherein the logic unit further comprises:
a parallel-to-serial controller module for converting the first set of parallel data into the second set of parallel data, and the logic unit transmits the second set of parallel data to an application-specific integrated circuit (ASIC) or a system on chip (SOC) processor through the second transmission bus, wherein bit width of the first set and the second set of parallel data are different.
6. The high speed memory chip module of claim 5, wherein the second transmission bus is a bus comprising the protocol of Universal Serial Bus (USB), a Serial Advanced Technology Attachment (SATA) bus, a Universal Flash Storage (UFS) bus, a mobile industry processor interface (MIPI) bus, or a Peripheral Component Interconnect Express (PCIE) bus.
7. The high speed memory chip module of claim 5, wherein a signal swing of data transmitted through the first transmission bus and a signal swing of data received through the first transmission bus are different.
8. The high speed memory chip module of claim 5, wherein a signal swing of data transmitted through the second transmission bus and

a signal swing of data received through the second transmission bus are different.

9. The high speed memory chip module of claim 5, wherein a transmitting data rate of the first transmission bus and a receiving data rate of the first transmission bus are different.
10. The high speed memory chip module of claim 5, wherein a transmitting data rate of the second transmission bus and a receiving data rate of the second transmission bus are different.
11. The high speed memory chip module of claim 1, wherein each of the memory cell array ICs of the type of memory cell array group corresponds to a first seal ring and the logic unit corresponds to a second seal ring, a circuit of each of the memory cell array ICs is surrounded by a first seal ring and a circuit of the logic unit is surrounded by the second seal ring.
12. The high speed memory chip module of claim 11, wherein at least one through silicon via (TSV) exists outside a first seal ring of each of the memory cell array ICs.
13. The high speed memory chip module of claim 12, further comprising:
a metal layer disposed over a topmost memory cell array of the type of memory cell array group, wherein the metal layer covers more than 50% area of the topmost memory cell array.
14. The high speed memory chip module of claim 12, wherein the at least one TSV is used for connecting to a power or a ground supply.
15. The high speed memory chip module of claim 11, wherein at least one TSV exists outside the second seal ring of the logic unit.
16. The high speed memory chip module of claim 15, wherein the logic unit is stacked over a topmost memory cell array IC of the type

of memory cell array group.

17. The high semiconductor speed memory chip module of claim 16, further comprising: a metal layer disposed over the logic unit, wherein the metal layer covers more than 50% area of the logic unit.
18. The high speed memory chip module of claim 15, wherein the at least one TSV is used for connecting to a power or a ground supply.
19. A electronics system device with a high speed memory chip module, the device comprising:
 - an ASIC processor;
 - a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs, each of the memory cell array ICs has an (I/O) data bus; and
 - a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an (I/O) data bus of each of the memory cell array ICs, wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus, and transmits the second set of parallel data to the ASIC processor;wherein the ASIC processor executes a predetermined function corresponding to the second set of parallel data while the ASIC processor is under operating condition, wherein bit width of the first set and the second set of parallel data are different.
20. The electronics system device of claim 19, further comprising: an interposer, wherein at least one memory cell array IC of the memory cell array group and the logic unit are disposed over

two opposite sides of the interposer, respectively, wherein the interposer comprises silicon or oxide glass material, wherein a dicing method for at least one memory cell array ICs comprises a Laser cutting process.

21. The electronics system device of claim 19, further comprising:
an interposer, wherein the multiple memory cell array ICs are disposed over the interposer respectively, and the interposer is disposed over the logic unit, wherein the interposer comprises silicon or oxide glass material.
22. The electronics system device of claim 19, wherein the logic unit comprises:
a parallel-to-serial controller module for converting the first set of parallel data into the second set of parallel data.
23. The electronics system device of claim 22, wherein a signal swing of data transmitted through the first transmission bus and a signal swing of data received through the first transmission bus are different.
24. The electronics system device of claim 22, wherein a signal swing of data transmitted through the second transmission bus and a signal swing of data received through the second transmission bus are different.
25. The electronics system device of claim 22, wherein a transmitting data rate of the first transmission bus and a receiving data rate of the first transmission bus are different.
26. The electronics system device of claim 22, wherein a transmitting data rate of the second transmission bus and a receiving data rate of the second transmission bus are different.
27. The electronics system device of claim 19, wherein each of the

memory cell array ICs of the type of memory cell array group corresponds to a first seal ring and the logic unit corresponds to a second seal ring, a circuit of each of the memory cell array ICs is surrounded by the first seal ring and a circuit of the logic unit is surrounded by the second seal ring.

28. The electronics system device of claim 27, wherein at least one TSV exists outside a first seal ring of each of the memory cell array ICs.
29. The electronics system device of claim 28, further comprising:
a metal layer disposed over a topmost memory cell array IC of the type of memory cell array group, wherein the metal layer covers more than 50% area of the topmost memory cell array IC, wherein the memory cell array ICs are stacked over the logic unit.
30. The electronics system device of claim 28, wherein the at least one TSV is used for connecting to a power or a ground supply.
31. The electronics system device of claim 27, wherein at least one TSV exists outside the second seal ring of the logic unit.

Title

HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE

Cross Reference To Related Applications

[0001] This application claims the benefit of U.S. Provisional Application No. 61/546,039, filed on October 11, 2011 and entitled "High Speed Memory Platform," the contents of which are incorporated herein by reference.

Background of the Invention

1. Field of the Invention

[0002] The present invention relates to a high speed memory chip module and a electronics system device with a high speed memory chip module, and particularly to a high speed memory chip module and an electronics system device with a high speed memory chip module that have lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, enhanced electromagnetic interference (EMI) shielding effect, better heat dissipation capability, and an external noise isolation function.

2. Description of the Prior Art

[0003] Generally speaking, memories are usually designed as standard memory module or chip which are independent from logic units based on certain industry standard (e.g. Joint Electronic Device Engineering Council, JEDEC is the exemplary one). That is to say, memories are designed typically as standard memory module or chip for various logic units based on certain industry standard, but not for predetermined logic units.

[0004] In the prior art, because memory semiconductor process generations are typically more advanced and different from logic unit semiconductor process generations. That is to say, a chip or module memory system, integrating discrete memories with the advanced semiconductor process generations, may face poorer heat dissipation,

higher power consumption and bad noise interference, so the chip or module memory system with integrating memories and logic units still suffers from much manufacturing difficulty.

Summary of the Invention

[0005] An embodiment provides a high speed memory chip module. The high speed memory chip module includes a type of memory cell array group and a logic unit. The type of memory cell array group includes multiple memory cell array integrated circuits (ICs). Each of the memory cell array ICs has an input/output (I/O) data bus. The memory cell array IC further includes at least one memory cell array and corresponds to a first metal-oxide-semiconductor field-effect transistor (MOSFET) gate length corresponding to a first MOSFET process. The logic unit is used for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of the data bus of each of the memory cell array ICs, wherein the logic unit corresponds to a second MOSFET process, the second MOSFET process corresponds to a second MOSFET gate length of a standard logic cell for the logic unit, and the first MOSFET gate length is longer than the second MOSFET gate length. The logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.

[0006] Another embodiment provides an electronics system device with a high speed memory chip module. The electronics system device includes an ASIC processor, a type of memory cell array group and a logic unit. The type of memory cell array group comprises multiple memory cell array ICs, each of the memory cell array ICs has an (I/O) data bus. The logic unit is used for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first

transmission bus is wider than bus width of the data bus of each of the memory cell array ICs. The logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus, and transmits the second set of parallel data to the ASIC processor. The ASIC processor executes a predetermined function corresponding to the second set of parallel data while the ASIC processor is under operating condition, wherein bit width of the first set and the second set of parallel data are different. In one embodiment, the system power efficiency can be higher if bit width of the first transmission bus is wider than the second one. On the other hand, in another embodiment, the system data transmission bandwidth and noise level can be best optimized if the second transmission bus is wider than the first one.

[0007] The present invention provides a high speed memory chip module and an electronics system device with a high speed memory chip module. The high speed memory chip module and the electronics system device have advantages as follows: first, a signal swing of data transmitted through a first transmission bus and a signal swing of data transmitted through a second transmission bus can be varied with different memory interface standards or be better optimized with different semiconductor processes. The present invention not only has the ability to lower power consumption while operating, but also has the advantage to achieve higher transmission efficiency or bandwidth. Second, the present invention can utilize a plurality of through silicon via (TSV) outside a first seal ring of each memory cell array IC or a plurality of TSV outside a second seal ring of a logic unit to form a metal fence function. The conductive or metal fence of the present invention can perform a better EMI shielding effect, better heat dissipation capability, or an external noise isolation function based on the magnetic-electronic theory available today. Therefore, compared to the prior art, the present invention has the advantage of achieving lower power consumption, higher transmission efficiency, better EMI shielding effect, better heat dissipation capability, and

with better external noise isolation functions.

[0008] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0009] FIG. 1 is a diagram illustrating a high speed memory chip module according to an embodiment.

[0010] FIG. 2 is a diagram illustrating a cross-section of the high speed memory chip module.

[0011] FIG. 3 is a diagram illustrating a cross-section of the high speed memory chip module according to another embodiment.

[0012] FIG. 4 is a diagram illustrating a cross-section of the high speed memory chip module according to another embodiment.

[0013] FIG. 5 is a diagram illustrating a cross-section of the high speed memory chip module according to another embodiment.

[0014] FIG. 6 is a diagram illustrating a cross-section of the high speed memory chip module according to another embodiment.

[0015] FIG. 7 is a diagram illustrating each of the memory cell array ICs corresponding to a first seal ring and the logic unit corresponding to a second seal ring.

[0016] FIG. 8 is an explosion diagram illustrating a plurality of TSVs existing outside a first seal ring of each of the memory cell array ICs, where the plurality of TSVs are used for connecting to a power or a ground supply.

[0017] FIG. 9 is an explosion diagram illustrating the high speed memory chip module further including a metal layer and an insulation layer when the high speed memory chip module has the 3D structure.

[0018] FIG. 10 is a cross-section diagram illustrating heat dissipation paths of the high speed memory chip module in FIG. 9.

[0019] FIG. 11 is a cross-section diagram illustrating heat dissipation paths of a high speed memory chip according to another embodiment.

[0020] FIG. 12 is a top view illustrating an edge of the memory cell array IC showing cracks during the assembly or package manufacturing process of the high speed memory chip module in FIG. 8.

[0021] FIG. 13 is a diagram illustrating a electronics system device with a high speed memory chip module according to another embodiment.

Detailed Description

[0022] Please refer to FIG. 1. Fig. 1 is a diagram illustrating a high speed memory chip module 100 according to an embodiment. The high speed memory chip module 100 includes a type of memory cell array group 101 and a logic unit 106, where the type of memory cell array group 101 includes a memory cell array integrated circuit (IC) 102 which is a Dynamic Random Access Memory (DRAM) IC and a memory cell array IC 104 which is a flash or non-volatile memory (NVM) IC. But, the present invention is not limited to the high speed memory chip module 100 including the type memory cell array group 101 which includes the memory cell array IC 102 and the memory cell array IC 104, and also not limited to the memory cell array IC 102 being a DRAM IC and the memory cell array IC 104 being a flash or non-volatile memory IC. That is to say, the memory cell array IC 102 and the memory cell array IC 104 can also be other type of memory ICs. In addition, each of the memory cell array ICs 102, 104 has an input/output (I/O) data bus and at least one memory cell array. For example, the memory cell array IC 102 has an I/O data bus 1022 and two memory cell arrays, and the memory cell array IC 104 has an I/O data bus 1042 and two memory cell arrays, where the data bus 1022 and the data bus 1042 have a wired or wireless transmission function along with the logic unit. But, the present invention is not limited to the memory cell array IC 102 having two memory cell arrays and the memory cell array IC 104 having two memory cell arrays. As shown in FIG. 1, the logic unit 106 is used for accessing the memory cell array IC 102 and the memory cell array IC 104 through a first transmission bus 108, where the first transmission bus 108 is used for transmitting a first set of parallel data, and bus width (e.g. 128 bits or 256 bits or more) of the first transmission bus 108 is wider than bus width (e.g. 8

bits or 16 bits or more) of the I/O data bus 1022 and bus width (e.g. 8 bits or 16 bits or more) of the I/O data bus 1042. When the logic unit 106 accesses the first set of parallel data through the first transmission bus 108, the logic unit 106 utilizes a parallel-to-serial controller 1062 included thereof to convert the first set of parallel data into a second set of parallel data, and transmits the second set of parallel data to an application-specific integrated circuit (ASIC) 112 (or system on chip (SOC) processor through a second transmission bus 110 (e.g. a 32 bits serial bus), where the second transmission bus 110 can be comprised of protocol of a Universal Serial Bus 2.0 (USB 2.0), a USB 3.0, a Serial Advanced Technology Attachment (SATA) bus, a Universal Flash Storage (UFS) bus, a mobile industry processor interface (MIPI) bus, or a Peripheral Component Interconnect Express (PCIE) bus. Then, the ASIC processor 112 can execute a predetermined function according to the second set of parallel data. As shown in FIG. 1, the logic unit 106 can be designed as a "parallel-to-serial bus" bridge, receives the first set of parallel data through the first transmission bus 108 with wider bus width (e.g. 128 bits or 256 bits or more), and utilizes the parallel-to-serial controller 1062 to convert the first set of parallel data into the second set of parallel data. In addition, the second transmission bus 110 and the first transmission bus 108 can also be wireless transmission buses to optimize between the power and throughput performance. For example, the second transmission bus 110 and the first transmission bus 108 can be buses for transmitting light or electromagnetic waves. As mentioned in one embodiment, the system power efficiency can be higher if bit width of the first transmission bus is wider than the second transmission bus. On the other hand, in another embodiment, the system data transmission bandwidth and noise level can be best optimized if the second transmission bus is wider than the first transmission bus.

[0023] Please refer to FIG. 2. FIG. 2 is a diagram illustrating a cross-section of the high speed memory chip module 100. As shown in FIG. 2, the memory cell array IC 102, the memory cell array IC 104,

and the logic unit 106 are stacked each other (the memory cell array IC 102 and the memory cell array IC 104 are stacked over the logic unit 106) through Flip-Chip, where the Flip-Chip forms bumps on pads of the memory cell array IC 102, the memory cell array IC 104, and the logic unit 106, and then utilizes the bumps to make the memory cell array IC 102, the memory cell array IC 104, and the logic unit 106 be stacked over each other.

[0024] Please refer to FIG. 3. FIG. 3 is a diagram illustrating a cross-section of the high speed memory chip module 100 according to another embodiment. As shown in FIG. 3, the memory cell array IC 102, the memory cell array IC 104, and the logic unit 106 utilize wire bonding to connect to a substrate 114, where the memory cell array IC 102 and the memory cell array IC 104 are stacked over the logic unit 106.

[0025] Please refer to FIG. 4. FIG. 4 is a diagram illustrating a cross-section of the high speed memory chip module 100 according to another embodiment. As shown in FIG. 4, the high speed memory chip module 100 further includes an interposer 116, where the interposer 116 can be silicon material or oxide glass material. But, the present invention is not limited to the interposer 116 being the silicon material or the oxide glass material. As shown in FIG. 4, the memory cell array IC 102 is stacked over the memory cell array IC 104, and the memory cell array IC 104 and the logic unit 106 are disposed over the two opposite sides of the interposer 116, respectively. In addition, the memory cell array IC 102, the memory cell array IC 104, and the logic unit 106 can utilize the wire bonding, the Flip-Chip, through silicon vias (TSVs), or wireless transmission to connect to each other.

[0026] Please refer to FIG. 5. FIG. 5 is a diagram illustrating a cross-section of the high speed memory chip module 100 according to another embodiment. As shown in FIG. 5, the high speed memory chip module 100 further includes interposers 118, 120. As shown in FIG.

5, the memory cell array IC 102 is stacked over the interposer 118, the interposer 118 is stacked over the memory cell array IC 104, the memory cell array IC 104 is stacked over the interposer 120, the interposer 120 is stacked over the logic unit 106, and the logic unit 106 is stacked over the substrate 114. In addition, the memory cell array IC 102, the memory cell array IC 104, and the logic unit 106 can utilize the wire bonding, the Flip-Chip, the TSVs, or the wireless transmission to connect to each other.

[0027] Please refer to FIG. 6. FIG. 6 is a diagram illustrating a cross-section of the high speed memory chip module 100 according to another embodiment. As shown in FIG. 6, the high speed memory chip module 100 further includes an interposer 119. As shown in FIG. 6, the memory cell array IC 102 and the memory cell array IC 104 are stacked over the interposer 119, the interposer 119 is stacked over the logic unit 106, and the logic unit 106 is stacked over the substrate 114. In addition, the memory cell array IC 102, the memory cell array IC 104, and the logic unit 106 can utilize the wire bonding, the Flip-Chip, the TSVs, or the wireless transmission to connect to each other.

[0028] In addition, packages of the high speed memory chip modules in FIG. 2 to FIG. 6 can be Package-in-Package (PIP), Package on package (POP), or System in Package (SIP). In addition, the high speed memory chip modules in FIG. 2, FIG. 3, FIG. 5, and FIG. 6 are exemplary packages of three-dimensional (3D) structure, and the high speed memory chip module in FIG. 4 is an exemplary package of mixed 3D plus 2.5D structure.

[0029] In addition, a signal swing of data transmitted through the first transmission bus 108 (that is, a voltage difference between a logic level "0" and a logic level "1" transmitted through the first transmission bus 108) is the same as a signal swing of data received through the first transmission bus 108 (e.g. 1.8V), where the signal swing of data transmitted through the first transmission bus 108 and

the signal swing of data received through the first transmission bus 108 can be varied with different memory standards of the memory cell array ICs 102, 104. In addition, for saving power, the logic unit 106 can adjust a signal swing (e.g. 1.8V) of data inputted to the logic unit 106 from the first transmission bus 108 to another or lower signal swing (e.g. 1.2V) inputted to the second transmission bus 110 from the logic unit 106. In addition, a signal swing of data transmitted through the second transmission bus 110 can be the same as a signal swing of data received through the second transmission bus 110 (e.g. 1.2V) whenever required.

[0030] In addition, because a semiconductor process of the memory cell array ICs 102, 104 may be different from semiconductor processes of the logic unit 106 and the ASIC (or SOC) processor 112 (e.g. the semiconductor process of the memory cell array ICs 102, 104 can be a 0.13um-90nm semiconductor process, the semiconductor process of the logic unit 106 can be a 28nm-20nm process, and the process of the ASIC (OR SOC) processor 112 can be a 28nm-13nm semiconductor process), the metal-oxide-semiconductor field-effect transistor (MOSFET) gate length of the semiconductor process of the memory cell array ICs 102, 104 is usually longer than the MOSFET gate length of the semiconductor processes of the logic unit 106 and the ASIC (or SOC) processor 112. In another embodiment of the present invention, a signal swing of data transmitted through the first transmission bus 108 can be different from a signal swing of data received through the first transmission bus 108, and a signal swing of data transmitted through the second transmission bus 110 can also be different from a signal swing of data received through the second transmission bus 110.

[0031] In addition, in another embodiment of the present invention, a signal swing of data transmitted through the first transmission bus 108 can be different from a signal swing of data received through the first transmission bus 108, and a signal swing of data transmitted through the second transmission bus 110 can be the same as a signal

swing of data received through the second transmission bus 110.

[0032] In addition, in another embodiment of the present invention, a signal swing of data transmitted through the first transmission bus 108 can be the same as a signal swing of data received through the first transmission bus 108, and a signal swing of data transmitted through the second transmission bus 110 can be different from a signal swing of data received through the second transmission bus 110.

[0033] For saving power and take the advantage of different semiconductor processes, in another embodiment of the present invention, a transmitting data rate of the first transmission bus 108 can be different from a receiving data rate of the first transmission bus 108, and a transmitting data rate of the second transmission bus 110 can also be different from a receiving data rate of the second transmission bus 110. In addition, in another embodiment of the present invention, the transmitting data rate of the first transmission bus 108 can be the same as the receiving data rate of the first transmission bus 108, and the transmitting data rate of the second transmission bus 110 can also be the same as the receiving data rate of the second transmission bus 110. In addition, in another embodiment of the present invention, a transmitting data rate of the first transmission bus 108 can be different from a receiving data rate of the first transmission bus 108, and a transmitting data rate of the second transmission bus 110 can also be different from a receiving data rate of the second transmission bus 110, and a signal swing of data transmitted through the first transmission bus 108 can be different from a signal swing of data received through the first transmission bus 108, and a signal swing of data transmitted through the second transmission bus 110 can also be different from a signal swing of data received through the second transmission bus 110.

[0034] In addition, as shown in FIG. 1, the type of memory cell array group 101 composed of the memory cell array IC 102 and the memory cell array IC 104 can have different size and bus width. For example,

if size and bus width of each memory cell array of the memory cell array IC 102 and the memory cell array IC 104 are 512M and 32 bits, size and bus width of the type of memory cell array group 101 can be 512M and 128 bits, or 1G and 64 bits. But, the present invention is not limited to size and bus width of the type of memory cell array group 101 composed of the memory cell array IC 102 and the memory cell array IC 104 being 512M and 128 bits, or 1G and 64 bits. In addition, if size and bus width of the memory cell array IC 102 are 512M and 64 bits and size and bus width of the memory cell array IC 104 are 1G and 64 bits, size and bus width of the type of memory cell array group 101 composed of the memory cell array IC 102 and the memory cell array IC 104 can be 1.5G and 128 bits.

[0035] Please refer to FIG. 7. FIG. 7 is a diagram illustrating each of the memory cell array IC 102 and the memory cell array IC 104 corresponding to a first seal ring and the logic unit corresponding to a second seal ring. As shown in FIG. 7, a circuit of each of the memory cell array IC 102 and the memory cell array IC 104 is surrounded by a first seal ring and a circuit of the logic unit 106 is surrounded by the second seal ring.

[0036] Please refer to FIG. 8. FIG. 8 is an explosion diagram illustrating a plurality of TSVs existing outside a first seal ring of each of the memory cell array ICs, where the plurality of TSVs are used for connecting to a power or a ground supply. But, the present invention is not limited to a plurality of TSVs existing outside a first seal ring of each memory cell array IC. That is to say, at least one TSV exists outside a first seal ring of each memory cell array IC. As shown in FIG. 8, relative positions and an amount of a plurality of TSVs existing outside a first seal ring of each memory cell array IC are the same. Because relative positions and an amount of a plurality of TSVs existing outside a first seal ring of each memory cell array IC are the same, when the memory cell array IC 102 and the memory cell array IC 104 are stacked each other, a metal fence 121 surrounding the memory cell array IC 102 and the memory cell array

IC 104 can be formed through a plurality of TSVs existing outside a first seal ring of each memory cell array IC (FIG. 8 only shows two sides of the metal fence 121), where the metal fence 121 has electromagnetic interference (EMI) shielding effect, better heat dissipation capability, and with better external noise isolation functions. In addition, because a plurality of TSVs existing outside a first seal ring of each memory cell array IC are used for connecting to the power or the ground supply, power or ground line areas within a first seal ring of each memory cell array IC for connecting to the power or the ground supply can be saved.

[0037] Please refer to FIG. 9. FIG. 9 is an explosion diagram illustrating the high speed memory chip module 100 further including a metal layer 122 and an insulation layer 124 when the high speed memory chip module 100 has the 3D structure. As shown in FIG. 9, the metal layer 122 is disposed over a topmost memory cell array of the memory cell array IC 102, and the insulation layer 124 is disposed between the metal layer 122 and the topmost memory cell array of the memory cell array IC 102, where the metal layer 122 can be electrically connected to the topmost memory cell array of the memory cell array IC 102 through at least one TSV of the insulation layer 124, and the metal layer 122, which can be a single piece or a slotted piece, covers more than 50% area of the topmost memory cell array of the memory cell array IC 102. In another embodiment, the metal layer can be connected to a power or a ground supply through a least one TSV as to perform better EMI shielding performance.

[0038] Please refer to FIG. 10. FIG. 10 is a cross-section diagram illustrating heat dissipation paths of the high speed memory chip module 100 in FIG. 9. As shown in FIG. 10, the high speed memory chip module 100 can utilize a plurality of TSVs existing outside first seal rings of the memory cell array IC 102 to upward dissipate heat through the metal layer 122, or utilize the metal fence 121 to dissipate heat to a substrate 114 or a motherboard 128 through a plurality of TSVs of the logic unit 106 and the substrate 114 (as

shown in arrows in FIG. 10).

[0039] Please refer to FIG. 11. FIG. 11 is a cross-section diagram illustrating heat dissipation paths of a high speed memory chip 900 according to another embodiment, where a difference between the high speed memory chip module 900 and the high speed memory chip module 100 in FIG. 10 is that a logic unit 106 of the high speed memory chip module 900 is stacked over the type of memory cell array group 101. A plurality of TSVs exist outside a first seal ring of each of the memory cell array IC 102 and the memory cell array IC 104, and the plurality of TSVs existing outside the second seal ring of the logic unit 106 are used for connecting to the power or the ground supply. But, the present invention is not limited to the plurality of TSVs existing either inside or outside of the second seal ring of the logic unit 106. That is to say, at least one TSV exists outside the second seal ring of the logic unit 106. As shown in FIG. 11, the metal layer 122 is disposed over the logic unit 106, and the insulation layer 124 is disposed between the metal layer 122 and the logic unit 106, where the metal layer 122 can be electrically connected to the logic unit 106 through at least one TSV of the insulation layer 124, and the metal layer 122 covers more than 50% area of the logic unit 106. In addition, as shown in FIG. 11, the high speed memory chip module 900 can utilize the plurality of TSVs existing outside the second seal ring of the logic unit 106 to upward dissipate heat through the metal layer 122, or utilize the metal fence 121 to dissipate heat to the motherboard 128 through the plurality of TSVs of the substrate 114 (as shown in arrows in FIG. 11). In addition, because the plurality of TSVs existing outside the second seal ring of the logic unit 106 are used for connecting to the power or the ground supply, power or ground supply line area within the second seal ring of the logic unit 106 for connecting to the power or the ground supply can be saved.

[0040] Please refer to FIG. 12. FIG. 12 is a top view illustrating an edge of the memory cell array IC 102 showing cracks during the assembly or package manufacturing process of the high speed memory

chip module 100 in FIG. 8. As shown in FIG. 12, when an edge of the memory cell array IC 102 shows cracks, the cracks will not impact the nominal function of the memory cell array IC and it will just make TSVs 130, 132 connected to the power short-circuit together, and TSVs 134, 136 connected to the ground supply short-circuit together. Thus, because the TSVs 130, 132 are short-circuit together, and the TSVs 134, 136 are short-circuit together, the metal fence 121 becomes wider, resulting in the EMI shielding effect, the heat dissipation capability, and the external noise isolation function of the metal fence 121 being enhanced. In addition, because the EMI shielding effect, the heat dissipation capability, and the external noise isolation function of the metal fence 121 are enhanced, the cracks in FIG. 12 will not impact the nominal function and as a result it can also increase the assembly or package manufacturing yield of the high speed memory chip module 100.

[0041] On the other hand, the conventional diamond-saw cutting method cannot cut the multiple memory cell array ICs into individual dies without creating the die-edge cracks. In another embodiment, to overcome the die-edge crack drawbacks of diamond-saw cutting method, the dicing or cutting method comprises at least a Laser cutting or dicing process step for at least one of the multiple memory cell array ICs. As an exemplary case, the multiple memory cell array ICs can be treated by the Laser cutting process step either before or after a conventional diamond-saw cutting steps to reduce the die-edge cracks and improve the manufacturing yield and final system device level reliability.

[0042] Please refer to FIG. 13. FIG. 13 is a diagram illustrating a electronics system device 1200 with a high speed memory chip module according to another embodiment. The electronics system device 1200 utilizes the PIP, the POP, or the SIP to integrate the ASIC (or SOC) processor 112, the memory cell array IC 102, the memory cell array IC 104, and the logic unit 106. Because the ASIC (or SOC) processor 112, the memory cell array IC 102, the memory cell array IC 104, and

the logic unit 106 are the same as the ASIC (or SOC) processor 112, the memory cell array IC 102, the memory cell array IC 104, and the logic unit 106 in FIG. 1, so further descriptions thereof are omitted for simplicity.

[0043] To sum up, the high speed memory chip module and the electronics system device with the high speed memory chip module provided by the present invention have advantages as follows: first, a signal swing of data transmitted through the first transmission bus and a signal swing of data transmitted through the second transmission bus can be varied with different memory standards or different semiconductor processes. So, the present invention not only has lower power consumption while operating, but also has higher transmission efficiency. Second, the present invention can utilize a plurality of TSVs outside a first seal ring of each memory cell array or a plurality of TSVs outside a second seal ring of the logic unit to form a metal fence, so the present invention has better EMI shielding effect, better heat dissipation capability, and an external noise isolation function based on the magnetic-electronic theory available today. Therefore, compared to the prior art, the present invention has lower power consumption, higher transmission efficiency, better EMI shielding effect, better heat dissipation capability, and with better external noise isolation functions.

[0044] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Electronic Patent Application Fee Transmittal				
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7	Abstract	1482202.PDF	25032 4e064f45fa9a74ec792a83b69c1a4060889920b7	no	1
Warnings:					
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8	Claims	1482200.PDF	35961 bb608a8413d3ee914a6bafbfdc5cb2f599ed1819	no	6
Warnings:					
Information:					
9	Specification	1482199.PDF	69913 5a4a2a58bd1152a0a671b96738345fc67ed2111b	no	15
Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	36691 b4d726e3b29b304d9d5ea112f87116591cafb8bbd	no	2
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