

DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.
2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.
3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as “MARC”) code and contain information such as a physical description of the material, metadata from the material’s publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item’s MARC record indicates the date of an item’s public availability.
5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book’s physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library’s collection, it is my experience

that an item's 008 field accurately indicates the date of an item's public availability.

6. I am familiar with the Internet Archive, a digital library accessible to the general public. Among other services that the Internet Archive makes available to the general public is the Wayback Machine, an online archive of the web. The Internet Archive's Wayback Machine service archives webpages as of a certain capture date to track changes in the web over time. The Internet Archive has been in operation as a nonprofit library since 1996 and has hosted the Wayback Machine service since its inception in 2001. During my time as a librarian, I frequently used the Internet Archive's Wayback Machine for research and instruction purposes. This includes teaching instructional classes on using the Wayback Machine to library patrons and using the Wayback Machine to research reference inquiries that require hard-to-find online resources. I consider the Internet Archive's recordskeeping to be as rigorous and detailed as other formal library recordskeeping practices such as MARC records, OCLC records and Dublin Core.

7. I have reviewed Exhibit EX1009, "Development of a 3-D Stack Package Using Silicon Interposer for High-Power Application" by Navas Khan, et al. as published in IEEE Transactions on Advanced Packaging February 2008.
8. Attached hereto as Appendix KHAN01 is a true and correct copy of the MARC record for IEEE Transactions on Advanced Packaging as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix KHAN01 accurately describes the title, publisher and ISSN number of IEEE Transactions on Advanced Packaging. The Showing Results field present on page 5 of this record indicates the library's collection includes the February 2008 issue of IEEE Transactions on Advanced Packaging containing "Development of a 3-D Stack Package Using Silicon Interposer for High-Power Application".
9. Attached hereto as Appendix KHAN02 is a true and correct copy of "Development of a 3-D Stack Package Using Silicon Interposer for High-Power Application" as published in IEEE Transactions on Advanced Packaging as held by the Penn State University Library. These scans were secured from the library's collection. In comparing Exhibit EX1009 to Appendix KHAN02, it is my determination that Exhibit EX1009 is a true

and correct copy of "Development of a 3-D Stack Package Using Silicon Interposer for High-Power Application" by Navas Khan, et al. as published in IEEE Transactions on Advanced Packaging.

10. The 008 field of the MARC record in Appendix KHAN01 indicates the date of record creation. The 008 field of Appendix KHAN01 indicates the Penn State University Library first acquired IEEE Transactions on Advanced Packaging as of June 21, 2000 and held the journal in perpetuity until the publication of "Development of a 3-D Stack Package Using Silicon Interposer for High-Power Application". Considering this information, it is my determination that IEEE Transactions on Advanced Packaging February 2008 and therefore "Development of a 3-D Stack Package Using Silicon Interposer for High-Power Application" was made available to the public shortly after its initial publication in February 2008.

11. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of \$200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

12.I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 1/30/2026

A handwritten signature in black ink, appearing to read 'June Ann Munford', with a stylized flourish at the end.

June Ann Munford

APPENDIX CV

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.
- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.
- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over \$400,000 and total assets of approximately \$1,300,000.

- Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.
- Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.
- Led the organization and digitization of the library's archival records.
- Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.
- Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013

Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

- Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.
- Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.
- Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013

Library Assistant, Hart Area Public Library

Hart, MI

- Responsible for verifying imported MARC records and original MARC cataloging for the local-level collection as well as the Michigan Electronic Library.
- Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter

- Treasurer, 2012

Library Of Michigan

- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014

- New Directors Conference Panel Member

Southwest Michigan Library Cooperative

- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008

Petoskey, MI

- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011

Nashville, TN

- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012

Fairbanks, AK

- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 • Fish & Richardson

Apple v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 • Erise IP

Implicit, LLC v. Netscout Systems, Inc (Case No. 2:18-cv-53-JRG)

2019 • Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Case No. IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (Case No. IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (Case No. IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (Case No. IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Case No. 4:21-cv-149-ALM)

2024 ● Willkie-Farr

Netflix, Inc. v. VideoLabs. Inc. (Case No. IPR2023-00628)

2024 ● Quinn Emanuel Urquhart & Sullivan

Purdue University v. Wolfsped (Case No. 1:21-CV-840)

2024 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00393)

2025 ● Perkins Coie

Amazon.com, Inc. v. Nokia Technologies Oy (Case No. IPR2024-00572)

2025 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00373)

Limited Case and Clientele History

Alston & Bird

- Ericsson

v. Collision Communications (Case No. IPR2022-01233)

- Nokia

v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

v. Roku Inc (Case No. IPR2022-00818)

Alavi & Anaipakos PLLC

- Stingray Group Inc. and Stingray Music USA, Inc.

v. Edwin A. Hernandez-Mondragon and Eglia Corp. (Case No. 1:24-cv-21226-RAR)

Arnold & Porter

- Ivantis

v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis
v. Cathx (Case No. 5:21-cv-00077-RWS)

Buchanan, Ingersoll & Rooney PC

- Google LLC, AT&T Service Inc., T Mobile USA Inc., Cellco Partnership, Ericsson Inc. & Nokia of America Corp.
v. KT Corp & Pegasus Wireless Innovation LLC (Case No. IPR2025-00293)

Deschert LLP

- Smaxtec Animal Care
v. ST Reproductive Technologies, LLC (Case No. IPR2024-00885)

Duane Morris

- Kangxi Communication Technologies
v. Skyworks Solutions Inc. (Case No. IPR2025-00373)
- Microsoft
v. Edge Networking Systems LLC (Case No. 1:24-cv-00215)

Erise I.P.

- Apple
v. Ericsson Inc. (Case No. IPR2022-00715)
v. Future Link Systems (Case No. IPRs 6317804, 6622108, 6807505, and 7917680)
v. INVT (Case No. 20-1881)
v. Navblazer LLC (Case No. IPR2020-01253)
v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

- v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)
- v. Telefonaktiebolaget LM Ericsson (Case No. IPR2022-00275)
- v. Theta IP, LLC (Case No. IPR2024-00818)
- v. THL Holding Company LLC (Case No. 1:23-cv-00548)

- Fanduel

- v. CGT (Case No. 19-1393)

- Garmin

- v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout

- v. Longhorn HD LLC (Case No. 2:20-cv-00349)
 - v. Implicit, LLC (Case No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC

- v. Bot M8 LLC (Case No. IPR2020-01288)
 - v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Tesla

- v. Charge Fusion Technologies LLC (Case No. IPR2025-00032)

- Unified Patents

- v. GE Video Compression (Case No. 2:19-cv-248)

Fish & Richardson

- Apple

- v. AliveCor (Case No. 3:21-cv-03958)
 - v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)
 - v. Koss Corporation (Case No. IPR2021-00305)

- v. Masimo (Case No. IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)
- v. Neonode (Case No. 21-cv-08872-EMC)
- v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
- v. Resonant Sys. (Case No. 7:23-cv-00077-ADA)
- AsusTek Computer Inc.
 - v. Videolabs, Inc. (Case No. 22-CV-00720-ADA)
- Dell
 - v. Neo Wireless (Case No. IPR2022-00616)
- Dish Network
 - v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)
 - v. Entropic Communications LLC (Case No. IPR2024-00393)
 - v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)
 - v. TQ Delta LLC (Case No. 18-1798)
- Evapco Dry Cooling
 - v. SPG Dry Cooling (Case No. IPR2021-00688)
- Genetec
 - v. Sensormatic Electronics (Case No. 1:20-CV-00760)
- Huawei
 - v. Bell Northern Research LLC (Case No. IPR2019-01174)
- Kianxis
 - v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics
 - v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)
- MediaTek
 - v. MOSAID (Case No. IPR2024-00718)
- Metaswitch
 - v. Sonus Networks (Case No. IPR2018-01719)
- Microsoft
 - v. Throughputer Inc (Case No. IPR2022-00757)
- Mom Enterprises
 - v. Ddrops Company (Case No. 1:22-cv-00332)
- MLC Intellectual Property
 - v. MicronTech (Case No. 3:14-cv-03657-SI)
- Nearmap Inc
 - v. EagleView Technologies (Case No. IPR2022-01009)
- Neuroderm Ltd.
 - v. Abbvie, Inc (Case No. PGR2022-00040)
- Posco Co Ltd.
 - v. Pascal Drillet et al. (Case No. IPR2025-00370)
- Realtek Semiconductor
 - v. Future Link (Case No. IPR2021-01182)

- Quectel
 - v. Koninklijke Philips (Case No. 1:20-cv-01710)
- Samsung
 - v. Aire Technology (Case No. IPR2022-00877)
 - v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)
 - v. Communication Technologies Inc (Case No. IPR2022-01221)
 - v. Jawbone Innovations (Case No. IPR2022-00865)
 - v. MemoryWeb LLC (Case No. IPR2022-00885)
 - v. Dodots Licensing Solutions (Case No. IPR2023-00701)
 - v. Telefonaktiebolaget LM Ericsson (Case No. IPR2021-00615)
- Texas Instruments
 - v. Vantage Micro LLC (Case No. IPR2020-01261)
- Xilinx
 - v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Goodwin Proctor

- Intel
 - v. Proxense, LLC (Case No. 6:24-cv-00283)
- Samsung Electronics
 - v. Mobile Data Technologies (Case No. 2:24-cv-00435)
- Taiwan Semiconductor Manufacturing Company Ltd.
 - v. Advanced Integrated Circuit Process LLC (Case No. 2:24-cv-00623)

Groombridge Wu

- Nearmap

v. Eagle View Technologies Inc. and Pictometry International Corp. (Case No. 2:21-cv-00283-TS-DAO)

Irell & Manella

- Curium

Latham & Watkins LLP

- Apple

v. Advanced Coding Research LLC

Leydig, Voit & Mayer, Ltd.

- Public Availability Consultancy

O'Melveny & Myers

- Apple

v. Maxell (Case No. 5:19-cv-00036-RWS)

- Disney Media & Entertainment Distribution LLC

v. Digital Media Technology Holdings, LLC (Case No. 2:22-cv-01642)

- Micron Technology Inc.

v. Besang Inc (Case No. IPR2023-00900)

- Samsung

v. Daedalus Prime LLC (1335 Investigation)

Perkins-Coie

- Amazon
 - v. Nokia (Case No. IPR2024-00847 and IPR2024-00848)
 - v. Nokia Technologies Oy (Case No. IPR2024-00572)
- Heru Industries
 - v. The UAB Research Foundation (Case No. IPR2022-01148)
- Intel Corporation
 - v. BeSang Inc. (Case No. IPR2023-00991)
 - v. BitMICRO (Case No. 5:23-cv-00625)
 - v. Telefonaktiebolaget L M Ericsson (Case No. IPR2024-00610)
- Realtek Semiconductor
 - v. Future Link (Case No. IPR2021-01182)
- r-pac
 - v. Adasa, Inc. (Case No. 1:2024cv06102)
- Twitter Inc
 - v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)
- TCL Industries
 - v. Koninklijke Philips NV (Case No. IPR2021-00495, IPR2021-00496 and IPR2021-00497)
- VusionGroup
 - v. Hanshow (Case No. IPR2024-00857)

Pillsbury Winthrop Shaw Pittman

- Intel

- v. FG SRC LLC (Case No. 6:20-cv-00315)

- Gravel Rating Systems

- v. Costco (Case No. 4:21-cv-149)

- v. Lowe's Home Centers (Case No. 4:21-cv-150)

- v. T-Mobile USA (Case No. 4:21-cv-152)

- v. Kohl's Inc. (Case No. 4:21-cv-258)

- v. Under Armor (Case No. 4:21-cv-356)

Quinn Emanuel

- Exact Sciences Corporation

- v. Geneoscopy, Inc. (Case No. IPR2024-00459 and IPR2024-1330)

- ServiceNow, Inc.

- v. InQusient, Inc. (Case No. 22-900-CJB)

- Wolfsped

- v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Sheppard, Mullin, Richter & Hampton LLP

- Advanced Micro Devices, Inc and Pensando Systems, Inc.

- v. Concurrent Ventures LLC and Xtreamedge, Inc. (Case No. IPR2025-00478)

- Cadence Design Systems Inc.

- v. Semiconductor Design Technologies (Case No. 3:23-cv-01001)

Shook, Hardy & Bacon LLP

- HP Inc.

v. Universal Connectivity Technologies (Case No. 1:23-cv-01177)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

Wilmer, Cutler, Pickering, Hale and Dorr

- Apple

v. Shunock (Case No. 1:23-cv-08598)

- Quest Diagnostics Inc., Haystack Oncology Inc. and Haystack Oncology GmbH

v. Natera, Inc. (Case No. 1:23-cv-08598)

- Roche Diabetes, Inc.

v. Trividia Health, Inc. (Case No. 1:24-cv-00668)

Willkie, Farr & Gallagher LLP

- Lenovo, Dell, HP

v. Universal Connectivity Technologies Inc. (Case No. 2:2023cv00449)

- Neurent

v. The Foundry, LLC (Case No. IPR2024-00669)

- Netflix, Inc.

v. VideoLabs, Inc. (Case No. IPR2023-00628)

APPENDIX KHAN01



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019 a| DO NOT EDIT this 360 MARC RECORD

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035 a| (WaSeSS)ssj0014842

037 b| IEEE Service Center, 445 Hoes Lane, P.O. Box 1331 Piscataway, NJ 08855-1331

040 a| NTD b| eng e| pn c| NTD d| OCLCQ d| NSD d| U9S d| OCLCQ d| HNK d| UKMGB d| DLC d| OCLCQ d| UMC d| OCLCF d| OCLCQ d| OCLCA d| AU@ d| NJT d| OCLCO d| OCL d| OCLCQ d| U3W d| OCLCQ d| OCLCL d| WaSeSS

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082 1 0 a| 621.3 2 | 13 1 | https://id.oclc.org/worldcat/ddc/E3tbg7YcX8rFmFjd3wHMgmjw3v

130 0 a| IEEE transactions on advanced packaging (Online)

210 0 a| IEEE trans. adv. packaging b| (Online)

222 0 a| IEEE transactions on advanced packaging b| (Online)

245 1 0 a| IEEE transactions on advanced packaging h| [electronic resource] : b| a publication of the IEEE Components, Packaging, and Manufacturing Technology Society and the Lasers and Electro Optics Society.

246 3 0 a| Transactions on advanced packaging

246 3 0 a| Advanced packaging

246 3 a| Institute of Electrical and Electronics Engineers transactions on advanced packaging

246 1 i| Available from some providers with title: a| Advanced Packaging, IEEE Transactions on

260 a| Piscataway, NJ : b| Institute of Electrical and Electronics Engineers, c| 1999-2010.

310 a| Quarterly

362 0 a| Vol. 22, no. 1 (Feb. 1999)-v. 33, no. 4 (Nov. 2010).

500 a| Title from IEEEExplore homepage (viewed June 21, 2000).

500 a| Merged with: IEEE transactions on components and packaging technologies (Online), and: IEEE transactions on electronics packaging manufacturing (Online), to form: IEEE transactions on components, packaging, and manufacturing technology.

538 a| Mode of access: World Wide Web.

650 0 a| Electronic packaging v| Periodicals.

650 0 a| Electronic industries v| Periodicals.

650 0 a| Electric apparatus and appliances v| Periodicals.

655 0 a| Electronic journals.

710 2 a| Components, Packaging & Manufacturing Technology Society. 1 | https://id.oclc.org/worldcat/entity/E39QH7JmpbhGgyjdbbxkJMgT

710 2 a| Lasers and Electro-optics Society (Institute of Electrical and Electronics Engineers) 1 | https://id.oclc.org/worldcat/entity/E39QQPVp7Pp6mg463FMrhXbm9t.

710 2 a| Institute of Electrical and Electronics Engineers. 1 | https://id.oclc.org/worldcat/entity/E39QH7JmppbjgFY6j8mDDMWwRg.

776 0 8 i| Print version: t| IEEE transactions on advanced packaging x| 1521-3323 w| (DLC) 99111625 w| (OCoLC)39742480

780 0 0 t| IEEE transactions on components, packaging, and manufacturing technology. Part B, Advanced packaging (Online) x| 1558-3686 w| (DLC) 2005215261 w| (OCoLC)44452804

785 0 7 t| IEEE transactions on components and packaging technologies (Online) x| 1557-9972 w| (DLC) 2005215203 w| (OCoLC)44466312

785 0 7 t| IEEE transactions on electronics packaging manufacturing (Online) x| 1558-0822 w| (DLC) 2005215258 w| (OCoLC)44507293

785 0 7 t| IEEE transactions on components, packaging, and manufacturing technology x| 2156-3985 w| (DLC) 2010204546 w| (OCoLC)646186284

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Uniform Title	IEEE transactions on advanced packaging (Online)
Additional Titles	IEEE trans. adv. packaging (Online), Transactions on advanced packaging, Advanced packaging, Institute of Electrical and Electronics Engineers transactions on advanced packaging, and Available from some providers with title: Advanced Packaging, IEEE Transactions on
Published	Piscataway, NJ : Institute of Electrical and Electronics Engineers, 1999-2010.
Additional Creators	Components, Packaging & Manufacturing Technology Society , Lasers and Electro-optics Society (Institute of Electrical and Electronics Engineers) , and Institute of Electrical and Electronics Engineers

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[IEEE transactions on components, packaging, and manufacturing technology. Part B, Advanced packaging \(Online\)](#)

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[IEEE transactions on electronics packaging manufacturing \(Online\)](#)
[IEEE transactions on components, packaging, and manufacturing technology](#)

Dates of Publication and/or Sequential Designation

Vol. 22, no. 1 (Feb. 1999)-v. 33, no. 4 (Nov. 2010).

Subject(s)

[Electronic packaging—Periodicals](#)
[Electronic industries—Periodicals](#)
[Electric apparatus and appliances—Periodicals](#)

Genre(s)

[Electronic journals](#)

ISSN

1557-9980

Publication Frequency

Quarterly

Note

Title from IEEEExplore homepage (viewed June 21, 2000).
Merged with: IEEE transactions on components and packaging technologies (Online), and: IEEE transactions on electronics packaging manufacturing (Online), to form: IEEE transactions on components, packaging, and manufacturing technology.

Technical Details

Mode of access: World Wide Web.





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APPENDIX KHAN02

Development of 3-D Stack Package Using Silicon Interposer for High-Power Application

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Abstract

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Abstract:

Stacking of many functional chips in a 3-D stack package leads to high heat dissipation. Therefore, a new platform technology is required to assemble chips vertically and remove the heat effectively. A 3-D stacked package with silicon interposers was developed to integrate one ASIC and two memory chips in a package. Electrical connections in the silicon interposer were formed by through silicon via. Silicon interposer has much high thermal conductivity than organic interposer, therefore the package thermal resistance is lower. Thermal performances of the 3-D package were analyzed and thermal enhancements like thermal via, thermal bridging were evaluated. The designed package showed 5 times lesser thermal resistance compared to a similar package with organic substrate. An additional silicon heat spreader was designed and attached to the package for high power application. Thermal analysis was performed to optimize package thermal performances and experimental validation was carried out. The designed 3-D stack package is suitable for 20 W application.

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I. Introduction

Microelectronics packaging is driven by the continuous increase in demands for smaller, faster, and cheaper products with enhanced performances. Flip-chip technology and multichip packaging are developed to meet the market needs. In recent years, the concept of multichip packaging is evolved into system-in-a-package (SiP) [1]. Major advantages of SiP are that different types and generations of devices are assembled in a single package, providing high flexibility for systems designers. One way of integrating more devices into a smaller volume is 3-D packaging techniques by stacking the chips vertically. The 3-D packaging... stacking and package stacking. In chip stacking technology, dice are... advantages of increased die combination and flexibility. Disadvantages are loop snaps and testability. In package stacking, packages are stacked one over the other to over come the chip stacking limitations [2]. The 3-D packaging is preferred for many communications and computing system, because of its smaller footprint, shorter signal routing, reduced wiring density, etc. However, special considerations are

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Development of 3-D Stack Package Using Silicon Interposer for High-Power Application

Navas Khan, Seung Wook Yoon, Akella G. K. Viswanath, V. P. Ganesh, Ranganathan Nagarajan, *Member, IEEE*, David Witorsa, Samuel Lim, and Kripesh Vaidyanathan

Abstract—Stacking of many functional chips in a 3-D stack package leads to high heat dissipation. Therefore, a new platform technology is required to assemble chips vertically and remove the heat effectively. A 3-D stacked package with silicon interposers was developed to integrate one ASIC and two memory chips in a package. Electrical connections in the silicon interposer were formed by through silicon via. Silicon interposer has much high thermal conductivity than organic interposer, therefore the package thermal resistance is lower. Thermal performances of the 3-D package were analyzed and thermal enhancements like thermal via, thermal bridging were evaluated. The designed package showed 5 times lesser thermal resistance compared to a similar package with organic substrate. An additional silicon heat spreader was designed and attached to the package for high power application. Thermal analysis was performed to optimize package thermal performances and experimental validation was carried out. The designed 3-D stack package is suitable for 20 W application.

Index Terms—High-power 3-D package design, silicon carrier, through silicon via.

I. INTRODUCTION

MICROELECTRONICS packaging is driven by the continuous increase in demands for smaller, faster, and cheaper products with enhanced performances. Flip-chip technology and multichip packaging are developed to meet the market needs. In recent years, the concept of multichip packaging is evolved into system-in-a-package (SiP) [1]. Major advantages of SiP are that different types and generations of devices are assembled in a single package, providing high flexibility for systems designers. One way of integrating more devices into a smaller volume is 3-D packaging techniques by stacking the chips vertically. The 3-D packaging can be broadly classified as chip stacking and package stacking. In chip stacking technology, dice are stacked. This technology has advantages of increased die combination and flexibility. Disadvantages are loop snaps and testability. In package stacking, packages are stacked one over the other to overcome the chip stacking limitations [2]. The 3-D packaging is preferred for many communications and computing system, because of its smaller footprint, shorter signal routing, reduced wiring density,

etc. However, special considerations are required in stacking different function devices due to differences in production and testing methodologies.

In this paper, a platform technology for stacking processor/logic and memory chips is reported. The availability of fully tested memory in die form is crucial for the 3-D stack package yield. A single bad die in a 3-D stack package can have a significant impact on overall cost. Therefore, package-on-package (PoP) is preferred for such application. The memory and logic packages can be easily combined based on system design needs with lower cost by PoP concept. However, the reduction in system volume comes at the expense of difficulty in heat dissipation. Therefore, 3-D stack package design needs better thermal design approach to tackle the multiple heat sources in a vertically stacked structure. Typically, the logic die is housed in the lower stack of the 3-D package for shorter electrical path. The heat from the die is mainly conducted through the solder bumps. Smaller the bump size and number, higher the heat flow resistance. Therefore, heat removal from the inner-stack may require parallel heat flow path and high thermally conductive interposers [3]. Also thinner interposers and dice reduce package junction-to-air thermal resistance. A new thermal management approach is needed to dissipate high power in small volumes [4]. In this work, a 3-D stack package was developed with silicon carriers for stacking one ASIC chip dissipating 20 W and two memory chips. The high-power ASIC chip was mounted on the lower stack, direct access to the external heat sink is difficult. Thermal design approach for the 3-D stack package to meet the 20 W heat dissipation with air cooling method was studied in this work. Thermal performance of the 3-D package was evaluated and thermal enhancements methods were reported.

II. THREE-DIMENSIONAL PACKAGE CONSTRUCTION

A schematic of the 3-D stack package developed for this work is shown in Fig. 1. The 3-D package overall dimensions are 13.5 mm × 13.5 mm × 1.4 mm, having 276 peripheral I/O. Carrier 1 is designed to mount a flip-chip (Chip 1) representing an ASIC device. The chip 1 dimensions are 8.5 mm × 8.5 mm × 0.1 mm with 1000 I/O at a bump pitch of 0.25 mm. Carrier 2 is designed to mount two memory chips, having overall dimensions of 4.5 mm × 9.0 mm × 0.1 mm and 80 I/O. The two silicon carriers were stacked one over other using 8 mil solder balls. Electrical connections through the silicon carrier were formed by through silicon via (TSV) technology. Some of the advantages of using silicon for the interposer are low thermo-mechanical stresses, finer line width and spacing, wafer level batch fabrication, high thermal conductivity.

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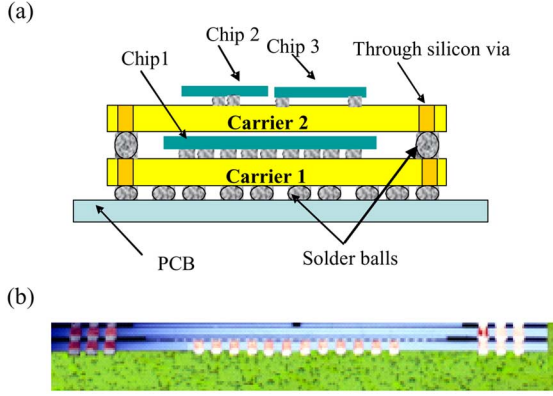


Fig. 1. (a) Schematic of 3-D stack package. (b) Cross section of 3-D stack package.

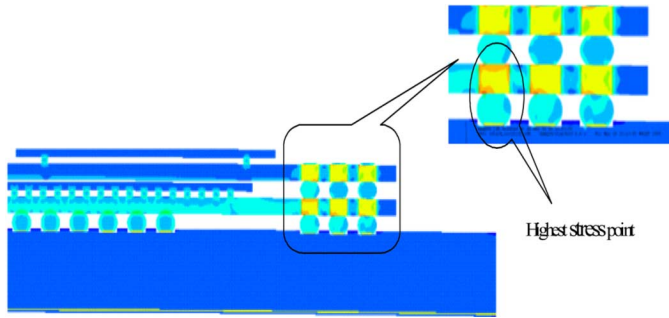


Fig. 2. Package Von mises stress contour.

III. STRUCTURAL DESIGN

Structural parameters like carrier thickness, chip thickness and via diameter were analyzed for the minimum thermo-mechanical stress. The finite element (FE) analysis was performed using ABAQUS [5]. Four node plane strain quadrilateral elements and reduced integration were used for the thermo-mechanical analysis. The stress free temperature state was taken as 125 °C, highest temperature of thermal cycle test [6]. The package thermal stresses were analyzed for the temperature loading of 125 °C to -40 °C. The carrier thickness of 450 μm and 200 μm were analyzed and package stress and warpage were compared. Thinner carrier resulted in 15% reduction of Von Mises stress, 28% reduction of shear stress, but the package warpage is 16% higher than thicker carrier. Fig. 2 shows the Von Mises stress contour and critical location in the package. The maximum Von Mises stress in the package with 450 μm carrier is observed at the interface between TSV and solder ball at the bottom carrier. But for the thinner carrier, the maximum stress concentration is shifted to the interface between solder ball and printed circuit board (PCB) copper pad. Thicker carrier is found suitable for low warpage package design. Also thicker carrier is required for better thermal performance. Thicker the carrier wafer, it is easier to handle during the via formation and metallization processes. All the analyses were performed without any underfill between carrier 1 and the PCB.

Large coefficient of thermal expansion (CTE) mismatch between the copper via and the silicon carrier is a concern for the reliability of the TSV interconnections. Interfacial stress be-

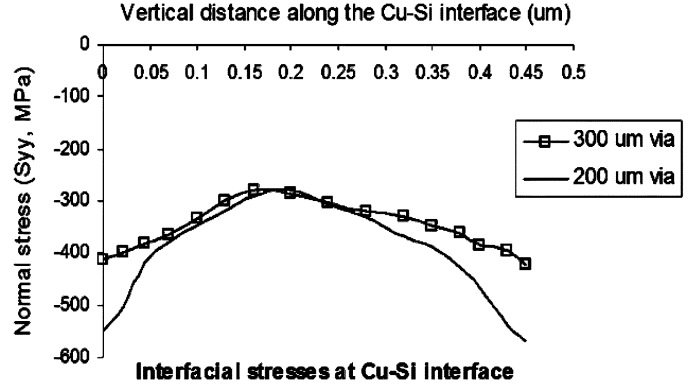


Fig. 3. Interfacial stress distribution in the via.

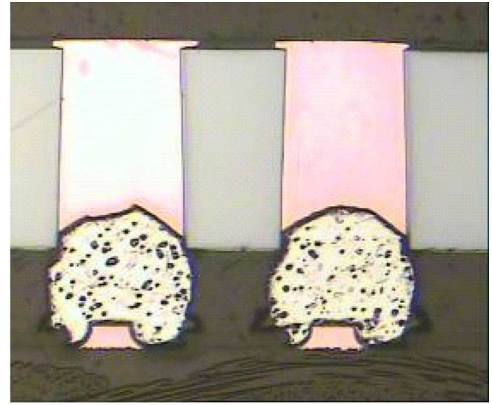


Fig. 4. Cross section of TSV.

tween the via and the silicon carrier was analyzed. Carrier with 200 μm via diameter has 5.5% higher Von Mises stress and 35% higher maximum shear stress compared to a carrier with 300 μm diameter via. Therefore 300 μm via was chosen for the package design. Fig. 3 shows the interfacial stress distribution along the carrier thickness.

Based on the structural optimization, 450- μm -thick silicon carrier with 300 μm diameter via was fabricated for the package assembly. 8-in silicon wafer was used for the carrier fabrication. The TSV was formed by etching blind via by deep reactive ion etching to a depth of 450 μm . Then the wafer was thinned to 450 μm . An insulation layer and a barrier layer of SiO₂ and Si₃N₄ were deposited on the through hole wafer. Then the wafer was attached onto a support wafer using dry film and lamination process. The support wafer was deposited with Cu seed layer for electroplating. All the through holes in the wafer were filled with copper by bottom-up electroplating process. Then the wafer was separated from the support wafer. Two metal layers for signal/power routing were deposited on topside of the carrier wafer with SiO₂ as dielectric layer. The bottom side of the copper via was plated with eNiAu for solder ball attachment. Fig. 4 shows a cross section of the TSV carrier with solder ball.

IV. THERMAL DESIGN

Three-dimensional package thermal design is a challenge for high-power application. Detailed thermal analyzes was con-

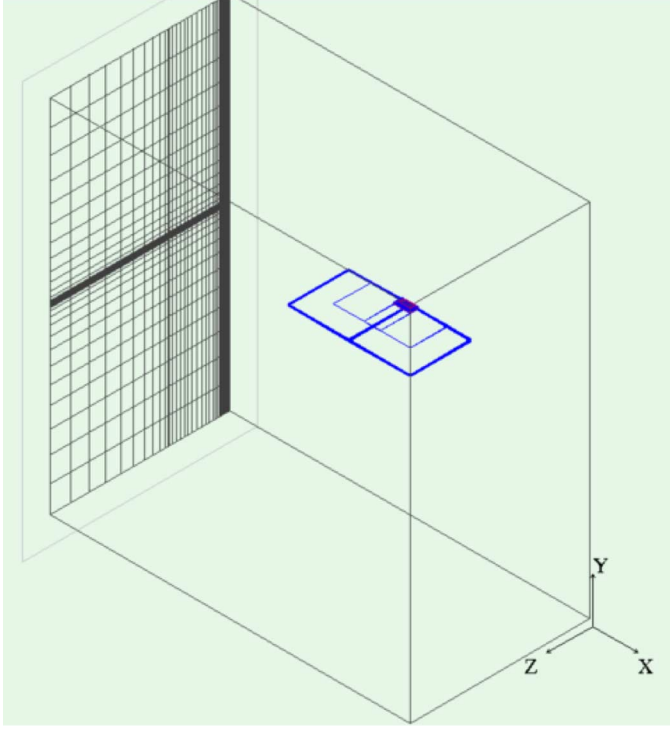


Fig. 5. Thermal model of the package.

ducted in this study to optimize the package design for 20 W application. First, the package thermal performance without any external heat sink was extracted and validated. Thermal analysis was performed with 0.8 W heat load in chip 1 and 0.1 W heat load in chip 2 & 3. Flotherm [7] was used for all the thermal analysis in this study. All the solder balls and solder bumps were modeled as individual block for better analysis accuracy. The metal layers on the carriers were modeled using collapsed cuboid having thermal conductivity equivalent to 10% metal coverage on the carrier surface. A half model was developed and appropriate symmetry conditions were assigned. A four layer PCB of size 101.5 mm × 101.5 mm × 1.6 mm was modeled along with the package representing test board. The test board details are taken from the JEDEC standard JESD 51-9. The test board top copper traces were modeled with different thermal conductivity equivalent to the percentage area average with in and around the package footprint. Fig. 5 shows thermal model of the 3-D package. Overall dimension for the computational domain is 300 mm × 150 mm × 300 mm along X, Y, and Z, respectively. Finer grids were defined near the package and PCB surfaces to capture the natural convection boundary layer. The numbers of computational grids were 168 × 51 × 90 along X, Y, and Z directions. Grid dependency of the simulation result was verified by rerunning the model with grids 1.5 times higher than the base model. The outer faces of the computational domain were attached with ambient condition of 25 °C. The airflow with in the solution domain was assumed to be laminar. Radiation heat transfer form the PCB and package surface was taken into account. All the material properties used for the analysis is given in Table I.

TABLE I
MATERIAL PROPERTIES

Element	Thermal conductivity (W/mK)
Carrier and Chip	117
Solder ball and Solder bump	50
Via in silicon carrier	390
PCB dielectric	0.8 in plane 0.3 through plane
PCB top layer traces	42.9
PCB top layer ball pads	135
Thermal adhesive	2

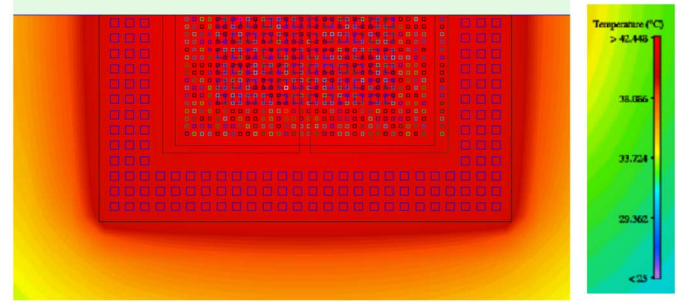


Fig. 6. Temperature distribution in the silicon carrier.

There is no standard for 3-D package thermal performance evaluation. Therefore, Chip 1 to ambient thermal resistance ($Ja1'$) of the package is taken as measure of merit for this study.

$$Ja1' = \frac{\text{Chip 1 temperature} - \text{Ambient temperature}}{\text{Total power}}.$$

Chip1 is mostly the high power dissipating component in the package, hence $Ja1'$ is used for the design evaluation. The analysis was run with 1 W of total heat dissipation. Maximum temperature of Chip1 is 42.4 °C and $Ja1'$ is 17.4 °C/W. Thermal resistance of the 3-D package with silicon carrier is considerable low and the 3-D packaging technology with silicon carrier is promising for high-power application. By virtue of the carrier high thermal conductivity, heat from the chip 1 is spread uniformly and it offers low resistance path to the PCB. Fig. 6 shows the temperature distribution in carrier 1, which is very uniform and the temperature variation from the carrier center to edge is less than 2 °C. A small portion of the heat generated in the package is dissipated from the package surfaces, but major portion of the heat is dissipated from the PCB. Thermal analysis result shows that 96% of the package heat is dissipated through the PCB. The package thermal resistance with 200-μm-thick carrier was also analyzed and found to be 18.7 °C/W.

Thermal performance of the package with organic substrate instead of Silicon carrier was analyzed for a comparison purpose. The organic substrate thermal conductivity of is much lower than Silicon. We analyzed thermal resistance of a 3-D package with organics substrate having similar dimensions as explained in the earlier section. The organic material thermal conductivity was taken as 0.2 W/mK. Substrate via were modeled as block having anisotropic thermal conductivity of 47 W/mK in plane, 88 W/mK through plane. The modeling

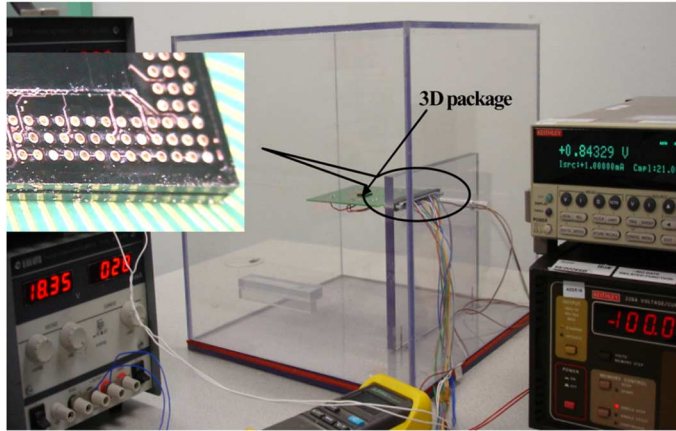


Fig. 7. Experimental setup for Jb1' characterization.

approach, simulation boundary conditions were similar to the case explained earlier. Maximum temperature of chip1 temperature with organic substrate is 114.5 °C and Jb1' is 89.5 °C/W. Heat flow analysis in the package shows that only 84% of the package heat is dissipated through the PCB. In case of silicon substrate, 96% of the heat is dissipated through the PCB. Thermal simulation was performed with additional 144 thermal via in the organic substrate. The thermal via were placed at the bottom stack substrate directly below the chip1. The maximum temperature of chip 1 with additional thermal via is 109.1 °C, which is marginally lower than the case without via. Our thermal analysis clearly shows that, 3-D package with laminate substrate has higher package thermal resistance and the substrate thermal conductivity is the main contributor. The 3-D package with silicon carrier showed 5 times lower thermal resistance compared to the organic carrier for the same heat dissipation.

V. NATURAL CONVECTION PACKAGE CHARACTERIZATION

Three-dimensional package with silicon carrier was developed for thermal characterization and model validation. Thermal characterization requires a test die with heater and temperature sensor. It was difficult to procure test die similar to the die dimensions used in this study. We used a test die available in our laboratory, which has dimensions of 8.9 mm × 8.9 mm. The test die was bumped and thinned to 100 μm. Each carrier was assembled with test die. The two carriers were stacked one over other using SnPb eutectic solder balls. The 3-D package was assembled onto a four-layer test board. Fig. 7 shows the assembled board mounted horizontally inside a closed box as defined in JESD 51-2 for natural convection thermal characterization. The test chip in carrier 1 and carrier 2 were connected to a separate power source and supplied with 0.8 W and 0.2 W, respectively. Four such packages were characterized and average of maximum temperature of chip 1 is compared. The pad design of the test die allowed us to bump only 104 peripheral bumps. But our original chip 1 design is a full array of 1000 bumps. Therefore a new thermal model was built with 104 solder bumps on chip 1 and chip 2. The measurement result is compared with the new model result for the validation purpose. Measurement and simulation data

TABLE II
MODEL VALIDATION RESULTS FOR NATURAL COOLING

Rise in chip 1 temperature above ambient by measurement	Rise in chip 1 temperature above ambient by simulation	% error with respect to measurement
24.2 °C	22.4	7.4%

are compared in Table II. The simulation result is found to have good agreement with measurement result, which validates our modeling approach and boundary conditions.

VI. THERMAL DESIGN APPROACH FOR HIGH-POWER APPLICATION

Our objective was to design a 3-D package for chip 1 dissipating 20 W and chip 2 & 3 dissipating 1 W heat. The 3-D package with silicon carrier was found to have lower thermal resistance compared to one having organic substrate. We optimized further the package design to meet our target. Three types of thermal enhancements techniques were studied in this work viz. thermal via, thermal bridging using polymer adhesive and heat spreader. Thermal analyses were performed using the same model with additional thermal enhancements. Thermal analysis was carried out with a heat load of 2.8 W in chip1 and 0.1 W each in chip 2 and chip 3. First, the package thermal performance was studied with 144 thermal via in the carrier 1. Maximum temperature of chip 1 with thermal via is 77.5 °C as compared to 78.5 °C without thermal via. Silicon has good thermal conductivity, therefore thermal via in the silicon carrier is not effective in reducing the package thermal resistance.

Second thermal enhancement was done by bridging the gap between chip 1 and carrier 2 using thermal adhesive. Polymer based thermal adhesive is commonly used for the packaging application. We analyzed package thermal performance with polymer adhesive having thermal conductivity of 2 W/mK, which thermally bridges the chip 1 and carrier 2. The maximum temperature of chip 1 with thermal adhesive is found to be 73.9°C. The thermal bridging helps to dissipate 45% of the chip 1 heat through the carrier 2 by forming a parallel heat flow path.

The above two thermal enhancement techniques improves the chip 1 heat dissipation limits, however it is not meeting our target value of 20 W. It is important to understand the package heat flow path and thermal resistance from chip1 to PCB and chip1 to package casing to design suitable cooling solution. Thermal model was developed to estimate chip 1 to PCB thermal resistance. A ring type cold plate of 40 mm × 40 mm was modeled around the package with a constant temperature boundary condition and assumed good thermal contact with the PCB. Chip1 to PCB thermal resistance (Jb1') was calculated based on increase rise in chip1 temperature above the cold plate temperature for the total package heat dissipation. The package Jb1' is found to be 9.2 °C/W. The heat path from chip 1 to PCB offering high resistance and any cooling solution on the PCB will not be effective. An alternate method of cooling the chip 1 was evaluated by attaching a heat sink on the package top surface. A flat cold plate of dimensions 50 mm × 50 mm × 2 mm was modeled on top of the chip 2 and chip 3 with a constant

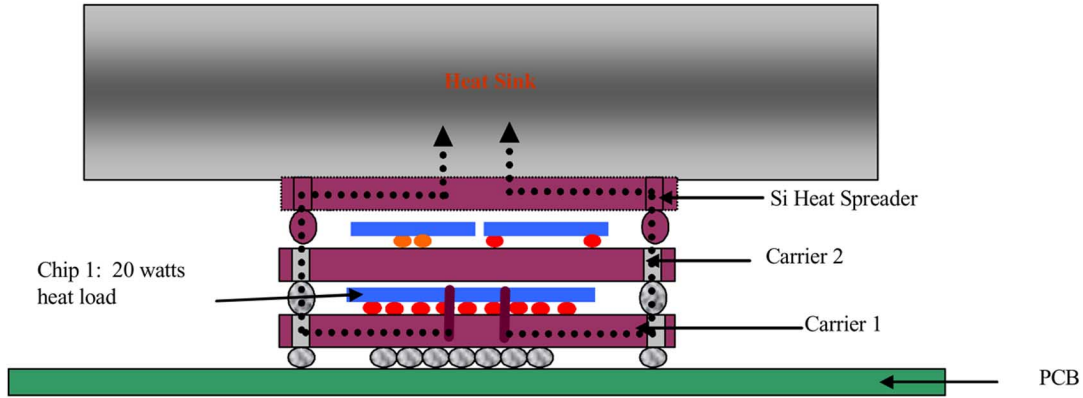


Fig. 8. Schematic of 3-D package with Silicon heat spreader.

temperature boundary condition. The chip 1 to case thermal resistance ($Jc1'$) was calculated based on increase rise in chip1 temperature above the cold plate temperature for the total heat dissipation. $Jc1'$ for the package is found to be 4.7°C/W , which is still high for the 20 W heat load. The heat path from chip 1 to the package case is smaller, therefore it was decided to improve further the design with additional heat spreader. A silicon heat spreader was attached to the carrier 2 using 276 peripheral solders balls. The heat spreader dimensions are $13.5\text{ mm} \times 13.5\text{ mm} \times 0.4\text{ mm}$. The heat spreader provides good thermal connectivity to carrier 1, carrier 2 with the external heat sink. Fig. 8 shows a schematic of the package with silicon heat spreader and external heat sink. The modeling approach, material properties are given in the previous section. Heat source of 20 W attached to chip1 and 0.5 W each to chip 2 & 3. Many types of air cooled heat sinks are available in the market, but the choice heat sink is depending on the end user application. Therefore, a flat plate of dimensions $50\text{ mm} \times 50\text{ mm} \times 2\text{ mm}$ was modeled with a constant temperature boundary condition to represent the external heat sink. A thin layer $50\text{-}\mu\text{m}$ -thick thermal adhesive was modeled at the interface between the silicon heat spreader and the cold plate. Maximum temperature of chip 1 with this thermal enhancement is 73.9°C . We also computed the chip 1 temperature using copper heat spreader instead of silicon heat spreader, which is found to be 72.5°C .

Silicon heat spreader is preferred for our package design. If the chip and heat spreader material is same and CTE mismatch is avoided. Fig. 9 shows temperature distribution of the package with 21 W heat dissipation. The heat flow analysis shows that 95% of chip 1 heat is dissipated through external heat sink. The 3-D package design with silicon heat spreader and external heat sink is found meeting our requirements.

VII. MODEL VALIDATION

A two-stack package with silicon heat spreader was developed and assembled for model validation. Each stack was assembled with $8.9\text{ mm} \times 8.9\text{ mm}$ thermal test chip similar to the package assembled for thermal characterization in natural convection. The package was mounted on a four layer PCB. The package was tested with a cold plate by attaching it with the heat spreader. A thin layer of thermal grease was applied at the interface between the cold plate and the package. The package

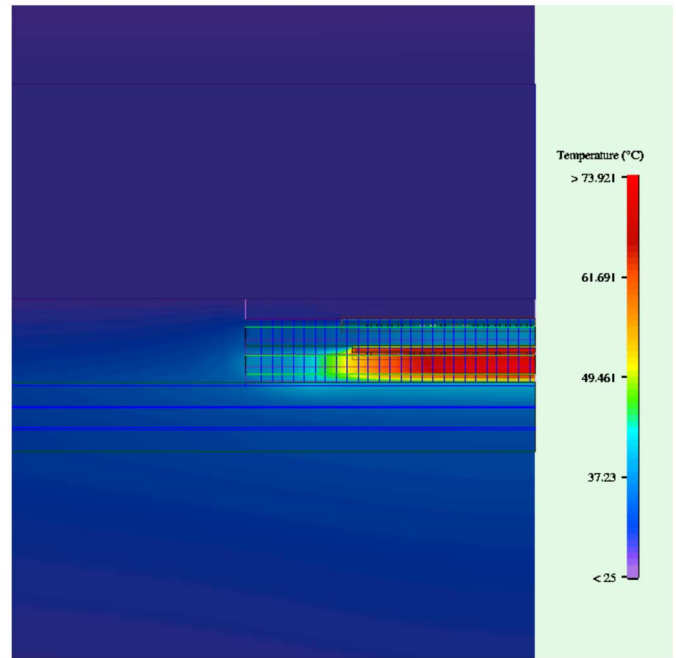


Fig. 9. Temperature distribution with silicon heat spreader and cold plate.

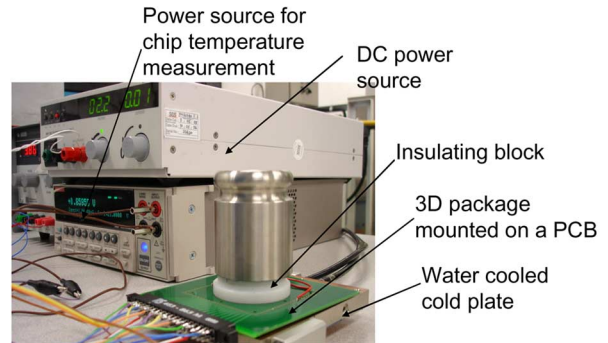


Fig. 10. Experimental setup for model validation.

was pressed against the cold plate using 1 Kg of dead weight. Fig. 10 shows the photograph of the experimental setup.

The thermal test chip has only 104 peripheral bumps, as compared to a full array of 1000 bumps in the designed package. Fewer solder bumps in the test chip allowed us to test the package

TABLE III
MODEL VALIDATION RESULTS

Chip 1 power	Rise in chip1 temperature by measurement	Rise in chip1 temperature by simulation	% error with respect to measurement
6.4 W	53.8 °C	48.4 °C	10%

only with 6.4 W in chip 1. A separate power source was connected to chip 2 and supplied with 1 W of power. The chip 1 and cold plate temperatures were recorded at steady state measurement condition. Two packages were tested and an average of maximum chip 1 temperature is reported. The measurement and simulation results are given in Table III. The measurement result has good agreement with the thermal model prediction.

VIII. CONCLUSION

Three-dimensional packaging technology is finding more and more application in portable products, because of the compact package design and better electrical performances. But high heat dissipation from the stacked chip is a challenge. A 3-D package with silicon interposers was developed. Thermal performance of the package with silicon interposer is better than the package with organic substrate. The package was designed to house Processor/ASIC in the stack 1 dissipating 20 W power and two memory chips on the stack 2 dissipating 0.5 W each. The package design was optimized for better structural and thermal performances. Thermal enhancement techniques like thermal via, thermal bridging were analyzed and the package design was found suitable for 3 W power by natural convection cooling. The package thermal performance was further improved by designing a silicon heat spreader. The 3-D package with silicon heat spreader was suitable for dissipating 20 W power with an external heat sink. Prototypes of the 3-D package with silicon interposers were built and characterized. Package thermal performances were extracted and the simulation results found agreeing well with measurement data.

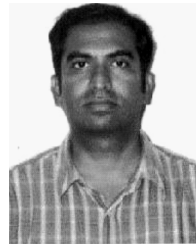
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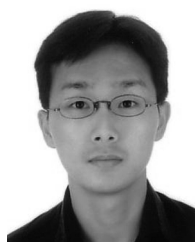
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