

16 Application Specific Integrated Circuits (ASICs)

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16.1 Introduction

The abbreviation ASIC stands for Application Specific Integrated Circuits. Compared with standard circuits an ASIC is designed and manufactured according to specifications resulting from its application. The ASIC user is able to specify the circuit function at design level and/or by means of configuration options. If the function of an IC is only controlled by software then it is not called an ASIC [16.7].

Figure 16.1 shows a possible **classification of monolithically integrated circuits**. Examples of standard ICs are operational amplifiers (standard analog), TTL and CMOS Logic ICs (standard logic), microprocessors, RAM and ROM. Examples of ASICs are Field Programmable (FPGAs), Gate Arrays, Macro Cell, Standard Cell ICs and Full Custom ICs [16.5].

In some cases the classification standard IC/ASIC is difficult. If an ASIC design is so successful that it sells in large numbers it finally becomes a standard IC. Also the classification ROM/FPGA is not always clear.

16.1.1 Technological Characteristics of ASICs

Some technological characteristics show the dynamic progress in the field of ASICs.

The so called **feature size** of a certain technology is a measure of the length of the smallest MOS transistor, sometimes also for the minimal allowable distance between two connection lines on the chips. The feature size λ is in the order of the length of a transistor. With decreasing feature size the area needed is reduced and the transistor performance improves, at the same time the manufacturing will be more demanding.

The silicon chip of the IC, the so called **die** varies in its area from some mm² to several cm². The bigger the die and the smaller λ the more transistors can be integrated into one IC.

As a measure of the complexity of an IC one can consider the number of **gate equivalents**. A gate equivalent is equal to a NAND gate with two inputs.

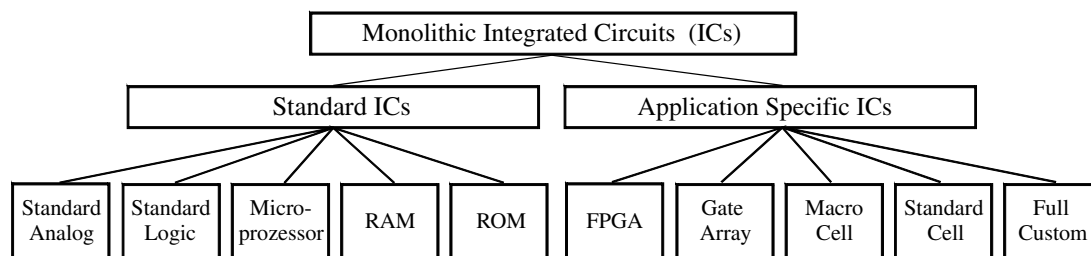


Fig. 16.1 Classification of monolithically integrated circuits

The **Semiconductor Industry Association (SIA)**, an organization supported by all major semiconductor manufacturers, forecasts the progress of the semiconductor technology by means of so called **road maps** and specifies the needed processes and installations [16.9]. Table 16.1 shows the road map for microprocessors from which it can be derived that the integration density and the speed will allow one to build ASICs with more complex functionality and lower prices. The SIA considers the ASICs as one of the motors of technology with respect to integration density, performance, and package. For this compare chapter 1 and 2.

Table 16.1 Road map of semiconductor technology

Year of first production	2001	2005	2010	2016
feature size [nm]	150	80	50	25
max. clock rate [GHz]	1.7	5.1	11.5	28.7

16.1.2 Design Goals for ASICs

Compared to system realizations with standard ICs ASICs show several advantages. The most important design goals for a system are [16.7]:

- cost effective solution;
- low design effort with respect to time and cost;
- high performance, i.e., functionality, speed;
- low power dissipation;
- small volume and weight;
- high reliability;
- low cost for mounting and test.

In order to reach the goals with ASICs certain conditions have to be fulfilled. The methods of design and realization of ASICs the so called **design styles** have to be chosen optimally with respect to the system environment. The preferred design style is dependent on the expected number of parts, on the design time provided, and on the performance desired.

With respect to the most important goal of cost effectiveness the cost of design and manufacturing have to be considered. A related analysis will be carried out in section 16.3.

There are trade offs between different goals, e.g., higher performance generally demands a higher design effort and also results in a higher power dissipation.

16.1.3 Case Study: CD Player, ASIC as Key Component

Figure 16.2 shows a block diagram of a CD player without showing the operating and display unit [16.12]. The CD player consists of a ‘mechadeck’ comprising mechanical and optical components, of an ASIC for signal processing and control tasks, and of several standard ICs. The player is able to communicate via a bus interface with the processor of the operating and display unit. A further interface to the outer world is formed by the stereo audio signal.

The CD rotates within the ‘mechadeck’. The ‘pickup’ to be found there also comprises the laser and six photo-diodes for reading the CD. The position of the pickup has to be controlled with respect to track and z-coordinate (focus).

The core of the CD player is formed by the ASIC ‘CD one Chip’, which takes over all important functions with respect to signal processing and position control. Embedded into the ASIC are:

- a standard microprocessor;
- a signal processor (DSP);
- memory (SRAM);
- a digital analog converter (Audio-DAC);
- a preamplifier for the read signals of the photo diodes.

The rather complicated decoding and error-correction of the read signal by means of the Reed-Solomon algorithm is realized in a hard wired form. The DSP is partly needed for the complicated calculation of the control signals for track and focus from the read signals. The ASIC contains mechanisms for automatic adjustment which enables the construction of a nearly adjustment-free CD player.

The CD player comprises as standard ICs an operational amplifier and some driver ICs. This poses the question of, why those functions realized with standard ICs are not integrated into the ASIC ‘CD one Chip’. On one hand, the technology used in the ASIC is not suitable for some functions, on the other hand, the used standard ICs are so cheap that a further integration does not make sense.

The ASIC ‘CD one Chip’ meets many of the design goals discussed in the previous paragraph. The IC was designed in full custom style, which

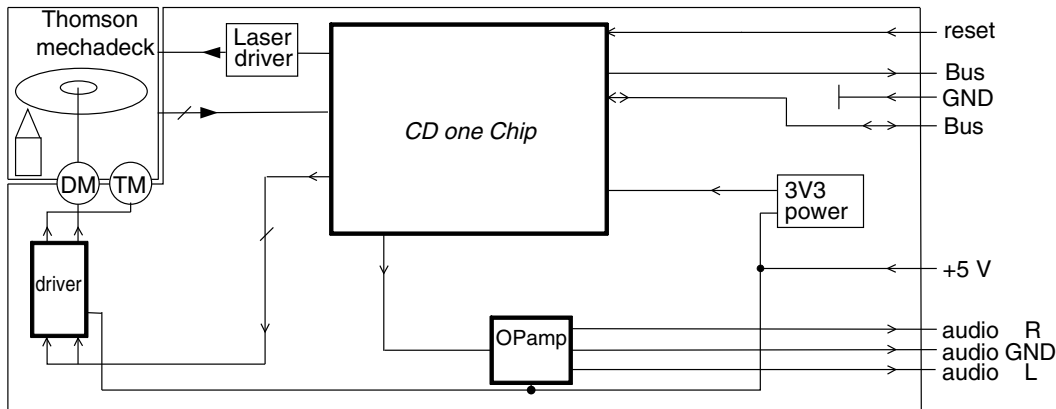


Fig. 16.2 Block diagram of a CD player

meant a high design effort, but led to a very compact layout. In a $0.5\ \mu\text{m}$ technology only $30\ \text{mm}^2$ chip area was needed to realize the complex functions. Taking a sales volume of the 'CD one Chip' in the order of several millions into account this approach led to a cost effective solution.

Compared with a solution with standard ICs the advantages are:

- lower number of components;
- lower power dissipation;
- smaller volume and weight;
- higher reliability;
- lower cost for mounting and test.

In addition, by using an ASIC a certain protection against copying the design by a competitor is given.

Compared with a predecessor model with standard ICs the discussed CD player needs 30 % less PCB area, the overall cost savings are 20 %.

16.2 Design Styles

In this section the different design styles (fig. 16.1) will be presented and discussed with respect to their advantages and disadvantages.

The term semi custom ASICs covers the following different design styles:

- standard cells;
- macro cells;
- gate array;
- PLD;
- FPGA.

Compared with full custom ASICs the design of semi custom ASICs predominantly uses pre-designed cells from libraries.

Often several design styles are used simultaneously when designing an ASIC, e.g., part of the IC can consist of macro cells, the rest of standard cells.

An integrated circuit is manufactured by means of 12 to 25 **masks**, dependent on the complexity of the technology used. More than half of those are needed to structure transistors and other components. The rest define the connections via metal lines and contacts. The choice of the design style depends on whether all masks for a certain ASIC have to be custom specific or only a part of them. In the latter case wafers can be produced with non-custom specific masks and kept in stock, which saves design and manufacturing time.

16.2.1 Full Custom Design Style

For a full custom ASIC, the design and layout are specific. In the extreme case every component is inserted individually in design and layout. This maximum design freedom enables an optimal design with respect to performance, size and power consumption. The cell layout is possible in whatever form is required. For a full custom ASIC all masks are specific.

A full custom design shows the **advantages** of optimal performance, optimal component density, and flexible forms. With a very high number of parts this design style is most economical.

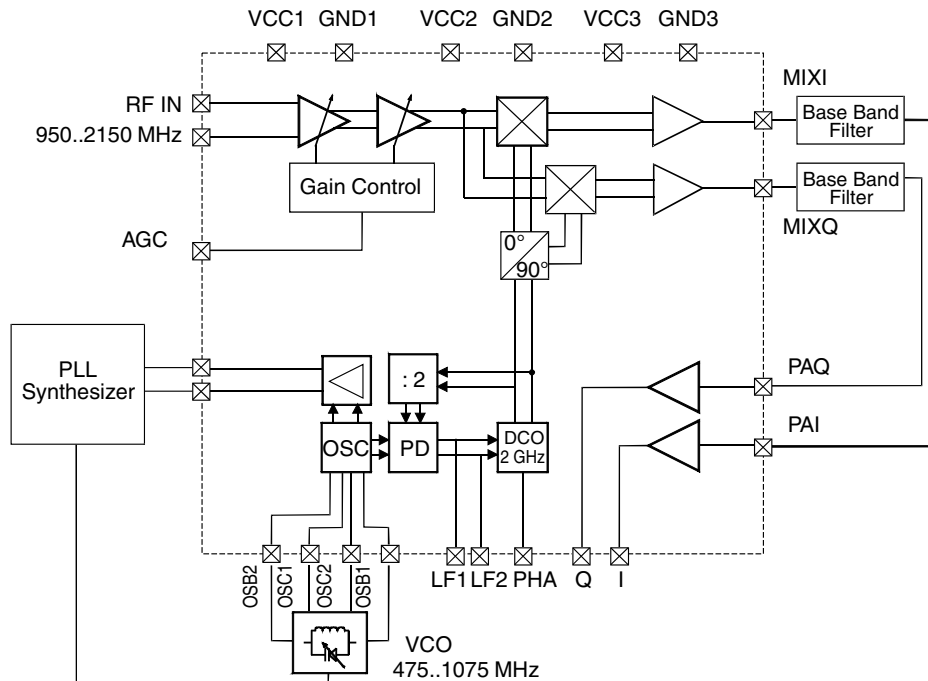


Fig. 16.3 Block diagram of a full custom ASIC for direct conversion of digital satellite TV signals

The **disadvantages** of the full custom design style are:

- high design effort with respect to time and cost;
- high design risk using untested cells.

Design and layout of a full custom ASIC demands a lot of experience. The full custom design style is most common with mixed signal and analog applications.

As an example of a full custom ASIC an IC for direct conversion of digital satellite TV signals will be considered, where the block diagram is shown in fig. 16.3 [16.1]. The incoming signal at RF IN is first amplified and then converted into two orthogonal base band signals by means of two mixers, which are fed with two orthogonal oscillator signals. These signals are generated by an internal delay cell oscillator (DCO), which is synchronized by means of an internal phase detector (PD) with an oscillator connected to an external tank circuit. After external base band filtering the signals are fed back into the IC and amplified in order to reach a sufficiently high level for digitization. The input signals and the oscillator signals of the DCO are in the frequency range from 950 to 2,150 MHz. The specifications with respect to linearity, to tuning

range of the oscillators, and to deviation from quadrature were so tight that only a full custom design was possible. The design realized by means of a 20 GHz process demanded a very high design effort with several iteration steps.

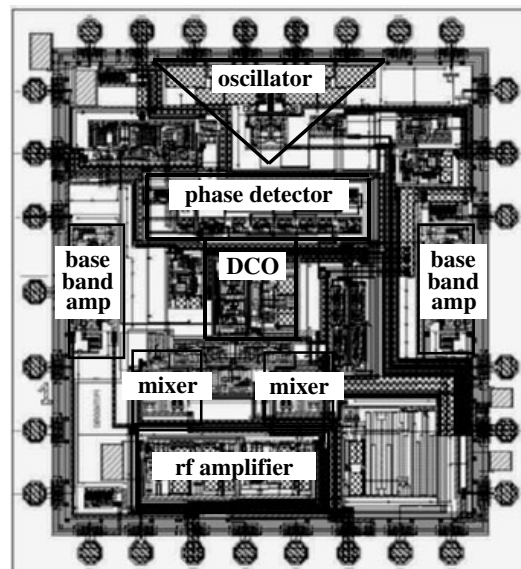


Fig. 16.4 Layout of the direct conversion IC of fig. 16.3

Figure 16.4 shows the layout of the direct conversion IC. The individual cell outlines typical for full custom design can be recognized. In order to design such a layout a lot of experience is needed because it is so difficult to meet the tight specifications regarding cross talk and quadrature deviation. Even in this pronounced full custom layout repeating cells can be recognized, which is caused partly by symmetry.

The design was accomplished without using pre-designed cells from a library, but, of course, experience gained from previous designs was of great value.

16.2.2 Standard Cells

The term standard cell signifies a pre-defined block, which in general represents a logic function of low complexity (e.g., NAND, NOR or FlipFlop). Figure 16.5 shows a NOR standard cell in ECL technology [16.8] which is used in a standard cell layout (fig. 16.6). The power supply lines are the lines above and below the logic circuit. Input and output are to be found on the left hand and right hand side, respectively.

Standard cells are designed as full custom designs and stored in libraries after having been tested and optimized. The libraries can either be prepared individually or be provided by the manufacturer of the technology, or can be bought from a suitable company. The placement of standard cells is principally free but normally they are placed in **rows of cells** with 'running through' supply lines. Therefore the cells have to have the same height (see fig. 16.6). Figure 16.6 shows in the upper left part some full custom cells which can be integrated without complying with the standard cell pattern. All masks are specific for a certain ASIC.

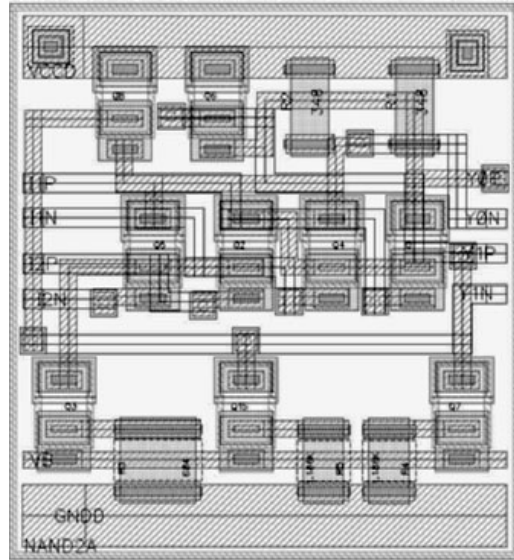


Fig. 16.5 NOR standard cell in ECL technology

The standard cell design is supported by one or several libraries of optimized base cells for which simulation and layout data are available. Some cells can be parameterized. Design and layout in standard cell design are well supported by EDA tools. For details of libraries see chapter 19.

Figure 16.7 shows the top layout of a circuit which consists of standard cells and macro cells discussed in paragraph 16.2.3. Several cell rows can be distinguished. Between the rows wide wiring channels are provided. In order to allow wiring in vertical direction gaps in the cell rows are provided, the so called feed throughs. The standard cell design has some **advantages** compared with the full custom design:

- the design time is much shorter;
- because of the lower design effort this approach is economical with a medium number of parts;
- the design risk is lower because of the use of a tested library.

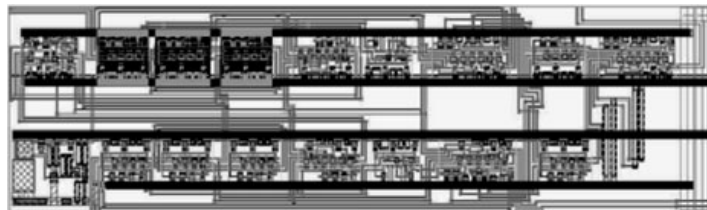


Fig. 16.6 Rows of standard cells using NOR standard cell form fig. 16.5

Though the standard cell design appears attractive there are still some **disadvantages**:

- transistors cannot be designed independently and optimally, thus the performance is sub-optimal;
- with a small number of parts this approach can be uneconomical as all masks have to be produced.

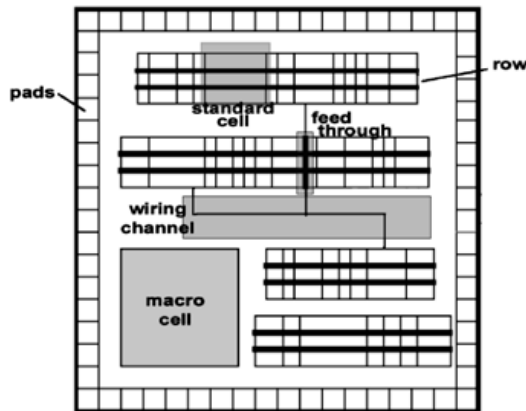


Fig. 16.7 Top layout of a circuit which consists of standard cells and a macro cell

16.2.3 Macro Cells

The term macro cell or mega cell signifies a **pre-defined block**, which shows a much higher complexity than a standard cell. Examples of macro cells are:

- RAM cell;
- ROM cell;
- serial interfaces;
- timer;
- arithmetic logic units (ALUs);
- processor cores.

Figure 16.7 shows a macro cell combined with standard cells. The form of a macro cell is flexible. In general no row structure is formed. Macro cells can be placed like standard cells at will. All masks are specific for a certain ASIC.

Macro cells are traded as so called **intellectual properties (IP)**, which are discussed in detail in chapter 7. **Hard macro** and **soft macro** have to be distinguished. A **hard macro** has a fixed layout and is described by a simulation, which includes layout influences. The embedding of a hard macro is equivalent to placing of a component.

A **soft macro** is typically defined by a netlist or by VHDL code. Layout and simulation data still have to be generated.

The design style with macro cells shows the **advantages**:

- Fast design with high productivity;
- Short time to market;
- Economical with medium number of parts;
- Low design risk because of use of libraries.

The **disadvantages** are:

- insertion of a macro cell into an individual design demands a certain effort;
- the price of IPs can be remarkable;
- the design style can be uneconomical with a small number of parts as all masks have to be produced.

16.2.4 Gate Array

On a gate array (GA) transistors; and possibly other components; are connected to form **pre-defined base cells which are arranged in a matrix**. Each of the squares of the inner section of the ASIC shown in fig. 16.8 represents a base cell. The designer defines only those masks, which signify contacts and connection lines between base cells. This procedure is called **personalization** of a gate array and this kind is called a **masked gate array (MGA)**. The manufacturer keeps pre-fabricated wafers in stock. Hence only the masks for the metal connections have to be produced for customization which reduces production time and cost.

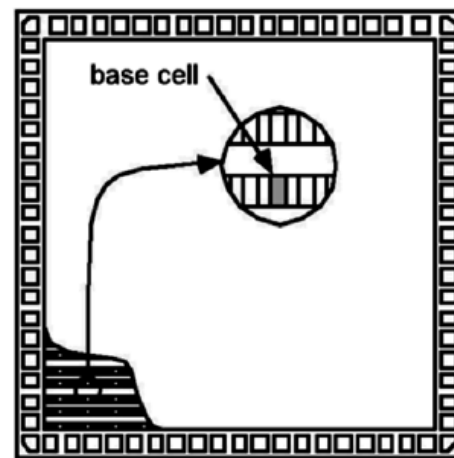


Fig. 16.8 Masked gate array

There are three types of MGAs:

- MGAs with wiring channels;
- Channelless MGAs;
- Structured MGAs.

Figure 16.8 shows a MGA with wiring channels where the base cells of the array are grouped in rows as in a standard cell design. Contrary to the latter the wiring channels cannot be chosen at will but are fixed geometrically. The fixed arrangement of base cells and wiring channels reduces the gate density remarkably compared to a standard cell design.

Figure 16.9 shows a **channelless MGA** which is also called a **Sea of Gates**. There are no special wiring channels between the cells. Instead the wiring is arranged across the base cells. This is possible as those base cells which are crossed by wires are not used and have no contact with the wires. Channelless MGAs allow a higher gate density than MGAs with wiring channels because the wiring can be configured freely.

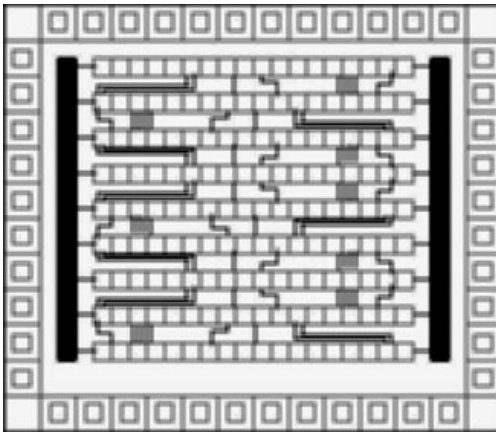


Fig. 16.9 Channelless gate array or Sea-of-Gates

Figure 16.10 shows a so called **structured MGA**. In addition to matrix-like arranged base cells which cover the main part of the area there are ranges with macro cells which contain a RAM or a processor core for instance. With this approach the possibilities of gate arrays and macro cells can be combined.

The great **advantage** of gate arrays lies in that only a few masks have to be produced custom specifically. Compared to the previously discussed design styles this leads to shorter design times and to higher economy when only a small number of

parts is required. Compared with standard cell design gate arrays show the **disadvantage** of a lower equivalent gate density and therefore a higher price per part. In addition analog circuits can only be realized on gate arrays with great difficulty.

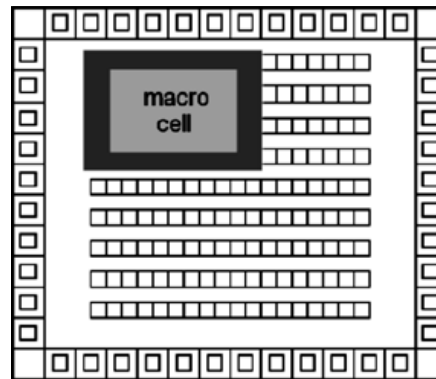


Fig. 16.10 Structured gate array

In the following paragraph the **Gate Forest Technology of IMS** will be discussed as an example of the sea of gates technology. This technology provides masters with 2,000 to 120,000 gate equivalents, which can use up to 408 I/O connections. In addition to digital master cells there are also analog cells. The technology is therefore suitable for mixed signal applications.

The right hand side of fig. 16.11 shows two non-personalized master base cells which contain two NMOS and two PMOS transistors respectively. This shows that a master base cell forms a gate equivalent. The transistor gate wires in polysilicon are already provided yet the cells themselves are unwired.

On the left hand side of fig. 16.11 one cell is wired as an inverter and another cell is wired as a NAND gate with two inputs. In order to personalize the cells two layers 'metal 1' and 'metal 2' are provided. In addition contacts and vias are needed.

Figure 16.12 shows part of the layout of an A/D-converter described in [16.6] as an example of a personalized gate array. For reasons of clarity only the layers 'metal 1' and 'metal 2' are shown. Bond pads related to I/O connection and interface circuits can be recognized as also some gates belonging to the successive approximation register. Normally the gate density is higher than shown

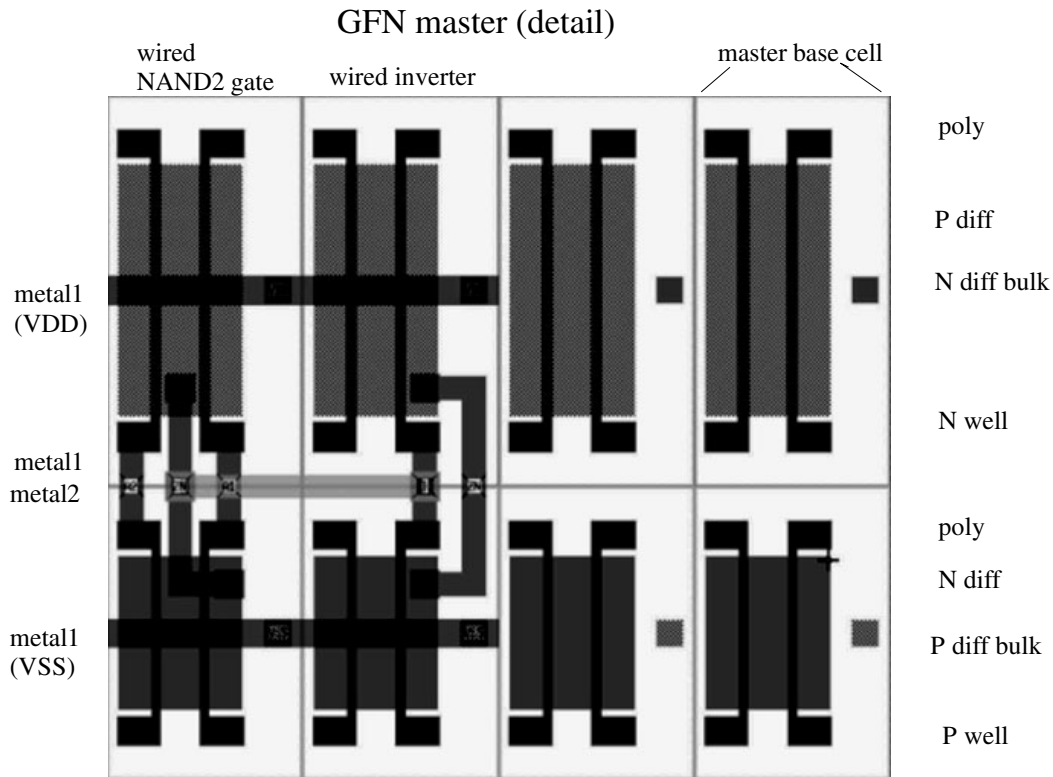


Fig. 16.11 Detail of a master in 'Gate-Forest' technology

in the section, but then the different circuit blocks could hardly be recognized.



Fig. 16.12 Detail of a personalized gate array in 'Gate-Forest' technology

16.2.5 Programmable Logic: FPGA

The term **Field Programmable Gate Array (FPGA)** signifies programmable logic devices (PLDs) with complex logic cells. As with all PLDs the logic function can be configured custom-specifically by software. Here the FPGAs will be discussed only briefly in order to compare them with other design styles. For a more detailed discussion see chapter 18.

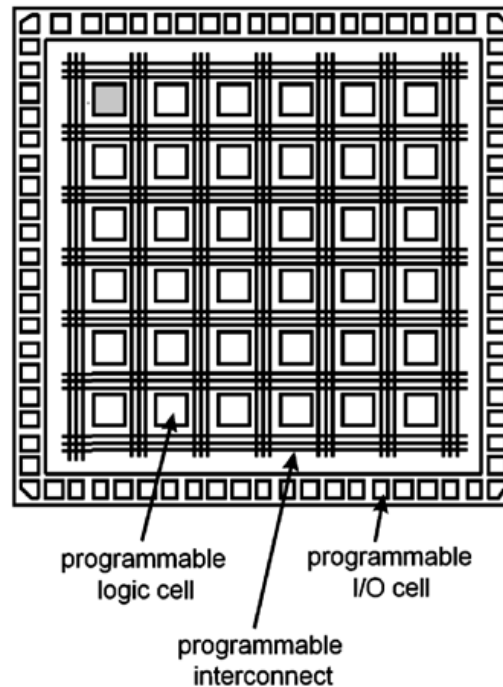


Fig. 16.13 Field programmable gate array (FPGA)

Table 16.2 Comparison between design styles

	full custom	standard cell	macro cell	gate array	FPGA
custom specific masks	all	all	all	max. 50 % of all masks	none
cell measures	variable	fixed	variable	fixed	fixed
cell placement	free	rows	free	matrix	matrix
function of a cell	variable	selectable	fixed	fixed	programmable
wiring	variable	variable channels	variable	variable or fixed channels	programmable
area utilization	excellent	good	good	moderate	poor
performance	excellent	high	high	moderate	low
design productivity [gates/day]	50	200	400	350	500
design time	man years	man months	man months	man weeks	man weeks
production time	12 weeks	12 weeks	12 weeks	3 weeks	hours
economical at number of parts/year	> 100,000	10,000 ... 100,000	10,000 ... 100,000	100 ... 10,000	< 1,000

Figure 16.13 shows that logic cells, interconnect and I/O cells are configurable. Typically the logic cells are arranged as in gate-arrays.

The main **advantage** of FPGAs lies in the extremely short design time. This is because the configuration can be done by software without technological steps involved. The designer himself can program the FPGA and sometimes re-program it. This makes FPGAs attractive for a small number of parts or for a prototype design of an ASIC still to be designed. Compared to real ASICs FPGAs have the **disadvantages** of higher cost per part and usually lower performance.

16.2.6 Comparison of the Design Styles

Table 16.2 shows the different design styles with respect to properties, advantages and disadvantages for comparison. It is difficult in some cases to attribute a certain feature to a certain design style as the actual ASIC project is of influence. Therefore the statements can only be interpreted as typical. The information was partly taken from [16.11], [16.10], [16.13] and [16.3].

Some properties and features require the following brief explanations:

- **custom specific masks** supplies information on the necessary number of masks and technological steps. In the case of FPGA the actual IC is ready and no masks are needed;

- **cell measures** signifies the cell form (fixed or variable);
- **cell placement** signifies the grouping of cells;
- **wiring** signifies how the cells can be wired;
- **area utilization** signifies the gate density reached;
- **performance** is related to speed and power consumption;
- **design productivity** gives a typical value for the number of gates a designer is able to add to the design per day;
- **design time** results from the number of the gates needed to produce the ASIC;
- **production time** refers to the time used for technological steps. In the case of FPGA production is equivalent to a programming procedure;
- **economical at number of parts/year** provides a range where a certain design style appears economically sensible. This feature is discussed in detail in the next paragraph.

16.3 Economical Aspects

In this section ASIC design styles will be discussed with respect to economical aspects. The costs of ASIC manufacturing, which generally alter rapidly, are not often published by the semiconductor manufacturer. Thus the following values can only be considered as approximate.

16.3.1 ASIC as Product

At first some terms will be introduced which are related to the evaluation of costs and profits of ASICs.

‘Fixed costs’ (FC) are those costs of a product, that are independent of the number of parts sold. With ASICs there are, for instance, the costs of masks or of the CAD installation. The fixed costs have to be taken into account in proportion to every IC sold.

‘Variable costs’ (VC) are those costs of a product, which are proportional to the number of parts sold. With ICs there are, for instance, the costs of a die or a case. Generally the lifetime of a product on the market is restricted and superseded by better successor products. This lifetime is called **‘product lifetime’** (PLT). Within PLT a certain **number of parts** of a product will be sold. This is called **‘sales volume’** (SV).

The costs per IC are found by

$$ICcost = VC + \frac{FC}{SV} \quad (16.1)$$

The **‘production costs’** (PC) are found by

$$PC = FC + VC \cdot SV \quad (16.2)$$

16.3.2 Fixed Costs

Training comprises acquaintance of the technology related **design kit**, which contains the design rules and the libraries and, in addition, getting to know EDA tools, computers, and system organization are taken into account. The more specific the tools, the higher the training costs.

The costs for computer and software include the costs for buying a workstation and the license costs for EDA tools. The proportion of these costs is dependent on the project time, which differs with each of the design styles.

The **design costs** comprise the costs for design staff and costs for generating the layout of the ASIC. The starting point for table 16.3 is a medium sized ASIC with 20,000 gate equivalents. In order to estimate the number of days required for the design it is necessary to have an idea of the **productivity**, i.e., the design speed (gates/day) which is dependent on the design style. In addition, the

experience of the designer, the design method, and the EDA tools play a role.

Part of the design time is needed to design the testability of the IC and to generate the so called **test vectors**.

In addition to the design time of the original circuit the time for **evaluating the IC** samples and for a possible **redesign** has to be taken into account. This effort regarded to be proportional to the effort of the original design.

The non-recurring costs for production of an ASIC are called **Non-Recurring Engineering Costs (NRE)**. These comprise the generation of custom specific masks the number of which is dependent on the design style. The information about masks cost is related to a technology with a feature size of 0.35 μm. In addition, the cost of the production of some ASIC samples and the costs of test related preparation and programming were added to the NRE. Not taken into account were costs for the so called industrialization which qualification and investigation of production methods under different conditions.

Other fixed costs comprise costs for documentation, marketing and advertising. Here the figures vary so much that it does not make sense to insert concrete values.

If the evaluation of the ASIC samples show that the performance of the IC does not fulfil the expectations, the design has to be improved. Especially with full custom design the probability of a redesign is high, because untested cells are used. With semi custom ICs the test results are normally in accordance with the simulation results found during the design. Every redesign causes costs for design and NRE. More important, however, is the resulting time loss and the lower product lifetime of number of parts.

The **total fixed costs** are the sum of training costs, computer and software costs, design costs, mask costs, cost for test preparation, and other costs.

16.3.3 Variable Costs

Table 16.4 gives an overview of the variable costs of an ASIC related to different design styles where some data were taken from [16.10].

Table 16.3 Fixed cost for an exemplary ASIC

	Full custom	Standard cell	Macro cell	Gate array	FPGA
<i>Trainig</i>					
days	10	5	5	5	2
cost/day	500 €	500 €	500 €	500 €	500 €
cost trainig	5,000 €	2,500 €	2,500 €	2,500 €	1,000 €
<i>Hardware</i>	5,000 €	2,500 €	2,500 €	1,000 €	500 €
<i>Software</i>	100,000 €	25,000 €	25,000 €	5,000 €	2,500 €
<i>Design</i>					
size (gate equivalent)	20,000	20,000	20,000	20,000	20,000
design productivity (gate equ./day)	50	200	400	350	500
days design	400	100	50	57	40
days evaluation	80	20	10	11	8
days redesign	40	0	0	0	0
cost/day	500 €	500 €	500 €	500 €	500 €
design cost	260,000 €	60,000 €	30,000 €	34,285.71 €	24,000 €
<i>NRE</i>					
no. masks	15	15	15	4	0
cost/mask	2,500 €	2,500 €	2,500 €	2,500 €	5,000 €
cost masks	37,500 €	37,500 €	37,500 €	10,000 €	0 €
cost samples	10,000 €	10,000 €	10,000 €	1,500 €	0 €
days test preparation	10	5	5	5	
cost/day	500 €	500 €	500 €	500 €	500 €
cost test preparation	5,000 €	2,500 €	2,500 €	2,500 €	0 €
<i>Other fixed costs</i>					
documentation					
marketing					
total fixed cost	422,500 €	140,000 €	110,000 €	56,785.71 €	28 000 €

Table 16.4 Variable cost for an exemplary ASIC

	Full custom	Standard cell	Macro cell	Gate array	FPGA
<i>Die cost</i>					
no. Gate equivalents	20,000	20,000	20,000	20,000	20,000
gate density/cm ²	40,000	35,000	35,000	25,000	20,000
density factor	0.90	0.65	0.65	0.50	0.30
die area/cm ²	0.56	0.88	0.88	1.60	3.33
wafer diameter/inch	8	8	8	8	8
complete dies/wafer	498	301	301	152	62
defect density/cm ²	0.50	0.50	0.50	0.50	0.50
yield	0.77	0.67	0.67	0.51	0.30
good dies/wafer	384	202	202	78	19
cost wafer	1,000 €	1,000 €	1,000 €	1,000 €	1,000 €
die cost	2.61 €	4.95 €	4.95 €	12.88 €	53.96 €
<i>Package cost</i>					
no. pins	68	68	68	68	68
cost/pin	0.02 €	0.02 €	0.02 €	0.02 €	0.02 €
package cost	1.02 €	1.02 €	1.02 €	1.02 €	1.02 €
<i>Test cost</i>	0.25 €	0.25 €	0.25 €	0.25 €	0.25 €
Total variable cost	3.88 €	6.22 €	6.22 €	14.15 €	55.23 €

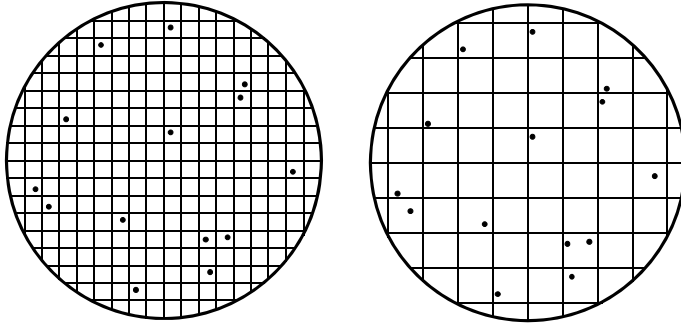


Fig. 16.14 Wafer including defects with dies of different areas

In order to determine the **cost of a die** the required **area** of the die is calculated first. For this purpose the **number of gates** is divided by the **gate density** and multiplied by the **density factor**. The gate density and the density factor of the layout are dependent on technology and design style.

Figure 16.14 shows a wafer with medium sized dies (left) and large dies (right). The dots represent defects caused by errors during production. The dies near the periphery are incomplete and cannot be used. The number of **complete dies** is given by

$$= \frac{\text{wafer area}}{\text{die area}} - \frac{\text{wafer circumference}}{\text{die edge length}} \quad (16.3)$$

The **defect density** is a quality feature of the technology. A single defect on a die will generally make the die unusable. In order to avoid too high a failure rate with a $0.5\mu\text{m}$ technology a defect density of less than $1/\text{cm}^2$ is necessary.

The **yield** is dependent on defect density (Dd) and die area (DA) [16.4]:

$$\text{Yield} = \left(\frac{1}{1 + \frac{Dd \cdot DA}{2}} \right)^2 \quad (16.4)$$

For an established technology a yield of more than 80 % is expected. The number of intact dies is calculated by multiplication of the number of whole dies with the yield.

The **costs per processed wafer** refer to an $0.5\mu\text{m}$ technology. The costs per die are finally determined from the costs per wafer divided by the number of intact dies.

The **package costs** are approximately proportional to the number of pins but also depend on form

and material of course. The numbers given refer to rather cheap SMD plastic cases.

The last row in table 16.4 shows the **test costs** per IC. Every single IC is tested by means of test vectors.

The **total variable costs** of an IC are equal to the costs per die, case costs and package costs.

16.3.4 Design Style Comparison

With the data provided in section 16.3 the IC costs can now be determined according to equation (16.1). Figure 16.15 shows the IC costs as function of the sales volume during the lifetime of an IC for the different design styles, in which the fixed costs were taken from table 16.3 and the variable costs from table 16.4.

With increasing sales volume the fixed costs are less significant and the IC costs decrease. At a sales volume of approximately 1,000 the **break even volume (BEV)** between the FPGA and the gate array design style is to be found. Referring to the above data, the BEV between gate array and standard cells or macro cells lies at 10,000 parts. Only above 100,000 parts does the full custom solution become optimal.

There are a few ways of lowering the IC costs. The fixed costs are mainly determined by the **design productivity**. For this trained designers, modern design methodology, and good EDA tools are necessary. The costs of masks and of sample production can be lowered if the concept of a so called **multi-project wafer (MPW)** is applied. Here several different designs can be processed on one wafer. Also for production of a low number of parts or in the starting phase of a product the MPW can be an attractive approach.

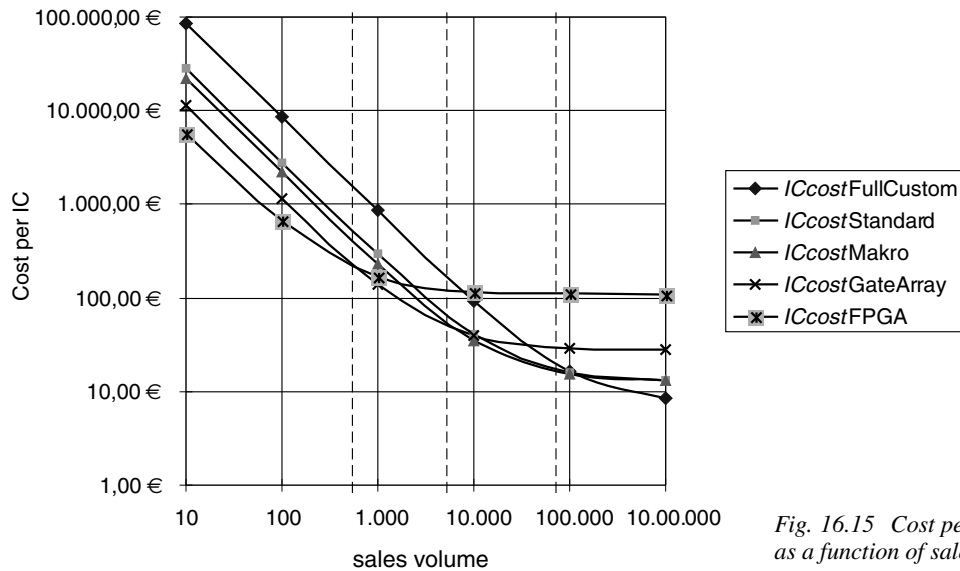


Fig. 16.15 Cost per IC as a function of sales volume

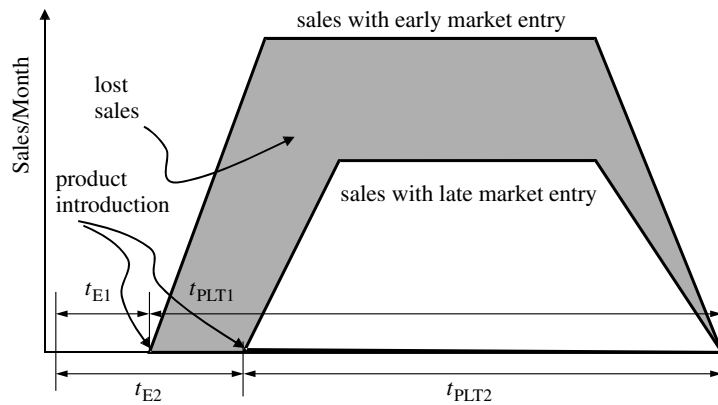


Fig. 16.16 Monthly sales of a product

The price of an IC is determined by the IC costs plus the required **profit per part**. The achievable price mainly depends on competition, which in turn depends on when the innovative product is put to market. The following consideration highlights the design speed as the decisive factor in the success of an IC.

Figure 16.16 shows the monthly sales of a product first under the assumption of an early introduction to the market, second with later introduction [16.2]. If the product is introduced later the product lifetime will be shortened from t_{PLT1} to t_{PLT2} . In addition this product will have a lower market share. Both factors lead to a loss of turnover and lower the sales volume.

The design styles presented differ in design and production time t_E : for the exemplary ASIC the

FPGA solution required a design time of 48 days and no time for production whereas the full custom design solution required 520 days design time and 50 days production time. Of course, distributing the workload to several designers can shorten the time required for the development of an IC.

It becomes clear that a combination of different design styles is of great advantage. In order to achieve a fast product introduction a FPGA or gate array solution could be chosen, whereas for mass production a solution with lower variable costs is appropriate.

The design methodology has to be chosen in such a way that a change in design style does not lead to too high a development effort.

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