

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Ken et al.	
U.S. Patent No.:	9,164,942	Attorney Docket No. 50095-0275IP1
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Title:	HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP MODULE	

DECLARATION OF DR. DAVID LIU

I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: February 13, 2026_____

By: _____

David Liu, Ph.D.

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I, David Liu, Ph.D., declare that:

I. INTRODUCTION

1. I have been retained on behalf of Apple Inc. (“Apple”) to offer technical opinions related to U.S. Patent No. 9,164,942 (“the ’942 patent”) (EX1001). I understand that Apple is requesting that the Patent Trial and Appeal Board (Board) institute an *Inter Partes* Review (IPR) proceeding of the ’942 patent.

2. I have been asked to provide my independent analysis of the ’942 patent in light of the prior art publications cited in this Declaration.

3. I am not and never have been an employee of Apple. I received no compensation for this Declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’942 patent, the prior art publications cited below, and issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’942 patent.

4. My analysis here is based on my years of education, research, and experience, as well as my investigation and study of relevant materials, including those cited in this Declaration.

5. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further,

I may consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

6. My analysis of the materials produced in this proceeding is ongoing, and I will continue to review any new material as it is provided. This Declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

7. My education and experience are described more fully in the attached curriculum vitae, provided as an appendix. For ease of reference, I have highlighted certain information below.

8. I am over the age of 18 and am competent to write this Declaration. I have personal knowledge or have developed knowledge—based upon education, training, or experience—of the technologies of the matters set forth herein.

9. My curriculum vitae (“CV”) is filed concurrently as an appendix and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My CV also includes information about my expert witness experience, with case numbers where available.

10. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

11. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

12. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. ("TI"). At TI, my job responsibilities included process integration, device modeling, high-voltage complementary metal oxide semiconductor (CMOS) process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

13. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. ("AMD") where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5 μ m and 0.35 μ m Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology to accommodate x-decoder transistors and high-voltage transistors for negative gate erase operations. While at AMD, I was awarded a Spotlight Award for developing

a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

14. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

15. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

16. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm).

17. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

18. Since 2007, I have served as a technical consultant where I have provided expert advice regarding semiconductor memory technologies, including both DRAM and Flash memory technologies; CMOS process technology, and

semiconductor device physics. As part of this, I have considered, assessed, and assisted with the design of various different memory devices, both volatile memories and non-volatile memories, including NAND flash and monolithic 3D memory structures.

19. I hold over 99 U.S. patents, a vast majority of which are directly related to Nonvolatile memory device technology. For example, U.S. Patent No. 5,250,464 relates to use of sidewall layers of silicone dioxide and silicon nitride to form a sidewall anti-fuse structure.

20. In writing this Declaration, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- U.S. Patent App. Pub. No. 2004/0260864 (“Lee”) – EX1004
- PCT App. Pub. No. WO2008/124503 (“Tsern”) – EX1005
- U.S. Patent No. 7,645,692 (“Matsubara”) – EX1006
- U.S. Patent No. 7,785,933 (“Dozen”) – EX1007
- U.S. Patent No. 5,498,990 (“Leung”) – EX1008
- “Development of 3D Stack Package Using Silicon Interposer for High-Power Application.” N. Khan *et al. IEEE Transactions on Advanced Packaging*, Vol. 32, No. 1, February 2008 – EX1009
- U.S. Patent No. 6,226,755 (“Reeves”) – EX1010
- U.S. Patent No. 8,193,635 (“Bruno”) – EX1011

- U.S. Patent Pub. No. 2010/0187671 (“Lin”) – EX1013
- U.S. Patent No. 8,344,496 (“White”) – EX1014
- U.S. Patent No. 6,353,538 (“Ali”) – EX1015
- U.S. Patent No. 8,502,375 (“Liao”) – EX1016
- U.S. Patent Pub. No. 2004/0158669 (“Weng”) – EX1017
- U.S. Patent No. 6,184,808 (“Nakamura”) – EX1019
- U.S. Patent No. 8,895,345 (“Akiyama”) – EX1020
- U.S. Patent No. 5,848,080A (“Dahm”) – EX1021
- U.S. Patent No. 6,412,786 (“Pan”) – EX1022
- U.S. Patent App. Pub. No. 2007/0109831 (“Raghuram”) – EX1023
- U.S. Patent No. 5,844,853 (“Kitsukawa”) – EX1024
- U.S. Patent No. 8,405,214 (“Willey”) – EX1025
- U.S. Patent No. 8,174,868 (“Liaw”) – EX1026
- U.S. Patent No. 6,949,951 (“Young”) – EX1027
- U.S. Patent No. 7,983,051 (“Lee-051”) – EX1028
- *Semiconductor Device Fundamentals*. Robert F. Pierret, 1996
 (“Pierret”) – EX1030
 “Application Specific Integrated Circuits
 (ASICs).” Martin Reiger. *The Electronic Design Automation
 Handbook*. Jansen, D. ed., 2003 (“Rieger”) – EX1031

21. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '942 Patent at the time of the earliest possible priority date of the '942 Patent, and I have done so during my review of these materials.

22. The '942 patent has a filing date of October 11, 2012, and claims a priority date of October 11, 2011 ("the Critical Date"). Counsel has informed me that the Critical Date represents the earliest possible priority date to which the challenged claims of '942 patent are entitled, and I have therefore used that Critical Date in my analysis below. I have not assessed whether the '942 patent is entitled to the October 11, 2011 priority date.

23. I have no financial interest in the parties or in the outcome of this proceeding. I am being compensated for my work as an expert on an hourly basis. My compensation is not dependent on the outcome of these proceedings or the content of my opinions.

24. In writing this declaration, I have considered the following: my own knowledge and experience, including my work experience in electrical engineering and memory development, and my experience in working with others involved in those fields. In addition, I have analyzed various publications and materials, in addition to other materials I cite in my declaration.

25. My opinions, as explained below, are based on my education, experience, and expertise in the fields relating to the '942 patent. Unless otherwise stated, my testimony below refers to the knowledge of one of ordinary skill in the art as of the Critical Date, or before. Any figures that appear within this document have been prepared with the assistance of Counsel and reflect my understanding of the '942 patent and the prior art discussed below.

III. SUMMARY OF CONCLUSIONS FORMED

26. This declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions, based upon my knowledge and experience and my review of the prior art publications listed above, I believe that:

- Claim 19 is obvious in view of Lee
- Claims 19, 22, 25, and 26 are obvious in view of Lee and Tsern
- Claim 21 is obvious over Lee, Tsern, and Khan
- Claim 20 is obvious over Lee, Tsern, Khan, and Dozen
- Claims 23 and 24 are obvious over Lee, Tsern, and Leung
- Claims 27, 28, and 31 are obvious over Lee, Tsern, and Lin
- Claim 29 is obvious over Lee, Tsern, Lin, and Ali
- Claim 30 is obvious over Lee, Tsern, Lin, and White
- Claims 1, 5, 9, and 10 are obvious over Lee, Tsern, and Matsubara
- Claim 2 is obvious over Lee, Tsern, Matsubara, and Dozen

- Claim 3 is obvious over Lee, Tsern, Matsubara, and Khan
- Claim 4 is obvious over Lee, Tsern, Matsubara, Khan, and Dozen
- Claim 6 is obvious over Lee, Tsern, Matsubara, and Weng
- Claims 7 and 8 are obvious over Lee, Tsern, Matsubara, and Leung
- Claims 11, 12, and 15 are obvious over Lee, Tsern, Matsubara, and Lin
- Claim 13 is obvious over Lee, Tsern, Matsubara, Lin, and Ali
- Claims 14 and 18 are obvious over Lee, Tsern, Matsubara, Lin, and White
- Claim 16 is obvious over Lee, Tsern, Matsubara, Lin, and Liao
- Claim 17 is obvious over Lee, Tsern, Matsubara, Lin, Liao, and White

IV. LEVEL OF ORDINARY SKILL IN THE ART

27. In my opinion, a person of ordinary skill in the art as of the Critical Date of the '942 Patent (hereinafter a "POSITA") as of October 11, 2011 would have had at least a master's degree in electrical engineering, or a comparable field, and at least two years of professional experience working with semiconductor memory, including DRAM. Additional years of experience could substitute for an advanced-level degree (and vice versa).

28. Based on my experiences, I have a good understanding of the capabilities of one of ordinary skill. Indeed, I have worked closely with many such

persons over the course of my career. From my industry experience, I am familiar with what a skilled person would have known and found predictable in the art. Furthermore, I possess those capabilities myself.

V. SUMMARY OF THE '942 PATENT

29. The '942 Patent relates to “a high speed memory chip module.” EX1001, Abstract. This module includes “multiple memory cell array integrated circuits,” with a logic unit coupled to the memory cell array ICs via a first transmission bus. *Id.* The logic unit is also coupled to a second transmission bus. *Id.*, claim 1. The patent claims features related to width of the buses of the memory chip module and gate lengths of the memory cell array ICs and logic unit. But the configuration of the memory chip module claimed in the '942 Patent was not new, nor were the claimed bus width and gate length relationships, as I will demonstrate here.

VI. PRIOR ART ANALYSIS

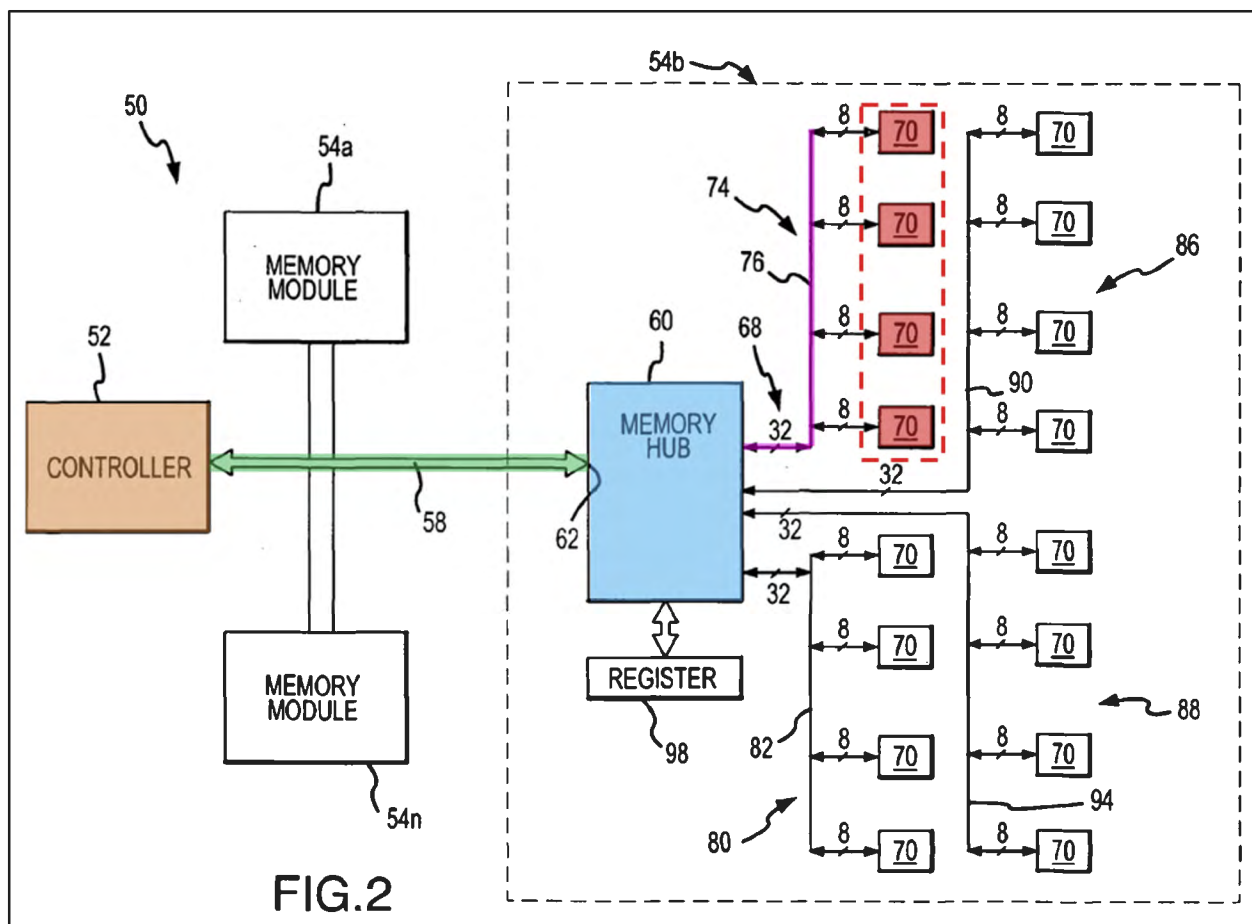
A. [Ground 1A] Lee Renders Obvious Claim 19

1. Lee

30. Lee describes a memory system that includes a memory module that is configurable “in a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously addressed.” EX1004, [0009]. For instance, “[w]hen programmed for a high bandwidth, the memory hub simultaneously accesses the memory devices in all of the ranks,” and “[w]hen

programmed for a high memory depth, the memory hub accesses the memory devices in only one of the ranks at a time.” *Id.* The configurability of Lee’s memory module allows “the data format [to be] optimized for a particular application being executed in a computer system or other electronic system containing the memory system.” *Id.*, [0020].

31. FIG. 2, *infra*, illustrates such a memory system. *See* EX1004, [0015]. In this system, a controller 52 (orange) is “coupled to several memory modules 54*a, b ... n* through a high-speed link 58” (green). *Id.* Specifically, each memory module 54 “includes a memory hub 60 [blue] ... coupled to the high-speed link 58 and a bus system 68 coupled to several memory devices 70,” *e.g.*, DRAM. *Id.* In Lee’s architecture, “the memory devices 70 are divided into four groups or ‘ranks’ [each] coupled to the memory hub 60 through a respective bus system.” *Id.*, [0016]. For instance, the four memory devices 70 in the first rank 74, indicated in red, are “coupled to the memory hub 60 through a first bus system 76” (pink). *Id.* Similarly, the memory devices in the other ranks 80, 86, 88 “are each coupled to the memory hub 60 through respective bus systems” 82, 90, 94. *Id.*

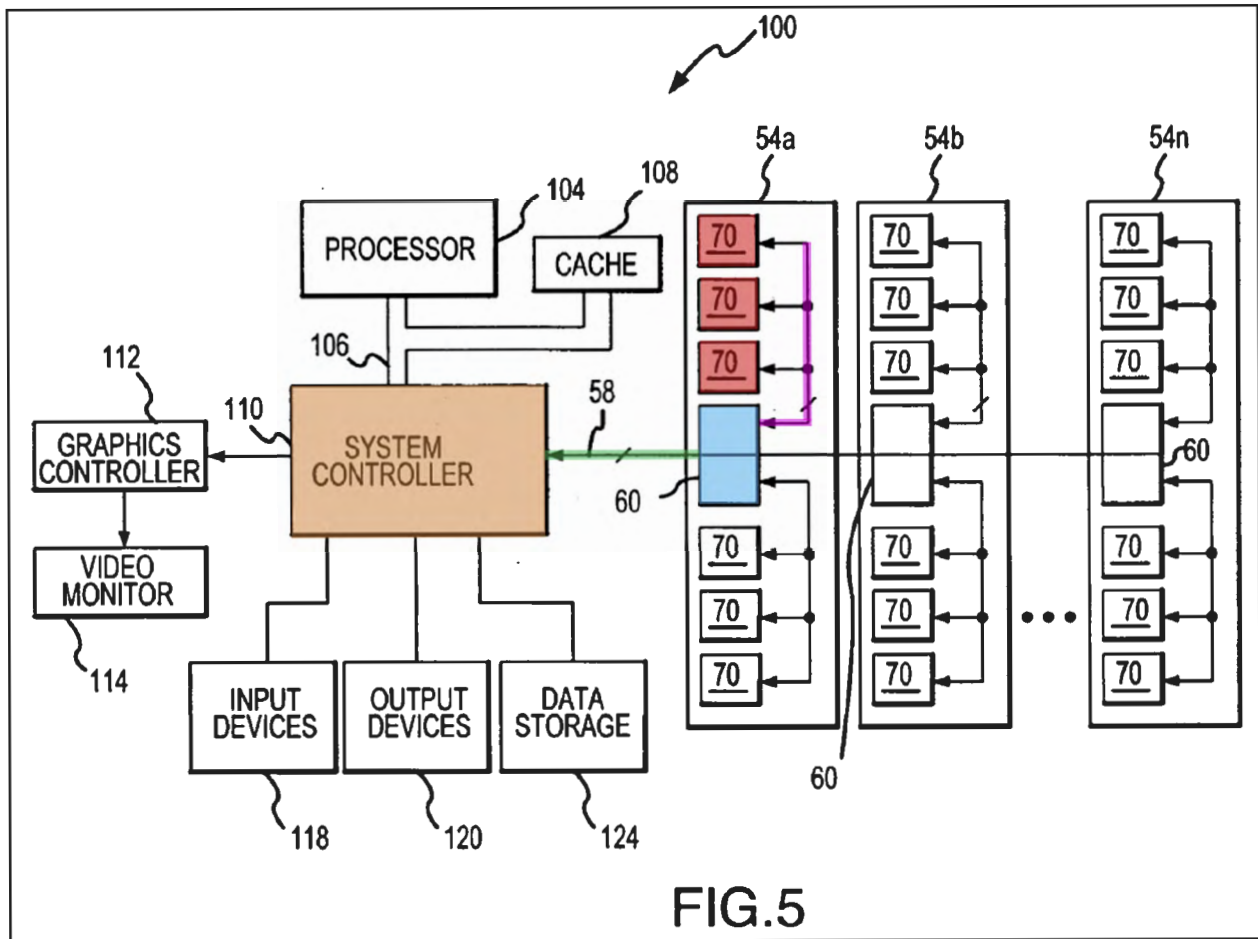


Excerpt from Lee, FIG. 2 (annotated)

32. Lee describes the configurability of its memory system: “In operation, a non-volatile register 98 in the memory module 54 is programmed to configure the memory hub 60 depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]. First, in the “high memory bandwidth” mode, “the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access.” *Id.* These “128 bits of data” from all of the memory devices 70 “can be coupled through the high-speed link 58 by either

increasing the speed of the link 58 or the size of the data word coupled through the link 58,” *e.g.*, such that “in the high-speed mode, a 128-bit data word may be coupled through the link 58,” or “[a]lternatively, the link 58 may transfer only a 32-bit data word, but it may operate at four times the speed of the memory devices 70.” *Id.* Second, in the “high memory depth mode, only one rank 74, 80, 86, 88 may be addressed at a time.” *Id.*, [0018]. In this mode, “only 32 bits of data will be coupled to or from the memory module 54 with each memory address,” but “the address space is 4 times deeper than the address space in the high bandwidth mode.” *Id.*

33. Lee’s FIG. 5, *infra*, illustrates a computer system implementing Lee’s configurable memory system 50. *See* EX1004, [0023]. In this system, the controller that is coupled to the memory hubs 60 of the memory modules 54 is a “system controller 110” (orange). EX1004, [0025]. The system controller facilitates access to the memory modules by the processor 104 of the computer system. *Id.*



Excerpt from Lee, FIG. 5 (annotated)

34. Lee is from the same field of endeavor (*e.g.*, memory systems) as the '942 Patent. *See* EX1001, 1:17-25; EX1004, [0001].

35. Also, Lee is pertinent to the problem the '942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, "lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability"). *See* EX1001, 1:17-25; EX1004, [0001]. For instance, Lee's memory systems are architected to enable high speed, configurable memory access, which is relevant to

development of “high speed” memory systems with “higher data transmission efficiency.” *See* EX1004, [0016]-[0017]; EX1001, 1:17-25.

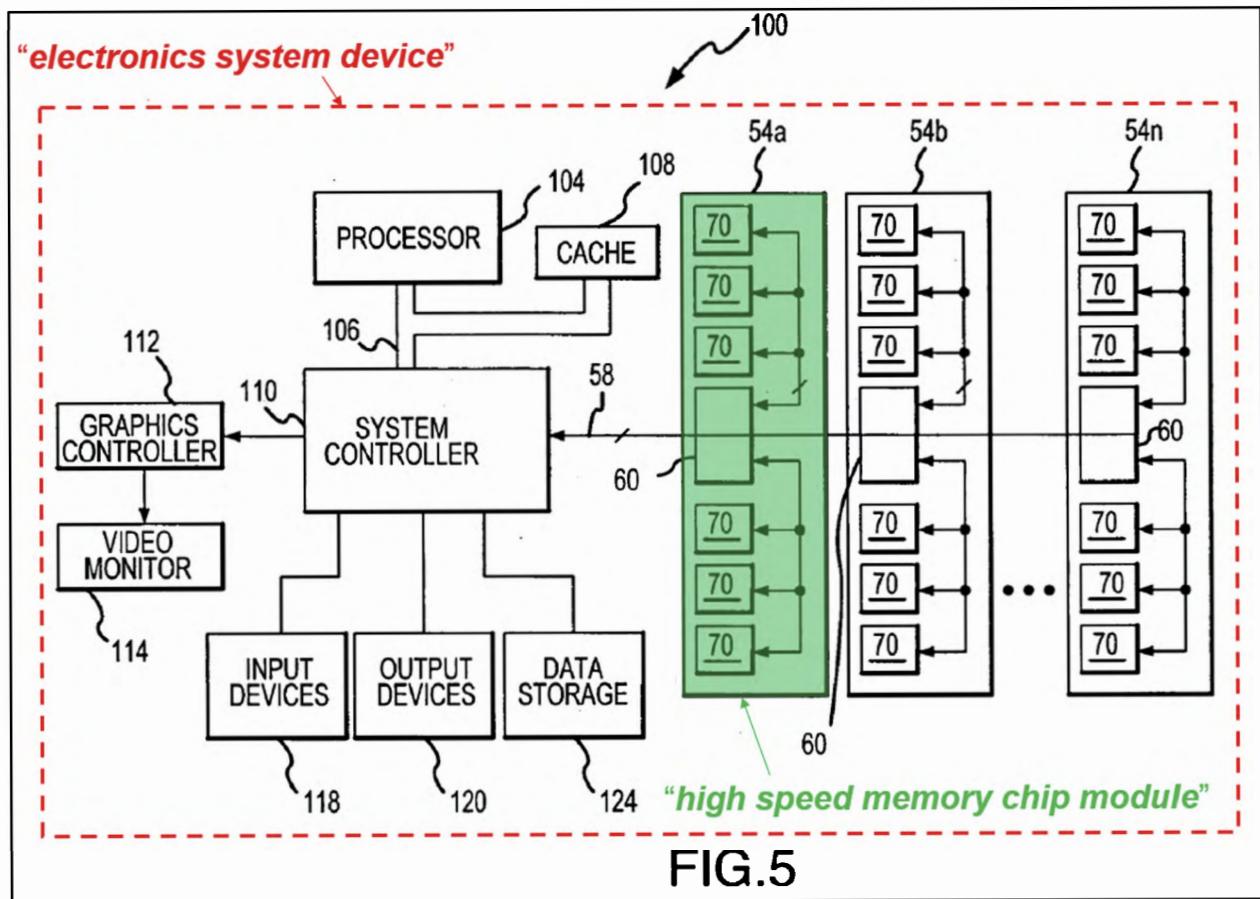
2. Analysis of claims

36. For the reasons below, claim 19 is obvious over Lee.

(a) Claim 19

[19pre]: A electronics system device with a high speed memory chip module, the device comprising:

37. Lee’s “computer system 100” corresponds to the claimed *electronics system device*, as illustrated in FIG. 5, which I have reproduced and annotated below. EX1004, [0023]; *see* claim 28.



Excerpt from Lee, FIG. 5 (annotated)

38. This computer system includes a “memory system 50” that is illustrated in more detail in FIG. 2. The memory system “includes a controller 52 coupled to several memory modules 54a, b ... n through a high-speed link 58,” where each memory module includes “memory devices 70,” such as “dynamic random access memory devices (‘DRAMs’).” *Id.*, [0015]-[0016], [0023]; *see* Abstract (“A computer system includes a controller coupled to a plurality of memory modules”), [0014] (“FIG. 5 is a block diagram of a computer system using the memory system of FIG. 2”), FIG. 2. Each of the memory modules 54 of the

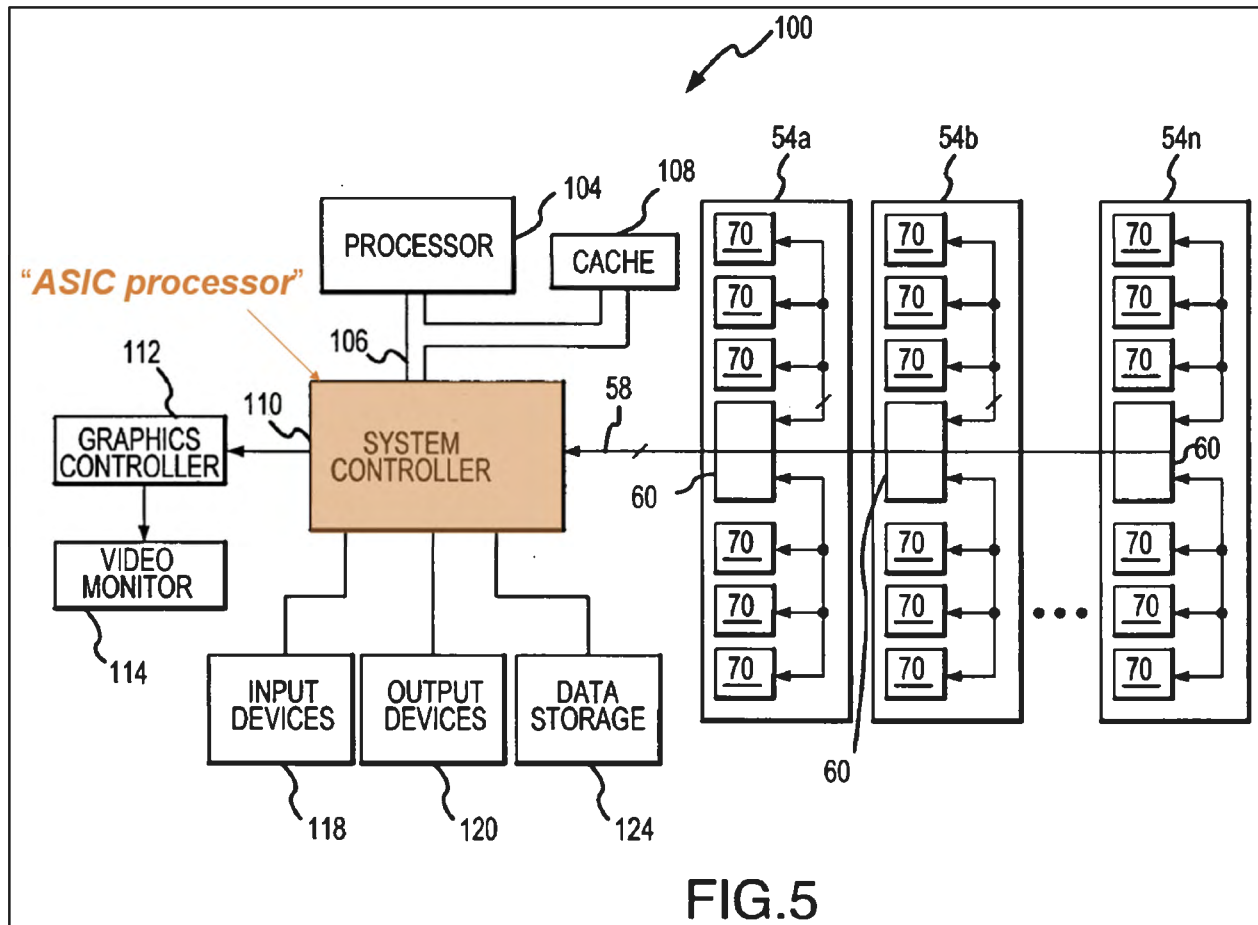
memory system (*e.g.*, memory module 54a, which I have highlighted above in green) corresponds to a ***memory chip module***, as claimed, *e.g.*, because each module includes memory chips, such as DRAMs.

39. Lee's memory modules are coupled to the controller "through a high-speed link," such as "a bus formed by multiple conductors, an optical communication link, an[] RF communication link, or some other type of high-speed communication link." EX1004, [0015]. For instance, data can be coupled through the high-speed link "at a rate of 2 GB/sec," "1 GB/sec," or "500 B/sec." EX1004, [0017]. Given this description of the high-speed nature of Lee's system, Lee's memory modules can be considered ***high speed memory modules***, as claimed.

[19a] an ASIC processor;

40. Lee's computer system includes "a system controller 110, which is also sometimes referred to as a 'North Bridge' or 'memory controller.'" EX1004, [0023]. I have highlighted the controller orange in FIG. 5, reproduced below. A POSITA would have understood Lee's North Bridge controller to be an ***ASIC processor***, given that this is how North Bridge controllers are typically implemented. For instance, Reeves explains that "Northbridge 14 is generally considered an application specific chip set, or application specific integrated circuit (ASIC) that provides connectivity to various buses, and integrates other system

functions such as memory interface.” EX1010, 5:30-33. Similarly, Bruno indicates that a North Bridge is an example of an ASIC: “an ASIC die having data routing functionality, such as a north bridge.” EX1011, [0032].



Excerpt from Lee, FIG. 5 (annotated)

41. Alternatively or additionally, a POSITA would have found it obvious to implement Lee’s North Bridge system controller 110 as an *ASIC processor*, for a number of reasons.

42. First, ASICs provide performance advantages that would have driven a POSITA to use an ASIC for implementation of Lee’s North Bridge controller.

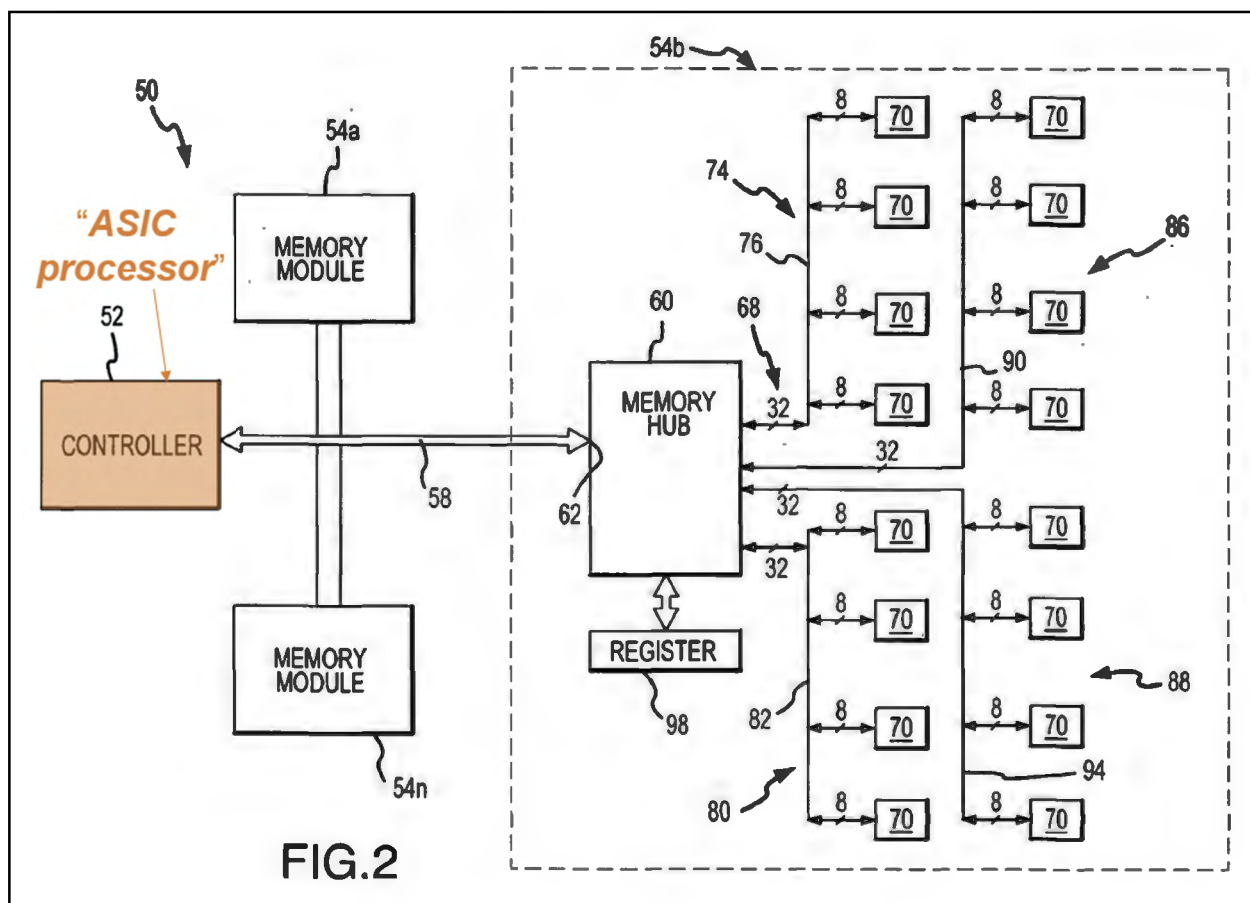
ASIC chips are custom-built to perform a specific task. EX1031, 384. As a result of this targeted design, they are capable of high-speed, low-energy operation. In addition, they are compact and inexpensive. *See* EX1031, 385 (listing advantages of ASICs, including “cost effective solution, low design effort with respect to time and cost; high performance, i.e., functionality, speed; low power dissipation; small volume and weight; high reliability; low cost for mounting and test”).

43. Second, there is a finite number of ways to implement a North Bridge controller: *e.g.*, as an ASIC or as a general-purpose chip. The results of the implementation of the North Bridge controller as an ASIC would have been predictable, and this implementation would likely have been successful given that predictability.

44. Third, the implementation of Lee’s North Bridge controller as an ASIC is merely an application of known techniques (specifically, an ASIC memory controller) to a known system (Lee’s memory system), and it yields predictable results (that is, a memory system in which the controller is an ASIC).

45. A POSITA would have expected success in implementing Lee’s North Bridge system controller as an ASIC processor because, as I noted above, it was conventional to implement North Bridge controllers as ASICs, *e.g.*, as indicated by Reeves and Bruno. *See* EX1010, 5:30-33; EX1011, [0032].

46. As I mentioned earlier, Lee's FIG. 5, which illustrates the North Bridge ASIC processor, "is a block diagram of a computer system using the memory system of FIG. 2." EX1004, [0014]; *see* [0023] ("A computer system 100 using the memory system 50 shown in FIG. 2 is shown in FIG. 5"). FIG. 2, reproduced below, provides additional detail of this memory system, which "includes a controller 52 coupled to several memory modules 54*a*, *b* ... *n* through a high-speed link 58." EX1004, [0015]. It is my opinion that the controller 52 of Lee's FIG. 2 (highlighted in orange) is also a North Bridge controller, consistent with the North Bridge controller 110 of Lee's FIG. 5. That is, the controller 52 of FIG. 2 is *an ASIC processor*. This is because Lee explicitly indicates the correspondence between FIG. 2 and FIG. 5 systems (*i.e.*, that the memory system of FIG. 2 is used in the computer system of FIG. 5). This is also because of the evident similarity in structure between the two figures: the controller 110 of FIG. 5 is connected to the memory hub 60 of the memory module 54*a* via the high-speed link 58, just like the controller 52 is connected to the memory hub 60 via the high-speed link 58 in FIG. 2. *See* EX1004, [0015]. Alternatively/additionally, it is my opinion a POSITA would have found it obvious to implement Lee's FIG. 2 controller 52 as an ASIC processor given Lee's teachings of the same in the similarly structured FIG. 5 system, and given the advantages of ASIC processors I previously discussed.

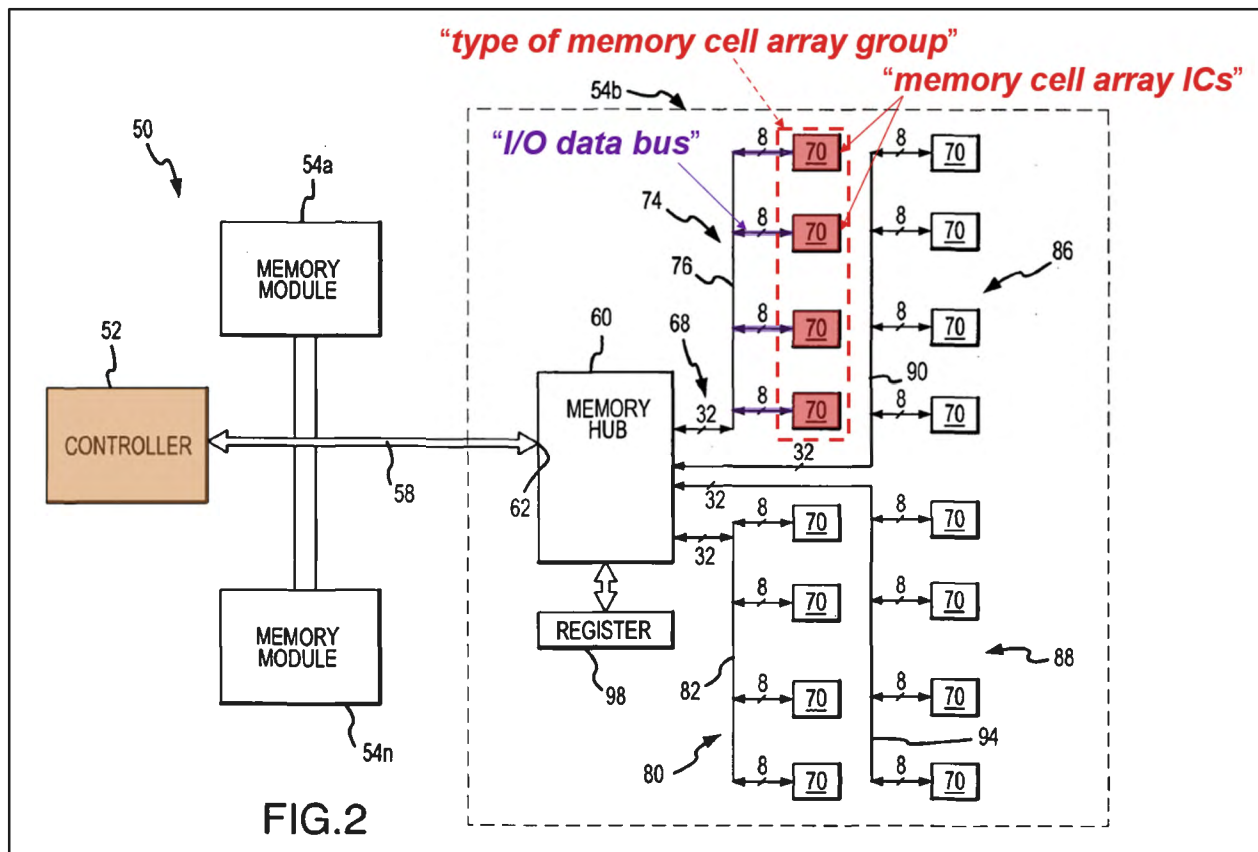


Excerpt from Lee, FIG. 2 (annotated)

[19b] a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs, each of the memory cell array ICs has an (I/O) data bus; and

47. Lee's memory system includes "several memory modules 54a, b ... n," with each memory module including "memory devices 70 [] divided into four groups or 'ranks.'" EX1004, [0016]; see Abstract ("a plurality of memory modules each of which includes ... a plurality of memory devices divided into a plurality of ranks"), claim 1, claim 13, claim 28, FIG. 5.

48. Lee's memory devices 70 (some of which I have highlighted in red in FIG. 2, reproduced below) correspond to the *memory cell array ICs* of claim 19. For instance, this is because Lee's memory devices 70 are integrated circuit memory devices: "The memory devices 70 may be, for example, dynamic random access memory devices ('DRAMs') or some other type of memory devices." EX1004, [0016]; *see* claim 11 ("the memory devices comprises dynamic random access memory devices"), claim 12. DRAM devices (as well as other types of memory devices) are *integrated circuits (ICs)*. For instance, Tsern refers to "[i]ntegrated circuit memory devices" such as DRAM, SRAM, and flash memory. EX1005, 12. And Liao describes "memory die such as NAND flash memory die ... [or] other types of semiconductor die ... such as for example NOR, DRAM and various other memory die." EX1016, 4:56-60.



Excerpt from Lee, FIG. 2 (annotated)

49. In Lee’s system, “the memory devices 70” (corresponding to the claimed *memory cell array ICs*) “are divided into four groups or ‘ranks.’” EX1004, [0016]. I have outlined one group in dashed red lines in FIG. 2. Each group/rank of memory devices corresponds to the claimed *type of memory cell array group* that *comprises multiple memory cell array ICs* at least because it is a group of memory cells (e.g., a group of memory devices 70). For instance, “a first rank 74” (outlined in red) “includes four memory devices 70” (i.e., four *memory cell array ICs*). EX1004, [0016]. Similarly, each of the second rank 80, third rank 86, and fourth rank 88 is a type of memory cell array group that contains four

memory devices, *i.e.*, a ***type of memory cell array group*** that ***comprises multiple memory cell array ICs***. *See id.*, [0016], claim 13 (“a plurality of memory devices arranged in a plurality of ranks”), claim 1, claim 28, FIG. 5. Alternatively or additionally, the multiple groups/ranks together (*i.e.*, the first, second, third, and fourth ranks together) correspond to a ***type of memory cell array group***.

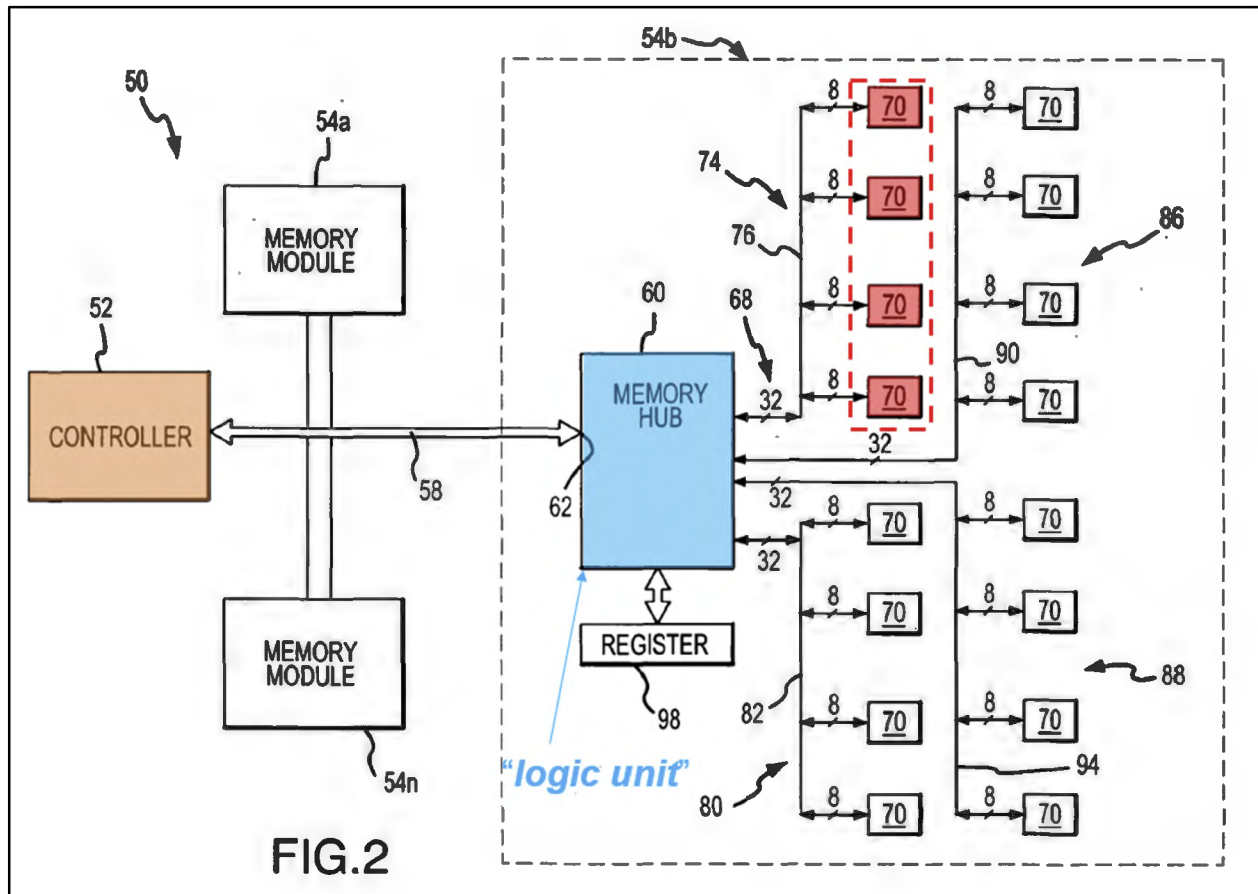
50. Each memory device 70 (***memory cell array IC***) has “an 8-bit data bus.” EX1004, [0016]. This data bus, which I have marked in purple for the four memory devices of the first rank, corresponds to the claimed (***I/O***) ***data bus***.

[19c] a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with¹ the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an (I/O) data bus of each of the memory cell array ICs,

51. Each memory module in Lee’s memory system includes “a memory hub 60,” highlighted in blue in FIG. 2, *infra*. EX1004, [0016]; *see* [0009], [0017]-[0020], claims 1-3. The memory hub corresponds to the claimed ***logic unit*** at least

¹ As best understood, I interpret the phrase “transmitting a first set of parallel data **along with** the memory cell array ICs” as “transmitting a first set of parallel data **to/from** the memory cell array ICs.”

because it is “programmable to configure the memory module in a plurality of data formats,” *i.e.*, programmable to carry out logic tasks. EX1004, claim 1; *see* [0009], [0017]-[0020], claims 4-5.



Excerpt from Lee, FIG. 2 (annotated)

52. The memory hub 60 is coupled to the memory devices 70 through “a bus system 68,” which enables access to the memory devices of each rank “through a respective bus system” 76, 82, 90, 94. EX1004, [0016]. That is, the memory hub (*logic unit*) is *for accessing* the memory devices (*the type of memory cell array group*). Each of these bus systems 76, 82, 90, 94 individually

corresponds to the claimed ***first transmission bus***. Alternatively or additionally, the bus system 68 (which is composed of the four individual bus systems 76, 82, 90, 94) corresponds to the ***first transmission bus***. I discuss each of these options in turn.

*Each of Lee's bus systems individually corresponds to a ***first transmission bus****

53. Each rank of memory devices is coupled to the memory hub 60 by a respective bus system 76, 82, 90, 94. I have highlighted the bus system 76 in pink in FIG. 2, below. I sometimes refer to each of these rank-specific bus systems as individual bus systems. The bus system for a single rank (*i.e.*, an individual bus system) corresponds to the claimed ***first transmission bus***, and the memory hub (***logic unit***) can ***access*** the memory cell array ICs in that rank through that bus system. For instance, the first rank 74 of memory devices (a ***type of memory cell array group***) are “coupled to the memory hub 60 through a first bus system 76 having a 32-bit data bus,” *i.e.*, through a ***first transmission bus***. EX1004, [0016]. A similar situation applies to the coupling between the memory hub 60 and the other ranks of memory devices. For instance, “a second rank 80 containing four memory devices 70 are coupled to the memory hub 60 through a second bus system 82 having a 32-bit data bus. Similarly, third and fourth ranks 86, 88 are each coupled to the memory hub 60 through respective bus systems 90, 94 each

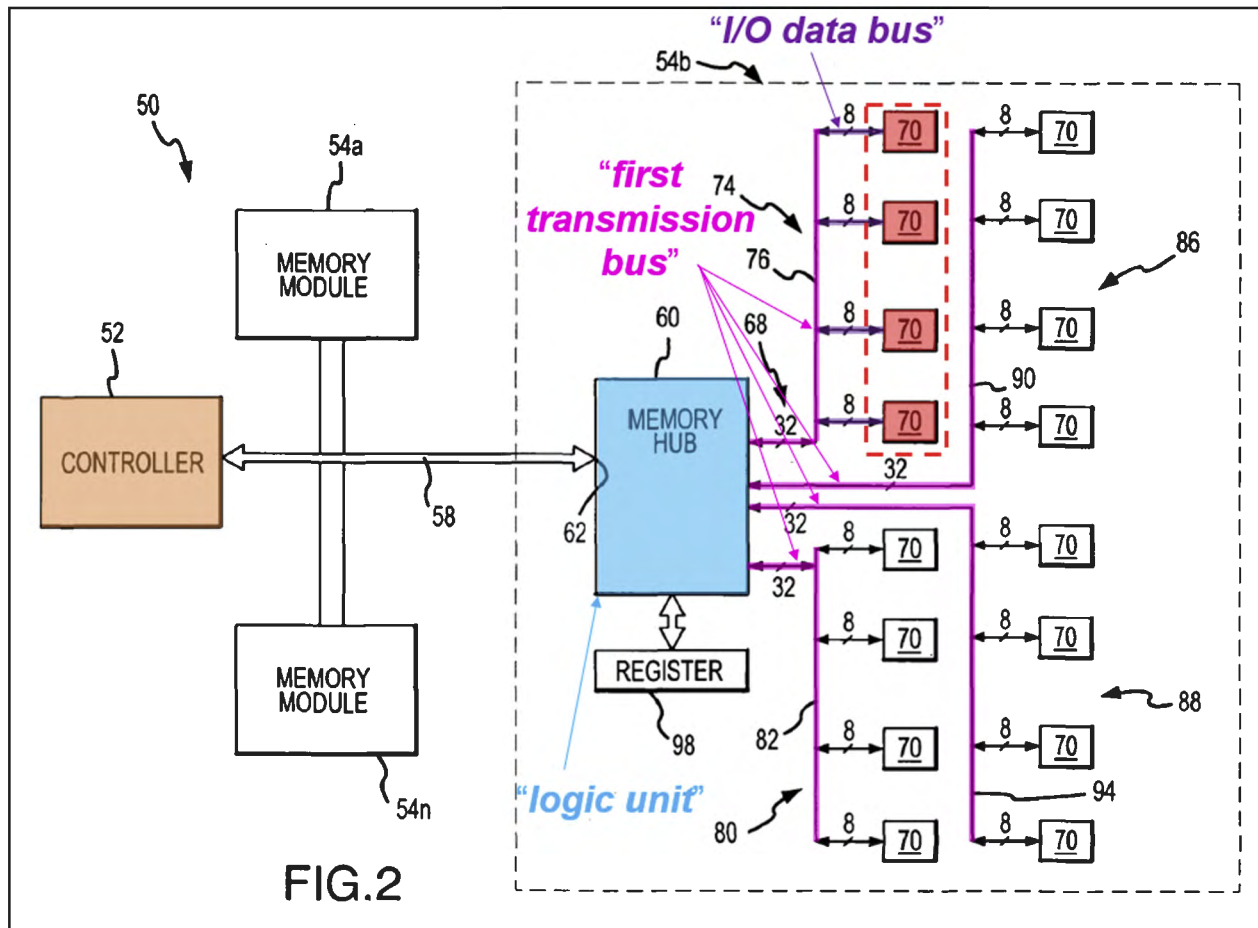
to the bus system, such that “the four memory devices 70” of each rank “together provide 32 bits for the 32-bit data buses.” EX1004, [0016]. The bus system for an individual rank is a “32-bit data bus,” *i.e.*, 32 bits of data (8 from each memory device) are carried on ***parallel*** on the bus system. EX1004, [0016]; *see* [0017] (“for a high memory bandwidth, the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices”), [0018] (“In the high memory depth mode, only one rank 74, 80, 86, 88 may be addressed at a time”), claim 6 (“the memory devices in each rank are collectively operable to read or write N-bit data words”), [0009], [0019], claims 2, 3, 4, and 7. That is, the data transmitted on the bus system for an individual rank are 32 bits of parallel data (corresponding to the claimed ***first set of parallel data***).

55. The data bus for each memory device (corresponding to the claimed (***I/O data bus***), purple in FIG. 2), as I previously discussed) is an “8-bit data bus,” *i.e.*, has a ***bus width*** of 8 bits. *See* EX1004, [0016] (“each of the memory devices 70 have an 8-bit data bus”), FIG. 2. The first bus system 76 (corresponding to the claimed ***first transmission bus***, pink in FIG. 2) is a “32-bit data bus,” *i.e.*, has a ***bus width*** of 32 bits. *See* EX1004, [0016] (“a first bus system 76 having a 32-bit data bus ... a second bus system 82 having a 32-bit data bus ... bus systems 90, 94 each having a 32-bit data bus”). That is, the bus widths of the first bus system and the I/O data bus satisfy the claimed limitation that the ***bus width of the first***

transmission bus (32 bits) is *wider than the bus width of each I/O data bus* (8 bits).

Lee's bus system 68 corresponds to the *first transmission bus*

56. In an alternative or additional mapping of Lee to claim 19, Lee's "bus system 68" (pink in FIG. 2, below) as a whole corresponds to the claimed *first transmission bus*. EX1004, [0016]. The bus system 68 is composed of the four individual bus systems 76, 82, 90, 94 for the four ranks of memory devices. EX1004, [0016] ("bus system 68 coupled to several memory devices 70"). Access to the memory devices is provided through the bus system 68, *e.g.*, because each bus system provides the memory hub (*logic unit*) with access to the memory devices in its corresponding rank. The bus system 68 is *used for transmitting data along with (to/from) the memory cell array ICs* at least because each individual bus system 76, 82, 90, 94 of the bus system 68 is used for transmitting data to/from the memory cell array ICs, as I discussed above. See EX1004, [0016]-[0019].



Excerpt from Lee, FIG. 2 (annotated)

57. Each individual bus system transmits 32 bits of *parallel data*, as I discussed above. Thus, the data transmitted on the collective bus system 68 (*first transmission bus*) correspond to *a first set of parallel data*, because it is composed of 4 sets of parallel data on the four individual bus systems. See EX1004, [0016]-[0019]. Moreover, the individual bus systems 76, 82, 90, 94 are connected in parallel to the memory hub, which allows the memory hub to “address[] all of the memory devices simultaneously so that 128 bits of data are written to or read from the memory devices.” EX1004, [0017]. This means that the parallel data

transmitted on one of the individual bus systems 76, 82, 90, 94 is transmitted in parallel to the data transmitted on the other three bus systems. Again, that makes the data transmitted on the collective bus system 68 a ***first set of parallel data***. See claim 3 (“the memory module is operable to [] address all of the ranks of memory devices in a first mode to simultaneously couple data to or from all of the memory devices in the memory module”), claim 4. Under either explanation, the data transmitted on the collective bus system 68 (***first transmission bus***) are “128 bits of data” (***a first set of parallel data***) transmitted “simultaneously” and in parallel on the four individual bus systems. EX1004, [0017].

58. The bus width of the bus system 68 is equal to the total bus width of the four constituent bus systems, each of which is 32 bits wide, as I discussed above. See EX1004, [0016], FIG. 2. That is, the bus width of the bus system 68 (***bus width of the first transmission bus***) is 128 bits, *i.e.*, ***wider than*** the 8-bit bus width of each I/O data bus. See EX1004, [0016], FIG. 2.

[19d] wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus, and transmits the second set of parallel data to the ASIC processor;

59. Lee’s system includes a “high-speed link 58” (marked in green in FIG. 2, below) coupled to the memory hub 60. EX1004, [0016]. Lee describes

that “[t]he high-speed link 58 may be a bus formed by multiple conductors, an optical communication link, and [sic] RF communication link, or some other type of high-speed communication link.” *Id.*, [0015]; *see* [0017]-[0019], [0025], claim 13. The high-speed link corresponds to the claimed ***second transmission bus***.

Excerpt from Lee, FIG. 2 (annotated)

through the link 58.” EX1004, [0017]. This 128-bit data word transmitted on the link 58 constitutes 128 bits of parallel data, *i.e.*, it corresponds to the ***second set of parallel data***. In another example, Lee’s high-speed link can “couple 64-bit data words” or “32-bit data word[s].” *Id.* In these cases, the 64-bit data word (64 bits of parallel data) or 32-bit data word (32 bits of parallel data) corresponds to the ***second set of parallel data***. *Id.* That the data transmitted on the high-speed link 58 are parallel data (*e.g.*, 128 bits, 64 bits, or 32 bits of parallel data) is made apparent by Lee’s description that the high-speed link has “a capacity for coupling data having a predetermined bus width between the controller 52 and each memory module.” *Id.*, [0015].

61. Lee describes that the high-speed link “has a capacity for coupling data ... between the controller 52 and each memory module 54.” EX1004, [0015]. That is, the high-speed link (which corresponds to the claimed ***second transmission bus***) transmits data (specifically, the ***second set of parallel data***) to the controller 52 (orange above), which corresponds to the claimed ***ASIC processor*** (as I discussed for element [19a]). *See also* claim 13 (“a communications link coupling the input/output port of the controller to the input/output ports of the memory hubs in the respective memory modules”).

62. It is my opinion that a POSITA would have found obvious that Lee’s memory hub (corresponding to the claimed ***logic unit***) is ***used for converting the***

first set of parallel data (i.e., the data on the first transmission bus) *into the second set of parallel data* (i.e., the data on the second transmission bus). This is the case when a single one of Lee's bus systems corresponds to the claimed first transmission bus (and thus when the data transmitted on an individual one of Lee's bus systems corresponds to the claimed *first set of parallel data*). This is also the case when Lee's collective bus system 68 corresponds to the claimed first transmission bus (and thus when the data transmitted on Lee's collective bus system 68 corresponds to the claimed *first set of parallel data*). I discuss each of these in more detail in the following paragraphs.

Conversion of data when an individual one of Lee's bus systems corresponds to the claimed first transmission bus (and thus when the data transmitted on an individual one of Lee's bus systems corresponds to the claimed first set of parallel data)

63. This section addresses the case in which one of Lee's individual bus systems (e.g., the bus system 76) corresponds to the claimed *first transmission bus*, and the 32 bits of parallel data transmitted on the bus system 76 thus corresponds to the claimed *first set of parallel data*.

64. Lee's system has two operation modes: high memory bandwidth mode and high memory depth mode. See EX1004, [0017]. In high memory bandwidth mode, "the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access." EX1004, [0017]. This means that, when reading

from the memory devices, the memory hub receives, at once, multiple sets of parallel data transmitted along the multiple bus systems 76, 82, 90, 94, one set of data from each rank of memory devices. *See* EX1004, [0016]-[0017], FIG. 2. Specifically, 32 bits are received through each of the four bus systems 76, 82, 90, 94. *Id.*, [0017]; *see* [0019] (describing another option in which two ranks (rather than all four) are accessed simultaneously: “one pair of ranks 74, 80 are simultaneously accessed and the other pair of ranks 86, 88 are simultaneously accessed”). These simultaneously received 128 bits of data include the 32 bits (*first set of parallel data*) transmitted on the first bus system 76, as well as 32 bits transmitted on each other bus system 82, 90, 94.

65. Lee then describes two implementations for transmission of that 128 bits of parallel data on the high-speed link 58 (corresponding to the claimed *second transmission bus*), as I discuss in the following paragraphs. *See* EX1004, [0017]. Both involve *converting the first set of parallel data* (e.g., the data transmitted on the first bus system 76) *into the second set of parallel data* (the data transmitted on the high-speed bus 58).

66. One way Lee implements “high memory bandwidth” mode is described as follows: “128 bits of data are written to or read from the memory devices” (that is, 32 bits of parallel data through each of the four bus systems 76, 82, 90, 94, as I discussed above). However, “the link 58 may transfer only a 32-bit

data word” or a “64-bit data word[.]” EX1004, [0017]. This 32-bit or 64-bit data word corresponds to the *second set of parallel data*, as I also discussed above. In order to receive 128 bits of data simultaneously through multiple bus systems 76, 82, 90, 94, and transmit that data in a 64- or 32-bit word through a single bus system (*i.e.*, the high-speed link 58), a POSITA would have found obvious that the data received from the multiple bus systems 76, 82, 90, 94 (including the 32-bit *first set of parallel data* from the bus system 76) would have to be *converted* to the data of a different bit width transmitted on a single bus (*i.e.*, to the *second set of parallel data*). For instance, this conversion can be done by operations involving multiplexing.

67. In more detail, in this implementation, the bit width of the parallel data that is simultaneously received through the multiple bus systems (*i.e.*, a bit width of 128 bits) is different from the bit width of the parallel data that is then transmitted through the high-speed link 58 (*e.g.*, 32-bit words (bit width of 32 bits) or 64-bit words (bit width of 64 bits)). The processing of receiving data of one bit width (128 bits) from one bus system including multiple buses and then transmitting that same data in a different bit width (64 bits or 32 bits) on a different, single bus involves *converting* the received data (*i.e.*, 128 bits of received data, including the 32-bit data corresponding to *the first set of parallel data*) to the transmitted data (*second set of parallel data*).

68. An example of this conversion is described in Nakamura. Nakamura describes “a parallel-to-parallel converter for converting an ‘m’-bit parallel signal into an ‘n’-bit parallel signal.” EX1019, Abstract. That is, Nakamura describes that the process of changing a signal of one bit width (e.g., 128 bits, in the Lee example) to a signal of a different bit width (e.g., 64 bits or 32 bits) involves *converting* the data from the initial bit width to the different bit width.

69. Another way Lee implements “high memory bandwidth” mode is described as follows: “[t]he 128 bits of data [are] coupled through the high-speed link by [] increasing ... the size of the data word coupled through the link 58.” EX1004, [0017]. For instance, a “128-bit data word” (*second set of parallel data*) “may be coupled through the link 58.” EX1004, [0017]. That is, Lee’s memory hub (*logic unit*) receives 128 bits of data through four distinct bus systems (including the 32-bit *first set of parallel data*), and *converts* that received data to a “128-bit data word” for transmission on a single bus system: the high-speed link 58. EX1004, [0017]; *see* [0019] (“64 bits of data are coupled through the high-speed link 58”). A POSITA would have found obvious that receiving data simultaneously through multiple bus systems and then transmitting that data through a single bus system involves *converting*, by the memory hub (*logic unit*) the data received from the multiple bus systems (i.e., 128 bits of simultaneously received data, including the 32-bit *first set of parallel data* transmitted on the first

bus system 76) into the data transmitted on the single high-speed link 58 (*the second set of parallel data*). For instance, converting parallel data received simultaneously from multiple buses into parallel data transmitted on a single bus involves processes such as multiplexing.

Conversion of data when the collective bus system 68 corresponds to the claimed first transmission bus (and thus when the data transmitted collectively on bus system 68 corresponds to the claimed first set of parallel data)

70. This section addresses the case in which Lee’s bus system 68 (that includes the four individual bus systems) corresponds to the claimed *first transmission bus*, and the 128 bits of parallel data transmitted on the bus system 68 thus corresponds to the claimed *first set of parallel data*.

71. When operating in “high memory bandwidth” mode, the “128 bits of data” that are “simultaneously” “read from the memory devices” collectively correspond to the *first set of parallel data*, as I discussed above for [19c].

72. In one implementation, the 128 bits are transmitted simultaneously on the collective bus system 68, but “the link 58 may transfer only a 32-bit data word” or a “64-bit data word[]” (*second set of parallel data*). EX1004, [0017]. Again, like I discussed above, a POSITA would have found obvious that the memory hub receiving data of one bit width simultaneously through multiple bus systems and then transmitting that data, now of a different bit width, through a single bus system involves *converting* the received data (*first set of parallel data*) to the

transmitted data (*second set of parallel data*), e.g., by multiplexing the received data. In order to receive data of one bit width (128 bits on the bus system 68) and then transmit that same data in a different bit width (one 32- or 64-bit word on the high-speed link 58) a POSITA would have found obvious that the received data (*first set of parallel data*) would have to be *converted* to the transmitted data (*second set of parallel data*). See EX1004, [0017]. For instance, such a conversion of parallel data of one bit width to parallel data of another bit width is described by Nakamura. See EX1019, Abstract).

73. In another implementation described by Lee, these data are received through four individual bus systems (that together correspond to the claimed *first transmission bus*) and *converted* to a “128-bit data word” for transmission on a single bus system: the high-speed link 58. EX1004, [0017]; see [0019]. As I discussed above, POSITA would have found obvious that receiving data simultaneously through multiple bus systems and then transmitting that data through a single bus system involves *converting*, by the memory hub (*logic unit*) the data received from the multiple bus systems (*first set of parallel data*) into the data transmitted on the single high-speed link 58 (*second set of parallel data*), e.g., by multiplexing.

[19e] wherein the ASIC processor executes a predetermined function corresponding to the second set of parallel data while the ASIC processor is under

operating condition,

74. Lee describes that its controller 52 (corresponding to the claimed *ASIC processor*) is to “serve[] as a communications path to the processor 104 for a variety of other components,” including the memory modules 54. EX1004, [0024]. Specifically, “the system controller ... generate[s] memory requests that are coupled to the memory modules.” *Id.*, [0026]; *see* [0015] (“the high-speed link 58 also couples address and command signals from the controller 52 to the memory modules 54”), [0009] (“a controller operable to receive a memory request and to transmit a corresponding memory request to an input/output port”). The controller (*ASIC processor*) generating memory requests corresponds to *the ASIC processor executing a predetermined function*, *e.g.*, because the ASIC is programed/designed/configured to carry out this function.

75. Notably, an ASIC is a chip that is designed specifically to execute a predetermined function (*e.g.*, rather than being designed generically as a general-purpose chip). Thus, the function that is carried out by the ASIC controller is predetermined at least in the sense that the ASIC is designed to execute that function. This is described by Reiger, which explains that “[c]ompared with standard circuits an ASIC is designed and manufactured according to specifications resulting from its application.” EX1031, 384.

76. Generating a memory request by the controller (*ASIC processor*), such as a memory read or write request, results in data being transmitted along Lee's high-speed bus to or from the memory module. As I discussed above, these data transmitted along the high-speed bus correspond to the claimed second set of parallel data. That is, because the controller's generation of a memory request (corresponding to the claimed *executing a predetermined function*) results in transmission of the second set of parallel data, this functionality satisfies the claim requirement that the predetermined function *corresponds to the second set of parallel data*).

77. The controller can function only when it is powered on. A POSITA thus would have understood that the controller is capable of generating a memory request only when powered on (e.g., while it is *under operating condition*). Thus, Lee's system satisfies the claim requirement that the ASIC executes its predetermined function *while the ASIC processor is under operating condition*.

[19f] wherein bit width of the first set and the second set of parallel data are different.

Different bit widths when the data transmitted on one of Lee's bus systems corresponds to the first set of parallel data

78. As I discussed above, one mapping that satisfies the claimed *first set of parallel data* is the data transmitted on Lee's first bus system 76. The *bit width* of this *first set of parallel data* transmitted on the individual bus system 76 is 32

bits: “each of the memory devices 70 have an 8-bit data bus so that the four memory devices 70 together provide 32 bits for the 32-bit data buses.” EX1004, [0016]; *see* FIG. 2.

79. When Lee’s system is operated in “high memory bandwidth” mode, the high-speed link can be configured such that “a 128-bit data word may be coupled through the link 58.” EX1004, [0017]. That is, the data carried on the high-speed link (*i.e.*, the ***second set of parallel data***) can have a ***bit width*** of 128 bits. Lee’s high-speed link can alternatively be configured to “couple 64-bit data words.” EX1004, [0017]; *see* [0019] (“64 bits of data are coupled through the high-speed link 58 with each memory access”). That is, the data carried on the high-speed link (*i.e.*, the ***second set of parallel data***) can have a ***bit width*** of 64 bits. Either of these bit widths of Lee’s second set of parallel data—*e.g.*, 128 bits or 64 bits—is ***different*** from the 32-bit width of the first set of parallel data. *See* EX1004, claim 6 (“wherein the memory devices in each rank are collectively operable to read or write N-bit data words, and wherein the memory hub further comprises an input/output port that is operable to receive or transmit M*N-bit data words, where M is the number of ranks of memory devices in the memory module”).

Different bit widths when the data transmitted collectively on Lee's bus system 68 corresponds to the first set of parallel data

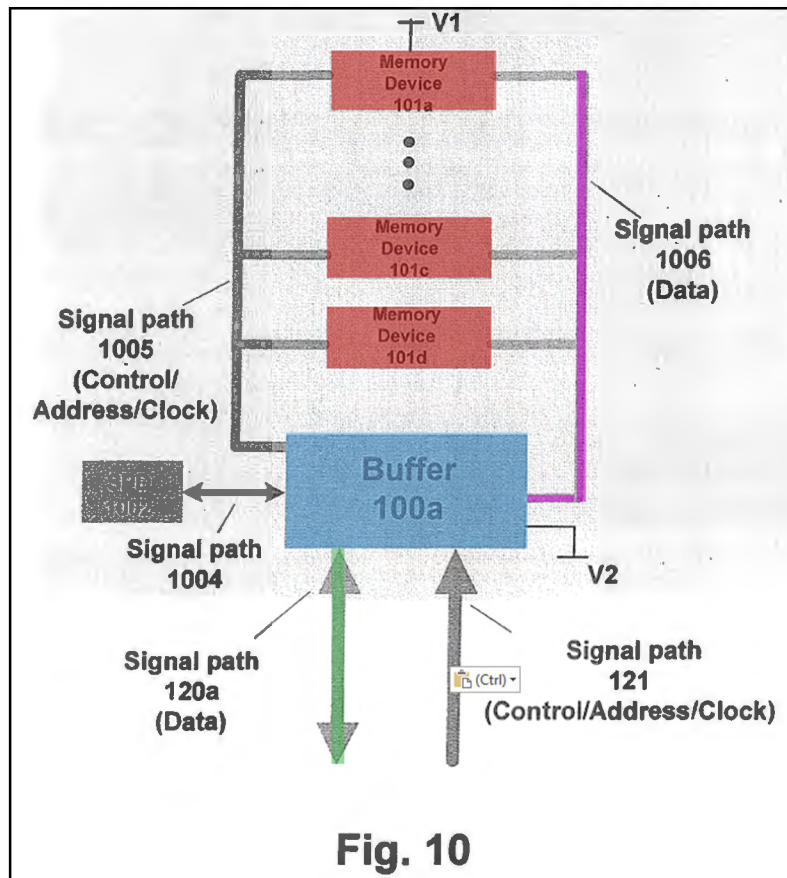
80. As I also discussed above, an alternative mapping that satisfies the claimed ***first set of parallel data*** is the data transmitted on Lee's collective bus system 68. Lee's "memory hub 60 addresses all of the memory devices 70 simultaneously" through bus system 68 "so that 128 bits of data are written to or read from the memory devices 70 each memory access." EX1004, [0017]. In this mapping, the bit width of the first set of parallel data corresponds to the bit width of the entire collective bus system 68, *i.e.*, the ***first set of parallel data*** transmitted through the bus system 68 has a ***bit width*** of 128 bits. EX1004, [0017].

81. When Lee's system is operated in "high memory bandwidth" mode, Lee's high-speed link can be configured to "couple 64-bit data words." EX1004, [0017]; *see* [0019] ("64 bits of data are coupled through the high-speed link 58 with each memory access"). That is, the data carried on the high-speed link (*i.e.*, the ***second set of parallel data***) can have a ***bit width*** of 64 bits. Lee's high-speed link can alternatively be configured to "transfer only a 32-bit data word." EX1004, [0017]. That is, the data carried on the high-speed link (*i.e.*, the ***second set of parallel data***) can have a ***bit width*** of 32 bits. Either of these bit widths of Lee's second set of parallel data—*e.g.*, 64 bits or 32 bits—is ***different*** from the 128-bit width of the first set of parallel data.

B. [Ground 1B]: Lee and Tsern Render Obvious Claims 19, 22, and 25-26

1. Tsern (EX1005)

82. Like Lee, Tsern relates to “topologies (data and/or control/address information)” of a memory system “between an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices.” EX1005, Abstract. One example of Tsern’s memory system is illustrated in Fig. 10, which I have reproduced and annotated below. This system includes “a plurality of integrated circuit memory devices 101a-d [highlighted in red] and a buffer 100a [highlighted in blue].” *Id.*, 22. “[D]ata may be transferred between the plurality of integrated circuit memory devices 101a-d and buffer 100a on a signal path 1006 (data),” marked in pink. *Id.* A “signal path 120a,” green, “transfer[s] data (read and write data)” between the buffer device 100a and “a memory module connector interface.” *Id.*, 12.



Excerpt from Tsern, Fig. 10 (annotated)

83. The components of Tsern’s buffer device 100a are illustrated in Fig. 18, reproduced below. *See* EX1005, 30. Signal data is provided to the buffer device 100a through a buffer interface 1103a, while an interface 1820b “transfer[s] data between buffer 100a and one or more memory devices.” *Id.*, 31-33. The interface is “programmable to access different memory widths,” such as “to connect to 16 ‘x4’ width memory devices, 8 ‘x8’ width memory devices or 4 ‘x16’ width memory devices.” *Id.*, 37. A multiplexer 1830 (orange) “perform[s] bandwidth-concentrating operations between buffer interface 100a and interface

1820b,” *e.g.*, “utiliz[ing] the combined bandwidth of multiple data paths [1006] coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” *Id.*, 33. The buffer interface 1103a includes a “[c]onfigurably serialization/deserialization circuit 1891,” *orange*, that “performs serialization and deserialization functions” on the data “depending upon a stored serialization ratio,” *e.g.*, depending on “memory device access width.” *Id.*, 38.

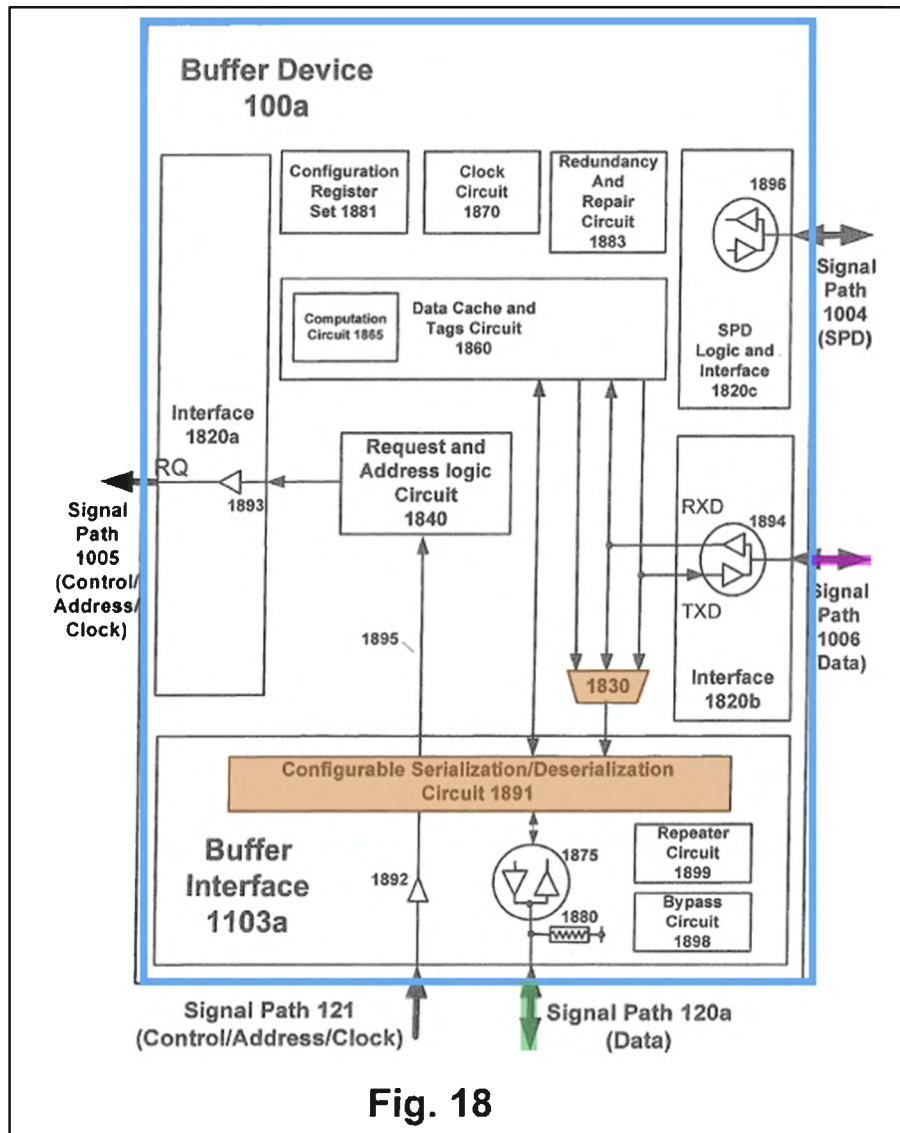


Fig. 18

Excerpt from Tsern, Fig. 18 (annotated)

84. Another of Tsern's buffer devices is buffer device 3600, shown in Fig. 36, reproduced below. The buffer device 3600 "operates similar to buffer 100a" in that it receives "read data via one or more signal paths 1006" (marked in pink) from memory devices and "in response, transmits corresponding signals to a master" along a signal path 120a (marked in green). EX1005, 68. As with buffer

100a, the buffer device 3600 includes an “interface 3611” that “can be segmented into at least three different configurations or segmentation modes: 1) Four 4-bit interfaces (4x4), 2) Two 4-bit interfaces (2x4) or 3) Two 8-bit interfaces (2x8),” which “allow[s] flexibility in memory module or memory stack configurations.” *Id.*, 69. The buffer device 3600 also includes “data path 3606 and data path router 3610,” both highlighted in orange, that “merge separate read data from more than one memory device into a single merged read data or read stream output at interface 3601,” *e.g.*, merging the read data from the memory devices received via the pink signal paths 1600 into a single data stream for transmission along the single data path 120a. *Id.*

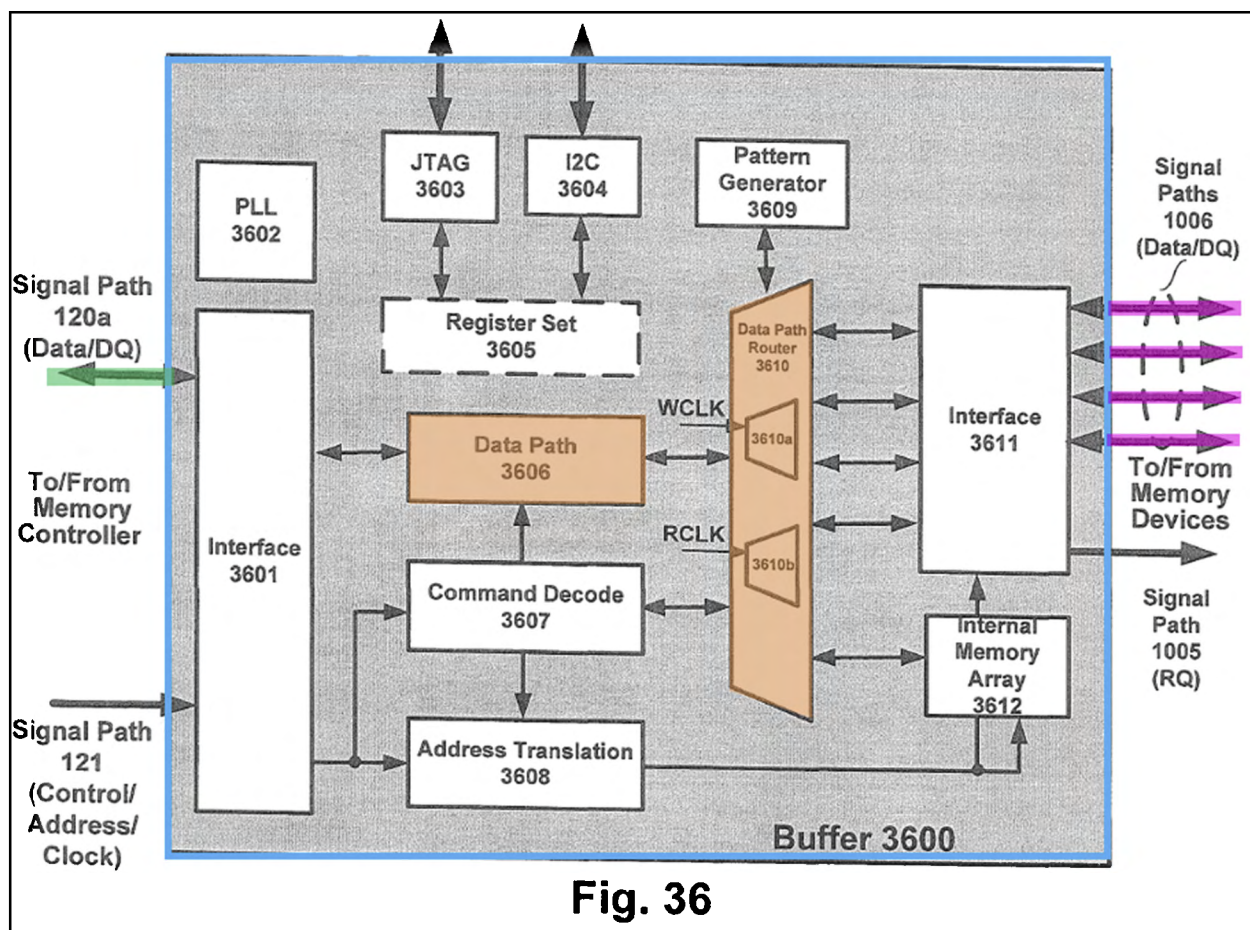
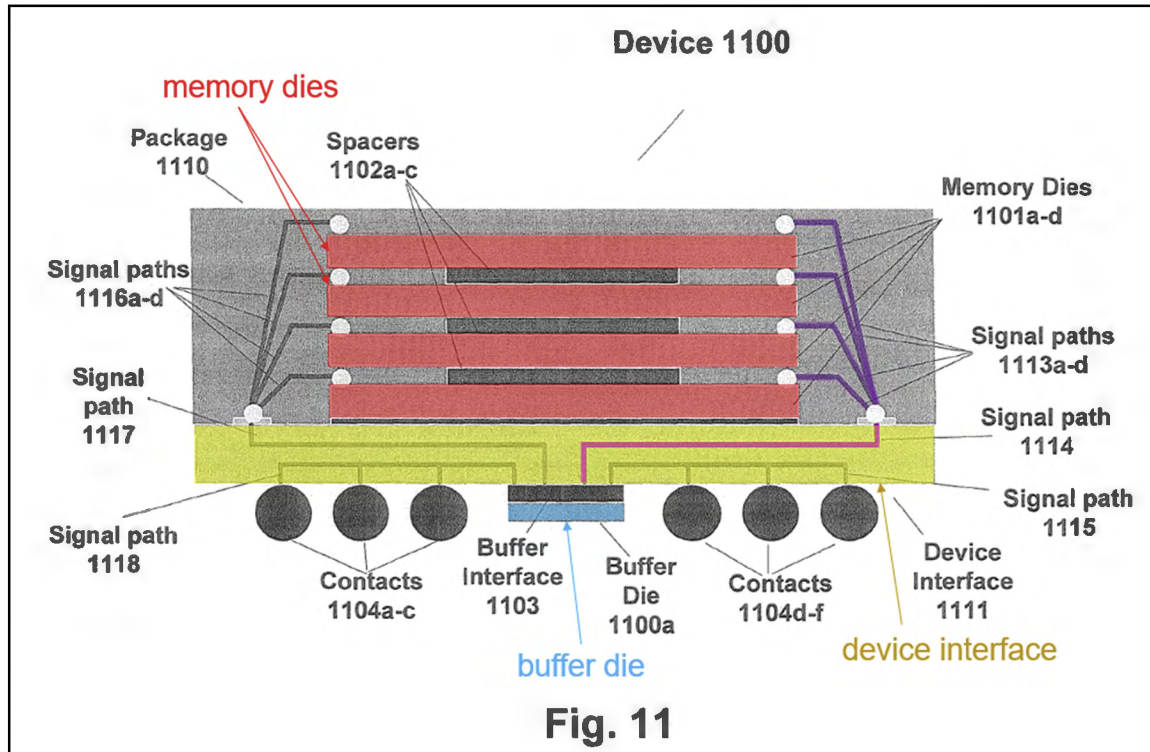


Fig. 36

Excerpt from Tsern, Fig. 36 (annotated)

85. Fig. 11, reproduced below, shows one way that the physical integrated circuit chips of Tsern's system can be assembled. This figure shows a package of the integrated circuit memory dies 1101a-d (shown in red) and buffer die 1100a (in blue) in a "stacked" arrangement. EX1005, 26. "Signals are [] transferred between a plurality of memory dies 1101a-d and buffer die 1100a" via signal paths 1113a-d (in purple) and signal path 1114 (in pink). "[S]pacers 1102a-c are positioned between integrated circuit memory dies 1101a-d ... to dissipate heat." *Id.* In addition, "buffer die 1100a is disposed away from" the memory die and

separated by a device interface 1111 (yellow) “to alleviate heat dissipation near the memory die.” *Id.*



Excerpt from Tsern, Fig. 11 (annotated)

86. Tsern is from the same field of endeavor (*e.g.*, memory systems) as the '942 Patent. *See* EX1001, 1:17-25; EX1005, Abstract.

87. Also, Tsern is reasonably pertinent to the problem the '942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25; EX1005, Abstract. For instance, Tsern’s

memory systems “enable configurable effective memory organization,” which is relevant to development of efficient memory systems. *See* EX1005, 6.

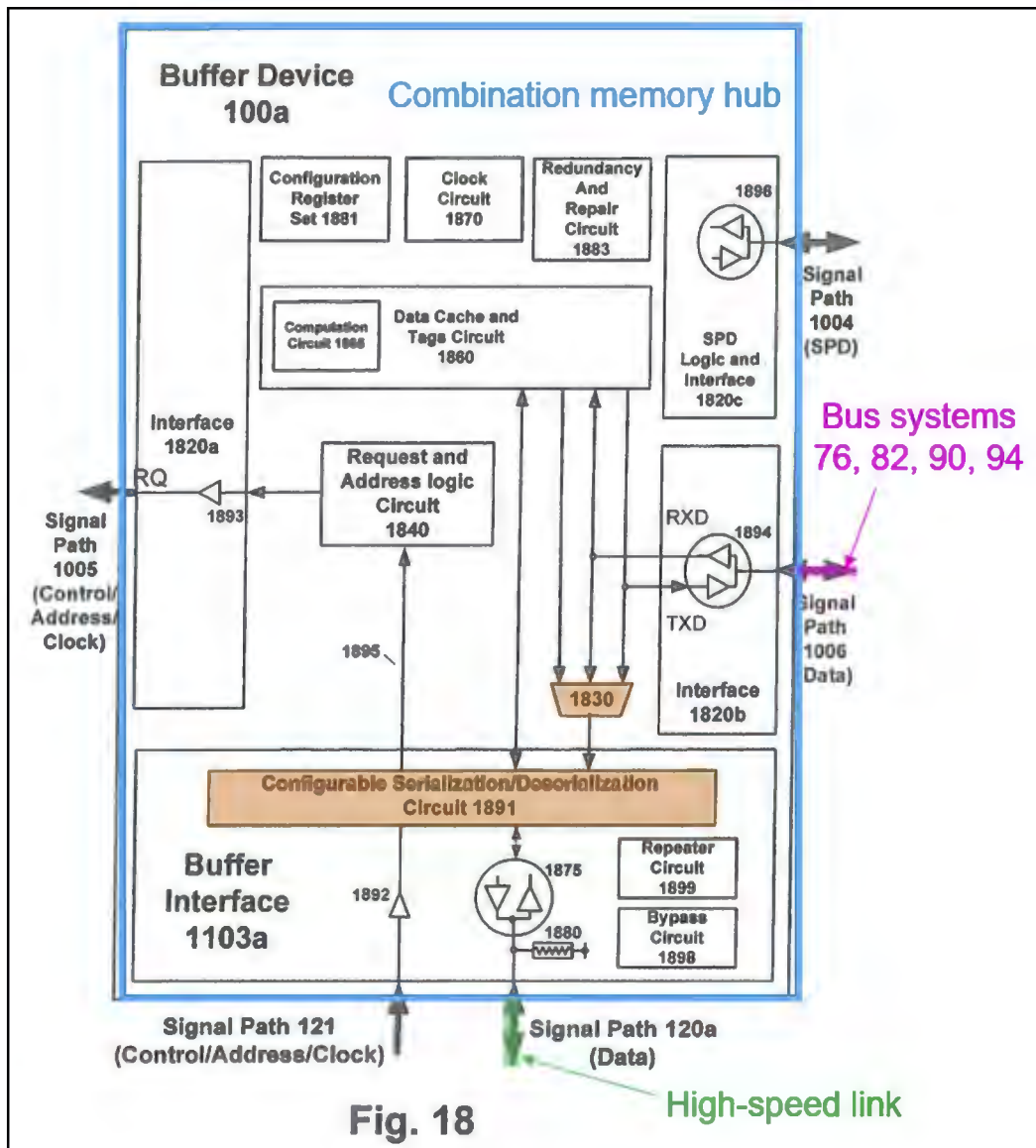
2. The Lee-Tsern Combination

88. A system based on the combination of Lee and Tsern uses the structure of Lee’s memory system 50 as a starting point. *See*, for instance, the illustrations in Lee’s FIGS. 2 and 5. Specifically, consistent with Lee’s system, “memory devices 70 are divided into four groups or ‘ranks’ coupled to the memory hub 60 [blue] through a respective bus system.” EX1004, [0016]. The memory hub is also coupled to a memory controller through a “high-speed link 58.” *Id.* The memory system is operable in “high memory bandwidth” or “high memory depth” mode, as I discussed above for Lee’s system. EX1004, [0017].

89. Tsern’s buffer device 100a is similar to Lee’s memory hub 60, in that it “provides access to a plurality of respective integrated circuit memory devices.” EX1005, 12; *see* 30 (“One or more memory devices 101a-d may respond by transmitting data to buffer 100a which receives the data via one or more signal paths 1006 and in response, transmits corresponding signals to a master”). In the Lee-Tsern combination system, based on this similarity, the memory hub is implemented based on Tsern’s buffer device. *See* EX1005, 12, 30, Fig. 18. In addition, optionally, the combination memory hub is implemented as an integrated circuit, consistent with Tsern’s teachings that its buffer device is an “integrated

circuit buffer device.” EX1005, Abstract; *see* 30 (“Fig. 18 illustrates a block diagram of a buffer device 100a (or die, such as buffer die 1100a)”); Fig. 11.

90. One example of how the Lee-Tsern combination is implemented is based on Tsern’s description of the buffer device 100a of Fig. 18. I have illustrated this example in the composite figure below. Specifically, the memory hub of the combination is an integrated circuit that has structure and function based on Tsern’s buffer device 100a. Generally, Tsern’s buffer device 100a and Lee’s memory hub 60 have similar functions: they both handle communications between a memory controller and “a plurality of respective integrated circuit memory devices,” and they do so via (1) a single signal path between the memory hub/buffer device and the controller and (2) multiple signal paths between the memory hub and the memory devices. EX1005, 12; *see* 30 (“One or more memory devices 101a-d may respond by transmitting data to buffer 100a which receives the data via one or more signal paths 1006 and in response, transmits corresponding signals to a master”), Abstract (“topologies (data and/or control/address information) between an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices”).



Lee-Tsern composite figure based on Tsern, Fig. 18

91. As I discussed earlier, Tsern’s buffer device 100a includes a “buffer interface 1103a [that] couples signal path[] 120a to buffer 100a.” EX1005, 31. The signal path 120a couples the buffer device 100a to a master, such as a memory controller. See EX1005, 22, 30, Fig. 18. This structure is generally similar to Lee’s high-speed link 58 coupling the memory hub 60 to the controller 52. See

EX1004, [0015]-[0016], FIG. 2. Based on this teaching of Tsern and its similarity to the structure of Lee's system, the combination memory hub (outlined in blue in the composite figure above) is implemented with a buffer interface (based on the buffer interface 1103a of Tsern's buffer device 100a) that couples the high-speed link 58 of the combination (green in the composite figure above; based on the signal path 120a of Tsern's buffer device 100a) to the controller (*e.g.*, corresponding to Tsern's master). *See* EX1004, [0015]-[0016], FIG. 2.

92. Tsern's buffer device 100a also includes an "[i]nterface 1820b" that is "coupled to signal path 1006 to transfer data between buffer 100a and one or more memory devices 101a-d." EX1005, 32-33. Importantly, Tsern describes that the "number of ... data signal lines between buffer 100a and memory devices 101a-d are programmable in order to accommodate different numbers of memory devices." *Id.*, 37. This structure is generally similar to Lee's buses 76, 82, 88, 90 that transfer data between the memory hub and multiple memory devices 70. *See* EX1004, FIG. 2. Based on this teaching of Tsern and its similarity to the structure of Lee's system, the combination memory hub is implemented with an interface (based on the interface 1820b of Tsern's buffer device 100a) that is coupled to the bus systems 76, 82, 90, 94 of the combination (*e.g.*, corresponding to Tsern's signal paths 1006) to enable data transfer between the memory hub and the ranks of memory devices. *See* EX1004, [0016], FIG. 2.

93. Other aspects of the combination memory hub are implemented as taught by Tsern for its buffer device 100a. For instance, among other aspects, a “multiplexer 1830 [orange] may perform bandwidth-concentrating operations between buffer interface 100a and interface 1820b,” *e.g.*, allowing the buffer to “utilize[] the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” EX1005, 33. Providing a mechanism to combine multiple data paths of simultaneously received data into a single data path for connection to a memory controller enables implementation of the high memory bandwidth mode of operation described by Lee, in which data received at the memory hub simultaneously from multiple bus systems is combined onto the single high-speed link 58. ; *see* EX1004, [0017]. The memory hub of the combination can also implement a “[c]onfigurable serialization/deserialization circuit 1891” (orange) that enables employment of “an access interleaving or multiplexing scheme ... to ensure that all storage locations within memory devices 101a-d can be accessed.” EX1005, 38.

94. A second example of how the Lee-Tsern combination is implemented is based on Tsern’s teachings of the “integrated circuit buffer device 3600” of Fig. 36. I have illustrated this example in the composite figure below. Specifically, the memory hub of the combination is an integrated circuit that has structure and function based on Tsern’s buffer device 3600. Like Tsern’s buffer device 100a,

the buffer device 3600 also has functions and structure that are similar to Lee's memory hub. Specifically, Tsern's buffer device 3600 manages communication of data and control signals between a memory controller and memory devices, as does Lee's memory hub. See EX1005, 68.

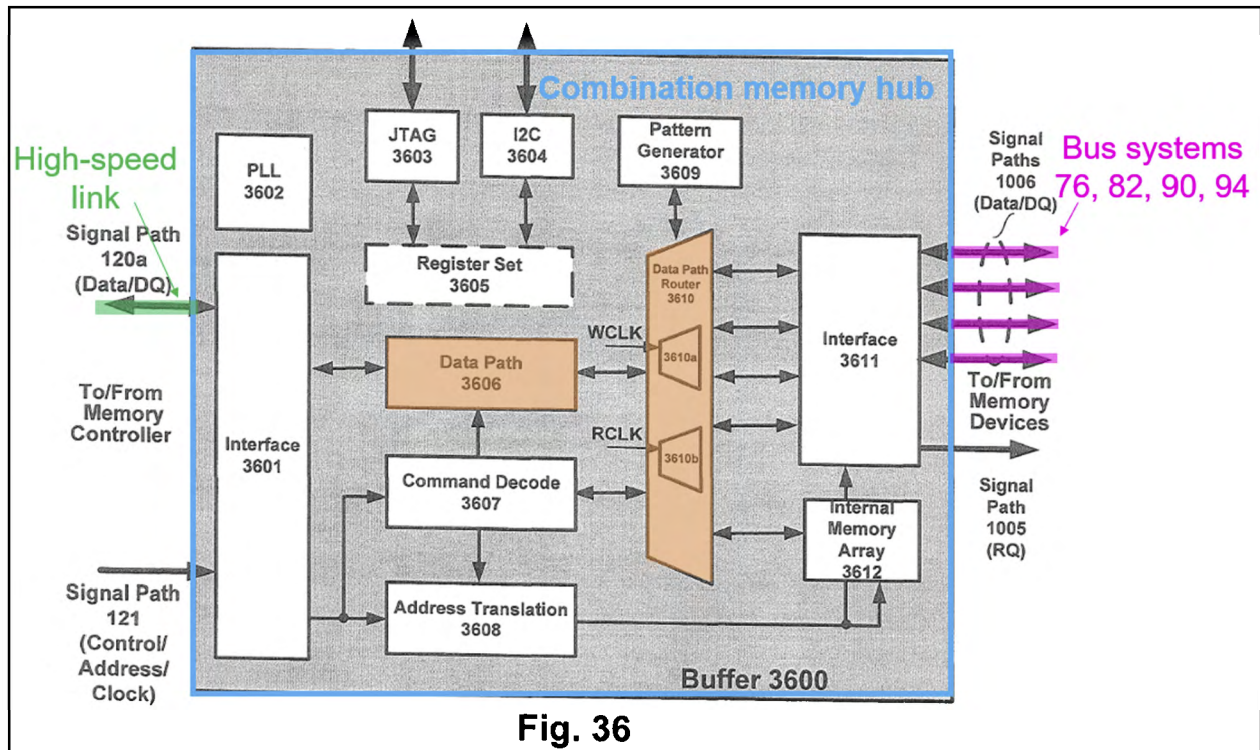


Fig. 36

Excerpt from Tsern, Fig. 36 (annotated)

95. Tsern's buffer device 3600 includes an interface 3601 that couples signal path 120a to the buffer device 3600. See EX1005, 67-68. The signal path 120a couples the buffer device 3600 to a master, such as a memory controller. See *id.*, 68. This structure is generally similar to Lee's high-speed link 58 coupling the memory hub 60 to the controller 52. See EX1004, [0015]-[0016], FIG. 2. Based on this teaching of Tsern and its similarity to the structure of Lee's system, the

combination memory hub (outlined in blue in the composite figure above) is implemented with an interface (based on the interface 3601 of Tsern's buffer device 3600) that couples the high-speed link of the combination (green in the composite figure above; based on the signal path 120a of Tsern's buffer device 3600) to the controller. *See* EX1004, [0015]-[0016], FIG. 2.

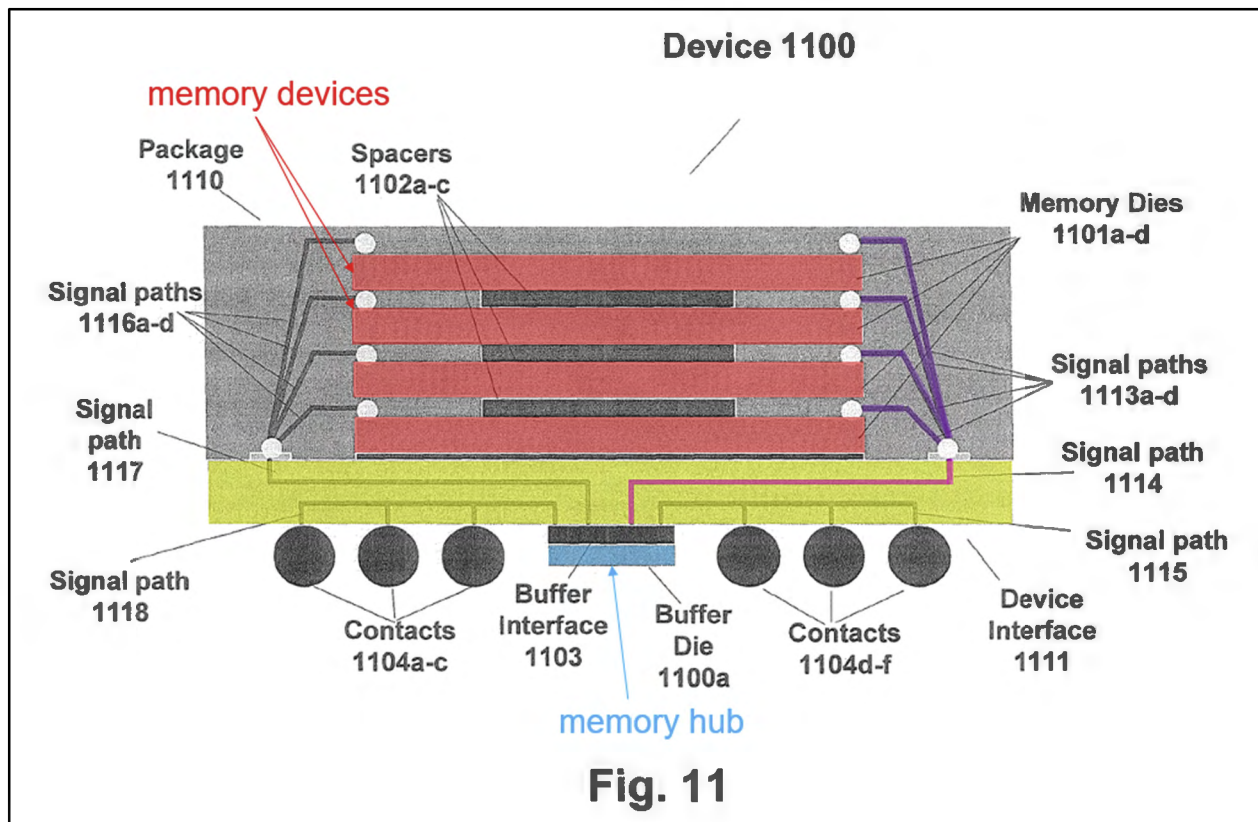
96. Tsern's buffer device 3600 also includes an interface 3611 to communicate data between the buffer device and one or more memory devices via multiple signal paths 1006. *See* EX1005, 67. This structure is generally similar to Lee's buses 76, 82, 88, 90 that transfer data between the memory hub and multiple memory devices 70. *See* EX1004, FIG. 2. Based on this teaching of Tsern and its similarity to the structure of Lee's system, the combination memory hub is implemented with an interface (based on the interface 3611 of Tsern's buffer device 3600) that is coupled to the bus systems 76, 82, 90, 94 of the combination (*e.g.*, corresponding to Tsern's signal paths 1006) to enable data transfer between the memory hub and the ranks of memory devices. *See* EX1004, [0016], FIG. 2.

97. Other aspects of the combination memory hub are implemented as taught by Tsern for its buffer device 3600. For instance, the combination memory hub includes "data path 3606 and data path router 3610," orange in the composite figure above, that "merge separate read data from more than one memory device" into a single merged read data or read stream." EX1005, 68; *see* 71 (describing

that the data path router “includes a plurality of signal paths used to merge read data from different memory devices as well as parse write data into write data portions to be stored in multiple memory devices”). The “separate read data” are from the multiple memory devices (*e.g.*, DRAM) of the combination system, and they are merged into a single data stream that is output onto the high-speed link of the combination. *See* EX1004, [0016]-[0020], FIG. 2.

98. In the combination system, the memory hub IC and memory devices of at least one of the ranks can be arranged based on the stacked configuration illustrated in Tsern’s Fig. 11. Specifically, and as shown in the composite figure below, the memory device ICs (highlighted in red) are “stacked” on a top surface of a “device interface 1111” (highlighted in yellow), and the combination memory hub IC (highlighted in blue) is on the opposite surface of the device interface.

EX1005, 26. “[S]ignal paths 1114,” *e.g.*, one or more of the bus systems 76, 82, 90, 94 (pink) of the combination memory system (*see* EX1004, [0016]) are “disposed in device interface 1111” to allow signals (*e.g.*, data) to be communicated between the memory hub and the memory devices. EX1005, 26.



Lee-Tsern composite figure based on Tsern, Fig. 11

3. Motivation for the Combination and Expectation of Success

Motivation for implementing functionality of Tsern's buffer device in the combination memory hub

99. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement the combination memory hub to have functionality based on Tsern's buffer devices (e.g., based on the Fig. 18 or Fig. 36 embodiment of Tsern's buffer device).

100. First, a POSITA would have been motivated to implement Lee's memory hub based on Tsern's teachings of similarly situated buffer devices because of this very similarity, and because the specifics provided by Tsern are just

details simply not specified by Lee regarding how to implement a memory hub. Specifically, Lee's memory hub receives a first set of parallel data from multiple memory devices along multiple bus systems, and transmits that received data as a second set of parallel data along a single bus system to a memory controller. *See* [19c]-[19d] of Ground 1A, *supra*. Tsern discloses buffer devices with similar functionality: they receive parallel data from multiple memory devices along multiple buses, and transmit data to a memory controller along a single bus system. A POSITA would have motivated to look to Tsern for teachings of how to implement the details of the buffer architecture.

101. Second, implementing the memory hub of the combination based on Tsern's buffer devices is merely the application of known techniques (that is, a specific implementation of a memory hub that converts a received set of parallel data to a transmitted set of parallel data) to a known structure (the memory hub in Lee's memory system), and it yields predictable results (specifically, a memory hub implementing elements enabling conversion of a received set of parallel data to a transmitted set of parallel data).

102. A POSITA would have had a reasonable expectation of success in implementing the memory hub of the combination based on Tsern's buffer devices because memory system technology is predictable. Also, a POSITA would have had a reasonable expectation of success because the location and functionality of

Tsern's buffer devices in Tsern's memory system is generally consistent with that of Lee's memory hub in Lee's memory system. Specifically, both Tsern's buffer devices and Lee's memory hub manage communication of data to/from ranks of integrated circuit memory devices along multiple transmission buses, and communication of data to/from a memory controller along a single transmission bus. *See* EX1004, [0009], [0015]-[0020], FIG. 2; EX1005, Figs. 11, 18, 36.

Motivation for implementation of the memory hub as an integrated circuit

103. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement the memory hub in the combination as an integrated circuit.

104. First, it was conventional to implement the memory hub of a memory cell array system as an integrated circuit, and a POSITA would have been motivated to pursue this standard implementation for compatibility with conventional processes and structures. For instance, Khan describes an ASIC (a type of integrated circuit) in a memory system. *See* EX1009, 1. Liao also describes integrated circuit controller die in the context of a memory system. *See* EX1016, 6:53-54, Fig. 18.

105. Second, a POSITA would have recognized that implementation of a memory hub as an integrated circuit is smaller, more efficient, and less expensive than implementation of the memory hub functionality through a circuit composed

of discrete components, given that these are standard and well-known advantages of integrated circuits. *See* EX1024, 1:15-18 (“Due to many technological advances, integrated circuits, or “chips,” incorporate many millions of transistors on a single monolithic device. This provides many advantages, including improved speed and reduced size”).

106. Third, Lee does not specify particularly the nature of the memory hub. A POSITA would have been motivated to implement the combination memory hub as an integrated circuit, especially given the advantages of integrated circuits, because implementing the memory hub as an IC is just an implementation detail.

107. Fourth, implementing the memory hub as an integrated circuit is merely the application of known techniques (a memory hub as an integrated circuit) to a known structure (*e.g.*, the combination memory hub) to yield predictable results (an integrated circuit memory hub).

108. A POSITA would have had a reasonable expectation of success in implementing the memory hub as an integrated circuit because this was a conventional approach to implementation of memory hubs. *See* EX1009, 1; EX1016, 6:53-54.

Motivation for a stacked arrangement of memory device ICs and memory hub

109. It is my opinion that there are a number of reasons that would have motivated a POSITA to arrange the memory devices and memory hub in a stack in the Lee-Tsern combination.

110. First, a POSITA would have been motivated to pursue the combination arrangement because the stacked arrangement, with the device interface 1111 between the memory devices and the memory hub, positions the memory hub “away from” the memory devices “to alleviate heat dissipation near the memory devices,” helping to avoid an overheating situation. EX1005, 26.

111. Second, a POSITA would have been motivated to pursue this implementation because stacking of chips allows for “integrating more devices into a smaller volume,” which in turn enables performance advantages, including “smaller footprint, shorter signal routing, reduced wiring density.” EX1009, 1.

112. Third, arranging the memory devices and memory hub chips in a stacked arrangement is merely the application of known techniques (*e.g.*, a stacked arrangement of chips in a memory module) to a known system (Lee’s DRAM memory chips and memory hub), and it yields predictable results (specifically, a memory module in which memory chips are stacked above the memory hub, and separated from the memory hub by a device interface).

113. A POSITA would have had a reasonable expectation of success in implementing a stacked chip arrangement because semiconductor packaging technology is predictable. Moreover, a POSITA would have had a reasonable expectation of success because a stacked package of memory chips and logic chips was conventional and well-understood, *e.g.*, as evidenced by Khan and Liao, both of which I discussed above. *See* EX1009, 1; EX1016, Fig. 18.

4. Analysis of claims

114. For the reasons below, claims 19, 22, and 25-26 are obvious over the combination of Lee and Tsern.

(a) Claim 19

[19pre] A electronics system device with a high speed memory chip module, the device comprising:

[19a] an ASIC processor;

[19b] a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs, each of the memory cell array ICs has an (I/O) data bus; and

[19c] a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an (I/O) data bus of each of the memory cell array ICs,

115. These limitations are rendered obvious by the Lee-Tsern combination for reasons similar to those I discussed above for elements [19pre]-[19c] of Ground 1A.

[19d] wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus, and transmits the second set of parallel data to the ASIC processor;

116. In the Lee-Tsern combination system, the high-speed link 58 corresponds to the claimed ***second transmission bus***, and the data carried on the high-speed link 58 corresponds to the claimed ***second set of parallel data***, for reasons similar to those I discussed above for element [19d] of Ground 1A. Also, the memory hub 60 of the combination (which corresponds to the claimed ***logic unit***) ***transmits the second set of parallel data to the ASIC processor***, for reasons similar to those I discussed above for element [19d] of Ground 1A.

Tsern's buffer device 100a renders obvious parallel-to-parallel conversion

117. In one example of the Lee-Tsern combination system, the memory hub (corresponding to the claimed ***logic unit***) is implemented based on Tsern's description of its buffer device 100a, e.g., the buffer device illustrated in Fig. 18. In this example, based on the teachings of Tsern about the buffer device 100a, and as I discuss in more detail in the following paragraphs, the memory hub (***logic***

unit) is used for converting the first set of parallel data into the second set of parallel data.

118. As I discussed previously, in Tsern's system, data is communicated between the buffer device 100a and a memory controller via a signal path 120a. *See* EX1005, 12, 14-15. Tsern describes that the "buffer interface 1103a has a programmable width for signal path 120a," indicating that the signal path 120a can carry data of various widths, and specifically data of greater than one bit in width. *Id.*, 38. Data of greater than one bit in width are parallel data. That is, based on Tsern's disclosure that the signal path 120a has a programmable width, a POSITA would have understood that the signal path 120a can carry *parallel data*, *i.e.*, data of width greater than one bit. This is consistent with Lee's high-speed link 58, which also carries parallel data, as I discussed above for Ground 1A.

119. Also in Tsern's system, data is communicated between the buffer device 100a and multiple memory devices via multiple "signal paths 1006." EX1005, 38; *see id.* ("The number of signal paths 1006 may be increased or decreased as the memory device access width changes"). Each signal path communicates with a corresponding memory device. Tsern describes that the buffer device interface 1820b, which connects to the signal paths 1006 (*see* Fig. 18), "may be programmed to connect to 16 'x4' width memory devices, 8 'x8' width memory devices or 4 'x16' width memory devices." *Id.*, 37. That is, Tsern

describes that the memory devices (which are connected to the respective signal paths) provide data of 4-bit, 8-bit, or 16-bit widths. These data (which are *parallel data*) are carried by the signal paths 1006. That is, based on this disclosure, a POSITA would have understood that each signal path 1006 carries *parallel data*, e.g., in order to interface with 4-, 8-, or 16-bit width memory devices. This is consistent with Lee's bus systems 76, 82, 90, 94, which also carry parallel data from the respective ranks memory devices, as I discussed above for Ground 1A.

120. Thus, when reading from the memory devices, Tsern's buffer device 100a receives parallel data from the memory devices along multiple signal paths, and then transmits parallel data to the memory controller along a single signal path. This involves *converting* the parallel data carried along the multiple signal paths 1006 to parallel data carried along the signal path 120a. For instance, the conversion of the parallel data on signal paths 1006 to the parallel data on the signal path 120a is accomplished through components including a "configurable serialization/deserialization circuit 1891," which "performs serialization and deserialization functions depending upon a stored serialization ratio." EX1005, 38. That is, the circuit 1891 converts the multiple sets of parallel data received along the signal paths 1006 to a single set of parallel data for transmission along the signal path 120a. A "multiplexer 1830" also participates in converting the parallel data on signal paths 1006 to the parallel data on the signal path 120a through its

“bandwidth-concentrating operations” to “utilize[] the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” EX1005, 33; *see* EX1019, Abstract (showing conversion of parallel data from one bit width to parallel data of another bit width).

121. This parallel-to-parallel conversion functionality is implemented in the memory hub of the combination as shown in the composite figure below. The memory hub (corresponding to the claimed *logic unit*) is implemented based on Tsern’s buffer device 100a, *e.g.*, based on Tsern’s teachings that buffer device 100a components are *used for converting the first set of parallel data into a second set of parallel data*, as I discussed in the previous paragraph. Specifically, as taught by Lee (and consistent with operation of Tsern’s buffer device 100a) the combination memory hub communicates a *first set of parallel data* to/from memory devices (*e.g.*, ranks of DRAM devices) via bus systems 76, 82, 90, 94 (which correspond individually or collectively to the claimed *first transmission bus*, as I discussed for Ground 1A) (pink), as taught by Lee. *See* [19c], *supra*. The combination memory hub also communicates a *second set of parallel data* to/from a memory controller via high-speed bus 58 (which corresponds to the claimed *second transmission bus*, as I also discussed above for Ground 1A) (green), as also taught by Lee and consistent with operation of Tsern’s buffer device 100a.

122. Elements of the combination memory hub, including a configurable serialization/deserialization circuit 1891 and a multiplexer 1830 (orange *infra*) based on Tsern, ***convert the first set of parallel data into a second set of parallel data, i.e.,*** convert the parallel data received on one or all of the bus systems 76, 82, 90, 94 into parallel data for transmission on the high-speed bus 58. This is consistent with the operation of these components as disclosed by Tsern, which I explained earlier in this section.

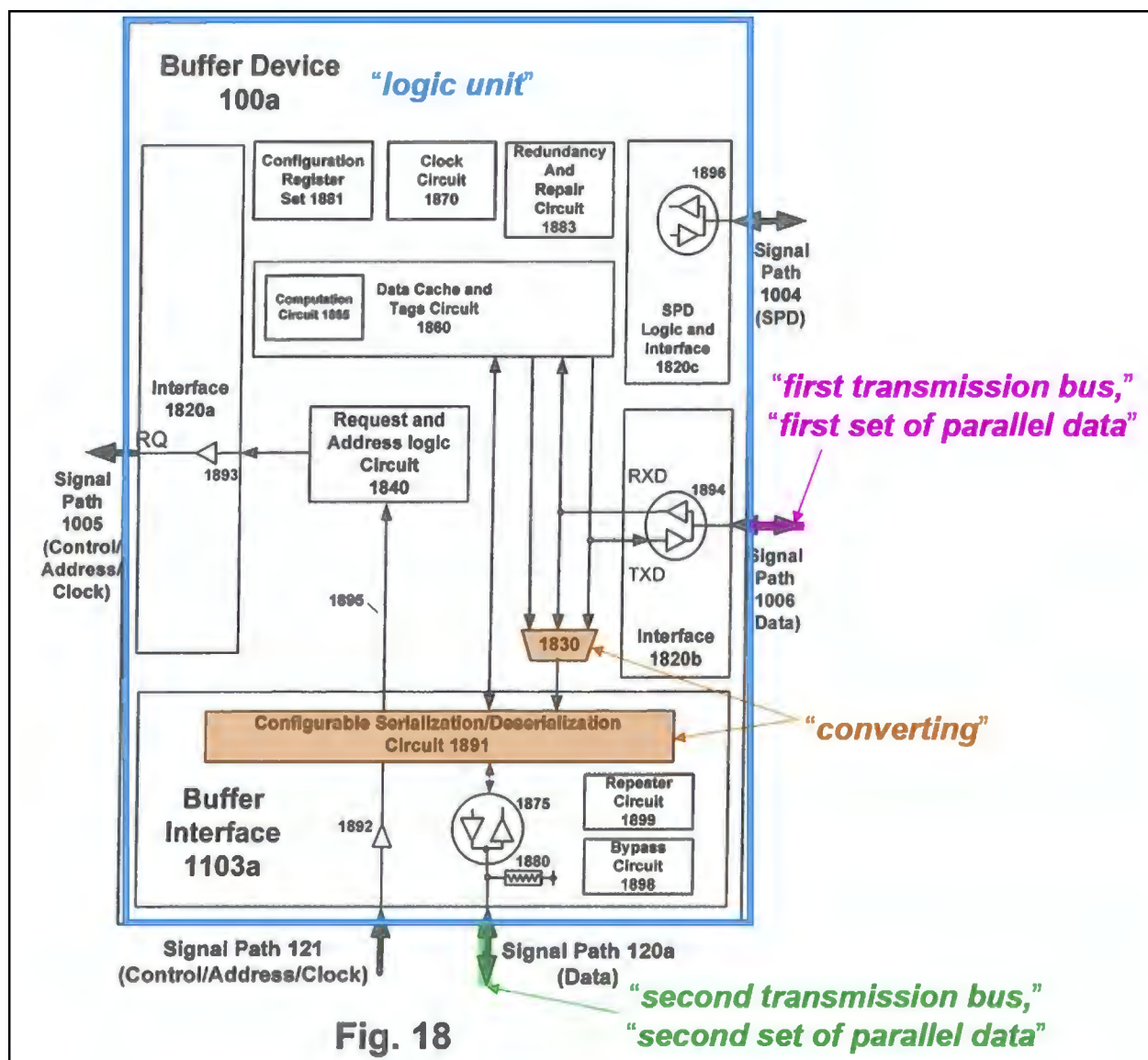


Fig. 18

Lee-Tsern composite figure based on Tsern, Fig. 18

Tsern's buffer device 3600 renders obvious parallel-to-parallel conversion

123. In another example of the Lee-Tsern combination system, the memory hub (corresponding to the claimed **logic unit**) is implemented based on Tsern's description of its buffer device 3600, e.g., the buffer device illustrated in Fig. 36. In this example, based on the teachings of Tsern about the buffer device 3600, and

as I discuss in more detail in the following paragraphs, the memory hub (*logic unit*) is *used for converting the first set of parallel data into the second set of parallel data*.

124. As I discussed previously, in Tsern's system, data is communicated between the buffer device 3600 and multiple memory devices via the multiple "signal paths 1006." EX1005, 68. Each of these signal paths 1006 carries *parallel data*, as I discussed above in the context of the first example of the Lee-Tsern combination. EX1005, 37-38. In addition, data is communicated between the buffer device 3600 and a memory controller via a signal path 120a, which also carries *parallel data*, as I also discussed above for the first example of the combination. *See* EX1005, 12, 14-15, 38.

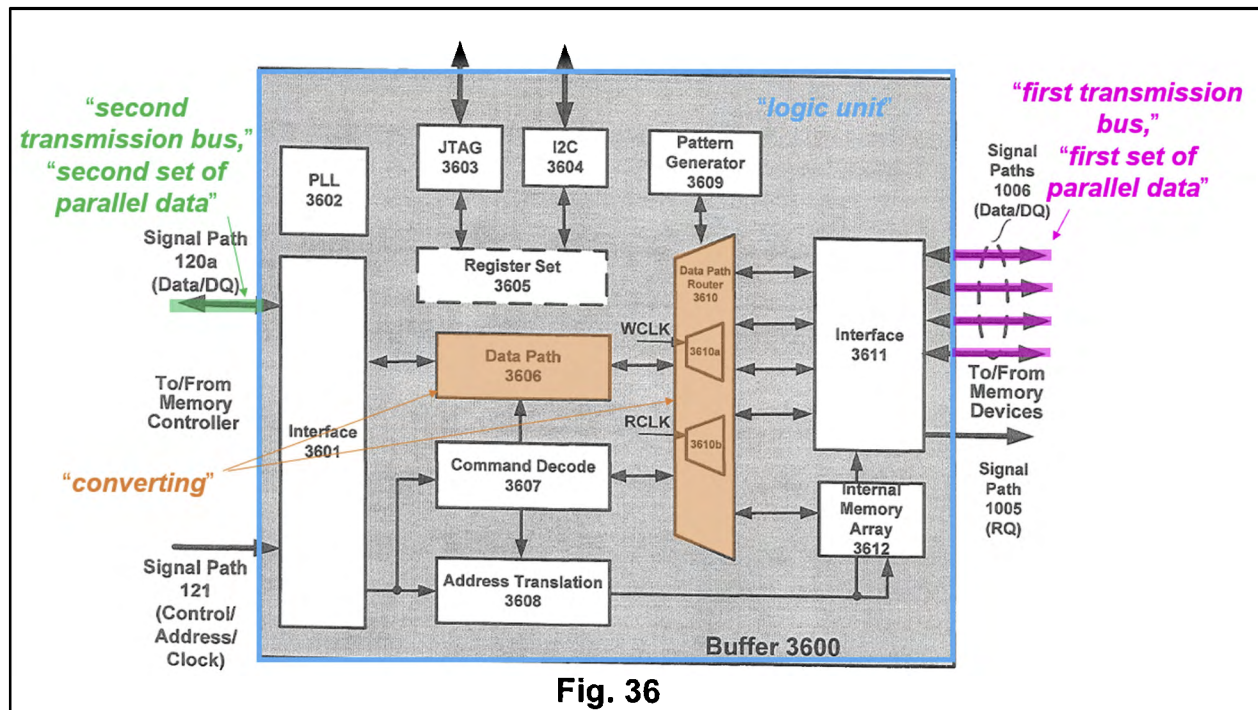
125. Thus, when reading from the memory devices, Tsern's buffer device 3600 receives parallel data from the memory devices along multiple signal paths, and then transmits parallel data to the memory controller along a single signal path. This involves *converting* the parallel data carried along the multiple signal paths 1006 to parallel data output through interface 3601 onto the signal path 120a. For instance, the conversion of the parallel data on signal paths 1006 to the parallel data on the signal path 120a is accomplished through components including "data path 3606 and data path router 3610," which "merge separate read data from more than one memory device into a single merged read data or read stream output at

interface 3601.” EX1005, 36. That is, these components convert the multiple sets of parallel data received along the signal paths 1006 to a single set of parallel data for transmission along the signal path 120a.

126. This parallel-to-parallel conversion functionality is implemented in the memory hub of the combination as shown in the composite figure below. The memory hub (corresponding to the claimed *logic unit*) is implemented based on Tsern’s buffer device 3600, *e.g.*, based on Tsern’s teachings that buffer device 3600 components are *used for converting the first set of parallel data into a second set of parallel data*, as I discussed in the previous paragraph. Specifically, as taught by Lee (consistent with operation of Tsern’s buffer device 3600), the combination memory hub communicates a *first set of parallel data* to/from memory devices (*e.g.*, ranks of DRAM devices) via bus systems 76, 82, 90, 94 (which correspond individually or collectively to the claimed *first transmission bus*, as I discussed for Ground 1A) (pink), as taught by Lee. *See* [19c], *supra*. The combination memory hub also communicates a *second set of parallel data* to/from a memory controller via high-speed bus 58 (which corresponds to the claimed *second transmission bus*, as I also discussed above for Ground 1A) (green), as also taught by Lee and consistent with operation of Tsern’s buffer device 3600.

127. Elements of the combination memory hub based on Tsern, including “data path 3606 and data path router 3610” (orange *infra*), *convert* (“merge”) *the*

first set of parallel data into a second set of parallel data, i.e., convert the parallel data received on one or all of the bus systems 76, 82, 90, 94 into parallel data for transmission on the high-speed bus 58. This is consistent with the operation of these components as disclosed by Tsern, which I explained earlier in this section. See EX1005, 68.



Lee-Tsern composite figure based on Tsern, Fig. 36

[19e] wherein the ASIC processor executes a predetermined function corresponding to the second set of parallel data while the ASIC processor is under operating condition,

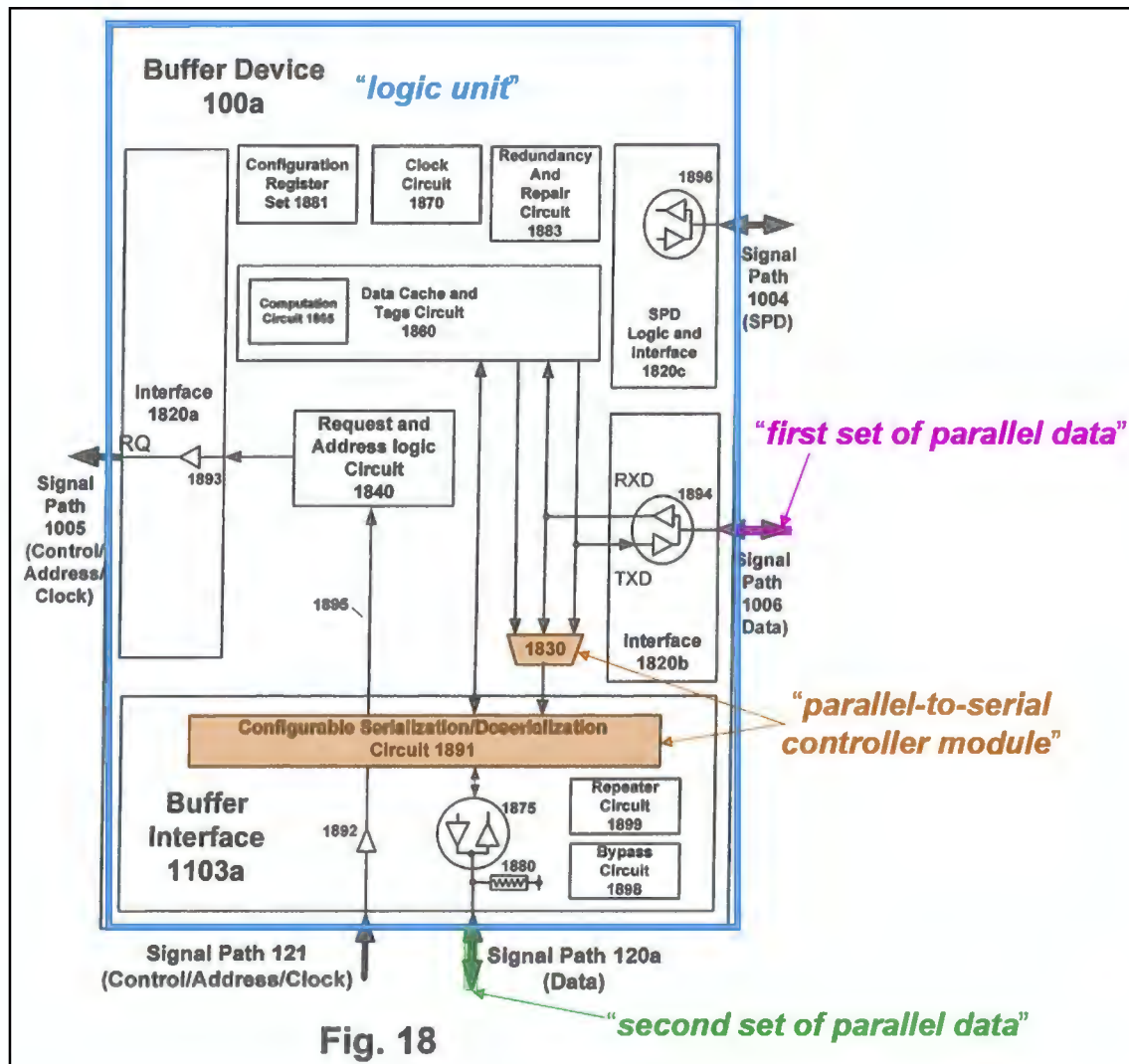
[19f] wherein bit width of the first set and the second set of parallel data are different.

128. These limitations are rendered obvious by the Lee-Tsern combination for reasons similar to those I discussed above for elements [19e]-[19f] of Ground 1A.

(b) ***Claim 22***

[22] The electronics system device of claim 19, wherein the logic unit comprises: a parallel-to-serial controller module for converting the first set of parallel data into the second set of parallel data.

129. In the Lee-Tsern combination in which the memory hub is implemented based on Tsern's buffer device 100a of Fig. 18, Tsern's configurable serialization/deserialization circuit 1891 and a multiplexer 1830 (highlighted in orange in the composite figure below) correspond to ***a parallel-to-serial controller module***, because their functionality causes the first set of parallel data to be converted into the second set of parallel data, as I discussed above for claim 19 of the Lee-Tsern ground. *See* EX1005, 33, 38.



Lee-Tsern composite figure based on Tsern, Fig. 18

130. Alternatively/additionally, in the Lee-Tsern combination in which the memory hub is implemented based on Tsern's buffer device 3600 of Fig. 36, Tsern's data path 3606 and data path router 3610 (highlighted in orange in the composite figure below) correspond to *a parallel-to-serial controller module*, e.g., because their functionality causes the first set of parallel data to be converted into

the second set of parallel data, as I discussed above for claim 19 of the Lee-Tsern ground. See EX1005, 68.

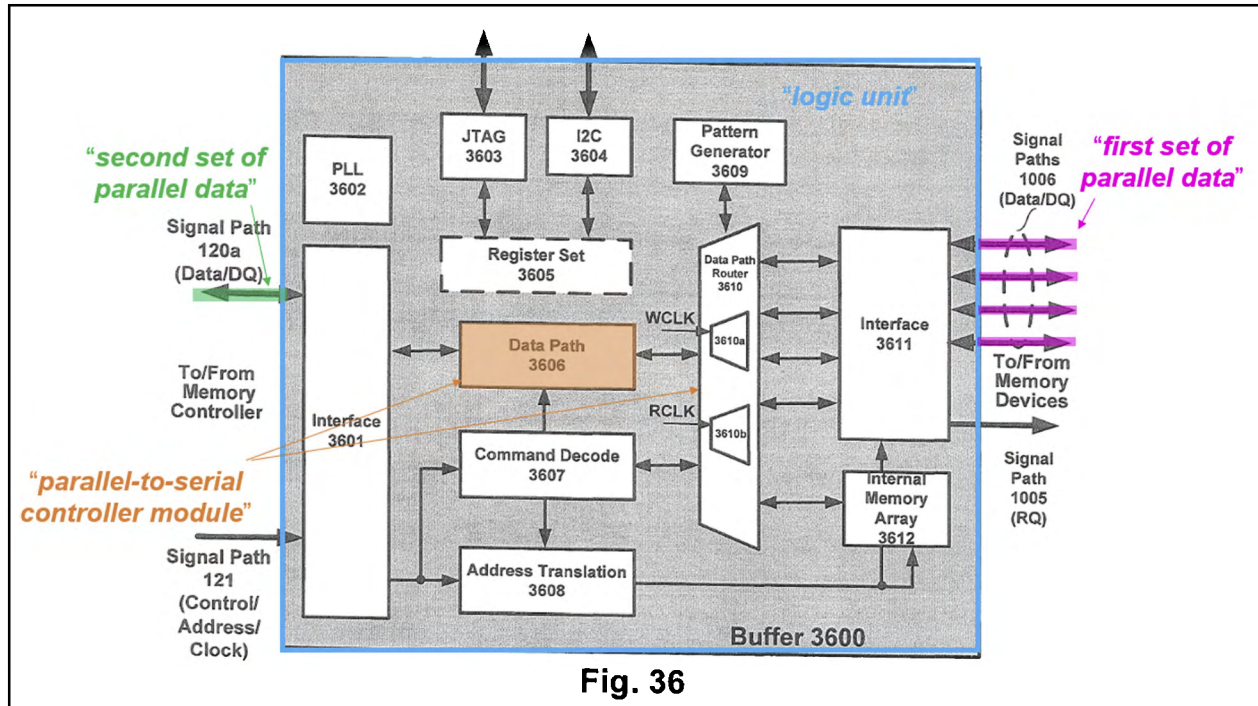


Fig. 36

Lee-Tsern composite figure based on Tsern, Fig. 36

(c) **Claim 25**

[25] The electronics system device of claim 22, wherein a transmitting data rate of the first transmission bus and a receiving data rate of the first transmission bus are different.

131. In the Lee-Tsern combination, based on Lee, in the "high memory bandwidth" mode, "the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access." EX1004, [0017]. That is, 32 bits of data are transmitted simultaneously on each of the four individual bus systems 76, 82, 90,

94. The data rate of the bus system 68 including the four individual bus systems 76, 82, 90, 94 (which corresponds to the claimed *first transmission bus*) in high memory bandwidth mode is 128 bits per memory access.

132. Lee also describes that when operated in “high memory depth mode, only one rank 74, 80, 86, 88 may be addressed at a time,” in which case “only 32 bits of data will be coupled to or from the memory module 54 with each memory access.” *Id.* That is, data is transmitted on only one of the individual bus systems 76, 82, 90, 94 at a time. The data rate of the bus system 68 including the four individual bus systems 76, 82, 90, 94 (which corresponds to the claimed *first transmission bus*) in high memory depth mode is only 32 bits per memory access.

133. Based on Lee, the combination system can operate in either high memory bandwidth or high memory depth mode. EX1004, [0017]. This allows for flexibility and optimization of the system’s functionality: “By allowing the memory hub 60 to configure the data format of the memory module 54, the data format can be optimized for a particular application being executed ... The data format is therefore not fixed as in conventional memory systems.” *Id.*, [0019]. This means that the system can sometimes operate in high memory bandwidth mode (in which case the data rate is 128 bits per memory access) and at other times can operate in high memory depth mode (in which case the data rate is 32 bits per memory access), *i.e.*, the system can operate at different data rates.

134. This operation can be either for writing data to the memory devices or for reading data from the memory devices, *e.g.*, for when the first transmission bus is used for either transmitting data or for receiving data. When the system operates, *e.g.*, in high memory bandwidth mode for a given instance of transmitting data (128 bits per memory access) (*transmitting data rate of the first transmission bus*), and in high memory depth mode for a different instance of receiving data (32 bits per memory access) (*receiving data rate of the first transmission bus*), the *transmitting data rate and receiving data rate of the first transmission bus are different*.

(d) **Claim 26**

[26] *The electronics system device of claim 22, wherein a transmitting data rate of the second transmission bus and a receiving data rate of the second transmission bus are different.*

135. As I discussed above, Lee's system can be "configure[d]" to operate in high memory bandwidth or high memory depth mode. EX1004, [0017]; *see* [0019]. In the combination, the system is configurable to operate in these two modes, based on Lee. As a result, in the combination, "[i]n the high memory depth mode, the high-speed link 58 can operate at a slower data rate than in the high bandwidth mode." EX1004, [0018]. This means that the data rate of the high-speed link (corresponding to the claimed *second transmission bus*) differs based on the mode of operation. When, for instance, the system is configured for high

memory bandwidth mode for a given instance of writing data, and is configured in high memory depth mode for a different instance of reading data, the reading is performed at “slower data rate” than the writing, *i.e.*, the ***transmitting data rate and receiving data rate of the second transmission bus are different***.

136. An adjustable data rate on the high-speed link has advantages: “By allowing the memory hub 60 to configure the data format of the memory module 54, the data format can be optimized for a particular application being executed ... The data format is therefore not fixed as in conventional memory systems.” EX1004, [0019].

137. Alternatively or additionally, in the combination, Lee describes that in the “high memory bandwidth” mode, “the high-speed link 58 may couple data at a rate of 2 GB/sec,” or “may couple 64-bit data words at a rate of 1 GB/sec,” *i.e.*, the high-speed link (***second transmission bus***) can be operated at different data rates. EX1004, [0017]. These data rates are applicable when data “are written to or read from” the memory devices 70, *i.e.*, they can be either transmitting data rates or receiving data rates. *Id.* Lee’s system can be “configure[d]” to operate in a certain mode. *See* EX1004, [0017], [0019]. When the system operates such that the high-speed link has one data rate (*e.g.*, “a rate of 2 GB/sec”) for a given instance of writing data (***transmitting data rate of the second transmission bus***), and a different data rate (*e.g.*, “a rate of 1 GB/sec”) for a different instance of reading

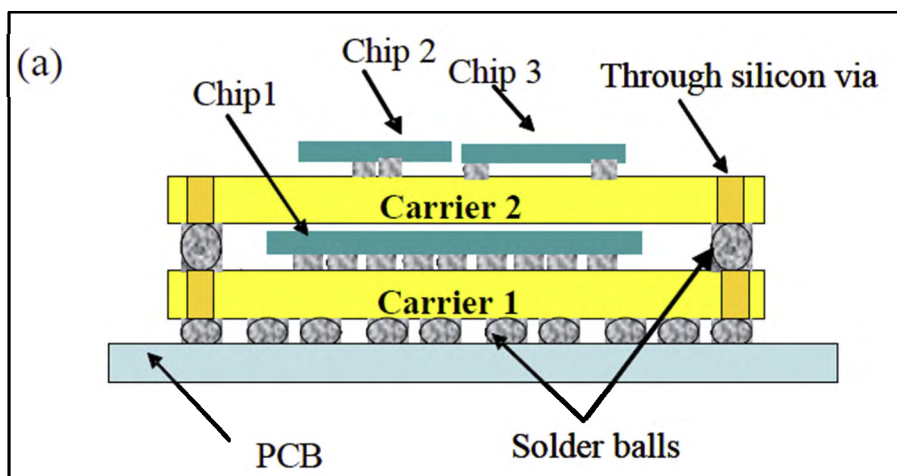
data (*receiving data rate of the second transmission bus*), the *transmitting data rate and receiving data rate of the second transmission bus are different*.

C. [Ground 1C]: Lee, Tsern, and Khan Render Obvious Claim 21

1. Khan (EX1009)

138. Khan describes a “3D stacked package with silicon interposers” that “integrate[s] one ASIC and two memory chips in a package.” EX1009, 1. The vertical stacking of this configuration is advantageous in that it provides “smaller footprint, shorter signal routing, [and] reduced wiring density.” *Id.*

139. In Khan’s package, illustrated in Fig. 1(a), *infra*, Carrier 1 “house[s] a Flip-chip (Chip 1) representing an ASIC device,” and “Carrier 2 is designed [to] house two memory chips,” Chips 2 and 3. EX1009, 1. The carriers are silicon interposers. *Id.* The use of silicon for the interposers is advantageous, *e.g.*, because silicon offers “low thermo-mechanical stresses, finer line width and spacing, wafer level batch fabrication, [and] high thermal conductivity,” *e.g.*, as compared to interposers of other materials. *Id.*



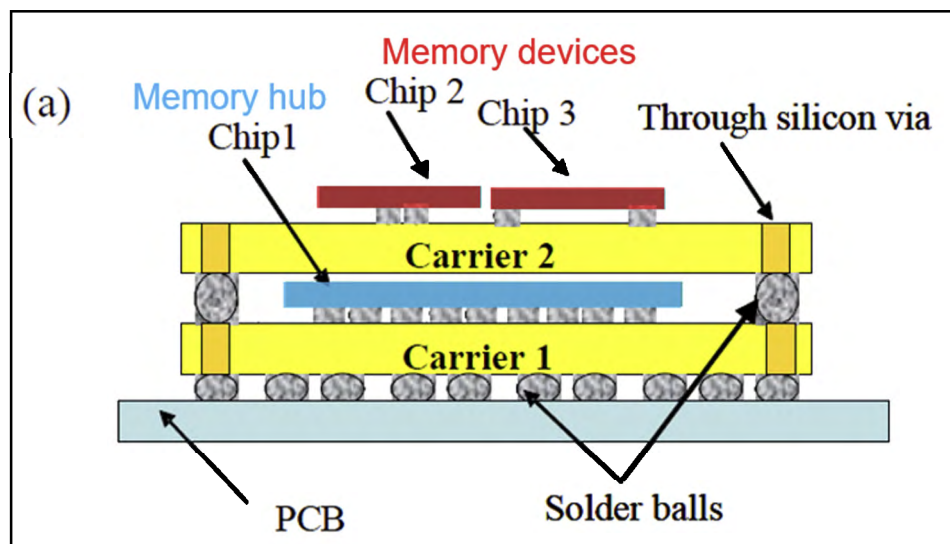
Excerpt from Khan, Fig. 1(a)

140. Khan is from the same field of endeavor (*e.g.*, memory systems) as the '942 Patent. *See* EX1001, 1:17-25; EX1009, Abstract.

141. Also, Khan is reasonably pertinent to the problem the '942 Patent was trying to solve in integrating discrete memories with the advanced semiconductor process generations (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25; EX1009, Abstract. For instance, Khan’s motivation stems from taking advantages of having different types and generations of devices assembled in a single package, in which a stacked arrangement helps to “remove the heat effectively,” which is relevant to development of memory systems with “better heat dissipation capability.” EX1009, Abstract; EX1001, 1:17-25.

2. The Lee-Tsern-Khan Combination

142. In a system based on the combination of Lee, Tsern, and Khan, the memory hub 60 (implemented as an integrated circuit based on Tsern, as I discussed above) and at least one rank of memory devices 70 are assembled into a 3D stack package based on Khan's teachings of a stacked assembly. I have illustrated this in the composite figure below. Specifically, the memory hub (indicated in blue below) is housed on Carrier 1, and the memory devices (indicated in red) are housed on Carrier 2.



Lee-Tsern-Khan composite figure based on Khan, Fig. 1(a)

3. Motivation to Combine and Expectation of Success

143. It is my opinion that there are a number of reasons that would have motivated a POSITA to arrange the memory devices and memory hub in the Lee-Tsern-Khan combination based on Khan's 3D stack package.

144. First, 3D stacking of chips allows for “integrating more devices into a smaller volume,” which in turn enables performance advantages, including “smaller footprint, shorter signal routing, reduced wiring density.” EX1009, 1. A POSITA would have been motivated to pursue 3D stacking of the memory hub and memory devices in the combination to achieve these advantages.

145. Second, a stacked assembly such as the one described by Khan can “remove[] the heat effectively” from the chips in the 3D stack. EX1009, 1. Thermal management is a key area of interest in the realm of semiconductor packaging technology, and a POSITA would have been motivated to pursue 3D stacking in the approach described by Khan in order to facilitate good thermal behavior in the system.

146. Third, a POSITA would have been motivated specifically to use silicon as the material for the interposer because of several performance advantages provided by silicon. For instance, “silicon has much high[er] thermal conductivity than organic interposers, which reduces drastically the package thermal resistance.” EX1009, 1. Other “advantages of using silicon for the interposer” include “low thermo-mechanical stresses, finer line width and spacing, [and] wafer level batch fabrication.” *Id.*.

147. Fourth, the arrangement of the memory hub and memory device ICs in a stacked arrangement based on Khan is merely an application of known

techniques (specifically, a particular arrangement of chips in a memory module) to a known system (*e.g.*, a memory system including memory device and memory hub ICs), and it yields predictable results (that is, a memory module in which memory chips and memory hub are stacked above and below a silicon interposer).

148. A POSITA would have had a reasonable expectation of success in arranging the chips of the combination in a stacked arrangement based on Khan because semiconductor packaging technology is predictable, and because a stacked package of memory chips and logic chips was conventional and well-understood. For instance, other examples of stacked chips in the context of memory modules are provided in Tsern (*see* EX1005, Fig. 11), Liao (*see* EX1016, Fig. 18), and Raghuram (*see* EX1023, FIG. 2).

4. Analysis of claims

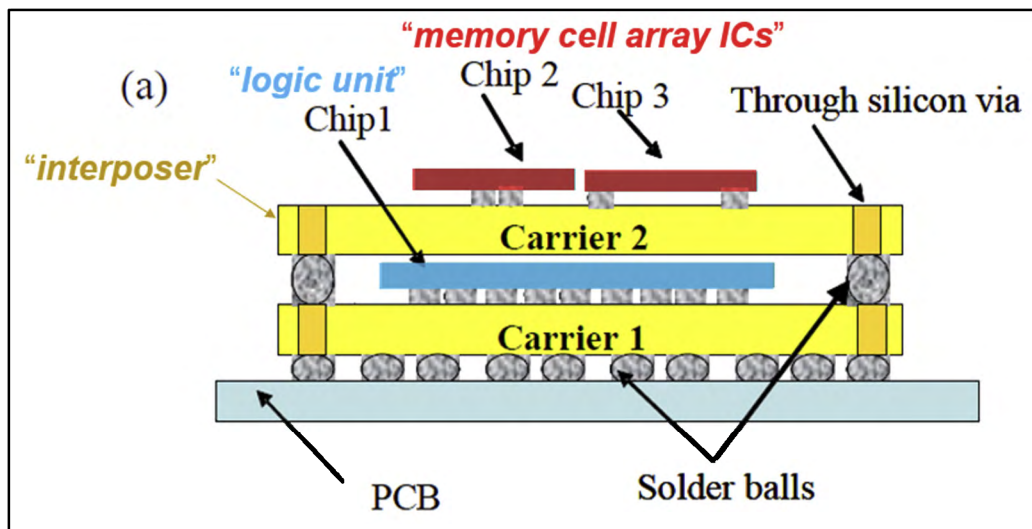
149. For the reasons below, claim 21 is obvious over the combination of Lee, Tsern, and Khan.

(a) Claim 21

[21a] The electronics system device of claim 19, further comprising: an interposer, wherein the multiple memory cell array ICs are disposed over the interposer respectively, and the interposer is disposed over the logic unit,

150. In Lee-Tsern-Khan combination, the memory devices 70 (corresponding to the claimed **memory cell array ICs**) and memory hub 60 (corresponding to the claimed **logic unit**) are arranged in a “3D stack package,”

based on Khan, and as illustrated in the composite figure below. EX1009, 1, Fig. 1(a). Specifically, the memory hub (colored blue) is housed on a first carrier, and the memory devices (red) are housed on a second carrier. See EX1009, 1, Fig. 1(a). The second carrier (marked Carrier 2 by Khan) corresponds to the claimed *interposer*, e.g., because it is a substrate disposed between ICs. In this 3D stack package, as illustrated below, the memory devices are housed on the second carrier (satisfying the claimed requirement that the *memory cell array ICs are disposed over the interposer*), and the memory hub is below the interposer (satisfying the claimed requirement that the *interposer is disposed over the logic unit*).



Lee-Tsern-Khan composite figure based on Khan, Fig. 1(a)

[21b] wherein the interposer comprises silicon or oxide glass material.

151. Carrier 2 (corresponding to the *interposer*) is a “silicon interposer,” based on Khan. EX1009, 1. Khan also describes reasons why a silicon interposer

would be used: “Some of the advantages of using silicon for the interposer are, low thermo-mechanical stresses, finer line width and spacing, wafer level batch fabrication, high thermal conductivity.” *Id.*, 1.

D. [Ground 1D]: Lee, Tsern, Khan, and Dozen Render Obvious Claim 20

1. Dozen (EX1007)

152. Dozen describes a “method for manufacturing a highly-reliable semiconductor device.” EX1007, Abstract. For instance, Dozen describes manufacturing memory devices, *e.g.*, DRAM, SRAM, or flash memory, in an “element substrate 1102.” EX1007, Abstract, 4:9-26. Among other processing steps, Dozen describes that “where a plurality of semiconductor devices are included in the element substrate 1102, the plurality of semiconductor devices may be obtained by dividing the element substrate and the sealing layers,” *e.g.*, by “dicing, scribing, using a cutting machine ..., laser cutting, or the like.” EX1007, 11:60-67.

153. Dozen is pertinent to the problem the ’942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25. For instance, Dozen’s manufacturing process produces a “highly-reliable semiconductor device ... with a high yield.” EX1007, Abstract.

A high yield process for manufacturing reliable chips used in a memory system is relevant to reducing the greenhouse gas emission rate associated with that memory system, *e.g.*, because higher yield of reliable chips reduces waste. *See* EX1001, 1:17-25.

2. The Lee-Tsern-Khan-Dozen Combination

154. In a system based on the combination of Lee, Tsern, Khan, and Dozen, the memory devices are, for instance, DRAM devices, as taught by Lee. EX1004, [0016]. Based on Dozen's teachings about fabrication of DRAM devices, the DRAM devices of the combination are "formed in [an] element substrate," such as a wafer. EX1007, 4:9-26. Among other processing steps, individual DRAM chips are obtained from that substrate "by dividing the element substrate and the sealing layers," *e.g.*, by "dicing, scribing, using a cutting machine ..., laser cutting, or the like." EX1007, 11:60-67.

3. Motivation to Combine

155. It is my opinion that there are a number of reasons that would have motivated a POSITA to employ laser dicing of the DRAM chips in the Lee-Tsern-Khan-Dozen combination based on Dozen's teachings.

156. First, laser dicing advantageously enables high degrees of precision to be achieved at high processing speeds. This is explained by Akiyama, which identifies laser dicing as achieving "high throughput, low costs, high yield, and

high-precision.” EX1020, 7:9-11. Similarly, Dahm describes laser dicing in the context of “high precision cutting.” EX1021, 1:6-8.

157. Second, laser dicing is a contactless processing method, and thus does not subject tools to wear, generates little waste, and does not run significant risks of contamination. *See* EX1021, 1:22-32.

158. Fourth, implementation of laser dicing for the memory cell array chips is one of a finite number of predictable solutions (*e.g.*, laser dicing, physical dicing, scribing), and with a reasonable expectation of success (discussed *infra*). *See* EX1020, Abstract; EX1021, 1:6-9.

159. Fifth, use of laser dicing to dice the DRAM chips in the Lee-Tsern-Khan combination is merely the application of known techniques (specifically, laser dicing of integrated circuits) to a known system (*e.g.*, Lee’s memory (*e.g.*, DRAM) chips), and it yields predictable results (that is, DRAM memory chips separated by a laser dicing process).

160. A POSITA would have had a reasonable expectation of success in using laser dicing for the DRAM chips of the combination because memory system technology and integrated circuit dicing technology are predictable, and because laser dicing of integrated circuit chips was conventional and well-understood. For instance, other examples of laser dicing of integrated circuits are provided by

Akiyama and Dahn, which I discussed above. *See* EX1020, Abstract; EX1021, 1:6-9.

4. Analysis of claims

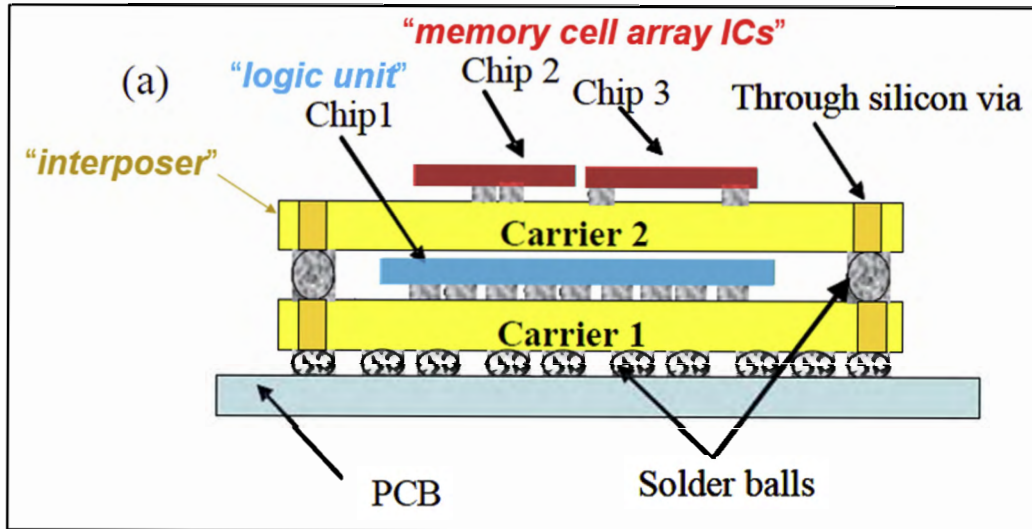
161. For the reasons below, claim 20 is obvious over the combination of Lee, Tsern, Khan, and Dozen.

(a) ***Claim 20***

[20a] The electronics system device of claim 19, further comprising: an interposer, wherein at least one memory cell array IC of the memory cell array group and the logic unit are disposed over two opposite sides of the interposer, respectively,

162. In Lee-Tsern-Khan combination, the memory devices 70 (corresponding to the claimed ***memory cell array ICs***) and memory hub 60 (corresponding to the claimed ***logic unit***) are arranged in a “3D stack package,” based on Khan, and as illustrated in the composite figure below. EX1009, 1, Fig. 1(a). Specifically, the memory hub (colored blue) is housed on a first carrier, and the memory devices (red) are housed on a second carrier. *See* EX1009, 1, Fig. 1(a). The second carrier (marked Carrier 2 by Khan) corresponds to the claimed ***interposer***, e.g., because it is a substrate disposed between ICs. In this 3D stack package, as illustrated below, the memory devices and the memory hub are disposed on opposite sides of Carrier 2 (satisfying the claimed requirement that the

at least one memory cell array IC and the logic unit are disposed over two opposite sides of the interposer).



Lee-Tsern-Khan composite figure based on Khan, Fig. 1(a)

[20b] wherein the interposer comprises silicon or oxide glass material,

163. Carrier 2 (corresponding to the *interposer*) is a “silicon interposer,” based on Khan, as I discussed above for element [21b]. EX1009, 1.

[20c] wherein a dicing method for at least one memory cell array ICs comprises a Laser cutting process.

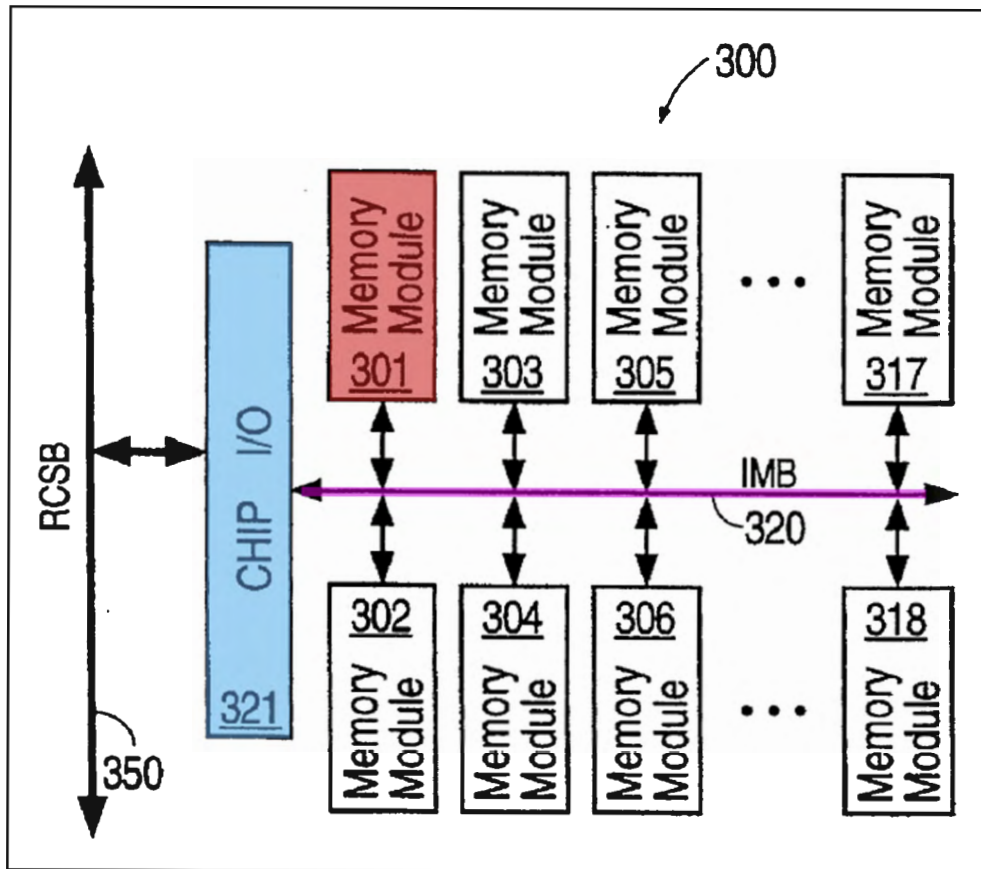
164. In the combination, memory devices (*e.g.*, DRAM devices, corresponding to the claimed *memory cell array ICs*) are formed in a wafer, *e.g.*, using conventional CMOS processes. See EX1007, 4:50-62. The wafer is then divided into individual memory devices by “dicing, scribing, using a cutting machine ..., laser cutting, or the like,” as taught by Dozen and as was

conventional. EX1007, 11:60-67. This processing satisfies the claimed requirement that *a dicing method for at least one memory cell array IC comprises a Laser cutting process.*

E. [Ground 1E]: Lee, Tsern, and Leung Render Obvious Claims 23 and 24

1. Leung (EX1008)

165. Leung describes a “memory system having several memory devices coupled to a memory controller through an I/O bus.” EX1008, Abstract. Each of Leung’s memory devices includes “multiple memory modules,” highlighted in red in FIG. 3, reproduced below, that are “coupled to a chip I/O interface [blue] through an internal bus [pink].” EX1008, Abstract.



Excerpt from Leung, FIG. 3 (annotated)

166. The internal bus in Leung’s system (also referred to as an “internal memory bus (IMB)”) is used “to communicate between the module bus interface (MBI) and the chip I/O. EX1008, 10:25-27. It “employs a unique signaling architecture designated here Directionally Asymmetric Signal Swing (DASS), which minimizes bus line driver size and noise associated with driving large capacitive loads.” EX1008, 10:25-35. Specifically, the internal memory bus is implemented such that “[l]arge signal swing is used in the point-to-multiple destinations mode, when master is driving the bus, while small swing is used in the point-to-point mode when one of many memory devices drives the bus.” *Id.*, 11:3-

7. This implementation “takes advantage of the asymmetry of communication in a master-slave communication environment where communication from master to slave is one-to-many (broadcast), but communication from slave to master is one-to-one” to “capitalize[] on the benefits of using both large and small signal swings on the same bus.” *Id.*, 10:66-11:3.

167. A one-to-many communications environment refers to a situation in which one device (sometimes called the master device) communicates concurrently to multiple connected devices (called the slave devices). A one-to-one communications environment refers to a situation in which communication is between two individual devices, e.g., from a slave device to a master device.

168. To implement Leung’s asymmetrical signal swing, “the chip I/O drives the IMB with full CMOS swing” using “normal CMOS inverters” for master-to-slaves (one-to-many) communication, *i.e.*, for communication from the chip I/O to the memory modules. EX1008, 11:52-54. In reverse, for slave-to-master (one-to-one) communication, “the MBI drives the IMB with a reduced signal swing.” *Id.*, 11:52-54. The reduced signal swing is achieved by “clamp[ing]” the signal swing “by the receiving circuitry in the chip I/O,” *e.g.*, using the feedback circuitry illustrated in FIG. 8. *Id.*, 11:55-58.

169. Leung is from the same field of endeavor (*e.g.*, memory systems) as the ’942 Patent.

170. Also, Leung is reasonably pertinent to the problem the '942 Patent was trying to solve in combining a type of memory cell array group and a logic unit (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25; EX1008, Abstract. For instance, with Leung’s architecture of combined logic and memory system, “the standby current ... can be eliminated,” which is relevant to development of memory systems with reduced greenhouse gas emissions. EX1008, 2:5-53; *see* EX1001, 1:17-25. Moreover, Leung’s asymmetrical signal swing “optimizes the speed, area and power of the bus system,” which is relevant to development of a high speed, low power, efficient memory system. EX1008, 2:60-63; *see* EX1001, 1:17-25.

2. The Lee-Tsern-Leung Combination

171. In the Lee-Tsern-Leung combination, the teachings of Leung regarding “asymmetrical signal swing” in the context of “a master-slave communication environment” are integrated into the communications along the high-speed link 58 and the bus systems 68 in the combination memory system. EX1008, 2:59-60, 10:66-11:3.

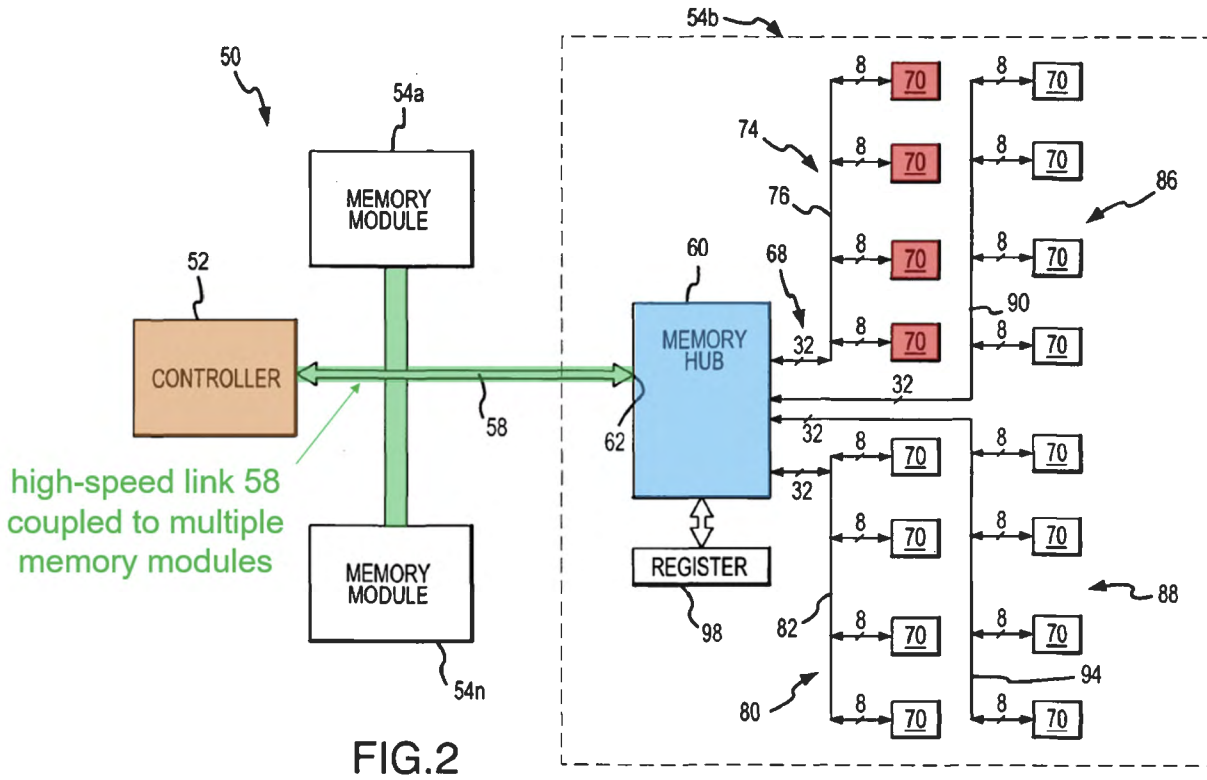
172. Specifically, in the combination, each of the individual bus systems 76, 82, 90, 94 that connects the memory hub to the respective rank of memory

devices is an example of the “master-slave communication environment” referenced by Leung, *i.e.*, in that each bus system connects a single memory hub (master) to multiple memory devices (slaves). In the Lee-Tsern-Leung combination, an asymmetrical signal swing is implemented on at least one of Lee’s bus systems 76, 82, 90, 94, based on Leung’s teachings of the suitability and advantages of asymmetrical signal swing in master-slave environments. *See* EX1008, 2:59-62, 10:64-11:7. This asymmetry involves using a “[l]arge signal swing” for communications from the memory hub to the ranks of memory devices (the one-to-many situation), and a “small swing” for communications from memory devices to the memory hub (the one-to-one situation). *Id.*, 11:3-7.

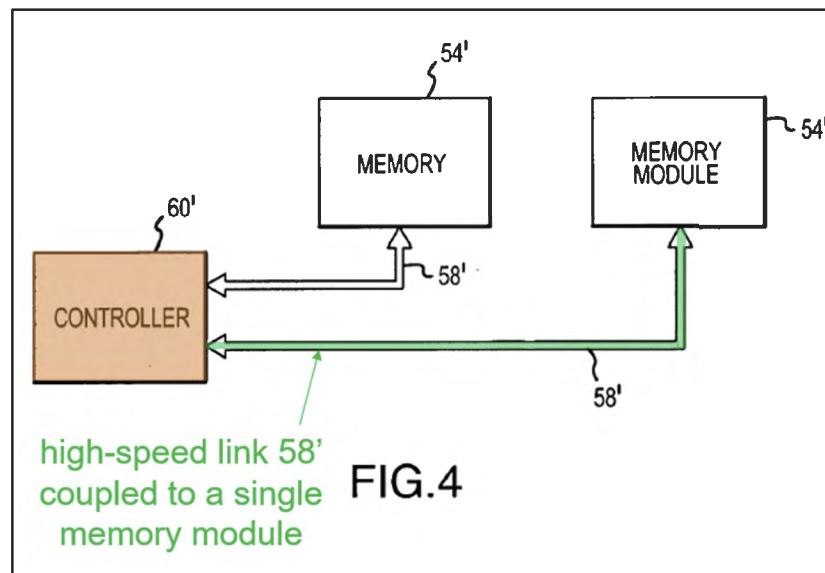
173. For instance, this asymmetry can be achieved using “first bus driver circuitry for generating a first signal swing for data transfer over said bus along a first direction, and a second bus driver circuitry for generating a second signal swing for data transfer over the bus along a second bus direction.” EX1008, 4:43-48. In more detail, “normal CMOS inverters” in the memory hub drive the bus systems 76, 82, 90, 94 with “full CMOS swing” for “one-to-many” communications from the memory hub to the memory devices of the corresponding rank. EX1008, 11:1-7, 52-54. In the opposite direction, for “one-to-one” communications from a memory device to the memory hub, “the signal

swing is clamped by [] receiving circuitry” in the memory hub, such as the circuitry illustrated in Leung’s FIG. 8. EX1008, 11:1-7, 54-57.

174. An asymmetric signal swing is implemented on the high-speed link 58 of the combination system based on Leung. The high-speed link 58 is another an example of a “master-slave communication environment.” EX1008, 10:67-11:1. This is because “the controller 60 is coupled to the memory modules 54 through the high-speed link 58 using multi-drop topography,” *i.e.*, coupled to multiple modules 54. This master-slave environment is illustrated in Lee’s FIG. 2, shown below. Notably, Lee contrasts this configuration—in which the controller is coupled to multiple memory modules—to the different configuration, shown in FIG. 4 (also below), in which there is “a separate high-speed link 58’ [] coupled to each memory module 54.” EX1004, [0022]; *see* FIG. 2 (*compare* to FIG. 4).



Excerpt from Lee, FIG. 2 (annotated)



Excerpt from Lee, FIG. 4 (annotated)

175. Specifically, “full CMOS swing” is implemented for “one-to-many” communications along the high-speed link 58 from the controller to the memory modules. EX1008, 11:1-7, 52-54. For “one-to-one” communications from a memory module to the controller along the high-speed link 58, “the signal swing is clamped by [] receiving circuitry” in the memory hub, *e.g.*, circuitry such as that illustrated in Leung’s FIG. 8. EX1008, 11:1-7, 54-57.

3. Motivation to Combine

176. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement an asymmetric signal swing on the bus systems of the Lee-Tsern-Leung combination memory system.

177. First, a POSITA would have recognized that implementation of an asymmetric signal swing “capitalizes on the benefits of using both large and small signal swings on the same bus,” allowing various performance benefits to be achieved. EX1008, 10:65-66. For instance, “[s]mall swing buses ... can be used to reduce power supply noise and the size of the bus line drivers, but small swing signal translators or amplifiers for each signal of the bus must be present in every memory module,” which “results in significant consumption of silicon area and power dissipation.” *Id.*, 10:56-63; *see* 1:32-59 (describing that reduced signal swing systems “enable high speed operations” and “reduce[] ... power consumption”). By contrast, systems with full signal swing avoid the silicon area

and power dissipation challenges typically associated with small signal swing systems.

178. Second, the architecture that enables implementation of asymmetric swing advantageously “minimizes bus line driver size and noise associated with driving large capacitive loads.” EX1008, 10:33-35. A reduction in circuit element size is advantageous, *e.g.*, in enabling compact, space-efficient devices. A reduction in noise is advantageous to ensure proper signal processing.

179. Third, a POSITA would have been motivated to implement an asymmetrical signal swing as taught by Leung, in the specific context of the master-slave environments of the combination memory system, because “an asymmetrical signal-swing internal bus optimizes the speed, area and power of the bus system with few masters and many slave devices.” EX1008, 2:59-62.

180. Fourth, implementation of asymmetrical signal swing for the buses of the combination memory system is merely the application of known techniques (*e.g.*, asymmetric signal swing in a memory array system) to a known structure (*e.g.*, Lee’s memory system), and yields predictable results (*e.g.*, a memory system having an asymmetrical signal swing on its bus systems).

181. A POSITA would have had a reasonable expectation of success in implementing asymmetrical signal swing in the combination memory system because memory system technology is predictable. Moreover, a POSITA would

have had a reasonable expectation of success because the asymmetrical (master-slave) circuit structures of Leung's system is generally similar in architecture to the asymmetric structure instantiated by Lee's memory hub connected to multiple ranks of memory cell devices, and by Lee's memory controller connected to multiple memory modules. *See* EX1008, 10:67-11:6; EX1004, [0009].

4. Analysis of claims

182. For the reasons below, claims 23 and 24 are obvious over the combination of Lee, Tsern, and Leung

(a) *Claim 23*

[23] The electronics system device of claim 22, wherein a signal swing of data transmitted through the first transmission bus and a signal swing of data received through the first transmission bus are different.

183. In the Lee-Tsern-Leung combination system, the signal swing on one or more of the bus systems 76, 82, 90, 94 (corresponding individually or collectively the ***first transmission bus***, as I discussed previously) is implemented an asymmetric signal swing based on Leung. Specifically, the bus systems are implemented to have “a first signal swing for data transfer over said bus along a first bus direction, and ... a second signal swing for data transfer over the bus along a second bus direction,” thus satisfying the claimed requirement that ***a signal swing of data transmitted through the first transmission bus and a signal swing of data received through the first transmission bus are different.*** EX1008, 4:43-

44; *see* Abstract (“a circuit for driving the internal bus with a full CMOS-swing in one bus direction and with a reduced CMOS-swing in the other bus direction”), 2:59-63 (“an asymmetrical signal-swing internal bus optimizes the speed, area and power of the bus system with few masters and many slave devices”), 11:64-12:12, 12:13-19, claim 16.

184. Specifically, for data transmitted from the memory hub to the memory devices along one of the bus systems (*i.e.*, a “one-to-many” environment in which the single memory hub communicates with multiple memory devices in multiple ranks), a “[l]arge signal swing is used,” based on Leung’s teachings of the suitability of a large signal swing for a one-to-many environment. EX1008, 11:1-7, 52-53. The large signal swing for communications from the memory hub to the memory devices is achieved by circuitry, *e.g.*, in the memory hub, that drives the bus system using “normal CMOS inverters,” as taught by Leung. EX1008, 11:1-7, 52-53; *see* 4:48-49 (“The first signal swing is a full CMOS-swing”).

185. In the opposite direction, for data transmitted from a memory device to the memory hub along the bus system (*i.e.*, a “one-to-one” environment), a “small swing” is used,” again based on Leung’s teachings of the suitability of a small signal swing for a one-to-one environment. *Id.*, 11:1-7, 53-57. The small signal swing for communications from a memory device to the memory hub is achieved, *e.g.*, by “clamp[ing]” the signal swing using feedback circuitry

implemented in the memory hub, as taught by Leung. *Id.*, 11:1-7, 53-57; *see* 4:49-51 (“the second signal swing is a reduced swing substantially smaller than the first signal swing”).

(b) ***Claim 24***

[24] *The electronics system device of claim 22, wherein a signal swing of data transmitted through the second transmission bus and a signal swing of data received through the second transmission bus are different.*

186. In the Lee-Tsern-Leung combination system, the signal swing on the high-speed link 58 (corresponding to the claimed ***second transmission bus***) is an “asymmetric signal swing” based on Leung. Specifically, the high-speed link 58 is implemented to have “a first signal swing for data transfer over said bus along a first bus direction, and ... a second signal swing for data transfer over the bus along a second bus direction,” thus satisfying the claimed requirement that ***a signal swing of data transmitted through the second transmission bus and a signal swing of data received through the second transmission bus are different.***

EX1008, 4:43-44; *see* Abstract, 2:59-63, 11:64-12:12, 12:13-19, claim 16.

187. Specifically, for data transmitted from the controller to the memory modules along the high-speed link (*i.e.*, a “one-to-many” environment in which the single controller communicates with multiple memory modules), a “[l]arge signal swing is used.” EX1008, 11:1-7, 52-53; *see* 4:48-49. The large signal swing for communications from the memory hub to the memory devices is achieved by

circuitry, *e.g.*, in the memory hub, that drives the bus system using “normal CMOS inverters,” as taught by Leung. EX1008, 11:1-7, 52-53; *see* 4:48-49 (“The first signal swing is a full CMOS-swing”).

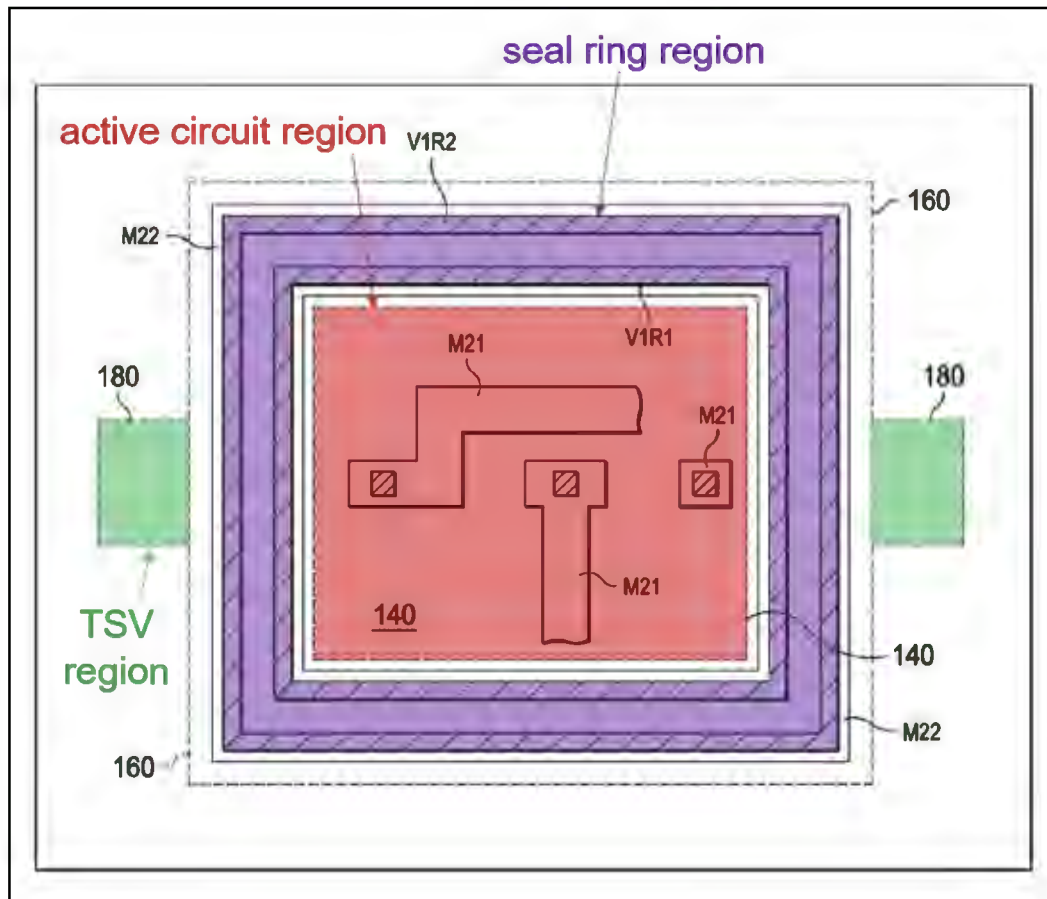
188. In the opposite direction, for data transmitted from a memory module to the controller along the high-speed link (*i.e.*, a “one-to-one” environment), a “small swing” is used,” again based on Leung’s teachings of the suitability of a small signal swing for a one-to-one environment. *Id.*, 11:1-7, 53-57. The small signal swing for communications from a memory device to the memory hub is achieved *e.g.*, by “clamp[ing]” the signal swing using feedback circuitry implemented in the memory hub, as taught by Leung. *Id.*, 11:1-7, 53-57; *see* 4:49-51 (“the second signal swing is a reduced swing substantially smaller than the first signal swing”).

F. [Ground 1F]: Lee, Tsern, and Lin Render Obvious Claim 27, 28, and 31

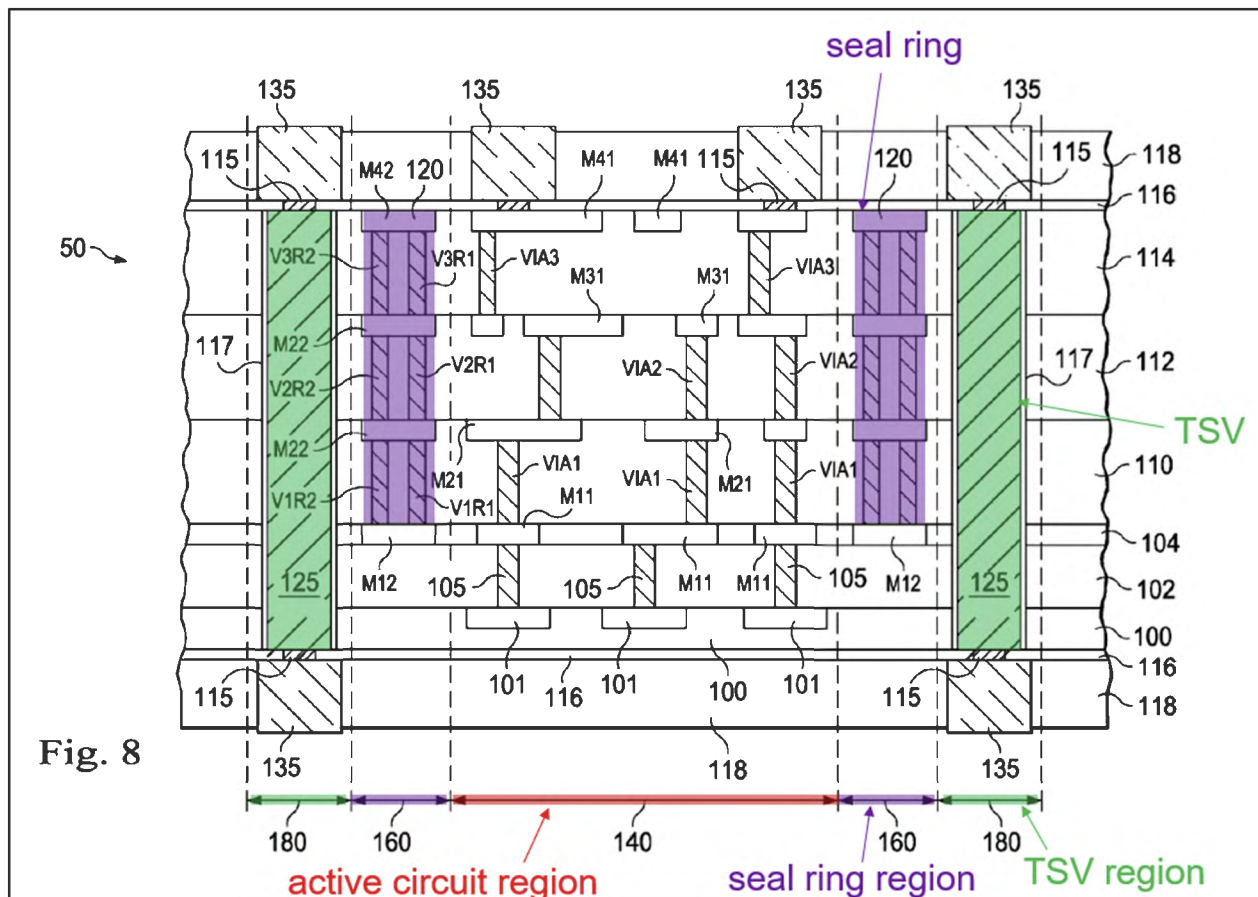
1. Lin

189. Lin describes “formation of a seal ring in a semiconductor integrated circuit (IC) die.” EX1013, Abstract. This is shown in top view in Fig. 3b and side view in Fig. 8, both of which I have reproduced and annotated below. As illustrated in these figures, Lin describes a wafer that includes “an active circuit region 140,” highlighted in red. *Id.*, [0016]. The active circuit region “defines a wafer surface area where semiconductor devices are formed in its underlying

substrate area and coupled together to make functional circuit units.” *Id.*, [0016]. That is, the logic circuitry for the IC, such as transistors and associated connections, is formed in the active circuit region. A “seal ring region 160” (highlighted in purple) “encompass[es] an adjacent active circuit region.” *Id.*, [0016]. As can be seen particularly in the top view of Fig. 3b, the seal ring region surrounds the active circuit region. The seal ring region “defines a wafer surface area where one or more seal rings are formed in the wafer,” *e.g.*, seal ring 120, as can be seen in Fig. 8. *Id.*, [0024]. The seal ring is a “stacking structure” that is formed of metal features in multiple interconnect layers. *Id.* Finally, “TSV regions 180” (green) “defines a wafer surface area where a through-silicon via [TSV] is to be formed,” *e.g.*, TSVs 125, as shown in Fig. 8. *Id.*, [0016], [0028].



Excerpt from Lin, Fig. 3b (annotated)



Excerpt from Lin, Fig. 8 (annotated)

190. The objective of Lin’s seal ring design is to act as a barrier in order to “prevent[] moistures or other undesired chemical agents from diffusing into the active circuit region during the subsequent processes of forming TSVs.” EX1013, Abstract. Without a seal ring, damage can occur to the active circuit region during later TSV formation processes. As Lin explains, “the formation of the TSV recesses in the inter-metal dielectric layers typically involves multiple etch processes,” and during this processing, “moisture or other chemical agents in a water processing facility ay leach into the low-k inter-metal dielectric layers from

the side wall of the TSV recesses and diffuse throughout the inter-metal dielectric layers.” *Id.*, [0006]. The result is that this “may lead to undesired characteristic change of the low-k dielectric materials,” which “can be significant and cause serious device performance degradation and yield loss.” *Id.*

191. Lin is reasonably pertinent to the problem the ’942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25. For instance, Lin’s seal rings “prevent[] moistures or other undesired chemical agents from diffusing into the active circuit region during the subsequent processes of forming TSVs,” which improves reliability and yield. EX1013, Abstract. A high yield process for manufacturing reliable chips used in a memory system is relevant to reducing the greenhouse gas emission rate associated with that memory system, *e.g.*, because higher yield of reliable chips reduces waste. *See* EX1001, 1:17-25.

2. The Lee-Tsern-Lin Combination

192. In a system based on the combination of Lee, Tsern, and Lin, the memory hub 60 and the memory devices 70 are IC chips (as I have already discussed), with each of the chips structured based on the teachings of Lin to include a seal ring and one or more TSVs. In the case of the memory hub chip,

logic circuitry (*e.g.*, transistors and associated circuitry) for execution of memory hub functionality is formed in the active circuit region of the chip, *e.g.*, as is the case for Lin's active circuit region 140. In the case of the memory devices (*e.g.*, DRAM chips), memory circuitry (*e.g.*, transistors and associated circuitry) for storage/execution of storage related functions is formed in the active circuit region of each chip, again as is the case for Lin's active circuit region 140. *See* EX1013, [0015], Fig. 3b, Fig. 8. A seal ring, *e.g.*, a stacking structure as described by Lin for the seal ring 120, is formed in a seal ring region surrounding the active circuit region, *e.g.*, as is the case for the seal ring formed in Lin's seal ring region 160. *See id.*, [0016], [0024], Fig. 3b, Fig. 8. Outside of the seal ring region, TSVs are formed in a TSV region, again based on Lin's teachings. *See id.*, [0016], [0028], Fig. 3b, Fig. 8.

3. Motivation to Combine and Expectation of Success

193. It is my opinion that there are a number of reasons that would have motivated a POSITA to structure the memory hub and memory device ICs in the combination to each include a seal ring and one or more TSVs, based on the teachings of Lin.

194. First, having TSVs in the ICs (*e.g.*, memory hub ICs and/or memory device ICs) in the Lee-Tsern-Lin combination system allows the chips to be stacked "as three-dimensional structures." EX1013, [0003]. Being able to arrange

chips in a stacked arrangement is advantageous for several reasons. First, stacking of chips “significantly reduce[s] the communication path length between components on different dies,” and as a result, “the overall system speed is ... increased.” *Id.*, [0003]. Also, stacking of chips provides additional benefits including “improved form factors, lower costs, and greater integration through system-on-chip (SOC) solutions.” *Id.*, [0004]. I note that a stacked arrangement of memory hub and memory device ICs is consistent with the stacked arrangement of chips illustrated in Tsern’s Fig. 11, and which is an example of how the chips in the Lee-Tsern memory system would have been arranged, as I discussed above.

195. Second, the formation of a seal ring has advantages that are described by Lin. Specifically, the positioning of a seal ring between the active circuit region and the TSVs “block[s] moistures or other undesirable chemical agents from diffusing into [the] active circuit region 140 during the various wafer processing steps” involved in forming the TSVs. EX1013, [0016]. As a result, good quality, reliable ICs can be fabricated. Indeed, Lin describes that seal rings “prevent deleterious affects [sic] of the TSV formation process from impacting the active region.” *Id.*, [0023]. In contrast, in ICs without such seal rings, “moisture or other chemical agents in a wafer processing facility may leach into the low-k inter-metal dielectric layers from the side wall of the TSV recesses and diffuse throughout the inter-metal dielectric layers, which may lead to uncharacteristic change of the low-

k dielectric materials” and resulting in “serious device performance degradation and yield loss.” *Id.*, [0006].

196. Third, the incorporation of seal rings and TSVs in the memory hub and memory cell ICs of the combination is merely an application of known techniques (specifically, seal rings and TSVs in ICs, as taught by Lin) to a known structure (*e.g.*, memory hub and memory device ICs of the memory system based on the Lee-Tsern combination), and it yields predictable results (that is, a memory system in which the memory hub and memory device ICs have seal rings and TSVs).

197. A POSITA would have had a reasonable expectation of success in implementing seal rings and TSVs in the memory hub and memory device ICs of the combination because integrated circuit structure is predictable, and because implementation of both TSVs and seal rings in ICs was conventional. For instance, among other examples of TSVs and seal rings in the literature, White describes TSVs in integrated circuits that are used to route power and ground to an interior-located active region. *See* EX1014, Abstract, FIG. 1A. And Pan describes integrated circuits with die seal rings. *See* EX1022, Abstract. Finally, a POSITA also would have had a reasonable expectation of success because the structures enabled by incorporation of TSVs and seal rings into the memory hub and memory device ICs of the combination (that is, a stacked arrangement of chips) is

consistent with one way in which the Lee-Tsern combination can be arranged. *See* EX1005, Fig. 11.

4. Analysis of claims

198. For the reasons below, claims 27, 28, and 31 are obvious over the combination of Lee, Tsern, and Lin.

(a) **Claim 27**

[27] The electronics system device of claim 19, wherein each of the memory cell array ICs of the type of memory cell array group corresponds to a first seal ring and the logic unit corresponds to a second seal ring, a circuit of each of the memory cell array ICs is surrounded by the first seal ring and a circuit of the logic unit is surrounded by the second seal ring.

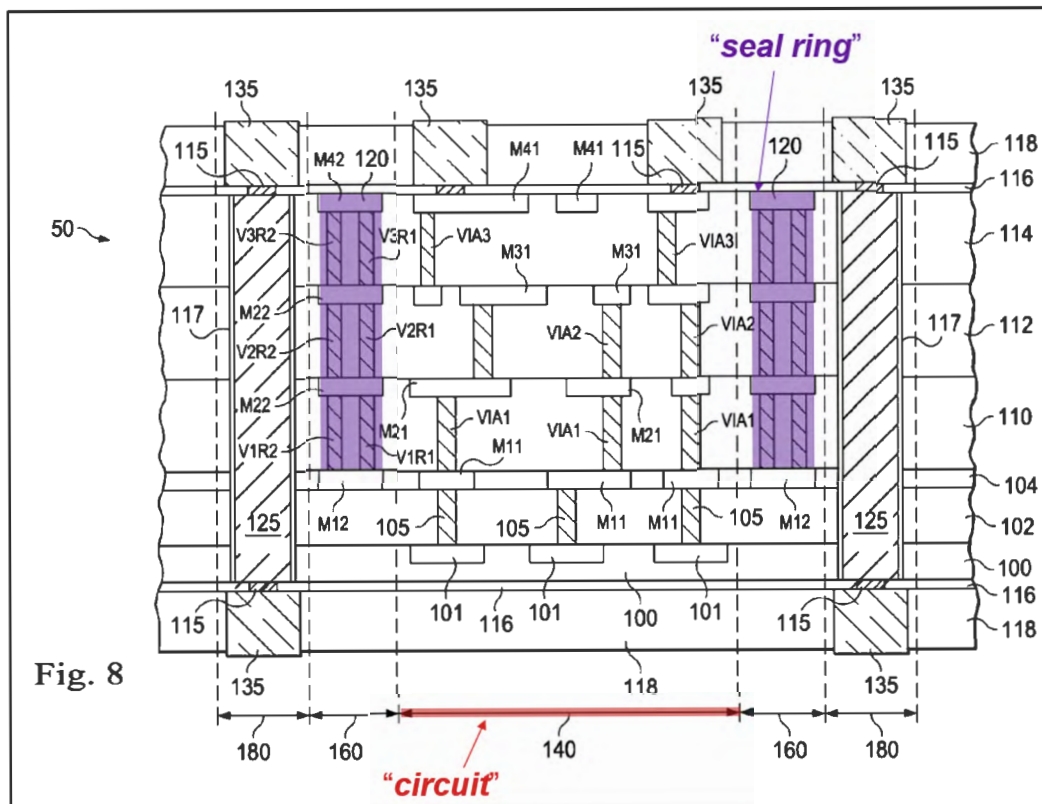
199. In the Lee-Tsern-Lin combination, the memory hub (corresponding to the claimed **logic unit**) and each memory device (corresponding to the claimed **memory cell array ICs**) are integrated circuits that have a structure based on the teachings of Lin.

200. Specifically, in the case of the memory hub chip, logic circuitry (*e.g.*, transistors and associated circuitry) for execution of memory hub functionality is formed in the active circuit region of the chip, *e.g.*, as is the case for Lin's active circuit region 140. This "active circuit region" corresponds to the claimed **circuit of the logic unit** at least because it includes "semiconductor devices ... coupled together to make functional circuit units." EX1013, [0016]. Similarly, in the case

of the memory devices (e.g., DRAM chips), memory circuitry (e.g., transistors and associated circuitry) for storage/execution of storage related functions is formed in the active circuit region of each chip, again as is the case for Lin's active circuit region 140. See EX1013, [0015], Fig. 3b, Fig. 8. This "active circuit region" corresponds to the claimed *circuit of each of the memory cell array ICs* at least because it includes "semiconductor devices ... coupled together to make functional circuit units." EX1013, [0016]. The active circuit region is highlighted in red in Lin's Figs. 3b and 8, which I have reproduced and annotated below.

201. Also based on Lin, each integrated circuit (i.e., the memory hub and each memory device) includes "a stacking structure 120 in the seal ring region 160, ... also interchangeably referred to as seal ring 120." EX1013, [0024]. I have highlighted both the seal ring region 160 and the seal ring 120 itself in purple. When this structure is applied to the memory devices, each memory device has a seal ring, which satisfies the claimed requirement that *each memory cell array IC corresponds to a first seal ring*. Likewise, when this structure is applied to the memory hub, the memory hub has a seal ring, which satisfies the claimed requirement that the *logic unit corresponds to a second seal ring*. See also [0008] ("a seal ring is interposed between the active region and the TSV, the seal ring comprising a plurality of stacked features formed in respective ones of the plurality of metal interconnect layers"), [0016] ("numerous active regions, seal ring regions,

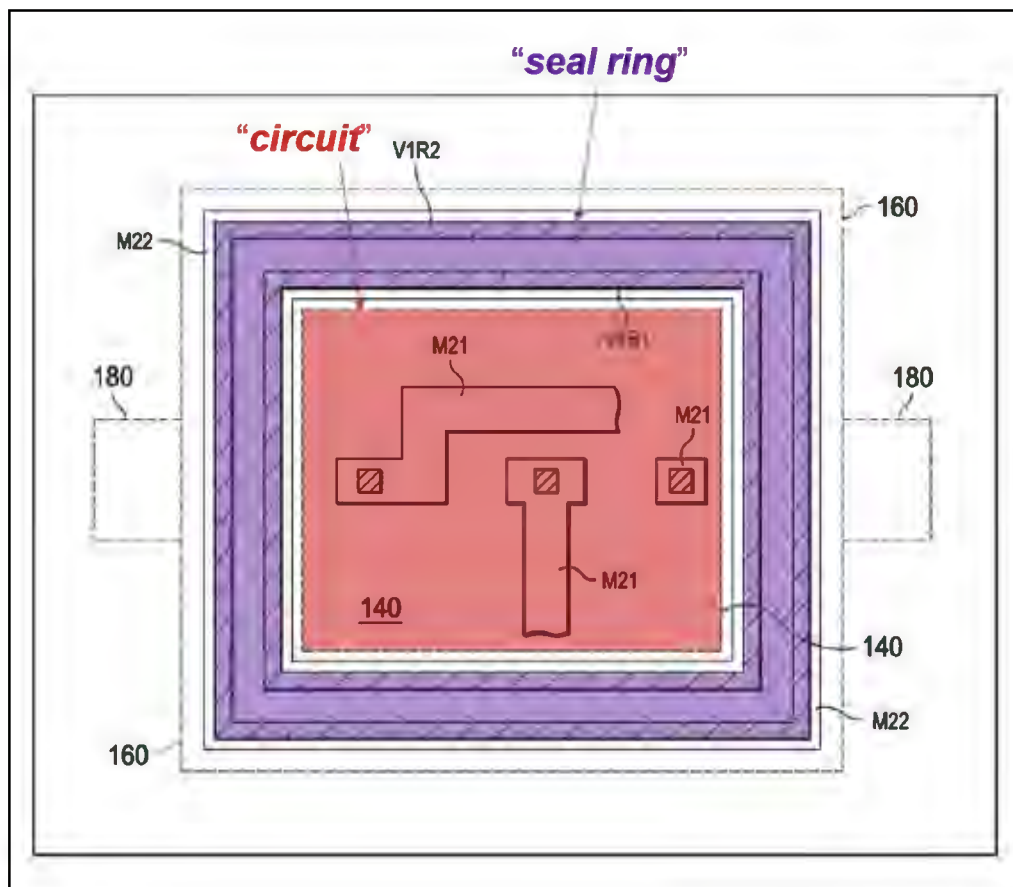
and TSV regions can ... be formed on a given die”), [0024] (“the diffusion of these undesired species is substantially blocked from diffusing into an adjacent active circuit region 140 on wafer 50 by seal ring 120”), [0035] (“The 3D stacking structure comprises a die 50 with a seal ring 120), Abstract, [0002], [0007]-[0010], [0012]-[0013], [0016], [0024], claim 1, FIGS. 8-9.



Excerpt from Lin, Fig. 8 (annotated)

202. Consistent with the structure of Lin’s IC, the seal ring of each IC “encompasses an adjacent active circuit region 140.” EX1013, [0024]; *see* Abstract (“A seal ring is formed in the inter-metal dielectric (IMD) layers of an IC die, enclosing an active circuit region”). The seal ring surrounding the active

circuit region can be seen in Lin's Fig. 3b, below. This arrangement satisfies the claimed requirements that *a circuit of each of the memory cell array ICs is surrounded by the first seal ring* (i.e., a seal ring encompasses/surrounds the active circuit region of each memory device IC) and that *a circuit of the logic unit is surrounded by the second seal ring* (i.e., a seal ring encompasses/surrounds the active circuit region of the memory hub IC).

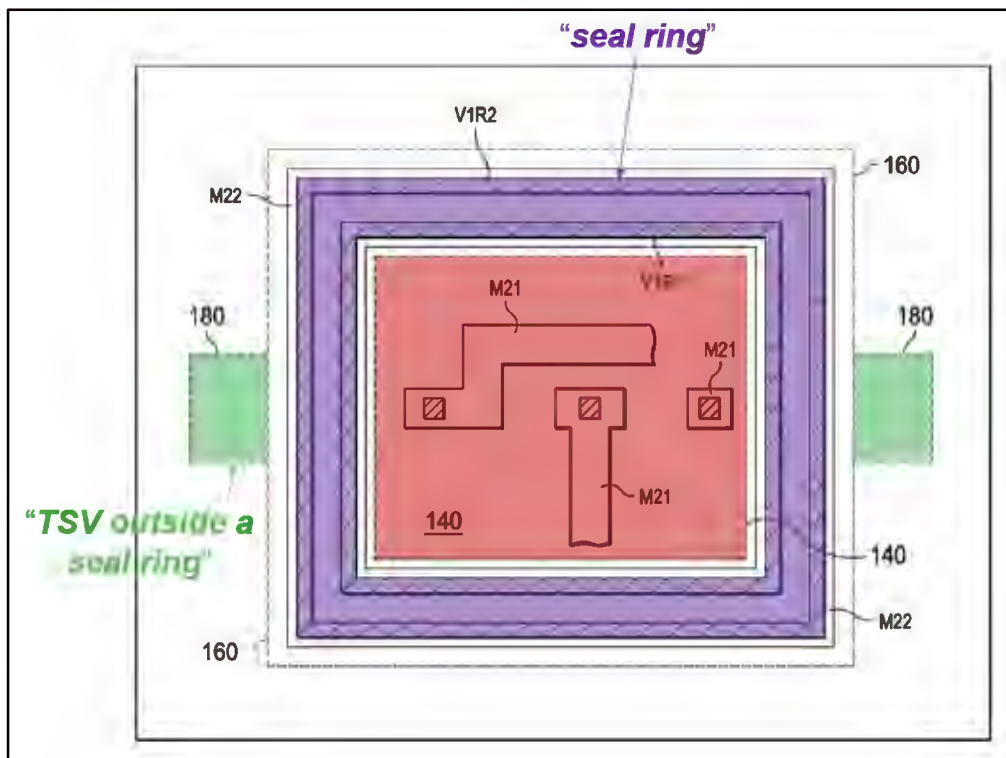


Except from Lin, Fig. 3b (annotated)

(b) **Claim 28**

[28] *The electronics system device of claim 27, wherein at least one TSV exists outside a first seal ring of each of the memory cell array ICs.*

203. Based on Lin, each combination memory cell IC has a “through-silicon via[]” (corresponding to the claimed *at least one TSV*) formed in a “TSV region.” EX1013, [0016], [0028]. I have highlighted both the TSV and the TSV region green in Figs. 3b and 8, below. As described by Lin, the “TSV region [is] separated from active circuit region by the seal ring.” EX1013, [0010]. This means that the seal ring (purple) is positioned between the TSV region and the active circuit region (red), and can be seen in both Figs. 3b and 8. This arrangement satisfies the claimed requirement that *at least one TSV exists outside of the seal ring* at least because the TSV is formed in the TSV region, which is on an opposite side of the seal ring from the active circuit region.



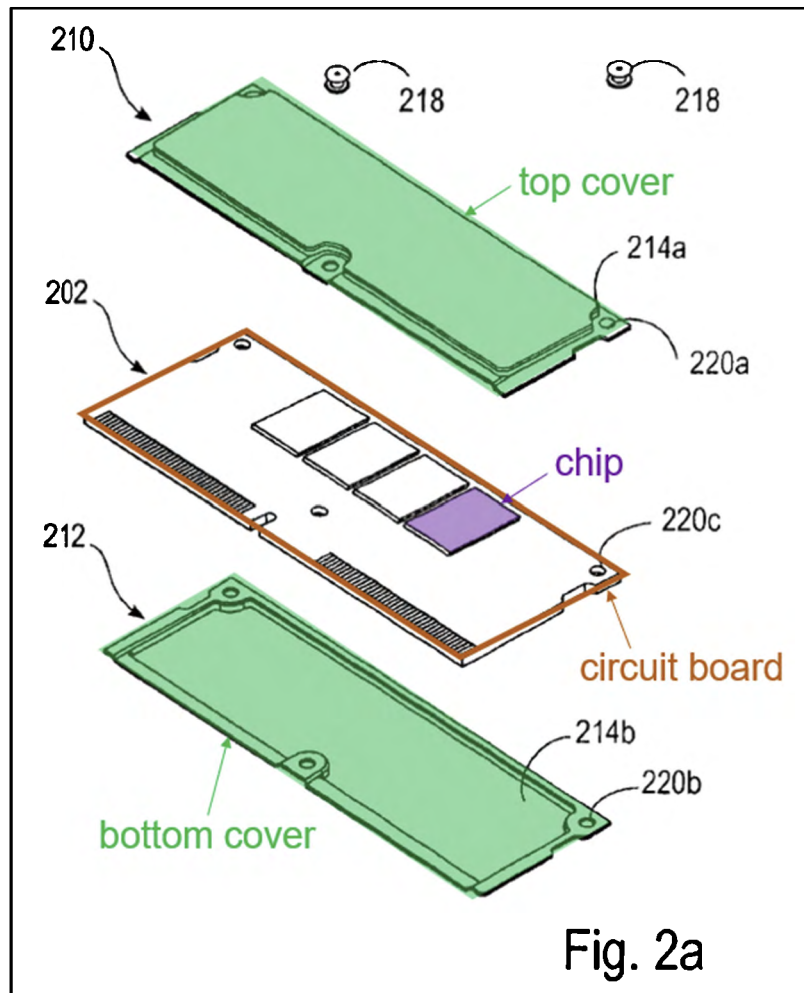
Except from Lin, Fig. 3b (annotated)

one TSV exists outside of the seal ring at least because the TSV is formed in the TSV region, which is on an opposite side of the seal ring from the active circuit region.

G. [Ground 1G]: Lee, Tsern, Lin, and Ali Render Obvious Claim 29

1. Ali

205. Ali describes a “packaging cover for a multi-chip memory module.” EX1015, 2:27-28. The packaging cover, illustrated in FIG. 2a, below, includes a top cover 210 and a bottom cover 212, both of which I have highlighted in green. Each cover has “a size large enough to cover/encapsulate the chips 204-210 on the circuit board 202.” *Id.*, 3:7-9. I have highlighted one chip in purple, and outlined the circuit board in orange. Ali’s packaging includes a “thermally conductive gel [that] provides a thermal coupling between the memory chips and the inner surface of the packaging cover.” *Id.*, 3:34-36. When “the cover[s] of the packaging are assembled ... a seal is formed encapsulating the memory chips and conductive gel within the package.” *Id.*, 3:45-50. The covers may be made of “metal material,” so that “the surface of the covers may act as a heat sink mechanism in spreading localized heat sources from one or more of the chips into the larger conductive surface area of the packaging cover.” *Id.*, 3:53-62.



Excerpt from Ali, Fig. 2a (annotated)

206. Ali from the same field of endeavor (*e.g.*, memory systems) as the '942 Patent. *See* EX1001, 1:17-25; EX1015, Abstract.

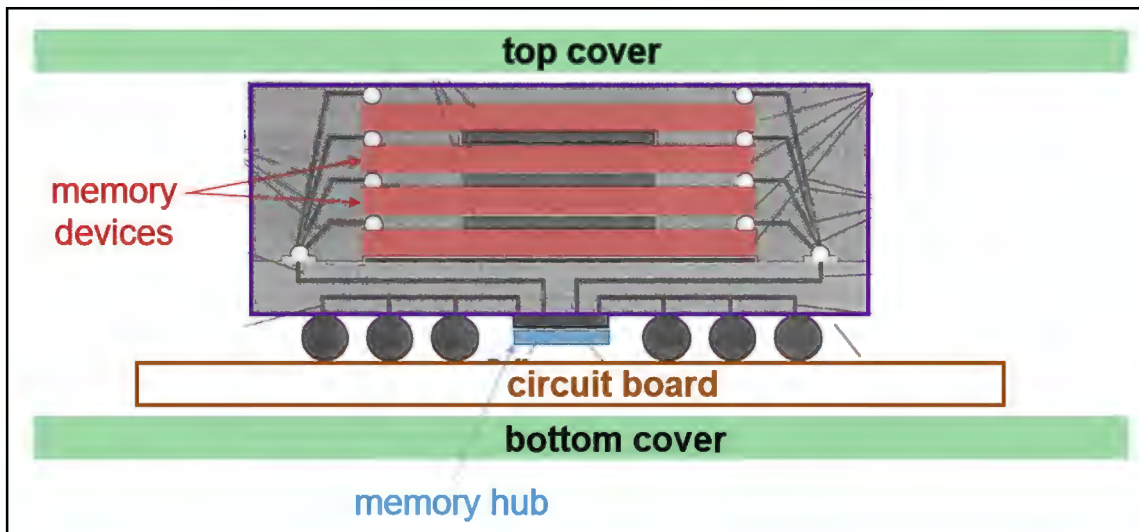
207. Also, Ali is reasonably pertinent to the problem the '942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25; EX1015, Abstract. For instance, Ali's

packaging cover “provides localized heat dissipation,” which is relevant to development of memory systems with “better heat dissipation capability.”

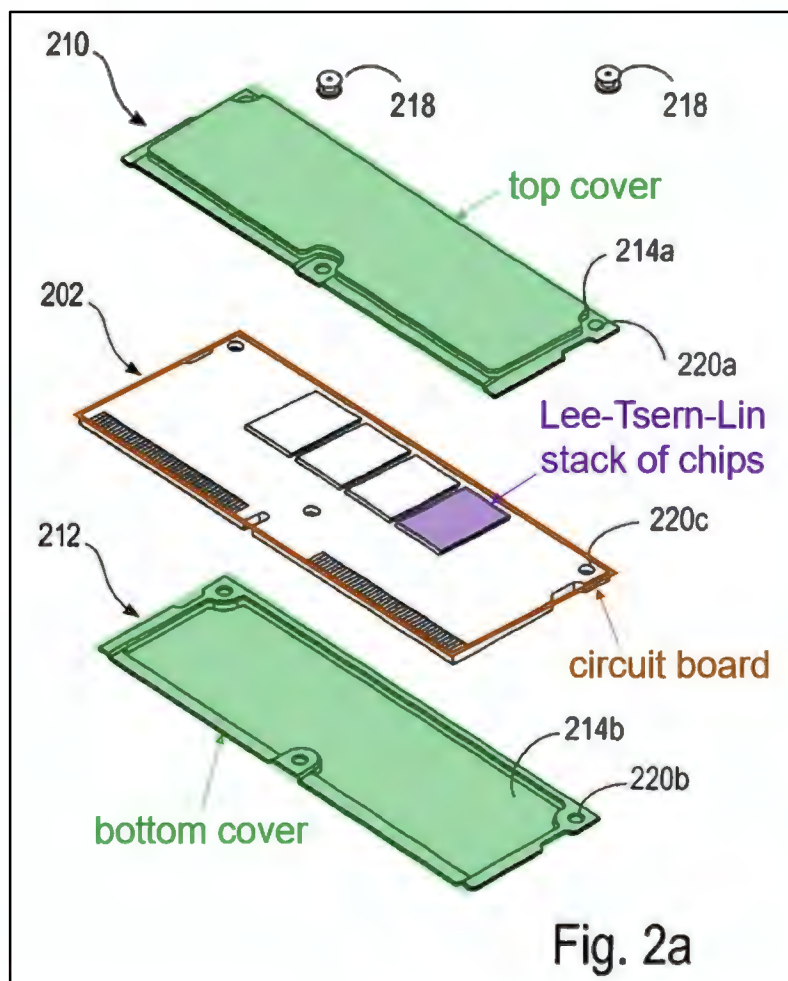
EX1015, Abstract; EX1001, 1:17-25.

2. The Lee-Tsern-Lin-Ali Combination

208. In a system based on the combination of Lee, Tsern, Lin, and Ali, the memory device ICs and memory hub IC are arranged in a stacked arrangement, *e.g.*, based on Tsern’s Fig. 11, as I discussed earlier. For instance, each rank of memory devices can be arranged in a respective stack. The chip stacks are packaged between top and bottom covers, based on Ali, *e.g.*, as illustrated in the first composite figure below, which shows a single stack of chips. For instance, multiple chip stacks (one for each rank of memory devices) are assembled on a circuit board and packaged in a “package covering” based on Ali, such that “top and bottom covers will cover/encapsulate” the stack(s) of chips “on both sides.” EX1015, 3:4-6. The “top and bottom covers [are] made of metal material” to “act as a heat sink mechanism.” *Id.*, 3:57-59.



Lee-Tsern-Lin-Ali composite figure based on Tsern, Fig. 11



Lee-Tsern-Lin-Ali composite figure based on Ali, Fig. 2a

3. Motivation to Combine and Expectation of Success

209. It is my opinion that there are a number of reasons that would have motivated a POSITA to package chip stacks in a packaging cover based on Ali.

210. First, encapsulating the chip stacks in metal covers provides “heat sink” functionality, “spreading localized heat sources” from one or more of the chip stacks and thus helping to prevent overheating. EX1015, 3:57-61. For instance, the ability to dissipate heat is relevant when “varying amounts of heat” are generated among the various stacks, and where the amount of heat “changes dynamically among the chips.” EX1015, 1:45-50.

211. Second, packaging the chip stacks provides “protection of the memory module,” *e.g.*, remedying an otherwise “very fragile attachment” of the stacks “to the board.” EX1015, 3:1-3; *see* 1:25-27 (“the interconnection between the chips and the circuit board is very fragile and susceptible to mechanical damages”). For instance, because the covers are “rigid,” they “protect[] the memory chips against mechanical loads ... [and] also helps to increase the surface area of any concentrated load/force such that the induced mechanical stresses are minimized.” EX1015, 4:15-22.

212. Third, to the extent that multiple chip stacks are encapsulated in a single package, the packaging can “accommodate for the potential variances in the height among the multiple” stacks of the memory module.” EX1015, 1:53-55.

213. Fourth, packaging chip stacks in a package is merely the application of known techniques (specifically, packaging of chips in a multi-chip memory module) to a known structure (*e.g.*, the Lee-Tsern stack of memory chips and memory hub), and it yields predictable results (that is, a packaged chip stack).

214. A POSITA would have had a reasonable expectation of success in packaging the chip stacks of the combination based on Ali's teachings because packaging technology was predictable, and because Ali relates to packaging in the specific context of memory modules. *See* EX1015, Abstract.

4. Analysis of claims

215. For the reasons below, claim 29 is obvious over the combination of Lee, Tsern, and Ali.

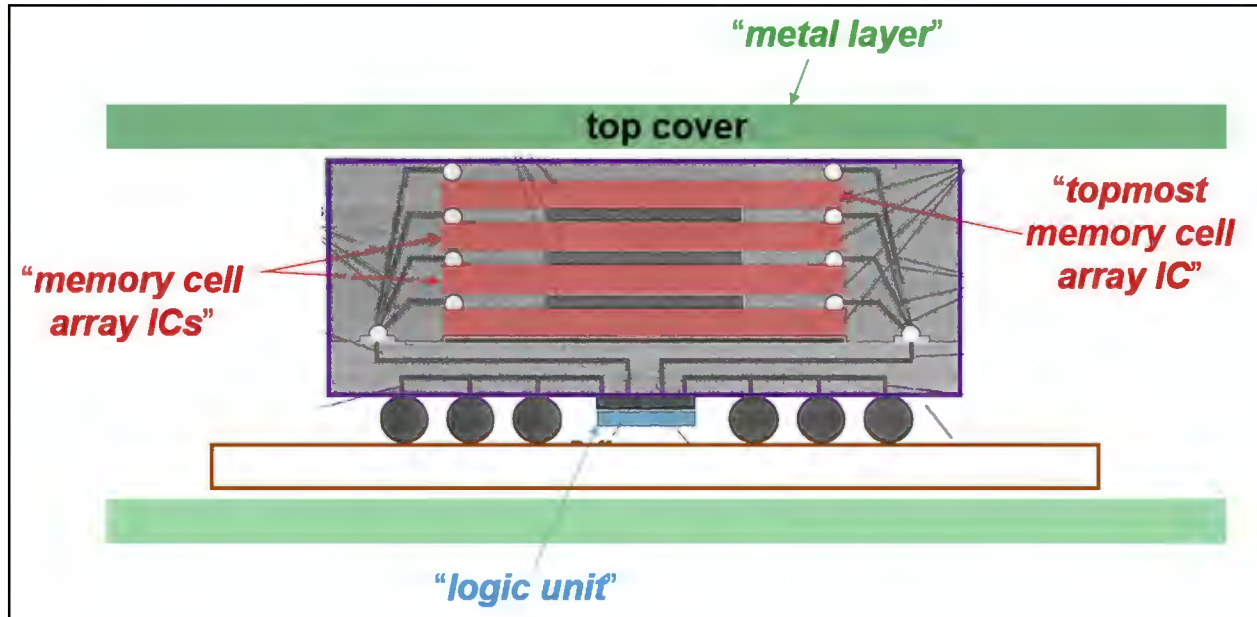
(a) Claim 29

[29a] The electronics system device of claim 28, further comprising: a metal layer disposed over a topmost memory cell array IC of the type of memory cell array group, wherein the metal layer covers more than 50% area of the topmost memory cell array IC

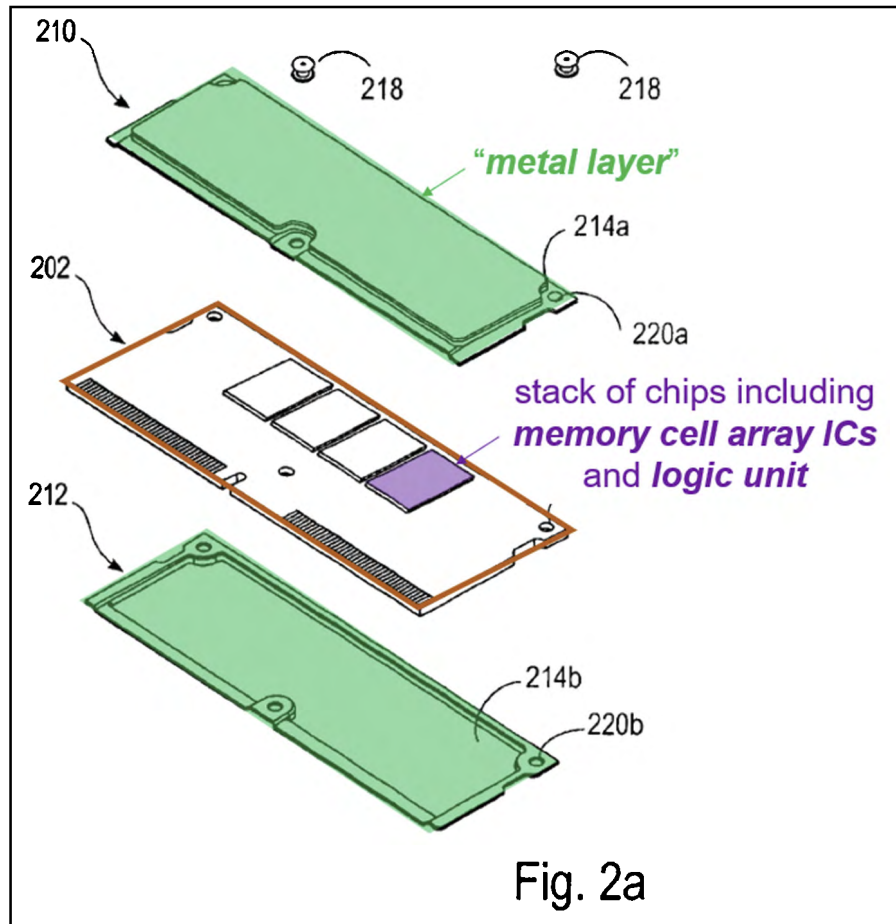
216. In the combination, the "top cover 210" (highlighted green in the two composite figures below), which is "made of metal material," corresponds to a **metal layer**. EX1015, 3:7, 57-58; *see* Abstract, 3:64-4:2; 4:14-15, claim 10.

217. The memory cell array ICs and logic unit, stacked as taught by Tsern, are packaged in packaging based on Ali, *e.g.*, between top and bottom covers, as

illustrated in the two composite figures below, such that “the top and bottom covers will cover/encapsulate” a stack of chips “on both sides.” EX1015, 3:111-12; *see* Abstract, 2:1-2, 2:49-50, claim 1, Fig. 2a. When the top cover “cover[s]” the stack, it is *disposed over the topmost memory cell array IC*. Moreover, because the covers “have a size large enough to cover/encapsulate” the stack of chips, the top cover (*metal layer*) is sized to *cover more than 50% area of the topmost memory cell array IC*. EX1015, 3:8-9.



Lee-Tsern-Lin-Ali composite figure based on Tsern, Fig. 11



Lee-Tsern-Lin-Ali composite figure based on Ali, Fig. 2a

[29b] wherein the memory cell array ICs are stacked over the logic unit.

218. In the stacked arrangement of chips based on Tsern, the memory cell array ICs (red in the composite figure above) are ***stacked over*** the logic unit (blue). See EX1005, 26 (“a plurality of integrated circuit memory dies 1101a-d and a buffer die 1100a may be stacked”), Fig. 11.

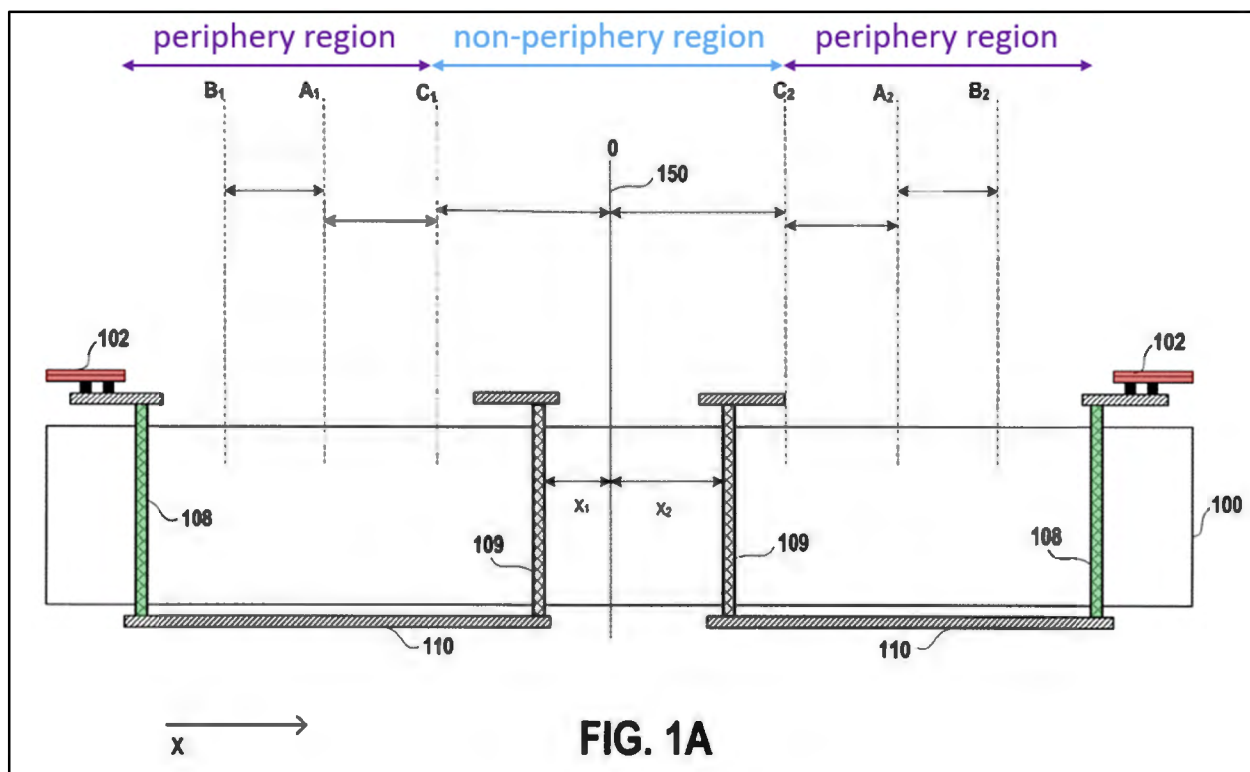
H. [Ground 1H]: Lee, Tsern, Lin, and White Render Obvious Claim 30

1. White

219. White describes an “integrated circuit with distributed power using through-silicon vias (TSVs).” EX1014, Abstract. White’s integrated circuit has a “non-periphery region ... where the active device processing occurs,” marked in blue in FIG. 1A, below. EX1014, 3:26-30. Surrounding the non-periphery region is a “periphery region,” marked in purple. EX1014, 3:26-30; *see* 3:29-44. White provides various options for the extent of the periphery and non-periphery regions, and the marked regions below are consistent with one of these options.

Specifically, White states that “[i]n one IC layout, the non-periphery region could span the area between C1 and C2” (as marked in the figure below), while “in another IC layout, the non-periphery region may span the area between A1 and A2.” *Id.*, 3:31-36. Similarly, regarding the periphery region, “[i]n one IC layout, the periphery portion extends from the bonding pads 102 [marked in red] to B1 and B2, while in another IC layout the periphery portion extends from the bonding pads 102 to C1 and C2.” *Id.*, 3:38-41.

220. “TSVs 108 and 109” (highlighted in green in FIG. 1A, below) “may be used to route power and ground from the bonding pads 102, to the non-periphery region.” *Id.*, 3:48-49. For instance, “a power source” can be “coupled to the conductive bondpads 102.” *Id.*, 4:35.



Excerpt from White, FIG. 1A (annotated)

221. White is reasonably pertinent to the problem the '942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25. For instance, White’s TSV-mediated power supply architecture “provid[es] a constant voltage to circuits located within the non-periphery region,” which is relevant to questions of power consumption. EX1014, 2:5-7; *see* EX1001, 1:17-25.

2. The Lee-Tsern-Lin-White Combination

222. The ICs of the Lee-Tsern-Lin-White combination have peripherally located TSVs based on the teachings of Lin, as I discussed above for the Lee-Tsern-Lin ground. *See* EX1013, [0016], [0028], Fig. 3b, Fig. 8. The TSVs are located exterior to the active circuit region, as also taught by Lin. *See id.*, Fig. 3b, Fig. 8. In the Lee-Tsern-Lin-White combination, these peripheral TSVs connect to bonding pads to “route power and ground from the bonding pads 102, to the non-periphery region,” *e.g.*, to the active circuit region where the semiconductor devices are formed (*e.g.*, memory circuitry, for the memory device ICs; or memory hub circuitry, for the memory hub IC). EX1014, 3:48-49; *see* EX1013, [0016].

3. Motivation to Combine and Expectation of Success

223. A POSITA would have been motivated to use the TSVs of the Lee-Tsern-Lin ICs for connection to power or ground, as taught by White, for at least the following reasons.

224. First, distributing power from peripheral to non-peripheral regions of a chip using TSVs, as taught by White, advantageously “reduces the effect of resistive voltage drops on a conducting line,” contributing to improved performance and stability. EX1014, 4:16-29.

225. Second, the use of TSVs to connect to power or ground was conventional, and a POSITA would have been motivated to design the chips of the

combination consistent with conventional IC design approaches. EX1014, 3:1-2 (“there are several well-known methods which can be used to manufacture TSVs”); EX1025, [0025] (describing a “TSV 150 which couples to bond pad 44 for coupling bond pad 44 to ground”)

226. Third, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, TSVs connected to power or ground) to a known structure (*e.g.*, the Lee-Tsern-Lin ICs, having peripheral TSVs), and it yields predictable results (*e.g.*, an IC in which a peripheral IC is used for connection to power/ground, *e.g.*, to provide power to non-peripheral active circuit elements).

227. A POSITA would have had a reasonable expectation of success in pursuing this implementation because the positioning of the TSVs in the Lee-Tsern-Lin combination ICs (*i.e.*, peripheral to the active circuit region) is consistent with the positioning of White’s TSVs (*i.e.*, in the peripheral region of the chip). *See* EX1013, Figs. 3b, 8; EX1014, 3:26-30, 3:48-49, FIG. 1A.

Moreover, a POSITA would have had a reasonable expectation of success in pursuing this implementation because integrated circuit structure is predictable. A POSITA also would have expected success because using TSVs for connection to power/ground was conventional. *See* EX1014, 3:1-2; EX1025, [0025].

4. Analysis of claims

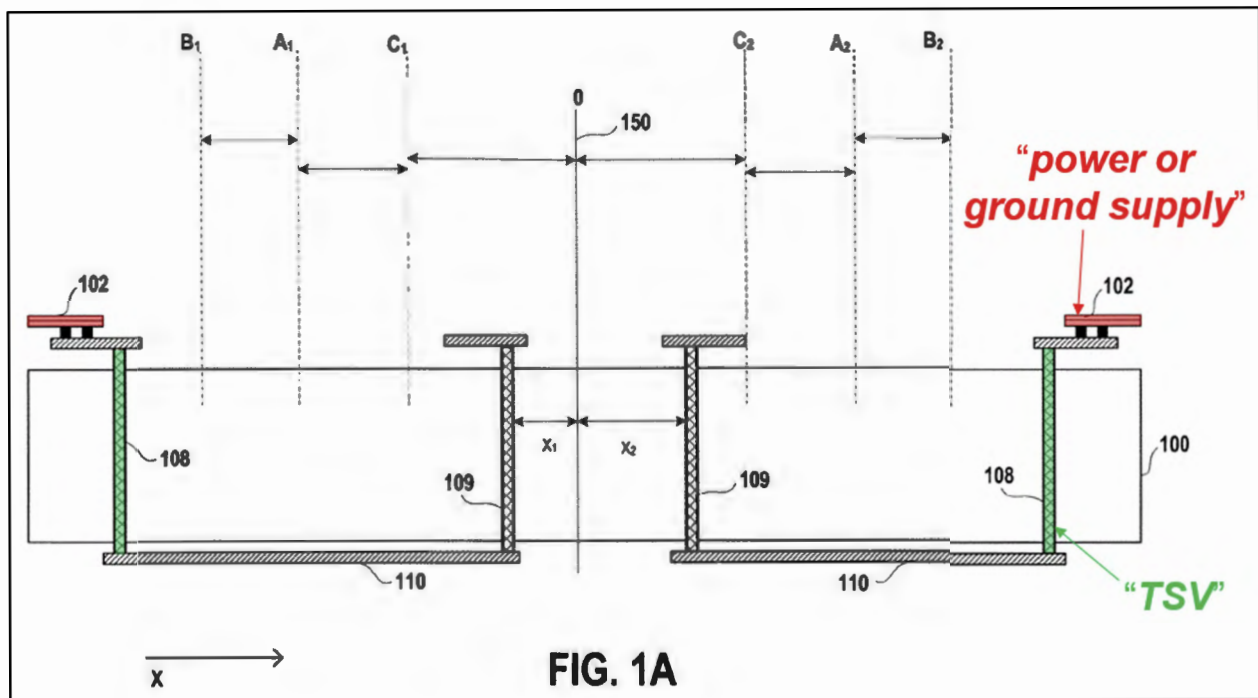
228. For the reasons below, claim 30 is obvious over the combination of Lee, Tsern, Lin, and White.

(a) ***Claim 30***

[30] The electronics system device of claim 28, wherein the at least one TSV is used for connecting to a power or a ground supply.

229. In the combination, at least one of the TSVs (*see* [28], *supra*) is implemented based on White's "through-silicon vias 108 ... formed within the periphery region of the IC chip" to "route power and ground from the bonding pads 102, to the non-periphery region of the integrated circuit chip." EX1014, 3:48-50; *see* 2:57-58 ("distributing power to the interior of an integrated circuit (IC) chips using through-silicon-vias (TSVs)"). The bonding pads (red in FIG. 1A, *infra*) "provide power and ground" and thus correspond to ***a power or ground supply***. EX1014, 3:17-19; *see* Abstract ("Power is distributed from the conducting pads to the TSVs ... thus supplying power and ground to circuits located within the non-peripheral region of the integrated circuit chip"), 1:46-48 ("The integrated circuit has conducting pads for providing power and ground located within the peripheral region of the top surface"), 3:64-66 ("Power and ground are provided to the integrated circuit from bonding pads"). The peripheral TSVs (green) are connected to the bonding pads, *i.e.*, ***used for connecting to the power/ground supply***, as shown in FIG. 1A. *See id.*, 1:53-56 ("Power is distributed from the

conducting pads to the TSVs within the non-peripheral region through the TSVs within the peripheral region, thus supplying power and ground to circuits”), 1:38-40 (“a method and apparatus for distributing power to the interior portion of an integrated circuit using through-silicon-vias (TSVs)”), 3:47-50 (“a number of TSVs 108 and 109 may be used to route power and ground from the bonding pads 102, to the non-periphery region of the integrated circuit chip 100”), 4:17-21 (“Using a plurality of TSVs to distribute power to the non-periphery region of the integrated circuit reduces the effect of resistive voltage drops on a conducting line and the observed voltage at the non-periphery region of the integrated circuit is roughly the same as the power supply voltage”), 4:37-46 (“Logic elements 104 located within the non-periphery region can then receive power and ground from the TSVs”), 2:57-58, 3:7-8, 4:24-26, 4:58-63, 5:38-45, 5:65-67, 6:24-26, 6:49-64, claim 1, claim 9.



Excerpt from White, FIG. 1A (annotated)

I. [Ground II]: Lee, Tsern, and Matsubara Render Obvious Claims 1, 5, 9, and 10

1. Matsubara (EX1006)

230. Matsubara, in the context of embedded DRAM semiconductor devices, describes the structure of both memory (*e.g.*, DRAM) transistors and logic transistors. Specifically, Matsubara describes a semiconductor device having a “DRAM memory element” and a “logic Nch region.” EX1006, 3:65-4:2. In this device, “[a] minimum gate length of the transistor provided to the logic Nch region 102 is smaller than a minimum gate length of the transistor provided to the DRAM region.” EX1006, 4:2-7. Matsubara notes that the “relatively small gate length” of the logic transistors is “in view of improving the operation speed.” *Id.*, 6:21-23.

By contrast, “the gate length is not a key factor of governing the operation speed of DRAM,” and instead, “[t]he DRAM region 104 is controlled under an allowable level of junction leakage more strictly than in the logic Nch region.” *Id.*, 6:32-39. To achieve this desired stability, given the lesser importance of speed for DRAM cells, “[t]he minimum gate length of the transistors provided to the DRAM region 104 is set larger than the minimum gate length of the transistors provided to the logic Nch region.” *Id.*, 6:34-37.

231. Matsubara is reasonably pertinent to the problem the '942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25; EX1006, Abstract. For instance, Matsubara relates to structure of DRAM integrated circuits, which is relevant to development of memory chip modules that can include arrays of memory device ICs. *See* EX1006, Abstract; EX1001, 1:17-25.

2. The Lee-Tsern-Matsubara Combination

232. The Lee-Tsern-Matsubara combination system is based on the structure of Lee's memory system 50. Specifically, as taught by Lee, integrated circuit “memory devices 70,” *e.g.*, DRAM devices, are divided into four groups or ‘ranks’ coupled to the memory hub 60 [blue] through a respective bus system.”

EX1004, [0016]. The memory hub is also coupled to a memory controller through a “high-speed link 58.” *Id.* Based on Tsern, the combination memory hub is implemented as an integrated circuit, as I discussed above. EX1005, Abstract, 30, Fig. 11.

233. Integrated circuits, such as the memory hub and the memory devices of the combination system, are composed of transistors (among other elements). *See* EX1006, 4:2-4 (“The logic Nch region 102 and the DRAM region 104 are provided with a second transistor 112 and a first transistor 114, respectively). Indeed, this is the nature of integrated circuits, as explained by Kitsukawa: “Due to many technological advances, integrated circuits, or “chips,” incorporate many millions of transistors on a single monolithic device. This provides many advantages, including improved speed and reduced size.” EX1024, 1:15-20.

234. In the combination, based on the teachings of Matsubara the transistors of the memory hub are dimensioned differently from the transistors of the memory devices. Specifically, as taught by Matsubara, the “gate length of the transistors” of the memory devices “is set larger than the minimum gate length of the transistors provided to the logic [] region,” *i.e.*, the transistors of the integrated circuit memory hub. EX1006, 6:34-37.

235. Notably, it was conventional as of the Critical Date that for a given process generation, the gate length of memory (*e.g.*, DRAM) transistors was longer

than the gate length of logic transistors. This is because the performance requirements for the two types of devices are different.

236. Specifically, and as I discuss in the following paragraphs, the key design criterion for logic transistors is speed, and accordingly, a short gate length is preferable. For memory (*e.g.*, DRAM) transistors, speed is less critical; the key design criterion instead is stability, achievable by longer gate lengths.

237. For instance, Matsubara itself indicates that “[t]he DRAM region 104 is controlled under an allowable level of junction leakage more strictly than in the logic Nch region 102,” *i.e.*, because minimizing leakage is important for DRAM cells to ensure storage stability—a concern that is less applicable to logic elements. EX1006, 6:37-39.

238. Kitsukawa provides more detail about these different design criteria for logic and memory transistors, explaining that the “internal voltage level” of the DRAM “must be relatively low to work with the small memory cell circuits of the DRAM’s array ... as well as to reduce the overall power consumption of the DRAM. Output circuits 5, however, work off the higher VDD voltage. In this way, the speed of the output circuits 5 is enhanced.” EX1024, 1:45-52; *see* 1:26-32 (describing that “reducing the external power supply ... [is] typically at the cost of reduced chip speed”), 2:3-20 (describing that a “DRAM memory cell requires a very small internal voltage that balances dielectric leakage characteristics and

memory cell stability, while circuits in an area peripheral to the memory cell area require another internal voltage that balances speed and power consumption”).

239. These different design criteria (*i.e.*, speed as a priority for logic cells; stability and low power consumption for memory cells) are achieved by designing logic transistors and memory transistors to have different gate length. A transistor with a longer gate length operates at lower power and is more stable than a transistor with a shorter gate length, but because of its longer gate length, it operates at slower speed than a transistor with a shorter gate length. Matsubara explains this, stating that “[t]he logic region containing the logic Nch region 102 has a relatively small gate length in view of improving the operation speed,” while “[o]n the other hand, the gate length is not a key factor of governing the operation speed of DRAM provided to the DRAM region 104,” so “[t]he minimum gate length of the transistors provided to the DRAM region 104 is set larger than the minimum gate length of the transistors provided to the logic Nch region 102.” EX1006, 6:32-37. Similarly, Liaw confirms that “[l]ogic devices usually use smaller gate length for improved drive current as well as lower gate capacitance.” EX1026, 4:6-8. The reason that longer gate length transistors have less leakage is explained by Young: “the longer the gate length (channel length) of the transistor, the less leakage current (*i.e.*, off state current) occurs across the transistor from source to drain.” EX1027, 3:28-34.

240. Thus, designing logic and memory cells for different performance criteria was conventional, and is achieved by a difference in dimensions between the two types of devices that allows for satisfaction of these differing performance criteria between the two types of devices: speed, for the memory hub; and stability and low leakage, for the memory devices.

3. Motivation to Combine

241. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement the memory device transistors to have a longer gate length than the memory hub transistors.

242. First, a POSITA would have been motivated to implement these dimensions to facilitate conformity with differing performance criteria between logic transistors and memory transistors. Specifically, and as I discussed above, speed is a key design parameter in logic transistors, and is achieved by a short gate length. . In memory transistors, speed is less crucial, but stability and low leakage current are key design objectives, which are achieved by longer gate lengths. *See* EX1006, 6:32-39; EX1024, 1:15-52, 2:3-20; EX1026, 4:6-8; EX1027, 3:28-34.

243. Second, an integrated circuit system in which memory transistors have a longer gate length than the gate length of the logic transistors was conventional, and a POSITA would have been motivated to pursue this implementation for

consistency with conventional integrated circuit design rules and protocols. *See* EX1006, 6:32-39; EX1026, 4:6-8; EX1027, 3:28-34.

244. Third, implementing memory transistors with a longer gate length than logic transistors is merely the application of known techniques (*e.g.*, different gate lengths in integrated circuits of different types (*e.g.*, memory vs. logic) to achieve different performance objectives) to a known structure (*e.g.*, the memory device and memory hub ICs of the combination) to yield predictable results (*e.g.*, a memory system in which the memory device transistors have a longer gate length than the memory hub transistors).

245. A POSITA would have had a reasonable expectation of success in pursuing this implementation because memory system technology and integrated circuit fabrication technology are predictable. Moreover, a POSITA would have expected success because integrated circuit designs in which memory cells have transistors with longer gate length than logic cells was conventional. *See* EX1006, 6:32-39; EX1026, 4:6-8; EX1027, 3:28-34.

4. Analysis of claims

246. For the reasons below, claims 1, 5, and 9-10 are obvious over the combination of Lee, Tsern, and Matsubara.

(a) Claim 1

[Ipre] A reconfigurable high speed memory chip module, comprising

247. I previously discussed for element [19pre] of Ground 1A that the system based on the Lee-Tsern-Matsubara combination includes a ***high speed memory chip module***.

248. The memory chip module of the combination is ***reconfigurable***, consistent with Lee's teachings that the memory hub can be "configure[d] ... depending upon whether a high memory bandwidth or a high memory depth is desired." EX1004, [0017]. A reconfigurable memory system has advantages: "By allowing the memory hub 60 to configure the data format of the memory module 54, the data format can be optimized for a particular application being executed in a computer system or other electronic system containing the memory system 50. For example, when executing a graphics intensive application like a video game, the memory system 50 can be configured in the high bandwidth mode. When a computer system is executing a database application, for example, the memory system 50 can be configured in the high memory depth mode. The data format is therefore not fixed as in conventional memory systems." *Id.*, [0020]).

[1a.1] a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array integrated circuits (ICs), each of the memory cell array ICs has an input/output (I/O) data bus and

249. This limitation is rendered obvious by the combination of Lee, Tsern, and Matsubara for reasons similar to those I discussed above for element [19b] of Ground 1A.

[1a.2] at least one memory cell array corresponding to a first metal-oxide-semiconductor field-effect transistor (MOSFET) process, wherein the first MOSFET process corresponding to a first MOSFET gate length; and

250. MOSFET refers to “metal-oxide-semiconductor field-effect transistor” and is a description of a common type of transistor fabricated on a silicon wafer in a CMOS (complementary metal-oxide-semiconductor) fabrication process, which is a conventional process for integrated circuit fabrication (*e.g.*, for fabrication of both memory and logic integrated circuits). For instance, the Pierret textbook explains that “[a] key component of present-day microelectronics [is] the metal-oxide-semiconductor field effect transistor (MOSFET). EX1030, 526; *see* EX1024, 1:15-32. I understand a “MOSFET process” to refer to the process of making field-effect transistors for implementation of the memory cell array ICs of the memory cell array.

251. In the combination, the memory devices of the memory cell array are “dynamic random access memory devices (‘DRAMs’) or some other type of memory devices.” EX1004, [0016]. DRAMs, as well as other types of memory devices, are semiconductor integrated circuits that include transistors, which means

that DRAMs (and other integrated circuit memory devices) are produced by a MOSFET process. *See* EX1030, 526 (“The DRAM cell ... is an integrated combination of a charge storage element ... and a MOSFET utilized as a switch”); EX1005, 12 (Tsern refers to “[i]ntegrated circuit memory devices” such as DRAM, SRAM, and flash memory”); EX1016, 4:56-60 (“memory die such as NAND flash memory die ... [or] other types of semiconductor die ... such as for example NOR, DRAM and various other memory die”).

252. That is, the memory devices (*at least one memory cell array*) of the combination are integrated circuits that include transistors and thus are MOSFET devices, *i.e.*, they *correspond to a first MOSFET process*.

253. As I noted above, MOSFET devices include transistors. *See* EX1024, 1:15-32. The gate length of a transistor is distance between the source and the drain in the transistor, and is defined by the configuration and dimensions of the features formed during the MOSFET fabrication process. *See* EX1030, 527. Accordingly, a given MOSFET process corresponds to a MOSFET gate length of the transistors formed during that MOSFET fabrication process. *Id.* For instance, the transistors of the memory device integrated circuits in the combination system have a *gate length*. Thus, I consider that the *first MOSFET process* (*i.e.*, the process used to fabricate the memory device integrated circuits of the combination)

corresponds to a first MOSFET gate length (i.e., the gate length of the transistors of those memory device integrated circuits).

[1b.1] a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an I/O data bus of each of the memory cell array ICs,

254. This limitation is rendered obvious by the combination of Lee, Tsern, and Matsubara for reasons similar to those I discussed above for claim [19c] of Ground 1A.

[1b.2] wherein the logic unit corresponds to a second MOSFET process, the second MOSFET process corresponds to a second MOSFET gate length, and the first MOSFET gate length is longer than the second MOSFET gate length;

255. In the combination, the memory hub (**logic unit**) is implemented as an integrated circuit, consistent with Tsern's teachings of a similarly functioning integrated circuit buffer unit. See EX1005, Abstract ("an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices"), Fig. 12. As I discussed above for element [1a.2], integrated circuits (e.g., the combination memory hub) are semiconductor devices that are produced by a MOSFET process. See EX1030, 526; EX1024, 1:15-32. That is, the integrated circuit memory hub (**logic unit**) of

the combination includes transistors and thus is fabricated in a MOSFET process, *i.e.*, the logic unit *corresponds to a second MOSFET process*.

256. To the extent PO argues that the *first MOSFET process* and the *second MOSFET process* refer to different MOSFET processes, a POSITA would have understood this to be the case. For instance, the circuit layout, dimensions, and/or materials differ between logic devices (*e.g.*, the memory hub) and memory devices (*e.g.*, the DRAM memory devices), and thus, different processes are used to fabricate the two types of devices. *See* EX1006, 2:51-54 (addressing differences in materials between memory and logic cells), 6:32-39 (addressing differences in gate length between memory and logic cells); EX1026, 4:6-8; EX1027, 3:28-34. Moreover, in the combination, the memory hub and the memory devices are each distinct integrated chips, *e.g.*, multiple chips capable of being arranged in a stacked arrangement such as illustrated in Tsern's Figs. 11 and 12. Distinct fabrication processes are used to fabricate distinct integrated circuit chips, *i.e.*, the memory hub is fabricated in a MOSFET process that differs from the MOSFET process used to fabricate the memory chips.

257. As I discussed above for element [1a.1], a given MOSFET process corresponds to a MOSFET gate length of the transistors formed during that MOSFET fabrication process. *Id.* For instance, the transistors of the memory hub integrated circuit in the combination system have a *gate length*. Thus, I consider

that the *second MOSFET process* (*i.e.*, the process used to fabricate the integrated circuit memory hub) *corresponds to a second MOSFET gate length* (*i.e.*, the gate length of the transistors of the memory hub).

258. In the combination, the gate length of the transistors in the memory devices (*first gate length*) is *longer than* the gate length of the transistors in the memory hub (*second gate length*), based on the teachings of Matsubara, and as was conventional in the art as of the Critical Date. Specifically, based on Matsubara “[t]he minimum gate length of the transistors” in the memory devices “is set larger than the minimum gate length of the transistors” in the memory hub. EX1006, 6:34-37; *see* Abstract (“A minimum gate length of the second transistors provided in the logic region is smaller than a minimum gate length of the first transistors provided in the DRAM region”), 4:4-7 (“A minimum gate length of the transistor provided to the logic Nch region 102 is smaller than a minimum gate length of the transistor provided to the DRAM region 104”), 2:3-9, 3:14-23, 2:44-50, 4:37-42, 6:21-39, 6:59-65, 8:51-54, claim 1.

259. As I discussed above, it was conventional to design memory cells with longer gate length than logic cells, to achieve stability and lower power operation for memory cells while allowing for higher power and higher speed operation for logic cells. *See* EX1006, 6:21-39; EX1024, 1:15-52, 2:3-20; EX1026, 4:6-8; EX1027, 3:28-34.

[1c] wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus.

260. This limitation is rendered obvious by the combination of Lee, Tsern, and Matsubara for reasons similar to those I discussed above for element [19d] of Grounds 1A and 1B.

(b) **Claim 5**

[5a] The high speed memory chip module of claim 1, wherein the logic unit further comprises: a parallel-to-serial controller module for converting the first set of parallel data into the second set of parallel data, and

261. This limitation is rendered obvious by the combination of Lee, Tsern, and Matsubara for reasons similar to those I discussed above for element [20c] of Ground 1B.

[5b] the logic unit transmits the second set of parallel data to an application-specific integrated circuit (ASIC) or a system on chip (SOC) processor through the second transmission bus,

262. This limitation is rendered obvious by the combination of Lee, Tsern, and Matsubara for reasons similar to those I discussed above for elements [19a] and [19e] of Ground 1A, *supra*. In the combination, the memory hub (**logic unit**) is coupled to the controller (**ASIC**) via the high-speed link (**second transmission bus**), *i.e.*, for transmission of the second set of parallel data to the ASIC. *See*

EX1004, [0015] (“the high-speed link 58 will have a capacity for coupling data having a predetermined bus width between the controller 52 and each memory module 54”), Fig. 2, Fig. 5.

[5c] wherein bit width of the first set and the second set of parallel data are different.

263. This limitation is rendered obvious by the combination of Lee, Tsern, and Matsubara for reasons similar to those I discussed above for element [19f] of Ground 1A.

(c) **Claim 9**

[9] The high speed memory chip module of claim 5, wherein a transmitting data rate of the first transmission bus and a receiving data rate of the first transmission bus are different.

264. This limitation is rendered obvious by the combination of Lee, Tsern, and Matsubara for reasons similar to those I discussed above for claim [25] of Ground 1B.

(d) **Claim 10**

[10] The high speed memory chip module of claim 5, wherein a transmitting data rate of the second transmission bus and a receiving data rate of the second transmission bus are different.

265. This limitation is rendered obvious by the combination of Lee, Tsern, and Matsubara for reasons similar to those I discussed above for claim [26] of Ground 1B.

J. [Ground 1J]: Lee, Tsern, Matsubara, and Dozen Render Obvious Claim 2

1. Analysis

(a) Claim 2

[2a] The high speed memory chip module of claim 1, wherein the multiple memory cell array ICs of the type of memory cell array group comprise a flash IC or a Dynamic Random Access Memory (DRAM) IC,

266. In the combination system based on Lee, Tsern, Matsubara, and Dozen, the memory devices (corresponding to the claimed *memory cell array ICs*) are “dynamic random access memory devices (‘DRAMs’),” as taught by Lee. EX1004, [0016]; *see* claims 11-12.

[2b] wherein a dicing method for at least one memory cell array IC comprises a Laser cutting process.

267. This limitation is rendered obvious for reasons similar to those I discussed above for element [20c] of Ground 1D.

K. [Ground 1K]: Lee, Tsern, Matsubara, and Khan Render Obvious Claim 3

268. For the reasons below, claim 3 is obvious over the combination of Lee, Tsern, Matsubara, and Khan.

1. Analysis of claims

(a) Claim 3

[3a] The high speed memory chip module of claim 1, further comprising: an interposer, wherein at least one memory cell array IC of the memory cell array group and the logic unit are disposed over two opposite sides of the interposer, respectively,

[3b] wherein the interposer comprises silicon or oxide glass material.

269. This claim is rendered obvious by the combination of Lee, Tsern, Matsubara, and Khan for reasons similar to those I discussed above for claim 20 of Ground 1D.

L. [Ground 1L]: Lee, Tsern, Matsubara, Khan, and Dozen Render Obvious Claim 4

1. Analysis of claims

270. For the reasons below, claim 4 is obvious over the combination of Lee, Tsern, Matsubara, Khan, and Dozen.

(a) Claim 4

[4a] The high speed memory chip module of claim 1, further comprising: an interposer, wherein the multiple memory cell array ICs are disposed over the interposer respectively, and the interposer is disposed over the logic unit,

[4b] wherein the interposer comprises silicon or oxide glass material,

271. Limitations [4a] and [4b] are rendered obvious by the combination of Lee, Tsern, Matsubara, Khan, and Dozen for reasons similar to those I discussed above for [21a] and [21b] of Ground 1C.

[4c] wherein a dicing method for at least one memory cell array IC comprises a Laser cutting process.

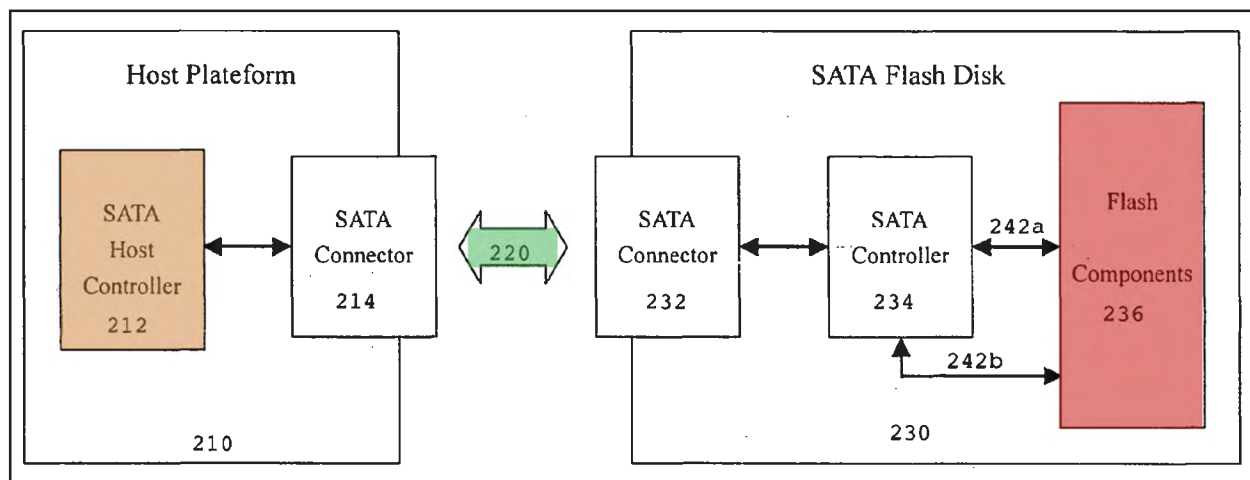
272. Limitation [4c] is rendered obvious by the combination of Lee, Tsern, Matsubara, Khan, and Dozen for reasons similar to those I discussed above for [20c] of Ground 1D.

M. [Ground 1M]: Lee, Tsern, Matsubara, and Weng Render Obvious Claim 6

1. Weng

273. Weng describes “semiconductor memory devices ... which are connected to a host platform using the SATA (Serial Advanced Technology Attachment) PC Bus.” EX1017, [0001]. As illustrated in Fig. 2, below, “a flash memory system” includes “a host platform 210 which is a non-volatile storage operation to the SATA flash memory disk 230.” *Id.*, [0052]. The host platform 210 “is connected to the SATA flash memory disk 230 by means of an SATA cable 220,” green. *Id.*, [0053]. On the host platform, a “SATA main controller 212,” orange, “is used to control and manage all SATA transferring on the SATA bus.” *Id.* For instance, responsive to a request from the SATA main controller, a

“SATA flash device controller 234 [blue] performs various operations such as ‘read’, ‘write’ and ‘erase’ to the flash memory component 236 [red].” *Id.*, [0056].



Excerpt from Weng, Fig. 2 (annotated)

274. Weng is from the same field of endeavor (*e.g.*, memory systems) as the '942 Patent. *See* EX1001, 1:17-25; EX1017, Abstract.

275. Also, Weng is reasonably pertinent to the problem the '942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25; EX1017, Abstract. For instance, Weng’s SATA communication protocol, in the context of a memory system, enables low voltage operation with “power consumption suitable for mobile use,” which is relevant to development of a low power memory system. EX1017, [0020]-[0026]; *see* EX1001, 1:17-25.

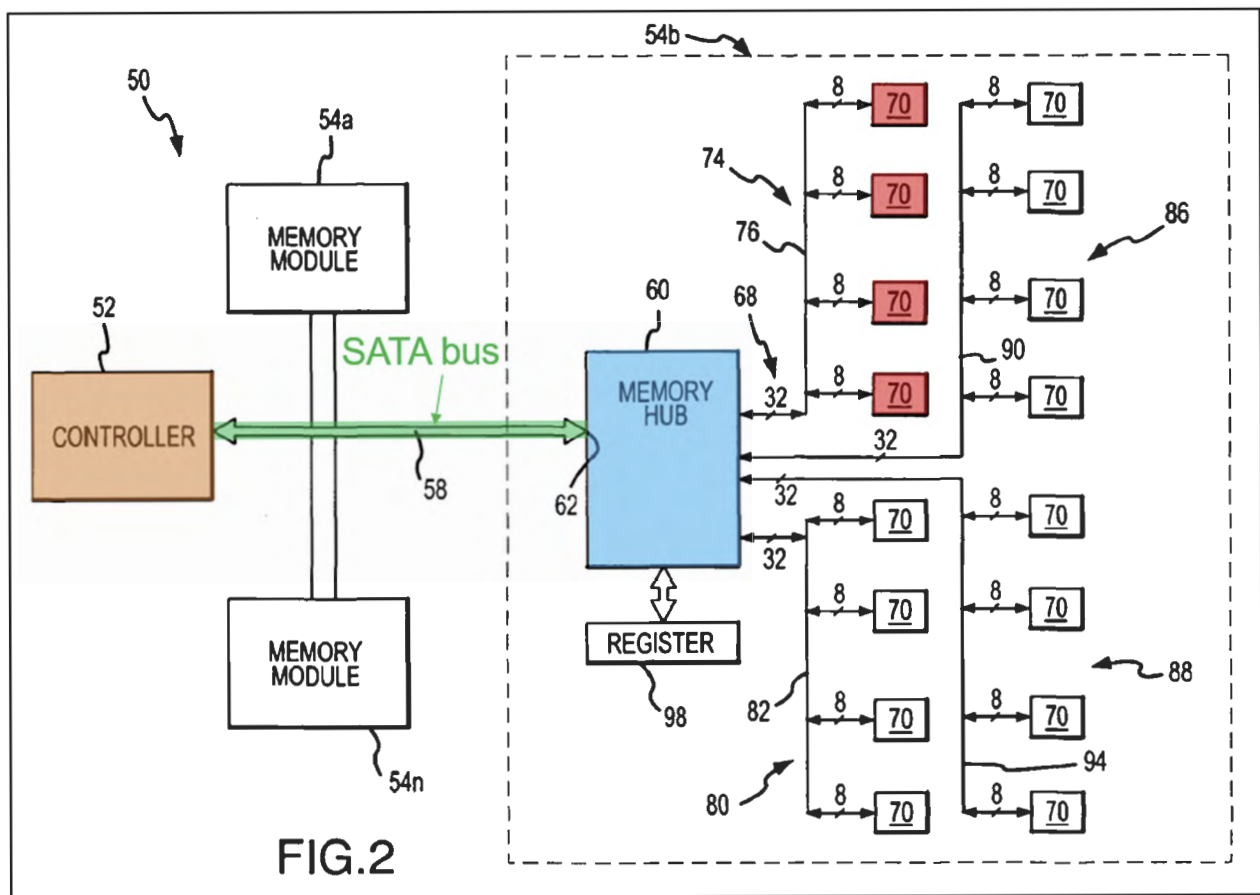
2. The Lee-Tsern-Matsubara-Weng Combination

276. The Lee-Tsern-Matsubara-Weng combination is structured based on the structure of Lee's FIG. 2 system, with a memory hub connected to a memory controller and to ranks of memory devices. *See* EX1004, Abstract. Lee indicates that the memory devices of its system are not limited to DRAM devices: "The memory devices 70 may be, for example, dynamic random access memory devices ('DRAMs') or some other type of memory devices." *Id.*, [0016]. In the Lee-Tsern-Matsubara-Weng combination, for instance, the memory devices can be flash memory. I note that this is also consistent with Tsern, which, in the context of a memory system structured similarly to that of Lee, indicates that the memory devices can be DRAM, SRAM, or flash memory. EX1005, 12.

277. Notably, the structure of Weng's system is generally consistent with that of Lee's system, in that a host platform including an ASIC host controller 212 (*e.g.*, akin to Lee's memory controller) is connected to memory devices via a controller 234 in the flash module (*e.g.*, akin to Lee's memory hub 60 in the memory module 54). *See* EX1004, FIG. 2; EX1017, [0037], Fig. 2. Based on this similarity in architecture, the communication protocols in the combination system are implemented based on Weng.

278. Specifically, in the Lee-Tsern-Matsubara-Weng combination, the high-speed bus 58 connecting the controller to the memory modules is

implemented as a SATA cable based on Weng's teachings of a host platform
 "connected to [a] SATA flash memory disk 230 by means of an SATA cable."
 EX1017, [0052]. Consistent with the operation of Weng's system, in the
 combination system, when the memory hub receives a request received from the
 controller via the SATA bus, the memory hub "performs various operations such
 as 'read', 'write' and 'erase'" to the memory devices 70. EX1017, [0056].



Lee-Tsern-Matsubara-Weng composite figure based on Lee, FIG. 2

3. Motivation to Combine and Expectation of Success

279. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement the high-speed link as a SATA connection based on Weng.

280. First, as described by Weng, SATA connections have a number of advantages, including (among others), “[f]avorable (low) voltage,” “[s]upports lower cost device architectures,” “includes efficient power delivery,” “[t]ransfer rate exceeding best ATA(~150 MB/s)with higher scalability,” “[p]rotocol is simple,” and “[e]asy installation/configuration.” EX1017, [0016]-[0035]. A POSITA would have been motivated to use a SATA cable to access these performance and design advantages.

281. Second, a SATA cable connecting a memory controller to memory devices was commonplace, and a POSITA would have been motivated to employ conventional protocols in the combination system for alignment with standard approaches to implementing memory systems. For instance, Lee-051 describes a SATA interface connection between an interface controller and flash memory units. *See* EX1028, 2:55-62.

282. Third, implementing the high-speed bus of the combination as a SATA cable is merely the application of known techniques (*e.g.*, a SATA cable connecting a memory controller to memory devices) to a known structure (*e.g.*, the

combination memory system including memory modules connected by a transmission bus to a memory controller), and it yields predictable results (*e.g.*, a memory system in which the memory controller is connected to the memory modules by a SATA bus).

283. A POSITA would have had a reasonable expectation of success in pursuing this implementation because memory system technology is predictable, and because SATA protocol connections were conventional and predictable. *See* EX1028, 2:55-62. Moreover, a POSITA would have expected success because of the generally similar architecture between Lee's memory system and Weng's memory system. Specifically, Lee's system has a controller connected to a memory hub that controls access to memory devices, while Weng's system similarly has a controller connected to a SATA controller that controls access to memory devices. *See*, EX1004, FIG. 2; EX1017, Fig. 2. Finally, a POSITA would have expected success because Lee's system is compatible with various types of memory devices (*see* EX1004, [0016]), such as the flash memory devices of Weng's SATA-based system.

4. Analysis of claims

284. For the reasons below, claim 6 is obvious over the combination of Lee, Tsern, Matsubara, and Weng.

(a) **Claim 6**

[6] The high speed memory chip module of claim 5, wherein the second transmission bus is a bus comprising the protocol of Universal Serial Bus (USB), a Serial Advanced Technology Attachment (SATA) bus, a Universal Flash Storage (UFS) bus, a mobile industry processor interface (MIPI) bus, or a Peripheral Component Interconnect Express (PCIE) bus.

285. In the combination, as shown below the high-speed link 58 (corresponding to the claimed ***second transmission bus***) is implemented as a “SATA cable” based on Weng. EX1017, [0050]; *see* FIG. 2. Thus, the high-speed link 58 satisfies the claimed requirement that ***the second transmission bus is a bus comprising the protocol of ... a SATA bus***. *See also* the following cites in Weng demonstrating that the connection between the host controller and the controller in the memory module (*e.g.*, the high-speed link, in the combination) implements SATA protocol: [0001] (“The present invention is related to semiconductor memory devices, and in particular to erasable and programmable nonvolatile memory modules which are connected to a host platform using the SATA (Serial Advanced Technology Attachment) PC Bus”), [0037] (“a flash memory device, containing one or more flash modules, in which the flash memory is mapped to the address space of an ASIC or a controller which has an SATA-defined electrical interface and an SATA-defined logical interface. This controller/ASIC (hereinafter termed a ‘controller’) supports the SATA functionality according to the SATA

standard, thereby supporting enumeration onto the SATA bus, as well as data reception and transmission over SATA pipes to and from SATA endpoints), [0050] (“the SATA flash memory disk 230 comprises an SATA logical interface 112 and flash memory logical interface 120, and SATA flash device connector 232 receives electrical signals from SATA cable 220. The SATA cable carries the electrical signals from main controller”), [0053] (“the host platform 210 is connected to the SATA flash memory disk 230 by means of an SATA cable 220, the host platform 210 is connected to the SATA cable 220 by means of an SATA main connector 214. When the SATA flash memory disk 230 is connected to the SATA cable 220 by means of an SATA flash device connector 232, one characteristic of host platform 210 is an SATA main controller 212 which is used to control and manage all SATA transferring on the SATA bus”), [0048].

287. Claim 7 is rendered obvious by the combination of Lee, Tsern, Matsubara, and Leung for reasons similar to those I discussed above for [23] of Ground 1E.

(b) **Claim 8**

[8] The high speed memory chip module of claim 5, wherein a signal swing of data transmitted through the second transmission bus and a signal swing of data received through the second transmission bus are different.

288. Claim 8 is rendered obvious by the combination of Lee, Tsern, Matsubara, and Leung for reasons similar to those I discussed above for [24] of Ground 1E.

O. [Ground 1O]: Lee, Tsern, Matsubara, and Lin Render Obvious Claims 11, 12, and 15

1. Analysis of claims

289. For the reasons below, claims 11, 12, and 15 are obvious over the combination of Lee, Tsern, Matsubara, and Lin.

(a) **Claim 11**

[11] The high speed memory chip module of claim 1, wherein each of the memory cell array ICs of the type of memory cell array group corresponds to a first seal ring and the logic unit corresponds to a second seal ring, a circuit of

each of the memory cell array ICs is surrounded by a first seal ring² and a circuit of the logic unit is surrounded by the second seal ring.

290. Claim 11 is rendered obvious by the combination of Lee, Tsern, Matsubara, and Lin for reasons similar to those I discussed above for [27] of Ground 1F.

(b) ***Claim 12***

[12] The high speed memory chip module of claim 11, wherein at least one through silicon via (TSV) exists outside a first seal ring of each of the memory cell array ICs.

291. Claim 12 is rendered obvious by the combination of Lee, Tsern, Matsubara, and Lin for reasons similar to those I discussed above for [28] of Ground 1F.

(c) ***Claim 15***

[15] The high speed memory chip module of claim 11, wherein at least one TSV exists outside the second seal ring of the logic unit.

292. Claim 15 is rendered obvious by the combination of Lee, Tsern, Matsubara, and Lin for reasons similar to those I discussed above for [31] of Ground 1F, *supra*.

² I interpret the phrase “a first seal ring” to refer to the previously recited “first seal ring,” *e.g.*, by analogy to similarly phrased claim 27.

P. [Ground 1P]: Lee, Tsern, Matsubara, Lin, and Ali Render Obvious Claim 13

1. Analysis of claims

293. For the reasons below, claim 13 is obvious over the combination of Lee, Tsern, Matsubara, Lin, and Ali.

(a) Claim 13

[13] The high speed memory chip module of claim 12, further comprising: a metal layer disposed over a topmost memory cell array³ of the type of memory cell array group, wherein the metal layer covers more than 50% area of the topmost memory cell array.

294. Claim 13 is rendered obvious by the combination of Lee, Tsern, Matsubara, Lin, and Ali for reasons similar to those I discussed above for [29] of Ground 1G.

Q. [Ground 1Q]: Lee, Tsern, Matsubara, Lin, and White Render Obvious Claims 14 and 18

1. Analysis of claims

295. For the reasons below, claims 14 and 18 are obvious over the combination of Lee, Tsern, Matsubara, Lin, and White

³ I interpret the phrase “a topmost memory cell array” as “a topmost memory cell array IC,” for proper antecedent basis and by analogy to similarly phrased claim 29.

(a) **Claim 14**

[14] The high speed memory chip module of claim 12, wherein the at least one TSV is used for connecting to a power or a ground supply.

296. Claim 14 is rendered obvious by the combination of Lee, Tsern, Matsubara, Lin, and White for reasons similar to those I discussed above for [30] of Ground 1H.

(b) **Claim 18**

[18] The high speed memory chip module of claim 15, wherein the at least one TSV is used for connecting to a power or a ground supply.

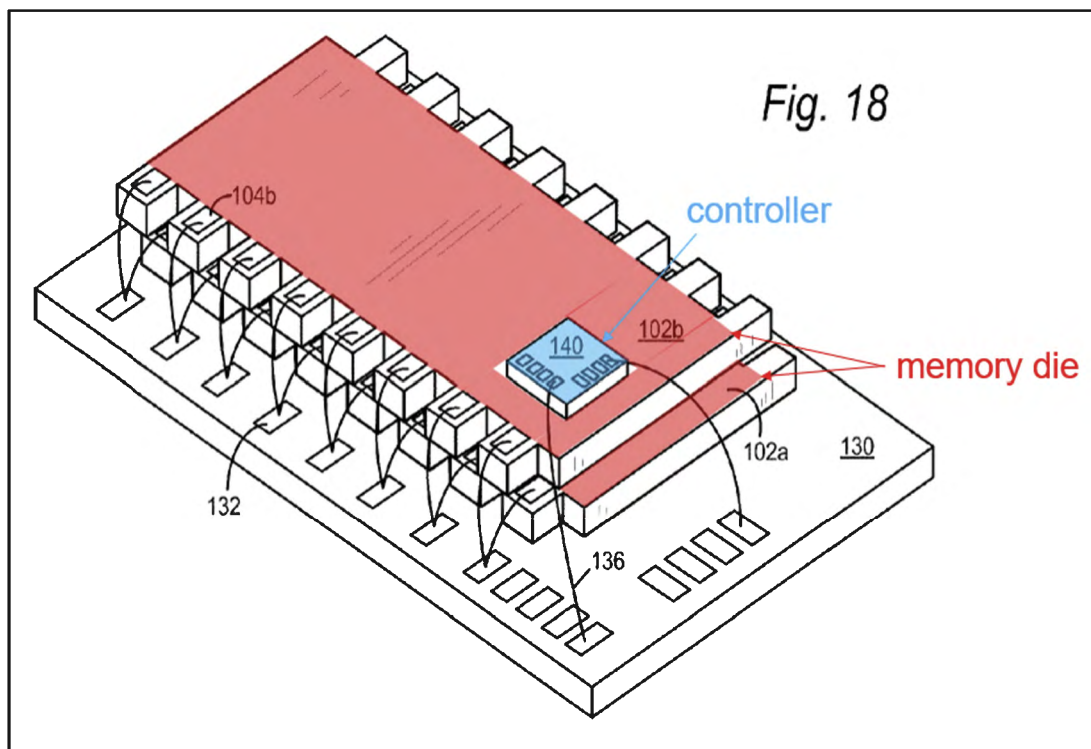
297. In the combination, the peripheral TSV of the logic unit is connected to bonding pads that provide power and ground, and thus the TSV is ***used for connecting to the power/ground supply***, for reasons similar to those I discussed above for [30] of Ground 1H.

R. [Ground 1R]: Lee, Tsern, Matsubara, Lin, and Liao Render Obvious Claim 16

1. Liao

298. Liao describes a “low profile semiconductor package” including one semiconductor die 102b “stacked on” another semiconductor die 102a (both of which are highlighted in red in Fig. 18, reproduced below) and mounted on a substrate 130. EX1016, 3:9-10, 5:33-34. The semiconductor die are, *e.g.*, “memory die such as NAND flash memory die ... [or] other types of

semiconductor die ... such as for example NOR, DRAM and various other memory die.” *Id.*, 4:56-60. The die are “cut with corrugations that define protrusions [] and recesses” that protrude from their sides to “allow additional die pairs to be affixed directly atop the die 102a and 102b.” *Id.*, 4:35-38, 6:8-11. “[O]nce all die 102 have been provided in the die stack, a controller die 140 [blue] may be affixed atop the stack.” *Id.*, 6:53-54.



Excerpt from Liao, Fig. 18 (annotated)

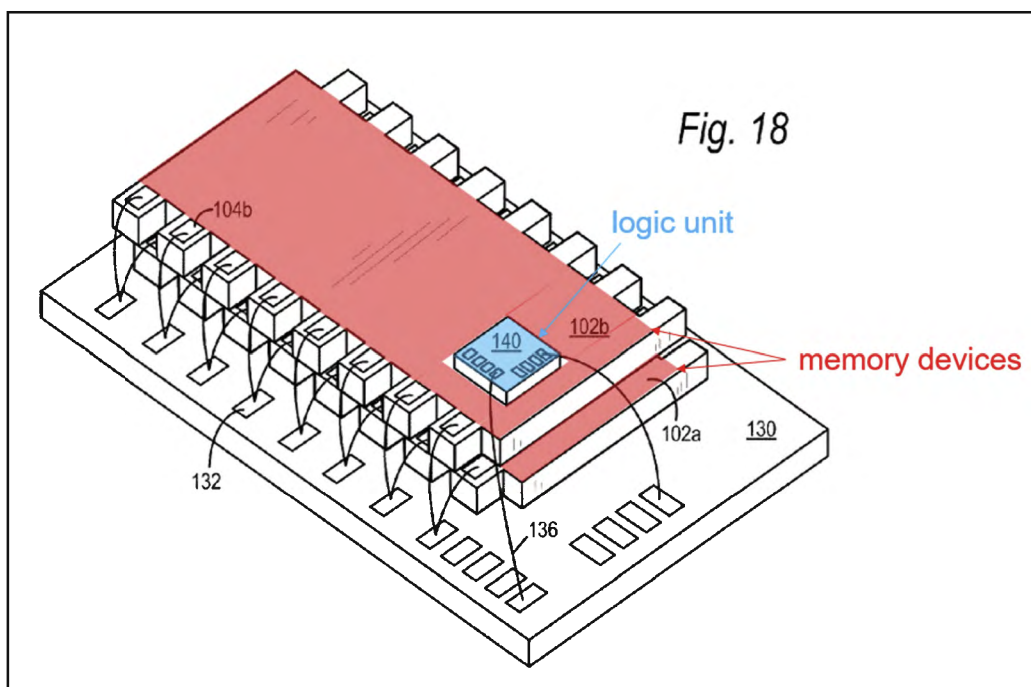
299. Liao is from the same field of endeavor (*e.g.*, memory systems) as the '942 Patent. *See* EX1001, 1:17-25; EX1016, 4:56-50.

300. Also, Liao is reasonably pertinent to the problem the '942 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with,

among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:17-25; EX1016, 4:56-50. For instance, Liao’s stacked chip arrangement “allows a large number of die in the stack while still fitting within a standard memory card form factor,” which is relevant to development of an efficient memory system. EX1016, 6:48-50; *see* EX1001, 1:17-25.

2. The Lee-Tsern-Matsubara-Lin-Liao Combination

301. In the Lee-Tsern-Matsubara-Lin-Liao combination, the memory hub IC 60 and at least one rank of memory devices 70 are assembled into a stacked package in an arrangement as taught by Liao. Specifically, and as illustrated in the composite figure below, the memory devices are stacked on top of one another and mounted on a substrate to form a “die stack,” and the memory hub IC is “affixed atop the stack” of memory devices. EX1016, 6:53-56; *see* Figs. 17-18.



Lee-Tsern-Matsubara-Lin-Liao composite figure based on Liao, Fig. 18

3. Motivation to Combine and Expectation of Success

302. It is my opinion that there are a number of reasons that would have motivated a POSITA to arrange the memory devices and memory hub based on Liao's die stack arrangement.

303. First, a POSITA in general would have been motivated to arrange the chips of the combination in a stack because 3D stacking of chips advantageously allows for "integrating more devices into a smaller volume," which in turn enables performance advantages, including "smaller footprint, shorter signal routing, reduced wiring density." EX1009, 1.

304. Second, a POSITA would have been motivated to implement a stacked arrangement in particular based on the specific stacked arrangement

described by Liao because this arrangement “allow[s] a large number of die in the stack while still fitting within a standard memory card form factor.” EX1016, 6:47-49.

305. Third, assembling chips into a stack is merely the application of known techniques (specifically, a semiconductor package having a die stack) to a known structure (*e.g.*, a memory system including DRAM chips and memory hub), and it yields predictable results (that is, a memory module having a stack of memory chips topped by a memory hub chip).

306. A POSITA would have expected success in packaging the chips of the combination based on Liao’s teachings because semiconductor packaging technology is predictable, and because a stacked package of memory chips and logic chips was conventional and well-understood. For instance, other examples of stacked chips in the context of memory modules are provided in Tsern (*see* EX1005, Fig. 11), Raghuram (*see* EX1023, FIG. 2), and Khan (*see* EX1009, Fig. 1(a)).

4. Analysis of claims

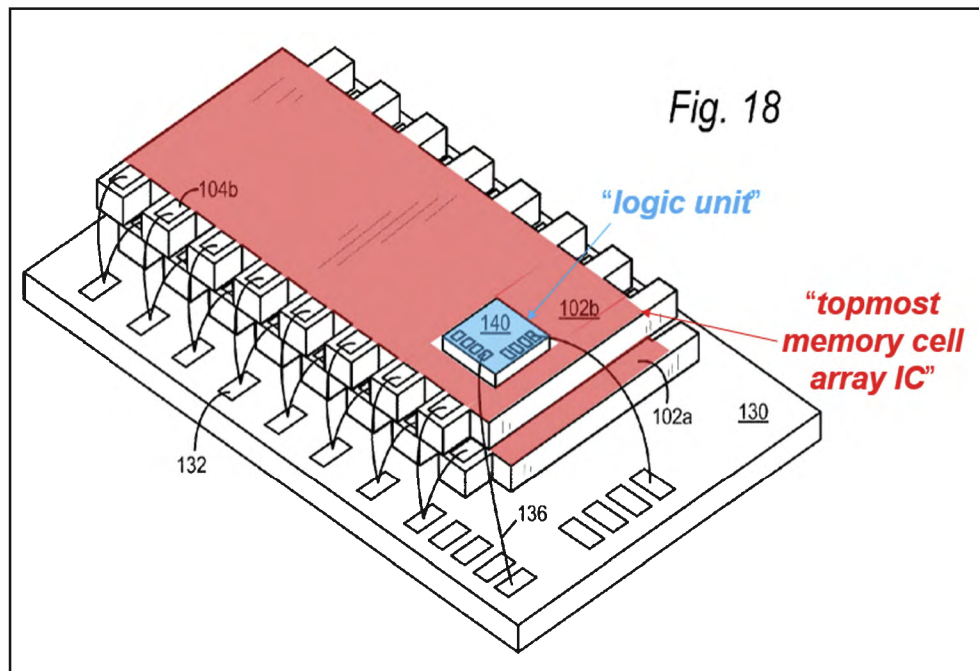
307. For the reasons below, claim 16 is obvious over the combination of Lee, Tsern, Matsubara, Lin, and Liao.

(a) Claim 16

[16] The high speed memory chip module of claim 15, wherein the logic unit is stacked over a topmost memory cell array IC of the type of memory cell array

group.

308. In the Lee-Tsern-Matsubara-Lin-Liao combination, the memory devices 70 (corresponding to the claimed *memory cell array ICs*) of at least one rank are stacked on top of one another to form a “die stack,” consistent with Liao’s teaching of stacked memory die. EX1016, 6:53-54; see Abstract, 4:56-60, 5:33-34, 6:4-15, 6:45-52. This is illustrated in Liao’s Fig. 18, annotated below. Based on Liao’s teaching of the positioning of the controller die, the memory hub 60 (corresponding to the claimed *logic unit*) is “affixed atop the stack,” thus satisfying the claimed requirement that *the logic unit is stacked over a topmost memory cell array IC*. EX1016, 6:53-56; see Figs. 17-18.



Excerpt from Liao, Fig. 18 (annotated)

**S. [Ground 1S]: Lee, Tsern, Matsubara, Lin, Liao, and White
Render Obvious Claim 17**

1. Analysis of claims

309. For the reasons below, claim 17 is obvious over the combination of Lee, Tsern, Matsubara, Lin, Liao, and White.

(a) Claim 17

[17] The high semiconductor speed memory chip module of claim 16, further comprising: a metal layer disposed over the logic unit, wherein the metal layer covers more than 50% area of the logic unit.

310. In the system based on the combination of Lee, Tsern, Matsubara, Lin, Liao, and White, the memory cell array ICs and logic unit IC are stacked based on Liao such that the logic unit is on top of the stack (as I discussed for claim 16 of Ground 1R). The chip stacks are packaged between a top cover and a bottom cover based on Ali, as I discussed above for element [29a] of Ground 1G. In this configuration, the top cover (which corresponds to the claimed *metal layer*, as I discussed above for [29a]) “cover[s]” the stack and thus is disposed over all of the ICs in the stack, including the memory cell array ICs and the logic unit IC. This arrangement thus satisfies the claimed requirement of *a metal layer disposed over the logic unit*.

311. Moreover, as I also discussed above for element [29a], the covers “have a size large enough to cover/encapsulate” the stack of chips, and thus they

are sized to cover the logic unit at the top of the stack. The metal top cover thus satisfies the claimed requirement of *a metal layer that covers more than 50% area of the logic unit*. EX1015, 3:8-9; *see* [29a] of Ground 1G.

VII. LEGAL PRINCIPLES

A. Obviousness

312. I have been informed that a patent claim is invalid as “obvious” under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a POSITA, taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others. For purposes of my analysis above and because I know of no indication from the patent owner or others to the contrary, I have applied a date of August 13, 2015, as the date of invention in my obviousness analyses, although in many cases the same analysis would hold true even at an earlier time than August 13, 2015.

313. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason to

modify the single prior art reference, or combine two or more references, in order to achieve the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or “common sense” of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

314. I have also been informed of the Supreme Court decision *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), which I am informed guides obviousness analyses. Under *KSR*, the mere application of a known technique to a piece of prior art ready for the improvement is obvious. In addition, the selection of one of a finite number of identified, predictable solutions to achieve a predictable result is obvious. Further, the simple substitution of one known element for another to obtain a predictable result is obvious.

APPENDIX A

DAVID KUAN-YU LIU, Ph.D.

2055 15TH St. N, #2007, VA 22201 • (510) 579-5029
davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 18 years of experience serving as expert consultant.
 - Named inventor on 99 US patents.
- Consultant and expert witness for past 18 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

EXPERT WITNESS WORK - CASE EXPERIENCE:

Case: **Advanced Memory Technologies, Inc. v. Micron Technology, Inc.**
Jurisdiction: Civil Action No. 1:25-cv-01036 (W.D. Tex.)
Work Product: Expert consulting work relating to Booster Circuit. Patent analysis and prior art review toward preparation of EPR petition support and draft of declaration.
Nature of Case: EPR.
Counsel: Retained by Fish & Richardson (Contact: Tim Riffe)
Date: 11/25 – Present

Case: **Apple v. WeCrevention, Inc.**
Jurisdiction: Post-Grant Patent Matters Adverse to WeCrevention, Inc.
Work Product: Expert consulting work relating to High Speed Chip Memory Module. Patent analysis and prior art review toward preparation of IPR petition support and draft of declaration.
Nature of Case: IPR.
Counsel: Retained by Fish & Richardson (Contact: Dr. Hyun Jin In)
Date: 11/25 – Present

Case: **Monterey Research LLC v. Renesas Electronics Corp.**
Jurisdiction: Civil Action No. 2:24-cv-00238-JRG (E.D. Tex.)
Work Product: Expert consulting work relating to Charge Trapping Nonvolatile Memory. Patent analysis and prior art review toward preparation of IPR petition support and draft of declaration.
Nature of Case: Civil action and IPR.
Counsel: Retained by Morrison Foerster (Contact: Yuka Teraguchi)
Date: 03/25 – Present

Case: **Palisade Techs., LLP v. Micron Tech., Inc.**
Jurisdiction: Civil Action N.D. Cal, No. 7:24-cv-00262 (W.D. Tex.)
Work Product: Expert consulting work relating to 3D NAND Flash Memory Technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 2 patents.
Nature of Case: Civil action and IPR.
Counsel: Retained by O'Melveny & Myers LLP (Contact: John Kappos)
Date: 12/24 – 01/26

Case: **Yangtze Memory Technologies Company, Ltd. vs. Micron Technology, Inc.**
Jurisdiction: Civil Action N.D. Cal, No. 3:223-cv-05792-RFL
Easter District of Texas
Work Product: Expert consulting work relating to 3D NAND Flash Memory Technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents. ***Deposed on 3 petitions that have been instituted.***
Nature of Case: Civil action and IPR.
Counsel: Retained by Orrick, Herrington & Sutcliffe (Contact: Jason Lang)
Date: 03/24 – Present

Case: **Force MOS Technology Co., Ltd. vs. Inergy Technology, Inc.**
Jurisdiction: Civil Action E.D. TX, No. 2:22-cv-00460-JRG
Easter District of Texas
Work Product: Expert consulting work relating to Vertical Trench DMOS process technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 2 patents. Declaration for claim construction on 3 patents. ***Deposed on Claim Construction Declaration, and deposed on declarations for IPR petitions, and deposed on reply declaration.*** Continuing work on claim construction and technical consulting.
Nature of Case: Civil action and IPR.
Counsel: Retained by Baker McKenzie (Contact: McKenzie Martin)
Date: 10/23 – 10/25

Case: **GlobalFoundries U.S. vs. International Business Machines**
Jurisdiction: 03348-KMK-AEK (S.D.N.Y. 2023)
Work Product: Expert consulting work relating to trade secrets involving advanced CMOS process and device technology (Nanosheet technology). Reviewed evidence and summarized findings.
Nature of Case: Civil action.
Counsel: Retained by Latham & Watkins (Contact: Sami Al-Marzoog)
Date: 10/23 – 2/25

Case: **Element Capital. vs. Beijing BOE Display Technology Co., Ltd.**
Jurisdiction: Civil Action No. 2:22-cv-00118-JRG
Eastern District of Texas
Work Product: Expert consulting work relating to OLED technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 3 patents.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Linhong Zhang)
Date: 4/23 – 12/23

Case: **Sonrai Memory Ltd. vs. Micron Technology, Inc.,**
Jurisdiction: Civil Action No. 6:22-cv-000855-FB
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration resulting in institution of
the petition and ***deposed on supplemental declaration.***
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Tim Riffe)
Date: 12/22 – 7/24

Case: **Daedalus Prime LLC vs. Samsung Electronics Co.,**
Jurisdiction: Civil Action E.D. TX, Marshall Div., No. 2:22-cv-353
Eastern District of Texas, Marshall Div., and
Investigation No. 337-TA-1336
Work Product: Expert consulting work relating to FINFET process technology.
Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration on 2 patents. Source code
database viewing (GDS layout and process flow documents) for
supporting of non-infringement position.
Nature of Case: Civil action and ITC Investigation on Certain Semiconductor Devices,
Mobile Devices Containing the Same and Components Thereof..
Counsel: Retained by Fish & Richardson (Contact: Kevin Su)
Date: 10/22 – 4/23

Case: **Netlist, Inc. vs. Samsung Electronics Co. Ltd. et al.,**
Jurisdiction: Civil Action No. 2:21-cv-00463
Eastern District of Texas
Work Product: Expert consulting work relating to memory modules.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Tony Nguyen)
Date: 8/22 – 12/22

Case: **Vervain, LLC vs. Micron Technology & related IPR Petition**
Jurisdiction: Action No. 6:21-cv-00487-ADA
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration on 4 patents, all 4 petitions
instituted, and ***deposed on both initial declaration and reply
declaration on all 4 patents.***
Counsel: Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared
Bobrow)
Date: 8/21 – 2/23

Case: **Monterey Research vs. Qualcomm PTAB Matter**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Jones Day (Contact: David Cochran)
Date: 12/21 – 2/22

Case: **Semiconductor Energy Laboratory Co., OLED Patent Matters**
Jurisdiction: Action No. 8:21-cv-00554-JAK-ADS
Central District of California
Work Product: Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Bryan Basso)
Date: 9/21 – 4/22

Case: **Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Erise IP (Contact: Paul Hart)
Date: 8/21 – 9/21

Case: **Texas Instruments IPR Petition**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Josh Griswold)
Date: 9/20 – 4/21

Case: **Micron Technology vs. UMC/JinHua**
Jurisdiction: Case No. 4:17-CV-06932-MMC
United States District Court for the Northern District of California
Work Product: Testifying expert, trade secret documents review, and declaration submission.
Nature of Case: Trade secret contention of Micron confidential documents.
Counsel: Retained by Jones Day (Contact: Randy Kay)
Date: 3/17 – 12/23

Case: **SK Hynix vs. BitMicro**
Jurisdiction: Investigation No. 337-TA-1097
United States International Trade Commission
Work Product: Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, **deposition taken**, issued witness statement.
Nature of Case: ITC infringement case concerning module stacking of SDRAM.
Counsel: Retained by Fish Richardson (Contact: Joseph Colaianni)
Date: 11/18 – 4/19

Case: ***Rohm Company IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Matt Colvin)
Date: 4/18 – 8/18

Case: ***Apple Inc., vs. Qualcomm Incorporated***
Jurisdiction: Case No. 3:17-CV-02402
United States District Court for the Southern District of California
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, ***2 depositions taken.***
Counsel: Fish & Richardson (Contact: Tony Nguyen)
Date: 1/18 – 5/19

Case: ***Macronix vs. Toshiba***
Jurisdiction: Investigation No. 337-TA-1046
United States International Trade Commission
Work Product: Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, ***deposition taken for 2 patents,*** issued witness statement and rebuttal witness statement, ***testified in ITC court on both infringement and invalidity.***
Nature of Case: ITC infringement case concerning advanced NAND Flash memory.
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 4/17 – 10/18

Case: ***Novatek Microelectronics Corp. IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date: 2/17 – 4/17

Case: ***Taiwan Semiconductor Manufacturing Company IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: John Goetz)
Date: 7/15 – 4/17

Case: **Triune Systems, LLC vs. Wayne Chen, et al.,**
Jurisdiction: Case No. 296-03209-2013,
District Court of Collin County, TX
Work Product: Testifying expert, database viewing, expert report, *video-taped testimony*
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: **Macronix vs. Spansion**
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: **Macronix vs. Spansion**
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: **Keranos, LLC v. Analog Devices et. al.**
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: **Silicon Storage Technology, Inc. v. Xicor, LLC**
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Testifying expert: issuing expert report, declarations, and
deposition taken.
Nature of Case: Patent infringement case concerning minimizing source current
during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

PROFESSIONAL EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 12 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35 μ m and 0.18 μ m CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00

Programmable Silicon Solutions, Sunnyvale, California

Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98

AMIC Technology, Santa Clara, California

Director of Flash Technology. Responsible for developing 0.35 μ m ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97

Altera Corp., San Jose, California

Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35 μ m generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96

Information Storage Devices, San Jose, California

Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95

Advanced Micro Devices, Sunnyvale, California

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5 μ m and 0.35 μ m flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K.-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.
8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.
9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994
10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.
11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.
12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.
13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.
14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.
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