

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Ken et al.
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Title: HIGH SPEED MEMORY CHIP MODULE AND ELECTRONICS
SYSTEM DEVICE WITH A HIGH SPEED MEMORY CHIP
MODULE

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PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 9,164,942
PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

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EX1005	PCT Pub. No. WO2008/124503 (“Tsern”)
EX1006	U.S. Patent No. 7,645,692 (“Matsubara”)
EX1007	U.S. Patent No. 7,785,933 (“Dozen”)
EX1008	U.S. Patent No. 5,498,990 (“Leung”)
EX1009	“Development of 3D Stack Package Using Silicon Interposer for High-Power Application.” N. Khan <i>et al. IEEE Transactions on Advanced Packaging</i> , Vol. 32, No. 1, February 2008 (“Khan”)
EX1010	U.S. Patent No. 6,226,755 (“Reeves”)
EX1011	U.S. Patent No. 8,193,635 (“Bruno”)
EX1012	RESERVED
EX1013	U.S. Patent Pub. No. 2010/0187671 (“Lin”)
EX1014	U.S. Patent No. 8,344,496 (“White”)
EX1015	U.S. Patent No. 6,353,538 (“Ali”)
EX1016	U.S. Patent No. 8,502,375 (“Liao”)
EX1017	U.S. Patent Pub. No. 2004/0158669 (“Weng”)

EX1018	RESERVED
EX1019	U.S. Patent No. 6,184,808 (“Nakamura”)
EX1020	U.S. Patent No. 8,895,345 (“Akiyama”)
EX1021	U.S. Patent No. 5,848,080 (“Dahm”)
EX1022	U.S. Patent No. 6,412,786 (“Pan”)
EX1023	U.S. Patent App. Pub. No. 2007/0109831 (“RaghuRam”)
EX1024	U.S. Patent No. 5,844,853 (“Kitsukawa”)
EX1025	U.S. Patent No. 8,405,214 (“Willey”)
EX1026	U.S. Patent No. 8,174,868 (“Liaw”)
EX1027	U.S. Patent No. 6,949,951 (“Young”)
EX1028	U.S. Patent No. 7,983,051 (“Lee-051”)
EX1029	Declaration of June Ann Munford
EX1030	<i>Semiconductor Device Fundamentals</i> (excerpts). Robert F. Pierret, 1996 (“Pierret”)
EX1031	“Application Specific Integrated Circuits (ASICs).” Martin Reiger. <i>The Electronic Design Automation Handbook</i> . Jansen, D., ed., 2003 (“Rieger”)
EX1032	RESERVED
EX1033	Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2025) United States Courts (uscourts.gov), available at: fcms_na_distprofile1231.2025.pdf

LISTING OF CLAIMS

Claim 1	
[1pre]	A high speed memory chip module, comprising:
[1a.1]	a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array integrated circuits (ICs), each of the memory cell array ICs has an input/output (I/O) data bus and
[1a.2]	at least one memory cell array corresponding to a first metal-oxide-semiconductor field-effect transistor (MOSFET) process, wherein the first MOSFET process corresponding to a first MOSFET gate length; and
[1b.1]	a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an I/O data bus of each of the memory cell array ICs,
[1b.2]	wherein the logic unit corresponds to a second MOSFET process, the second MOSFET process corresponds to a second MOSFET gate length, and the first MOSFET gate length is longer than the second MOSFET gate length;
[1c]	wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus.
Claim 2	
[2a]	The high speed memory chip module of claim 1, wherein the multiple memory cell array ICs of the type of memory cell array group comprise a flash IC or a Dynamic Random Access Memory (DRAM) IC,
[2b]	wherein a dicing method for at least one memory cell array IC comprises a Laser cutting process.

Claim 3	
[3a]	The high speed memory chip module of claim 1, further comprising: an interposer, wherein at least one memory cell array IC of the memory cell array group and the logic unit are disposed over two opposite sides of the interposer, respectively,
[3b]	wherein the interposer comprises silicon or oxide glass material.
Claim 4	
[4a]	The high speed memory chip module of claim 1, further comprising: an interposer, wherein the multiple memory cell array ICs are disposed over the interposer respectively, and the interposer is disposed over the logic unit,
[4b]	wherein the interposer comprises silicon or oxide glass material,
[4c]	wherein a dicing method for at least one memory cell array IC comprises a Laser cutting process.
Claim 5	
[5a]	The high speed memory chip module of claim 1, wherein the logic unit further comprises: a parallel-to-serial controller module for converting the first set of parallel data into the second set of parallel data, and
[5b]	the logic unit transmits the second set of parallel data to an application-specific integrated circuit (ASIC) or a system on chip (SOC) processor through the second transmission bus, wherein bit width of the first set and the second set of parallel data are different.
Claim 6	
[6]	The high speed memory chip module of claim 5, wherein the second transmission bus is a bus comprising the protocol of Universal Serial Bus (USB), a Serial Advanced Technology Attachment (SATA) bus, a Universal Flash Storage (UFS) bus, a mobile industry processor interface (MIPI) bus, or a Peripheral Component Interconnect Express (PCIe) bus.

Claim 7	
[7]	The high speed memory chip module of claim 5, wherein a signal swing of data transmitted through the first transmission bus and a signal swing of data received through the first transmission bus are different.
Claim 8	
[8]	The high speed memory chip module of claim 5, wherein a signal swing of data transmitted through the second transmission bus and a signal swing of data received through the second transmission bus are different.
Claim 9	
[9]	The high speed memory chip module of claim 5, wherein a transmitting data rate of the first transmission bus and a receiving data rate of the first transmission bus are different.
Claim 10	
[10]	The high speed memory chip module of claim 5, wherein a transmitting data rate of the second transmission bus and a receiving data rate of the second transmission bus are different.
Claim 11	
[11]	The high speed memory chip module of claim 1, wherein each of the memory cell array ICs of the type of memory cell array group corresponds to a first seal ring and the logic unit corresponds to a second seal ring, a circuit of each of the memory cell array ICs is surrounded by a first seal ring and a circuit of the logic unit is surrounded by the second seal ring.
Claim 12	
[12]	The high speed memory chip module of claim 11, wherein at least one through silicon via (TSV) exists outside a first seal ring of each of the memory cell array ICs.

Claim 13	
[13]	The high speed memory chip module of claim 12, further comprising: a metal layer disposed over a topmost memory cell array of the type of memory cell array group, wherein the metal layer covers more than 50% area of the topmost memory cell array.
Claim 14	
[14]	The high speed memory chip module of claim 12, wherein the at least one TSV is used for connecting to a power or a ground supply.
Claim 15	
[15]	The high speed memory chip module of claim 11, wherein at least one TSV exists outside the second seal ring of the logic unit.
Claim 16	
[16]	The high speed memory chip module of claim 15, wherein the logic unit is stacked over a topmost memory cell array IC of the type of memory cell array group.
Claim 17	
[17]	The high semiconductor speed memory chip module of claim 16, further comprising: a metal layer disposed over the logic unit, wherein the metal layer covers more than 50% area of the logic unit.
Claim 18	
[18]	The high speed memory chip module of claim 15, wherein the at least one TSV is used for connecting to a power or a ground supply.
Claim 19	
[19pre]	A electronics system device with a high speed memory chip module, the device comprising:
[19a]	an ASIC processor;
[19b]	a type of memory cell array group, wherein the type of memory cell

	array group comprises multiple memory cell array ICs, each of the memory cell array ICs has an (I/O) data bus; and
[19c]	a logic unit for accessing the type of memory cell array group through a first transmission bus, wherein the first transmission bus is used for transmitting a first set of parallel data along with the memory cell array ICs, and bus width of the first transmission bus is wider than bus width of an (I/O) data bus of each of the memory cell array ICs,
[19d]	wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus, and transmits the second set of parallel data to the ASIC processor;
[19e]	wherein the ASIC processor executes a predetermined function corresponding to the second set of parallel data while the ASIC processor is under operating condition,
[19f]	wherein bit width of the first set and the second set of parallel data are different.
Claim 20	
[20a]	The electronics system device of claim 19, further comprising: an interposer, wherein at least one memory cell array IC of the memory cell array group and the logic unit are disposed over two opposite sides of the interposer, respectively,
[20b]	wherein the interposer comprises silicon or oxide glass material,
[20c]	wherein a dicing method for at least one memory cell array ICs comprises a Laser cutting process.
Claim 21	
[21a]	The electronics system device of claim 19, further comprising: an interposer, wherein the multiple memory cell array ICs are disposed over the interposer respectively, and the interposer is disposed over the logic unit,
[21b]	wherein the interposer comprises silicon or oxide glass material.

Claim 22	
[22]	The electronics system device of claim 19, wherein the logic unit comprises: a parallel-to-serial controller module for converting the first set of parallel data into the second set of parallel data.
Claim 23	
[23]	The electronics system device of claim 22, wherein a signal swing of data transmitted through the first transmission bus and a signal swing of data received through the first transmission bus are different.
Claim 24	
[24]	The electronics system device of claim 22, wherein a signal swing of data transmitted through the second transmission bus and a signal swing of data received through the second transmission bus are different.
Claim 25	
[25]	The electronics system device of claim 22, wherein a transmitting data rate of the first transmission bus and a receiving data rate of the first transmission bus are different.
Claim 26	
[26]	The electronics system device of claim 22, wherein a transmitting data rate of the second transmission bus and a receiving data rate of the second transmission bus are different.
Claim 27	
[27]	The electronics system device of claim 19, wherein each of the memory cell array ICs of the type of memory cell array group corresponds to a first seal ring and the logic unit corresponds to a second seal ring, a circuit of each of the memory cell array ICs is surrounded by the first seal ring and a circuit of the logic unit is surrounded by the second seal ring.

Claim 28	
[28]	The electronics system device of claim 27, wherein at least one TSV exists outside a first seal ring of each of the memory cell array ICs.
Claim 29	
[29a]	The electronics system device of claim 28, further comprising: a metal layer disposed over a topmost memory cell array IC of the type of memory cell array group, wherein the metal layer covers more than 50% area of the topmost memory cell array IC,
[29b]	wherein the memory cell array ICs are stacked over the logic unit.
Claim 30	
[30]	The electronics system device of claim 28, wherein the at least one TSV is used for connecting to a power or a ground supply.
Claim 31	
[31]	The electronics system device of claim 27, wherein at least one TSV exists outside the second seal ring of the logic unit.

Apple Inc. (“Petitioner”) petitions for IPR of claims 1-31 (the “Challenged Claims”) of U.S. Patent No. 9,164,942 (“the ’942 Patent”), assigned to WeCrevention, Inc. (“Patent Owner”/“PO”). Compelling evidence presented in this Petition demonstrates at least a reasonable likelihood that Petitioner will prevail with respect to at least one of the Challenged Claims. Accordingly, Petitioner respectfully submits that an IPR should be instituted, and that the Challenged Claims should be canceled as unpatentable.

I. REQUIREMENTS FOR IPR—37 C.F.R. §42.104

A. Grounds for Standing—37 C.F.R. §42.104(a)

Petitioner certifies that the ’942 Patent is available for IPR. Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the below-identified grounds.

B. Challenge and Relief Requested—37 C.F.R. §42.104(b)

Petitioner requests IPR of the Challenged Claims on the below grounds. Dr. David Liu provides supporting explanations in an expert declaration. EX1003, ¶¶1-314.

Asserted Grounds		
Ground	Claims	Basis
1A	19	§103: Lee
1B	19, 22, 25-26	§103: Lee-Tsern
1C	21	§103: Lee-Tsern-Khan

1D	20	§103: Lee-Tsern-Khan-Dozen
1E	23-24	§103: Lee-Tsern-Leung
1F	27-28, 31	§103: Lee-Tsern-Lin
1G	29	§103: Lee-Tsern-Lin-Ali
1H	30	§103: Lee-Tsern-Lin-White
1I	1, 5, 9-10	§103: Lee-Tsern-Matsubara
1J	2	§103: Lee-Tsern-Matsubara-Dozen
1K	3	§103: Lee-Tsern-Matsubara-Khan
1L	4	§103: Lee-Tsern-Matsubara-Khan-Dozen
1M	6	§103: Lee-Tsern-Matsubara-Weng
1N	7-8	§103: Lee-Tsern-Matsubara-Leung
1O	11-12, 15	§103: Lee-Tsern-Matsubara-Lin
1P	13	§103: Lee-Tsern-Matsubara-Lin-Ali
1Q	14, 18	§103: Lee-Tsern-Matsubara-Lin-White
1R	16	§103: Lee-Tsern-Matsubara-Lin-Liao
1S	17	§103: Lee-Tsern-Matsubara-Lin-Liao-White

The '942 Patent claims priority from several previously filed applications, the earliest of which was filed on October 11, 2011. Each of the above identified references qualifies as prior art under 35 USC §§102(a), (b), or (e) (as shown below) even if October 11, 2011 ("Critical Date") is used as the priority date of the '942 Patent.¹

¹ Petitioner does not concede that the claims of the '942 Patent are entitled to this priority date.

Reference	Prior Art Date	Status
Lee	12/23/2004 (published)	§102(b)
Tsern	10/16/2008 (published)	§102(b)
Khan ²	2008 (published)	§102(b)
Dozen	8/31/2010 (patented)	§102(b)
Leung	3/12/1996 (patented)	§102(b)
Lin	7/29/2010 (published)	§102(b)
Ali	3/5/2002 (patented)	§102(b)
White	4/29/2009 (filed)	§102(e)
Matsubara	1/12/2010 (patented)	§102(b)
Weng	8/12/2004 (published)	§102(b)
Liao	7/29/2010 (filed)	§102(e)

II. THE '942 PATENT

A. Summary

The '942 Patent relates to a “high speed memory chip module” that includes a “type of memory cell array group and a logic unit.” EX1001, Abstract. The type of memory cell array group includes “multiple memory cell array integrated circuits (ICs),” *e.g.*, a Dynamic Random Access Memory (DRAM) IC. *Id.*, Abstract, 3:40-51. The logic unit is “used for accessing the memory cell array IC[s],” and “convert[s] [a] first set of parallel data” from the memory cell ICs “into

² See generally EX1029.

a second set of parallel data,” which it “transmits ... to an application-specific integrated circuit (ASIC).” *Id.*, 3:61-4:9; EX1003, ¶29.

B. Prosecution History

The '942 Patent was allowed in a first action Notice of Allowance, with the Reasons for Allowance stating that “there is no teaching, suggestion, or motivation for combination in the prior art to a high speed memory including where the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through a second transmission bus.” EX1002, 14-15.

III. LEVEL OF ORDINARY SKILL

The range of qualifications for a POSITA would have included at least a master’s degree in electrical engineering, or a comparable field, and at least two years of professional experience working with DRAM. EX1003, ¶27. Additional years of experience could substitute for an advanced-level degree (and vice versa). *Id.*

IV. CLAIM CONSTRUCTION—37 C.F.R. §42.104(b)(3)

All claim terms should be construed according to their ordinary and customary meaning under the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. Petitioner submits that no claim terms need be construed to resolve issues of controversy in the present Petition, but

reserves the right to respond to construction issues raised by Patent Owner.

Wellman, Inc. v. Eastman Chem. Co., 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Petitioner is not conceding that each challenged claim satisfies all statutory requirements, nor waiving arguments/grounds that cannot be raised in this proceeding.

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A: Claim 19 Is Obvious Over Lee

The section below introduces Lee.³

1. Lee

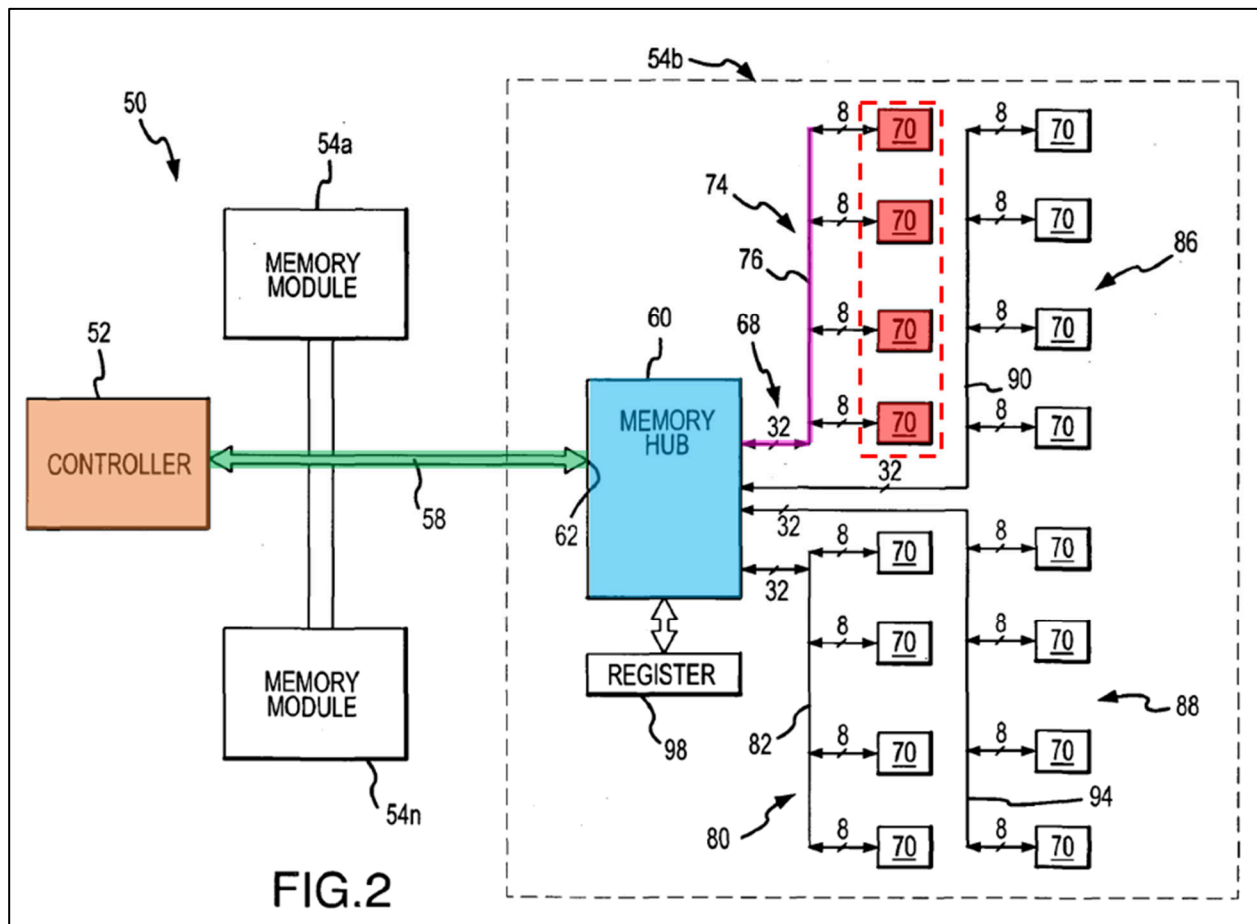
Lee describes a memory system that includes a memory module that is configurable “in a plurality of data formats.” EX1004, [0009].⁴ “When programmed for a high bandwidth, the memory hub simultaneously accesses the

³ This discussion of Lee is incorporated into Grounds 1A-1S. Similarly, discussion of other references is incorporated into all grounds advancing the same.

⁴ In below addressing invalidity of the Challenged Claims over the teachings of the cited references, Petitioner relies on the teachings of those references as would have been understood by a POSITA, without necessarily relying upon incorporation of each or any of the disclosed or referenced exemplary details.

memory devices in all of the ranks,” and “[w]hen programmed for a high memory depth, the memory hub accesses the memory devices in only one of the ranks at a time.” *Id.*; EX1003, ¶30.

In this system (*see* FIG. 2, *infra*), a controller 52 (orange) is “coupled to several memory modules 54*a, b ... n* through a high-speed link 58” (green). EX1004, [0015]. Each memory module “includes a memory hub 60 [blue] ... coupled to the high-speed link 58 and a bus system 68 coupled to several memory devices 70,” *e.g.*, DRAM. *Id.* “[T]he memory devices 70 are divided into four groups or ‘ranks’ [each] coupled to the memory hub 60 through a respective bus system” 76 (pink), 82, 90, 94. *Id.*, [0016]; EX1003, ¶31.



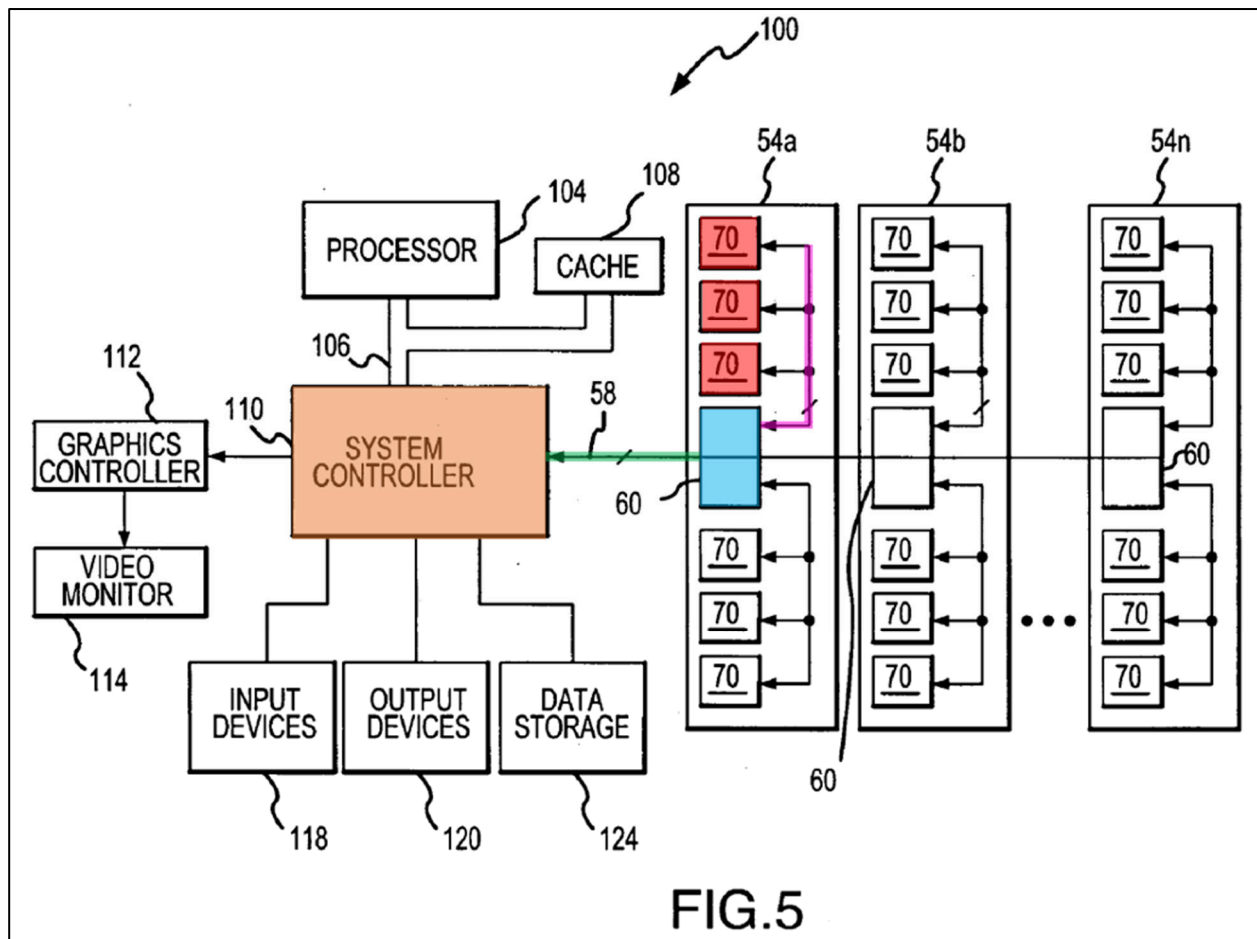
Lee, FIG. 2 (annotated)

Lee's mode of operation is configured by "a non-volatile register 98 in the memory module 54." EX1004, [0017]. First, in "high memory bandwidth" mode, "the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access." *Id.* These "128 bits of data" from all of the memory devices "can be coupled through the high-speed link 58 by either increasing the speed of the link 58 or the size of the data word coupled through the link 58." *Id.* Second, in "high

memory depth mode, only one rank ... [is] addressed at a time.” *Id.*, [0018];

EX1003, ¶32.

In a computer system (*see* FIG. 5, *infra*) implementing Lee’s configurable memory system, the memory hubs (blue of the memory modules are coupled to a “system controller” (orange) that facilitates access to the memory modules by the system processor 104. EX1004, [0023], [0025]; EX1003, ¶33.



Lee, FIG. 5 (annotated)

Lee is analogous art to the '942 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1004, [0001], [0016]-[0017]; EX1003, ¶¶34-35.

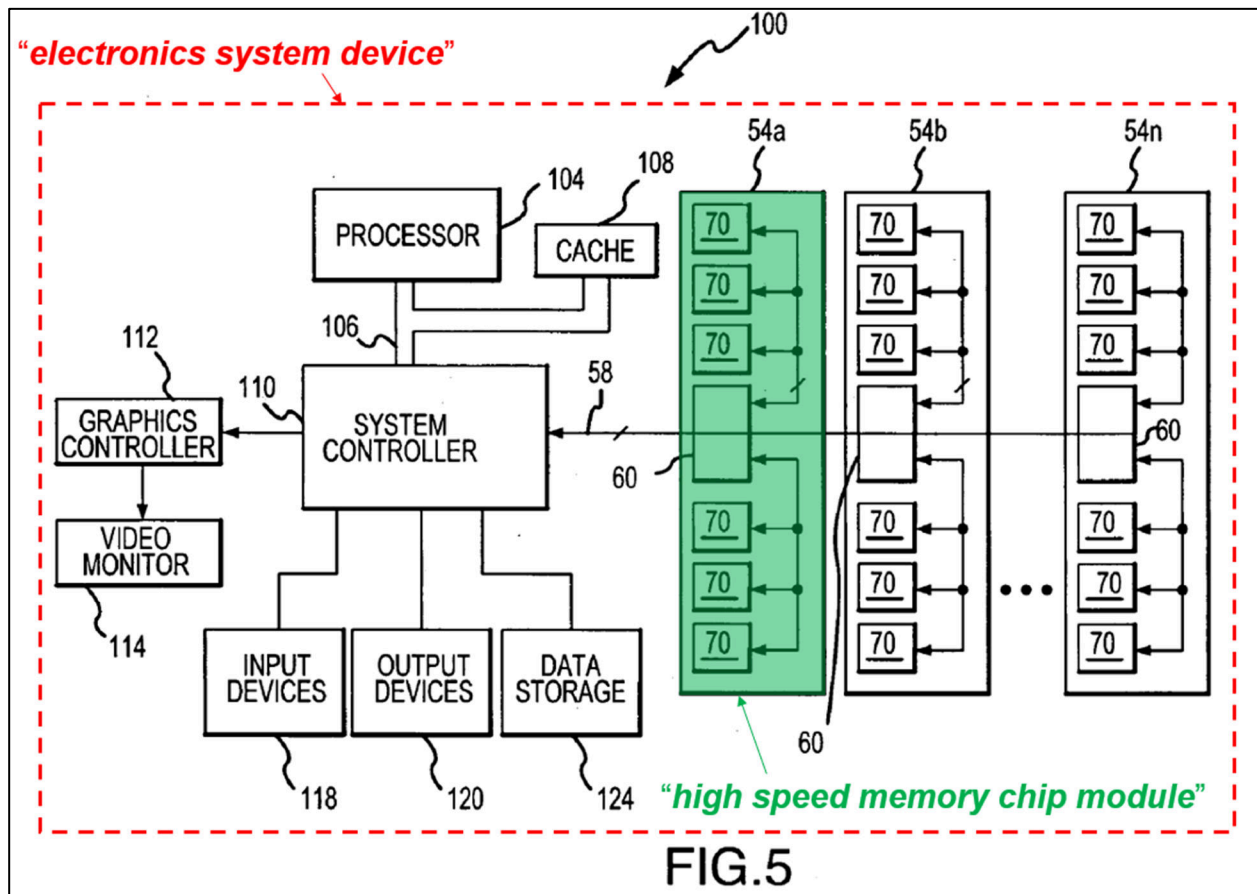
2. Analysis

(a) Claim 19

[19pre]⁵

Lee's "computer system 100" is an *electronics system device*. EX1004, [0023]; *see* FIG. 5 (*infra*), claim 28. EX1003, ¶¶36-37.

⁵ Petitioner does not concede that the preambles of the Challenged Claims are limiting.



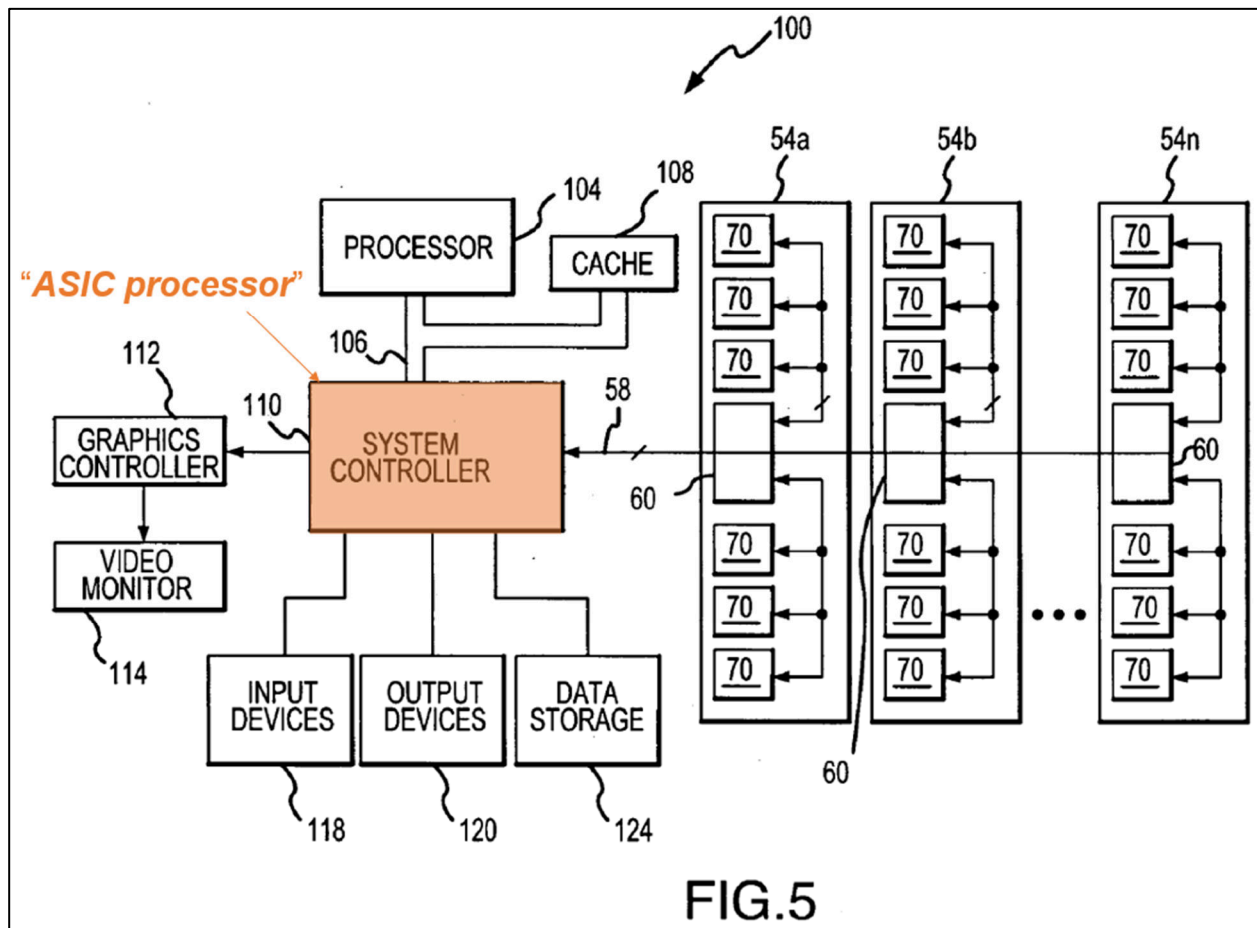
Lee, FIG. 5 (annotated)

Lee's computer system includes a "memory system 50" that "includes a controller 52 coupled to several memory modules 54a, b ... n through a high-speed link 58," where each memory module includes "memory devices 70." *Id.*, [0015]-[0016], [0023]; *see* Abstract, [0014] ("FIG. 5 is a block diagram of a computer system using the memory system of FIG. 2"), FIG. 2. Each memory module 54 (e.g., memory module 54a, green) corresponds to a **memory chip module**, because it includes memory chips. EX1003, ¶38.

The memory module is a *high speed memory chip module* because it is coupled to the controller “through a high-speed link.” EX1004, [0015]; *see* [0017]; EX1003, ¶39.

[19a]

Lee’s system includes “a system controller 110, which is also sometimes referred to as a ‘North Bridge’ or ‘memory controller,’” orange in FIG. 5, *infra*. EX1004, [0023]. A POSITA would have understood that a North Bridge controller is an *ASIC processor*. *See* EX1010, 5:30-33 (“Northbridge 14 is generally considered an ... application specific integrated circuit (ASIC)”); EX1011, [0032] (“an ASIC die ... such as a north bridge”); EX1003, ¶40.



Lee, FIG. 5 (annotated)

Alternatively/additionally, a POSITA would have found it obvious to implement Lee's controller as an *ASIC processor*, as follows. EX1003, ¶¶41-44.

First, ASICs provide performance advantages. EX1003, ¶42. Because ASIC chips are custom-built to perform a specific task, they are compact, inexpensive, and capable of high-speed, low-energy operation. EX1003, ¶42 (citing EX1031, 384-385 (listing advantages of ASICs)).

Second, implementation of Lee's controller as an ASIC is an application of known techniques (an ASIC memory controller) to a known system (Lee's

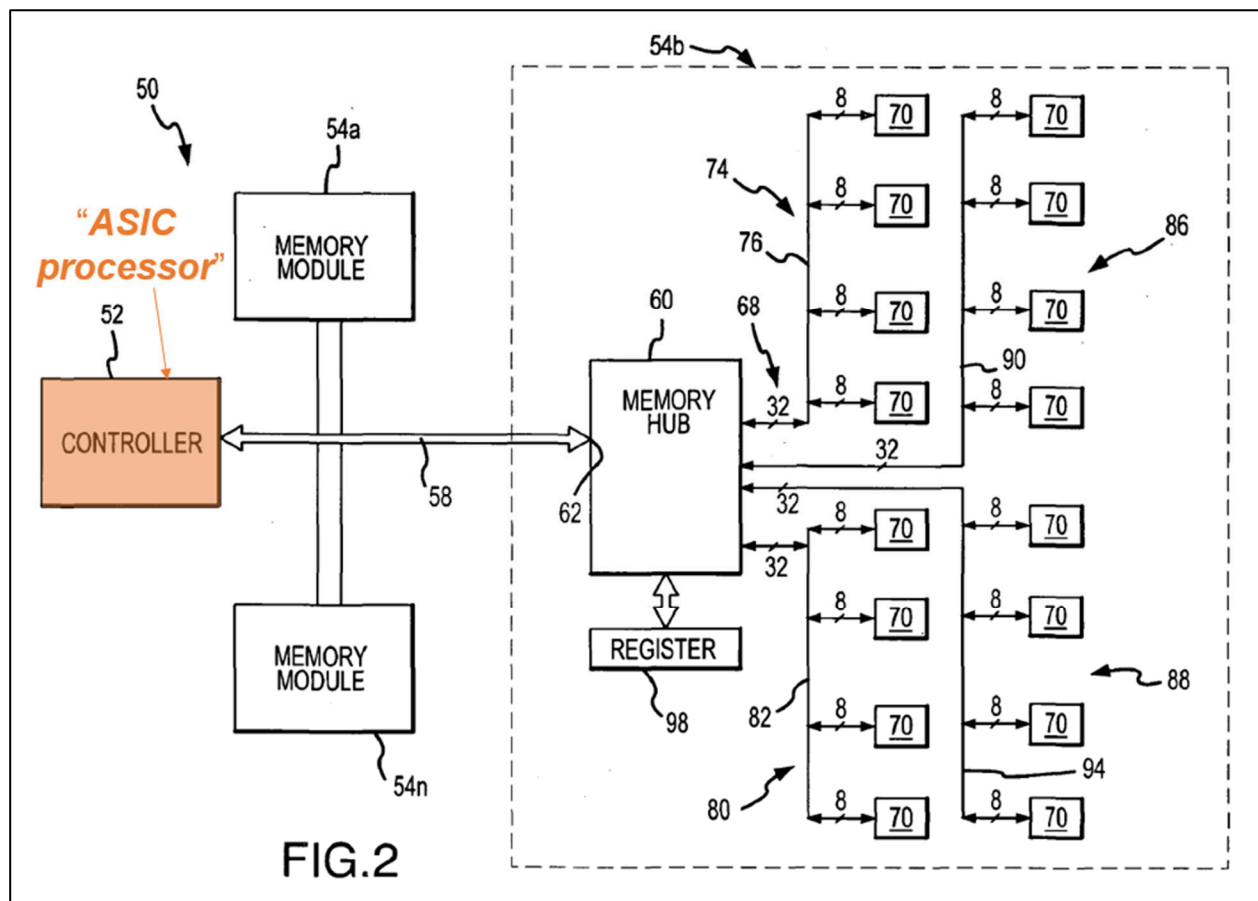
memory system) to yield predictable results (a memory system having an ASIC controller). EX1003, ¶42; *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421 (2007).

Third, implementation of Lee's controller as an ASIC is one of a finite number of predictable solutions (*e.g.*, implementation of the controller as an ASIC or as a general-purpose chip), and with a reasonable expectation of success (discussed *infra*). EX1003, ¶43; *see KSR*, 550 U.S. at 421.

A POSITA would have expected success in implementing Lee's North Bridge controller as an ASIC processor because ASIC implementation of North Bridge controllers was standard. *See* EX1010, 5:30-33; EX1011, [0032]; EX1003, ¶45.

Lee's FIG. 5, showing the North Bridge ASIC processor, illustrates "a computer system using the memory system of FIG. 2." EX1004, [0014]; *see* [0023]. FIG. 2, *infra*, illustrates a "memory system 50 [that] includes a controller 52 coupled to several memory modules 54*a*, *b* ... *n* through a high-speed link 58." EX1004, [0015]. A POSITA have understood that the controller 52 of Lee's FIG. 2 (orange) is also a North Bridge controller, consistent with the North Bridge controller 110 of FIG. 5, and thus that the controller 52 is *an ASIC processor*. EX1003, ¶46. This is because of the stated correspondence between FIG. 2 and FIG. 5 systems, and because the controller 110 of FIG. 5 is connected to the

memory hub via the high-speed link 58, like the controller 52 in FIG. 2. *See* EX1004, [0015]; EX1003, ¶46. Alternatively/additionally, a POSITA would have found it obvious to implement Lee's FIG. 2 controller 52 as an ASIC processor given Lee's teachings related to in the similarly structured FIG. 5 system, and given advantages of ASIC processors, discussed *supra*. EX1003, ¶46.



Lee, FIG. 2 (annotated)

[19b]

Lee's memory system includes "several memory modules 54a, b ... n," each of which includes "memory devices 70 [] divided into four groups or 'ranks.'"

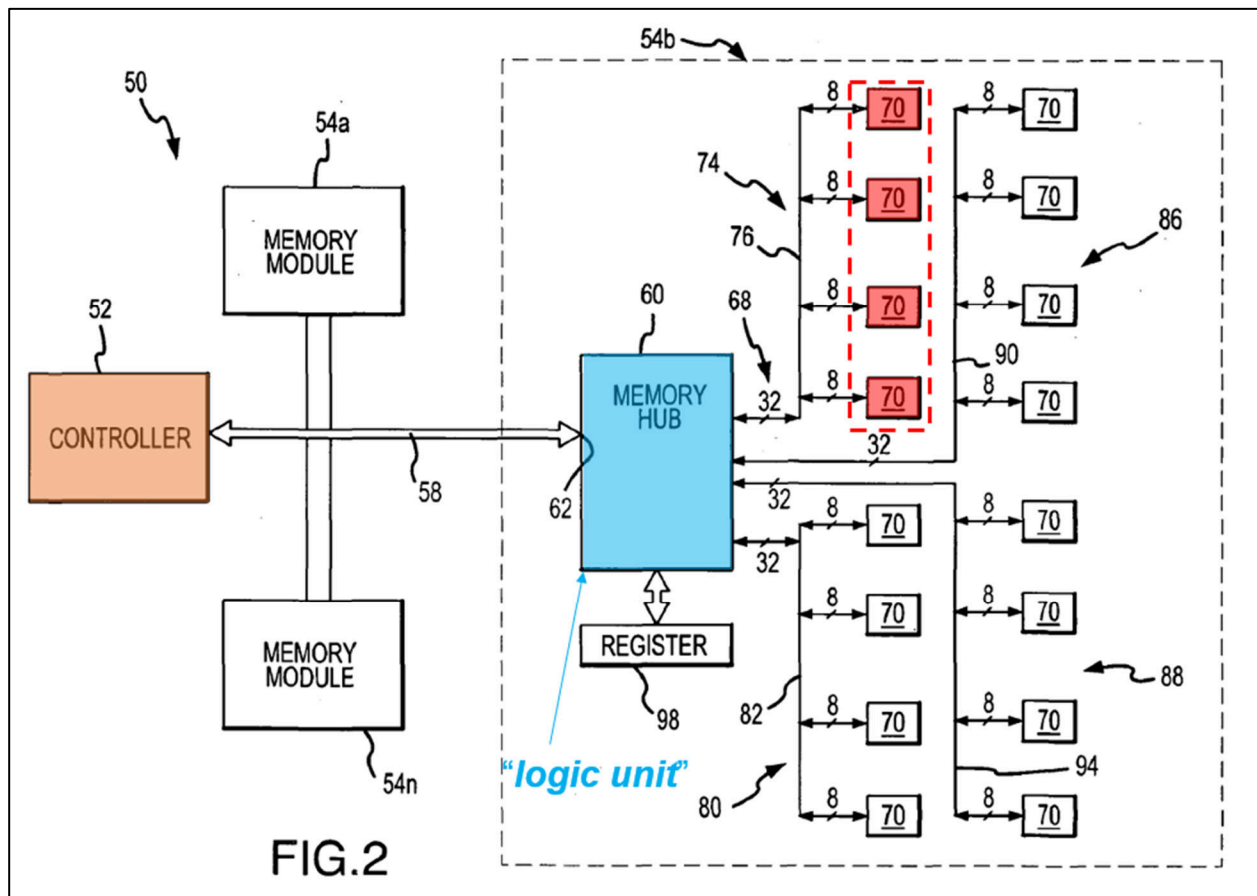
“[T]he memory devices 70 are divided into four groups or ‘ranks.’”

EX1004, [0016]. Each group/rank corresponds to a *type of memory cell array group* because it is a group of memory cells (*e.g.*, memory devices 70). EX1003, ¶49. For instance, “a first rank 74” (*type of memory cell array group*) (red in FIG. 2, *supra*) “includes four memory devices 70” (*comprises multiple memory cell array ICs*), and likewise for ranks 80, 86, 88. EX1004, [0016]; *see* claims 1, 13, 28, FIG. 5; EX1003, ¶49. Alternatively/additionally, the multiple groups/ranks collectively correspond to a *type of memory cell array group*. EX1003, ¶49.

Each memory device 70 (*memory cell array IC*) has “an 8-bit data bus” (*(I/O) data bus*) (purple *supra*). EX1004, [0016]; EX1003, ¶50.

[19c]

Lee’s “memory hub 60” (blue in FIG. 2, *infra*) corresponds to a *logic unit* because it is “programmable to configure the memory module in a plurality of data formats.” EX1004, [0016], claim 1; *see* [0009], [0017]-[0020], claims 1-5; EX1003, ¶51.

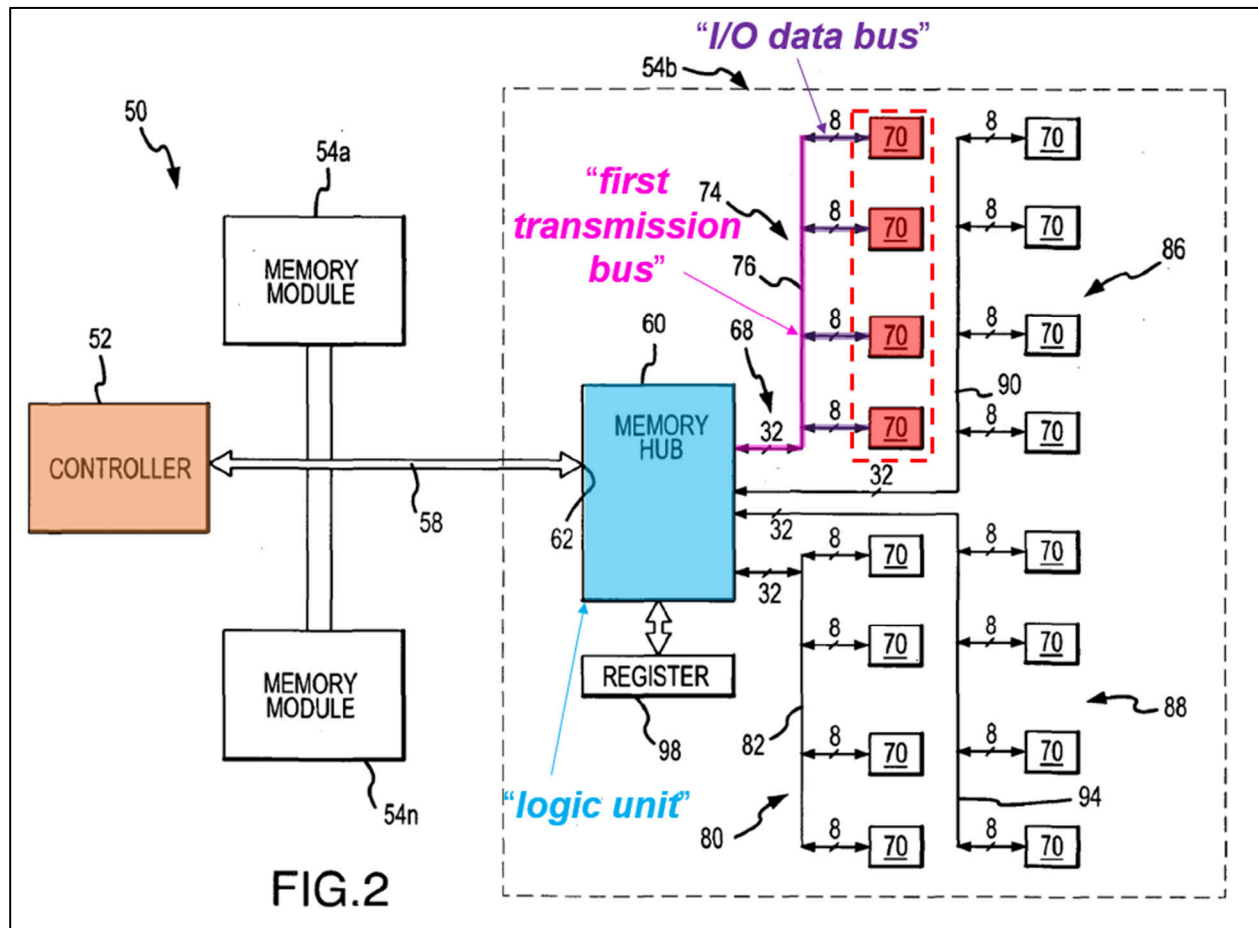


Lee, FIG. 2 (annotated)

The memory hub 60 (*logic unit*) is coupled to (*for accessing*) the memory devices 70 through “a bus system 68,” which enables access to the memory devices of each rank “through a respective bus system” 76, 82, 90, 94. EX1004, [0016]. Each bus system individually corresponds to a *first transmission bus*. EX1003, ¶52. Alternatively/additionally, the bus system 68 (composed of the four bus systems 76, 82, 90, 94) corresponds to the *first transmission bus*. *Id.*

Each of Lee's bus systems individually corresponds to a **first transmission bus**

The bus system for each rank corresponds to a **first transmission bus** through which the memory hub can **access** the memory cell array ICs in that rank. EX1003, ¶53. For instance, the first rank 74 (**type of memory cell array group**) of memory devices are "coupled to the memory hub 60 through a first bus system 76 having a 32-bit data bus" (**first transmission bus**) (pink in FIG. 2, *infra*). EX1004, [0016]; *see id.*, claim 2, claim 14; EX1003, ¶53.



Lee, FIG. 2 (annotated)

The bus system for each rank is a “32-bit data bus,” and “the four memory devices 70 together provide 32 bits for the 32-bit data buses.” EX1004, [0016].

That is, the bus system for each rank (*first transmission bus*) is *used for transmitting data along with*⁶ (*to/from*) *the memory cell array ICs*, e.g., for transmitting the data provided from the memory devices of the rank. EX1003, ¶54. The data transmitted on the bus system for each rank (*first transmission bus*) are *a first set of parallel data*, e.g., 32 parallel bits of data carried on the “32-bit data bus.” EX1004, [0016]; *see* [0017] (“the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices”), [0018], claim 6, [0009], [0019], claims 2, 3, 4, and 7; EX1003, ¶54.

In the example of Lee’s FIG. 2, the *bus width of the (I/O) data bus of each of the memory cell array ICs* (purple in FIG. 2, *supra*; *see* [19b]) is 8 bits. *See* EX1004, [0016] (“each of the memory devices 70 have an 8-bit data bus”), FIG. 2; EX1003, ¶55. The *bus width of the first transmission bus* (e.g., first bus system

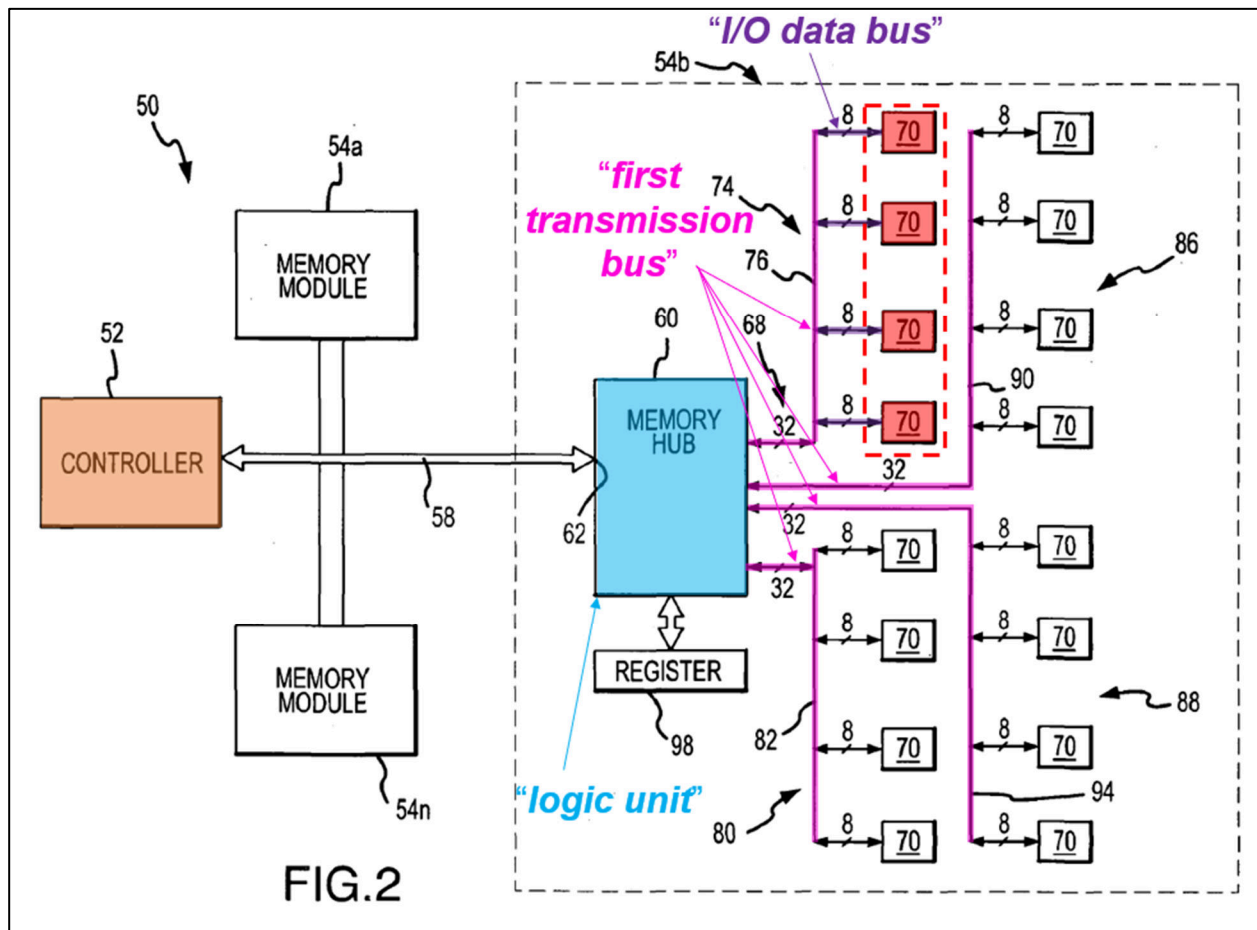
⁶ Without conceding that the claims are not indefinite, Petitioner interprets the phrase “along with the memory cell array ICs” as “to/from the memory cell array ICs.” EX1003, ¶51.

76, pink) is 32 bits, *i.e.*, ***wider than the bus width of each I/O data bus***. See

EX1004, [0016] (“a first bus system 76 having a 32-bit data bus”); EX1003, ¶55.

Lee’s bus system 68 corresponds to the ***first transmission bus***

Alternatively/additionally, Lee’s “bus system 68” (pink in FIG. 2, *infra*), which is composed of the four bus systems 76, 82, 90, 94, corresponds to the ***first transmission bus*** through which the memory hub can ***access*** the memory cell array ICs. EX1004, [0016] (“bus system 68 coupled to several memory devices 70”); EX1003, ¶56. The bus system 68 is ***used for transmitting data along with (to/from) the memory cell array ICs*** because each individual bus system 76, 82, 90, 94 of the bus system 68 is so used, discussed *supra*. See EX1004, [0016]-[0019]; EX1003, ¶56.



Lee, FIG. 2 (annotated)

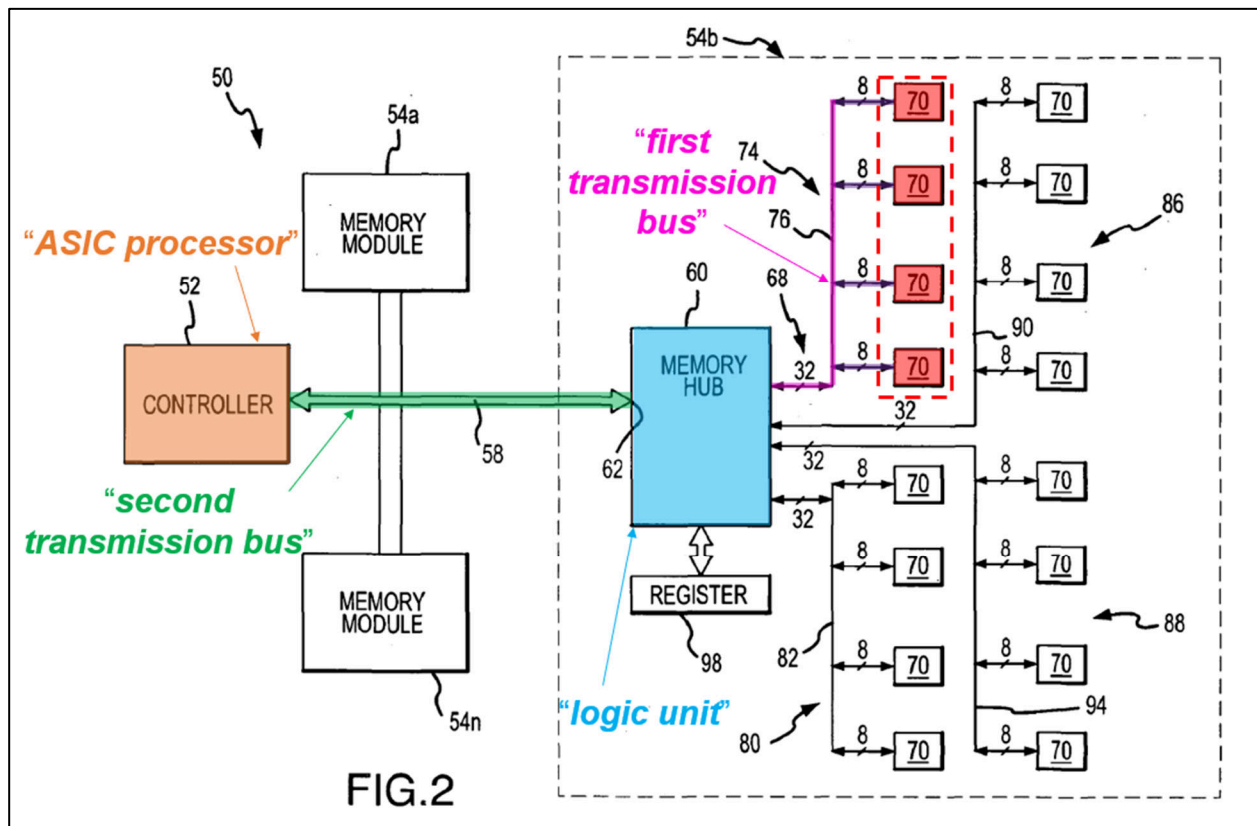
Each individual bus system transmits *parallel data*, as discussed *supra*, and thus the data transmitted on the bus system 68 (*first transmission bus*) are a *first set of parallel data*. See EX1004, [0016]-[0019]; EX1003, ¶57. Alternatively/ additionally, the individual bus systems 76, 82, 90, 94 are connected in parallel to the memory hub, *e.g.*, so that the memory hub can “address[] all of the memory devices simultaneously.” EX1004, [0017]; *see* claims 3-4; EX1003, ¶57. Accordingly, the parallel data transmitted on each individual bus system 76, 82, 90, 94 is parallel to the data transmitted on each other individual bus system.

Thus, the data transmitted on the bus system 68 (***first transmission bus***) are ***a first set of parallel data***, e.g., “128 bits of data” transmitted “simultaneously” and in parallel on the four constituent bus systems. EX1004, [0017]; EX1003, ¶57.

The bus width of the bus system 68 is equal to the total bus width of the four constituent bus systems, each of which is 32 bits wide, discussed *supra*. See EX1004, [0016], FIG. 2; EX1003, ¶58. That is, the bus width of the bus system 68 (***bus width of the first transmission bus***) is 128 bits, *i.e.*, ***wider than*** the 8-bit bus width of each I/O data bus. See EX1004, [0016], FIG. 2; EX1003, ¶58.

[19d]

Lee’s system includes a “high-speed link 58” (***second transmission bus***) (green in FIG. 2, *infra*) coupled to the memory hub 60. EX1004, [0016]; see [0015], [0017]-[0019], [0025], claim 13; EX1003, ¶59.



Lee, FIG. 2 (annotated)

The data transmitted on Lee’s high-speed link (*second transmission bus*) is *a second set of parallel data*. EX1003, ¶60. When operated in “high memory bandwidth” mode, Lee’s high-speed link can be configured such that “a 128-bit data word may be coupled through the link 58,” *i.e.*, the 128-bit data word corresponds to the *second set of parallel data*. EX1004, [0017]. Lee’s high-speed link can alternatively be configured to “couple 64-bit data words” or “32-bit data word[s],” *i.e.*, the 64-bit data word or 32-bit data word corresponds to the *second set of parallel data*. *Id.*; EX1003, ¶60.

The high-speed link “has a capacity for coupling data ... between the controller 52 and each memory module 54,” *i.e.*, the high-speed link (***second transmission bus***) transmits the ***second set of parallel data*** carried on the high-speed link to the controller 52 (orange) (***to the ASIC processor***). EX1004, [0015]; *see* claim 13; EX1003, ¶61.

A POSITA would have found obvious that Lee’s memory hub (***logic unit***) is ***used for converting the first set of parallel data into the second set of parallel data***, both when the ***first set of parallel data*** are the data transmitted on an individual bus systems and alternatively/additionally, when the ***first set of parallel data*** are the data transmitted on the collective bus system 68, discussed *infra*. EX1003, ¶62.

Conversion of data when an individual bus system corresponds to the first transmission bus

In “high memory bandwidth” mode, Lee’s memory hub “simultaneously” receives multiple sets of parallel data from the multiple bus systems 76, 82, 90, 94. EX1004, [0016]-[0017], FIG. 2. By “simultaneously” addressing “all of the memory devices,” “128 bits of data are ... read from the memory devices,” *i.e.*, 32 bits are received through each of the four bus systems. *Id.*, [0017]; *see* [0019]; EX1003, ¶¶63-64. These simultaneously received 128 bits of data include the 32 bits (***first set of parallel data***) transmitted on the first bus system 76. Lee describes

two implementations for transmission of that 128 bits of data on the high-speed link 58, discussed *infra*. See EX1004, [0017]; EX1003, ¶65. Both of these implementations involve ***converting the first set of parallel data*** (the data transmitted on the first bus system 76) ***into the second set of parallel data*** (the data transmitted on the high-speed bus 58). EX1003, ¶65.

In one implementation of “high memory bandwidth” mode, “128 bits of data are ... read from the memory devices” (*i.e.*, 32 bits through each of the four bus systems), but “the link 58 may transfer only a 32-bit data word” or a “64-bit data word[]” (***second set of parallel data***). EX1004, [0017]; EX1003, ¶66. A POSITA would have found obvious that receiving 128 bits of data simultaneously through multiple bus systems and then transmitting that data in a 64- or 32-bit word through a single bus system involves the memory hub ***converting*** the received data (including ***the first set of parallel data***) to the transmitted data (***second set of parallel data***), *e.g.*, by multiplexing the received data. EX1003, ¶¶66-68 (citing EX1019, Abstract (“a parallel-to-parallel converter for converting an ‘m’-bit parallel signal into an ‘n’-bit parallel signal). Specifically, the bit width of the parallel data received through the multiple bus systems (128 bits of simultaneously received data) is different from the bit width of the parallel data transmitted through the high-speed link 58 (*e.g.*, one 32-bit or 64-bit word). See EX1004, [0017]; EX1003, ¶¶66-68. A POSITA would have recognized that this

implementation—*i.e.*, receiving data of one bit width and then transmitting that same data in a different bit width—involves **converting** the received data (including ***the first set of parallel data***) to the transmitted data (***second set of parallel data***). EX1003, ¶¶66-68 (citing EX1019, Abstract).

In another implementation, “[t]he 128 bits of data [are] coupled through the high-speed link by [] increasing ... the size of the data word coupled through the link 58.” EX1004, [0017]. For instance, a “128-bit data word” (***second set of parallel data***) “may be coupled through the link 58.” EX1004, [0017]. That is, Lee’s memory hub (***logic unit***) receives 128 bits of data through four distinct bus systems, and **converts** that received data to a “128-bit data word” for transmission on the single high-speed link 58. EX1004, [0017]; *see* [0019]; EX1003, ¶69. A POSITA would have found obvious that receiving data simultaneously through multiple bus systems and then transmitting that data through a single bus system involves **converting**, by the memory hub (***logic unit***) the data received from the multiple bus systems (*i.e.*, 128 bits of simultaneously received data, including the 32-bit ***first set of parallel data*** transmitted on the first bus system 76) into the data transmitted on the single high-speed link 58 (***the second set of parallel data***). *See* EX1003, ¶69.

Conversion of data when the bus system 68 corresponds to the second transmission bus

Alternatively/additionally, in “high memory bandwidth” mode, the “128 bits of data” that are “simultaneously” “read from the memory devices” collectively correspond to the *first set of parallel data*, discussed *supra* for [19c]. EX1003, ¶¶70-71.

In one implementation, the 128 bits (*first set of parallel data*) are read simultaneously from the bus system 68, but “the link 58 may transfer only a 32-bit data word” or a “64-bit data word[]” (*second set of parallel data*). EX1004, [0017]; EX1003, ¶72. A POSITA would have found obvious that receiving 128 bits of data simultaneously through multiple bus systems and then transmitting that data as a 64- or 32-bit word through a single bus system involves *converting* the received data (*first set of parallel data*) to the transmitted data (*second set of parallel data*), *e.g.*, by multiplexing the received data. EX1003, ¶72 (citing EX1019, Abstract).

In another implementation, the 128 bits of data are received through four distinct bus systems that constitute the bus system 68 and *converted* to a “128-bit data word” for transmission on the single high-speed link 58, discussed *supra*. EX1004, [0017]; *see* [0019]; EX1003, ¶73. A POSITA would have found obvious that receiving data simultaneously through multiple bus systems and then

transmitting that data through a single bus system involves *converting*, by the memory hub (*logic unit*) the data received from the multiple bus systems (*first set of parallel data*) into the data transmitted on the single high-speed link 58 (*second set of parallel data*), *e.g.*, by multiplexing. EX1003, ¶73.

[19e]

Lee's controller 52 (*ASIC processor*) "generate[s] memory requests that are coupled to the memory modules." *Id.*, [0026]; *see* [0015], [0009], [0024]. The controller generating memory requests corresponds to *the ASIC processor executing a predetermined function*. EX1003, ¶74. Indeed, an ASIC is a chip that is designed to execute a predetermined function. EX1003, ¶75 (citing EX1031, 384).

Generating a memory request by the controller (*predetermined function*) results in the transmission of the second set of data along Lee's high-speed bus to/from the memory module, *i.e.*, *the predetermined function corresponds to the second set of parallel data*. EX1003, ¶76.

A POSITA would have understood that the controller is capable of generating a memory request when powered on, *i.e.*, *while the ASIC processor is under operating condition*. EX1003, ¶77.

[19f]

Different bit widths when an individual bus system corresponds to the first transmission bus

Lee's bus system 76 transmits **a first set of parallel data** with a **bit width** of 32 bits: "the four memory devices 70 together provide 32 bits for the 32-bit data buses." EX1004, [0016]; *see* FIG. 2; EX1003, ¶78.

In "high memory bandwidth" mode, Lee's high-speed link can be configured such that "a 128-bit data word may be coupled through the link 58" or to "couple 64-bit data words," *i.e.*, the **second set of parallel data** has a **bit width** of 128 or 64 bits. EX1004, [0017]; *see* [0019]; EX1003, ¶79. Either of these bit widths of the second set of parallel data—*e.g.*, 128 or 64 bits—is **different** from the 32-bit width of the first set of parallel data. EX1003, ¶79; *see* EX1004, claim 6.

Different bit widths when Lee's bus system 68 corresponds to the first transmission bus

Lee's "memory hub 60 addresses all of the memory devices 70 simultaneously" through bus system 68 "so that 128 bits of data are written to or read from the memory devices 70," *i.e.*, the **first set of parallel data** has a **bit width** of 128 bits. EX1004, [0017]; EX1003, ¶80.

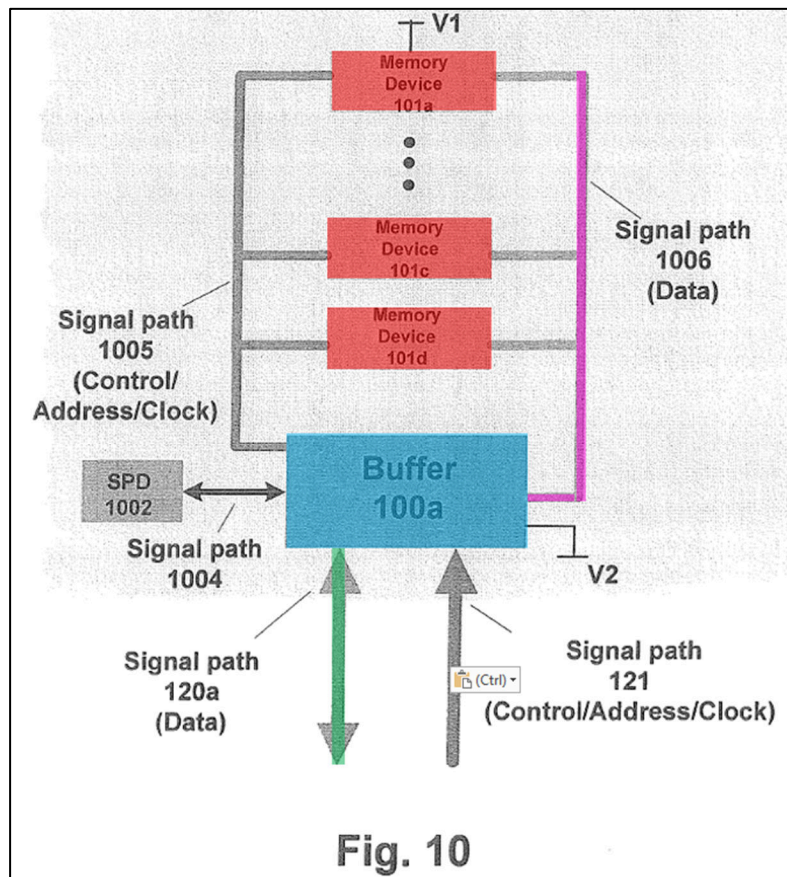
In "high memory bandwidth" mode, Lee's high-speed link can be configured to "couple 64-bit data words" or to "transfer only a 32-bit data word," *i.e.*, the **second set of parallel data** has a **bit width** of 64 or 32 bits. EX1004, [0017]; *see*

[0019]; EX1003, ¶81. Either of these bit widths of the second set of parallel data—*e.g.*, 64 bits or 32 bits—is *different* from the 128-bit width of the first set of parallel data. EX1003, ¶81.

B. GROUND 1B: Claims 19, 22, and 25-26 Are Obvious over Lee-Tsern

1. Tsern

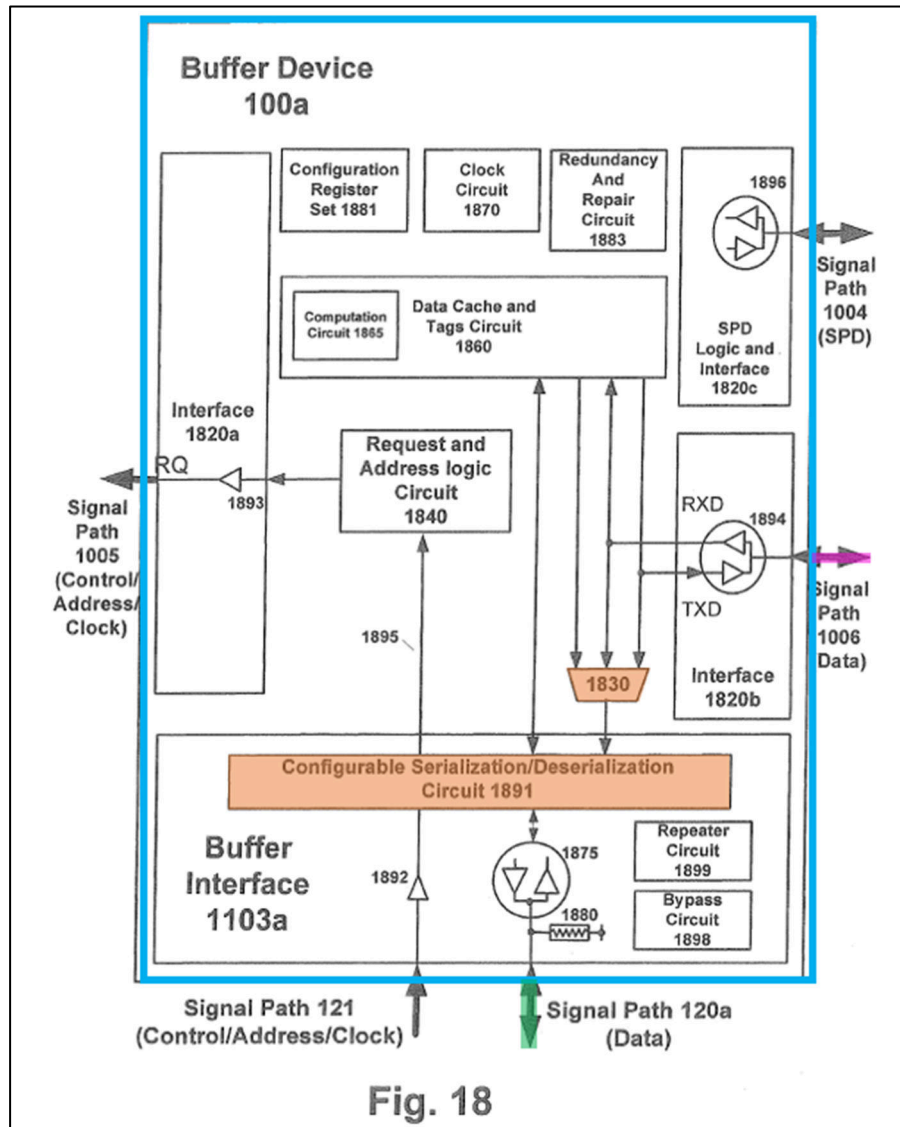
Like Lee, Tsern relates to a memory system having connections “between an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices.” EX1005, Abstract. The system (*see* Fig. 10, *infra*), includes “integrated circuit memory devices 101a-d [red] and a buffer 100a [blue],” with data transferred therebetween “on a signal path 1006,” pink. *Id.* A “signal path 120a,” green, “transfer[s] data” between the buffer and “a memory module connector interface.” *Id.*, 12; EX1003, ¶82.



Tsern, Fig. 10 (annotated)

An example buffer device 100a (*see* 18, *infra*) includes an interface 1820b “transfer[s] data between buffer 100a and one or more memory devices.” EX1005, 30, 32-33. The interface can “access different memory widths,” such as “16 ‘x4’ width memory devices, 8 ‘x8’ width memory devices or 4 ‘x16’ width memory devices.” *Id.*, 37. A multiplexer 1830 (orange) “perform[s] bandwidth-concentrating operations between buffer interface 100a and interface 1820b,” *e.g.*, “utiliz[ing] the combined bandwidth of multiple data paths [1006] coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” *Id.*,

33. The buffer interface 1103a, coupled to the signal path 120a to communicate data to a memory controller, includes a “[c]onfigurable serialization/deserialization circuit 1891,” orange, that “performs serialization and deserialization functions” on the data depending on “memory device access width.” *Id.*, 31, 38; EX1003, ¶83.



Tsern, Fig. 18 (annotated)

Another example buffer device 3600 “operates similar to buffer 100a” in that it receives “read data via one or more signal paths 1006” from memory devices and “transmits corresponding signals to a master.” EX1005, 68. This buffer device (*see* Fig. 36, *infra*) includes “data path 3606 and data path router 3610,” *orange*, that “merge separate read data from more than one memory device into a single merged read data or read stream output at interface 3601.” *Id.* The buffer device 3600 includes an “interface 3611” that has “at least three different configurations or segmentation modes: 1) Four 4-bit interfaces (4x4), 2) Two 4-bit interfaces (2x4) or 3) Two 8-bit interfaces (2x8),” which “allow[s] flexibility in memory module or memory stack configurations.” *Id.*, 69; EX1003, ¶84.

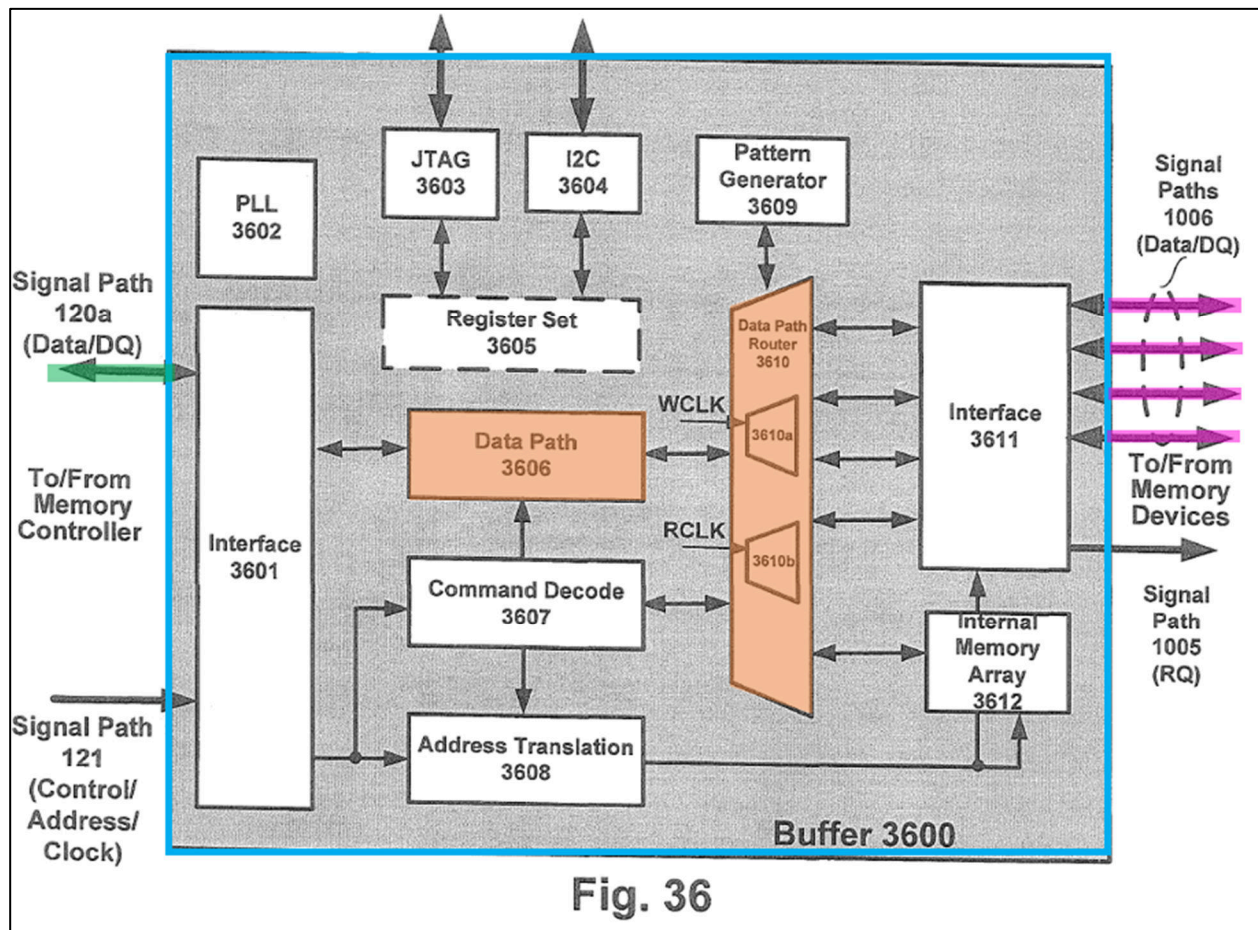
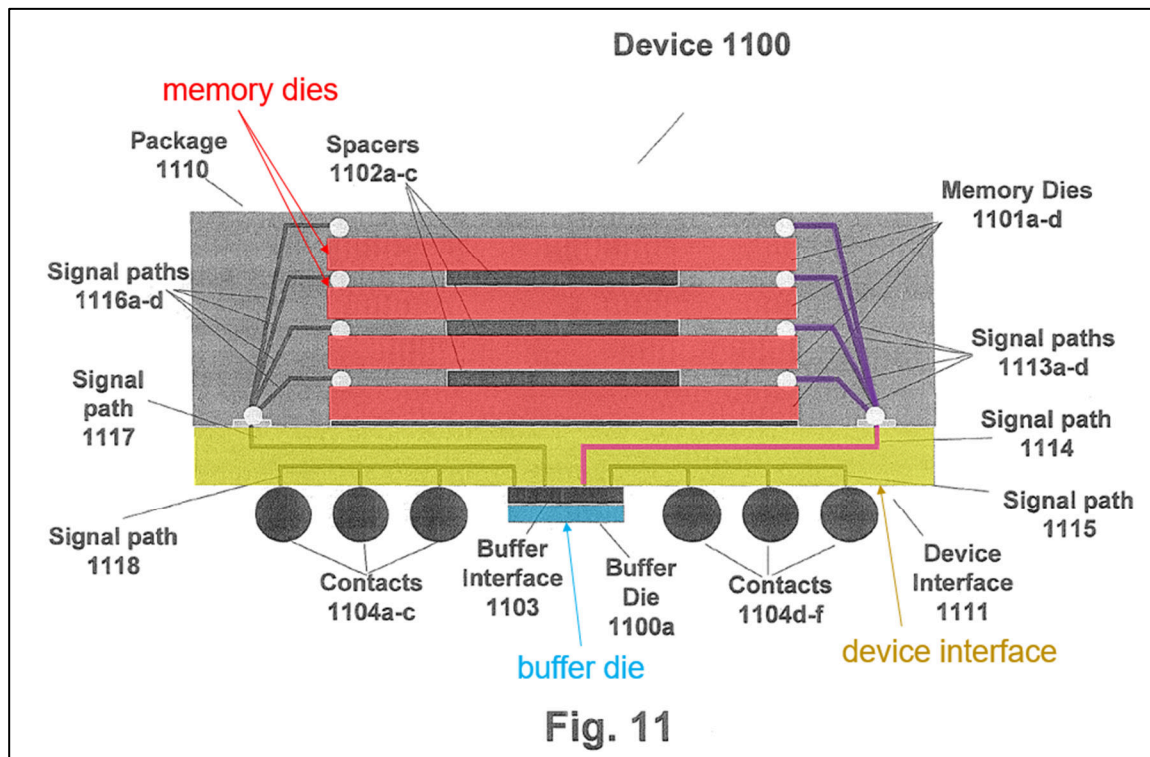


Fig. 36

Tsern, Fig. 36 (annotated)

Fig. 11, *infra*, shows a “stacked” package of IC memory dies and buffer die 1100a, e.g., one of the buffer devices 100a, 3600 discussed *supra*. EX1005, 26; EX1003, ¶85.



Tsern, Fig. 11 (annotated)

Tsern is analogous art to the '942 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1005, Abstract, 6; EX1003, ¶¶86-87.

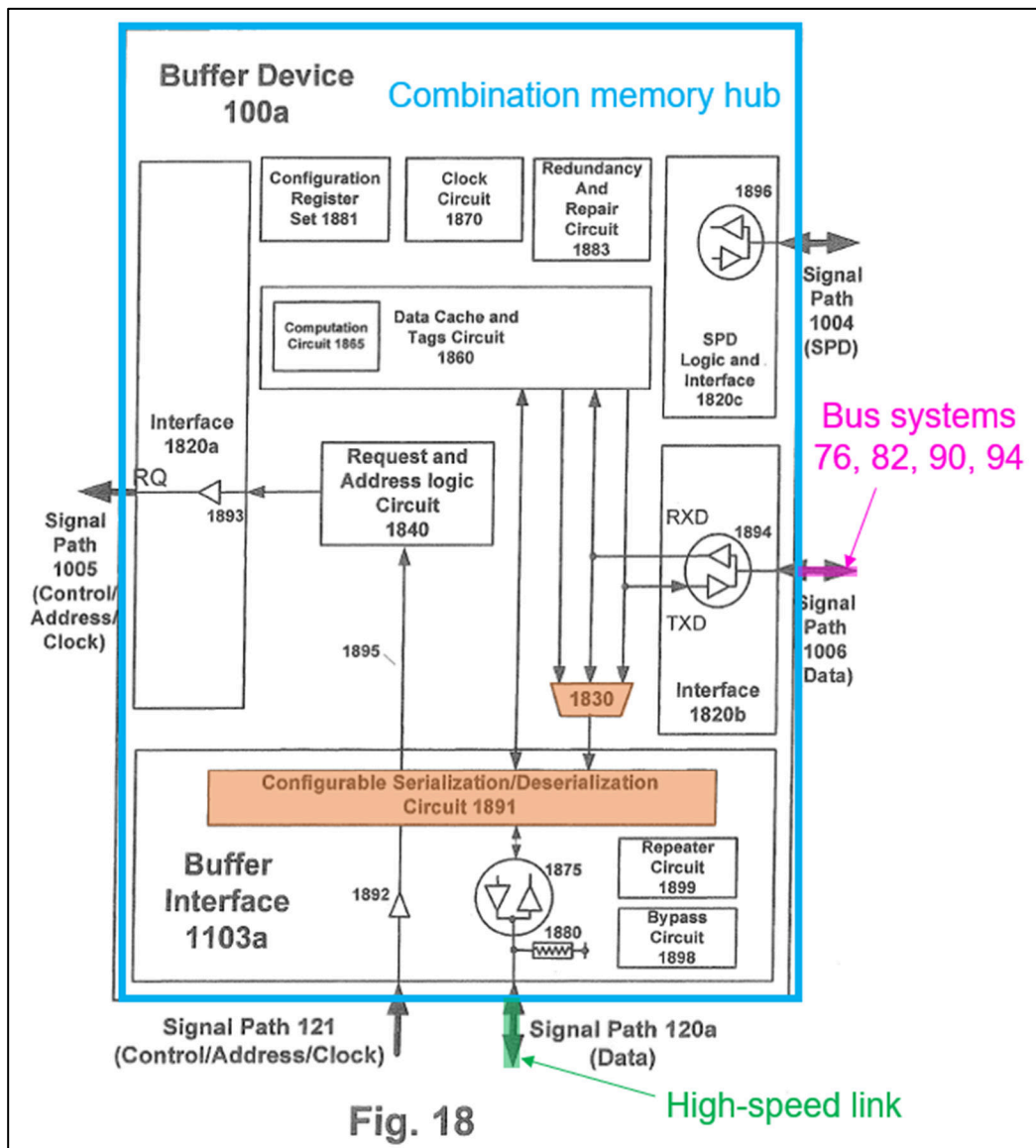
2. The Lee-Tsern Combination

The Lee-Tsern system is based on Lee's memory system. EX1003, ¶88. Four ranks of memory devices 70 are coupled to the memory hub 60 through a respective bus system. *See* EX1004, [0016]. The memory hub is also coupled to a memory controller through a "high-speed link 58." *Id.* The memory system is operable in "high memory bandwidth" or "high memory depth" mode. EX1004,

[0017]; EX1003, ¶88. The combination memory hub is implemented as an “integrated circuit buffer device” based on Tsern’s buffer device 100a or 3600.

See EX1005, Abstract, 12, 30, Fig. 11, Fig. 18; EX1003, ¶89.

In one example of the combination, illustrated *infra*, the memory hub is implemented based on Tsern’s buffer device 100a. *See* EX1005, 12, 30, Abstract, Fig. 18; EX1003, ¶90.



Lee-Tsern figure based on Tsern, Fig. 18

Tsern's buffer device 100a includes a buffer interface 1103a coupling the buffer device to a memory controller a signal path 120a, similar to Lee's high-speed link 58 coupling the memory hub to the controller 52. *See* EX1005, 22, 30-31; EX1004, [0015]-[0016], FIG. 2. Based on similarity, the combination memory hub has a buffer interface that couples the memory hub to the controller via the

high-speed link 58 (green *supra*). *See* EX1004, [0015]-[0016], FIG. 2; EX1003, ¶91.

Tsern's buffer device 100a also includes an "[i]nterface 1820b" "coupled to signal path 1006 to transfer data between buffer 100a and one or more memory devices 101a-d." EX1005, 32-33. The "number of ... data signal lines between buffer 100a and memory devices 101a-d are programmable in order to accommodate different numbers of memory devices." *Id.*, 37. Based on these teachings, the combination memory hub has an interface that is coupled to the bus systems 76, 82, 90, 94 of the combination to transfer data between the memory hub and the memory devices. *See* EX1004, [0016], FIG. 2; EX1003, ¶92.

Other aspects of the combination memory hub are implemented based on Tsern. EX1003, ¶93. For instance, a "multiplexer 1830 [orange] may perform bandwidth-concentrating operations," allowing the buffer to "utilize[] the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a," *e.g.*, enabling implementation of high memory bandwidth mode. *EX1005*, 33; *see* EX1004, [0017]; EX1003, ¶93. The combination memory hub also has a "[c]onfigurabe serialization/deserialization circuit 1891" (orange) that provides "an access interleaving or multiplexing scheme ... to ensure that all storage locations within memory devices 101a-d can be accessed." EX1005, 38; EX1003, ¶93.

In an alternative example of the combination, illustrated *infra*, the memory hub is implemented based on Tsern's integrated circuit buffer device 3600. See EX1005, 68, Fig. 36; EX1003, ¶¶94.

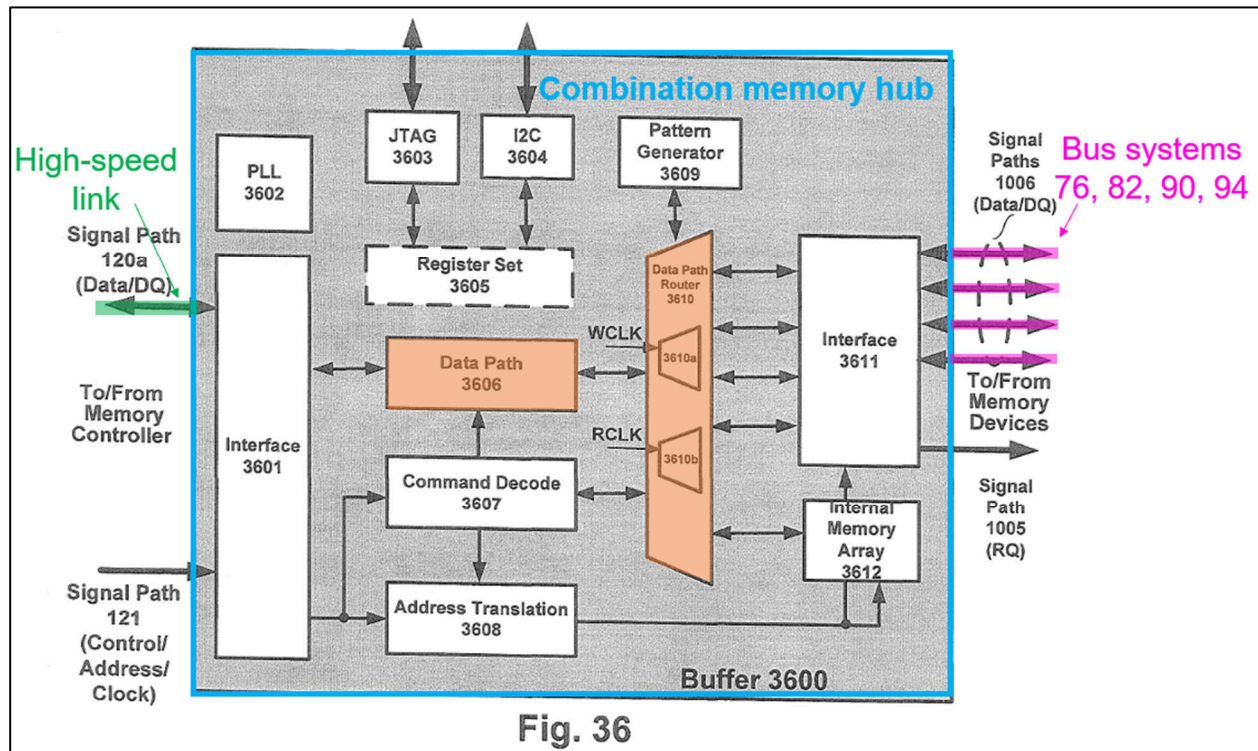


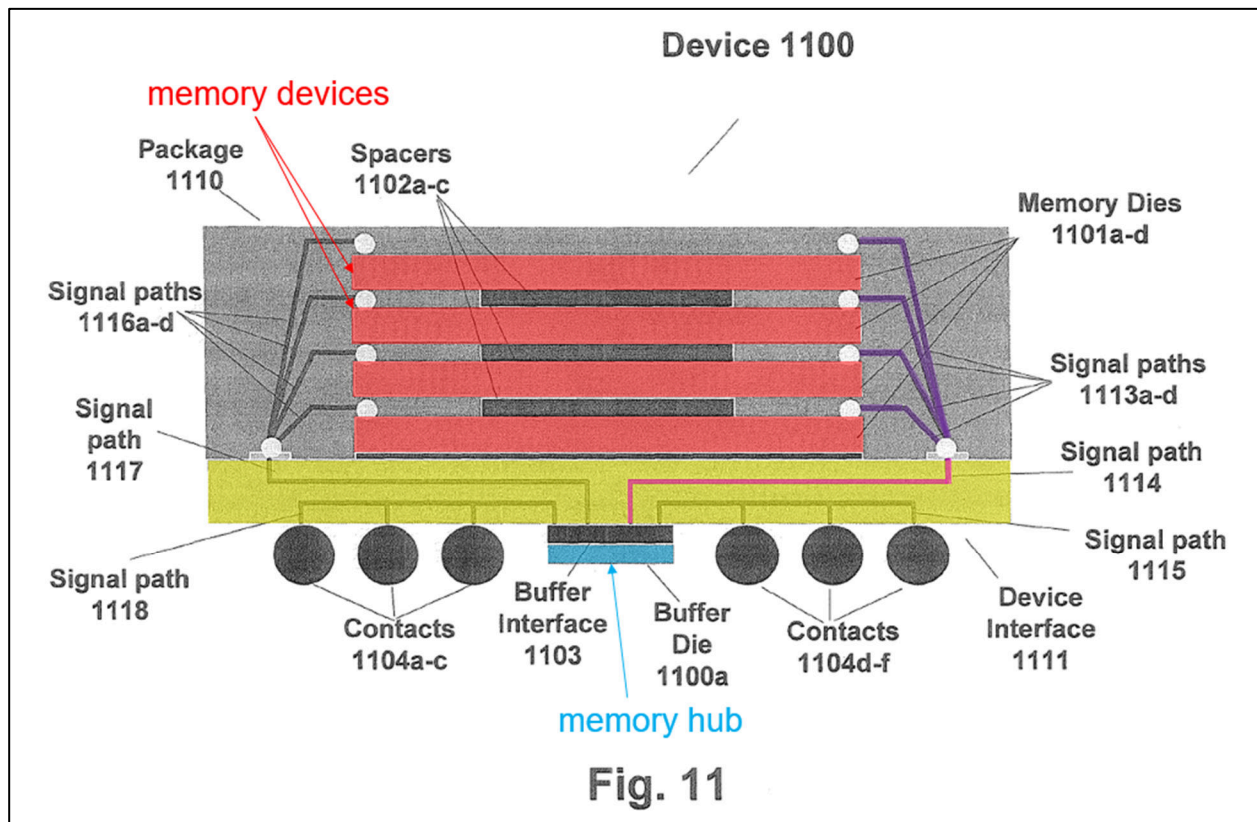
Fig. 36

Tsern, Fig. 36 (annotated)

This combination memory hub includes “interfaces 3601 and 3611” to communicate data between, respectively, the memory hub and a memory controller via the combination high-speed link (green *supra*), and between the memory hub and the ranks of memory devices via bus systems 76, 82, 90, 94 (pink *supra*). EX1005, 67; see EX1004, [0016]-[0020], FIG. 2; EX1003, ¶¶95-96. Based on Tsern, the combination memory hub includes “data path 3606 and data path router

3610,” orange *supra*, that “merge separate read data from more than one memory device” into a single merged read data or read stream output,” for output onto the high-speed link. EX1005, 68; *see* EX1004, [0016]-[0020], FIG. 2; EX1003, ¶¶95-96. The data path router includes “signal paths used to merge read data from different memory devices as well as parse write data into write data portions to be stored in multiple memory devices.” EX1005, 71; EX1003, ¶97..

Optionally, in the combination, the memory devices (red *infra*) of at least one of the ranks are arranged “stacked” on a top surface of a “device interface 1111” (yellow), and the memory hub IC (blue) is disposed on the opposite surface of the device interface. EX1005, 26, Fig. 11; EX1003, ¶98.



Lee-Tsern figure based on Tsern, Fig. 11

3. Motivation for the Combination and Expectation of Success

Motivation for implementing functionality of Tsern's buffer device in the combination memory hub

A POSITA would have been motivated to implement the combination
memory hub to have functionality based on embodiments of Tsern's buffer devices
as follows. EX1003, ¶¶99-101.

First, a POSITA would have been motivated to implement Lee’s memory hub based on Tsern’s teachings of similarly situated buffer devices because doing so is a mere implementation detail for a feature—the implementation of a memory

hub—that that is not described in detail by Lee. EX1003, ¶100; *see KSR*, 550 U.S. at 421 (“A person of ordinary skill is also a person of ordinary creativity, not an automaton.”). Both Lee’s memory hub and Tsern’s buffer device receive a first set of parallel data from multiple memory devices along multiple bus systems, and transmits that received data as a second set of parallel data along a single bus to a controller. *See* [19c]-[19d] of Ground 1A. Given this similarity, a POSITA would have looked to Tsern for implementation details. EX1003, ¶100.

Second, this implementation is merely the application of known techniques (*e.g.*, a specific implementation of a memory hub that converts a received set of parallel data to a transmitted set of parallel data) to a known structure (*e.g.*, the memory hub in Lee’s memory system) to yield predictable results (*e.g.*, a memory hub implementing elements enabling conversion of a received set of parallel data to a transmitted set of parallel data). EX1003, ¶101; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success in pursuing this implementation because memory system technology is predictable, and because the location and functionality of the buffer devices in Tsern’s memory system is generally consistent with that of the memory hub in Lee’s memory system. *See* EX1004, [0009], [0015]-[0020], FIG. 2; EX1005, Figs. 11, 18, 36; EX1003, ¶102.

Motivation for implementation of the memory hub as an IC

A POSITA would have been motivated to implement the memory hub as an IC as follows. EX1003, ¶¶103-107.

First, implementing a memory hub of a memory cell array system as an IC was conventional, and compatible with conventional processes and structures. EX1003, ¶104 (citing EX1009, 1; EX1016, 6:53-54, Fig. 18).

Second, implementation of a memory hub as an IC is smaller, more efficient, and less expensive than implementation of the memory hub functionality through a circuit composed of discrete components. *See* EX1022, 1:15-18; EX1003, ¶105.

Third, implementing the combination memory hub as an IC is a mere implementation detail for a feature—the specific nature of the memory hub—that that is not specified by Lee. EX1003, ¶106; *see KSR*, 550 U.S. at 421.

Fourth, this implementation is merely the application of known techniques (*e.g.*, implementation of a memory hub as an IC) to a known structure (*e.g.*, the combination memory hub) to yield predictable results (*e.g.*, an IC memory hub). EX1003, ¶107; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success in implementing the memory hub as an IC because this was a conventional approach to implementation of memory hubs. *See* EX1009, 1; EX1016, 6:53-54; EX1003, ¶108.

Motivation for a stacked arrangement of ICs

A POSITA would have been motivated to implement a stacked arrangement of memory devices and memory hub because (1) in the stacked arrangement based on Tsern, the memory hub “is disposed away from” the memory devices “to alleviate heat dissipation near the memory devices (EX1005, 26); (2) stacking of chips allows for “integrating more devices into a smaller volume,” which enables performance advantages such as smaller size, shorter signal distance, and lower wiring density (EX1009, 1); and (3) it is merely the application of known techniques (a particular arrangement of chips in a memory module) to a known system (Lee’s memory chips and memory hub) to yield predictable results (a memory module in which memory chips are stacked above the memory hub). EX1003, ¶¶109-112; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success in implementing a stacked chip arrangement because semiconductor packaging technology is predictable and because a stacked package of memory and logic chips was conventional. *See, e.g.*, EX1009, 1; EX1016, Fig. 18; EX1003, ¶113.

4. Analysis

(a) Claim 19

[19pre]-[19c]

See [19pre]-[19c] of Ground 1A, *supra*. EX1003, ¶¶114-115.

[19d]

The Lee-Tsern system includes a *second set of parallel data* carried on Lee's high-speed link 58 (*second transmission bus*). Also in the combination, the memory hub 60 (*logic unit*) *transmits the second set of parallel data to the ASIC processor*, based on Lee. See [19d] of Ground 1A. EX1003, ¶116.

Tsern's buffer device 100a renders obvious parallel-to-parallel conversion

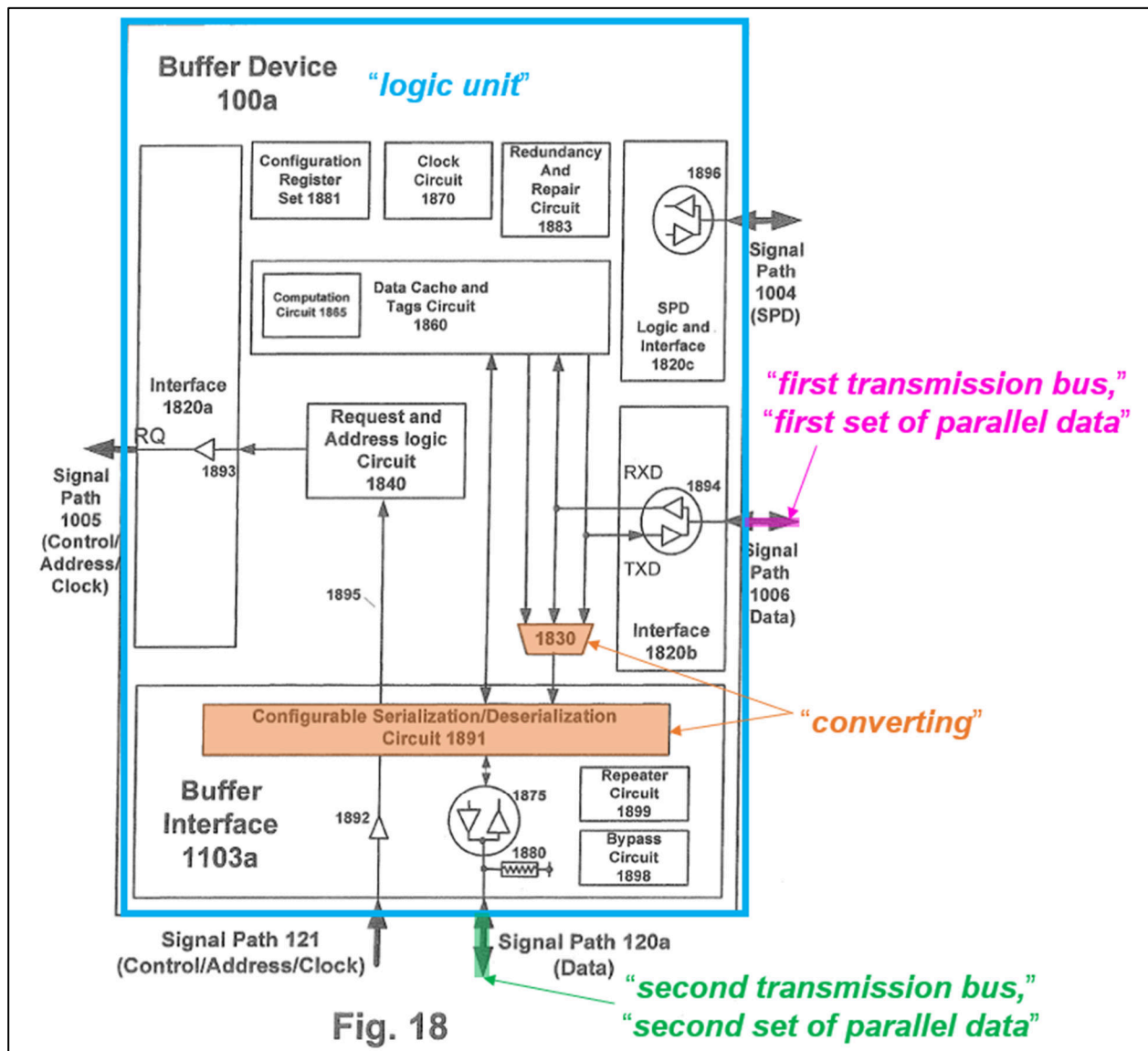
In one example, the combination memory hub (*logic unit*) is implemented based on Tsern's buffer device 100a. EX1003, ¶117.

In Tsern, data are communicated between the buffer device and a memory controller via a signal path 120a. See EX1005, 12, 14-15. The "buffer interface 1103a has a programmable width for signal path 120a." *Id.*, 38. Based on this disclosure, a POSITA would have understood that the signal path 120a carries *parallel data*, i.e., data of width greater than one bit. EX1003, ¶118.

Also in Tsern, data are communicated between buffer device 100a and memory devices via "signal paths 1006." EX1005, 38. The interface 1820b, which connects to the signal paths 1006 (see Fig. 18), "may be programmed to connect to 16 'x4' width memory devices, 8 'x8' width memory devices or 4 'x16' width memory devices." *Id.*, 37. Based on this disclosure, a POSITA would have understood that each signal path 1006 carries *parallel data*, e.g., 4-, 8-, or 16-bit width data from those memory devices. EX1003, ¶119.

Tsern's buffer device 100a ***converts*** the parallel data from the multiple signal paths 1006 to parallel data for the single signal path 120a through a “configurable serialization/deserialization circuit 1891,” which “performs serialization and deserialization functions,” and through a “multiplexer 1830,” which “utilizes the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” EX1005, 33, 38; EX1003, ¶120.

In the combination, illustrated *infra*, the memory hub (***logic unit***) is implemented based on the parallel-to-parallel capability of Tsern's buffer device 100a. EX1003, ¶121. Specifically, the combination memory hub communicates a ***first set of parallel data*** to/from memory devices via bus systems 76, 82, 90, 94 (pink), and communicates a ***second set of parallel data*** to/from a memory controller via high-speed bus 58 (green). *See* [19c]-[19d] of Ground 1A; EX1003, ¶121. Elements of the combination memory hub, including a configurable serialization/deserialization circuit 1891 and a multiplexer 1830 (orange *infra*), ***convert the first set of parallel data into a second set of parallel data***, consistent with Tsern. EX1003, ¶122.



Lee-Tsern figure based on Tsern, Fig. 18

Tsern's buffer device 3600 renders obvious parallel-to-parallel conversion

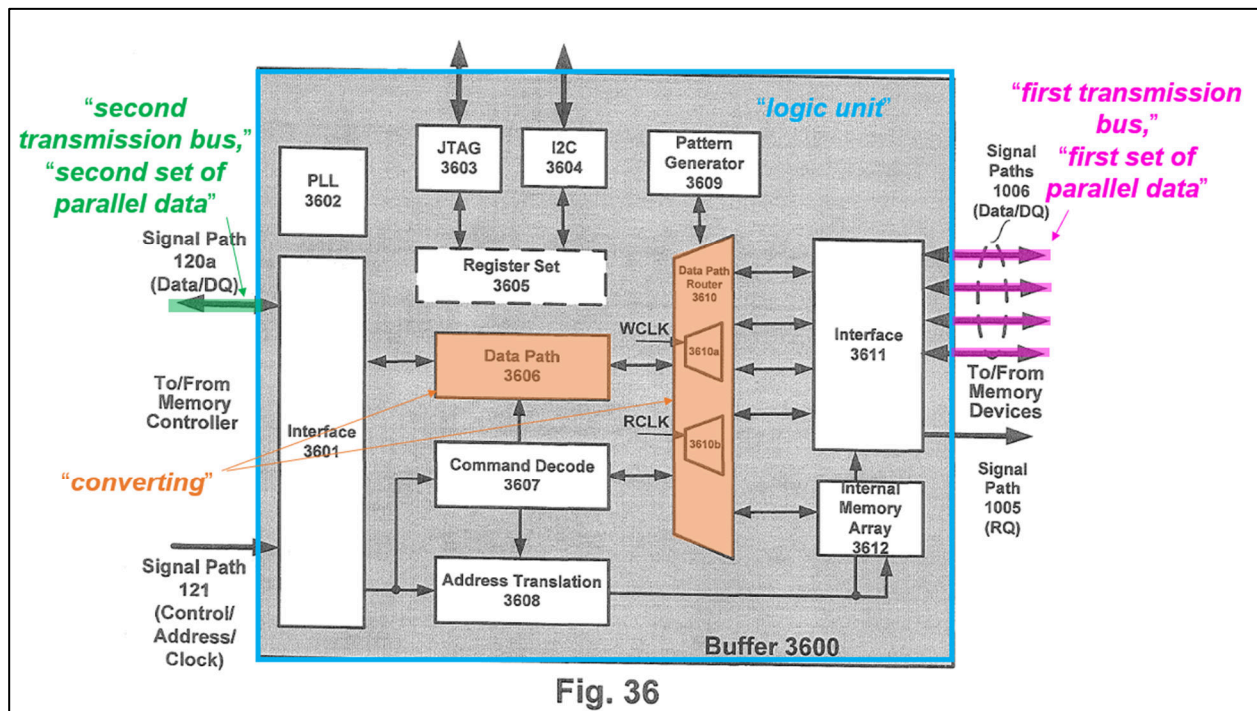
In alternative/additional example, the combination memory hub (*logic unit*) is implemented based on Tsern's buffer device 3600. EX1003, ¶123.

In Tsern, data are communicated between the buffer device and a memory controller via a signal path 120a, which carries *parallel data*, discussed *supra*.

EX1005, 68. Data are also communicated between the buffer device 3600 and memory devices via “signal paths 1006,” each of which carries *parallel data*, discussed *supra*. EX1005, 68; EX1003, ¶124.

Tsern’s buffer device 3600 *converts* the parallel data from the multiple signal paths 1006 to parallel data output through interface 3601 onto the single signal path 120a through a “data path 3606 and data path router 3610,” which “merge separate read data from more than one memory device into a single merged read data or read stream output at interface 3601.” EX1005, 36; EX1003, ¶125.

In the combination, illustrated *infra*, the memory hub (*logic unit*) is implemented based on the parallel-to-parallel capability of Tsern’s buffer device 3600. EX1003, ¶126. Specifically, the combination memory hub communicates a *first set of parallel data* to/from memory devices via bus systems 76, 82, 90, 94, and communicates a *second set of parallel data* to/from a memory controller via high-speed bus 58 (green). *See* [19c]-[19d] of Ground 1A, *supra*; EX1003, ¶126. Elements of the combination memory hub, including “data path 3606 and data path router 3610” (orange *infra*), *convert* (“merge”) *the first set of parallel data into a second set of parallel data*, consistent with their operation as disclosed by Tsern, discussed *supra*. EX1005, 68; EX1003, ¶127.



Lee-Tsern figure based on Tsern, Fig. 36

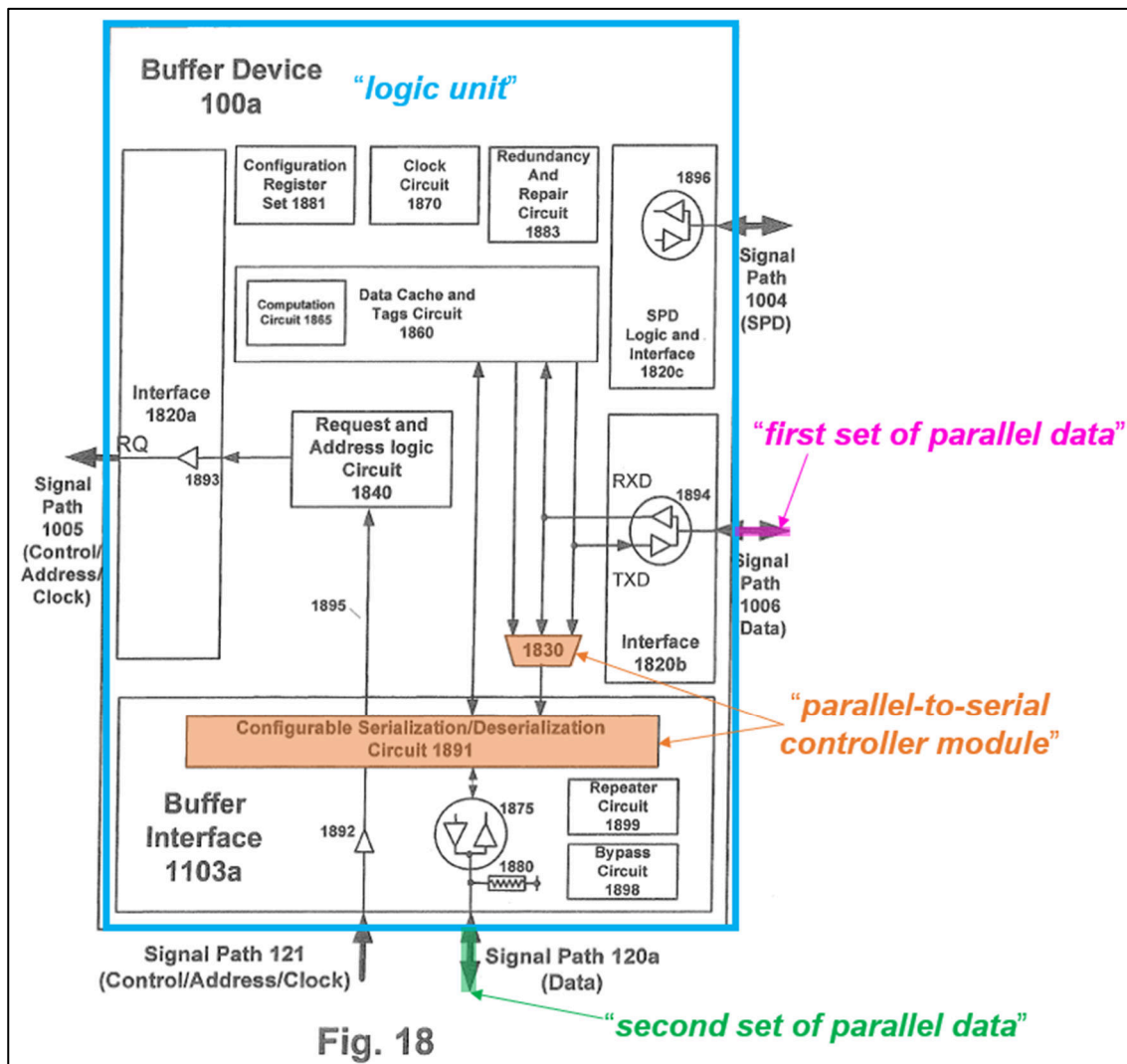
[19e]-[19f]

See [19e]-[19f] of Ground 1A. EX1003, ¶128.

(b) Claim 22

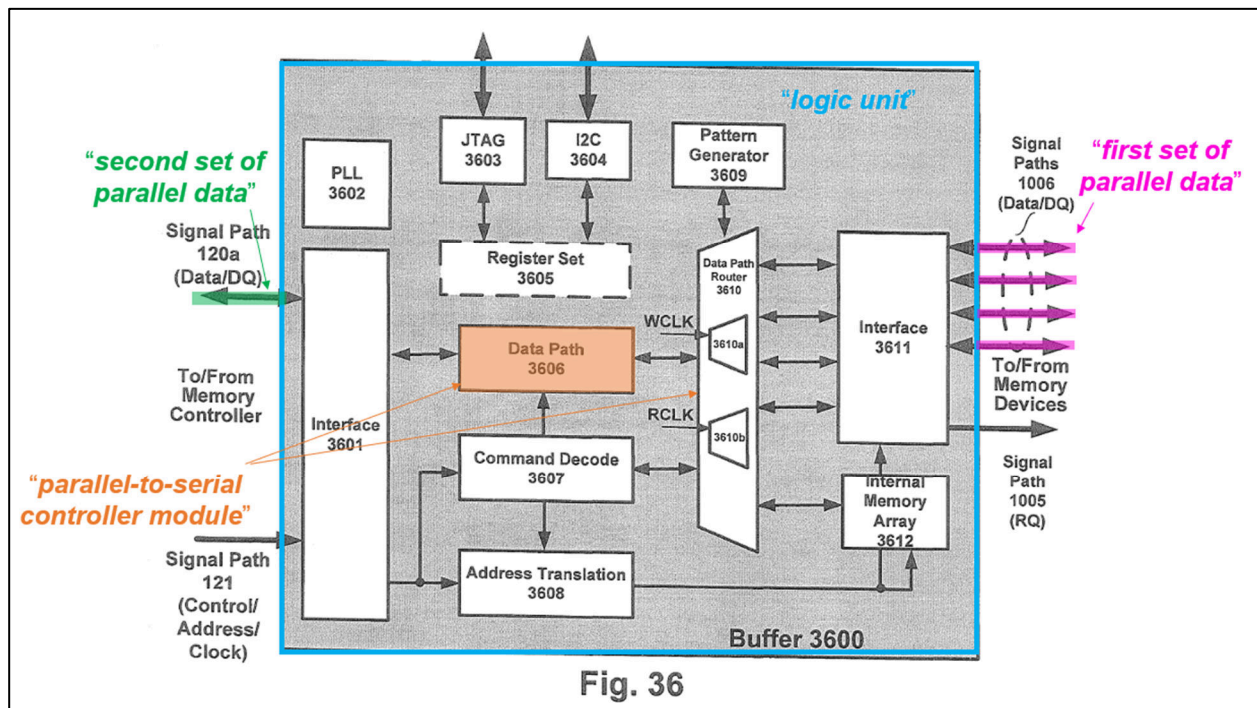
[22]

When the combination memory hub is implemented based on Tsern's buffer device 100a, the serialization/deserialization circuit 1891 and a multiplexer 1830 (orange *infra*) together correspond to *a parallel-to-serial controller module*, e.g., because they control conversion of the first set of parallel data into the second set of parallel data. See EX1005, 33, 38; EX1003, ¶129.



Lee-Tsern figure based on Tsern, Fig. 18

Alternatively/additionally, when the memory hub is implemented based on Tsern's buffer device 3600, Tsern's data path 3606 and data path router 3610 (orange *infra*) correspond to **a parallel-to-serial controller module**, e.g., because they control conversion of the first set of parallel data into the second set of parallel data. See EX1005, 68; EX1003, ¶130.



Lee-Tsern figure based on Tsern, Fig. 36

(c) **Claim 25**

[25]

In the combination, Lee describes that in the “high memory bandwidth” mode, “the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access.” EX1004, [0017]. That is, the data rate of the first transmission bus (*i.e.*, the bus system 68 including the four individual bus systems 76, 82, 90, 94) in high memory bandwidth mode is 128 bits per memory access. EX1003, ¶¶131-132. Lee also describes that alternatively, in “high memory depth mode, only one rank 74, 80, 86, 88 may be addressed at a time,” such that “only 32 bits of

data will be coupled to or from the memory module 54 with each memory access.”

Id. That is, the data rate of the first transmission bus (*i.e.*, the bus system 68 including the four individual bus systems 76, 82, 90, 94) in high memory depth mode is 32 bits per memory access. EX1003, ¶¶131-132.

Lee’s system can be “configure[d]” to operate in high memory bandwidth or high memory depth mode. EX1004, [0017]; *see* [0019] (“By allowing the memory hub 60 to configure the data format of the memory module 54, the data format can be optimized for a particular application being executed ... The data format is therefore not fixed as in conventional memory systems”); EX1003, ¶133. When the system operates, *e.g.*, in high memory bandwidth mode for a given instance of writing data (128 bits per memory access) (***transmitting data rate of the first transmission bus***), and in high memory depth mode for a different instance of reading data (32 bits per memory access) (***receiving data rate of the first transmission bus***), the ***transmitting data rate and receiving data rate of the first transmission bus are different.*** EX1003, ¶134.

(d) **Claim 26**

[26]

In the combination, Lee describes that “[i]n the high memory depth mode, the high-speed link 58 can operate at a slower data rate than in the high bandwidth mode,” *i.e.*, the ***data rate of the second transmission bus*** differs based on the

mode of operation. EX1004, [0018]. As discussed *supra*, Lee's system can be "configure[d]" to operate in high memory bandwidth or high memory depth mode. EX1004, [0017]; *see* [0019]; EX1003, ¶135. When, for instance, the system is configured for high memory bandwidth mode for a given instance of writing data, and is configured in high memory depth mode for a different instance of reading data, the reading is performed at "slower data rate" than the writing, *i.e.*, the ***transmitting data rate and receiving data rate of the second transmission bus are different***. EX1003, ¶¶135-136.

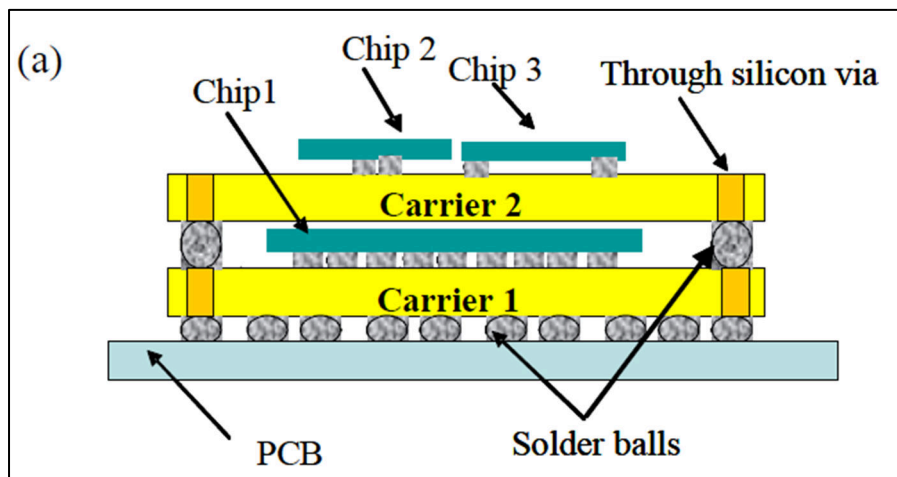
Alternatively/additionally, in the combination, Lee describes that in the "high memory bandwidth" mode, "the high-speed link 58 may couple data at a rate of 2 GB/sec," or "may couple 64-bit data words at a rate of 1 GB/sec," *i.e.*, the high-speed link (***second transmission bus***) can be operated at different data rates. EX1004, [0017]. These data rates are applicable when data "are written to or read from" the memory devices 70, *i.e.*, they can be either transmitting data rates or receiving data rates. *Id.*; EX1003, ¶137. As discussed *supra*, Lee's system can be "configure[d]" to operate in a certain mode. *See* EX1004, [0017], [0019]; EX1003, ¶137. When the system operates such that the high-speed link has one data rate (*e.g.*, "a rate of 2 GB/sec") for a given instance of writing data (***transmitting data rate of the second transmission bus***), and a different data rate (*e.g.*, "a rate of 1 GB/sec") for a different instance of reading data (***receiving data***

rate of the second transmission bus), the transmitting data rate and receiving data rate of the second transmission bus are different. EX1003, ¶137.

C. GROUND 1C: Claim 21 Is Obvious Over Lee-Tsern-Khan

1. Khan

Khan describes a “3D stacked package with silicon interposers” that “integrate[s] one ASIC and two memory chips in a package.” EX1009, 1. Carrier 1 houses “(Chip 1) representing an ASIC device,” and Carrier 2 “house[s] two memory chips,” Chips 2 and 3. EX1009, 1; *see* Fig. 1(a), *infra*; EX1003, ¶¶138-139.

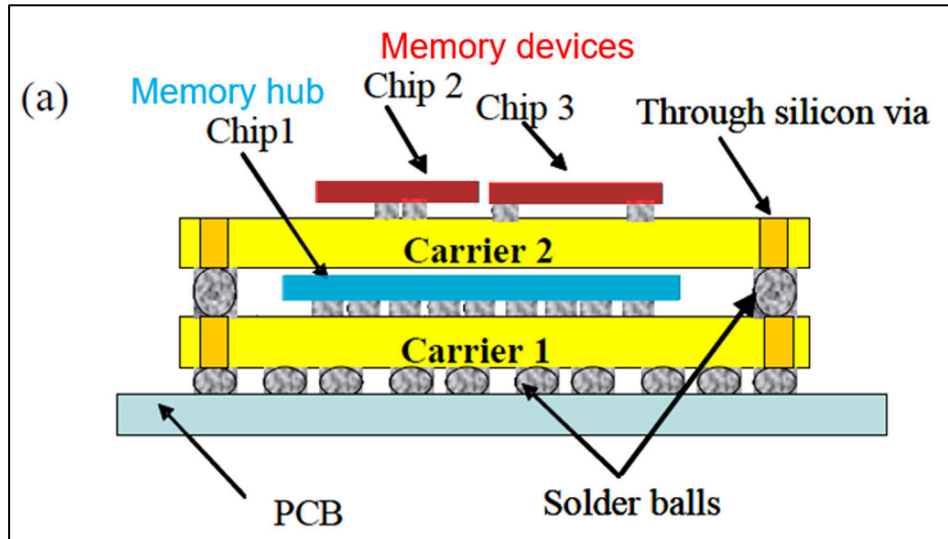


Khan, Fig. 1(a)

Khan is analogous art to the '942 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1009, Abstract; EX1003, ¶¶140-141.

2. The Lee-Tsern-Khan Combination

In the combination, the memory hub IC and at least one rank of memory devices are assembled into a 3D stack based on Khan, illustrated *infra*. EX1003, ¶142.



Lee-Tsern-Khan figure based on Khan, Fig. 1(a)

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to stack the memory devices and memory hub because (1) First, stacking of chips allows for “integrating more devices into a smaller volume,” enabling performance advantages including “smaller footprint, shorter signal routing, reduced wiring density”; (2) this structure “removes the heat effectively” from the chips; and (3) it is merely the application of known techniques (stacked chips in a memory module) to a known structure (a memory module including memory device and memory hub chips) to

yield predictable results (a memory module in which memory chips and memory hub are stacked with a silicon interposer). EX1009, 1; EX1003, ¶¶143-147; *see KSR*, 550 U.S. at 417. A POSITA would have been motivated to use a silicon interposer because of performance advantages provided by silicon, including thermal conductivity, low stress, and fine line width capability. *See* EX1009, 1; EX1003, ¶146.

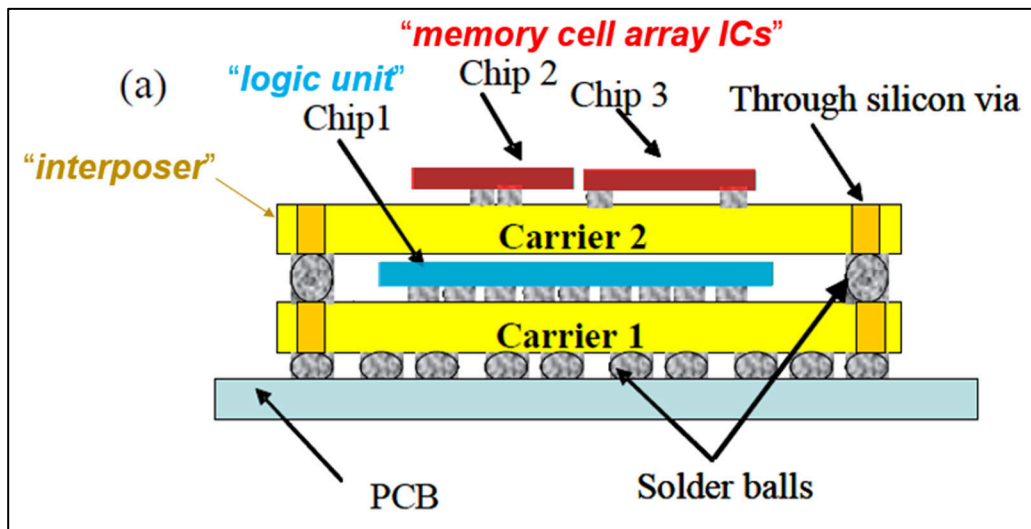
A POSITA would have expected success because semiconductor packaging technology is predictable and because a stacked package of memory and logic chips was conventional. *See, e.g.*, EX1005, Fig. 11; EX1016, Fig. 18; EX1023, FIG. 2; EX1003, ¶148.

4. Analysis

(a) Claim 21

[21a]

In the combination, the memory devices (*memory cell array ICs*) and memory hub (*logic unit*) are arranged in a “3D stack package,” based on Khan, illustrated *infra*. EX1009, 1, Fig. 1(a); EX1003, ¶¶149-150. The memory hub is housed on a first carrier, and the memory devices are housed on a second carrier (*interposer*), *yellow infra, i.e.*, the *memory cell array ICs are disposed over the interposer* and *the interposer is disposed over the logic unit*. EX1003, ¶150.



Lee-Tsern-Khan figure based on Khan, Fig. 1(a)

[21b]

The interposer is a "silicon interposer." EX1009, 1; EX1003, ¶151.

D. GROUND 1D: Claim 20 Is Obvious Over Lee-Tsern-Khan-Dozen

1. Dozen

Dozen describes manufacturing memory devices. *See* EX1007, Abstract, 4:9-26. Dozen describes that "where a plurality of semiconductor devices are included in the element substrate 1102, the plurality of semiconductor devices may be obtained by dividing the element substrate and the sealing layers," *e.g.*, by "laser cutting." EX1007, 11:60-67; EX1003, ¶152.

Dozen is analogous art to the '942 Patent: it is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1007, Abstract; EX1003, ¶153.

2. The Lee-Tsern-Khan-Dozen Combination

In the combination, memory devices are “formed in [an] element substrate,” and individual memory device chips are obtained from the substrate “by “laser cutting.” EX1007, 4:9-26, 11:60-67; EX1003, ¶154.

3. Motivation to Combine

A POSITA would have been motivated to employ laser dicing of the memory devices because (1) it enables high degrees of precision to be achieved at high processing speeds; (2) it is a contactless processing method, and thus does not subject tools to wear, generates little waste, and does not run significant risks of contamination; (3) it is one of a finite number of predictable solutions (*e.g.*, laser dicing, physical dicing, scribing), and with a reasonable expectation of success (discussed *infra*); and (4) it is merely the application of known techniques (laser dicing of ICs) to a known structure (Lee’s memory chips) to yield predictable results (memory chips separated by a laser dicing process). EX1003, ¶155-159 (citing EX1020, Abstract, 7:9-11; EX1021, 1:6-9, 1:22-32); *see KSR*, 550 U.S. at 417, 421.

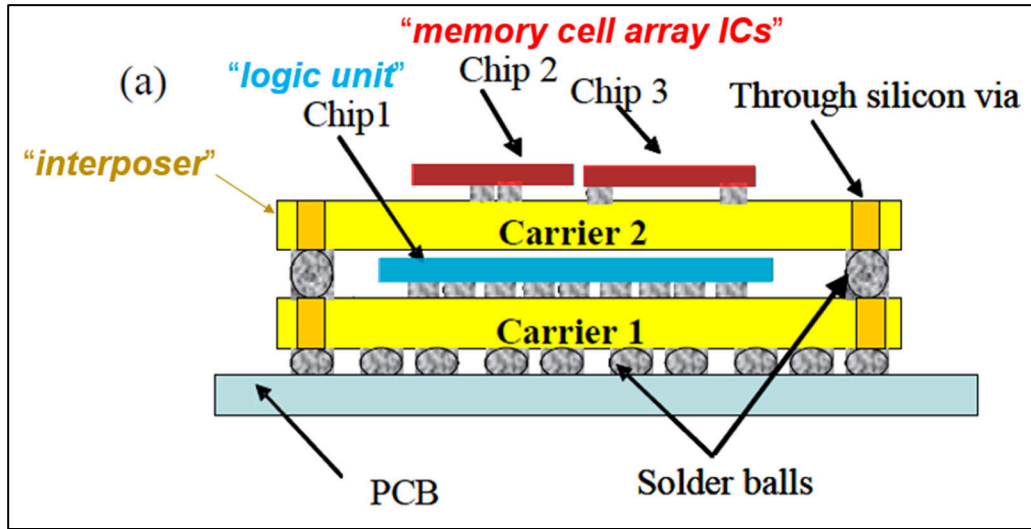
A POSITA would have expected success because memory system technology and IC dicing technology are predictable, and because laser dicing of ICs was conventional. *See, e.g.*, EX1020, Abstract; EX1021, 1:6-9; EX1003, ¶160.

4. Analysis

(a) Claim 20

[20a]

In Lee-Tsern-Khan-Dozen, at least one of the memory devices (*memory cell array ICs*) and the memory hub (*logic unit*) are *disposed over two opposite sides* of the second carrier (*interposer*), as illustrated *infra*. See [21a]; EX1009, 1, Fig. 1(a); EX1003, ¶¶161-162.



Lee-Tsern-Khan based on Khan, Fig. 1(a)

[20b]

See [21b]. EX1003, ¶163.

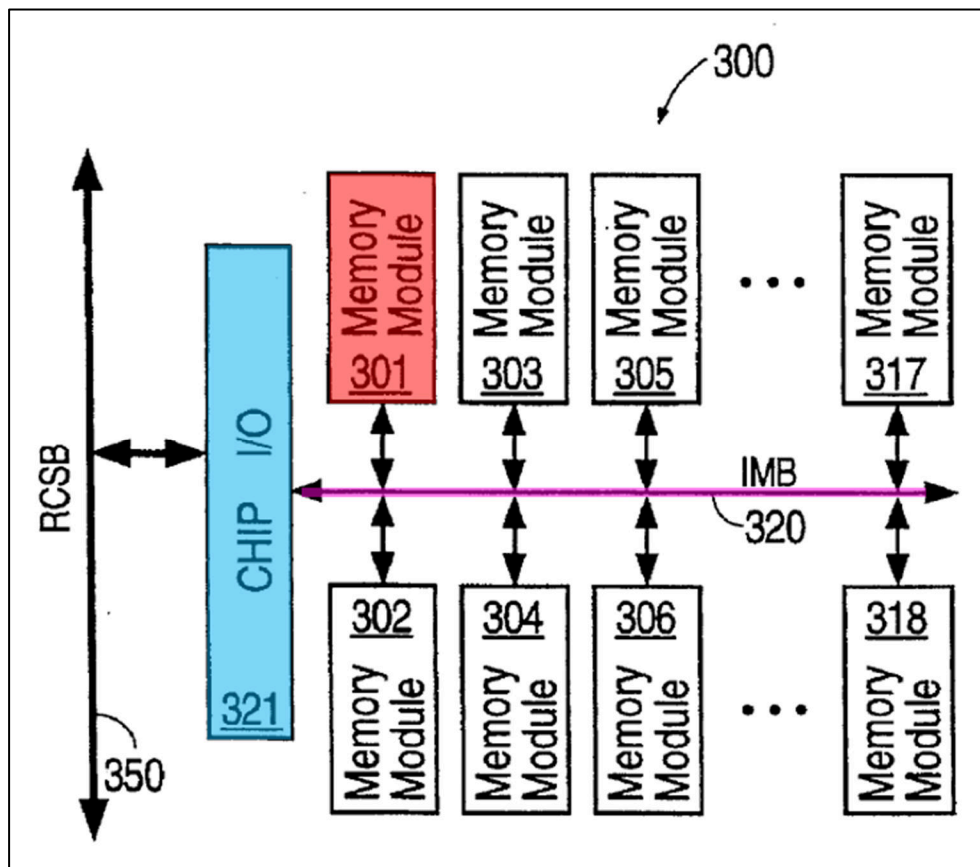
[20c]

In the combination, a substrate is divided into individual memory devices (*memory cell array ICs*) by "laser cutting" (*a dicing method comprises a laser cutting process*), based on Dozen. EX1007, 11:60-67; EX1003, ¶164.

E. GROUND 1E: Claims 23-24 Are Obvious Over Lee-Tsern-Leung

1. Leung

Leung describes a memory system including “multiple memory modules [red in FIG. 3, *infra*] coupled to a chip I/O interface [blue] through an internal bus [pink].” EX1008, Abstract; EX1003, ¶165.



Leung, FIG. 3 (annotated)

The internal memory bus that “communicate[s] between the module bus interface (MBI) and the chip I/O “employs ... Directionally Asymmetric Signal Swing (DASS).” EX1008, 10:25-35. Specifically, “[l]arge signal swing is used in

the point-to-multiple destinations mode, when master is driving the bus, while small swing is used in the point-to-point mode when one of many memory devices drives the bus.” *Id.*, 11:3-7; *see* 10:66-11:3; EX1003, ¶¶166-167.

To implement Leung’s asymmetrical signal swing, “the chip I/O drives the IMB with full CMOS swing” using “normal CMOS inverters” for communication from chip I/O to memory modules. EX1008, 11:52-54. In reverse, “the MBI drives the IMB with a reduced signal swing” by “clamp[ing]” the signal swing “by the receiving circuitry in the chip I/O.” *Id.*, 11:52-58; *see* FIG. 8; EX1003, ¶168.

Leung is analogous art to the ’942 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the ’942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1008, Abstract, 2:5-63; EX1003, ¶¶169-170.

2. The Lee-Tsern-Leung Combination

The teachings of Leung regarding asymmetrical signal swing are integrated into the Lee-Tsern-Leung system. *See* EX1008, 2:59-60, 10:66-11:3; EX1003, ¶171. Specifically, Lee’s bus systems 76, 82, 90, 94 connecting the memory hub to memory devices are examples of a “master-slave communication environment.” EX1003, ¶172. In the combination, an asymmetrical signal swing is implemented on at least one of these bus systems. *See* EX1008, 2:59-62, 10:64-11:7; EX1003, ¶172. For “one-to-many” communications from the memory hub to memory devices, “normal CMOS inverters” in the memory hub drive the bus systems 76,

82, 90, 94 with “full CMOS swing.” EX1008, 11:1-7, 52-54; *see* 4:43-48; EX1003, ¶¶172-173. For “one-to-one” communications from memory device to memory hub, “the signal swing is clamped by [] receiving circuitry” in the memory hub. EX1008, 11:1-7, 54-57; EX1003, ¶¶172-173.

Also in the combination, an asymmetric signal swing is implemented on the high-speed link 58, which is another example of a “master-slave communication environment” (EX1008, 10:67-11:1), *e.g.*, in that “the controller 60 is coupled to the memory modules 54 through the high-speed link 58 using multi-drop topography.” EX1004, [0022]; *see* FIG. 2 (*compare* to FIG. 4); EX1003, ¶174. “[F]ull CMOS swing” is implemented for “one-to-many” communications from the controller to the memory modules, while “the signal swing is clamped” for “one-to-one” communications from a memory module to the controller. EX1008, 11:1-7, 52-57; EX1003, ¶¶174-175.

3. Motivation to Combine

A POSITA would have been motivated to implement an asymmetric signal swing on the bus systems of the Lee-Tsern-Leung combination as follows. EX1003, ¶¶176-180.

First, implementation of an asymmetric signal swing “capitalizes on the benefits of using both large and small signal swings on the same bus.” EX1008, 10:65-66; EX1003, ¶177.

Second, the architecture that enables implementation of asymmetric swing advantageously “minimizes bus line driver size and noise associated with driving large capacitive loads.” EX1008, 10:33-35; EX1003, ¶178.

Third, “an asymmetrical signal-swing internal bus optimizes the speed, area and power of the bus system with few masters and many slave devices.” EX1008, 2:59-62; EX1003, ¶179.

Fourth, this implementation is merely the application of known techniques (asymmetric signal swing in a memory system) to a known structure (the combination memory system) to yield predictable results (a memory system having asymmetrical signal swings on one or more of its bus systems). EX1003, ¶180; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because memory system technology is predictable, and because Leung’s asymmetrical, master-slave circuit are generally similar to the asymmetric structures of the buses in Lee’s memory system. *See* EX1008, 10:67-11:6; EX1004, [0009]; EX1003, ¶181.

4. Analysis

(a) Claim 23

[23]

In the combination, the signal swing on one or more of the bus systems 76, 82, 90, 94 (individually or collectively the *first transmission bus*) is an

“asymmetric signal swing” based on Leung, *i.e.*, “a first signal swing for data transfer over said bus along a first bus direction, and ... a second signal swing for data transfer over the bus along a second bus direction” (*a signal swing of data transmitted through the first transmission bus and a signal swing of data received through the first transmission bus are different*). EX1008, 4:43-44; *see* Abstract (“driving the internal bus with a full CMOS-swing in one bus direction and with a reduced CMOS-swing in the other bus direction”), 4:48-51 (“the second signal swing is a reduced swing substantially smaller than the first signal swing”), 2:59-63, 11:64-12:12, 12:13-19, claim 16; EX1003, ¶¶182-185. Specifically, for data transmitted from the memory hub to the memory devices (a “one-to-many” environment), a “[l]arge signal swing is used.” EX1008, 11:1-7, 52-53. For data transmitted from a memory device to the memory hub (a “one-to-one” environment), a “small swing” is used.” *Id.*, 11:1-7, 53-57; EX1003, ¶¶182-185.

(b) **Claim 24**

[24]

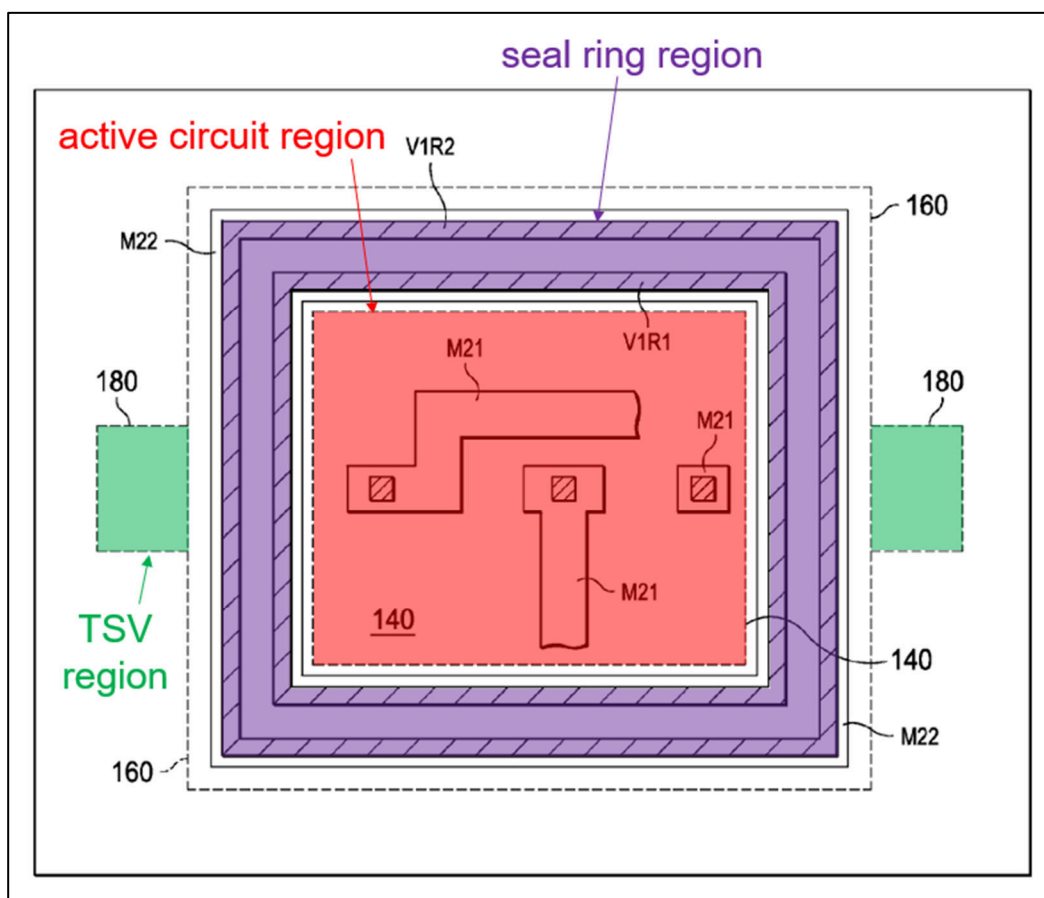
In the combination, the signal swing on the high-speed link 58 (*second transmission bus*) is an “asymmetric signal swing” based on Leung, *i.e.*, “a first signal swing for data transfer over said bus along a first bus direction, and ... a second signal swing for data transfer over the bus along a second bus direction” (*a signal swing of data transmitted through the second transmission bus and a*

signal swing of data received through the second transmission bus are different"). EX1008, 4:43-44; *see* Abstract, 2:59-63, 4:48-51, 11:64-12:12, 12:13-19, claim 16; EX1003, ¶¶186-188. For data transmitted from the controller to the memory modules ("one-to-many"), a "[l]arge signal swing is used," while from a "small swing" is used for data transmitted from a memory module to the controller ("one-to-one"). *Id.*, 11:1-7, 52-57; EX1003, ¶¶186-188.

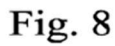
F. GROUND 1F: Claims 27-28 and 31 Are Obvious Over Lee-Tsern-Lin

1. Lin

Lin describes a wafer including "an active circuit region 140" (red in Fig. 3b and Fig. 8, *infra*) that "defines a wafer surface area where semiconductor devices are formed ... and coupled together to make functional circuit units." EX1013, [0016]. A "seal ring region 160" (purple) "encompass[es] an adjacent active circuit region" and "defines a wafer surface area where one or more seal rings are formed in the wafer," *e.g.*, "seal ring 120." *Id.*, [0016], [0024]. "[T]hrough-silicon via[s]" (*e.g.*, TSV 125) are formed in "TSV regions 180" (green). *Id.*, [0016], [0028]; EX1003, ¶¶189-190.



Lin, Fig. 3b (annotated)



Lin, Fig. 8 (annotated)

Lin is analogous art to the '942 Patent: it is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1013, Abstract; EX1003, ¶191.

2. The Lee-Tsern-Lin Combination

In the combination, the memory hub and the memory devices are ICs each including a seal ring and TSVs, based on Lin. EX1003, ¶192. Specifically, logic circuitry (for the memory hub chip) and memory circuitry (for the memory devices) are formed in an active circuit region of the respective chips. *See*

EX1013, [0015], Fig. 3b, Fig. 8; EX1003, ¶192. A seal ring surrounds the active circuit region, and TSVs are formed outside of the seal ring region. *See* EX1013, [0015], Fig. 3b, Fig. 8; EX1003, ¶192.

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to implement the memory hub and memory device ICs to each include a seal ring and TSV(s) because (1) TSVs allow the chips to be stacked, providing benefits such as increased system speed, lower costs, and better integration; (2) a seal ring positioned between the active circuit region and the TSVs “block[s] moistures or other undesirable chemical agents from diffusing into [the] active circuit region 140” involved in forming the TSVs, thereby enabling fabrication of good quality ICs; and (3) it is merely the application of known techniques (seal rings and TSVs in ICs) to a known structure (a memory system with memory hub and memory device ICs) to yield predictable results (memory hub and memory device ICs having seal rings and TSVs).

EX1013, [0003]-[0004], [0006], [0016], [0023]; EX1003, ¶¶193-196; *see KSR*, 550 U.S. at 417.

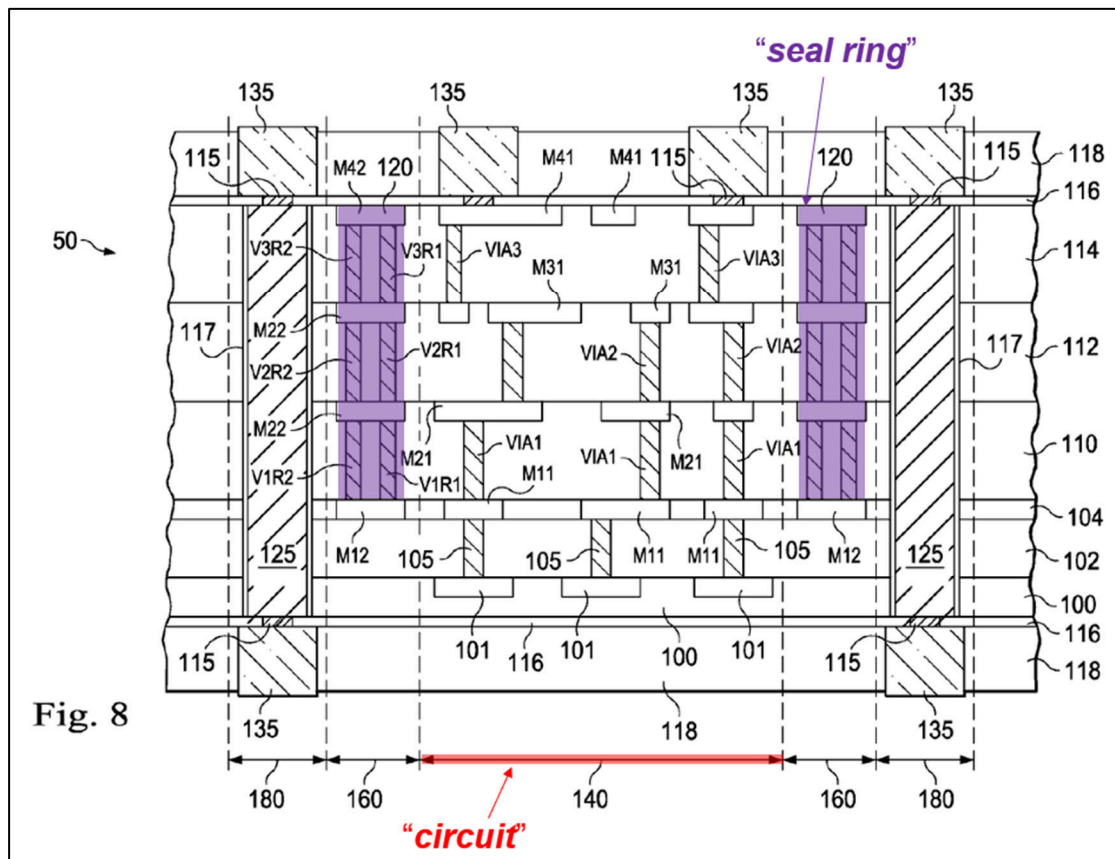
A POSITA would have expected success because IC structure is predictable and because TSVs and seal rings in ICs was conventional. *See* EX1014, Abstract; EX1022, Abstract; EX1003, ¶197.

4. Analysis

(a) Claim 27

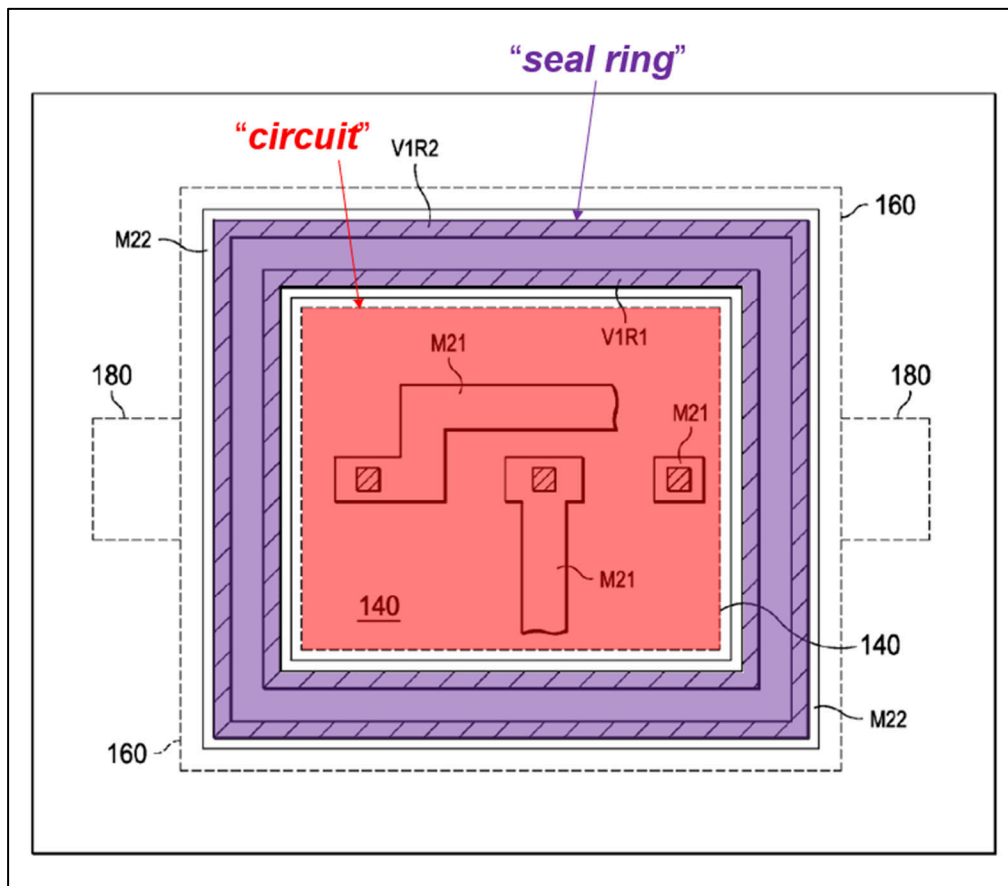
[27]

In the combination, the memory hub and each memory device are ICs structured with a seal ring and TSVs, based on Lin. EX1003, ¶¶198-201. Specifically, each IC includes a “seal ring 120” (purple in Fig. 8, *infra*), *i.e.*, each memory device (*memory cell array IC*) includes (*corresponds to*) *a first seal ring* and the memory hub (*logic unit*) *corresponds to* a second seal ring. EX1013, [0024]; *see* Abstract, [0002], [0007]-[0010], [0012]-[0013], [0016], [0024], [0035], claim 1, FIGS. 8-9; EX1003, ¶¶199-201.



Lin, Fig. 8 (annotated)

Each IC also includes “an active circuit region 140 [that] defines a wafer surface area where semiconductor devices are formed ... and coupled together to make functional circuit units.” EX1013, [0016]. The active circuit region (red *supra*; see also Fig. 3b, *infra*) in each IC corresponds to ***a circuit, e.g., a circuit of each of the memory cell array ICs and a circuit of the logic unit*** (memory hub). EX1003, ¶202. Consistent with Lin, the seal ring of each IC “encompasses an adjacent active circuit region” (***a circuit of each IC is surrounded by the respective seal ring***). EX1013, [0024]; see Fig. 3b, Abstract; EX1003, ¶202.

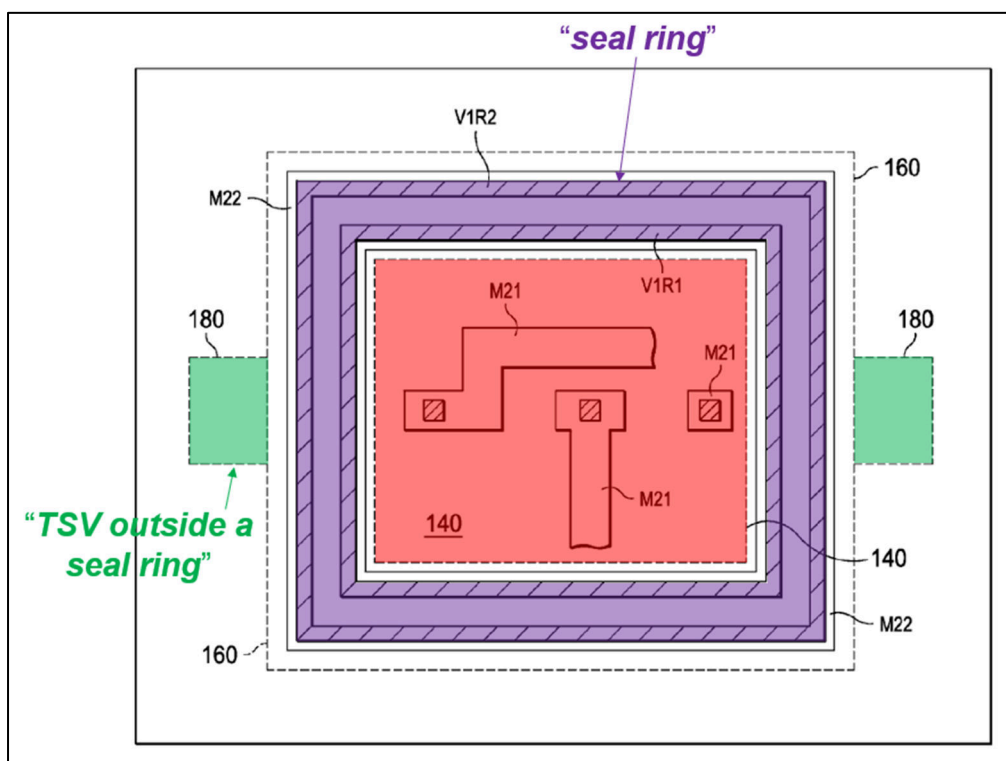


Except from Lin, Fig. 3b (annotated)

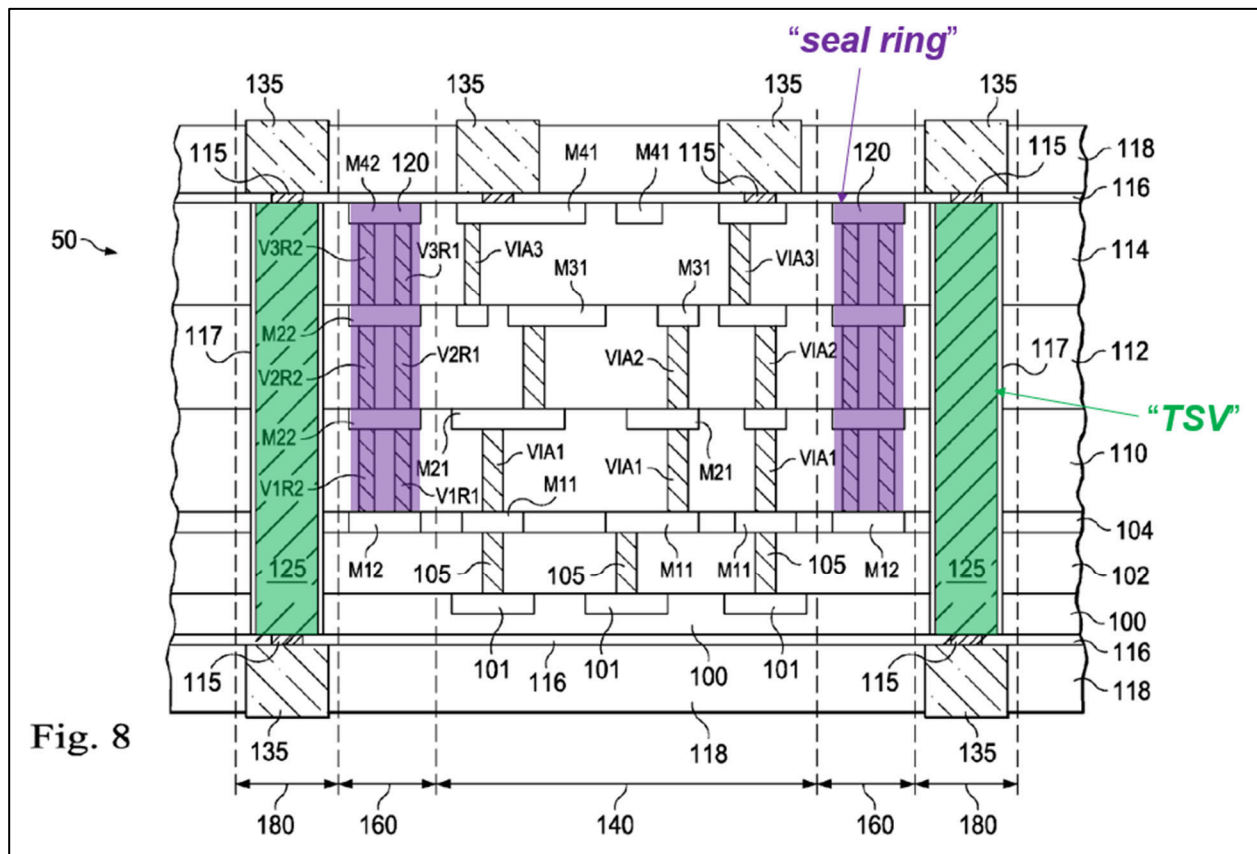
(b) Claim 28

[28]

Based on Lin, each combination memory cell IC has a “through-silicon via[]” (*at least one TSV*) formed in a “TSV region,” green in Figs. 3b and 8, *infra*. EX1013, [0016], [0028]; EX1003, ¶203. “[T]he TSV region [is] separated from active circuit region by the seal ring,” *i.e.*, the seal ring (purple) is disposed between the TSV region and the active circuit region (red), and thus the TSV *exists outside of the seal ring*. See EX1013, [0010], Figs. 3b, 8; EX1003, ¶203.



Except from Lin, Fig. 3b (annotated)



Lin, Fig. 8 (annotated)

(c) Claim 31

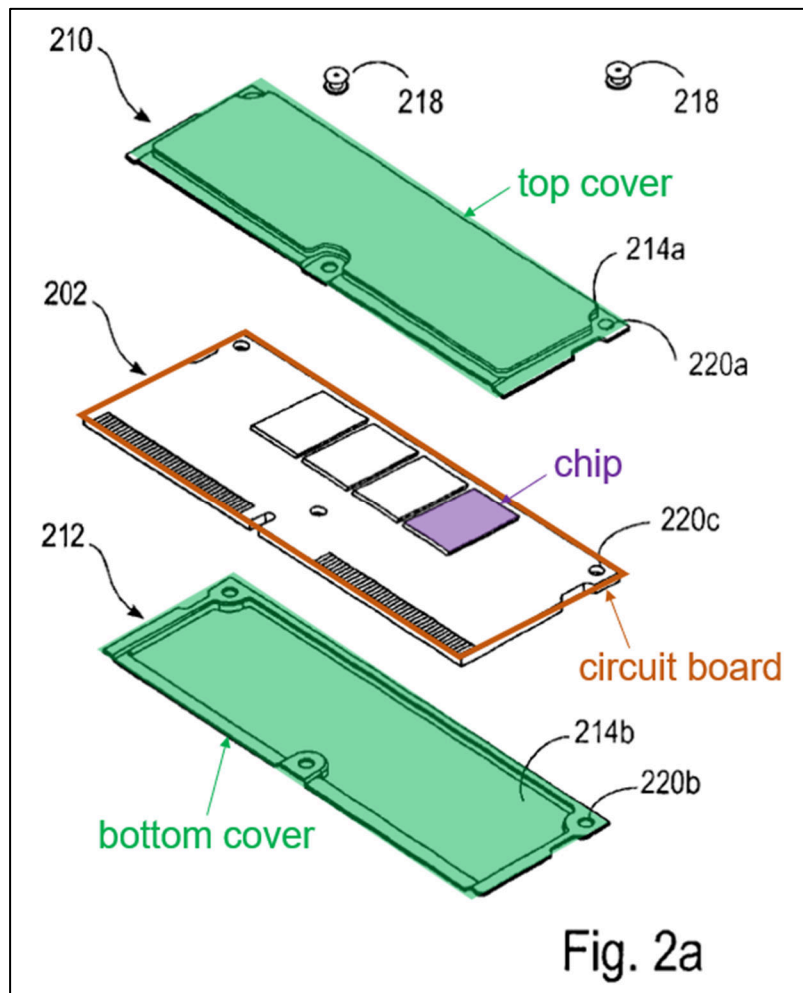
[31]

Based on Lin, the logic unit IC has a “through-silicon via[]” (*at least one TSV*) formed in a “TSV region” that is “separated from active circuit region by the seal ring (*exists outside of the seal ring*)”. EX1013, [0010]; *see* [0016], [0028], Fig. 3b, Fig. 8; *see* [28]; EX1003, ¶204.

G. GROUND 1G: Claim 29 is Obvious Over Lee-Tsern-Lin-Ali

1. Ali

Ali describes a “packaging cover for a multi-chip memory module” including a top cover 210 and a bottom cover 212, green in FIG. 2a, *infra*, “each hav[ing] a size large enough to cover/encapsulate the chips 204-210 [purple] on the circuit board 202.” *Id.*, 2:27-28, 3:7-9. A “thermally conductive gel provides a thermal coupling between the memory chips and the inner surface of the packaging cover.” *Id.*, 3:34-36. The covers may be made of metal to act as a heat sink. *See id.*, 3:53-62; EX1003, ¶205.



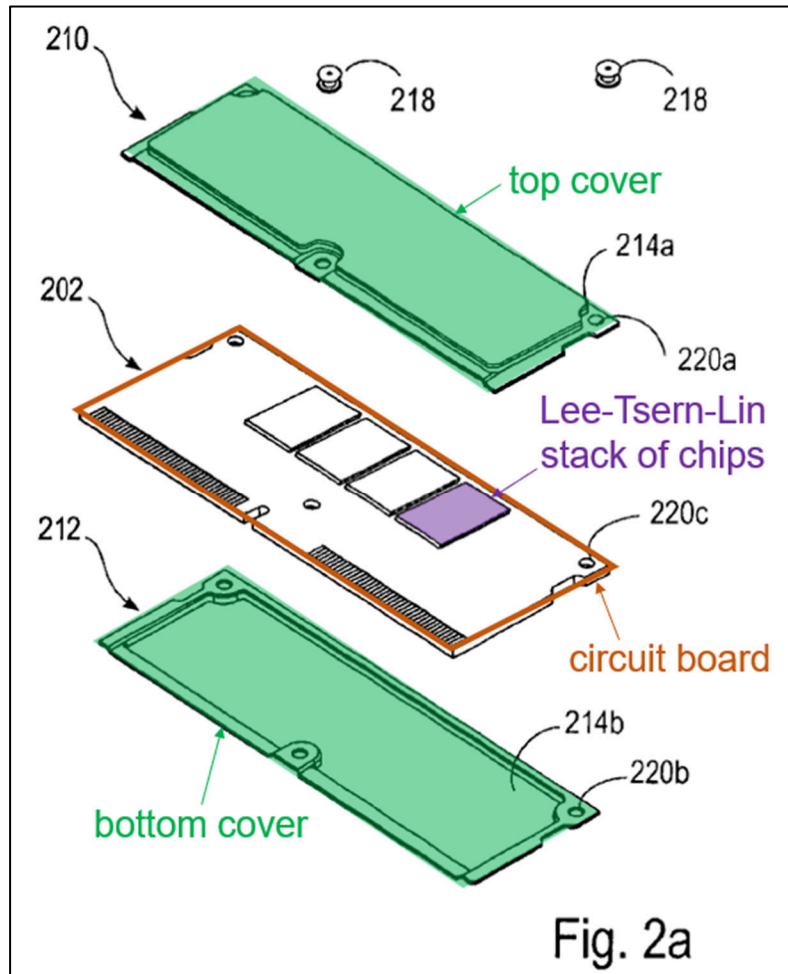
Ali, Fig. 2a (annotated)

Ali is analogous art to the '942 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1015, Abstract; EX1003, ¶¶206-207.

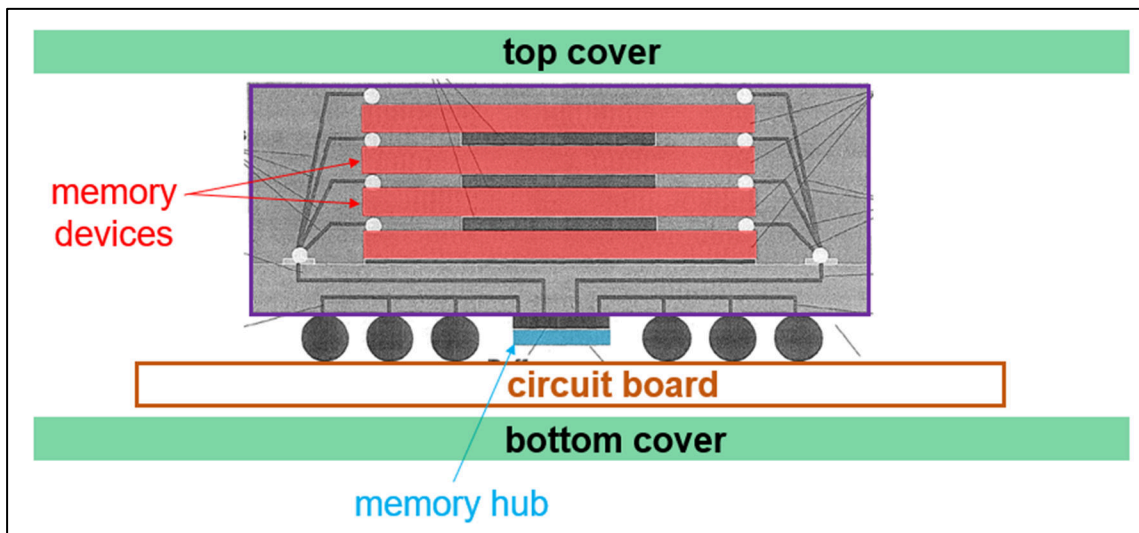
2. The Lee-Tsern-Lin-Ali Combination

In the combination, the memory devices and memory hub are stacked, *e.g.*, based on Tsern's Fig. 11. *See* §V.B.2, *supra*; EX1003, ¶208. For instance, each rank of memory devices can be arranged in a respective stack. As illustrated *infra*,

multiple stacks (purple) of chips are assembled on a circuit board and packaged in a metal “package covering” based on Ali, such that “top and bottom covers will cover/encapsulate” the stack(s) of chips. EX1015, 3:4-6; *see* 3:57-59; EX1003, ¶208.



Lee-Tsern-Lin-Ali figure based on Ali, Fig. 2a



Lee-Tsern-Lin-Ali figure based on Tsern, Fig. 11

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to package chip stacks in a cover because (1) encapsulating the chip stacks in metal covers provides “heat sink” functionality, helping to prevent overheating (EX1015, 3:57-61; *see* 1:45-50); (2) packaging the chip stacks in “rigid” covers provides “protection of the memory module” (*id.*, 3:1-3, 4:15-22; *see* 1:25-27); (3) when multiple chips stacks are encapsulated in a single package, the packaging can “accommodate for the potential variances in the height among the multiple” stacks (*id.*, 1:53-55); and (4) it is merely the application of known techniques (packaging of chips in a multi-chip memory module) to a known structure (*e.g.*, the combination chip stacks) to yield predictable results (a packaged chip stack). EX1015, 3:57-61; *see* 1:45-50; EX1003, ¶¶209-213; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because packaging technology was predictable, and because Ali relates to packaging in the context of memory modules. *See* EX1015, Abstract; EX1003, ¶214.

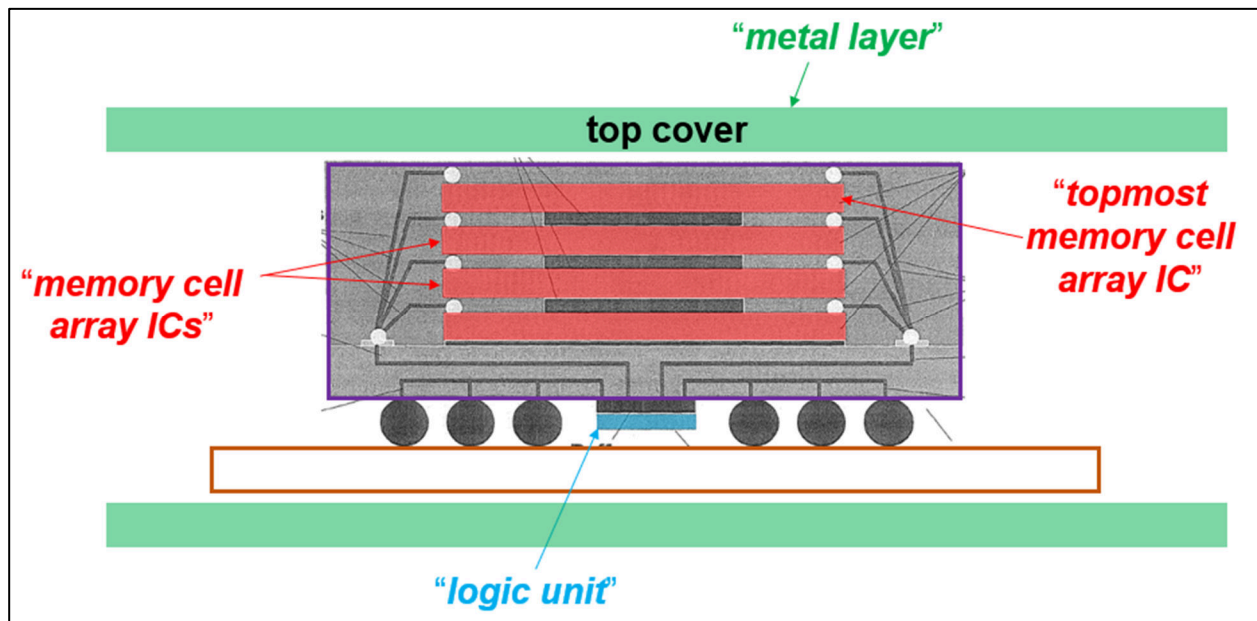
4. Analysis

(a) Claim 29

[29a]

In the combination, the “top cover 210” (green *infra*), “made of metal material,” corresponds to a ***metal layer***. EX1015, 3:7, 57-58; *see* Abstract, 3:64-4:2; 4:14-15, claim 10; EX1003, ¶¶215-216.

The memory cell array ICs and logic unit, stacked based Tsern (*see* §V.B.2, *supra*), are packaged between top and bottom covers based on Ali, as illustrated *infra*, such that “the top and bottom covers will cover/encapsulate” the stacked chips. EX1015, 3:111-12; *see* Abstract, 2:1-2, 2:49-50, claim 1, Fig. 2a; EX1003, ¶217. Because the top cover “cover[s]” the stack, it is ***disposed over the topmost memory cell array IC***. Moreover, because the covers “have a size large enough to cover/encapsulate” the stack of chips, the top cover is sized to ***cover more than 50% area of the topmost memory cell array IC***. EX1015, 3:8-9; EX1003, ¶217.



Lee-Tsern-Lin-Ali figure based on Tsern, Fig. 11

[29b]

In the combination chip stack, the memory cell array ICs (red *supra*) are **stacked over** the logic unit (blue) based on Tsern. *See* EX1005, 26, Fig. 11; EX1003, ¶218.

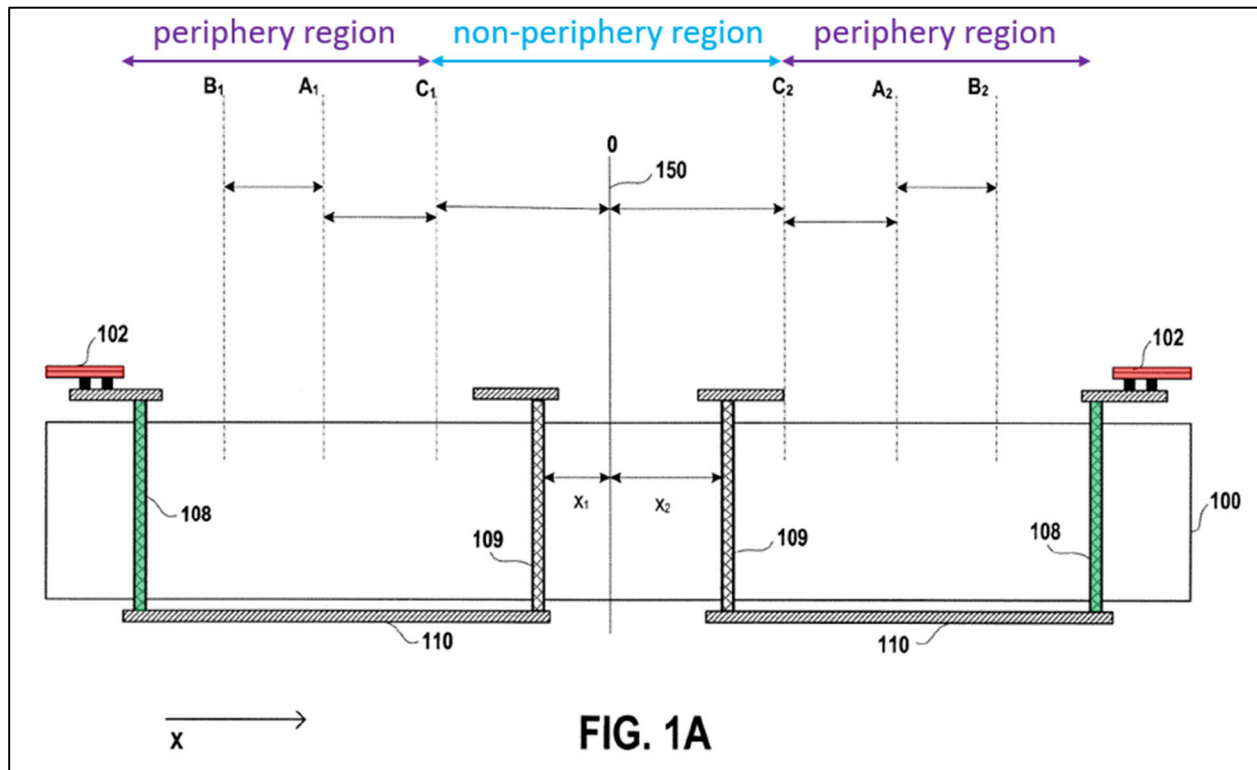
H. GROUND 1H: Claim 30 is Obvious Over Lee-Tsern-Lin-White

1. White

White describes an “integrated circuit with distributed power using through-silicon vias (TSVs).” EX1014, Abstract. White’s IC has a “non-periphery region ... where the active device processing occurs,” and a surrounding “periphery region.” EX1014, 3:26-30; *see* 3:29-44. TSVs (green in FIG. 1A, *infra*) “route

power and ground from the bonding pads 102 [red], to the non-periphery region.”

Id., 3:48-49; EX1003, ¶¶219-220.



White, FIG. 1A (annotated)

White is analogous art to the '942 Patent: it is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1014, 2:5-7; EX1003, ¶221.

2. The Lee-Tsern-Lin-White Combination

In the combination, TSVs (*e.g.*, TSVs based on Lin; *see* §V.F.2, *supra*) “route power and ground from [] bonding pads 102, to the non-periphery region,”

e.g., to the active circuit region. EX1014, 3:48-49; *see* EX1013, [0016]; EX1003, ¶222.

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to use the Lee-Tsern-Lin TSVs for connection to power/ground because (1) power distribution through TSVs “reduces the effect of resistive voltage drops on a conducting line” (EX1014, 4:16-29); (2) using TSVs to connect to power/ground was conventional (*see* EX1014, 3:1-2; EX1025, [0025]); and (3) it is merely the application of known techniques (TSVs connected to power/ground) to a known structure (the Lee-Tsern-Lin ICs, having peripheral TSVs) to yield predictable results (an IC with peripheral TSVs providing power/ground to non-peripheral circuits). EX1003, ¶¶223-226; *see KSR*, 550 U.S. at 417.

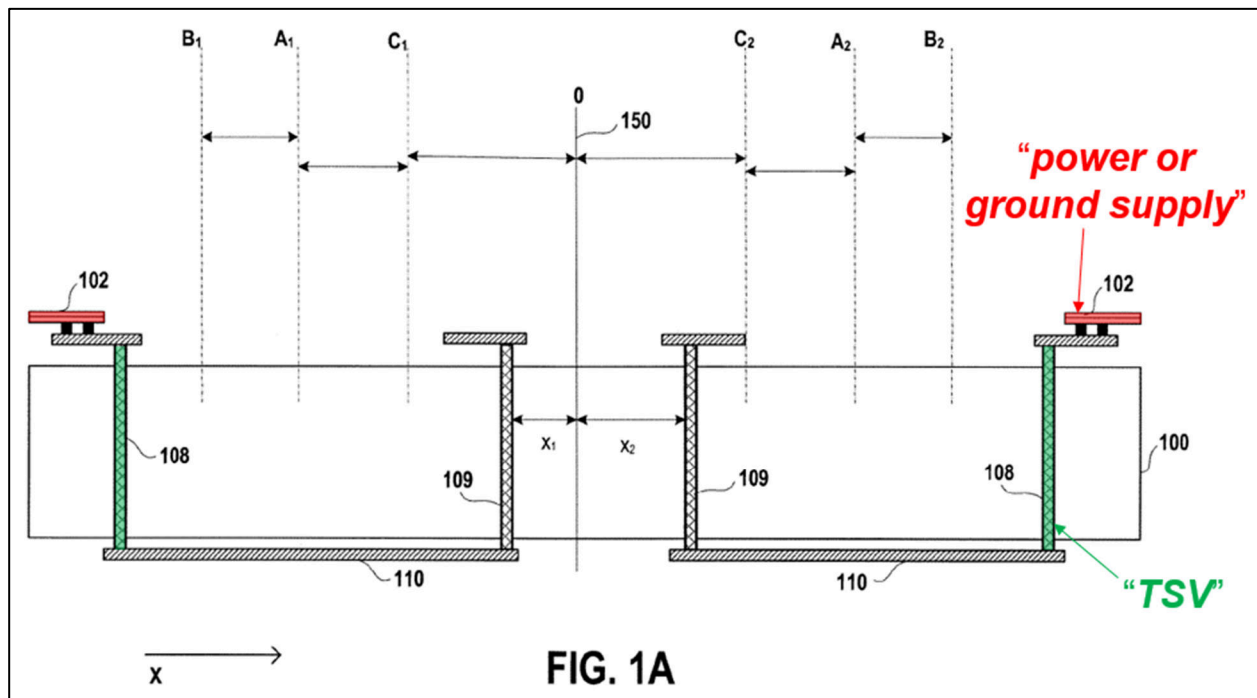
A POSITA would have expected success because the peripheral positioning of the Lee-Tsern-Lin TSVs is consistent with White’s TSVs, because IC structure is predictable and because using TSVs for connection to power/ground was conventional. *See* EX1013, Figs. 3b, 8; EX1014, 3:26-30, 3:48-49, FIG. 1A; EX1003, ¶227 (citing EX1014, 3:1-2; EX1025, [0025]).

4. Analysis

(a) Claim 30

[30]

In the combination, a peripheral TSV (*see* [28], *supra*) is implemented based on White to “route power and ground from the bonding pads 102, to the non-periphery region.” EX1014, 3:48-50; *see* 2:57-58; EX1003, ¶¶228-229. The bonding pads (red in FIG. 1A, *infra*) “provide power and ground” and thus correspond to ***a power or ground supply***. EX1014, 3:17-19; *see* Abstract, 1:46-48, 3:64-66. The peripheral TSVs (green) are connected to the bonding pads, *i.e.*, ***used for connecting to the power/ground supply***. *See id.*, FIG. 1A, 1:38-40, 1:53-56, 4:17-21, 2:57-58, 3:7-8, 3:47-50, 4:24-26, 4:37-46, 4:58-63, 5:38-45, 5:65-67, 6:24-26, 6:49-64, claim 1, claim 9; EX1003, ¶229.



White, FIG. 1A (annotated)

I. GROUND 1I: Claims 1, 5, and 9-10 Are Obvious Over Lee-Tsern-Matsubara

1. Matsubara

Matsubara describes a semiconductor device having a “DRAM region” and a “logic Nch region.” EX1006, 3:65-4:7. Matsubara describes that “[t]he minimum gate length of the transistors provided to the DRAM region 104 is set larger than the minimum gate length of the transistors provided to the logic Nch region.” *Id.*, 6:34-37. The “relatively small gate length” of the logic transistors is “in view of improving the operation speed.” *Id.*, 6:21-23. By contrast, “the gate length is not a key factor of governing the operation speed of DRAM,” and instead,

“[t]he DRAM region 104 is controlled under an allowable level of junction leakage more strictly than in the logic Nch region.” *Id.*, 6:32-39; EX1003, ¶230.

It was conventional as of the Critical Date that for a given process generation, the gate length of memory (*e.g.*, DRAM) transistors was longer than the gate length of logic transistors, given different performance criteria for the two types of devices. EX1003, ¶¶235-240. Specifically, and as explained further by Dr. Liu, logic transistors were designed for speed, and accordingly, had short gate lengths; while memory (*e.g.*, DRAM) transistors were designed for stability, achievable by longer gate lengths. EX1003, ¶¶235-240 (citing EX1006, 6:32-39; EX1024, 1:26-32, 1:45-52, 2:3-20; EX1026, 4:6-8; EX1027, 3:28-3).

Matsubara is analogous art to the '942 Patent: it is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1006, Abstract; EX1003, ¶231.

2. The Lee-Tsern-Matsubara Combination

The Lee-Tsern-Matsubara system is based on the structure of Lee's memory system 50. EX1003, ¶232. Specifically, based on Lee, memory device ICs, *e.g.*, DRAM devices, are coupled to the memory hub 60 through a respective bus system. *See* EX1004, [0016]. The memory hub (an IC, based on Tsern) is also coupled to a memory controller through a “high-speed link 58.” *Id.*; *see* EX1005, Abstract, 30, Fig. 11; EX1003, ¶232.

ICs, such as the memory hub and the memory devices of the combination, are composed of transistors (among other elements). EX1003, ¶233 (citing EX1006, 4:2-4; EX1024, 1:15-20). In the combination, based on Matsubara—and as was conventional—the transistors of the memory hub are dimensioned differently from the transistors of the memory devices. EX1003, ¶234. Specifically, the “gate length of the transistors” of the memory devices “is set larger than the minimum gate length of the transistors provided to the logic [] region,” *i.e.*, the transistors of the IC memory hub. EX1006, 6:34-37; EX1003, ¶234. This difference in dimensions allows for satisfaction of differing performance criteria between the two types of devices: speed, for the memory hub; and stability and low leakage, for the memory devices. EX1003, ¶¶235-240 (citing EX1006, 6:32-39; EX1024, 1:26-32, 1:45-52, 2:3-20; EX1026, 4:6-8; EX1027, 3:28-3).

3. Motivation to Combine

A POSITA would have been motivated to implement the memory transistors to have a longer gate length than the memory hub transistors as follows. EX1003, ¶¶241-244.

First, these relative dimensions to facilitate conformity with differing performance criteria between logic transistors and memory transistors. EX1003, ¶242. Specifically, speed is a key design parameter in logic transistors, while

stability is more important for memory devices. *See* EX1024, 1:23-32, 1:45-52, 2:3-20; EX1006, 6:37-39; EX1003, ¶242. The high speed demanded for logic devices is achieved by a short gate length, while the stability for memory devices is achieved by longer gate lengths. *See* EX1006, 6:32-37 (“[t]he logic region containing the logic Nch region 102 has a relatively small gate length in view of improving the operation speed,” while “[o]n the other hand, the gate length is not a key factor of governing the operation speed of DRAM provided to the DRAM region 104,” so “[t]he minimum gate length of the transistors provided to the DRAM region 104 is set larger than the minimum gate length of the transistors provided to the logic Nch region 102”); EX1026, 4:6-8; EX1027, 3:28-34; EX1003, ¶242.

Second, memory transistors having a longer gate length than the gate length of logic transistors was conventional. EX1003, ¶243 (citing EX1006, 6:32-39; EX1024, 1:15-52, 2:3-20; EX1026, 4:6-8; EX1027, 3:28-34).

Third, this implementation is merely the application of known techniques (different types of transistors having different gate lengths to achieve differing performance objectives) to a known structure (the memory device and memory hub ICs of the combination) to yield predictable results (a memory system in which the memory device ICs have a longer gate length than the memory hub IC). EX1003, ¶244; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because memory system technology and IC fabrication technology are predictable, and because IC designs in which memory cells have transistors with longer gate length than logic cells was conventional. *See* EX1006, 6:32-39; EX1024, 1:15-52, 2:3-20; EX1026, 4:6-8; EX1027, 3:28-34; EX1003, ¶245.

4. Analysis

(a) Claim 1

[1pre]

The Lee-Tsern-Matsubara combination includes a *high speed memory chip module*. *See* [19pre] of Grounds 1A-1B; EX1003, ¶¶246-247.

The memory chip module is *reconfigurable*, *e.g.*, because it can be “configure[d] ... depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]; *see* [0020] (“By allowing the memory hub 60 to configure the data format of the memory module 54 ... The data format is therefore not fixed”); EX1003, ¶248.

[1a.1]

See [19b] of Grounds 1A-1B; EX1003, ¶249.

[1a.2]

In the combination, the memory devices are, *e.g.*, “dynamic random access memory devices (‘DRAMs’).” EX1004, [0016]. DRAMs (among other memory

devices) are produced by a MOSFET process, a conventional and widely-used process for fabricating memory devices, *i.e.*, the memory devices (***at least one memory cell array***) of the combination ***correspond to a first MOSFET process***. See EX1030, 526, 611; EX1005, 12; EX1016, 4:56-60; EX1003, ¶¶250-252.

MOSFET devices include transistors. EX1003, ¶253 (citing EX1030, 526, 611; EX1024, 1:15-32). The gate length of a transistor is distance between its source and drain, and is defined by the dimensions of the features formed during the MOSFET fabrication process. EX1003, ¶253 (citing EX1030, 527).

Accordingly, a given MOSFET process corresponds to a MOSFET gate length of the transistors formed during that fabrication process, *i.e.*, the ***first MOSFET process corresponds to a first MOSFET gate length*** of the memory cell transistors formed during that first process. EX1003, ¶253.

[1b.1]

See [19c] of Grounds 1A-1B; EX1003, ¶254.

[1b.2]

The combination memory hub IC (***logic unit***) is produced by a MOSFET process, *i.e.*, the memory hub (***logic unit***) ***corresponds to a second MOSFET process***. See [1a.2]; EX1005, Abstract, Fig. 12; EX1030, 526, 611; EX1024, 1:15-32; EX1003, ¶255.

To the extent PO argues that the *first* and *second MOSFET process* refer to different MOSFET processes, a POSITA would have understood this to be the case. EX1003, ¶256. Circuit layout, dimensions, and/or materials differ between logic devices (*e.g.*, the memory hub) and memory devices, and thus, different processes are used to fabricate the two types of devices. EX1003, ¶256 (citing EX1006, 2:51-54, 6:32-39; EX1026, 4:6-8; EX1027, 3:28-34). Moreover, in the combination, the memory hub and the memory devices are each distinct ICs, *e.g.*, able to be arranged in a stacked arrangement such as illustrated in Tsern's Fig. 11. EX1003, ¶256. Different fabrication processes are used to fabricate distinct IC devices. *Id.*

A given MOSFET process corresponds to a MOSFET gate length of the transistors formed during that fabrication process, *i.e.*, the *second MOSFET process corresponds to a second MOSFET gate length* of the memory hub transistors formed during that second process. *See* [1a.1]; EX1003, ¶257.

In the combination, the gate length of the memory device transistors (*first gate length*) is *longer than* the gate length of the memory hub transistors hub (*second gate length*), based on Matsubara, and as was conventional. EX1003, ¶¶258-259. Specifically, “[t]he minimum gate length of the transistors” in the memory devices “is set larger than the minimum gate length of the transistors” in

the memory hub. EX1006, 6:34-37; *see* Abstract, 4:4-7, 2:3-9, 3:14-23, 2:44-50, 4:37-42, 6:21-39, 6:59-65, 8:51-54, claim 1; EX1003, ¶¶258-259.

[1c]

See [19d] of Grounds 1A-1B; EX1003, ¶260.

(b) Claim 5

[5a]

See [20c] of Ground 1B; EX1003, ¶261.

[5b]

See [19a] and [19e] of Ground 1A. In the combination, the memory hub (*logic unit*) is coupled to the controller (*ASIC*) via the high-speed link (*second transmission bus*), for transmission of the second set of parallel data to the ASIC. *See* EX1004, [0015] (“the high-speed link 58 will have a capacity for coupling data ... between the controller 52 and each memory module 54”), Fig. 2, Fig. 5; EX1003, ¶262.

[5c]

See [19f] of Ground 1A; EX1003, ¶263.

(c) Claim 9

[9]

See [25] of Ground 1B; EX1003, ¶264.

(d) **Claim 10**

[10]

See [26] of Ground 1B; EX1003, ¶265.

J. GROUND 1J: Claim 2 is Obvious Over Lee-Tsern-Matsubara-Dozen

1. Analysis

(a) **Claim 2**

[2a]

In Lee-Tsern-Matsubara-Dozen, the memory devices (*memory cell array ICs*) are “dynamic random access memory devices (‘DRAMs’),” based on Lee. EX1004, [0016]; *see* claims 11-12; EX1003, ¶266.

[2b]

See [20c]. EX1003, ¶267.

K. GROUND 1K: Claim 3 Is Obvious Over Lee-Tsern-Matsubara-Khan

1. Analysis

(a) **Claim 3**

[3a]-[3b]

See [20a]-[20b]; EX1003, ¶¶268-269.

L. GROUND 1L: Claim 4 Is Obvious Over Lee-Tsern-Matsubara-Khan-Dozen

1. Analysis

(a) Claim 4

[4a]-[4b]

See [21a]-[21b]; EX1003, ¶¶270-271.

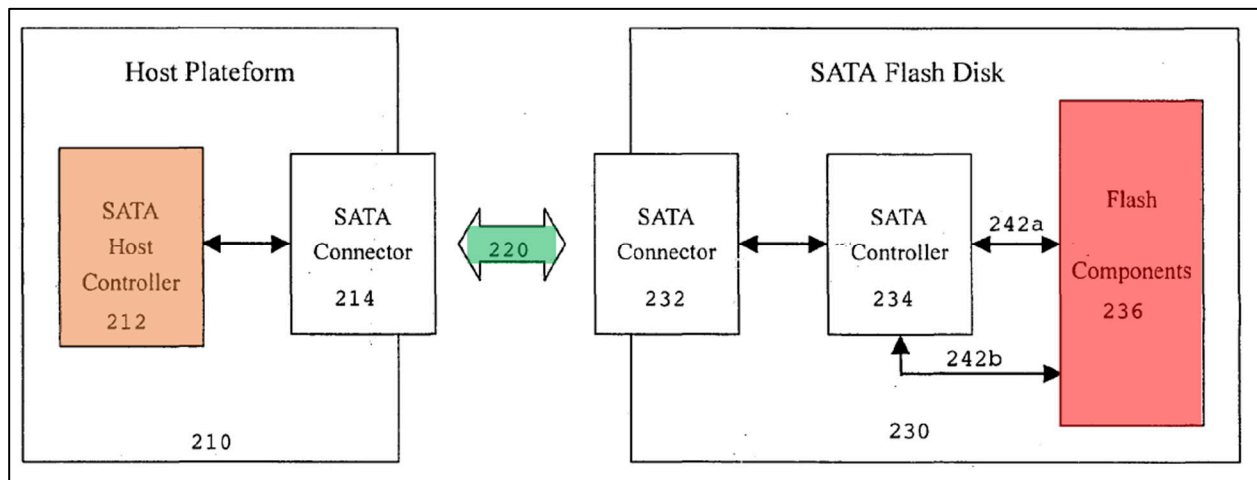
[4c]

See [20c]. EX1003, ¶272.

M. GROUND 1M: Claim 6 Is Obvious Over Lee-Tsern-Matsubara-Weng

1. Weng

Weng describes “semiconductor memory devices ... which are connected to a host platform using the SATA (Serial Advanced Technology Attachment) PC Bus.” EX1017, [0001]. A “flash memory system” includes “a host platform 210” “connected to the SATA flash memory disk 230 by means of an SATA cable 220,” green in Fig. 2, *infra. Id.*, [0052]-[0053]. On the host platform, a “SATA main controller,” orange, manages “all SATA transferring on the SATA bus,” *e.g.*, reading, writing, or erasing to the flash memory components 236 (red) on the flash disk. *Id.*, [0053], [0056]; EX1003, ¶273.

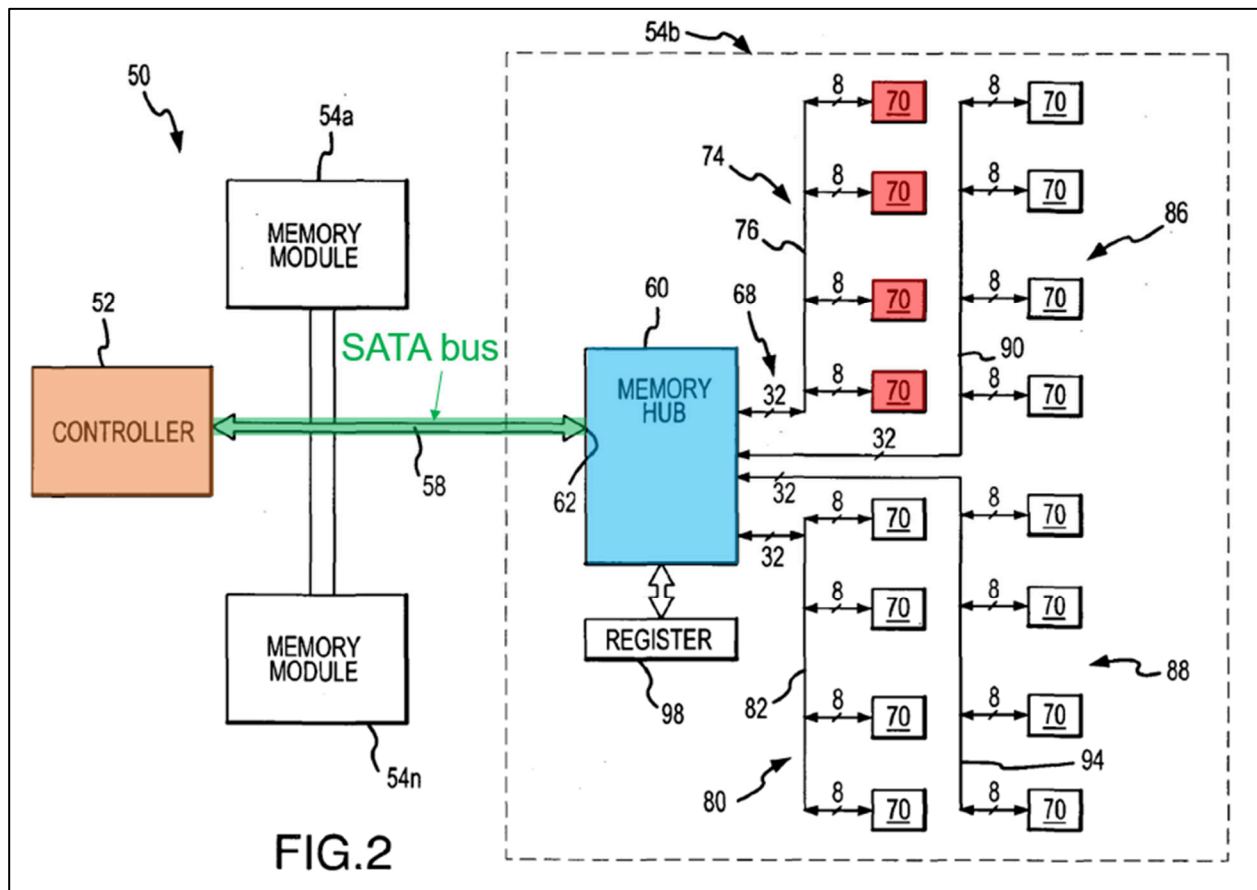


Weng, Fig. 2 (annotated)

Weng is analogous art to the '942 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1017, Abstract, [0020]-[0026]; EX1003, ¶¶274-275.

2. The Lee-Tsern-Matsubara-Weng Combination

In the combination, the high-speed bus 58 connecting the controller to the memory modules is implemented as a SATA cable based on Weng's teachings of a host platform "connected to [a] SATA flash memory disk 230 by means of an SATA cable." EX1017, [0052]; EX1003, ¶¶276-278. Consistent with Weng, responsive to a request received from the controller via the SATA bus, the memory hub "performs various operations such as 'read', 'write' and 'erase'" to the memory devices 70. EX1017, [0056]; EX1003, ¶¶276-278.



Lee-Tsern-Matsubara-Weng figure based on Lee, FIG. 2

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to implement the high-speed link as a SATA connection as follows. EX1003, ¶¶279-282.

First, SATA connections have a number of advantages, including (among others), low voltage, low cost, efficiency, high transfer rate, and simplicity. *See* EX1017, [0016]-[0035]; EX1003, ¶280.

Second, a SATA cable connecting a memory controller to memory devices was commonplace, and a POSITA would have been motivated to employ

conventional protocols in the combination. EX1003, ¶281 (citing EX1028, 2:55-62).

Third, this implementation is merely the application of known techniques (a SATA cable connecting a memory controller to memory devices) to a known structure (a memory system including memory modules and a memory controller) to yield predictable results (a memory system in which the memory controller is connected to the memory modules by a SATA bus). EX1003, ¶282; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because memory system technology is predictable, and because SATA protocol connections were conventional. EX1003, ¶283 (citing EX1028, 2:55-62). Moreover, a POSITA would have expected success because of the generally similar architecture between Lee's and Weng's memory systems. *See* EX1004, FIG. 2; EX1017, Fig. 2; EX1003, ¶283. Finally, a POSITA would have expected success because Lee's system is compatible with various types of memory devices (*see* EX1004, [0016]), such as Weng's flash memory devices. EX1003, ¶283.

4. Analysis

(a) Claim 6

[6]

In the combination, the high-speed link (*second transmission bus*) is implemented as a “SATA cable” based on Weng (*comprising the protocol of a SATA bus*). EX1017, [0050]; *see* [0001], [0037], [0048], [0050], [0053], FIG. 2; EX1003, ¶¶284-285.

N. GROUND 1N: Claims 7-8 Are Obvious Over Lee-Tsern-Matsubara-Leung

1. Analysis

(a) Claim 7

[7]

See [23]; EX1003, ¶¶286-287.

(b) Claim 8

[8]

See [24]; EX1003, ¶¶288.

O. GROUND 1O: Claims 11-12 and 15 Are Obvious Over Lee-Tsern-Matsubara-Lin

1. Analysis

(a) Claim 11

[11]

See [27]; EX1003, ¶289-290

(b) Claim 12

[12]

See [28]; EX1003, ¶291.

(c) Claim 15

[15]

See [31]; EX1003, ¶292.

P. GROUND 1P: Claim 13 is Obvious Over Lee-Tsern-Matsubara-Lin-Ali

1. Analysis

(a) Claim 13

[13]

See [29]; EX1003, ¶293-294.

Q. GROUND 1Q: Claims 14 and 18 Are Obvious Over Lee-Tsern-Matsubara-Lin-White

1. Analysis

(a) Claim 14

[14]

See [30]; EX1003, ¶¶295-296.

(b) Claim 18

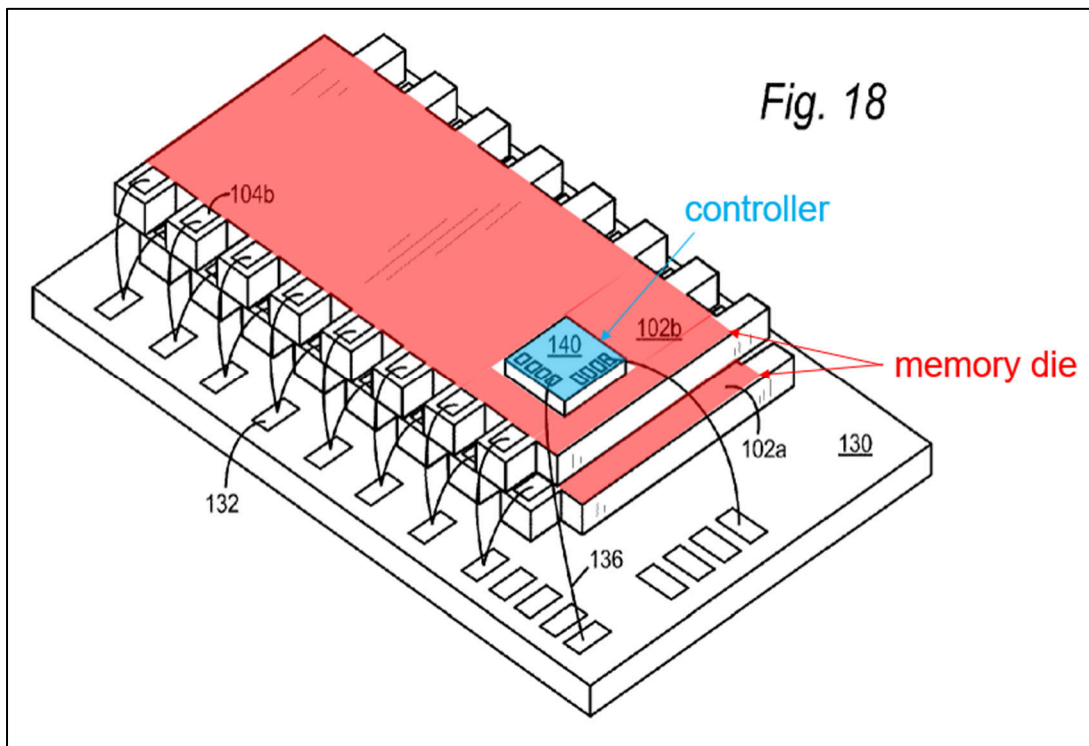
[18]

In Lee-Tsern-Matsubara-Lin-White, the peripheral TSV of the logic unit is connected to bonding pads that provide power/ground, *i.e.*, the TSV is *used for connecting to a power/ground supply*. See [30]; EX1003, ¶297.

R. GROUND 1R: Claim 16 is Obvious Over Lee-Tsern-Matsubara-Lin-Liao

1. Liao

Liao describes a semiconductor package including one semiconductor die 102a, 102b, *e.g.*, memory die (red in Fig. 18, *infra*) “stacked on” one another, with “a controller die 140 [blue] ... atop the stack.” EX1016, 3:9-10, 4:56-60, 5:33-34, 6:53-54; EX1003, ¶298.



Liao, Fig. 18 (annotated)

Liao is analogous art to the '942 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '942 Patent was trying to solve. *See* EX1001, 1:17-25; EX1016, 4:56-50, 6:48-50; EX1003, ¶¶299-300.

2. The Lee-Tsern-Matsubara-Lin-Liao Combination

In Lee-Tsern-Matsubara-Lin-Liao, the memory hub and at least one rank of memory devices are packaged in a stack, with the memory hub “affixed atop the stack” of memory devices. EX1016, 6:53-56; *see* Figs. 17-18; EX1003, ¶301.

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to stack the memory devices and memory hub because (1) stacking of chips allows for “integrating more devices

into a smaller volume,” enabling “smaller footprint, shorter signal routing, reduced wiring density” (EX1009, 1); (2) Liao’s stacked arrangement “allow[s] a large number of die in the stack while still fitting within a standard memory card form factor” (EX1016, 6:47-49); and (3) it is merely the application of known techniques (a semiconductor package having a die stack) to a known structure (a memory system including memory chips and memory hub) to yield predictable results (a memory module having a stack of memory chips topped by a controller chip). EX1003, ¶¶302-305; *see KSR*, 550 U.S. at 417.

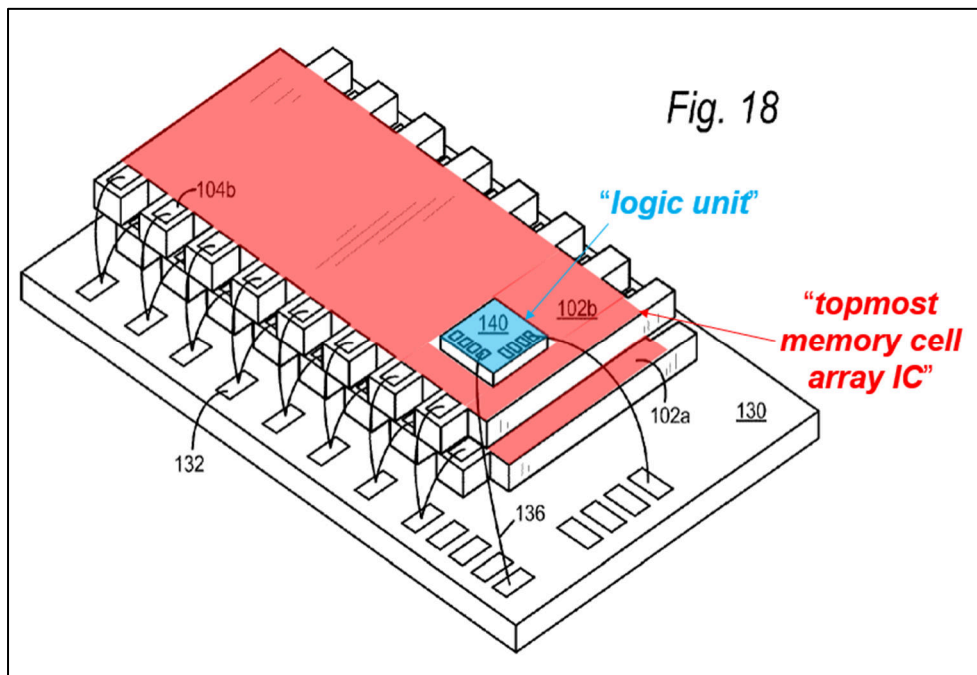
A POSITA would have expected success because semiconductor packaging technology is predictable and because a stacked package of memory and logic chips was conventional. *See, e.g.*, EX1005, Fig. 11; EX1009, Fig. 1(a); EX1003, ¶306.

4. Analysis

(a) Claim 16

[16]

In the combination, the memory devices (*memory cell array ICs*) (red in Liao’s Fig. 18, *infra*) of at least one rank form a “die stack,” and the memory hub (*logic unit*) is “affixed atop the stack” (*stacked over a topmost memory cell array IC*), based on Liao. EX1016, 6:53-56; *see* Abstract, 4:56-60, 5:33-34, 6:4-15, 6:45-52, Figs. 17-18; EX1003, ¶¶307-308.



Liao, Fig. 18 (annotated)

S. GROUND 1S: Claim 17 is Obvious Over Lee-Tsern-Matsubara-Lin-Liao-White

1. Analysis

(a) Claim 17

[17]

In Lee-Tsern-Matsubara-Lin-Liao-White, the stacked memory cell array and logic unit ICs are packaged based on Ali such that the top cover (*metal layer*) covers the stack, *i.e., is disposed over the logic unit* (see [29a]), where the top cover has “a size large enough to cover/encapsulate” the stack (and thus to cover the logic unit at the top) (*covers more than 50% area of the logic unit*) see [16]). EX1015, 3:8-9; EX1003, ¶¶309-311.

VI. PAYMENT OF FEES—37 C.F.R. §42.103

Petitioner authorizes the Patent and Trademark Office to charge any fees to Deposit Account No. 06-1050.

VII. MANDATORY NOTICES—37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest—37 C.F.R. § 42.8(b)(1)

Petitioner, Apple Inc., is the real party-in-interest.

B. Related Matters—37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the '942 Patent. The '942 Patent is the subject of civil action: *WeCrevention, Inc. v. Dell Inc. et al*, 2-25-cv-01040 (EDTX) dated Oct. 10, 2025; *WeCrevention, Inc. v. Apple Inc.*, 7-25-cv-00458 (WDTX), dated Oct. 07, 2025; *WeCrevention Inc. v. Lenovo Group Limited et al*, 2-25-cv-01008 (EDTX), dated Oct. 03, 2025; *WeCrevention, Inc. v. Apple Inc.*, 2-25-cv-00951 (EDTX) dated Sep. 16, 2025.

C. Lead And Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

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Respectfully submitted,

Dated: February 13, 2026

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,744 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 13, 2026

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 13, 2026, a complete and entire copy of this Petition for *Inter partes* Review, Power of Attorney, and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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