

DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.
2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.
3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as “MARC”) code and contain information such as a physical description of the material, metadata from the material’s publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item’s MARC record indicates the date of an item’s public availability.
5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book’s physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library’s collection, it is my experience

that an item's 008 field accurately indicates the date of an item's public availability.

6. I am familiar with the Internet Archive, a digital library accessible to the general public. Among other services that the Internet Archive makes available to the general public is the Wayback Machine, an online archive of the web. The Internet Archive's Wayback Machine service archives webpages as of a certain capture date to track changes in the web over time. The Internet Archive has been in operation as a nonprofit library since 1996 and has hosted the Wayback Machine service since its inception in 2001. During my time as a librarian, I frequently used the Internet Archive's Wayback Machine for research and instruction purposes. This includes teaching instructional classes on using the Wayback Machine to library patrons and using the Wayback Machine to research reference inquiries that require hard-to-find online resources. I consider the Internet Archive's recordskeeping to be as rigorous and detailed as other formal library recordskeeping practices such as MARC records, OCLC records and Dublin Core.
7. I have reviewed Exhibit EX1017, "Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor" by Masakatsu

Nakai, et al as published in IEEE Journal of Solid-State Circuits January 2005.

8. Attached hereto as Appendix NAKAI01 is a true and correct copy of the MARC record for IEEE Journal of Solid-State Circuits as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix NAKAI01 accurately describes the title, publisher and ISSN number of IEEE Journal of Solid-State Circuits. The Showing Results field present on page 3 of this record indicates the library's collection includes the January 2005 issue of IEEE Journal of Solid-State Circuits containing "Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor".
9. Attached hereto as Appendix NAKAI02 is a true and correct copy of "Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor" as published in IEEE Journal of Solid-State Circuits as held by the Penn State University Library. These scans were secured from the library's collection. In comparing Exhibit EX1017 to Appendix NAKAI02, it is my determination that Exhibit EX1017 is a true and correct copy of "Dynamic Voltage and Frequency Management for a Low-Power Embedded

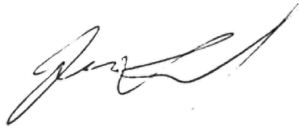
Microprocessor" by Masakatsu Nakai, et al as published in IEEE Journal of Solid-State Circuits.

10. The 008 field of the MARC record in Appendix NAKAI01 indicates the date of record creation. The 008 field of Appendix NAKAI01 indicates the Penn State University Library first acquired IEEE Journal of Solid-State Circuits as of July 18, 2000 and held the journal in perpetuity until the publication of "Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor". Considering this information, it is my determination that IEEE Journal of Solid-State Circuits January 2005 and therefore "Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor" was made available to the public shortly after its initial publication in January 2005.

11. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of \$200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

12.I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 1/30/2026

A handwritten signature in black ink, appearing to read 'June Ann Munford', with a stylized, flowing script.

June Ann Munford

APPENDIX CV

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.
- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.
- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over \$400,000 and total assets of approximately \$1,300,000.

- Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.
- Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.
- Led the organization and digitization of the library's archival records.
- Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.
- Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013

Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

- Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.
- Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.
- Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013

Library Assistant, Hart Area Public Library

Hart, MI

- Responsible for verifying imported MARC records and original MARC cataloging for the local-level collection as well as the Michigan Electronic Library.
- Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter

- Treasurer, 2012

Library Of Michigan

- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014

- New Directors Conference Panel Member

Southwest Michigan Library Cooperative

- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008

Petoskey, MI

- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011

Nashville, TN

- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012

Fairbanks, AK

- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Case No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Case No. IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (Case No. IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (Case No. IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (Case No. IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Case No. 4:21-cv-149-ALM)

2024 ● Willkie-Farr

Netflix, Inc. v. VideoLabs. Inc. (Case No. IPR2023-00628)

2024 ● Quinn Emanuel Urquhart & Sullivan

Purdue University v. Wolfsped (Case No. 1:21-CV-840)

2024 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00393)

2025 ● Perkins Coie

Amazon.com, Inc. v. Nokia Technologies Oy (Case No. IPR2024-00572)

2025 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00373)

Limited Case and Clientele History

Alston & Bird

- Ericsson

v. Collision Communications (Case No. IPR2022-01233)

- Nokia

v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

v. Roku Inc (Case No. IPR2022-00818)

Alavi & Anaipakos PLLC

- Stingray Group Inc. and Stingray Music USA, Inc.

v. Edwin A. Hernandez-Mondragon and Eglia Corp. (Case No. 1:24-cv-21226-RAR)

Arnold & Porter

- Ivantis

v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis
v. Cathx (Case No. 5:21-cv-00077-RWS)

Buchanan, Ingersoll & Rooney PC

- Google LLC, AT&T Service Inc., T Mobile USA Inc., Cellco Partnership, Ericsson Inc. & Nokia of America Corp.
v. KT Corp & Pegasus Wireless Innovation LLC (Case No. IPR2025-00293)

Deschert LLP

- Smaxtec Animal Care
v. ST Reproductive Technologies, LLC (Case No. IPR2024-00885)

Duane Morris

- Kangxi Communication Technologies
v. Skyworks Solutions Inc. (Case No. IPR2025-00373)
- Microsoft
v. Edge Networking Systems LLC (Case No. 1:24-cv-00215)

Erise I.P.

- Apple
v. Ericsson Inc. (Case No. IPR2022-00715)
v. Future Link Systems (Case No. IPRs 6317804, 6622108, 6807505, and 7917680)
v. INVT (Case No. 20-1881)
v. Navblazer LLC (Case No. IPR2020-01253)
v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

- v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)
- v. Telefonaktiebolaget LM Ericsson (Case No. IPR2022-00275)
- v. Theta IP, LLC (Case No. IPR2024-00818)
- v. THL Holding Company LLC (Case No. 1:23-cv-00548)

- Fanduel

- v. CGT (Case No. 19-1393)

- Garmin

- v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout

- v. Longhorn HD LLC (Case No. 2:20-cv-00349)
- v. Implicit, LLC (Case No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC

- v. Bot M8 LLC (Case No. IPR2020-01288)
- v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Tesla

- v. Charge Fusion Technologies LLC (Case No. IPR2025-00032)

- Unified Patents

- v. GE Video Compression (Case No. 2:19-cv-248)

Fish & Richardson

- Apple

- v. AliveCor (Case No. 3:21-cv-03958)
- v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)
- v. Koss Corporation (Case No. IPR2021-00305)

- v. Masimo (Case No. IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)
- v. Neonode (Case No. 21-cv-08872-EMC)
- v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
- v. Resonant Sys. (Case No. 7:23-cv-00077-ADA)
- AsusTek Computer Inc.
 - v. Videolabs, Inc. (Case No. 22-CV-00720-ADA)
- Dell
 - v. Neo Wireless (Case No. IPR2022-00616)
- Dish Network
 - v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)
 - v. Entropic Communications LLC (Case No. IPR2024-00393)
 - v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)
 - v. TQ Delta LLC (Case No. 18-1798)
- Evapco Dry Cooling
 - v. SPG Dry Cooling (Case No. IPR2021-00688)
- Genetec
 - v. Sensormatic Electronics (Case No. 1:20-CV-00760)
- Huawei
 - v. Bell Northern Research LLC (Case No. IPR2019-01174)
- Kianxis
 - v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics
 - v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)
- MediaTek
 - v. MOSAID (Case No. IPR2024-00718)
- Metaswitch
 - v. Sonus Networks (Case No. IPR2018-01719)
- Microsoft
 - v. Throughputer Inc (Case No. IPR2022-00757)
- Mom Enterprises
 - v. Ddrops Company (Case No. 1:22-cv-00332)
- MLC Intellectual Property
 - v. MicronTech (Case No. 3:14-cv-03657-SI)
- Nearmap Inc
 - v. EagleView Technologies (Case No. IPR2022-01009)
- Neuroderm Ltd.
 - v. Abbvie, Inc (Case No. PGR2022-00040)
- Posco Co Ltd.
 - v. Pascal Drillet et al. (Case No. IPR2025-00370)
- Realtek Semiconductor
 - v. Future Link (Case No. IPR2021-01182)

- Quectel
 - v. Koninklijke Philips (Case No. 1:20-cv-01710)
- Samsung
 - v. Aire Technology (Case No. IPR2022-00877)
 - v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)
 - v. Communication Technologies Inc (Case No. IPR2022-01221)
 - v. Jawbone Innovations (Case No. IPR2022-00865)
 - v. MemoryWeb LLC (Case No. IPR2022-00885)
 - v. Dodots Licensing Solutions (Case No. IPR2023-00701)
 - v. Telefonaktiebolaget LM Ericsson (Case No. IPR2021-00615)
- Texas Instruments
 - v. Vantage Micro LLC (Case No. IPR2020-01261)
- Xilinx
 - v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Goodwin Proctor

- Intel
 - v. Proxense, LLC (Case No. 6:24-cv-00283)
- Samsung Electronics
 - v. Mobile Data Technologies (Case No. 2:24-cv-00435)
- Taiwan Semiconductor Manufacturing Company Ltd.
 - v. Advanced Integrated Circuit Process LLC (Case No. 2:24-cv-00623)

Groombridge Wu

- Nearmap

v. Eagle View Technologies Inc. and Pictometry International Corp. (Case No. 2:21-cv-00283-TS-DAO)

Irell & Manella

- Curium

Latham & Watkins LLP

- Apple

v. Advanced Coding Research LLC

Leydig, Voit & Mayer, Ltd.

- Public Availability Consultancy

O'Melveny & Myers

- Apple

v. Maxell (Case No. 5:19-cv-00036-RWS)

- Disney Media & Entertainment Distribution LLC

v. Digital Media Technology Holdings, LLC (Case No. 2:22-cv-01642)

- Micron Technology Inc.

v. Besang Inc (Case No. IPR2023-00900)

- Samsung

v. Daedalus Prime LLC (1335 Investigation)

Perkins-Coie

- Amazon
 - v. Nokia (Case No. IPR2024-00847 and IPR2024-00848)
 - v. Nokia Technologies Oy (Case No. IPR2024-00572)
- Heru Industries
 - v. The UAB Research Foundation (Case No. IPR2022-01148)
- Intel Corporation
 - v. BeSang Inc. (Case No. IPR2023-00991)
 - v. BitMICRO (Case No. 5:23-cv-00625)
 - v. Telefonaktiebolaget L M Ericsson (Case No. IPR2024-00610)
- Realtek Semiconductor
 - v. Future Link (Case No. IPR2021-01182)
- r-pac
 - v. Adasa, Inc. (Case No. 1:2024cv06102)
- Twitter Inc
 - v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)
- TCL Industries
 - v. Koninklijke Philips NV (Case No. IPR2021-00495, IPR2021-00496 and IPR2021-00497)
- VusionGroup
 - v. Hanshow (Case No. IPR2024-00857)

Pillsbury Winthrop Shaw Pittman

- Intel

- v. FG SRC LLC (Case No. 6:20-cv-00315)

- Gravel Rating Systems

- v. Costco (Case No. 4:21-cv-149)

- v. Lowe's Home Centers (Case No. 4:21-cv-150)

- v. T-Mobile USA (Case No. 4:21-cv-152)

- v. Kohl's Inc. (Case No. 4:21-cv-258)

- v. Under Armor (Case No. 4:21-cv-356)

Quinn Emanuel

- Exact Sciences Corporation

- v. Geneoscopy, Inc. (Case No. IPR2024-00459 and IPR2024-1330)

- ServiceNow, Inc.

- v. InQuisient, Inc. (Case No. 22-900-CJB)

- Wolfsped

- v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Sheppard, Mullin, Richter & Hampton LLP

- Advanced Micro Devices, Inc and Pensando Systems, Inc.

- v. Concurrent Ventures LLC and Xtreamedge, Inc. (Case No. IPR2025-00478)

- Cadence Design Systems Inc.

- v. Semiconductor Design Technologies (Case No. 3:23-cv-01001)

Shook, Hardy & Bacon LLP

- HP Inc.

v. Universal Connectivity Technologies (Case No. 1:23-cv-01177)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

Wilmer, Cutler, Pickering, Hale and Dorr

- Apple

v. Shunock (Case No. 1:23-cv-08598)

- Quest Diagnostics Inc., Haystack Oncology Inc. and Haystack Oncology GmbH

v. Natera, Inc. (Case No. 1:23-cv-08598)

- Roche Diabetes, Inc.

v. Trividia Health, Inc. (Case No. 1:24-cv-00668)

Willkie, Farr & Gallagher LLP

- Lenovo, Dell, HP

v. Universal Connectivity Technologies Inc. (Case No. 2:2023cv00449)

- Neurent

v. The Foundry, LLC (Case No. IPR2024-00669)

- Netflix, Inc.

v. VideoLabs, Inc. (Case No. IPR2023-00628)

APPENDIX NAKAI01



Keyword



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019 a| DO NOT EDIT this 360 MARC RECORD

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030 a| IJSCBC

035 a| (WaSeSS)ssj0014481

037 b| IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854

040 a| NTD b| eng e| pn c| NTD d| OCLCQ d| NSD d| U9S d| OCLCQ d| OCLCO d| OCLCQ d| UMC d| AU@ d| UKMGB d| VT2 d| NJT d| UMC d| OCLCO d| OCLCQ d| UAB d| OCLCL d| OCLCQ d| WaSeSS

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082 1 0 a| 621 2| 13 1| https://id.oclc.org/worldcat/ddc/E4djYmFy7KK4mwFQy33t3Tt7kT

210 0 a| IEEE j. solid-state circuits b| (Online)

222 0 a| IEEE journal of solid-state circuits b| (Online)

245 0 0 a| IEEE journal of solid-state circuits h| [electronic resource].

246 3 0 a| Journal of solid-state circuits

260 a| New York, N.Y. : b| Institute of Electrical and Electronics Engineers, Inc., c| [1966]-

310 a| Monthly, b| 1991-

321 a| Quarterly, b| 1966-

362 1 a| Began with: Volume SC-1, number 1 (September 1966).

538 a| Mode of access: World Wide Web.

550 a| Issued by the IEEE Solid-State Circuits Council, <1981->; by: IEEE Solid-State Circuits Society, 1997-

588 0 a| Volume SC-1, number 1 (September 1966); title from PDF table of contents page (IEEE Xplore, viewed August 20, 2020).

588 a| Latest issue consulted: Volume 55, number 8 (August 2020) (IEEE Xplore, viewed August 20, 2020).

650 0 a| Semiconductors v| Periodicals.

650 0 a| Integrated circuits v| Periodicals.

650 0 a| Solid state electronics v| Periodicals.

655 0 a| Electronic journals.

710 2 a| IEEE Solid-State Circuits Council. 1| https://id.oclc.org/worldcat/entity/E39QQPVp7PrjrdwwBK96vvhb9t.

710 2 a| IEEE Solid-State Circuits Society. 1| https://id.oclc.org/worldcat/entity/E39QQPVp7T63PGrdTVTrYpTtWt.

776 0 8 i| Print version: t| IEEE journal of solid-state circuits x| 0018-9200 w| (DLC) 89657065 w| (OCoLC)1589745

856 4 0 u| http://SK8ES4MC2L.search.serialssolutions.com/?V=1.0&L=SK8ES4MC2L&S=JCs&C=IEEEJOUOFS&T=marc

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IEEE journal of solid-state circuits [electronic resource].

Additional Titles

IEEE j. solid-state circuits (Online) and Journal of solid-state circuits

Published

New York, N.Y. : Institute of Electrical and Electronics Engineers, Inc., [1966]-

Additional Creators

[IEEE Solid-State Circuits Council](#) and [IEEE Solid-State Circuits Society](#)

Access Online

[serialssolutions.com](#)

Dates of Publication and/or Sequential Designation

Began with: Volume SC-1, number 1 (September 1966).

Subject(s)

[Semiconductors—Periodicals](#)[Integrated circuits—Periodicals](#)[Solid state electronics—Periodicals](#)

Genre(s)

[Electronic journals](#)

ISSN

1558-173X

Grouping ISSN

0018-9200

Publication Frequency

Monthly, 1991-

Quarterly, 1966-

Technical Details

Mode of access: World Wide Web.

Issuing Body

Issued by the IEEE Solid-State Circuits Council, <1981->; by: IEEE Solid-State Circuits Society, 1997-

[View MARC record](#) | catkey: 49923886

PennState

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IEEE journal of solid-state circuits

ISSN: 0018-9200

Peer Reviewed

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APPENDIX NAKAI02

Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor

Masakatsu Nakai, Satoshi Akui, Katsunori Seno, Tetsumasa Meguro, Takahiro Seki, Tetsuo Kondo, Akihiko Hashiguchi, Hirokazu Kawahara, Kazuo Kumano, and Masayuki Shimura

Abstract—High-performance and low-power microprocessors are key to PDA applications. In this paper, a dynamic voltage and frequency management (DVFM) scheme with leakage power compensation effect is introduced in a microprocessor with 128-bit wideband 64-Mb embedded DRAM. The DVFM scheme autonomously controls clock frequency from 8 to 123 MHz in steps of 0.5 MHz and also adaptively controls supply voltage from 0.9 to 1.6 V in steps of 5 mV, achieving 82% power reduction in Personal Information Management scheduler application and 40% power reduction in MPEG4 movie playback. This low-power embedded microprocessor, fabricated with 0.18- μm CMOS embedded DRAM technology, enables high-performance operations such as audio and video applications. As process technology shrinks, this adaptive leakage power compensation scheme will become more important in realizing high-performance and low-power mobile consumer applications.

Index Terms—Delay synthesizer, dynamic frequency control (DFC), dynamic voltage and frequency management (DVFM), dynamic voltage control (DVC), embedded DRAM, leakage compensation, wideband bus architecture.

I. INTRODUCTION

DYNAMIC voltage and/or frequency control schemes have been reported in [1]–[5]. Our approach offers both dynamic frequency control (DFC) and dynamic voltage control (DVC). Clock frequency is autonomously and dynamically controlled while supply voltage is adaptively controlled resulting in the leakage power compensation effect. This dynamic voltage and frequency management (DVFM) approach achieved 82% power reduction in a Personal Information Management (PIM) application.

Handheld audio and video applications require high-performance and low-power processor hardware. In the case of a multi-application product such as a PDA, performance and power requirements vary widely, depending on the application being run. For example, the targeted power consumption for a movie application is typically 250 mW, 75 mW for an audio application, 50 mW for a schedule application, and 3 mW for standby mode.

As process technology shrinks, variation among chips' characteristics becomes larger. The fluctuations in operation speed

and power consumption also become serious. Also, the increase of power consumption by the subthreshold leakage is a critical problem for battery-driven devices. Research activity is intensive in this area [6], [7].

General methods of power reduction are voltage scaling and lowering the operating clock frequency. In our DVFM approach, clock frequency is autonomously and dynamically controlled while voltage is adaptively controlled at the same time. A delay synthesizer in the DVC circuit emulates and provides the circuit delay information while the DFC circuit determines optimum operating frequency for the microprocessor to perform desired functions efficiently. To lower the operating frequency, this microprocessor incorporates a 2-D graphics engine, a DSP core, and a 128-bit wideband bus architecture with 64-Mb of embedded DRAM.

Section II explains the design concepts used to simultaneously achieve high-performance and low-power consumption. Section III describes in detail the techniques used in our DVFM scheme to achieve low power consumption and leakage-compensation effect. Section IV reports the magnitude of power reduction achieved through use of the DVFM. Finally, Section V summarizes this work.

II. DESIGN CONCEPT

Fig. 1 shows a block diagram of this microprocessor. It has four 128-bit data-width 16-Mb embedded DRAM macros. The processor blocks are connected to the embedded DRAM by a 128-bit bus for high memory bandwidth requirements. Other devices are connected via a bus bridge to a 32-bit bus. A CPU and many peripheral blocks are connected by the 32-bit CPU bus. DSP and audio IF block for audio applications are connected via shared memory to the CPU bus. Embedded DRAM, wideband bus architecture and some hardware engines like a 2-D graphics engine and DSP not only improve audio/video performance, but also significantly reduce power consumption by reducing the required clock frequency and input/output power. The 2-D graphics engine executes image processing such as picture size conversion, efficiently. If embedded DRAM is not used, the microprocessor has to communicate with the external memory. In this case, power consumption is increased as a result of driving the external memory interface pins. Furthermore, embedded DRAM with wideband bus has higher data transfer rate than external memory, so the processor can operate at a lower frequency and supply voltage. The maximum data transfer rate of the wideband bus is 7.86 GB/s.

The DVFM block, clock generator and dc–dc IF block control the supply voltage and clock frequency. The supply voltage

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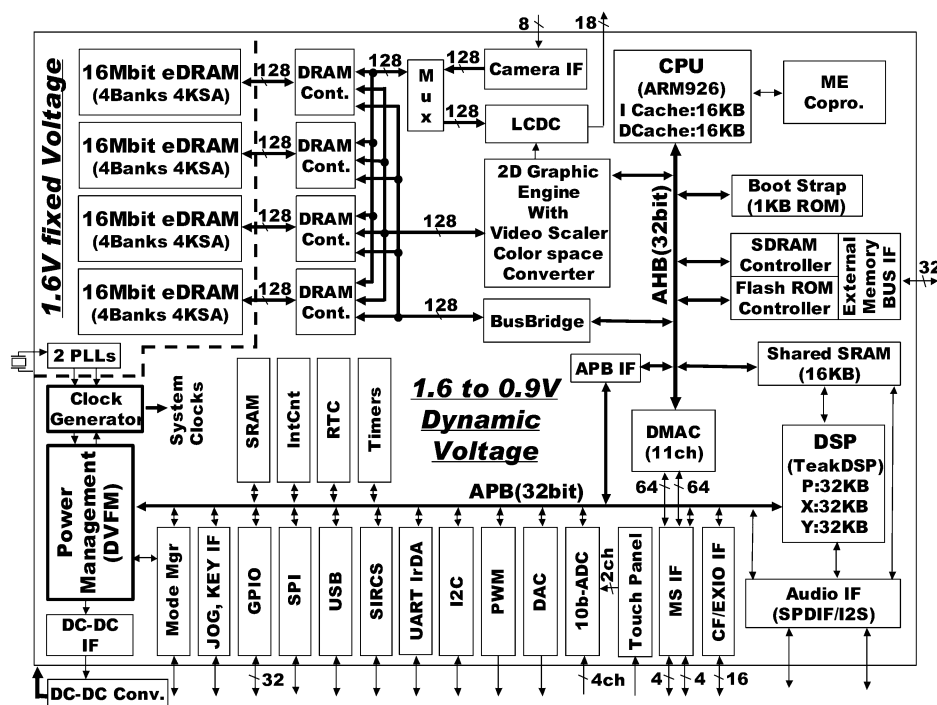


Fig. 1. LSI block diagram.

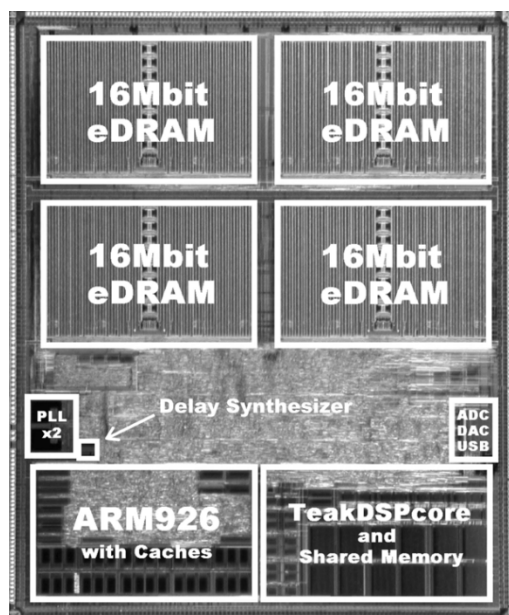


Fig. 2. Die microphotograph.

of the DRAM macros and phase-locked loops (PLLs) is fixed to 1.6 V, but the supply voltage of other logic circuit blocks is controlled dynamically by the DVFM in the range between 0.9 and 1.6 V. Peripheral circuit blocks that communicate with external devices are driven by fixed frequency clocks, but all other circuit blocks are driven by the dynamically controlled system clock. In this implementation the system clock is set between 8 and 123 MHz with a control resolution of 0.5 MHz. The embedded DRAM macros and an external SDRAM are also driven by the same system clock. The DVFM circuit block controls supply voltage and clock frequency for a large part of this LSI.

TABLE I
LSI SPECIFICATION

Technology	0.18 μ m 5-Metal CMOS (Embedded DRAM)
Voltage	3.3V, 2.5V(IO, Analog) 1.6V(OSC, PLL) 1.6V, 3.2V(eDRAM, Word line) 0.9V-1.6V Dynamic Change (Logic)
Clock	8-123MHz(CPU,CPU Bus,128bit Bus,etc.) 96, 48, 38.4, 24, 19.2, 22.5792 14.769MHz, etc. (Peripherals)
Logic	1.35Million Gate
eDRAM	64Mbit
SRAM/ROM	1.3Mbit/20kbit
Die Size	10.93mm x 13.18mm
Package	368Pin LFLGA

Therefore, our DVFM scheme is highly effective in realizing ultra-low power consumption.

Fig. 2 and Table I show the microphotograph and specification of the microprocessor. The chip is fabricated using a 0.18- μm 5-metal CMOS embedded DRAM process. The logic circuit gate count is 1.35 million and the chip size is 10.93 mm by 13.18 mm. The logic part of microprocessor is designed using standard cells, except the four embedded DRAM macros, analog cells like the PLL, and a delay synthesizer circuit which emulates the critical paths of the LSI.

III. DYNAMIC VOLTAGE AND FREQUENCY MANAGEMENT SCHEME

Fig. 3 shows the DVFM block which consists of the DFC and DVC units. The DVC emulates the critical-path characteristic

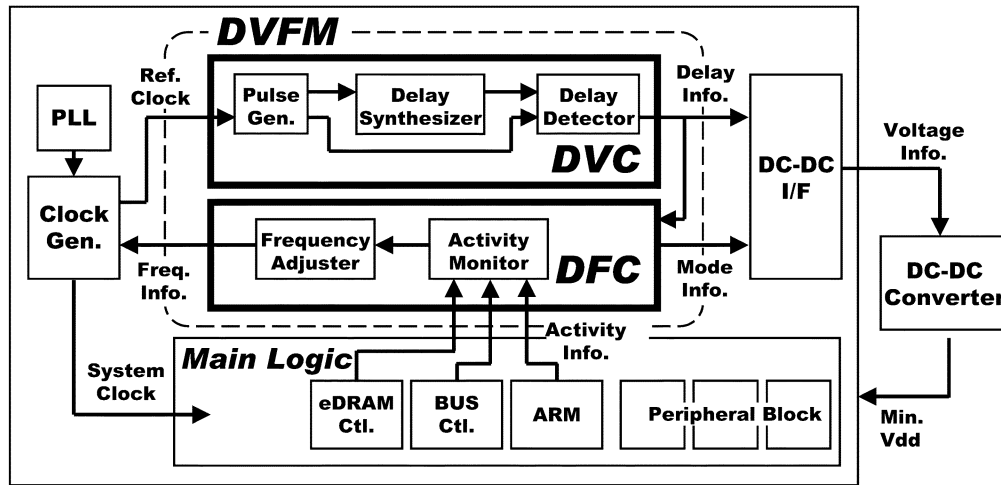


Fig. 3. DVFM block diagram.

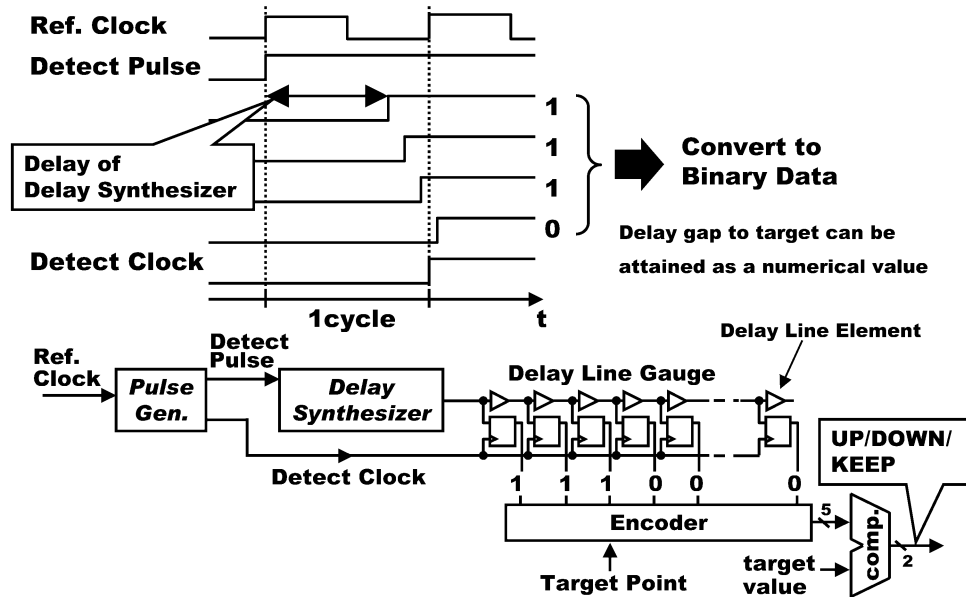


Fig. 4. Delay measurement.

using a delay synthesizer and controls the dynamic supply voltage. The DFC controls the clock frequency at the required minimum value by monitoring LSI activity autonomously. The details of each block are explained below.

A. Dynamic Voltage Control (DVC)

The DVC block consists of three major parts: the pulse generator, the delay synthesizer, and the delay detector. The pulse generator creates a detect pulse signal and also a detect clock signal as shown in Fig. 4. The detect pulse propagates through the delay synthesizer and reaches the delay detector. The delay detector consists of a delay line gauge and flip-flops. The flip-flops capture the signal from the delay synthesizer at the positive edge of the detect clock and digitizes the delay propagation. By comparing the digitized delay value with the target value, the delay detector determines whether to increase, decrease, or keep the present supply voltage value. The minimum operating voltage from 0.9 to 1.6 V at 5-mV step is supplied in real time by controlling off-chip dc-dc converter to adjust the digitized value

to target, thus maintaining LSI operation correctly at the given clock frequency. Because the delay line gauge with 5-bit output needs to detect even small delay fluctuation, each of the 32 delay line elements consists of two inverters, resulting in better sensitivity, >6 mV/digit. When supply voltage increases by 6 mV, the delay line gauge's output increases a digit. Since the delay line gauge has better sensitivity, 5-mV step voltage control is accomplished. To attain the stable control, the equivalent voltage resolution of the delay line gauge must be larger than the supply voltage resolution.

Fig. 5 shows the details of the delay synthesizer. The delay characteristic of the actual LSI is composed of not only a simple transistor delay factor, but also wire delay and other factors. The delay synthesizer consists of three programmable delay components, gate delay, RC delay, and a rise/fall delay component. The gate delay component includes two types of NAND gates, one of nominal gate length and another of long gate length. The RC delay component includes wires from each of the four metal layers and its total length is 14 mm. These three components

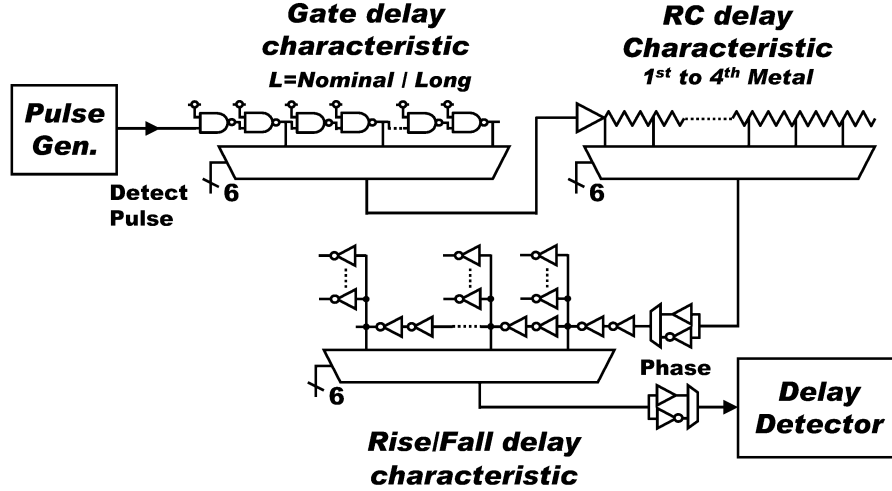


Fig. 5. Delay synthesizer.

were chosen from analyzed results of some LSI's characteristics. Use of a delay-tracking unit as a method for reproducing the circuit configuration of the critical path has been reported [8]. However, in this technique, the delay-tracking unit has to be designed for every LSI, and it cannot be reused in other LSIs. On the other hand, our delay synthesizer can emulate the critical-path's characteristics by using only three components. Desired delay characteristics can be synthesized by combining those delay factors which are controlled by 6-bit signals. Additionally, by changing these 6-bit control signals, it is also possible to emulate two or more critical paths by time-sharing. This delay synthesizer module block has the reusability as IP, and can be used in other LSI chips with the same process generation.

Fig. 6 shows the accuracy of the delay synthesizer in tracking the main logic delay. Fig. 6(a) shows the frequency-voltage characteristic with delay modeled using only nominal gate-length NAND gates. Fig. 6(b) shows the frequency-voltage characteristic achieved with our multi-component delay synthesizer circuit. Each paired line shows process deviation in Fig. 6. The solid line shows emulation characteristic, the dashed line shows the critical path's characteristic. The real LSI characteristics cannot be emulated by using only nominal gate delay without the delay synthesizer, as shown in Fig. 6(a). On the other hand, the delay synthesizer can track well within 4% voltage accuracy over the full range of process deviation and voltage, as shown in Fig. 6(b). The relation between the transistor current and the delay characteristics of each delay synthesizer's components is modeled in order to determine the parameters of the delay synthesizer. Also the characteristic of the critical path is modeled similarly. To extract the critical path's characteristic, the test vectors, which make power consumption maximum, are chosen as the critical-path access that is derived from timing analysis. Then the parameters are decided to fit the model of the critical path. The delay percentage with the parameters in the silicon were nominal gate delay 25%, long gate delay 38%, RC delay 25%, and rise/fall delay 12%. These parameters are fixed for all chips in actual manufacturing.

The most notable feature of the DVC is its ability to adapt itself to compensate for leakage power over process deviation that

becomes more pronounced as process technology shrinks. Fig. 7 shows the leakage-compensation effect achieved by using DVC. In this figure, the horizontal axis shows process deviation while the vertical axis shows measured power consumption. The solid line shows total power consumption which includes dynamic power and leakage power. The dashed line shows dynamic power consumption only. The dynamic power is constant under process deviation because supply voltage is constant. The leakage and total power increase as the threshold voltage (V_{th}) becomes lower. The DVC detects the fluctuation of circuit delay due to the process deviation, and adaptively controls the supply voltage to maintain the efficient LSI operation. When the V_{th} becomes lower, DVC reduces supply voltage, so the maximum total power consumption decreases. That is, our DVC adaptively compensates leakage power by minimizing supply voltage according to the process deviation and temperature fluctuation.

B. Dynamic Frequency Control (DFC)

The DFC consists of an activity monitor and a frequency adjuster as shown in Fig. 3. The DFC block controls the clock frequency at the required minimum value autonomously in hardware without special power-management software. The activity monitor calculates the total LSI activity periodically from activity information of embedded DRAM, bus, and CPU. The frequency adjuster circuit unit calculates the optimum clock frequency based on the activity value derived from the activity monitor to reserve the required number of inactive margin cycles within the monitoring period and indicates the next clock frequency to the clock generator. Fig. 8 shows the details of the activity monitor. The activity monitor counts the maximum value of activities from the CPU, the Bus Ctl, and the eDRAM Ctl at an arbitrary period that can be set via software.

Fig. 9 shows the frequency decision flow. In this figure, "Act" stands for the effective frequency to ensure proper operation over the current monitoring period, "Margin" the clock frequency margin to ensure proper operation, and "Step" the minimum step value for the controlled frequency. The clock frequency of the next monitoring period is a function of the

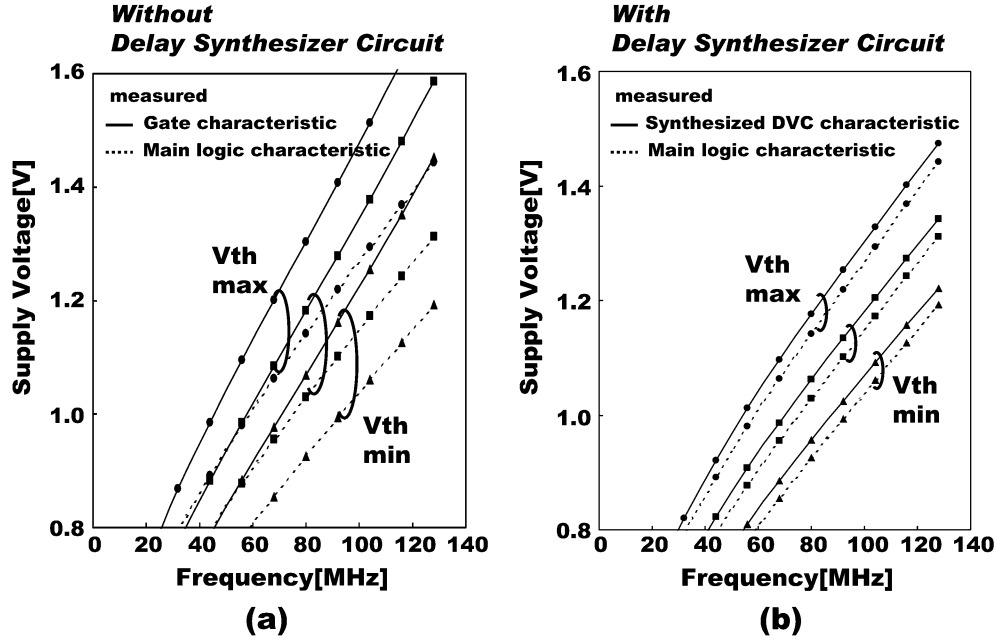


Fig. 6. Tracking characteristic.

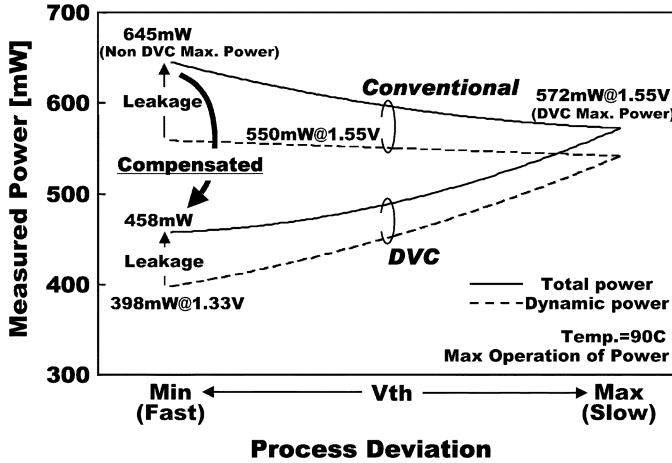


Fig. 7. Leakage-compensation effect.

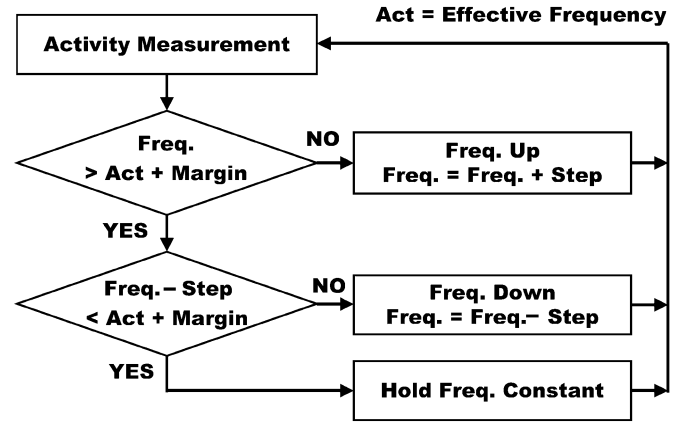


Fig. 9. Frequency decision flow.

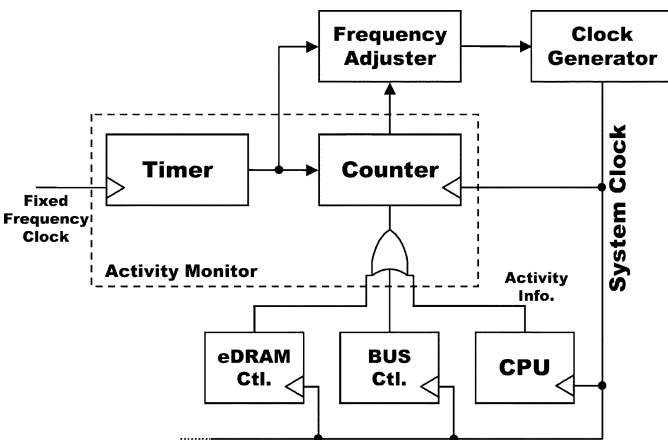


Fig. 8. Activity monitor.

activity information of the current monitoring period and the margin setting. At the end of each monitoring period, the DFC

uses the activity data to determine the required minimum clock frequency. When the clock frequency of the monitoring period just ending is less than the value of Act plus Margin, the clock frequency of the next monitoring period is increased by the Step value. On the other hand, if the current clock frequency minus the Step value is greater than the value of Act plus Margin, the next frequency is decreased by the Step value. Otherwise, the clock frequency is held constant. In actual application, normally the value of Margin is set to 2–3 MHz, and it can be changed via software. To guarantee the proper operation of applications with real-time performance requirements, it is possible to set a lower limit on the system clock frequency via software. The clock frequency may also be set directly via software to allow abrupt performance change in response to external events.

C. Frequency and Voltage Control Scenarios

Fig. 10 describes the operation of the DVFM. When the clock frequency is required to increase, the DVC reference clock is switched to the next higher frequency in advance and the DFC

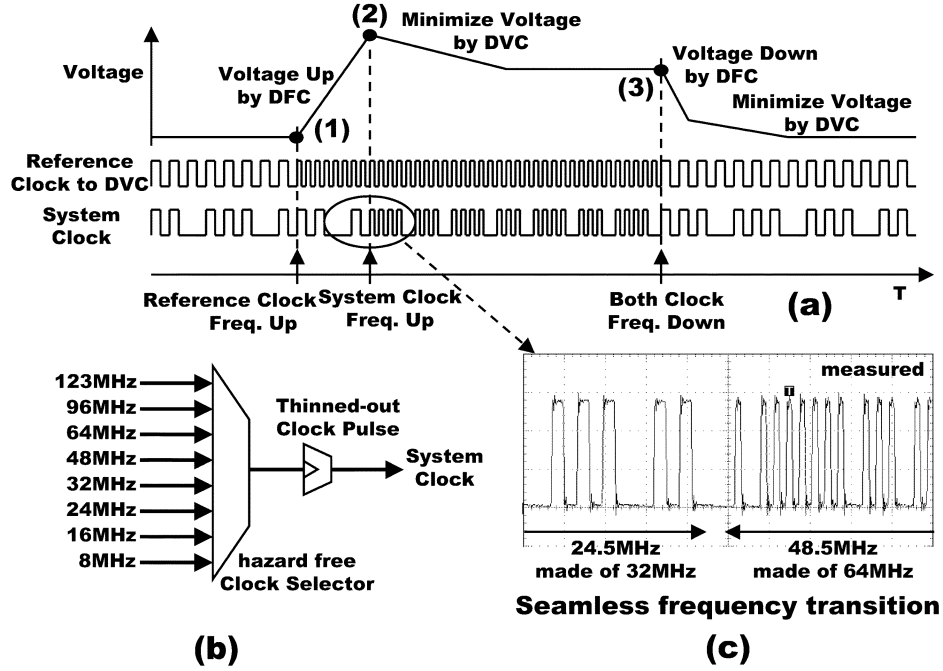


Fig. 10. Frequency and voltage control scenarios in DVFM and system clock transition.

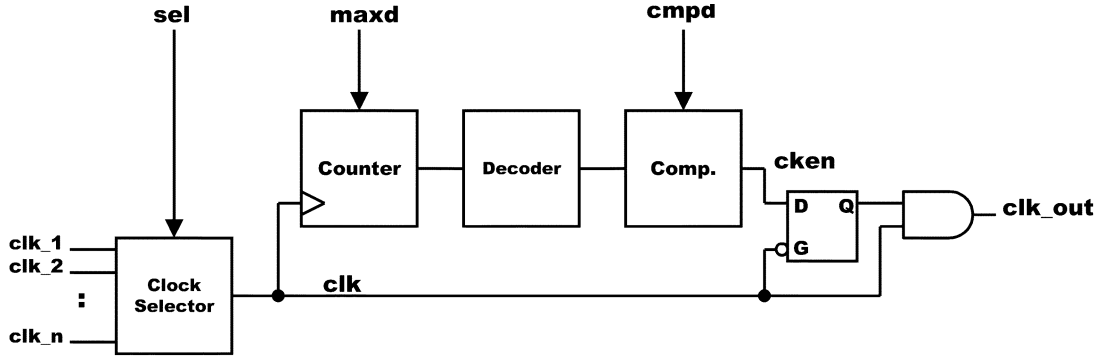


Fig. 11. Clock thinning circuit.

directs the dc–dc converter to raise the supply voltage rapidly at the point (1) in Fig. 10(a). The main logic clock frequency is changed after the DVC confirms the voltage has increased enough at the point (2) in Fig. 10(a). The feedback loop of the DVC maintains the supply voltage at the minimum level needed for device operation at current clock frequency. When the clock frequency is lowered, both the DVC reference clock and the system clock are changed simultaneously and at the same time, the supply voltage starts to decrease at the point (3) in Fig. 10(a). Since the DVC can act as the monitor of internal voltage, the safe control of the voltage and the frequency can be made easily. Note that the thinned-out clock must not be supplied to the DVC. Fig. 10(c) shows a measurement of a system clock transition from 24.5 to 48.5 MHz along with the system clock generation scheme. In this case, these thinned-out system clock frequencies of both 24.5 and 48.5 MHz were generated from 32 and 64 MHz base clocks, respectively. Fig. 11 shows the clock thinning circuit that consists of counter, decoder, comparator and clock enabler. In this figure, the “maxd” is base clock frequency and the “cmpb” is degree of thinning. For example, when 32 MHz clock is chosen and target frequency is 28 MHz, maxd is set to

32, and cmpb is set to 4. The decoder carries out equalization of the thinning period. The system clock is selected from the eight base clocks between 8 and 123 MHz, then thinned out to attain the frequency between them and is switched seamlessly from frequency to frequency as shown in Fig. 10(b). Therefore, the LSI can operate continuously without PLL relock or system reset when the clock frequency changes.

IV. POWER REDUCTION EFFECT

This section describes the power reduction effect of DVFM. Fig. 12(a) shows the power consumption in the case of MPEG4 playback. In the conventional design technique that does not use wideband bus architecture, the power consumption is 741 mW. It cannot be satisfied of the power budget as explained in Section I. The power consumption in the input/output becomes considerably reduced by introducing wideband embedded DRAM architecture. The power was reduced by 53%. Moreover, the DVFM optimizes the operating frequency and the supply voltage, resulting in the final power consumption of 210 mW, enabling long movie playback on a portable device.

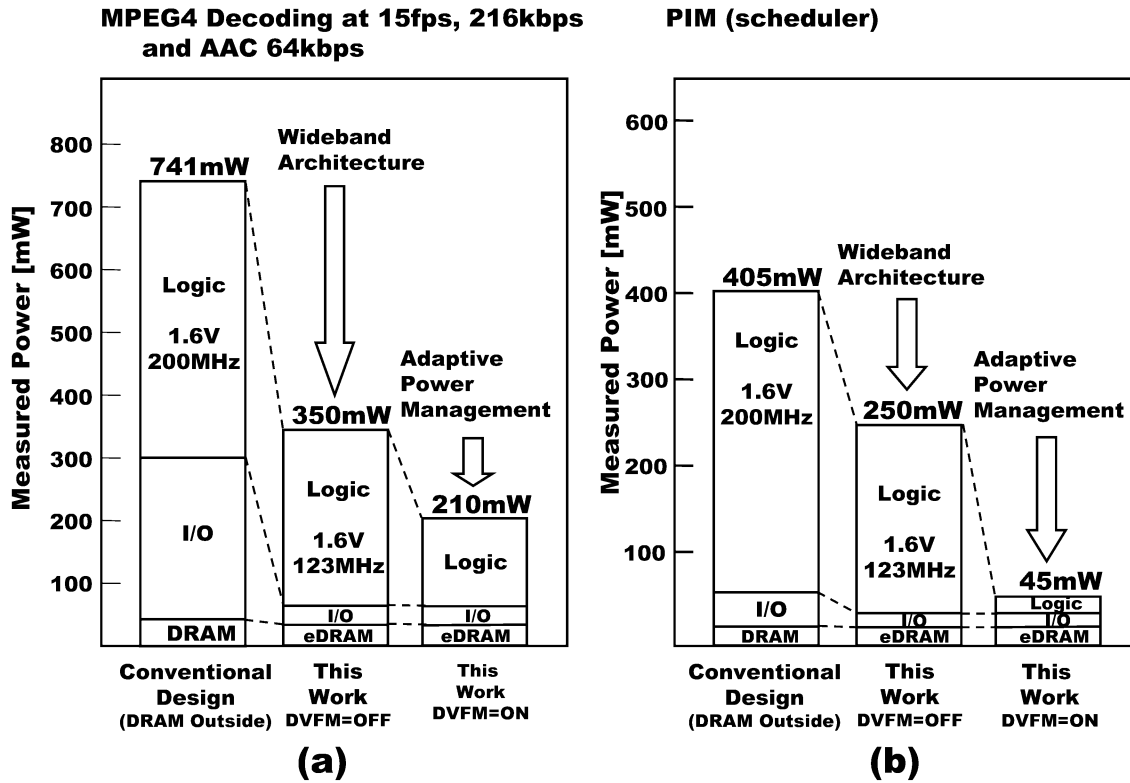


Fig. 12. Comparison of power consumption.

Efficiency loss of the external dc–dc converter is not included in this value.

Fig. 12(b) is the case of the PIM application. The power consumption in the input/output is smaller than in case of MPEG4 application because of less access to the memory blocks. Also, high-frequency operation is not needed for PIM application. At this situation, DVFM detects small activity from the hardware and, as a result, lowers the operating clock frequency to the minimum allowable value. Furthermore, the power consumption can be reduced to 45 mW by voltage optimization. Finally, 83% power reduction is achieved.

V. CONCLUSION

The DVFM scheme with leakage compensation was introduced. Our DVFM scheme autonomously controls the clock frequency from 8 to 123 MHz in steps of 0.5 MHz and adaptively controls voltage from 0.9 to 1.6 V in steps of 5-mV resolution. Our delay synthesizer can track well within 4% voltage accuracy over the full range of process deviation and voltage. The system clock is switched seamlessly from frequency to frequency. Therefore, the LSI can operate continuously without PLL relock or system reset when the clock frequency changes.

In a PIM application for a low-power embedded microprocessor, 82% power reduction was achieved. As process technology shrinks, this adaptive leakage-compensation scheme will become more important in realizing high-performance and low-power mobile consumer applications.

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REFERENCES

- [1] P. Macken *et al.*, "A voltage reduction technique for digital systems," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1990, pp. 238–239.
- [2] K. Suzuki *et al.*, "A 300 MIPS/W RISC core processor with variable supply-voltage scheme in variable threshold-voltage CMOS," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1997, pp. 587–590.
- [3] S. Sakiyama *et al.*, "A lean power management technique: The lowest power consumption for the given operating speed of LSIs," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1997, pp. 99–100.
- [4] T. Burd *et al.*, "A dynamic voltage scaled microprocessor system," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2000, pp. 294–295.
- [5] K. Nowka *et al.*, "A 0.9 V to 1.95 V dynamic voltage-scalable and frequency-scalable 32 b PowerPC processor," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2002, pp. 340–341.
- [6] K. Nose *et al.*, " V_{th} -hopping scheme to reduce subthreshold leakage for low-power processors," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 413–419, Mar. 2002.
- [7] J. Tschanz *et al.*, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1396–1402, Nov. 2002.
- [8] M. Dean, "STRiP: A Self-Timed RISC Processor," Ph.D. thesis, Dept. Electr. Eng., Stanford Univ., Stanford, CA, June 1992.



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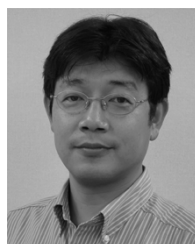
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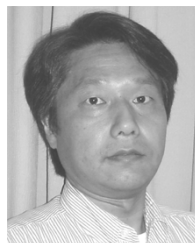


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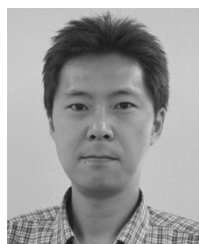
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