

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Ken et al.
U.S. Patent No.: 9,201,834 Attorney Docket No. 50095-0276IP1
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Title: RECONFIGURABLE HIGH SPEED MEMORY CHIP MODULE
AND ELECTRONIC DEVICE WITH A RECONFIGURABLE
HIGH SPEED MEMORY CHIP MODULE

DECLARATION OF DR. DAVID LIU

I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: February 13, 2026_____

By: _____

David Liu, Ph.D.

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I, David Liu, Ph.D., declare that:

I. INTRODUCTION

1. I have been retained on behalf of Apple Inc. (“Apple”) to offer technical opinions related to U.S. Patent No. 9,201,834 (“the ’834 patent”) (EX1001). I understand that Apple is requesting that the Patent Trial and Appeal Board (Board) institute an *Inter Partes* Review (IPR) proceeding of the ’834 patent.

2. I have been asked to provide my independent analysis of the ’834 patent in light of the prior art publications cited in this Declaration.

3. I am not and never have been an employee of Apple. I received no compensation for this Declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’834 patent, the prior art publications cited below, and issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’834 patent.

4. My analysis here is based on my years of education, research, and experience, as well as my investigation and study of relevant materials, including those cited in this Declaration.

5. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further,

I may consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

6. My analysis of the materials produced in this proceeding is ongoing, and I will continue to review any new material as it is provided. This Declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

7. My education and experience are described more fully in the attached curriculum vitae, provided as an appendix. For ease of reference, I have highlighted certain information below.

8. I am over the age of 18 and am competent to write this Declaration. I have personal knowledge or have developed knowledge—based upon education, training, or experience—of the technologies of the matters set forth herein.

9. My curriculum vitae (“CV”) is filed concurrently as an appendix and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My CV also includes information about my expert witness experience, with case numbers where available.

10. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

11. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

12. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. ("TI"). At TI, my job responsibilities included process integration, device modeling, high-voltage complementary metal oxide semiconductor (CMOS) process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

13. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. ("AMD") where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5 μ m and 0.35 μ m Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology to accommodate x-decoder transistors and high-voltage transistors for negative gate erase operations. While at AMD, I was awarded a Spotlight Award for developing

a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

14. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

15. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

16. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm).

17. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

18. Since 2007, I have served as a technical consultant where I have provided expert advice regarding semiconductor memory technologies, including both DRAM and Flash memory technologies; CMOS process technology, and

semiconductor device physics. As part of this, I have considered, assessed, and assisted with the design of various different memory devices, both volatile memories and non-volatile memories, including NAND flash and monolithic 3D memory structures.

19. I hold over 99 U.S. patents, a vast majority of which are directly related to Nonvolatile memory device technology. For example, U.S. Patent No. 5,250,464 relates to use of sidewall layers of silicone dioxide and silicon nitride to form a sidewall anti-fuse structure.

20. In writing this Declaration, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- U.S. Patent App. Pub. No. 2004/0260864 (“Lee”) – EX1004
- PCT App. Pub. No. WO2008/124503 (“Tsern”) – EX1005
- U.S. Patent App. Pub. No. 2010/0235554 (“Chang”) – EX1006
- U.S. Patent No. 7,785,933 (“Dozen”) – EX1007
- U.S. Patent App. Pub. No. 2011/0063927 (“Dono”) – EX1008
- “Development of 3D Stack Package Using Silicon Interposer for High-Power Application.” N. Khan *et al. IEEE Transactions on Advanced Packaging*, Vol. 32, No. 1, February 2008 (“Khan”) – EX1009
- U.S. Patent No. 6,226,755 (“Reeves”) – EX1010

- U.S. Patent App. Pub. No. 2007/0109831 (“Raghuram”) – EX1011
- U.S. Patent Pub. No. 2010/0187671 (“Lin”)
- U.S. Patent No. 8,344,496 (“White”) – EX1014
- U.S. Patent No. 6,869,829 (“Hikita”) – EX1015
- U.S. Patent No. 8,502,375 (“Liao”) – EX1016
- “Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor.” M. Nakai et al. IEEE Journal of Solid-State Circuits, Vol. 40, No. 1, January 2005 (“Nakai”) – EX1017
- U.S. Patent No. 6,184,808 (“Nakamura”) – EX1019
- U.S. Patent No. 8,895,345 (“Akiyama”) – EX1020
- U.S. Patent No. 5,848,080A (“Dahm”) – EX1021
- U.S. Patent No. 5,844,853 (“Kitsukawa”) – EX1022
- U.S. Patent Pub. No. 2008/0265378 (“Lee-378”) – EX1023
- U.S. Patent No. 8,803,322 (“Yang”) – EX1024
- U.S. Patent No. 8,405,214 (“Willey”) – EX1025
- “Application Specific Integrated Circuits (ASICs).” Martin Reiger. *The Electronic Design Automation Handbook*. Jansen, D. ed., 2003 (“Rieger”) – EX1031

21. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the ’834 Patent at the

time of the earliest possible priority date of the '834 Patent, and I have done so during my review of these materials.

22. The '834 patent has a filing date of November 2, 2012, and claims a priority date of October 11, 2011 ("the Critical Date"). Counsel has informed me that the Critical Date represents the earliest possible priority date to which the challenged claims of '834 patent are entitled, and I have therefore used that Critical Date in my analysis below. I have not assessed whether the '834 patent is entitled to the October 11, 2011 priority date.

23. I have no financial interest in the parties or in the outcome of this proceeding. I am being compensated for my work as an expert on an hourly basis. My compensation is not dependent on the outcome of these proceedings or the content of my opinions.

24. In writing this declaration, I have considered the following: my own knowledge and experience, including my work experience in electrical engineering and memory development, and my experience in working with others involved in those fields. In addition, I have analyzed various publications and materials, in addition to other materials I cite in my declaration.

25. My opinions, as explained below, are based on my education, experience, and expertise in the fields relating to the '834 patent. Unless otherwise stated, my testimony below refers to the knowledge of one of ordinary skill in the

art as of the Critical Date, or before. Any figures that appear within this document have been prepared with the assistance of Counsel and reflect my understanding of the '834 patent and the prior art discussed below.

III. SUMMARY OF CONCLUSIONS FORMED

26. This declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions, based upon my knowledge and experience and my review of the prior art publications listed above, I believe that:

- Claims 1, 2, 4 are obvious over Lee and Chang
- Claims 1, 2, 4 are obvious over Lee, Chang, and Tsern
- Claims 5, 13, 14 are obvious over Lee, Chang, Tsern, and Raghuram
- Claims 6-8, 18, 19 are obvious over Lee, Chang, Tsern, and White
- Claim 9 is obvious over Lee, Chang, and Dozen or Lee, Chang, Tsern, and Dozen
- Claim 10 is obvious over Lee, Chang, Tsern, and Dozen
- Claim 12 is obvious over Lee, Chang, Tsern, Raghuram, and White
- Claims 15, 16 are obvious over Lee, Chang, Tsern, Raghuram, and Hikita
- Claims 21, 23 are obvious over Lee, Chang, Dono, and Nakai

IV. LEVEL OF ORDINARY SKILL IN THE ART

27. In my opinion, a person of ordinary skill in the art as of the Critical Date of the '834 Patent (hereinafter a "POSITA") as of October 11, 2011 would have had at least a master's degree in electrical engineering, or a comparable field, and at least two years of professional experience working with semiconductor memory, including DRAM. Additional years of experience could substitute for an advanced-level degree (and vice versa).

28. Based on my experiences, I have a good understanding of the capabilities of one of ordinary skill. Indeed, I have worked closely with many such persons over the course of my career. From my industry experience, I am familiar with what a skilled person would have known and found predictable in the art. Furthermore, I possess those capabilities myself.

V. SUMMARY OF THE '834 PATENT

29. The '834 Patent relates to "a reconfigurable high speed memory chip module." EX1001, Abstract. This module includes "multiple memory cell array integrated circuits," with a logic unit coupled to the memory cell array ICs via a first transmission bus. *Id.* The logic unit is also coupled to a second transmission bus. *Id.*, claim 1. Both of the transmission buses have a "programmable transmitting or receiving data rate" and a "programmable transmitting or receiving signal swing." *Id.* But the configuration of the memory chip module claimed in

the '834 Patent was not new, nor was the concept of programmable signal swings and data rates on transmission buses of a memory chip module, as I will demonstrate here.

VI. PRIOR ART ANALYSIS

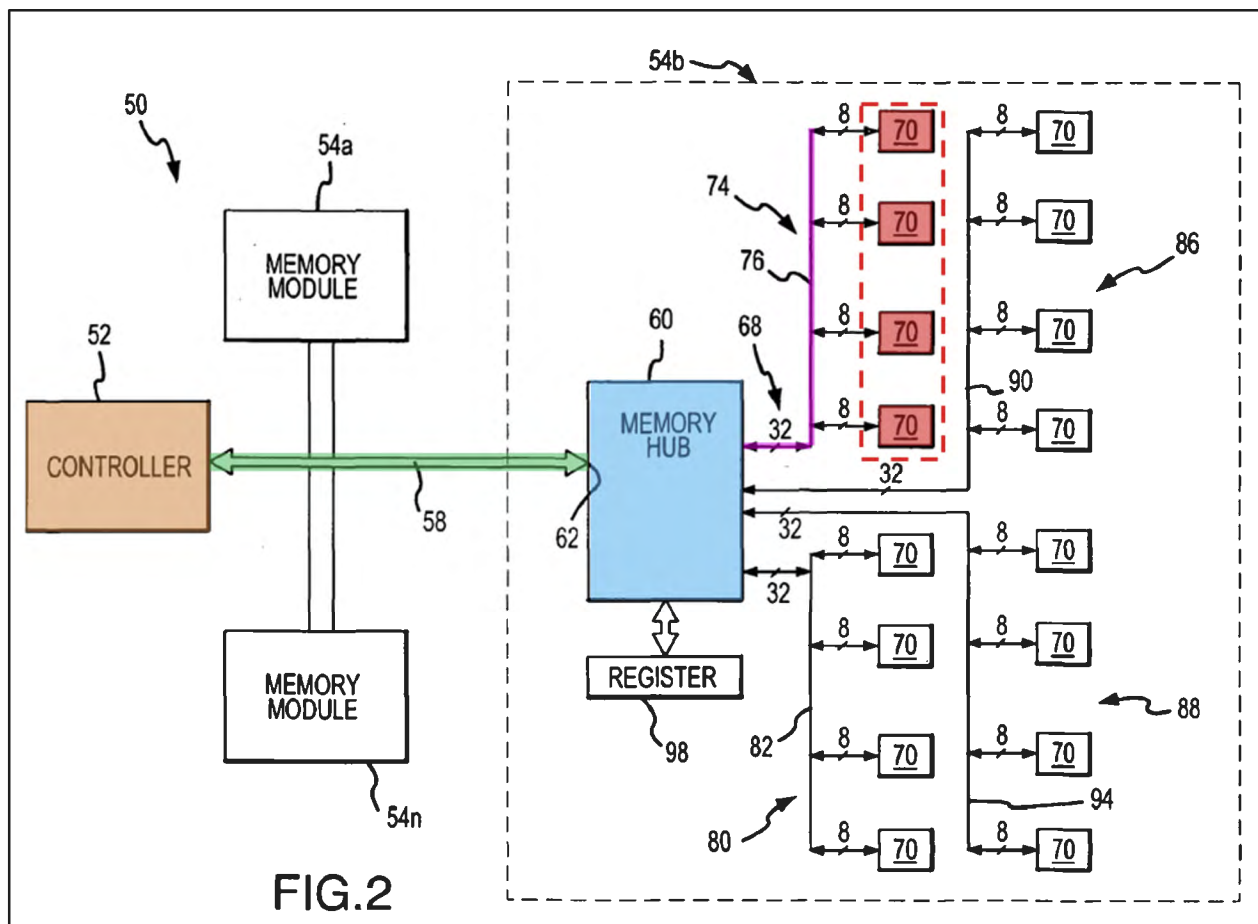
A. [Ground 1A] Lee and Chang Render Obvious Claims 1, 2, and 4

1. Lee

30. Lee describes a memory system that includes a memory module that is configurable “in a plurality of data formats each corresponding to a respective number of ranks of memory devices that are simultaneously addressed.” EX1004, [0009]. For instance, “[w]hen programmed for a high bandwidth, the memory hub simultaneously accesses the memory devices in all of the ranks,” and “[w]hen programmed for a high memory depth, the memory hub accesses the memory devices in only one of the ranks at a time.” *Id.* The configurability of Lee’s memory module allows “the data format [to be] optimized for a particular application being executed in a computer system or other electronic system containing the memory system.” *Id.*, [0020].

31. FIG. 2, *infra*, illustrates such a memory system. *See* EX1004, [0015]. In this system, a controller 52 (orange) is “coupled to several memory modules 54*a, b ... n* through a high-speed link 58” (green). *Id.* Specifically, each memory module 54 “includes a memory hub 60 [blue] ... coupled to the high-speed link 58 and a bus system 68 coupled to several memory devices 70,” *e.g.*, DRAM. *Id.* In

Lee's architecture, "the memory devices 70 are divided into four groups or 'ranks' [each] coupled to the memory hub 60 through a respective bus system." *Id.*, [0016]. For instance, the four memory devices 70 in the first rank 74, indicated in red, are "coupled to the memory hub 60 through a first bus system 76" (pink). *Id.* Similarly, the memory devices in the other ranks 80, 86, 88 "are each coupled to the memory hub 60 through respective bus systems" 82, 90, 94. *Id.*



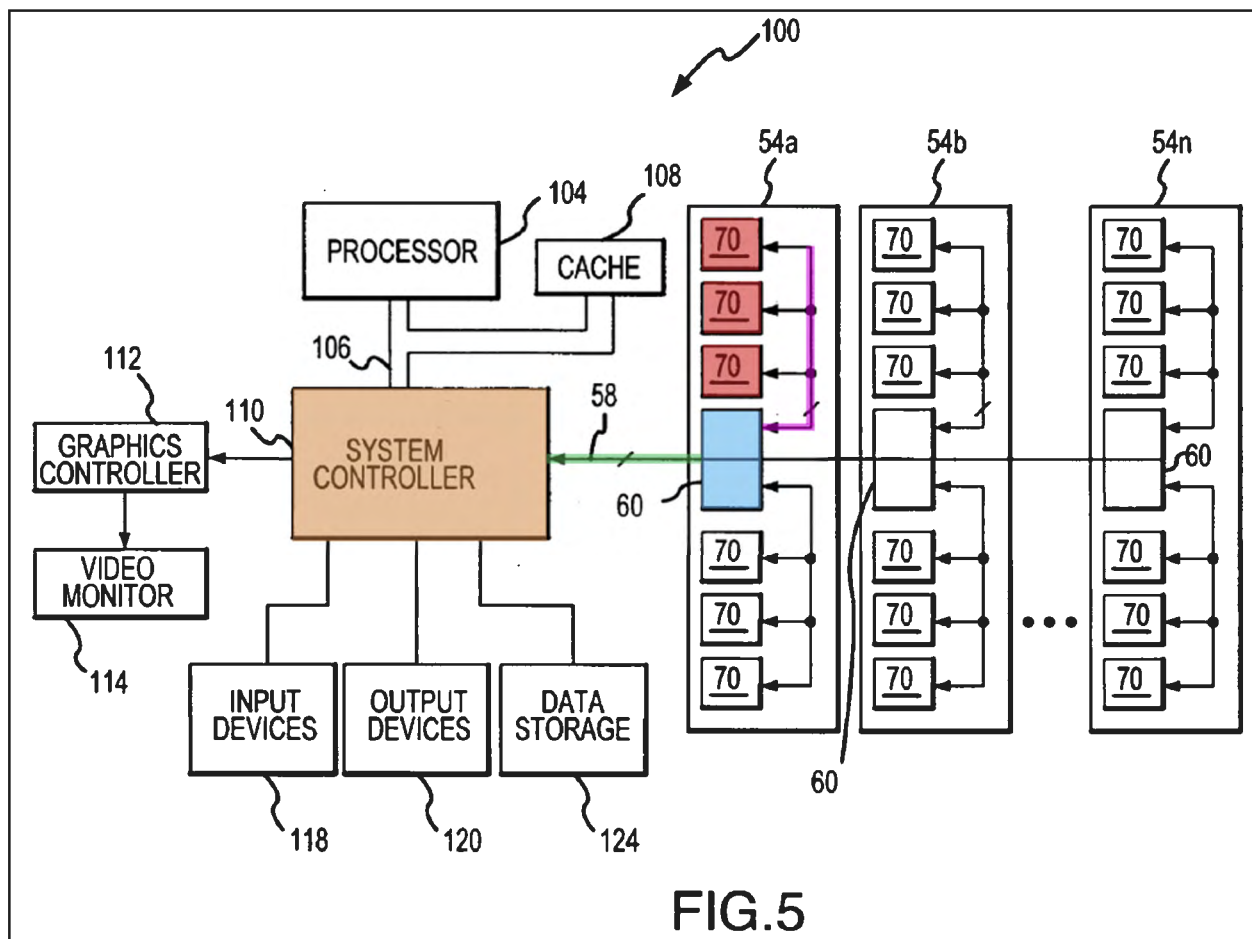
Excerpt from Lee, FIG. 2 (annotated)

32. Lee describes the configurability of its memory system: "In operation, a non-volatile register 98 in the memory module 54 is programmed to configure

the memory hub 60 depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]. First, in the “high memory bandwidth” mode, “the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access.” *Id.* These “128 bits of data” from all of the memory devices 70 “can be coupled through the high-speed link 58 by either increasing the speed of the link 58 or the size of the data word coupled through the link 58,” *e.g.*, such that “in the high-speed mode, a 128-bit data word may be coupled through the link 58,” or “[a]lternatively, the link 58 may transfer only a 32-bit data word, but it may operate at four times the speed of the memory devices 70.” *Id.* Second, in the “high memory depth mode, only one rank 74, 80, 86, 88 may be addressed at a time.” *Id.*, [0018]. In this mode, “only 32 bits of data will be coupled to or from the memory module 54 with each memory address,” but “the address space is 4 times deeper than the address space in the high bandwidth mode.” *Id.*

33. Lee’s FIG. 5, *infra*, illustrates a computer system implementing Lee’s configurable memory system 50. *See* EX1004, [0023]. In this system, the controller that is coupled to the memory hubs 60 of the memory modules 54 is a “system controller 110” (orange). EX1004, [0025]. The system controller

facilitates access to the memory modules by the processor 104 of the computer system. *Id.*.



Excerpt from Lee, FIG. 5 (annotated)

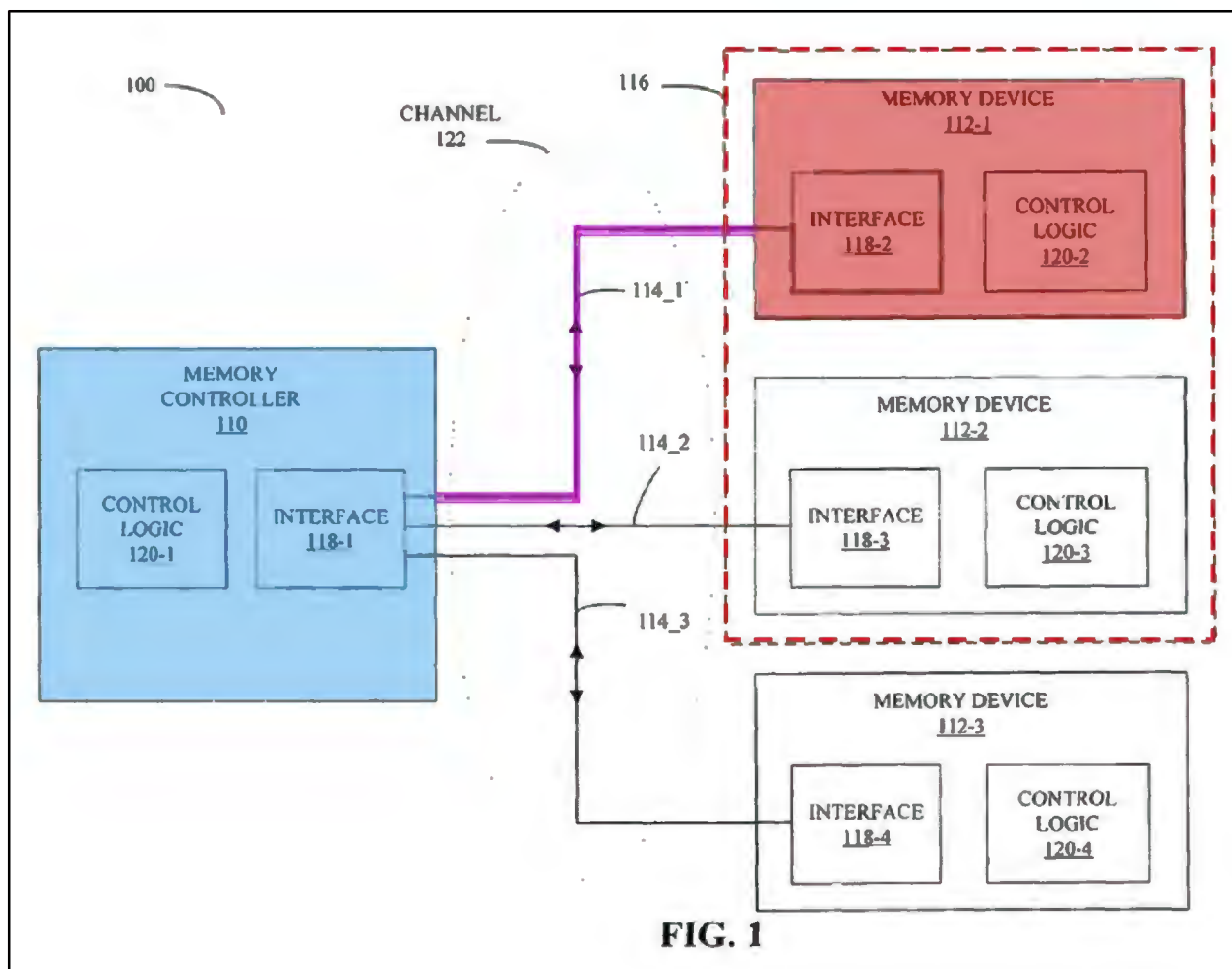
34. Lee is from the same field of endeavor (*e.g.*, memory systems) as the '834 Patent. *See* EX1001, 1:28-33; EX1004, [0001].

35. Also, Lee is pertinent to the problem the '834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”).

See EX1001, 1:28-33; EX1004, [0001]. For instance, Lee’s memory systems are architected to enable high speed, configurable memory access, which is relevant to development of “high speed” memory systems with “higher data transmission efficiency.” *See* EX1004, [0016]-[0017]; EX1001, 1:28-33.

2. Chang (EX1006)

36. Chang describes a “memory system 100” that includes “at least one memory controller 110,” highlighted in blue in FIG. 1, below. EX1006, [0020]-[0021]. For instance, the memory controller can be “a local memory controller (such as a DRAM memory controller.” *Id.* The memory system also includes “memory devices 112” (one highlighted in red) that are “configured as a memory bank 116.” *Id.*, [0023]. The “[m]emory controller 110 and memory devices 112 are coupled by one or more links 114 in a channel 122” for transmission of “[s]ignals corresponding to data and/or commands.” *Id.*, [0024]-[0025].

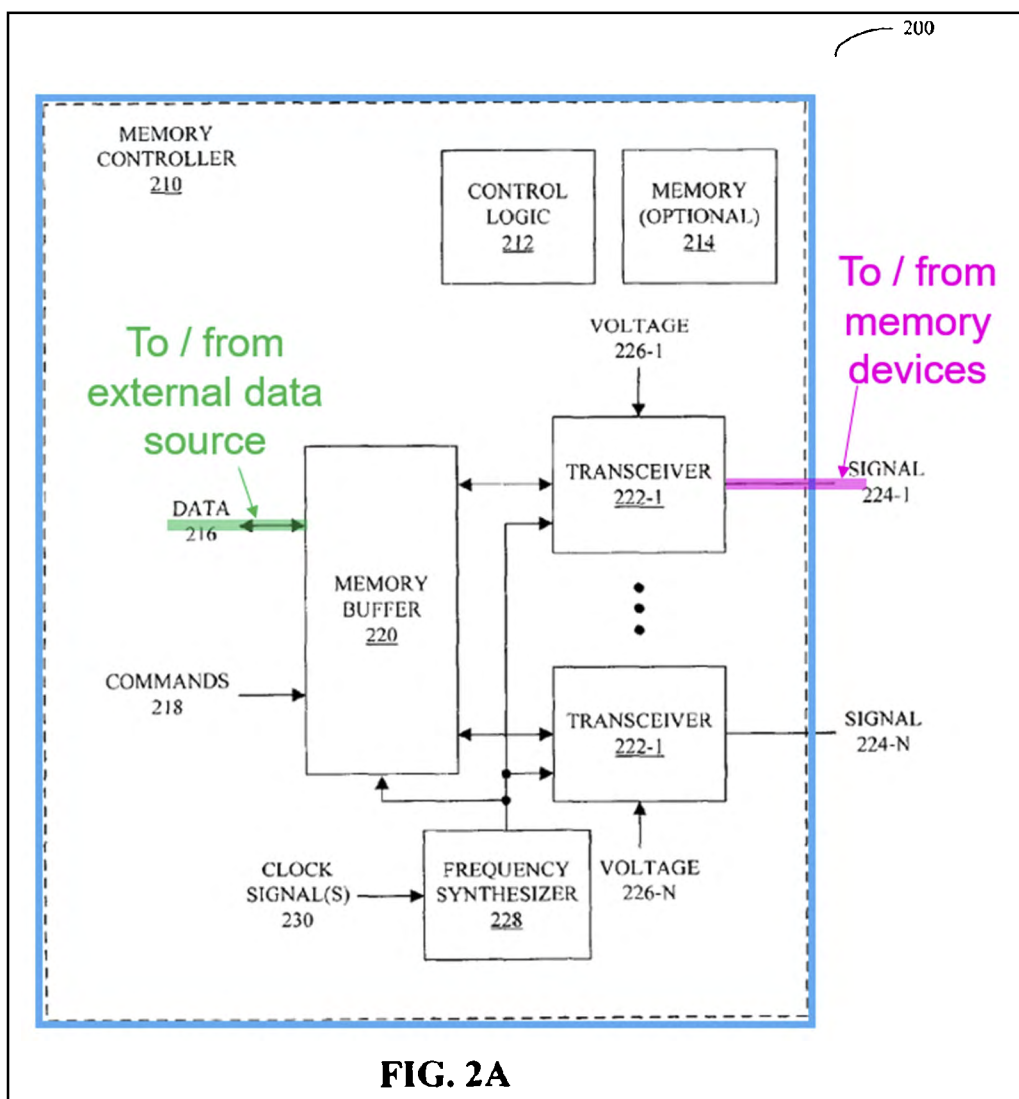


Excerpt from Chang, FIG. 1 (annotated)

37. Chang describes approaches for “error detection and/or correction.” EX1006, [0035]. For instance, “control logic 120 in the memory controller 110 and/or one of the memory device 112 may take a variety of remedial actions in the event of an error or a degradation of one or more of the performance metrics during communication between the memory controller 110 and one or more of the memory devices 112.” *Id.*, [0036]. These remedial actions include “re-transmitting previous data; transmitting previous or new data ... using an increased

transmission power than the transmission power used in a previous transmission; reducing the data rate in one or more of the sub-channels relative to the data rate used in a previous transmission; transmitting data with reduced intersymbol interference ...; adjusting a period of the one or more timing signals,” among others. *Id.*, [0036].

38. Chang’s memory controller is illustrated in more detail in FIG. 2A, which I have reproduced below. Chang describes that “[d]ata 216 to be transmitted by the memory controller 210 to a memory device (such as one of the memory devices 112 in FIG. 1) is temporarily stored in memory buffer 220 ..., forwarded to transceivers 222, and is transmitted as (analog or digital signals) 224.” EX1006, [0042]. That is, data 216 is received from an external data source is handled in the memory controller and then transmitted to the memory devices, *e.g.*, via links 114. I have marked the data received at the memory controller in green, and the transmission of data from the memory controller 210 to a memory device in pink.



Excerpt from Chang, FIG. 2A (annotated)

39. Chang describes that “voltage levels and/or a voltage swing of the signals 224 that are transmitted” to the memory devices “may be based on voltages 226 provided by a power supply.” EX1006, [0045]. Similarly, “logic levels of the data that is received” at the memory controller from an external data source “may be based on voltages 226 provided by the power supply.” *Id.* Chang describes that “[t]hese voltages may be fixed or may be adjustable.” *Id.* That is, the voltage

levels / voltage swing of the data communicated between the memory controller and the memory devices (indicated in pink in FIG. 2A above) are, in some cases, based on an adjustable power supply voltage. Likewise, the logic levels of the data received by the memory controller (indicated in green in FIG. 2A above) are, in some cases, also based on an adjustable power supply voltage. I understand Chang's reference to "logic levels" to refer to the value (*e.g.*, voltage value) of a logical "1" and "0," such that Chang's disclosure of logic levels being based on an adjustable power supply voltage indicates that the voltages of the logical "1" and "0" (*i.e.*, the signal swing) are based on that adjustable power supply voltage.

40. Chang is from the same field of endeavor (*e.g.*, memory systems) as the '834 Patent. *See* EX1001, 1:28-33; EX1006, [0001]

41. Also, Chang is reasonably pertinent to the problem the '834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, "lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability"). *See* EX1001, 1:28-33; EX1006, [0001]. For instance, Chang's memory systems "may be dynamically configured (*e.g.*, reprogrammed)", which is relevant to development of efficient memory systems. *See* EX1006, Abstract.

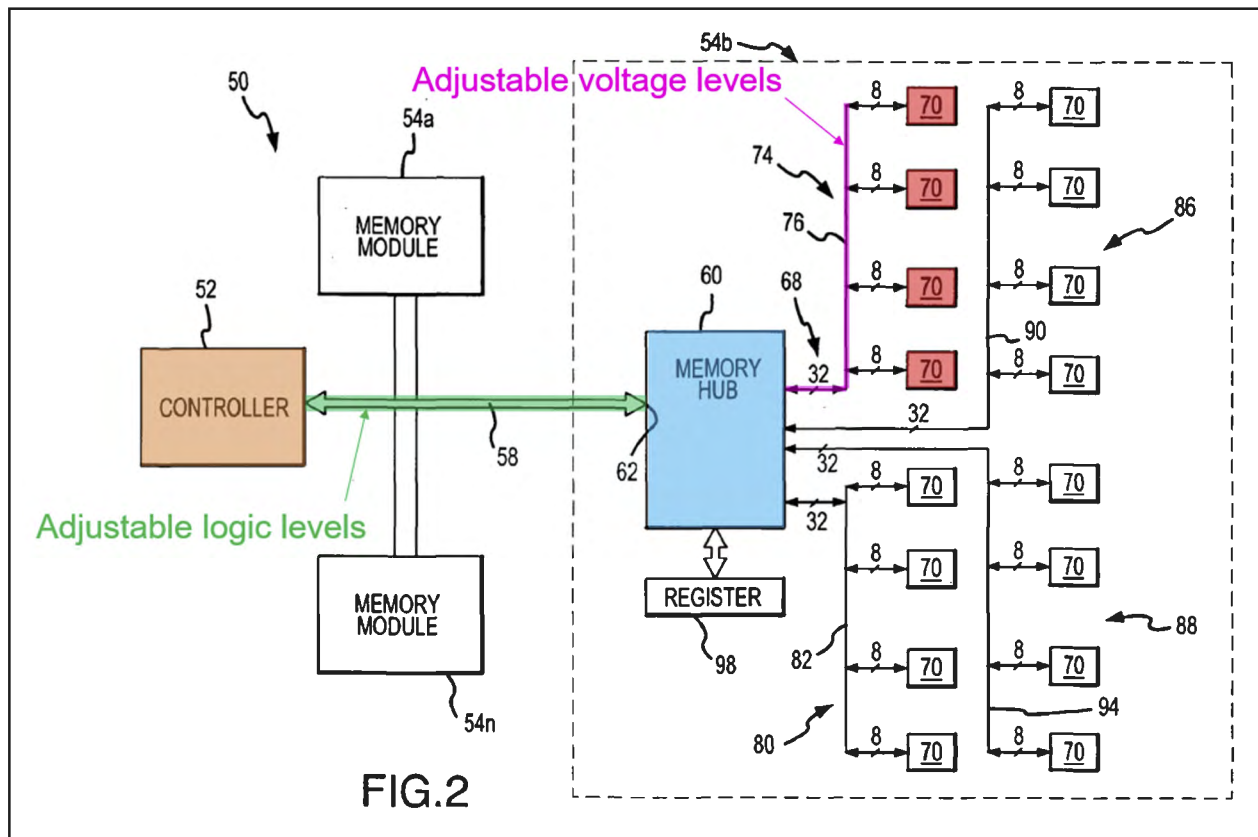
3. The Lee-Chang Combination

42. A system based on the combination of Lee and Chang uses the structure of Lee's memory system 50 as a starting point. *See*, for instance, the illustrations in Lee's FIGS. 2 and 5. Specifically, consistent with Lee's system, "memory devices 70" are divided into four groups or 'ranks' coupled to the memory hub 60 [blue] through a respective bus system." EX1004, [0016]. The memory hub is also coupled to a memory controller through a "high-speed link 58." *Id.* The memory system is operable in "high memory bandwidth" or "high memory depth" mode, consistent with the functionality of Lee's system. EX1004, [0017].

43. In the combination, data transmission characteristics along the various bus systems are based on teachings of Chang, as I have illustrated in the composite figure below.

44. For instance, Chang describes that "[d]ata 216 to be transmitted by the memory controller 210 to a memory device" can have "logic levels" that are "based on voltages 226 provided by [a] power supply," where the "voltages may be fixed or may be adjustable." EX1006, [0042], [0045]. Chang's data 216 are data provided from an external data source to Chang's memory controller, which is a configuration analogous to data provided to Lee's memory hub 60 along the high-speed bus 58. In the combination, based on this similarity, the data

transmission characteristics of the high-speed bus 58 are based on these teachings of Chang. Specifically, the “logic levels” (*e.g.*, signal swing, as I discussed above) of the data transmitted along the high-speed bus 58 in the combination system are based on “fixed or ... adjustable” “voltages [] provided by [a] power supply,” as taught by Chang. EX1006, [0045].



Lee-Chang composite figure based on Lee, FIG. 2

45. Chang also describes that “voltage levels and/or a voltage swing of the signals 224 that are transmitted” to the memory devices “may be based on voltages 226 provided by a power supply,” where again, the power supply “voltages may be fixed or may be adjustable.” EX1006, [0045]. Chang’s signals

224 are data transmitted from Chang's memory controller to the memory devices, which is a configuration analogous to data transmitted along Lee's bus systems 76, 82, 90, 94 from the memory hub 60 to the memory devices 70. In the combination, based on this similarity, the "voltage levels and/or a voltage swing of the signals" of the data transmitted along the bus systems 76, 82, 90, 94 between memory hub 60 and memory devices 70 are based on "fixed or ... adjustable" "voltages [] provided by the power supply," as taught by Chang. EX1006, [0045].

46. Data rate characteristics of the various bus systems in the combination system are also based on Chang. Chang describes "reducing the data rate" of a transmission channel between memory controller and memory devices as a remedial action in response to an error or degradation in performance metric. EX1006, [0036]. This transmission channel on which the data rate can be reduced is analogous to the bus systems 76, 82, 90, 94 in the combination system that connect the memory hub to the memory devices. In the combination, based on this similarity, the data rate for data transmission along one or more of the bus systems 76, 82, 90, 94 is "reduc[ed] ... relative to the data rate used in a previous transmission" as a "remedial action[] in the event of an error or a degradation of one or more of the performance metrics," based on Chang. EX1006, [0036].

4. Motivation to Combine and Expectation of Success

47. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement programmable voltage swing in the bus systems of the Lee-Chang combination.

48. First, a POSITA would have been motivated to implement programmable signal swing in the Lee-Chang combination because adjusting voltages “based on one or more performance metrics associated with communication to and/or from” the memory hub advantageously allows for real-time responsiveness to operating conditions. Chang, [0046]. For instance, the ability to adjust voltage (and thus signal swing) based on operational status allows for selection of a voltage that is best suited to the operational situation. This can facilitate continuous, efficient, and low-error operation of the memory system.

49. Second, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (specifically, adjustable signal swing on transmission buses in a memory system) by a known system (Lee’s memory system), and it yields predictable results (namely, a memory system in which signal swing is adjustable on transmission buses of the system).

50. A POSITA would have had a reasonable expectation of success in pursuing this implementation because memory system technology is predictable.

Moreover, a POSITA would have expected success because Chang's disclosure of adjustable signal swing is in the context of a memory system that is structured similarly to Lee's system, *e.g.*, with a memory controller / memory hub connected between an external data source and multiple memory devices.

51. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement programmable data rate in the bus systems of the Lee-Chang combination.

52. First, a POSITA would have been motivated to implement programmable data rate in the Lee-Chang combination because doing so is a mechanism to implement a "remedial action[]" responsive to "an error or a degradation of one or more of the performance metrics during communication between" the memory hub and the memory devices of the combination. EX1006, [0036]. Implementation of remedial actions facilitates continuous and low-error operation of the memory system, *e.g.*, by providing a mechanism for continued operation of the system even in the face of an error condition or problematic performance metric.

53. Second, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (specifically, adjustable data rate on transmission buses in a memory system) by a known system (Lee's memory system) to yield predictable results (namely, a

memory system in which data rate is adjustable on transmission buses of the system).

54. A POSITA would have had a reasonable expectation of success in pursuing this implementation because memory system technology is predictable. Moreover, a POSITA would have expected success because Chang's disclosure of adjustable data rate is in the context of a memory system that is structured similarly to Lee's system, *e.g.*, with a memory controller / memory hub connected between an external data source and multiple memory devices.

5. Analysis of claims

55. For the reasons below, claims 1, 2, and 4 are obvious over Lee and Chang.

(a) Claim 1

[1pre] A reconfigurable high speed memory chip module, comprising

56. The computer system of the Lee-Chang combination includes a "memory system 50" that is illustrated in FIG. 2, reproduced below. The memory system "includes a controller 52 coupled to several memory modules 54*a, b ... n* through a high-speed link 58," where each memory module includes "memory devices 70," such as "dynamic random access memory devices ('DRAMs')." *Id.*, [0015]-[0016], [0023]; *see* Abstract ("A computer system includes a controller coupled to a plurality of memory modules"), [0014] ("FIG. 5 is a block diagram of

through the high-speed link “at a rate of 2 GB/sec,” “1 GB/sec,” or “500 B/sec.” EX1004, [0017]. Given this description of the high-speed nature of Lee’s system, Lee’s memory modules can be considered *high speed memory modules*, as claimed.

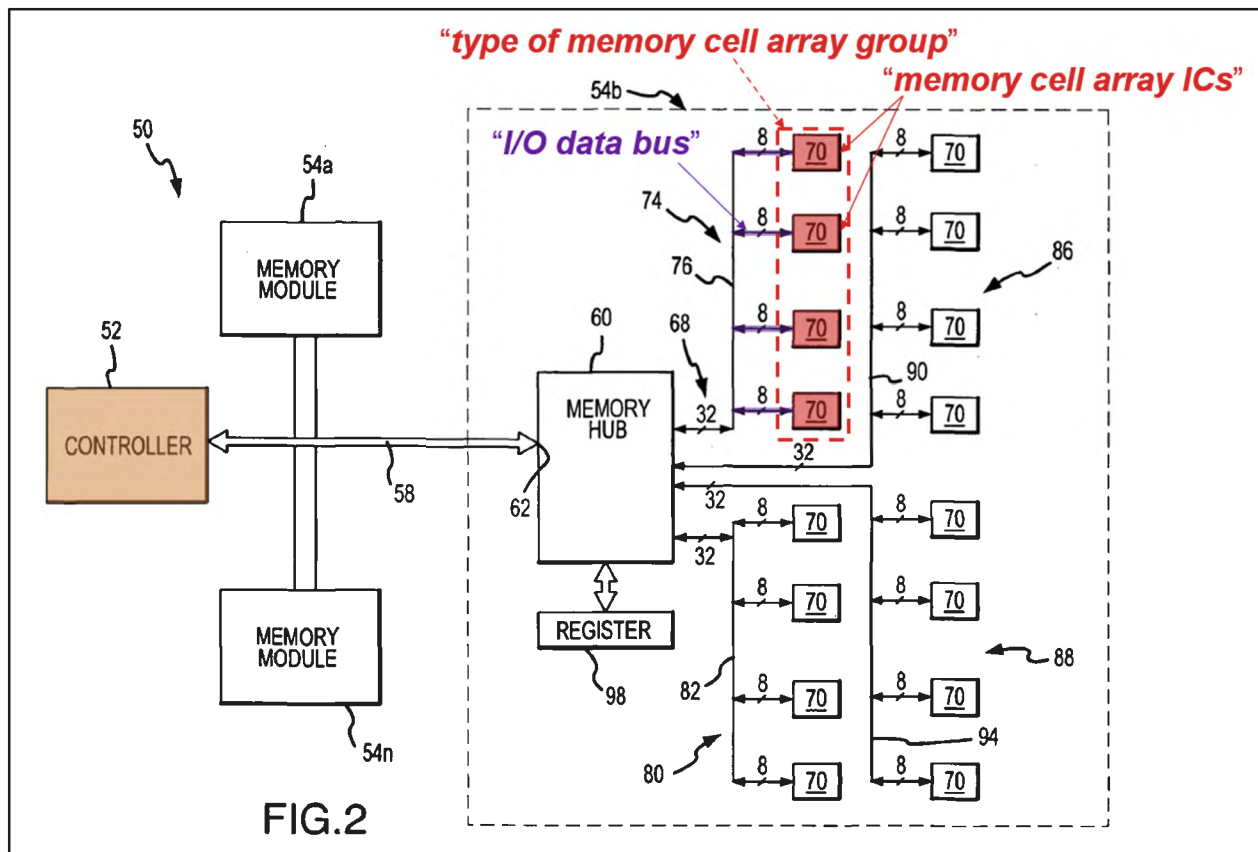
58. The memory chip module of the combination is *reconfigurable*, consistent with Lee’s teachings that the memory hub can be “configure[d] ... depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]. A reconfigurable memory system has advantages: “By allowing the memory hub 60 to configure the data format of the memory module 54, the data format can be optimized for a particular application being executed in a computer system or other electronic system containing the memory system 50. For example, when executing a graphics intensive application like a video game, the memory system 50 can be configured in the high bandwidth mode. When a computer system is executing a database application, for example, the memory system 50 can be configured in the high memory depth mode. The data format is therefore not fixed as in conventional memory systems.” *Id.*, [0020]).

[1a] a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array integrated circuits (ICs);

59. In the Lee-Chang combination, based on Lee, the memory system includes “several memory modules 54*a, b ... n*,” with each memory module

including “memory devices 70 [] divided into four groups or ‘ranks.’” EX1004, [0016]; *see* Abstract (“a plurality of memory modules each of which includes ... a plurality of memory devices divided into a plurality of ranks”), claim 1, claim 13, claim 28, FIG. 5.

60. Lee’s memory devices 70 (some of which I have highlighted in red in FIG. 2, reproduced below) correspond to the *memory cell array ICs* of claim 19. For instance, this is because Lee’s memory devices 70 are integrated circuit memory devices: “The memory devices 70 may be, for example, dynamic random access memory devices (‘DRAMs’) or some other type of memory devices.” EX1004, [0016]; *see* claim 11 (“the memory devices comprises dynamic random access memory devices”), claim 12. DRAM devices (as well as other types of memory devices) are *integrated circuits (ICs)*. For instance, Tsern refers to “[i]ntegrated circuit memory devices” such as DRAM, SRAM, and flash memory. EX1005, 12. And Liao describes “memory die such as NAND flash memory die ... [or] other types of semiconductor die ... such as for example NOR, DRAM and various other memory die.” EX1016, 4:56-60.



Excerpt from Lee, FIG. 2 (annotated)

61. In Lee's system, "the memory devices 70" (corresponding to the claimed *memory cell array ICs*) "are divided into four groups or 'ranks.'" EX1004, [0016]. I have outlined one group in dashed red lines in FIG. 2. Each group/rank of memory devices corresponds to the claimed *type of memory cell array group* that *comprises multiple memory cell array ICs* at least because it is a group of memory cells (e.g., a group of memory devices 70). For instance, "a first rank 74" (outlined in red) "includes four memory devices 70" (i.e., four *memory cell array ICs*). EX1004, [0016]. Similarly, each of the second rank 80, third rank 86, and fourth rank 88 is a type of memory cell array group that contains four

memory devices, *i.e.*, a ***type of memory cell array group*** that ***comprises multiple memory cell array ICs***. *See id.*, [0016], claim 13 (“a plurality of memory devices arranged in a plurality of ranks”), claim 1, claim 28, FIG. 5. Alternatively or additionally, the multiple groups/ranks together (*i.e.*, the first, second, third, and fourth ranks together) correspond to a ***type of memory cell array group***.

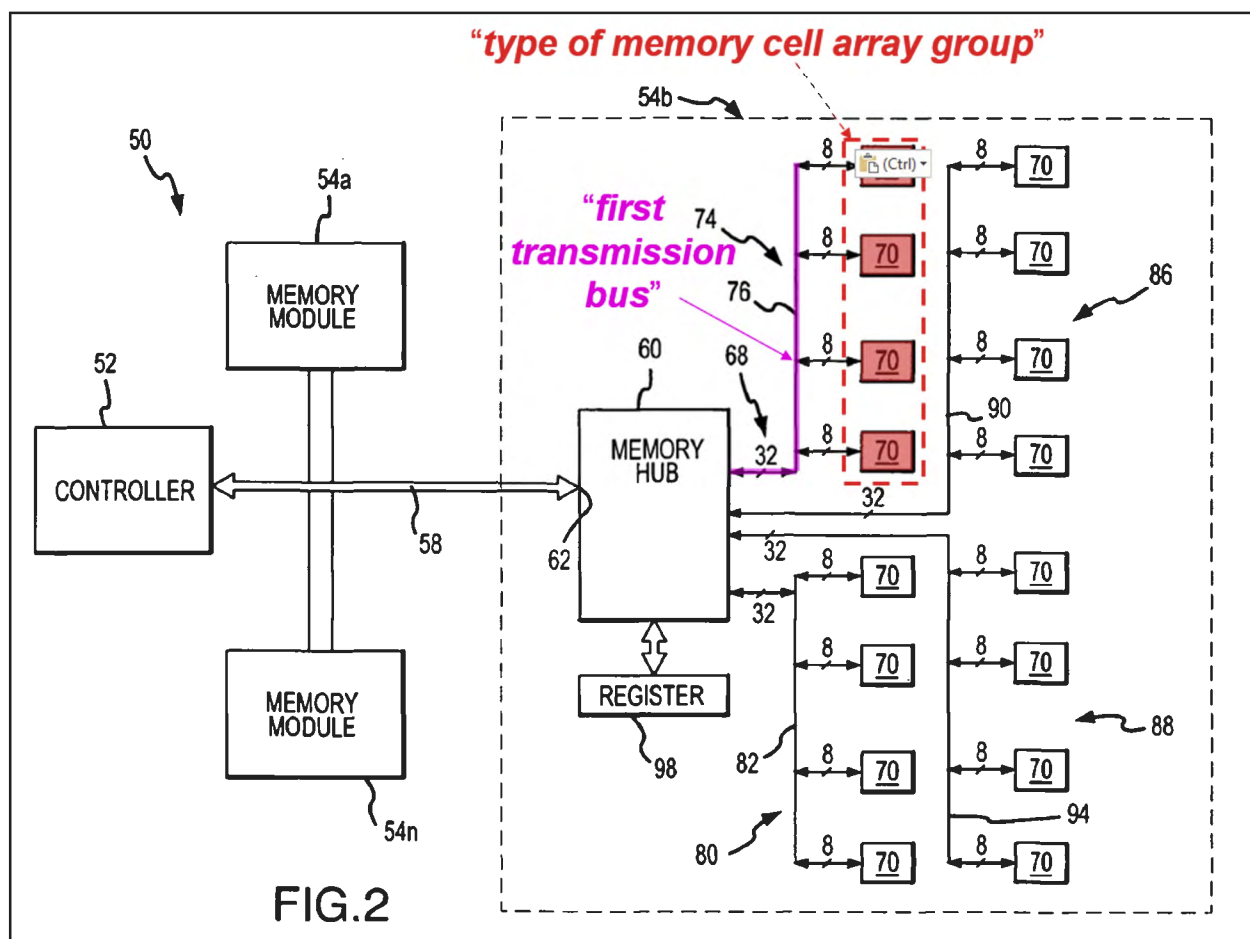
[1b] a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing;

62. Based on Lee, a memory hub 60 in the Lee-Chang combination system is coupled to the memory devices 70 through “a bus system 68,” which enables access to the memory devices of each rank “through a respective bus system” 76, 82, 90, 94. EX1004, [0016]. That is, the memory hub (***logic unit***) is ***for accessing*** the memory devices (***the type of memory cell array group***). Each of these bus systems 76, 82, 90, 94 individually corresponds to the claimed ***first transmission bus***. Alternatively or additionally, the bus system 68 (which is composed of the four individual bus systems 76, 82, 90, 94) corresponds to the ***first transmission bus***. I discuss each of these options in turn.

Each of Lee’s bus systems individually corresponds to a first transmission bus

63. Each rank of memory devices is coupled to the memory hub 60 by a respective bus system 76, 82, 90, 94. I have highlighted the bus system 76 in pink

in FIG. 2, below. I sometimes refer to each of these rank-specific bus systems as individual bus systems. The bus system for a single rank (*i.e.*, an individual bus system) corresponds to the claimed ***first transmission bus***, and the memory hub (***logic unit***) can ***access*** the memory cell array ICs in that rank through that bus system. For instance, the first rank 74 of memory devices (a ***type of memory cell array group***) are “coupled to the memory hub 60 through a first bus system 76 having a 32-bit data bus,” *i.e.*, through a ***first transmission bus***. EX1004, [0016]. A similar situation applies to the coupling between the memory hub 60 and the other ranks of memory devices. For instance, “a second rank 80 containing four memory devices 70 are coupled to the memory hub 60 through a second bus system 82 having a 32-bit data bus. Similarly, third and fourth ranks 86, 88 are each coupled to the memory hub 60 through respective bus systems 90, 94 each having a 32-bit data bus.” *Id*; see claim 2 (“the memory hub is coupled to the memory devices in each of the ranks through respective busses”), claim 14.



Excerpt from Lee, FIG. 2 (annotated)

64. The data rate of the first transmission bus in the combination system is *programmable* based on the teachings of Chang. Specifically, Chang describes that “control logic 120 in the memory controller 110 and/or one or more of the memory device 112 may take a variety of remedial actions in the event of an error or a degradation of one or more of the performance metrics,” including “reducing the data rate in one or more of the sub-channels relative to the data rate used in a previous transmission.” EX1006, [0036]. In the combination, based on Chang’s teaching, “the data rate in one or more sub-channels,” *e.g.*, on one or more of the

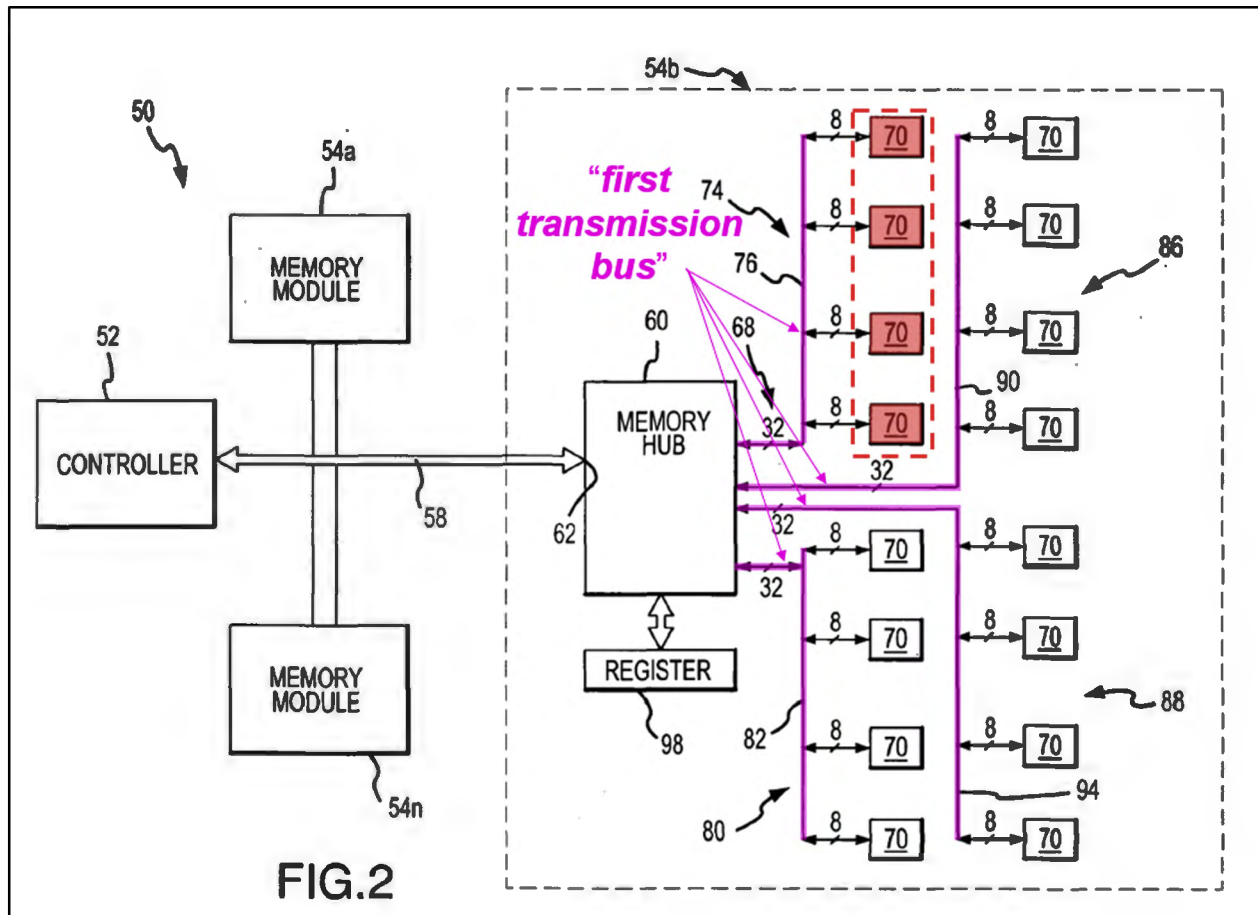
bus systems 76, 82, 90, 94, is reduced “relative to the data rate used in a previous transmission,” as a “remedial action[] in the event of an error or a degradation of one or more of the performance metrics.” EX1006, [0036]. That is, “reducing the data rate” means that the ***data rate*** on the first transmission bus (*i.e.*, on one or more of the bus systems 76, 82, 90, 94) can be varied.

65. Chang describes that these remedial actions such as reducing the data rate are performed by “control logic 120 in the memory controller [] and/or one or more of the memory devices.” EX1006, [0036]. Chang’s disclosure that the data rate is reduced by execution of control logic corresponds to the claimed requirement that the ***data rate is programmable***, *e.g.*, because it is controlled by logic (programmed). EX1006, [0036].

Lee’s bus system 68 corresponds to the first transmission bus

66. In an alternative or additional mapping of Lee to claim 19, Lee’s “bus system 68” (pink in FIG. 2, below) as a whole corresponds to the claimed ***first transmission bus***. EX1004, [0016]. The bus system 68 is composed of the four individual bus systems 76, 82, 90, 94 for the four ranks of memory devices. EX1004, [0016] (“bus system 68 coupled to several memory devices 70”). Access to the memory devices is provided through the bus system 68, *e.g.*, because each bus system provides the memory hub (***logic unit***) with access to the memory devices in its corresponding rank. The bus system 68 is ***used for transmitting data***

along with (to/from) the memory cell array ICs at least because each individual bus system 76, 82, 90, 94 of the bus system 68 is used for transmitting data to/from the memory cell array ICs, as I discussed above. See EX1004, [0016]-[0019].



Excerpt from Lee, FIG. 2 (annotated)

67. In the combination, based on Lee, in the “high memory bandwidth” mode, “the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access.” EX1004, [0017]. That is, 32 bits of data are transmitted simultaneously on each of the four individual bus systems 76, 82, 90, 94. The data

rate of the bus system 68 including the four individual bus systems 76, 82, 90, 94 (which corresponds to the claimed *first transmission bus*) in high memory bandwidth mode is 128 bits per memory access (*e.g.*, transmitting data rate or receiving data rate).

68. Lee also describes that when operated in “high memory depth mode, only one rank 74, 80, 86, 88 may be addressed at a time,” in which case “only 32 bits of data will be coupled to or from the memory module 54 with each memory access.” *Id.* That is, data is transmitted on only one of the individual bus systems 76, 82, 90, 94 at a time. The data rate of the bus system 68 including the four individual bus systems 76, 82, 90, 94 (which corresponds to the claimed *first transmission bus*) in high memory depth mode is only 32 bits per memory access (*e.g.*, transmitting data rate or receiving data rate).

69. Based on Lee, the combination system can operate in either high memory bandwidth or high memory depth mode. EX1004, [0017]. This allows for flexibility and optimization of the system’s functionality: “By allowing the memory hub 60 to configure the data format of the memory module 54, the data format can be optimized for a particular application being executed ... The data format is therefore not fixed as in conventional memory systems.” *Id.*, [0019]. This means that the system can sometimes operate in high memory bandwidth mode (in which case the data rate is 128 bits per memory access) and at other times

can operate in high memory depth mode (in which case the data rate is 32 bits per memory access), *i.e.*, the system can operate at different data rates.

70. Specifically, the mode of operation is programmable by way of “a non-volatile register 98 in the memory module 54,” which “is programmed to configure the memory hub 60 depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]; *see* claim 5 (“a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub”). Because the data rate of the first transmission bus differs between the two modes of operation, and the selection of the mode of operation is programmed, the data rate (*e.g.*, transmitting data rate or receiving data rate) of the first transmission bus is **programmable**, thus satisfying the claimed requirement that the first transmission bus have a **programmable** data rate..

71. Alternatively or additionally, the data rate of the bus system 68 including the first transmission bus is **programmable** based on Chang’s teachings of “reducing the data rate” as a remedial action, as I discussed above. *See* EX1006, [0035]-[0036].

The combination first transmission bus has a programmable transmitting or receiving signal swing

72. The system of the Lee-Chang combination is implemented based on Chang’s description that “voltage levels and/or a voltage swing of the signals 224

that are transmitted” to the memory devices “may be based on voltages 226 provided by a power supply,” where the power supply “voltages may be fixed or may be adjustable.” EX1006, [0045]. Chang’s signals 224 are data transmitted from Chang’s memory controller to the memory devices, which is a configuration analogous to data transmitted along Lee’s bus systems 76, 82, 90, 94 (which correspond individually or collectively to the claimed *first transmission bus*) from the memory hub 60 to the memory devices 70. Based on this disclosure of Chang and the similar structures of the Lee and Chang systems, in the system of the Lee-Chang combination, “voltage levels and/or a voltage swing of the signals 224 that are transmitted” between the memory hub and the memory devices (*i.e.*, along the bus systems 76, 82, 90, 94) are “based on voltages 226 provided by a power supply” where the “voltages ... may be adjustable.” EX1006, [0045].

73. A voltage swing (signal swing) that is based on an adjustable voltage is itself adjustable. That is, the voltage swing (*signal swing*) of data transmitted along one or more of the bus systems (individually or collectively the *first transmission bus*) between memory hub and memory devices, *i.e.*, *a signal swing of the first transmission bus*, is adjustable.

74. In more detail, Chang describes that the voltages are “adjusted based on one or more performance metrics associated with communication to and/or from the memory controller 210.” EX1006, [0046]. A POSITA would have

understood Chang’s system to have been programmed to change the voltages based on performance metrics, *e.g.*, to ensure satisfaction of performance metrics. Thus, the voltage swing (***signal swing***) of the first transmission bus is ***programmable*** at least because it is based on a programmable voltage provided by a power supply.

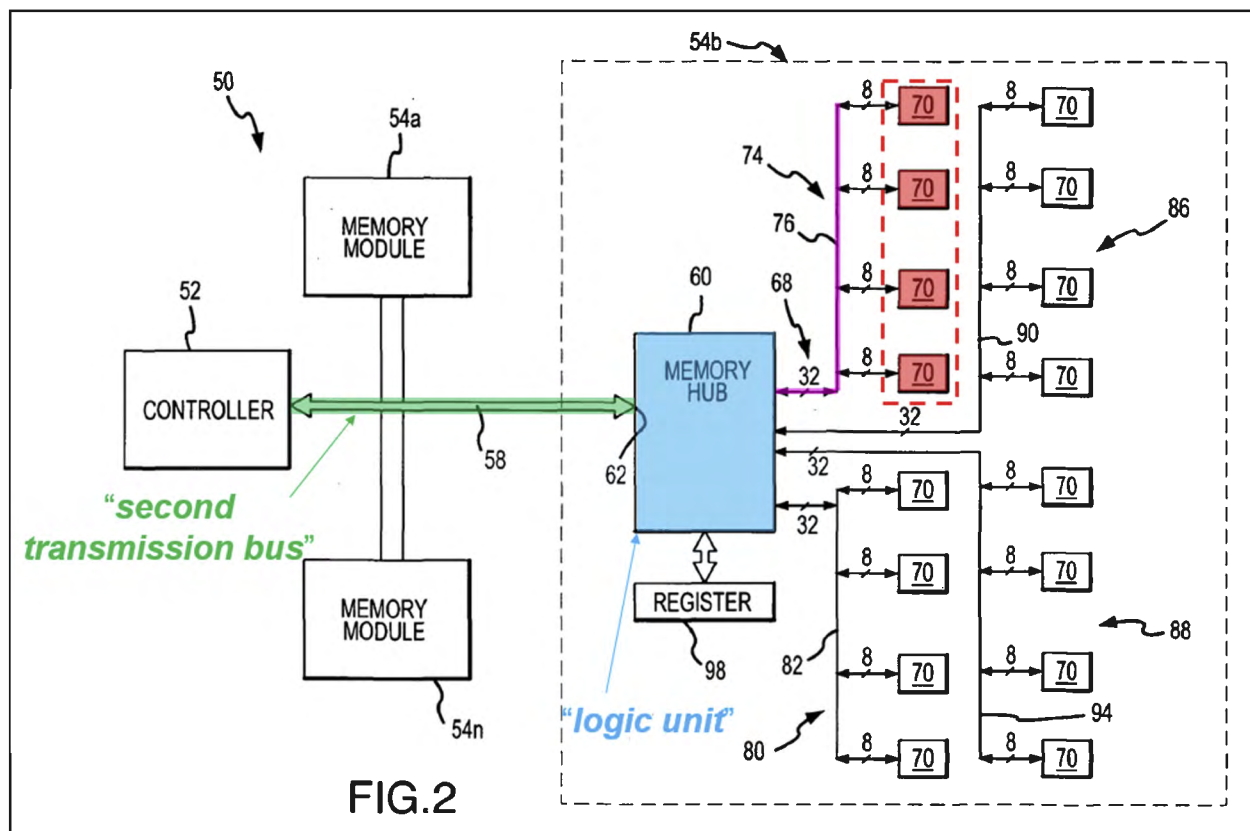
Id. For instance, in a system having a parameter (*e.g.*, power supply voltage and/or voltage swing) that is adjusted based on a performance metric can be programmed to detect the performance metric and to adjust the parameter (*e.g.*, power supply voltage and/or voltage swing) appropriately, *e.g.*, to return the performance metric to a target range and/or to maintain the performance metric in the target range.

[1c] a second transmission bus coupled to the logic unit¹ having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing; and

75. Based on Lee, each memory module in the combination memory system includes “a memory hub 60,” highlighted in blue in FIG. 2, *infra.* EX1004, [0016]; *see* [0009], [0017]-[0020], claims 1-3. The memory hub corresponds to the claimed ***logic unit*** at least because it is “programmable to configure the

¹ I note that the term “the logic unit” recited in claim element [1c] lacks antecedent basis. I briefly address the “logic unit” of the Lee-Chang combination here and also refer to further discussion in my analysis for claim element [1d].

memory module in a plurality of data formats,” *i.e.*, programmable to carry out logic tasks. EX1004, claim 1; *see* [0009], [0017]-[0020], claims 4-5.



Excerpt from Lee, FIG. 2 (annotated)

76. Also based on Lee, the combination system includes a “high-speed link 58” (marked in green in FIG. 2, below) coupled to the memory hub 60. EX1004, [0016]. Lee describes that “[t]he high-speed link 58 may be a bus formed by multiple conductors, an optical communication link, and [sic] RF communication link, or some other type of high-speed communication link.” *Id.*, [0015]; *see* [0017]-[0019], [0025], claim 13. The high-speed link corresponds to the claimed *second transmission bus*.

77. As described by Lee, “[e]ach of the memory modules 54 includes a memory hub 60 having an input/output port 62 coupled to the high-speed link 58,” satisfying the claimed requirement that the second transmission bus (*i.e.*, the high-speed link 58) is ***coupled to*** the logic unit (*i.e.*, the memory hub). EX1004, [0016]; *see* [0022], FIG. 2, FIG. 5.

The combination second transmission bus has a programmable transmitting or receiving data rate

78. As I discussed above, Lee’s system can be “configure[d]” to operate in high memory bandwidth or high memory depth mode. EX1004, [0017]; *see* [0019]. In the combination, the system is configurable to operate in these two modes, based on Lee. As a result, in the combination, “[i]n the high memory depth mode, the high-speed link 58 can operate at a slower data rate than in the high bandwidth mode.” EX1004, [0018]. This means that the data rate of the high-speed link (corresponding to the claimed ***second transmission bus***) differs based on the mode of operation. An adjustable data rate on the high-speed link has advantages: “By allowing the memory hub 60 to configure the data format of the memory module 54, the data format can be optimized for a particular application being executed ... The data format is therefore not fixed as in conventional memory systems.” EX1004, [0019].

79. More specifically, the data rate of the high-speed link (***second transmission bus***) is ***programmable*** because it is controlled by a “a non-volatile

register 98 in the memory module 54.” EX1004, [0017]. Specifically, the register 98 “is programmed to configure the memory hub 60 depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]; *see* claim 5 (“a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub”). That is, the register is programmed to configure the memory system to operate in high bandwidth or high depth mode, each of which has a different data rate on the second transmission bus. The data rate on the second transmission bus is thus *programmable*. The programmable data rate is either a *transmitting data rate* or a *receiving data rate* because Lee describes that its high memory bandwidth and high memory depth modes are for both reading data and writing data. *See* EX1004, [0017] (describing data “written to or read from the memory devices”).

80. Alternatively or additionally, in the combination, Lee describes that in the “high memory bandwidth” mode, “the high-speed link 58 may couple data at a rate of 2 GB/sec,” or “may couple 64-bit data words at a rate of 1 GB/sec,” *i.e.*, the high-speed link (*second transmission bus*) can be operated at different data rates. As I discussed *above*, Lee’s system can be “configure[d]” to operate in a certain mode, *i.e.*, the mode of operation is *programmable*. *See* EX1004, [0017], [0019]. Different modes of operation have different data rates on the second transmission

bus, and thus the data rate on the second transmission bus is *programmable data rate*. EX1004, [0017]. The programmable data rate is either a *transmitting data rate* or a *receiving data rate* because Lee describes high memory bandwidth mode for both reading and writing data. *Id.*

The combination second transmission bus has a programmable transmitting or receiving signal swing

81. The system of the Lee-Chang combination is implemented based on Chang's description that "[d]ata 216 to be transmitted by the memory controller 210 to a memory device" can have "logic levels" that are "based on voltages 226 provided by [a] power supply," where the power supply "voltages may be fixed or may be adjustable." EX1006, [0045]. Chang's data 216 are data transmitted to Chang's memory controller from an external source, which is a configuration analogous to data transmitted along Lee's high-speed link 58 (which corresponds to the claimed *second transmission bus*) from the controller 52 to the memory hub 60. Based on this disclosure of Chang and the similar structures of the Lee and Chang systems, in the system of the Lee-Chang combination, data transmitted along the high-speed link 58 have "logic levels" that are "based on voltages 226 provided by [a] power supply," where the power supply "voltages ... may be adjustable." EX1006, [0045].

82. A voltage swing (signal swing) that is based on an adjustable voltage is itself adjustable. That is, the voltage swing (*signal swing*) of data transmitted

along the high-speed bus 58 to the memory hub, *i.e.*, ***a signal swing of the second transmission bus***, is adjustable.

83. In more detail, Chang describes that the voltages are “adjusted based on one or more performance metrics associated with communication to and/or from the memory controller 210.” EX1006, [0046]. A POSITA would have understood Chang’s system to have been programmed to implement adjustment of voltages based on performance metrics, *e.g.*, to ensure satisfaction of performance metrics. Thus, the voltage swing (***signal swing***) of the second transmission bus is ***programmable*** at least because it is based on a programmable voltage provided by a power supply. *Id.*

[Id] a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus, and further used for converting a first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.

84. The memory hub 60 is coupled to the memory devices 70 through “a bus system 68,” which enables access to the memory devices of each rank “through a respective bus system” 76, 82, 90, 94. EX1004, [0016]. That is, memory hub (corresponding to the claimed ***logic unit***) is ***for accessing the type of memory cell array group***.

85. The access to the memory cell array group is provided through the individual bus systems 76, 82, 90, 94 of the overall bus system 68 (individually or collectively corresponding to the claimed ***first transmission bus***). These bus systems are ***coupled to*** the logic unit to provide access to the memory devices (***for accessing the type of memory cell array group through the first transmission bus***). “the memory devices 70 are divided into four groups or ‘ranks’ coupled to the memory hub 60 through a respective bus system,” such that “the four memory devices 70 together provide 32 bits for the 32-bit data buses.” EX1004, [0016]; *see id.* (“More particularly, a first rank 74 includes four memory devices 70 coupled to the memory hub 60 through a first bus system 76 having a 32-bit data bus. A second rank 80 containing four memory devices 70 are coupled to the memory hub 60 through a second bus system 82 having a 32-bit data bus. Similarly, third and fourth ranks 86, 88 are each coupled to the memory hub 60 through respective bus systems 90, 94 each having a 32-bit data bus”), [0017]-[0019], claim 2.

Parallel data on the first transmission bus

86. The bus system for an individual rank (*e.g.*, the first bus system 76) corresponds to the claimed ***first transmission bus***. Each bus system transmits data provided from the memory devices 70 of its rank to the memory hub, and vice versa. In more detail, in Lee’s system, each memory device 70 has “8-bit data

bus,” *i.e.*, the 8-bit data bus for each memory device provides 8 bits of parallel data to the bus system, such that “the four memory devices 70” of each rank “together provide 32 bits for the 32-bit data buses.” EX1004, [0016]. The bus system for an individual rank is a “32-bit data bus,” *i.e.*, 32 bits of data (8 from each memory device) are carried on ***parallel*** on the bus system. EX1004, [0016]; *see* [0017] (“for a high memory bandwidth, the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices”), [0018] (“In the high memory depth mode, only one rank 74, 80, 86, 88 may be addressed at a time”), claim 6 (“the memory devices in each rank are collectively operable to read or write N-bit data words”), [0009], [0019], claims 2, 3, 4, and 7. That is, the data transmitted on the bus system for an individual rank are 32 bits of parallel data (corresponding to the claimed ***first set of parallel data***).

87. In an alternative or additional mapping of Lee to claim 19, Lee’s “bus system 68” (pink in FIG. 2, below) as a whole corresponds to the claimed ***first transmission bus***. EX1004, [0016]. The bus system 68 is composed of the four individual bus systems 76, 82, 90, 94 for the four ranks of memory devices. EX1004, [0016] (“bus system 68 coupled to several memory devices 70”). Each individual bus system transmits 32 bits of ***parallel data***, as I discussed above. Thus, the data transmitted on the collective bus system 68 (***first transmission bus***) correspond to ***a first set of parallel data***, because it is composed of 4 sets of

parallel data on the four individual bus systems. *See* EX1004, [0016]-[0019].

Moreover, the individual bus systems 76, 82, 90, 94 are connected in parallel to the memory hub, which allows the memory hub to “address[] all of the memory devices simultaneously so that 128 bits of data are written to or read from the memory devices.” EX1004, [0017]. This means that the parallel data transmitted on one of the individual bus systems 76, 82, 90, 94 is transmitted in parallel to the data transmitted on the other three bus systems. Again, that makes the data transmitted on the collective bus system 68 a ***first set of parallel data***. *See* claim 3 (“the memory module is operable to [] address all of the ranks of memory devices in a first mode to simultaneously couple data to or from all of the memory devices in the memory module”), claim 4. Under either explanation, the data transmitted on the collective bus system 68 (***first transmission bus***) are “128 bits of data” (***a first set of parallel data***) transmitted “simultaneously” and in parallel on the four individual bus systems. EX1004, [0017].

Parallel data on the second transmission bus

88. The data transmitted on Lee’s high-speed link (the claimed ***second transmission bus***) is ***a second set of parallel data***. This is apparent from Lee’s description of the data transmitted on the high-speed link. For instance, Lee’s system can be operated in “high memory bandwidth” mode, in which case the high-speed link can be configured such that “a 128-bit data word may be coupled

through the link 58.” EX1004, [0017]. This 128-bit data word transmitted on the link 58 constitutes 128 bits of parallel data, *i.e.*, it corresponds to the ***second set of parallel data***. In another example, Lee’s high-speed link can “couple 64-bit data words” or “32-bit data word[s].” *Id.* In these cases, the 64-bit data word (64 bits of parallel data) or 32-bit data word (32 bits of parallel data) corresponds to the ***second set of parallel data***. *Id.* That the data transmitted on the high-speed link 58 are parallel data (*e.g.*, 128 bits, 64 bits, or 32 bits of parallel data) is made apparent by Lee’s description that the high-speed link has “a capacity for coupling data having a predetermined bus width between the controller 52 and each memory module.” *Id.*, [0015].

The combination logic unit is for converting the first set of parallel data to the second set of parallel data

89. It is my opinion that a POSITA would have found obvious that Lee’s memory hub (corresponding to the claimed ***logic unit***) is ***used for converting the first set of parallel data*** (*i.e.*, the data on the first transmission bus) ***into the second set of parallel data*** (*i.e.*, the data on the second transmission bus). This is the case when a single one of Lee’s bus systems corresponds to the claimed first transmission bus (and thus when the data transmitted on an individual one of Lee’s bus systems corresponds to the claimed ***first set of parallel data***). This is also the case when Lee’s collective bus system 68 corresponds to the claimed first transmission bus (and thus when the data transmitted on Lee’s collective bus

system 68 corresponds to the claimed ***first set of parallel data***). I discuss each of these in more detail in the following paragraphs.

Conversion of data when an individual one of Lee's bus systems corresponds to the claimed first transmission bus (and thus when the data transmitted on an individual one of Lee's bus systems corresponds to the claimed first set of parallel data)

90. This section addresses the case in which one of Lee's individual bus systems (e.g., the bus system 76) corresponds to the claimed ***first transmission bus***, and the 32 bits of parallel data transmitted on the bus system 76 thus corresponds to the claimed ***first set of parallel data***.

91. Lee's system has two operation modes: high memory bandwidth mode and high memory depth mode. See EX1004, [0017]. In high memory bandwidth mode, "the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access." EX1004, [0017]. This means that, when reading from the memory devices, the memory hub receives, at once, multiple sets of parallel data transmitted along the multiple bus systems 76, 82, 90, 94, one set of data from each rank of memory devices. See EX1004, [0016]-[0017], FIG. 2. Specifically, 32 bits are received through each of the four bus systems 76, 82, 90, 94. *Id.*, [0017]; see [0019] (describing another option in which two ranks (rather than all four) are accessed simultaneously: "one pair of ranks 74, 80 are simultaneously accessed and the other pair of ranks 86, 88 are simultaneously

accessed”). These simultaneously received 128 bits of data include the 32 bits (*first set of parallel data*) transmitted on the first bus system 76, as well as 32 bits transmitted on each other bus system 82, 90, 94.

92. Lee then describes two implementations for transmission of that 128 bits of parallel data on the high-speed link 58 (corresponding to the claimed *second transmission bus*), as I discuss in the following paragraphs. See EX1004, [0017]. Both involve *converting the first set of parallel data* (e.g., the data transmitted on the first bus system 76) *into the second set of parallel data* (the data transmitted on the high-speed bus 58).

93. One way Lee implements “high memory bandwidth” mode is described as follows: “128 bits of data are written to or read from the memory devices” (that is, 32 bits of parallel data through each of the four bus systems 76, 82, 90, 94, as I discussed above). However, “the link 58 may transfer only a 32-bit data word” or a “64-bit data word[.]” EX1004, [0017]. This 32-bit or 64-bit data word corresponds to the *second set of parallel data*, as I also discussed above. In order to receive 128 bits of data simultaneously through multiple bus systems 76, 82, 90, 94, and transmit that data in a 64- or 32-bit word through a single bus system (i.e., the high-speed link 58), a POSITA would have found obvious that the data received from the multiple bus systems 76, 82, 90, 94 (including the 32-bit *first set of parallel data* from the bus system 76) would have to be *converted* to the

data of a different bit width transmitted on a single bus (*i.e.*, to the ***second set of parallel data***). For instance, this conversion can be done by operations involving multiplexing.

94. In more detail, in this implementation, the bit width of the parallel data that is simultaneously received through the multiple bus systems (*i.e.*, a total bit width of 128 bits) is different from the bit width of the parallel data that is then transmitted through the high-speed link 58 (*e.g.*, 32-bit words (bit width of 32 bits) or 64-bit words (bit width of 64 bits). The processing of receiving data of one bit width (128 bits) from one bus system including multiple buses and then transmitting that same data in a different bit width (64 bits or 32 bits) on a different, single bus involves ***converting*** the received data (*i.e.*, 128 bits of received data, including the 32-bit data corresponding to ***the first set of parallel data***) to the transmitted data (***second set of parallel data***).

95. An example of this conversion is described in Nakamura. Nakamura describes “a parallel-to-parallel converter for converting an ‘m’-bit parallel signal into an ‘n’-bit parallel signal.” EX1019, Abstract. That is, Nakamura describes that the process of changing a signal of one bit width (*e.g.*, 128 bits, in the Lee example) to a signal of a different bit width (*e.g.*, 64 bits or 32 bits) involves ***converting*** the data from the initial bit width to the different bit width.

96. Another way Lee implements “high memory bandwidth” mode is described as follows: “[t]he 128 bits of data [are] coupled through the high-speed link by [] increasing ... the size of the data word coupled through the link 58.” EX1004, [0017]. For instance, a “128-bit data word” (*second set of parallel data*) “may be coupled through the link 58.” EX1004, [0017]. That is, Lee’s memory hub (*logic unit*) receives 128 bits of data through four distinct bus systems (including the 32-bit *first set of parallel data*), and *converts* that received data to a “128-bit data word” for transmission on a single bus system: the high-speed link 58. EX1004, [0017]; *see* [0019] (“64 bits of data are coupled through the high-speed link 58”). A POSITA would have found obvious that receiving data simultaneously through multiple bus systems and then transmitting that data through a single bus system involves *converting*, by the memory hub (*logic unit*) the data received from the multiple bus systems (*i.e.*, 128 bits of simultaneously received data, including the 32-bit *first set of parallel data* transmitted on the first bus system 76) into the data transmitted on the single high-speed link 58 (*the second set of parallel data*). For instance, converting parallel data received simultaneously from multiple buses into parallel data transmitted on a single bus involves processes such as multiplexing.

Conversion of data when the collective bus system 68 corresponds to the claimed first transmission bus (and thus when the data transmitted collectively on bus system 68 corresponds to the claimed first set of parallel data)

97. This section addresses the case in which Lee's bus system 68 (that includes the four individual bus systems) corresponds to the claimed ***first transmission bus***, and the 128 bits of parallel data transmitted on the bus system 68 thus corresponds to the claimed ***first set of parallel data***.

98. When operating in "high memory bandwidth" mode, the "128 bits of data" that are "simultaneously" "read from the memory devices" collectively correspond to the ***first set of parallel data***, as I discussed above.

99. In one implementation, the 128 bits are transmitted simultaneously on the collective bus system 68, but "the link 58 may transfer only a 32-bit data word" or a "64-bit data word[]" (***second set of parallel data***). EX1004, [0017]. Again, like I discussed above, a POSITA would have found obvious that the memory hub receiving data of one bit width simultaneously through multiple bus systems and then transmitting that data, now of a different bit width, through a single bus system involves ***converting*** the received data (***first set of parallel data***) to the transmitted data (***second set of parallel data***), e.g., by multiplexing the received data. In order to receive data of one bit width (128 bits on the bus system 68) and then transmit that same data in a different bit width (one 32- or 64-bit word on the high-speed link 58) a POSITA would have found obvious that the received data

(*first set of parallel data*) would have to be *converted* to the transmitted data (*second set of parallel data*). See EX1004, [0017]. For instance, such a conversion of parallel data of one bit width to parallel data of another bit width is described by Nakamura. See EX1019, Abstract.

100. In another implementation described by Lee, these data are received through four individual bus systems (that together correspond to the claimed *first transmission bus*) and *converted* to a “128-bit data word” for transmission on a single bus system: the high-speed link 58. EX1004, [0017]; see [0019]. As I discussed above, POSITA would have found obvious that receiving data simultaneously through multiple bus systems and then transmitting that data through a single bus system involves *converting*, by the memory hub (*logic unit*) the data received from the multiple bus systems (*first set of parallel data*) into the data transmitted on the single high-speed link 58 (*second set of parallel data*), e.g., by multiplexing.

(b) **Claim 2**

[2a] The reconfigurable high speed memory chip module of claim 1, wherein the first transmission bus is used for transmitting the first set of parallel

data along with² the multiple memory cell array ICs, and

101. The bus system for an individual rank (e.g., the first bus system 76) (corresponding to the claimed *first transmission bus*) is *used for transmitting data along with (to/from) the memory cell array ICs*, in that each bus system transmits data provided from the memory devices 70 of its rank to the memory hub, and vice versa. In more detail, in Lee's system, each memory device 70 has "8-bit data bus," i.e., the 8-bit data bus for each memory device provides 8 bits of parallel data to the bus system, such that "the four memory devices 70" of each rank "together provide 32 bits for the 32-bit data buses." EX1004, [0016].

102. Alternatively/additionally, the bus system 68 (corresponding to the claimed *first transmission bus*) is *used for transmitting data along with (to/from) the memory cell array ICs* at least because each individual bus system 76, 82, 90, 94 of the bus system 68 is used for transmitting data to/from the memory cell array ICs, as I discussed above. See EX1004, [0016]-[0019].

[2b] bus width of the first transmission bus is wider than bus width of an

² As best understood, I interpret the phrase "transmitting a first set of parallel data along with the memory cell array ICs" as "transmitting a first set of parallel data to/from the memory cell array ICs."

70 have an 8-bit data bus”), FIG. 2. The first bus system 76 (corresponding to the claimed *first transmission bus*, pink in FIG. 2) is a “32-bit data bus,” *i.e.*, has a *bus width* of 32 bits. *See* EX1004, [0016] (“a first bus system 76 having a 32-bit data bus ... a second bus system 82 having a 32-bit data bus ... bus systems 90, 94 each having a 32-bit data bus”). That is, the bus widths of the first bus system and the I/O data bus satisfy the claimed limitation that the *bus width of the first transmission bus* (32 bits) is *wider than the bus width of each I/O data bus* (8 bits).

Alternatively/additionally, the bus width of the bus system 68 is equal to the total bus width of the four constituent bus systems, each of which is 32 bits wide, as I discussed above. *See* EX1004, [0016], FIG. 2. That is, the bus width of the bus system 68 (*bus width of the first transmission bus*) is 128 bits, *i.e.*, *wider than* the 8-bit bus width of each I/O data bus. *See* EX1004, [0016], FIG. 2.

(c) **Claim 4**

[4] *The reconfigurable high speed memory chip module of claim 1, wherein programmability of the first transmission bus or the second transmission bus corresponds to a one-time programming (OTP), a multi-time programming (MTP), a Flash Memory, an embedded memory, an anti-fuse, a register, firmware, or software.*

105. In the combination, based on Lee, the combination can be “configure[d]” to operate in high memory bandwidth or high memory depth mode,

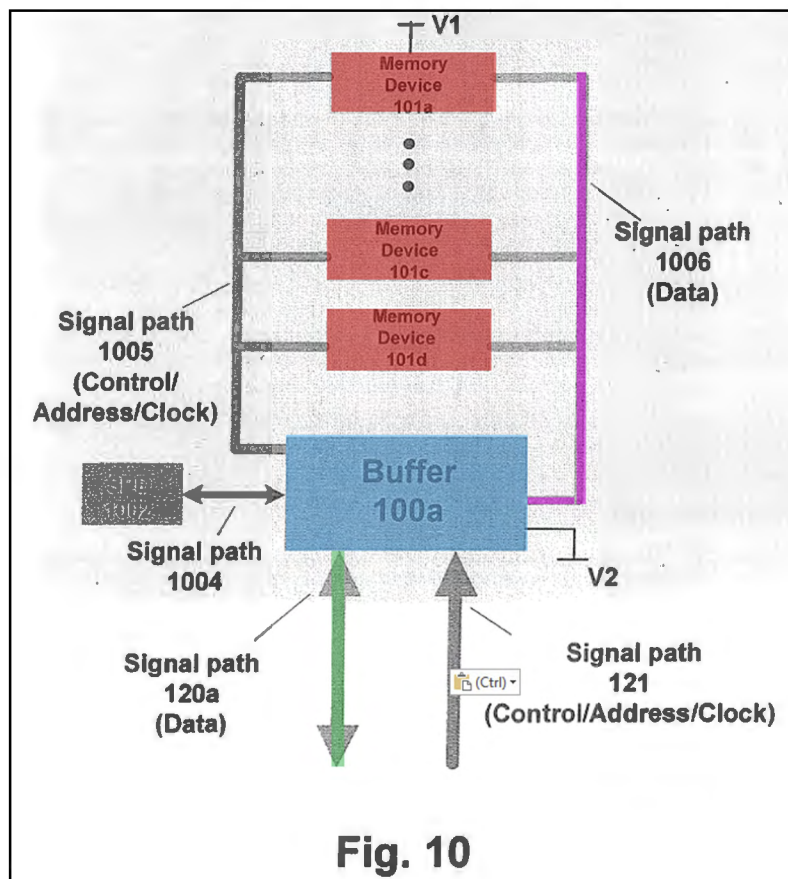
which corresponds to *programmability of the first transmission bus* and/or to *programmability of the second transmission bus*, as I discussed above for elements [1b] and [1c]. See EX1004, [0017], [0019]. Specifically, the mode of operation is *programmable* by way of “a non-volatile register 98 in the memory module 54,” which “is programmed to configure the memory hub 60 depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]. This corresponds to the claimed requirement that *programmability of the first/second transmission bus corresponds to a register* (namely, the non-volatile register 98). See claim 5 (“a programmable storage device coupled to the memory hub, the programmable storage device being programmed to control the operating mode of the memory hub”). Additionally a POSITA would have understood that OTP, MTP and Flash memory are common choices to implement a non-volatile register.

B. [Ground 1B]: Claims 1, 2, and 4 Are Obvious over Lee, Chang, and Tsern

1. Tsern (EX1005)

106. Like Lee, Tsern relates to “topologies (data and/or control/address information)” of a memory system “between an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices.” EX1005, Abstract. One example of Tsern’s memory system is illustrated in Fig. 10, which I have reproduced and annotated

below. This system includes “a plurality of integrated circuit memory devices 101a-d [highlighted in red] and a buffer 100a [highlighted in blue].” *Id.*, 22. “[D]ata may be transferred between the plurality of integrated circuit memory devices 101a-d and buffer 100a on a signal path 1006 (data),” marked in pink. *Id.* A “signal path 120a,” green, “transfer[s] data (read and write data)” between the buffer device 100a and “a memory module connector interface.” *Id.*, 12.



Excerpt from Tsern, Fig. 10 (annotated)

107. The components of Tsern’s buffer device 100a are illustrated in Fig. 18, reproduced below. *See* EX1005, 30. Signal data is provided to the buffer

device 100a through a buffer interface 1103a, while an interface 1820b “transfer[s] data between buffer 100a and one or more memory devices.” *Id.*, 31-33. The interface is “programmable to access different memory widths,” such as “to connect to 16 ‘x4’ width memory devices, 8 ‘x8’ width memory devices or 4 ‘x16’ width memory devices.” *Id.*, 37. A multiplexer 1830 (orange) “perform[s] bandwidth-concentrating operations between buffer interface 100a and interface 1820b,” *e.g.*, “utiliz[ing] the combined bandwidth of multiple data paths [1006] coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” *Id.*, 33. The buffer interface 1103a includes a “[c]onfigurabe serialization/deserialization circuit 1891,” orange, that “performs serialization and deserialization functions” on the data “depending upon a stored serialization ratio,” *e.g.*, depending on “memory device access width.” *Id.*, 38.

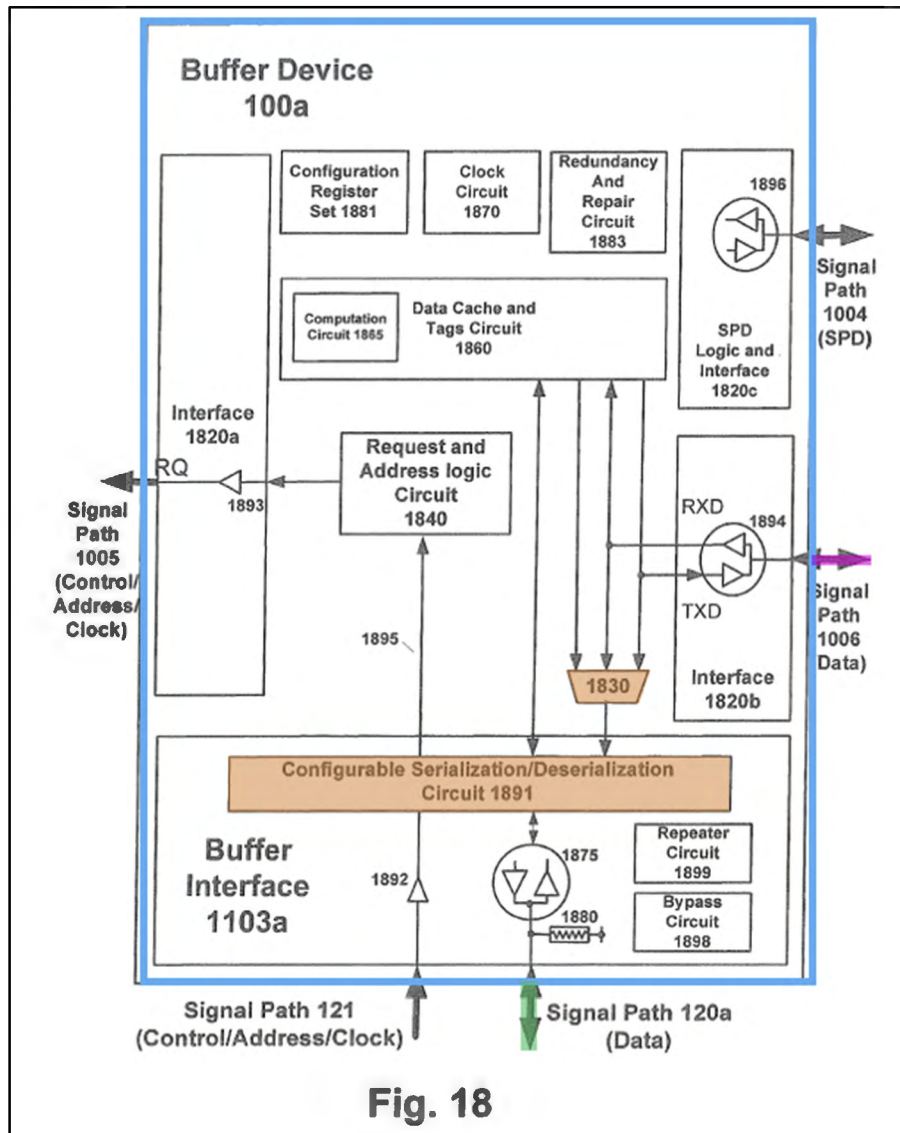


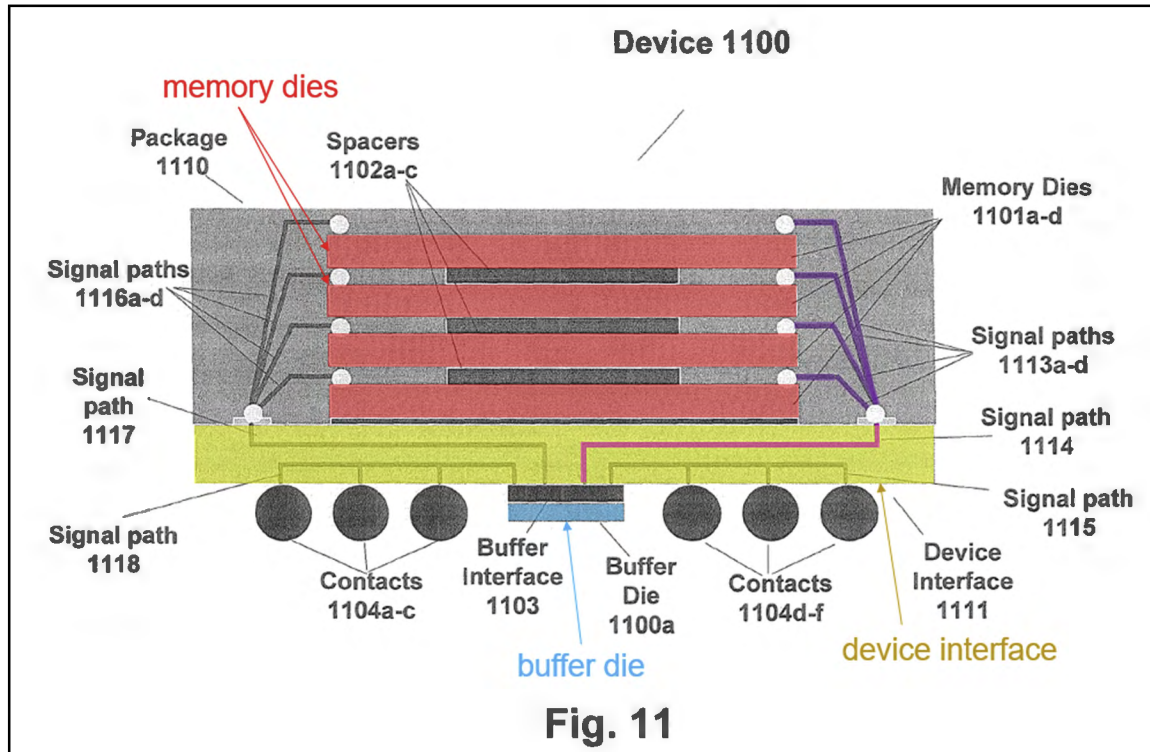
Fig. 18

Excerpt from Tsern, Fig. 18 (annotated)

108. Another of Tsern’s buffer devices is buffer device 3600, shown in Fig. 36, reproduced below. The buffer device 3600 “operates similar to buffer 100a” in that it receives “read data via one or more signal paths 1006” (marked in pink) from memory devices and “in response, transmits corresponding signals to a master” along a signal path 120a (marked in green). EX1005, 68. As with buffer

100a, the buffer device 3600 includes an “interface 3611” that “can be segmented into at least three different configurations or segmentation modes: 1) Four 4-bit interfaces (4x4), 2) Two 4-bit interfaces (2x4) or 3) Two 8-bit interfaces (2x8),” which “allow[s] flexibility in memory module or memory stack configurations.” *Id.*, 69. The buffer device 3600 also includes “data path 3606 and data path router 3610,” both highlighted in orange, that “merge separate read data from more than one memory device into a single merged read data or read stream output at interface 3601,” *e.g.*, merging the read data from the memory devices received via the pink signal paths 1600 into a single data stream for transmission along the single data path 120a. *Id.*

separated by a device interface 1111 (yellow) “to alleviate heat dissipation near the memory die.” *Id.*



Excerpt from Tsern, Fig. 11 (annotated)

110. Tsern is from the same field of endeavor (*e.g.*, memory systems) as the '834 Patent. *See* EX1001, 1:28-33; EX1005, Abstract.

111. Also, Tsern is reasonably pertinent to the problem the '834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:28-33; EX1005, Abstract. For instance, Tsern’s

memory systems “enable configurable effective memory organization,” which is relevant to development of efficient memory systems. *See* EX1005, 6.

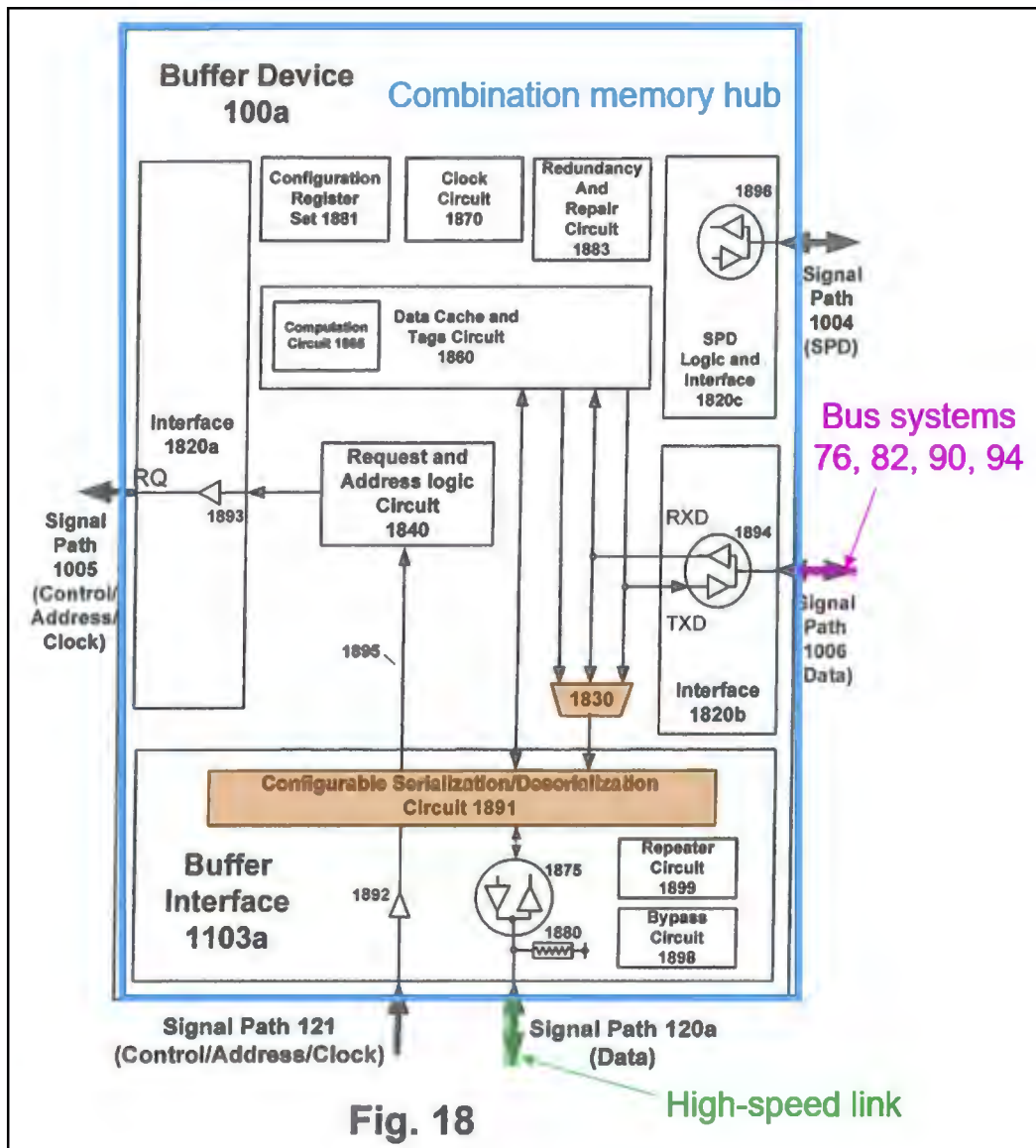
2. The Lee-Chang-Tsern Combination

112. A system based on the combination of Lee, Chang, and Tsern uses the structure of Lee’s memory system 50 as a starting point. *See*, for instance, the illustrations in Lee’s FIGS. 2 and 5. Specifically, consistent with Lee’s system, “memory devices 70 are divided into four groups or ‘ranks’ coupled to the memory hub 60 [blue] through a respective bus system.” EX1004, [0016]. The memory hub is also coupled to a memory controller through a “high-speed link 58.” *Id.* The memory system is operable in “high memory bandwidth” or “high memory depth” mode, as I discussed above for Lee’s system. EX1004, [0017]. The signal swing on the transmission buses is programmable, based on Chang and as I discussed above for Ground 1A.

113. Tsern’s buffer device 100a is similar to Lee’s memory hub 60, in that it “provides access to a plurality of respective integrated circuit memory devices.” EX1005, 12; *see* 30 (“One or more memory devices 101a-d may respond by transmitting data to buffer 100a which receives the data via one or more signal paths 1006 and in response, transmits corresponding signals to a master”). In the Lee-Chang-Tsern combination system, based on this similarity, the memory hub is implemented based on Tsern’s buffer device. *See* EX1005, 12, 30, Fig. 18. In

addition, optionally, the combination memory hub is implemented as an integrated circuit, consistent with Tsern's teachings that its buffer device is an "integrated circuit buffer device." EX1005, Abstract; *see* 30 ("Fig. 18 illustrates a block diagram of a buffer device 100a (or die, such as buffer die 1100a)"), Fig. 11.

114. One example of how the Lee-Chang-Tsern combination is implemented is based on Tsern's description of the buffer device 100a of Fig. 18. I have illustrated this example in the composite figure below. Specifically, the memory hub of the combination is an integrated circuit that has structure and function based on Tsern's buffer device 100a. Generally, Tsern's buffer device 100a and Lee's memory hub 60 have similar functions: they both handle communications between a memory controller and "a plurality of respective integrated circuit memory devices," and they do so via (1) a single signal path between the memory hub/buffer device and the controller and (2) multiple signal paths between the memory hub and the memory devices. EX1005, 12; *see* 30 ("One or more memory devices 101a-d may respond by transmitting data to buffer 100a which receives the data via one or more signal paths 1006 and in response, transmits corresponding signals to a master"), Abstract ("topologies (data and/or control/address information) between an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices").



Lee-Chang-Tsern composite figure based on Tsern, Fig. 18

115. As I discussed earlier, Tsern’s buffer device 100a includes a “buffer interface 1103a [that] couples signal path[] 120a to buffer 100a.” EX1005, 31. The signal path 120a couples the buffer device 100a to a master, such as a memory controller. See EX1005, 22, 30, Fig. 18. This structure is generally similar to Lee’s high-speed link 58 coupling the memory hub 60 to the controller 52. See

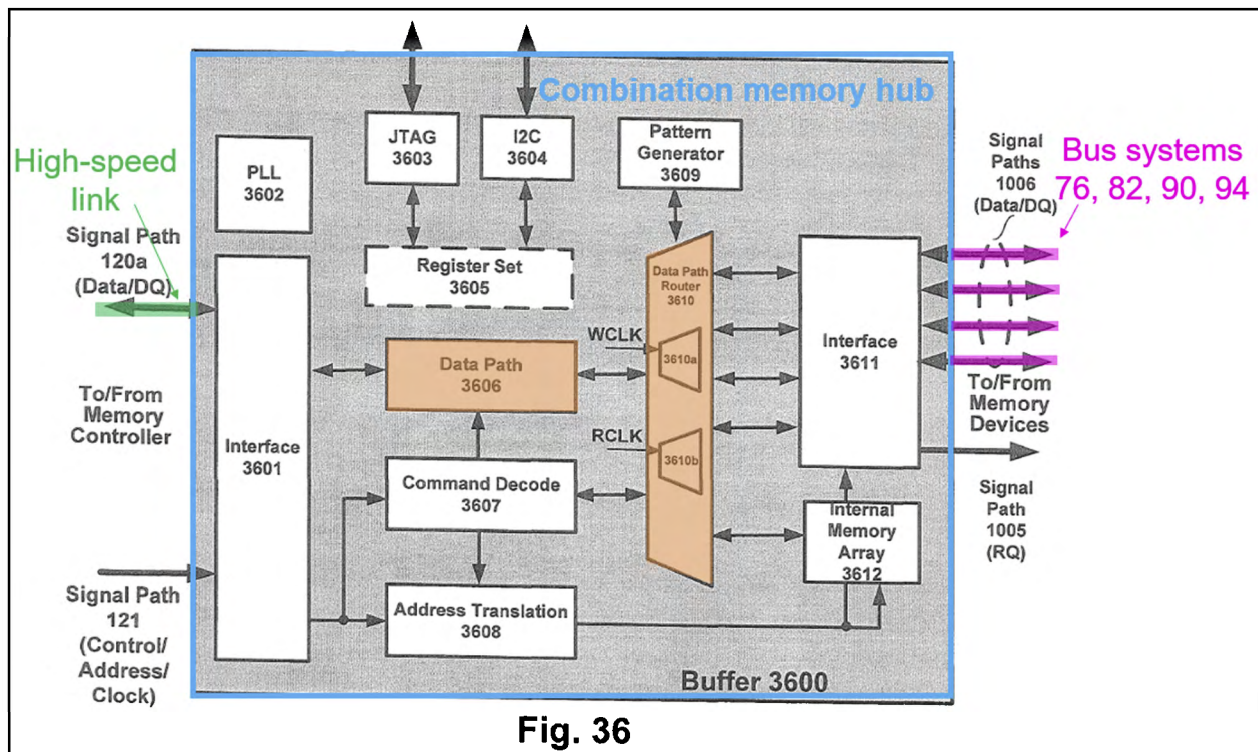
EX1004, [0015]-[0016], FIG. 2. Based on this teaching of Tsern and its similarity to the structure of Lee's system, the combination memory hub (outlined in blue in the composite figure above) is implemented with a buffer interface (based on the buffer interface 1103a of Tsern's buffer device 100a) that couples the high-speed link 58 of the combination (green in the composite figure above; based on the signal path 120a of Tsern's buffer device 100a) to the controller (*e.g.*, corresponding to Tsern's master). *See* EX1004, [0015]-[0016], FIG. 2.

116. Tsern's buffer device 100a also includes an "[i]nterface 1820b" that is "coupled to signal path 1006 to transfer data between buffer 100a and one or more memory devices 101a-d." EX1005, 32-33. Importantly, Tsern describes that the "number of ... data signal lines between buffer 100a and memory devices 101a-d are programmable in order to accommodate different numbers of memory devices." *Id.*, 37. This structure is generally similar to Lee's buses 76, 82, 88, 90 that transfer data between the memory hub and multiple memory devices 70. *See* EX1004, FIG. 2. Based on this teaching of Tsern and its similarity to the structure of Lee's system, the combination memory hub is implemented with an interface (based on the interface 1820b of Tsern's buffer device 100a) that is coupled to the bus systems 76, 82, 90, 94 of the combination (*e.g.*, corresponding to Tsern's signal paths 1006) to enable data transfer between the memory hub and the ranks of memory devices. *See* EX1004, [0016], FIG. 2.

117. Other aspects of the combination memory hub are implemented as taught by Tsern for its buffer device 100a. For instance, among other aspects, a “multiplexer 1830 [orange] may perform bandwidth-concentrating operations between buffer interface 100a and interface 1820b,” *e.g.*, allowing the buffer to “utilize[] the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” EX1005, 33. Providing a mechanism to combine multiple data paths of simultaneously received data into a single data path for connection to a memory controller enables implementation of the high memory bandwidth mode of operation described by Lee, in which data received at the memory hub simultaneously from multiple bus systems is combined onto the single high-speed link 58. ; *see* EX1004, [0017]. The memory hub of the combination can also implement a “[c]onfigurable serialization/deserialization circuit 1891” (orange) that enables employment of “an access interleaving or multiplexing scheme ... to ensure that all storage locations within memory devices 101a-d can be accessed.” EX1005, 38.

118. A second example of how the Lee-Tsern combination is implemented is based on Tsern’s teachings of the “integrated circuit buffer device 3600” of Fig. 36. I have illustrated this example in the composite figure below. Specifically, the memory hub of the combination is an integrated circuit that has structure and function based on Tsern’s buffer device 3600. Like Tsern’s buffer device 100a,

the buffer device 3600 also has functions and structure that are similar to Lee's memory hub. Specifically, Tsern's buffer device 3600 manages communication of data and control signals between a memory controller and memory devices, as does Lee's memory hub. See EX1005, 68.



Excerpt from Tsern, Fig. 36 (annotated)

119. Tsern's buffer device 3600 includes an interface 3601 that couples signal path 120a to the buffer device 3600. See EX1005, 67-68. The signal path 120a couples the buffer device 3600 to a master, such as a memory controller. See *id.*, 68. This structure is generally similar to Lee's high-speed link 58 coupling the memory hub 60 to the controller 52. See EX1004, [0015]-[0016], FIG. 2. Based on this teaching of Tsern and its similarity to the structure of Lee's system, the

combination memory hub (outlined in blue in the composite figure above) is implemented with an interface (based on the interface 3601 of Tsern's buffer device 3600) that couples the high-speed link of the combination (green in the composite figure above; based on the signal path 120a of Tsern's buffer device 3600) to the controller. *See* EX1004, [0015]-[0016], FIG. 2.

120. Tsern's buffer device 3600 also includes an interface 3611 to communicate data between the buffer device and one or more memory devices via multiple signal paths 1006. *See* EX1005, 67. This structure is generally similar to Lee's buses 76, 82, 88, 90 that transfer data between the memory hub and multiple memory devices 70. *See* EX1004, FIG. 2. Based on this teaching of Tsern and its similarity to the structure of Lee's system, the combination memory hub is implemented with an interface (based on the interface 3611 of Tsern's buffer device 3600) that is coupled to the bus systems 76, 82, 90, 94 of the combination (*e.g.*, corresponding to Tsern's signal paths 1006) to enable data transfer between the memory hub and the ranks of memory devices. *See* EX1004, [0016], FIG. 2.

121. Other aspects of the combination memory hub are implemented as taught by Tsern for its buffer device 3600. For instance, the combination memory hub includes "data path 3606 and data path router 3610," orange in the composite figure above, that "merge separate read data from more than one memory device" into a single merged read data or read stream." EX1005, 68; *see* 71 (describing

that the data path router “includes a plurality of signal paths used to merge read data from different memory devices as well as parse write data into write data portions to be stored in multiple memory devices”). The “separate read data” are from the multiple memory devices (*e.g.*, DRAM) of the combination system, and they are merged into a single data stream that is output onto the high-speed link of the combination. *See* EX1004, [0016]-[0020], FIG. 2.

3. Motivation for the Combination and Expectation of Success

Motivation for implementing functionality of Tsern’s buffer device in the combination memory hub

122. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement the combination memory hub to have functionality based on Tsern’s buffer devices (*e.g.*, based on the Fig. 18 or Fig. 36 embodiment of Tsern’s buffer device).

123. First, a POSITA would have been motivated to implement Lee’s memory hub based on Tsern’s teachings of similarly situated buffer devices because of this very similarity, and because the specifics provided by Tsern are just details simply not specified by Lee regarding how to implement a memory hub. Specifically, Lee’s memory hub receives a first set of parallel data from multiple memory devices along multiple bus systems, and transmits that received data as a second set of parallel data along a single bus system to a memory controller. *See* [1b]-[1d] of Ground 1A, *supra*. Tsern discloses buffer devices with similar

functionality: they receive parallel data from multiple memory devices along multiple buses, and transmit data to a memory controller along a single bus system. A POSITA would have motivated to look to Tsern for teachings of how to implement the details of the buffer architecture.

124. Second, implementing the memory hub of the combination based on Tsern's buffer devices is merely the application of known techniques (that is, a specific implementation of a memory hub that converts a received set of parallel data to a transmitted set of parallel data) to a known structure (the memory hub in Lee's memory system), and it yields predictable results (specifically, a memory hub implementing elements enabling conversion of a received set of parallel data to a transmitted set of parallel data).

125. A POSITA would have had a reasonable expectation of success in implementing the memory hub of the combination based on Tsern's buffer devices because memory system technology is predictable. Also, a POSITA would have had a reasonable expectation of success because the location and functionality of Tsern's buffer devices in Tsern's memory system is generally consistent with that of Lee's memory hub in Lee's memory system. Specifically, both Tsern's buffer devices and Lee's memory hub manage communication of data to/from ranks of integrated circuit memory devices along multiple transmission buses, and

communication of data to/from a memory controller along a single transmission bus. *See* EX1004, [0009], [0015]-[0020], FIG. 2; EX1005, Figs. 11, 18, 36.

Motivation for implementation of the memory hub as an integrated circuit

126. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement the memory hub in the combination as an integrated circuit.

127. First, it was conventional to implement the memory hub of a memory cell array system as an integrated circuit, and a POSITA would have been motivated to pursue this standard implementation for compatibility with conventional processes and structures. For instance, Khan describes an ASIC (a type of integrated circuit) in a memory system. *See* EX1009, 1. Liao also describes integrated circuit controller die in the context of a memory system. *See* EX1016, 6:53-54, Fig. 18.

128. Second, a POSITA would have recognized that implementation of a memory hub as an integrated circuit is smaller, more efficient, and less expensive than implementation of the memory hub functionality through a circuit composed of discrete components, given that these are standard and well-known advantages of integrated circuits. *See* EX1022, 1:15-18 (“Due to many technological advances, integrated circuits, or “chips,” incorporate many millions of transistors

on a single monolithic device. This provides many advantages, including improved speed and reduced size”).

129. Third, Lee does not specify particularly the nature of the memory hub. A POSITA would have been motivated to implement the combination memory hub as an integrated circuit, especially given the advantages of integrated circuits, because implementing the memory hub as an IC is just an implementation detail.

130. Fourth, implementing the memory hub as an integrated circuit is merely the application of known techniques (a memory hub as an integrated circuit) to a known structure (*e.g.*, the combination memory hub) to yield predictable results (an integrated circuit memory hub).

131. A POSITA would have had a reasonable expectation of success in implementing the memory hub as an integrated circuit because this was a conventional approach to implementation of memory hubs. *See* EX1009, 1; EX1016, 6:53-54.

4. Analysis of claims

132. For the reasons below, claims 1, 2, and 4 are obvious over the combination of Lee, Chang, and Tsern.

(a) Claim 1

[1pre] A reconfigurable high speed memory chip module, comprising

[1a] a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array integrated circuits (ICs);

[1b] a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing;

[1c] a second transmission bus coupled to the logic unit having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing; and

133. These limitations are rendered obvious by the Lee-Chang-Tsern combination for reasons similar to those I discussed above for elements [1pre]-[1c] of Ground 1A.

[1d] a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus, and further used for converting a first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.

134. The Lee-Chang-Tsern combination system includes a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus, and has a first set of parallel data of the first transmission bus and a second set of parallel data on the second transmission bus, as I discussed above for Ground 1A. Specifically, in the Lee-Chang-Tsern combination system, the high-speed link 58 corresponds to the claimed second transmission bus, and the data carried on the high-speed link 58 corresponds to the claimed second set of parallel data, for reasons similar to those I discussed above

for element [1c]-[1d] of Ground 1A. Also in the combination system, the bus systems 76, 82, 90, 94 individually or collectively correspond to the claimed first transmission bus, and the data carried on an individual bus system or on all four bus systems together correspond to the claimed first set of parallel data.

Tsern's buffer device 100a renders obvious parallel-to-parallel conversion

135. In one example of the Lee-Tsern combination system, the memory hub (corresponding to the claimed ***logic unit***) is implemented based on Tsern's description of its buffer device 100a, *e.g.*, the buffer device illustrated in Fig. 18. In this example, based on the teachings of Tsern about the buffer device 100a, and as I discuss in more detail in the following paragraphs, the memory hub (***logic unit***) is *used for converting the first set of parallel data into the second set of parallel data*.

136. As I discussed previously, in Tsern's system, data is communicated between the buffer device 100a and a memory controller via a signal path 120a. *See* EX1005, 12, 14-15. Tsern describes that the "buffer interface 1103a has a programmable width for signal path 120a," indicating that the signal path 120a can carry data of various widths, and specifically data of greater than one bit in width. *Id.*, 38. Data of greater than one bit in width are parallel data. That is, based on Tsern's disclosure that the signal path 120a has a programmable width, a POSITA would have understood that the signal path 120a can carry ***parallel data***, *i.e.*, data

of width greater than one bit. This is consistent with Lee's high-speed link 58, which also carries parallel data, as I discussed above for Ground 1A.

137. Also in Tsern's system, data is communicated between the buffer device 100a and multiple memory devices via multiple "signal paths 1006." EX1005, 38; *see id.* ("The number of signal paths 1006 may be increased or decreased as the memory device access width changes"). Each signal path communicates with a corresponding memory device. Tsern describes that the buffer device interface 1820b, which connects to the signal paths 1006 (*see* Fig. 18), "may be programmed to connect to 16 'x4' width memory devices, 8 'x8' width memory devices or 4 'x16' width memory devices." *Id.*, 37. That is, Tsern describes that the memory devices (which are connected to the respective signal paths) provide data of 4-bit, 8-bit, or 16-bit widths. These data (which are ***parallel data***) are carried by the signal paths 1006. That is, based on this disclosure, a POSITA would have understood that each signal path 1006 carries ***parallel data***, *e.g.*, in order to interface with 4-, 8-, or 16-bit width memory devices. This is consistent with Lee's bus systems 76, 82, 90, 94, which also carry parallel data from the respective ranks memory devices, as I discussed above for Ground 1A.

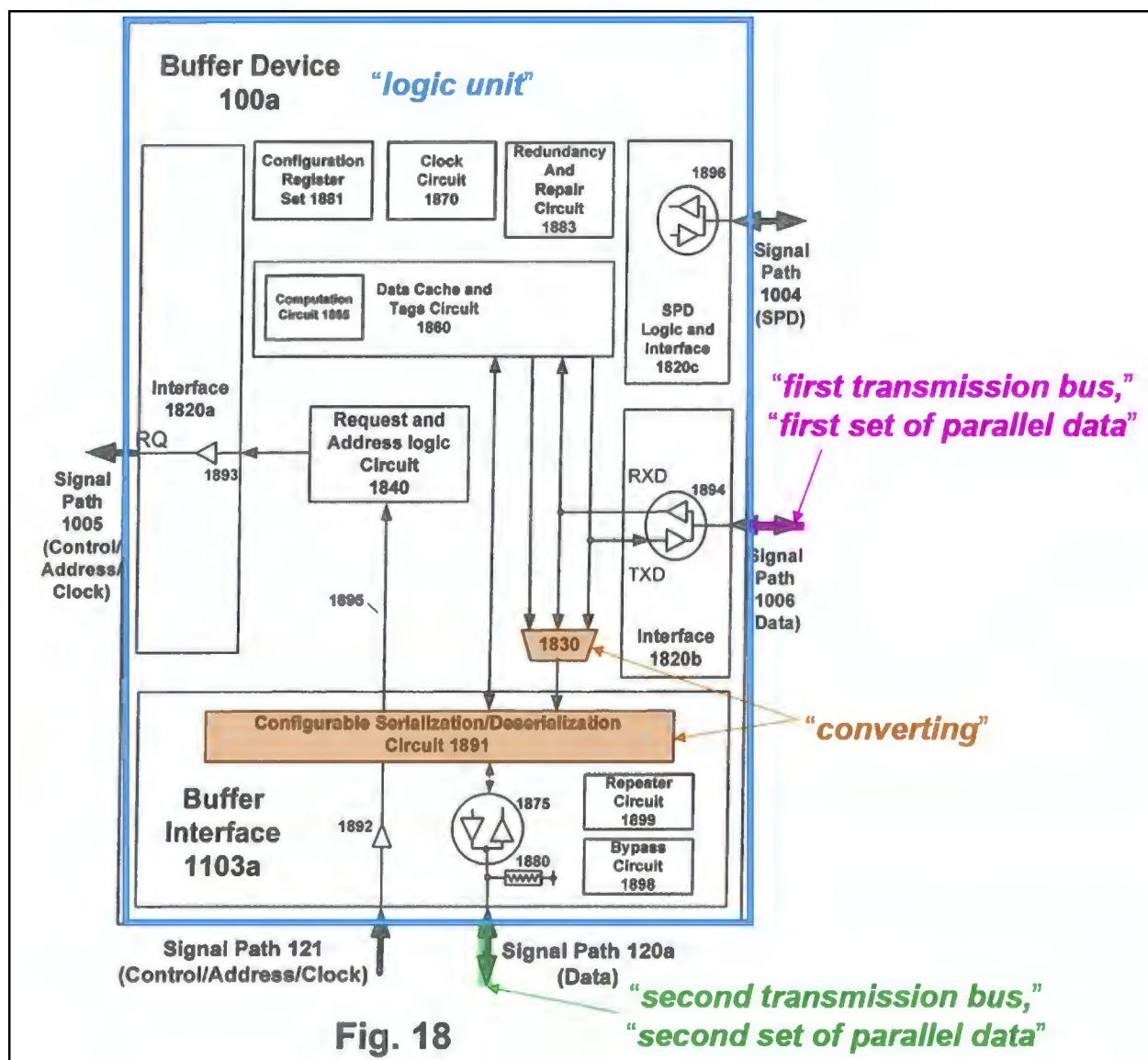
138. Thus, when reading from the memory devices, Tsern's buffer device 100a receives parallel data from the memory devices along multiple signal paths, and then transmits parallel data to the memory controller along a single signal path.

This involves **converting** the parallel data carried along the multiple signal paths 1006 to parallel data carried along the signal path 120a. For instance, the conversion of the parallel data on signal paths 1006 to the parallel data on the signal path 120a is accomplished through components including a “configurable serialization/deserialization circuit 1891,” which “performs serialization and deserialization functions depending upon a stored serialization ratio.” EX1005, 38. That is, the circuit 1891 converts the multiple sets of parallel data received along the signal paths 1006 to a single set of parallel data for transmission along the signal path 120a. A “multiplexer 1830” also participates in converting the parallel data on signal paths 1006 to the parallel data on the signal path 120a through its “bandwidth-concentrating operations” to “utilize[] the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” EX1005, 33; *see* EX1019, Abstract (showing conversion of parallel data from one bit width to parallel data of another bit width).

139. This parallel-to-parallel conversion functionality is implemented in the memory hub of the combination as shown in the composite figure below. The memory hub (corresponding to the claimed ***logic unit***) is implemented based on Tsern’s buffer device 100a of Fig. 18, *e.g.*, based on Tsern’s teachings that buffer device 100a components are ***used for converting the first set of parallel data into a second set of parallel data***, as I discussed in the previous paragraph.

Specifically, as taught by Lee (and consistent with operation of Tsern's buffer device 100a) the combination memory hub communicates a ***first set of parallel data*** to/from memory devices (*e.g.*, ranks of DRAM devices) via bus systems 76, 82, 90, 94 (which correspond individually or collectively to the claimed ***first transmission bus***, as I discussed for Ground 1A) (pink), as taught by Lee. *See* [1b], *supra*. The combination memory hub also communicates a ***second set of parallel data*** to/from a memory controller via high-speed bus 58 (which corresponds to the claimed ***second transmission bus***, as I also discussed above for Ground 1A) (green), as also taught by Lee and consistent with operation of Tsern's buffer device 100a.

140. Elements of the combination memory hub, including a configurable serialization/deserialization circuit 1891 and a multiplexer 1830 (orange *infra*) based on Tsern, ***convert the first set of parallel data into a second set of parallel data, i.e.***, convert the parallel data received on one or all of the bus systems 76, 82, 90, 94 into parallel data for transmission on the high-speed bus 58. This is consistent with the operation of these components as disclosed by Tsern, which I explained earlier in this section.



Lee-Chang-Tsern composite figure based on Tsern, Fig. 18

Tsern's buffer device 3600 renders obvious parallel-to-parallel conversion

141. In another example of the Lee-Chang-Tsern combination system, the memory hub (corresponding to the claimed *logic unit*) is implemented based on Tsern's description of its buffer device 3600, *e.g.*, the buffer device illustrated in Fig. 36. In this example, based on the teachings of Tsern about the buffer device

3600, and as I discuss in more detail in the following paragraphs, the memory hub (*logic unit*) is *used for converting the first set of parallel data into the second set of parallel data*.

142. As I discussed previously, in Tsern's system, data is communicated between the buffer device 3600 and multiple memory devices via the multiple "signal paths 1006." EX1005, 68. Each of these signal paths 1006 carries *parallel data*, as I discussed above in the context of the first example of the Lee-Tsern combination. EX1005, 37-38. In addition, data is communicated between the buffer device 3600 and a memory controller via a signal path 120a, which also carries *parallel data*, as I also discussed above for the first example of the combination. *See* EX1005, 12, 14-15, 38.

143. Thus, when reading from the memory devices, Tsern's buffer device 3600 receives parallel data from the memory devices along multiple signal paths, and then transmits parallel data to the memory controller along a single signal path. This involves *converting* the parallel data carried along the multiple signal paths 1006 to parallel data output through interface 3601 onto the signal path 120a. For instance, the conversion of the parallel data on signal paths 1006 to the parallel data on the signal path 120a is accomplished through components including "data path 3606 and data path router 3610," which "merge separate read data from more than one memory device into a single merged read data or read stream output at

interface 3601.” EX1005, 36. That is, these components convert the multiple sets of parallel data received along the signal paths 1006 to a single set of parallel data for transmission along the signal path 120a.

144. This parallel-to-parallel conversion functionality is implemented in the memory hub of the combination as shown in the composite figure below. The memory hub (corresponding to the claimed *logic unit*) is implemented based on Tsern’s buffer device 3600, *e.g.*, based on Tsern’s teachings that buffer device 3600 components are *used for converting the first set of parallel data into a second set of parallel data*, as I discussed in the previous paragraph. Specifically, as taught by Lee (consistent with operation of Tsern’s buffer device 3600), the combination memory hub communicates a *first set of parallel data* to/from memory devices (*e.g.*, ranks of DRAM devices) via bus systems 76, 82, 90, 94 (which correspond individually or collectively to the claimed *first transmission bus*, as I discussed for Ground 1A) (pink), as taught by Lee. *See* [1b], *supra*. The combination memory hub also communicates a *second set of parallel data* to/from a memory controller via high-speed bus 58 (which corresponds to the claimed *second transmission bus*, as I also discussed above for Ground 1A) (green), as also taught by Lee and consistent with operation of Tsern’s buffer device 3600.

145. Elements of the combination memory hub based on Tsern, including “data path 3606 and data path router 3610” (orange *infra*), *convert* (“merge”) *the*

first set of parallel data into a second set of parallel data, i.e., convert the parallel data received on one or all of the bus systems 76, 82, 90, 94 into parallel data for transmission on the high-speed bus 58. This is consistent with the operation of these components as disclosed by Tsern, which I explained earlier in this section. See EX1005, 68.

Lee-Chang-Tsern composite figure based on Tsern, Fig. 36

[2a] The reconfigurable high speed memory chip module of claim 1,
wherein the first transmission bus is used for transmitting the first set of parallel
data along with the multiple memory cell array ICs, and

146. These limitations are rendered obvious by the Lee-Chang-Tsern combination for reasons similar to those I discussed above for elements [2a]-[2b] of Ground 1A, *supra*.

(c) **Claim 4**

[4] The reconfigurable high speed memory chip module of claim 1, wherein programmability of the first transmission bus or the second transmission bus corresponds to a one-time programming (OTP), a multi-time programming (MTP), a Flash Memory, an embedded memory, an anti-fuse, a register, firmware, or software.

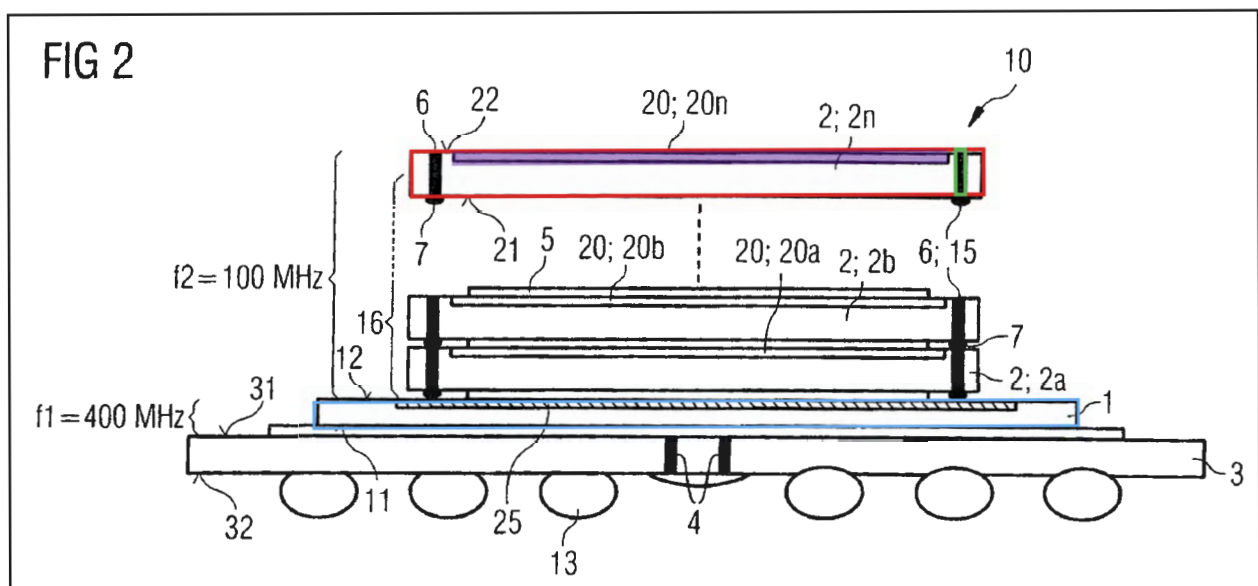
147. These limitations are rendered obvious by the Lee-Chang-Tsern combination for reasons similar to those I discussed above for claim [4] of Ground 1A.

C. [Ground 1C]: Lee, Chang, Tsern, and Raghuram Render Obvious Claims 5, 13, and 14

1. Raghuram (EX1008)

148. Raghuram describes “a semiconductor product” in which “second semiconductor chips 2,” red in FIG. 2, below, are “stacked on one another and on the first semiconductor chip 1 [blue] by means of electrically conductive connecting means 15, which comprise through-hole fillings 6 [green] and bond balls 7.” EX1011, [0088]. The second semiconductor chips “each comprise at least one memory bank,” such as a DRAM memory bank, and “[t]he integrated circuit of the first semiconductor chip 1 essentially is formed of a input/output

circuitry.” *Id.*, [0036], [0085]. The memory banks 20, purple, are “provided at top main surfaces 22 of the second semiconductor chips 2” and “essentially extend over the entire top main surface 22 of the respective semiconductor chip 2. *Id.*, [0089], [0091]. The electrical contacts (*e.g.*, through-hole fillings) are arranged “[i]n the remaining portion of the upper main surface” that is not “covered with the memory bank 20.” *Id.*, [0091].



Excerpt from Raghuram, FIG. 2 (annotated)

149. Raghuram is from the same field of endeavor (*e.g.*, memory systems) as the '834 Patent. *See* EX1001, 1:28-33; EX1011, Abstract.

150. Also, Raghuram is reasonably pertinent to the problem the '834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation

capability”). *See* EX1001, 1:28-33; EX1011, Abstract. For instance, Raghuram’s memory systems provide “increased storage capacity” and are “operable at higher frequencies than conventional memory chips,” advantages that are relevant to development of high-speed, efficient memory systems. *See* EX1011, [0007].

2. The Lee-Chang-Tsern-Raghuram Combination

151. In the Lee-Chang-Tsern-Raghuram combination, the memory hub 60 and one or more ranks of memory devices 70 are assembled into “a semiconductor product” based on the teachings of Raghuram. EX1011, [0088]. Specifically, the memory devices of the combination correspond to Raghuram’s second semiconductor chips 2, and the memory hub of the combination corresponds to Raghuram’s first semiconductor chip 1. Memory banks (highlighted in purple in the composite figure below) of the memory devices (outlined in red) are “provided at top main surfaces 22 of the second semiconductor chips 2” (*i.e.*, at the top surfaces of the memory device chips). EX1011, [0088]-[0089]. The memory device chips themselves are “stacked on one another and on the first semiconductor chip 1,” *i.e.*, on the memory hub (outlined in blue). EX1011, [0088]-[0089]. The chips are connected “by means of electrically conductive connecting means 15, which comprise through-hole fillings 6 [marked in green] and bond balls 7,” which are arranged in “the remaining portion of the main

EX1009, 1 (describing that 3D stacked chips enables performance advantages by “integrating more devices into a smaller volume”).

154. Second, the arrangement described by Raghuram advantageously has “an increased number of memory cells without any increase of the load capacitance and parasitic electrical influences for inputting and outputting information to and from the memory chips.” EX1011, [0007].

155. Third, the arrangement described by Raghuram advantageously is “operable at higher frequencies than conventional memory chips without the need to reduce the clock frequency.” EX1011, [0007].

156. Fourth, with the use of through-hole fillings connecting the stacked chips, “no bond wires are required that would need to be provided laterally beyond the size of the second semiconductor chips,” advantageously reducing the size and complexity of the package. EX1011, [0088].

157. Fifth, a POSITA would have been motivated to arrange Lee’s DRAM memory chips and memory hub as taught by Raghuram because doing so is a mere implementation detail for a feature—the physical arrangement of the chips—that that is not specified by Lee.

158. Sixth, this arrangement is merely the application of known techniques (e.g., a particular arrangement of chips in a memory module) to a known structure (e.g., Lee’s DRAM memory chips and memory hub), and it yields predictable

results (e.g., a memory module in which memory chips are stacked above a memory hub chip).

159. A POSITA would have had a reasonable expectation of success in arranging the chips based on Raghuram because memory system technology is predictable and because a stacked package of memory chips and logic chips was conventional and well-understood. *See, e.g.,* EX1005, Fig. 11; EX1009, 1; EX1016, Fig. 18.

4. Analysis of claims

160. For the reasons below, claims 5, 13, and 14 are obvious over Lee, Chang, Tsern, and Raghuram.

(a) Claim 5

[5a] The reconfigurable high speed memory chip module of claim 1, wherein at least one through silicon via (TSV) exists within a non-active circuit region surrounding or partially surrounding an active circuit region of each of the memory cell array ICs, and

161. In a system based on the Lee-Chang-Tsern-Raghuram combination, the memory hub IC 60 and one or more ranks of memory device ICs 70 are assembled into “a semiconductor product” based on the teachings of Raghuram. EX1011, [0088]. Specifically, the memory devices (corresponding to the claimed ***memory cell array ICs***) and memory hub (corresponding to the claimed ***logic unit***) are arranged based on Raghuram’s arrangement of second semiconductor chips 2

163. Based on Raghuram, “the memory banks [20] essentially extend over the entire top main surface 22 of the respective second semiconductor chip 2.” EX1011, [0091]. The “portion of the upper main surface covered with the memory bank 20,” purple in the figure above, corresponds to the claimed *active circuit region of a memory cell array IC*, e.g., because it contains the memory circuitry for the memory cell array IC. *Id.*

164. “[O]nly electrical contacts to be contacted by the conductive connecting means” (including the *TSVs*) are “arranged” “[i]n the remaining portion of the main surface” that is not “covered with the memory bank.” EX1011, [0091]. This remaining portion, highlighted green in the figure above, corresponds to *a non-active circuit region of a memory cell array IC*, e.g., because it is the region of the chip that does not contain memory circuitry. *See id.* (“[O]nly electrical contacts ... need to be arranged,” and “no further input/output circuitry” is to be provided). The non-active circuit region, which contains the TSVs, *surrounds* the memory bank (corresponding to the claimed *active circuit region*), e.g., as illustrated in FIG. 2. *Id.*; *see* EX1011, [0091] (“the portion of the upper main surface covered with the memory bank 20 may be more than 85%, preferably more than 90% and more preferably more than 95% of the entire upper main surface 22. In the remaining portion of the main surface only electrical contacts to be contacted by the conductive connecting means 15 need to be arranged”). This

satisfies the claimed requirement that *at least one TSV exists within a non-active circuit region surrounding or partially surrounding an active circuit region.*

[5b] the active circuit region is used for forming at least one active device of the memory cell array IC.

165. The “portion of the upper main surface covered with the memory bank 20” (corresponding to the claimed *active circuit region of a memory cell array IC*) contains the memory bank, which “includ[es] a plurality of memory cells.” EX1011, [0008], [0091]. Memory cells correspond to the claimed *at least one active device*, e.g., because memory cells contain circuitry for carrying out memory device functionality, e.g., data storage. This satisfies the claimed requirement that *the active circuit region is used for forming at least one active device.*

(b) **Claim 13**

[13] The reconfigurable high speed memory chip module of claim 5, wherein the non-active circuit region has a width less than about 50 um.

166. It is my opinion that a non-active circuit region having a “width less than about 50 um” is just a straightforward and obvious design choice. For instance, the '834 Patent does not describe any unexpected results or solution related to non-active circuit regions of this width. Moreover, a non-active circuit region having a width of less than about 50 μm was conventional. For instance,

Lee-378 describes scribe lines (*e.g.*, non-active regions surrounding areas in an integrated circuit containing active devices) that have widths “of between about 20 μm and about 180 μm .” EX1023, [0022]. In this context, a POSITA would have considered non-active circuit regions of various conventional widths, among which a width less than about 50 μm .

(c) ***Claim 14***

[14] The reconfigurable high speed memory chip module of claim 5, wherein the at least one TSV has a width less than about 20 μm .

167. It is my opinion that at least one TSV having a “width less than about 20 μm ” is just a straightforward and obvious design choice. For instance, the ’834 Patent does not describe any unexpected results or solution related to TSVs of this width. Moreover, a TSV having a width of less than about 20 μm was conventional. *See* EX1024, [0018] (describing TSVs having a width “in a range from about 1 μm to about 20 μm ”). In this context, a POSITA would have considered TSVs of various conventional widths, among which a width less than about 20 μm .

D. [Ground 1D]: Lee, Chang, Tsern, and White Render Obvious Claims 6-8, 18, and 19

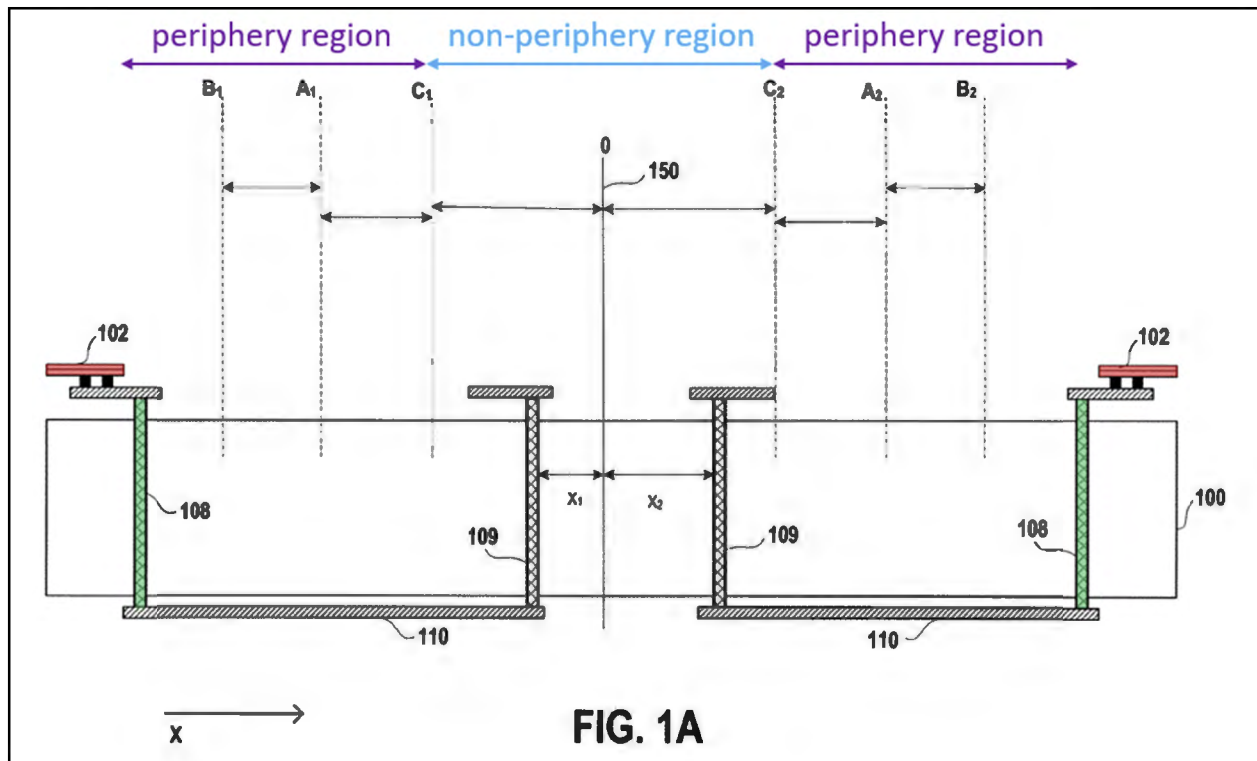
1. White

168. White describes an “integrated circuit with distributed power using through-silicon vias (TSVs).” EX1014, Abstract. White’s integrated circuit has a

“non-periphery region ... where the active device processing occurs,” marked in blue in FIG. 1A, below. EX1014, 3:26-30. Surrounding the non-periphery region is a “periphery region,” marked in purple. EX1014, 3:26-30; *see* 3:29-44. White provides various options for the extent of the periphery and non-periphery regions, and the marked regions below are consistent with one of these options.

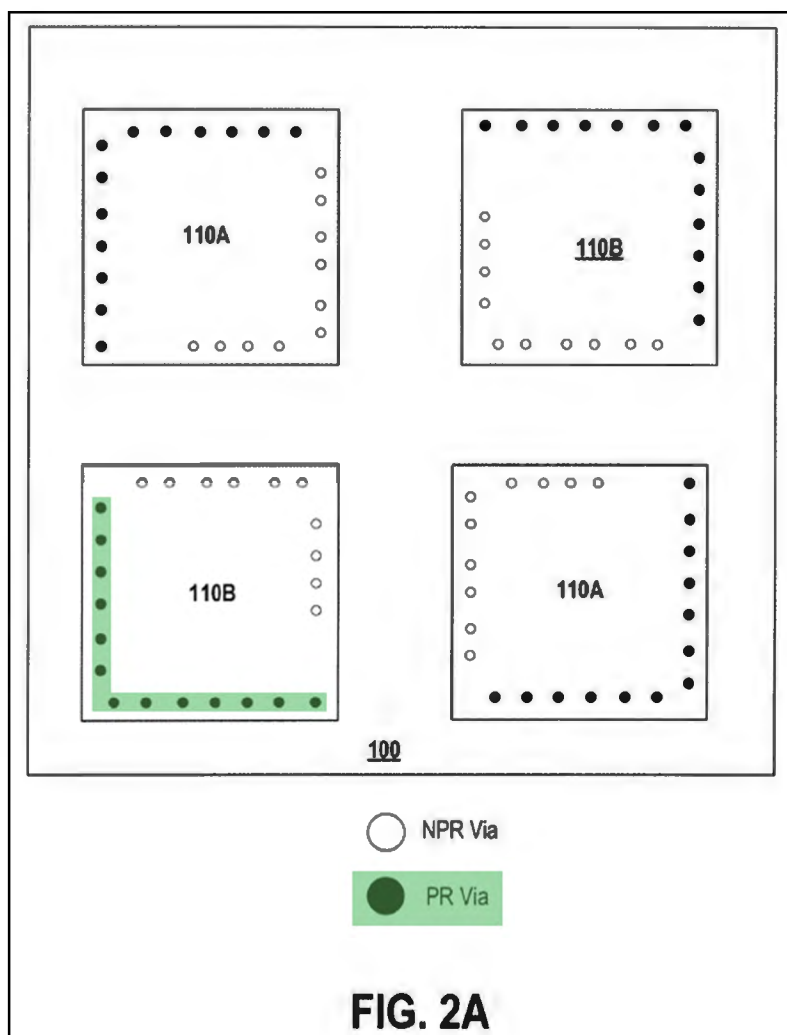
Specifically, White states that “[i]n one IC layout, the non-periphery region could span the area between C1 and C2” (as marked in the figure below), while “in another IC layout, the non-periphery region may span the area between A1 and A2.” *Id.*, 3:31-36. Similarly, regarding the periphery region, “[i]n one IC layout, the periphery portion extends from the bonding pads 102 [marked in red] to B1 and B2, while in another IC layout the periphery portion extends from the bonding pads 102 to C1 and C2.” *Id.*, 3:38-41.

169. “TSVs 108 and 109” (highlighted in green in FIG. 1A, below) “may be used to route power and ground from the bonding pads 102, to the non-periphery region.” *Id.*, 3:48-49. For instance, “a power source” can be “coupled to the conductive bondpads 102.” *Id.*, 4:35.



Excerpt from White, FIG. 1A (annotated)

170. White's FIG. 2A, *infra*, shows a bottom view of "an integrated circuit with conductive areas to distribute power and ground to the non-periphery region." EX1014, 4:48-50. "TSVs in the periphery region [PR]," some of which are highlighted in green, "provide ground to the ground conductive areas 110A and power to the power conductive areas 110B." *Id.*, 4:58-61.



Excerpt from White, FIG. 2A (annotated)

171. White is reasonably pertinent to the problem the '834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:28-33. For instance, White’s TSV-mediated power supply architecture “provid[es] a constant voltage to circuits located within the

non-periphery region,” which is relevant to questions of power consumption.

EX1014, 2:5-7; *see* EX1001, 1:28-33.

2. The Lee-Chang-Tsern-White Combination

172. In the system based on the Lee-Chang-Tsern-White combination, the memory hub 60 and the memory devices 70 are IC chips (as I have already discussed), with each of the chips structured based on the teachings of White to include peripheral TSVs that provide power/ground to non-peripheral active devices. In the case of the memory hub chip, logic circuitry (*e.g.*, transistors and associated circuitry) for execution of memory hub functionality is formed in the non-peripheral region of the chip, *e.g.*, as is the case for White’s non-peripheral region. *See* EX1014, 3:26-30; *see* FIG. 1A. In the case of the memory devices (*e.g.*, DRAM chips), memory circuitry (*e.g.*, transistors and associated circuitry) for storage/execution of storage related functions is formed in the active circuit region of each chip, again as is the case for White’s non-peripheral region. TSVs in the periphery region are coupled to conductive bond pads and used to “route power and ground from the bonding pads 102, to the non-periphery region.”

EX1014, 3:48-49.

3. Motivation to Combine and Expectation of Success

173. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement peripheral TSVs in the memory hub and memory device ICs in the combination.

174. First, having TSVs in the ICs (*e.g.*, memory hub ICs and/or memory device ICs) allows the chips to be stacked “as three-dimensional structures.”

EX1013, [0003]. Being able to arrange chips in a stacked arrangement is advantageous for several reasons. First, stacking of chips “significantly reduce[s] the communication path length between components on different dies,” and as a result, “the overall system speed is ... increased.” *Id.*, [0003]. Also, stacking of chips provides additional benefits including “improved form factors, lower costs, and greater integration through system-on-chip (SOC) solutions.” *Id.*, [0004].

175. Second, distributing power from peripheral to non-peripheral regions of a chip using TSVs, as taught by White, advantageously “reduces the effect of resistive voltage drops on a conducting line,” contributing to improved performance and stability. EX1014, 4:16-29.

176. Third, the use of TSVs to connect to power or ground was conventional, and a POSITA would have been motivated to design the chips of the combination consistent with conventional IC design approaches. EX1014, 3:1-2 (“there are several well-known methods which can be used to manufacture

TSVs”); EX1025, [0025] (describing a “TSV 150 which couples to bond pad 44 for coupling bond pad 44 to ground”).

177. Fourth, the implementation of TSVs in the ICs of the combination system merely the application of known techniques (TSVs in integrated circuits) to a known structure (the memory hub and memory device ICs of the combination memory system), and it yields predictable results (that is, memory hub and memory device ICs implemented with TSVs).

178. A POSITA would have had a reasonable expectation of success in implementing TSVs in the chips of the combination system because integrated circuit structure is predictable. Moreover, a POSITA would have had a reasonable expectation of success because implementation of TSVs in ICs, and uses of TSVs for connection to power/ground, was conventional, in both memory and logic chips. *See* EX1014, 3:1-2; EX1025, [0025].

4. Analysis of claims

179. For the reasons below, claims 6-8, 18, and 19 are obvious over Lee, Chang, Tsern, and White.

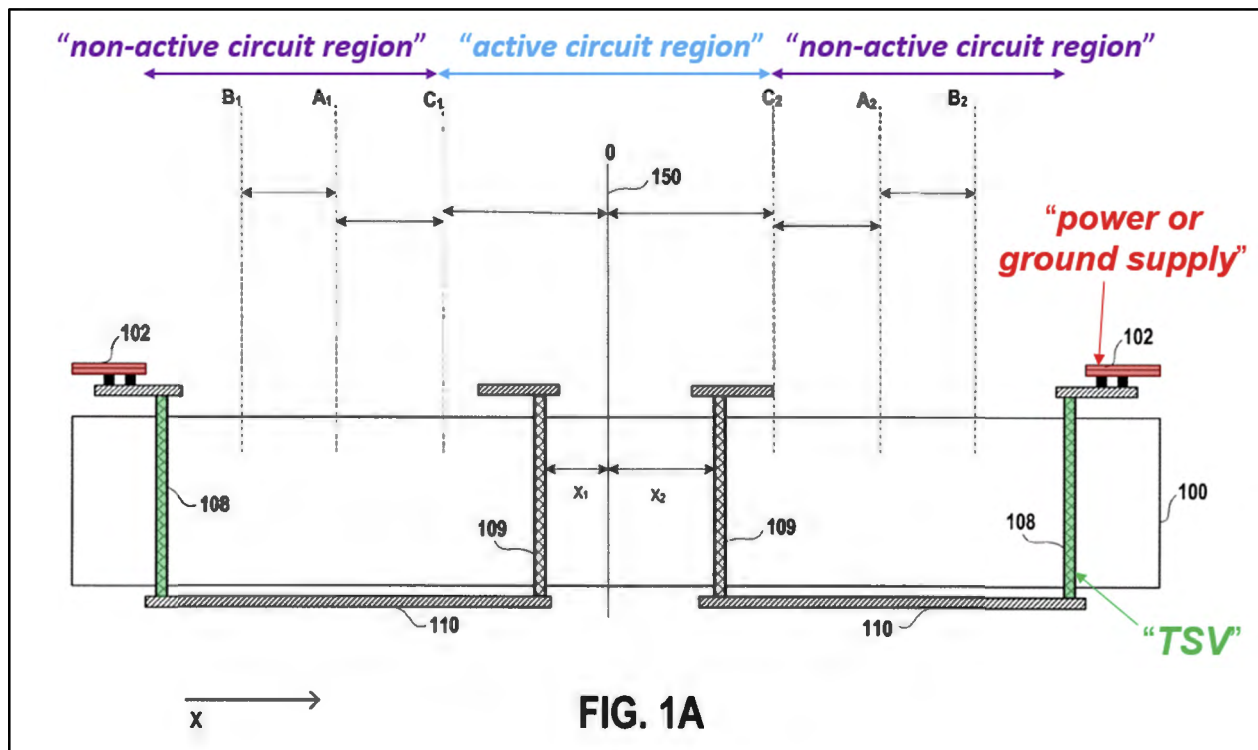
(a) Claim 6

[6a] The reconfigurable high speed memory chip module of claim 1, wherein at least one TSV exists within a non-active circuit region surrounding or partially surrounding an active circuit region of the logic unit, and the active circuit region is used for forming at least one active device of the logic unit,

180. In the Lee-Chang-Tsern-White combination, the memory hub (corresponding to the claimed ***logic unit***) is an integrated circuit that have a structure based on White. Specifically, the memory hub is structured to have “a periphery region (PR) and a non-periphery region (NPR),” with TSVs providing power from the periphery region to the non-periphery region. EX1014, 3:26-28.

181. The non-periphery region (marked in blue in FIG. 1A, below) “is the interior area where the active device processing occurs.” EX1014, 3:28-30 *see* 1:56-57 (“circuits located within the non-peripheral region of the integrated circuit chip”). In the memory hub (***logic unit***) chip of the combination, the circuitry for memory hub processing is located in the non-peripheral region. The non-periphery region corresponds to the claimed ***active circuit region used for forming at least one active device of the logic unit*** at least because it contains “circuits” for “active device processing.” *See id.*; 3:31-36 (“The area encompassed by the non-periphery region varies depending on the specific layout of the active processing region of the integrated circuit 100. In one IC layout, the non-periphery region could span the area between C₁ and C₂, and in another IC layout, the non-periphery region may span the area between A₁ and A₂”), 4:1-3 (“logic elements which are located within the non-periphery region of the integrated circuit”), 4:27-29 (“The integrated circuit chip 100 has a number of logic elements 104 distributed throughout the non-periphery region.”), claims 1 and 9 (“a plurality of circuits

located within the non-periphery region of the integrated circuit chip ... the plurality of circuits further comprising: a plurality of logic elements”) 4:13-15, 4:37-40, 4:61-62, 5:41-42, 5:53-55, 5:61-64.



Excerpt from White, FIG. 1A (annotated)

182. The periphery region (marked in purple in FIG. 1A) “is defined from the bonding pad 102 area [red] to the boundary of the non-periphery region.”

EX1014, 3:37-38. That is, the periphery region is outside of the area where active device processing occurs, and thus the periphery region (purple) corresponds to a *non-active circuit region surrounding/partially surrounding the active circuit region* (the non-periphery region). *See id.*, 3:38-41 (“In one IC layout, the periphery portion extends from the bonding pads 102 to B₁ and B₂, while in

another IC layout the periphery portion extends from the bonding pads 102 to C₁ and C₂”).

183. Based on White, “through-silicon-vias 108” (marked in green) are “formed within the periphery region of the IC chip,” thus satisfying the claimed requirement that *at least one TSV exists within the non-active circuit region*.

EX1014, 3:48-50; *see* Abstract (“A number of through-silicon-vias are distributed within the peripheral region”), 1:48-50, 1:62-63, 4:31-32, 4:58-60, 6:38-40, claim 1.

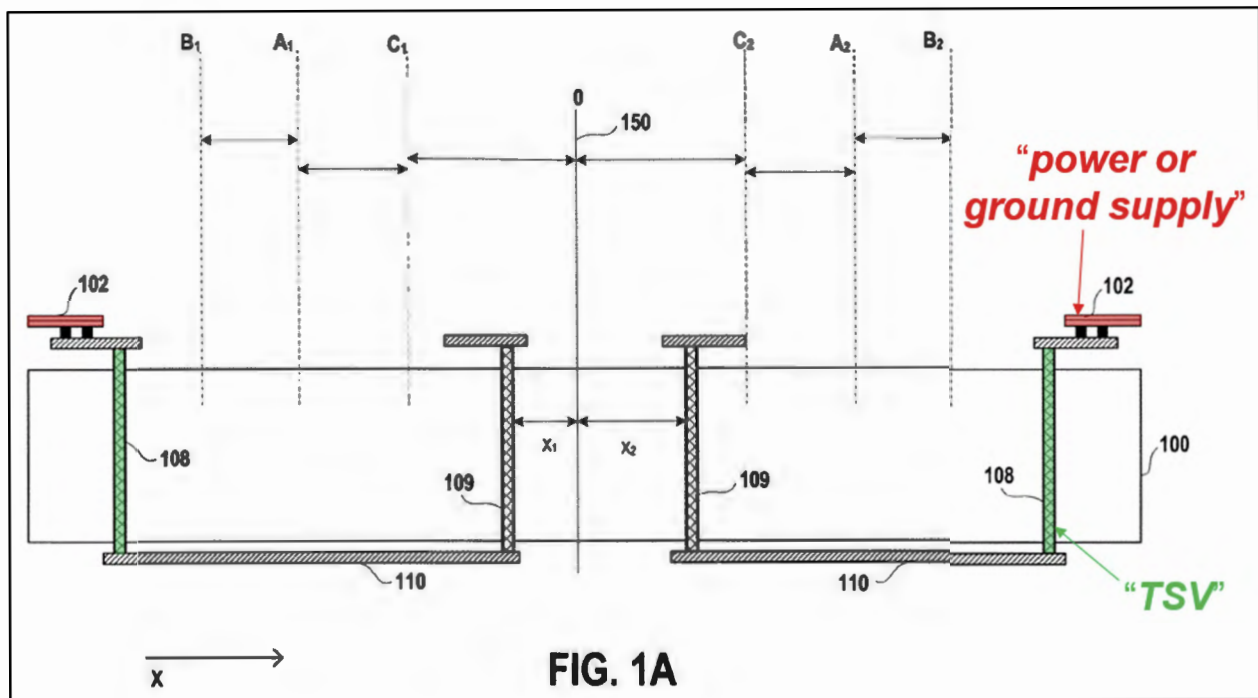
[6b] wherein the at least one TSV is used for connecting to a power or a ground supply.

184. The TSVs of the combination memory hub, based on White, “route power and ground from the bonding pads 102, to the non-periphery region of the integrated circuit chip.” EX1014, 3:48-50; *see* 2:57-58 (“distributing power to the interior of an integrated circuit (IC) chips using through-silicon-vias (TSVs)”).

The bonding pads (red in FIG. 1A, below) “provide power and ground” and thus correspond to *a power or ground supply*. EX1014, 3:17-19; *see* Abstract (“Power is distributed from the conducting pads to the TSVs ... thus supplying power and ground to circuits located within the non-peripheral region of the integrated circuit chip”), 1:46-48 (“The integrated circuit has conducting pads for providing power and ground located within the peripheral region of the top surface”), 3:64-66

(“Power and ground are provided to the integrated circuit from bonding pads”).

The peripheral TSVs are connected to the bonding pads and thus are *used for connecting to the power/ground supply*, as shown in FIG. 1A. *See id.*, 1:53-56 (“Power is distributed from the conducting pads to the TSVs within the non-peripheral region through the TSVs within the peripheral region, thus supplying power and ground to circuits”), 1:38-40 (“a method and apparatus for distributing power to the interior portion of an integrated circuit using through-silicon-vias (TSVs)”), 3:47-50 (“a number of TSVs 108 and 109 may be used to route power and ground from the bonding pads 102, to the non-periphery region of the integrated circuit chip 100”), 4:17-21 (“Using a plurality of TSVs to distribute power to the non-periphery region of the integrated circuit reduces the effect of resistive voltage drops on a conducting line and the observed voltage at the non-periphery region of the integrated circuit is roughly the same as the power supply voltage”), 4:37-46 (“Logic elements 104 located within the non-periphery region can then receive power and ground from the TSVs”), 2:57-58, 3:7-8, 4:24-26, 4:58-63, 5:38-45, 5:65-67, 6:24-26, 6:49-64, claim 1, claim 9.



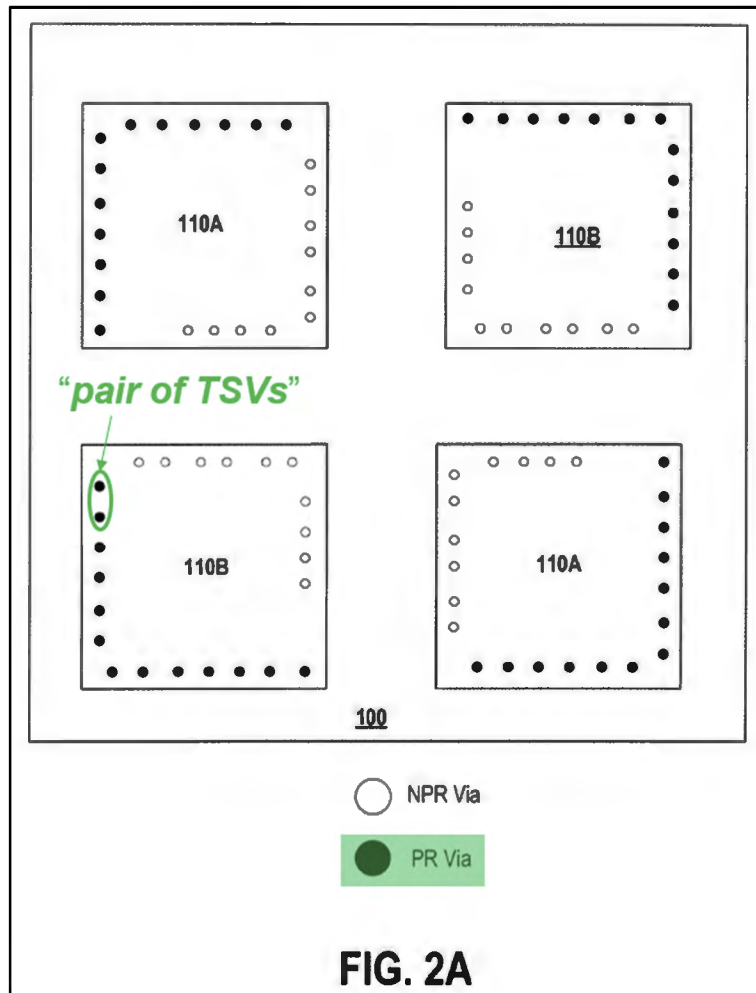
Excerpt from White, FIG. 1A (annotated)

(b) **Claim 7**

[7a] *The reconfigurable high speed memory chip module of claim 1, wherein at least one pair of TSVs exist in neighboring within a non-active circuit region surrounding or partially surrounding an active circuit region of each of the memory cell array ICs, and*

185. In the combination, based on White, each memory device (corresponding to the claimed **memory cell array IC**) includes at least one TSV (e.g., TSVs 108) ***within a non-active circuit region surrounding or partially surrounding an active circuit region***, for at least similar reasons as those I discussed in claim 6 for the logic unit. See EX1014, FIG. 1A, 3:26-55.

186. In the combination memory devices, the “TSVs in the peripheral region [PR]” are arranged based on White’s FIG. 2A, reproduced below. EX1014, 4:58-60. Each two adjacent TSVs corresponding to the claimed *at least one pair of TSVs*. I have circled one such pair.



Excerpt from White, FIG. 2A (annotated)

187. The TSVs of the pair are *neighboring*, *e.g.*, because they are adjacent and non-overlapping. I note that the '834 Patent states the following regarding neighboring TSVs: “at least one pair of TSVs electrically coupled together to a

power or ground supply exist in neighboring (i.e. non-overlapped or contacted physically, where a spacing between the pair of TSVs is less than about 10-30 μm) within a non-active circuit region.” EX1001, 12:49-51. To the extent that Patent Owner argues that the claimed term “neighboring” implies a specified separation distance between TSVs, *e.g.*, less than 10-30 μm (*see*), such a distance is a straightforward and obvious design choice. For instance, the ’834 Patent does not describe any unexpected results or solution related to a TSV separation of less than 10-30 μm .

[7b] wherein the at least one pair of TSVs are used for connecting to a power or a ground supply.

188. The highlighted pair of TSVs in FIG. 2A, *supra*, “provide[s] ... power to the power conductive areas 110B,” and pairs of TSVs in the conductive areas 110A “provide ground to the ground conductive areas 110A,” *e.g.*, by coupling to conductive bondpads. EX1014, 4:58-65. This satisfies the claimed requirement that ***the at least one pair of TSVs are used for connecting to a power or a ground supply***. Moreover, the TSVs based on White are used for connecting to power/ground as I discussed above for element [6b].

(c) ***Claim 8***

[8a] The reconfigurable high speed memory chip module of claim 1, wherein at least one pair of TSVs exist in neighboring within a non-active circuit region surrounding or partially surrounding an active circuit region of the logic

unit, and

[8b] wherein the at least one pair of TSVs are used for connecting to a power or a ground supply.

189. In the combination, based on White, in the memory hub (*logic unit*), *a pair of TSVs exist in neighboring within a non-active circuit region surrounding or partially surrounding an active circuit region*, where the *TSVs are used for connecting to power/ground*, for at least similar reasons as those I discussed above for claim 7. EX1014, 3:26-55, 4:48-65, FIGS. 1A, 2B. Moreover, the TSVs are neighboring, e.g., in that they are in the peripheral region, which is adjacent to but not overlapping with the non-peripheral region (non-active circuit region)

(d) ***Claim 18***

[18] The reconfigurable high speed memory chip module of claim 6, wherein the non-active circuit region has a width less than about 50 μm .

190. It is my opinion that a non-active circuit region having a “width less than about 50 μm ” is just a straightforward and obvious design choice. For instance, the ’834 Patent does not describe any unexpected results or solution related to non-active circuit regions of this width. Moreover, a non-active circuit region having a width of less than about 50 μm was conventional. See EX1023, [0022]. In this context, a POSITA would have considered non-active circuit

regions of various conventional widths, among which a width less than about 50 μm .

(e) ***Claim 19***

[19] The reconfigurable high speed memory chip module of claim 6, wherein the at least one TSV has a width less than about 20 μm .

191. It is my opinion that at least one TSV having a “width less than about 20 μm ” is just a straightforward and obvious design choice. For instance, the ’834 Patent does not describe any unexpected results or solution related to TSVs of this width. Moreover, a TSV having a width of less than about 20 μm was conventional. *See* EX1024, [0018]. In this context, a POSITA would have considered TSVs of various conventional widths, among which a width less than about 20 μm .

E. [Ground 1E]: Lee, Chang, and Dozen or Lee, Chang, Tsern, and Dozen Render Obvious Claim 9

1. Dozen (EX1007)

192. Dozen describes a “method for manufacturing a highly-reliable semiconductor device.” EX1007, Abstract. For instance, Dozen describes manufacturing memory devices, *e.g.*, DRAM, SRAM, or flash memory, in an “element substrate 1102.” EX1007, Abstract, 4:9-26. Among other processing steps, Dozen describes that “where a plurality of semiconductor devices are included in the element substrate 1102, the plurality of semiconductor devices may

be obtained by dividing the element substrate and the sealing layers,” *e.g.*, by “dicing, scribing, using a cutting machine ..., laser cutting, or the like.” EX1007, 11:60-67.

193. Dozen is pertinent to the problem the ’834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:28-33. For instance, Dozen’s manufacturing process produces a “highly-reliable semiconductor device ... with a high yield.” EX1007, Abstract. A high yield process for manufacturing reliable chips used in a memory system is relevant to reducing the greenhouse gas emission rate associated with that memory system, *e.g.*, because higher yield of reliable chips reduces waste. *See* EX1001, 1:28-33.

2. The Lee-Chang-Dozen and Lee-Chang-Tsern-Dozen Combinations

194. In a system based on the combination of Lee, Chang, and Dozen, or Lee, Chang, Tsern, and Dozen, the memory devices are, for instance, DRAM devices, as taught by Lee. EX1004, [0016]. Based on Dozen’s teachings about fabrication of DRAM devices, the DRAM devices of the combination are “formed in [an] element substrate,” such as a wafer. EX1007, 4:9-26. Among other processing steps, individual DRAM chips are obtained from that substrate “by

dividing the element substrate and the sealing layers,” *e.g.*, by “dicing, scribing, using a cutting machine ..., laser cutting, or the like.” EX1007, 11:60-67.

3. Motivation to Combine

195. It is my opinion that there are a number of reasons that would have motivated a POSITA to employ laser dicing of the DRAM chips in the Lee-Chang-Dozen or Lee-Chang-Tsern-Dozen combination based on Dozen’s teachings.

196. First, laser dicing advantageously enables high degrees of precision to be achieved at high processing speeds. This is explained by Akiyama, which identifies laser dicing as achieving “high throughput, low costs, high yield, and high-precision.” EX1020, 7:9-11. Similarly, Dahm describes laser dicing in the context of “high precision cutting.” EX1021, 1:6-8.

197. Second, laser dicing is a contactless processing method, and thus does not subject tools to wear, generates little waste, and does not run significant risks of contamination. EX1021, 1:22-32.

198. Fourth, implementation of laser dicing for the memory cell array chips is one of a finite number of predictable solutions (*e.g.*, laser dicing, physical dicing, scribing), and with a reasonable expectation of success (discussed *infra*). *See* EX1020, Abstract; EX1021, 1:6-9.

199. Fifth, use of laser dicing to dice the DRAM chips in the Lee-Tsern-Khan combination is merely the application of known techniques (specifically,

laser dicing of integrated circuits) to a known system (e.g., Lee's memory (e.g., DRAM) chips), and it yields predictable results (that is, DRAM memory chips separated by a laser dicing process).

200. A POSITA would have had a reasonable expectation of success in using laser dicing for the DRAM chips of the combination because memory system technology and integrated circuit dicing technology are predictable, and because laser dicing of integrated circuit chips was conventional and well-understood. For instance, other examples of laser dicing of integrated circuits are provided by Akiyama and Dahn, which I discussed above. *See* EX1020, Abstract; EX1021, 1:6-9.

4. Analysis of claims

201. For the reasons below, claim 9 is obvious over Lee, Chang, and Dozen or Lee, Chang, Tsern, and Dozen.

(a) Claim 9

[9] The reconfigurable high speed memory chip module of claim 1, wherein a dicing method for at least one memory cell array IC of the multiple memory cell array ICs comprises a laser process.

202. In the combination, memory devices (e.g., DRAM devices, corresponding to the claimed **memory cell array ICs**) are formed in a wafer, e.g., using conventional CMOS processes. *See* EX1007, 4:50-62. The wafer is then divided into individual memory devices by “dicing, scribing, using a cutting

machine ..., laser cutting, or the like,” as taught by Dozen and as was conventional. EX1007, 11:60-67. This processing satisfies the claimed requirement that *a dicing method for at least one memory cell array IC comprises a Laser cutting process.*

F. [Ground 1F]: Lee, Chang, Tsern, and Dozen Render Obvious Claim 10

1. Analysis of claims

203. For the reasons below, claim 10 is obvious over Lee, Chang, Tsern, and Dozen.

(a) Claim 10

[10] The reconfigurable high speed memory chip module of claim 1, wherein a dicing method for the logic unit comprises a laser process.

204. Claim 10 is rendered obvious by the combination of Lee, Chang, Tsern, and Dozen for reasons similar to those I discussed above for claim 9 of Ground 1E.

G. [Ground 1G]: Lee, Chang, Tsern, Raghuram, and White Render Obvious Claim 12

1. Analysis of claims

205. For the reasons below, claim 12 is obvious over Lee, Chang, Tsern, Raghuram, and White.

(a) Claim 12

[12] The reconfigurable high speed memory chip module of claim 5,

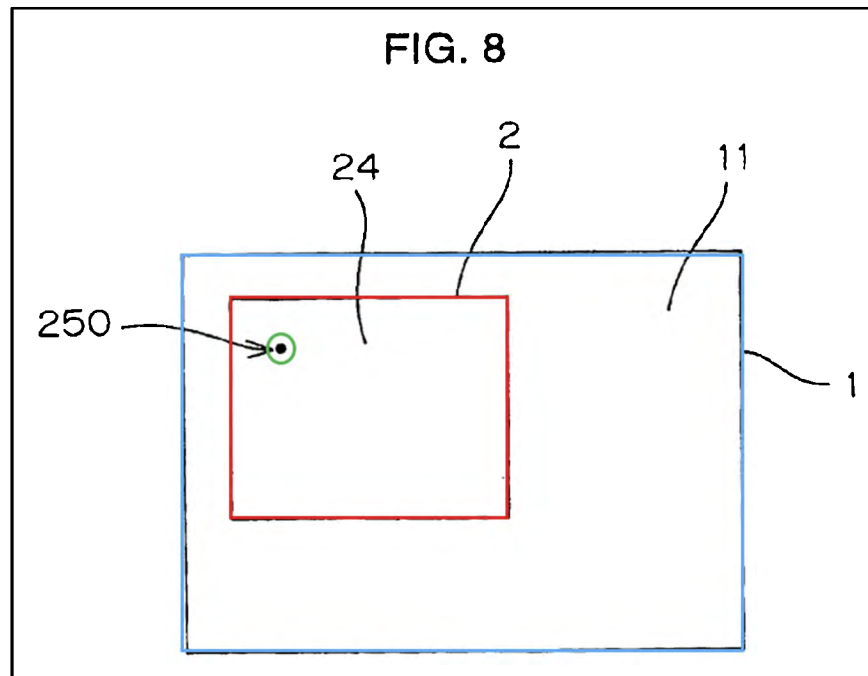
wherein the at least one TSV is used for connecting to a power or a ground supply.

206. Claim 12 is rendered obvious by the combination of Lee, Chang, Tsern, Raghuram, and White for reasons similar to those I discussed above for element [7b] of Ground 1D.

H. [Ground 1H]: Lee, Chang, Tsern, Raghuram, and Hikita Render Obvious Claims 15 and 16

1. Hikita

207. Hikita describes a “chip-on-chip semiconductor device” composed of a primary chip 1 (outlined in blue in FIG. 8, reproduced below) “in a stacked relation” with secondary chips 2 (outlined in red red). EX1015, 12:33-52. A “back mark 250,” circled in green, is “provided on the back face 24 of the secondary chip 2” to “allow for recognition of the orientation of the secondary chip 2, the arrangement of the electrodes 23 provided on the front face 21 of the secondary chip 2, and the like.” *Id.*, 14:28-34.



Excerpt from Hikita, FIG. 8 (annotated)

208. Hikita is reasonably pertinent to the problem the '834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:28-33. For instance, Hikita’s chip-on-chip structures are relevant for arrangement of ICs in memory systems. *See* EX1015, 1:61.

2. The Lee-Chang-Tsern-Raghuram-Hikita Combination

209. In the Lee-Chang-Tsern-Raghuram-Hikita combination, one or more of the ICs (*e.g.*, the memory device ICs and/or the memory hub) are provided with a “back mark ... on the back face” of the chip. EX1015, 14:28-48. As taught by

Hikita, this allows the orientation of the chip to be recognized when assembled with other chips, *e.g.*, in a stacked arrangement.

3. Motivation to Combine and Expectation of Success

210. It is my opinion that there are a number of reasons that would have motivated a POSITA to incorporate orientation marks into one or more of the ICs of the combination memory system.

211. First, in the context of stacked chips (as is the case for the Lee-Chang-Tsern-Raghuram combination, which I discussed above for Ground 1C), orientation marks allow chip orientation to be “recognized by way of the back mark [] so that there is no possibility that the secondary chip 2 is mounted on the primary chip 1 with a 180-degree angular offset.” EX1015, 14:38-42. The ability to recognize chip orientation, and to properly orient the chips during assembly, ensures proper assembly of the chip stack.

Second, a POSITA would have been motivated to use orientation marks because, as explained by Hikita, “the positioning of the semiconductor chips is easy” with these marks, and thus “the time required for assembling the chip-on-chip structure can be reduced.” EX1015, 3:12-14.

212. Third, using orientation marks on chips to aid with assembly is merely the application of known techniques (specifically, orientation marks in ICs) to a known structure (the stacked memory hub and memory device ICs of the

combination memory system), and it yields predictable results (that is, memory hub and memory device ICs implemented with orientation marks to facilitate stacking).

213. A POSITA would have had a reasonable expectation of success in implementing orientation marks because integrated circuit structure is predictable and conventional.

4. Analysis of claims

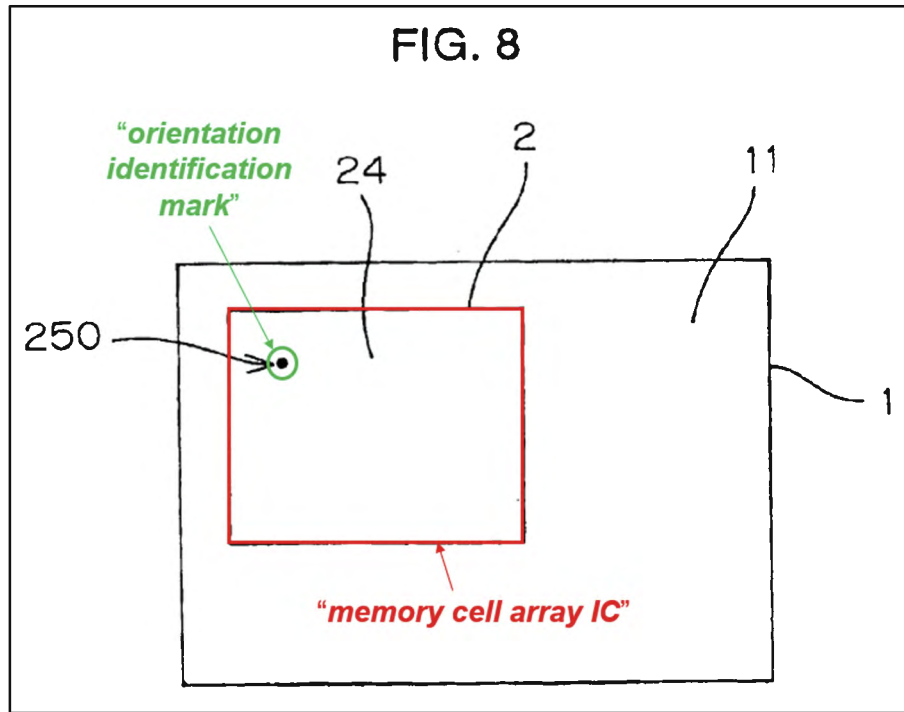
214. For the reasons below, claims 15 and 16 are obvious over Lee, Chang, Tsern, Raghuram, and Hikita.

(a) *Claim 15*

[15] The reconfigurable high speed memory chip module of claim 5, wherein a corner of the memory cell array IC has an orientation identification mark wherein the orientation identification mark is formed by a process comprising Laser step.

215. In the Lee-Chang-Tsern-Raghuram-Hikita combination system, a “back mark 250” (which corresponds to the claimed ***orientation identification mark***) is “provided on the back face” of the memory cell array IC. EX1015, 14:28-33 This orientation mark is to “allow[] for recognition of the orientation” of the memory cell array IC, “the arrangement of the electrodes [] provided on the front face” of the memory cell array IC, “and the like.” *Id.*, 14:28-33; *see* 14:38-43 (“the orientation of the secondary chip 2 can be recognized by way of the back

mark 250”), 15:44-48, FIG. 10. As illustrated in FIG. 8, which I have reproduced below, the back mark (*orientation identification mark*) is located in *a corner* of the IC, as required by the claim.



Excerpt from Hikita, FIG. 8 (annotated)

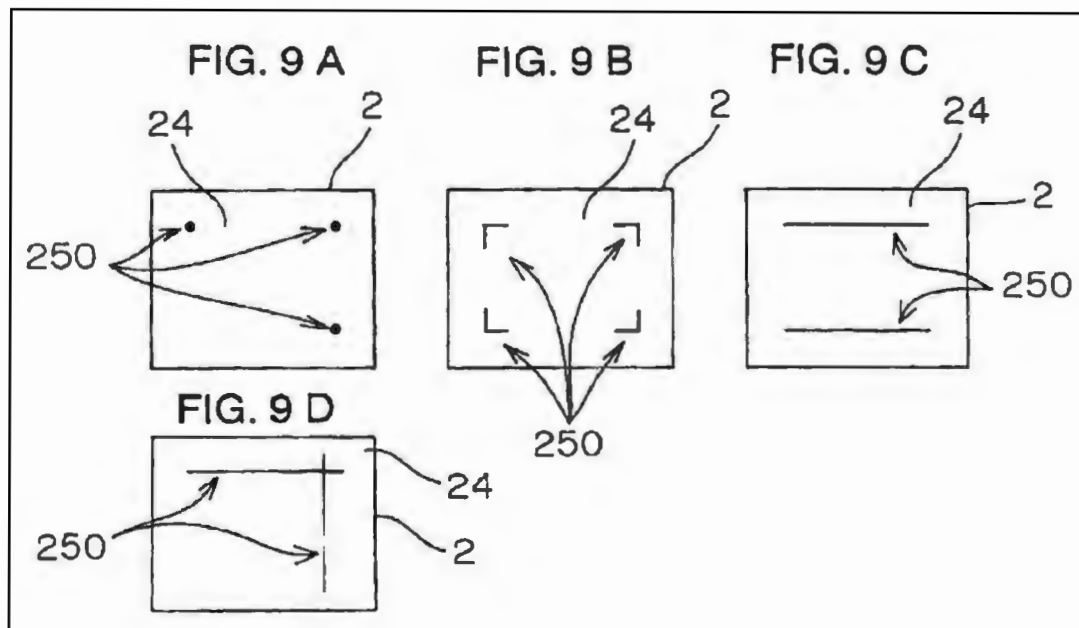
216. Also based on the teachings of Hikita, “formation of the back marks” (corresponding to the claimed *orientation identification mark*) “may be achieved by a ... a laser process,” thus satisfying the claimed requirement that *the orientation identification mark is formed by a process comprising Laser step*. EX1015, 15:2122.

(b) **Claim 16**

[16] *The reconfigurable high speed memory chip module of claim 5, wherein a corner of the memory cell array IC has an orientation identification*

mark wherein the orientation identification mark comprises at least one of an edge cut, a line of drawing, two lines of drawing, a hole, or an arbitrary pattern.

217. In the combination, based on Hikita, the back mark (corresponding to the claimed ***orientation identification mark***) can be a “point or circle,” a “hook- or L-shape,” a symbol such as “+” or “-,” a “line which extends along an edge,” “crossed lines,” or “any notations and marks such as characters and symbols.” EX1015, 15:1-11; *see* FIGS. 8 and 9A-9D, reproduced below. These shapes/symbols correspond to at least the claimed ***line of drawing, two lines of drawing of drawing ..., or an arbitrary pattern.***

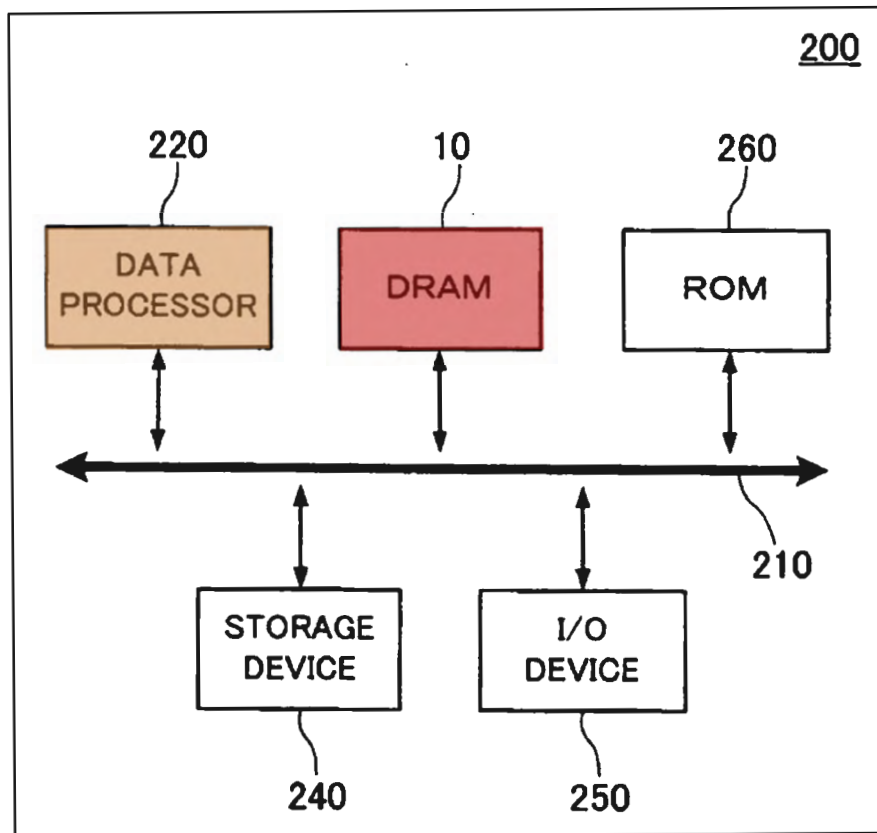


Excerpt from Hikita, FIGS. 9A-9D

I. [Ground 1I]: Claims 21 and 23 Are Obvious Over Lee, Chang, Dono, and Nakai Render Obvious Claims 21 and 23

1. Dono

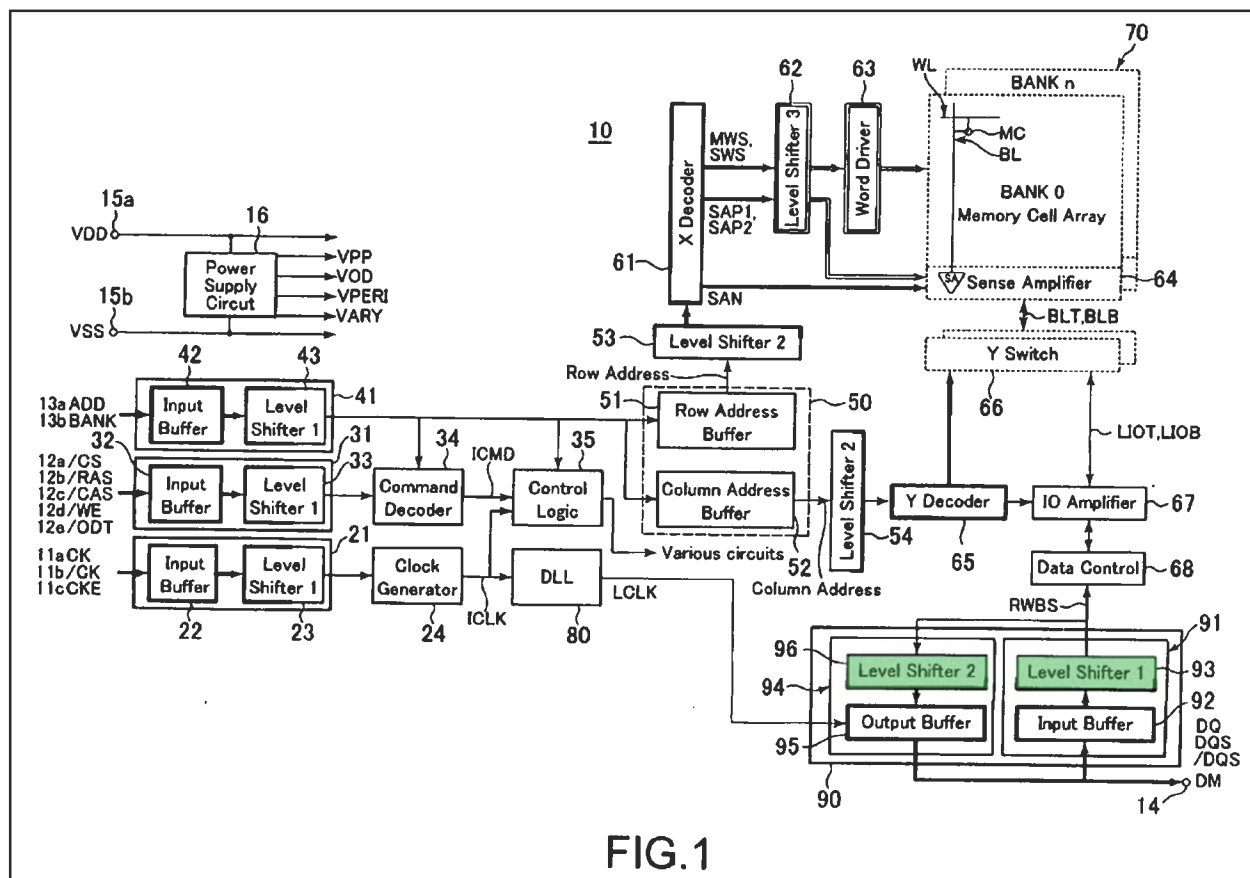
218. Dono describes a “data processing system” including “a data processor 220” (orange in FIG. 11 below) and a “semiconductor device (DRAM) 10” (red) “connected to each other via a system bus 210.” EX1008, [0100]. In Dono’s system the “internal operation voltage VPERI” of the DRAM cell is “lower than an external voltage VDD.” *Id.*, [0004]. I note that it was conventional for DRAM cells to operate at a lower voltage than an external voltage (*e.g.*, a voltage of other system components). *See id.*, [0004]-[0005]. For instance, Dono explains that “a DDR2 SDRAM of 60-nm generation has an external voltage VDD of 1.8V,” while the “peripheral circuit voltage VPERI [is] 1.3 V.” *Id.*, [0005]. To bridge these two different voltages, “a signal from a data processor 220 is supplied to the DRAM 10 via the system bus 210,” and the “DRAM processes the signal from the data processor 220 having the amplitude VDD by converting the signal to a low voltage signal of the internal operation voltage VPERI.” *Id.*, [0103].



Excerpt from Dono, FIG. 11 (annotated)

219. In more detail, Dono's system performs this signal conversion using level shifters that increase the voltage from VDD to VPERI, or decrease the voltage from VPERI to VDD. For instance, voltage reduction is performed by a "level shifter" (level shifter 93, green in FIG. 1, reproduced below) that "reduce[s] the amplitude of the external signal to VPERI," for data signals being transmitted to the DRAM cells. EX1008, [0041]. In reverse, "[d]ata read from a memory cell of the DRAM 10 is converted to a signal having the amplitude VDD, and is transferred to the data processor via the system bus 210," using a "level shifter"

(level shifter 96, green in FIG. 1) that “increase[s] the amplitude VPERI of an internal signal to VDD.” *Id.*, [0041], [0103].



Excerpt from Dono, FIG. 1 (annotated)

220. Dono is from the same field of endeavor (*e.g.*, memory systems) as the '834 Patent. *See* EX1001, 1:28-33; EX1008, [0100].

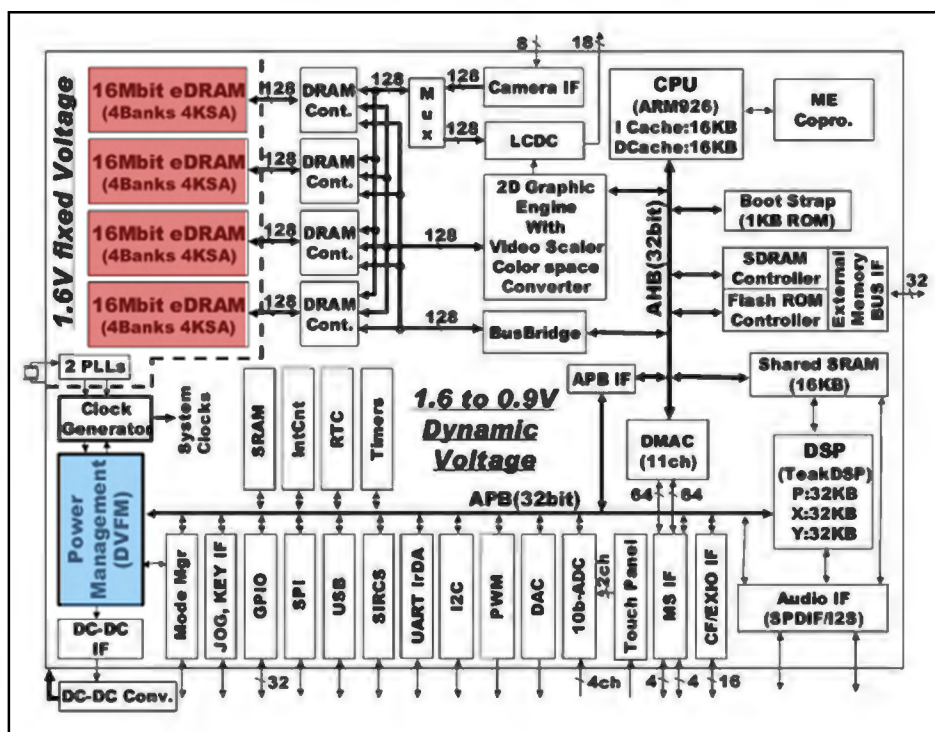
221. Also, Dono is reasonably pertinent to the problem the '834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation

capability”). *See* EX1001, 1:28-33; EX1008, [0100]. For instance, Dono’s DRAM architectures are relevant to development of high-speed, efficient memory systems. *See* EX1008, [0024].

2. Nakai

222. Nakai describes a “dynamic voltage and frequency management (DVFM) scheme” for “a microprocessor with ... embedded DRAM.” EX1017, 1. In Nakai’s system, “[c]lock frequency is autonomously and dynamically controlled while supply voltage is adaptively controlled,” achieving significant “power reduction.” *Id.*.

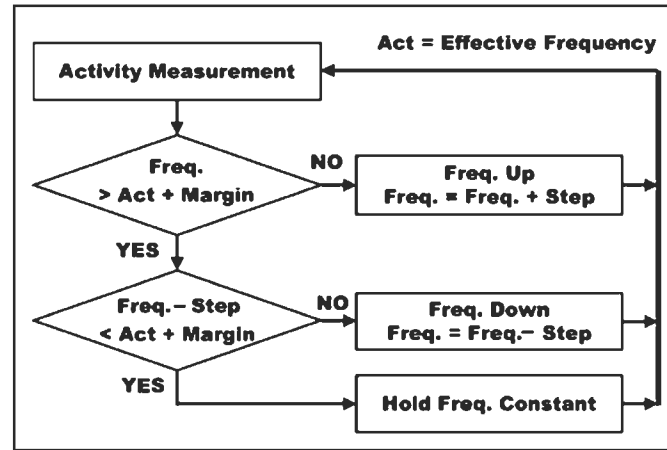
223. Nakai’s system includes “four 128-bit data-width 16-Mb embedded DRAM macros,” red in Fig. 1, below, with “processor blocks [] connected to the embedded DRAM by a 128-bit bus for high memory bandwidth requirements.” EX1017, 1. “Other devices are connected via a bus bridge to a 32-bit bus.” *Id.* The system also includes a “DVFM block [blue], clock generator, and dc-dc IF block [that] control the supply voltage and clock frequency.” *Id.* The supply voltage of circuit blocks other than “the DRAM macros and phase-locked loops” is “controlled dynamically by the DVFM in the range between 0.9 and 1.6 V.” *Id.*, 2. In addition, while “[p]eripheral circuit blocks that communicate with external devices are driven by fixed frequency clocks, ... all other circuit blocks are driven by the dynamically controlled system clock.” *Id.*.



Excerpt from Nakai, Fig. 1 (annotated)

224. In Nakai's system, the dynamic frequency control (DFC) "controls the clock frequency at the required minimum value autonomously in hardware without special power-management software." EX1017, 4. Generally, "total LSI activity" is calculated "periodically from activity information of embedded DRAM, bus, and CPU." *Id.* Each monitoring period, "the DFC uses the activity data to determine the required minimum clock frequency." *Id.*, 5. As shown in Fig. 9, "[w]hen the clock frequency of the monitoring period just ending is less than the value of Act plus Margin, the clock frequency of the next monitoring period is increased," and similarly the clock frequency of the next period is decreased "if the current clock frequency minus the Step value is greater than the value of Act plus Margin." *Id.*

Nakai also notes that “[t]he clock frequency may [] be set directly via software to allow abrupt performance change in response to external events.” *Id.*



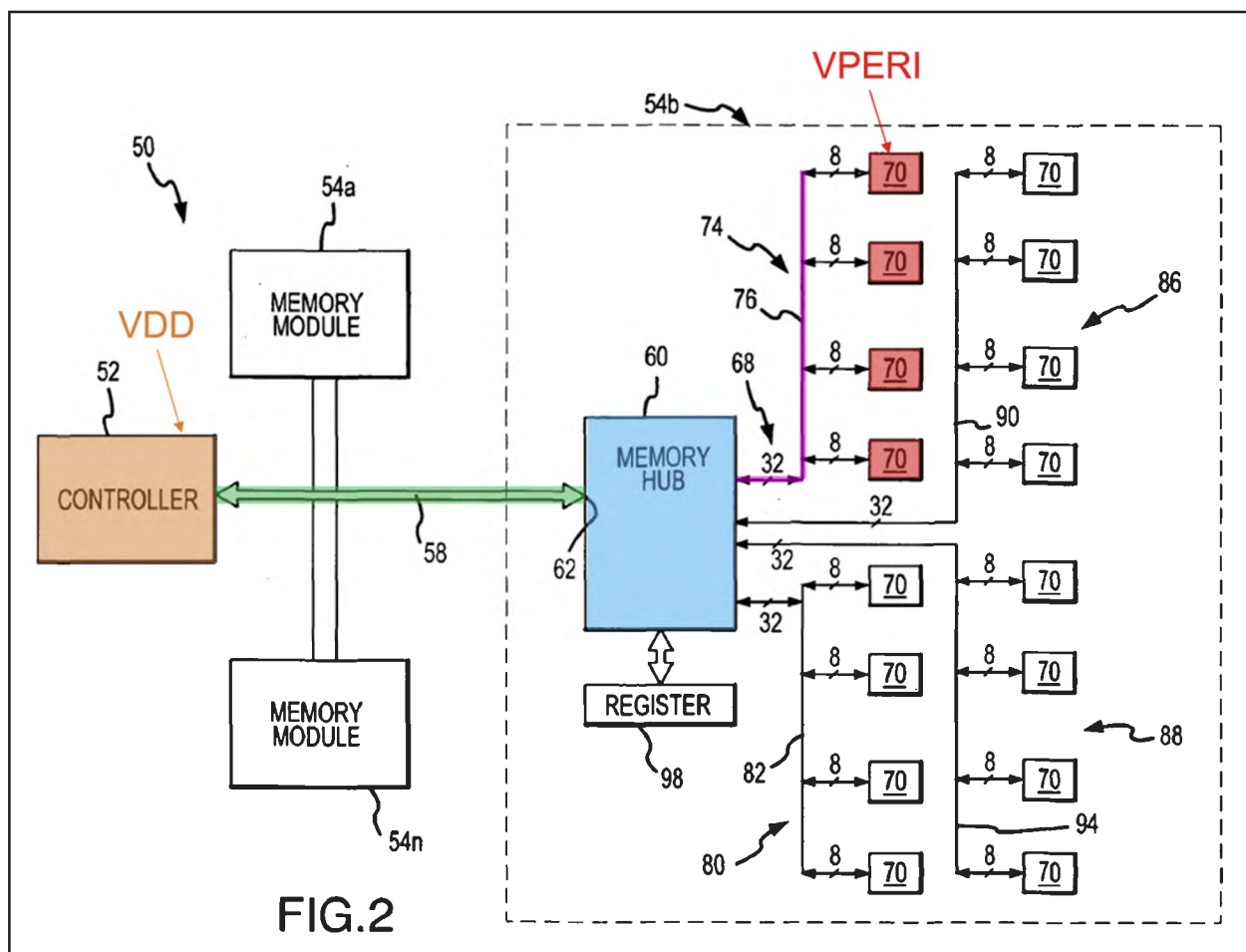
Excerpt from Nakai, Fig. 9

225. Nakai is from the same field of endeavor (*e.g.*, memory systems) as the '834 Patent. *See* EX1001, 1:28-33; EX1017, Abstract.

226. Also, Nakai is reasonably pertinent to the problem the '834 Patent was trying to solve (*e.g.*, development of a high speed memory chip module with, among other advantages, “lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, ... better heat dissipation capability”). *See* EX1001, 1:28-33; EX1017, Abstract. For instance, Nakai’s dynamic voltage and frequency management scheme achieves dramatic power reductions, which is relevant to development of memory systems with “lower power consumption.” *See* EX1017, Abstract; EX1001, 1:28-33.

3. The Lee-Chang-Dono-Nakai Combination

227. In the Lee-Chang-Dono-Nakai combination, the memory devices 70 (*e.g.*, DRAM devices) of Lee's system have an "internal operation voltage VPERI" that is "lower than an external voltage VDD" of the memory controller (*e.g.*, Lee's system controller 52), based on Dono, and as I have illustrated in the composite figure below. EX1008, [0004]; *see* EX1004, [0025], FIG. 5. Level shifters are implemented to reduce the voltage (for writing) and to increase the voltage (for reading). Specifically, for "input write data," a "first level shifter 93 is provided to reduce the amplitude of the external signal [from VDD] to VPERI." EX1008, [0040]. For "output read data," a "second level shifter 96 is provided to increase the amplitude VPERI of an internal signal to VDD." *Id.* For instance, the level shifters can be implemented, *e.g.*, in the memory hub of the combination system, to shift the VDD voltage on the high-speed link 58 to the lower VPERI voltage on the DRAM buses 76, 82, 90, 94.

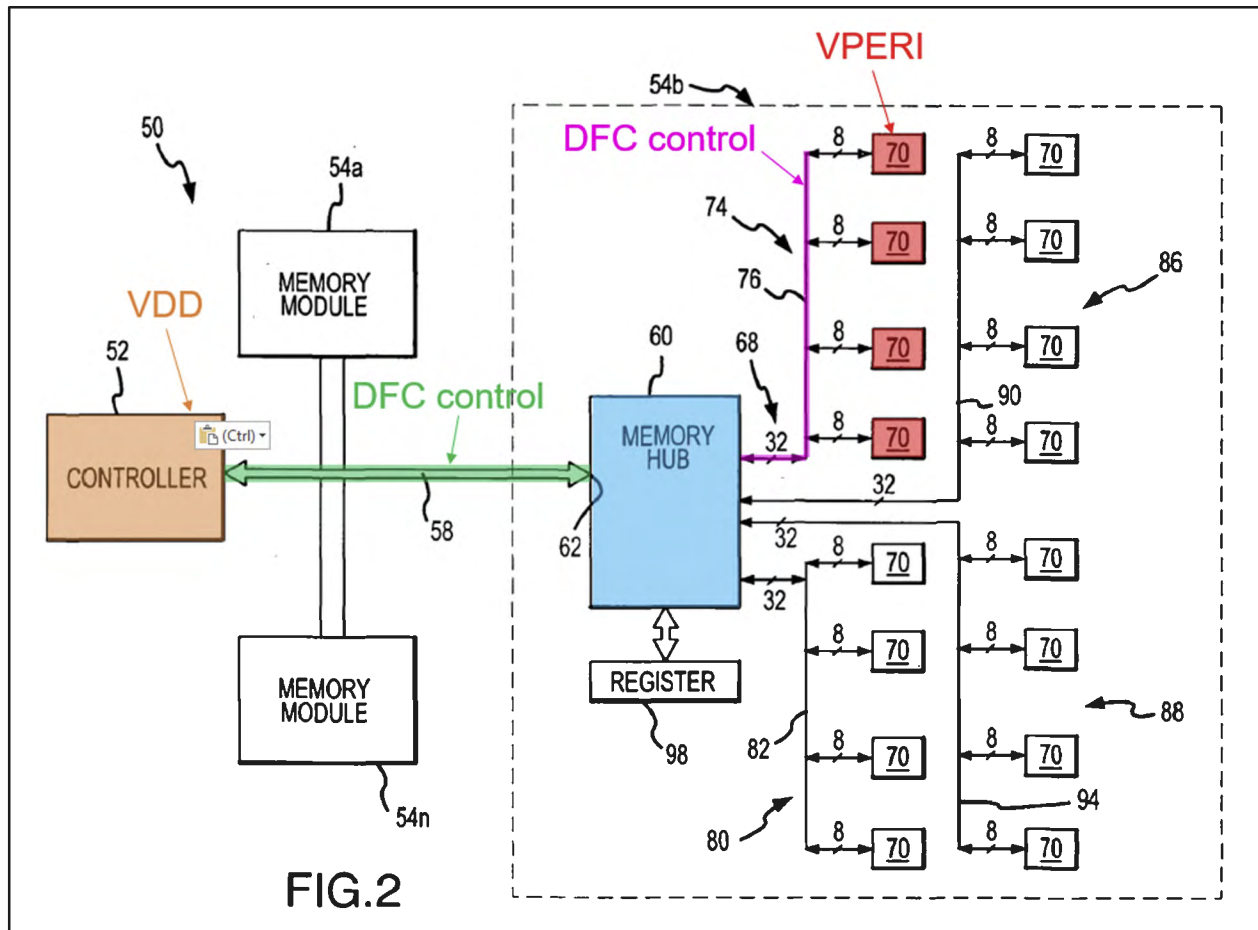


Lee-Chang-Dono-Nakai composite figure based on Lee, FIG. 2

228. Optionally in the combination, dynamic frequency control is implemented based on the teachings of Nakai (*e.g.*, in combination with aspects of Nakai's dynamic voltage control) to reduce power consumption. Specifically, dynamic frequency control is implemented on "all other circuit blocks" besides "[p]eripheral circuit blocks that communicate with external devices," as taught by Nakai. Based on this teaching, in the context of the Lee-Chang-Dono-Nakai combination, dynamic frequency control is implemented on, *e.g.*, the high-speed

link 58 and the memory module bus systems 76, 82, 90, 94, as illustrate below.

This is because these transmission buses, and the memory modules, are not peripheral circuit blocks communicating with external devices, and thus are eligible for Nakai's dynamic frequency control. For instance, a "DFC block," *e.g.*, implemented in the controller 52, controls the clock frequency ... autonomously in hardware" based on system activity, and adjusts the clock frequency on the high-speed link and memory module bus systems as appropriate. EX1017, 4; *see* 5, Figs. 8-9. In addition, the system may be configured such that "[t]he clock frequency may also be set directly via software to allow abrupt performance change in response to external events." EX1017, 5.



Lee-Chang-Dono-Nakai composite figure based on Lee, FIG. 2

4. Motivation to Combine and Expectation of Success

Motivation to implement lower voltage in the DRAM cells than in the memory controller

229. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement the Lee-Chang-Dono-Nakai system such that the DRAM memory devices operate at a different (lower) voltage than that of the memory controller.

230. First, a POSITA would have been motivated to pursue this implementation because logic cells (e.g., in the memory controller) operating at

high voltage allows for higher power operation and faster performance; while the lower bit line voltage in the memory cells (*e.g.*, in the DRAM devices) enables better stability. This is described by Kitsukawa, which states that the “internal voltage level” of the DRAM “must be relatively low to work with the small memory cell circuits of the DRAM’s array ... as well as to reduce the overall power consumption of the DRAM. Output circuits 5, however, work off the higher VDD voltage. In this way, the speed of the output circuits 5 is enhanced.”

EX1022, 1:45-52; *see* 1:26-32 (describing that “reducing the external power supply ... [is] typically at the cost of reduced chip speed”), 2:3-20 (describing that a “DRAM memory cell requires a very small internal voltage that balances dielectric leakage characteristics and memory cell stability, while circuits in an area peripheral to the memory cell area require another internal voltage that balances speed and power consumption”).

231. Second, a POSITA would have been motivated to operate the DRAM at lower voltage than the controller because DRAM operating at different voltage than logic transistors (*e.g.*, with bit line voltages lower than the voltage of the logic cells) was conventional. Indeed, Dono itself describes this, explaining that in the “Related Art,” “an internal operation voltage VPERI [] is lower than an external voltage VDD.” EX1008, [0004]; *see* [0005]; *see also* Kitsukawa’s discussion at EX1022, 1:45-49.

232. Third, operating the DRAM cells at a lower voltage than the controller is merely the application of known techniques (*e.g.*, DRAM operating at a different voltage than a memory controller) by a known system (*e.g.*, the memory system based on Lee), and it yields predictable results (*e.g.*, a memory system in which the DRAM cells operate at a different voltage than the memory controller).

233. A POSITA would have had a reasonable expectation of success in pursuing this implementation because memory system technology is predictable, and because operating DRAM cells at a lower voltage than a memory controller was conventional. *See* EX1008, [0004]-[0005]; EX1022, 1:45-49. Moreover, a POSITA would have had a reasonable expectation of success because Dono's disclosure of the voltage relationship between DRAM and memory controller is in the context of a memory system, *e.g.*, relevant to the architecture of Lee's system.

Motivation to implement dynamic frequency control

234. It is my opinion that there are a number of reasons that would have motivated a POSITA to implement dynamic frequency control in the combination memory system, based on the teachings of Nakai.

235. First, a POSITA would have been motivated to implement dynamic frequency control based on Nakai because dynamic frequency control offers the ability to achieve a reduction in power consumption. *See* EX1017, 2 ("our DVFM scheme is highly effective in realizing ultra-low power consumption").

236. Second, a POSITA would have been prompted to implement dynamic frequency control because doing so is merely the application of known techniques (e.g., frequency management in the context of a DRAM memory system) to a known structure (e.g., a memory system including DRAM memory chips and memory hub), and it yields predictable results (e.g., a memory system in which clock frequency is dynamically controlled to reduce power consumption).

237. A POSITA would have had a reasonable expectation of success because memory system technology is predictable, and because Nakai's disclosure of dynamic frequency control is in the context of a DRAM-based memory system, e.g., relevant to the architecture of Lee's system.

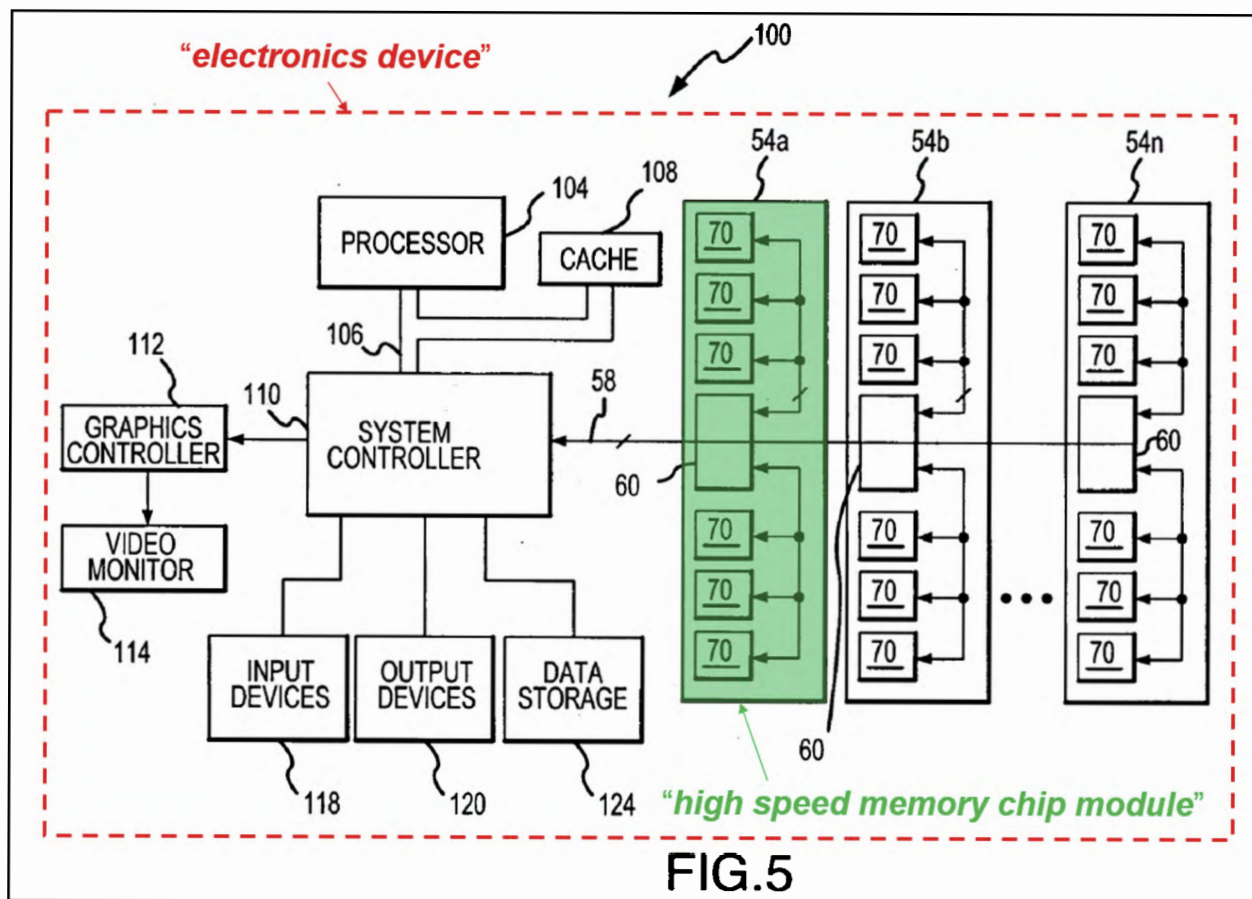
5. Analysis of claims

238. For the reasons below, claims 21 and 23 are obvious over Lee, Chang, Dono, and Nakai.

(a) *Claim 21*

[21pre] An electronics device with a reconfigurable high speed memory chip module, the electronics system device comprising:

239. In the Lee-Chang-Dono-Nakai combination, Lee's "computer system 100" corresponds to the claimed *electronics system device*, as illustrated in FIG. 5, which I have reproduced and annotated below. EX1004, [0023]; see claim 28.



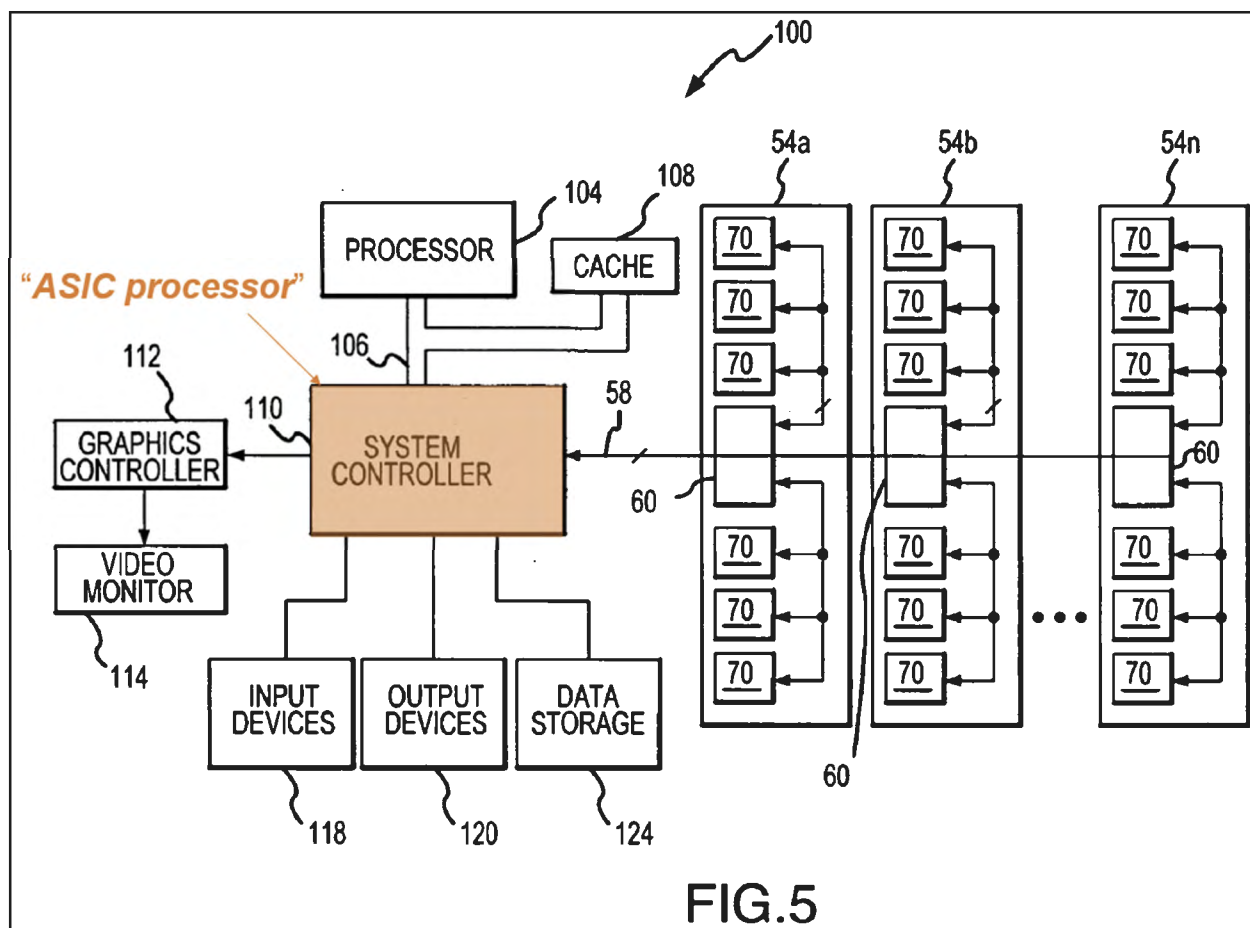
Excerpt from Lee, FIG. 5 (annotated)

240. This computer system includes a “memory system 50” that is illustrated in more detail in FIG. 2. The memory system “includes a controller 52 coupled to several memory modules 54a, b ... n through a high-speed link 58,” where each memory module includes “memory devices 70,” such as “dynamic random access memory devices (‘DRAMs’).” *Id.*, [0015]-[0016], [0023]; *see* Abstract (“A computer system includes a controller coupled to a plurality of memory modules”), [0014] (“FIG. 5 is a block diagram of a computer system using the memory system of FIG. 2”), FIG. 2. Each of the memory modules 54 of the

memory system (e.g., memory module 54a, which I have highlighted above in green) corresponds to a *reconfigurable high speed memory chip module*, as I discussed above for claim element [1pre].

[21a] an application-specific integrated circuit (ASIC) processor;

241. Lee's computer system includes "a system controller 110, which is also sometimes referred to as a 'North Bridge' or 'memory controller.'" EX1004, [0023]. I have highlighted the controller orange in FIG. 5, reproduced below. A POSITA would have understood Lee's North Bridge controller to be an *ASIC processor*, given that this is how North Bridge controllers are typically implemented. For instance, Reeves explains that "Northbridge 14 is generally considered an application specific chip set, or application specific integrated circuit (ASIC) that provides connectivity to various buses, and integrates other system functions such as memory interface." EX1010, 5:30-33. Similarly, Bruno indicates that a North Bridge is an example of an ASIC: "an ASIC die having data routing functionality, such as a north bridge." EX1011, [0032].



Excerpt from Lee, FIG. 5 (annotated)

242. Alternatively or additionally, a POSITA would have found it obvious to implement Lee's North Bridge system controller 110 as an *ASIC processor*, for a number of reasons.

243. First, ASICs provide performance advantages that would have driven a POSITA to use an ASIC for implementation of Lee's North Bridge controller. ASIC chips are custom-built to perform a specific task. This is described by Reiger, which explains that "[c]ompared with standard circuits an ASIC is designed and manufactured according to specifications resulting from its

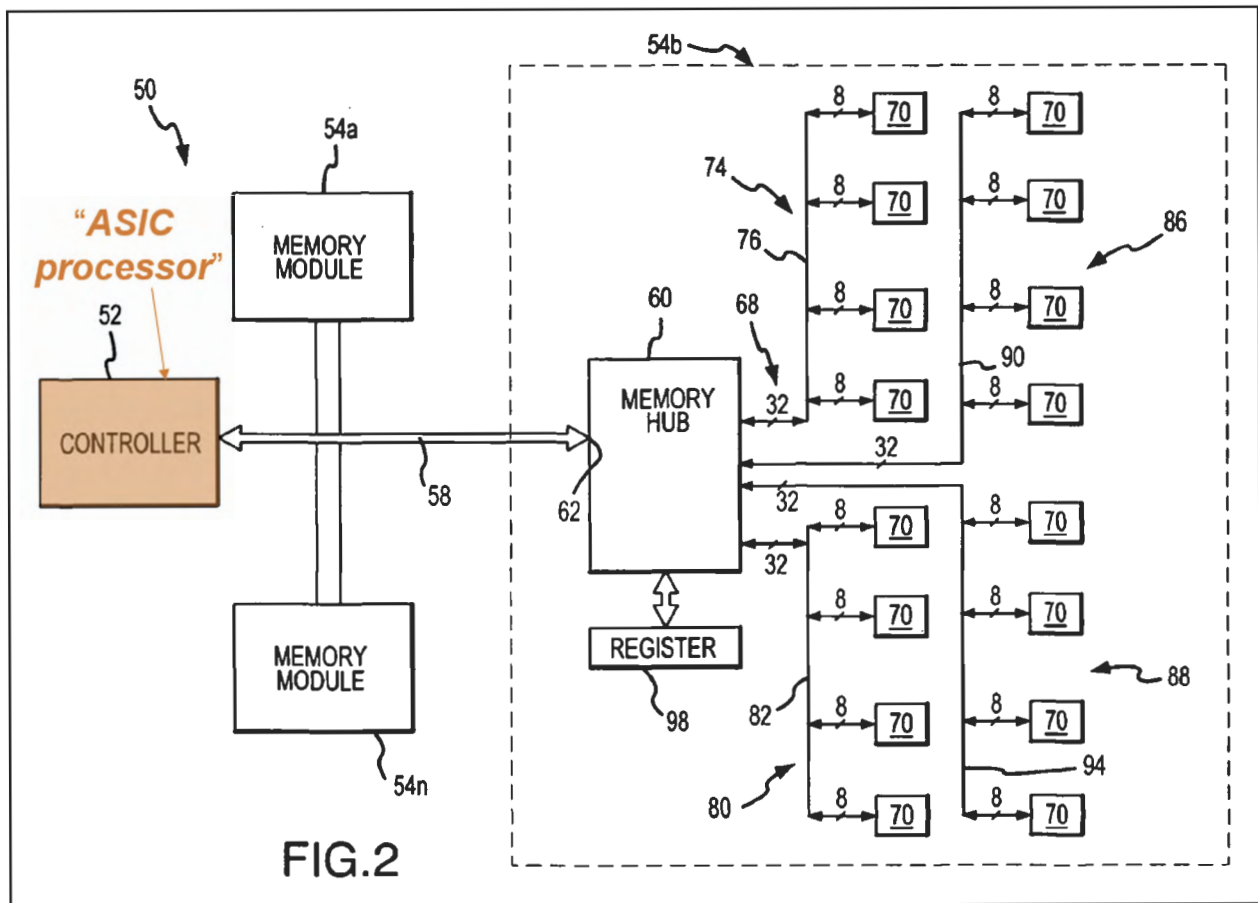
application.” EX1031, 384. As a result of this targeted design, they are capable of high-speed, low-energy operation. In addition, they are compact and inexpensive. *See* EX1031, 385 (listing advantages of ASICs, including “cost effective solution, low design effort with respect to time and cost; high performance, i.e., functionality, speed; low power dissipation; small volume and weight; high reliability; low cost for mounting and test”).

244. Second, there is a finite number of ways to implement a North Bridge controller: *e.g.*, as an ASIC or as a general-purpose chip. The results of the implementation of the North Bridge controller as an ASIC would have been predictable, and this implementation would likely have been successful given that predictability.

245. Third, the implementation of Lee’s North Bridge controller as an ASIC is merely an application of known techniques (specifically, an ASIC memory controller) to a known system (Lee’s memory system), and it yields predictable results (that is, a memory system in which the controller is an ASIC).

246. A POSITA would have expected success in implementing Lee’s North Bridge system controller as an ASIC processor because, as I noted above, it was conventional to implement North Bridge controllers as ASICs, *e.g.*, as indicated by Reeves and Bruno. *See* EX1010, 5:30-33; EX1011, [0032].

247. As I mentioned earlier, Lee's FIG. 5, which illustrates the North Bridge ASIC processor, "is a block diagram of a computer system using the memory system of FIG. 2." EX1004, [0014]; *see* [0023] ("A computer system 100 using the memory system 50 shown in FIG. 2 is shown in FIG. 5"). FIG. 2, reproduced below, provides additional detail of this memory system, which "includes a controller 52 coupled to several memory modules 54*a*, *b* ... *n* through a high-speed link 58." EX1004, [0015]. It is my opinion that the controller 52 of Lee's FIG. 2 (highlighted in orange) is also a North Bridge controller, consistent with the North Bridge controller 110 of Lee's FIG. 5. That is, the controller 52 of FIG. 2 is *an ASIC processor*. This is because Lee explicitly indicates the correspondence between FIG. 2 and FIG. 5 systems (*i.e.*, that the memory system of FIG. 2 is used in the computer system of FIG. 5). This is also because of the evident similarity in structure between the two figures: the controller 110 of FIG. 5 is connected to the memory hub 60 of the memory module 54*a* via the high-speed link 58, just like the controller 52 is connected to the memory hub 60 via the high-speed link 58 in FIG. 2. *See* EX1004, [0015]. Alternatively/additionally, it is my opinion a POSITA would have found it obvious to implement Lee's FIG. 2 controller 52 as an ASIC processor given Lee's teachings of the same in the similarly structured FIG. 5 system, and given the advantages of ASIC processors I previously discussed.



Excerpt from Lee, FIG. 2 (annotated)

[21b] a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs;

248. This limitation is rendered obvious by the Lee-Chang-Dono-Nakai combination for reasons similar to those I discussed above for element [1a] of Ground 1A.

[21c] a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing corresponding to firmware

or software comprised in the ASIC processor;

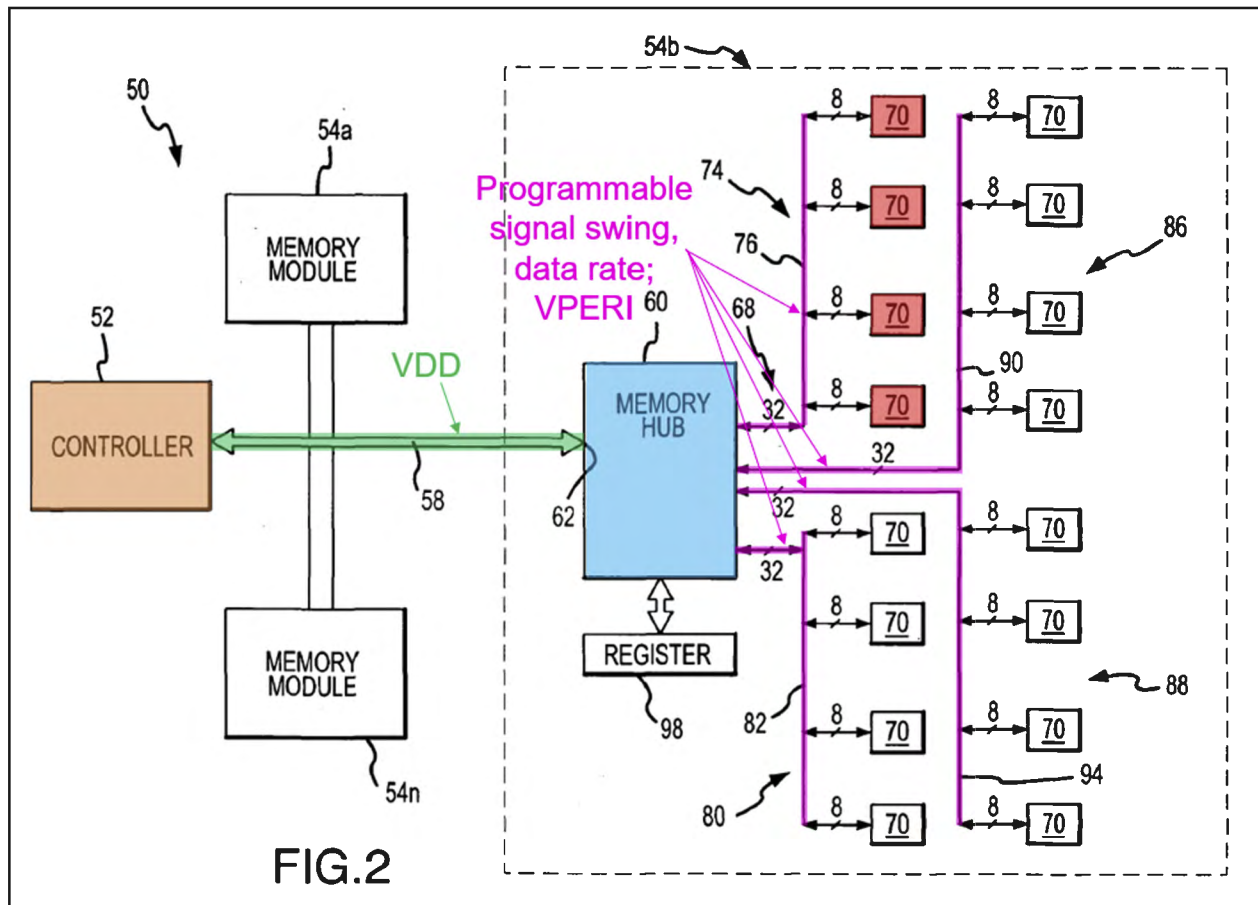
249. The Lee-Chang-Dono-Nakai combination renders obvious a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing for reasons similar to those I discussed above for element [1b] of Ground 1A.

Programmable signal swing on the first transmission bus

250. As I discussed in [1b] of Ground 1A, above, the signal swing on the first transmission bus (*e.g.*, bus system 68, pink in the composite figure below; or an individual bus system 76) is programmable. Based on Dono, the programmable signal swing *corresponds to firmware/software in the ASIC processor*, as I will discuss in the following paragraphs.

Programmable signal swing on the first transmission bus

251. As I discussed in [1b] of Ground 1A, above, the signal swing on the first transmission bus (*e.g.*, bus system 68, pink in the composite figure below; or an individual bus system 76) is programmable. Based on Dono, the programmable signal swing *corresponds to firmware/software in the ASIC processor*, as I will discuss in the following paragraphs.



Lee-Chang-Dono-Nakai composite figure based on Lee, FIG. 2

252. In particular, based on Dono, and as was conventional, the combination system is implemented such that the “internal operation voltage” (*e.g.*, VPERI) of the DRAM memory devices 70 (red) is “lower than an external voltage” (*e.g.*, VDD) of the memory controller 52 (orange). EX1008, [0004]; *see* [0005], [0009], [0040], [0076]. This is implemented through level-shifting the voltage from VDD to VPERI (for write operations), or from VPERI to VDD (for read operations). Specifically, “[a] signal output from the semiconductor device to an external device,” *e.g.*, from a memory device 70 to the memory controller 52,

“is level-shifted from the internal operation voltage VPERI to the external voltage VDD before being output.” EX1008, [0004], [0040]. This is performed by a “level shifter” that “increases the amplitude VPERI of an internal signal to VDD.” For instance, the level shifter can be implemented in the memory hub 60, to shift the voltage from VPERI (the voltage of signals carried on the bus systems 76, 82, 90, 94) to VDD (the voltage of signals carried on the high-speed link 58). The same is also true in reverse: an incoming signal with data to be written to memory is level-shifted by a level shifter (*e.g.*, implemented in the memory hub) from the external voltage VDD (the voltage of signals carried on the high-speed link 58) to the internal DRAM operation voltage VPERI (the voltage of signals carried on the bus systems 76, 82, 90, 94). *Id.* That is, a signal that is outbound from the memory controller 52 along the high-speed bus 58 to the combination memory hub 60 is at the external voltage VDD, where it is level-shifted to the internal DRAM operation voltage VPERI for transmission along the bus systems 76, 82, 90, 94 to the DRAM memory devices. *Id.*

253. The voltage VPERI is the voltage of the signal transmitted along the bus systems 76, 82, 90, 94 (corresponding individually or collectively to the claimed ***first transmission bus***). The external voltage VDD is the voltage at which the memory controller (corresponding to the claimed ***ASIC processor***) operates, *i.e.*, the voltage at which firmware and/or software executed by the ASIC

operates. The voltage VPERI on the first transmission bus *corresponds to* the external voltage VDD of the ASIC (and the voltage at which the ASIC firmware/software operates) because the voltage VDD is “level-shifted” by a specified amount to be converted into VPERI, *i.e.*, and amount that is defined by the difference between the DRAM cell voltage VPERI and the memory controller voltage VDD. *See* EX1008, [0040].

254. The signal swing of the signal on the first transmission bus (*e.g.*, the voltage difference between logic levels of transmitted data) depends on the voltage VPERI of the signal transmitted along the first transmission bus. This is because the signal swing on a transmission bus relates to the voltage values for logical “1” and “0” signals. These two voltage values are determined, in part, based on the baseline voltage VPERI of the signals transmitted on that bus. Thus, because the voltage VPERI of the signal transmitted along the first transmission bus corresponds to the external voltage VDD at which the memory controller (*ASIC processor*) operates (and thus to firmware and/or software of the ASIC processor), the signal swing of the first transmission bus likewise *corresponds to firmware and/or software of the ASIC processor*.

255. Overall, in the Lee-Chang-Dono-Nakai combination, the signal swing thus is programmable, *e.g.*, based on Chang’s teachings of the signal swing’s dependence on an adjustable voltage (*see* EX1006, [0045]), and corresponds to

ASIC firmware/software because the DRAM voltage is level-shifted relative to the voltage at which the ASIC firmware/software operates.

Programmable data rate on the first transmission bus

256. As I discussed in element [1b] of Ground 1A, above, the data rate on the first transmission bus is programmable based on the teachings of Lee and/or based on the teachings of Chang.

257. To the extent the claims are interpreted to require that the programmable data rate *corresponds to firmware/software in the ASIC processor*, this is further rendered obvious in the combination based on the teachings of Nakai, as I discuss in the following paragraphs.

258. Based on Nakai, “all ... circuit blocks” other than “[p]eripheral circuit blocks that communicate with external devices” are “driven by the dynamically controlled system clock.” EX1017, 2. In the combination system, circuit blocks that are subject to dynamic frequency control include the bus system 68 (*first transmission bus*) and the high-speed link 58 (*second transmission bus*), because these circuit elements are not peripheral circuit blocks and are not circuit blocks that communicate with external devices.

259. In one implementation of the combination, “[t]he clock frequency” of the first and second transmission buses is “set directly via software” to allow abrupt performance change in response to external events.” EX1017. The clock

frequency corresponds to the claimed ***data rate*** because the clock frequency controls how quickly events occur, *e.g.*, how quickly data is transferred. Because the clock frequency (***data rate***) is set via software, it is ***programmable***. This means that the ***first transmission bus has a programmable transmitting/receiving data rate***. EX1017, 5. The programmable data rate ***corresponds to firmware/software in the ASIC processor*** because it is “set ... via software,” *e.g.*, software implemented in the memory controller (***ASIC processor***). EX1017, 5.

260. Alternatively or additionally, “the DFC block controls the clock frequency” of the first and second transmission buses “autonomously” based on “activity data,” *e.g.*, such that “the clock frequency of the next monitoring period is increased” or “decreased” as appropriated based a calculated “optimum clock frequency.” EX1017, 4-5; *see* Figs. 8-9. Autonomous optimization of clock frequency (***data rate***) on the first and second transmission buses corresponds to the ***first transmission bus having a programmable transmitting/receiving data rate***.

The programmable data rate ***corresponds to firmware in the ASIC processor*** because it is controlled ... “autonomously in hardware” by the DFC, which is implemented in the memory controller (***ASIC processor***). EX1017, 4.

[21d] a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus; and

261. *See* [1d] of Ground 1A, *supra*.

[21e] a second transmission bus coupled between the logic unit and the ASIC processor having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing associated to the firmware or the software comprised in the ASIC processor.

262. The Lee-Chang-Dono-Nakai combination renders obvious a second transmission bus having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing. See [1c] of Ground 1A, *supra*.

Programmable signal swing on the second transmission bus

263. The high-speed bus (corresponding to the claimed *second transmission bus*, green in Lee's FIG. 2, below) is *coupled between the logic unit* (corresponding to the claimed memory hub, blue) *and the ASIC processor* (corresponding to the claimed memory controller, orange), as I discussed above for elements [1c]-[1d] of Ground 1A; EX1004, [0015], [0025], FIG. 2, FIG. 5.

264. As I discussed in [1c] of Ground 1A, above, the signal swing on the second transmission bus (*e.g.*, high speed link 58, green in the composite figure *infra*) is programmable. Based on Dono, the programmable signal swing *corresponds to firmware/software in the ASIC processor*, as I will discuss in the following paragraphs.

267. The signal swing of the second transmission bus (*e.g.*, the voltage difference between logic levels of transmitted data) depends on the voltage VDD of the signal transmitted along the second transmission bus. This is because the signal swing on a transmission bus relates to the voltage values for logical “1” and “0” signals. These two voltage values are determined, in part, based on the baseline voltage VPERI of the signals transmitted on that bus. Thus, because the voltage VDD of the signal transmitted along the second transmission bus is associated to the external voltage VDD at which the memory controller (*ASIC processor*) operates (and thus to firmware and/or software of the ASIC processor), the signal swing of the second transmission bus likewise *is associated to firmware and/or software of the ASIC processor*.

Programmable data rate on the first transmission bus

268. As discussed in [1c] of Ground 1A, *supra*, the data rate on the second transmission bus is programmable.

269. To the extent the claims are interpreted to require that the programmable data rate *corresponds to firmware/software in the ASIC processor*, this is rendered obvious in the combination based on the teachings of Nakai, as discussed in the following paragraphs.

270. First, “[t]he clock frequency” (*data rate*) of the second transmission bus is “set directly via software” (*programmable*), as I discussed above for [21c],

i.e., the second transmission bus has a programmable transmitting/receiving data rate corresponding to firmware/software in the ASIC processor]. EX1017, 5.

271. Alternatively/additionally, autonomous optimization of clock frequency (*data rate*) on the second transmission bus corresponds to the *second transmission bus having a programmable transmitting/receiving data rate*, and the programmable data rate *corresponds to firmware in the ASIC processor* because it is controlled ... “autonomously in hardware,” as I discussed above for [21c]. EX1017, 4.

(b) **Claim 23**

[23] The electronic device of claim 21, wherein the programmability of the first transmission bus and the second transmission bus are associated with an OTP, an MTP, a Flash Memory, an embedded memory, an anti-fuse memory, a register, the firmware or the software.

272. Claim 23 is rendered obvious by the combination of Lee, Chang, Dono, and Nakai for reasons similar to those I discussed above for claim [4] of Ground 1A.

VII. LEGAL PRINCIPLES

A. Obviousness

273. I have been informed that a patent claim is invalid as “obvious” under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a POSITA, taking into account (1) the scope and content of the prior art,

(2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others. For purposes of my analysis above and because I know of no indication from the patent owner or others to the contrary, I have applied a date of August 13, 2015, as the date of invention in my obviousness analyses, although in many cases the same analysis would hold true even at an earlier time than August 13, 2015.

274. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason to modify the single prior art reference, or combine two or more references, in order to achieve the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or “common sense” of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more

than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

275. I have also been informed of the Supreme Court decision *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), which I am informed guides obviousness analyses. Under *KSR*, the mere application of a known technique to a piece of prior art ready for the improvement is obvious. In addition, the selection of one of a finite number of identified, predictable solutions to achieve a predictable result is obvious. Further, the simple substitution of one known element for another to obtain a predictable result is obvious.

APPENDIX A

DAVID KUAN-YU LIU, Ph.D.

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davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 18 years of experience serving as expert consultant.
 - Named inventor on 99 US patents.
- Consultant and expert witness for past 18 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

EXPERT WITNESS WORK - CASE EXPERIENCE:

Case: **Advanced Memory Technologies, Inc. v. Micron Technology, Inc.**
Jurisdiction: Civil Action No. 1:25-cv-01036 (W.D. Tex.)
Work Product: Expert consulting work relating to Booster Circuit. Patent analysis and prior art review toward preparation of EPR petition support and draft of declaration.
Nature of Case: EPR.
Counsel: Retained by Fish & Richardson (Contact: Tim Riffe)
Date: 11/25 – Present

Case: **Apple v. WeCrevention, Inc.**
Jurisdiction: Post-Grant Patent Matters Adverse to WeCrevention, Inc.
Work Product: Expert consulting work relating to High Speed Chip Memory Module. Patent analysis and prior art review toward preparation of IPR petition support and draft of declaration.
Nature of Case: IPR.
Counsel: Retained by Fish & Richardson (Contact: Dr. Hyun Jin In)
Date: 11/25 – Present

Case: **Monterey Research LLC v. Renesas Electronics Corp.**
Jurisdiction: Civil Action No. 2:24-cv-00238-JRG (E.D. Tex.)
Work Product: Expert consulting work relating to Charge Trapping Nonvolatile Memory. Patent analysis and prior art review toward preparation of IPR petition support and draft of declaration.
Nature of Case: Civil action and IPR.
Counsel: Retained by Morrison Foerster (Contact: Yuka Teraguchi)
Date: 03/25 – Present

Case: **Palisade Techs., LLP v. Micron Tech., Inc.**
Jurisdiction: Civil Action N.D. Cal, No. 7:24-cv-00262 (W.D. Tex.)
Work Product: Expert consulting work relating to 3D NAND Flash Memory Technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 2 patents.
Nature of Case: Civil action and IPR.
Counsel: Retained by O'Melveny & Myers LLP (Contact: John Kappos)
Date: 12/24 – 01/26

Case: **Yangtze Memory Technologies Company, Ltd. vs. Micron Technology, Inc.**
Jurisdiction: Civil Action N.D. Cal, No. 3:223-cv-05792-RFL
Easter District of Texas
Work Product: Expert consulting work relating to 3D NAND Flash Memory Technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents. ***Deposed on 3 petitions that have been instituted.***
Nature of Case: Civil action and IPR.
Counsel: Retained by Orrick, Herrington & Sutcliffe (Contact: Jason Lang)
Date: 03/24 – Present

Case: **Force MOS Technology Co., Ltd. vs. Inergy Technology, Inc.**
Jurisdiction: Civil Action E.D. TX, No. 2:22-cv-00460-JRG
Easter District of Texas
Work Product: Expert consulting work relating to Vertical Trench DMOS process technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 2 patents. Declaration for claim construction on 3 patents. ***Deposed on Claim Construction Declaration, and deposed on declarations for IPR petitions, and deposed on reply declaration.*** Continuing work on claim construction and technical consulting.
Nature of Case: Civil action and IPR.
Counsel: Retained by Baker McKenzie (Contact: McKenzie Martin)
Date: 10/23 – 10/25

Case: **GlobalFoundries U.S. vs. International Business Machines**
Jurisdiction: 03348-KMK-AEK (S.D.N.Y. 2023)
Work Product: Expert consulting work relating to trade secrets involving advanced CMOS process and device technology (Nanosheet technology). Reviewed evidence and summarized findings.
Nature of Case: Civil action.
Counsel: Retained by Latham & Watkins (Contact: Sami Al-Marzoog)
Date: 10/23 – 2/25

Case: **Element Capital. vs. Beijing BOE Display Technology Co., Ltd.**
Jurisdiction: Civil Action No. 2:22-cv-00118-JRG
Eastern District of Texas
Work Product: Expert consulting work relating to OLED technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 3 patents.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Linhong Zhang)
Date: 4/23 – 12/23

Case: **Sonrai Memory Ltd. vs. Micron Technology, Inc.,**
Jurisdiction: Civil Action No. 6:22-cv-000855-FB
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration resulting in institution of
the petition and ***deposed on supplemental declaration.***
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Tim Riffe)
Date: 12/22 – 7/24

Case: **Daedalus Prime LLC vs. Samsung Electronics Co.,**
Jurisdiction: Civil Action E.D. TX, Marshall Div., No. 2:22-cv-353
Eastern District of Texas, Marshall Div., and
Investigation No. 337-TA-1336
Work Product: Expert consulting work relating to FINFET process technology.
Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration on 2 patents. Source code
database viewing (GDS layout and process flow documents) for
supporting of non-infringement position.
Nature of Case: Civil action and ITC Investigation on Certain Semiconductor Devices,
Mobile Devices Containing the Same and Components Thereof..
Counsel: Retained by Fish & Richardson (Contact: Kevin Su)
Date: 10/22 – 4/23

Case: **Netlist, Inc. vs. Samsung Electronics Co. Ltd. et al.,**
Jurisdiction: Civil Action No. 2:21-cv-00463
Eastern District of Texas
Work Product: Expert consulting work relating to memory modules.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Tony Nguyen)
Date: 8/22 – 12/22

Case: **Vervain, LLC vs. Micron Technology & related IPR Petition**
Jurisdiction: Action No. 6:21-cv-00487-ADA
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration on 4 patents, all 4 petitions
instituted, and ***deposed on both initial declaration and reply
declaration on all 4 patents.***
Counsel: Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared
Bobrow)
Date: 8/21 – 2/23

Case: **Monterey Research vs. Qualcomm PTAB Matter**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Jones Day (Contact: David Cochran)
Date: 12/21 – 2/22

Case: **Semiconductor Energy Laboratory Co., OLED Patent Matters**
Jurisdiction: Action No. 8:21-cv-00554-JAK-ADS
Central District of California
Work Product: Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Bryan Basso)
Date: 9/21 – 4/22

Case: **Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Erise IP (Contact: Paul Hart)
Date: 8/21 – 9/21

Case: **Texas Instruments IPR Petition**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Josh Griswold)
Date: 9/20 – 4/21

Case: **Micron Technology vs. UMC/JinHua**
Jurisdiction: Case No. 4:17-CV-06932-MMC
United States District Court for the Northern District of California
Work Product: Testifying expert, trade secret documents review, and declaration submission.
Nature of Case: Trade secret contention of Micron confidential documents.
Counsel: Retained by Jones Day (Contact: Randy Kay)
Date: 3/17 – 12/23

Case: **SK Hynix vs. BitMicro**
Jurisdiction: Investigation No. 337-TA-1097
United States International Trade Commission
Work Product: Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, **deposition taken**, issued witness statement.
Nature of Case: ITC infringement case concerning module stacking of SDRAM.
Counsel: Retained by Fish Richardson (Contact: Joseph Colaianni)
Date: 11/18 – 4/19

Case: ***Rohm Company IPR Petition***

Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.

Counsel: Retained by Fish & Richardson (Contact: Matt Colvin)

Date: 4/18 – 8/18

Case: ***Apple Inc., vs. Qualcomm Incorporated***

Jurisdiction: Case No. 3:17-CV-02402

United States District Court for the Southern District of California

Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, ***2 depositions taken.***

Counsel: Fish & Richardson (Contact: Tony Nguyen)

Date: 1/18 – 5/19

Case: ***Macronix vs. Toshiba***

Jurisdiction: Investigation No. 337-TA-1046

United States International Trade Commission

Work Product: Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, ***deposition taken for 2 patents***, issued witness statement and rebuttal witness statement, ***testified in ITC court on both infringement and invalidity.***

Nature of Case: ITC infringement case concerning advanced NAND Flash memory.

Counsel: Retained by Fish Richardson (Contact: David Barken)

Date: 4/17 – 10/18

Case: ***Novatek Microelectronics Corp. IPR Petition***

Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.

Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)

Date: 2/17 – 4/17

Case: ***Taiwan Semiconductor Manufacturing Company IPR Petition***

Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.

Counsel: Retained by Fish & Richardson (Contact: John Goetz)

Date: 7/15 – 4/17

Case: **Triune Systems, LLC vs. Wayne Chen, et al.,**
Jurisdiction: Case No. 296-03209-2013,
District Court of Collin County, TX
Work Product: Testifying expert, database viewing, expert report, *video-taped testimony*
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: **Macronix vs. Spansion**
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: **Macronix vs. Spansion**
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: **Keranos, LLC v. Analog Devices et. al.**
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: **Silicon Storage Technology, Inc. v. Xicor, LLC**
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Testifying expert: issuing expert report, declarations, and
deposition taken.
Nature of Case: Patent infringement case concerning minimizing source current
during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

PROFESSIONAL EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 12 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35 μ m and 0.18 μ m CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00

Programmable Silicon Solutions, Sunnyvale, California

Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98

AMIC Technology, Santa Clara, California

Director of Flash Technology. Responsible for developing 0.35 μ m ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97

Altera Corp., San Jose, California

Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35 μ m generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96

Information Storage Devices, San Jose, California

Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95

Advanced Micro Devices, Sunnyvale, California

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5 μ m and 0.35 μ m flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K.-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.
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10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.
11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.
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14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.
15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.

16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.
17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.
18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.
19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.
20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.
21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.
22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.
23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.
24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.
25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997
26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.
27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.
28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.
29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998
30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.
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32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.

33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.
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35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.
36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.
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46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.
47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.
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50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.

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72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010
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74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010
75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011
76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011
77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011
78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012
79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012
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81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012
82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.

83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.
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85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.
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87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.
88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.
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91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.
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94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
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96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.
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98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.
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3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
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7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
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