

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Ken et al.
U.S. Patent No.: 9,201,834 Attorney Docket No.: 50095-0276IP1
Issue Date: December 1, 2015
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Filing Date: November 2, 2012
Title: RECONFIGURABLE HIGH SPEED MEMORY CHIP MODULE
AND ELECTRONIC DEVICE WITH A RECONFIGURABLE
HIGH SPEED MEMORY CHIP MODULE

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PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 9,201,834
PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

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LIST OF EXHIBITS

EX1001	U.S. Patent No. 9,201,834 to Ken et al. (“the ’834 Patent”)
EX1002	Excerpts from the Prosecution History of the ’834 Patent
EX1003	Declaration and Curriculum Vitae of Dr. David Liu
EX1004	U.S. Patent App. Pub. No. 2004/0260864 (“Lee”)
EX1005	PCT Pub. No. WO2008/124503 (“Tsern”)
EX1006	U.S. Patent App. Pub. No. 2010/0235554 (“Chang”)
EX1007	U.S. Patent No. 7,785,933 (“Dozen”)
EX1008	U.S. Patent App. Pub. No. 2011/0063927 (“Dono”)
EX1009	“Development of 3D Stack Package Using Silicon Interposer for High-Power Application.” N. Khan <i>et al. IEEE Transactions on Advanced Packaging</i> , Vol. 32, No. 1, February 2008 (“Khan”)
EX1010	U.S. Patent No. 6,226,755 (“Reeves”)
EX1011	U.S. Patent App. Pub. No. 2007/0109831 (“RaghuRam”)
EX1012	RESERVED
EX1013	U.S. Patent Pub. No. 2010/0187671 (“Lin”)
EX1014	U.S. Patent No. 8,344,496 (“White”)
EX1015	U.S. Patent No. 6,869,829 (“Hikita”)
EX1016	U.S. Patent No. 8,502,375 (“Liao”)

- EX1017 “Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor.” M. Nakai et al. IEEE Journal of Solid-State Circuits, Vol. 40, No. 1, January 2005 (“Nakai”)
- EX1018 RESERVED
- EX1019 U.S. Patent No. 6,184,808 (“Nakamura”)
- EX1020 U.S. Patent No. 8,895,345 (“Akiyama”)
- EX1021 U.S. Patent No. 5,848,080A (“Dahm”)
- EX1022 U.S. Patent No. 5,844,853 (“Kitsukawa”)
- EX1023 U.S. Patent Pub. No. 2008/0265378 (“Lee-378”)
- EX1024 U.S. Patent No. 8,803,322 (“Yang”)
- EX1025 U.S. Patent No. 8,405,214 (“Willey”)
- EX1026 Declaration of June Ann Munford
- EX1027-1030 RESERVED
- EX1031 “Application Specific Integrated Circuits (ASICs).” Martin Reiger. *The Electronic Design Automation Handbook*. Jansen, D. ed., 2003 (“Rieger”)
- EX1032 RESERVED
- EX1033 Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2025) | United States Courts (uscourts.gov), available at: [fcms_na_distprofile1231.2025.pdf](https://www.uscourts.gov/fcms_na_distprofile1231.2025.pdf)

LISTING OF CLAIMS

Claim 1	
[1pre]	A reconfigurable high speed memory chip module, comprising
[1a]	a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array integrated circuits (ICs);
[1b]	a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing;
[1c]	a second transmission bus coupled to the logic unit having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing; and
[1d]	a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus, and further used for converting a first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.
Claim 2	
[2a]	The reconfigurable high speed memory chip module of claim 1, wherein the first transmission bus is used for transmitting the first set of parallel data along with the multiple memory cell array ICs, and
[2b]	bus width of the first transmission bus is wider than bus width of an input/output (I/O) data bus of each of the memory cell array ICs.
Claim 4	
[4]	The reconfigurable high speed memory chip module of claim 1, wherein programmability of the first transmission bus or the second transmission bus corresponds to a one-time programming (OTP), a multi-time programming (MTP), a Flash Memory, an embedded memory, an anti-fuse, a register, firmware, or software.

Claim 5	
[5a]	The reconfigurable high speed memory chip module of claim 1, wherein at least one through silicon via (TSV) exists within a non-active circuit region surrounding or partially surrounding an active circuit region of each of the memory cell array ICs, and
[5b]	the active circuit region is used for forming at least one active device of the memory cell array IC.
Claim 6	
[6a]	The reconfigurable high speed memory chip module of claim 1, wherein at least one TSV exists within a non-active circuit region surrounding or partially surrounding an active circuit region of the logic unit, and the active circuit region is used for forming at least one active device of the logic unit,
[6b]	wherein the at least one TSV is used for connecting to a power or a ground supply.
Claim 7	
[7a]	The reconfigurable high speed memory chip module of claim 1, wherein at least one pair of TSVs exist in neighboring within a non-active circuit region surrounding or partially surrounding an active circuit region of each of the memory cell array ICs, and
[7b]	wherein the at least one pair of TSVs are used for connecting to a power or a ground supply.
Claim 8	
[8a]	The reconfigurable high speed memory chip module of claim 1, wherein at least one pair of TSVs exist in neighboring within a non-active circuit region surrounding or partially surrounding an active circuit region of the logic unit, and
[8b]	wherein the at least one pair of TSVs are used for connecting to a power or a ground supply.

Claim 9	
[9]	The reconfigurable high speed memory chip module of claim 1, wherein a dicing method for at least one memory cell array IC of the multiple memory cell array ICs comprises a laser process.
Claim 10	
[10]	The reconfigurable high speed memory chip module of claim 1, wherein a dicing method for the logic unit comprises a laser process.
Claim 12	
[12]	The reconfigurable high speed memory chip module of claim 5, wherein the at least one TSV is used for connecting to a power or a ground supply.
Claim 13	
[13]	The reconfigurable high speed memory chip module of claim 5, wherein the non-active circuit region has a width less than about 50 μm .
Claim 14	
[14]	The reconfigurable high speed memory chip module of claim 5, wherein the at least one TSV has a width less than about 20 μm .
Claim 15	
[15]	The reconfigurable high speed memory chip module of claim 5, wherein a corner of the memory cell array IC has an orientation identification mark wherein the orientation identification mark is formed by a process comprising Laser step.
Claim 16	
[16]	The reconfigurable high speed memory chip module of claim 5, wherein a corner of the memory cell array IC has an orientation identification mark wherein the orientation identification mark comprises at least one of an edge cut, a line of drawing, two lines of drawing, a hole, or an arbitrary pattern.

Claim 18	
[18]	The reconfigurable high speed memory chip module of claim 6, wherein the non-active circuit region has a width less than about 50 um.
Claim 19	
[19]	The reconfigurable high speed memory chip module of claim 6, wherein the at least one TSV has a width less than about 20 um.
Claim 21	
[21pre]	An electronics device with a reconfigurable high speed memory chip module, the electronics system device comprising:
[21a]	an application-specific integrated circuit (ASIC) processor;
[21b]	a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array ICs;
[21c]	a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing corresponding to firmware or software comprised in the ASIC processor;
[21d]	a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus; and
[21e]	a second transmission bus coupled between the logic unit and the ASIC processor having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing associated to the firmware or the software comprised in the ASIC processor.
Claim 23	
[23]	The electronic device of claim 21, wherein the programmability of the first transmission bus and the second transmission bus are associated with an OTP, an MTP, a Flash Memory, an embedded memory, an anti-fuse memory, a register, the firmware or the software.

Apple Inc. (“Petitioner”) petitions for IPR of claims 1-2, 4-10, 12-16, 18-19, 21, and 23 (the “Challenged Claims”) of U.S. Patent No. 9,201,834 (“the ’834 Patent”), assigned to WeCvention, Inc. (“Patent Owner”/“PO”). Compelling evidence presented in this Petition demonstrates at least a reasonable likelihood that Petitioner will prevail with respect to at least one of the Challenged Claims. Accordingly, Petitioner respectfully submits that an IPR should be instituted, and that the Challenged Claims should be canceled as unpatentable.

I. REQUIREMENTS FOR IPR—37 C.F.R. §42.104

A. Grounds for Standing—37 C.F.R. §42.104(a)

Petitioner certifies that the ’834 Patent is available for IPR. Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the below-identified grounds.

B. Challenge and Relief Requested—37 C.F.R. §42.104(b)

Petitioner requests IPR of the Challenged Claims on the below grounds. Dr. David Liu provides supporting explanations in an expert declaration. EX1003, ¶¶1-275.

Asserted Grounds		
Ground	Claims	Basis
1A	1-2, 4	§103: Lee-Chang
1B	1-2, 4	§103: Lee-Chang-Tsern

1C	5, 13-14	§103: Lee-Chang-Tsern-RaghuRam
1D	6-8, 18-19	§103: Lee-Chang-Tsern-White
1E	9	§103: Lee-Chang-Dozen or Lee-Chang-Tsern-Dozen
1F	10	§103: Lee-Chang-Tsern-Dozen
1G	12	§103: Lee-Chang-Tsern-RaghuRam-White
1H	15-16	§103: Lee-Chang-Tsern-RaghuRam-Hikita
1I	21, 23	§103: Lee-Chang-Dono-Nakai

The '834 Patent claims priority from several previously filed applications, the earliest of which was filed on October 11, 2011. Each of the above identified references qualifies as prior art under pre-AIA 35 USC §§102(a), (b), or (e) (as shown in the table below) even if October 11, 2011 ("Critical Date") is used as the priority date of the '834 Patent.¹

Reference	Prior Art Date	Status
Lee	12/23/2004 (published)	§102(b)
Chang	9/16/2010 (published)	§102(b)
Tsern	10/16/2008 (published)	§102(b)
RaghuRam	5/17/2007 (published)	§102(b)
White	4/29/2009 (filed)	§102(e)
Dozen	8/31/2010 (patented)	§102(b)
Hikita	3/22/2005 (patented)	§102(b)
Dono	3/17/2011 (published)	§102(a)

¹ Petitioner does not concede that the claims of the '834 Patent are entitled to this priority date.

Reference	Prior Art Date	Status
Nakai ²	2005 (published)	§102(b)

II. THE '834 PATENT

A. Summary

The '834 Patent relates to a “high speed memory chip module” that includes a “type of memory cell array group and a logic unit.” EX1001, Abstract. The type of memory cell array group includes “multiple memory cell array integrated circuits (ICs),” *e.g.*, a Dynamic Random Access Memory (DRAM) IC. *Id.*, Abstract, 3:44-48. The logic unit is “used for accessing the memory cell array IC[s],” and “convert[s] [a] first set of parallel data” from the memory cell ICs “into a second set of parallel data,” which it “transmits ... to an application-specific integrated circuit (ASIC).” *Id.*, 4:36-52; EX1003, ¶29.

B. Prosecution History

The '834 Patent was subject to a single office action, identifying several dependent claims as directed to allowable subject matter. The reasons for allowance stated that claim 3 was allowable because “the prior arts ... do not teach a second transmission bus coupled to the logic unit having a second programmable

² See generally EX1026.

transmitting or receiving data rate, a second programmable or receiving signal swing; wherein the logic unit is further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.” EX1002, 39-44. To secure grant, applicant incorporated features of allowable claim 3 into the independent claims.

III. LEVEL OF ORDINARY SKILL

The range of qualifications for a POSITA would have included at least a master’s degree in electrical engineering, or a comparable field, and at least two years of professional experience working with DRAM. EX1003, ¶29. Additional years of experience could substitute for an advanced-level degree (and vice versa). *Id.*

IV. CLAIM CONSTRUCTION—37 C.F.R. §42.104(b)(3)

All claim terms should be construed according to their ordinary and customary meaning under the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. Petitioner submits that no claim terms need be construed to resolve issues of controversy in the present Petition, but reserves the right to respond to construction issues raised by Patent Owner.

Wellman, Inc. v. Eastman Chem. Co., 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Petitioner is not conceding that each challenged claim satisfies all

statutory requirements, nor waiving arguments/grounds that cannot be raised in this proceeding.

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A: Claims 1-2 and 4 Are Obvious Over Lee-Chang

The sections below introduce Lee, Chang, and the Lee-Chang combination.³

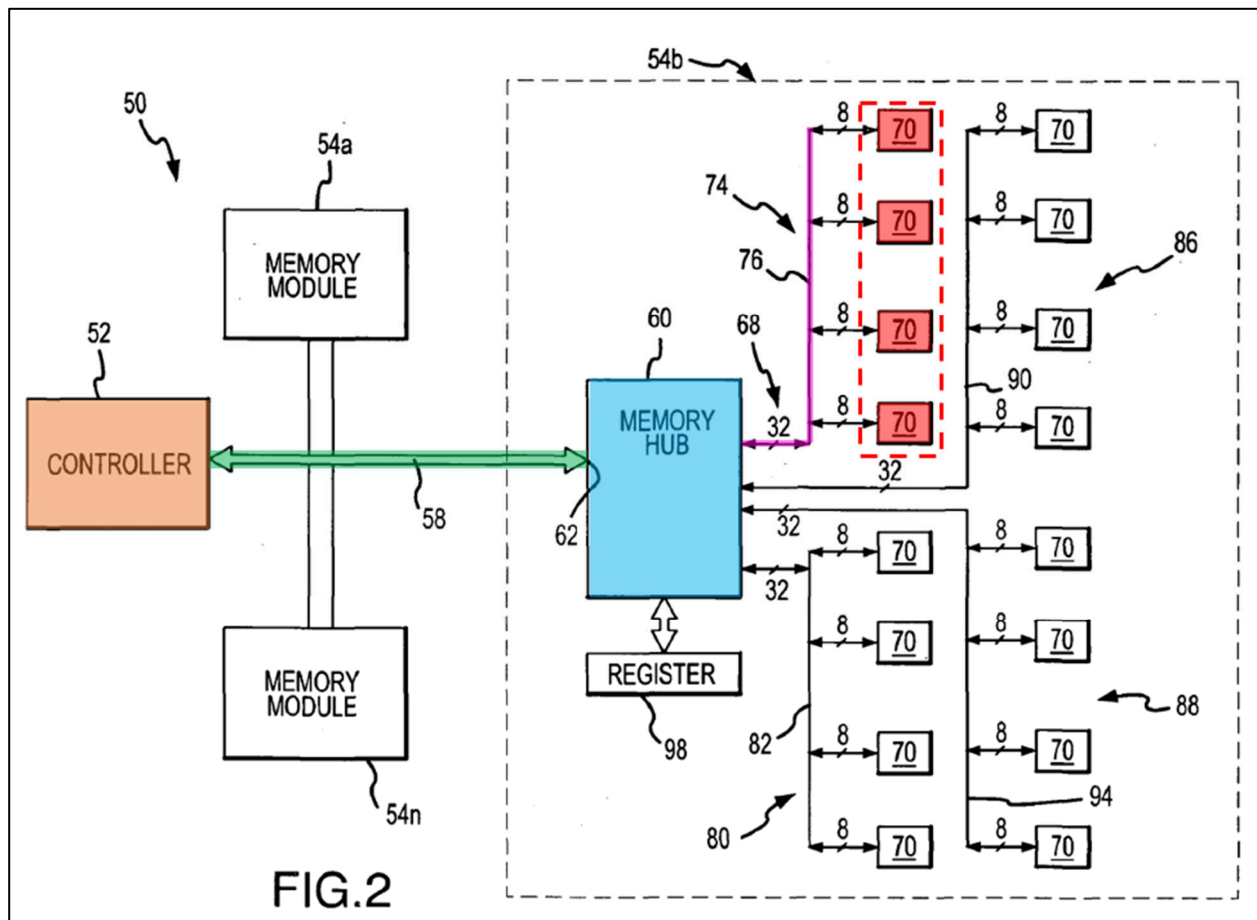
1. Lee

Lee describes a memory system that includes a memory module that is configurable “in a plurality of data formats.” EX1004, [0009].⁴ “When programmed for a high bandwidth, the memory hub simultaneously accesses the memory devices in all of the ranks,” and “[w]hen programmed for a high memory depth, the memory hub accesses the memory devices in only one of the ranks at a time.” *Id.*; EX1003, ¶30

³ This discussion of Lee and Chang is incorporated into Grounds 1A-1I. Similarly, discussion of other references is incorporated into all grounds advancing the same.

⁴ In below addressing invalidity of the Challenged Claims over the teachings of the cited references, Petitioner relies on the teachings of those references as would have been understood by a POSITA, without necessarily relying upon incorporation of each or any of the disclosed or referenced exemplary details.

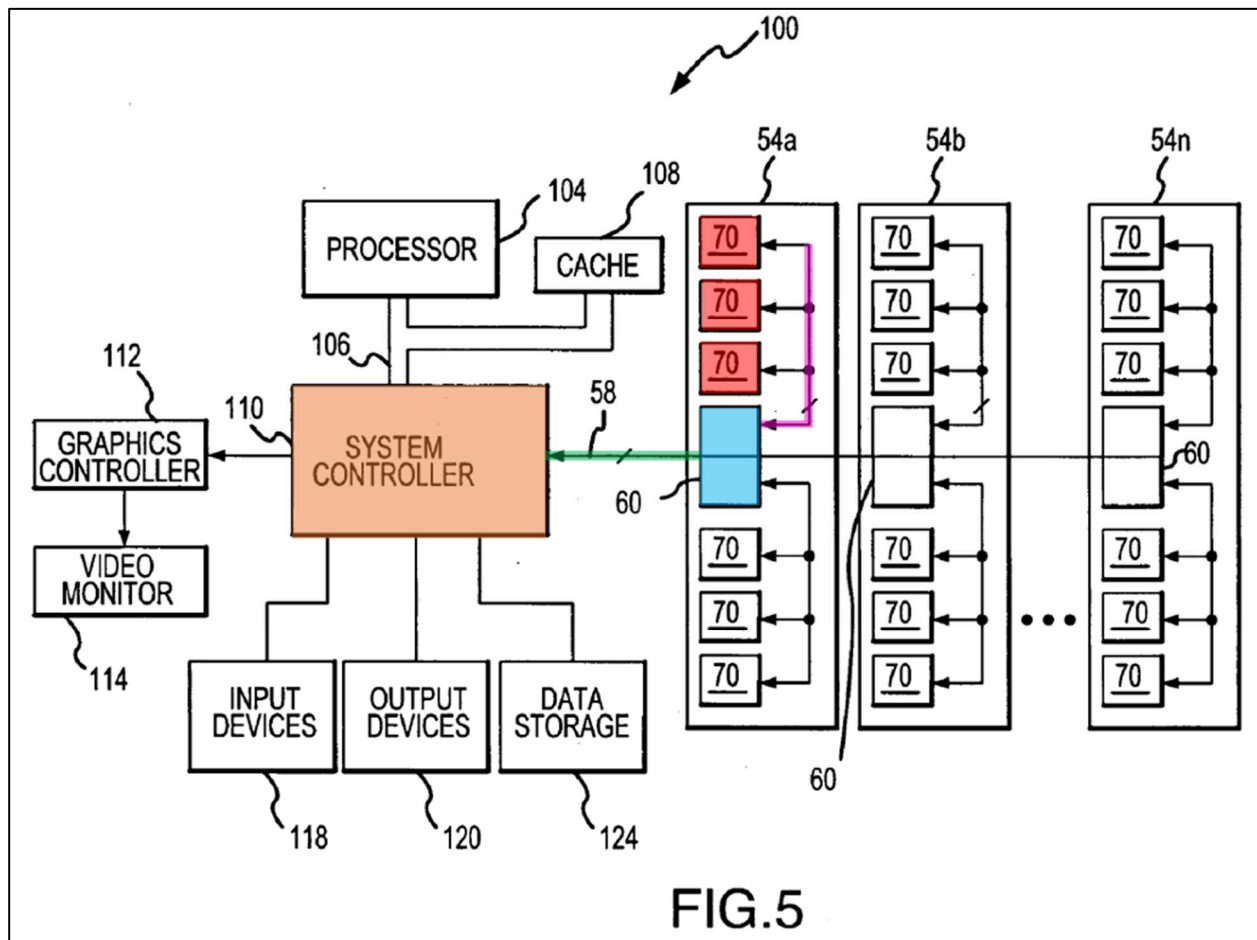
In this system (*see* FIG. 2, *infra*), a controller 52 (orange) is “coupled to several memory modules 54*a*, *b* ... *n* through a high-speed link 58” (green). EX1004, [0015]. Each memory module 54 “includes a memory hub 60 [blue] ... coupled to the high-speed link 58 and a bus system 68 coupled to several memory devices 70,” *e.g.*, DRAM. *Id.* “[T]he memory devices 70 are divided into four groups or ‘ranks’ [each] coupled to the memory hub 60 through a respective bus system” 76 (pink), 82, 90, 94. *Id.*, [0016]; EX1003, ¶31.



Lee, FIG. 2 (annotated)

Lee's mode of operation is configured by "a non-volatile register 98 in the memory module 54." EX1004, [0017]. First, in "high memory bandwidth" mode, "the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access." *Id.* These "128 bits of data" from all of the memory devices "can be coupled through the high-speed link 58 by either increasing the speed of the link 58 or the size of the data word coupled through the link 58." *Id.* Second, in "high memory depth mode, only one rank ... [is] addressed at a time." *Id.*, [0018]; EX1003, ¶32.

In a computer system (*see* FIG. 5, *infra*) implementing Lee's configurable memory system, the memory hubs (blue of the memory modules are coupled to a "system controller" (orange) that facilitates access to the memory modules by the system processor 104. EX1004, [0023], [0025]; EX1003, ¶33.



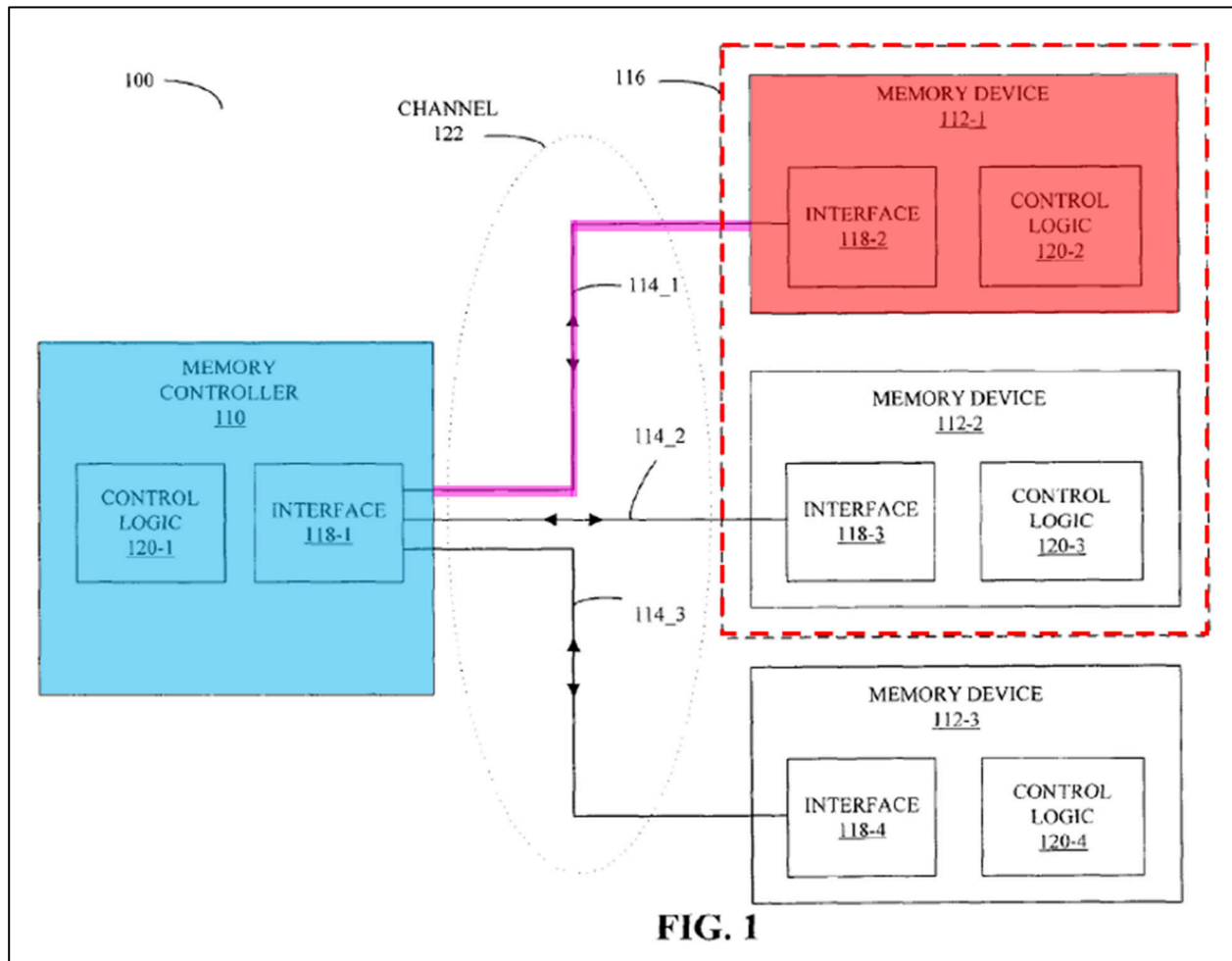
Lee, FIG. 5 (annotated)

Lee is analogous art to the '834 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '834 Patent was trying to solve. *See* EX1001, 1:28-33; EX1004, [0001], [0016]-[0017]; EX1003, ¶¶34-35.

2. Chang

Chang describes a “memory system 100” that includes a “memory controller 110,” blue in FIG. 1, *infra*, e.g., “a DRAM memory controller.” EX1006, [0020]-[0021]. “[M]emory devices 112” (red) that are “configured as a memory bank

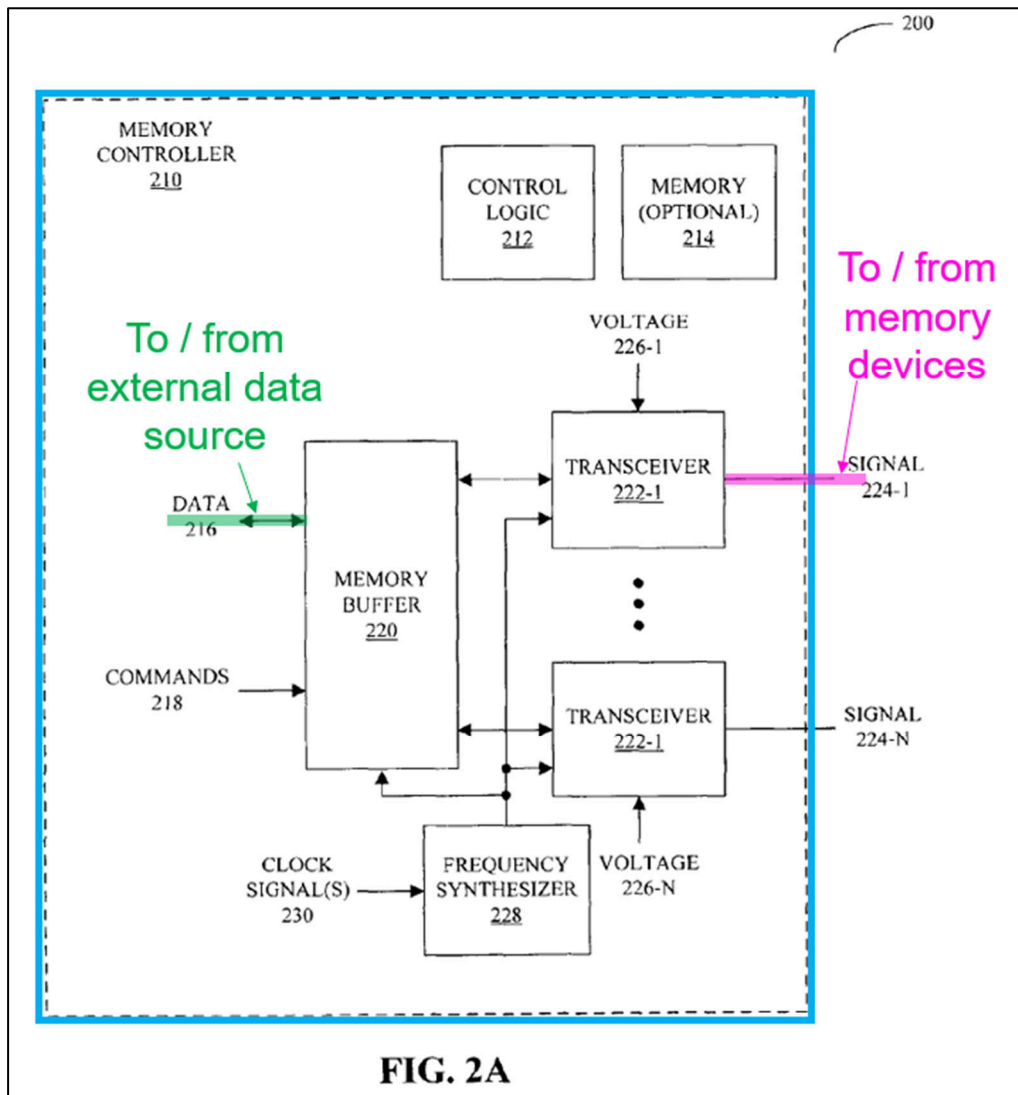
116.” *Id.*, [0023]. The “[m]emory controller 110 and memory devices 112 are coupled by one or more links 114” for transmission of “[s]ignals corresponding to data and/or commands.” *Id.*, [0024]-[0025]; EX1003, ¶36.



Chang, FIG. 1 (annotated)

Chang describes approaches for “error detection and/or correction.” EX1006, [0035]. “[C]ontrol logic 120 in the memory controller 110 and/or one of the memory device 112 may take a variety of remedial actions in the event of an error or a degradation of one or more of the performance metrics,” including

“reducing the data rate in one or more of the sub-channels relative to the data rate used in a previous transmission.” *Id.*, [0036]. “Data 216 to be transmitted by the memory controller 210 to a memory device” is “forwarded to transceivers 222, and is transmitted as (analog or digital signals) 224.” EX1006, [0042]; *see* FIG. 2A, *infra*; EX1003, ¶¶37-38.



Chang, FIG. 2A (annotated)

Chang describes that “voltage levels and/or a voltage swing of the signals 224 that are transmitted” to the memory devices are “based on voltages 226 provided by a power supply.” EX1006, [0045]. Similarly, “logic levels of the data that is received” at the memory controller from an external data source are “based on voltages 226 provided by the power supply.” *Id.* “These voltages may be fixed or may be adjustable.” *Id.*; EX1003, ¶39.

Chang is analogous art to the '834 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '834 Patent was trying to solve. *See* EX1001, 1:28-33; EX1006, Abstract, [0001]; EX1003, ¶¶40-41.

3. The Lee-Chang Combination

The Lee-Chang system is based on Lee's memory system 50. EX1003, ¶42. Four ranks of memory devices are coupled to the memory hub 60 through respective bus systems. *See* EX1004, [0016]. The memory hub is coupled to a memory controller through a “high-speed link 58.” *Id.* The memory system is operable in “high memory bandwidth” or “high memory depth” mode. EX1004, [0017]; EX1003, ¶42.

In the combination, data transmission characteristics are based on Chang, illustrated *infra*. EX1003, ¶43. Chang describes that “[d]ata 216 to be transmitted by the memory controller 210 to a memory device” can have “logic levels” that are “based on voltages 226 provided by [a] power supply,” where the “voltages may

provided by a power supply.” EX1006, [0045]. Chang’s signals 224 are data transmitted from Chang’s memory controller to the memory devices, *e.g.*, akin to data transmitted along Lee’s bus systems 76, 82, 90, 94. EX1003, ¶45. In the combination, the “voltage levels and/or a voltage swing of the signals” of the data transmitted along the bus systems between memory hub 60 and memory devices 70 are based on “fixed or ... adjustable” “voltages [] provided by the power supply,” based on Chang. EX1006, [0045]; EX1003, ¶45.

Optionally, the data rate for data transmission along one or more of the bus systems 76, 82, 90, 94 is “reduc[ed] ... relative to the data rate used in a previous transmission” as a “remedial action[],” based on Chang. EX1006, [0036]; EX1003, ¶46.

4. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to implement programmable signal swing in the Lee-Chang combination as follows. EX1003, ¶¶47-50.

First, as recognized in Chang, integration of a programmable signal swing enables responsiveness to “performance metrics associated with communication to and/or from” the memory hub, *e.g.*, facilitating continuous and low-error operation of the memory system. EX1006, [0046]; EX1003, ¶48.

Second, this implementation is merely the application of known techniques (adjustable signal swing on transmission buses in a memory system) by a known

system (Lee's memory system) to yield predictable results (a memory system in which signal swing is adjustable on transmission buses of the system). EX1003, ¶49; *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success because memory system technology is predictable, and because Chang's disclosure of adjustable signal swing is in the context of a memory system that is structured similarly to Lee's system. EX1003, ¶50.

A POSITA would have been motivated to implement programmable data rate in the Lee-Chang combination as follows. EX1003, ¶¶51-54.

First, programmable data rate provides a mechanism for "remedial action[]" responsive to "an error or a degradation of one or more of the performance metrics during communication between" the memory hub and the memory devices of the combination, *e.g.*, facilitating continuous and low-error operation of the memory system. Chang, [0036]; EX1003, ¶52.

Second, this implementation is merely the application of known techniques (adjustable data rate on transmission buses in a memory system) by a known system (Lee's memory system) to yield predictable results (a memory system in which data rate is adjustable on transmission buses of the system). EX1003, ¶53; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because memory system technology is predictable, and because Chang’s disclosure of adjustable data rate is in the context of a memory system that is structured similarly to Lee’s system. EX1003, ¶54.

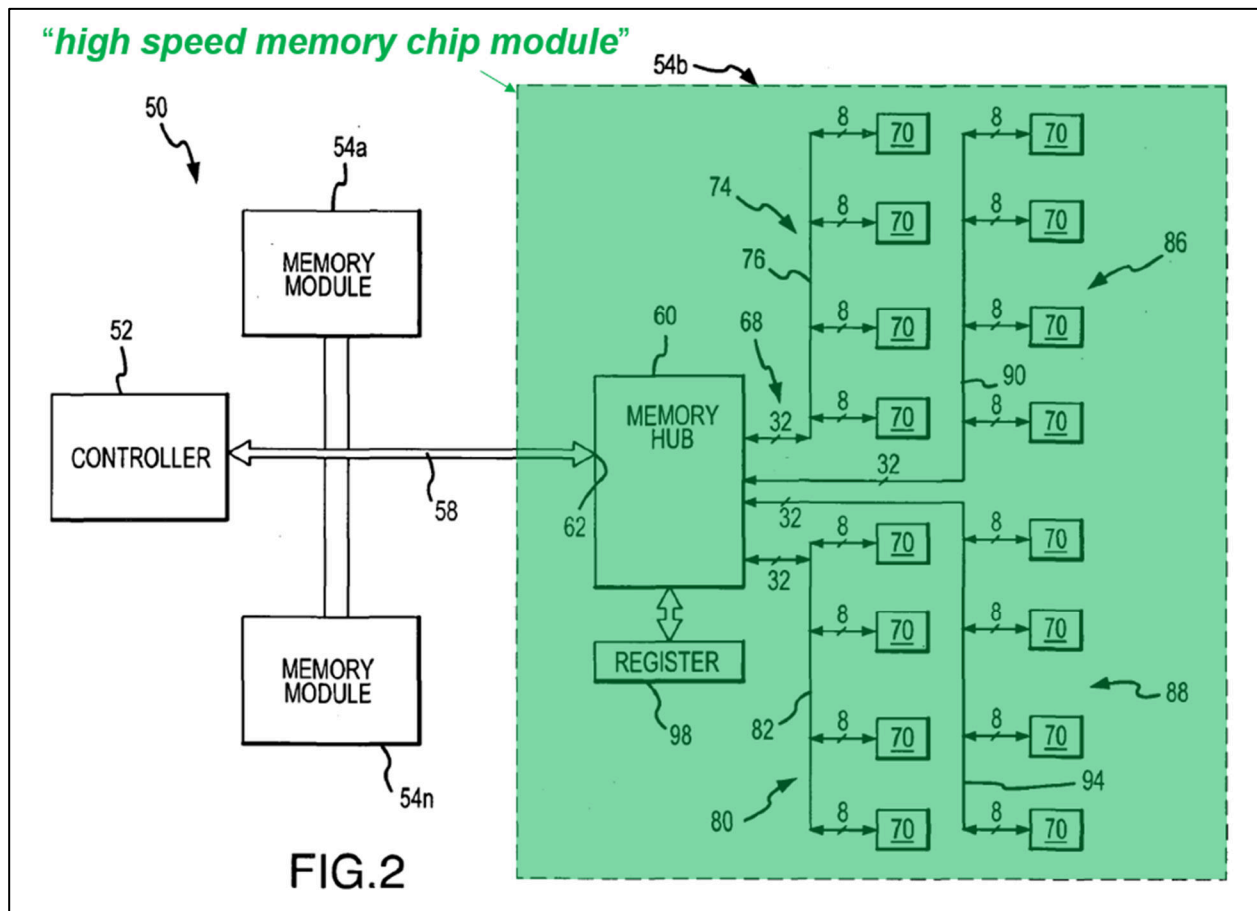
5. Analysis

(a) Claim 1

[1pre]⁵

Based on Lee, the Lee-Chang computer system includes a “memory system 50” that “includes a controller 52 coupled to several memory modules 54a, b ... n through a high-speed link 58,” where each memory module includes “memory devices 70.” *Id.*, [0015]-[0016], [0023]; *see* Abstract, [0014] (“FIG. 5 is a block diagram of a computer system using the memory system of FIG. 2”), FIG. 2. Each memory module 54 (*e.g.*, memory module 54a, green) corresponds to a ***memory chip module***, because it includes memory chips. EX1003, ¶¶55-56.

⁵ Petitioner does not concede that the preambles of the Challenged Claims are limiting.



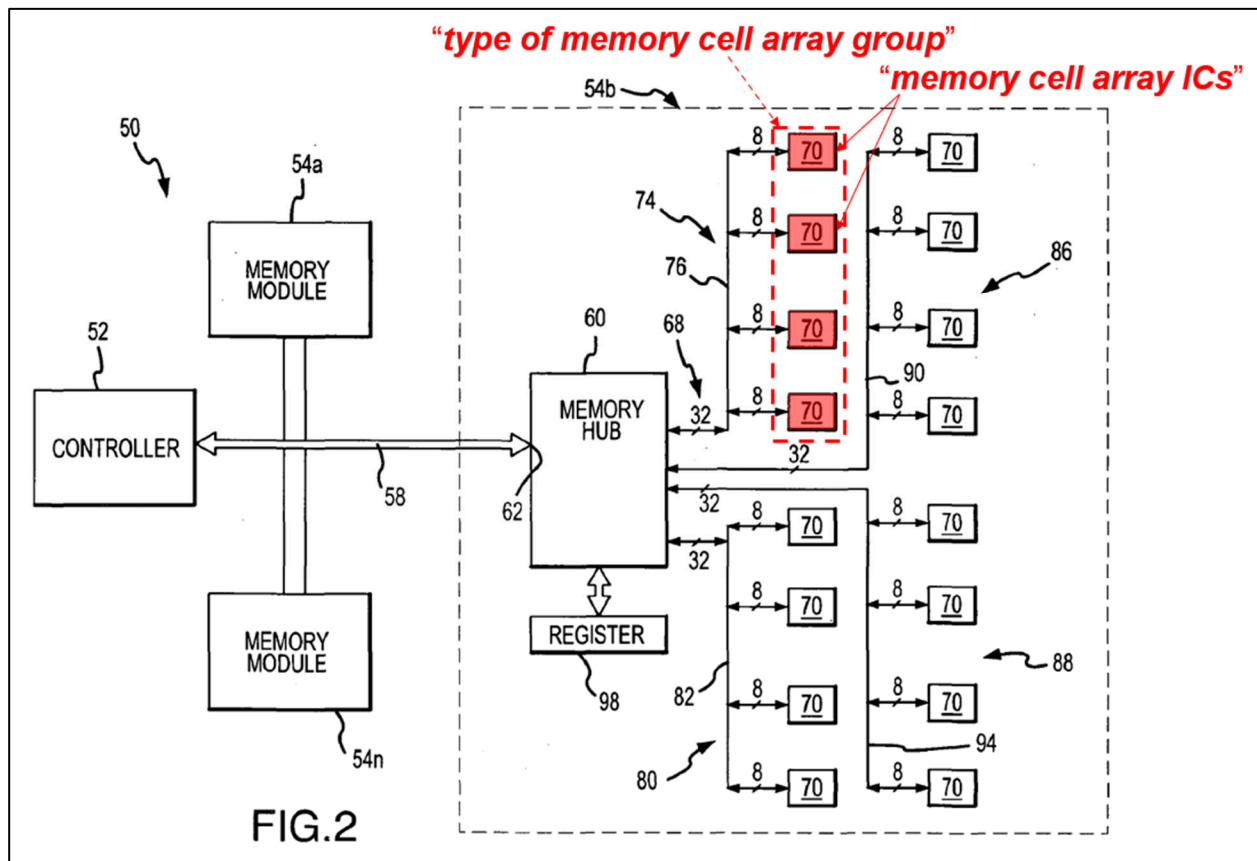
Lee, FIG. 2 (annotated)

The memory module is a *high speed memory chip module* because it is coupled to the controller “through a high-speed link.” EX1004, [0015]; *see* [0017]; EX1003, ¶57.

The memory module is *reconfigurable* because it can be “configure[d] ... depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]; *see* [0020] (“By allowing the memory hub 60 to configure the data format of the memory module 54 ... The data format is therefore not fixed”); EX1003, ¶58.

[1a]

Based on Lee, the combination system includes “several memory modules 54a, b ... n,” each of which includes “memory devices 70 [] divided into four groups or ‘ranks.’” EX1004, [0016]; *see* Abstract, claim 1, claim 13, claim 28, FIG. 5. Lee’s memory devices 70 (some of which are highlighted in red in FIG. 2, *infra*) correspond to ***memory cell array ICs***, *e.g.*, because they are integrated circuit memory devices: “The memory devices 70 may be, for example, dynamic random access memory devices (‘DRAMs’) or some other type of memory devices.” EX1004, [0016]; *see* claims 11-12. DRAM devices (among other types of memory devices) are ***integrated circuits (ICs)***. EX1003, ¶¶59-60 (citing EX1005, 12; EX1016, 4:56-60).



Lee, FIG. 2 (annotated)

“[T]he memory devices 70 are divided into four groups or ‘ranks.’”

EX1004, [0016]. Each group/rank corresponds to a *type of memory cell array group* because it is a group of memory cells (e.g., memory devices 70). EX1003, ¶61. For instance, “a first rank 74” (*type of memory cell array group*) (red in FIG. 2, *supra*) “includes four memory devices 70” (*comprises multiple memory cell array ICs*), and likewise for ranks 80, 86, 88. EX1004, [0016]; *see* claims 1, 13, 28, FIG. 5. Alternatively/additionally, the multiple groups/ranks collectively correspond to a *type of memory cell array group*. EX1003, ¶61.

[1b]

In the combination, based on Lee, a memory hub 60 is coupled to the memory devices (*type of memory cell array group*) through “a bus system 68,” which enables access to the memory devices of each rank “through a respective bus system” 76, 82, 90, 94. EX1004, [0016]. Each of these bus systems individually corresponds to a *first transmission bus*. EX1003, ¶62.

Alternatively/additionally, the bus system 68 (composed of the four bus systems 76, 82, 90, 94) corresponds to the *first transmission bus*. EX1003, ¶62.

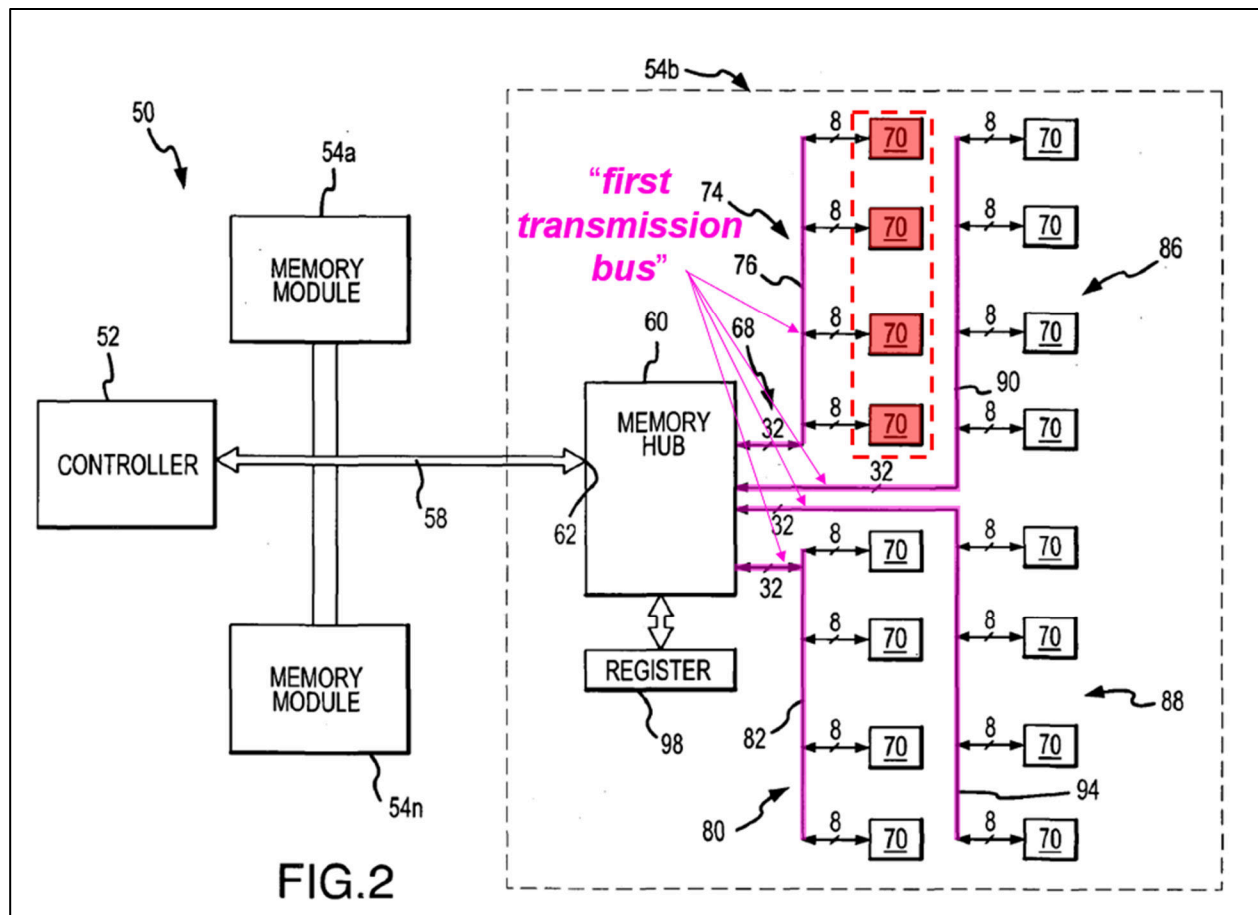
Each of Lee’s bus systems individually corresponds to a *first transmission bus*

In the combination, the bus system for each rank corresponds to a *first transmission bus* through which the memory hub can *access* the memory cell array ICs in that rank. EX1003, ¶63. For instance, the first rank 74 (*type of memory cell array group*) of memory devices are “coupled to the memory hub 60 through a first bus system 76 having a 32-bit data bus” (*first transmission bus*) (pink in FIG. 2, *infra*). EX1004, [0016]; *see id.*, claim 2, claim 14; EX1003, ¶63.

one or more of the memory devices,” e.g., the *data rate is programmable* by way of the control logic. EX1006, [0036]; EX1003, ¶65.

Lee’s bus system 68 corresponds to the *first transmission bus*

Alternatively/additionally, in the combination, Lee’s “bus system 68” (pink in FIG. 2, *infra*), which is composed of four bus systems 76, 82, 90, 94, corresponds to the *first transmission bus* coupled to the memory cell ICs. EX1004, [0016] (“bus system 68 coupled to several memory devices 70”); EX1003, ¶66.



Lee, FIG. 2 (annotated)

In the combination, Lee describes that in “high memory bandwidth” mode, “the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access,” *i.e.*, the ***data rate of the first transmission bus*** (*i.e.*, the bus system 68 including the four individual bus systems 76, 82, 90, 94) is 128 bits per memory access. EX1004, [0017]; EX1003, ¶67.

Lee describes that alternatively, in “high memory depth mode, only one rank 74, 80, 86, 88 may be addressed at a time,” such that “only 32 bits of data will be coupled to or from the memory module 54 with each memory access.” *Id.* That is, ***the data rate of the first transmission bus*** (the bus system 68) in high memory depth mode is 32 bits per memory access. EX1003, ¶68.

The combination system can be “configure[d]” to operate in high memory bandwidth or high memory depth mode. EX1004, [0017]; *see* [0019]. The mode of operation is ***programmable*** by way of “a non-volatile register 98 in the memory module 54,” which “is programmed to configure the memory hub 60 depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]; *see* claim 5 (“a programmable storage device ... being programmed to control the operating mode of the memory hub”); EX1003, ¶70. Because the data rate of the first transmission bus differs between the two modes

of operation, and the selection of the mode of operation is programmable, the data rate of the first transmission bus is ***programmable***. EX1003, ¶70.

Alternatively/additionally, the data rate of the first transmission bus is ***programmable*** based on Chang's teachings of reducing the data rate, discussed *supra*. See EX1006, [0035]-[0036]; EX1003, ¶71.

The combination first transmission bus has a programmable transmitting or receiving signal swing

In the combination, based on Chang, “voltage levels and/or a voltage swing of the signals 224 that are transmitted” between the memory hub and the memory devices (along the bus systems 76, 82, 90, 94) are “based on voltages 226 provided by a power supply” where the “voltages ... may be adjustable.” EX1006, [0045]; EX1003, ¶72. A voltage swing (signal swing) that is based on an adjustable voltage is itself adjustable. EX1003, ¶73. That is, the voltage swing (***signal swing***) of data transmitted along one or more of the bus systems between memory hub and memory devices (***a signal swing of the first transmission bus***) is adjustable. *Id.*

Specifically, the power supply voltages are “adjusted based on one or more performance metrics associated with communication to and/or from the memory controller 210.” EX1006, [0046]. A POSITA would have understood Chang's system to have been programmed to change the voltages based on performance

metrics, *e.g.*, to ensure satisfaction of performance metrics. EX1003, ¶74. Thus, the voltage swing (*signal swing*) of the first transmission bus is *programmable* because it is based on a programmable voltage power supply. *Id.*

[1c]

The combination system's "a memory hub 60" (blue in FIG. 2, *infra*) corresponds to *a logic unit*⁶ because it is "programmable to configure the memory module in a plurality of data formats." EX1004, [0016], claim 1; *see* [0009], [0017]-[0020], claims 1-5; EX1003, ¶75.

⁶ Petitioner notes the lack of antecedent basis for "the logic unit" and incorporates the analysis for claim element [1d] for further discussion of this feature. EX1003, ¶75.

The combination second transmission bus has a programmable transmitting or receiving data rate

In the combination, Lee describes that “[i]n the high memory depth mode, the high-speed link 58 can operate at a slower data rate than in the high bandwidth mode,” *i.e.*, the ***data rate of the second transmission bus*** differs based on the mode of operation. EX1004, [0018]. Lee’s system can be “configure[d]” to operate in high memory bandwidth or high memory depth mode, *i.e.*, programmed to operate such that data is transmitted along the second transmission bus at different data rates (***second transmission bus has a programmable transmitting or receiving data rate***). EX1004, [0017]; *see* [0019]; EX1003, ¶78. The mode of operation (and thus the data rate of the second transmission bus) is ***programmable*** by way of “a non-volatile register 98 in the memory module 54,” which “is programmed to configure the memory hub 60 depending upon whether a high memory bandwidth or a high memory depth is desired.” EX1004, [0017]; *see* claim 5 (“a programmable storage device ... being programmed to control the operating mode of the memory hub”); EX1003, ¶79.

Alternatively/additionally, in “high memory bandwidth” mode, “the high-speed link 58 may couple data at a rate of 2 GB/sec,” or “at a rate of 1 GB/sec,” *i.e.*, the high-speed link (***second transmission bus***) can be operated at different

data rates, *i.e.*, has a ***programmable transmitting or receiving data rate***. EX1004, [0017]; EX1003, ¶80.

The combination second transmission bus has a programmable transmitting or receiving signal swing

In the combination, based on Chang, “[d]ata 216 to be transmitted by the memory controller 210 to a memory device” (along the high-speed bus 58) have “logic levels” that are “based on voltages 226 provided by [a] power supply,” where the “voltages ... may be adjustable.” EX1006, [0045]; EX1003, ¶81. A voltage swing (signal swing) that is based on an adjustable voltage is itself adjustable. EX1003, ¶82. That is, the voltage swing (***signal swing***) of data transmitted along the high-speed bus 58 to the memory hub (***a signal swing of the second transmission bus***) is adjustable. *Id.*

Specifically, the power supply voltages are “adjusted based on one or more performance metrics associated with communication to and/or from the memory controller 210.” EX1006, [0046]. A POSITA would have understood Chang’s system to have been programmed to change the voltages based on performance metrics, *e.g.*, to ensure satisfaction of performance metrics. EX1003, ¶83. Thus, the voltage swing (***signal swing***) of the second transmission bus is ***programmable*** because it is based on a programmable voltage power supply. *Id.*

[1d]

The combination memory hub (*logic unit*) is *coupled to* the first transmission bus *for accessing the type of memory cell array group through the first transmission bus*: “the memory devices 70 are divided into four groups or ‘ranks’ coupled to the memory hub 60 through a respective bus system,” such that “the four memory devices 70 together provide 32 bits for the 32-bit data buses.” EX1004, [0016]; *see id.* (“More particularly, a first rank 74 includes four memory devices 70 coupled to the memory hub 60 through a first bus system 76 having a 32-bit data bus”), [0017]-[0019], claim 2; EX1003, ¶¶84-85.

Parallel data on the first transmission bus

In the combination, the data transmitted on the bus system for each rank (*first transmission bus*) are *a first set of parallel data*, e.g., 32 parallel bits of data carried on the “32-bit data bus.” EX1004, [0016]; *see* [0017] (“the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices”), [0018], claim 6, [0009], [0019], claims 2, 3, 4, and 7; EX1003, ¶86.

Each individual bus system transmits *parallel data*, and thus the data transmitted on the collective bus system 68 (*first transmission bus*) are *a first set of parallel data*. *See* EX1004, [0016]-[0019]; EX1003, ¶87. Alternatively/ additionally, the individual bus systems 76, 82, 90, 94 are connected in parallel to

the memory hub, *e.g.*, so that the memory hub can “address[] all of the memory devices simultaneously so that 128 bits of data are written to or read from the memory devices.” EX1004, [0017]; *see* claim 3, claim 4. Accordingly, the parallel data transmitted on each individual bus system 76, 82, 90, 94 is also parallel to the data transmitted on each other individual bus system. EX1003, ¶87. Thus, the data transmitted on the collective bus system 68 (***first transmission bus***) are ***a first set of parallel data***, *e.g.*, “128 bits of data” transmitted “simultaneously” and in parallel on the four constituent bus systems. EX1004, [0017]; EX1003, ¶87.

Parallel data on the second transmission bus

The data transmitted on Lee’s high-speed link (***second transmission bus***) is ***a second set of parallel data***. EX1003, ¶88. When operated in “high memory bandwidth” mode, Lee’s high-speed link can be configured such that “a 128-bit data word may be coupled through the link 58,” *i.e.*, the 128-bit data word corresponds to the ***second set of parallel data***. EX1004, [0017]. Lee’s high-speed link can alternatively be configured to “couple 64-bit data words” or “32-bit data word[s],” *i.e.*, the 64-bit data word or 32-bit data word corresponds to the ***second set of parallel data***. EX1004, [0017]; EX1003, ¶88.

The combination logic is for converting the first set of parallel data to the second set of parallel data

A POSITA would have found obvious that Lee's memory hub (***logic unit***) is ***used for converting the first set of parallel data into the second set of parallel data***, both when the ***first set of parallel data*** are the data transmitted on an individual bus systems and alternatively/additionally, when the ***first set of parallel data*** are the data transmitted on the collective bus system 68, discussed *infra*.

EX1003, ¶89.

Conversion of data when an individual bus system corresponds to the first transmission bus

In “high memory bandwidth” mode, Lee's memory hub “simultaneously” receives multiple sets of parallel data from the multiple bus systems 76, 82, 90, 94. EX1004, [0016]-[0017], FIG. 2. By “simultaneously” addressing “all of the memory devices,” “128 bits of data are ... read from the memory devices,” *i.e.*, 32 bits are received through each of the four bus systems. *Id.*, [0017]; *see* [0019]. These simultaneously received 128 bits of data include the 32 bits (***first set of parallel data***) transmitted on the first bus system 76. Lee describes two implementations for transmission of that 128 bits of data on the high-speed link 58, discussed *infra*. *See* EX1004, [0017]; EX1003, ¶¶90-92. Both implementations involve ***converting the first set of parallel data*** (transmitted on the first bus system

76) *into the second set of parallel data* (transmitted on the high-speed bus 58).

EX1003, ¶92.

In one implementation of “high memory bandwidth” mode, “128 bits of data are ... read from the memory devices” (*i.e.*, 32 bits through each of the four bus systems), but “the link 58 may transfer only a 32-bit data word” or a “64-bit data word[]” (*second set of parallel data*). EX1004, [0017]. A POSITA would have found obvious that receiving 128 bits of data simultaneously through multiple bus systems and then transmitting that data in a 64- or 32-bit word through a single bus system involves the memory hub **converting** the received data (including *the first set of parallel data*) to the transmitted data (*second set of parallel data*), *e.g.*, by multiplexing the received data. EX1003, ¶¶93-95 (citing EX1019, Abstract (“a parallel-to-parallel converter for converting an ‘m’-bit parallel signal into an ‘n’-bit parallel signal)). Specifically, the bit width of the parallel data received through the multiple bus systems (128 bits of simultaneously received data) is different from the bit width of the parallel data transmitted through the high-speed link 58 (*e.g.*, one 32-bit or 64-bit word). *See* EX1004, [0017]. A POSITA would have recognized that this implementation—*i.e.*, receiving data of one bit width and then transmitting that same data in a different bit width—involves **converting** the received data (including *the first set of parallel data*) to the transmitted data (*second set of parallel data*). EX1003, ¶¶93-95 (citing EX1019, Abstract).

In another implementation, “[t]he 128 bits of data [are] coupled through the high-speed link by [] increasing ... the size of the data word coupled through the link 58.” EX1004, [0017]. For instance, a “128-bit data word” (*second set of parallel data*) “may be coupled through the link 58.” *Id.*, [0017]. That is, Lee’s memory hub (*logic unit*) receives 128 bits of data through four distinct bus systems, and *converts* that received data to a “128-bit data word” for transmission on the single high-speed link 58. *Id.*, [0017]; *see* [0019]; EX1003, ¶96. A POSITA would have found obvious that receiving data simultaneously through multiple bus systems and then transmitting that data through a single bus system involves *converting*, by the memory hub (*logic unit*) the data received from the multiple bus systems (*i.e.*, 128 bits of simultaneously received data, including the 32-bit *first set of parallel data* transmitted on the first bus system 76) into the data transmitted on the single high-speed link 58 (*the second set of parallel data*). EX1003, ¶96.

Conversion of data when the bus system 68 corresponds to the second transmission bus

Alternatively/additionally, in “high memory bandwidth” mode, the “128 bits of data” that are “simultaneously” “read from the memory devices” collectively correspond to the *first set of parallel data*, discussed *supra*. EX1003, ¶¶97-98.

In one implementation, the 128 bits (*first set of parallel data*) are read simultaneously from the bus system 68, but “the link 58 may transfer only a 32-bit data word” or a “64-bit data word[]” (*second set of parallel data*). EX1004, [0017]; EX1003, ¶99. A POSITA would have found obvious that receiving 128 bits of data simultaneously through multiple bus systems and then transmitting that data as a 64- or 32-bit word through a single bus system involves *converting* the received data (*first set of parallel data*) to the transmitted data (*second set of parallel data*), *e.g.*, by multiplexing the received data. EX1003, ¶99 (citing EX1019, Abstract).

In another implementation, the 128 bits of data are received through four distinct bus systems that constitute the bus system 68 and *converted* to a “128-bit data word” for transmission on the single high-speed link 58, discussed *supra*. EX1004, [0017]; *see* [0019]; EX1003, ¶100. A POSITA would have found obvious that receiving data simultaneously through multiple bus systems and then transmitting that data through a single bus system involves *converting*, by the memory hub (*logic unit*) the data received from the multiple bus systems (*first set of parallel data*) into the data transmitted on the single high-speed link 58 (*second set of parallel data*), *e.g.*, by multiplexing. EX1003, ¶100.

(b) **Claim 2**

[2a]

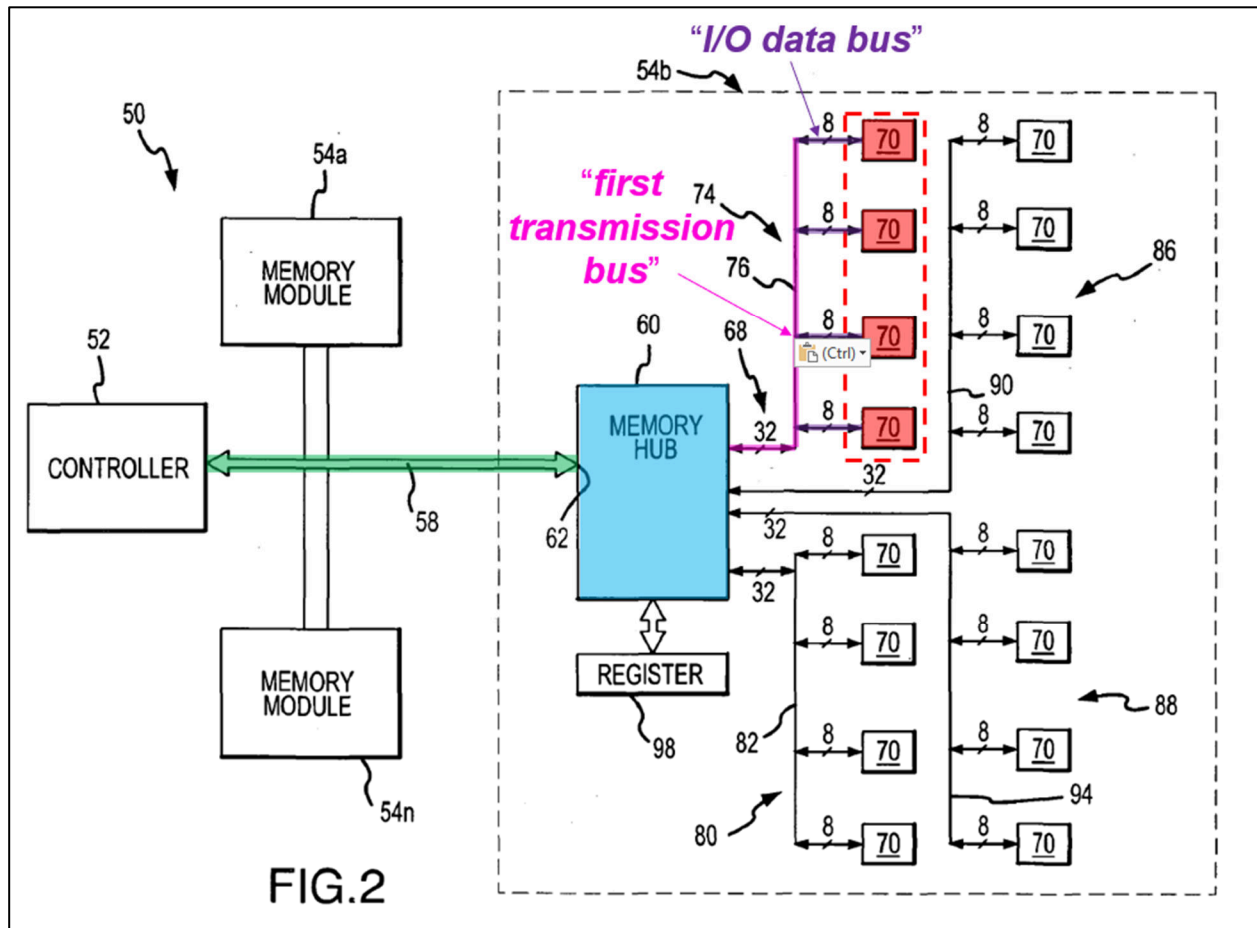
In the combination, the bus system for each rank (*first transmission bus*) is a “32-bit data bus,” and “the four memory devices 70 together provide 32 bits for the 32-bit data buses.” EX1004, [0016]. That is, the bus system for each rank (e.g., the first bus system 76) (*first transmission bus*) is *used for transmitting data along with⁷ (to/from) the memory cell array ICs*, e.g., for transmitting the data to/from the memory devices of the rank. EX1003, ¶101.

Alternatively/additionally, the bus system 68 (*first transmission busa*) is *used for transmitting data along with⁸ (to/from) the memory cell array ICs* because each individual bus system 76, 82, 90, 94 of the bus system 68 is so used, discussed *supra*. See EX1004, [0016]-[0019]; EX1003, ¶102.

⁸ Without conceding that the claims are not indefinite, Petitioner interprets the phrase “*along with* the memory cell array ICs” as “*to/from* the memory cell array ICs.” EX1003, ¶101.

[2b]

In the combination, each memory device 70 (*memory cell array IC*) has “an 8-bit data bus” (*I/O data bus*) (purple in FIG. 2, *infra*). EX1004, [0016]; EX1003, ¶103.



Lee, FIG. 2 (annotated)

In the combination, based on the example of Lee’s FIG. 2, the ***bus width of the (I/O) data bus of each of the memory cell array ICs*** is 8 bits. See EX1004, [0016] (“each of the memory devices 70 have an 8-bit data bus”), FIG. 2. The ***bus width of the first transmission bus*** (e.g., first bus system 76, pink in FIG. 2, *supra*)

is 32 bits, *i.e.*, ***wider than the bus width of each I/O data bus***. See EX1004, [0016] (“a first bus system 76 having a 32-bit data bus”); EX1003, ¶104.

Alternatively/additionally, the bus width of the bus system 68 (***first transmission bus***) is 128 bits, *i.e.*, equal to the total bus width of the four constituent bus systems, each of which is 32 bits wide. That is, the 128-bit bus width of the bus system 68 (***bus width of the first transmission bus***) is ***wider than*** the 8-bit ***bus width of each I/O data bus***. See EX1004, [0016], FIG. 2; EX1003, ¶105.

(c) **Claim 4**

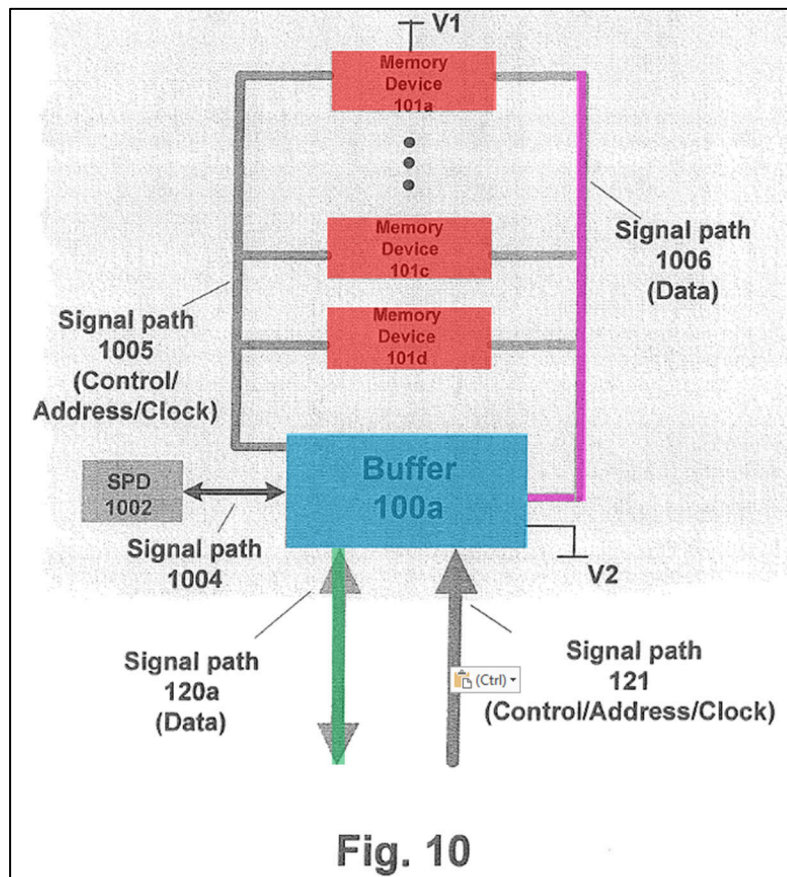
[4]

Based on Lee, the combination can be “configure[d]” to operate in high memory bandwidth or high memory depth mode, which corresponds to ***programmability of the first transmission bus*** and/or ***the second transmission bus*** (see [1b]-[1c]). See EX1004, [0017], [0019]; EX1003, ¶105. The mode of operation is ***programmable*** by way of “a non-volatile register 98 in the memory module 54,” which “is programmed to configure the memory hub 60 depending upon whether a high memory bandwidth or a high memory depth is desired,” *i.e.*, ***programmability of the first/second transmission bus corresponds to a register***. EX1004, [0017]; see claim 5 (“[a] programmable storage device being programmed to control the operating mode of the memory hub”); EX1003, ¶105.

B. GROUND 1B: Claims 1-2 and 4 Are Obvious Over Lee-Chang-Tsern

1. Tsern

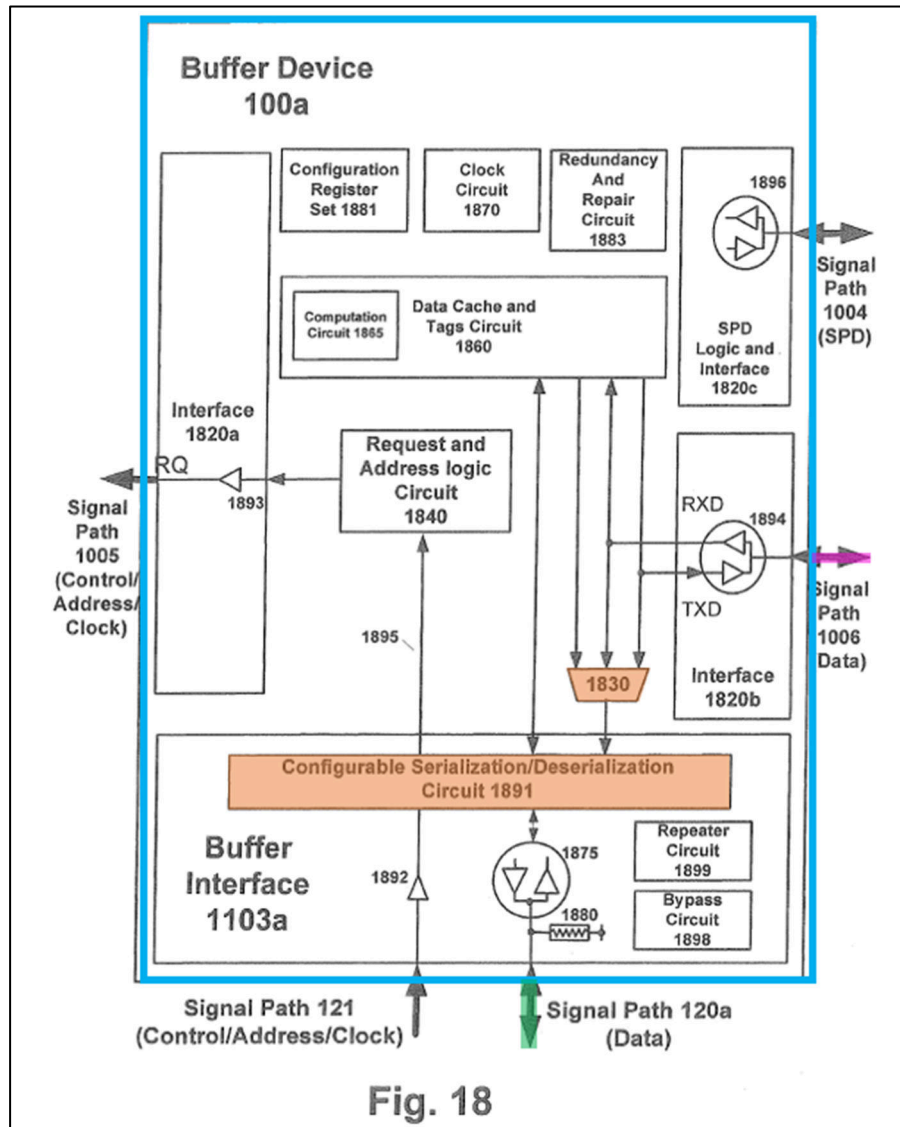
Like Lee, Tsern relates to a memory system having connections “between an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices.” EX1005, Abstract. The system (*see* Fig. 10, *infra*), includes “integrated circuit memory devices 101a-d [red] and a buffer 100a [blue],” with data transferred therebetween “on a signal path 1006,” pink. *Id.* A “signal path 120a,” green, “transfer[s] data” between the buffer and “a memory module connector interface.” *Id.*, 12; EX1003, ¶106.



Tsern, Fig. 10 (annotated)

An example buffer device 100a (*see* 18, *infra*) includes an interface 1820b “transfer[s] data between buffer 100a and one or more memory devices.” EX1005, 30, 32-33. The interface can “access different memory widths,” such as “16 ‘x4’ width memory devices, 8 ‘x8’ width memory devices or 4 ‘x16’ width memory devices.” *Id.*, 37. A multiplexer 1830 (orange) “perform[s] bandwidth-concentrating operations between buffer interface 100a and interface 1820b,” *e.g.*, “utiliz[ing] the combined bandwidth of multiple data paths [1006] coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” *Id.*,

33. The buffer interface 1103a, coupled to the signal path 120a to communicate data to a memory controller, includes a “[c]onfigurable serialization/deserialization circuit 1891,” orange, that “performs serialization and deserialization functions” on the data depending on “memory device access width.” *Id.*, 31, 38; EX1003, ¶107.

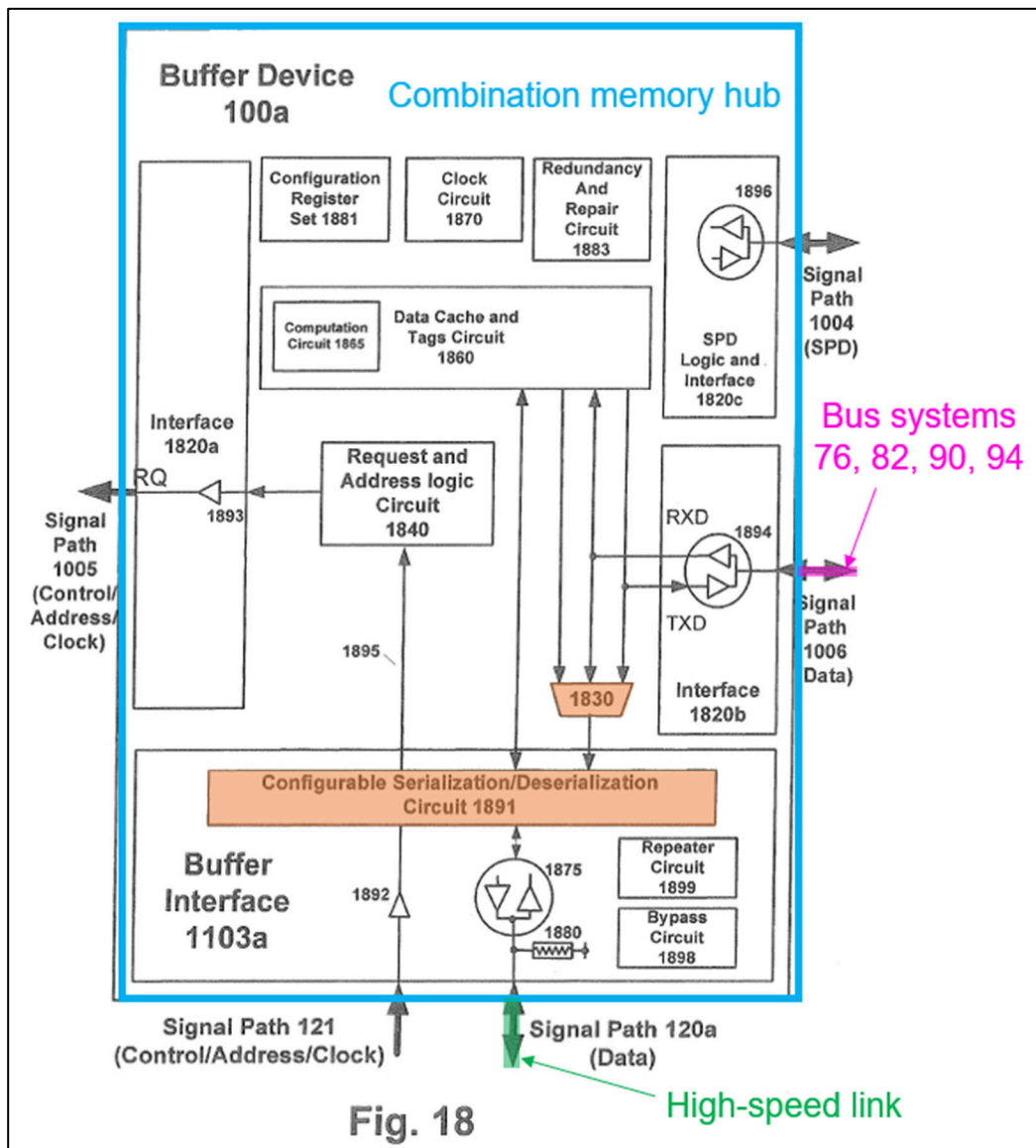


Tsern, Fig. 18 (annotated)

Another example buffer device 3600 “operates similar to buffer 100a” in that it receives “read data via one or more signal paths 1006” from memory devices and “transmits corresponding signals to a master.” EX1005, 68. This buffer device (*see* Fig. 36, *infra*) includes “data path 3606 and data path router 3610,” *orange*, that “merge separate read data from more than one memory device into a single merged read data or read stream output at interface 3601.” *Id.* The buffer device 3600 includes an “interface 3611” that has “at least three different configurations or segmentation modes: 1) Four 4-bit interfaces (4x4), 2) Two 4-bit interfaces (2x4) or 3) Two 8-bit interfaces (2x8),” which “allow[s] flexibility in memory module or memory stack configurations.” *Id.*, 69; EX1003, ¶¶108-109.

coupled to a memory controller through a “high-speed link 58.” *Id.* The memory system is operable in “high memory bandwidth” or “high memory depth” mode. EX1004, [0017]. The signal swing on the transmission buses is programmable based on Chang, *See* Ground 1A. EX1003, ¶112. The combination memory hub is implemented as an “integrated circuit buffer device” based on Tsern’s buffer device 100a or 3600. *See* EX1005, Abstract, 12, 30, Fig. 11, Fig. 18; EX1003, ¶¶113-114.

In one example of the combination, illustrated *infra*, the memory hub is implemented based on Tsern’s buffer device 100a. *See* EX1005, 12, 30, Abstract, Fig. 18; EX1003, ¶114.



Lee-Chang-Tsern figure based on Tsern, Fig. 18

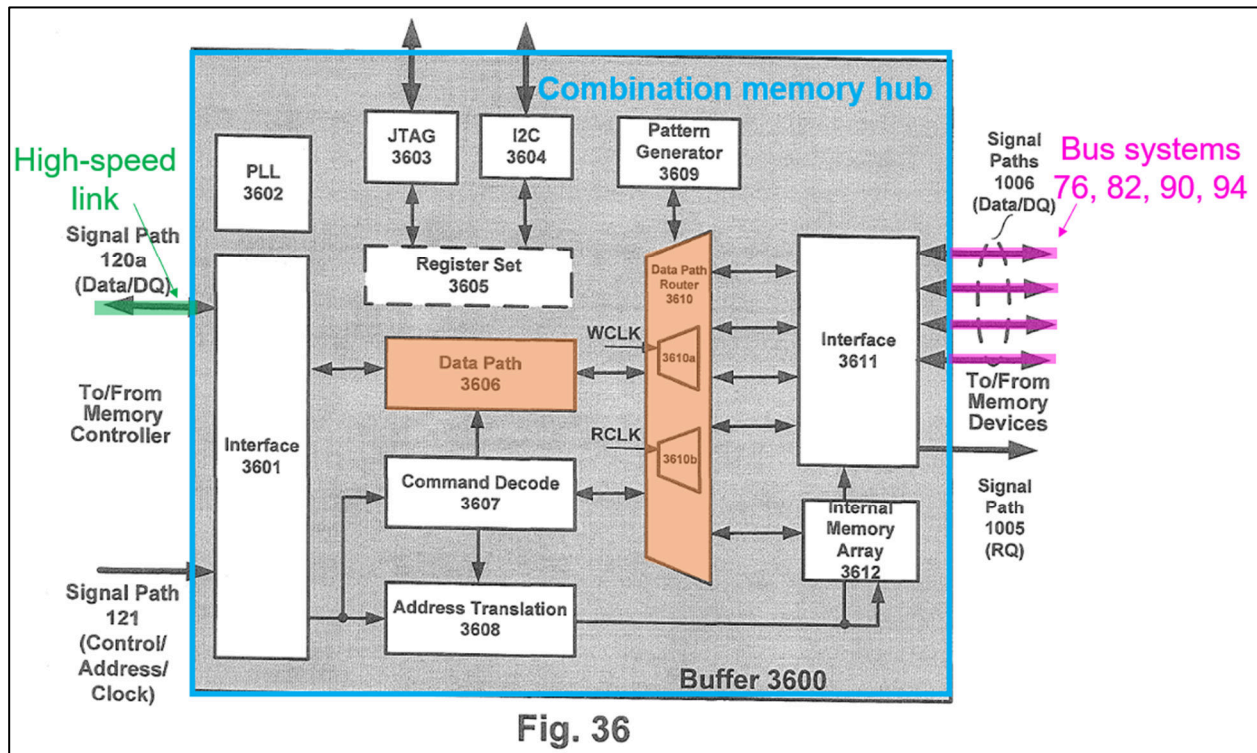
Tsern's buffer device 100a includes a buffer interface 1103a coupling the buffer device to a memory controller a signal path 120a, similar to Lee's high-speed link 58 coupling the memory hub to the controller 52. *See* EX1005, 22, 30-31; EX1004, [0015]-[0016], FIG. 2. Based on similarity, the combination memory hub has a buffer interface that couples the memory hub to the controller via the

high-speed link 58 (green *supra*). See EX1004, [0015]-[0016], FIG. 2; EX1003, ¶115.

Tsern's buffer device 100a also includes an "[i]nterface 1820b" "coupled to signal path 1006 to transfer data between buffer 100a and one or more memory devices 101a-d." EX1005, 32-33. The "number of ... data signal lines between buffer 100a and memory devices 101a-d are programmable in order to accommodate different numbers of memory devices." *Id.*, 37. Based on these teachings, the combination memory hub has an interface that is coupled to the bus systems 76, 82, 90, 94 of the combination to transfer data between the memory hub and the memory devices. See EX1004, [0016], FIG. 2; EX1003, ¶116.

Other aspects of the combination memory hub are implemented based on Tsern. EX1003, ¶117. A "multiplexer 1830 [orange] may perform bandwidth-concentrating operations," allowing the buffer to "utilize[] the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a," *e.g.*, enabling implementation of high memory bandwidth mode. EX1005, 33; *see* EX1004, [0017]. The combination memory hub also has a "[c]onfigurable serialization/ deserialization circuit 1891" (orange) that provides "an access interleaving or multiplexing scheme ... to ensure that all storage locations within memory devices 101a-d can be accessed." EX1005, 38; EX1003, ¶117.

In an alternative example of the combination, illustrated *infra*, the memory hub is implemented based on Tsern's integrated circuit buffer device 3600. See EX1005, 68, Fig. 36; EX1003, ¶118.



Lee-Chang-Tsern figure based on Tsern, Fig. 36

This combination memory hub includes “interfaces 3601 and 3611” to communicate data between, respectively, the memory hub and a memory controller via the combination high-speed link (green *supra*), and between the memory hub and the ranks of memory devices via bus systems 76, 82, 90, 94 (pink *supra*). EX1005, 67; see EX1004, [0016]-[0020], FIG. 2; EX1003, ¶¶119-120. Based on Tsern, the combination memory hub includes “data path 3606 and data path router 3610,” orange *supra*, that “merge separate read data from more than one memory

device” into a single merged read data or read stream output,” for output onto the high-speed link. EX1005, 68; *see* EX1004, [0016]-[0020], FIG. 2; EX1003, ¶121. The data path router includes “signal paths used to merge read data from different memory devices as well as parse write data into write data portions to be stored in multiple memory devices.” EX1005, 71.

3. Motivation to Combine and Expectation of Success

Motivation for implementing functionality of Tsern’s buffer device in the combination memory hub

A POSITA would have been motivated to implement the combination memory hub to have functionality based on embodiments of Tsern’s buffer devices as follows. EX1003, ¶¶122-125.

First, a POSITA would have been motivated to implement Lee’s memory hub based on Tsern’s teachings of similarly situated buffer devices because doing so is a mere implementation detail for a feature—the implementation of a memory hub—that that is not described in detail by Lee. EX1003, ¶123; *see KSR*, 550 U.S. at 421 (“A person of ordinary skill is also a person of ordinary creativity, not an automaton.”). Both Lee’s memory hub and Tsern’s buffer device receive a first set of parallel data from multiple memory devices along multiple bus systems, and transmits that received data as a second set of parallel data along a single bus to a

controller. *See* [1b]-[1d] of Ground 1A. Given this similarity, a POSITA would have looked to Tsern for implementation details. EX1003, ¶123.

Second, this implementation is merely the application of known techniques (*e.g.*, a specific implementation of a memory hub that converts a received set of parallel data to a transmitted set of parallel data) to a known structure (*e.g.*, the memory hub in Lee's memory system) to yield predictable results (*e.g.*, a memory hub implementing elements enabling conversion of a received set of parallel data to a transmitted set of parallel data). EX1003, ¶124; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success in pursuing this implementation because memory system technology is predictable, and because the location and functionality of the buffer devices in Tsern's memory system is generally consistent with that of the memory hub in Lee's memory system. *See* EX1004, [0009], [0015]-[0020], FIG. 2; EX1005, Figs. 11, 18, 36; EX1003, ¶125.

Motivation for implementation of the memory hub as an IC

A POSITA would have been motivated to implement the memory hub as an IC as follows. EX1003, ¶¶126-131.

First, implementing a memory hub of a memory cell array system as an IC was conventional, and compatible with conventional processes and structures. EX1003, ¶127 (citing EX1009, 1; EX1016, 6:53-54, Fig. 18).

Second, implementation of a memory hub as an IC is smaller, more efficient, and less expensive than implementation of the memory hub functionality through a circuit composed of discrete components. *See* EX1022, 1:15-18; EX1003, ¶128.

Third, implementing the combination memory hub as an IC is a mere implementation detail for a feature—the specific nature of the memory hub—that that is not specified by Lee. EX1003, ¶129; *see KSR*, 550 U.S. at 421.

Fourth, this implementation is merely the application of known techniques (implementation of a memory hub as an IC) to a known structure (the combination memory hub) to yield predictable results (an IC memory hub). EX1003, ¶130; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success in implementing the memory hub as an IC because this was a conventional approach to implementation of memory hubs. *See* EX1009, 1; EX1016, 6:53-54; EX1003, ¶131.

4. Analysis

(a) Claim 1

[1pre]-[1c]

See [1pre]-[1c] of Ground 1A. EX1003, ¶133.

[1d]

The Lee-Chang-Tsern system includes *a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the*

first transmission bus, and has *a first set of parallel data of the first transmission bus* and *a second set of parallel data on the second transmission bus*. See [1d] of Ground 1A; EX1003, ¶134.

Tsern's buffer device 100a renders obvious parallel-to-parallel conversion

In one example, the combination memory hub (*logic unit*) is implemented based on Tsern's buffer device 100a. EX1003, ¶135.

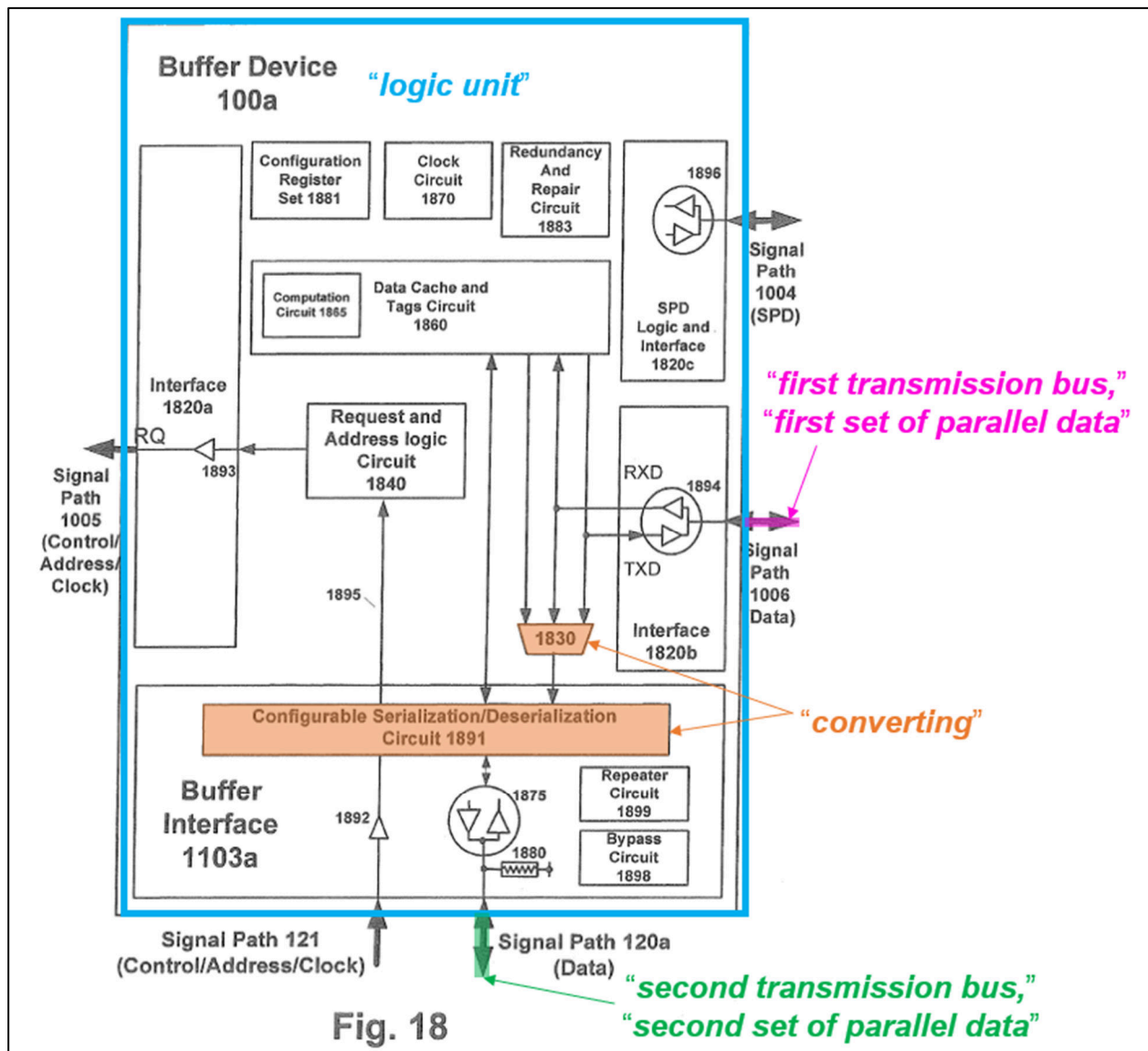
In Tsern, data are communicated between the buffer device and a memory controller via a signal path 120a. See EX1005, 12, 14-15. The "buffer interface 1103a has a programmable width for signal path 120a." *Id.*, 38. Based on this disclosure, a POSITA would have understood that the signal path 120a carries *parallel data*, *i.e.*, data of width greater than one bit. EX1003, ¶136.

Also in Tsern, data are communicated between buffer device 100a and memory devices via "signal paths 1006." EX1005, 38. The interface 1820b, which connects to the signal paths 1006 (*see* Fig. 18), "may be programmed to connect to 16 'x4' width memory devices, 8 'x8' width memory devices or 4 'x16' width memory devices." *Id.*, 37. Based on this disclosure, a POSITA would have understood that each signal path 1006 carries *parallel data*, *e.g.*, 4-, 8-, or 16-bit width data from those memory devices. EX1003, ¶137.

Tsern's buffer device 100a *converts* the parallel data from the multiple signal paths 1006 to parallel data for the single signal path 120a through a

“configurable serialization/deserialization circuit 1891,” which “performs serialization and deserialization functions,” and through a “multiplexer 1830,” which “utilizes the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.” EX1005, 33, 38; EX1003, ¶138.

In the combination, illustrated *infra*, the memory hub (*logic unit*) is implemented based on the parallel-to-parallel capability of Tsern’s buffer device 100a. EX1003, ¶139. Specifically, the combination memory hub communicates a *first set of parallel data* to/from memory devices via bus systems 76, 82, 90, 94 (pink), and communicates a *second set of parallel data* to/from a memory controller via high-speed bus 58 (green). *See* [19c]-[19d] of Ground 1A; EX1003, ¶139. Elements of the combination memory hub, including a configurable serialization/deserialization circuit 1891 and a multiplexer 1830 (orange *infra*), *convert the first set of parallel data into a second set of parallel data*, consistent with their operation as disclosed by Tsern, discussed *supra*. EX1003, ¶140.



Lee-Chang-Tsern figure based on Tsern, Fig. 18

Tsern's buffer device 3600 renders obvious parallel-to-parallel conversion

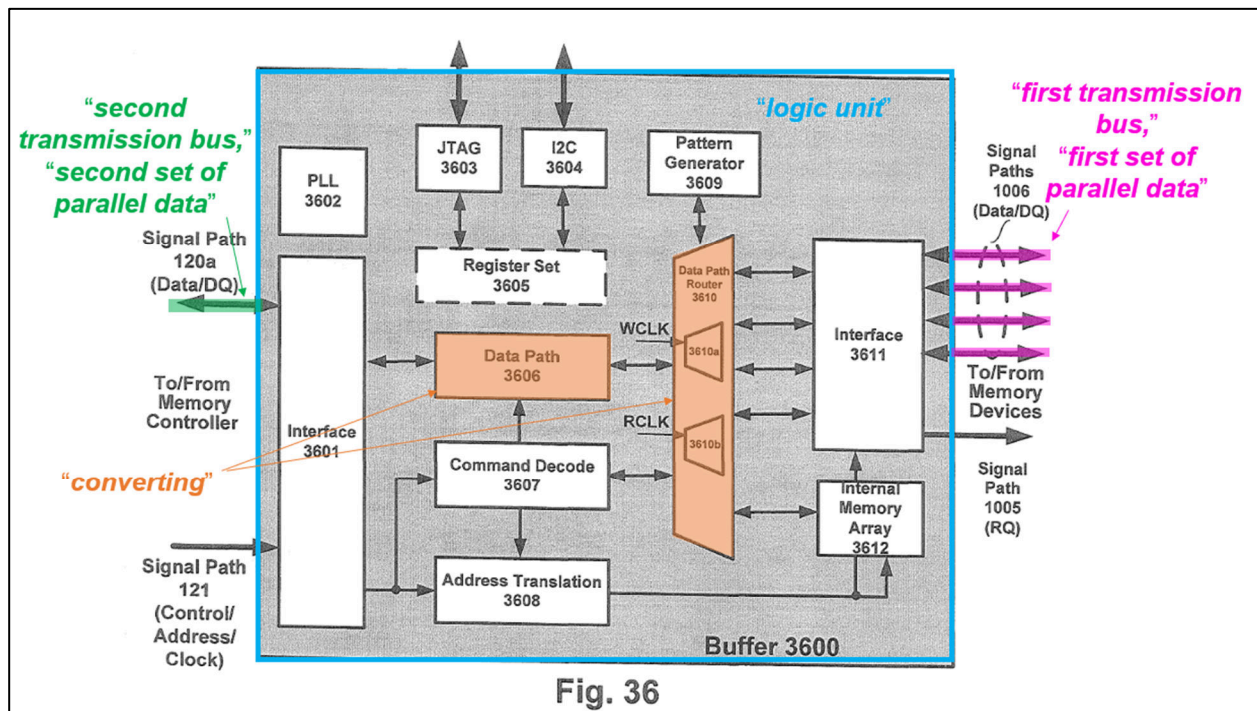
In alternative/additional example, the combination memory hub (*logic unit*) is implemented based on Tsern's buffer device 3600. EX1003, ¶141.

In Tsern, data are communicated between the buffer device and a memory controller via a signal path 120a, which carries *parallel data*, discussed *supra*.

Data are also communicated between the buffer device 3600 and memory devices via “signal paths 1006,” each of which carries *parallel data*, discussed *supra*. EX1005, 68; EX1003, ¶142.

Tsern’s buffer device 3600 *converts* the parallel data from the multiple signal paths 1006 to parallel data output through interface 3601 onto the single signal path 120a through a “data path 3606 and data path router 3610,” which “merge separate read data from more than one memory device into a single merged read data or read stream output at interface 3601.” EX1005, 36; EX1003, ¶143.

In the combination, illustrated *infra*, the memory hub (*logic unit*) is implemented based on the parallel-to-parallel capability of Tsern’s buffer device 3600. EX1003, ¶144. Specifically, the combination memory hub communicates a *first set of parallel data* to/from memory devices via bus systems 76, 82, 90, 94, and communicates a *second set of parallel data* to/from a memory controller via high-speed bus 58 (green). *See* [19c]-[19d] of Ground 1A. Elements of the combination memory hub, including “data path 3606 and data path router 3610” (orange *infra*), *convert* (“merge”) *the first set of parallel data into a second set of parallel data*, consistent with their operation as disclosed by Tsern, discussed *supra*. EX1005, 68; EX1003, ¶¶144-145.



Lee-Chang-Tsern figure based on Tsern, Fig. 36

(b) Claim 2

[2a]-[2b]

See [2a]-[2b] of Ground 1A; EX1003, ¶146.

(c) Claim 4

[4]

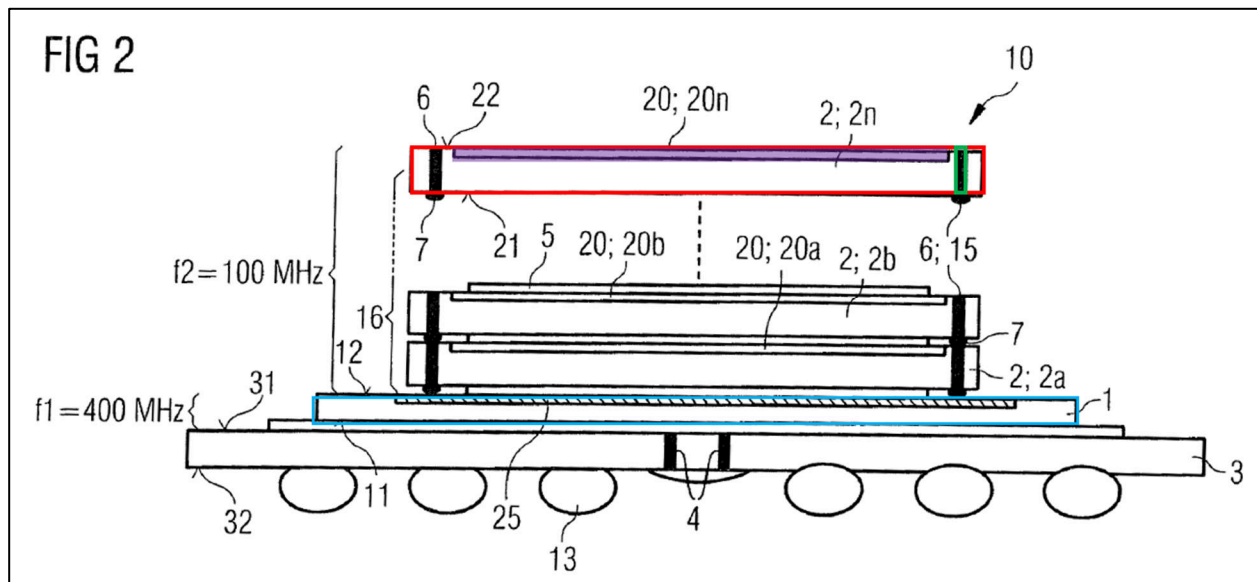
See [4] of Ground 1A; EX1003, ¶147.

C. GROUND 1C: Claims 5 and 13-14 Are Obvious Over Lee-Chang-Tsern-RaghuRam

1. RaghuRam

RaghuRam describes “a semiconductor product” in which “second semiconductor chips 2,” red in FIG. 2, *infra*, are “stacked on one another and on

the first semiconductor chip 1 [blue]” and connected by “through-hole fillings 6 [green] and bond balls 7.” EX1011, [0088]. The second semiconductor chips “each comprise at least one memory bank” 20, *e.g.*, a DRAM memory bank, that “extend[s] over the entire top main surface 22 of the respective semiconductor chip 2.” *Id.*, [0089], [0091]. “The integrated circuit of the first semiconductor chip 1 essentially is formed of a input/output circuitry.” *Id.*, [0036], [0085]; EX1003, ¶148.

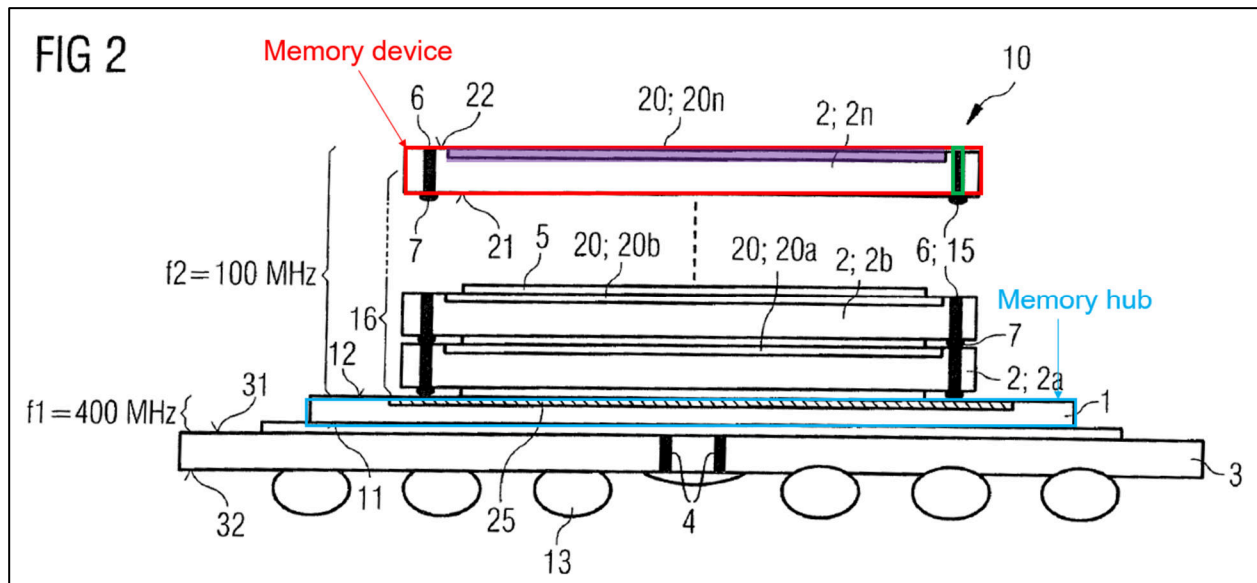


RaghuRam, FIG. 2 (annotated)

RaghuRam is analogous art to the '834 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '834 Patent was trying to solve. *See* EX1001, 1:28-33; EX1011, Abstract, [0007]; EX1003, ¶¶149-150.

2. The Lee-Chang-Tsern-RaghuRam Combination

In the combination, memory banks are “provided at top main surfaces 22 of” the memory devices 70, which are “stacked on one another and on the first semiconductor chip 1,” *i.e.*, on the memory hub, *e.g.*, illustrated *infra*. EX1011, [0088]-[0089]. The chips are connected by “through-hole fillings 6 and bond balls 7.” EX1011, [0088], [0091]; EX1003, ¶151.



Lee-Chang-Tsern-RaghuRam figure based on RaghuRam, FIG. 2

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to stack the memory devices and memory hub because (1) a stacked arrangement of chips provides “an increased storage capacity” (EX1011, [0007]; *see* EX1009, 1); (2) RaghuRam’s stacked arrangement has “an increased number of memory cells without any increase of the load capacitance and parasitic electrical influences” (EX1011, [0007]); (3)

RaghuRam's stacked arrangement advantageously is "operable at higher frequencies than conventional memory chips without the need to reduce the clock frequency" EX1011, [0007]; (4) by connecting the stacked chips with through-hole fillings, "no bond wires are required," reducing package size and complexity (EX1011, [0088]); (5) arranging the memory device and memory hub chips based on RaghuRam is a mere implementation detail for a feature—the physical arrangement of the chips—that is not specified by Lee (*see KSR*, 550 U.S. at 421); and (6) it is merely the application of known techniques (stacked chips in a memory module) to a known structure (Lee's memory device and memory hub chips) to yield predictable results (a memory module in which memory chips are stacked above a memory hub chip). EX1003, ¶¶152-158; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because memory system technology is predictable and because a stacked package of memory and logic chips was conventional. *See, e.g.*, EX1005, Fig. 11; EX1009, 1; EX1016, Fig. 18; EX1003, ¶159.

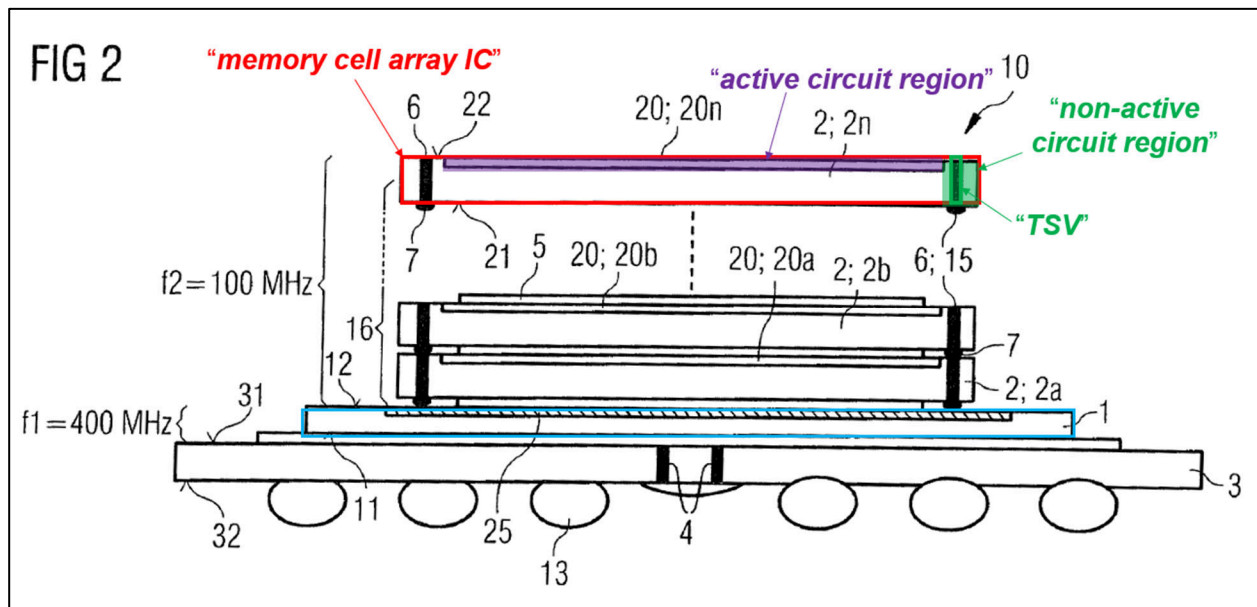
4. Analysis

(a) Claim 5

[5a]

In the combination, the memory hub 60 and one or more ranks of memory devices 70 are assembled into “a semiconductor product” based on RaghuRam. EX1011, [0088]; EX1003, ¶¶160-161. Specifically, memory banks are “provided at top main surfaces 22 of the second semiconductor chips 2” (*memory cell array ICs*), which are “stacked on one another and on the first semiconductor chip 1,” *i.e.*, on the memory hub (*logic unit*), *e.g.*, as illustrated in RaghuRam’s FIG. 2, *infra*. EX1011, [0088]-[0089]; EX1003, ¶161.

The chips are connected “by means of electrically conductive connecting means 15, which comprise through-hole fillings 6 and bond balls 7.” EX1011, [0088]. The through-hole fillings 6 (green) correspond to *at least one TSV*. EX1003, ¶162.



RaghuRam, FIG. 2 (annotated)

Based on RaghuRam, "the memory banks [20] essentially extend over the entire top main surface 22 of the respective second semiconductor chip 2." EX1011, [0091]. The "portion of the upper main surface covered with the memory bank 20," purple *supra*, corresponds to *an active circuit region of a memory cell array IC*, e.g., because it contains the memory circuitry. *Id.*; EX1003, ¶163.

The "electrical contacts" (*TSV*) are "arranged" "[i]n the remaining portion of the main surface" that is not "covered with the memory bank." EX1011, [0091]. This remaining portion, green *supra*, corresponds to *a non-active circuit region of a memory cell array IC*, e.g., because it is the region of the chip that does not contain memory circuitry. EX1003, ¶164. The non-active circuit region *surrounds* the active circuit region, e.g., as illustrated in FIG. 2. *Id.*; see EX1011,

[0091] (“the portion of the upper main surface covered with the memory bank 20 may be more than 85%, preferably more than 90% and more preferably more than 95% of the entire upper main surface 22. In the remaining portion of the main surface only electrical contacts to be contacted by the conductive connecting means 15 need to be arranged”); EX1003, ¶164.

[5b]

The “portion of the upper main surface covered with the memory bank 20” (*active circuit region of a memory cell array IC* contains the memory bank, which “includ[es] a plurality of memory cells” (*active devices*), *i.e., is used for forming at least one active device*. EX1011, [0008], [0091]; EX1003, ¶165.

(b) Claim 13

[13]

The width of the non-active circuit region is a straightforward design choice. For instance, a non-active circuit region “width less than about 50 um” presents no unexpected results or solution, and was conventional. EX1003, ¶166 (citing EX1023, [0022]); *see In re Kuhle*, 526 F.2d 553, 555 (CCPA 1975); *In re Chu*, 66 F.3d 292, 298-99 (Fed. Cir. 1995).

(c) **Claim 14**

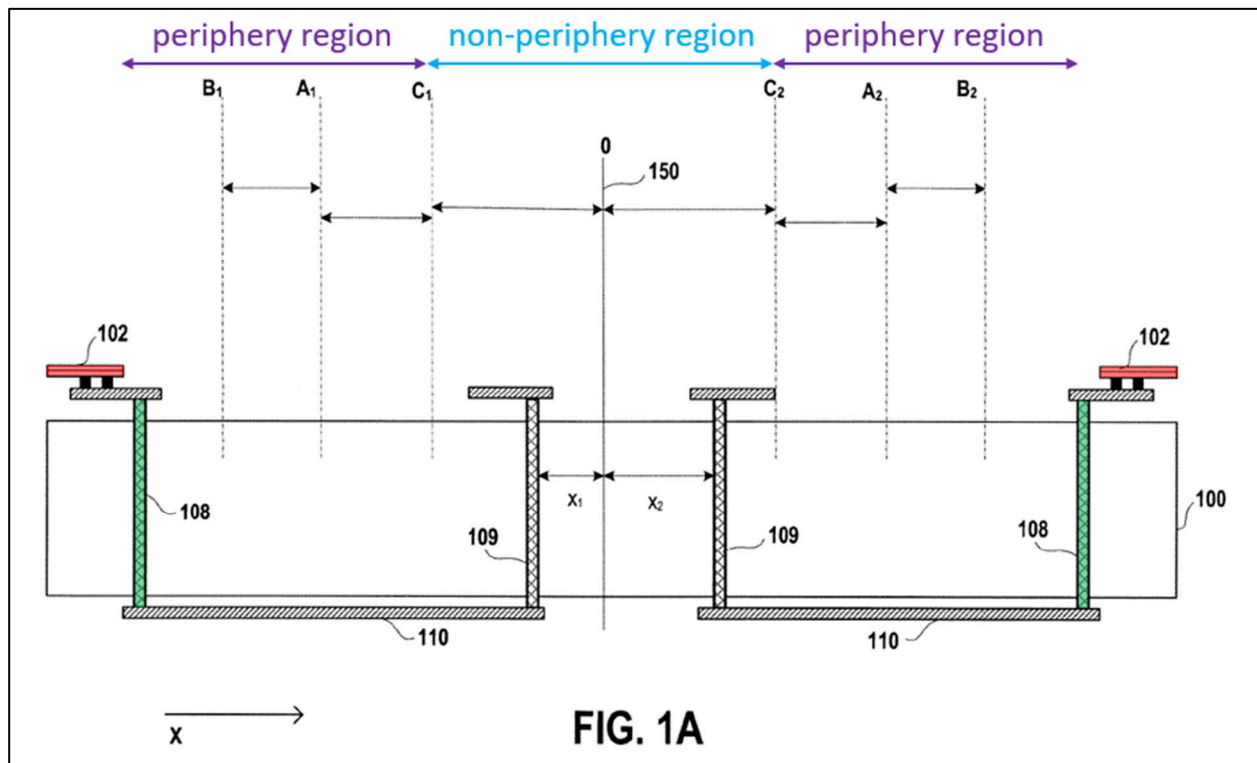
[14]

The TSV width is a straightforward design choice. For instance, a TSV “width less than about 20 um” presents no unexpected results or solution, and was conventional. EX1003, ¶167 (citing EX1024, [0018]); *see Kuhle*, 526 F.2d at 555; *Chu*, 66 F.3d at 298-99.

D. GROUND 1D: Claims 6-8 and 18-19 Are Obvious Over Lee-Chang-Tsern-White

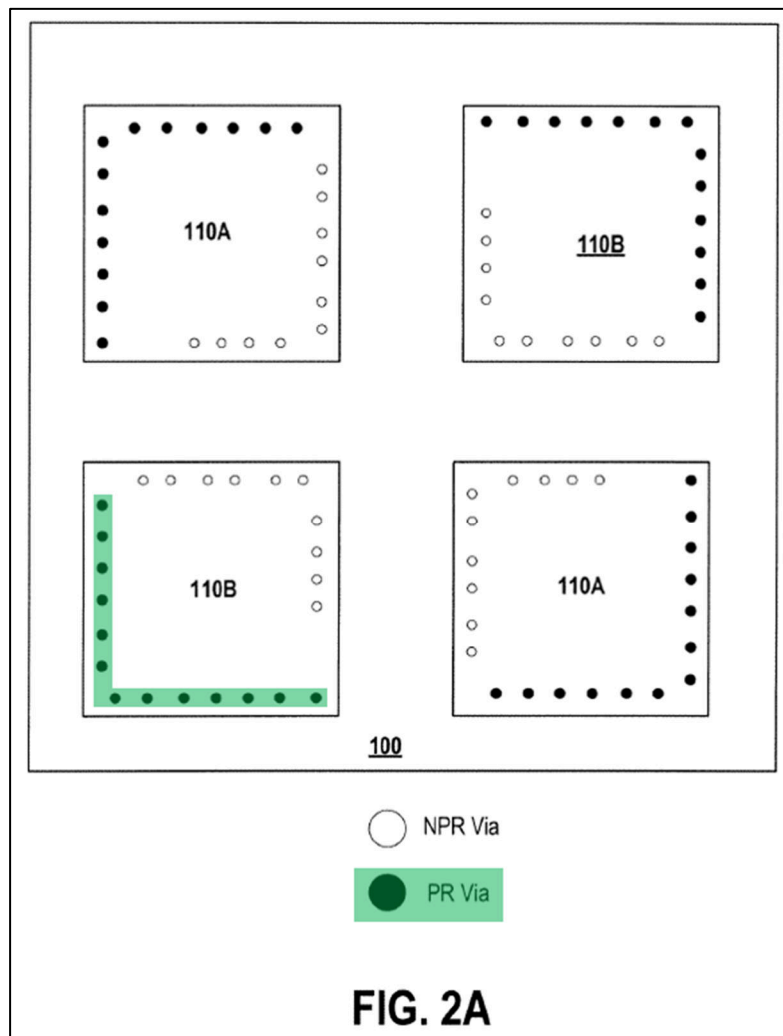
1. White

White describes an “integrated circuit with distributed power using through-silicon vias (TSVs).” EX1014, Abstract. White’s IC has a “non-periphery region ... where the active device processing occurs,” and a surrounding “periphery region.” EX1014, 3:26-30; *see* 3:29-44. TSVs (green in FIG. 1A, *infra*) “route power and ground from the bonding pads 102 [red], to the non-periphery region.” *Id.*, 3:48-49; EX1003, ¶¶168-169.



White, FIG. 1A (annotated)

As illustrated in the bottom view of White's FIG. 2A, *infra*, "TSVs in the periphery region [PR]," some of which are highlighted in green, "provide ground to the ground conductive areas 110A and power to the power conductive areas 110B." EX1014, 4:48-61; EX1003, ¶170.



White, FIG. 2A (annotated)

White is analogous art to the '834 Patent: it is reasonably pertinent to the problem the '834 Patent was trying to solve. *See* EX1001, 1:28-33; EX1014, 2:5-7; EX1003, ¶171.

2. The Lee-Chang-Tsern-White Combination

In the combination, the memory hub and the memory device ICs have peripheral TSVs “route power and ground from [] bonding pads 102, to the non-

periphery region,” *e.g.*, to the active circuit region containing the logic circuitry or memory circuitry), based on White. EX1014, 3:48-49; EX1003, ¶172.

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to implement peripheral TSVs in the combination ICs because (1) TSVs allow the chips to be stacked, providing benefits such as increased system speed, lower costs, and better integration (*see* EX1013, [0003]-[0004]); (2) power distribution through TSVs “reduces the effect of resistive voltage drops on a conducting line” (EX1014, 4:16-29); (3) using TSVs to connect to power/ground was conventional (*see* EX1014, 3:1-2; EX1025, [0025]); and (4) it is merely the application of known techniques (TSVs in ICs) to a known structure (the memory hub and memory device ICs of the combination) to yield predictable results (memory hub and memory device ICs implemented with TSVs). EX1003, ¶173-177; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success in pursuing this implementation because IC structure is predictable and because implementation of TSVs in ICs, and uses of TSVs for connection to power/ground, was conventional, in both memory and logic chips. *See* EX1014, 3:1-2; EX1025, [0025]; EX1003, ¶178.

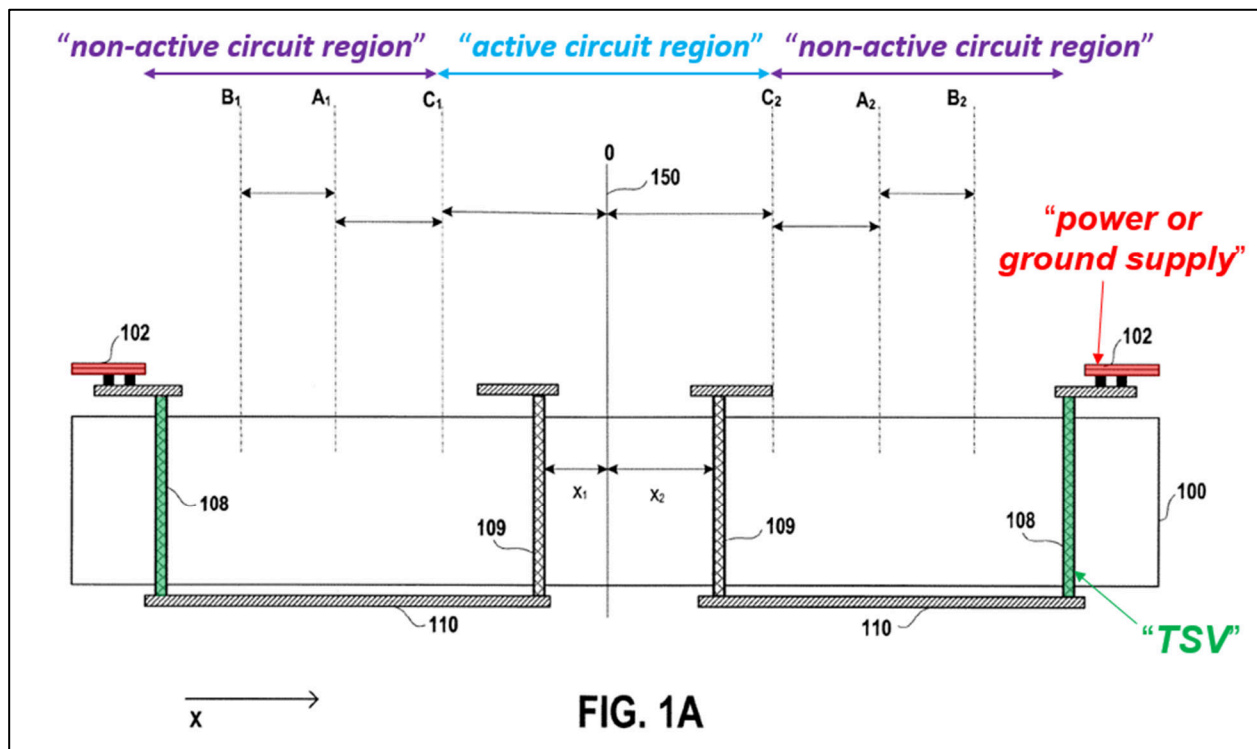
4. Analysis

(a) Claim 6

[6a]

In the combination, the memory hub (*logic unit*) has “a periphery region (PR) and a non-periphery region (NPR).” EX1014, 3:26-28; EX1003, ¶¶179-180.

The non-periphery region (blue in FIG. 1A, *infra*) “is the interior area where the active device processing occurs,” *e.g.*, corresponds to *an active circuit region used for forming at least one active device of the logic unit*. EX1014, 3:28-30; *see* 1:56-57, 3:31-36, 4:1-3, 4:27-29, claims 1 and 9, 4:13-15, 4:37-40, 4:61-62, 5:41-42, 5:53-55, 5:61-64; EX1003, ¶181.



White, FIG. 1A (annotated)

The periphery region (purple) “is defined from the bonding pad 102 area [red] to the boundary of the non-periphery region,” *i.e.*, outside of the area where active device processing occurs, and corresponds to a ***non-active circuit region surrounding/partially surrounding the active circuit region*** (the non-periphery region). EX1014, 3:37-38; *see* 3:38-41; EX1003, ¶182.

Based on White, “through-silicon-vias 108,” green, are “formed within the periphery region of the IC chip” (***at least one TSV exists within the non-active circuit region***). EX1014, 3:48-50; *see* Abstract, 1:48-50, 1:62-63, 4:31-32, 4:58-60, 6:38-40, claim 1; EX1003, ¶183.

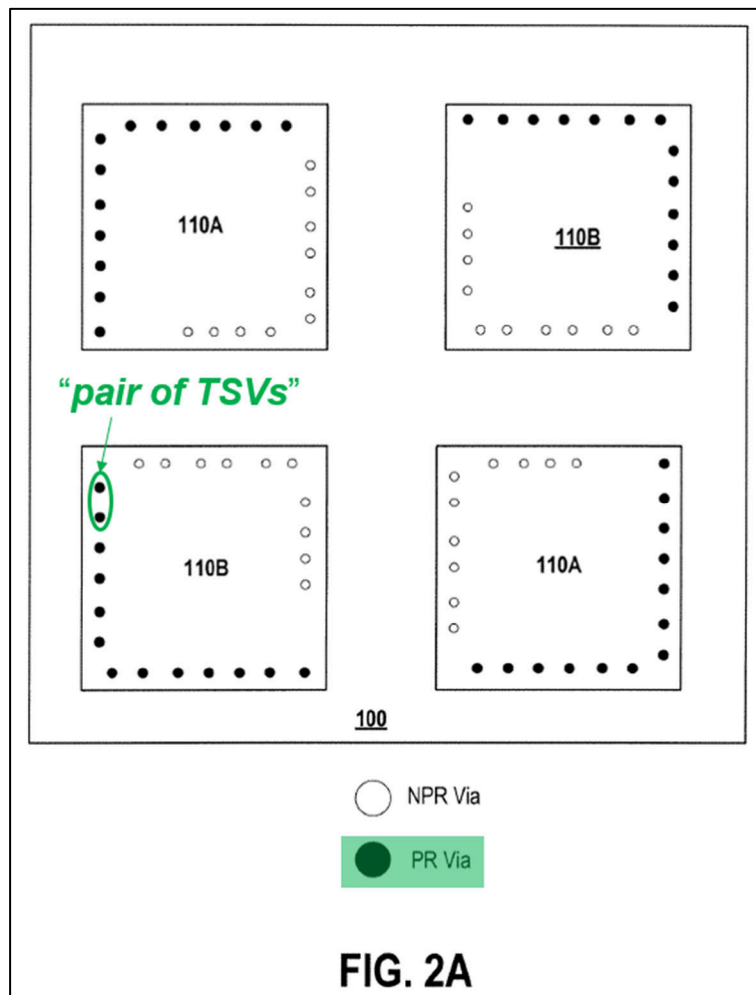
[6b]

The combination TSVs “route power and ground from the bonding pads 102, to the non-periphery region.” EX1014, 3:48-50; *see* 2:57-58. The bonding pads (red in FIG. 1A, *infra*) “provide power and ground” and thus correspond to a ***power or ground supply***. EX1014, 3:17-19; *see* Abstract, 1:46-48, 3:64-66. The peripheral TSVs (green) are connected to the bonding pads, *i.e.*, ***used for connecting to the power/ground supply***. *See id.*, FIG. 1A, 1:38-40, 1:53-56, 4:17-21, 2:57-58, 3:7-8, 3:47-50, 4:24-26, 4:37-46, 4:58-63, 5:38-45, 5:65-67, 6:24-26, 6:49-64, claim 1, claim 9; EX1003, ¶184.

(b) **Claim 7**

[7a]

In the combination, based on White, each memory device (*memory cell array IC*) includes *at least one TSV* (e.g., TSVs 108) *within a non-active circuit region surrounding or partially surrounding an active circuit region*, where the TSVs are *used for connecting to power/ground*. See [6a], *supra*; EX1014, FIG. 1A, 3:26-55. The “TSVs in the peripheral region [PR]” are arranged based on White’s FIG. 2A, *infra*, e.g., providing *at least one pair of TSVs*. EX1014, 4:58-60; EX1003, ¶¶185-186.



White, FIG. 2A (annotated)

The TSVs of the pair are *neighboring*, *e.g.*, because they are adjacent and non-overlapping. EX1003, ¶187. To the extent that PO argues that neighboring TSVs implies a specified separation distance, *e.g.*, less than 10-30 μm (*see* EX1001, 12:49-51), such a distance is a straightforward design choice because it presents no unexpected results or solution. EX1003, ¶187; *see Kuhle*, 526 F.2d at 555; *Chu*, 66 F.3d at 298-99.

[7b]

The highlighted pair of TSVs in FIG. 2A, *supra*, “provide[s] ... power to the power conductive areas 110B,” and pairs of TSVs in the conductive areas 110A “provide ground to the ground conductive areas 110A,” *e.g.*, by coupling to conductive bondpads (*the at least one pair of TSVs are used for connecting to a power or a ground supply*). EX1014, 4:58-65; *see* [6b]; EX1003, ¶188.

(c) **Claim 8**

[8a]-[8b]

In the combination, based on White, in the memory hub (*logic unit*), a *pair of TSVs exist in neighboring within a non-active circuit region surrounding or partially surrounding an active circuit region*, where the TSVs are *used for connecting to power/ground*. *See* [7a]-[7b], *supra*; EX1014, 3:26-55, 4:48-65, FIGS. 1A, 2B; EX1003, ¶189.

(d) **Claim 18**

[18]

See [13]; EX1003, ¶190.

(e) **Claim 19**

[19]

See [14]; EX1003, ¶191.

**E. GROUND 1E: Claim 9 Is Obvious Over Lee-Chang-Dozen
or Lee-Chang-Tsern-Dozen**

1. Dozen

Dozen describes manufacturing memory devices, *e.g.*, DRAM, SRAM, or flash memory. *See* EX1007, Abstract, 4:9-26. Dozen describes that “where a plurality of semiconductor devices are included in the element substrate 1102, the plurality of semiconductor devices may be obtained by dividing the element substrate and the sealing layers,” *e.g.*, by “laser cutting.” EX1007, 11:60-67; EX1003, ¶192.

Dozen is analogous art to the ’834 Patent: it is reasonably pertinent to the problem the ’834 Patent was trying to solve. *See* EX1001, 1:28-33; EX1007, Abstract; EX1003, ¶193.

**2. The Lee-Chang-Dozen and Lee-Chang-Tsern-Dozen
Combinations**

In the combination, the memory devices are “formed in [an] element substrate,” and individual memory device chips are obtained from the substrate “by “laser cutting.” EX1007, 4:9-26, 11:60-67; EX1003, ¶194.

3. Motivation to Combine

A POSITA would have been motivated to employ laser dicing of the memory devices because (1) it enables high degrees of precision to be achieved at high processing speeds; (2) it is a contactless processing method, and thus does not

subject tools to wear, generates little waste, and does not run significant risks of contamination; (3) it is one of a finite number of predictable solutions (*e.g.*, laser dicing, physical dicing, scribing), and with a reasonable expectation of success (discussed *infra*); and (4) it is merely the application of known techniques (laser dicing of ICs) to a known structure (Lee's memory chips) to yield predictable results (memory chips separated by a laser dicing process). EX1003, ¶¶195-199 (citing EX1020, Abstract, 7:9-11; EX1021, 1:6-9, 1:22-32); *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because memory system technology and IC dicing technology are predictable, and because laser dicing of IC chips was conventional. *See, e.g.*, EX1020, Abstract; EX1021, 1:6-9; EX1003, ¶200.

4. Analysis

(a) Claim 9

[9]

In the combination, a substrate is divided into individual memory devices (*memory cell array ICs*) by “laser cutting” (*a dicing method comprises a laser cutting process*), based on Dozen. EX1007, 11:60-67; EX1003, ¶¶201-202.

F. GROUND 1F: Claim 10 Is Obvious Over Lee-Chang-Tsern-Dozen

1. Analysis

(a) Claim 10

[10]

In the combination, a substrate is divided into individual memory hub ICs (*logic unit*) by “laser cutting” (*a dicing method comprises a laser cutting process*), based on Dozen. EX1007, 11:60-67; EX1003, ¶¶203-204.

G. GROUND 1G: Claim 12 Is Obvious Over Lee-Chang-Tsern-RaghuRam-White

1. Analysis

(a) Claim 12

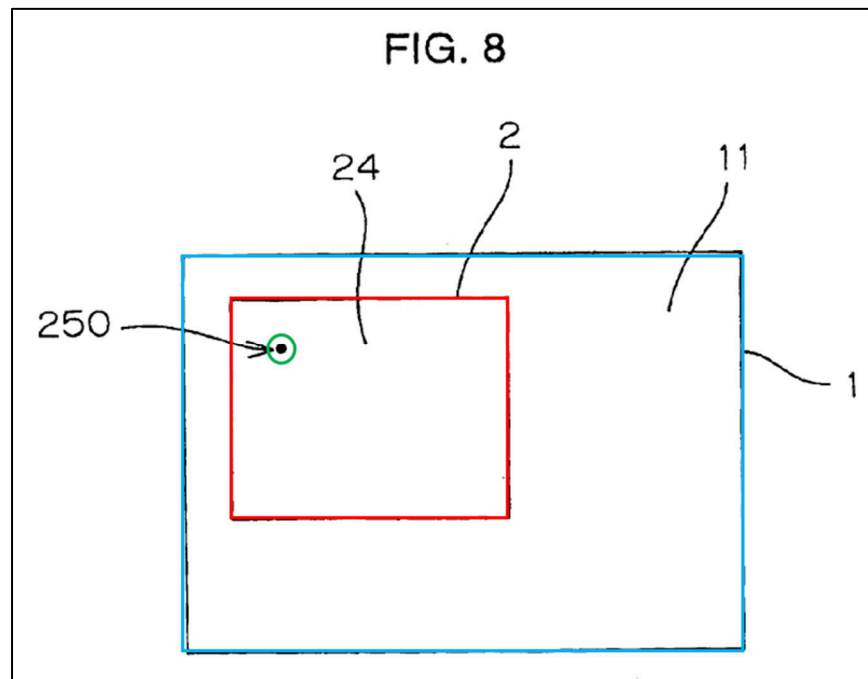
[12]

See [7b]; EX1003, ¶¶205-206.

H. GROUND 1H: Claims 15-16 Are Obvious Over Lee-Chang-Tsern-RaghuRam-Hikita

1. Hikita

Hikita describes a “chip-on-chip semiconductor device” including a primary chip 1 (blue in FIG. 8, *infra*) “in a stacked relation” with secondary chips 2 (red). EX1015, 12:33-52. A “back mark 250,” green, “on the back face 24 of the secondary chip” “allow[s] for recognition of the orientation of the secondary chip.” *Id.*, 14:28-34; EX1003, ¶207.



Hikita, FIG. 8 (annotated)

Hikita is analogous art to the '834 Patent: it is reasonably pertinent to the problem the '834 Patent was trying to solve. *See* EX1001, 1:28-33; EX1015, 1:61; EX1003, ¶208.

2. The Lee-Chang-Tsern-RaghuRam-Hikita Combination

In the combination, one or more of the ICs (*e.g.*, the memory device ICs and/or the memory hub) have a “back mark ... on the back face” of the chip to allow the orientation of the chip to be recognized when assembled into a stack with other chips. EX1015, 14:28-48; EX1003, ¶209.

3. Motivation to Combine and Expectation of Success

A POSITA would have been motivated to incorporate orientation marks into one or more of the ICs because (1) in the context of stacked chips (as is the case for the Lee-Chang-Tsern-RaghuRam combination; *see* Ground 1C), orientation marks allow chip orientation to be recognized, ensuring proper assembly of the chip stack (*see* EX1015, 14:38-42); (2) with such marks, “the positioning of the semiconductor chips is easy,” and thus assembly time “can be reduced” (EX1015, 3:12-14); and (3) it is merely the application of known techniques (orientation marks in ICs) to a known structure (the stacked chips of the combination system) to yield predictable results (memory hub and memory device ICs having orientation marks to facilitate stacking). EX1003, ¶¶210-212; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because IC structure is predictable and because orientation marks in ICs were conventional. EX1003, ¶213.

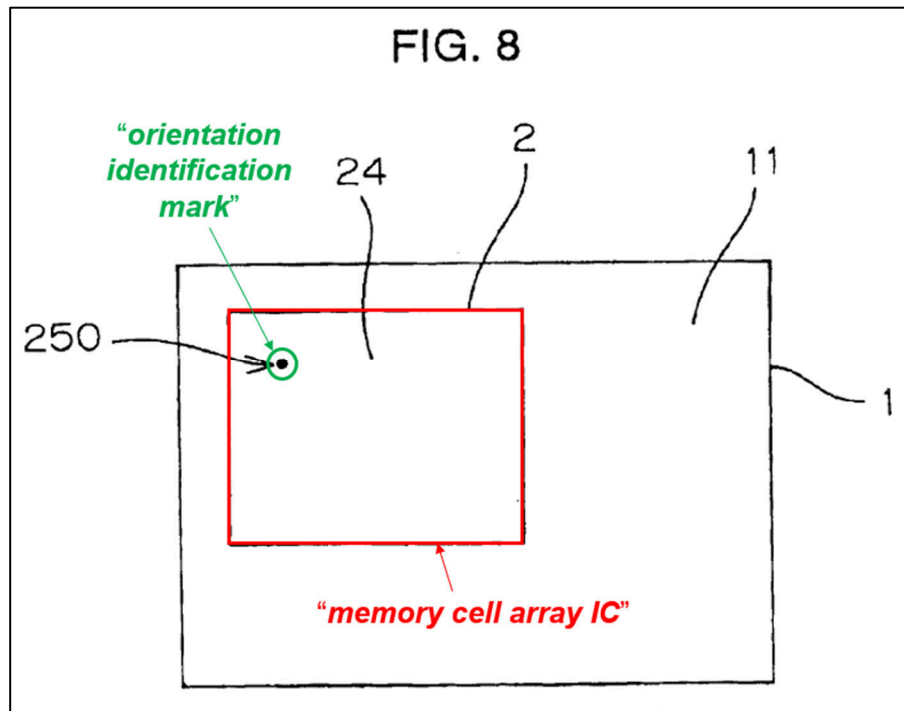
4. Analysis

(a) Claim 15

[15]

In the combination, a “back mark 250” (*orientation identification mark*) is “provided on the back face” of the memory cell array IC, to “allow[] for recognition of the orientation” of the IC. EX1015, 14:28-33; *see* 14:38-43, 15:44-

48, FIG. 10. As illustrated in FIG. 8, the back mark (*orientation identification mark*) is located in *a corner* of the IC. EX1003, ¶¶214-215.



Hikita, FIG. 8 (annotated)

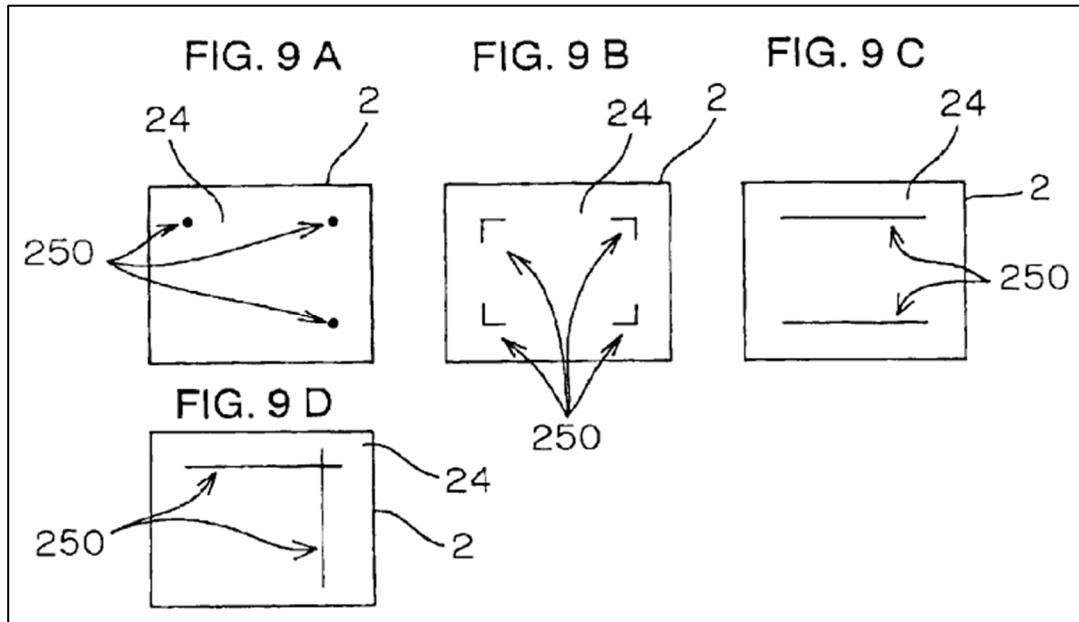
Based on Hikita, the back marks are formed “by a ... a laser process” (*formed by a process comprising Laser step*). EX1015, 15:2122; EX1003, ¶216.

(b) **Claim 16**

[16]

Based on Hikita, the back mark (*orientation identification mark*) can be a “point or circle,” a “hook- or L-shape,” a symbol such as “+” or “-,” a “line which extends along an edge,” or “crossed lines” (*a line of drawing, two lines of drawing*

..., or an arbitrary pattern). EX1015, 15:1-11; see FIGS. 8 and 9A-9D, *infra*;
EX1003, ¶217.



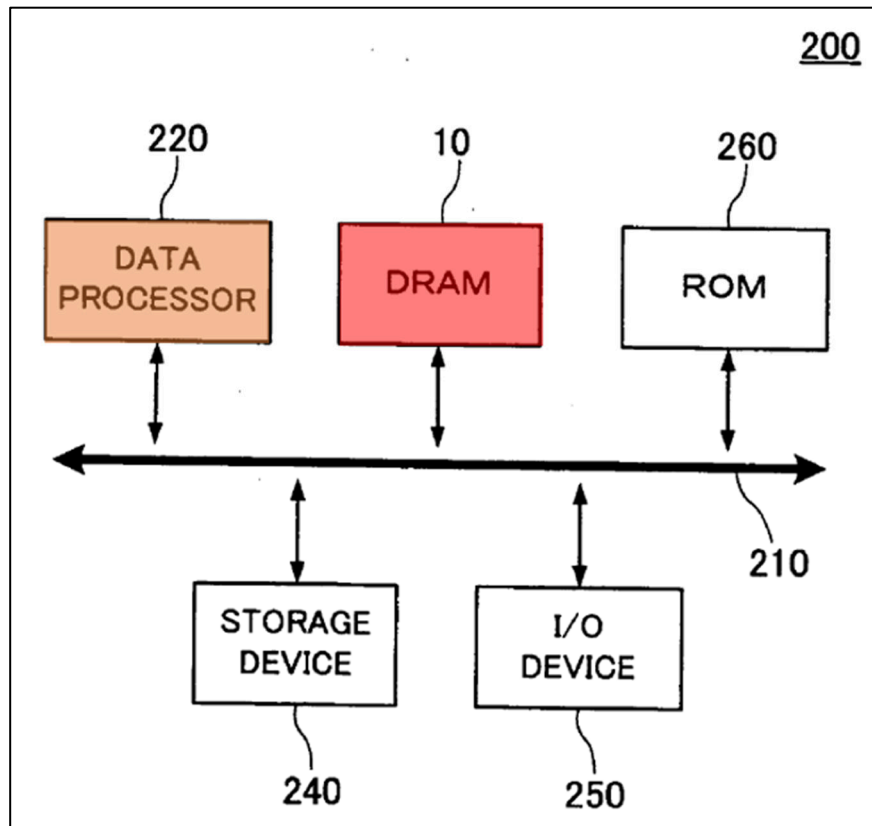
Hikita, FIGS. 9A-9D

I. GROUND 1I: Claims 21 and 23 Are Obvious Over Lee-Chang-Dono-Nakai

1. Dono

Dono describes a “data processing system” including “a data processor 220” (orange in FIG. 11, *infra*) and a “semiconductor device (DRAM) 10” (red) connected “via a system bus 210.” EX1008, [0100]. In Dono’s system—and as was conventional—the “internal operation voltage VPERI” of the DRAM cell is “lower than an external voltage VDD.” *Id.*, [0004]; see [0005]. To bridge these two different voltages, “DRAM processes the signal from the data processor 220

having the amplitude VDD by converting the signal to a low voltage signal of the internal operation voltage VPERI.” *Id.*, [0103]; EX1003, ¶218.



Dono, FIG. 11 (annotated)

This signal conversion is performed by a “level shifter” (*e.g.*, level shifter 93, green in FIG. 1, *infra*) that “reduce[s] the amplitude of the external signal to VPERI.” *Id.*, [0041]. In reverse, “[d]ata read from a memory cell of the DRAM 10 is converted to a signal having the amplitude VDD” using a “level shifter” (*e.g.*, level shifter 96, green). *Id.*, [0041], [0103]; EX1003, ¶219.

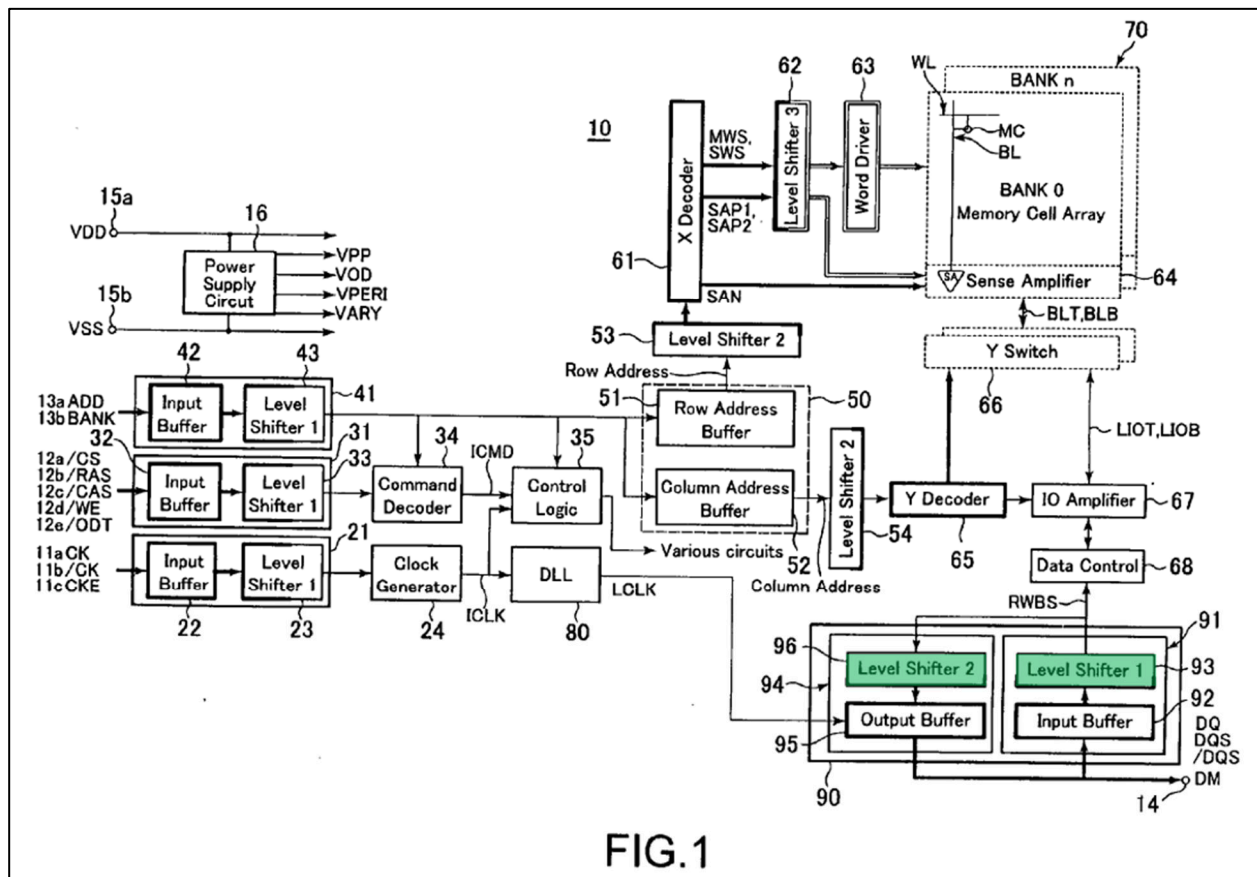


FIG. 1

Dono, FIG. 1 (annotated)

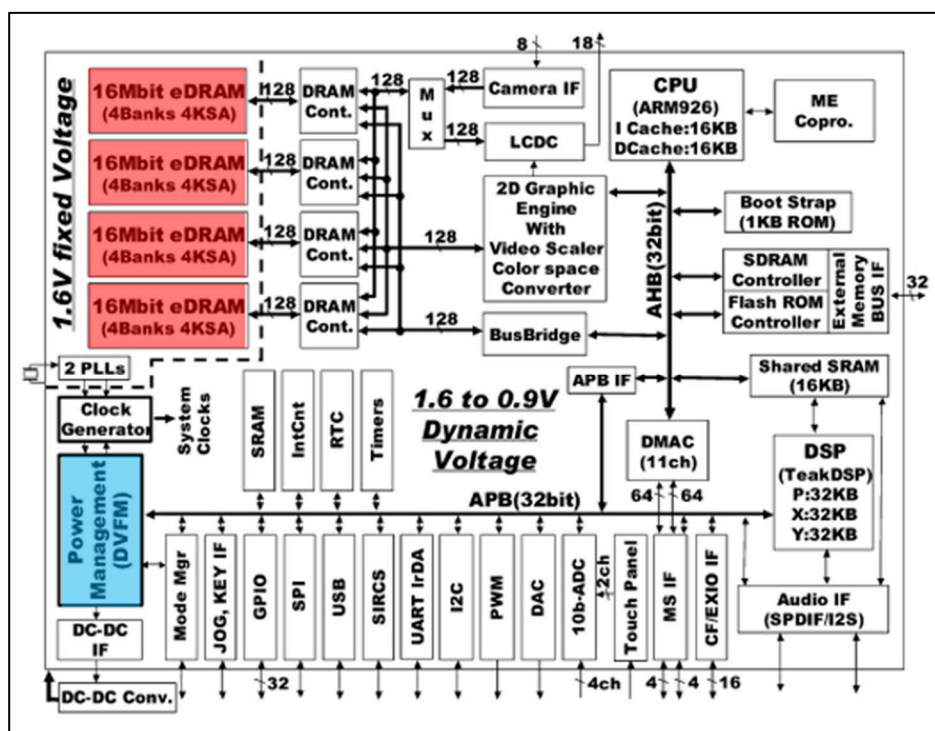
Dono is analogous art to the '834 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '834 Patent was trying to solve. *See* EX1001, 1:28-33; EX1008, [0024], [0100]; EX1003, ¶¶220-221.

2. Nakai

Nakai describes a “dynamic voltage and frequency management (DVFM) scheme” for “a microprocessor with ... embedded DRAM.” EX1017, 1. In Nakai’s system, “[c]lock frequency is autonomously and dynamically controlled

while supply voltage is adaptively controlled,” achieving significant “power reduction.” *Id.*; EX1003, ¶222.

Nakai’s system includes “four 128-bit data-width 16-Mb embedded DRAM macros,” red in Fig. 1, *infra*, with “processor blocks [] connected to the embedded DRAM by a 128-bit bus for high memory bandwidth requirements.” EX1017, 1. The system also includes a “DVFM block [blue], clock generator, and dc-dc IF block [that] control the supply voltage and clock frequency.” *Id.* The supply voltage of circuit blocks other than “the DRAM macros and phase-locked loops” is “controlled dynamically by the DVFM in the range between 0.9 and 1.6 V.” *Id.*, 2. In addition, while “all other circuit blocks [other than peripheral circuit blocks] are driven by the dynamically controlled system clock.” *Id.*; EX1003, ¶223.



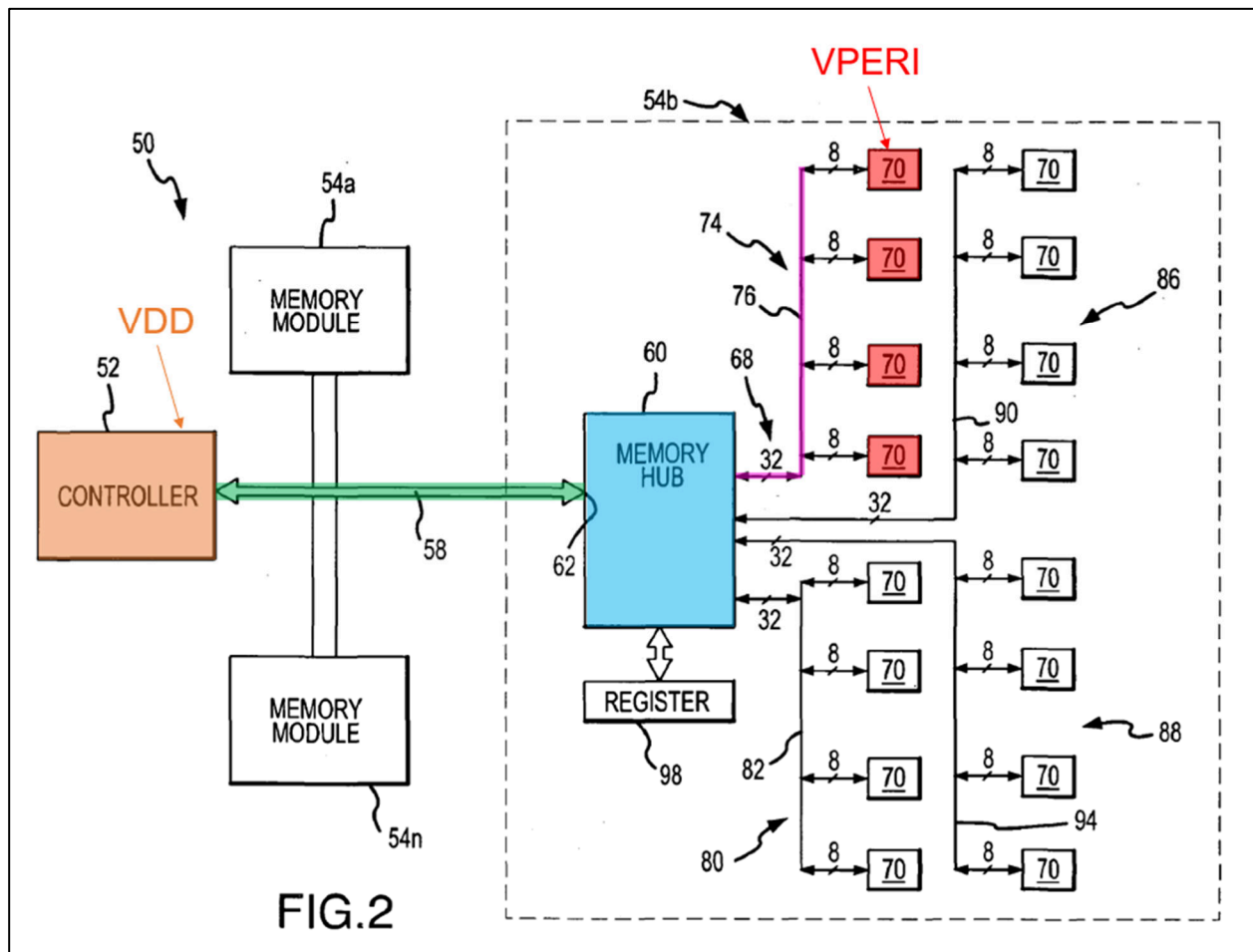
Nakai, Fig. 1 (annotated)

The dynamic frequency control (DFC) “controls the clock frequency at the required minimum value autonomously in hardware without special power-management software.” EX1017, 4. Generally, the activity of “embedded DRAM, bus, and CPU” is used “to determine the required minimum clock frequency,” and at the end of each period, the clock frequency of the next period is increased or decreased as needed based on the monitored activity. *Id.*, 4-5; *see* Fig. 9. Also, “[t]he clock frequency may [] be set directly via software to allow abrupt performance change in response to external events.” *Id.*; EX1003, ¶224.

Nakai is analogous art to the '834 Patent: it is from the same field of endeavor and is reasonably pertinent to the problem the '834 Patent was trying to solve. *See* EX1001, 1:28-33; EX1017, Abstract; EX1003, ¶¶225-226.

3. The Lee-Chang-Dono-Nakai Combination

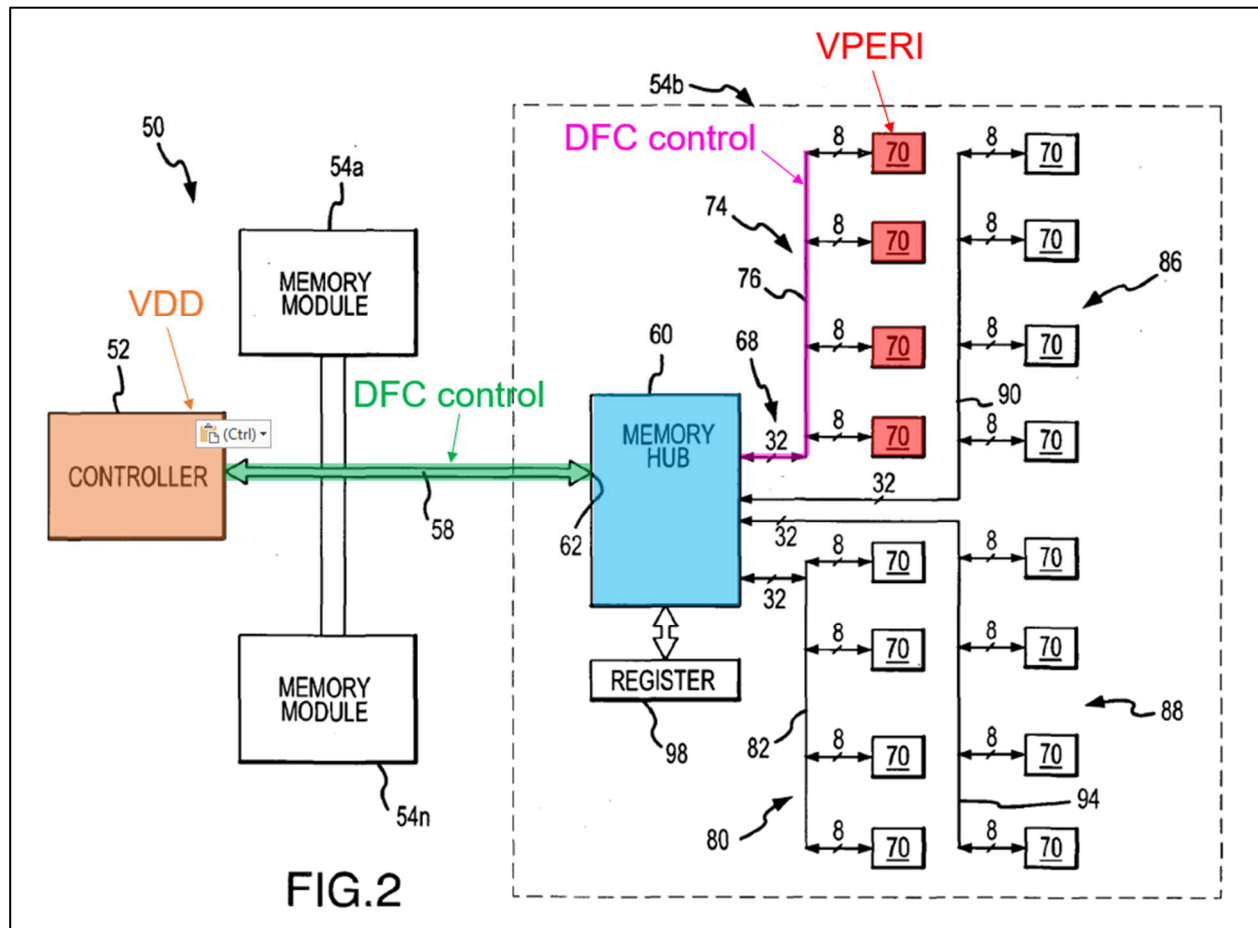
In the combination, the memory devices 70 (*e.g.*, DRAM devices) of Lee's system have an "internal operation voltage VPERI" that is "lower than an external voltage VDD" of the memory controller (*e.g.*, system controller 52), illustrated *infra*. EX1008, [0004]; *see* EX1004, [0025], FIG. 5; EX1003, ¶227. For "input write data," a "level shifter ... reduce[s] the amplitude of the external signal [from VDD] to VPERI." EX1008, [0040]. For "output read data," a "level shifter ... increase[s] the amplitude VPERI of an internal signal to VDD." EX1008, [0004]; EX1003, ¶227.



Lee-Chang-Dono-Nakai figure based on Lee, FIG. 2

Optionally, dynamic frequency control is implemented on, *e.g.*, the high-speed link 58 and the memory module bus systems 76, 82, 90, 94, based on Nakai, to reduce power consumption. EX1003, ¶228. For instance, a “DFC block,” *e.g.*, implemented in the controller 52, controls the clock frequency ... autonomously in hardware” based on system activity, and adjusts the clock frequency on the high-speed link and memory module bus systems as appropriate. EX1017, 4; *see* 5, Figs. 8-9. Also, “[t]he clock frequency may also be set directly via software to

allow abrupt performance change in response to external events.” EX1017, 5;
EX1003, ¶228.



Lee-Chang-Dono-Nakai figure based on Lee, FIG. 2

4. Motivation to Combine and Expectation of Success

Motivation to implement lower voltage in the DRAM cells than in the memory controller

A POSITA would have been motivated to have the DRAM devices operate at a lower voltage than the memory controller as follows. EX1003, ¶¶229-232.

First, logic cells (*e.g.*, in the controller) operating at high voltage allows for higher power operation and faster performance; while the lower bit line voltage in the memory cells (*e.g.*, in the DRAM devices) enables better stability. EX1003, ¶230 (citing EX1022, 1:26-52, 2:3-20).

Second, DRAM operating at different voltage than logic transistors (*e.g.*, with bit line voltages lower than the voltage of the logic cells) was conventional. EX1003, ¶231 (citing EX1008, [0004]-[0005]; EX1022, 1:45-49).

Third, this implementation is merely the application of known techniques (DRAM operating at a different voltage than a memory controller) by a known system (the combination memory system) to yield predictable results (a memory system in which the DRAM cells operate at a different voltage than the memory controller). EX1003, ¶232; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success because memory system technology is predictable, and the relative DRAM and logic voltages of the combination was conventional. EX1003, ¶233 (citing EX1008, [0004]-[0005]; EX1022, 1:45-49). Moreover, a POSITA would have expected success because Dono's disclosure of the voltage relationship between DRAM and memory controller is in the context of a memory system, *e.g.*, relevant to Lee's system architecture. EX1003, ¶233.

Motivation to implement dynamic frequency control

A POSITA would have been motivated to implement dynamic frequency control in the combination memory system as follows. EX1003, ¶¶234-236.

First, a POSITA would have been motivated to implement dynamic frequency control based on Nakai because of the ability to achieve a reduction in power consumption. *See* EX1017, 2 (“our DVFM scheme is highly effective in realizing ultra-low power consumption”); EX1003, ¶235.

Second, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (frequency management in the context of a DRAM memory system) to a known structure (a memory system including DRAM memory chips and memory hub) to yield predictable results (a memory system in which clock frequency is dynamically controlled to reduce power consumption). EX1003, ¶236; *see KSR*, 550 U.S. at 417.

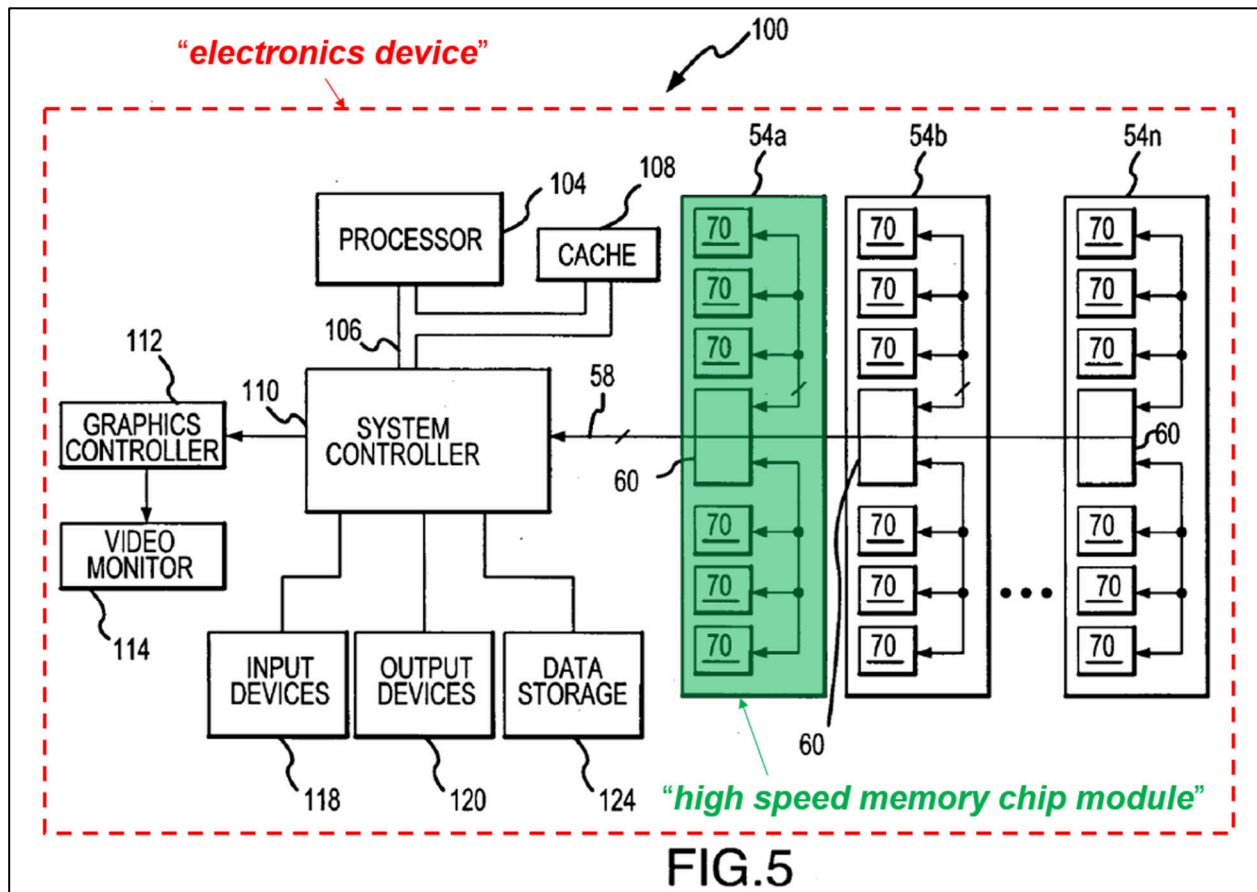
A POSITA would have expected success because memory system technology is predictable, and because Nakai’s disclosure of dynamic frequency control is in the context of a DRAM-based memory system, *e.g.*, relevant to the architecture of Lee’s system. EX1003, ¶237.

5. Analysis

(a) Claim 21

[21pre]

In the combination, Lee's "computer system 100" is an *electronics system device*. EX1004, [0023]; see FIG. 5 (*infra*), claim 28. EX1003, ¶¶238-239.



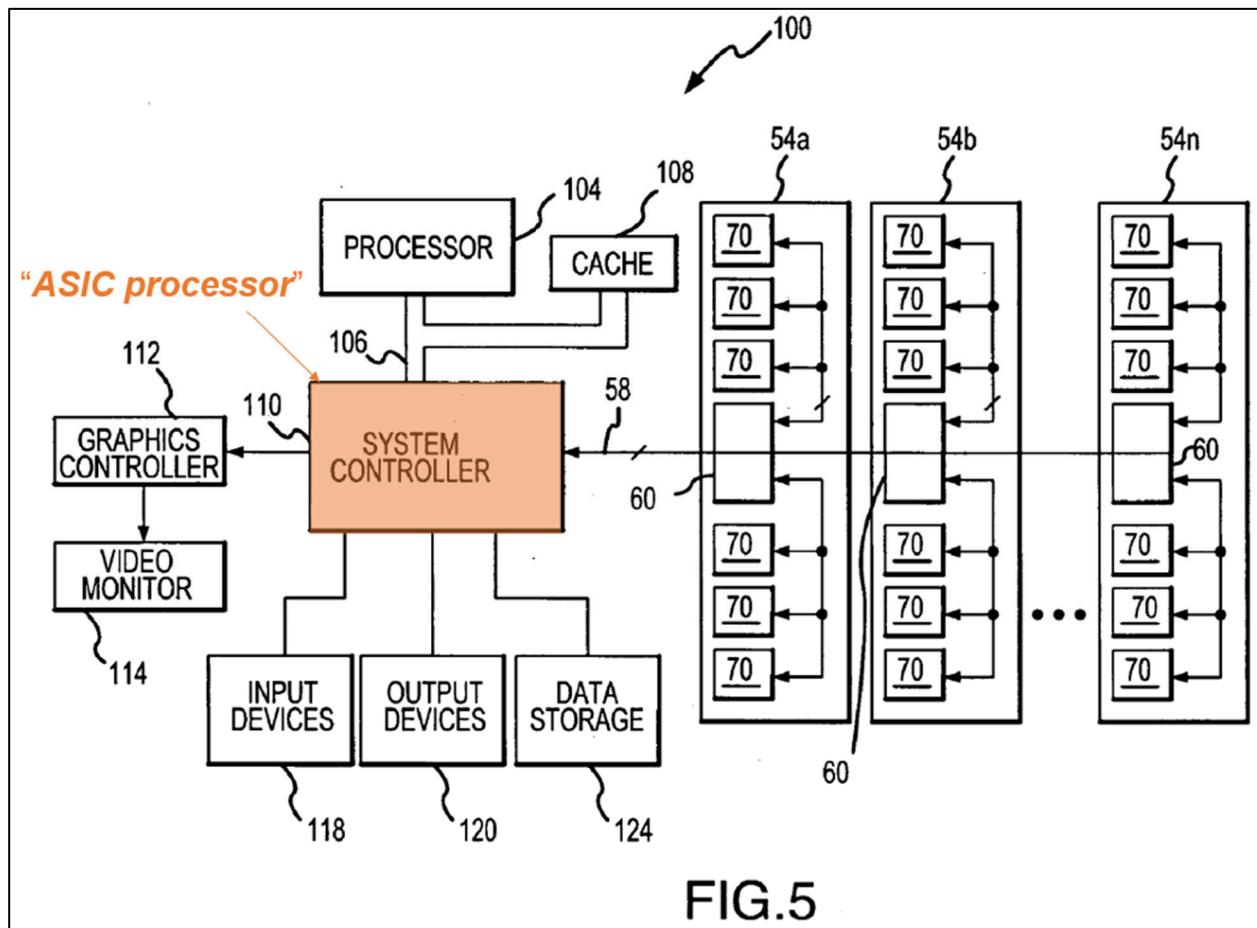
Lee, FIG. 5 (annotated)

The computer system 100 includes a "memory system 50" that "includes a controller 52 coupled to several memory modules 54a, b ... n through a high-speed link 58," where each memory module includes "memory devices 70," such as

“dynamic random access memory devices (‘DRAMs’).” *Id.*, [0015]-[0016], [0023]; *see* Abstract (“A computer system includes a controller coupled to a plurality of memory modules”), [0014] (“FIG. 5 is a block diagram of a computer system using the memory system of FIG. 2”), FIG. 2. Each memory module 54 (*e.g.*, memory module 54a, *green supra*) corresponds to a ***reconfigurable high speed memory chip module***. *See* [1pre] of Ground 1A; EX1003, ¶240.

[21a]

Based on Lee, the combination system includes “a system controller 110, which is also sometimes referred to as a ‘North Bridge’ or ‘memory controller,’” orange in FIG. 5, *infra*. EX1004, [0023]. A POSITA would have understood that a North Bridge controller is an ***ASIC processor***. *See* EX1010, 5:30-33 (“Northbridge 14 is generally considered an ... application specific integrated circuit (ASIC)”); EX1011, [0032] (“an ASIC die ... such as a north bridge”); EX1003, ¶241.



Lee, FIG. 5 (annotated)

Alternatively/additionally, a POSITA would have found it obvious to implement Lee's controller as an *ASIC processor*, as follows. EX1003, ¶¶242-245.

First, ASICs provide performance advantages. Because ASIC chips are custom-built to perform a specific task, they are compact, inexpensive, and capable of high-speed, low-energy operation. EX1003, ¶243 (citing EX1031, 384-385 (listing advantages of ASICs)).

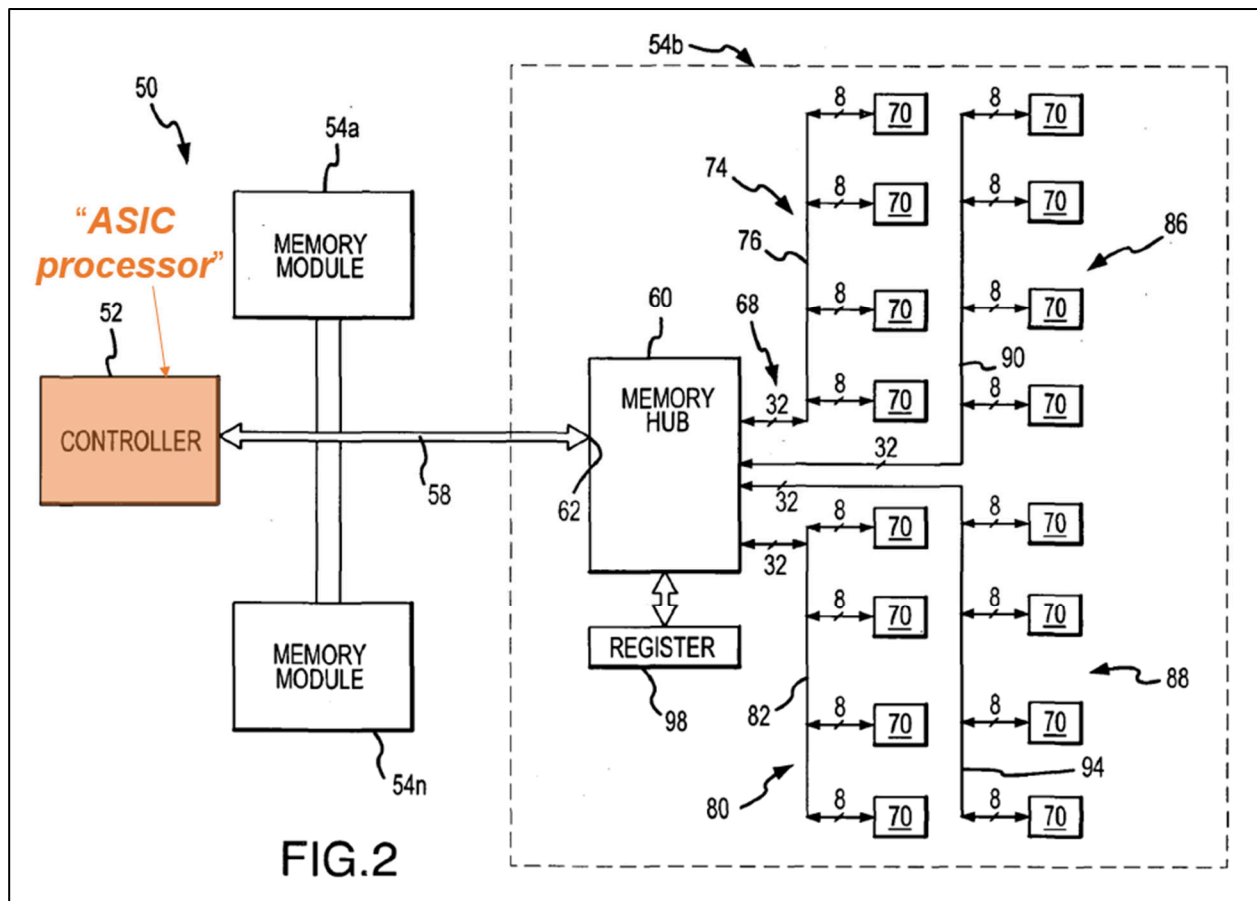
Second, implementation of Lee's controller as an ASIC is one of a finite number of predictable solutions (*e.g.*, implementation of the controller as an ASIC or as a general-purpose chip), and with a reasonable expectation of success (discussed *infra*). EX1003, ¶244; *see KSR*, 550 U.S. at 421.

Third, implementation of Lee's controller as an ASIC is an application of known techniques (an ASIC memory controller) to a known system (Lee's memory system) to yield predictable results (a memory system having an ASIC controller). EX1003, ¶245; *see KSR*, 550 U.S. at 417.

A POSITA would have expected success in implementing Lee's North Bridge controller as an ASIC processor because ASIC implementation of North Bridge controllers was standard. *See* EX1010, 5:30-33; EX1011, [0032]; EX1003, ¶246.

Lee's FIG. 5, showing the North Bridge ASIC processor, illustrates "a computer system using the memory system of FIG. 2." EX1004, [0014]; *see* [0023]. FIG. 2, *infra*, illustrates a "memory system 50 [that] includes a controller 52 coupled to several memory modules 54*a*, *b* ... *n* through a high-speed link 58." EX1004, [0015]. A POSITA have understood that the controller 52 of Lee's FIG. 2 (orange) is also a North Bridge controller, consistent with the North Bridge controller 110 of FIG. 5, and thus that the controller 52 is *an ASIC processor*. EX1003, ¶247. This is because of the stated correspondence between FIG. 2 and

FIG. 5 systems, and because the controller 110 of FIG. 5 is connected to the memory hub via the high-speed link 58, like the controller 52 in FIG. 2. *See* EX1004, [0015]. Alternatively/additionally, a POSITA would have found it obvious to implement Lee's FIG. 2 controller 52 as an ASIC processor given Lee's teachings related to in the similarly structured FIG. 5 system, and given advantages of ASIC processors, discussed *supra*. EX1003, ¶247.



Lee, FIG. 2 (annotated)

[21b]

See [1a] of Grounds 1A-1B; EX1003, ¶248.

[21c]

The Lee-Chang-Dono-Nakai combination renders obvious *a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing*. See [1b] of Ground 1A, EX1003, ¶249. *Programmable signal swing on the first transmission bus*

The signal swing on the first transmission bus (e.g., bus system 68, pink *infra*; or an individual bus system 76) is programmable. See [1b] of Ground 1A. Based on Dono, the programmable signal swing *corresponds to firmware/software in the ASIC processor*, discussed in the following paragraphs. EX1003, ¶¶250-251.

“increases the amplitude VPERI of an internal signal to VDD.” EX1008, [0004], [0040]. The same is also true in reverse: an incoming signal is level-shifted by a level shifter from the external voltage VDD to the internal DRAM operation voltage VPERI. *Id.*; EX1003, ¶252. That is, a signal that is outbound from the memory controller 52 along the high-speed bus 58 to the combination memory hub 60 is at the external voltage VDD, where it is level-shifted to the internal DRAM operation voltage VPERI for transmission along the bus systems 76, 82, 90, 94 to the DRAM memory devices. *Id.*

The voltage VPERI of the signal transmitted along the bus systems 76, 82, 90, 94 (individually or collectively the *first transmission bus*) *corresponds to* the external voltage VDD at which the memory controller (*ASIC processor*) operates in that it is “level-shifted” by a specified amount defined by the difference between the DRAM cell voltage VPERI and the memory controller voltage VDD. *See* EX1008, [0040]; EX1003, ¶253. The external voltage VDD at which the memory controller (*ASIC processor*) operates is also the voltage at which firmware and/or software of the ASIC processor operates, and thus the voltage VPERI of the signal transmitted along the first transmission bus *corresponds to* the voltage VDD at which the *ASIC firmware/software* operates. EX1003, ¶253.

The signal swing of the first transmission bus (*e.g.*, the voltage difference between logic levels of transmitted data) depends on the voltage VPERI of the

signal transmitted along the first transmission bus. EX1003, ¶254. Thus, because the voltage V_{PERI} of the signal transmitted along the first transmission bus corresponds to the external voltage V_{DD} at which the memory controller (*ASIC processor*) operates (and thus to firmware and/or software of the ASIC processor), the signal swing of the first transmission bus likewise *corresponds to firmware and/or software of the ASIC processor*. EX1003, ¶¶254-255.

Programmable data rate on the first transmission bus

The data rate on the first transmission bus is programmable. See [1b] of Ground 1A. EX1003, ¶256.

To the extent the claims are interpreted to require that the programmable data rate *corresponds to firmware/software in the ASIC processor*, this is rendered obvious in the combination based on Nakai, discussed in the following paragraphs. EX1003, ¶257.

Based on Nakai, “all ... circuit blocks” other than “[p]eripheral circuit blocks that communicate with external devices” are “driven by the dynamically controlled system clock.” EX1017, 2. In the combination system, circuit blocks that are subject to dynamic frequency control include the bus system 68 (*first transmission bus*) and the high-speed link 58 (*second transmission bus*), because these circuit elements are not circuit blocks that communicate with external devices. EX1003, ¶257.

In one implementation, “[t]he clock frequency” (*data rate*) of the first and second transmission buses is “set directly via software” (*programmable*) to allow abrupt performance change in response to external events,” *i.e.*, the *first transmission bus has a programmable transmitting/receiving data rate*. EX1017, 5; EX1003, ¶259. The programmable data rate *corresponds to firmware/software in the ASIC processor* because it is “set ... via software,” *e.g.*, software implemented in the memory controller (*ASIC processor*). EX1017, 5; EX1003, ¶259.

Alternatively/additionally, “the DFC block controls the clock frequency” of the first and second transmission buses “autonomously” based on “activity data,” *e.g.*, such that “the clock frequency of the next monitoring period is increased” or “decreased” as appropriated based a calculated “optimum clock frequency.” EX1017, 4-5; *see* Figs. 8-9. Autonomous optimization of clock frequency (*data rate*) on the first and second transmission buses corresponds to the *first transmission bus having a programmable transmitting/receiving data rate*. EX1003, ¶260. The programmable data rate *corresponds to firmware in the ASIC processor* because it is controlled ... “autonomously in hardware” by the DFC, which is implemented in the memory controller (*ASIC processor*). EX1017, 4; EX1003, ¶260.

[21d]

See [1d] of Grounds 1A-1B; EX1003, ¶261.

[21e]

The Lee-Chang-Dono-Nakai combination renders obvious *a second transmission bus having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing*. See [1c] of Ground 1A; EX1003, ¶262.

Programmable signal swing on the second transmission bus

The high-speed bus (*second transmission bus*, green in FIG. 2, *infra*) is *coupled between the logic unit* (memory hub, blue) *and the ASIC processor* (memory controller, orange). See [1c]-[1d] of Ground 1A; EX1004, [0015], [0025], FIG. 2, FIG. 5; EX1003, ¶263.

The signal swing on the second transmission bus (e.g., high speed link 58, green *infra*) is programmable. See [1c] of Ground 1A. Based on Dono, the programmable signal swing *corresponds to firmware/software in the ASIC processor*, discussed in the following paragraphs. EX1003, ¶264.

The signal swing of the second transmission bus (*e.g.*, the voltage difference between logic levels of transmitted data) depends on the voltage VDD of the signal transmitted along the second transmission bus. EX1003, ¶267. Thus, because the voltage VDD of the signal transmitted along the second transmission bus is associated to the external voltage VDD at which the memory controller (*ASIC processor*) operates (and thus to firmware and/or software of the ASIC processor), the signal swing of the second transmission bus likewise *is associated to firmware and/or software of the ASIC processor. Id.*

Programmable data rate on the first transmission bus

The data rate on the second transmission bus is programmable. *See* [1c] of Ground 1A. EX1003, ¶268.

To the extent the claims are interpreted to require that the programmable data rate *corresponds to firmware/software in the ASIC processor*, this is rendered obvious in the combination based on Nakai, discussed in the following paragraphs. EX1003, ¶269.

First, “[t]he clock frequency” (*data rate*) of the second transmission bus is “set directly via software” (*programmable*), *i.e.*, the *second transmission bus has a programmable transmitting/receiving data rate corresponding to firmware/software in the ASIC processor. See* [21c]; EX1017, 5; EX1003, ¶270.

Alternatively/additionally, autonomous optimization of clock frequency (*data rate*) on the second transmission bus corresponds to the *second transmission bus having a programmable transmitting/receiving data rate*, and the programmable data rate *corresponds to firmware in the ASIC processor* because it is controlled ... “autonomously in hardware.” See [21c]; EX1017, 4; EX1003, ¶271.

(b) **Claim 23**

[23]

See [4] of Grounds 1A-1B; EX1003, ¶272.

VI. PAYMENT OF FEES—37 C.F.R. §42.103

Petitioner authorizes the Patent and Trademark Office to charge any fees to Deposit Account No. 06-1050.

VII. MANDATORY NOTICES—37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest—37 C.F.R. § 42.8(b)(1)

Petitioner, Apple Inc., is the real party-in-interest.

B. Related Matters—37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the '834 Patent. The '834 Patent is the subject of civil action: *WeCrevention, Inc. v. Dell Inc. et al*, 2-25-cv-01040 (EDTX) dated Oct. 10, 2025; *WeCrevention, Inc. v. Apple Inc.*, 7-25-cv-00458 (WDTX), dated Oct. 07, 2025; *WeCrevention Inc. v. Lenovo Group Limited et al*, 2-25-cv-01008 (EDTX), dated Oct. 03, 2025; *WeCrevention, Inc. v. Apple Inc.*, 2-25-cv-00951 (EDTX) dated Sep. 16, 2025.

C. Lead And Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0276IP1@fr.com.

Respectfully submitted,

Dated: February 13, 2026

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,945 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 13, 2026

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 13, 2026, a complete and entire copy of this Petition for *Inter partes* Review, Power of Attorney, and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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