

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,

Petitioner,

v.

WECREVENTION, INC.,

Patent Owner.

Patent No. 9,201,834

Filing Date: November 2, 2012

Issue Date: December 1, 2015

Inventors: Weng-Dah Ken, Chao-Chun Lu, and Jan-Mye Sung

Title: RECONFIGURABLE HIGH SPEED MEMORY CHIP MODULE AND
ELECTRONIC DEVICE WITH A RECONFIGURABLE HIGH SPEED
MEMORY CHIP MODULE

PATENT OWNER'S PRELIMINARY RESPONSE

Case No. IPR2026-00240

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LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions in <i>WeCrevention, Inc. v. Apple Inc.</i> , Case No. 7:25-cv-00458-ADA (W.D. Tex.), dated January 20, 2026
2002	Defendant's Invalidity and Subject Matter Eligibility Contentions in <i>WeCrevention Inc. v. Apple Inc.</i> , Case No. 7:25-cv-00458-ADA (W.D. Tex.), dated March 17, 2026
2003	Federal Register, Vol. 90, No. 199, dated Friday, October 17, 2025
2004	Scheduling Order (Dkt. 32) in <i>WeCrevention, Inc. v. Apple Inc.</i> , Case No. 7:25-cv-00458-ADA (W.D. Tex.), dated January 21, 2026
2005	https://marketrealist.com/2019/12/will-china-still-be-second-home-apple/
2006	Appeal Statistics, Patent Trial and Appeal Board, dated October 31, 2025
2007	Patent Trial and Appeals Board (PTAB) data at a glance December 2025
2008	March 24, 2025 guidance memorandum from Chief Administrative Patent Judge Boalick
2009	Director Squires Memorandum, Additional Discretionary Institution Considerations — U.S. Manufacturing and Small Business Use of AIA Proceedings (Mar. 11, 2026)
2010	MacRumors / Financial Times, Apple Plans to Source All U.S.-Bound iPhones from India by End of 2026, Apr. 25, 2025
2011	Korea Economic Daily / MacRumors, Samsung Becomes Apple's Primary LPDDR5X Supplier for iPhone 17, Providing 60–70% of Memory, Dec. 22, 2025
2012	SK hynix Newsroom, <i>Semiconductor 101: SK hynix on Where Chips Are Made & Used</i> (Apr. 3, 2025)
2013	Apple Newsroom, Apple Increases U.S. Commitment to \$600 Billion, Announces American Manufacturing Program, Aug. 6, 2025, https://www.apple.com/newsroom/2025/08/apple-increases-us-commitment-to-600-billion-usd-announces-ambitious-program/

Exhibit No.	Description of Document
2014	Samsung Semiconductor Newsroom, <i>Samsung Begins Mass Production of 16Gb LPDDR5 DRAM at World's Largest Semiconductor Line</i> (Sept. 9, 2020)
2015	SK hynix Inc., <i>SK hynix Signs Investment Agreement of Advanced Chip Packaging with Indiana</i> (Apr. 3, 2024)
2016	Apple's Opening Claim Construction Brief in <i>WeCrevention, Inc. v. Apple Inc.</i> , Case No. 7:25-cv-00458-ADA (W.D. Tex.) Dkt. 40, dated May 6, 2026

I. INTRODUCTION

Apple's Petition for *inter partes* review of the '834 Patent should be denied. It fails for reasons that emerge from Apple's own filings, from the prior art Apple itself selected, and from the prosecution history of the '834 Patent. Each of the independent defects identified below is, on its own, sufficient to defeat institution; taken together, they show a Petition that did not, and on the references Apple chose could not, demonstrate a reasonable likelihood of success on any Challenged Claim.

First, Apple's claim-construction posture is inconsistent across forums. In the parallel district-court litigation,¹ Apple has expressly proposed that the preambles of the '834 Patent's claims are limiting because the preamble phrase "*reconfigurable high speed memory chip module*" supplies "a fundamental characteristic of the claimed invention" that is "necessary to give life, meaning, and vitality" to the claims. Ex. 2016 at 4, 9. In this Petition, however, Apple takes the opposite position by footnote: "Petitioner does not concede that the preambles of the Challenged Claims are limiting." Pet. 15 n.5. Apple offers no explanation for the inconsistency. Under *Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20 at 4-5 (Director Nov. 3, 2025) (*precedential*), and *Tesla, Inc. v. Intell. Ventures II LLC*, IPR2025-00340, Paper 18 at 3-4 (Director Nov. 5, 2025), an unexplained inconsistency on whether the preamble is limiting warrants denial of institution.

¹ *WeCrevention, Inc. v. Apple Inc.*, Case No. 7-25-cv-00458 (W.D. Tex.)

Second, the '834 Patent's prosecution history independently warrants denial under § 325(d) on facts that are substantially stronger than the ordinary *Advanced Bionics* case. Both primary references in every Ground of the Petition—Lee (Ex. 1004) and Chang (Ex. 1006)—were specifically considered by the Examiner. In the March 27, 2015 Non-Final Office Action, the Examiner rejected original Claims 1, 2, and 22 under 35 U.S.C. § 102(e) as anticipated by Lee, mapping Lee's "bus system 68" to the claimed first transmission bus, Lee's memory hub 60 to the logic unit, and Lee's controller 52 to the claimed ASIC processor—the same mappings Apple now advances. Ex. 1002, 42. In the same Office Action, the Examiner cited Chang (US 2010/0235554) in the Notice of References Cited (PTO-892), Row L. *Id.*, 45. Applicant overcame the Lee rejection by amending Claim 1 to add the very limitations Apple now alleges Lee-Chang renders obvious—the second transmission bus with "*a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing,*" and the logic unit "*further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.*" *Id.*, 28 (Amendment) (emphasis added). The Examiner allowed the amended claims on the express ground that "the prior arts, cited in its entirety, or in combination, do not teach a second transmission bus coupled to the logic unit having a second programmable transmitting or receiving data rate, a second programmable

transmitting or receiving signal swing” and the logic unit “*further used for converting.*” Ex. 1002, 43. (emphasis added) Apple now asks the Board to find obvious the precise features that the Examiner found to overcome a rejection based on Lee, without acknowledging—much less identifying material error in—the Examiner’s prior consideration. Section 325(d) exists to prevent just such a tactic. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (*precedential*).

Third, every Ground in the Petition depends on Chang (Ex. 1006) to supply the “*programmable transmitting or receiving signal swing*” limitations of Claim 1[1b] and 1[1c]—and Chang does not disclose programmability as claimed. For example, Chang’s purported data-rate teaching is a remedial-action mechanism that may “reduc[e] the data rate in one or more of the sub-channels” in the event of “an error or a degradation of one or more of the performance metrics.” *Id.*, [0036]. The defect is not curable: Chang is the sole prior art Apple identifies for both [1b]/[1c] limitations, and every other Ground builds on Ground 1A’s Lee + Chang combination. Pet. 1–2; Pet. 48 (Ground 1B incorporating Ground 1A mappings); Pet. 95 (Ground 1I [21e] “*See [1c]*”).

Fourth, Apple’s mapping for the “*converting*” limitation ([1d]) is defective on independent grounds. Lee, on its face, does not describe “*converting*” one set of parallel data into another. Lee describes coupling 128 bits of data through the high-

speed link 58 either by “increasing the speed of the link 58” or by varying “the size of the data word coupled through the link 58.” Ex. 1004, [0017]; Pet. 7–8. That language describes how the same 128-bit payload travels onto the link, not a conversion of one set of data into a different set. Faced with that gap in Lee, Apple does precisely what the Stewart Memorandum forbids: Apple’s expert characterizes Lee’s coupling as a “*convers[ion]*” by citing Nakamura (Ex. 1019)—a reference asserted nowhere in the Petition—for the proposition that “a parallel-to-parallel converter for converting an ‘m’-bit parallel signal into an ‘n’-bit parallel signal” was known in the art. Pet. 31 (citing Ex. 1003, ¶¶ 93–95 (citing Ex. 1019, Abstract))

Fifth, Apple’s Lee-Chang combination (Ground 1A) and its Lee-Chang-Tsern combinations (Grounds 1B–1I) independently fail because each destroys Lee’s principle of operation. Lee’s defining feature is its high-bandwidth mode in which “the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access.” Ex. 1004, [0017]. Chang’s remedial-action teaching that the controller may “reduc[e] the data rate in one or more of the sub-channels” in response to errors is incompatible with Lee’s simultaneous-parallel-access architecture: if one sub-channel’s rate is reduced, Lee’s 128-bit simultaneous read across all four sub-channels can no longer occur. Ex. 1006, [0036]. The Lee-Chang-Tsern Grounds present the same conflict in starker form: Tsern’s “configurable

serialization/deserialization circuit 1891” “performs serialization and deserialization functions” to bridge mismatched interface widths—the opposite of Lee’s simultaneous-parallel-access architecture. Ex. 1005, 38. Substituting Tsern’s serialization-based scheme for Lee’s simultaneous parallel access either eliminates Lee’s parallel-128-bit operation (defeating Lee’s purpose) or requires re-architecting Tsern’s buffer in a way Tsern does not contemplate. *See In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984). Further, Apple’s purported motivation to combine is conclusory *KSR* boilerplate (“known technique applied to known system to yield predictable results”). Pet. 13–15, 46–47.

Any one of the foregoing—the unexplained claim-construction inconsistency, the § 325(d) basis for denial under *Advanced Bionics* on the unusually strong facts of the Lee rejection and Chang listing on the notice of references cited, Chang’s failure to disclose the runtime programmability the ’834 Patent claims require, the disguised multi-reference reliance on Nakamura in violation of § 104(b)(4) and the Stewart Memorandum, and the destruction of Lee’s principle of operation in the Lee-Chang and Lee-Chang-Tsern Grounds—is independently a sufficient basis to deny institution. Together, these issues and defects leave Apple far short of the reasonable-likelihood threshold. The Petition should be denied.

II. CLAIM CONSTRUCTION

Patent Owner agrees with Apple’s position in the Petition that all terms should

be given their plain and ordinary meaning. Pet. 4.

III. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this Preliminary Response only, Patent Owner applies Petitioner's definition of a person of ordinary skill in the art (POSITA). Pet. 4. Patent Owner reserves the right to advance an alternative definition in any subsequent filing should the Board institute review.

IV. PETITIONER HAS NOT DEMONSTRATED A REASONABLE LIKELIHOOD OF SUCCESS, AND THE PETITION SHOULD BE DENIED

Obviousness rests on factual determinations including the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question is whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983). Failure to identify the differences between the claimed subject matter and the prior art is fatal to an obviousness challenge. *See Apple, Inc. v. Contentguard Holdings, Inc.*, IPR2015-00355, Paper 9 at 9–10 (P.T.A.B. June 26, 2015).

The Board must support the conclusion that a POSITA not only could have made, but *would have* been motivated to combine the prior-art references in the way the claim recites and reasonably expected success. *Pers. Web Techs., LLC v. Apple*,

Inc., 848 F.3d 987, 994 (Fed. Cir. 2017); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016). The combinability determination requires a plausible articulated rationale. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013). “Knowledge of a problem and motivation to solve it *are entirely different from* motivation to combine particular references.” *Innogenetics, N.V. v. Abbott Lab’ys*, 512 F.3d 1363, 1373 (Fed. Cir. 2008). (emphasis added) Where the proposed combination would render the primary reference unsatisfactory for its intended purpose, or change its principle of operation, there is no motivation to combine. *In re Gordon*, 733 F.2d at 902.

35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.104(b) require the petition to identify “*with particularity*” each claim challenged, the grounds for the challenge, and how each claim element is found in the prior art relied upon for that ground. The Board may deny petitions that fail to comply. *See* July 31, 2025 Memorandum from Then-Acting Director Stewart Regarding Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4).

Independently, the Board may exercise its discretion to deny institution under 35 U.S.C. § 314(a). *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016) (“the agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion”). The Director has held in a precedential decision that a petitioner who advances different claim-construction positions in district court and

at the Board “**should explain sufficiently why the different positions are warranted, even in instances that do not implicate Section 112(f),**” and that failure to do so warrants denial. *Revvo Techs.*, IPR2025-00632, Paper 20 at 5. (emphasis added).

A. The Petition Should Be Denied Because Petitioner Takes Inconsistent Claim-Construction Positions Across Forums Without Explanation

After filing this Petition, Apple filed an Opening Claim Construction Brief in the parallel district-court litigation, *WeCrevention, Inc. v. Apple Inc.*, Case No. 7:25-cv-00458-ADA (W.D. Tex.) (Ex. 2016), taking the position that the preambles of the independent claims of the ’834 Patent are limiting. Here, however, Apple expressly does not concede that the preambles of the Challenged Claims are limiting. The disparity is unexplained, and under the Director’s guidance, that defect alone warrants denial of institution.

1. Apple’s Inconsistent Positions Across the Two Forums

Apple’s district-court position. Apple’s Opening Claim Construction Brief expressly proposes that the “*reconfigurable high speed memory chip module*” term in the preambles of the ’834 Patent’s claims is limiting. *Id.*, 6. Apple maintains in district court that the preamble “contains the core of what the inventors actually invented,” that the preamble “supplies fundamental structure required by the body of the claims,” and that “the preamble here therefore breathes ‘life, meaning, and

vitality’ into the claim because no other limitations in the claims capture the modular structure imparted by ‘[reconfigurable] high speed memory chip module.’” *Id.*, 7, 9, 12. Apple goes so far as to argue in district court that **without** treating the preamble as limiting, the claims “could map to disparate and remote components: a ‘memory cell array group’ in a data center, a ‘logic unit’ in a remote device, and the ‘buses’ being network links.” *Id.*, 12.

Apple’s IPR position. Apple’s Petition takes the opposite position by footnote: **“Petitioner does not concede that the preambles of the Challenged Claims are limiting.”** Pet. 15 n.5. (emphasis added) The reservation is not incidental. For example, Apple’s mapping of the preamble of Claim 1 in Ground 1A—“*A reconfigurable high speed memory chip module, comprising*”—directs the Board to Lee’s **memory system 50** and Lee’s **memory module 54** (Ex. 1004, [0015]–[0016]; Pet. 15–16) without ever showing that Lee specifically discloses a “*reconfigurable high speed memory chip module*” in the sense Apple urges in district court. Apple’s mapping equates Lee’s memory module 54 with the claimed module simply because “it includes memory chips” (*id.*), and characterizes the module as “high speed” because it “is coupled to the controller ‘through a high-speed link.’” Pet. 16 (citing Ex. 1004, [0015], [0017]). That is precisely the kind of “disparate and remote components” mapping Apple’s district-court brief argues is inappropriate should the preambles be deemed limiting in district court.

Apple’s positions are irreconcilable, and Apple cannot simultaneously be right in both forums. Either the preamble carries the structural weight Apple ascribes to it in district court (in which case Apple’s IPR mapping ignores limitations the claims contain), or the preamble does not carry that weight (in which case Apple’s district-court construction is wrong). Apple offers no explanation for the inconsistency. The hedge “Petitioner does not concede” is itself an admission that Apple knew, when it filed the Petition, that it was taking a position inconsistent with one Apple intended to advance in district court.

2. The Unexplained Inconsistency Warrants Denial Under *Revvo, Tesla, and Cambridge*

An unexplained inconsistency between a petitioner’s claim-construction positions in district court and at the Board warrants denial of institution. In *Revvo Techs.*, the Director held: **“the petitioner should explain sufficiently why the different [claim construction] positions are warranted.”** See IPR2025-00632, Paper 20 at 4–5. (emphasis added) On remand, the Board again granted institution, and the Director subsequently *sua sponte* initiated review and again denied institution. *Id.*, Papers 30 (Jan. 14, 2026) and 36 (Director Jan. 26, 2026).

The Director applied *Revvo* in *Tesla, Inc.*, IPR2025-00340. The *Tesla* petitioner argued indefiniteness in district court but said in the IPR that no claim term required express construction. The Director rejected the petitioner’s

explanation: “Petitioner’s statement that it cannot raise indefiniteness challenges in an *inter partes* review is not a sufficient explanation. Indeed, the statement amounts to an assertion that a petitioner should be permitted to raise inconsistent invalidity challenges in the two forums.” *Id.*, Paper 18 at 3. Applying *Revvo*, the Director was express in denying institution in *Tesla*: “[a]llowing a petitioner to advance a claim construction before the Board when that petitioner has made inconsistent indefiniteness arguments in district court fails to further, but instead detracts from, the Office’s goal of ‘**providing greater predictability and certainty in the patent system.**’” *Id.* at 4 (emphasis added) (citing *Revvo Techs.*, IPR2025-00632, Paper 20 at 4–5; *see also Cambridge Mobile Telematics, Inc. v. Sfara, Inc.*, IPR2024-00952, Paper 12 at 8 (P.T.A.B. Dec. 13, 2024) (“[a]t a minimum, the Petition should have explained why the plain and ordinary meaning . . . should apply in this proceeding (why the inconsistent positions are warranted) or set forth an alternative . . . claim construction.”)).

Apple’s footnote 5 is not an explanation; it is a flag. It is a candid admission that Apple is taking inconsistent positions and intends to maintain both. *Revvo* requires that Apple explain *why* the different positions are warranted—but Apple has merely reserved the right to maintain them. That is insufficient. *Tesla*, IPR2025-00340, Paper 18 at 3.

3. The Inconsistency Has Substantive Consequences for the Petition

The inconsistency is not a technicality. Apple’s district-court position—that the preamble is limiting because it conveys “the modular structure imparted by ‘[reconfigurable] high speed memory chip module’” (Ex. 2016 at 12)—supplies meaningful structural content. Specifically, in district court Apple urges that the preamble must be limiting to prevent the claims from mapping to “disparate and remote components,” such as “a ‘memory cell array group’ in a data center, a ‘logic unit’ in a remote device, and the ‘buses’ being network links.” *Id.*, Apple’s IPR mapping nevertheless equates Lee’s memory module 54 with the claimed “reconfigurable high speed memory chip module” solely because Lee’s module “includes memory chips” (Pet. 15) and is “coupled to the controller ‘through a high-speed link’” (Pet. 16)—a thin equation that does not engage with the structural content Apple’s district-court brief insists the preamble carries. Apple cannot have it both ways. For Apple to argue in district court that the preambles of the ’834 Patent are limiting (to further Apple’s non-infringement positions) only to then argue here that the preambles are not limiting (to further Apple’s invalidity defenses) certainly does not provide greater predictability and certainty in the patent system—and is a plainly unfair tactic.

B. The Petition Independently Warrants Discretionary Denial Under 35 U.S.C. § 325(d) Because the Examiner Specifically Considered Lee and Chang and Allowed the Claims Only After Applicant Amended to Overcome a Lee Anticipation Rejection

The '834 Patent's prosecution history presents an unusually strong basis for discretionary denial under § 325(d). Both primary references in every Ground of the Petition—Lee (Ex. 1004) and Chang (Ex. 1006)—were specifically considered by the Examiner. The Examiner used Lee as the basis for an anticipation rejection of the original claims that Apple now seeks to invalidate. And the Challenged Claims issued only after Applicant amended them to overcome that Lee anticipation rejection by adding the very limitations Apple's Petition now alleges Lee's combination with Chang renders obvious. Apple's Petition does not acknowledge any of this prosecution history. Both prongs of the *Advanced Bionics* framework therefore favor denial.

Lee and Chang were before the Examiner. In the March 27, 2015 Non-Final Office Action, the Examiner cited both Lee (US 2004/0260864) and Chang (US 2010/0235554) in the Notice of References Cited (PTO-892), Rows K and L, respectively. Ex. 1002, 45. Lee is the same Lee Apple asserts in Ground 1A; Chang is the same Chang Apple asserts in Ground 1A.

The Examiner did not merely cite Lee—the Examiner used Lee as the basis for a § 102(e) anticipation rejection of original Claims 1, 2, and 22 of the application

that became the '834 Patent. *Id.*, 42 (“Claims 1-2, 22 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lee et al. (US Pub No. 2004/0260864).”). The Examiner’s element-by-element mapping of Lee closely tracks Apple’s present mapping: Lee’s bus system 68 was mapped to the claimed “*first transmission bus*”; Lee’s memory hub 60 was mapped to the claimed “*logic unit*”; for original Claim 22 (the predecessor of issued Claim 21), Lee’s controller 52 was mapped to the claimed “*ASIC processor*”, with Lee’s non-volatile register 98 mapped to the claimed “*firmware . . . comprised in the ASIC processor.*” *Id.* (rejection of original Claims 1, 2, 22 over Lee). These are the same Lee features Apple now seeks to map onto the very claim language that issued only after Applicant amended out of that rejection.

Applicant overcame the Lee rejection by amending Claim 1 to add the second-transmission-bus programmability and converting limitations from then-allowable Claim 3. Applicant’s Amendment, filed September 28, 2015, added to Claim 1: “*a second transmission bus coupled to the logic unit having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing,*” and the logic unit “*further used for converting a first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.*” *Id.*, 28 (Amendment showing additions). Apple’s Petition itself confirms this: “To secure grant, applicant incorporated features of

allowable claim 3 into the independent claims.” Pet. 4.

The Examiner then issued a Notice of Allowance. The Examiner’s express Reasons for Allowance were that “the prior arts, cited in its entirety, or in combination, do not teach a second transmission bus coupled to the logic unit having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing” and the logic unit “*further used for converting the first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.*” Ex. 1002, 43. (emphasis added) That is the precise claim language Apple’s Petition asserts Lee-Chang renders obvious.

Under *Advanced Bionics*, the Board must consider whether “the same or substantially the same prior art or arguments previously were presented to the Office,” and if so, whether “the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” IPR2019-01469, Paper 6 at 7-8. Both prongs favor denial here. On prong one, Lee and Chang are not merely the same references the Examiner considered—Lee was the basis for an actual § 102(e) anticipation rejection that Applicant overcame by amendment, and Chang appears in the very same PTO-892. Ex. 1002, 42, 45. On prong two, Apple’s Petition does not even acknowledge the Lee § 102(e) rejection or the Examiner’s Reasons for Allowance, much less identify any material error in the Examiner’s consideration

of Lee or Chang. Apple’s position—that Lee-Chang renders obvious the precise claim features that issued only after Applicant amended to overcome Lee—is in direct conflict with the Examiner’s reasoning, and Apple has not shown the Examiner erred.

The result is the rare case in which the patent owner is not merely arguing that the Examiner considered the references in some general sense, but rather that the prosecution history expressly and dispositively addresses what Apple now asks the Board to find. *Advanced Bionics* and § 325(d) exist for this circumstance—and the Board should exercise deny institution.

C. Every Ground Fails Because Chang Does Not Disclose a “Programmable Transmitting or Receiving Data Rate” as Claimed

Chang (Ex. 1006) is one of the two sources Apple identifies for the “programmable transmitting or receiving data rate” of the first and second transmission buses (Pet. 20-21, citing Chang, [0036]), with Apple’s only alternative being a strained reading of Lee’s mode-switching language. *Id.*, 19–20. On the record Apple presents, Chang does not disclose that limitation. Chang describes a **remedial-action** mechanism that may “reduc[e] the data rate in one or more of the sub-channels” in the event of “an error or a degradation of one or more of the performance metrics” (Ex. 1006, [0036]). The teaching is not a “programmable . . . data rate” the ’834 Patent claims require, as the ’834 Patent specification confirms.

Because every Ground depends on Chang to supply [1b]’s and [1c]’s programmability limitations, the defect carries through to every ground in the Petition. Pet. 1–2 (asserted-grounds table—Lee + Chang combination with secondary references); *id.*, 48 (Ground 1B: “[1pre]–[1c] *See* [1pre]–[1c] of Ground 1A”); *id.*, 90 (Ground 1I: “[21c] ... *See* [1b] of Ground 1A”); *id.*, 95 (Ground 1I “[21e] ... *See* [1c] of Ground 1A”).

Apple identifies two sources for its “*data rate*” mapping: (i) Lee’s high memory bandwidth vs. high memory depth modes, and (ii) Chang’s remedial-action reduction of “the data rate in one or more of the sub-channels.” *Id.*, 19–20. Neither supplies a “*programmable . . . data rate*” as claimed by the ’834 Patent claims and disclosed in the specification.

Lee describes mode-switching that is fundamentally about addressing—“when programmed for a high bandwidth, the memory hub simultaneously accesses the memory devices in all of the ranks,” and “when programmed for a high memory depth, the memory hub accesses the memory devices in only one of the ranks at a time.” Ex. 1004, [0017]–[0018]. The “high memory depth” mode “operate[s] at a slower data rate than in the high bandwidth mode” as a **consequence** of the addressing reconfiguration, not as a runtime-programmable data-rate feature. *Id.* Apple’s reading of Lee’s addressing scheme as itself a programmable-data-rate teaching strips the mode-switching language of its context.

Chang’s [0036] teaching, as already noted, is a *remedial-action* mechanism triggered by errors or performance degradation. Ex. 1006, [0036]. That is not a runtime-“*programmable . . . data-rate.*” There is no OTP/MTP/Flash/register/firmware/software mechanism in [0036], and no indication that the reduction is performed by reference to a stored configuration value the way Claim 4’s programmability resources operate.

D. Ground 1A Independently Fails Because Apple’s [1d] “*Converting*” Mapping Cross-Cites Nakamura—a Reference Not Asserted in Any Ground—and Because Lee Discloses Coupling of 128-Bit Parallel Data, Not Conversion

Claim 1[1d] requires that the logic unit be “*further used for converting a first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.*” Ex. 1001, Cl. 1. Apple’s Ground 1A mapping for this limitation fails because (i) Lee, on its face, does not describe a conversion operation—only the **coupling** of the same 128 bits of data through the high-speed link at different speeds or word sizes—and (ii) Apple attempts that bridge that gap in Lee by citing Nakamura (Ex. 1019), a reference not asserted in Ground 1A (or in any other ground). The Stewart Memorandum precludes the latter, and Lee on its own does not supply the former.

1. Lee Describes the Coupling of 128 Bits Through the High-Speed Link, Not Conversion

The Lee paragraph on which Apple’s “conversion” theory rests is [0017]. Pet.

7–8. Lee says: “The 128 bits of data can be coupled through the high-speed link 58 by either increasing the speed of the link 58 or the size of the data word **coupled** through the link 58. For example, in the high-speed mode, a 128-bit data word may be **coupled** through the link 58. Therefore, for every memory access, 128 data bits will be **coupled** through the link 58. Alternatively, the link 58 may transfer only a 32-bit data word, but it may operate at four times the speed of the memory devices 70.” Ex. 1004, [0017] (emphasis added).

Lee uses the language of coupling, not “converting.” Lee describes two formats through which the same 128-bit payload may travel onto the link—either as a single 128-bit word or as four serially-sent 32-bit words at four times the speed—and confirms that “[t]herefore, for every memory access, 128 data bits will be **coupled** through the link 58.” *Id.* The data quantity is preserved (128 bits), the data content is preserved (the same bits read from memory), and the difference between the two formats is a **transmission-format** difference rather than a transformation of one set of data into a different set. That is bandwidth equivalence; it is not conversion. The ’834 Patent specification, by contrast, describes “converting” as a substantive operation performed by a “parallel-to-serial controller” within the logic unit, where the first bus operates at one bit width and the second bus operates at a different bit width: “the logic unit 106 utilizes a bus width parallel-to-serial controller 1062 included thereof to convert the first set of parallel data into a second

set of parallel data, and transmits the second set of parallel data to an application-specific integrated circuit (ASIC) 112 . . . through a second transmission bus 110.” EX1001, 4:45-55. Lee’s mode-switching language describes addressing reconfiguration (the high-bandwidth mode addresses all memory devices simultaneously; the high-memory-depth mode addresses one rank at a time), not conversion of data between bus widths. Ex. 1004, [0017]–[0018].

2. Apple Fills the Gap in Lee with Nakamura, a Reference Not Asserted in Any Ground

In view of Lee’s coupling language, Apple simply has its expert characterize Lee’s coupling as “*converting*” by importing Nakamura: “A POSITA would have found obvious that receiving 128 bits of data simultaneously through multiple bus systems and then transmitting that data in a 64- or 32-bit word through a single bus system involves the memory hub converting the received data (including the first set of parallel data) to the transmitted data (second set of parallel data), e.g., by multiplexing the received data. Ex. 1003, ¶¶93–95 (citing Ex. 1019 (Nakamura), Abstract (‘a parallel-to-parallel converter for converting an ‘m’-bit parallel signal into an ‘n’-bit parallel signal’)).” Pet. 30–31. Per Apple, Nakamura supplies the substantive proposition that Lee’s asserted multiplexing is “*converting*” within the meaning of the claim. Apple repeats the same citation chain at Pet. 31 and Pet. 33.

Nakamura (Ex. 1019) is not in Ground 1A’s asserted basis (“§ 103: Lee-

Chang”). Pet., 1. It is not asserted in any other ground. Pet., 1–2. Yet Nakamura supplies the dispositive characterization that purportedly transforms Lee’s function into the claimed “converting.” That is again the precise use of expert testimony and non-asserted prior art that the Stewart Memorandum forbids: “expert testimony, common sense, and other evidence that is not ‘prior art consisting of patents or printed publications’ . . . may not be used to supply a missing claim limitation.” Stewart Memorandum, July 31, 2025, at 2. The Petition must “specify where each element of the claim is found in the prior art patents or printed publications relied upon” within the ground. 37 C.F.R. § 42.104(b)(4).

3. Apple’s Bus-System-68 Alternative Theory Does Not Cure the Defect

Apple offers an “alternatively/additionally” theory in which Lee’s collective “bus system 68” (composed of the four individual bus systems 76, 82, 90, 94) is the “*first transmission bus*.” Pet. 32–33. On that theory, Apple says, the 128 bits read simultaneously across bus system 68 are the first set of parallel data, and either a 32-bit or 64-bit word transmitted on link 58 is the second set of parallel data. Pet. 33.

That alternative inherits the same defects. Lee still does not describe a “*converting*”; Lee describes how the same 128 bits are coupled through link 58 in different formats. Ex. 1004, [0017]. Apple’s alternative mapping again cross-cites Nakamura to bridge the gap: “receiving 128 bits of data simultaneously through

multiple bus systems and then transmitting that data as a 64- or 32-bit word through a single bus system involves converting the received data ..., e.g., by multiplexing the received data. Ex. 1003, ¶99 (citing Ex. 1019, Abstract).” Pet. 33.

The Petition thus leaves Patent Owner and the Board to guess which alternative theory operates in any of the downstream Grounds 1B–1I that incorporate Ground 1A’s [1d] mapping by reference. Apple does not specify which of the two competing first-transmission-bus theories is operative for any of those grounds. That ambiguity is itself incompatible with the “particularity” § 104(b)(4) requires. Ground 1A’s [1d] mapping, Ground 1I’s [21c] cross-reference to [1b] (Pet. 90), and the grounds that build on either of them, thus all fail.

E. The Lee-Chang Combination (Ground 1A) and the Lee-Chang-Tsern Combinations (Grounds 1B–1I) Independently Fail Because Each Destroys Lee’s Principle of Operation

Apple’s Lee-Chang and Lee-Chang-Tsern combinations all suffer from the same architectural conflict with Lee: each requires Lee’s memory hub to abandon the simultaneous-128-bit-parallel-access architecture that is Lee’s defining feature. Each combination therefore either defeats Lee’s stated purpose or requires the secondary reference (Chang or Tsern) to be re-architected in a way the reference itself does not contemplate. *In re Gordon*, 733 F.2d at 902.

1. Lee's Principle of Operation Is Simultaneous Parallel Access to All Memory Devices in High-Bandwidth Mode

Lee's defining architectural feature is the high-bandwidth mode in which **“the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access.”** Ex. 1004, [0017]. The four ranks of memory devices are accessed in parallel through four separate 32-bit bus systems (76, 82, 90, 94) that together “provide 32 bits for the 32-bit data buses” each and “simultaneously” produce the 128-bit access. *Id.*, [0016]–[0017]. Lee's configurability (high-bandwidth vs. high-memory-depth) is achieved by reprogramming “a non-volatile register 98 in the memory module 54” to select the access mode, not by inserting any rate-reducing or serializing layer between the memory devices and the hub. *Id.*, [0017]. The simultaneous parallel access in high-bandwidth mode is the very feature Lee uses to deliver high bandwidth.

2. Inserting Chang's Remedial-Action Data-Rate Reduction into Lee Defeats Lee's High-Bandwidth Mode

Apple's Ground 1A combination imports Chang's teaching that the controller may “reduce[] the data rate in one or more of the sub-channels” as a remedial action in response to errors or performance degradation. Ex. 1006, [0036]; Pet. 13–14. If that teaching is implemented in Lee's architecture, the result conflicts with Lee's

simultaneous-128-bit-parallel-access scheme: reducing the data rate on one (or more) of Lee's four 32-bit bus systems 76, 82, 90, 94 means those sub-channels no longer operate in lockstep, and Lee's simultaneous 128-bit access across all four sub-channels can no longer occur. The combined system would no longer be Lee's system. *In re Gordon*, 733 F.2d at 902. Apple offers no rationale for how Lee's simultaneous-parallel-access architecture can be maintained while Chang's per-sub-channel rate-reduction is implemented. The motivation Apple articulates—that the combination is “merely the application of known techniques to a known system to yield predictable results” (Pet. 13–14)—is conclusory *KSR* boilerplate that does not engage with the architectural conflict.

3. Inserting Tsern's Configurable Serialization/Deserialization Buffer into Lee Either Defeats Lee's Purpose or Repurposes Tsern in a Way Tsern Does Not Contemplate

Apple's Lee-Chang-Tsern combinations (Grounds 1B–1I) substitute Tsern's serialization/deserialization buffer for Lee's memory hub, which destroys Lee's principle of operation. Lee's defining feature is its high-bandwidth mode in which “the memory hub 60 addresses all of the memory devices 70 simultaneously so that 128 bits of data are written to or read from the memory devices 70 each memory access.” Ex. 1004, [0017]. Tsern's buffer interface, by contrast, includes “a [c]onfigurable serialization/deserialization circuit 1891” that “performs serialization

and deserialization functions” depending on “memory device access width” to bridge mismatched interface widths. Ex. 1005, 31, 38. Substituting Tsern’s serialization-based bandwidth-concentration architecture for Lee’s simultaneous-parallel-access architecture either eliminates Lee’s 128-bit parallel operation (defeating Lee’s stated purpose) or re-architects Tsern’s buffer in a manner Tsern itself does not contemplate. *See In re Gordon*, 733 F.2d at 902. Apple’s motivation rationale—“application of known techniques to a known system to yield predictable results”—is conclusory *KSR* boilerplate that does not engage with the architectural conflict. Pet. 41–47. Patent Owner previews this destruction-of-purpose theory here and reserves further argument for the Patent Owner Response if institution is granted.

F. Ground 1I (Claims 21 and 23) Independently Fails Because Apple’s [21a] Mapping Cross-Cites References Outside Ground 1I and Because Neither Dono Nor Nakai Supplies the “*Firmware or Software Comprised in the ASIC Processor*” Limitation

Ground 1I (Lee-Chang-Dono-Nakai) targets Claims 21 and 23. Pet. 75–98. The Ground fails on three independent grounds, in addition to inheriting Ground 1A’s [1d]/[1b]/[1c] defects via Apple’s express cross-references at Pet. 86-95. First, Apple’s [21a] mapping (the “*ASIC processor*” limitation) cross-cites two references outside Ground 1I in violation of 37 C.F.R. § 42.104(b)(4) and the July 31, 2025 Stewart Memorandum. Second, Dono’s level shifter is internal to the DRAM device

and does not occupy the data path between the logic unit and the memory ICs, so Dono cannot supply the claim’s programmable-signal-swing-corresponding-to-firmware-or-software limitation. Third, Nakai’s own specification disavows the “*firmware or software*” tie-in the claim requires by describing the relevant control as operating “autonomously in hardware without special power-management software.” Ex. 1017, 4.

1. Apple’s [21a] Mapping Improperly Fills the “ASIC Processor” Gap in Lee with Expert Testimony and Non-Asserted References

Claim [21a] recites “*an application-specific integrated circuit (ASIC) processor.*” Ex. 1001, Cl. 21. (emphasis added) Lee describes its controller in non-ASIC terms—“a controller 52” coupled to memory modules through a “high-speed link 58.” Ex. 1004, [0015]. Elsewhere Lee describes “a system controller 110, which is also sometimes referred to as a ‘North Bridge’ or ‘memory controller.’” *Id.*, [0023]. Lee says nothing about whether the controller is implemented as an ASIC.

To bridge that gap, Apple offers expert testimony that “a North Bridge controller is an ASIC processor.” Pet. 86 (citing Ex. 1003, ¶ 241). That is the precise use of “expert testimony . . . to supply a missing claim limitation” that the Stewart Memorandum prohibits. Stewart Memorandum, July 31, 2025, at 2. The “general knowledge” of a POSITA that Lee’s North Bridge purportedly “is” an ASIC

processor is not a teaching of Lee or any other reference Apple asserts in Ground 1I; it is a characterization drawn from outside the Ground.

Apple’s expert, in turn, supports that characterization by citing Reeves (Ex. 1010) and RaghuRam (Ex. 1011): “*See* EX1010, 5:30–33 (‘Northbridge 14 is generally considered an . . . application specific integrated circuit (ASIC)’); EX1011, [0032] (‘an ASIC die . . . such as a north bridge’); EX1003, ¶241.” Pet. 86. The “ASIC” characterization Apple’s expert offers comes from Reeves and RaghuRam, not from any reference Apple asserts in Ground 1I. The result is a multi-reference § 103 combination in substance—Lee + Chang + Dono + Nakai + Reeves + RaghuRam—presented as a Lee-Chang-Dono-Nakai ground that does not assert Reeves or RaghuRam. That framing is expressly prohibited by § 42.104(b)(4), which requires that the Petition “specify where each element of the claim is found in the prior art patents or printed publications relied upon” within a given ground. The Stewart Memorandum makes the prohibition explicit: a petitioner cannot use expert testimony or general knowledge to import additional prior art into a ground that does not assert that art.

Apple offers an alternative theory that “a POSITA would have found it obvious to implement Lee’s controller as an ASIC processor.” Pet. 86–88. But the support Apple offers for that alternative—that ASIC implementation “was standard” and provides “performance advantages”—is itself sourced to the same out-of-ground

references (Reeves at 5:30–33, RaghuRam at [0032], and Ex. 1031). Pet. 87–88 (citing Ex. 1010, 5:30–33; Ex. 1011, [0032]; Ex. 1031, 384–385; Ex. 1003, ¶¶ 242–246). Without Reeves, RaghuRam, and Ex. 1031—none of which Apple asserts in Ground 1I—the alternative theory is unsupported attorney argument and conclusory *KSR* boilerplate. *See Pers. Web Techs.*, 848 F.3d at 994.

2. Dono’s Level Shifter Is Internal to the DRAM and Does Not Occupy the First Transmission Bus Between the Logic Unit and the Memory ICs

Claim 21 requires that the first and second transmission bus signal swing be “*corresponding to firmware or software comprised in the ASIC processor.*” Ex. 1001, Cl. 21[21c], [21e]. Apple’s Ground 1I mapping uses Dono (Ex. 1008) for this limitation. Apple maps Dono’s teaching that “a level shifter . . . reduce[s] the amplitude of the external signal [from VDD] to VPERI” (Ex. 1008, [0040]) to the first transmission bus, reasoning that the bus voltage “corresponds to the external voltage VDD” and that VDD “is also the voltage at which firmware and/or software of the ASIC processor operates.” Pet. 91–93 (mapping at [21c]).

The mapping fails on the architectural facts of Dono. Dono’s level shifter is **internal to the DRAM device**, not external to it. Dono’s [0040] describes the level shifter as part of the DRAM’s on-chip circuitry that converts between the DRAM’s internal operating voltage VPERI and the external interface voltage VDD—a function performed at the DRAM’s I/O pins, not on the transmission bus between

the logic unit and the memory cell array ICs that Claim 21 recites. Ex. 1008, [0040], [0103]. The “*first transmission bus*” the claim recites is the bus between “*the type of memory cell array group*” and the logic unit, not the internal data path within a memory IC. Ex. 1001, Cl. 21. (emphasis added) Apple’s mapping equates Dono’s within-DRAM voltage shifting with a programmable signal swing on the first transmission bus, but Dono’s shifter neither occupies that bus nor responds to firmware or software in any “*ASIC processor*.”

1. Nakai Expressly Disavows the “*Firmware or Software*” that the Claim Requires

Apple’s Ground 1I mapping uses Nakai (Ex. 1017) to supply the programmable data rate “*corresponding to firmware or software comprised in the ASIC processor*” for Claims 21’s [21c] and [21e]. Pet. 93–95 (Apple’s mapping at [21c] for first-bus data-rate programmability with reliance on Nakai); Pet. 95 (Apple’s mapping at [21e] for second-bus data-rate programmability incorporating the same Nakai theory).

Nakai’s own text disavows the firmware/software tie-in the claim requires. Nakai expressly states that its dynamic frequency control (“DFC”) “controls the clock frequency at the required minimum value **autonomously in hardware without special power-management software**.” Ex. 1017, 4. That sentence is the express disavowal: Nakai’s DFC operates without software, not with software, and

certainly not with firmware or software “*comprised in the ASIC processor*” as Claim 21 requires.

Apple’s Petition acknowledges that Nakai’s clock-frequency control “is autonomously and dynamically controlled” (Pet. 77, quoting Ex. 1017, 1) and that “the clock frequency may [] be set directly via software to allow abrupt performance change in response to external events” (Pet. 79, quoting Ex. 1017, 5). The “may [] be set directly via software” snippet is the only language Apple can point to for any software involvement—but Nakai’s sentence describes a fallback override capability for “abrupt” events, not the routine programmable-data-rate feature Claim 21 requires, and Nakai’s preceding sentence (“autonomously in hardware without special power-management software”) confirms that the routine operation is hardware-only. Ex. 1017, 4–5. Even if the override sentence were sufficient, Apple does not identify any teaching in Nakai that the override software is “*comprised in the ASIC processor*” as Claim 21 requires. Thus, the mapping fails on Nakai’s own text.

Ground 1I should be denied. Each of the three defects above is independently sufficient. Additionally, Ground 1I inherits Ground 1A’s Chang defect (§ IV.C, *supra*), [1d] converting defect (§ IV.D, *supra*), § 325(d) bar (§ IV.B, *supra*), and Lee-Chang destruction-of-purpose problem (§ IV.E, *supra*), by Apple’s own cross-references at Pet. 89-95. Pet. 89 (“[21b] *See* [1a] of Grounds 1A-1B”); Pet. 90

("[21c] ... *See* [1b] of Ground 1A"); Pet. 95 ("[21d] *See* [1d] of Grounds 1A-1B");
Pet. 95 ("[21e] ... *See* [1c] of Ground 1A").

V. CONCLUSION

For each of the foregoing reasons—any one of which is independently sufficient—Patent Owner respectfully requests that the Board deny institution.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S PRELIMINARY RESPONSE has 6,974 words in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

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CERTIFICATE OF SERVICE

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