UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	05/04/2021	10998017	ETRP0143USA3	3080

27765 7590 04/14/2021

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Der-Min Yuan, New Taipei City, TAIWAN;
Etron Technology, Inc., Hsinchu, TAIWAN;
Yen-An Chang, Miaoli County, TAIWAN;
Wei-Ming Huang, Hsinchu County, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)

PART B – FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate " FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 03/03/2021

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.,
New Taipei City,
Taiwan

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Edie Hung	(Typed or printed name)
/Edie Hung/	(Signature)
03/31/2021	(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

TITLE OF INVENTION: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0	$0	$600	06/03/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2135	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ " Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Winston Hsu
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE or COUNTRY)
Etron Technology, Inc.	Hsinchu, Taiwan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. Fees Submitted: ☑ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment (*Please first reapply any previously paid fee shown above*):

☑ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-3105

5. Change of Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29. NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27. NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status. NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Winston Hsu/ Date 03/29/2021

Typed or printed name Winston Hsu Registration No. 41526

Electronic Patent Application Fee Transmittal

Application Number:	16151347
Filing Date:	04-Oct-2018
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Filer:	Roger Gwan-Jye Chen/Edie Hung
Attorney Docket Number:	ETRP0143USA3

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	600	600

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**600**

Electronic Acknowledgement Receipt

EFS ID:	42314842
Application Number:	16151347
International Application Number:	
Confirmation Number:	3080
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Edie Hung
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0143USA3
Receipt Date:	31-MAR-2021
Filing Date:	04-OCT-2018
Time Stamp:	02:53:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$600
RAM confirmation Number	E20213U354322650
Deposit Account	503105
Authorized User	Edie Hung

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	4165641.PDF	762443 c2f28a88208cca5170e4260e4a0e690eeb04 4e35	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30532 0cca51bdd1077fcd7cc00ded4cb9c76cf443 c262	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	792975		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 03/03/2021
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 03/03/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

TITLE OF INVENTION: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	06/03/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 03/03/2021
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

TITLE OF INVENTION: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	06/03/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2135	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

27765 7590 03/03/2021
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 03/03/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/151,347	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 02/25/2021.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1 and 3 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

PART I ***THE EXAMINER'S EVALUATION OF THE APPLICATION***

SECTION A ***RELEVANT ART CITED BY THE EXAMINER***

1. *TAKAHASHI et al. (US 2010/0290300 A1).*
2. *Mohammad (US 2009/0122620 AI).*
3. *NAKANURA (US 2008/0117700 A1).*

SECTION B ***DISTINGUISHING FEATURES RECITED IN THE CLAIMS***

The following is an ***Examiner's Statement of Reasons for Allowance*** *See* ***MPEP 1302.14***

4. The primary reasons for allowance of claims 1 and 3 in the instant application is the combination with the inclusion of the following limitations: **"wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell; wherein DRAM memory cells operate at the first voltage and peripheral circuit operates at the second voltage; wherein the first voltage and the second voltage are capable of making the DRAM applied to an embedded display port (eDP)"**

The prior art of record including the disclosures of TAKAHASHI *et al. (US* 2010/0290300 *A1),* Mohammad *(US* 2009/0122620 *AI),* and NAKANURA *(US*

2008/0117700 A1) neither anticipates nor renders obvious the above-recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays should be clearly labeled "Comments on Statement of Reasons for Allowance"

PART II **THE ATTENTION OF FUTURE CORRESPONDENT**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

February 25, 2021

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/00; Y02D10/14; Y02D10/151	02/25/2021	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE
711	105	02/25/2021	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF
PALM and EAST Inventor Search Updated	04/28/2020	HF
EAST Text Search Updated	04/28/2020	HF
Assignee/ Inventor Search Updated	11/20/2020	HF
EAST Text Search Updated	11/20/2020	HF
Assignee/ Inventor Search Updated	02/25/2021	HF
EAST Text Search Updated	02/25/2021	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE
G11C7/1075	G11C7/00	02/25/2021	HF
G11C11/4074	G11C11/00	02/25/202	HF
G06F12/0882	G06F12/00	02/25/202	HF

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC						
Symbol					**Type**	**Version**
G11C	/	7	/	1075	F	2013-01-01
G11C	/	11	/	4074	I	2013-01-01
G06F	/	12	/	0882	A	2013-01-01
G06F	/	3	/	0653	A	2013-01-01
G06F	/	12	/	0238	A	2013-01-01
G06F	/	13	/	4278	A	2013-01-01
G06F	/	3	/	061	A	2013-01-01
G06F	/	3	/	0656	A	2013-01-01
G06F	/	12	/	0692	A	2013-01-01
G06F	/	12	/	063	A	2013-01-01
G06F	/	12	/	0866	A	2013-01-01
G06F	/	13	/	4221	A	2013-01-01
G11C	/	11	/	40615	A	2013-01-01
Y02D	/	10	/	00	A	2018-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 2	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135 (Primary Examiner)	25 February 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office

Part of Paper No.: 20210225-A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G11C	/	7	/	10

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
711	105

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 2	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135 (Primary Examiner)	25 February 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office

Part of Paper No.: 20210225-A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
	2														
2	3														
	4														
	5														
	6														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 2	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135 (Primary Examiner)	25 February 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office Part of Paper No.: 20210225-A

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	3	((dynamic adj random adj access adj memory) or DRAM) with ((compatible or appl$4 or used or utiliz$4) near5 ((embedded adj display adj port) or eDP))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:01
L3	1	(((dynamic adj random adj access adj memory) or DRAM) with ((compatible or appl$4 or used or utiliz$4) near5 ((embedded adj display adj port) or eDP))).CLM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:04
L4	3	2 AND ((G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/00 OR Y02D10/14 OR Y02D10/151).CPC. OR (711/105).CCLS. OR (G11C7/10 OR G11C11/4074).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:37
L5	56	Yuan-Der-Min.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:40
L6	44	Chang-Yen-An.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:40
L7	117	Huang-Wei-Ming.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:40
L8	1	3 and (L5 or L6 or L7)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2021/02/25 15:40

			EPO; JPO; DERWENT; IBM_TDB			
L9	17	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:40
L12	845	(ETRON adj TECHNOLOGY).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:41
L13	1	9 and 12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:42
L14	0	2 and 12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 15:43

2/25/2021 3:45:24 PM
C:\Users\hfarrokh\Documents\EAST\Workspaces\13922242.wsp

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 3080

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/151,347	10/04/2018 **RULE**	711	2135	ETRP0143USA3

APPLICANTS
Etron Technology, Inc., Hsinchu, TAIWAN;

INVENTORS
Der-Min Yuan, New Taipei City, TAIWAN;
Yen-An Chang, Miaoli County, TAIWAN;
Wei-Ming Huang, Hsinchu County, TAIWAN;

**** CONTINUING DATA ***************************
This application is a CON of 13/922,242 06/19/2013 ABN
which claims benefit of 61/672,287 07/17/2012
and claims benefit of 61/768,406 02/23/2013

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
10/24/2018

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /HASHEM FARROKH/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TAIWAN	1	~~3~~ 2	1

ADDRESS
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

TITLE
DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

FILING FEE RECEIVED		
1720	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/151,347	Filing Date 10/04/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	02/25/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 2	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/TAMMY D MCBETH BROWN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Appl. No.	: 16/151,347	Confirmation No.	3080
First Named Inventor	: Der-Min Yuan		
Filed	: October 4, 2018		
TC/A.U.	: 2135		
Examiner	: FARROKH, HASHEM		
Docket No.	: ETRP0143USA3		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of November 25, 2020, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 4 this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended): A dynamic random access memory (DRAM), comprising:

a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is ~~not greater~~ lower than 1.1V; and

a peripheral circuit electrically connected to the DRAM core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is ~~not greater~~ lower than 1.1V, and

wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell;

wherein the first voltage and the second voltage are capable of making the DRAM ~~is only~~ be applied to an embedded display port (eDP).

2. (canceled)

3. (previously amended): The dynamic random access memory of claim 1, further comprising:

an input/output unit electrically connected to the peripheral circuit and the DRAM core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V.

4. (canceled)

5. (canceled)

6. (canceled)

Electronic Acknowledgement Receipt

EFS ID:	42016931
Application Number:	16151347
International Application Number:	
Confirmation Number:	3080
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Anna Lu
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0143USA3
Receipt Date:	25-FEB-2021
Filing Date:	04-OCT-2018
Time Stamp:	02:12:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	4131395.PDF	654833 866b7afb12e0947202ebc7519daae0c2e521a5c9	no	4

Warnings:

Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	4131394.PDF	81338 6a74d6b97badab4414c3136df185c5c8c832203c	no	1
Warnings:					
Information:					
3	Claims	4131393.PDF	82673 39ffd572599502083f1bba91e8c587dd3a5c3a25	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	818844		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Claim Rejections, 35 U.S.C. 112:

In regarded to claims 1, 3

Response:

Please refer to Figure, Table I, Table II, and paragraphs [0011-0012], [0015] of the present invention. Paragraphs [0011-0012] of the present invention disclose "Please refer to the figure. The figure is a diagram illustrating a **dynamic random access memory 100 applied to an embedded display port** according to an embodiment … **Table I** illustrates **operation voltages** (specified by the Joint Electron Device Engineering Council (JEDEC)) of a dynamic random access memory operating in the DDR I specification, a low power DDR I specification, the DDR II specification, and a low power DDR II specification … But, **the operation voltages** specified by the Joint Electron Device Engineering Council (as shown in Table I) **cannot satisfy requirements (that is, the low operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3**", and paragraph [0015] of the present invention discloses "As shown in Table Ⅱ, because **the operation voltages of the memory core unit 102** in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification **are the first predetermined voltage**, **the dynamic random access memory 100 has lower memory core power consumption**; because the **operation voltages of the peripheral circuit unit 104** in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification **are the second predetermined voltage**, **the dynamic random access memory 100 has lower access power consumption**…**so power consumption of the dynamic random access memory 100 is much lower than power consumption of the**

dynamic random access memory operating in the operation voltages specified by the Joint Electron Device Engineering Council", so according to Table I, Table Ⅱ, and paragraphs [0011-0012], [0015] of the present invention, it is very obvious that **the DRAM 100** provided by the present invention is **only used for solving the problem that the operation voltages** (shown in Table I) **of a DRAM** specified by Joint Electron Device Engineering Council (JEDEC) **cannot satisfy the requirements of the embedded display port (eDP) version 1.3**. Therefore, Table II and paragraph [0015] of the present invention **obviously teach** the technical feature "**the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP)**". Therefore, the previously presented claim 1 of the present invention can be amended according to the above-mentioned technical feature disclosed by Table II and paragraph [0015] of the present invention. In addition, "the first voltage is **not greater** than 1.1V" and "the second voltage is **not greater** than 1.1V" disclosed by the previously presented claim 1 of the present invention are replaced with "the first voltage is **lower** than 1.1V" and "the second voltage is **lower** than 1.1V", respectively. Table I and Table II of the present invention are shown as follows:

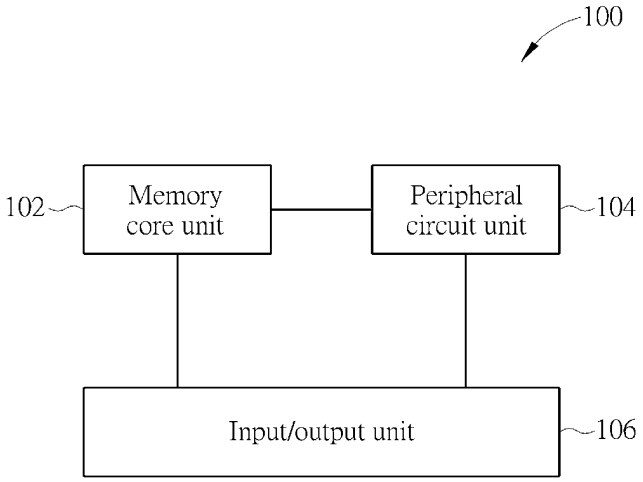
	memory core unit 102	peripheral circuit unit 104	input/output unit 106
DDR I	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V
Low Power DDR I	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
DDR II	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
Low Power DDR II	1.7V~1.95V	1.14V~1.30V	1.14V~1.30V

Table I

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	< 1.1V	< 1.1V	< 1.1V

Table II

In addition, Figure of the present invention is shown as follows:



Figure

To sum up, after the previously presented claim 1 of the present invention are amended, the currently amended claim 1 and the previously presented claim 3 **should not invoke** 35 U.S.C 112(a), or 35 U.S.C 112 (pre-AIA), first paragraph.

2. Claim Rejections, 35 U.S.C. 102(a)(1) & 35 U.S.C. 103:

Response:

The previously presented claims 4-6 are canceled.

To sum up, allowance of the currently amended claim 1 and the previously amended claim 3 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Roger Chen/ Date: 02/25/2021

Roger Chen, Patent Agent No. 67,314
5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan
Voice Mail: 302-729-1562
e-mail : RogerChen@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

27765 7590 11/25/2020
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
11/25/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 16/151,347	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 10/302020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 and 3-6 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 and 3-6 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 10/04/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/30/2020 has been entered.

This Office action is in response to the communication(s) filed on 10/30/2020. There are a total of 5 claims pending in the application. Claim 1 has been amended; claim 2 has been canceled; and claims 4-6 have been added.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to

> *enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

1. Claims 1 and 3-6 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

2. The independent claim 1 has been amended to recite, in part, the limitations:

"wherein the first voltage is not greater than 1.1V; wherein the second voltage is not greater than 1.1V".

The claimed specification does not describe or support the above limitations as claimed. The dependent claim 4 recites similar limitations and is rejected based on the same ground of rejection. The dependent claims 3 and 5-6 are rejected based by virtue of their dependency from their respected independent claims.

2. The independent claim 1 has been amended to recite, in part, the limitation:

"wherein the DRAM is **only** applied to an embedded display port teDP)."

The claimed specification does not describe or support the above limitations as claimed.

3. The independent claim 1 has been amended to recite, in part, the limitation:

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.*

Claims 4-6 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by TAKAHASHI et al. "TAKAHASHI" (US 2010/0290300 A1).

4. In regard to claim 4 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., ¶ 0047; Figs. 1-2)**, comprising: a DRAM core cell comprised in the DRAM **(e.g., ell array 102 in Fig. 1)**, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is not greater than 1.1V;" **(e.g., ¶ 0084, Fig. 8).** *The VDD of bit line (e.g., VDD applied to memory cells is 0.8 v.*

"and a peripheral circuit comprised in the DRAM **(e.g., ¶ 0078; Figs. 1-2)**, wherein the peripheral circuit is electrically connected to the DRAM core cell **[e.g., logic circuit (peripheral circuit) 105 in Fig. 1)**, and the peripheral circuit is supplied with a second

voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V, and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell." **[(e.g., ¶ 0078, the logic circuit 105 serving as a peripheral circuit… further reduced (e.g., VDD is 08 V or lower)].**

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.*

Claim 5-6 are rejected under 35 U.S.C. 103 as being unpatentable over TAKAHASHI in view Applicant Prior Art Admission (APAA).

5. In regard to claims 5-6 TAKAHASHI further teaches:

"wherein the first voltage is different from the second voltage." **(e.g., ¶ 0016 and TABLE III on page 2 of instant specification -- APAA).** *Table III specify the voltage of*

memory core (e.g., first voltage) as 1.8 V +/- 0.1 V and the voltage of peripheral circuit (e.g.. second voltage) as <1.1 V. The two voltages are different.

Paragraph [0016] of the claimed specification recites:

"[0016] Please refer to Table III. **Table III illustrates operation voltage ranges** of the dynamic random access memory 100 operating in the **DDR I specification, the low power DDR I specification, the DDR II specification, and the low power DDR II specification** according to another embodiment."

6. In regard to claim 5 TAKAHASHI further teaches:

"wherein the first voltage is greater than the second voltage." **(e.g., ¶ 0016 and TABLE III on page 2 of instant specification -- APAA).** *Table III specify the voltage of memory core (e.g., first voltage) as 1.8 V +/- 0.1 V and the voltage of peripheral circuit (e.g.. second voltage) as <1.1 V. The two voltages are different. The first voltage 1.8 V is greater than second voltage < 1.1 V*

Response to Remarks

Applicant arguments have been fully considered and they have been persuasive. The previous 103 rejection have been withdrawn. However, the amendments have changed the scope of claims are rejected on new ground of rejection. The claims, as shown above, are rejected under 35 USC 112(a), first paragraph as failing to comply with written description requirement. The newly added independent claim 4 is rejected under 35 USC 102 as being anticipated by TAKAHASHI. TAKAHASHI discloses a DRAM circuit including memory cells array portion and logic circuit (peripheral circuit)

portion. TAKAHASHI further discloses operation voltage two portion are lower than 1.1 V.

Conclusion

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. *The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.*

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2131

November 20, 2020

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF
PALM and EAST Inventor Search Updated	04/28/2020	HF
EAST Text Search Updated	04/28/2020	HF
Assignee/ Inventor Search Updated	11/20/2020	HF
EAST Text Search Updated	11/20/2020	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/21/2019	11/16/2015	10/01/2016	05/14/2017	09/18/2017	05/28/2018			
	1	✓	✓	✓	✓	✓				
	2	✓	-	-	-	-				
	3	✓	✓	✓	✓	✓				
	4					✓				
	5					✓				
	6					✓				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V"))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:02
L2	56	Yuan-Der-Min.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:02
L3	42	Chang-Yen-An.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:02
L4	116	Huang-Wei-Ming.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:02
L5	2	L1 and (L2 or L3 or L4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:02
L6	14	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:03

L7	6,207,650	(ETRON TECHNOLOGY).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:05
L8	1	6 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:06
L9	49	DRAM same ((embedded adj disolay adj port) or eDP)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:07
L10	0	6 and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:07
L11	4	(DRAM same ((embedded adj disolay adj port) or eDP)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:08
L12	0	L11 and (L2 or L3 or L4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:08
L13	6	(DRAM and ((embedded adj disolay adj port) or eDP)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:10

L14	0	13 and (L2 or L3 or L4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:10
L15	1,372	(DRAM and ((embedded adj disolay adj port) or eDP))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:10
L16	31	7 and 15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:11
L17	12	16 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:12
L18	14	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:18
L19	5	L18 AND ((G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/4074 OR G11C7/1075 OR Y02D10/14 OR Y02D10/151).CPC. OR (711/105).CCLS. OR (G11C7/10 OR G11C11/4074).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 23:18
S159	4	"16151347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/11/20 11:34

			DERWENT; IBM_TDB			
S160	1,728	((dynamic adj Random adj Access Memory) or DRAM or SDRAM or DDR) near2 ((integrated adj circuit) or chip or device) with ((operating adj voltage) with (less or lower or smaller) "1.1")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 12:13
S161	0	((dynamic adj Random adj Access Memory) or DRAM or SDRAM or DDR) near2 ((integrated adj circuit) or chip or device) with ((operating adj voltage) with ((less or lower or smaller) near2 "1.1"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 12:16
S162	13	DRAM adj10 ("1.1 v" or "1.1v")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 12:18
S163	6	S162 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 12:21
S164	1,072	((dynamic adj Random adj Access Memory) or DRAM or SDRAM or DDR) near2 ((integrated adj circuit) or chip or device) with "1.1"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 12:24
S165	59	((dynamic adj Random adj Access Memory) or DRAM or SDRAM or DDR) near2 ((integrated adj circuit) or chip or device) with ("1.1 V" or "1.1V")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 12:26
S166	24	S165 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/11/20 12:27

			DERWENT; IBM_TDB			
S167	6	((dynamic adj Random adj Access adj Memory) or DRAM or SDRAM or DDR) near2 ((integrated adj circuit) or chip or device) with ("1.1 V" or "1.1V")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 12:35
S168	4	(operating adj voltage) near5 ((less or lower or smaller) adj2 ("1.1 V" or "1.1V"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:01
S169	0	S168 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:02
S170	13	(VDD or (supply adj voltage)) near5 ((less or lower or smaller) adj2 ("1.1 V" or "1.1V"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:03
S171	8	S170 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:03
S172	16	DRAM with ((supply adj volate) or VDD) with ("1.1 v" or "1.1v")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:14
S173	5	S172 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/11/20 14:14

			DERWENT; IBM_TDB			
S174	7	((DRAM OR DDR) adj (chip or die or ASIC)) and (small near5 (operating adj voltage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:32
S175	7	S174 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:32
S176	10	((DRAM OR DDR) adj (chip or die or ASIC)) and (small near5 (VDD))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:34
S177	9	S176 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:35
S178	4	((DRAM OR DDR) adj (chip or die or ASIC)) and (("1.1 V" OR "1.1V") near5 (VDD))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:38
S179	12	((DRAM OR DDR) adj (chip or die or ASIC)) and (("1.0 V" OR "1.0V") near5 (VDD))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 14:42
S180	0	S179 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/11/20 14:42

			DERWENT; IBM_TDB			
S181	0	"20100290300".pn. and (VDD with (memory adj cell))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 15:36
S182	1	"20100290300".pn. and (VDD same (memory adj cell))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 15:37
S183	53	DRAM same (((embedd$3 near2 display) near2 (port or interface or link or bus or path)) or eDP)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 15:54
S184	16	S183 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 15:54
S185	18,188	(DRAM or DDR) with display	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 17:48
S186	1,392	(DRAM or DDR) with (display near2 (port or interface))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 17:49
S187	27	(DRAM or DDR) near2 (display near2 (port or interface))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/11/20 17:49

			DERWENT; IBM_TDB			
S188	17	S187 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 17:50
S189	1,298	embedded near5 display near5 port	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 18:01
S190	445	S189 and (dram or ddr)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 18:02
S191	10	S189 same (dram or ddr)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 18:02
S192	2	S191 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 18:02
S193	908	embedded adj display adj port	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 18:04
S194	14,974	(embedded adj display adj port) or eDP	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/11/20 18:05

			DERWENT; IBM_TDB			
S195	908	S193 and S194	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 18:05
S196	304	S195 and (?DRAM OR DDR)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 18:06
S197	3	S196 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/11/20 18:06

11/20/2020 11:20:51 PM
C:\Users\hfarrokh\Documents\EAST\Workspaces\13922242.wsp

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/151,347	Filing Date 10/04/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	10/30/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 5	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/KIMBERLY D WILLIAMS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/30EFS (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16/151,347	Filing Date	2018-10-04	Docket Number (if applicable)	ETRP0143USA3	Art Unit	2135
First Named Inventor	Der-Min Yuan			Examiner Name	FARROKH, HASHEM		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☒ Other Extension of time

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503105

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature
☐ Applicant Signature

PTO/SB/30EFS (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2020-10-30
Name	Winston Hsu	Registration Number	41526

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	16151347
Filing Date:	04-Oct-2018
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Filer:	Roger Gwan-Jye Chen/Jessie Su
Attorney Docket Number:	ETRP0143USA3

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	2253	1	740	740
Miscellaneous:				
RCE- 2ND AND SUBSEQUENT REQUEST	2820	1	1000	1000
		Total in USD ($)		**1740**

Electronic Acknowledgement Receipt

EFS ID:	40990924
Application Number:	16151347
International Application Number:	
Confirmation Number:	3080
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Jessie Su
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0143USA3
Receipt Date:	30-OCT-2020
Filing Date:	04-OCT-2018
Time Stamp:	05:02:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1740
RAM confirmation Number	E20200T602551646
Deposit Account	503105
Authorized User	Jessie Su

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.16 (National application filing, search, and examination fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	4006325.PDF	946093 c51716cb0cc4785e494ab2ac156f842abc1585da	no	13
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	4006324.PDF	85965 af087982f8394885886f446f541dc6f6a8d32565	no	1
Warnings:					
Information:					
3	Claims	4006323.PDF	89368 f9fcc9110ac8317c9faa6aca709eb132b77ad5d6	no	2
Warnings:					
Information:					
4	Extension of Time	4006304.PDF	630866 96783dffc7a0b5e208c309655f5c1b33561d101f	no	1
Warnings:					
Information:					
5	Request for Continued Examination (RCE)	4006303.pdf	324887 dfa47345ca3133c8a402d4846a1320d3e8abd849	no	3
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	32497 bc13de537f75403f3e8f9217103a398d09db add4	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	2109676

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Amendment of Claims:

The previously presented claim 1 is amended according to Table II and paragraph [0015] of the present invention, the new claim 4 is introduced according to Figure of the present invention and the previously presented claim 1 of the present invention, and the new claims 5, 6 are introduced according to Table Ⅲ of the present invention. No new matter is introduced. Allowance of the claim amendments is politely requested.

2. Rejections of claims under 35 U.S.C. 103:

In regarded to claim 1

Response:

Please refer to Figure, Table I, Table II, and paragraphs [0011-0012], [0015] of the present invention. Paragraphs [0011-0012] of the present invention disclose "Please refer to the figure. The figure is a diagram illustrating a **dynamic random access memory 100 applied to an embedded display port** according to an embodiment … **Table I** illustrates **operation voltages** (specified by the Joint Electron Device Engineering Council (JEDEC)) of a dynamic random access memory operating in the DDR I specification, a low power DDR I specification, the DDR II specification, and a low power DDR II specification … But, **the operation voltages** specified by the Joint Electron Device Engineering Council (as shown in Table I) **cannot satisfy**

requirements (that is, the low operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3", and paragraph [0015] of the present invention discloses "As shown in Table Ⅱ, because **the operation voltages of the memory core unit 102** in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification **are the first predetermined voltage**, **the dynamic random access memory 100 has lower memory core power consumption**; because the **operation voltages of the peripheral circuit unit 104** in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification **are the second predetermined voltage**, **the dynamic random access memory 100 has lower access power consumption**…**so power consumption of the dynamic random access memory 100 is much lower than power consumption of the dynamic random access memory operating in the operation voltages** specified by the Joint Electron Device Engineering Council", so according to Table I, Table Ⅱ, and paragraphs [0011-0012], [0015] of the present invention, it is very obvious that **the DRAM 100** provided by the present invention is **only used for solving the problem that the operation voltages** (shown in Table I) **of a DRAM** specified by Joint Electron Device Engineering Council (JEDEC) **cannot satisfy the requirements of the embedded display port (eDP) version 1.3**. Therefore, Table II and paragraph [0015] of the present invention **obviously teach** the technical feature "**the DRAM is only applied to an embedded display port (eDP)**". Table I and Table II of the present invention are shown as follows:

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
DDR I	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V
Low Power DDR I	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
DDR II	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
Low Power	1.7V~1.95V	1.14V~1.30V	1.14V~1.30V

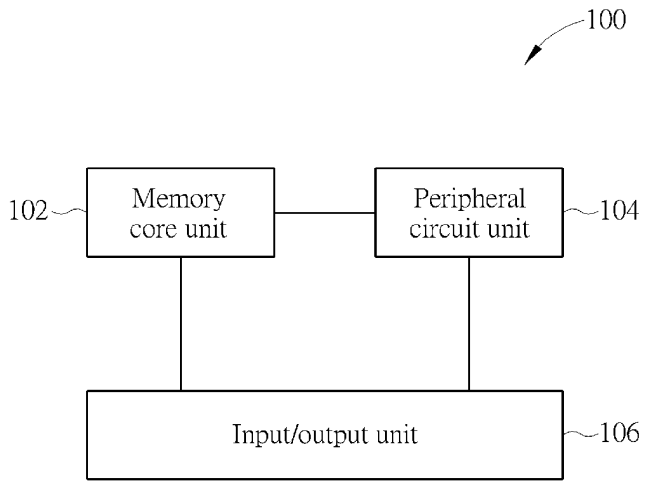
DDR II			

Table I

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	< 1.1V	< 1.1V	< 1.1V

Table II

In addition, Figure of the present invention is shown as follows:



Figure

However, please refer to FIG. 5 and paragraph [0004] of Mohammad (US20090122620). Paragraph [0004] of Mohammad discloses "**One problem with increased usage of SRAM in computing devices is that accesses to such memory**

incurs power usage that may affect the battery life of the computing device. **One problem in decreasing power usage of the SRAM includes a decreased access success rate of the memory**", so according to FIG. 5 of Mohammad, although the examiner holds that **the memory cells 502 and the MUX/Demux logic 516** of Mohammad **can be referred to the DRAM core cell and the peripheral circuit** of the present invention respectively, according to paragraph [0004] of Mohammad, it is very obvious that Mohammad is **not used for providing a DRAM applied to the embedded display port (eDP) version 1.3**. FIG. 5 of Mohammad is shown as follows:

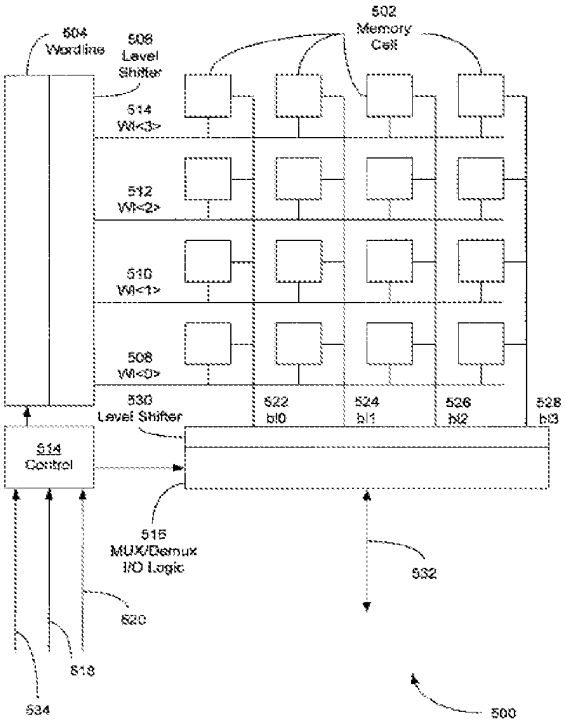


FIG. 5

In addition, please refer to paragraph [0021] of Takahashi (US20100290300). Paragraph [0021] of Takahashi discloses "The present inventors have found **a problem as described below**. In the technique disclosed in Patent Document 1, a **thick-film transistor is used as a central transistor of a memory cell, and a thin-film transistor, which is used for a logic circuit**, **is used as a precharge MOS transistor and a sense amplifier**. Patent Document 1 discloses that a **high voltage is not applied to** the

precharge MOS transistor **which is formed of a thin-film transistor**. However, unless a **voltage higher than** the power supply voltage as in the semiconductor memory circuit 1 is applied to the transistor for use in the precharge circuit, **the operation speed of the precharge circuit cannot be increased**. Accordingly, the present inventors have found **a problem** that the **semiconductor integrated device** fabricated using the technique as **disclosed in Patent Document 1** **has a limitation in achieving a higher speed operation**", so according to paragraph [0021] of Takahashi, Takahashi is very obviously **used for solving a problem** of **Patent Document 1** **having a limitation in achieving a higher speed operation**, that is, Takahashi is **also not used for providing a DRAM applied to the embedded display port (eDP) version 1.3**.

Therefore, because according to paragraph [0004] of Mohammad, Mohammad is **not used for providing a DRAM applied to the embedded display port (eDP) version 1.3**, and according to paragraph [0021] of Takahashi, Takahashi **is also not used for providing a DRAM applied to the embedded display port (eDP) version 1.3**, it is very obvious that both Mohammad and Takahashi **obviously fail to teach** the technical feature "**the DRAM** **is only applied to an embedded display port (eDP)**" disclosed by Table II and paragraph [0015] of the present invention.

In addition, please refer to FIGS. 1, 7 and paragraphs [0043], [0078] of Takahashi. Paragraph [0043] of Takahashi discloses "In the first exemplary embodiment, the present invention is applied to a semiconductor integrated device 100 such as a system LSI…As shown in FIG. 1, **the semiconductor integrated device 100** **includes a semiconductor memory circuit 101 and a logic circuit 105**", and paragraph [0078] of Takahashi discloses "**The semiconductor integrated device 200** **includes the semiconductor memory circuit 201 and the logic circuit 105**…The second exemplary embodiment assumes the case where transistors constituting **the logic circuit 105** **serving as a peripheral circuit** **of the semiconductor memory circuit 201** are further reduced in film thickness and the power supply voltage is also further reduced (e.g., **VDD is 0.8 V or lower**) as compared with the first exemplary embodiment", so according to paragraphs

[0043], [0078] of Takahashi, it is obviously that **both the semiconductor memory circuit 101 and semiconductor memory circuit 201** **do not include the logic circuit 105**, wherein the **semiconductor memory circuit 101 and the semiconductor memory circuit 201** **can be referred to** **the DRAM** of the present invention**,** that is, **the logic circuit 105** of Takahashi **cannot be referred to** **the peripheral circuit** of the present invention. Therfore, Takahashi **fails to teach** the technical feature "**peripheral circuit included in the DRAM**" disclosed by Figure of the present invention. FIGS. 1, 7 of Takahashi are shown as follows:

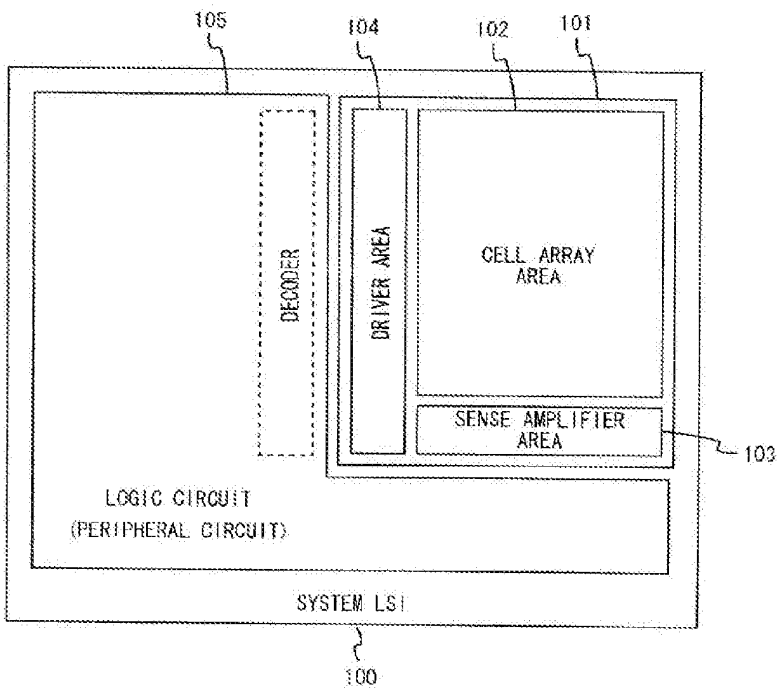


Fig. 1

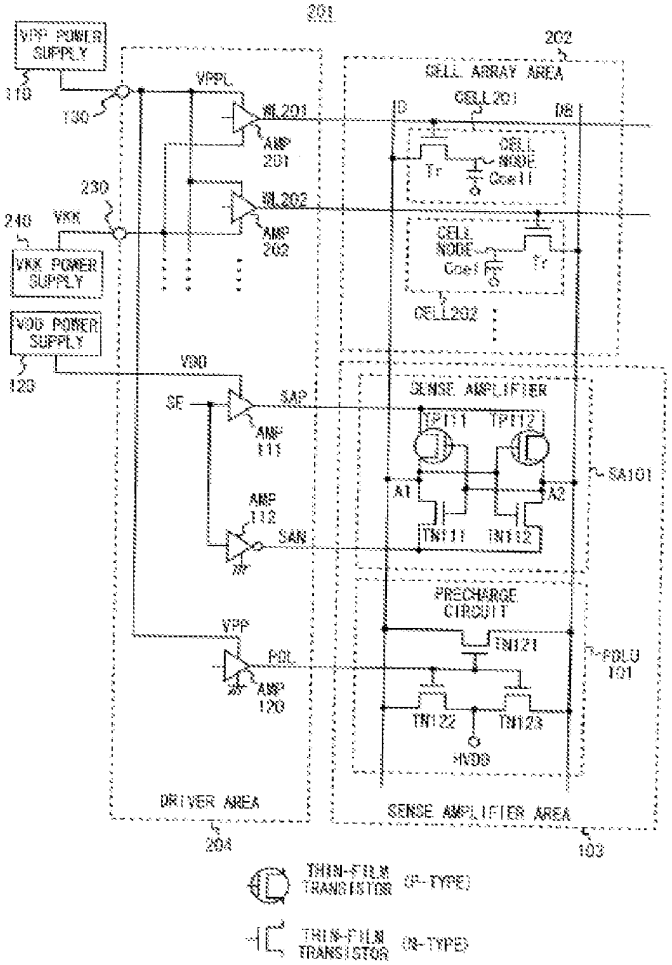
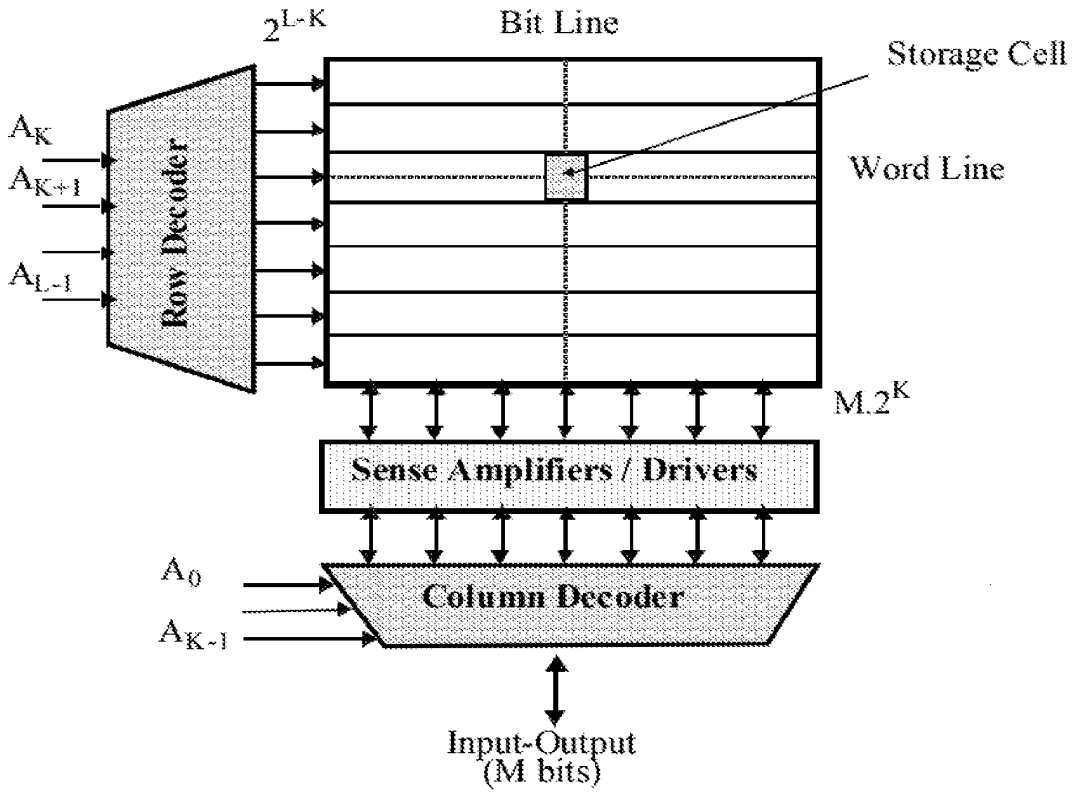


Fig. 7

In addition, please refer to the reference figure (**<u>array-structured memory</u>** which is obvious to one of ordinary skill in the art, **from website: https://my.eng.utah.edu/~cs6710/slides/memoryx6.pdf**). As shown in the reference figure, because the reference figure **<u>relates to</u> array-structured <u>memory</u>** and Figure of the present invention **<u>also relates to</u> the dynamic random access <u>memory</u> 100**, **storage cell** of the reference figure **<u>can be just referred to</u> the memory core unit** of the present invention, and **<u>row decoder, sense amplifiers/drivers, and column decoder</u>** of the

reference figure **can be just referred to** **the peripheral circuit unit 104** of the present invention. Therefore, according to the reference figure, although paragraph [0078] of Takahashi discloses "**the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201**", it is obvious that **the logic circuit 105 is not row decoder, sense amplifiers/drivers, and column decoder** (shown in the reference figure) in the **array-structured memory**, so according to the reference figure**, the logic circuit 105** of Takahashi **still cannot be referred to the peripheral circuit** of the present invention. That is, according to the reference figure**,** Takahashi **still fails to teach** the technical feature "**peripheral circuit included in the DRAM**" disclosed by Figure of the present invention. The reference figure is shown as follows:



Therefore, even if **the power supply voltage for the logic circuit 105** of Takahashi

can be reduced 0.8V or lower, but because **the logic circuit 105** of Takahashi **cannot be referred to the peripheral circuit** of the present invention, Takahashi **still fails to teach** the technical feature "**the DRAM is only applied to an embedded display port (eDP)**" disclosed by Table II and paragraph [0015] of the present invention.

Therefore, because both Mohammad and Takahashi obviously **fail to teach** the technical feature "**the DRAM is only applied to an embedded display port (eDP)**" disclosed by Table II and paragraph [0015] of the present invention, the currently amended claim 1 of the present invention should be patentable over Mohammad and Takahashi after the previously presented claim 1 of the present invention is amended according to the above-mentioned technical feature disclosed by Table II and paragraph [0015] of the present invention.

In regarded to claim 4

Response:

Please refer to FIGS. 3, 4 and paragraph [0047] of Mohammad. Paragraph [0047] of Mohammad discloses "FIG. 5 is a diagram illustrating a **memory 500 including level shifter/voltage scaling circuit 302** of FIG. 3 **for the wordline logic 504** and **MUX/Demux logic 516 and level shifter/voltage scaling circuit 402** of FIG. 4 **for the memory cells 502**", wherein the examiner holds that **the memory cells 502 and the MUX/Demux logic 516** of Mohammad **can be referred to the DRAM core cell and the peripheral circuit** of the present invention respectively. As shown in FIGS. 3, 4 of Mohammad, **both the level shifter/voltage scaling circuit 302 and the level shifter/voltage scaling circuit 402 receive the same voltage** (i.e. **the Vdd 206**), that is, **the same voltage** (i.e. **the Vdd 206**) **are provided to the memory cells 502 and the MUX/Demux logic 516** of Mohammad. However, the previously presented claim 1 of the present invention discloses "**the DRAM core cell is supplied with a first voltage; the peripheral circuit is supplied with a second voltage**". That is, according to the previously presented claim 1 of the present invention, **in the same chip** (i.e. **the DRAM**), **the DRAM core cell and the peripheral circuit receive different voltages** (i.e. **the first**

voltage and the second voltage) **less than 1.1V**. Therefore, because according to the previously presented claim 1 of the present invention, **in the same chip** (i.e. **the DRAM**), **the DRAM core cell and the peripheral circuit** **receive different voltages less than 1.1V**, but according to FIGS. 3, 4 of Mohammad, **both the level shifter/voltage scaling circuit 302 and the level shifter/voltage scaling circuit 402** **receive the same voltage**, **the memory cells 502 and the MUX/Demux logic 516** of Mohammad **cannot be referred to** **the DRAM core cell and the peripheral circuit** of the present invention respectively. That is, Mohammad obviously **fails to teach** the technical features "**DRAM core cell comprised in the DRAM; peripheral circuit comprised in the DRAM**". In addition, because Mohammad **only teaches** that **both the level shifter/voltage scaling circuit 302 and the level shifter/voltage scaling circuit 402** **receive the same voltage**, Mohammad also **fails to teach** the technical features "**the first voltage is different from the second voltage**" and "**the first voltage is greater than the second voltage**" disclosed in Table III of the present invention. FIGS. 3, 4 of Mohammad are shown as follows:

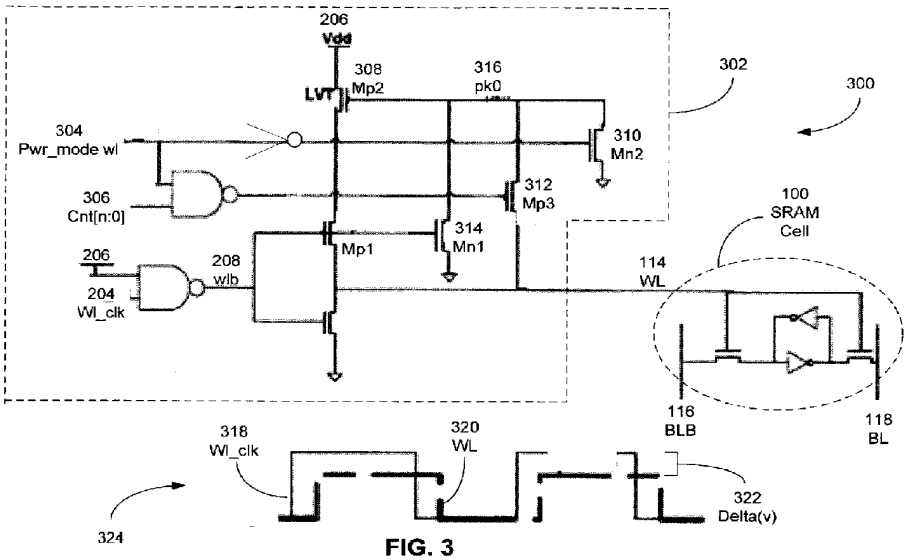


FIG. 3

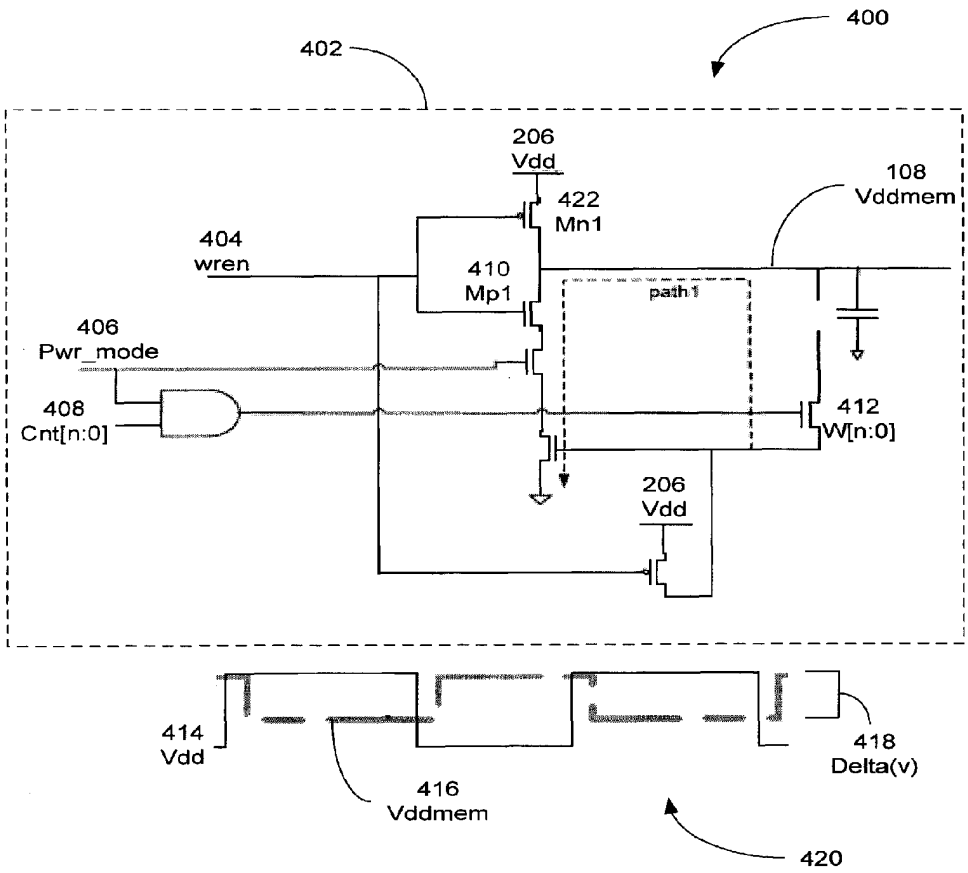


FIG. 4

Table III of the present invention is shown as follows:

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	1.8V±0.1V	< 1.1V	< 1.1V

In addition, because according to paragraphs [0043], [0078] of Takahashi and the reference figure, Takahashi obviously **fails to teach** the technical feature "**peripheral**

circuit comprised in the DRAM" disclosed by Figure of the present invention, of course, Takahashi also obviously **fails to teach** the technical features "**the first voltage is <u>different from</u> the second voltage**" and "**the first voltage is <u>greater than</u> the second voltage**" disclosed in Table Ⅲ of the present invention.

Therefore, because both Takahashi and Mohammad obviously **fail to teach** the technical features "**DRAM core cell t comprised in the DRAM; peripheral circuit comprised in the DRAM**" disclosed by Figure of the present invention, and "**the first voltage is <u>different from</u> the second voltage**" and "**the first voltage is <u>greater than</u> the second voltage**" disclosed in Table Ⅲ of the present invention, the new claim 4 of the present invention should be patentable over Mohammad and Takahashi, wherein the new claim 4 of the present invention is introduced according to the technical feature "**peripheral circuit comprised in the DRAM**" disclosed by Figure of the present invention and the previously presented claim 1 of the present invention.

To sum up, allowance of the currently amended claim 1, the new claims 4-6, and the previously amended claim 3 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Winston Hsu/ Date: 10/30/2020

Winston Hsu, Patent Agent No. 41,526
5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan
Voice Mail: 302-729-1562
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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Appl. No.	: 16/151,347	Confirmation No.	: 3080
First Named Inventor	: Der-Min Yuan		
Filed	: October 4, 2018		
TC/A.U.	: 2135		
Examiner	: FARROKH, HASHEM		
Docket No.	: ETRP0143USA3		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

In response to the Office action of May 1, 2020, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended): A dynamic random access memory (DRAM)~~ applied to an embedded display port (eDP)~~, comprising:

a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is ~~lower~~ not greater than 1.1V; and

a peripheral circuit electrically connected to the DRAM core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is ~~lower~~ not greater than 1.1V, and

wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell;

wherein the DRAM is only applied to an embedded display port (eDP).

2. (canceled)

3. (previously amended): The dynamic random access memory of claim 1, further comprising:

an input/output unit electrically connected to the peripheral circuit and the DRAM core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V.

4. (new): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM

core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is not greater than 1.1V; and

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V, and

wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell.

5. (new): The dynamic random access memory of claim 4, wherein the first voltage is different from the second voltage.

6. (new): The dynamic random access memory of claim 4, wherein the first voltage is greater than the second voltage.

PTO/AIA/22 (10-20)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): ETRP0143USA3

Application Number: 16/151,347 | Filed: 10/04/2018

For: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Art Unit: 2135 | Examiner: FARROKH, HASHEM

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	Micro Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$220	$110	$55	$
☐	Two months (37 CFR 1.17(a)(2))	$640	$320	$160	$
☑	Three months (37 CFR 1.17(a)(3))	$1,480	$740	$370	$ 740.00
☐	Four months (37 CFR 1.17(a)(4))	$2,320	$1,160	$580	$
☐	Five months (37 CFR 1.17(a)(5))	$3,160	$1,580	$790	$

☑ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☑ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-3105.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 41526.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Winston Hsu/	10/30/2020
Signature	Date
Winston Hsu	3027291562
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

UNITED STATES PATENT AND TRADEMARK OFFICE

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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
16/151,347	10/04/2018	Etron Technology, Inc.	ETRP0143USA3	119923

Acknowledgement of Change to Small Entity Status

The entity status change request below filed through Private PAIR on 08/31/2020 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant asserting small entity status. See 37 CFR 1.27.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Winston Hsu/
Name:	Winston Hsu
Registration Number:	41526

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

27765 7590 05/01/2020
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2131	

NOTIFICATION DATE	DELIVERY MODE
05/01/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 16/151,347	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 02/14/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 and 3 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 and 3 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 10/04/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This Office action is in response to the communication(s) filed on 02/14/2020. There are a total of 2 claims pending in the application. Claim 1 has been amended; claim 2 has been canceled; no new claims have been added.

INFORMATION CONCERNING CLAIMS:

Claim Rejections 35 USC §103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 3 are rejected under 35 U.S.C. 103 as being unpatentable over Mohammad "Mohammad" (US 2009/0122620) in view of TAKAHASHI et al. "TAKAHASHI" (US 2010/0290300 A1).

2. In regard to claim 1 Mohammad teaches:

A dynamic random access memory (DRAM) applied to an embedded display port (eDP), **(e.g., ¶ 0003)**, *comprising:"*

"a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage (e.g., ¶ 0045), and the DRAM core cell is a volatile memory cell;" **(e.g., ¶¶ 0045-0047; Figs. 3-5).**

"and a peripheral circuit **(e.g., Mux/Demux and I/O logic 518 in Figs. 5 and 6)** electrically connected to the DRAM core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage **(e.g., ¶¶ 0058-0063; Figs. 9-11; Low power, high yield memory as described above may be included in any processing devices including a memory, such as SRAM),** and wherein the memory core cell and the peripheral circuit are formed on a single chip **(e.g., ¶¶ 0061-0062; with the voltage level for low power, high yield memory used in circuits including DSP and display controller being less than 1.1V)**, and the peripheral circuit is external to the memory core cell," **(e.g., ¶¶ 0047 and 51; element 516 in Fig. 5)**. *Mux/Demux and I/O logic denoted as element 516 comprise peripheral circuit. However, Mohammad does not expressly teach while TAKAHASHI discloses:*

"DRAM core cell operate at first voltage, wherein the first voltage lower than 1.1V; and the peripheral circuit operate at the second voltage, wherein the second

voltage is lower than 1.1V;" **(e.g., ¶¶ 0078-0079; Figs. 1 and 7)** *power supply voltage further reduced (e.g., VDD is 0.8 V or lower).*

Disclosures by Mohammad and TAKAHASHI are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the systems and methods for low power, high yield memory taught by Mohammad to include the DRAM operating with a power supply voltage (VDD) of lower than 0.8V or lower disclosed by TAKAHASHI.

The motivation for including the DRAM operating at the supply voltage of 0.8 V or lower as taught by paragraph [0018] of TAKAHASHI is due the reduction in the DRAM parameter sizes; the reduction in the DRAM parameter sizes provides higher level of integration and higher operating speed.

Therefore, it would have been obvious to combine teaching of TAKAHASHI with Mohammad to obtain the invention as specified in the claim.

3. In regard to claim 3 Mohammad further teaches:

"An input/output unit electrically connected to the peripheral circuit and the memory core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V." **(e.g., ¶ 0045, ¶¶ 0049~0051, ¶¶ 0070-0077; Figs. 8-9; the low power, high yield memory includes input/output circuits to read/write data from/to memory cells).**

Response to Remarks

Applicant arguments have been fully considered but they are not persuasive.

Applicant has amended the independent claim 1 to replace "an interface port" with "an embedded DRAM port (eDP)". Page 4 of the Remarks states: "that dynamic access memory 100 shown in Figure of the present invention) is the DRAM satisfying the requirement of the embedded display port version 1.3. Table I of the present invention is shown as follows:"

There is nothing in table I that indicates the operating voltage is lower than 1.1 V. However, Table II of the specification shows that the operating voltage may be lower that 1.1 V. Thus, the rejection under 35 USC § 112(a) is withdrawn. Pages 5 and 14 of the Remarks make references to various portions of Mohammad disclosure and concludes that the method 700 is only applied to the SRAM rather than applying to the RAM without stating why the method 700 is only can be applied to SRAM. The Examiner agrees with the Applicant that the memory structure described by Mohammad for, most part, directed to structure of a SRAM. However, paragraph [0025] of Mohammad discloses:

"[0025] FIG. 1 is a prior art schematic illustrating a conventional six transistor (6T) SRAM cell 100. While the inventive concepts are described as being included in SRAM, **the inventive concepts may be included in other types of memory including, but not limited to, SDRAM.** The SRAM cell 100 includes two transistor pairs 104, 106 to connect the SRAM cell to Vddmem 108 and ground. Transistors PG1 110 and PG2 112 may be controlled by wordline (WL) voltage 114 and are used to access the memory cell 100 during read or write." *(Emphasis added).*

The Examiner respectfully submits that the SDRAM is considered to be a DRAM (e.g., synchronous DRAM). Furthermore, the disclosure by Takahashi describes a semiconductor memory device comprising a DRAM. Page 14 of the Remarks recites:

"it is very obvious that semiconductor memory circuit 201 is **a DRAM applied to the system LSI, rather than a DRAM applied to the embedded display port (eDP)**. Therefore, **Takahashi obviously fails to disclose the technical feature "dynamic random access memory (DRAM) applied to an interface port embedded display port (eDP) as presented** in the current amendment of claim 1"

Examiner respectfully submits that the DRAM disclosed comprises system LSI (e.g., see Figure 1 of TAKAHASHI), it DRAM core, peripheral, and other logic circuits.

Examiner further notes that the amendment and addition of phrase "embedded display port (eDP)" *is to the preamble of the claim 1 and does not affect the steps in the body of the claims that follow, therefore eDP does not have a patentable weight on the claim. Therefore, The Examiner respectfully submits that combination of Mohammed and TAKAHASHI teach or render obvious all limitations recited in claim including the newly added limitation(s). Accordingly, the Examiner maintain his position.*

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ann Lo can be reached on (571)272-9767. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2131

April 28, 2020

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF
PALM and EAST Inventor Search Updated	04/28/2020	HF
EAST Text Search Updated	04/28/2020	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/21/2019	11/16/2015	10/01/2016	05/14/2017	09/18/2017	05/28/2018			
	1	✓	✓	✓	✓					
	2	✓	-	-	-					
	3	✓	✓	✓	✓					

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	388	((embedded adj display adj port)) and (DRAM OR SDRAM or DDR)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 10:58
L10	368	9 and eDP	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 10:59
L11	7	10 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 10:59
L13	2	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V"))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:18
L14	56	Yuan-Der-Min.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:18
L15	38	Chang-Yen-An.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:18

L16	116	Huang-Wei-Ming.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:18
L17	2	L13 and (L14 or L15 or L16)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:18
L18	12	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:20
L19	5	L18 AND ((G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/4074 OR G11C7/1075 OR Y02D10/14 OR Y02D10/151).CPC. OR (711/105).CCLS. OR (G11C7/10 OR G11C11/4074).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:20
L20	822	(ETRON near2 TECHNOLOGY).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:22
L21	12	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:23
L22	1	20 and 21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/04/28 12:24

			DERWENT; IBM_TDB			
L23	5	21 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/04/28 12:24

4/28/2020 12:28:12 PM
C:\Users\hfarrokh\Documents\EAST\Workspaces\13922242.wsp

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/151,347	Filing Date 10/04/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	02/14/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 2	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/CAROL A BARNES/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Appl. No.	: 16/151,347	Confirmation No.	3080
First Named Inventor	: Der-Min Yuan		
Filed	: October 4, 2018		
TC/A.U.	: 2131		
Examiner	: FARROKH, HASHEM		
Docket No.	: ETRP0143USA3		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of November 15, 2019, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended): A dynamic random access memory (DRAM) applied to an ~~interface port~~ embedded display port (eDP), comprising:

   a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than ~~0.8V~~ 1.1V; and

   a peripheral circuit electrically connected to the DRAM core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than ~~0.8V~~ 1.1V, and

   wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell.

2. (canceled)

3. (previously amended): The dynamic random access memory of claim 1, further comprising:

   an input/output unit electrically connected to the peripheral circuit and the DRAM core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V.

Electronic Acknowledgement Receipt

EFS ID:	38587220
Application Number:	16151347
International Application Number:	
Confirmation Number:	3080
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Jessie Su
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0143USA3
Receipt Date:	14-FEB-2020
Filing Date:	04-OCT-2018
Time Stamp:	03:17:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	3732381.PDF	785443 6e86b19e8d21128f25712e37f96247c780078be3	no	15

Warnings:

Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	3732380.PDF	85914 553accf030a75b2143fbfa2b9b5bf88b071fa edc	no	1
Warnings:					
Information:					
3	Claims	3732379.PDF	86458 e9c97b88df76521af186d56ea2506de8b6fe ffc5	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	957815		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Claim Rejections, 35 U.S.C. 112:

The applicant amends "**lower than 0.8V**" of the previously presented claim 1 to "**lower than 1.1V**" to overcome 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph. No new matter is introduced. Allowance of the currently amended claim 1 is politely requested.

2. Amendment of Claims:

The previously presented claim 1 is further amended according to Figure, Table I, and paragraphs [0011-0012] of the present invention. No new matter is introduced. Allowance of the claim amendments is politely requested.

3. Rejections of claims under 35 U.S.C. 103:

Response:

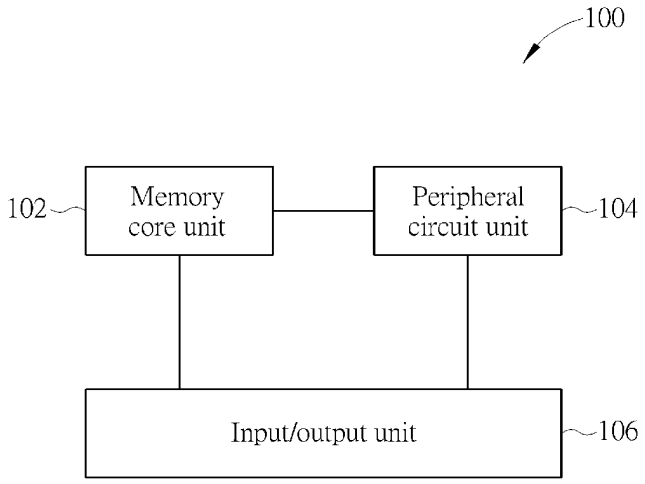
Please refer to Figure, Table I, and paragraphs [0011-0012] of the present invention. Paragraphs [0011-0012] of the present invention disclose "Please refer to the figure. The figure is a diagram illustrating a **dynamic random access memory 100 applied to an embedded display port** according to an embodiment … Table I illustrates operation voltages (specified by the Joint Electron Device Engineering Council (JEDEC)) of a dynamic random access memory operating in the DDR I specification, a low power DDR I specification, the DDR II specification, and a low power DDR II specification … But, **the operation voltages specified by the Joint Electron Device Engineering Council (as shown in Table I) cannot satisfy requirements (that is, the low operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3,**" so according to Figure, Table I, and

paragraphs [0011-0012] of the present invention, it is very obvious that the present invention **is used for solving the problem that <u>operation voltages of a DRAM applied to the embedded display port</u> specified by Joint Electron Device Engineering Council (JEDEC) <u>cannot satisfy requirements of the embedded display port (eDP) version 1.3</u>**. Therefore, it is very obvious that **dynamic random access memory 100** (shown in Figure of the present invention) **is <u>the DRAM satisfying the requirements of the embedded display port version 1.3</u>**. Table I of the present invention is shown as follows:

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
DDR I	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V
Low Power DDR I	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
DDR II	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
Low Power DDR II	1.7V~1.95V	1.14V~1.30V	1.14V~1.30V

Table I

In addition, Figure of the present invention is shown as follows:



Figure

However, please refer to FIGS. 5, 7 and paragraphs [0048], [0053-0054] of Mohammad (US20090122620). Paragraph [0048] of Mohammad discloses "Referring to the diagram of FIG. 5, **memory 500 includes memory cells 502 <u>(e.g., a 6T SRAM cell)</u>**," and paragraphs [0053-0054] of Mohammad disclose "**<u>If a read is to be performed</u>, then the wordline logic 504 scales the WL voltage and the logic 516 scales the BL voltage in 706** … **If a read is not to be performed <u>(i.e., a write is to be performed)</u> in 704, then the circuit 402 (FIG. 4) of the memory cell scales the supply voltage Vddmem in 710,**" so according to FIGS. 5, 7 and paragraphs [0048], [0053-0054] of Mohammad, it is very obvious that **<u>memory 500 is an SRAM</u>**. In addition, Step 704 of method 700 shown in FIG. 7 of Mohammad determines whether the computing devices performs the memory read or not, wherein **when the computing devices performs the memory read**, **Step 706 scales WL voltage and BL voltage**; and **when the computing devices does not perform the memory read** (that is, **performs the memory write), Step 710 scales supply voltage Vddmem**. However, because FIG. 7

of Mohammad **<u>does not disclose</u>** **that WL voltage, BL voltage, and supply voltage Vddmem are scaled <u>under situations other than the computing devices performing the memory read/write</u>**, and **<u>a DRAM</u>** **needs to scale WL voltage, BL voltage, and supply voltage Vddmem <u>under the situations other than the computing devices performing the memory read/write</u>** (for example, **<u>refreshing voltages saved by DRAM cells of the DRAM</u>**), **method 700 <u>is only applied to the SRAM rather than applying to the DRAM</u>**. FIGS. 5, 7 of Mohammad are shown as follows:

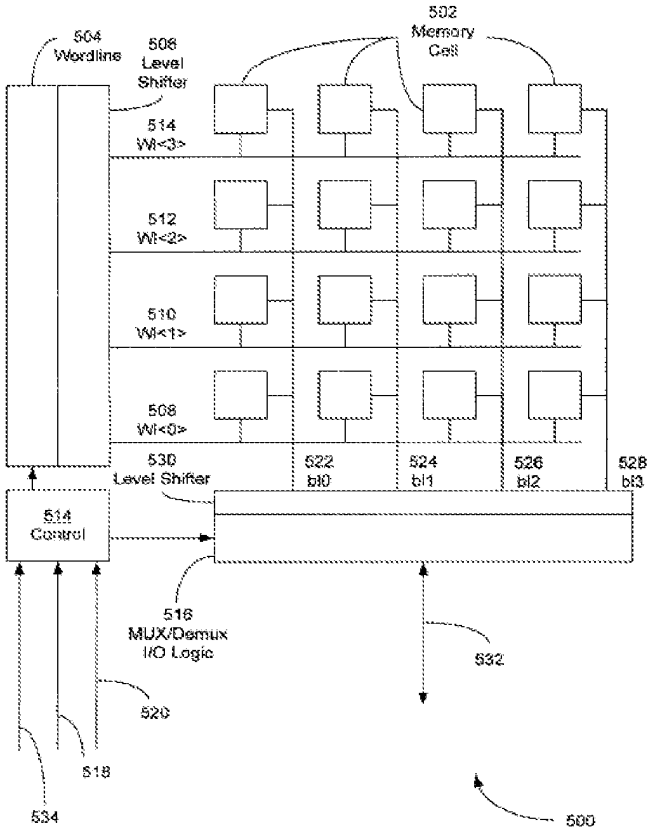


FIG. 5

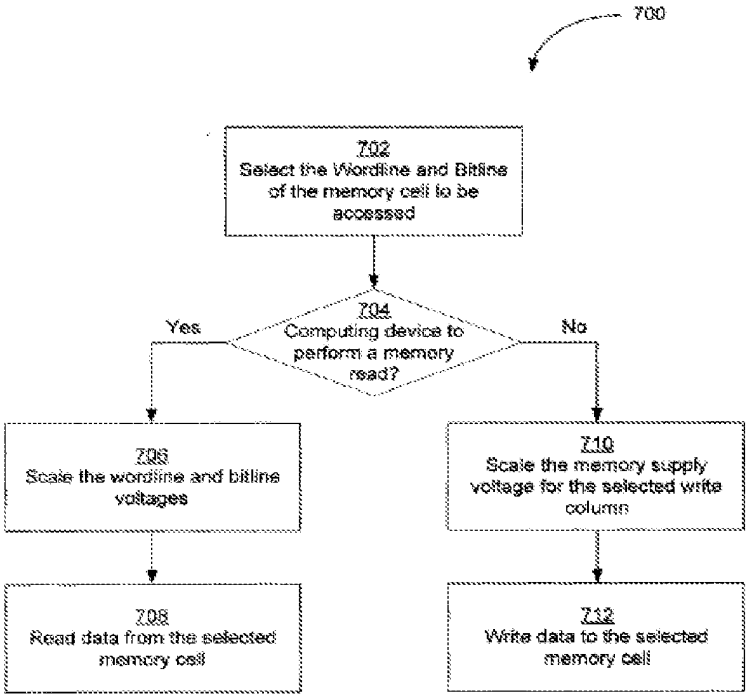


FIG. 7

In addition, please refer to FIGS. 3-5 and paragraphs [0003-0004], [0045-0047] of Mohammad. Paragraphs [0003-0004] of Mohammad disclose "As a result of the ever-increasing gap between processor frequencies and DRAM access times, **processors have steadily been using more on-die static random access memory (SRAM) to meet performance targets**. Presently, SRAM arrays are in over 70% of devices and use 50% of the chip area. **One problem with increased usage of SRAM in computing devices is that accesses to such memory incurs power usage that may affect the battery life of the computing device. One problem in decreasing power usage of the SRAM includes a decreased access success rate of the memory,**" and paragraphs [0045-0048] of Mohammad disclose "For the exemplary

circuits in FIGS. 3-4, **the minimum allowable voltage (Vddmin) for successful access of the memory is reduced** … **FIG. 5 is a diagram illustrating a memory 500** including level shifter/voltage scaling circuit 302 of FIG. 3 for the wordline logic 504 and MUX/Demux logic 516 and level shifter/voltage scaling circuit 402 of FIG. 4 for the memory cells 502," so according to FIGS. 3-5 and paragraphs [0003-0004], [0045-0047] of Mohammad, it is very obvious that Mohammad aims to solve the problem that the battery life of the computing device and the access success rate of the memory **are affected by the power usage of <u>the SRAM</u>**. Therefore, FIGS. 3-5 and paragraphs [0003-0004], [0045-0047] of Mohammad again shows that **<u>memory 500 is the SRAM rather than the DRAM</u>**. FIGS. 3-5 of Mohammad are shown as follows:

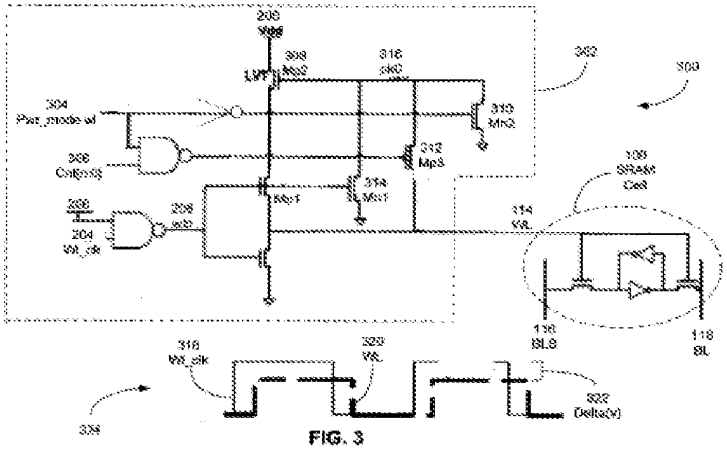


FIG. 3

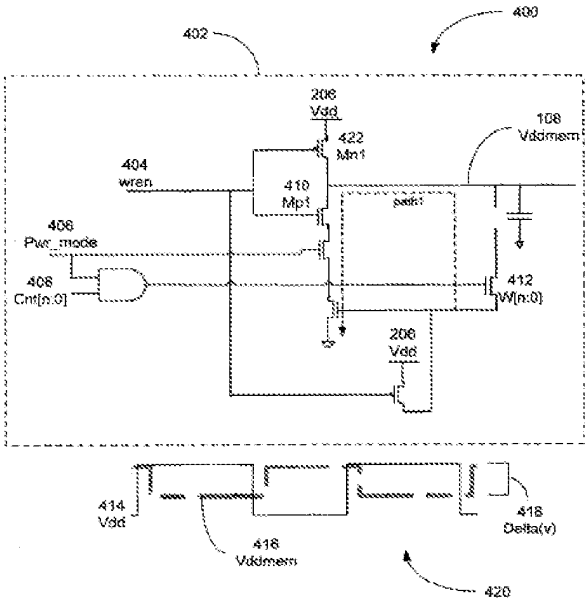

400
402
206
Vdd
422
Mn1
108
Vddmem
404
wren
410
Mp1
406
Pwr_mode
408
Cnt[n:0]
412
W[n:0]
206
Vdd
414
Vdd
416
Vddmem
418
Delta(v)
420

FIG. 4

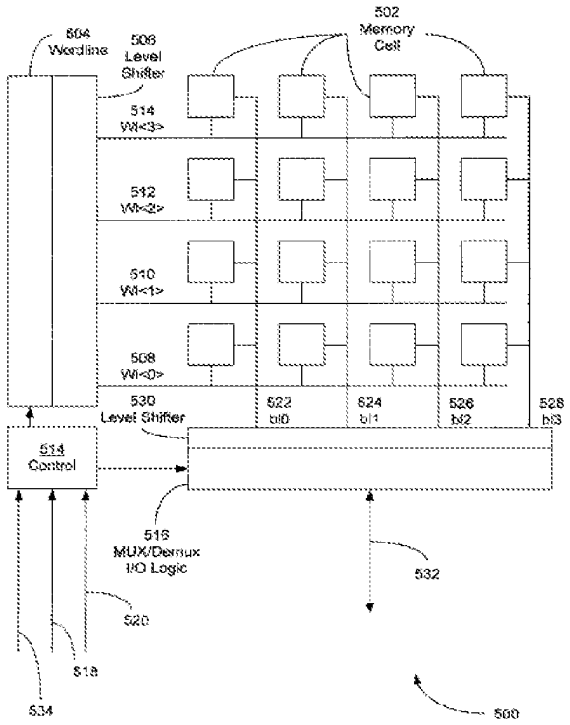


FIG. 5

Moreover, please refer to FIGS. 9-11 and paragraphs [0058-0065] of Mohammad. Paragraphs [0058-0065] of Mohammad disclose "**Low power, high yield memory as described above** **may be included in any processing devices** including a memory, **such as SRAM** … In a particular embodiment, **the DSP 904 includes a low power, high yield memory 962** as described in FIGS. 5 and 6 in order to reduce power consumption during memory accesses. In another embodiment, memory 912 may be low power, high yield memory as described in FIGS. 5 and 6 … In a particular embodiment, **the DSP 1004 includes a low power, high yield memory 1062** as described in FIGS. 5 and 6 in order to reduce power consumption during memory accesses," so according to FIGS. 9-11 and paragraphs [0058-0065] of Mohammad, it is very obvious that **the low power, high yield memory is still the SRAM**. Therefore, FIGS. 9-11 and paragraphs [0058-0065] of Mohammad also shows that **low power, high yield memory 962, 1062, 1162** (shown in FIGS. 9, 10, 11 respectively) **are SRAMs rather than DRAMs**. FIGS. 9-11 of Mohammad are shown as follows:

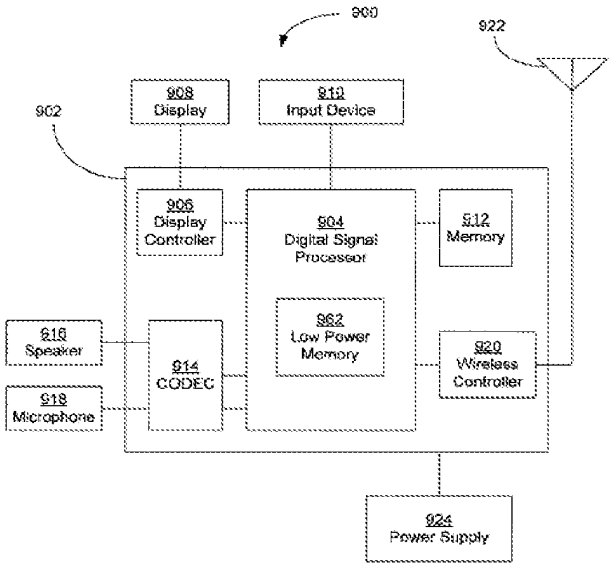

900
922
902
908
Display
910
Input Device
906
Display
Controller
904
Digital Signal
Processor
912
Memory
962
Low Power
Memory
916
Speaker
914
CODEC
920
Wireless
Controller
918
Microphone
924
Power Supply

FIG. 9

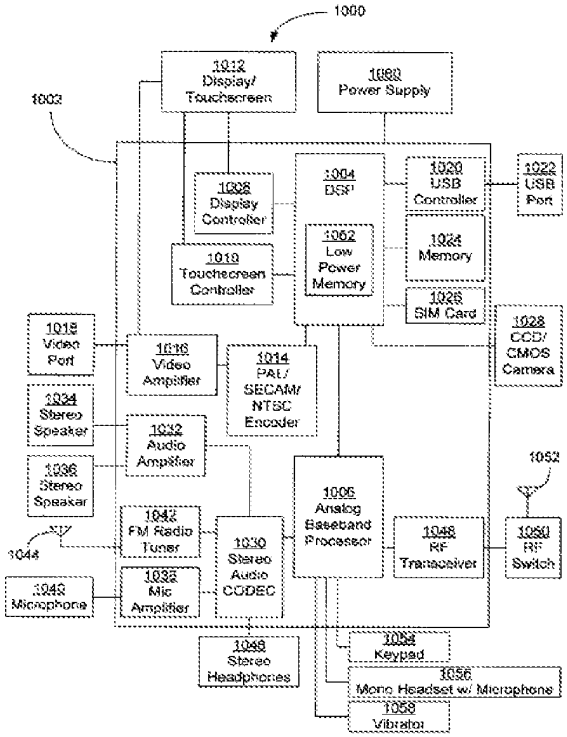

1000
1012 Display/ Touchscreen
1060 Power Supply
1002
1008 Display Controller
1004 DSP
1020 USB Controller
1022 USB Port
1010 Touchscreen Controller
1062 Low Power Memory
1024 Memory
1026 SIM Card
1018 Video Port
1016 Video Amplifier
1014 PAL/ SECAM/ NTSC Encoder
1028 CCD/ CMOS Camera
1034 Stereo Speaker
1032 Audio Amplifier
1036 Stereo Speaker
1052
1006 Analog Baseband Processor
1042 FM Radio Tuner
1030 Stereo Audio CODEC
1048 RF Transceiver
1050 RF Switch
1044
1038 Mic Amplifier
1040 Microphone
1054 Keypad
1046 Stereo Headphones
1056 Mono Headset w/ Microphone
1058 Vibrator

FIG. 10

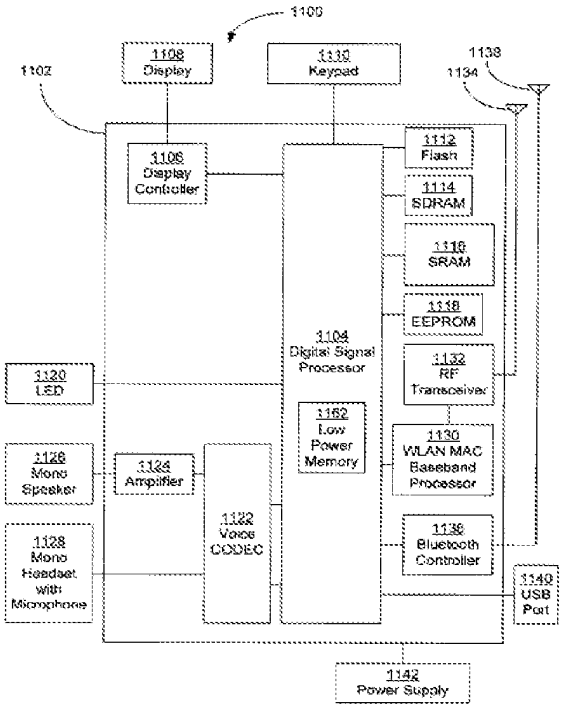


FIG. 11

In addition, please refer to the reference webpage "Random-access memory" retrieved from Wikipedia at URL: "https://en.wikipedia.org/wiki/Random-access_memory". Section "Memory Cell" of the reference webpage discloses "**In SRAM, the memory cell is a type of flip-flop circuit**, usually implemented using FETs. This means that SRAM requires very low power when not being accessed, but it is expensive and has low storage density. A second type, **DRAM, is based around a capacitor**. Charging and discharging this capacitor can store a "1" or a "0" in the cell. However, **the charge in this capacitor slowly leaks away, and must be refreshed periodically**," so according to the reference webpage, it is very obvious that **memory cells of the SRAM are based on flip-flop circuits implemented by FETs**, and **memory cells of the DRAM are based on capacitors**. Because **a structure of the SRAM and a structure of the DRAM are different**, **one of ordinary skilled in the art cannot simply replace the DRAM with the SRAM**. Moreover, because the memory cells of the DRAM are **based on capacitors, the memory cells of**

DRAM need to be refreshed (while **the memory cells of SRAM do not need to be refreshed**). Therefore, **a method applied to the SRAM cannot simply apply to the DRAM**.

In a brief summary, because according to FIGS. 3-5, 7, 9-11 and paragraphs [0003-0004], [0045-0048], [0053-0054], [0058-0065] of Mohammad, **method 700 is only applied to the SRAM rather than applying to the DRAM** and **memory 500 and low power, high yield memories 962, 1062, 1162 are SRAMs rather than DRAMs**; and according to reference webpage, **one of ordinary skilled in the art cannot simply replace the DRAM with the SRAM** and **the method applied to the SRAM cannot simply apply to the DRAM**, it is very obvious that **memory 500 (SRAM)** of Mohammad **cannot be referred to dynamic random access memory 100** of the present invention.

In addition, please refer to FIG. 7 and paragraphs [0078-0079] of Takahashi (US20100290300). Paragraphs [0078-0079] of Takahashi disclose "**The semiconductor memory circuit 201 is a built-in DRAM of a system LSI**, as with the first exemplary embodiment … **FIG. 7 shows the configuration of the semiconductor memory circuit 201** according to the second exemplary embodiment," so according to FIG. 7 and paragraphs [0078-0079] of Takahashi, it is very obvious that **semiconductor memory circuit 201 is a DRAM applied to the system LSI**, **rather than a DRAM applied to the embedded display port (eDP)**. Therefore, Takahashi obviously **fails to disclose the technical feature "dynamic random access memory (DRAM) applied to an interface port embedded display port (eDP)"** as presented in the currently amended claim 1. FIG. 7 of Takahashi is shown as follows:

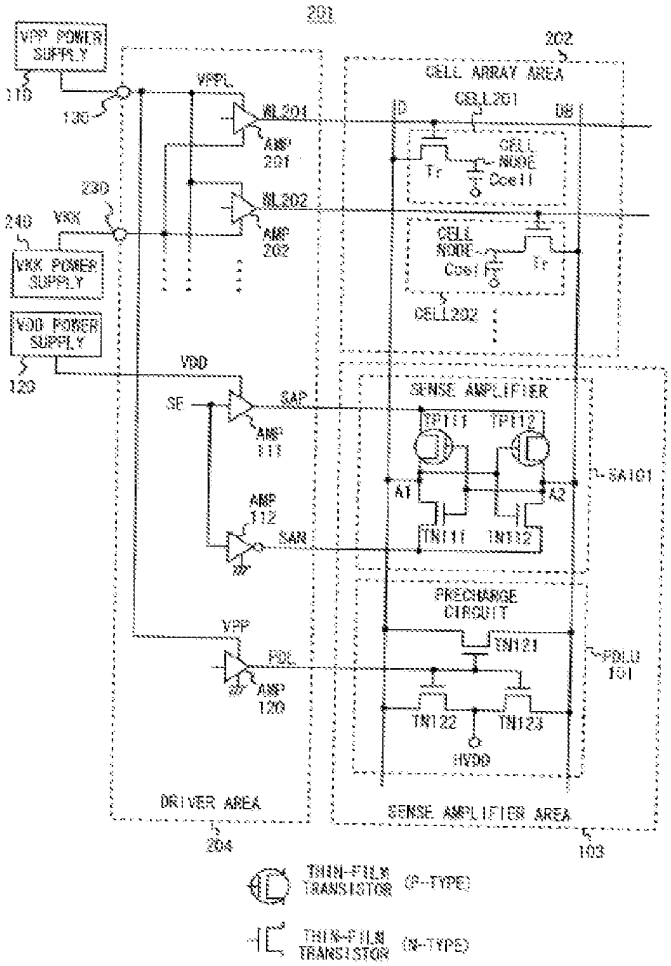


Fig. 7

To sum up, according to Figure, Table I, and paragraphs [0011-0012] of the present invention, **dynamic random access memory 100 is <u>the DRAM satisfying the requirements of the embedded display port version 1.3</u>**; and according to FIGS. 3-5, 7, 9-11 and paragraphs [0003-0004], [0045-0048], [0053-0054], [0058-0065] of Mohammad and the reference webpage, it is very obvious that **memory 500 (SRAM)** of Mohammad **<u>cannot be referred to</u> dynamic random access memory 100** of the present invention. In addition, according to FIG. 7 and paragraphs [0078-0079] of Takahashi, it is very obvious that Takahashi **<u>fails to disclose</u> the technical feature** "**<u>dynamic random access</u>**

memory (DRAM) applied to an interface port embedded display port (eDP)" as presented in the currently amended claim 1. Moreover, because **memory 500** of Mohammad **is the SRAM and semiconductor memory circuit 201** of Takahashi **is the DRAM**, **one of ordinary skilled in the art cannot combine memory 500** of Mohammad **and semiconductor memory circuit 201** of Takahashi to achieve the technical result of the currently amended claim 1. Therefore, the currently amended claim 1 should be patentable over Mohammad and Takahashi.

In addition, after the previously presented claim 1 is amended according to the above-mentioned technical features disclosed by Figure, Table I, and paragraphs [0011-0012] of the present invention, the currently amended claim 1 **should correspond to the allowable claims in TW and CN application**. Therefore, the applicant politely requests for reconsideration of the currently amended claim 1.

To sum up, allowance of the currently amended claim 1 and the previously presented claim 3 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Roger Chen/ Date: 02/14/2020

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Facsimile: 806-498-6673
e-mail : RogerChen@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

27765 7590 11/15/2019
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2131	

NOTIFICATION DATE	DELIVERY MODE
11/15/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 16/151,347	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 10/03/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 and 3 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 and 3 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 10/04/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/03/2019 has been entered.

This Office action is in response to the communication(s) filed on 10/03/2019. There are a total of 2 claims pending in the application. Claim 1 and 3 have been amended; claim 2 has been canceled; no new claims have been added.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

Claims 1 and 3 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

1. The independent claim 1 has been amended to recite that DRAM (the memory cells and peripheral circuit) operate at a voltage lower than 0.8V. The specification fails to describe or support the amendment as claimed. Claim 3 is rejected by virtue of its dependency from claim 1.

Claim Rejections - 35 USC §103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective

filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 3 are rejected under 35 U.S.C. 103 as being unpatentable over Mohammad "Mohammad" (US 2009/0122620) in view of TAKAHASHI et al. "TAKAHASHI" (US 2010/0290300 A1).

2. In regard to claim 1 Mohammad teaches:

A dynamic random access memory (DRAM) applied to an interface port ***(e.g., ¶ 0003)****, comprising:"*

"a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage (e.g., ¶ 0045), and the DRAM core cell is a volatile memory cell;" **(e.g., ¶¶ 0045-0047; Figs. 3-5).**

"and a peripheral circuit **(e.g., Mux/Demux and I/O logic 518 in Figs. 5 and 6)** electrically connected to the DRAM core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage **(e.g., ¶¶ 0058-0063; Figs. 9-11; Low power, high yield memory as described above may be included in any processing devices including a memory, such as SRAM)**, and wherein the memory core cell and the peripheral circuit are formed on a single chip **(e.g., ¶¶ 0061-0062; with the voltage level for low power, high yield memory used in circuits including DSP and display controller being less than 1.1V)**, and the peripheral circuit is external to the memory core cell," **(e.g., ¶¶ 0058-0063)**. *Mohammad teaches the limitations as given*

above, however, the reference does not expressly discloses a peripheral circuit unit which is a separate device from the memory core, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have peripheral devices connected to a memory core with the peripheral device also having a predetermined voltage which is lower than 1.1V for the peripheral device having both a digital signal processor with associated memory because DSP circuitry are commonly used in different types of peripheral devices with the low power, high yield voltage level providing low power consumption which benefits the overall system, Furthermore, location and voltage level of the integrated circuit elements/units are design and technology related. See for example, as an evidentiary document, Paragraphs [0117]-[0121] of the disclosure by "Shau (US 2005/0133852 A1). Shau teaches by changing/adjusting the design or fabrication parameters the voltage range for different units such as memory cell and logic/peripheral circuits can be kept the same or different. However, ***Mohammad does not expressly teach while*** *TAKAHASHI* ***discloses:***

"DRAM core cell operate at first voltage, wherein the first voltage lower than 0.8V; and the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 0.8V;" **(e.g., ¶¶ 0078-0079; Figs. 1 and 7)** *power supply voltage further reduced (e.g., VDD is 0.8 V or lower).*

Disclosures by Mohammad and TAKAHASHI are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the systems and methods for low power, high yield memory taught by Mohammad to include the DRAM operating with a power supply voltage (VDD) of lower than 0.8V or lower disclosed by TAKAHASHI.

The motivation for including the DRAM operating at the supply voltage of 0.8 V or lower as taught by paragraph [0018] of TAKAHASHI is due the reduction in the DRAM parameter sizes; the reduction in the DRAM parameter sizes provides higher level of integration and higher operating speed.

Therefore, it would have been obvious to combine teaching of TAKAHASHI with Mohammad to obtain the invention as specified in the claim.

3. In regard to claim 3 Mohammad further teaches:

"An input/output unit electrically connected to the peripheral circuit and the memory core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V." **(e.g., ¶ 0045, ¶¶ 0049~0051, ¶¶ 0070-0077; Figs. 8-9; the low power, high yield memory includes input/output circuits to read/write data from/to memory cells).**

Response to Remarks

Applicant arguments have been fully considered but they are not persuasive. Applicant has amended the independent claim 1 to recite that the DRAM memory cell

operate at a first voltage level and the peripheral circuits operates at a second voltage level, wherein the first voltage level and the second voltage level are lower than 0.8V.

In regard to the rejection of claims under 35 § 112(a), first paragraph as failing to comply with written description, Applicant states that table II and paragraph [0014] of claimed specification support/describe the amended limitation. For convenience the Table II and the paragraph [0014] is reproduced as shown below:

TABLE II

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	<1.1 V	<1.1 V	<1.1 V

[0014] As shown in Table II, operation voltages of the memory core unit **102** in the DDR I specification, the low power DDR I specification, the DDR II specification, and the low power DDR II specification are a first predetermined voltage, where the first predetermined voltage is lower than 1.1V; operation voltages of the peripheral circuit unit **104** in the DDR I specification, the low power DDR I specification, the DDR II specification, and the low power DDR II specification are a second predetermined voltage, where the second predetermined voltage is lower than 1.1V; and operation voltages of the input/output unit **106** in the DDR I specification, the low power DDR I specification, the DDR II specification, and the low power DDR II specification are a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.

The Table II that and Paragraph [0014] of the claimed specification shows that memory core unit, peripheral circuit unit, and input/output unit all operate at a voltage range <1.1 V. In page 4 of specification Applicant argues:

"so according to paragraph [0014] and Table II of the present invention, it is very obvious that the first predetermined voltage and the second predetermined voltage are defined by a voltage range (lower than LIVE wherein the voltage range includes two intervals: **a first interval that is between 0.8V and 1.1V**, and **a second interval that is**

lower than 0.8V. Therefore, it should be clear that the first predetermined voltage and the second predetermined voltage can be lower than 0.8V (which falls in the second interval)." *(Emphasis added)*.

The Examiner respectfully submits that not Table II, paragraph [0014], or any other portion(s) of the specification support, suggest, or indicate the operating voltage is lower than 0.8 V. The Examiner further note that the claims as initially filed describes operating voltage range is lower than 1.1 V.

Regarding the prior art rejection, Applicant states Mohammad does not disclosed that operating voltage is lower than 0.8 V. Mohammad teaches that operating voltage range is between 1 V and 0.8 V, which is lower than 1.1 V supported by the claimed specification. However, the Examiner has used disclosure of TAKAHASHI that teaches operating voltages of the DRAM cells and the peripheral or logic unit are lower than 0.8 V. The Examiner respectfully submits that Mohammad in view of TAKAHASHI teach or render all claim limitations obvious. Accordingly, Examiner maintains his position.

Conclusion

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ann Lo can be reached on (571)272-9767. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2131

November 11, 2019

Notice of References Cited	Application/Control No. 16/151,347	Applicant(s)/Patent Under Reexamination Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20100290300-A1	11-2010	TAKAHASHI; Hiroyuki	G11C11/4085	365/203
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/21/2019	11/16/2015	10/01/2016	05/14/2017	09/18/2017	05/28/2018			
	1	✓	✓	✓						
	2	✓	-	-						
	3	✓	✓	✓						

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	2	((memory near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with lower with ("1.1V" or "1.1 V"))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 17:55
L3	2	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V"))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 17:57
L4	54	Yuan-Der-Min.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 17:58
L5	33	Chang-Yen-An.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 17:58
L6	116	Huang-Wei-Ming.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 17:58
L7	2	3 and (L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 17:58
L8	12	(((memory or DRAM) near5 core) and (peripheral near5 (circuit or unit or logic)) and (voltage with (lower or less or smaller or below) with ("1.1V" or "1.1 V")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 17:59
L9	4	8 AND ((G06F12/0238 OR G06F12/063	US-PGPUB;	OR	ON	2019/11/11

		OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/4074 OR G11C7/1075 OR Y02D10/14 OR Y02D10/151).CPC. OR (711/105).CCLS. OR (G11C7/10 OR G11C11/4074).IPCR.)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			18:08
S101	3	"16151347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/10 13:20
S102	0	DRAM with vdd with ((lower or less or smaller or below) near5 "0.8")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/10 16:56
S103	124	vdd with ((lower or less or smaller or below) near5 "0.8")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/10 16:56
S104	30	S103 and (DRAM or SDRAM OR DDR$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/10 16:58
S105	11	S104 and (@ad< "20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/10 16:59
S106	0	DRAM with (input$output or I$1O) with ("1.1 v" or "1.1v")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:30
S107	123	DRAM with ("1.1 v" or "1.1v")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:31
S108	17179	DRAM with (input$output or I$1O)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2019/11/11 11:32

			JPO; DERWENT; IBM_TDB			
S109	4	S107 and S108	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:33
S110	1	S109 and (@ad< "20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:33
S111	0	DRAM adj5 ("1.1 v" or "1.1v")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:35
S112	13	DRAM adj10 ("1.1 v" or "1.1v")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:35
S113	6	S112 and (@ad< "20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:35
S114	23	((power adj supply) or VDD) with (input$output or I$1O) with ("1.1 v" or "1.1v")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:40
S115	11	S114 and (@ad< "20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:40
S116	0	S115 and DRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:41
S117	25	DRAM and ((input$output or I$1O) with ("1.1 v" or "1.1v"))	US-PGPUB; USPAT;	OR	ON	2019/11/11 11:41

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S118	7	S117 and (@ad< "20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/11/11 11:42

11/11/2019 6:10:09 PM
C:\Users\hfarrokh\Documents\EAST\Workspaces\13922242.wsp

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/151,347	Filing Date 10/04/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	10/03/2019	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 2	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/EFREM WARREN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16/151,347	Filing Date	2018-10-04	Docket Number (if applicable)	ETRP0143USA3	Art Unit	2131
First Named Inventor	Der-Min Yuan			Examiner Name	FARROKH, HASHEM		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503105

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature
☐ Applicant Signature

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Approved for use through 10/31/2008. OMB 0651-0031
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Signature of Registered U.S. Patent Practitioner			
Signature	/Roger Chen/	Date (YYYY-MM-DD)	2019-10-03
Name	Roger Chen	Registration Number	67314

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	16151347
Filing Date:	04-Oct-2018
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Filer:	Roger Gwan-Jye Chen/Edie Hung
Attorney Docket Number:	ETRP0143USA3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**1300**

Electronic Acknowledgement Receipt

EFS ID:	37351910
Application Number:	16151347
International Application Number:	
Confirmation Number:	3080
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Edie Hung
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0143USA3
Receipt Date:	03-OCT-2019
Filing Date:	04-OCT-2018
Time Stamp:	21:37:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1300
RAM confirmation Number	E201903L38197205
Deposit Account	503105
Authorized User	Edie Hung

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	3603848.PDF	823183 d74dd7d9fe2e29e7132574052b3eb1eac9c109c3	no	9
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	3603847.PDF	85486 5ace6cf470cda5f10dc2f1ac6b17fe3ab4feb550	no	1
Warnings:					
Information:					
3	Claims	3603845.PDF	86132 c4a68c5bdd10cb1bd184adaacc8d1d333fa3f778	no	1
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	3603641.pdf	324028 c558356d579ddcb511ec70c1d905c0bb7a4e6549	no	3
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30380 c491257abc133e1951741452d58598b4d59ba1b6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1349209		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Amendment of Claims:

The previously presented claim 1 is amended according to paragraph [0013] and Table Ⅱ of the present invention, and the previously presented claim 3 is amended accordingly. No new matter is introduced. Allowance of the claim amendments is politely requested.

2. Claim Rejections, 35 U.S.C. 112:

Response:

In this office action, the examiner holds that the specification of the present invention fails to describe or support the amendment of the previously presented claim 1, but the applicant respectfully disagrees with the above mentioned examiner's viewpoint.

Please refer to paragraph [0014] and Table Ⅱ of the present invention. Paragraph [0014] of the present invention discloses "As shown in Table Ⅱ, **operation voltages of the memory core unit 102** in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification **are a first predetermined voltage**, **where <u>the first predetermined voltage is lower than 1.1V</u>**; **operation voltages of the peripheral circuit unit 104** in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the

low power DDR Ⅱ specification **are a second predetermined voltage**, **where the second predetermined voltage is lower than 1.1V**", so according to paragraph [0014] and Table Ⅱ of the present invention, it is very obvious that **the first predetermined voltage and the second predetermined voltage are defined by a voltage range (lower than 1.1V)**, wherein **the voltage range includes two intervals**: **a first interval that is between 0.8V and 1.1V**, and **a second interval that is lower than 0.8V**. Therefore, it should be clear that **the first predetermined voltage and the second predetermined voltage can be lower than 0.8V** (which **falls in the second interval**).

In addition, according to MPEP 2163.05: "In the decision in In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976), the ranges described in the original specification included a range of "25%- 60%" and specific examples of "36%" and "50%." …, however a limitation to "between 35% and 60%" did meet the description requirement", a limitation to "**lower than 0.8V**" **should meet the description requirement** since "**lower than 0.8V**" **is inside the range** "**lower than 1.1V**." Therefore, the specification of the present invention **should support** the previously presented claim 1 in fact, and the previously presented claim 1 should comply with 35 U.S.C. 112(a) or 35 U.S.C. 112(pre-AIA). Therefore, allowance of the previously presented claim 1 is politely requested. Table Ⅱ of the present invention is shown as follows:

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	< 1.1V	< 1.1V	< 1.1V

Table Ⅱ

3. Claim Rejections, 35 U.S.C. 103:

Response:

In regard to claim 1

Please refer to Table II and paragraph [0013] of the present invention. Paragraph [0013] of the present invention discloses "Table Ⅱ illustrates operation **voltage ranges**

of the dynamic random access memory 100 operating in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification according to an embodiment." According to Table II and paragraph [0013] of the present invention, it is very obvious that **memory core unit 102 is a dynamic random access memory (DRAM) core cell**. In addition, according to paragraph [0014] and Table Ⅱ of the present invention and the above-mentioned reasons corresponding to "Claim Rejections, 35 U.S.C. 112", it is very obvious that **memory core unit 102 and peripheral circuit unit 104 can operate at voltages lower than 0.8V**.

However, please refer to paragraphs [0045], [0047] and FIGS. 3-4 of Mohammad (US20090122620). Paragraph [0045] of Mohammad discloses "For the exemplary circuits in FIGS. 3-4, the **minimum allowable voltage (Vddmin)** for successful access of the memory is reduced. For example, when **Vdd is a logic 1 for circuits 302, 402** of FIGS. 3 and 4, the **Vddmem voltage level** may be **lower than the Vdd voltage level** and still **allow for successful access of the memory**. In one embodiment, **Vddmin is 0.8 v as compared to 1.0 v for Vdd**", and paragraph [0047] of Mohammad discloses "memory 500 including **level shifter/voltage scaling circuit 302** of FIG. 3 **for the wordline logic 504 and MUX/Demux logic 516** and **level shifter/voltage scaling circuit 402** of FIG. 4 **for the memory cells 502**." First of all, according to FIG. 3 of Mohammad, it is very obvious that circuits 302, 402 **are applied to SRAM cell 100**, **rather than a DRAM cell**. Therefore, **SRAM cell 100** of Mohammad **cannot be referred to memory core unit 102 (the DRAM core cell)** of the present invention. In addition, according to paragraph [0045] and FIGS. 3, 4 of Mohammad, it is very obvious that **circuits 302, 402 are used for scaling voltage Vdd as voltage Vddmem**, wherein the **minimum allowable voltage Vddmem** (i.e. **voltage Vddmin) is 0.8V**. Therefore, it is very obvious that **SRAM cell 100 needs to operate at voltages higher than Vddmin (0.8V)**. Thus, Mohammad **not only fails to teach** the limitation of "a DRAM core cell, wherein **the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage**, and the DRAM core cell is a volatile memory cell, **wherein**

<u>the first voltage is lower than 0.8V</u>", but also **<u>teaches away</u>** the aforesaid limitation in claim 1 of this application.

In addition, according to paragraphs [0045], [0047] of Mohammad, because **level shifter/voltage scaling circuit 302** of FIG. 3 **<u>is applied to wordline logic 504 and MUX/Demux logic 516</u>** (wherein the examiner holds that **MUX/Demux logic 516 <u>can be referred to</u> peripheral circuit 104** of the present invention), it is also obvious that **wordline logic 504 and MUX/Demux logic 516 need to <u>operate at voltages higher than Vddmin (0.8V)</u>, <u>rather than operating at voltages lower than Vddmin (0.8V)</u>**. Therefore, Mohammad **<u>not only fails to teach</u>** the limitation of "a peripheral circuit electrically connected to the DRAM core cell, wherein **the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage**, wherein **<u>the second voltage is lower than 0.8V</u>**", but also teaches away the aforesaid limitation in claim 1 of this application. FIGS. 3-4 of Mohammad are shown as follows:

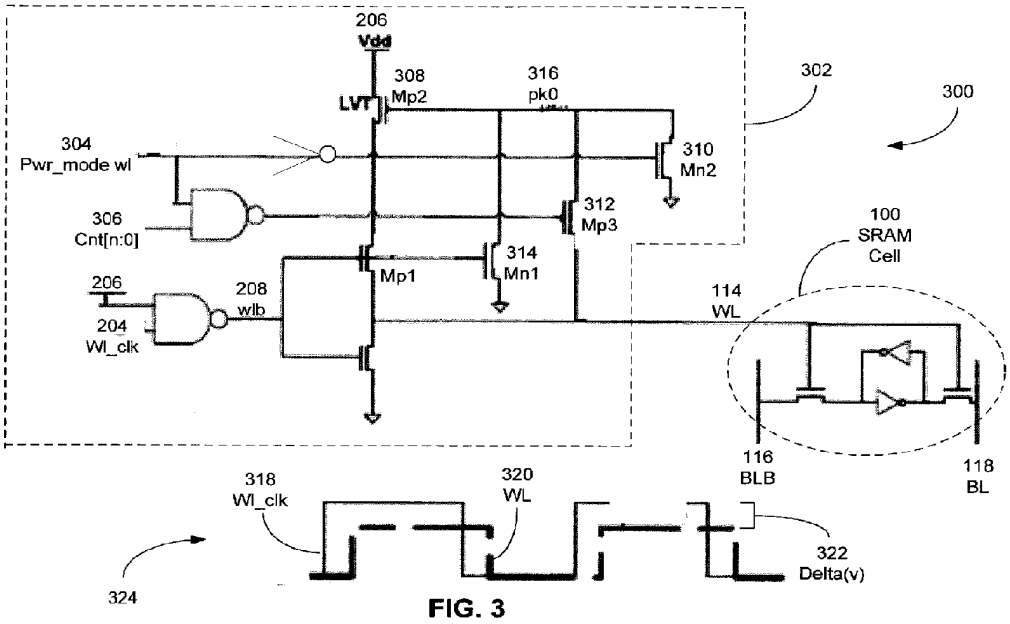

FIG. 3

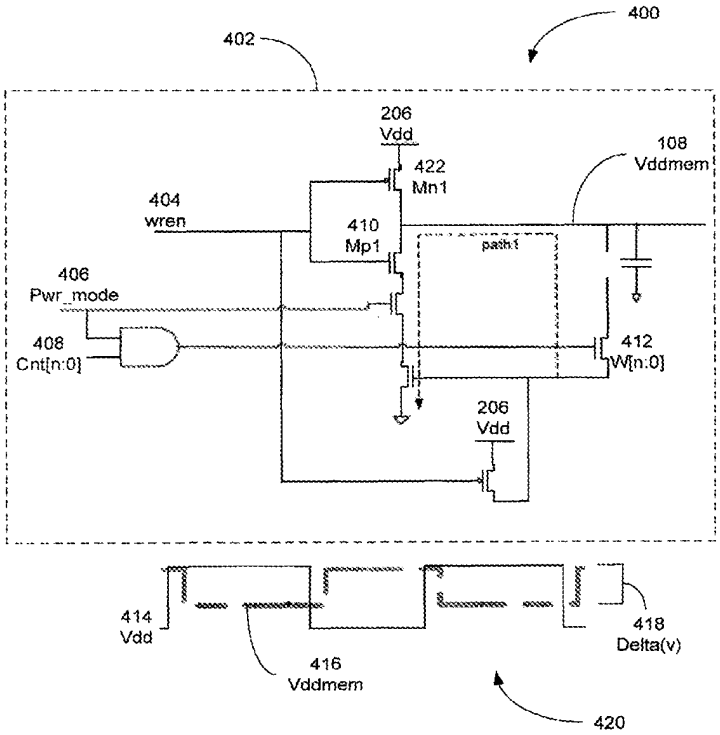

FIG. 4

On the other hand, please refer to paragraphs [0037], [0044] and FIGS. 2, 3 of Nakamura (US20080117700). Paragraph [0037] of Nakamura discloses "**Bit lines BLb and /BLb are <u>connected to sharing lines SA and /SA</u> via isolator BLIb**", and paragraph [0044] of Nakamura discloses "As will be described later, since power voltage VDD is applied to the gates of isolators BLIt and BLIb, power voltage VDD is clamped by isolators BLIt and BLIb, and **<u>the internal voltage of the array is lower (0.8 V in this embodiment) than power voltage VDD</u>** by a value equivalent to the threshold voltage of transistors N6 to N9", so according to paragraphs [0037], [0044] and FIGS. 2, 3 of Nakamura, Nakamura **<u>only discloses</u> that the internal voltage of top array TA <u>is lower than power voltage VDD</u>** and **the internal voltage <u>can be 0.8V</u>**. However, Nakamura **<u>does not disclose</u> that the internal voltage <u>can be lower than 0.8V</u>**. Therefore, Nakamura also **<u>fails to teach</u>** the limitation of "a DRAM core cell, wherein **the DRAM core cell is supplied with a first voltage within a first voltage range to make the**

DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein **the first voltage is lower than 0.8V**" in claim 1 of this application.

In addition, according to FIGS. 2, 3 of Nakamura, **sharing lines SA and /SA correspond to isolators BLIt and BLIb, P-type sense amplifier PSA, and N-type sense amplifiers NSAt and NSAb of array core 12** (which is referred to **peripheral circuit 104** of the present invention), wherein **an operation voltage of sharing line SA is up to 1.6V**. That is, **isolators BLIt and BLIb, P-type sense amplifier PSA, and N-type sense amplifiers NSAt and NSAb of array core 12 operate at 1.6V**. Therefore, Nakamura also **fails to teach** the limitation of "a peripheral circuit electrically connected to the DRAM core cell, wherein **the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage**, **wherein the second voltage is lower than 0.8V**." FIGS. 2, 3 of Nakamura are shown as follows:

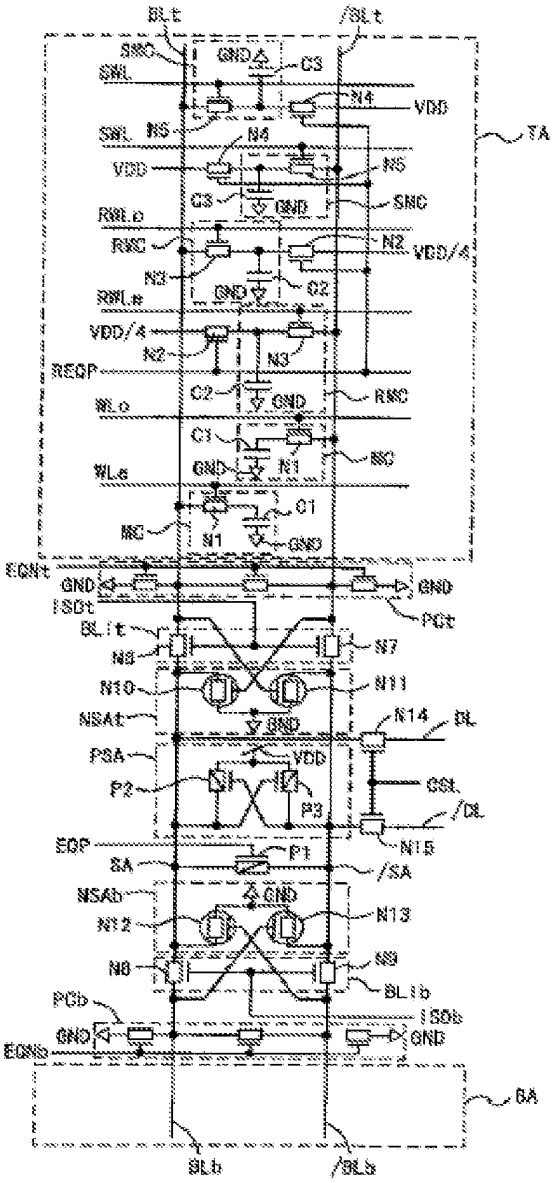
BLt
/BLt
SMC
GND
C3
SWL
N4
VDD
N5
TA
RWLo
RMC
N2
VDD/4
N3
C2
RWLe
REQP
WLo
C1
N1
MC
WLe
EQNt
ISOt
PCt
BLit
N6
N7
N10
N11
NSAt
N14
DL
PSA
P2
P3
CSL
/DL
N15
EQP
SA
P1
/SA
NSAb
N12
N13
N8
N9
BLib
PCb
ISOb
EQNb
BA
BLb
/BLb

FIG. 2

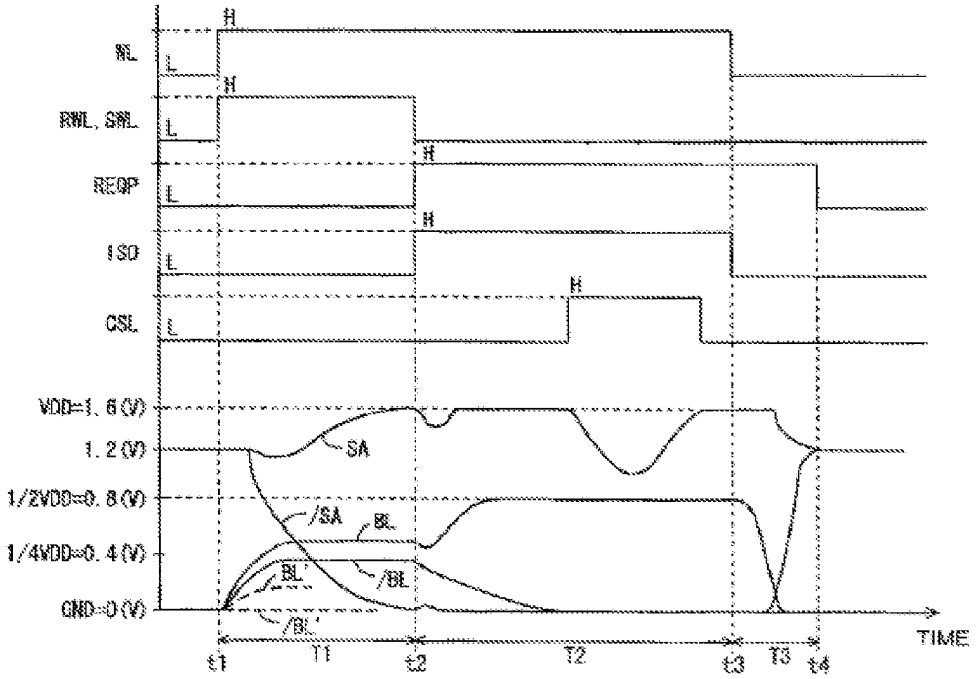

FIG. 3

To sum up, according to paragraphs [0013], [0014] and Table Ⅱ of the present invention, **memory core unit 102 <u>is a DRAM core cell</u>**, and **memory core unit 102 and peripheral circuit unit 104 <u>operate at voltages lower than 0.8V</u>**; however, both Mohammad and Nakamura fail to teach or suggest that the **memory core unit 102 and peripheral circuit unit 104 <u>operate at voltages lower than 0.8V</u>**, let alone that Mohammad teaches away the above-mentioned limitations. Therefore, the currently amended claim 1 of the present invention should be patentable over Mohammad and Nakamura. Therefore, allowance of the currently amended claims 1, 3 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Roger Chen/ Date: 10/03/2019

Roger Chen, Patent Agent No. 67,314
5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan
Voice Mail: 302-729-1562
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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Appl. No.	: 16/151,347	Confirmation No. : 3080
First Named Inventor	: Der-Min Yuan	
Filed	: October 4, 2018	
TC/A.U.	: 2131	
Examiner	: FARROKH, HASHEM	
Docket No.	: ETRP0143USA3	
Customer No.	: 27765	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

In response to the Office action of July 5, 2019, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended): A dynamic random access memory (DRAM) applied to an interface port, comprising:

   a ~~memory~~ DRAM core cell, wherein the ~~memory~~ DRAM core cell is supplied with a first voltage within a first voltage range to make the ~~memory~~ DRAM core cell operate at the first voltage, and the ~~memory~~ DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 0.8V; and

   a peripheral circuit electrically connected to the ~~memory~~ DRAM core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 0.8V, and

   wherein the ~~memory~~ DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the ~~memory~~ DRAM core cell.

2. (canceled)

3. (currently amended): The dynamic random access memory of claim 1, further comprising:

   an input/output unit electrically connected to the peripheral circuit and the ~~memory~~ DRAM core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

27765 7590 07/05/2019
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2131	

NOTIFICATION DATE	DELIVERY MODE
07/05/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 16/151,347	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 04/25/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 and 3 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 and 3 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 10/04/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This Office action is in response to the communication(s) filed on 04/25/2019. There are a total of 2 claims pending in the application. Claim 1 and 3 have been amended; claim 2 has been canceled; no new claims have been added.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> *(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.*

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

Claims 1 and 3 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

1. The independent claim 1 has been amended to recite that DRAM (the memory cells and peripheral circuit) operate at a voltage lower than 0.8V. The specification fails to describe or support the amendment.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.*

Claims 1 and 3 are rejected under 35 U.S.C. 103 as being unpatentable over Mohammad "Mohammad" (US 2009/0122620) in view of Nakamura "Nakamura" (US 2008/0117700 A1).

2. In regard to claim 1 Mohammad teaches:

A dynamic random access memory applied to an interface port **(e.g., ¶ 0003)**, comprising:"

"a memory core cell, wherein the memory core cell is supplied with a first voltage within a first voltage range to make the memory core cell operate at the first voltage **(e.g., ¶ 0045)**, and the memory core cell is a volatile memory cell;" **(e.g., ¶¶ 0045-0047; Figs. 3-5).**

and a peripheral circuit **(e.g., Mux/Demux and I/O logic 516 in Figs. 5 and 6)** electrically connected to the memory core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage **(e.g., ¶¶ 0058-0063; Figs. 9-11; Low power, high yield memory as described above may be included in any processing devices including a memory, such as SRAM)**, wherein the second voltage is lower than 1.IV, and wherein the memory core cell and the peripheral circuit are formed on a single chip **(e.g., ¶¶ 0061-0062; with the voltage level for low power, high yield memory used**

in circuits including DSP and display controller being less than 1.1V), and the peripheral circuit is external to the memory core cell." **(e.g., ¶¶ 0058-0063).** *Mohammad teaches the limitations as given above, however, the reference does not expressly discloses a peripheral circuit unit which is a separate device from the memory core, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have peripheral devices connected to a memory core with the peripheral device also having a predetermined voltage which is lower than 1 .IV for the peripheral device having both a digital signal processor with associated memory because DSP circuitry are commonly used in different types of peripheral devices with the low power, high yield voltage level providing low power consumption which benefits the overall system. Furthermore, location and voltage level of the integrated circuit elements/units are design and technology related. See for example, as an evidentiary document, Paragraphs [0117]-[0121] of the disclosure by "Shau" (US 2005/0133852 A1). Shau teaches by changing/adjusting the design or fabrication parameters the voltage range for different units such as memory cell and logic/peripheral circuits can be kept the same or different. However,* Mohammad does not expressly teach while Nakamura *discloses:*

"DRAM operating with a supply voltage lower than 0.8V" **(e.g., ¶ 0044; Figs. 1-2)** *operating the DRAM array with a supply voltage of lower than 0.8V.*

Disclosures by Mohammad and Nakamura are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the systems and methods for low power, high yield memory taught by Mohammad to include the DRAM array operating with a supply voltage of lower than 0.8V disclosed by Nakamura.

The motivation for including the DRAM array operating with a supply voltage of lower than 0.8V as taught by paragraph [0010] of Nakamura is to increase the operating speed for an integrated sense amplifier.

Therefore, it would have been obvious to combine teaching of Nakamura with Mohammad to obtain the invention as specified in the claim.

3. In regard to claim 3 Mohammad further teaches:

"an input/output unit electrically connected to the peripheral circuit and the memory core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V." **(e.g., ¶ 0045, ¶¶0049-0051, ¶¶ 0070-0077; Figs. 6-9; the low power, high yield memory includes input/output circuits to read/write data from/to memory cells).**

Response to Remarks

Applicant arguments have been fully considered but they are not persuasive. Applicant amended the independent claim 1 to recite the DRAM (e.g., memory cells and peripheral circuits) operates at a voltage level lower than 0.8V. The Applicant argues that Mohammad does not teach that DRAM may operate at a voltage lower than 0.8V. The Applicant argues that claim specification teaches that DRAM operates at lower than

0.8V. The Applicant argues that the amendment supported by the claimed specification. However, the Examiner respectfully submits that nowhere in the specification states that DRAM operates at an operating voltage lower than 0.8V.

The Table II that Applicant makes reference to show operating voltage less than <1.1V (e.g., less than 1.1V). Furthermore, the disclosure by Nakamura *is added that teaches that a DRAM array with an operating voltage lower than 0.8 volt. Accordingly, the Examiner maintain his position.*

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ann Lo can be reached on (571)272-9767. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2131

Monday, July 1, 2019

Notice of References Cited	Application/Control No. 16/151,347	Applicant(s)/Patent Under Reexamination Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20080117700-A1	05-2008	Nakamura; Yutaka	G11C11/4094	365/205
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/21/2019	11/16/2015	10/01/2016	05/14/2017	09/18/2017	05/28/2018			
	1	✓	✓							
	2	✓	-							
	3	✓	✓							

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	25	((((volatile adj memory) or SRAM or ?? RAM) near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) with (peripheral near2 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 12:34
L6	53	Yuan-Der-Min.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 12:34
L7	33	Chang-Yen-An.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 12:34
L8	116	Huang-Wei-Ming.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 12:34
L9	0	L5 and (L6 or L7 or L8)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 12:34
L10	81	((dynamic adj random adj access adj memory) or DRAM) near5 peripheral near5 (input$output or I$1O)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 12:35
L11	7	L10 AND ((G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/14 OR Y02D10/151).CPC. OR (711/105).CCLS. OR (G11C7/10).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 12:35

S78	283	VDD near2 ("0.8v" or "0.8 volt")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:20
S79	170	S78 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:21
S80	41	((Random adj access adj memory) or DRAM or RAM or SRAM or (volatile adj memory)) same (VDD near2 ("0.8v" or "0.8 volt"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:26
S81	32	S80 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:26
S82	0	((dynamic adj Random adj access adj memory) or DRAM or (volatile adj memory)) with ((supply adj voltage) or VDD) near5 ((less or lower) adj5 ("0.8v" or "0.8 volt"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:35
S83	0	((dynamic adj Random adj access adj memory) or DRAM or (volatile adj memory)) with ((supply adj voltage) or VDD) with ((less or lower) adj5 ("0.8v" or "0.8 volt"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:36
S84	3	memory with ((supply adj voltage) or VDD) with ((less or lower) adj5 ("0.8v" or "0.8 volt"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:37
S85	1	S84 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:37
S86	23	((supply adj voltage) or VDD) adj ((less or lower) adj5 ("0.8v" or "0.8 volt"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/06/30 10:38

			DERWENT; IBM_TDB			
S87	23	S86 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:39
S88	0	S87 and DRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/06/30 10:48
S89	124	((operating adj voltage) or (supply adj voltage) or VDD) with ((lower or less or smaller) adj ("0.8" or ".8"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 10:02
S90	90	S89 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 10:03
S91	18	S90 and DRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 10:05
S92	77	((operating adj voltage) or (supply adj voltage) or VDD) adj10 ((lower or less or smaller) adj ("0.8" or ".8"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 10:12
S93	65	S92 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/07/01 10:13

7/1/2019 12:38:16 PM
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/151,347	Filing Date 10/04/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	04/25/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 2	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/PAULA D MCCRAY STANLEY/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Appl. No.	: 16/151,347	Confirmation No.	3080
First Named Inventor	: Der-Min Yuan		
Filed	: October 4, 2018		
TC/A.U.	: 2131		
Examiner	: FARROKH, HASHEM		
Docket No.	: ETRP0143USA3		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of January 25, 2019, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended): A dynamic random access memory applied to an interface port, comprising:

a memory core cell, wherein the memory core cell is supplied with a first voltage within a first voltage range to make the memory core cell operate at the first voltage, and the memory core cell is a volatile memory cell, wherein the first voltage is lower than 0.8V; and

a peripheral circuit electrically connected to the memory core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than ~~1.1V~~0.8V, and

wherein the memory core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the memory core cell.

2. (canceled)

3. (currently amended): The dynamic random access memory of claim ~~2~~1, further comprising:

an input/output unit electrically connected to the peripheral circuit and the memory core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V.

Electronic Acknowledgement Receipt

EFS ID:	35824871
Application Number:	16151347
International Application Number:	
Confirmation Number:	3080
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Jessie Su
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0143USA3
Receipt Date:	25-APR-2019
Filing Date:	04-OCT-2018
Time Stamp:	04:52:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	3454369.PDF	784756 732d11941f02f9f99d7c41025db4db49f358edf7	no	6

Warnings:

Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	3454368.PDF	82255 4f03cd13ce1f34c257d7338cd45852644010f1d6	no	1
Warnings:					
Information:					
3	Claims	3454367.PDF	82737 5330d695d02959796941d9cf97228a2f7d8650f2	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	949748	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Amendment of Claims:

The original claim 1 is amended according to paragraph [0014] of the present invention, and the original claim 2 is canceled and the original claim 3 is amended accordingly. No new matter is introduced. Allowance of the claim amendments is politely requested.

2. Claim Rejections, 35 U.S.C. 103:

Response:

In regard to claim 1

Please refer to paragraphs [0045], [0047] and FIGS. 3-5 of Mohammad (US20090122620). Paragraph [0045] of Mohammad discloses "For the exemplary circuits in FIGS. 3-4, the **minimum allowable voltage (Vddmin)** for successful access of the memory is reduced. For example, when **Vdd is a logic 1 for circuits 302, 402** of FIGS. 3 and 4, the **Vddmem voltage level** may be **lower than the Vdd voltage level** and still **allow for successful access of the memory**. In one embodiment, **Vddmin is 0.8 v as compared to 1.0 v for Vdd**", and paragraph [0047] of Mohammad discloses "memory 500 including **level shifter/voltage scaling circuit 302** of FIG. 3 **for the wordline logic 504 and MUX/Demux logic 516** and **level shifter/voltage scaling circuit 402** of FIG. 4 **for the memory cells 502**", so according to paragraph [0045] and FIGS. 3, 4 of Mohammad, it is very obvious that **circuit 302 is supplied with voltage Vdd**, wherein the **minimum allowable voltage Vddmin is 0.8V**, that is, **circuit 302 must operate at voltage Vddmin (0.8V) or higher**. In addition, according to paragraphs [0045], [0047] of Mohammad, because **level shifter/voltage scaling circuit 302** of FIG. 3 **is applied to wordline logic 504 and MUX/Demux logic 516** (wherein the examiner holds that

MUX/Demux logic 516 **can be referred to** **peripheral circuit 104** of the present invention), it is also obvious that **wordline logic 504 and MUX/Demux logic 516 must** **operate at voltage Vddmin (0.8V) or higher**, **rather than operating under Vddmin (0.8V)**. In addition, according to paragraphs [0045], [0047] of Mohammad, because **level shifter/voltage scaling circuit 402** of FIG. 4 **is applied to memory cells 502**, and the **Vddmem voltage level** may be **lower than** **the Vdd voltage level**, Mohammad **only teaches** that **memory cells 502 can** **operate at voltage Vddmem or higher**, **rather than operating under voltage Vddmem**. That is, because Mohammad **fails to teach** that **voltage Vddmem** **is 0.8V**, Mohammad obviously **fails to teach** that **memory cells 502 can** **operate under 0.8V**. FIGS. 3-5 of Mohammad are shown as follows:

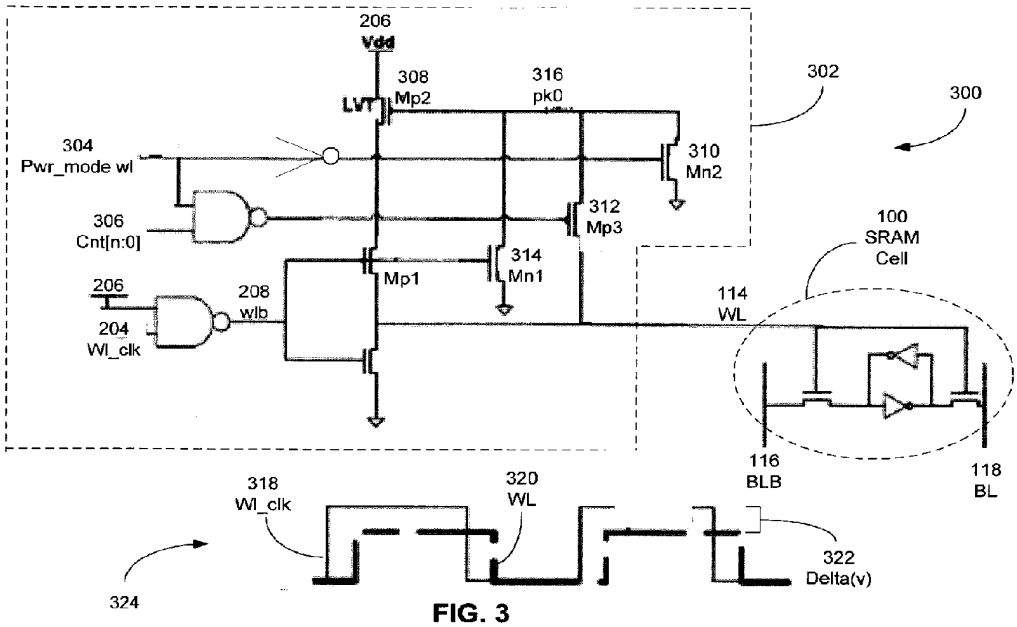

FIG. 3

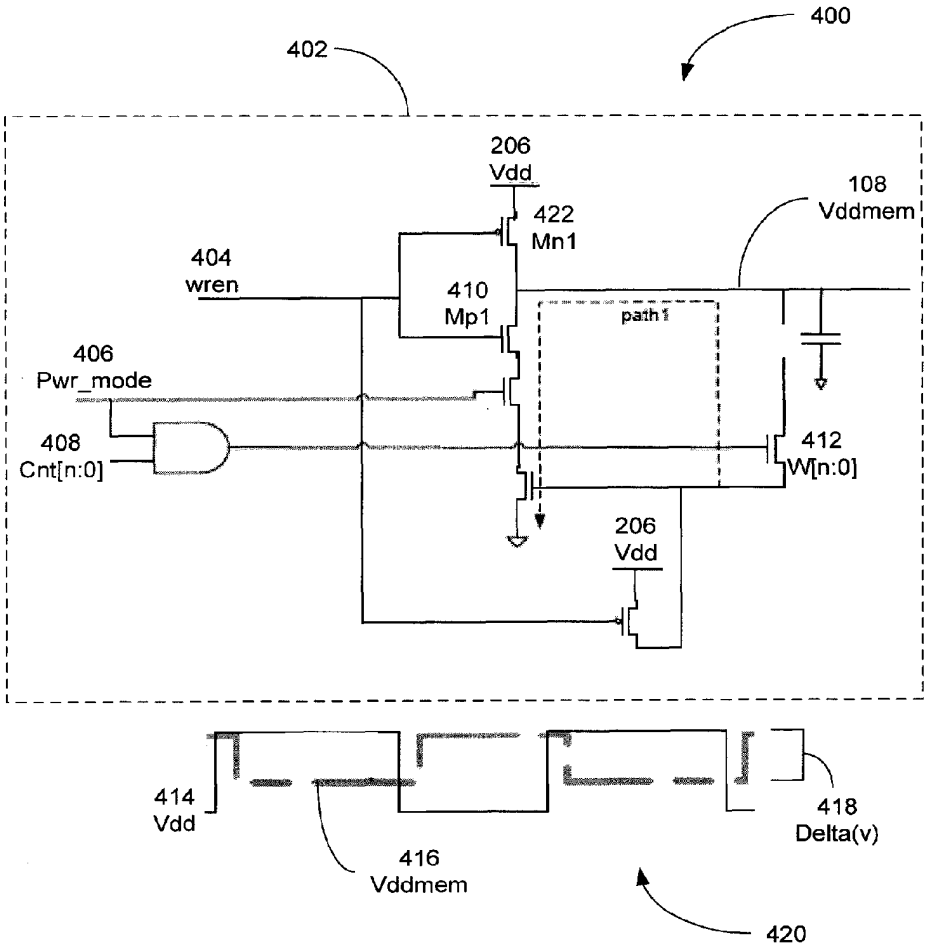
400
402
206
Vdd
422
Mn1
108
Vddmem
404
wren
410
Mp1
path 1
406
Pwr_mode
408
Cnt[n:0]
412
W[n:0]
206
Vdd
414
Vdd
416
Vddmem
418
Delta(v)
420

FIG. 4

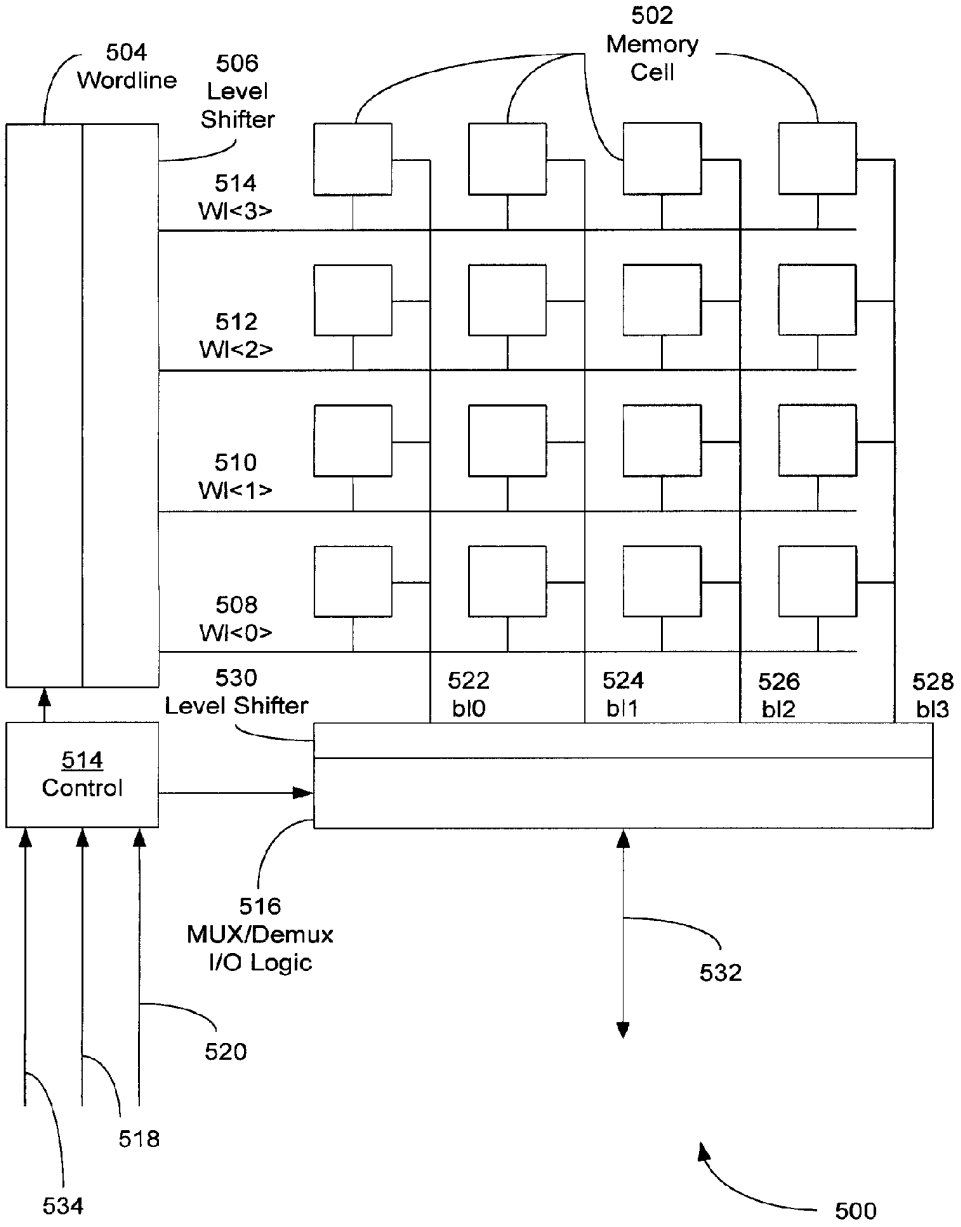

FIG. 5

However, please refer to paragraph [0014] and Table Ⅱ of the present invention. Paragraph [0014] of the present invention discloses "As shown in Table Ⅱ, **operation**

voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification **are a first predetermined voltage**, where the **first predetermined voltage is lower than 1.1V**; **operation voltages of the peripheral circuit unit 104** in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification **are a second predetermined voltage**, where the **second predetermined voltage is lower than 1.1V**", so according to paragraph [0014] of the present invention, because **first predetermined voltage is lower than 1.1V** and **second predetermined voltage is lower than 1.1V**, it is very obvious that **peripheral circuit unit 104 can operate under 0.8V**, and **memory core unit 102 can operate under 0.8V**. Table Ⅱ of the present invention is shown as follows:

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	< 1.1V	< 1.1V	< 1.1V

Table Ⅱ

Because according to paragraphs [0045], [0047] of Mohammad, Mohammad **fails to teach** that **wordline logic 504, MUX/Demux logic 516 and memory cells 502 can operate under 0.8V**, and according to paragraph [0014] of the present invention, it is very obvious that **peripheral circuit unit 104 can operate under 0.8V**, and **memory core unit 102 can operate under 0.8V**, Mohammad fails to teach or suggest the technical feature "**peripheral circuit unit 104 can operate under 0.8V**, and **memory core unit 102 can operate under 0.8V**" disclosed by paragraph [0014] of the present invention. Therefore, the currently amended claim 1 of the present invention should be patentable over Mohammad after the original claim 1 of the present invention are amended according to the above mentioned technical features disclosed by paragraph [0014] of the present invention.

To sum up, allowance of the currently amended claims 1, 3 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Roger Chen/ Date: 04/25/2019

Roger Chen, Patent Agent No. 67,314
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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3

CONFIRMATION NO. 3080

PUBLICATION NOTICE

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City,
TAIWAN

OC000000105507349

Title:DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Publication No.US-2019-0035440-A1
Publication Date:01/31/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/151,347	10/04/2018	Der-Min Yuan	ETRP0143USA3	3080

27765 7590 01/25/2019
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2131	

NOTIFICATION DATE	DELIVERY MODE
01/25/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 16/151,347	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	AIA Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 10/04/2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-3 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-3 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 10/04/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 10/25/2018.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

The instant application having application No. 16/151,347 has a total of 3 claims pending in the application; there are 1 independent claim and 2 dependent claims, all of which are ready for examination by the examiner.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING IDS:

The information disclosure statement (IDS) submitted on 10/25/2018 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.*

Claims 1-3 are rejected under 35 U.S.C. 103 as being unpatentable over Mohammad "Mohammad" (US 2009/0122620).

1. In regard to claim 1 Mohammad teaches:

A dynamic random access memory applied to an interface port **(e.g., ¶ 0003)**, comprising:"

"a memory core cell, wherein the memory core cell is supplied with a first voltage within a first voltage range to make the memory core cell operate at the first voltage **(e.g., ¶ 0045)**, and the memory core cell is a volatile memory cell;" **(e.g., ¶¶ 0045-0047; Figs. 3-5)**.

and a peripheral circuit **(e.g., Mux/Demux and I/O logic 516 in Figs. 5 and 6)** electrically connected to the memory core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage **(e.g., ¶¶ 0058-0063; Figs. 9-11; Low power, high yield memory as described above may be included in any processing devices including a memory, such as SRAM)**, wherein the second voltage is lower than 1.IV, and wherein the memory core cell and the peripheral circuit are formed on a single chip **(e.g., ¶¶ 0061-0062; with the voltage level for low power, high yield memory used in circuits including DSP and display controller being less than 1.1V)**, and the peripheral circuit is external to the memory core cell." **(e.g., ¶¶ 0058-0063).** *Mohammad teaches the limitations as given above, however, the reference does not expressly discloses a peripheral circuit unit which is a separate device from the memory core, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have peripheral devices connected to a memory core with the peripheral device also having a predetermined voltage which is lower than 1 .IV for the peripheral device having both a digital signal processor with associated memory because DSP circuitry are commonly used in different types of peripheral devices with the low power, high yield voltage level providing low power consumption which benefits the overall system. Furthermore, location and voltage level of the integrated circuit elements/units are design and technology related. See for example, as an evidentiary document, Paragraphs [0117]-[0121] of the disclosure by "Shau" (US 2005/0133852 A1). Shau teaches by changing/adjusting the design or fabrication parameters the voltage range*

for different units such as memory cell and logic/peripheral circuits can be kept the same or different.

2. In regard to claim 2 Mohammad further teaches:

"wherein the first voltage is lower than 1.1V." **(e.g., ¶ 0045; the voltage level for low power, high yield memory may be in range of 0.8v to 1.1v).**

3. In regard to claim 3 Mohammad further teaches:

"an input/output unit electrically connected to the peripheral circuit and the memory core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V." **(e.g., ¶ 0045, ¶¶0049-0051, ¶¶ 0070-0077; Figs. 6-9; the low power, high yield memory includes input/output circuits to read/write data from/to memory cells).**

Conclusion

The prior art made of record and not relied upon are as follows:

1. Sunwoo et al. (US 20090067217 A1).

3. Shau (US 20050133852 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ann Lo can be reached on (571)272-9767. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2131

Monday, January 21, 2019

Notice of References Cited	Application/Control No. 16/151,347	Applicant(s)/Patent Under Reexamination	
	Examiner HASHEM FARROKH	Art Unit 2131	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20090122620-A1	05-2009	Mohammad; Baker	G11C5/14	365/189.11
*	B	US-20050133852-A1	06-2005	Shau, Jeng-Jye	G11C7/18	257/315
*	C	US-20090067217-A1	03-2009	Sunwoo; Jung	G11C5/147	365/149
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/21/2019	11/16/2015	10/01/2016	05/14/2017	09/18/2017	05/28/2018			
	1	✓								
	2	✓								
	3	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/151,347	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16151347
	Filing Date	2018-10-04
	First Named Inventor	Der-Min Yuan
	Art Unit	2131
	Examiner Name	N/A Hashem Farrokh
	Attorney Docket Number	ETRP0143USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7295036	B1	2007-11-13	Zaveri	
	2	6551896	B2	2003-04-22	Hosoda	
	3	6097070		2000-08-01	Mandelman	
	4	6570787	B1	2003-05-27	Wang	
	5	6363014	B1	2002-03-26	Fastow	
	6	5928336	A	1999-07-27	Takeuchi	
	7	7894294	B2	2011-02-22	Pyeon	
	8	7692979	B2	2010-04-06	Fuji	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16151347
	Filing Date	2018-10-04
	First Named Inventor	Der-Min Yuan
	Art Unit	2131
	Examiner Name	N/A
	Attorney Docket Number	ETRP0143USA3

	9	7594129	B2	2009-09-22	Otani	
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110292448	A1	2011-12-01	OHASHI	
	2	20060259679	A1	2006-11-16	Schumann	
	3	20110252253	A1	2011-10-13	RUI	
	4	20060192282	A1	2006-08-31	Suwa	
	5	20030031043	A1	2003-02-13	Pochmuller	
	6	20060120138	A1	2006-06-08	Liaw	
	7	20060140004	A1	2006-06-29	Shukuri	
	8	20050010746	A1	2005-01-13	Chen	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16151347
	Filing Date	2018-10-04
	First Named Inventor	Der-Min Yuan
	Art Unit	2131
	Examiner Name	N/A
	Attorney Docket Number	ETRP0143USA3

	9	20130135955	A1	2013-05-30	McCombs	
	10	20110069562	A1	2011-03-24	Conte	
	11	20100095137	A1	2010-04-15	Bieswanger	
	12	20100074043	A1	2010-03-25	Kang	
	13	20100005439	A1	2010-01-07	SHIKATA	
	14	20090122620	A1	2009-05-14	Mohammad	
	15	20060047985	A1	2006-03-02	Otani	
	16	20120182076	A1	2012-07-19	Kim	
	17	20100008172	A1	2010-01-14	Yano	
	18	20130046941	A1	2013-02-21	Ma	
	19	20130132660	A1	2013-05-23	Li	

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.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	102187323	CN	A	2011-09-14			Abstract
	2	201123198	TW		2011-07-01			Abstract

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1	IBM Corp., East Fishkill, NY, USA, "Embedded DRAM technology: opportunities and challenges", IEEE SPECTRUM, Apr. 1999, page 56-64.	

EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	01/21/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Roger Chen/	Date (YYYY-MM-DD)	2018-10-25
Name/Print	Roger Chen	Registration Number	67314

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	491	VDD near2 ("1.0v" or "1.0 volt")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:14
L2	1508	peripheral near5 ((voltage or power) adj (range or level))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:15
L3	17	1 and L2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:15
L4	3177	(memory near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) with (peripheral near2 (circuits or unit or section))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:18
L5	0	1 and L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:18
L8	22	((((volatile adj memory) or SRAM or ??RAM) near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) with (peripheral near2 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:28
L9	52	Yuan-Der-Min.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:29
L10	32	Chang-Yen-An.in.	US-PGPUB;	OR	ON	2019/01/21

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			17:29
L11	113	Huang-Wei-Ming.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:29
L12	0	8 and (L9 or L10 or L11)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:29
L13	51	((((volatile adj memory) or SRAM or ??RAM) near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) and (peripheral near2 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:30
L14	0	13 and (L9 or L10 or L11)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:30
L15	79	((((volatile adj memory) or SRAM or ??RAM) near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) and (peripheral near5 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:31
L16	0	14 and (L9 or L10 or L11)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:31
L17	3934	((memory near2 cell) and (peripheral near5 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:37
L18	0	17 and (L9 or L10 or L11)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/01/21 17:37

			IBM_TDB			
L19	2289	((memory near5 unit) and (peripheral near5 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:38
L20	1	19 and (L9 or L10 or L11)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:39
L21	78	((dynamic adj random adj access adj memory) or DRAM) near5 peripheral near5 (input$output or I$1O)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:39
L22	6	L21 AND ((G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/14 OR Y02D10/151).CPC. OR (711/105).CCLS. OR (G11C7/10).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 17:39
L23	77	("7295036" "5928336" "6097070" "6363014" "6551896" "6570787" "7692979" "7894294" "7594129" "20030031043" "20050010746" "20060120138" "20060140004" "20060192282" "20060259679" "20110252253" "20050010746" "20060047985" "20090122620" "20100005439" "20100074043" "20100095137" "20110069562" "20120182076" "20060047985" "20090122620" "20100005439" "20100074043" "20100095137" "20110069562" "20120182076" "20130135955" "20100008172" "20130046941" "20130132660").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 18:00
L24	3814	((((volatile adj memory) or SRAM or ??RAM) near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) and (peripheral near5 (circuits or unit or section)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 18:01
L25	2	23 and 24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 18:02

S20	3	"20090122620".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/20 14:18
S21	3177	(memory near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) with (peripheral near2 (circuits or unit or section))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 10:56
S23	111	((SRAM or ??RAM) near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) with (peripheral near2 (circuits or unit or section))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 10:57
S24	92	S23 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 10:59
S25	1671079	(voltage or power) near5 (level or range)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 11:27
S26	25	S24 and S25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 11:28
S27	257033	(peripheral near2 (circuits or unit or section))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 11:43
S28	1055	S27 near5 S25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 11:44
S29	42	S21 and S28	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/01/21 11:44

			DERWENT; IBM_TDB			
S30	41	S29 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 11:44
S31	750	(lower or less or below or smaller) near5 ("1.1" adj (volt or "v"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:23
S32	0	S30 and S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:23
S33	1	S27 with S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:23
S34	1241	(lower or less or below or smaller) with ("1.1" adj (volt or "v"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:25
S35	905	S34 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:25
S36	13	S21 and S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:25
S37	1	S27 with S34	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:29
S38	14	S27 same S34	US-PGPUB; USPAT; USOCR;	OR	ON	2019/01/21 12:29

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S39	13	S38 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:29
S40	750	(lower or less or below or smaller) near5 ("1.1" adj (volt or "v"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:34
S41	1	peripheral with ((lower or less or below or smaller) near5 ("1.1" adj (volt or "v")))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:35
S42	3	peripheral near5 ("1.1" adj (volt or "v"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:36
S43	0	S42 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:37
S44	1508	peripheral near5 ((voltage or power) adj (range or level))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:38
S45	8270	("1.1" adj (volt or "v"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:39
S46	0	S44 with S45	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:39
S47	0	S44 same S45	US-PGPUB;	OR	ON	2019/01/21

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:39
S48	10	S44 and S45	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:39
S49	10	S48 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 12:39
S50	228	S34 and peripheral	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 13:23
S51	1	S34 with peripheral	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 13:23
S52	23	S34 same peripheral	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 13:24
S53	19	S52 and (@ad<"20120717")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 13:24
S54	0	DDR near5 (volrage near2 range)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/21 14:25

1/21/2019 6:22:03 PM
C:\Users\hfarrokh\Documents\EAST\Workspaces\13922242.wsp

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	Filing Date	2018-10-04
	First Named Inventor	Der-Min Yuan
	Art Unit	2131
	Examiner Name	N/A
	Attorney Docket Number	ETRP0143USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7295036	B1	2007-11-13	Zaveri	
	2	6551896	B2	2003-04-22	Hosoda	
	3	6097070		2000-08-01	Mandelman	
	4	6570787	B1	2003-05-27	Wang	
	5	6363014	B1	2002-03-26	Fastow	
	6	5928336	A	1999-07-27	Takeuchi	
	7	7894294	B2	2011-02-22	Pyeon	
	8	7692979	B2	2010-04-06	Fuji	

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	9	7594129	B2	2009-09-22	Otani	
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110292448	A1	2011-12-01	OHASHI	
	2	20060259679	A1	2006-11-16	Schumann	
	3	20110252253	A1	2011-10-13	RUI	
	4	20060192282	A1	2006-08-31	Suwa	
	5	20030031043	A1	2003-02-13	Pochmuller	
	6	20060120138	A1	2006-06-08	Liaw	
	7	20060140004	A1	2006-06-29	Shukuri	
	8	20050010746	A1	2005-01-13	Chen	

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	1	102187323	CN	A	2011-09-14			Abstract
	2	201123198	TW		2011-07-01			Abstract

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1	IBM Corp., East Fishkill, NY, USA, "Embedded DRAM technology: opportunities and challenges", IEEE SPECTRUM, Apr. 1999, page 56-64.	

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

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Signature	/Roger Chen/	Date (YYYY-MM-DD)	2018-10-25
Name/Print	Roger Chen	Registration Number	67314

Abstract of CN102187323

Dynamic utilization of power-down modes in multi-core memory modules

ABST:

Various embodiments of the present invention are directed to methods that enable a memory controller to choose a particular operation mode for virtual memory devices of a memory module based on dynamic program behavior. In one embodiment, a method for determining an operation mode for each virtual memory device of a memory module includes selecting a metric

(1001) that provides a standard by which performance and/or energy efficiency of the memory module is optimized during execution of one or more applications on a multicore processor. For each virtual memory device (1005), the method also includes collecting usage information (1006) associated with the virtual memory device over a period of time, determining an operation mode (1007) for the virtual memory device based on the metric and usage information, and entering the virtual memory device into the operation mode

(19)中华人民共和国国家知识产权局

(12)发明专利申请

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(43)申请公布日 2011.09.14

(21)申请号 200880131533.6

(22)申请日 2008.08.13

(85)PCT申请进入国家阶段日
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WO2010/019119 EN 2010.02.18

(71)申请人 惠普开发有限公司
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(72)发明人 安廷镐 N·P·朱皮
J·B·莱弗里奇 R·S·施赖博

(74)专利代理机构 中国专利代理(香港)有限公司 72001
代理人 李娜 王洪斌

(51)Int.Cl.
G06F 12/08(2006.01)
G06F 12/00(2006.01)

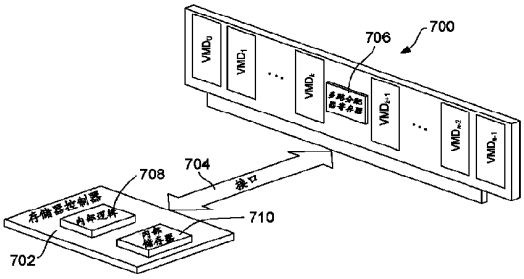
权利要求书 2 页 说明书 11 页 附图 16 页

(54)发明名称

多核存储器模块中的功率下降模式的动态利用

(57)摘要

本发明的各个实施例涉及使得存储器控制器能够基于动态程序行为针对存储器模块的虚拟存储器设备选择特定操作模式的方法。在一个实施例中,用于确定存储器模块的每个虚拟存储器设备的操作模式的方法包括选择提供标准的度量(1001),按照该标准优化存储器模块的性能和/或能量效率。对于每个虚拟存储器设备(1005),该方法还包括在一定的时间段内收集与虚拟存储器设备相关的使用信息(1006),基于度量和使用信息确定虚拟存储器设备的操作模式(1007),以及使得虚拟存储器设备进入该操作模式。



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1. 一种确定用于存储器模块的每个虚拟存储器设备的操作模式的方法，包含：

选择提供标准的度量（1001），按照该标准在多核处理器上的一个或多个应用的执行过程中优化所述存储器模块的性能和／或能量效率；以及

对于每个虚拟存储器设备（1005）：

在一定的时间段内收集与所述虚拟存储器设备相关的使用信息（1006）；

基于所述度量和使用信息确定所述虚拟存储器设备的操作模式（1007）；以及

使得所述虚拟存储器设备进入所述操作模式（1103，1105，1107，1108）。

2. 根据权利要求 1 所述的方法，其中该度量还包含最小总执行时间、最小总能量消耗、最小能量延迟乘积或者能够按照其来优化存储器模块的性能和／或能量效率的另一合适标准。

3. 根据权利要求 1 所述的方法，其中选择度量为最小总执行还包含对于不同时间段重复权利要求 1 的步骤。

4. 根据权利要求 1 所述的方法，还包含：

在所述一个或多个应用的执行过程中改变度量；以及

运行时系统，其配置成接收与所述一个或多个应用的存储器访问模式或所需存储量有关的特性信息和所述度量，解释该度量和特性信息，且指导存储器控制器使得每个虚拟存储器设备进入合适的操作模式。

5. 根据权利要求 1 所述的方法，其中该使用信息还包含确定以下项中的一个或多个：

当存储器控制器在该时间段内接收足够数目的存储器请求时存储器请求的频率；

在该时间段内的存储器请求的数目与执行的指令数目的比率；

分配给优于另一操作模式而选择一个操作模式的惩罚；

编译器向存储器控制器提供的与应用相关的存储器访问的频率；以及

应用在运行时确定的且发送到存储器控制器的存储器访问的频率。

6. 根据权利要求 1 所述的方法，其中选择度量还包含以下项之一：

计算机系统操作员选择度量；

一个或多个应用被编程为选择度量；

操作系统选择度量；以及

系统管理程序或运行时系统的其他元件调度、监控且支持运行时应用。

7. 根据权利要求 1 所述的方法，其中收集使用信息还包含存储器控制器（702）存储在该时间段内访问虚拟存储器设备的次数。

8. 根据权利要求 1 所述的方法，其中确定用于虚拟存储器设备的操作模式还包含：

基于度量确定至少一个阈值（1101）；以及

将使用信息与所述至少一个阈值进行比较（1102，1104，1106），其中当使用信息大于所述至少一个阈值时，使得该虚拟存储器设备进入待机模式（1108），否则使得该虚拟存储器设备进入节能模式（1103，1105，1107）。

9. 根据权利要求 8 所述的方法，其中当节能模式还包含至少一个功率下降模式时，每个功率下降模式与所述至少一个阈值之一相关。

10. 根据权利要求 9 所述的方法，其中当使用信息大于第一阈值且小于第二阈值时，使得虚拟存储器设备进入与第二阈值相关的功率下降模式。

11. 根据权利要求 1 所述的方法，其中该操作模式还包含当虚拟存储器设备不处理存储器请求且存储器模块的性能的优先级高于节省能量时的待机模式。

12. 一种系统，包含：

存储器控制器；以及

存储器模块，其包含至少一个虚拟存储器设备和连接到每个虚拟存储器设备和存储器控制器的多路分配器寄存器，其中该存储器控制器基于在一定的时间段内收集的使用信息的水平和度量使得至少一个虚拟存储器设备进入操作模式。

13. 根据权利要求 13 所述的系统，其中该虚拟存储器设备还包含一个或多个存储器芯片。

14. 根据权利要求 13 所述的系统，其中该度量还包含最小总执行时间、最小总能量消耗、最小能量延迟乘积或者能够按照其来优化存储器模块的性能和 / 或能量效率的另一合适标准。

15. 根据权利要求 13 所述的系统，其中操作模式还包含以下之一：

节能模式；以及

待机模式。

多核存储器模块中的功率下降模式的动态利用

技术领域

[0001] 本发明的实施例涉及存储器模块，且具体而言，涉及基于程序的动态操作使得存储器模块的独立虚拟存储器设备进入不同操作模式的方法。

背景技术

[0002] 在现代计算机系统中，对于存储器容量和带宽的需求保持增长。微处理器的近来的性能扩展取决于增加每芯片内核的数量，并且多核和很多内核的单芯片多处理器（“CMP”）通过每处理器多个存储器控制器而要求甚至更高的存储器带宽和容量。因此，主存储器模块的功率预算变得与当前计算机系统中的处理器的功率预算相似，或者甚至高于当前计算机系统中的处理器的功率预算。

[0003] 然而，典型的存储器模块是能量低效的。例如，当多个存储器模块连接到处理器的存储器控制器时，存储器模块的待机能量是总的主存储器能量使用的重要部分。当存储器模块并不积极响应于存储器请求时，大多数存储器模块是空闲的，在它们等待下一次存储器请求的同时使用待机能量，这是能量的低效使用。在很多当前存储器芯片中提供多种功率下降（power-down）模式以节省待机能量，且系统软件和硬件均使用这些功率下降模式来节省待机能量。然而，节省的功率量有限，因为相同的功率下降模式必须应用于模块中的所有存储器芯片。

[0004] 希望使得能够对存储在存储器系统中的信息进行访问的存储器系统和方法，所述存储器系统节省能量而不明显牺牲系统性能。

发明内容

[0005] 本发明的各个实施例涉及使得存储器控制器能够基于动态程序行为针对存储器模块的虚拟存储器设备选择特定操作模式的方法。在一个实施例中，用于确定存储器模块的每个虚拟存储器设备的操作模式的方法包括选择提供标准的度量，按照该标准，在多核处理器上的一个或多个应用的执行过程中，优化存储器模块的性能和／或能量效率。对于每个虚拟存储器设备，该方法还包括在一定的时间段内收集与虚拟存储器设备相关的使用信息，基于所述度量和使用信息确定虚拟存储器设备的操作模式，以及使得虚拟存储器设备进入该操作模式。

附图说明

[0006] 图 1A 示出具有八个存储器芯片的存储器模块的等距视图。

[0007] 图 1B 示出电路板上安装的存储器模块和存储器控制器的等距视图。

[0008] 图 2 示出构成存储器芯片的八个存储体（bank）的示意性表示。

[0009] 图 3A 示出传统存储器模块的示意性表示。

[0010] 图 3B 示出将命令广播到传统存储器模块的所有存储器芯片的示例。

[0011] 图 4A 示出根据本发明实施例配置的单个多核存储器模块的等距视图。

[0012] 图 4B 示出根据本发明实施例的电路板上安装的多核存储器模块和存储器控制器的等距视图。

[0013] 图 5A-5D 示出根据本发明的实施例配置的多核、双列直插存储器模块的一般示意性表示。

[0014] 图 6 示出根据本发明的实施例配置的示例性多核、双列直插存储器模块的示意性表示。

[0015] 图 7 示出根据本发明的实施例的电子地连接到存储器控制器的多核双列直插存储器模块。

[0016] 图 8A 示出条形图，该条形图呈现针对根据本发明的实施例的图 7 中示出的多核双列直插存储器模块的每个虚拟存储器设备的使用信息。

[0017] 图 8B 示出根据本发明的实施例的处于不同节能模式的图 7 中示出的多核双列直插存储器模块的三个虚拟存储器设备。

[0018] 图 9A 示出图 8A 中示出的条形图，其中根据优化根据本发明实施例的图 7 中示出的多核双列直插存储器模块的总执行时间来调节阈值。

[0019] 图 9B 示出根据本发明的实施例的处于节能模式的图 7 中示出的多核双列直插存储器模块的一个虚拟存储器设备。

[0020] 图 10 示出根据本发明的实施例的用于使得存储器模块的虚拟存储器设备动态地进入功率下降模式的方法的控制流程图。

[0021] 图 11 示出根据本发明的实施例的图 10A 的方法的子例程的控制流程图。

具体实施方式

[0022] 本发明的各种实施例涉及使得存储器控制器能够基于动态程序行为针对存储器模块的存储器芯片选择特定操作模式的方法。例如，存储器控制器可以配置成使得在一定的时间段内接收许多存储器请求的某些存储器芯片进入待机模式，从而当这些存储器芯片不在使用中时，它们可以快速地对存储器请求做出响应。与之对照，存储器控制器还可以使得在相同时间段内经历相对较低活动的其他存储器芯片进入许多节能模式之一。方法实施例是灵活的，因为系统性能可以与能量效率均衡。术语“性能”表示在一定的时间段内存储器系统执行的工作量。等待时间、响应时间和带宽是可用于比较在对存储器系统或其他存储器系统进行改变之前和之后的存储器系统的性能的度量。方法实施例允许给性能赋予比能量效率更高的优先级，方式是通过指导存储器控制器以与当给能量效率赋予比性能更高的优先级时存储器控制器将使得进入节能模式的存储器芯片相比，使得更少的存储器芯片进入节能模式。

[0023] 本发明的方法实施例可以应用于传统存储器模块和多核存储器模块，其被设计为改善存储器系统的能量效率而对系统性能具有小的影响。多核存储器模块包括存储器芯片，所述存储器芯片被划分成称为“虚拟存储器设备”（“VMD”）的一个或多个存储器芯片的组。存储器芯片可以是动态随机存取存储器（“DRAM”）芯片。

[0024] 详细描述按以下方式组织。在第一小节中描述传统存储器模块的一般性说明。在第二小节中描述多核存储器模块的说明。在第三小节中描述本发明的方法实施例。

[0025] <u>存储器模块</u>

存储器模块典型地包括形成被称为“双列直插存储器模块”（“DIMM”）的存储单元的印制电路板上安装的若干 DRAM 芯片。图 1A 示出包括八个 DRAM 芯片的单个 DIMM 的等距视图。然后在电路板上安装一个或多个 DIMM，并且由存储器控制器控制该一个或多个 DIMM。图 1B 示出电路板 106 上安装的存储器 102 和存储器控制器 104 的等距视图。存储器 102 由插入四个 DIMM 插槽 112-115 的四个 DIMM 108-111 组成。存储器控制器 104 是计算机芯片或多核微处理器芯片的部分，其管理发送到 DIMM 108-111 以及从 DIMM 108-111 发送的命令和数据流，并且将存储器 102 与计算机系统的其他主要组件（例如中央处理单元）对接。每一 DIMM 经由接口 118 与存储器控制器 104 进行电通信。接口 118 是载送从存储器控制器 104 到存储器 102 的时钟信号和命令以及 DIMM 108-111 与存储器控制器 104 之间的数据信号的总线。数据信号在 DIMM 108-111 中的 DRAM 芯片与存储器控制器 104 之间并行地发送。接口 118 可以支持单数据率（“SDR”）、双数据率（“DDR”）以及更高的数据率传送。SDR 指的是每时钟周期发送数据一次，以及 DDR 指的是在计算机系统时钟信号的上升沿和下降沿都发送数据。存储器控制器 104 和 DIMM 108-111 可以被配置为：根据 SDR 和 DDR 发送并且接收数据。在 DDR 中通过使用时钟的两个沿，数据信号在相同的极限频率操作，相比单数据率传输使得数据传输率加倍。

[0026] DRAM 芯片将比特存储在由晶体管和电容器组成的被称为 DRAM 存储器单元的结构中。单个 DRAM 芯片中存在数十亿个单元，以及可以以被称为“存储体”的许多二维阵列的二维布置组织这些单元。图 2 示出构成 DRAM 芯片 200 的标为 0-7 的八个存储体的示意性表示。如图 2 的示例中所示，每一存储体经由交叉信号线连接到行解码器、感测放大器以及列解码器。例如，存储体 0 经由与 x 轴平行走线的信号线（例如信号线 204）连接到行解码器 202。存储体 0 还经由与 y 轴平行走线的信号线（例如信号线 210）连接到感测放大器 206 和列解码器 208。存储器单元位于信号线交点处。例如，存储器单元 212 位于信号 204 和 210 交叉的点处。

[0027] 从存储器控制器 104 发送到存储器 102 的命令包括 READ（读）、WRITE（写）、ACTIVATE（激活）、REFRESH（刷新）和 PRECHARGE（预充电）。命令由控制信号和地址信号组成。控制信号表示命令执行的操作，以及地址信号标识在其执行命令的 DRAM 芯片中的存储体地址和行地址或列地址。例如，ACTIVATE 命令由激活控制信号和标识在 DRAM 芯片内的哪个存储体和行执行 ACTIVATE 命令的存储体地址和行地址组成。READ 和 WRITE 命令由读取和写入控制信号以及标识在 DRAM 芯片中的哪个存储体和列执行 READ 和 WRITE 命令的存储体地址和列地址组成。

[0028] 在两个步骤中访问 DRAM 芯片 200 的存储体中存储的数据。首先，存储器控制器（未示出）发送指定 DRAM 芯片 200 的行地址和存储体地址的 ACTIVATE 命令。将典型地是存储体的 8K 比特或 16K 比特的行中的所有比特激活到存储体内的感测放大器中。其次，发送指定存储体地址和列地址的一个或多个 READ/WRITE 命令。数据总线的大小和突发长度确定每 READ/WRITE 事务传送的比特的数量。突发长度是控制在数据块的单个突发事务或高速传输中执行的 READ/WRITE 操作的数量的常见的存储器有关的基本输入/输出系统设置。典型地，将突发长度设置为 4 或 8。当 DRAM 芯片接收到例如存储器 READ 请求时，芯片通过跨接口 118 的信号线提供数据来进行响应。突发长度确定响应于存储器 READ 请求发送的数据块的大小。具有 64 比特宽的数据总线（即 64 个单端信号线或 128 个差分信号线）和被配

置为支持 4 的突发长度的 DRAM 芯片的存储器模块响应于来自存储器控制器的单个 READ 请求发送 32 字节(4x64 比特 =32 字节)的数据块。另一方面,具有 64 比特宽的数据总线和被配置为支持 8 的突发长度的 DRAM 芯片的存储器模块响应于来自存储器控制器的单个 READ 请求发送 64 字节(8x64 比特 =64 字节)的数据块。

[0029] 当在 DRAM 芯片的同一存储体中的两个不同行中读取数据时,在可以读取第二行中的数据之前,必须写回第一行,对位线充电,以及通过 PRECHARGE 命令以及 ACTIVATE 命令锁存第二行。PRECHARGE 命令将该行写回到 DRAM 存储体,因为 ACTIVATE 命令破坏性地读取,所以这是必须的。在 READ 命令、WRITE 命令、ACTIVATE 命令和 PRECHARGE 命令中,存储体地址由小数量的比特给出。在同一存储体中,在第一 ACTIVATE 和第二 ACTIVATE 命令之间,这些命令操作一般花费大约 50ns。因此,除非 ACTIVATE 命令与 PRECHARGE 命令之间存在很多 READ/WRITE 命令,否则命令 / 地址 / 数据总线经常保持空闲。然而,如果在不同存储体中读取数据,则因为两个不同存储体之间的 ACTIVATE 至 ACTIVATE 时间短了大约 8ns,所以可以流水线化到不同存储体的命令。因此,通过交错不同存储体中的请求可以实现更高的吞吐量,当 ACTIVATE 和 PRECHARGE 命令对之间不存在很多 READ/WRITE 命令时尤其如此。

[0030] 图 3A 示出包括其中每一个具有 8 比特数据总线的 8 个 DRAM 芯片的传统 DIMM 300 的示意性表示。方向箭头 302 表示从存储器控制器(未示出)发送到称为寄存器 304 的可选设备的命令的分送。寄存器 304 位于存储器控制器与 DRAM 芯片之间的总线上。寄存器 304 锁存来自存储器控制器的命令信号,然后以更好的信号质量和定时裕度将它们转发到每一 DRAM 芯片,以减少存储器控制器上的电负载并且保持命令信号的稳定性。寄存器 304 也可以缓冲命令,并且将时钟信号广播到 DRAM 芯片,以在每存储器控制器具有多个 DIMM 的系统中促进对不同 DIMM 的交叠访问。寄存器 304 通过总线将命令广播到所有 8 个 DRAM 芯片,如通过分支方向箭头 306 和 308 指示的那样。在其它传统存储器模块中,将命令广播到 DRAM 芯片而不用寄存器 304。

[0031] 图 3B 示出传统 DIMM 操作的示例。如图 3B 的示例中所示,DIMM 300 内的所有 DRAM 芯片从存储器控制器接收相同命令,并且激活阴影区域 310 表示的每一 DRAM 芯片中的相同行。结果,DIMM 300 内的所有 DRAM 芯片充当具有更宽数据路径和更大行的单个 DRAM 芯片。

[0032] 如上参照图 2 描述的那样,DRAM 芯片行的大小典型地是 8 (或 16K 比特)。为了读取缓存线或者将缓存线写入 DIMM,将 READ/WRITE 命令广播到所有 DRAM 芯片,并且每一 DRAM 芯片激活相同行。换句话说,在由 8 个 DRAM 芯片组成的典型 DIMM 中,每一 DRAM 芯片激活包括 8K 比特的相同行地址。因而,一次激活 DIMM 的 DRAM 单元的 8×8Kbit 或 64Kbit,这大于待读取或写入的缓存线的大小。典型的缓存线处于 64 字节或 512 比特的量级。因为典型地以缓存线粒度读取或写入 READ/WRITE 命令 DIMM,所以对于单个 READ 或 WRITE 事务,超过 99% 的被激活的 DRAM 单元不被使用,这是能量的低效使用。

[0033] 多核存储器模块

多核存储器模块包含安装在印刷电路板上的分组成 VMD 的存储器芯片以及用于从存储器控制器接收命令的多路分配器寄存器(“多路分配器寄存器”)。在某些实施例中,存储器芯片可以是 DRAM 芯片。图 4A 示出根据本发明的实施例的包含布置在电路板 412 上的 8 个 DRAM 芯片 401-408 和多路分配器寄存器 410 的单个多核双列直插存储器模块 400 的等

距视图。DRAM 芯片 410-408 可以分组成包含一个或多个 DRAM 芯片的 VMD，其示例在下面更详细地描述。

[0034] 与传统 DIMM 一样，一个或多个 MCDIMM 可以安装在电路板上且通过存储器控制器控制。图 4B 示出根据本发明的实施例的安装在电路板 424 上的存储器 420 和存储器控制器 422 的等距视图。存储器 420 包含分别插入 DIMM 插槽 430-433 的 MCDIMM 426-429。MCDIMM 400 具有存储器控制器 422 和存储器模块 426-429 的多路分配器寄存器之间的接口 434。接口 434 包括从存储器控制器 422 到存储器 420 载送命令信号的总线以及在存储器控制器 422 和存储器 420 之间载送数据信号的数据总线。在该架构中，存储器控制器 422 发送的命令并不广播到存储器 420 的 DRAM 芯片。而是，存储器控制器 420 向 MCDIMM 426-429 的多路分配器寄存器发送命令。MCDIMM 426-429 中的每一个包括使得多路分配器寄存器能够直接向 VMD 发送命令的命令总线。

[0035] MCDIMM 与多核处理器兼容。例如，多个应用可以在多核处理器中并发地运行，其中每个内核运行一个多线程应用，且多核处理器中的存储器控制器服务于仅仅一个应用的请求。

[0036] 图 5A 示出根据本发明的实施例配置的 MCDIMM 500 的一般示意性表示。MCDIMM 500 包括 n 个 VMD，其中 n 是代表 MCDIMM 500 中的 VMD 的数目的整数。8 个 VMD 在图 5A 中示出且由 VMD_k 表示，其中下标 k 是范围从 1 到 n 的整数。MCDIMM 500 配置成使得每个 VMD 经由信号线的分离集合连接到多路分配器寄存器 502。下面参考图 5B 和 5C 描述多路分配器寄存器 502 的两个不同实施例。例如，VMD_0、VMD_1、VMD_k、VMD_{k+1}、VMD_{n-2} 和 VMD_{n-1} 经由信号线集合 504-509 连接到多路分配器寄存器 502。将 VMD 连接到多路分配器寄存器 502 的信号线的组合集合被称为“命令总线”。每个 VMD 可以由一个或多个存储器芯片（诸如 DRAM 芯片）组成。从存储器控制器（未示出）发送到 MCDIMM 500 的命令通过称为“命令路径”的信号线集合 510 到达多路分配器寄存器 502。每个 VMD 在通过双头箭头（诸如双头箭头 511）在图 5A 中标识的分离数据总线上与存储器控制器交换数据。

[0037] 图 5B 示出根据本发明的实施例配置的第一多路分配器寄存器 525 的示意性表示。多路分配器寄存器 525 由寄存器 512 和多路分配器 514 组成。多路分配器寄存器 525 经由图 5A 的命令路径 510 从存储器控制器接收命令。命令是时分复用的。换句话说，每个命令被编码在比特流中，所述比特流在固定的持续时间时隙中从存储器控制器发送到多路分配器寄存器 525。在图 5B 中，时分复用的命令的时隙由一系列矩形 515-520 表示。图 5B 中表示的每个命令包括意欲接收该命令的图 5A 中的 VMD 的索引。命令被发送到多路分配器寄存器 525 的顺序由存储器控制器确定。因而，在图 5B 中，命令以该顺序出现。嵌入在命令中的是标识待执行的特定种类的操作的控制信号、标识存储体、行或列的地址信号以及标识由存储器控制器分配为接收命令的特定 VMD 的 VMD 地址。例如，当命令要被发送到特定 VMD 时，存储器控制器创建包括标识该 VMD 的 VMD 地址的命令。一般而言，VMD 地址是包含 $\log_2 n$ 个比特的比特串。

[0038] 寄存器 512 是接收且临时存储命令的缓冲器。多路分配器 514 包括两个输入。如方向箭头 522 和 524 所表示的，寄存器向一个输入发送命令且向另一输入发送 VMD 地址。多路分配器 514 使用 VMD 地址来选择通向由 VMD 地址标识的 VMD 的命令总线的信号线的适当集合。在图 5B 中，命令总线的信号线的 n 个集合中的 6 个通过对应于信号线集合 504-509

的方向箭头 504-509 表示，且使用图 5A 中示出的相关 VMD 的索引进行标记。注意，在处理后续命令之前，每个命令在特定时间间隔内被多路分配器寄存器 525 单独处理。

[0039] 例如参考图 5A-5B，考虑存储器控制器向 VMD_k 发送命令 k+1 519。在图 5A 中，命令 k+1 519 沿着命令路径 510 被发送到多路分配器寄存器 525。如图 5B 所示，寄存器 512 接收且临时存储命令 k+1 519，且 VMD 地址和命令被发送到多路分配器 514，其然后选择信号线的适当集合 506 来向图 5A 中的 VMD_{k+1} 发送命令 k+1 519。在发送命令 k+1 519 之后，下一命令 1 518 以类似的方式被处理。

[0040] 如图 5B 所示，多路分配器寄存器 525 可选地包括与每个信号线集合相关的计数器。当 VMD 的 DRAM 芯片不能支持与缓存线的 READ 或 WRITE 事务相关的长突发长度时，可能需要计数器。多路分配器寄存器将缓存线划分为缓存线片段且将命令转换为多个命令，每个命令对应于缓存线片段。因而，由计数器发送的对应命令在发送到 VMD 的每个缓存线片段之前。例如，当不能将 VMD 的一个或多个 DRAM 芯片的突发长度设置得足够长以覆盖缓存线时，计数器将列级别命令（例如 READ 或 WRITE）转换为用于每一缓存线片段的若干 READ/WRITE 命令，从而可以分离地读取每一缓存线片段或将每一缓存线片段写入到 DRAM 芯片。每一计数器包括跟踪为划分的缓存线生成的命令的数量的计数设备。计数器执行的转换节省了来自存储器控制器的命令带宽。

[0041] 图 5C 示出根据本发明的实施例配置的第二多路分配器寄存器 527 的示意性表示。多路分配器寄存器 527 包含标为 0 至 n-1 的 n 个命令选择器以及广播总线 528，对于图 5A 中示出的 n 个 VMD 中的每一个都有一个命令选择器。如上面参考图 5B 所描述的，存储器控制器在命令路径 510 上向多路分配器寄存器 527 发送时分复用命令 515-520。命令选择器经由支路 529-534 电子地连接到广播总线 528，且每个命令选择器经由命令总线中的某个信号线集合连接到 VMD 之一。在图 5C 中，命令总线中的信号线的 n 个集合中的 6 个由对应于信号线集合 504-509 的方向箭头 504-509 表示且使用图 5A 示出的相关 VMD 的索引进行标记。如图 5C 所示，每个命令被广播到所有的 n 个命令选择器。每个命令选择器配置成提取嵌入在命令中的 VMD 地址以确定命令是否要被转发到对应的 VMD 或命令是否被寻址到不同 VMD，在命令被寻址到不同 VMD 的情况下，命令被丢弃。因而，对于广播到所有 n 个命令选择器的每个命令而言，该命令仅被命令选择器之一发送到对应的 VMD。例如，多路分配器寄存器 527 接收命令 n-2 520 且将其广播到所有 n 个命令选择器 0 至 n-1。然而，因为命令 n-2 520 包括 VMD_{n-2} 的地址，所以命令选择器 n-2 通过信号线集合 508 将命令 n-2 520 发送到 VMD_{n-2} 且其他命令选择器丢弃命令 n-2 520。注意，在处理后续命令之前，每个命令在特定时间间隔内被多路分配器寄存器 527 单独处理。

[0042] 图 5D 示出根据本发明的实施例配置的示例性命令选择器 n-2 的示意性表示。其他的 n-1 个命令选择器被类似配置。命令选择器 n-2 包含 AND（与）门 530、寄存器 / 计数器 532 以及随机存取存储器（“RAM”）定时控制 534。命令在支路 533 上被输入到命令选择器 n-1。AND 门 530 提取嵌入在每个命令中的 VMD 地址且接收系统时钟信号。AND 门 530 配置成在提取的 VMD 地址匹配对应的 VMD_{n-2} 的地址时向寄存器 / 计数器 532 发送选择信号。AND 门 530 接收时钟信号以确定寄存器 / 计数器何时锁存命令，且 AND 门 530 可以配置成在每个上升和 / 或下降时钟沿发送选择信号。寄存器 / 计数器 532 是在从 AND 门 530 接收到选择信号时临时存储命令且向对应的 VMD_{n-2} 发送命令的缓冲器。寄存器 / 计数器 532 还包

括如上面参考图 5B 所描述的执行缓存线和命令划分的计数器。RAM 定时控制 534 控制寄存器 / 计数器 532 的计数器部分。

[0043] 一般而言，AND 门在所有输入信号对应于比特“1”时输出对应于比特“1”的信号且在输入信号中的至少一个对应于比特“0”时输出对应于比特“0”的信号，其中比特“1”和“0”可以分别代表信号的高和低电压。命令选择器 0 至 n-1 的 AND 门可以包括某些输入信号线上的反相器。反相器将与比特“0”相关的信号转变成与比特“1”相关的信号且反之亦然。AND 门包括某些输入信号线上的反相器以将代表对应 VMD 的 VMD 地址转变成包含全“1”比特的比特流。AND 门然后向寄存器 / 计数器 532 输出对应于比特“1”的选择信号。例如，假设 VMD_{n-2} 的 VMD 地址包含比特流 11…1101。AND 门 530 包括反相器 536，其反转在线 538 上进入 AND 门 530 的信号的电压。因而，如图 5D 所示，当嵌入在命令中的 VMD 地址匹配地址 11…1101 时，地址被转变成 11…1111，且 AND 门 530 与时钟信号结合地向寄存器 / 计数器 532 输出代表比特“1”的选择信号，寄存器 / 计数器 532 锁存命令到信号线集合 508 上。对于其他地址，进入 AND 门 530 的比特流包括至少一个“0”比特，且 AND 门 530 不输出信号或者输出对应于比特“0”的低信号。因而，寄存器 / 计数器 532 不锁存命令到信号线集合 508 上。

[0044] 图 6A 示出根据本发明的实施例配置的 MCDIMM 600 的示意性表示。MCDIMM 600 包括由 VMD_k 标识的 4 个 VMD 以及多路分配器寄存器 602，其中 k 是范围从 0 到 3 的整数。每个 VMD 包含两个 DRAM 芯片，且多路分配器寄存器 602 可以如上面参考图 5B-5D 描述的那样被配置和操作。命令总线 MCDIMM 600 包含将每个 VMD 的 DRAM 芯片连接到多路分配器寄存器 602 的四个信号线集合 604-607。命令沿着命令路径 608 从存储器控制器(未示出)发送到多路分配器寄存器 602。根据 $\log_2 n$，其中 n 等于 4，VMD 可以被分配两比特 VMD 地址 00、01、10 和 11 之一，所述地址包括在命令中以标识意欲接收该命令的 VMD。每个 VMD 通过命令总线接收不同的命令且经由双头箭头(诸如双头箭头 610)所表示的其自己的数据总线独立于其他 VMD 传输数据。

[0045] 在图 6A-6B 的示例性 MCDIMM 600 中，每个存储器请求涉及两个 DRAM 芯片。DRAM 芯片对的等同阴影区域表示与不同命令相关的不同独立存储器请求。每个 VMD 通过命令总线接收命令且使用其自己的数据总线独立传输数据。因而，通过比传统 DIMM (见伴随图 3 的描述)激活更少的比特来节省能量。然而，与传统 DIMM 相比，因为数据总线大小小于传统 DIMM 中的数据总线大小，可能需要更多的时间来传送数据。例如，数据可以被划分成较小的串行化数据部分，其中每个部分通过 VMD 总线单独被发送到存储器控制器。以这种方式串行化数据增加了使用传统 DIMM 发送数据所需的时间量。该附加串行化等待时间问题可能对系统性能具有负面影响。

[0046] <u>本发明的方法实施例</u>

下面参考动态地改变 MCDIMM 的各个 VMD 的能量消耗描述本发明的方法实施例。存储器芯片可以进入若干不同的操作模式。例如，存储器芯片可以响应于存储器请求而进入活动(active)模式。当存储器芯片不再处理存储器请求时，存储器芯片可以进入待机模式，其中存储器芯片被提供以待机能量，该待机能量低于活动地处理存储器请求所需的能量，但是高得足以维持内部存储器芯片组件的操作，使得存储器芯片能够快速响应于另一存储器请求。然而，当每存储器通道存在多个存储器模块时，处于待机模式中的存储器芯片消耗

发送给存储器模块的总能量的显著部分。

[0047] 通过使得临时不在使用中的存储器芯片进入节能模式可以节省待机能量。处于节能模式中的存储器芯片必须被加电(power up),这增加了响应时间。例如,功率下降模式是通过关闭很多内部存储器芯片组件来节省能量的一种节能模式,然而,存在与该模式相关的很多性能限制。当存储器芯片处于功率下降模式时,正常的存储器芯片访问是不可能的,且存储器芯片必须被加电,因此进入和退出功率下降模式比进入和退出待机模式花费更多的时间。结果,使用功率下降模式典型地节省能量,但是导致较低的存储器系统性能。为了减小对存储器芯片加电所需的时间,很多存储器芯片还可以配置成具有多个功率下降模式。每个功率下降模式提供不同递增级别的能量节省。然而,能量节省的每个递增增加对应于对存储器芯片加电所需的更长的时间量。

[0048] 本发明的方法实施例对于运行在多核处理器上的一个或多个应用可以是透明的,因为挑选操作模式的决策可以完全由硬件做出,其还具有在运行时期间由编译器或一个或多个应用修改的灵活性。图7示出根据本发明的实施例的经由接口704电子地连接到存储器控制器702的MCDIMM 700。MCDIMM 700包含如上参考图5A描述的那样配置的多路分配器寄存器706和n个VMD。如图7所示,存储器控制器702配置有内部逻辑708和内部储存器710。关于每个VMD的使用的信息可以存储在内部储存器710中,且本发明的方法可以完全由存储器控制器内部逻辑708执行。

[0049] 方法实施例包括在运行在多核处理器上的一个或多个应用的运行时期间优化存储器模块的性能和/或能量效率。计算机系统操作员、一个或多个应用或者操作系统选择提供标准的度量,按照该标准优化存储器模块的性能和/或能量效率。该度量可以是最小总执行时间(“TET”)、最小总能量消耗(“TEC”)、最小能量延迟乘积(“EDP”)或可以按照其来优化存储器模块的性能和/或能量效率的任意其他合适标准。设置度量以最小化一个或多个应用的TET允许所述应用几乎全带宽地访问存储器模块提供的存储容量。换句话说,当存储器芯片并不活动地处理存储器请求时,不是使得存储器芯片进入功率下降模式,而是使得存储器芯片进入待机模式,从而存储器芯片能够快速响应于下一存储器请求。因而,TET是性能度量。另一方面,设置度量为TEC通过以下方式减小了针对每个存储器请求的容易可用的存储器芯片的数目:使得这些存储器芯片进入节能模式,这减小了带宽且延迟了存储器响应时间但是提供了优于设置度量为TET的能量节省。设置度量为最小化EDP提供了TET和TEC之间的折衷。EDP度量被定义为与存储器请求相关的能量和延迟的乘积。EDP可用于在给定性能水平提供最小能量,或者针对相同的能量提供更多的性能。

[0050] 一旦选择了度量,就确定在一个或多个应用的运行期间与每个VMD的使用有关的信息。使用信息被收集且存储在存储器控制器702中且可以包括以下项中的一个或多个:(1)当存储器控制器在一定的时间段内接收足够数量的存储器请求时每VMD的存储器请求的频率的记录;(2)在一定时间段内的存储器请求的数目与执行的指令数目的比率;(3)分配给优于另一操作模式而选择一个操作模式的惩罚;(4)编译器可以向存储器控制器702提供关于与它处理的一个或多个应用相关的每VMD的存储器访问的频率的信息;以及(5)运行时的一个或多个应用可以向存储器控制器702提供每VMD的存储器访问的频率的历史。

[0051] 存储器控制器将用于每个VMD的使用信息与一个或多个阈值进行比较且通过向

VMD 发送适当的命令而使得 VMD 进入对应的操作模式。例如，当与 VMD 相关的使用信息小于阈值时，存储器控制器使得 VMD 进入对应的功率下降模式，且当与 VMD 相关的使用信息大于阈值时，存储器控制器使得 VMD 进入待机模式。根据被选择用于优化存储器模块的使用的度量选择所述阈值。例如，本发明的实施例包括当度量设置为 TET 时，节能模式可以被绕过或者阈值可以被设置为低，使得很少的 VMD 进入节能模式。另一方面，通过设置度量为 TEC 或 EDP，阈值比与 TET 相关的阈值相对更高，使得若干 VMD 能够进入节能模式。

[0052] 本发明的实施例还包括运行在多核处理器上的一个或多个应用或者编译器向存储器控制器提供关于一个或多个应用的存储器访问模式或所需的存储器量的特性信息。特性信息和度量经由诸如操作系统或者虚拟机的运行时系统被发送到存储器控制器，所述虚拟机是类似于真实计算机的执行一个或多个应用的计算机的软件实现。运行时系统为存储器控制器解释度量和特性信息且可以指导存储器控制器选择用于应用的适当操作模式。例如，假设系统操作员在多个应用并发地运行在多核处理器的内核中的情况下选择 EDP 度量，其中应用作者或编译器提供的特性信息将大多数应用标识为频繁存储器访问应用。结果，运行时系统可以指导存储器控制器将 MCDIMM 配置为不使用功率下降模式，而不收集关于存储器访问的数目的统计信息。而且，调度、监控和支持运行应用的运行时系统的其他元件或系统管理程序可以指导存储器控制器配置 MCDIMM。

[0053] 图 8A 示出呈现根据本发明的实施例的 MCDIMM 700 的每个 VMD 的使用信息的条形图 800。图 800 的每一条可以代表在一定的时间段内访问 MCDIMM 700 的 VMD 的频率或次数。图 800 包括分别代表阈值 T_1、T_2 和 T_{max} 的三个虚线 801-803。所述阈值也与三个不同的功率下降模式 PDM_1、PDM_2 和 PDM_{max} 相关。PDM_{max} 通过关闭最大数量的内部存储器芯片组件比 PDM_1 和 PDM_2 节省更多的功率，但是要求最长的延迟时间来加电；PDM_1 通过关闭最少的内部存储器芯片组件提供最少的能量节省，但是要求最短的延迟时间来加电；且 PDM_2 提供 PDM_{max} 和 PDM_1 之间的能量节省且要求中间的延迟时间来加电。

[0054] 图 8A 中示出的阈值 T_1、T_2 和 T_{max} 801-803 可以代表通过设置度量为 TEC 或 EDP 确定的阈值。阈值代表可接受性能和能量效率之间的均衡。例如，条形图 800 揭示 VMD_0、VMD_2、VMD_k、VMD_{k+1}、和 VMD_{k-2} 全都具有超过阈值 T_1 的使用信息。换句话说，存储器控制器在一个或多个应用运行的时候经常使用这些 VMD。因而，不是使得这些 VMD 进入节能模式之一，当它们不活动地处理存储器请求时，存储器控制器使其进入待机模式。另一方面，如图 8B 所示，与 VMD_1 相关的使用信息小于 T_{max}，与 VMD_{n-3} 相关的使用信息大于 T_{max} 且小于 T_2，且与 VMD_{n-1} 相关的使用信息大于 T_2 且小于 T_1。因而，为了节省能量，存储器控制器使得 VMD_1 进入 PDM_{max}，使得 VMD_{n-3} 进入 PDM_2，且使得 VMD_{n-1} 进入 PDM_1，直到 VMD_1、VMD_{n-3} 和 VMD_{n-1} 被加电以响应于存储器请求为止。

[0055] 图 9A 示出条形图 800，其表示图 8A 中示出的 MCDIMM 700 的每个 VMD 的使用信息，但是阈值根据设置度量为 TET 而改变。注意表示与每个 VMD 相关的使用信息的条并未与图 8A 中示出的条有所不同。然而，因为度量变为 TET，图 8A 中表示的阈值 T_1、T_2 和 T_{max} 变为在图 9A 中由虚线 901-903 表示的阈值 T'_1、T'_2 和 T'_{max}。在该特定示例中，性能比能量效率更重要。因而，图 9A 揭示出仅一个 VMD 落在阈值之下。具体而言，与 VMD_1 相关的使用信息大于阈值 T'_2 且小于阈值 T'_1。存储器控制器使得 VMD_1 进入功率下降模式 PDM_1 达一定的时间段，直到 VMD_1 被加电以用于存储器请求为止。当剩余 VMD 不活动地处理存储器请求时，

存储器控制器使得这些 VMD 进入待机模式。

[0056] 在某些实施例中，存储器控制器可以选择使用哪个操作模式。在某些实施例中，当存储器被很频繁地使用或者性能更关键时，存储器控制器不使用节能模式。

[0057] 方法实施例是动态的，因为使用信息可以由存储器控制器定期地收集且与每个 VMD 相关的使用信息在一个或多个应用运行的时候被更新。结果，基于当前使用信息，VMD 可以在一个或多个应用运行的时候被定期地切换到不同操作模式，而不禁用存储器访问。另外，在某些实施例中，度量还可以在一个或多个应用运行的时候由计算机系统操作员改变。

[0058] 图 10 示出根据本发明的实施例的用于动态地使得存储器模块的 VMD 进入操作模式的方法的控制流程图。在步骤 1001，度量（诸如度量 TET、TEC 或 EDP）被选择以优化与运行一个或多个应用相关的存储器性能和 / 或能量消耗。如上所述，度量可以由计算机系统操作员、一个或多个应用或者操作系统选择。在步骤 1002，执行一个或多个应用。在步骤 1003，操作系统选择一个或多个内核来处理一个或多个应用。在步骤 1004，基于一个或多个应用的存储器要求，操作系统选择 MCDIMM 的一个或多个 VMD。在步骤 1005，根据度量和 / 或应用本身提供的特性信息，运行时系统可以指导存储器控制器到步骤 1006 且进入步骤 1006-1009 中实施的方法的节能部分。否则，运行时系统可以指导存储器控制器跳过方法的节能部分。例如，当一个或多个应用提供的特性信息将所述应用标识为频繁存储器访问应用时，运行时系统可以指导存储器控制器跳过步骤 1006-1009 中实施的方法的节能部分。在步骤 1006 的 for 循环中，针对存储器模块的每个 VMD 执行步骤 1007-1008。在步骤 1007，如上面参考图 7 所描述的，存储器控制器在一定的时间段内收集和存储 VMD 使用信息。在步骤 1008，存储器控制器基于度量和使用信息使得 VMD 进入操作模式，如下面在图 11 的控制流程图中描述的。例如，当 VMD 不活动地处理存储器请求时，存储器控制器可以使得 VMD 进入待机模式或者很多节能模式之一，如上面参考图 8-9 所述的。在步骤 1009，当所有 VMD 都进入操作模式时，前进到 1010，否则针对另一 VMD 重复步骤 1007 和 1008。在步骤 1010 中，当一个或多个应用的运行没有结束时，本发明的实施例可以可选地包括步骤 1011，否则当一个或多个应用结束运行时，前进到步骤 1012，其中针对不同组的一个或多个应用或者相同组的一个或多个应用的后续运行，重复步骤 1001-1009。在步骤 1011，在一个或多个应用仍在运行的时候，计算机系统操作员可以改变度量。例如，计算机系统操作员可以在步骤 1001 中初始设置度量为 TET，且稍后在一个或多个应用运行的时候改变度量为 TEC。

[0059] 图 11 示出根据本发明的实施例的用于动态地使得 VMD 进入功率下降模式的方法的控制流程图。在该实施例中，如参考图 8-9 所述，假设存储器芯片具有在步骤 1103、1105 和 1107 中表示的三个节能功率下降模式。在步骤 1101，如上面参考图 8-9 所述，基于图 10 的步骤 1001 中选择的度量确定对应于三个功率下降模式的阈值。存储器控制器使用在图 10 的步骤 1006 中收集和存储的使用信息在步骤 1102-1107 中选择一个或三个功率下降模式。功率下降模式是上面参考图 8A 所述的 PDM_1、PDM_2 和 PDM_{max}。在步骤 1102，当使用信息小于阈值 T_{max} 时，前进到步骤 1103，否则前进到步骤 1104。在步骤 1103，存储器控制器使得 VMD 进入 PDM_{max}。在步骤 1104，当使用信息小于阈值 T_2 时，前进到步骤 1105，否则前进到步骤 1106。在步骤 1105，存储器控制器使得 VMD 进入 PDM_2。在步骤 1106，当使用信息小于阈值 T_1 时，前进到步骤 1107，否则前进到步骤 1108。在步骤 1107，存储器控制器使得 VMD 进

入 PDM_1。在步骤 1108，存储器控制器使得 VMD 进入待机模式。在其他实施例中，存储器芯片可以配置有一个、两个或四个或更多不同的功率下降模式。

[0060] 为了解释的目的，前面的描述使用特定词汇来提供本发明的透彻理解。然而，本领域技术人员显而易见的是，为了实践本发明，并不需要具体细节。给出本发明具体实施例的前面描述，目的是进行说明和描述。它们并非意欲穷尽本发明或者将其限制为所公开的精确形式。显然，根据以上教导，很多修改和变化是可能的。示出并且描述实施例，以最佳地解释本发明的原理及其实际应用，由此使得本领域其他技术人员能够最佳地利用本发明以及具有适于所考虑的特定使用的各个修改的各个实施例。本发明的范围意欲由所附权利要求及其等同物所定义。

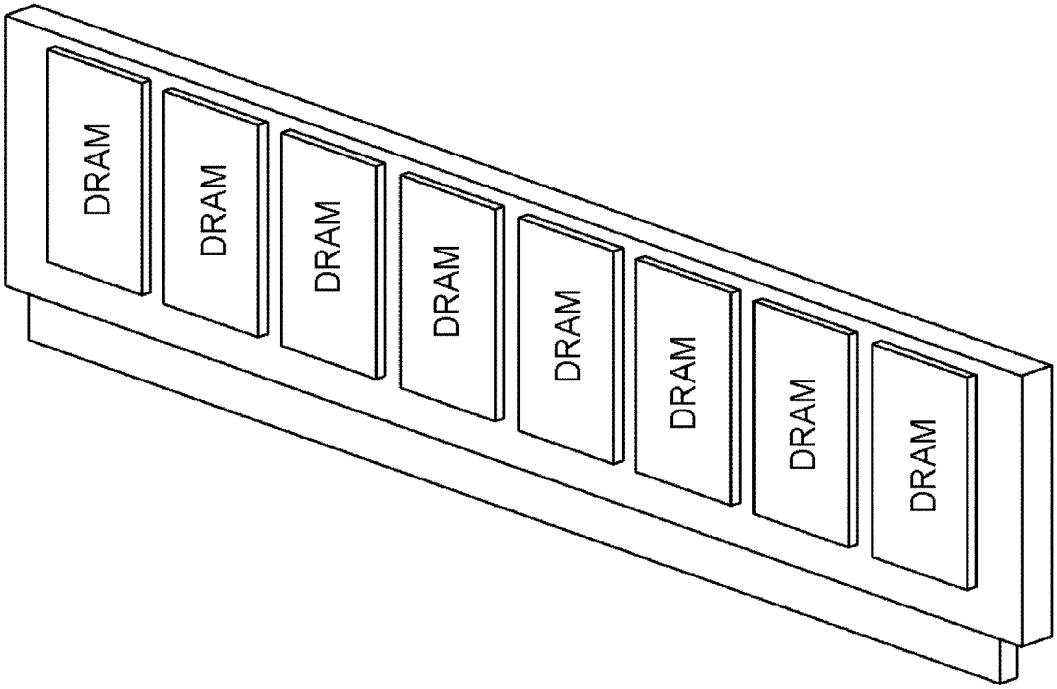


图 1A

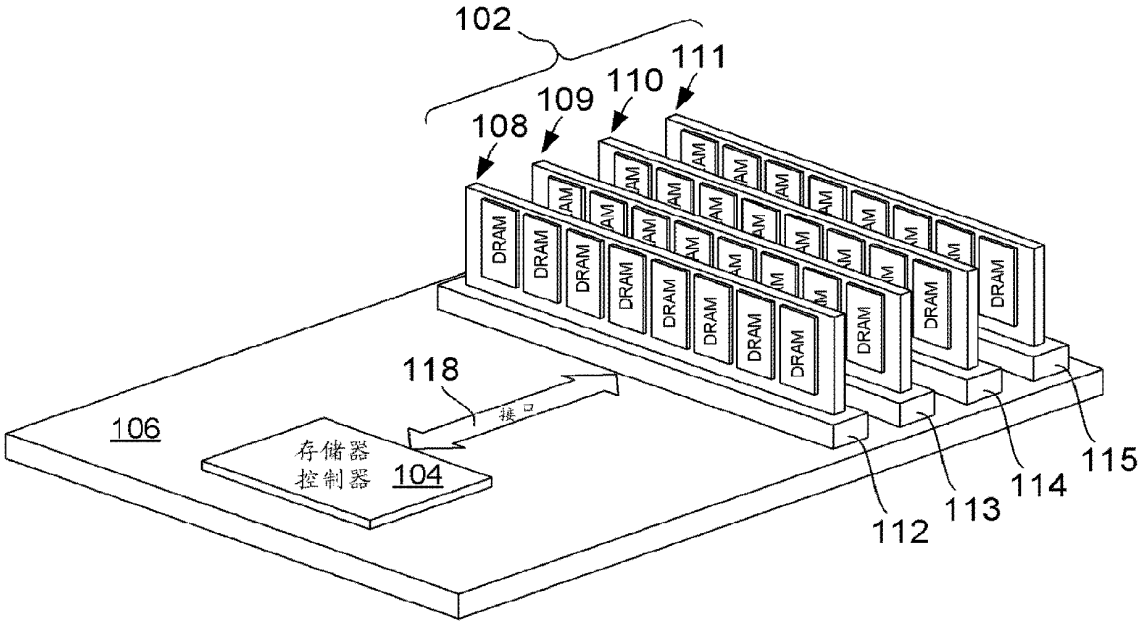


图 1B

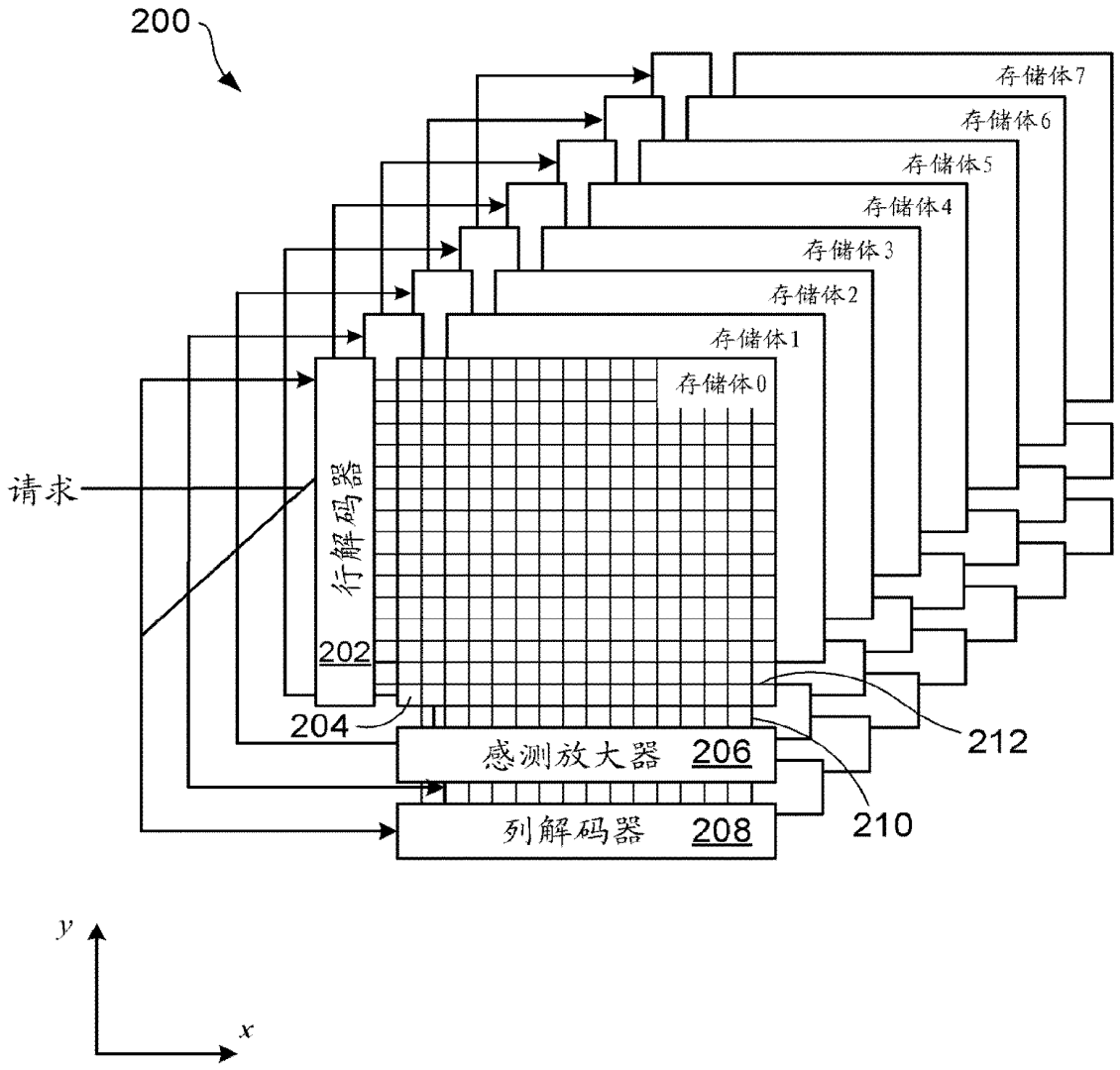

200
存储体7
存储体6
存储体5
存储体4
存储体3
存储体2
存储体1
存储体0
请求
行解码器
202
204
212
感测放大器 206
列解码器 208
210
y
x

图 2

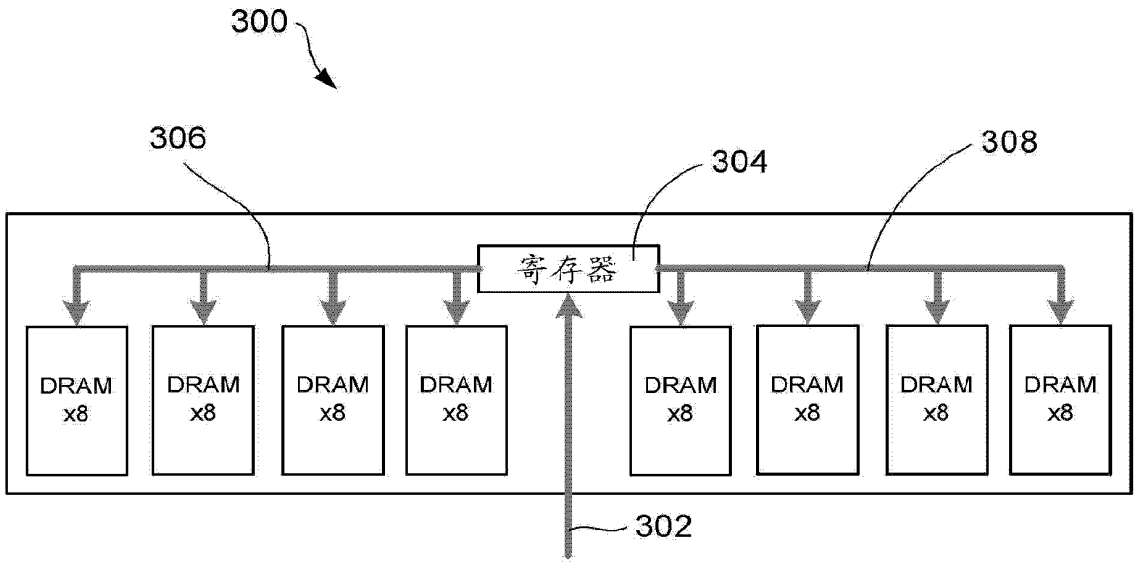

300
306
304
308
寄存器
DRAM x8
DRAM x8
DRAM x8
DRAM x8
DRAM x8
DRAM x8
DRAM x8
DRAM x8
302

图 3A

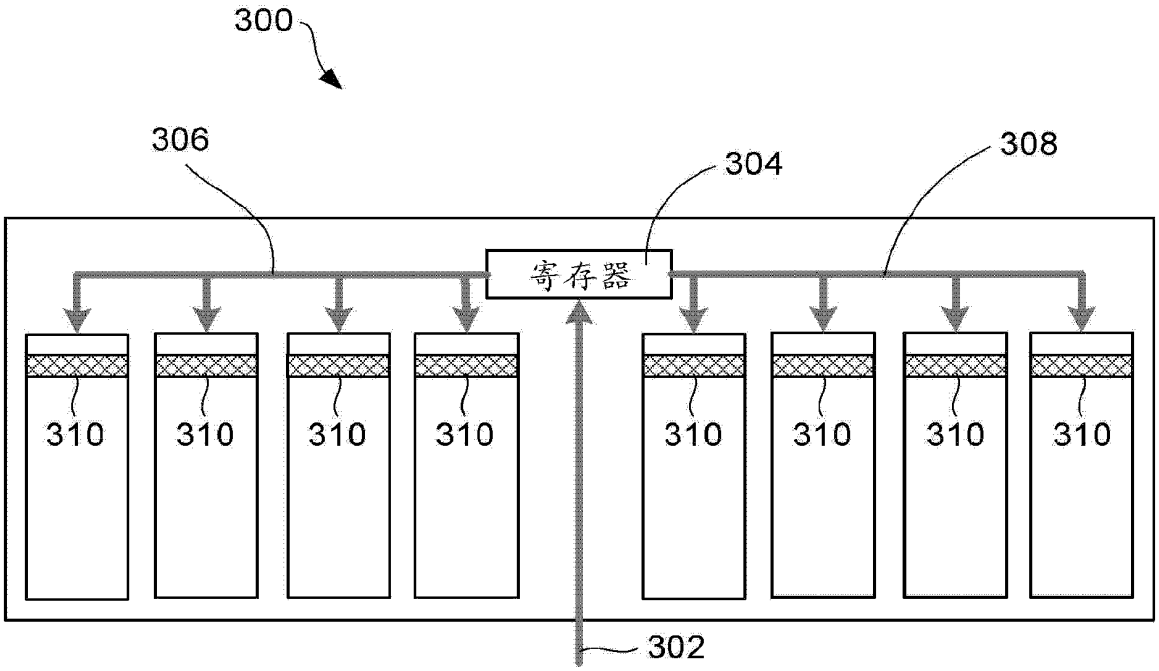

300
306
304
308
寄存器
310
310
310
310
310
310
310
310
302

图 3B

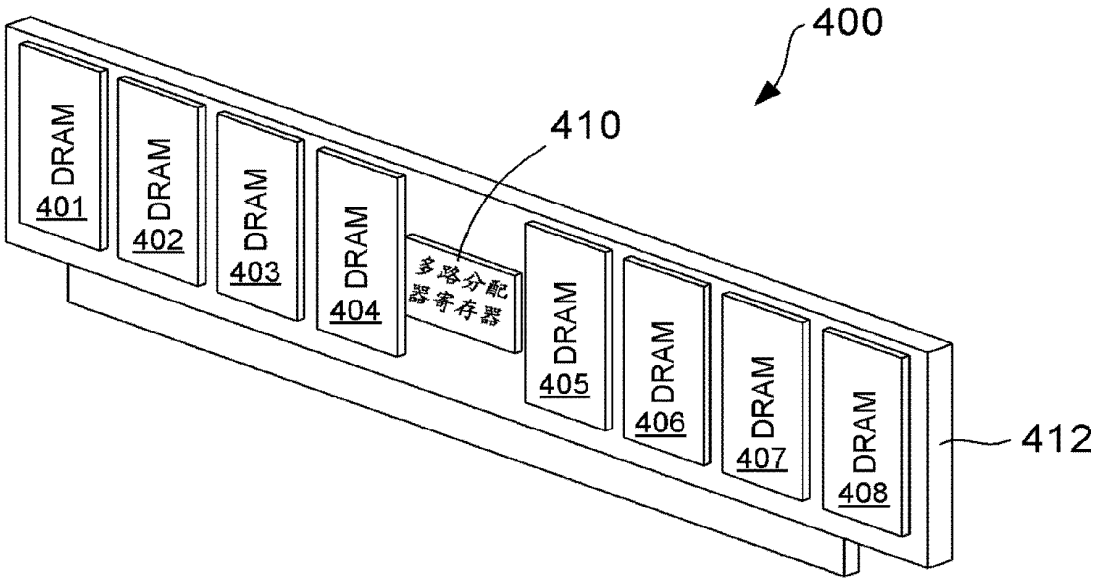

400
410
DRAM
401
DRAM
402
DRAM
403
DRAM
404
多路分配器寄存器
DRAM
405
DRAM
406
DRAM
407
DRAM
408
412

图 4A

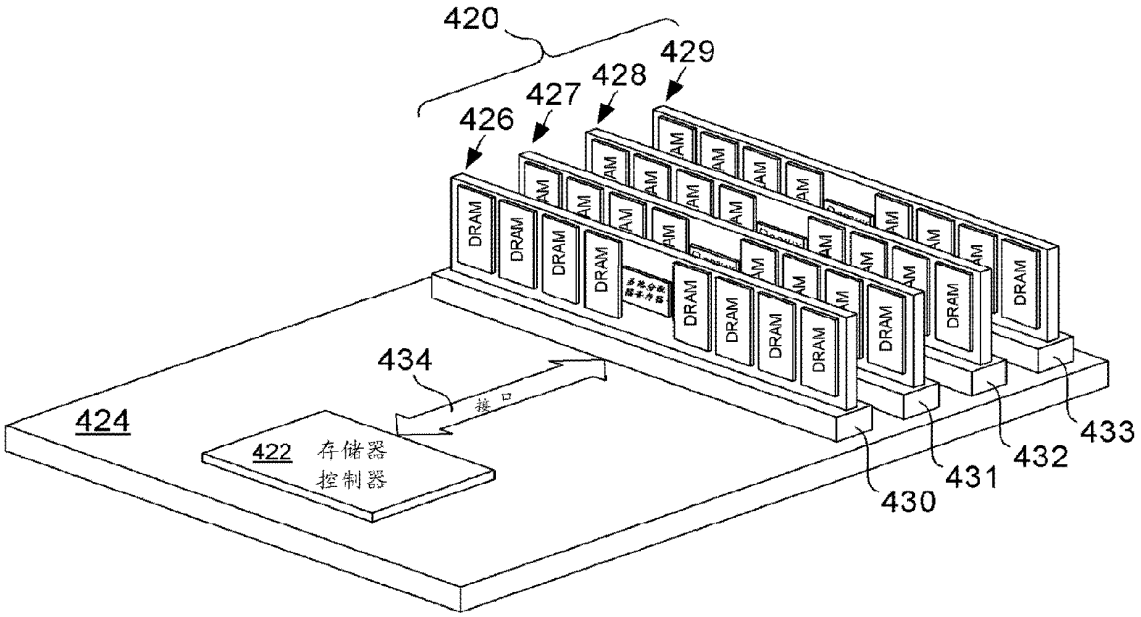

420
429
428
427
426
DRAM
AM
434
接口
424
422
存储器控制器
430
431
432
433

图 4B

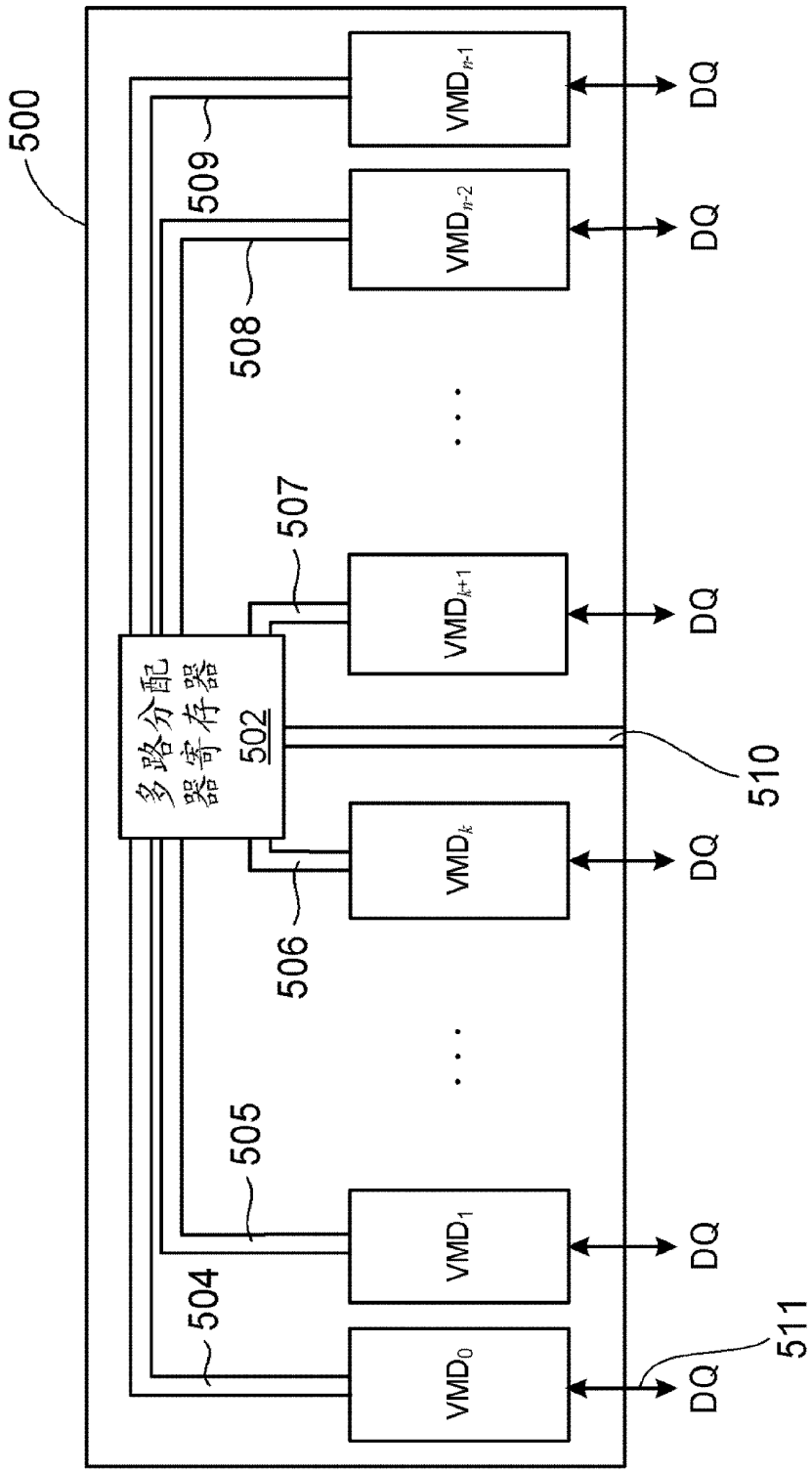

500
多路分配器寄存器
502
VMD0
VMD1
VMDk
VMDk+1
VMDn-2
VMDn-1
DQ
DQ
DQ
DQ
DQ
DQ
504
505
506
507
508
509
510
511

图 5A

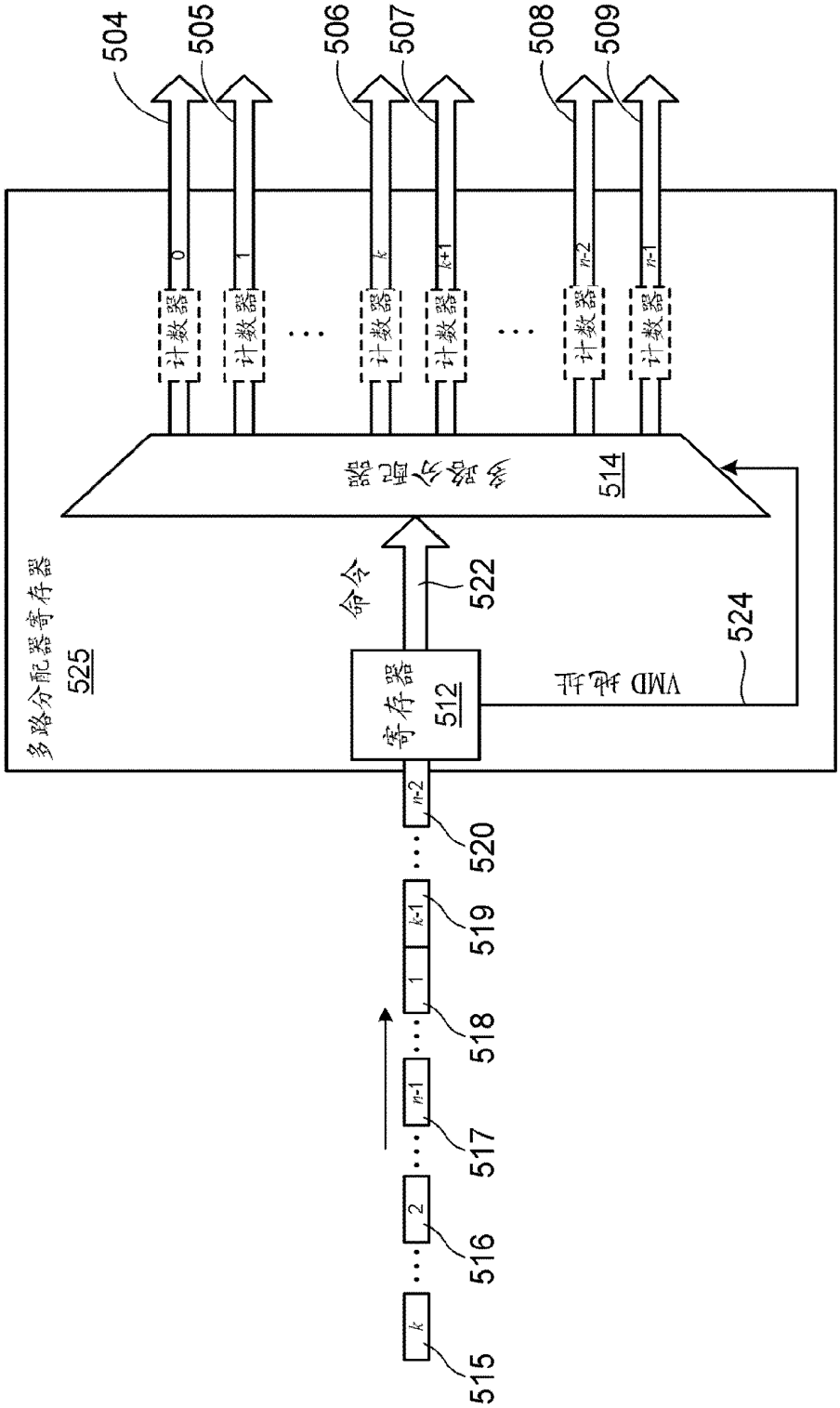

504
505
506
507
508
509
计数器
计数器
计数器
计数器
计数器
计数器
0
1
k
k+1
n-2
n-1
多路分配器
514
命令
522
524
多路分配器寄存器
525
寄存器
512
VMD 地址
n-2
520
k-1
519
1
518
n-1
517
2
516
k
515

图 5B

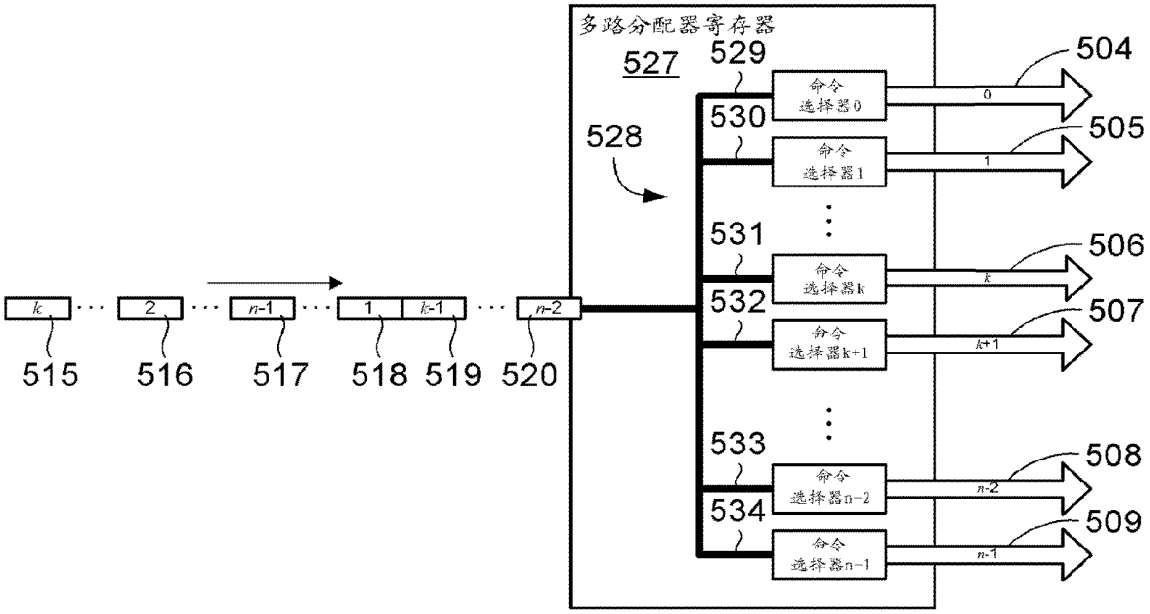
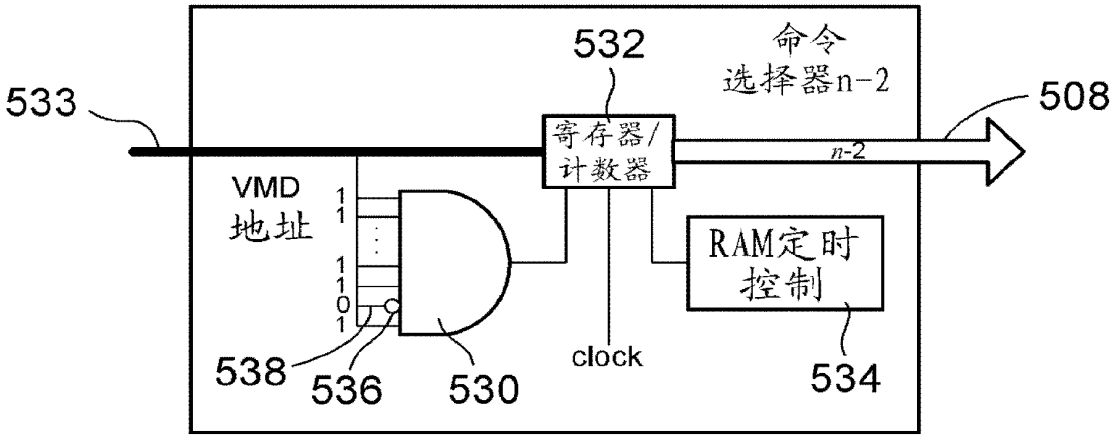


图 5C



VMD_{n-2} 地址 = 11 . . . 1101

图 5D

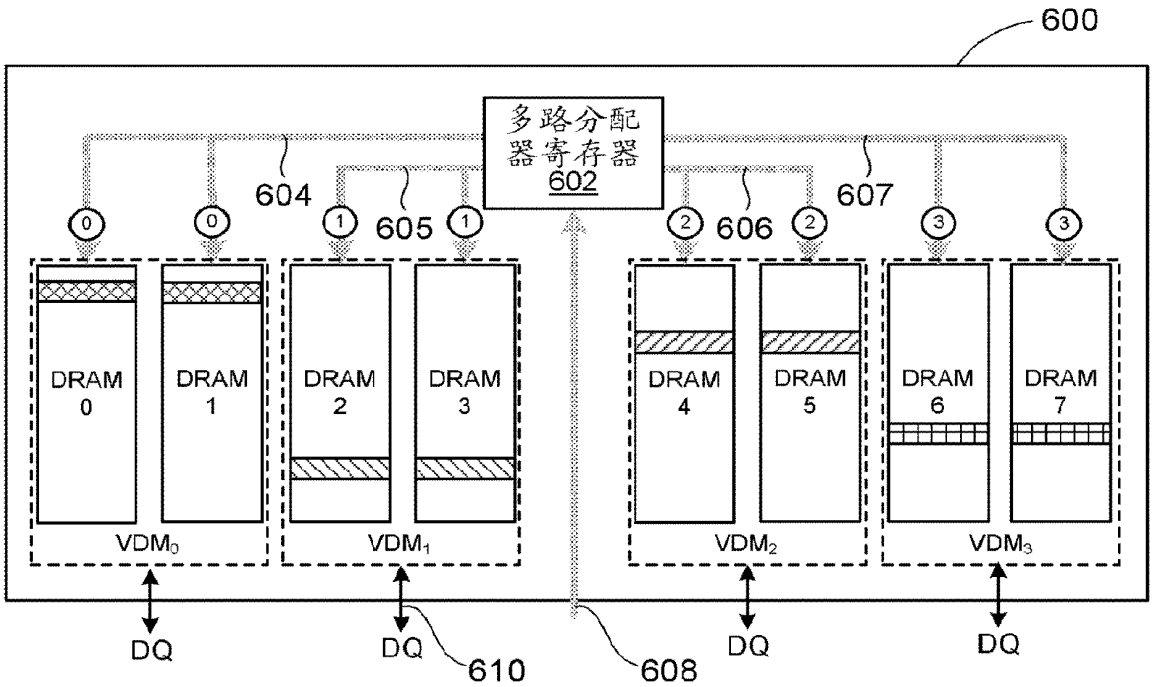

600
多路分配器寄存器
602
604
605
606
607
0
0
1
1
2
2
3
3
DRAM 0
DRAM 1
DRAM 2
DRAM 3
DRAM 4
DRAM 5
DRAM 6
DRAM 7
VDM0
VDM1
VDM2
VDM3
DQ
DQ
DQ
DQ
610
608

图 6

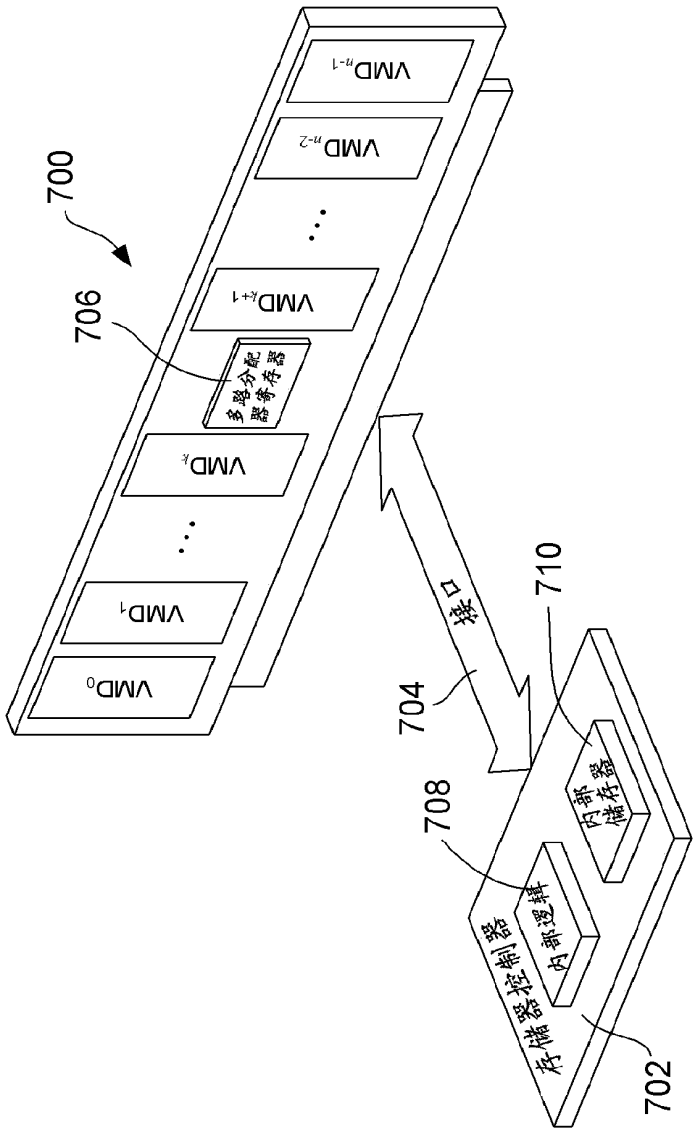

700
VMD0
VMD1
VMDk
多路分配器
VMDk+1
VMDn-2
VMDn-1
706
704
接口
710
内部存储器
708
内部逻辑
存储器控制器
702

图 7

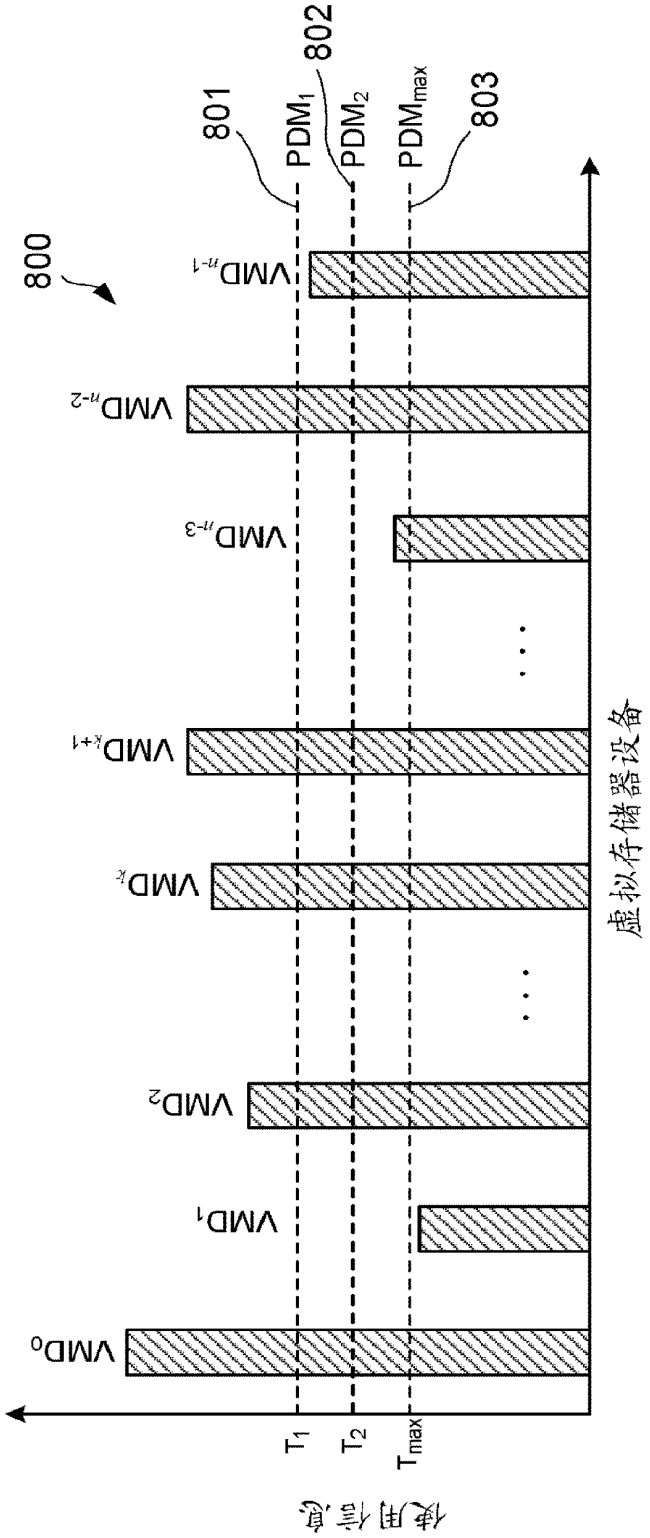

800
801
802
803
PDM1
PDM2
PDMmax
VMDn-1
VMDn-2
VMDn-3
VMDk+1
VMDk
VMD2
VMD1
VMD0
虚拟存储器设备
T1
T2
Tmax
使用信息

图 8A

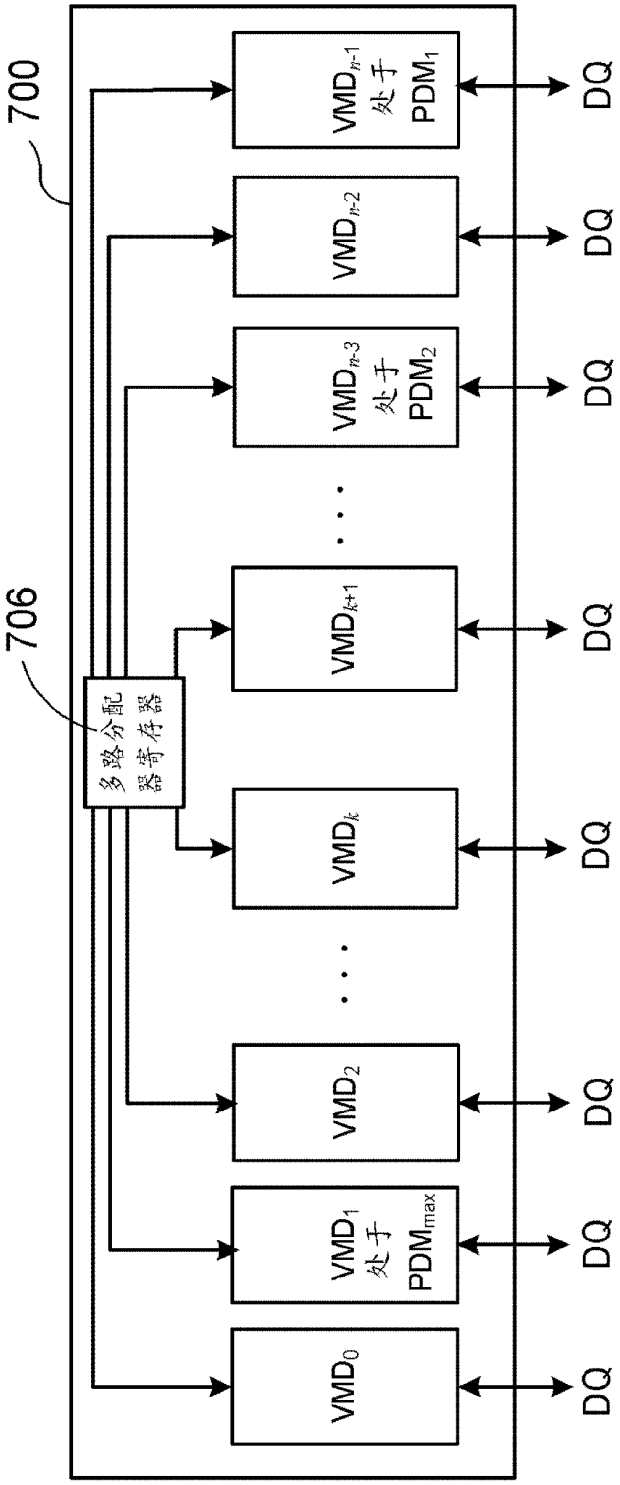

700
706
多路分配器寄存器
VMD0
VMD1 处于 PDMmax
VMD2
VMDk
VMDk+1
VMDn-3 处于 PDM2
VMDn-2
VMDn-1 处于 PDM1
DQ

图 8B

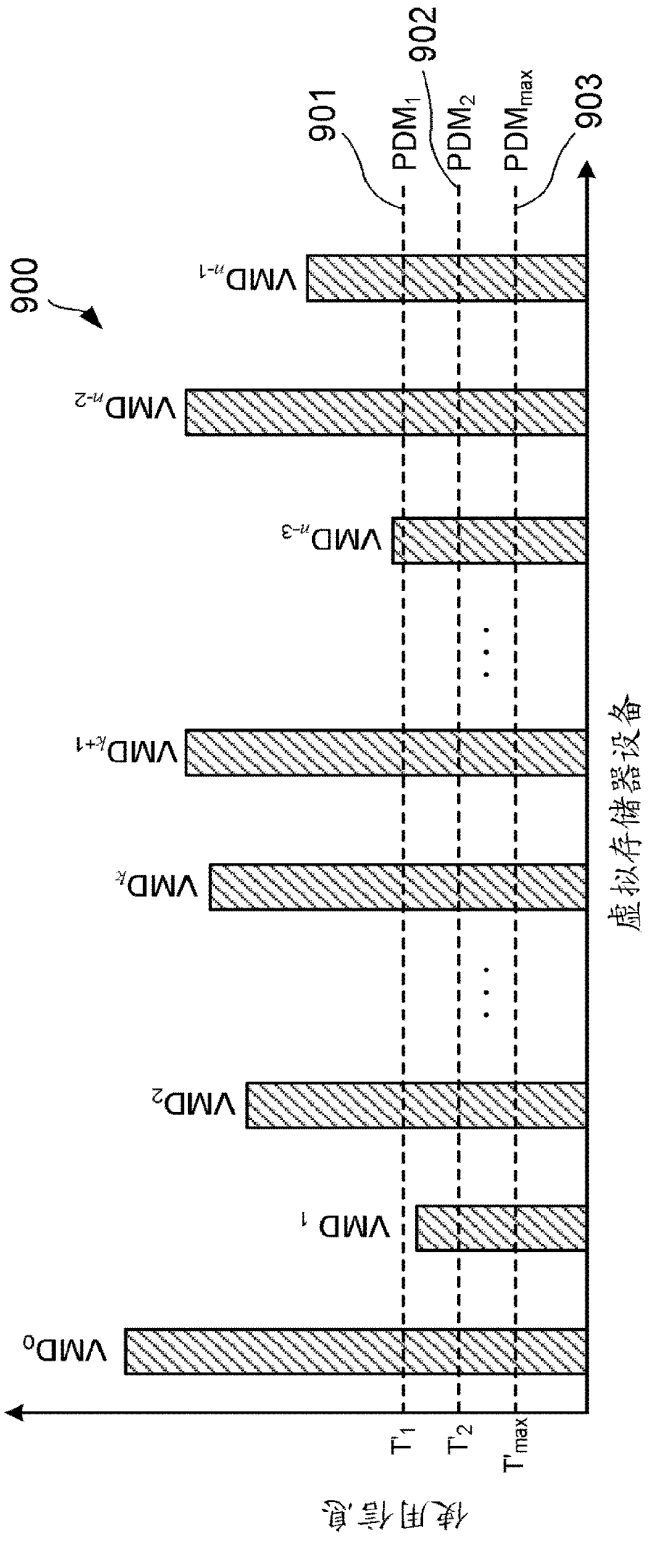

900
901
902
903
PDM1
PDM2
PDMmax
VMD0
VMD 1
VMD2
VMDk
VMDk+1
VMDn-3
VMDn-2
VMDn-1
虚拟存储器设备
T'1
T'2
T'max
使用信息

图 9A

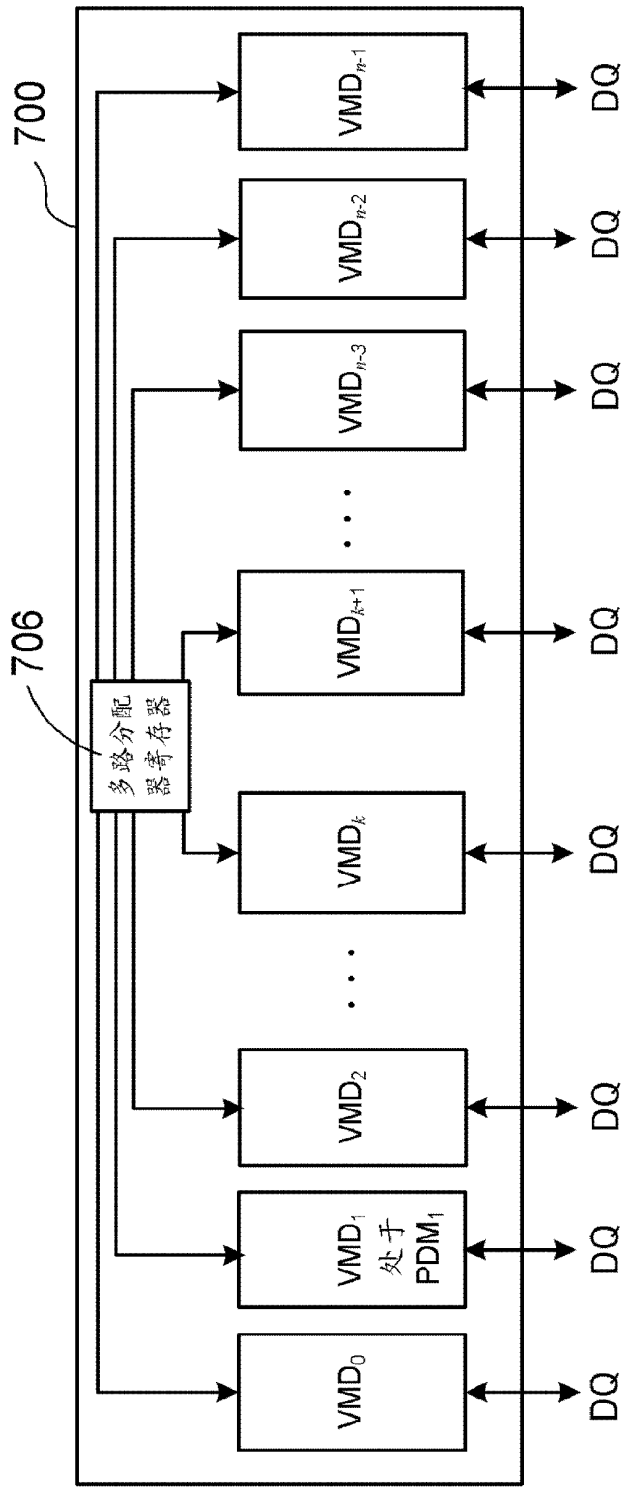

700
706
多路分配器寄存器
VMD0
VMD1 处于 PDM1
VMD2
VMDk
VMDk+1
VMDn-3
VMDn-2
VMDn-1
DQ
DQ
DQ
DQ
DQ
DQ
DQ

图 9B

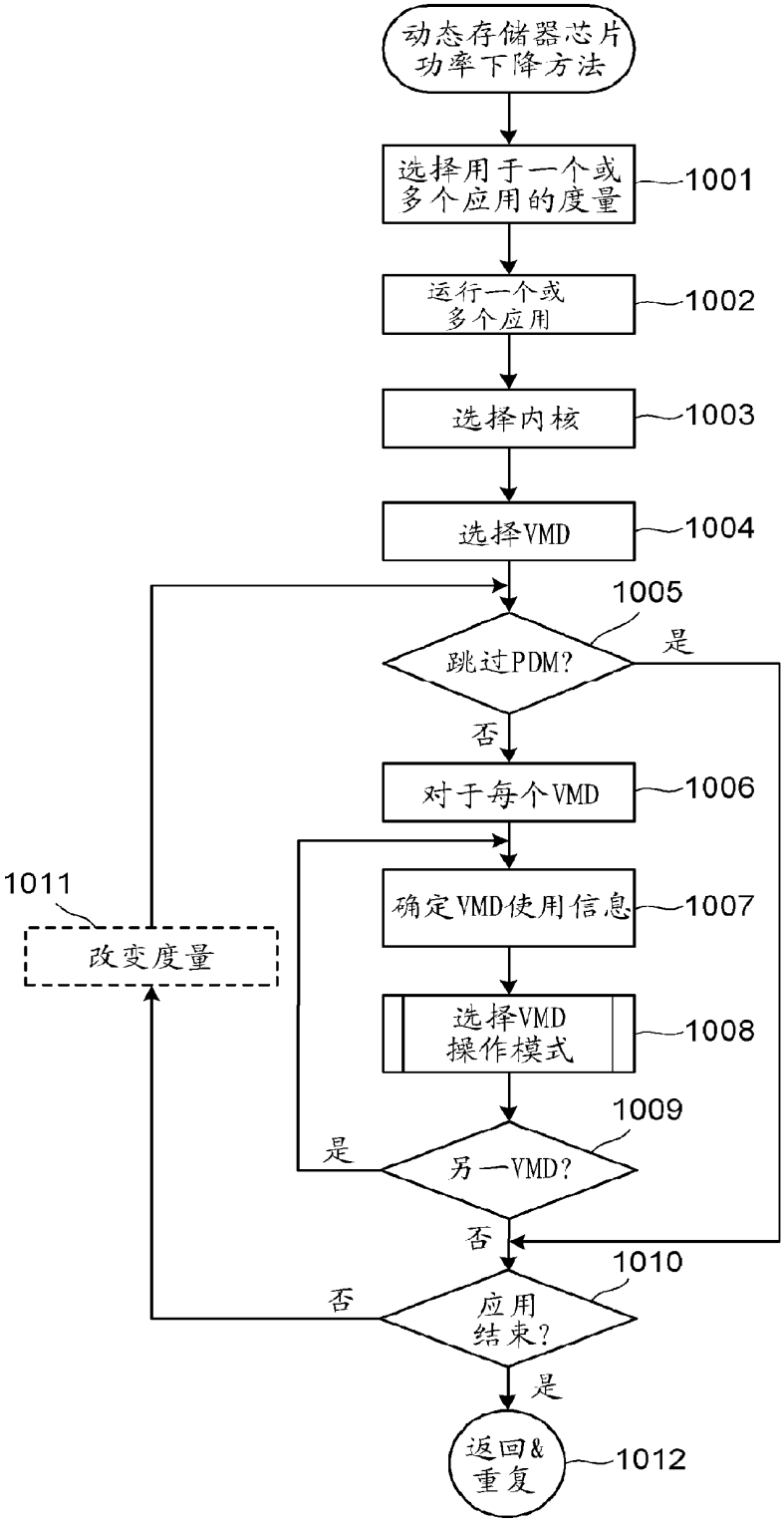

动态存储器芯片功率下降方法
选择用于一个或多个应用的度量
1001
运行一个或多个应用
1002
选择内核
1003
选择VMD
1004
1005
跳过PDM?
是
否
对于每个VMD
1006
1011
改变度量
确定VMD使用信息
1007
选择VMD操作模式
1008
1009
是
另一VMD?
否
1010
否
应用结束?
是
返回&重复
1012

图 10

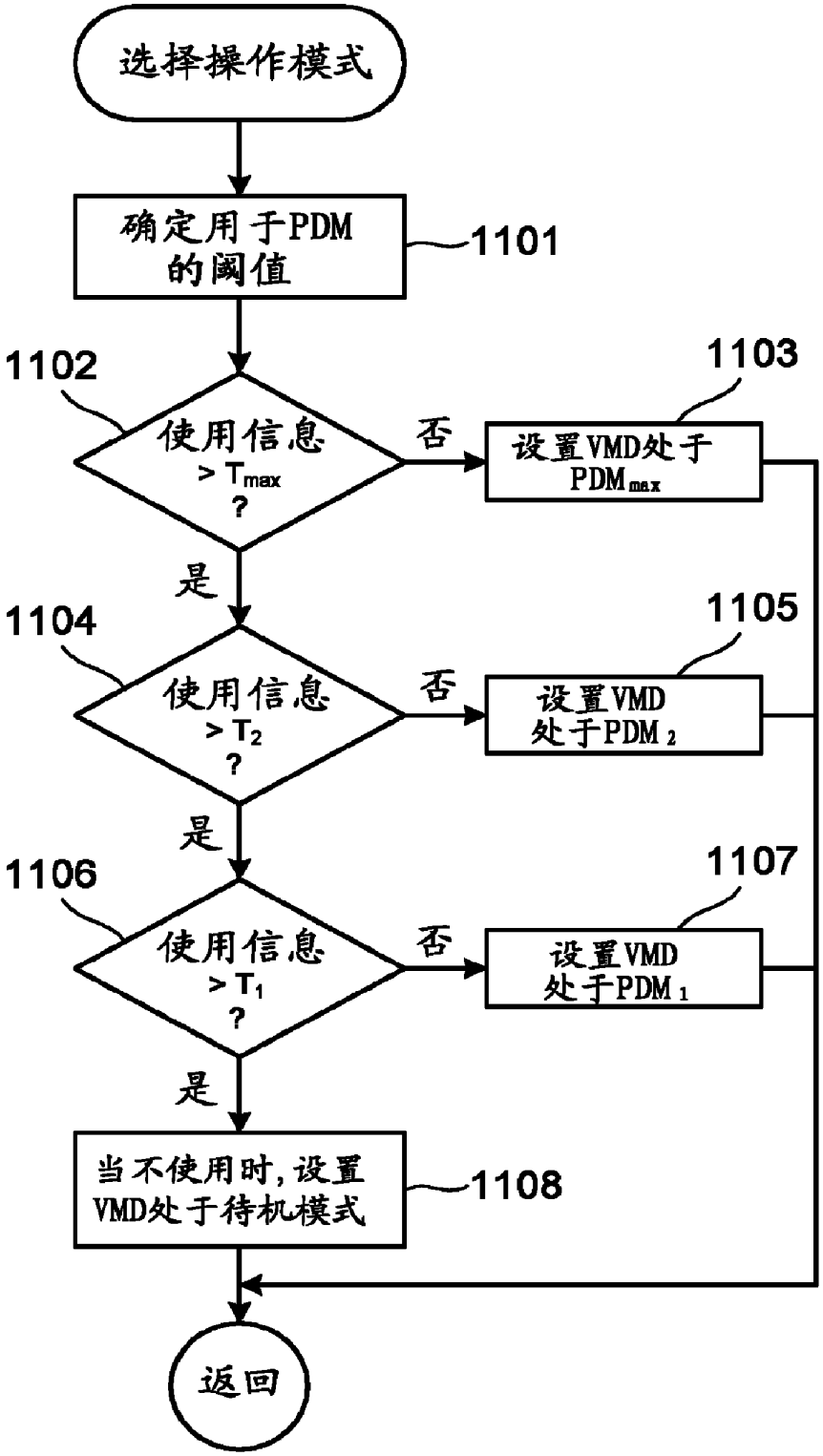

选择操作模式
确定用于PDM的阈值
1101
1102
使用信息 > T_{max} ?
否
1103
设置VMD处于 PDM_{max}
是
1104
使用信息 > T_2 ?
否
1105
设置VMD处于 PDM_2
是
1106
使用信息 > T_1 ?
否
1107
设置VMD处于 PDM_1
是
当不使用时，设置VMD处于待机模式
1108
返回

图 11

Abstract of TW201123198

Memory power supply circuit

ABST:
A memory power supply circuit includes a single-phase PWM signal controller, a first transistor and a second transistor, a first a field-effect transistor (FET) and a second FET. The first and the second transistors receive an enable signal and control the PWM signal controller to alternately output a high level voltage and a low level voltage via a high pass driving pin and a low pass driving pin thereof, to alternately control the first and the second FETs to be turned on and turned off. At the same time, a phase pin of the PWM signal controller outputs a PWM signal and receives a power supply via a capacitor and a resistor, and then outputs a power voltage to a memory.

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(71)申請人：鴻海精密工業股份有限公司 (中華民國) HON HAI PRECISION INDUSTRY CO., LTD. (TW)
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申請實體審查：無 申請專利範圍項數：10 項 圖式數：1 共 14 頁

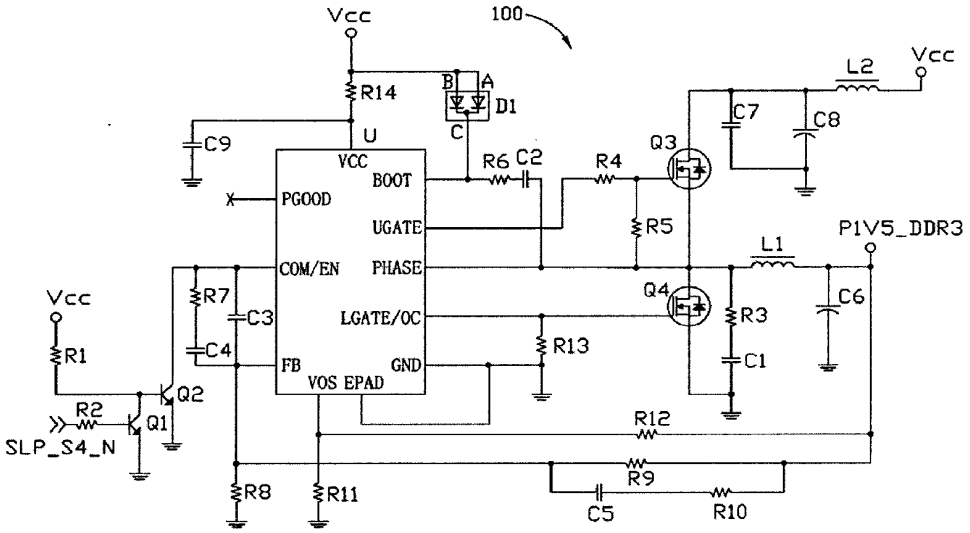
(54)名稱

記憶體供電電路

MEMORY POWER SUPPLY CIRCUIT

(57)摘要

一種記憶體供電電路，包括一單相脈寬調製訊號控制器、一第一及一第二電晶體、一第一及一第二場效應電晶體，該第一及第二電晶體接收一使能控制訊號並在該使能訊號輸入時控制該單相脈寬調製訊號控制器工作，以使該單相脈寬調製訊號控制器的高通驅動引腳及低通驅動引腳交替輸出高低電平以交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊號並透過一電容及一電阻接收電源，再透過一電感輸出一供電電壓給記憶體。



100：記憶體供電電路
C1-C9：電容
D1：二極體元件
L1：電感
L2：電感
Q1：電晶體
Q2：電晶體
Q3：場效應電晶體
Q4：場效應電晶體
R1-R14：電阻
U：單相脈寬調製訊號控制器
Vcc：5V 電源

智專收字第0982074484-0
DTD版本：1.0.0
專利案號：098143494
日期：98年12月18日

發明專利說明書

※申請案號：098143494　※ＩＰＣ分類：G11C 5/14 (2006.01)
※申請日：98.12.18

一、發明名稱：

記憶體供電電路

Memory Power Supply Circuit

二、中文發明摘要：

一種記憶體供電電路，包括一單相脈寬調製訊號控制器、一第一及一第二電晶體、一第一及一第二場效應電晶體，該第一及第二電晶體接收一使能控制訊號並在該使能訊號輸入時控制該單相脈寬調製訊號控制器工作，以使該單相脈寬調製訊號控制器的高通驅動引腳及低通驅動引腳交替輸出高低電平以交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊號並透過一電容及一電阻接收電源，再透過一電感輸出一供電電壓給記憶體。

三、英文發明摘要：

A memory power supply circuit includes a single-phase PWM signal controller, a first transistor and a second transistor, a first a field-effect transistor (FET) and a second FET. The first and the second transistors receive an enable signal and control the PWM signal controller to alternately output a high level voltage and a low level voltage via a high pass driving pin and a low pass driving pin thereof, to alternately control the first and the second FETs to be turned on and turned off. At the same time, a phase pin of the PWM signal controller outputs a PWM signal and receives a power supply via a capacitor and a resistor, and

then outputs a power voltage to a memory.

四、指定代表圖：

(一)本案指定代表圖為：第（1）圖

(二)本代表圖之元件符號簡單說明：

記憶體供電電路：100

單相脈寬調製訊號控制器：U

5V電源：Vcc

電晶體：Q1、Q2

場效應電晶體：Q3、Q4

電感：L1、L2

二極體元件：D1

電阻：R1-R14

電容：C1-C9

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

六、發明說明：

【發明所屬之技術領域】

[0001] 本發明係關於一種供電電路，尤指一種用於給記憶體提供電壓的供電電路。

【先前技術】

[0002] 隨著電子技術迅速發展，低壓大電流設計成為主流，因為電路設計中，電壓愈低，，電路消耗功率愈小。電源設計人員所面臨的最大挑戰是如何滿足更大的功率、更小的電壓容限以及更快的瞬態回應，並降低電源的總成本。隨著CPU電流和功率增大，記憶體電流也要求愈來愈大，並且記憶體供電電壓也愈來愈小。我們知道，最初DRAM記憶體的供電電壓是5V，SDRAM記憶體的供電電壓是3.3V，DDR記憶體的供電電壓是2.5V，DDR2記憶體的供電電壓是1.8V，DDR3記憶體的供電電壓則降為1.5V（其中DRAM、SDRAM、DDR、DDR2、DDR3為不同時期記憶體的不同標準）。同時記憶體頻率也愈來愈高，回應速度愈來愈快，當然消耗功率也愈來愈大，因此如何設計出大電流、低功耗的穩定電路是業界需要解決的問題。

【發明內容】

[0003] 鑒於上述內容，有必要提供一種大電流、低功耗的記憶體供電電路。

[0004] 一種記憶體供電電路，包括一單相脈寬調製訊號控制器、一第一及一第二電晶體、一第一及一第二場效應電晶體及一第一及一第二電感，該單相脈寬調製訊號控制器的使能引腳連接至該第二電晶體的集極，該第二電晶體

的射極接地，基極連接該第一電晶體的集極並透過一第一電阻連接至一電源，該第一電晶體的射極接地，基極透過一第二電阻接收一使能控制訊號，該單相脈寬調製訊號控制器的相位引腳透過該第一電感連接至一電壓輸出引腳以提供電壓給記憶體，還依次透過一第三電阻及一第一電容接地，該單相脈寬調製訊號控制器的高通驅動引腳透過一第四電阻連接至該第一場效應電晶體的閘極，該第一場效應電晶體汲極透過該第二電感連接至該電源，該第一場效應電晶體的源極連接至該第二場效應電晶體的汲極，該第一場效應電晶體的閘極還透過一第五電阻連接至該第二場效應電晶體的汲極，該單相脈寬調製訊號控制器的低通驅動引腳連接至該第二場效應電晶體的閘極，該第二場效應電晶體的源極接地，當該使能控制訊號輸入時，該第一電晶體導通，該第二電晶體截止，該單相脈寬調製訊號控制器的高通驅動引腳及低通驅動引腳交替輸出高低電平以交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊號並透過一第二電容及一第六電阻接收該電源，再透過該第一電感及該電壓輸出引腳輸出一供電電壓給該記憶體。

[0005] 上述記憶體供電電路透過該第一及第二電晶體接收該使能控制訊號，並在該使能訊號輸入時控制該單相脈寬調製訊號控制器工作，以使該單相脈寬調製訊號控制器交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊

號並透過一第二電容及一第六電阻接收該電源，再透過該第一電感及該電壓輸出引腳輸出一大電流、低功耗且穩定的供電電壓給該記憶體。

【實施方式】

[0006] 請參照圖1，本發明記憶體供電電路100的較佳實施方式包括一單相脈寬調製訊號控制器U、兩電晶體Q1及Q2、兩場效應電晶體Q3及Q4、十四個電阻R1-R14、九個電容C1-C9、兩電感L1及L2、一由兩並聯的二極體組成的二極體元件D1及一5V電源Vcc。本實施方式中，該單相脈寬調製訊號控制器U的型號為ISL6341CRZ，該二極體組件D1的型號為BAT54C，其他實施方式中也可根據需要選取其他型號。

[0007] 該單相脈寬調製訊號控制器U的使能引腳COM/EN連接至該電晶體Q2的集極，該電晶體Q2的射極接地，基極連接該電晶體Q1的集極並透過該電阻R1連接至該5V電源Vcc，該電晶體Q1的射極接地，基極透過該電阻R2接收一使能控制訊號SLP_S4_N。該單相脈寬調製訊號控制器U的使能引腳COM/EN透過該電容C3連接至其上的回饋引腳FB，還依次透過該電阻R7及電容C4連接至該回饋引腳FB。該回饋引腳FB透過該電阻R8接地，還透過該電阻R9連接一電壓輸出引腳P1V5_DDR3。該單相脈寬調製訊號控制器U的偵測引腳VOS透過該電阻R11接地，還透過該電阻R12連接該電壓輸出引腳P1V5_DDR3，該電容C5與電阻R10串聯後再與該電阻R9並聯，該電容C6連接在該電壓輸出引腳P1V5_DDR3與地之間，該電壓輸出引腳P1V5_DDR3連

接至一DDR3記憶體（未示出）的電源端，以提供1.5V電壓給該DDR3記憶體。

[0008] 該單相脈寬調製訊號控制器U的電源引腳VCC透過該電阻R14連接至該5V電源Vcc並透過該電容C9接地。該單相脈寬調製訊號控制器U的自舉引腳BOOT連接至該二極體元件D1的陰極C，該二極體元件D1的陽極A、B連接至該5V電源Vcc，該自舉引腳BOOT還依次透過該電阻R6及C2連接至該單相脈寬調製訊號控制器U的相位引腳PHASE，該相位引腳PHASE透過該電感L1連接至該電壓輸出引腳P1V5_DDR3，還依次透過該電阻R3及電容C1接地。該單相脈寬調製訊號控制器U的高通驅動引腳UGATE透過該電阻R4連接至該場效應電晶體Q3的閘極，該場效應電晶體Q3的汲極透過該電感L2連接至該5V電源Vcc，該兩電容C7及C8分別連接在該場效應電晶體Q3的汲極與地之間。

[0009] 該場效應電晶體Q3的源極連接至該場效應電晶體Q4的汲極，該場效應電晶體Q3的閘極還透過電阻R5連接至該場效應電晶體Q4的汲極，該單相脈寬調製訊號控制器U的低通驅動引腳LGATE/OC連接至該場效應電晶體Q4的閘極，該場效應電晶體Q4的源極接地。該低通驅動引腳LGATE/OC還透過該電阻R13接地，該單相脈寬調製訊號控制器U的接地引腳GND接地，該單相脈寬調製訊號控制器U的引腳EPAD接地，該單相脈寬調製訊號控制器U的引腳PGOOD空接。

[0010] 工作時，該使能控制訊號SLP_S4_N為低電平有效，即當該使能控制訊號SLP_S4_N為低電平時，系統進入S4狀態

（此狀態記憶體、硬碟均不工作），該電晶體Q1截止，該電晶體Q2導通，該單相脈寬調製訊號控制器U不工作。

[0011] 當該使能控制訊號SLP_S4_N變為低電平時，系統退出S4狀態，該電晶體Q1導通，該電晶體Q2截止，該單相脈寬調製訊號控制器U開始工作，該單相脈寬調製訊號控制器U的高通驅動引腳UGATE及低通驅動引腳LGATE/OC交替輸出高低電平以交替控制該兩場效應電晶體Q3及Q4導通及截止，同時該單相脈寬調製訊號控制器U的相位引腳PHASE輸出一脈寬調製訊號並透過該電容C2、電阻R6及二極體元件D1接收該5V電源Vcc，然後再透過該電感L1輸出一1.5V電壓給該記憶體。該1.5V電壓還透過電阻R9及電阻R8回饋至該單相脈寬調製訊號控制器U的回饋引腳FB，以調節該高通驅動引腳UGATE、低通驅動引腳LGATE/OC及相位引腳PHASE的輸出訊號，從而產生穩定該電壓輸出引腳P1V5_DDR3輸出電壓的作用，上述電路結構可使該電壓輸出引腳P1V5_DDR3輸出大電流、低功耗且穩定的供電訊號給該記憶體。

[0012] 其中，該二極體元件D1產生隔離電壓的作用，該單相脈寬調製訊號控制器U的偵測引腳VOS用於偵測該電壓輸出引腳P1V5_DDR3輸出的電壓是否正常。該電阻R7、電容C4、電阻R10及電容C5組成輸出補償回路，採用此電路架構可明顯提高輸出電壓與輸出電流的精度。該電感L2產生濾波整流的作用，電路中的其他電容元件產生濾波的作用，以提高電路的整體性能，也可根據需要增加或減少上述各元件。

[0013] 綜上所述，本發明符合發明專利要件，爰依法提出專利申請。惟，以上所述者僅為本發明之較佳實施例，舉凡熟悉本案技藝之人士，在爰依本發明精神所作之等效修飾或變化，皆應涵蓋於以下之申請專利範圍內。

【圖式簡單說明】

[0014] 圖1係本發明記憶體供電電路較佳實施方式的電路圖。

【主要元件符號說明】

[0015] 記憶體供電電路：100

[0016] 單相脈寬調製訊號控制器：U

[0017] 5V電源：Vcc

[0018] 電晶體：Q1、Q2

[0019] 場效應電晶體：Q3、Q4

[0020] 電感：L1、L2

[0021] 二極體元件：D1

[0022] 電阻：R1-R14

[0023] 電容：C1-C9

七、申請專利範圍：

1．一種記憶體供電電路，包括一單相脈寬調製訊號控制器、一第一及一第二電晶體、一第一及一第二場效應電晶體及一第一及一第二電感，該單相脈寬調製訊號控制器的使能引腳連接至該第二電晶體的集極，該第二電晶體的射極接地，基極連接該第一電晶體的集極並透過一第一電阻連接至一電源，該第一電晶體的射極接地，基極透過一第二電阻接收一使能控制訊號，該單相脈寬調製訊號控制器的相位引腳透過該第一電感連接至一電壓輸出引腳以提供電壓給記憶體，還依次透過一第三電阻及一第一電容接地，該單相脈寬調製訊號控制器的高通驅動引腳透過一第四電阻連接至該第一場效應電晶體的閘極，該第一場效應電晶體汲極透過該第二電感連接至該電源，該第一場效應電晶體的源極連接至該第二場效應電晶體的汲極，該第一場效應電晶體的閘極還透過一第五電阻連接至該第二場效應電晶體的汲極，該單相脈寬調製訊號控制器的低通驅動引腳連接至該第二場效應電晶體的閘極，該第二場效應電晶體的源極接地，當該使能控制訊號輸入時，該第一電晶體導通，該第二電晶體截止，該單相脈寬調製訊號控制器的高通驅動引腳及低通驅動引腳交替輸出高低電平以交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊號並透過一第二電容及一第六電阻接收該電源，再透過該第一電感及該電壓輸出引腳輸出一供電電壓給該記憶體。

2．如申請專利範圍第1項所述之記憶體供電電路，其中該單

相脈寬調製訊號控制器的使能引腳還透過一第三電容連接至其上的回饋引腳，還依次透過一第七電阻及一第四電容連接至該回饋引腳，該回饋引腳透過一第八電阻接地，還透過一第九電阻連接該電壓輸出引腳，一第五電容與一第十電阻串聯後再與該第九電阻並聯。

3．如申請專利範圍第2項所述之記憶體供電電路，其中該單相脈寬調製訊號控制器的偵測引腳透過一第十一電阻接地，還透過一第十二電阻連接該電壓輸出引腳，一第六電容連接在該電壓輸出引腳與地之間。

4．如申請專利範圍第3項所述之記憶體供電電路，其中該單相脈寬調製訊號控制器的自舉引腳依次透過該第六電阻及第二電容連接至該單相脈寬調製訊號控制器的相位引腳。

5．如申請專利範圍第4項所述之記憶體供電電路，其中該第六電阻與該電源之間還連接一二極體元件，該二極體元件的陰極連接該第六電阻的一端，該二極體元件的陽極連接至該電源。

6．如申請專利範圍第5項所述之記憶體供電電路，其中一第七及一第八電容分別連接在該第二場效應電晶體的汲極與地之間。

7．如申請專利範圍第6項所述之記憶體供電電路，其中該單相脈寬調製訊號控制器的低通驅動引腳還透過一第十三電阻連接至該單相脈寬調製訊號控制器的接地引腳並接地。

8．如申請專利範圍第7項所述之記憶體供電電路，其中該單相脈寬調製訊號控制器的電源引腳透過一第十四電阻連接該電源，還透過一第九電容接地。

9．如申請專利範圍第1項所述之記憶體供電電路，其中該記

憶體為DDR3記憶體。

10．如申請專利範圍第1項所述之記憶體供電電路，其中該電源為5V電源。

八、圖式：

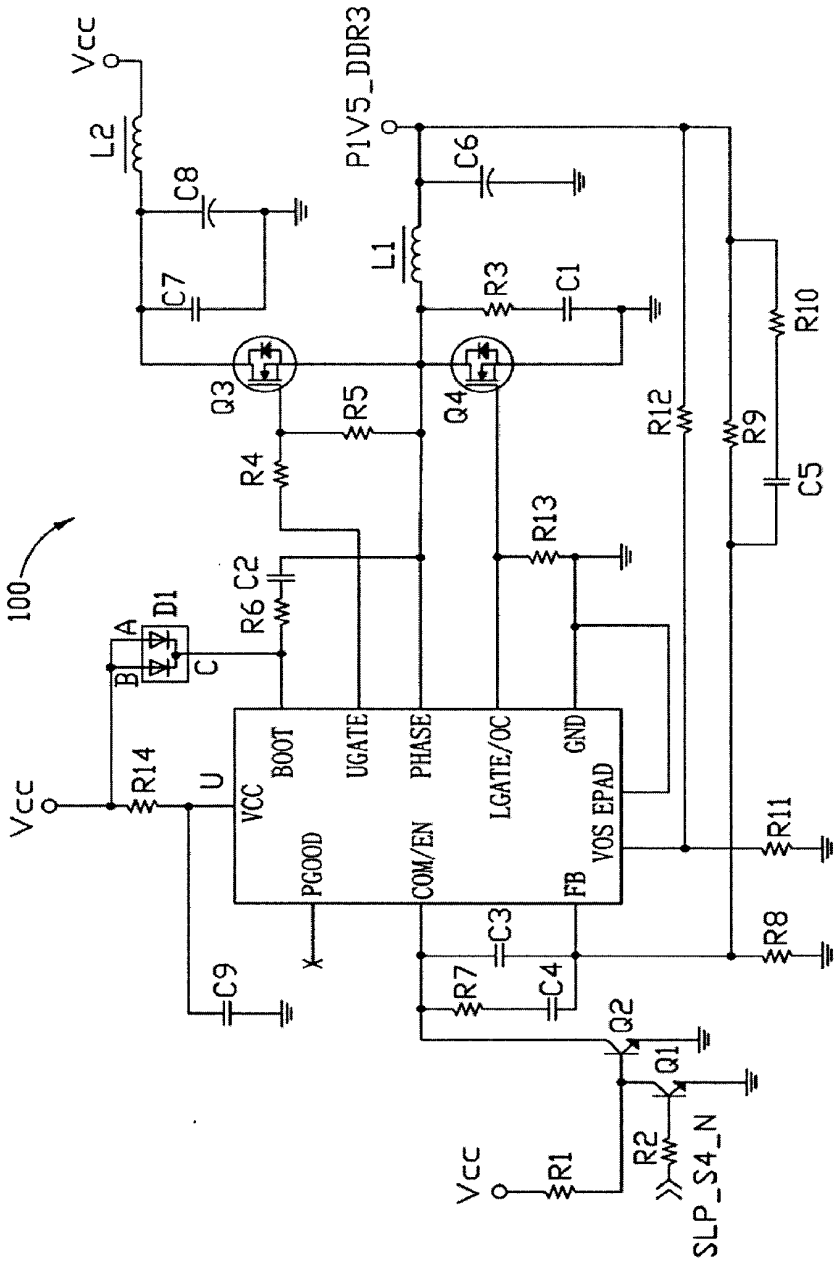

Vcc
L2
C8
C7
P1V5_DDR3
C6
L1
R3
C1
R10
Q3
R5
Q4
R12
R9
C5
R4
R13
100
C2
R6
D1
A
B
C
Vcc
R14
U
VCC
BOOT
UGATE
PHASE
LGATE/OC
GND
VOS EPAD
PGOOD
COM/EN
FB
R11
C3
R8
C9
R7
C4
Q2
Q1
Vcc
R1
R2
SLP_S4_N

圖 1

Electronic Acknowledgement Receipt

EFS ID:	34108945
Application Number:	16151347
International Application Number:	
Confirmation Number:	3080
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Winston Hsu/Sibyl Yu
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	ETRP0143USA3
Receipt Date:	25-OCT-2018
Filing Date:	04-OCT-2018
Time Stamp:	21:58:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3295004.PDF	31572 6906d63fb95fa16d0ba2d4184ae18a0ad9053b08	no	5

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2	Foreign Reference	CN_102187323.pdf	1647845 feaa0b5c79baedcb56bf8498459fae748d77d4ba	no	31
Warnings:					
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3	Foreign Reference	TW_201123198.pdf	579552 9f1476d2b918f76906fd0f243a2cee4f6ce87931	no	15
Warnings:					
Information:					
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
16/151,347

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	3 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/151,347	10/04/2018	2827	1720	ETRP0143USA3	3	1

CONFIRMATION NO. 3080

FILING RECEIPT

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City,
TAIWAN

OC000000103321217

Date Mailed: 10/25/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Yen-An Chang, Miaoli County, TAIWAN;
Wei-Ming Huang, Hsinchu County, TAIWAN;

Applicant(s)

Etron Technology, Inc., Hsinchu, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This application is a CON of 13/922,242 06/19/2013
which claims benefit of 61/672,287 07/17/2012
and claims benefit of 61/768,406 02/23/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 10/24/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/151,347**

Projected Publication Date: 01/31/2019

Non-Publication Request: No

Early Publication Request: No
Title

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Document Description: Power of Attorney

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Application Number	N/A
Filing Date	N/A
First Named Inventor	Der-Min Yuan
Title	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	ETRP0143USA3

SIGNATURE of Applicant or Patent Practitioner

Signature	/Winston Hsu/	Date (Optional)	10/03/2018
Name	Winston Hsu	Registration Number	41526
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 27765

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Etron Technology, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	DEC 22 2017
Name	Tony Wang		
Title	Associate Vice President		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

ETRO

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [✓] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Der-Min Yuan Date (Optional) : _____

Signature: Der-Min Yuan

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
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Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

As the below named inventor, I hereby declare that:

This declaration is directed to:

☑ The attached application, or

☐ United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Yen-An Chang Date (Optional) : _____

Signature: Yen-An Chang

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

As the below named inventor, I hereby declare that:

This declaration is directed to:

☑ The attached application, or

☐ United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Wei-Ming Huang Date (Optional) : _____

Signature: Wei Ming Huang.

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorized/Internet Communications Authorization Withdrawn

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS		
	Application No.	N/A
	Filing Date	N/A
	First Named Inventor	Der-Min Yuan
	Art Unit	N/A
	Examiner Name	N/A
	Practitioner Docket No.	ETRP0143USA3

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. To authorize permission for Internet Communications.

☑ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

II. To withdraw authorization for Internet Communications.

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 41526.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Winston Hsu/	10/03/2018
Signature	Date
Winston Hsu	3027291562
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0143USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Der-Min		Yuan	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	New Taipei City	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	No.2, Lane 10, Jhongsing St., Xinzhuang Dist.		
Address 2			
City	New Taipei City	State/Province	
Postal Code		Country i	TW

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yen-An		Chang	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Miaoli County	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	No.26, Bade 2nd Rd., Toufen City		
Address 2			
City	Miaoli County	State/Province	
Postal Code		Country i	TW

Inventor 3 Remove

Legal Name

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0143USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Wei-Ming		Huang	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Hsinchu County	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	6F., No.79, Sanchong 1st Rd., Zhudong Township		
Address 2			
City	Hsinchu County	**State/Province**	
Postal Code		**Country** i	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	27765		
Email Address	winstonhsu@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT		
Attorney Docket Number	ETRP0143USA3	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	1	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0143USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	13922242	2013-06-19
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13922242	Claims benefit of provisional	61672287	2012-07-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13922242	Claims benefit of provisional	61768406	2013-02-23

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0143USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0143USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0143USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

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Organization Name	Etron Technology, Inc.		
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Address 2			
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0143USA3
	Application Number	
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Signature	/Winston Hsu/			Date (YYYY-MM-DD)	2018-10-03
First Name	Winston	Last Name	Hsu	Registration Number	41526

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0143USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Filer:	Winston Hsu/Krystal Pan
Attorney Docket Number:	ETRP0143USA3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1720**

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EFS ID:	33913338
Application Number:	16151347
International Application Number:	
Confirmation Number:	3080
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Winston Hsu/Sibyl Yu
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	ETRP0143USA3
Receipt Date:	04-OCT-2018
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Time Stamp:	02:23:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1720
RAM confirmation Number	100418INTEFSW00007250503105
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	3276404.PDF	119045 bb81c4a3d3dc6e10a93457799aa8eb7b1a16e7c1	no	8
Warnings:					
Information:					
2	Claims	3276405.PDF	31257 eeccf5b4826c4a9e47eb23b05f5d85114952e289	no	1
Warnings:					
Information:					
3	Abstract	3276406.PDF	30154 4162aa6b4fa538e9153ed51be9cc48042e1a843c	no	1
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4	Drawings-only black and white line drawings	3276407.PDF	27665 281da0cfab6a415843d93a05939ff07f33c021ee	no	1
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7	Internet Communications Authorized	3276458.PDF	415134 a60a7ab7f71f07234a87521ac8145cc749ad2f2d	no	2
Warnings:					
Information:					
8	Application Data Sheet	3276470.PDF	1782460 3c0baa5190626a6f4c8ca630c5a8acf745bee59b	no	9
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	34606 cc25fd49d0227a59729b9fbfcbaf73e438e1d7e9	no	2
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Title

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Cross Reference To Related Applications

[0001] This is a continuation application of U.S. Patent Application No. 13/922,242, filed on June 19, 2013, which claims the benefit of U.S. Provisional Application No. 61/672,287, filed on July 17, 2012 and entitled "Flexible Memory Power Supply Architecture," and the benefit of U.S. Provisional Application No. 61/768,406, filed on February 23, 2013 and entitled "Mixed-Low-Voltage DRAM For Embedded Display Port." The above-mentioned applications are incorporated herein by reference.

Background of the Invention

1. Field of the Invention

[0002] The present invention relates to a dynamic random access memory, and particularly to a dynamic random access memory applied to an embedded display port.

2. Description of the Prior Art

[0003] An embedded display port (eDP) published by the Video Electronics Standards Association (VESA) is used for acting as a standard display panel interface to connect external devices. For example, the embedded display port can act as an interface between a video card and a notebook panel. In addition, the embedded display port version 1.3 published by the Video Electronics Standards Association adds a panel self refresh (PSR) function, where the panel self refresh function can make a graphic processing unit (GPU) turn off connection between the graphic processing unit and a liquid crystal panel when a frame displayed on the liquid crystal panel is frozen. Thus, power consumption of the graphic processing unit can be significantly reduced and battery endurance ability can be extended.

[0004] In addition, a timing controller supporting the panel self

refresh function of the liquid crystal display needs to include a frame buffer (e.g. a dynamic random access memory). When the graphic processing unit turns off the connection between the graphic processing unit and the liquid crystal panel, the frame buffer needs to store a last frame before the graphic processing unit turns off the connection between the graphic processing unit and the liquid crystal panel. Therefore, when no data transmission exists between the graphic processing unit and the liquid crystal panel, the timing controller can directly output the last frame stored in the frame buffer.

[0005] Although the panel self refresh function can make power consumption of the graphic processing unit be significantly reduced, power consumption of the timing controller is increased due to operation of the frame buffer. Therefore, how to design the frame buffer to reduce the power consumption of the timing controller becomes an important issue of memory manufacturers.

Summary of the Invention

[0006] An embodiment provides a dynamic random access memory applied to an embedded display port. The dynamic random access memory includes a memory core unit and a peripheral circuit unit. The memory core unit is used for operating in a first predetermined voltage. The peripheral circuit unit is electrically connected to the memory core unit for operating in a second predetermined voltage, where the second predetermined voltage is lower than 1.1V.

[0007] Another embodiment provides a dynamic random access memory applied to an embedded display port. The dynamic random access memory includes a memory core unit, a peripheral circuit unit, and an input/output unit. The memory core unit is used for operating in a first predetermined voltage. The peripheral circuit unit is electrically connected to the memory core unit for operating in a second predetermined voltage, where the second predetermined voltage is lower than 1.1V. The input/output unit is electrically connected

to the peripheral circuit unit and the memory core unit for operating in a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.

[0008] The present invention provides a dynamic random access memory applied to an embedded display port. The dynamic random access memory makes a memory core unit, a peripheral circuit unit, and an input/output unit thereof operate in lower voltages. Compared to the prior art, power consumption of the dynamic random access memory of the present invention is much lower than power consumption of a dynamic random access memory operating in operation voltages specified by the Joint Electron Device Engineering Council. Thus, when the dynamic random access memory of the present invention is applied to an embedded display port, the present invention can make system power consumption (e.g. power consumption of a graphic processing unit) be significantly reduced, not make power consumption of a timing controller be increased due to operation of a frame buffer, and extend battery endurance ability of a portable device.

[0009] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0010] The figure is a diagram illustrating a dynamic random access memory 100 applied to embedded display port according to an embodiment.

Detailed Description

[0011] Please refer to the figure. The figure is a diagram illustrating a dynamic random access memory 100 applied to an embedded display port according to an embodiment, where the dynamic random access memory 100 acts as a frame buffer of a timing controller of a liquid crystal display, and the dynamic random access memory 100 is

compatible with a single data rate (SDR) specification, a double data rate (DDR Ⅰ) specification, a double data rate two (DDR Ⅱ) specification, or a double data rate three (DDR Ⅲ) specification. As shown in the figure, the dynamic random access memory 100 includes a memory core unit 102, a peripheral circuit unit 104, and an input/output unit 106, where the peripheral circuit unit 104 is electrically connected to the memory core unit 102, and the input/output unit 106 is electrically connected to the peripheral circuit unit 104 and the memory core unit 102. Please refer to Table Ⅰ. Table Ⅰ illustrates operation voltages (specified by the Joint Electron Device Engineering Council (JEDEC)) of a dynamic random access memory operating in the DDR Ⅰ specification, a low power DDR Ⅰ specification, the DDR Ⅱ specification, and a low power DDR Ⅱ specification.

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
DDR Ⅰ	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V
Low Power DDR Ⅰ	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
DDR Ⅱ	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
Low Power DDR Ⅱ	1.7V~1.95V	1.14V~1.30V	1.14V~1.30V

Table Ⅰ

[0012] If the dynamic random access memory 100 is designed to have low power consumption to reduce power consumption of the timing controller, the dynamic random access memory 100 needs to have low operation power consumption (e.g. power consumption for the dynamic random access memory 100 outputting storage frames to the timing controller) and low standby power consumption. But, the operation voltages specified by the Joint Electron Device Engineering Council

(as shown in Table Ⅰ) can not satisfy requirements (that is, the low operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3.

[0013] Please refer to Table Ⅱ. Table Ⅱ illustrates operation voltage ranges of the dynamic random access memory 100 operating in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification according to an embodiment.

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	< 1.1V	< 1.1V	< 1.1V

Table Ⅱ

[0014] As shown in Table Ⅱ, operation voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a first predetermined voltage, where the first predetermined voltage is lower than 1.1V; operation voltages of the peripheral circuit unit 104 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a second predetermined voltage, where the second predetermined voltage is lower than 1.1V; and operation voltages of the input/output unit 106 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.

[0015] As shown in Table Ⅱ, because the operation voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR

Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the first predetermined voltage, the dynamic random access memory 100 has lower memory core power consumption; because the operation voltages of the peripheral circuit unit 104 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the second predetermined voltage, the dynamic random access memory 100 has lower access power consumption; and the operation voltages of the input/output unit 106 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the third predetermined voltage, the dynamic random access memory 100 has lower input/output power consumption. In addition, the input/output unit 106 is compatible with an interface provided by the prior art, so power consumption of the dynamic random access memory 100 is much lower than power consumption of the dynamic random access memory operating in the operation voltages specified by the Joint Electron Device Engineering Council.

[0016] Please refer to Table Ⅲ. Table Ⅲ illustrates operation voltage ranges of the dynamic random access memory 100 operating in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification according to another embodiment.

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	1.8V±0.1V	< 1.1V	< 1.1V

Table Ⅲ

[0017] As shown in Table Ⅲ, operation voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR Ⅰ specification,

the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a first predetermined voltage, where the first predetermined voltage is equal to 1.8V±0.1V; operation voltages of the peripheral circuit unit 104 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a second predetermined voltage, where the second predetermined voltage is lower than 1.1V; and operation voltages of the input/output unit 106 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.

[0018] As shown in Table Ⅲ, because the operation voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the first predetermined voltage, the dynamic random access memory 100 has higher charge pump efficiency; because the operation voltages of the peripheral circuit unit 104 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the second predetermined voltage, the dynamic random access memory 100 has lower access power consumption; and the operation voltages of the input/output unit 106 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the third predetermined voltage, the dynamic random access memory 100 has lower input/output power consumption. In addition, the input/output unit 106 is also compatible with an interface provided by the prior art, so power consumption of the dynamic random access memory 100 is much lower than power consumption of the dynamic random access memory operating in the operation voltages specified by the Joint Electron Device Engineering Council.

[0019] To sum up, the dynamic random access memory applied to an

embedded display port makes the memory core unit, the peripheral circuit unit, and the input/output unit operate in lower voltages. Compared to the prior art, power consumption of the dynamic random access memory of the present invention is much lower than power consumption of a dynamic random access memory operating in the operation voltages specified by the Joint Electron Device Engineering Council. Thus, when the dynamic random access memory of the present invention is applied to an embedded display port, the present invention can make system power consumption (e.g. power consumption of a graphic processing unit) be significantly reduced, not make power consumption of the timing controller be increased due to operation of the frame buffer, and extend battery endurance ability of a portable device.

[0020] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims

What is claimed is:

1. A dynamic random access memory applied to an interface port, comprising:

   a memory core cell, wherein the memory core cell is supplied with a first voltage within a first voltage range to make the memory core cell operate at the first voltage, and the memory core cell is a volatile memory cell; and

   a peripheral circuit electrically connected to the memory core cell, wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1V, and

   wherein the memory core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the memory core cell.

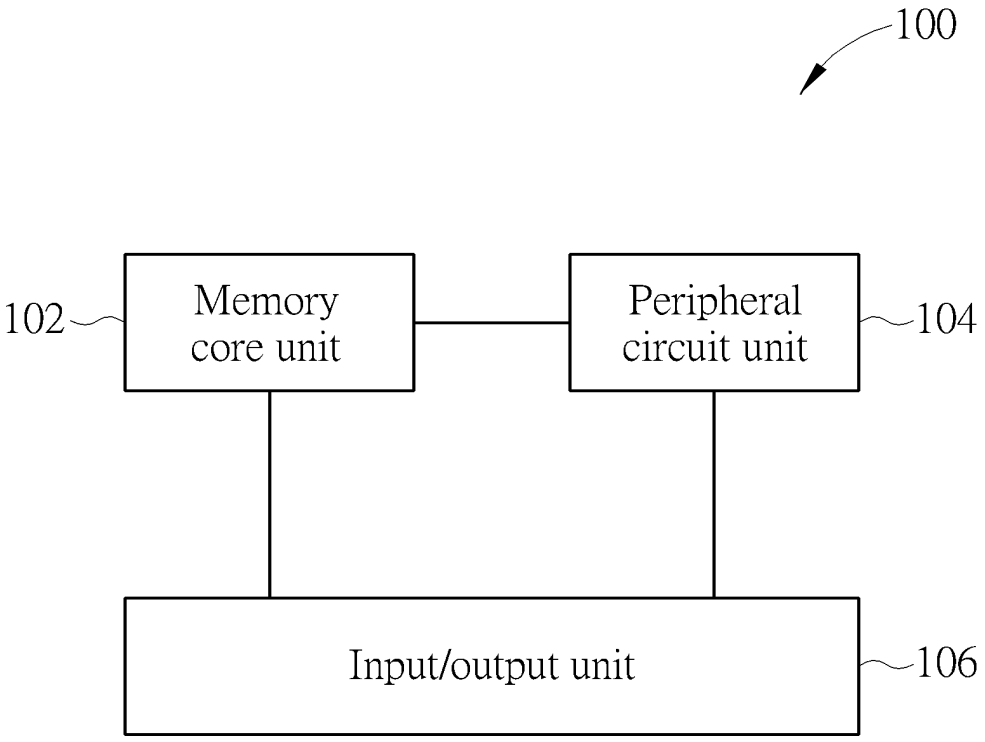
2. The dynamic random access memory of claim 1, wherein the first voltage is lower than 1.1V.

3. The dynamic random access memory of claim 2, further comprising:

   an input/output unit electrically connected to the peripheral circuit and the memory core cell for operating in a third voltage, wherein the third voltage is lower than 1.1V.

Abstract of Disclosure

A dynamic random access memory applied to an embedded display port includes a memory core unit, a peripheral circuit unit, and an input/output unit. The memory core unit is used for operating in a first predetermined voltage. The peripheral circuit unit is electrically connected to the memory core unit for operating in a second predetermined voltage, where the second predetermined voltage is lower than 1.1V. The input/output unit is electrically connected to the memory core unit and the peripheral circuit unit for operating in a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.


100
102
Memory core unit
Peripheral circuit unit
104
Input/output unit
106

Figure