DDR3 SDRAM

MT41J256M4 – 32 Meg x 4 x 8 Banks
MT41J128M8 – 16 Meg x 8 x 8 Banks
MT41J64M16 – 8 Meg x 16 x 8 Banks

Features

- V_{DD} = $V_{DD}Q$ = +1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- CAS (READ) latency (CL): 5, 6, 7, 8, 9, 10, or 11
- POSTED CAS ADDITIVE latency (AL): 0, CL - 1, CL - 2
- CAS (WRITE) latency (CWL): 5, 6, 7, 8, based on ^{t}CK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8,192 cycle refresh at 0°C to 85°C
  - 32ms at 85°C to 95°C
- Clock frequency range of 300–800 MHz
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

Options	Marking
• Configuration	
– 256 Meg x 4	256M4
– 128 Meg x 8	128M8
– 64 Meg x 16	64M16
• FBGA package (Pb-free) - x4, x8	
– 78-ball FBGA (8mm x 11.5mm) Rev. F	JP
– 78-ball FBGA (9mm x 11.5mm) Rev. D	HX
– 86-ball FBGA (9mm x 15.5mm) Rev. B	BY
• FBGA package (Pb-free) - x16	
– 96-ball FBGA (9mm x 15.5mm) Rev. B	LA
• Timing - cycle time	
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.25ns @ CL = 10 (DDR3-1600)	-125E
– 1.25ns @ CL = 9 (DDR3-1600)	-125F
– 1.5ns @ CL = 10 (DDR3-1333)	-15
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.5ns @ CL = 8 (DDR3-1333)	-15F
– 1.87ns @ CL = 8 (DDR3-1066)	-187
– 1.87ns @ CL = 7 (DDR3-1066)	-187E
– 2.5ns @ CL = 6 (DDR3-800)	-25
– 2.5ns @ CL = 5 (DDR3-800)	-25E
• Revision	:B/:D/:F

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-125	1600	11-11-11	13.75	13.75	13.75
-125E	1600	10-10-10	12.5	12.5	12.5
-125F	1600	9-9-9	11.25	11.25	11.25
-15	1333	10-10-10	15	15	15
-15E	1333	9-9-9	13.5	13.5	13.5
-15F	1333	8-8-8	12	12	12
-187	1066	8-8-8	15	15	15
-187E	1066	7-7-7	13.1	13.1	13.1
-25	800	6-6-6	15	15	15
-25E	800	5-5-5	12.5	12.5	12.5

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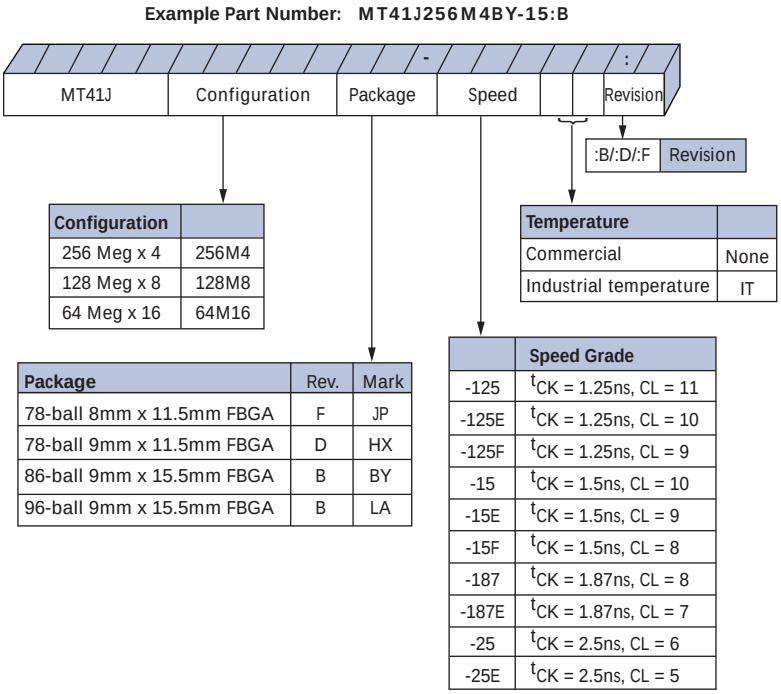
APPLE-1022

Table 2: Addressing

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	16K (A[13:0])	16K (A[13:0])	8K (A[12:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])

Figure 1: 1Gb DDR3 Part Numbers



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: www.micron.com.

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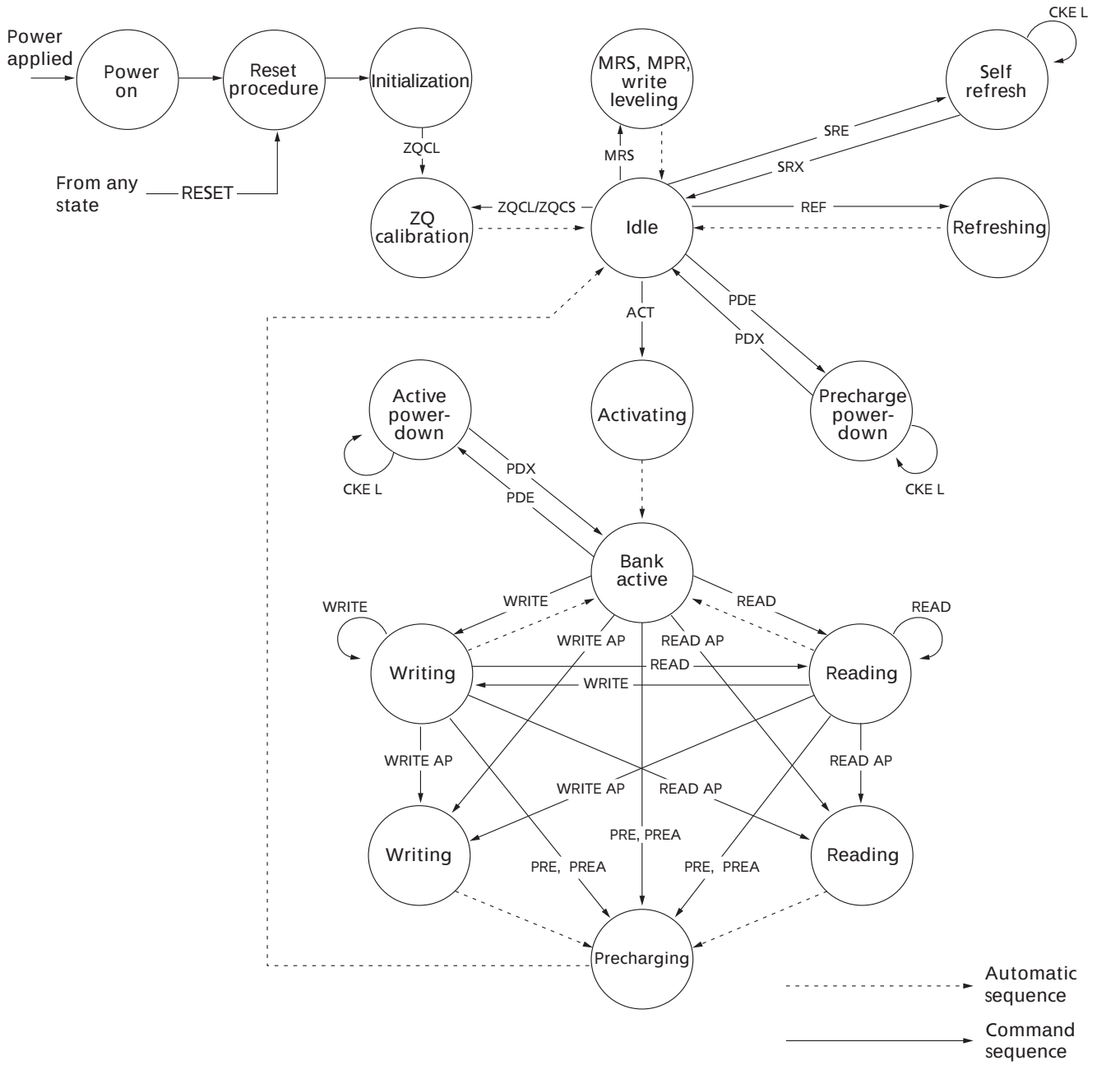
State Diagram

Figure 2: Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

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Functional Description

The DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

DDR3 SDRAM use READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms “DQS” and “CK” found throughout the data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported and can result in unknown operation.
- Row addressing is denoted as A[*n*:0](1Gb: *n* = 12 [x16]; 1Gb: *n* = 13 [x4, x8]).

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Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

Figure 3: 256 Meg x 4 Functional Block Diagram

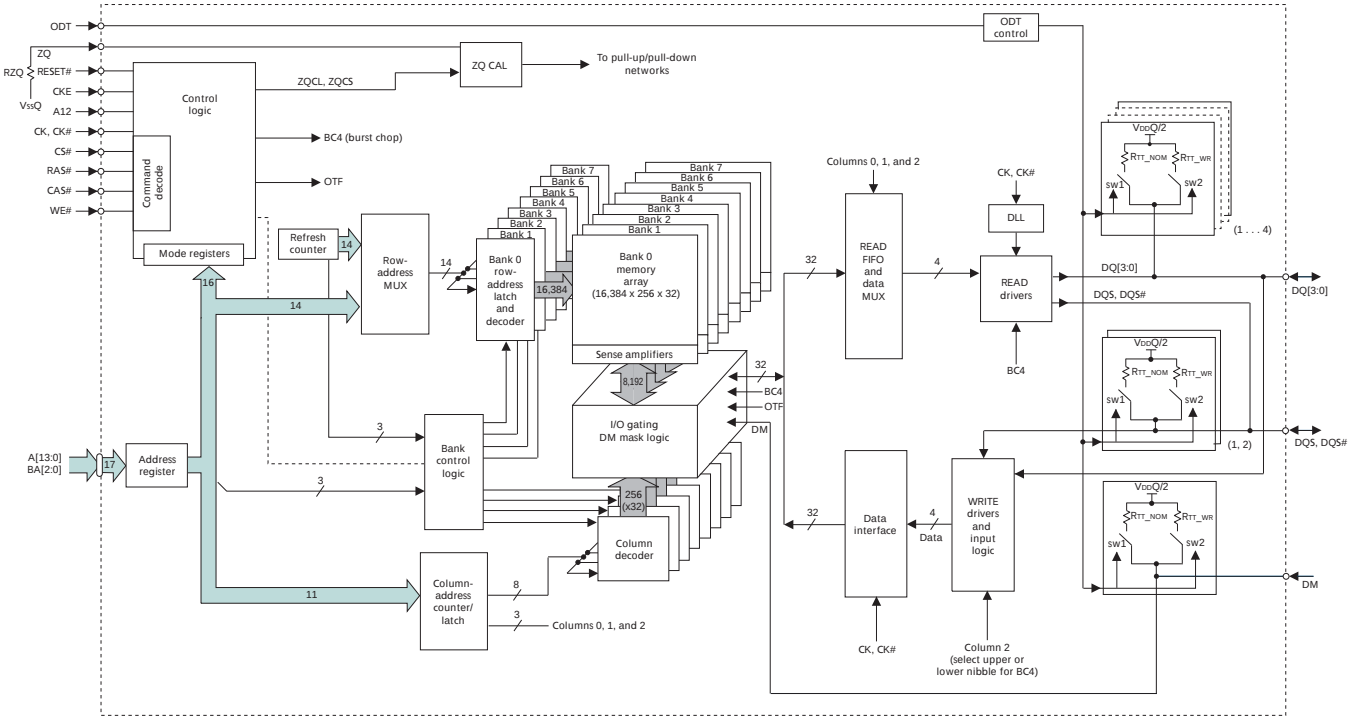

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Figure 4: 128 Meg x 8 Functional Block Diagram

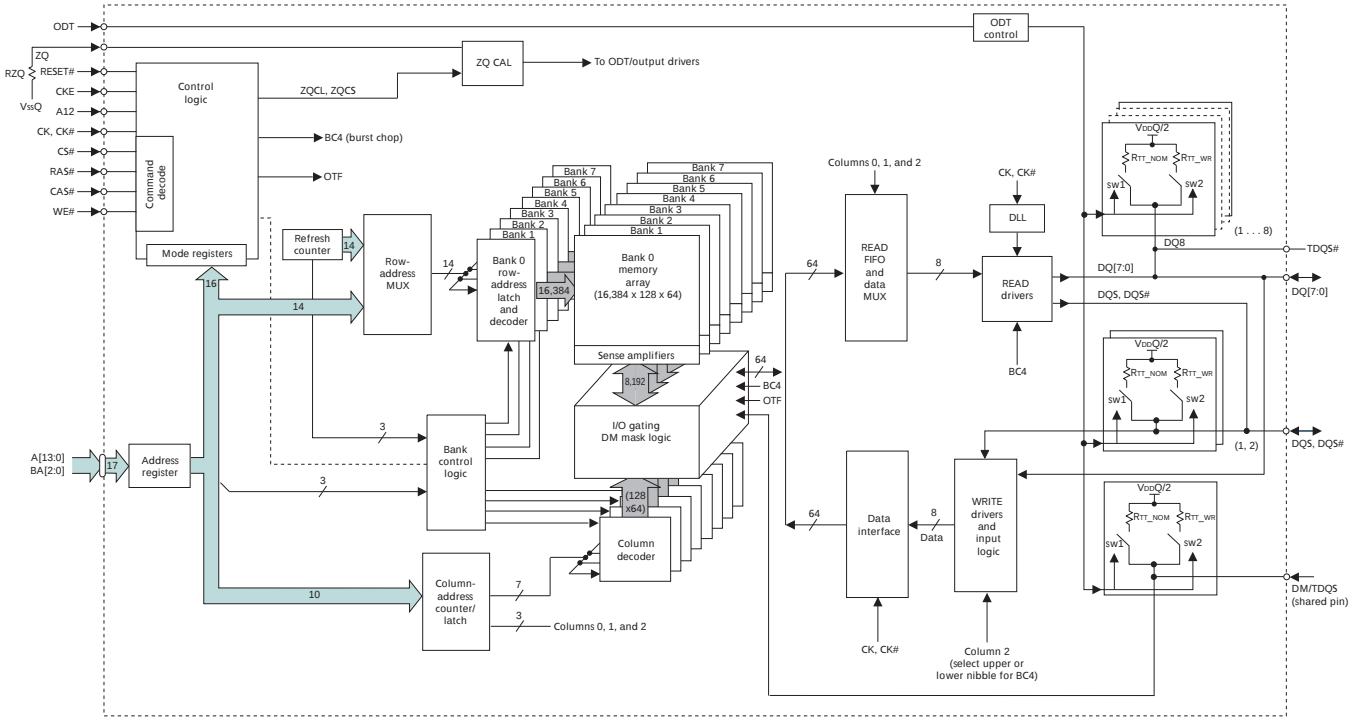
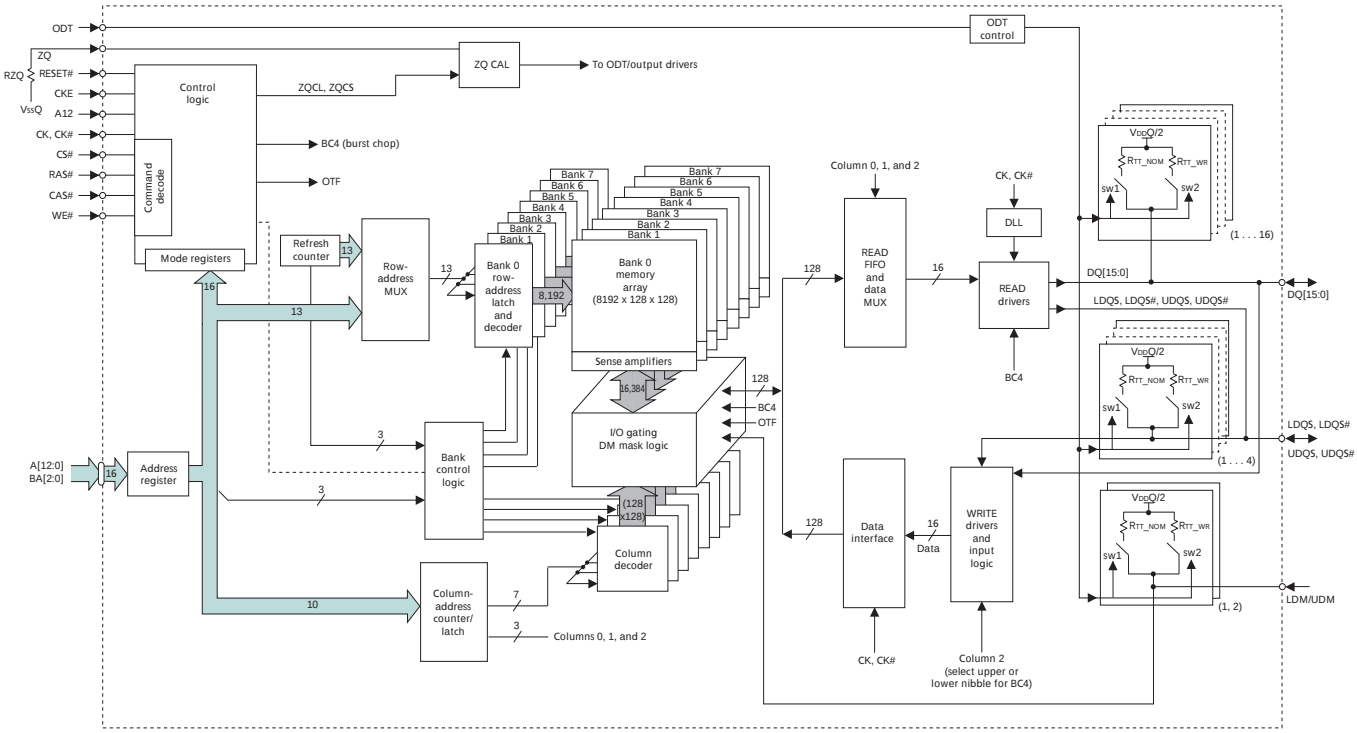


Figure 5: 64 Meg x 16 Functional Block Diagram



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Ball Assignments and Descriptions

Figure 6: 78-Ball FBGA – x4, x8 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	VSS	VDD	NC				NF, NF/TDQS#	VSS	VDD
B	VSS	VSSQ	DQ0				DM, DM/TDQS	VSSQ	VDDQ
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ
D	VSSQ	NF, DQ6	DQS#				VDD	VSS	VSSQ
E	VREFDQ	VDDQ	NF, DQ4				NF, DQ7	NF, DQ5	VDDQ
F	NC	VSS	RAS#				CK	VSS	NC
G	ODT	VDD	CAS#				CK#	VDD	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	VSS	BA0	BA2				NC	VREFCA	VSS
K	VDD	A3	A0				A12/BC#	BA1	VDD
L	VSS	A5	A2				A1	A4	VSS
M	VDD	A7	A9				A11	A6	VDD
N	VSS	RESET#	A13				NC	A8	VSS

Notes:
1. Ball descriptions listed in Table 3 on page 17 are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function.
3. Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3 on page 17).

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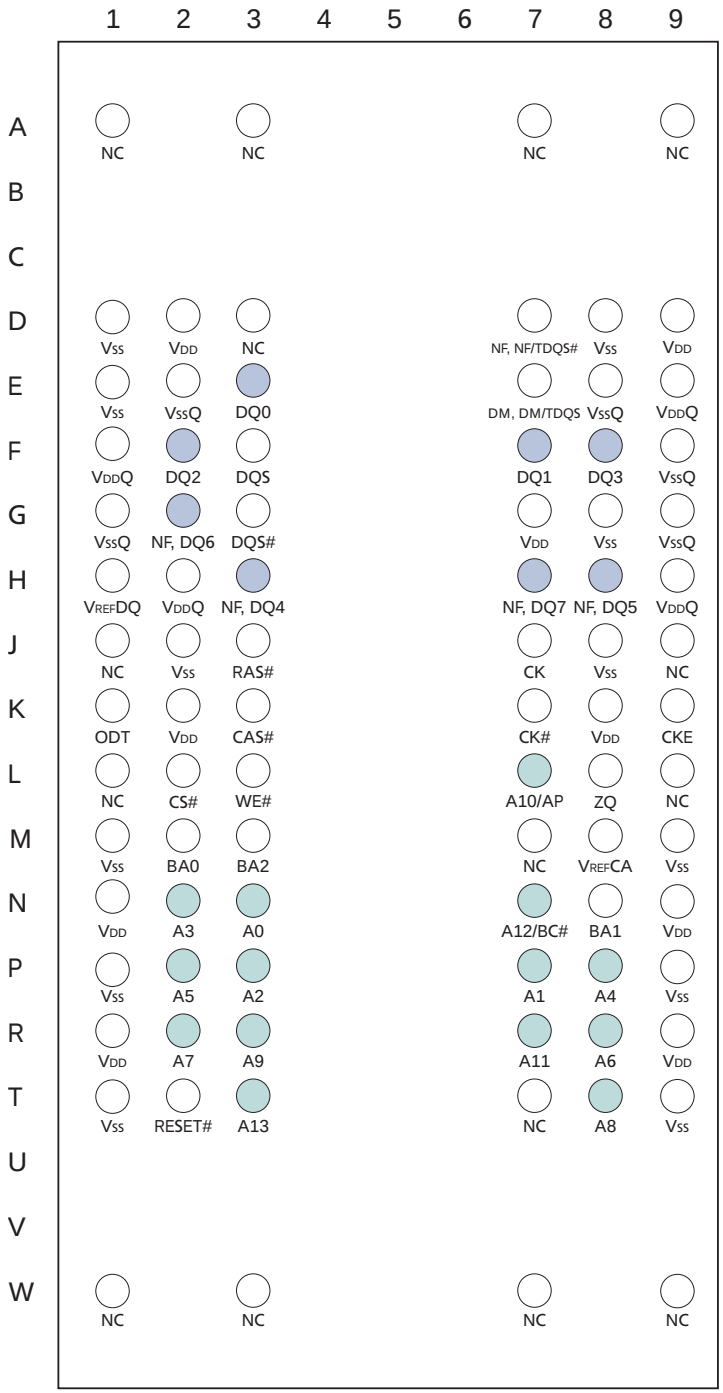
Figure 7: 86-Ball FBGA – x4, x8 Ball Assignments (Top View)



Notes:
1. Ball descriptions listed in Table 4 on page 19 are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function.
3. Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 4 on page 19).

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Figure 8: 96-Ball FBGA – x16 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	VDDQ	DQ13	DQ15				DQ12	VDDQ	VSS
B	VSSQ	VDD	VSS				UDQS#	DQ14	VSSQ
C	VDDQ	DQ11	DQ9				UDQS	DQ10	VDDQ
D	VSSQ	VDDQ	UDM				DQ8	VSSQ	VDD
E	VSS	VSSQ	DQ0				LDM	VSSQ	VDDQ
F	VDDQ	DQ2	LDQS				DQ1	DQ3	VSSQ
G	VSSQ	DQ6	LDQS#				VDD	VSS	VSSQ
H	VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ
J	NC	VSS	RAS#				CK	VSS	NC
K	ODT	VDD	CAS#				CK#	VDD	CKE
L	NC	CS#	WE#				A10/AP	ZQ	NC
M	VSS	BA0	BA2				NC	VREFCA	VSS
N	VDD	A3	A0				A12/BC#	BA1	VDD
P	VSS	A5	A2				A1	A4	VSS
R	VDD	A7	A9				A11	A6	VDD
T	VSS	RESET#	NC				NC	A8	VSS

Notes:
1. Ball descriptions listed in Table 5 on page 21 are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function.
3. Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 5 on page 21).

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Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Ball Assignments	Symbol	Type	Description
K3, L7, L3, K2, L8, L2, M8, M2, N8, M3, H7, M7, K7, N3	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC#, A13	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Table 62 on page 91.
J2, K8, J3	BA0, BA1, BA2	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
F7, G7	CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
G9	CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
H2	CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
B7	DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to VREFDQ. DM has an optional use as TDQS on the x8.
G1	ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
F3, G3, H3	RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.

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Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (continued)

Ball Assignments	Symbol	Type	Description
N2	RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DDQ} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.
B3, C7, C2, C8	DQ0, DQ1, DQ2, DQ3	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to V_{REF}DQ.
B3, C7, C2, C8, E3, E8, D2, E7	DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REF}DQ.
C3, D3	DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
B7, A7	TDQS, TDQS#	Output	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
A2, A9, D7, G2, G8, K1, K9, M1, M9	V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
B9, C1, E2, E9	V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
J8	V_{REF}CA	Supply	**Reference voltage for control, command, and address:** V_{REF}CA must be maintained at all times (including self refresh) for proper device operation.
E1	V_{REF}DQ	Supply	**Reference voltage for data:** V_{REF}DQ must be maintained at all times (including self refresh) for proper device operation.
A1, A8, B1, D8, F2, F8, J1, J9, L1, L9, N1, N9	V_{SS}	Supply	Ground.
B2, B8, C9, D1, D9	V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
H8	ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
A3, J7, N7, F9, H1, F1, H9	NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
A7, D2, E3, E7, E8	NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

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Table 4: 86-Ball FBGA – x4, x8 Ball Descriptions

Ball Assignments	Symbol	Type	Description
N3, P7, P3, N2, P8, P2, R8, R2, T8, R3, L7, R7, N7, T3	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9 A10/AP, A11, A12/BC#, A13	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Table 62 on page 91.
M2, N8, M3	BA0, BA1, BA2	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
J7, K7	CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
K9	CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
L2	CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
E7	DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to VREFDQ. DM has an optional use as TDQS on the x8.
K1	ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
J3, K3, L3	RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.

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Table 4: 86-Ball FBGA – x4, x8 Ball Descriptions (continued)

Ball Assignments	Symbol	Type	Description
T2	RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × $V_{DD}Q$ and DC LOW ≤ 0.2 × $V_{DD}Q$. RESET# assertion and desertion are asynchronous.
E3, F7, F2, F8	DQ0, DQ1, DQ2, DQ3	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to $V_{REF}DQ$.
E3, F7, F2, F8, H3, H8, G2, H7	DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to $V_{REF}DQ$.
F3, G3	DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
E7, D7	TDQS, TDQS#	Output	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
D2, D9, G7, K2, K8, N1, N9, R1, R9	V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
E9, F1, H2, H9	$V_{DD}Q$	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
M8	$V_{REF}CA$	Supply	**Reference voltage for control, command, and address:** $V_{REF}CA$ must be maintained at all times (including self refresh) for proper device operation.
H1	$V_{REF}DQ$	Supply	**Reference voltage for data:** $V_{REF}DQ$ must be maintained at all times (including self refresh) for proper device operation.
D1, D8, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	V_{SS}	Supply	Ground.
E2, E8, F9, G1, G9	$V_{SS}Q$	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
L8	ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to $V_{SS}Q$.
A1, A3, A7, A9, D3, J1, J9, L1, L9, M7, T7, W1, W3, W7, W9	NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
D7, G2, H3, H7, H8	NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

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Table 5: 96-Ball FBGA – x16 Ball Descriptions

Ball Assignments	Symbol	Type	Description
N3, P7, P3, N2, P8, P2, R8, R2, T8, R3, L7, R7, N7	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9 A10/AP, A11, A12/BC#	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Table 62 on page 91.
M2, N8, M3	BA0, BA1, BA2	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
J7, K7	CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
K9	CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
L2	CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
E7	LDM	Input	**Input data mask:** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to VREFDQ.
K1	ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
J3, K3, L3	RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.

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Table 5: 96-Ball FBGA – x16 Ball Descriptions (continued)

Ball Assignments	Symbol	Type	Description
T2	RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × $V_{DD}Q$ and DC LOW ≤ 0.2 × $V_{DD}Q$. RESET# assertion and desertion are asynchronous.
D3	UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to $V_{REF}DQ$.
E3, F7, F2, F8, H3, H8, G2, H7	DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to $V_{REF}DQ$.
D7, C3, C8, C2, A7, A2, B8, A3	DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, DQ15	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to $V_{REF}DQ$.
F3, G3	LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
C7, B7	UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
B2, D9, G7, K2, K8, N1, N9, R1, R9	V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
A1, A8, C1, C9, D2, E9, F1, H2, H9	$V_{DD}Q$	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
M8	$V_{REF}CA$	Supply	**Reference voltage for control, command, and address:** $V_{REF}CA$ must be maintained at all times (including self refresh) for proper device operation.
H1	$V_{REF}DQ$	Supply	**Reference voltage for data:** $V_{REF}DQ$ must be maintained at all times (including self refresh) for proper device operation.
A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	V_{SS}	Supply	Ground.
B1, B9, D1, D8, E2, E8, F9, G1, G9	$V_{SS}Q$	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
L8	ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to $V_{SS}Q$.
J1, J9, L1, L9, M7, T3, T7	NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

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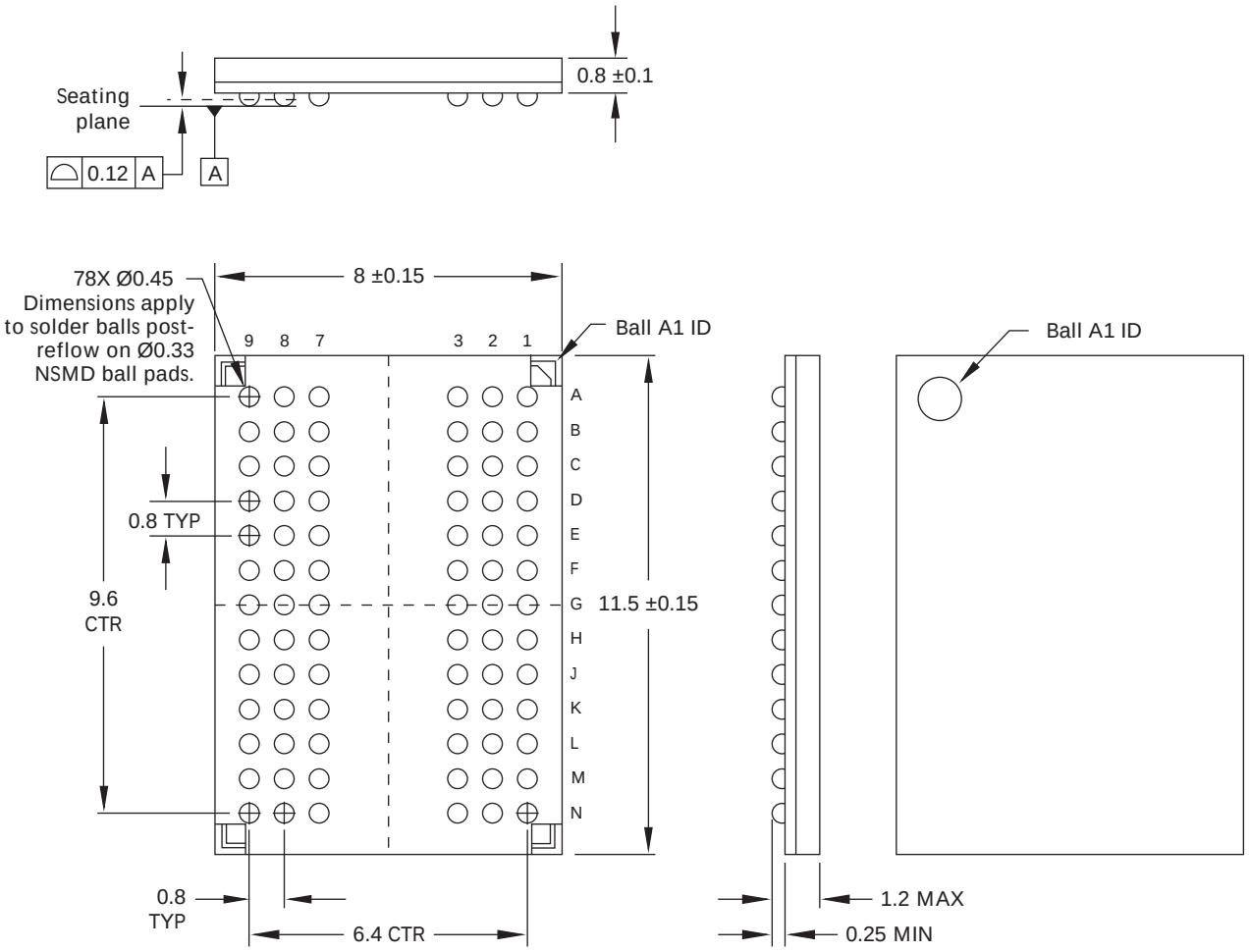
Package Dimensions

Figure 9: 78-Ball FBGA – x4, x8; "JP"



Notes: 1. All dimensions are in millimeters.

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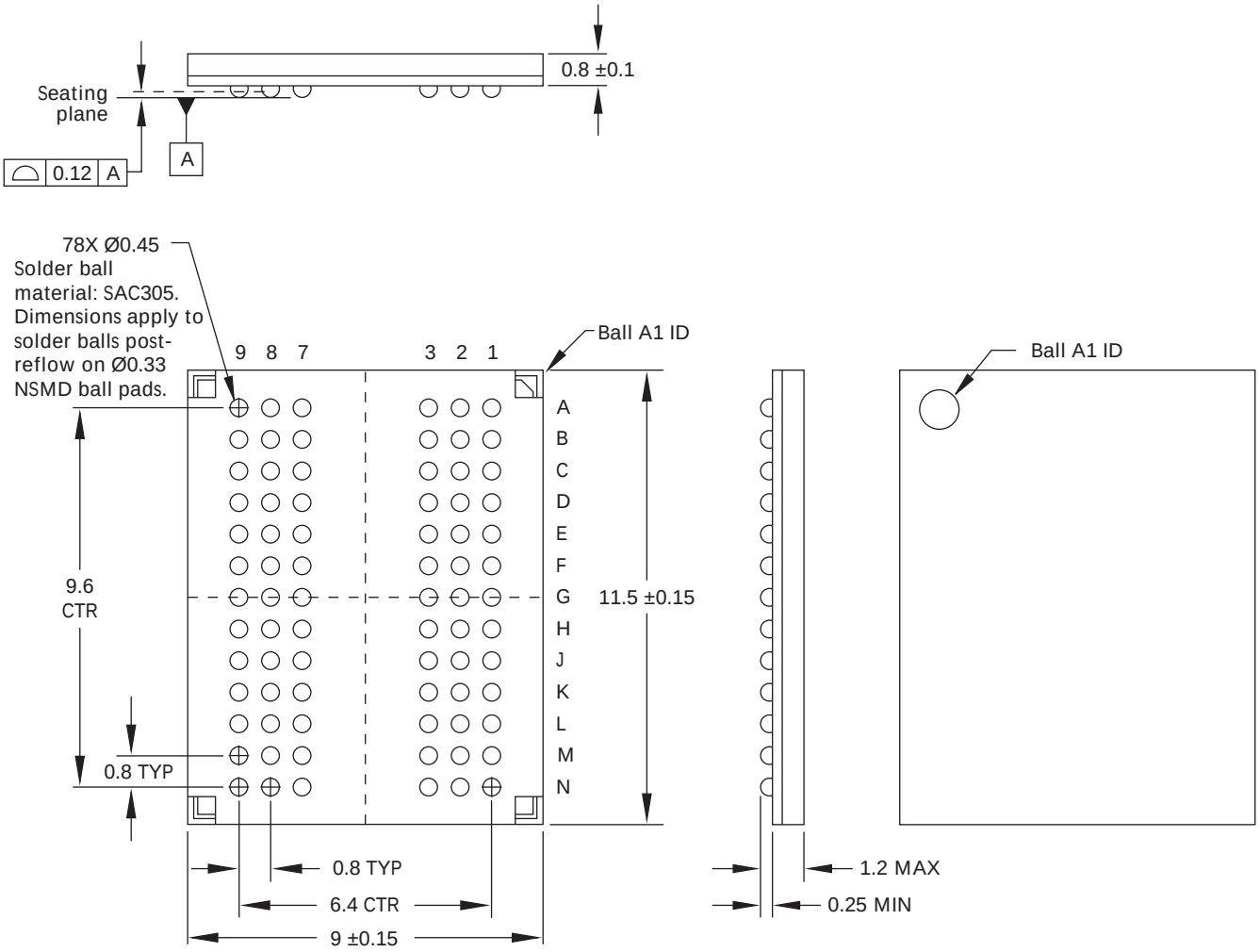
Figure 10: 78-Ball FBGA – x4, x8; "HX"



Notes: 1. All dimensions are in millimeters.

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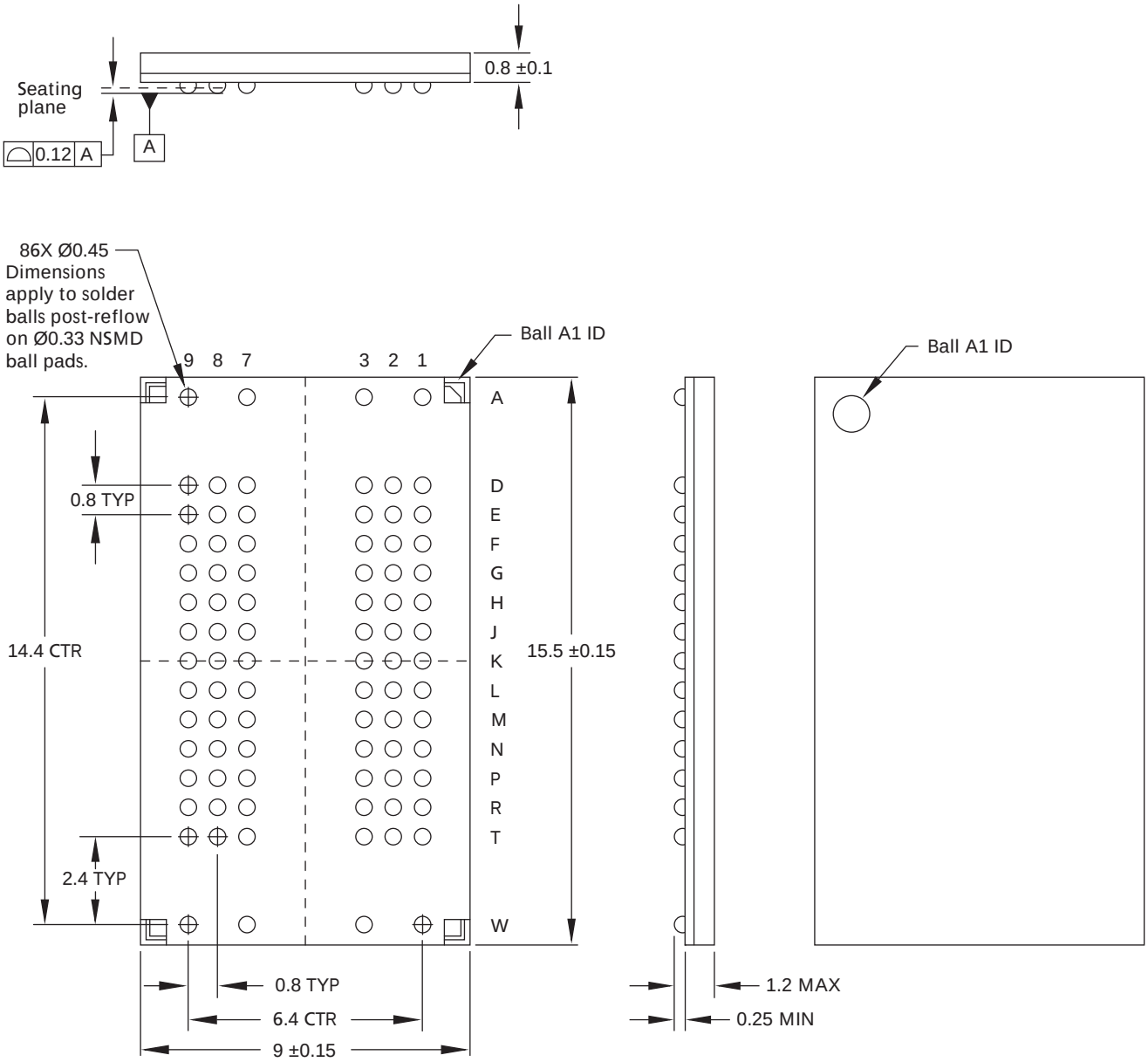
Figure 11: 86-Ball FBGA – x4, x8



Notes: 1. All dimensions are in millimeters.

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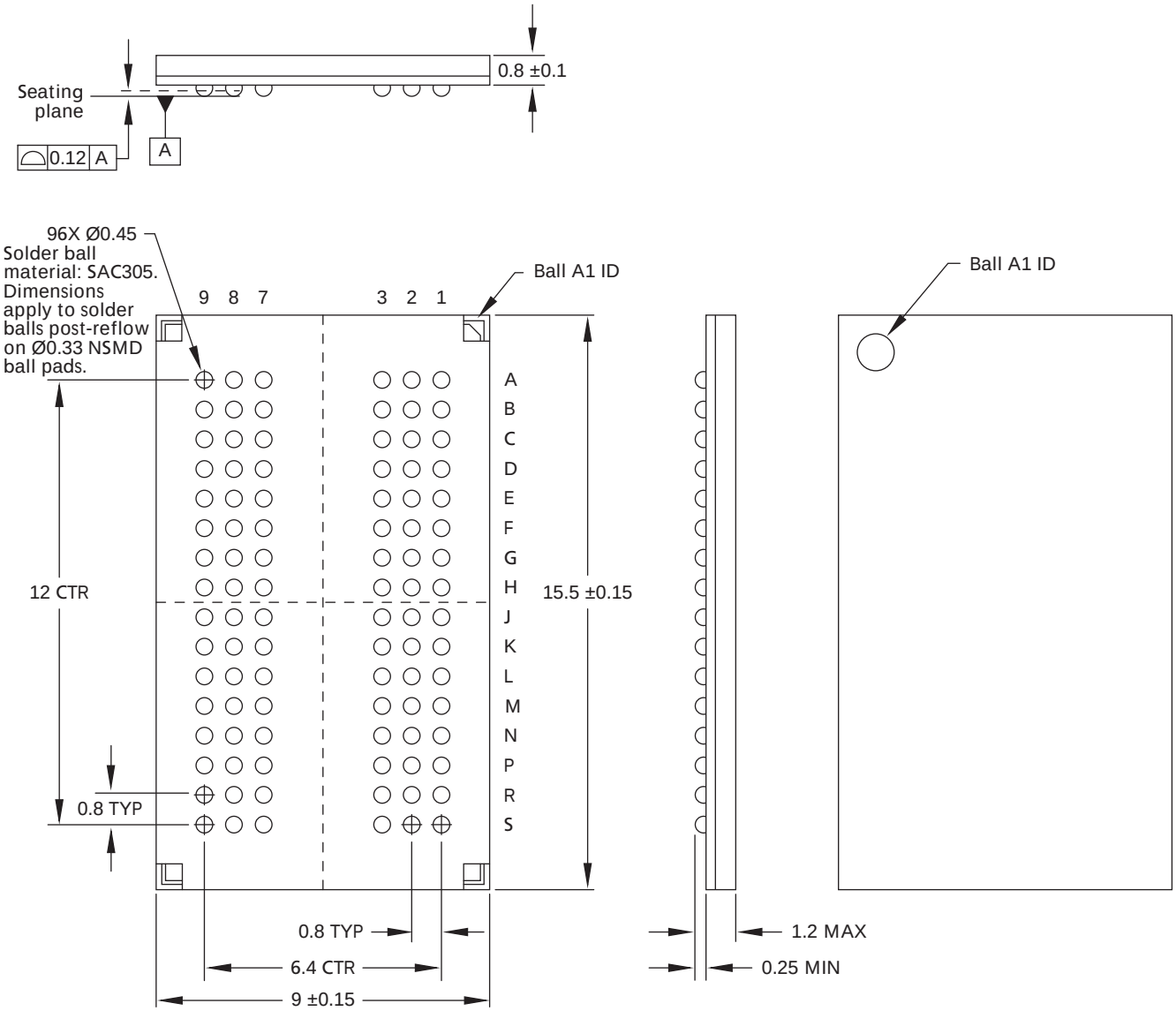
Figure 12: 96-Ball FBGA – x16



Notes: 1. All dimensions are in millimeters.

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Electrical Specifications

Absolute Ratings

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}	–0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V	
T_C	Operating case temperature	0	95	°C	2, 3
T_{STG}	Storage temperature	–55	150	°C	

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500mV, V_{REF} may be ≤300mV.
2. MAX operating case temperature. T_C is measured in the center of the package (see Figure 13 on page 28).
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

Input/Output Capacitance

Table 7: Input/Output Capacitance
Note 1 applies to the entire table

Capacitance Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CK and CK#	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	pF	
Single-end I/O: DQ, DM	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	pF	2
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	pF	3
ΔC: DQS to DQS#, TDQS, TDQS#	C_{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	pF	3
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	4
Inputs (CTRL, CMD, ADDR)	C_I	0.75	1.5	0.75	1.5	0.75	1.3	0.75	1.3	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	–0.5	0.3	–0.5	0.3	–0.4	0.2	–0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	$C_{DI_CMD_ADDR}$	–0.5	0.5	–0.5	0.5	–0.4	0.4	–0.4	0.4	pF	7

Notes:
1. V_{DD} = +1.5V ±0.075mV, V_{DDQ} = V_{DD}, V_{REF} = V_{SS}, *f* = 100 MHz, T_C = 25°C. $V_{OUT(DC)}$ = 0.5 × V_{DDQ}, V_{OUT} (peak-to-peak) = 0.1V.
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes TDQS, TDQS#. C_{DDQS} is for DQS vs. DQS# and TDQS vs. TDQS# separately.
4. C_{DIO} = C_{IO} (DQ) - 0.5 × (C_{IO} [DQS] + C_{IO} [DQS#]).
5. Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR = A[*n*:0], BA[2:0].
6. C_{DI_CTRL} = C_I (CTRL) - 0.5 × (C_{CK} [CK] + C_{CK} [CK#]).
7. $C_{DI_CMD_ADDR}$ = C_I (CMD_ADDR) - 0.5 × (C_{CK} [CK] + C_{CK} [CK#]).

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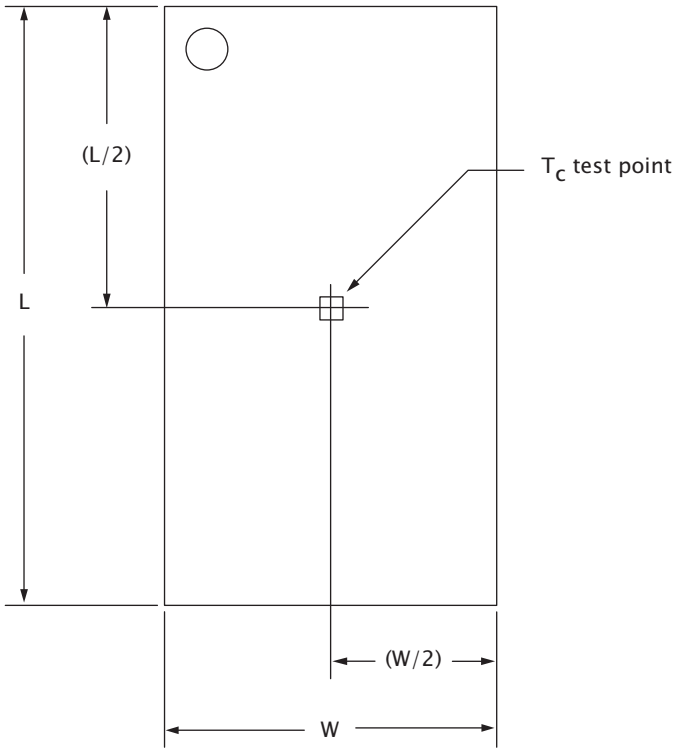
Thermal Characteristics

Table 8: Thermal Characteristics

Parameter/Condition		Symbol	Value	Units	Notes
Operating case temperature		T_C	0 to 85	°C	1, 2, 3
		T_C	0 to 95	°C	1, 2, 3, 4
Junction-to-case (TOP)	78-ball	ΘJC	3.2	°C/W	5
	86-ball		2.8		
	96-ball		2.8		

Notes:
1. MAX operating case temperature. T_C is measured in the center of the package (see Figure 13).
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate. The use of SRT or ASR (if available) must be enabled.
5. The thermal resistance data is based off of a number of samples from multiple lots and should be viewed as a typical number.

Figure 13: Thermal Measurement Point



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Electrical Specifications – IDD Specifications and Conditions

The following definitions are used within the IDD measurement tables:

- LOW: $V_{IN} \leq V_{IL(AC)}$ MAX; HIGH: $V_{IN} \geq V_{IH(AC)}$ MIN
- Stable: Inputs are stable at a HIGH or LOW level
- Floating: Inputs are $V_{REF} = V_{DDQ}/2$
- Switching: See Tables 10 and 11

Table 9: IDD Measurement Conditions Reference

Table Number	Measurement Conditions
Table 13 on page 31	IDD0 and IDD1
Table 14 on page 33	IDD2Ps, IDD2Pf, IDD2Q, IDD2N, IDD3P, and IDD3N
Table 15 on page 35	IDD4R, IDD4W
Table 16 on page 37	IDD5B, IDD6, IDD6ET
Table 17 on page 38	IDD7 (see Table 18 on page 38)

Table 10: Definition of Switching for Command and Address Input Signals

Switching for Address (Row/Column) and Command Signals (CS#, RAS#, CAS#, and/or WE#)	
Address (row/column)	If not otherwise stated, inputs are stable at HIGH or LOW during 4 clocks and then change to the opposite value (Ax Ax Ax Ax $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ Ax Ax Ax Ax . . .)
Bank address	If not otherwise stated, the bank addresses should be switched in a similar fashion as the row/column addresses
Command (CS#, RAS#, CAS#, WE#)	Define command background pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ . . . where: D = (CS#, RAS#, CAS#, WE#) = (HIGH, LOW, LOW, LOW) $\overline{D}$ = (CS#, RAS#, CAS#, WE#) = (HIGH, HIGH, HIGH, HIGH) If other commands are necessary (ACTIVATE for IDD0 or READ for IDD4R), the background pattern command is substituted by the respective CS#, RAS#, CAS#, and WE# levels of the necessary command

Table 11: Definition of Switching for Data Pins

Switching for Data Pins (DQ, DQS, DM)	
Data strobe (DQS)	Data strobe is changing between HIGH and LOW after every clock cycle
Data (DQ)	Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock
Data masking (DM)	No switching; DM must always be driven LOW

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Table 12: Timing Parameters

IDD Parameter		DDR3-800		DDR3-1066		DDR3-1333			DDR3-1600			Units
		-25E	-25	-187E	-187	-15F	-15E	-15	-125F	-125E	-125	
		5-5-5	6-6-6	7-7-7	8-8-8	8-8-8	9-9-9	10-10-10	9-9-9	10-10-10	11-11-11	
^{t}CK (MIN) IDD		2.5		1.875		1.5			1.25			ns
CL IDD		5	6	7	8	8	9	10	9	10	11	CK
^{t}RCD (MIN) IDD		12.5	15	13.13	15	12	13.5	15	11.25	12.5	13.75	ns
^{t}RC (MIN) IDD		50	52.5	50.63	52.50	48	49.5	51	46.25	47.5	48.75	ns
^{t}RAS (MIN) IDD		37.5	37.5	37.5	37.5	36	36	36	35	35	35	ns
^{t}RP (MIN)		12.5	15	13.13	15	12	13.5	15	11.25	12.5	13.75	ns
^{t}FAW	x4, x8	40	40	37.5	37.5	30	30	30	30	30	30	ns
	x16	50	50	50	50	45	45	45	40	40	40	ns
^{t}RRD IDD	x4, x8	10	10	7.5	7.5	6	6	6	6	6	6	ns
	x16	10	10	10	10	7.5	7.5	7.5	7.5	7.5	7.5	ns
^{t}RFC		110	110	110	110	110	110	110	110	110	110	ns

Notes:
1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC parametric test conditions.
3. IDD parameters are specified with ODT and the output buffer is disabled (MR1[12]).
4. Optional ASR is disabled unless stated otherwise.

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Table 13: IDD Measurement Conditions for IDD0 and IDD1

IDD Test	IDD0: Operating Current 0 One Bank ACTIVATE to PRECHARGE	IDD1: Operating Current 1 One Bank ACTIVATE to READ to PRECHARGE	Notes
Timing example	–	Figure 14 on page 32	
CKE	HIGH	HIGH	
External clock	On	On	
^{t}CK	^{t}CK (MIN) IDD	^{t}CK (MIN) IDD	
^{t}RC	^{t}RC (MIN) IDD	^{t}RC (MIN) IDD	
^{t}RAS	^{t}RAS (MIN) IDD	^{t}RAS (MIN) IDD	
^{t}RCD	n/a	^{t}RCD (MIN) IDD	
^{t}RRD	n/a	n/a	
^{t}RC	n/a	n/a	
CL	n/a	CL IDD	
AL	n/a	0	
CS#	HIGH between ACTIVATE and PRECHARGE	HIGH between ACTIVATE, READ, and PRECHARGE	
Command inputs	Switching—the only exceptions are ACTIVATE and PRECHARGE commands; Example of -25E IDD0 pattern: A0D$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$P0	Switching—the only exceptions are ACTIVATE and PRECHARGE commands; Example of -25E IDD1 pattern: A0D$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$R0$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$$\overline{\text{D}}$P0	1
Row/column addresses	Row addresses switching; Address input A10 must be LOW at all times	Row addresses switching; Address input A10 must be LOW at all times	1
Bank addresses	Bank address is fixed (bank *0*)	Bank address is fixed (bank *0*)	
Data I/O	Switching	Read data: Output data switches after every clock cycle, which means that read data is stable during falling DQS; I/O should be floating when no read data	2
Output buffer DQ, DQS	Off	Off	
ODT	Disabled	Disabled	
Burst length	n/a	8 fixed (via MR0)	
Active banks	Bank *0*; ACTIVATE-to-PRECHARGE loop	Bank *0*; ACTIVATE-to-READ-to-PRECHARGE loop	
Idle banks	All other	All other	
Special notes	n/a	n/a	

Notes: 1. For further definition of input switching, see Table 10 on page 29.
2. For further definition of data switching, see Table 11 on page 29.

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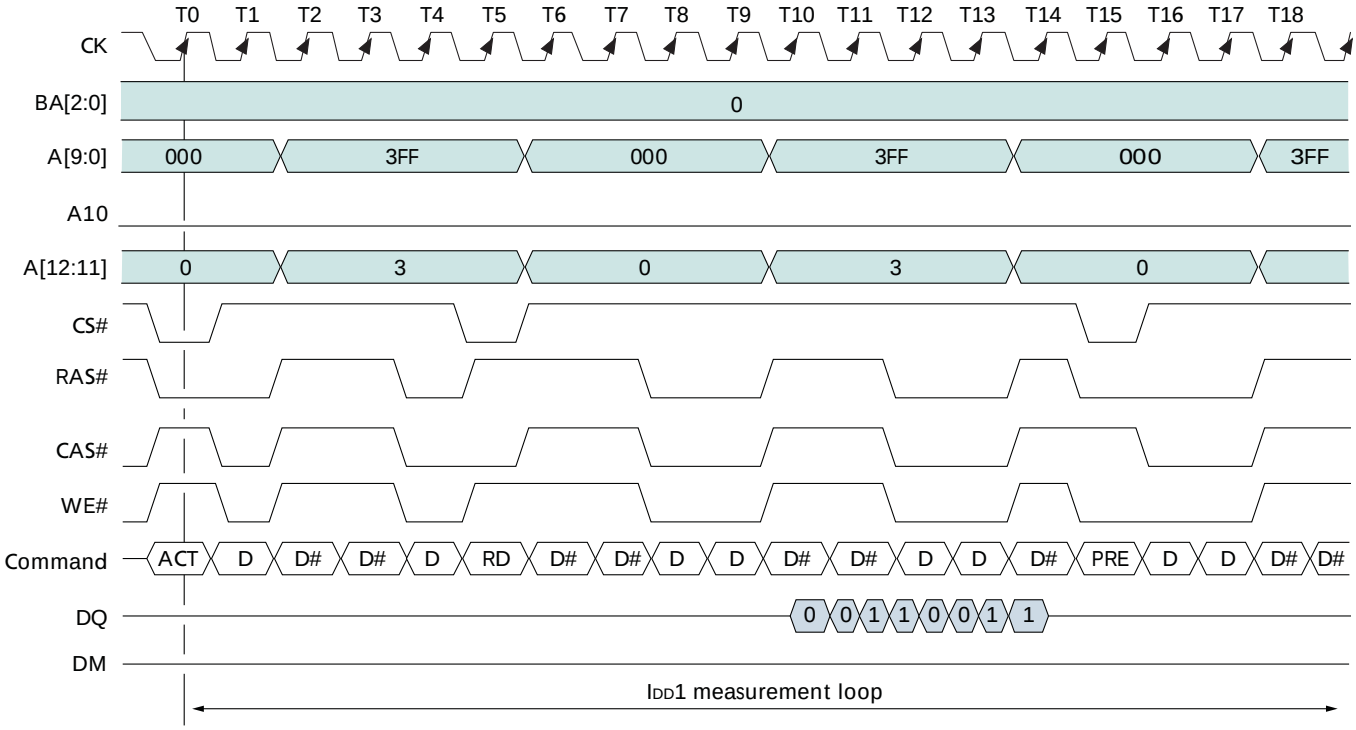
Figure 14: IDD1 Example – DDR3-800, 5-5-5, x8 (-25E)



Notes: 1. Data DQ is shown, but the output buffer should be switched off (per MR1[12] = 1) to achieve IOUT = 0mA (MR1[12] = 0 is reflected in this example; however, test conditions are MR1[12] = 1). Address inputs are split into three parts.

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Table 14: IDD Measurement Conditions for Power-Down Currents

Name	IDD2Ps Precharge Power-Down Current (Slow Exit)[1]	IDD2Pf Precharge Power-Down Current (Fast Exit)[1]	IDD2Q Precharge Quiet Standby Current	IDD2N Precharge Standby Current	IDD3P Active Power-Down Current	IDD3N Active Standby Current	Notes
Timing example	n/a	n/a	n/a	Figure 15 on page 34	n/a	Figure 15 on page 34	
CKE	LOW	LOW	HIGH	HIGH	LOW	HIGH	
External clock	On	On	On	On	On	On	
^{t}CK	^{t}CK (MIN) IDD	^{t}CK(MIN) IDD	^{t}CK(MIN) IDD	^{t}CK (MIN) IDD	^{t}CK (MIN) IDD	^{t}CK (MIN) IDD	
^{t}RC	n/a	n/a	n/a	n/a	n/a	n/a	
^{t}RAS	n/a	n/a	n/a	n/a	n/a	n/a	
^{t}RCD	n/a	n/a	n/a	n/a	n/a	n/a	
^{t}RRD	n/a	n/a	n/a	n/a	n/a	n/a	
^{t}RC	n/a	n/a	n/a	n/a	n/a	n/a	
CL	n/a	n/a	n/a	n/a	n/a	n/a	
AL	n/a	n/a	n/a	n/a	n/a	n/a	
CS#	Stable	Stable	HIGH	HIGH	Stable	HIGH	
Command inputs	Stable	Stable	Stable	Switching	Stable	Switching	2
Row/column addresses	Stable	Stable	Stable	Switching	Stable	Switching	2
Bank addresses	Stable	Stable	Stable	Switching	Stable	Switching	2
Data I/O	Floating	Floating	Floating	Switching	Floating	Switching	3
Output buffer DQ, DQS	Off	Off	Off	Off	Off	Off	
ODT	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	
Burst length	n/a	n/a	n/a	n/a	n/a	n/a	
Active banks	None	None	None	None	All	All	
Idle banks	All	All	All	All	None	None	
Special notes	n/a	n/a	n/a	n/a	n/a	n/a	

Notes:
1. MR0[12] defines DLL on/off behavior during precharge power-down only; DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).
2. For further definition of input switching, see Table 10 on page 29.
3. For further definition of data switching, see Table 11 on page 29.

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Figure 15: IDD2N/IDD3N Example – DDR3-800, 5-5-5, x8 (-25E)

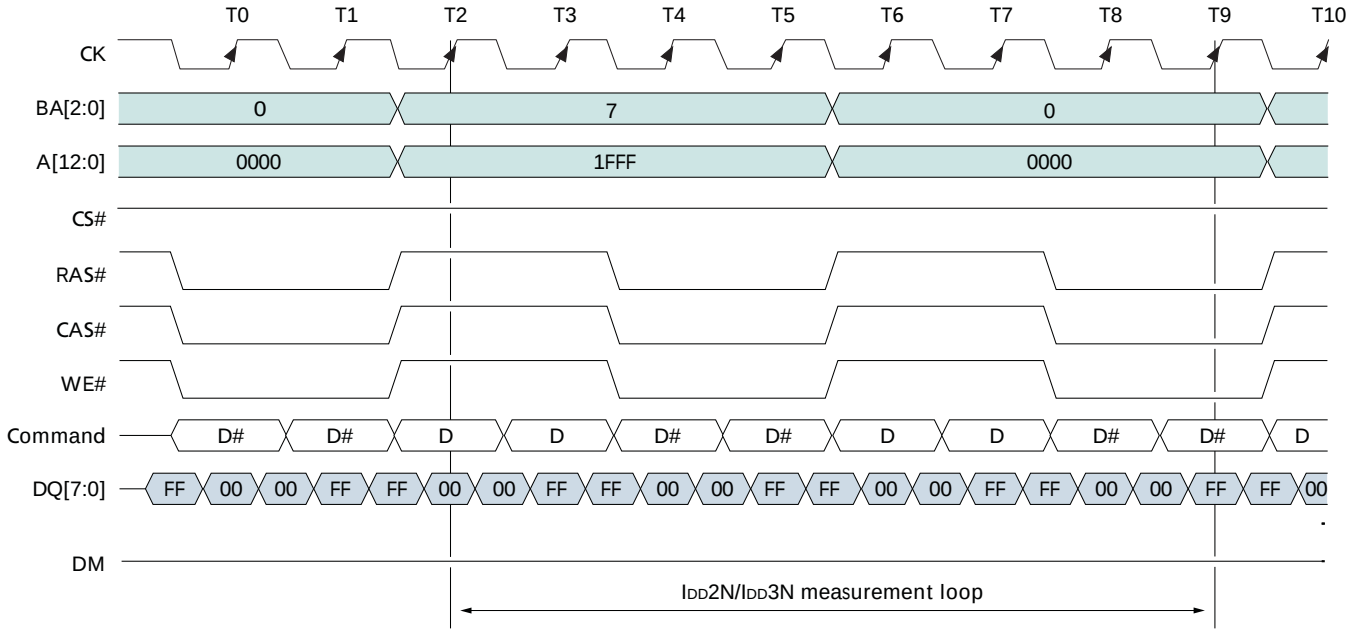

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Table 15: IDD Measurement Conditions for IDD4R, IDD4W

IDD Test	IDD4R: Burst Read Operating Current	IDD4W: Burst Write Operating Current	Notes
Timing diagram example	Figure 16 on page 36	–	
CKE	HIGH	HIGH	
External clock	On	On	
^{t}CK	^{t}CK (MIN) IDD	^{t}CK (MIN) IDD	
^{t}RC	n/a	n/a	
^{t}RAS	n/a	n/a	
^{t}RCD	n/a	n/a	
^{t}RRD	n/a	n/a	
^{t}RC	n/a	n/a	
CL	CL IDD	CL IDD	
AL	0	0	
CS#	HIGH between valid commands	HIGH between valid commands	
Command inputs	Switching; READ command/pattern: R0DDDR1DDDR2DDDR3DDDR4 . . . R*x* = READ from bank *x*	Switching; WRITE command/pattern: W0DDDW1DDDW2DDDW3DDDW4 . . . W*x* = WRITE to bank *x*	1
Row/column addresses	Column addresses switching; Address input A10 must always be LOW	Column addresses switching; Address input A10 must always be LOW	1
Bank addresses	Bank address looping (0-to-1-to-2-to-3 . . .)	Bank address looping (0-to-1-to-2-to-3 . . .)	
Data I/O	Seamless read data burst (BL8): Output data switches after every clock cycle, which means that read data is stable during falling DQS	Seamless write data burst (BL8): Input data switches after every clock cycle, which means that write data is stable during falling DQS	2
Output buffer DQ, DQS	Off	Off	
ODT	Disabled	Disabled	
Burst length	8 fixed (via MR0)	8 fixed (via MR0)	
Active banks	All	All	
Idle banks	None	None	
Special notes	n/a	DM always LOW	

Notes: 1. For further definition of input switching, see Table 10 on page 29.
2. For further definition of data switching, see Table 11 on page 29.

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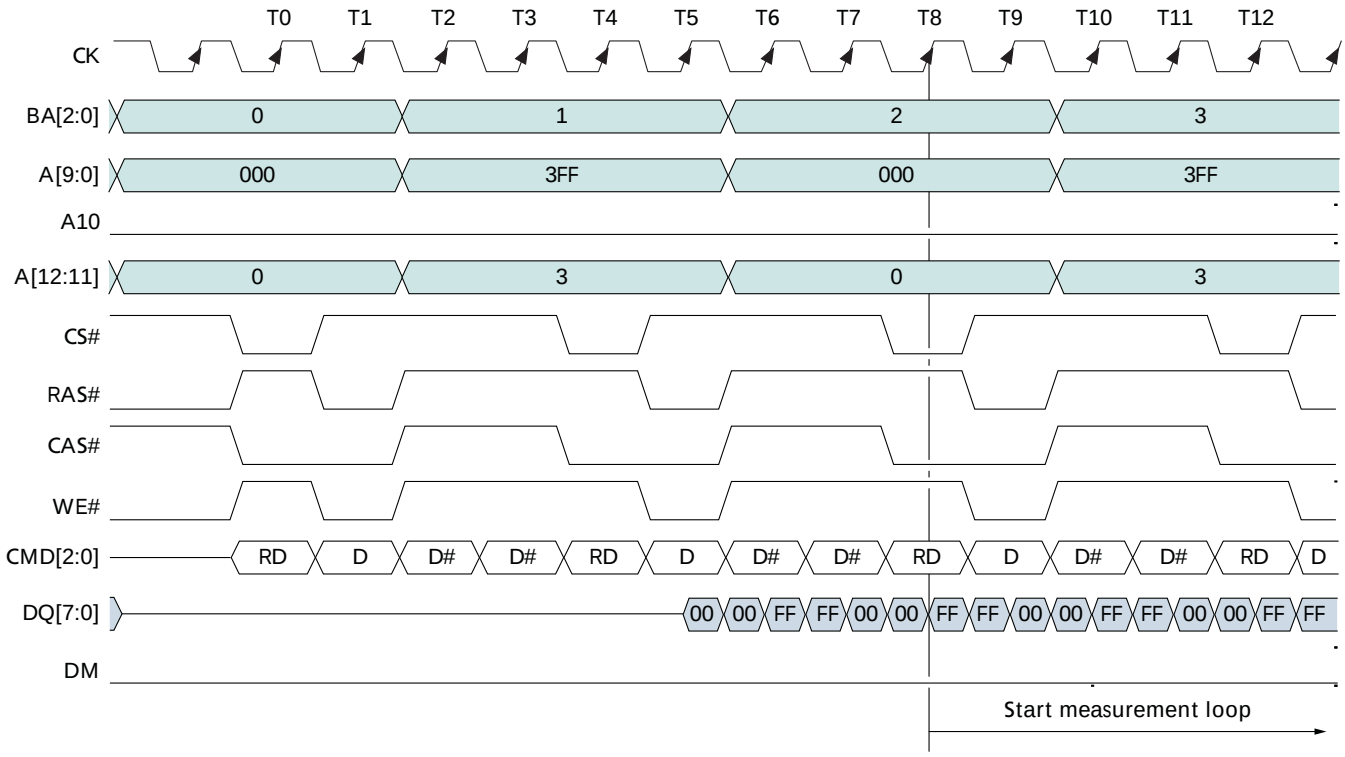
Figure 16: IDD4R Example – DDR3-800, 5-5-5, x8



Notes: 1. Data DQ is shown, but the output buffer should be switched off (per MR1[12] = 1) to achieve I_{OUT} = 0mA (MR1[12] = 0 is reflected in this example; however, test conditions are MR1[12] = 1). Address inputs are split into three parts.

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Table 16: IDD Measurement Conditions for IDD5B, IDD6, IDD6ET

IDD Test	IDD5B: Refresh Current	IDD6: Self Refresh Current Normal Temperature Range T_C = 0°C to 85°C	IDD6ET: Self Refresh Current Extended Temperature Range T_C = 0°C to 95°C	Notes
CKE	HIGH	LOW	LOW	
External clock	On	Off, CK and CK# = LOW	Off, CK and CK# = LOW	
^tCK	^tCK (MIN) IDD	n/a	n/a	
^tRC	n/a	n/a	n/a	
^tRAS	n/a	n/a	n/a	
^tRCD	n/a	n/a	n/a	
^tRRD	n/a	n/a	n/a	
^tRC	^tRFC (MIN) IDD	n/a	n/a	
CL	n/a	n/a	n/a	
AL	n/a	n/a	n/a	
CS#	HIGH between valid commands	Floating	Floating	
Command inputs	Switching	Floating	Floating	1
Row/column addresses	Switching	Floating	Floating	1
Bank addresses	Switching	Floating	Floating	1
Data I/O	Switching	Floating	Floating	2
Output buffer DQ, DQS	Disabled	Disabled	Disabled	
ODT	Disabled	Disabled	Disabled	
Burst length	n/a	n/a	n/a	
Active banks	REFRESH command every ^tRFC (MIN)	n/a	n/a	
Idle banks	None	n/a	n/a	
Special notes	n/a	SRT disabled	SRT enabled	

Notes:
1. For further definition of input switching, see Table 10 on page 29.
2. For further definition of data switching, see Table 11 on page 29.

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Table 17: IDD Measurement Conditions for IDD7

IDD Test	IDD7: All Banks Interleaved Read Current
CKE	HIGH
External clock	On
^{t}CK	^{t}CK (MIN) IDD
^{t}RC	^{t}RC (MIN) IDD
^{t}RAS	^{t}RAS (MIN) IDD
^{t}RCD	^{t}RCD (MIN) IDD
^{t}RRD	^{t}RRD (MIN) IDD
^{t}RC	n/a
CL	CL IDD
AL	CL - 1
CS#	HIGH between valid commands
Command inputs	See Table 10 on page 29 for patterns
Row/column addresses	Stable during DESELECTs (DES)
Bank addresses	Looping (see Table 10 on page 29 for patterns)
Data I/O	Read data (BL8): output data switches after every clock cycle, which means that read data is stable during falling DQS; I/O should be floating when no read data is being driven
Output buffer DQ, DQS	Off
ODT	Disabled
Burst length	8 fixed (via MR0)
Active banks	All, rotational
Idle banks	n/a

Table 18: IDD7 Patterns

Speed Bin	Width	IDD7 Pattern
DDR3-800 (-25, -25E)	x4, x8	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D A0 . . .
	x16	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D A0 . . .
DDR3-1066 (-187, -187E)	x4, x8	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D A0 . . .
	x16	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D A0 . . .
DDR3-1333 (-15, -15E, -15F)	x4, x8	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D A0 . . .
	x16	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D D D D D D A0 . . .
DDR3-1600 (-125E, -125F, -125)	x4, x8	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D A0 . . .
	x16	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D D D D D A0 . . .

Notes: 1. A0 = ACTIVATE bank *0*; RA0 = READ with auto precharge bank *0*; D = DESELECT.

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Electrical Characteristics – IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

Table 19: IDD Maximum Limits

Speed Bin							
IDD	Width	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units	Notes
IDD0	x4	65	75	85	95	mA	1, 2
	x8	90	100	110	120	mA	1, 2
	x16	90	100	110	120	mA	1, 2
IDD1	x4	85	95	105	115	mA	1, 2
	x8	110	120	130	140	mA	1, 2
	x16	110	130	150	170	mA	1, 2
IDD2P0	Slow	10	10	10	10	mA	1, 2
IDD2P1	Fast	25	25	30	35	mA	1, 2
IDD2Q	All	45	50	55	60	mA	1, 2
IDD2N	All	50	55	60	65	mA	1, 2
IDD3P	All	25	30	35	40	mA	1, 2
IDD3N	x4, x8	50	55	60	65	mA	1, 2
	x16	50	55	60	65	mA	1, 2
IDD4R	x4	130	160	200	250	mA	1, 2
	x8	130	160	200	250	mA	1, 2
	x16	190	230	270	315	mA	1, 2
IDD4W	x4	130	160	190	225	mA	1, 2
	x8	130	160	190	225	mA	1, 2
	x16	210	265	325	400	mA	1, 2
IDD5B	All	200	220	240	260	mA	1, 2
IDD6	All	7	7	7	7	mA	1, 2, 3
IDD6ET	All	9	9	9	9	mA	2, 4
IDD7	x4	230	250	315	400	mA	1, 2
	x8	350	390	490	600	mA	1, 2
	x16	350	380	420	460	mA	1, 2

Notes:
1. T_C = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase IDDx by up to an additional 2mA.
3. Restricted to T_C (MAX) = 85°C.
4. T_C = 85°C; ASR and ODT are disabled; SRT is enabled.

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Electrical Specifications – DC and AC

DC Operating Conditions

Table 20: DC Electrical Characteristics and Operating Conditions
All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1, 2
I/O supply voltage	V_{DDQ}	1.425	1.5	1.575	V	1, 2
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	I_I	–2	–	2	µA	
V_{REF} supply leakage current $V_{REF}DQ$ = V_{DD}/2 or $V_{REF}CA$ = V_{DD}/2 (All other pins not under test = 0V)	I_{VREF}	–1	–	1	µA	3, 4

Notes:
1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be less than or equal to V_{DD}. V_{SS} = V_{SSQ}.
2. V_{DD} and V_{DDQ} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
3. V_{REF} (see Table 21).
4. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.

Input Operating Conditions

Table 21: DC Electrical Characteristics and Input Conditions
All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Input reference voltage command/address bus	$V_{REF}CA(DC)$	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	1, 2
I/O reference voltage DQ bus	$V_{REF}DQ(DC)$	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	2, 3
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	–	0.5 × V_{DDQ}	–	V	4

Notes:
1. $V_{REF}CA(DC)$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on $V_{REF}CA$ may not exceed ±1 percent × V_{DD} around the $V_{REF}CA(DC)$ value. Peak-to-peak AC noise on $V_{REF}CA$ should not exceed ±2 percent of $V_{REF}CA(DC)$.
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. $V_{REF}DQ(DC)$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on $V_{REF}DQ$ may not exceed ±1 percent × V_{DD} around the $V_{REF}DQ(DC)$ value. Peak-to-peak AC noise on $V_{REF}DQ$ should not exceed ±2 percent of $V_{REF}DQ(DC)$.
4. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

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Table 22: AC Input Operating Conditions

Parameter/Condition	Symbol	DDR3-800 DDR3-1066	DDR3-1333 DDR3-1600	Units
Command and Address				
Input high AC voltage: Logic 1	$V_{IH(AC)}$ MIN	+175	+150 or +175	mV
Input high DC voltage: Logic 1	$V_{IH(DC)}$ MIN	+100	+100	mV
Input low DC voltage: Logic 0	$V_{IL(DC)}$ MAX	–100	–100	mV
Input low AC voltage: Logic 0	$V_{IL(AC)}$ MAX	–175	–150 or –175	mV
DQ and DM				
Input high AC voltage: Logic 1	$V_{IH(AC)}$ MIN	+175	+150	mV
Input high DC voltage: Logic 1	$V_{IH(DC)}$ MIN	+100	+100	mV
Input low DC voltage: Logic 0	$V_{IL(DC)}$ MAX	–100	–100	mV
Input low AC voltage: Logic 0	$V_{IL(AC)}$ MAX	–175	–150	mV

Notes:
1. All voltages are referenced to V_{REF}. V_{REF} is V_{REF}CA for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REF}DQ for DQ and DM inputs.
2. Input setup timing parameters (^{t}IS and ^{t}DS) are referenced at $V_{IL(AC)}$/$V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (^{t}IH and ^{t}DH) are referenced at $V_{IL(DC)}$/$V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).
5. For $V_{IH(AC)}$ and $V_{IL(AC)}$ levels of 150mV, special setup and hold derating and different ^{t}VAC numbers apply.

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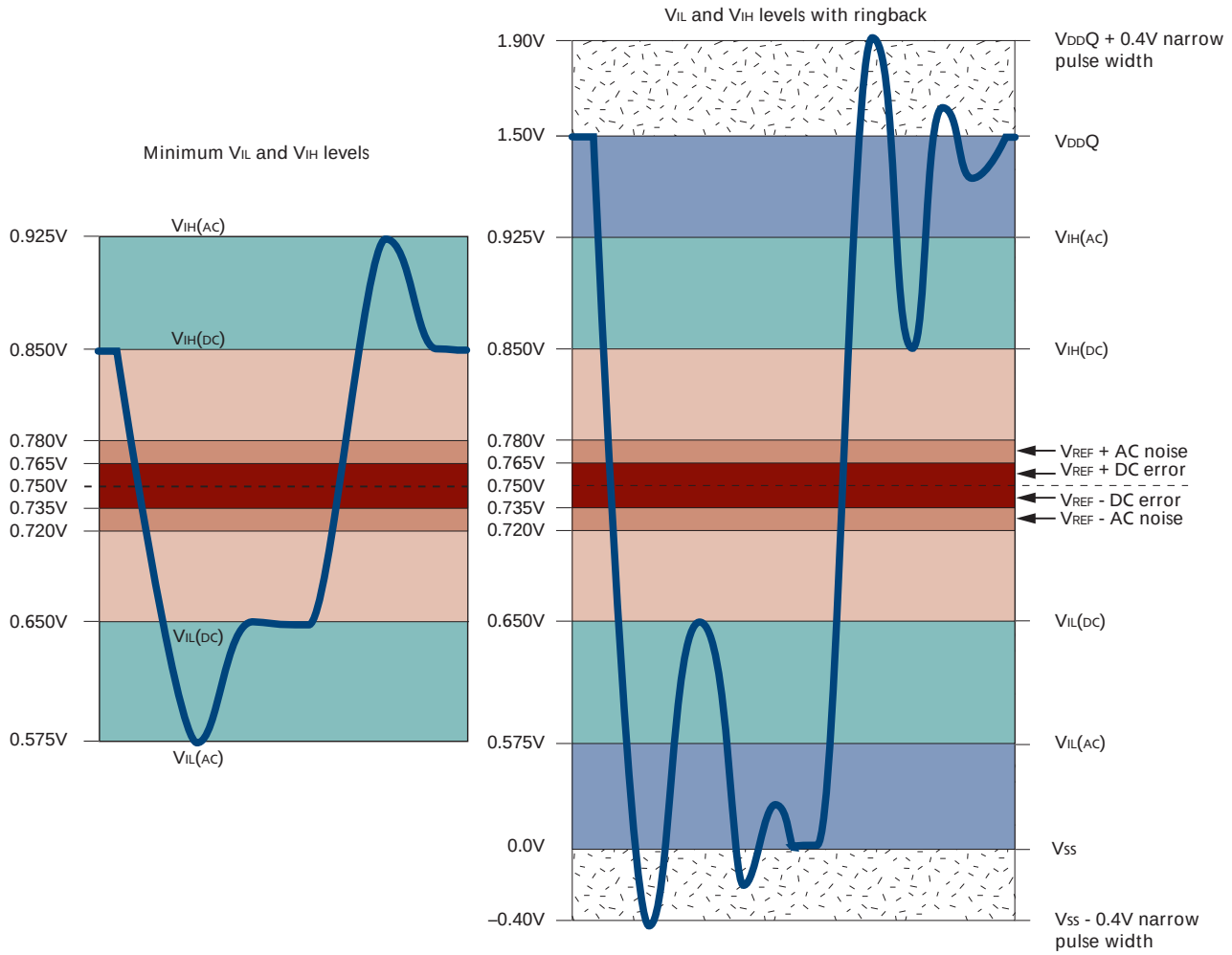
Figure 17: Input Signal



Notes: 1. Numbers in diagrams reflect nominal values.

AC Overshoot/Undershoot Specification

Table 23: Control and Address Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure 18 on page 43)	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 19 on page 43)	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (see Figure 18 on page 43)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns
Maximum undershoot area below VSS (see Figure 19 on page 43)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns

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Table 24: Clock, Data, Strobe, and Mask Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure 18 on page 43)	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 19 on page 43)	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD}/V_{DDQ} (see Figure 18 on page 43)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns
Maximum undershoot area below V_{SS}/V_{SSQ} (see Figure 19 on page 43)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns

Figure 18: Overshoot

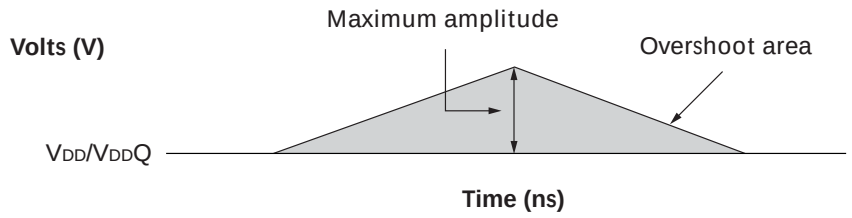

Figure 19: Undershoot

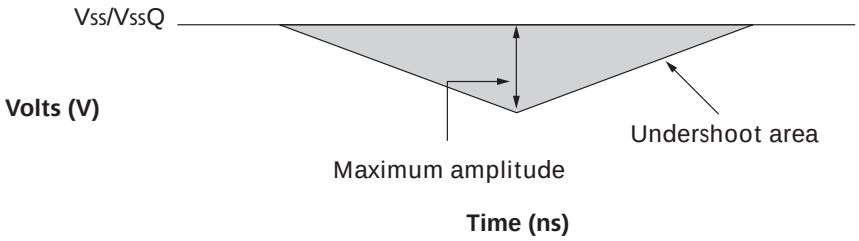

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Table 25: Differential Input Operating Conditions (CK, CK# and DQS, DQS#)
All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units
Differential input voltage	V_{IN}	–400	V_{DD} + 400	mV
Differential input midpoint voltage	$V_{MP(DC)}$	650	850	mV
Differential input voltage logic high	V_{IHDIFF}	200	V_{DD} + 400	mV
Differential input voltage logic low	V_{ILDIFF}	V_{SS}Q - 400	–200	mV
Differential input crossing voltage relative to V_{DD}/2 for CK, CK#	V_{IX}	$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150	mV
		$V_{REF(DC)}$ - 175	$V_{REF(DC)}$ + 175	mV
Differential input crossing voltage relative to V_{DD}/2 for DQS, DQS#		$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150	mV

Notes:
1. $V_{MP(DC)}$ specifies the input differential common mode voltage (V_{TR} + V_{CP})/2 where V_{TR} is the true input (CK, DQS) level and V_{CP} is the complementary input (CK#, DQS#) level. $V_{MP(DC)}$ is expected to be about 0.5 × V_{DD}Q.
2. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
3. Reference is V_{REF}CA(DC) for clock and for V_{REF}DQ(DC) for strobe.
4. Clock is referenced to V_{DD} and V_{SS}. Data strobe is referenced to V_{DD}Q and V_{SS}Q.
5. Differential input slew rate = 2 V/ns.
6. The V_{IX} extended range (±175mV) is allowed only for the clock. Additionally, the V_{IX} extended range is only allowed when the following conditions are met: The single-ended input signals are monotonic, have the single-ended swing V_{SEL}, V_{SEH} of at least V_{DD}/2 ±250mV, and the differential slew rate of CK, CK# is greater than 3 V/ns.

Figure 20: Single-Ended Requirements for Differential Signals

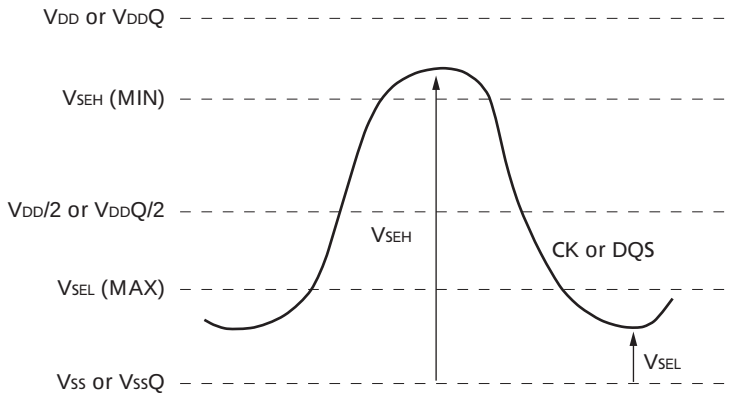

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Figure 21: Definition of Differential AC-Swing and ^{t}DVAC

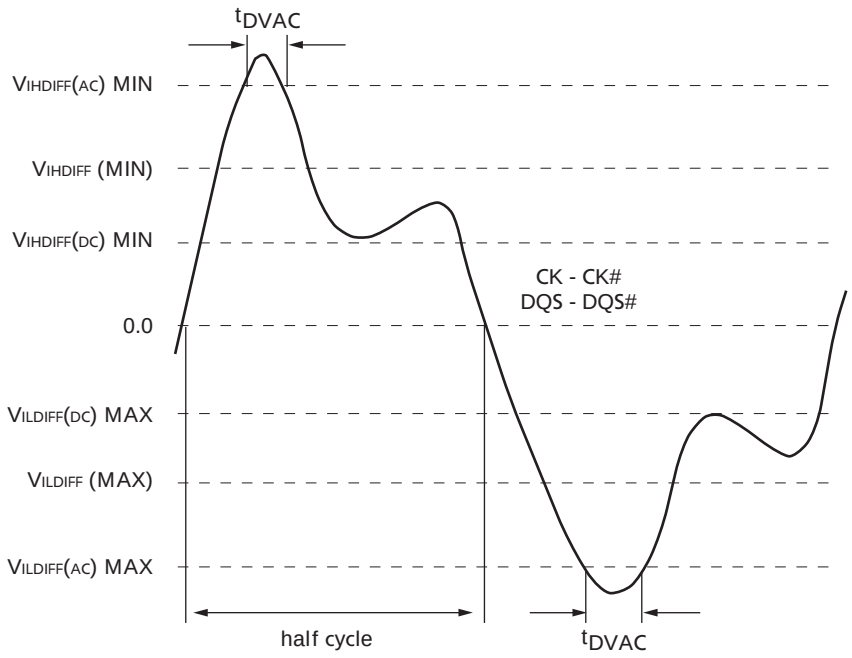

Table 26: Allowed Time Before Ringback (^{t}DVAC) for CK - CK# and DQS - DQS#
Below $V_{IL(AC)}$

Slew Rate (V/ns)	^{t}DVAC (ps) at |$V_{IHDIFF(AC)}$/$V_{ILDIFF(AC)}$|	
	350mV	300mV
>4.0	75	175
4.0	57	170
3.0	50	167
2.0	38	163
1.9	34	162
1.6	29	161
1.4	22	159
1.2	13	155
1.0	0	150
<1.0	0	150

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Slew Rate Definitions for Single-Ended Input Signals

Setup (^{t}IS and ^{t}DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IH(AC)}$ MIN. Setup (^{t}IS and ^{t}DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IL(AC)}$ MAX (see Figure 22 on page 47).

Hold (^{t}IH and ^{t}DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)}$ MAX and the first crossing of V_{REF}. Hold (^{t}IH and ^{t}DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)}$ MIN and the first crossing of V_{REF} (see Figure 22 on page 47).

Table 27: Single-Ended Input Slew Rate Definition

Input Slew Rates (Linear Signals)		Measured		
Input	**Edge**	**From**	**To**	**Calculation**
Setup	Rising	V_{REF}	$V_{IH(AC)}$ MIN	$\frac{V_{IH(AC)}\ MIN - V_{REF}}{\Delta TRS}$
	Falling	V_{REF}	$V_{IL(AC)}$ MAX	$\frac{V_{REF} - V_{IL(AC)}\ MAX}{\Delta TFS}$
Hold	Rising	$V_{IL(DC)}$ MAX	V_{REF}	$\frac{V_{REF} - V_{IL(DC)}\ MAX}{\Delta TFH}$
	Falling	$V_{IH(DC)}$ MIN	V_{REF}	$\frac{V_{IH(DC)}\ MIN - V_{REF}}{\Delta TRSH}$

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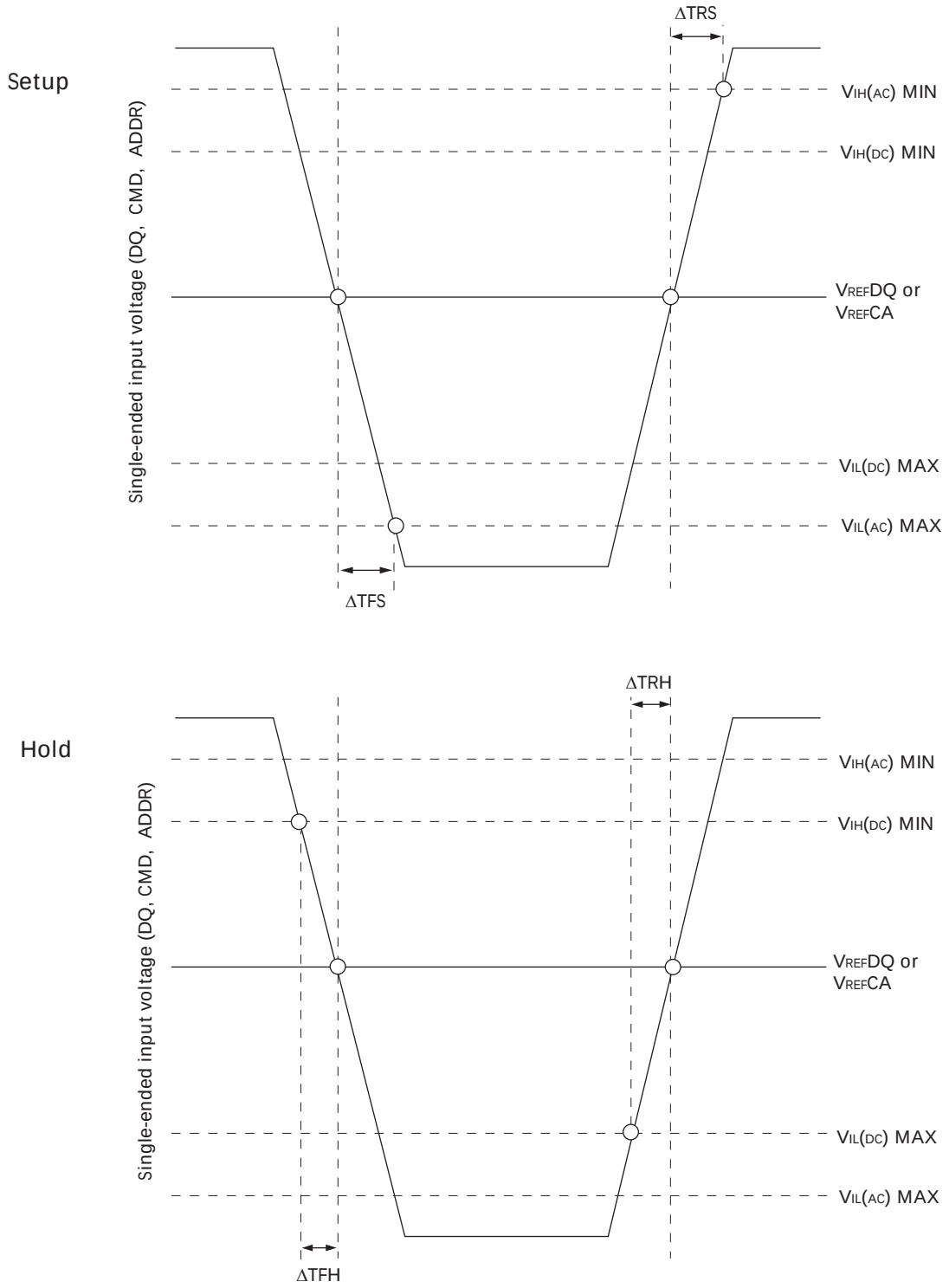
Figure 22: Nominal Slew Rate Definition for Single-Ended Input Signals



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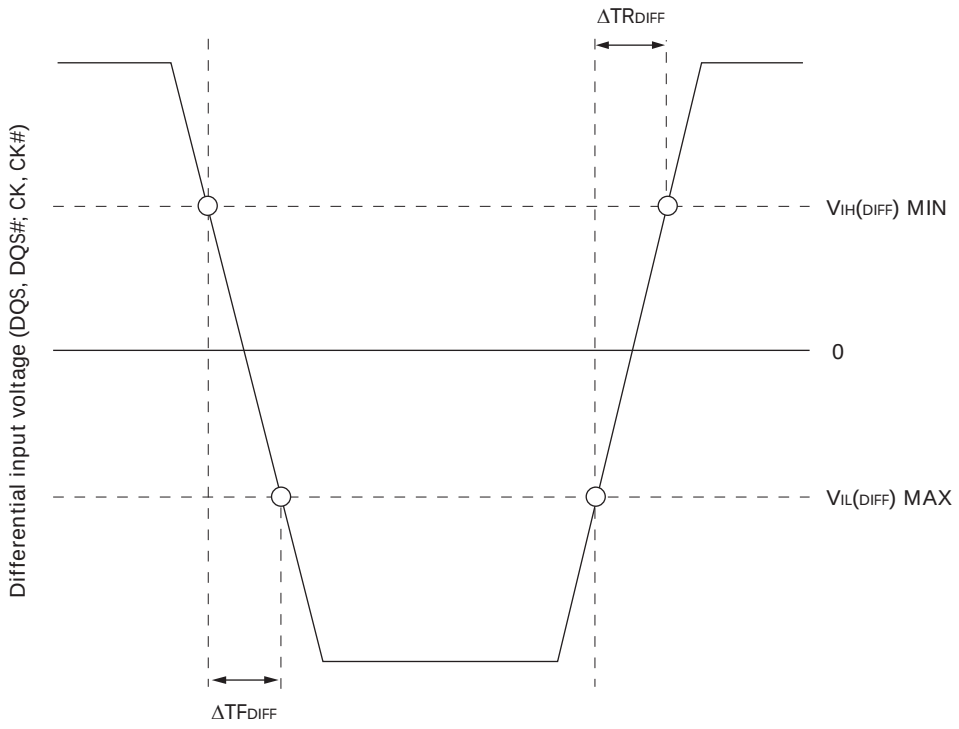
Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured, as shown in Table 28 and Figure 23. The nominal slew rate for a rising signal is defined as the slew rate between $V_{IL(DIFF)}$ MAX and $V_{IH(DIFF)}$ MIN. The nominal slew rate for a falling signal is defined as the slew rate between $V_{IH(DIFF)}$ MIN and $V_{IL(DIFF)}$ MAX.

Table 28: Differential Input Slew Rate Definition

Differential Input Slew Rates (Linear Signals)		Measured		
Input	**Edge**	**From**	**To**	**Calculation**
CK and DQS reference	Rising	$V_{IL(DIFF)}$ MAX	$V_{IH(DIFF)}$ MIN	$\frac{V_{IH(DIFF)}\ MIN - V_{IL(DIFF)}\ MAX}{\Delta TR_{(DIFF)}}$
	Falling	$V_{IH(DIFF)}$ MIN	$V_{IL(DIFF)}$ MAX	$\frac{V_{IH(DIFF)}\ MIN - V_{IL(DIFF)}\ MAX}{\Delta TF_{(DIFF)}}$

Figure 23: Nominal Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#



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ODT Characteristics

ODT effective resistance RTT is defined by MR1[9, 6, and 2]. ODT is applied to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls (x8 devices only). The ODT target values are listed in Table 29 and Table 30 on page 50. A functional representation of the ODT is shown in Figure 24. The individual pull-up and pull-down resistors (RTT_{PU} and RTT_{PD}) are defined as follows:

- RTT_{PU} = (VDDQ - VOUT)/|IOUT|, under the condition that RTT_{PD} is turned off
- RTT_{PD} = (VOUT)/|IOUT|, under the condition that RTT_{PU} is turned off

Figure 24: ODT Levels and I-V Characteristics

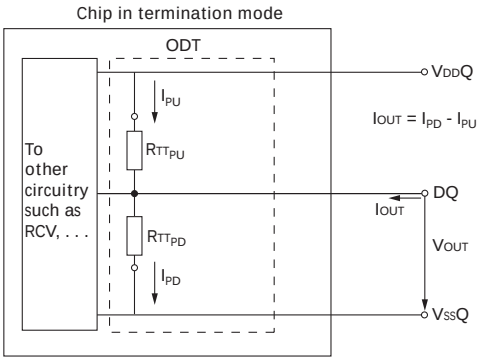

Table 29: On-Die Termination DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
RTT effective impedance	RTT_EFF	See Table 30 on page 50				1, 2
Deviation of VM with respect to VDDQ/2	ΔVM	–5		+5	%	1, 2, 3

Notes:
1. Tolerance limits are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS). Refer to "ODT Sensitivity" on page 50 if either the temperature or voltage changes after calibration.
2. Measurement definition for RTT: Apply VIH(AC) to pin under test and measure current I[VIH(AC)], then apply VIL(AC) to pin under test and measure current I[VIL(AC)]:

$$RTT = \frac{VIH(AC) - VIL(AC)}{|I(VIH(AC)) - I(VIL(AC))|}$$

3. Measure voltage (VM) at the tested pin with no load:

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1\right) \times 100$$

ODT Resistors

Table 30 on page 50 provides an overview of the ODT DC electrical characteristics. The values provided are not specification requirements; however, they can be used as design guidelines to indicate what RTT is targeted to provide:

- RTT 120Ω is made up of $RTT_{120PD240}$ and $RTT_{120PU240}$
- RTT 60Ω is made up of $RTT_{60PD120}$ and $RTT_{60PU120}$
- RTT 40Ω is made up of RTT_{40PD80} and RTT_{40PU80}
- RTT 30Ω is made up of RTT_{30PD60} and RTT_{30PU60}
- RTT 20Ω is made up of RTT_{20PD40} and RTT_{20PU40}

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Table 30: R_{TT} Effective Impedances

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 1, 0	120Ω	$R_{TT120PD240}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/1
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/1
		$R_{TT120PU240}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/1
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/1
	120Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/2
0, 0, 1	60Ω	$R_{TT60PD120}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/2
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/2
		$R_{TT60PU120}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/2
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/2
	60Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/4
0, 1, 1	40Ω	$R_{TT40PD80}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/3
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/3
		$R_{TT40PU80}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/3
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/3
	40Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/6
1, 0, 1	30Ω	$R_{TT30PD60}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/4
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/4
		$R_{TT30PU60}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/4
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/4
	30Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/8
1, 0, 0	20Ω	$R_{TT20PD40}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/6
		$R_{TT20PU40}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/6
	20Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/12

Notes: 1. Values assume an RZQ of 240Ω (±1 percent).

ODT Sensitivity

If either the temperature or voltage changes after I/O calibration, the tolerance limits listed in Table 29 on page 49 and Table 30 can be expected to widen according to Tables 31 and 32 on page 51.

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Table 31: ODT Sensitivity Definition

Symbol	Min	Max	Units
R_{TT}	0.9 - $dR_{TT}dT$ × |DT| - $dR_{TT}dV$ × |DV|	1.6 + $dR_{TT}dT$ × |DT| + $dR_{TT}dV$ × |DV|	RZQ/(2, 4, 6, 8, 12)

Notes: 1. ΔT = T - T(@ calibration), ΔV = V_{DDQ} - V_{DDQ}(@ calibration) and V_{DD} = V_{DDQ}.

Table 32: ODT Temperature and Voltage Sensitivity

Change	Min	Max	Units
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

Notes: 1. ΔT = T - T(@ calibration), ΔV = V_{DDQ} - V_{DDQ}(@ calibration) and V_{DD} = V_{DDQ}.

ODT Timing Definitions

ODT loading differs from that used in AC timing measurements. The reference load for ODT timings is shown in Figure 25. Two parameters define when ODT turns on or off synchronously, two define when ODT turns on or off asynchronously, and another defines when ODT turns on or off dynamically. Table 33 outlines and provides definition and measurement reference settings for each parameter (see Figure 34 on page 52).

ODT turn-on time begins when the output leaves High-Z and ODT resistance begins to turn on. ODT turn-off time begins when the output leaves Low-Z and ODT resistance begins to turn off.

Figure 25: ODT Timing Reference Load

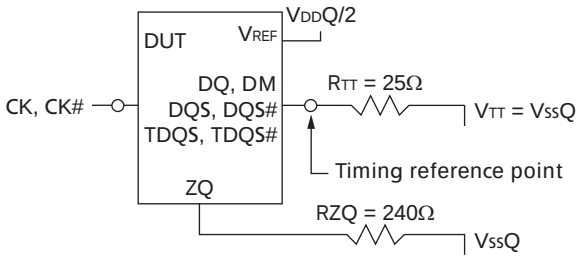

Table 33: ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
^{t}AON	Rising edge of CK - CK# defined by the end point of ODTL on	Extrapolated point at V_{SSQ}	Figure 26 on page 52
^{t}AOF	Rising edge of CK - CK# defined by the end point of ODTL off	Extrapolated point at V_{RTT_NOM}	Figure 26 on page 52
$^{t}AONPD$	Rising edge of CK - CK# with ODT first being registered HIGH	Extrapolated point at V_{SSQ}	Figure 27 on page 53
$^{t}AOFPD$	Rising edge of CK - CK# with ODT first being registered LOW	Extrapolated point at V_{RTT_NOM}	Figure 27 on page 53
^{t}ADC	Rising edge of CK - CK# defined by the end point of $ODTL_{CNW}$, $ODTL_{CWN4}$, or $ODTL_{CWN8}$	Extrapolated points at V_{RTT_WR} and V_{RTT_NOM}	Figure 28 on page 53

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Table 34: Reference Settings for ODT Timing Measurements

Measured Parameter	R_{TT_NOM} Setting	R_{TT_WR} Setting	V_{SW1}	V_{SW2}
^{t}AON	RZQ/4 (60Ω)	n/a	50mV	100mV
	RZQ/12 (20Ω)	n/a	100mV	200mV
^{t}AOF	RZQ/4 (60Ω)	n/a	50mV	100mV
	RZQ/12 (20Ω)	n/a	100mV	200mV
^{t}AONPD	RZQ/4 (60Ω)	n/a	50mV	100mV
	RZQ/12 (20Ω)	n/a	100mV	200mV
^{t}AOFPD	RZQ/4 (60Ω)	n/a	50mV	100mV
	RZQ/12 (20Ω)	n/a	100mV	200mV
^{t}ADC	RZQ/12 (20Ω)	RZQ/2 (120Ω)	200mV	300mV

Notes: 1. Assume an RZQ of 240Ω (±1 percent) and that proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).

Figure 26: ^{t}AON and ^{t}AOF Definitions

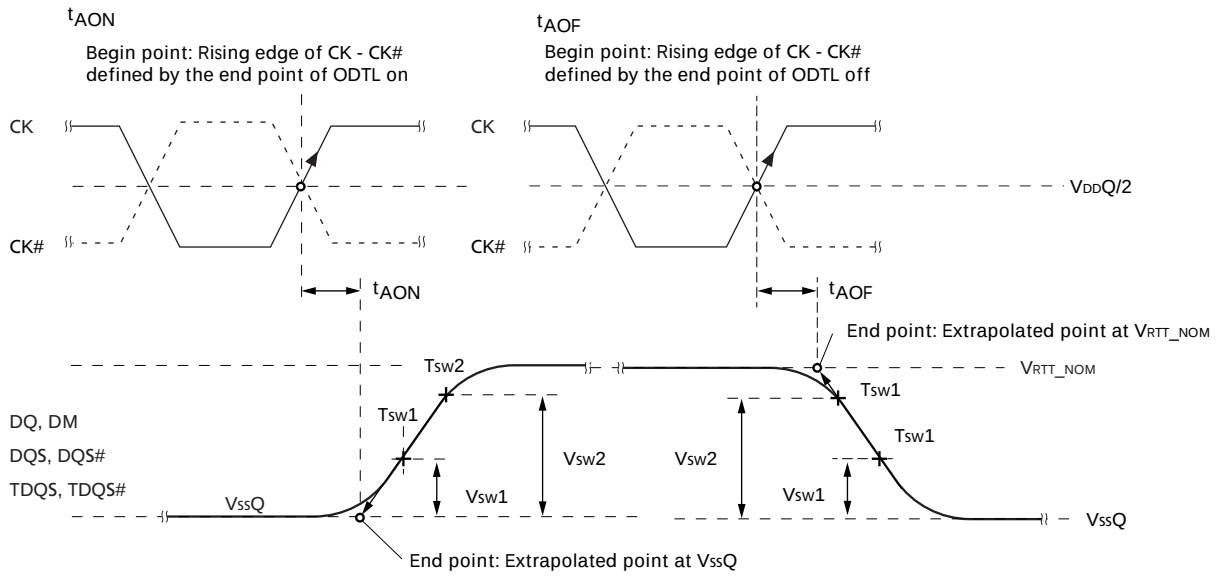

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Figure 27: ^{t}AONPD and ^{t}AOFPD Definition

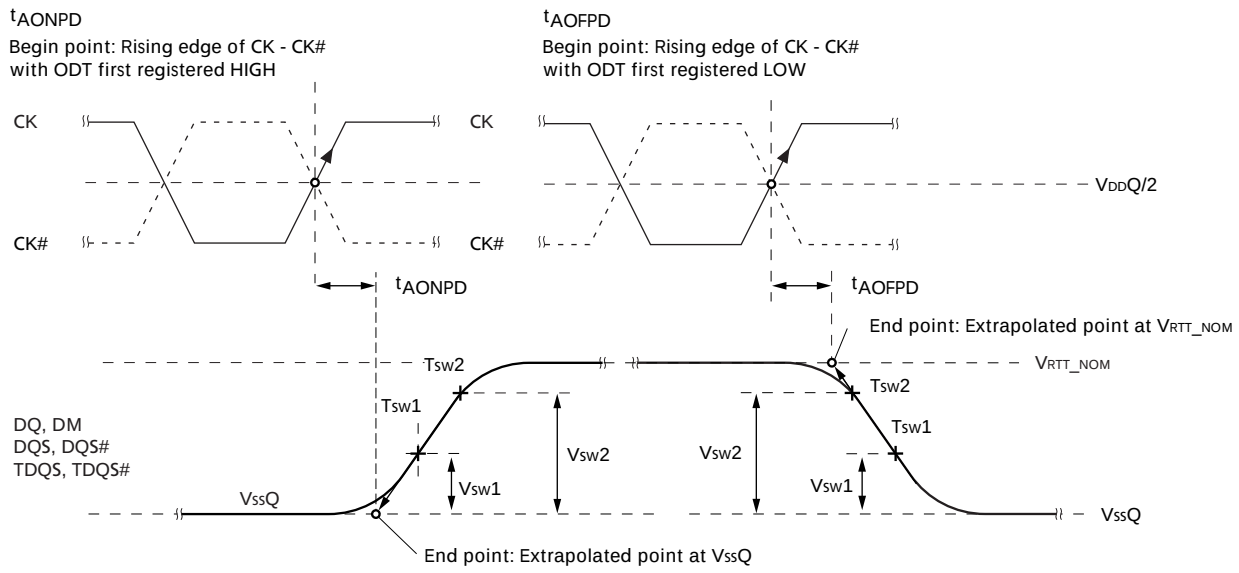
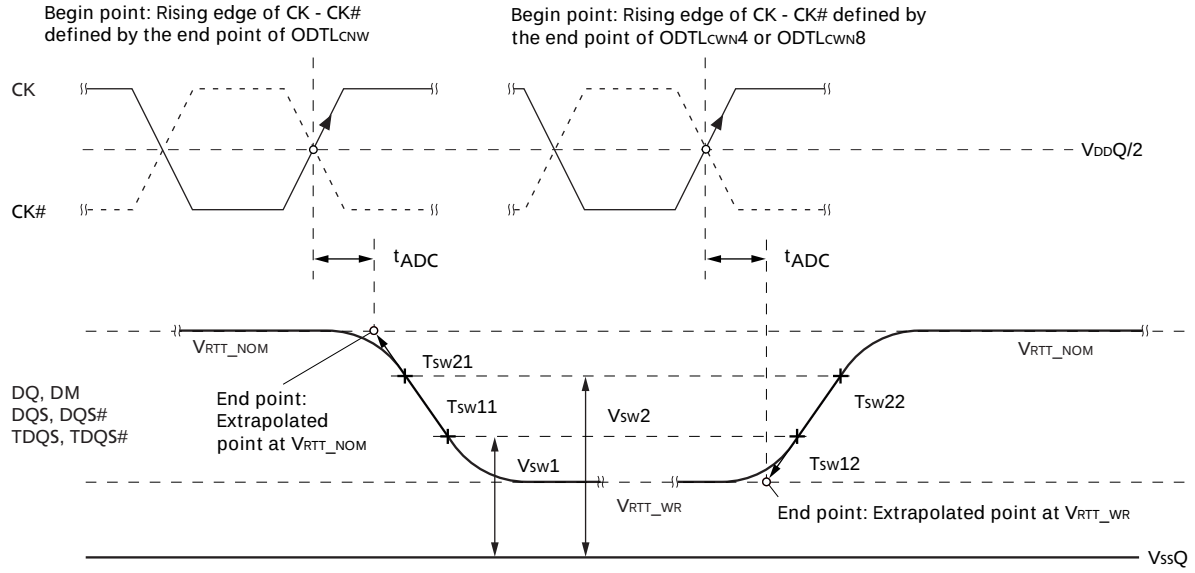


Figure 28: ^{t}ADC Definition



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Output Driver Impedance

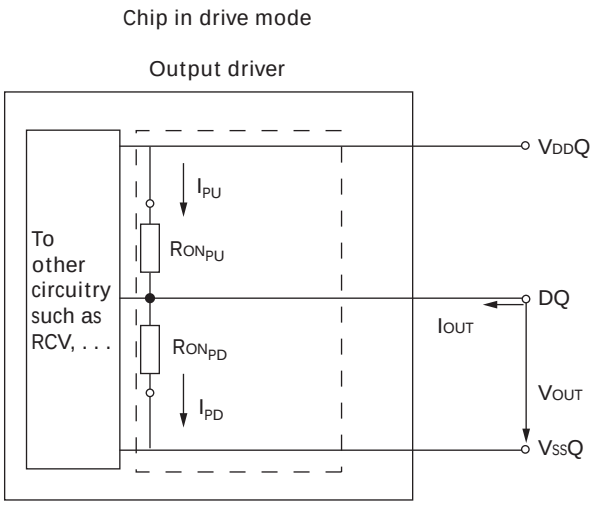
The output driver impedance is selected by MR1[5,1] during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed. Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown in Figure 29 on page 54. The output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:

- $RON_x = RZQ/y$ (with RZQ = 240Ω ±1 percent; x = 34Ω or 40Ω with y = 7 or 6, respectively)

The individual pull-up and pull-down resistors (RON_{PU} and RON_{PD}) are defined as follows:

- $RON_{PU} = (VDDQ - VOUT)/|IOUT|$, when RON_{PD} is turned off
- $RON_{PD} = (VOUT)/|IOUT|$, when RON_{PU} is turned off

Figure 29: Output Driver



34Ω Output Driver Impedance

The 34Ω driver (MR1[5, 1] = 01) is the default driver. Unless otherwise stated, all timings and specifications listed herein apply to the 34Ω driver only. Its impedance RON is defined by the value of the external reference resistor RZQ as follows: $RON_{34} = RZQ/7$ (with nominal RZQ = 240Ω ±1 percent) and is actually 34.3Ω ±1 percent. The 34Ω output driver impedance characteristics are listed in Table 35 on page 55.

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Table 35: 34Ω Driver Impedance Characteristics

MR1[5,1]	RON	Resistor	VOUT	Min	Nom	Max	Units	Notes
0,1	34.3Ω	Ron_{34PD}	0.2/VDDQ	0.6	1.0	1.1	RZQ/7	1
			0.5/VDDQ	0.9	1.0	1.1	RZQ/7	1
			0.8/VDDQ	0.9	1.0	1.4	RZQ/7	1
		RON_{34PU}	0.2/VDDQ	0.9	1.0	1.4	RZQ/7	1
			0.5/VDDQ	0.9	1.0	1.1	RZQ/7	1
			0.8/VDDQ	0.6	1.0	1.1	RZQ/7	1
Pull-up/pull-down mismatch (MM_{PUPD})			0.5/VDDQ	–10%	n/a	10	%	1, 2

Notes:
1. Tolerance limits assume RZQ of 240Ω (±1 percent) and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS). Refer to "34W Driver Output Sensitivity" on page 56 if either the temperature or the voltage changes after calibration.
2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both RON_{PU} and RON_{PD} at 0.5 × VDDQ:

$$MM_{PUPD} = \frac{RON_{PU} - RON_{PD}}{RON_{NOM}} x100$$

34Ω Driver

The 34Ω driver's current range has been calculated and summarized in Table 37 on page 56 for VDD = 1.5V, Table 38 on page 56 for VDD = 1.575V, and Table 39 on page 56 for VDD = 1.425V. The individual pull-up and pull-down resistors (RON_{34PD} and RON_{34PU}) are defined as follows:

- RON_{34PD} = (VOUT)/|IOUT|; RON_{34PU} is turned off
- RON_{34PU} = (VDDQ - VOUT)/|IOUT|; RON_{34PD} is turned off

Table 36: 34Ω Driver Pull-Up and Pull-Down Impedance Calculations

RON				Min	Nom	Max	Units
RZQ = 240Ω ±1 percent				237.6	240	242.4	Ω
RZQ/7 = (240Ω ±1 percent)/7				33.9	34.3	34.6	Ω
MR1[5,1]	**RON**	**Resistor**	**VOUT**	**Min**	**Nom**	**Max**	**Units**
0, 1	34.3Ω	RON_{34PD}	0.2 × VDDQ	20.4	34.3	38.1	Ω
			0.5 × VDDQ	30.5	34.3	38.1	Ω
			0.8 × VDDQ	30.5	34.3	48.5	Ω
		RON_{34PU}	0.2 × VDDQ	30.5	34.3	48.5	Ω
			0.5 × VDDQ	30.5	34.3	38.1	Ω
			0.8 × VDDQ	20.4	34.3	38.1	Ω

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Table 37: 34Ω Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ} = 1.5V$

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Units
0, 1	34.3Ω	R_{ON34PD}	I_{OL} @ 0.2 × V_{DDQ}	14.7	8.8	7.9	mA
			I_{OL} @ 0.5 × V_{DDQ}	24.6	21.9	19.7	mA
			I_{OL} @ 0.8 × V_{DDQ}	39.3	35.0	24.8	mA
		R_{ON34PU}	I_{OH} @ 0.2 × V_{DDQ}	39.3	35.0	24.8	mA
			I_{OH} @ 0.5 × V_{DDQ}	24.6	21.9	19.7	mA
			I_{OH} @ 0.8 × V_{DDQ}	14.7	8.8	7.9	mA

Table 38: 34Ω Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ} = 1.575V$

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Units
0, 1	34.3Ω	R_{ON34PD}	I_{OL} @ 0.2 × V_{DDQ}	15.5	9.2	8.3	mA
			I_{OL} @ 0.5 × V_{DDQ}	25.8	23	20.7	mA
			I_{OL} @ 0.8 × V_{DDQ}	41.2	36.8	26	mA
		R_{ON34PU}	I_{OH} @ 0.2 × V_{DDQ}	41.2	36.8	26	mA
			I_{OH} @ 0.5 × V_{DDQ}	25.8	23	20.7	mA
			I_{OH} @ 0.8 × V_{DDQ}	15.5	9.2	8.3	mA

Table 39: 34Ω Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ} = 1.425V$

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Units
0, 1	34.3Ω	R_{ON34PD}	I_{OL} @ 0.2 × V_{DDQ}	14.0	8.3	7.5	mA
			I_{OL} @ 0.5 × V_{DDQ}	23.3	20.8	18.7	mA
			I_{OL} @ 0.8 × V_{DDQ}	37.3	33.3	23.5	mA
		R_{ON34PU}	I_{OH} @ 0.2 × V_{DDQ}	37.3	33.3	23.5	mA
			I_{OH} @ 0.5 × V_{DDQ}	23.3	20.8	18.7	mA
			I_{OH} @ 0.8 × V_{DDQ}	14.0	8.3	7.5	mA

34Ω Driver Output Sensitivity

If either the temperature or the voltage changes after ZQ calibration, the tolerance limits listed in Table 35 on page 55 can be expected to widen according to Table 40 and Table 41 on page 57.

Table 40: 34Ω Output Driver Sensitivity Definition

Symbol	Min	Max	Units
R_{ON} @ 0.8 × V_{DDQ}	0.9 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.1 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/7
R_{ON} @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/7
R_{ON} @ 0.2 × V_{DDQ}	0.9 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.1 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/7

Notes: 1. ΔT = T - T(@ calibration), ΔV = V_{DDQ} - V_{DDQ}(@ calibration), and $V_{DD} = V_{DDQ}$.

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Table 41: 34Ω Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Units
dRONdTM	0	1.5	%/°C
dRONdVM	0	0.13	%/mV
dRONdTL	0	1.5	%/°C
dRONdVL	0	0.13	%/mV
dRONdTH	0	1.5	%/°C
dRONdVH	0	0.13	%/mV

Alternative 40Ω Driver

Table 42: 40Ω Driver Impedance Characteristics

MR1[5,1]	RON	Resistor	VOUT	Min	Nom	Max	Units	Notes
0,0	40Ω	RON_{40PD}	0.2 × VDDQ	0.6	1.0	1.1	RZQ/6	1, 2
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/6	1, 2
			0.8 × VDDQ	0.9	1.0	1.4	RZQ/6	1, 2
		RON_{40PU}	0.2 × VDDQ	0.9	1.0	1.4	RZQ/6	1, 2
			0.5 × VDDQ	0.9	1.0	1.1	RZQ/6	1, 2
			0.8 × VDDQ	0.6	1.0	1.1	RZQ/6	1, 2
Pull-up/pull-down mismatch (MM_{PUPD})			0.5 × VDDQ	–10%	n/a	10	%	1, 2

Notes:
1. Tolerance limits assume RZQ of 240Ω (±1 percent) and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS). Refer to "40W Driver Output Sensitivity" on page 57 if either the temperature or the voltage changes after calibration.
2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both RON_{PU} and RON_{PD} at 0.5 × VDDQ:

$$MM_{PUPD} = \frac{RON_{PU} - RON_{PD}}{RON_{Nom}} x100$$

40Ω Driver Output Sensitivity

If either the temperature or the voltage changes after I/O calibration, the tolerance limits listed in Table 42 can be expected to widen according to Table 43 and Table 44 on page 58.

Table 43: 40Ω Output Driver Sensitivity Definition

Symbol	Min	Max	Units
RON @ 0.8 × VDDQ	0.9 - dRONdTH × |ΔT| - dRONdVH × |ΔV|	1.1 + dRONdTH × |ΔT| + dRONdVH × |ΔV|	RZQ/6
RON @ 0.5 × VDDQ	0.9 - dRONdTM × |ΔT| - dRONdVM × |ΔV|	1.1 + dRONdTM × |ΔT| + dRONdVM × |ΔV|	RZQ/6
RON @ 0.2 × VDDQ	0.9 - dRONdTL × |ΔT| - dRONdVL × |ΔV|	1.1 + dRONdTL × |ΔT| + dRONdVL × |ΔV|	RZQ/6

Notes: 1. ΔT = T - T(@ calibration), ΔV = VDDQ - VDDQ(@ calibration), and VDD = VDDQ.

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Table 44: 40Ω Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
dRONdTM	0	1.5	%/°C
dRONdVM	0	0.15	%/mV
dRONdTL	0	1.5	%/°C
dRONdVL	0	0.15	%/mV
dRONdTH	0	1.5	%/°C
dRONdVH	0	0.15	%/mV

Output Characteristics and Operating Conditions

The DRAM uses both single-ended and differential output drivers. The single-ended output driver is summarized in Table 45 while the differential output driver is summarized in Table 46 on page 59.

Table 45: Single-Ended Output Driver Characteristics
All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units	Notes
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}; ODT is disabled; ODT is HIGH	I_{OZ}	–5	+5	µA	1
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)}$ = V_{REF} - 0.1 × V_{DDQ} and $V_{OH(AC)}$ = V_{REF} + 0.1 × V_{DDQ}	SR_{QSE}	2.5	5	V/ns	1, 2, 3
Single-ended DC high-level output voltage	$V_{OH(DC)}$	0.8 × V_{DDQ}		V	1, 2, 4
Single-ended DC mid-point level output voltage	$V_{OM(DC)}$	0.5 × V_{DDQ}		V	1, 2, 4
Single-ended DC low-level output voltage	$V_{OL(DC)}$	0.2 × V_{DDQ}		V	1, 2, 4
Single-ended AC high-level output voltage	$V_{OH(AC)}$	V_{TT} + 0.1 × V_{DDQ}		V	1, 2, 3, 5
Single-ended AC low-level output voltage	$V_{OL(AC)}$	V_{TT} - 0.1 × V_{DDQ}		V	1, 2, 3, 5
Delta R_{ON} between pull-up and pull-down for DQ/DQS	MM_{PUPD}	–10	+10	%	1, 6
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				3

Notes:
1. RZQ of 240Ω (±1 percent) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).
2. V_{TT} = V_{DDQ}/2.
3. See Figure 32 on page 60 for the test load configuration.
4. See Table 35 on page 55 for IV curve linearity. Do not use AC test load.
5. See Table 47 on page 61 for output slew rate.
6. See Table 35 on page 55 for additional information.
7. See Figure 30 on page 59 for an example of a single-ended output signal.

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Table 46: Differential Output Driver Characteristics
All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units	Notes
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}; ODT is disabled; ODT is HIGH	I_{OZ}	–5	+5	µA	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OLDIFF(AC)}$ = –0.2 × V_{DDQ} and $V_{OHDIFF(AC)}$ = +0.2 × V_{DDQ}	SRQ_{DIFF}	5	10	V/ns	1
Output differential cross-point voltage	$V_{OX(AC)}$	V_{REF} - 150	V_{REF} + 150	mV	1, 2, 3
Differential high-level output voltage	$V_{OHDIFF(AC)}$	+0.2 × V_{DDQ}		V	1, 4
Differential low-level output voltage	$V_{OLDIFF(AC)}$	–0.2 × V_{DDQ}		V	1, 4
Delta R_{ON} between pull-up and pull-down for DQ/DQS	MM_{PUPD}	–10	+10	%	1, 5
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				3

Notes:
1. RZQ of 240Ω (±1 percent) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}).
2. V_{REF} = V_{DDQ}/2.
3. See Figure 32 on page 60 for the test load configuration.
4. See Table 48 on page 62 for the output slew rate.
5. See Table 35 on page 55 for additional information.
6. See Figure 31 on page 60 for an example of a differential output signal.

Figure 30: DQ Output Signal

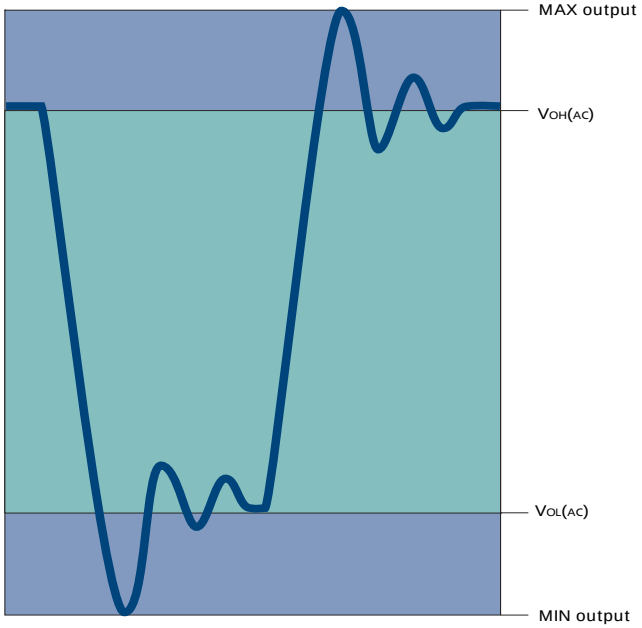

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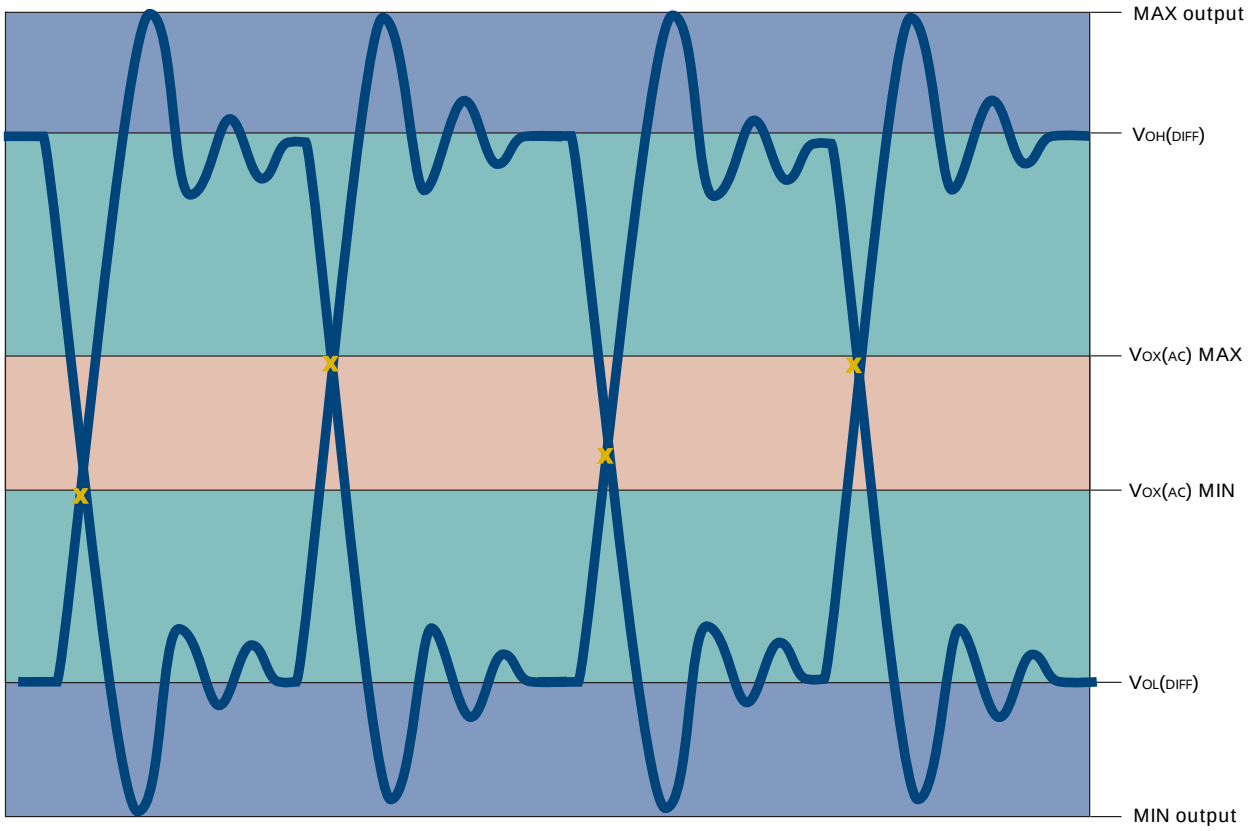
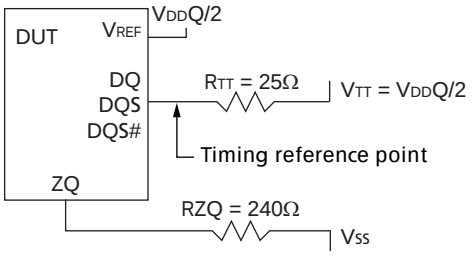
Figure 31: Differential Output Signal



Reference Output Load

Figure 32 on page 60 represents the effective reference load of 25Ω used in defining the relevant device AC timing parameters (except ODT reference timing) as well as the output slew rate measurements. It is not intended to be a precise representation of a particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Figure 32: Reference Output Load for AC Timing and Output Slew Rate



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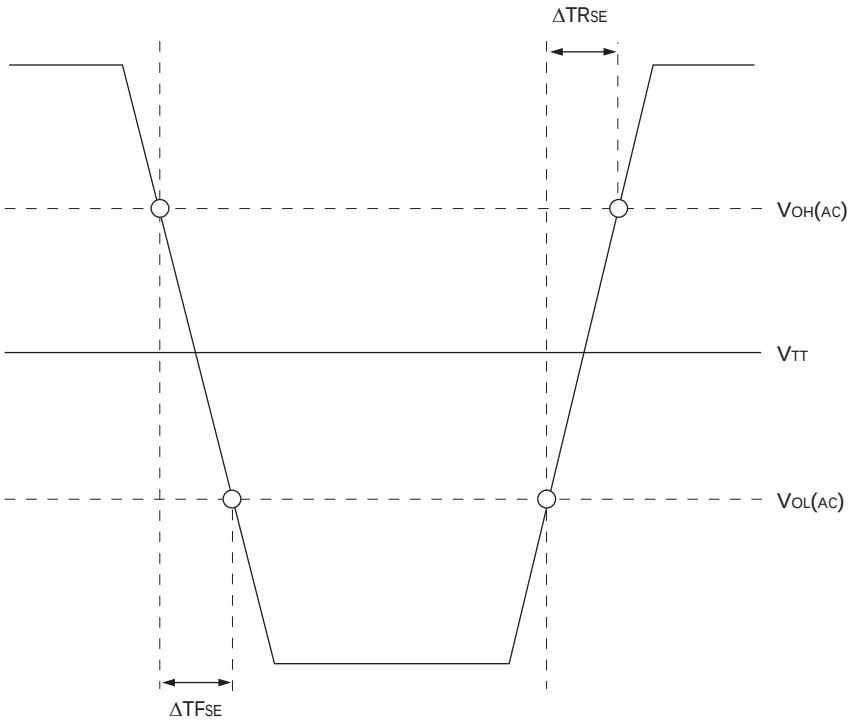
Slew Rate Definitions for Single-Ended Output Signals

The single-ended output driver is summarized in Table 45 on page 58. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC)$ and $V_{OH}(AC)$ for single-ended signals, as shown in Table 47 and Figure 33.

Table 47: Single-Ended Output Slew Rate Definition

Single-Ended Output Slew Rates (Linear Signals)		Measured		
Output	**Edge**	**From**	**To**	**Calculation**
DQ	Rising	$V_{OL}(AC)$	$V_{OH}(AC)$	$\frac{V_{OH}(AC) - V_{OL}(AC)}{\Delta TR_{SE}}$
	Falling	$V_{OH}(AC)$	$V_{OL}(AC)$	$\frac{V_{OH}(AC) - V_{OL}(AC)}{\Delta TF_{SE}}$

Figure 33: Nominal Slew Rate Definition for Single-Ended Output Signals



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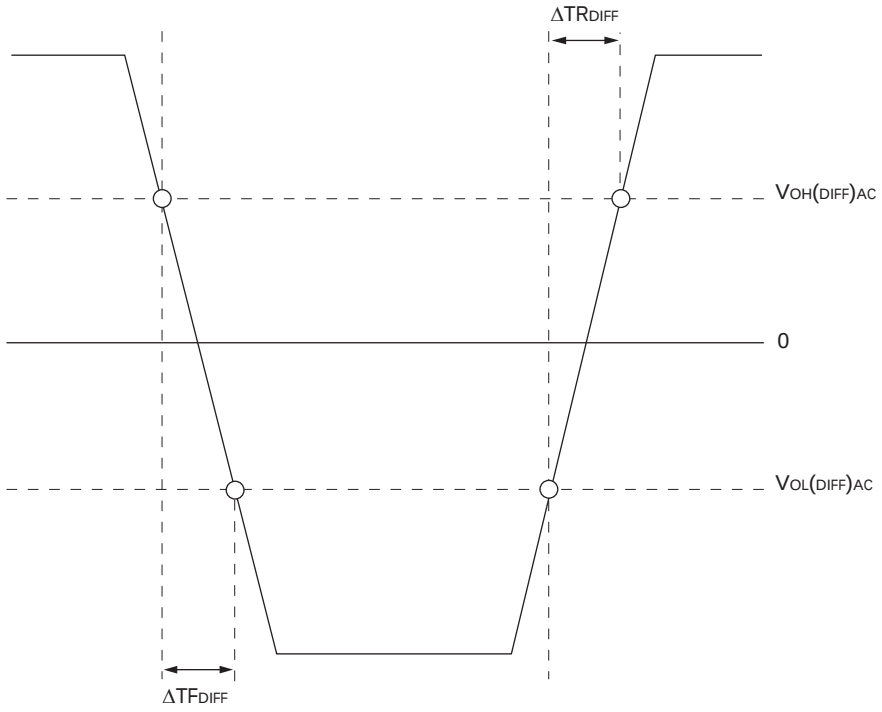
Slew Rate Definitions for Differential Output Signals

The differential output driver is summarized in Table 46 on page 59. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC)$ and $V_{OH}(AC)$ for differential signals, as shown in Table 48 and Figure 34.

Table 48: Differential Output Slew Rate Definition

Differential Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQS, DQS#	Rising	$V_{OLDIFF}(AC)$	$V_{OHDIFF}(AC)$	$\frac{V_{OHDIFF}(AC) - V_{OLDIFF}(AC)}{\Delta TR_{DIFF}}$
	Falling	$V_{OHDIFF}(AC)$	$V_{OLDIFF}(AC)$	$\frac{V_{OHDIFF}(AC) - V_{OLDIFF}(AC)}{\Delta TF_{DIFF}}$

Figure 34: Nominal Differential Output Slew Rate Definition for DQS, DQS#



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Speed Bin Tables

Table 49: DDR3-800 Speed Bins

DDR3-800 Speed Bin			-25E		-25			
CL-^{t}RCD-^{t}RP			5-5-5		6-6-6			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	12.5	–	15	–	ns	
PRECHARGE command period		^{t}RP	12.5	–	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	50	–	52.5	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	37.5	9 × ^{t}REFI	37.5	9 × ^{t}REFI	ns	1
CL = 5	CWL = 5	^{t}CK (AVG)	2.5	3.3	Reserved		ns	2, 3
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	2.5	3.3	ns	2
Supported CL settings			5, 6		6		CK	
Supported CWL settings			5		5		CK	

Notes:
1. ^{t}REFI depends on T_{OPER}.
2. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved settings are not allowed.

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Table 50: DDR3-1066 Speed Bins

DDR3-1066 Speed Bin			-187E		-187			
CL-^{t}RCD-^{t}RP			7-7-7		8-8-8			
Parameter		Symbol	Min	Max	Min	Max	Units	Notes
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.125	–	15	–	ns	
PRECHARGE command period		^{t}RP	13.125	–	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	50.625	–	52.5	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	37.5	9 × ^{t}REFI	37.5	9 × ^{t}REFI	ns	1
CL = 5	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		ns	2, 3
	CWL = 6	^{t}CK (AVG)	Reserved		Reserved		ns	3
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	2.5	3.3	ns	2
	CWL = 6	^{t}CK (AVG)	Reserved		Reserved		ns	2, 3
CL = 7	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	Reserved		ns	2, 3
CL = 8	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	1.875	<2.5	ns	2
Supported CL settings			6, 7, 8		6, 8		CK	
Supported CWL settings			5, 6		5, 6		CK	

Notes:
1. ^{t}REFI depends on T_{OPER}.
2. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved settings are not allowed.

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Table 51: DDR3-1333 Speed Bins

DDR3-1333 Speed Bin			-15F		-15E		-15			
CL-^{t}RCD-^{t}RP			8-8-8		9-9-9		10-10-10			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	12	–	13.5	–	15	–	ns	
PRECHARGE command period		^{t}RP	12	–	13.5	–	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	48	–	49.5	–	51	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	36	9 × ^{t}REFI	36	9 × ^{t}REFI	36	9 × ^{t}REFI	ns	1
CL = 5	CWL = 5	^{t}CK (AVG)	2.5	3.3	Reserved		Reserved		ns	2, 3
	CWL = 6, 7	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	2.5	3.3	2.5	3.3	ns	2
	CWL = 6	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	2, 3
	CWL = 7	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
CL = 7	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	1.875	<2.5	Reserved		ns	2, 3
	CWL = 7	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	2, 3
CL = 8	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	2
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	Reserved		Reserved		ns	2, 3
CL = 9	CWL = 5, 6	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	1.5	<1.875	Reserved		ns	2, 3
CL = 10	CWL = 5, 6	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	2
Supported CL settings			5, 6, 7, 8, 9, 10		6, 7, 8, 9, 10		6, 8, 10		CK	
Supported CWL settings			5, 6, 7		5, 6, 7		5, 6, 7		CK	

Notes:
1. ^{t}REFI depends on T_{OPER}.
2. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved settings are not allowed.

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Table 52: DDR3-1600 Speed Bins

DDR3-1600 Speed Bin			-125F		-125E		-125			
CL-^{t}RCD-^{t}RP			9-9-9		10-10-10		11-11-11			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	11.25	–	12.5	–	13.75	–	ns	
PRECHARGE command period		^{t}RP	11.25	–	12.5	–	13.75	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	46.25	–	47.5	–	48.75	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	35	9 × ^{t}REFI	35	9 × ^{t}REFI	35	9 × ^{t}REFI	ns	1
CL = 5	CWL = 5	^{t}CK (AVG)	2.5	3.3	2.5	3.3	Reserved		ns	2, 3
	CWL = 6, 7, 8	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	2.5	3.3	2.5	3.3	ns	2
	CWL = 6	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	2, 3
	CWL = 7, 8	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
CL = 7	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	1.875	<2.5	Reserved		ns	2, 3
	CWL = 7	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	2, 3
	CWL = 8	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
CL = 8	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	2
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	Reserved		Reserved		ns	2, 3
	CWL = 8	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	2, 3
CL = 9	CWL = 5, 6	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	1.5	<1.875	Reserved		ns	2, 3
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	Reserved		Reserved		ns	2, 3
CL = 10	CWL = 5, 6	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	2
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	1.25	<1.5	Reserved		ns	2, 3
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns	3
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns	2
Supported CL settings			5, 6, 7, 8, 9, 10, 11		5, 6, 7, 8, 9, 10, 11		6, 8, 10, 11		CK	
Supported CWL settings			5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		CK	

Notes:
1. ^{t}REFI depends on T_{OPER}.
2. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved settings are not allowed.

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Table 53: Electrical Characteristics and AC Operating Conditions (Sheet 1 of 7)
Notes: 1–8 apply to the entire table; notes appear on page 74

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing												
Clock period average: DLL disable mode	T_C = 0°C to 85°C	$^tCK_{DLL_DIS}$	8	7,800	8	7,800	8	7,800	8	7,800	ns	9
	T_C = >85°C to 95°C		8	3,900	8	3,900	8	3,900	8	3,900	ns	
Clock period average: DLL enable mode		^tCK (AVG)	See "Speed Bin Tables" on page 63 for ^tCK range allowed								ns	10, 11
High pulse width average		^tCH (AVG)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		^tCL (AVG)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Clock period jitter	DLL locked	$^tJIT_{PER}$	–100	100	–90	90	–80	80	–70	70	ps	13
	DLL locking	$^tJIT_{PER,\ LCK}$	–90	90	–80	80	–70	70	–60	60	ps	13
Clock absolute period		$^tCK(ABS)$	MIN = ^tCK (AVG) MIN + $^tJIT_{PER}$ MIN; MAX = ^tCK (AVG) MAX + $^tJIT_{PER}$ MAX								ps	
Clock absolute high pulse width		^tCH (ABS)	0.43	–	0.43	–	0.43	–	0.43	–	^tCK (AVG)	14
Clock absolute low pulse width		^tCL (ABS)	0.43	–	0.43	–	0.43	–	0.43	–	^tCK (AVG)	15
Cycle-to-cycle jitter	DLL locked	$^tJIT_{CC}$	200		180		160		140		ps	16
	DLL locking	$^tJIT_{CC,\ LCK}$	180		160		140		120		ps	16
Cumulative error across	2 cycles	$^tERR_{2PER}$	–147	147	–132	132	–118	118	–103	103	ps	17
	3 cycles	$^tERR_{3PER}$	–175	175	–157	157	–140	140	–122	122	ps	17
	4 cycles	$^tERR_{4PER}$	–194	194	–175	175	–155	155	–136	136	ps	17
	5 cycles	$^tERR_{5PER}$	–209	209	–188	188	–168	168	–147	147	ps	17
	6 cycles	$^tERR_{6PER}$	–222	222	–200	200	–177	177	–155	155	ps	17
	7 cycles	$^tERR_{7PER}$	–232	232	–209	209	–186	186	–163	163	ps	17
	8 cycles	$^tERR_{8PER}$	–241	241	–217	217	–193	193	–169	169	ps	17
	9 cycles	$^tERR_{9PER}$	–249	249	–224	224	–200	200	–175	175	ps	17
	10 cycles	$^tERR_{10PER}$	–257	257	–231	231	–205	205	–180	180	ps	17
	11 cycles	$^tERR_{11PER}$	–263	263	–237	237	–210	210	–184	184	ps	17
	12 cycles	$^tERR_{12PER}$	–269	269	–242	242	–215	215	–188	188	ps	17
	n = 13, 14 . . . 49, 50 cycles	$^tERR_{nPER}$	$^tERRnPER$ MIN = (1 + 0.68ln[n]) × $^tJIT_{PER}$ MIN $^tERRnPER$ MAX = (1 + 0.68ln[n]) × $^tJIT_{PER}$ MAX								ps	17

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Table 53: Electrical Characteristics and AC Operating Conditions (Sheet 2 of 7)
Notes: 1–8 apply to the entire table; notes appear on page 74

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DQ Input Timing												
Data setup time to DQS, DQS#	Base (specification)	^{t}DS AC175	75	–	25	–	–	–	–	–	ps	18, 19
	VREF @ 1 V/ns		250	–	200	–	–	–	–	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	^{t}DH AC175	150	–	100	–	–	–	–	–	ps	18,19
	VREF @ 1 V/ns		250	–	200	–	–	–	–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	^{t}DS AC150	–	–	–	–	30	–	10	–	ps	18, 19, 21
	VREF @ 1 V/ns		–	–	–	–	180	–	160	–	ps	19, 20,21
Data hold time from DQS, DQS#	Base (specification)	^{t}DH AC150	–	–	–	–	65	–	45	–	ps	18, 19, 21
	VREF @ 1 V/ns		–	–	–	–	165	–	145	–	ps	19, 20, 21
Minimum data pulse width		^{t}DIPW	600	–	490	–	400	–	360	–	ps	42
DQ Output Timing												
DQS, DQS# to DQ skew, per access		^{t}DQSQ	–	200	–	150	–	125	–	100	ps	
DQ output hold time from DQS, DQS#		^{t}QH	0.38	–	0.38	–	0.38	–	0.38	–	^{t}CK (AVG)	22
DQ Low-Z time from CK, CK#		^{t}LZ (DQ)	–800	400	–600	300	–500	250	–450	225	ps	23, 24
DQ High-Z time from CK, CK#		^{t}HZ (DQ)	–	400	–	300	–	250	–	225	ps	23, 24
DQ Strobe Input Timing												
DQS, DQS# rising to CK, CK# rising		^{t}DQSS	–0.25	0.25	–0.25	0.25	–0.25	0.25	–0.27	0.27	CK	26
DQS, DQS# differential input low pulse width		^{t}DQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		^{t}DQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		^{t}DSS	0.2	–	0.2	–	0.2	–	0.18	–	CK	26
DQS, DQS# falling hold from CK, CK# rising		^{t}DSH	0.2	–	0.2	–	0.2	–	0.18	–	CK	26
DQS, DQS# differential WRITE preamble		^{t}WPRE	0.9	–	0.9	–	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		^{t}WPST	0.3	–	0.3	–	0.3	–	0.3	–	CK	

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Table 53: Electrical Characteristics and AC Operating Conditions (Sheet 3 of 7)
Notes: 1–8 apply to the entire table; notes appear on page 74

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DQ Strobe Output Timing											
DQS, DQS# rising to/from rising CK, CK#	^{t}DQSCK	–400	400	–300	300	–255	255	–225	225	ps	24
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled	^{t}DQSCK DLL_DIS	1	10	1	10	1	10	1	10	ns	27
DQS, DQS# differential output high time	^{t}QSH	0.38	–	0.38	–	0.40	–	0.40	–	CK	22
DQS, DQS# differential output low time	^{t}QSL	0.38	–	0.38	–	0.40	–	0.40	–	CK	22
DQS, DQS# Low-Z time (RL - 1)	^{t}LZ (DQS)	–800	400	–600	300	–500	250	–450	225	ps	23, 24
DQS, DQS# High-Z time (RL + BL/2)	^{t}HZ (DQS)	–	400	–	300	–	250	–	225	ps	23, 24
DQS, DQS# differential READ preamble	^{t}RPRE	0.9	Note 25	0.9	Note 25	0.9	Note 25	0.9	Note 25	CK	24, 25
DQS, DQS# differential READ postamble	^{t}RPST	0.3	Note 28	0.3	Note 28	0.3	Note 28	0.3	Note 28	CK	24, 28

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Table 53: Electrical Characteristics and AC Operating Conditions (Sheet 4 of 7)
Notes: 1–8 apply to the entire table; notes appear on page 74

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Command and Address Timing												
DLL locking time		^{t}DLLK	512	–	512	–	512	–	512	–	CK	29
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	^{t}IS AC175	200	–	125	–	65	–	45	–	ps	30, 31
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	ps	20, 31
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	^{t}IH	275	–	200	–	140	–	120	–	ps	30, 31
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	ps	20, 31
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	^{t}IS AC150	–	–	–	–	190	–	170	–	ps	21, 30, 31
	V_{REF} @ 1 V/ns		–	–	–	–	340	–	320	–	ps	20, 21, 31
Minimum CTRL, CMD, ADDR pulse width		^{t}IPW	900	–	780	–	620	–	560	–	ps	42
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See "Speed Bin Tables" on page 63 for ^{t}RCD								ns	32
PRECHARGE command period		^{t}RP	See "Speed Bin Tables" on page 63 for ^{t}RP								ns	32
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See "Speed Bin Tables" on page 63 for ^{t}RAS								ns	32, 33
ACTIVATE-to-ACTIVATE command period		^{t}RC	See "Speed Bin Tables" on page 63 for ^{t}RC								ns	32
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	^{t}RRD	MIN = greater of 4CK or 10ns		MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 6ns		CK	32
	2KB page size		MIN = greater of 4CK or 10ns				MIN = greater of 4CK or 7.5ns				CK	32
Four ACTIVATE windows for 1KB page size		^{t}FAW	40	–	37.5	–	30	–	30	–	ns	32
Four ACTIVATE windows for 2KB page size			50	–	50	–	45	–	40	–	ns	32
Write recovery time		^{t}WR	MIN = 15ns; MAX = n/a								ns	32, 33, 34
Delay from start of internal WRITE transaction to internal READ command		^{t}WTR	MIN = greater of 4CK or 7.5ns; MAX = n/a								CK	32, 35
READ-to-PRECHARGE time		^{t}RTP	MIN = greater of 4CK or 7.5ns; MAX = n/a								CK	32, 33
CAS#-to-CAS# command delay		^{t}CCD	MIN = 4CK; MAX = n/a								CK	
Auto precharge write recovery + precharge time		^{t}DAL	MIN = WR + ^{t}RP/^{t}CK (AVG); MAX = n/a								CK	
MODE REGISTER SET command cycle time		^{t}MRD	MIN = 4CK; MAX = n/a								CK	
MODE REGISTER SET command update delay		^{t}MOD	MIN = greater of 12CK or 15ns; MAX = n/a								CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^{t}MPRR	MIN = 1CK; MAX = n/a								CK	

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Table 53: Electrical Characteristics and AC Operating Conditions (Sheet 5 of 7)
Notes: 1–8 apply to the entire table; notes appear on page 74

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Calibration Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	$^{t}ZQINIT$	512	–	512	–	512	–	512	–	CK	
	Normal operation	$^{t}ZQOPER$	256	–	256	–	256	–	256	–	CK	
ZQCS command: Short calibration time		$^{t}ZQCS$	64	–	64	–	64	–	64	–	CK	
Initialization and Reset Timing												
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = n/a								CK	
Begin power supply ramp to power supplies stable		$^{t}VDDPR$	MIN = n/a; MAX = 200								ms	
RESET# LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 200								ms	
RESET# LOW to I/O and RTT High-Z		^{t}IOz	MIN = n/a; MAX = 20								ns	36
Refresh Timing												
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC	MIN = 110; MAX = 9 × $^{t}REFI$ (REFRESH-to-REFRESH command period)								ns	
Maximum refresh period	T_C = 0°C to 85°C	–	64 (1X)								ms	37
	T_C = >85°C to 95°C		32 (2X)								ms	37
Maximum average periodic refresh	T_C = 0°C to 85°C	$^{t}REFI$	7.8 (64ms/8,192)								µs	37
	T_C = >85°C to 95°C		3.9 (32ms/8,192)								µs	37
Self Refresh Timing												
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = n/a								CK	
Exit self refresh to commands requiring a locked DLL		$^{t}XSDLL$	MIN = $^{t}DLLK$ (MIN); MAX = n/a								CK	29
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		$^{t}CKESR$	MIN = ^{t}CKE (MIN) + CK; MAX = n/a								CK	
Valid clocks after self refresh entry or power-down entry		$^{t}CKSRE$	MIN = greater of 5CK or 10ns; MAX = n/a								CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		$^{t}CKSRX$	MIN = greater of 5CK or 10ns; MAX = n/a								CK	

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Table 53: Electrical Characteristics and AC Operating Conditions (Sheet 6 of 7)
Notes: 1–8 apply to the entire table; notes appear on page 74

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Power-Down Timing												
CKE MIN pulse width		^{t}CKE (MIN)	Greater of 3CK or 7.5ns		Greater of 3CK or 5.625ns		Greater of 3CK or 5.625ns		Greater of 3CK or 5ns		CK	
Command pass disable delay		^{t}CPDED	MIN = 1; MAX = n/a								CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 × ^{t}REFI								CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL - 1CK								CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time								CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^{t}ANPD + ^{t}XPDLL								CK	
Power-Down Entry Minimum Timing												
ACTIVATE command to power-down entry		^{t}ACTPDEN	MIN = 1								CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	MIN = 1								CK	
REFRESH command to power-down entry		^{t}REFPDEN	MIN = 1								CK	38
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)								CK	
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1								CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)								CK	
	BC4MRS	^{t}WRPDEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)								CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAPDEN	MIN = WL + 4 + WR + 1								CK	
	BC4MRS	^{t}WRAPDEN	MIN = WL + 2 + WR + 1								CK	
Power-Down Exit Timing												
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 7.5ns; MAX = n/a				MIN = greater of 3CK or 6ns; MAX = n/a				CK	
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = n/a								CK	29

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Table 53: Electrical Characteristics and AC Operating Conditions (Sheet 7 of 7)
Notes: 1–8 apply to the entire table; notes appear on page 74

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
ODT Timing											
RTT synchronous turn-on delay	ODTL on	CWL + AL - 2CK								CK	39
RTT synchronous turn-off delay	ODTL off	CWL + AL - 2CK								CK	41
RTT turn-on from ODTL on reference	^{t}AON	–400	400	–300	300	–250	250	–225	225	ps	24, 39
RTT turn-off from ODTL off reference	^{t}AOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	40, 41
Asynchronous RTT turn-on delay (power-down with DLL off)	^{t}AONPD	MIN = 1; MAX = 9								ns	39
Asynchronous RTT turn-off delay (power-down with DLL off)	^{t}AOFPD	MIN = 1; MAX = 9								ns	41
ODT HIGH time with WRITE command and BL8	ODTH8	MIN = 6; MAX = n/a								CK	
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = n/a								CK	
Dynamic ODT Timing											
RTT_NOM-to-RTT_WR change skew	ODTLCNW	WL - 2CK								CK	
RTT_WR-to-RTT_NOM change skew - BC4	ODTLCNW4	4CK + ODTL off								CK	
RTT_WR-to-RTT_NOM change skew - BL8	ODTLCNW8	6CK + ODTL off								CK	
RTT dynamic change skew	^{t}ADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	40
Write Leveling Timing											
First DQS, DQS# rising edge	^{t}WLMRD	40	–	40	–	40	–	40	–	CK	
DQS, DQS# delay	^{t}WLDQSEN	25	–	25	–	25	–	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	^{t}WLS	325	–	245	–	195	–	163	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	^{t}WLH	325	–	245	–	195	–	163	–	ps	
Write leveling output delay	^{t}WLO	0	9	0	9	0	9	0	7.5	ns	
Write leveling output error	^{t}WLOE	0	2	0	2	0	2	0	2	ns	

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Notes

1. Parameters are applicable with $0°C \le T_C \le +95°C$ and V_{DD}/V_{DDQ} = +1.5V ±0.075V.
2. All voltages are referenced to V_{SS}.
3. Output timings are only valid for RON_{34} output buffer selection.
4. Unit "^tCK (AVG)" represents the actual ^tCK (AVG) of the input clock under operation. Unit "CK" represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except ^tIS, ^tIH, ^tDS, and ^tDH use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between $V_{IL}(AC)$ and $V_{IH}(AC)$.
6. All timings that use time-based values (ns, µs, ms) should use ^tCK (AVG) to determine the correct number of clocks (Table 53 on page 67 uses "CK" or "^tCK [AVG]" interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. The use of "strobe" or "DQS_{DIFF}" refers to the DQS and DQS# differential crossing point when DQS is the rising edge. The use of "clock" or "CK" refers to the CK and CK# differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is $V_{DDQ}/2$ for single-ended signals and the crossing point for differential signals (see Figure 32 on page 60).
9. When operating in DLL disable mode, Micron does not warrant compliance with normal mode timings or functionality.
10. The clock's ^tCK (AVG) is the average clock over any 200 consecutive clocks and ^tCK(AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1 percent of ^tCK (AVG) as a long-term jitter component; however, the spread-spectrum may not use a clock rate below ^tCK (AVG) MIN.
12. The clock's ^tCH (AVG) and ^tCL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (^tJITPER) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. ^tCH(ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. ^tCL(ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter (^tJITCC) is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.

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17. The cumulative jitter error (^{t}ERR*n*PER), where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.
18. ^{t}DS (base) and ^{t}DH (base) values are for a single-ended 1 V/ns DQ slew rate and 2 V/ns differential DQS, DQS# slew rate.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to VREF when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. Special setup and hold derating and different ^{t}VAC numbers apply when using 150mV AC threshold.
22. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JITPER of the input clock (output deratings are relative to the SDRAM input clock).
23. Single-ended signal parameter.
24. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting $^{t}ERR_{10PER}$ (MAX): ^{t}DQSCK (MIN), ^{t}LZ (DQS) MIN, ^{t}LZ (DQ) MIN, and ^{t}AON (MIN). The following parameters are required to be derated by subtracting $^{t}ERR_{10PER}$ (MIN): ^{t}DQSCK (MAX), ^{t}HZ (MAX), ^{t}LZ (DQS) MAX, ^{t}LZ (DQ) MAX, and ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITPER (MAX), while ^{t}RPRE (MAX) is derated by subtracting ^{t}JITPER (MIN).
25. The maximum preamble is bound by ^{t}LZDQS (MAX).
26. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
27. The ^{t}DQSCK DLL_DIS parameter begins CL + AL - 1 cycles after the READ command.
28. The maximum postamble is bound by ^{t}HZDQS (MAX).
29. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency ^{t}XPDLL, timing must be met.
30. ^{t}IS (base) and ^{t}IH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK# differential slew rate.
31. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
32. For these parameters, the DDR3 SDRAM device supports ^{t}nPARAM (*n*CK) = RU(^{t}PARAM [ns]/^{t}CK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}nRP (*n*CK) = RU(^{t}RP/^{t}CK[AVG]) if all input clock jitter specifications are met. This means for DDR3-800 6-6-6, of which ^{t}RP = 15ns, the device will support ^{t}nRP = RU(^{t}RP/^{t}CK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
33. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.

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34. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for ^{t}WR.
35. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS and OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
36. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
37. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands must be asserted at least once every 70.3µs.
38. Although CKE is allowed to be registered LOW after a REFRESH command when ^{t}REFPDEN (MIN) is satisfied, there are cases where additional time such as ^{t}XPDLL (MIN) is required.
39. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown in Figure 24 on page 49.
40. Half-clock output parameters must be derated by the actual $^{t}ERR_{10PER}$ and $^{t}JITDTY$ when input clock jitter is present. This results in each parameter becoming larger. The parameters ^{t}ADC (MIN) and ^{t}AOF (MIN) are each required to be derated by subtracting both $^{t}ERR_{10PER}$ (MAX) and $^{t}JITDTY$ (MAX). The parameters ^{t}ADC (MAX) and ^{t}AOF (MAX) are required to be derated by subtracting both $^{t}ERR_{10PER}$ (MAX) and $^{t}JITDTY$ (MAX).
41. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown in Figure 25 on page 51. This output load is used for ODT timings (see Figure 32 on page 60).
42. Pulse width of a input signal is defined as the width between the first crossing of V_{REF}(DC) and the consecutive crossing of V_{REF}(DC).

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Command and Address Setup, Hold, and Derating

The total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated by adding the data sheet ^{t}IS (base) and ^{t}IH (base) values (see Table 54; values come from Table 53 on page 67) to the Δ^{t}IS and Δ^{t}IH derating values (see Table 55 on page 78 and Table 56 on page 78), respectively. Example: ^{t}IS (total setup time) = ^{t}IS (base) + Δ^{t}IS. For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for some time ^{t}VAC (see Table 56 on page 78).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH[AC]/VIL[AC] at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/VIL(AC) (see Figure 17 on page 42 for input signal requirements). For slew rates which fall between the values listed in Table 56 on page 78 and Table 57 on page 79, the derating values may be obtained by linear interpolation.

Setup (^{t}IS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC) MIN. Setup (^{t}IS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC) MAX. If the actual signal is always earlier than the nominal slew rate line between the shaded "VREF(DC)-to-AC region," use the nominal slew rate for derating value (see Figure 35 on page 80). If the actual signal is later than the nominal slew rate line anywhere between the shaded "VREF(DC)-to-AC region," the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 37 on page 82).

Hold (^{t}IH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC) MAX and the first crossing of VREF(DC). Hold (^{t}IH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC) MIN and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between the shaded "DC-to-VREF(DC) region," use the nominal slew rate for derating value (see Figure 36 on page 81). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded "DC-to-VREF(DC) region," the slew rate of a tangent line to the actual signal from the DC level to the VREF(DC) level is used for derating value (see Figure 38 on page 83).

Table 54: Command and Address Setup and Hold Values Referenced at 1 V/ns – AC/DC-Based

Symbol	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units	Reference
^{t}IS (base)	200	125	65	45	ps	VIH(AC)/VIL(AC)
^{t}IH (base)	275	200	140	120	ps	VIH(DC)/VIL(DC)
^{t}IS (base): AC150	n/a	n/a	190	170	ps	VIH(AC)/VIL(AC)

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Table 55: DDR3-800, DDR3-1066, DDR3-1333, and DDR3-1600 Derating Values for $^{t}IS/^{t}IH$ – AC/DC-Based
AC175 threshold

$\Delta^{t}IS$, $\Delta^{t}IH$ Derating (ps) – AC/DC-Based AC175 Threshold: $V_{IH(AC)} = V_{REF(DC)} + 175mV$, $V_{IL(AC)} = V_{REF(DC)} - 175mV$																
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IH$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$
2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–2	–4	–2	–4	–2	–4	6	4	14	12	22	20	30	30	38	46
0.8	–6	–10	–6	–10	–6	–10	2	–2	10	6	18	14	26	24	34	40
0.7	–11	–16	–11	–16	–11	–16	–3	–8	5	0	13	8	21	18	29	34
0.6	–17	–26	–17	–26	–17	–26	–9	–18	–1	–10	7	–2	15	8	23	24
0.5	–35	–40	–35	–40	–35	–40	–27	–32	–19	–24	–11	–16	–2	–6	5	10
0.4	–62	–60	–62	–60	–62	–60	–54	–52	–46	–44	–38	–36	–30	–26	–22	–10

Table 56: DDR3-1333 and DDR3-1600 Derating Values for $^{t}IS/^{t}IH$ – AC/DC-Based
AC150 threshold

$\Delta^{t}IS$, $\Delta^{t}IH$ Derating (ps) – AC/DC-Based AC150 Threshold: $V_{IH(AC)} = V_{REF(DC)} + 150mV$, $V_{IL(AC)} = V_{REF(DC)} - 150mV$																
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IH$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$
2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	0	–4	0	–4	0	–4	8	4	16	12	24	20	32	30	40	46
0.8	0	–10	0	–10	0	–10	8	–2	16	6	24	14	32	24	40	40
0.7	0	–16	0	–16	0	–16	8	–8	16	0	24	8	32	18	40	34
0.6	–1	–26	–1	–26	–1	–26	7	–18	15	–10	23	–2	31	8	39	24
0.5	–10	–40	–10	–40	–10	–40	–2	–32	6	–24	14	–16	22	–6	30	10
0.4	–25	–60	–25	–60	–25	–60	–17	–52	–9	–44	–1	–36	7	–26	15	–10

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Table 57: Minimum Required Time ^{t}VAC Above $V_{IH(AC)}$ for Valid Transition
Below $V_{IL(AC)}$

Slew Rate (V/ns)	^{t}VAC at 175mV (ps)	^{t}VAC at 150mV (ps)
>2.0	75	175
2.0	57	170
1.5	50	167
1.0	38	163
0.9	34	162
0.8	29	161
0.7	22	159
0.6	13	155
0.5	0	150
<0.5	0	150

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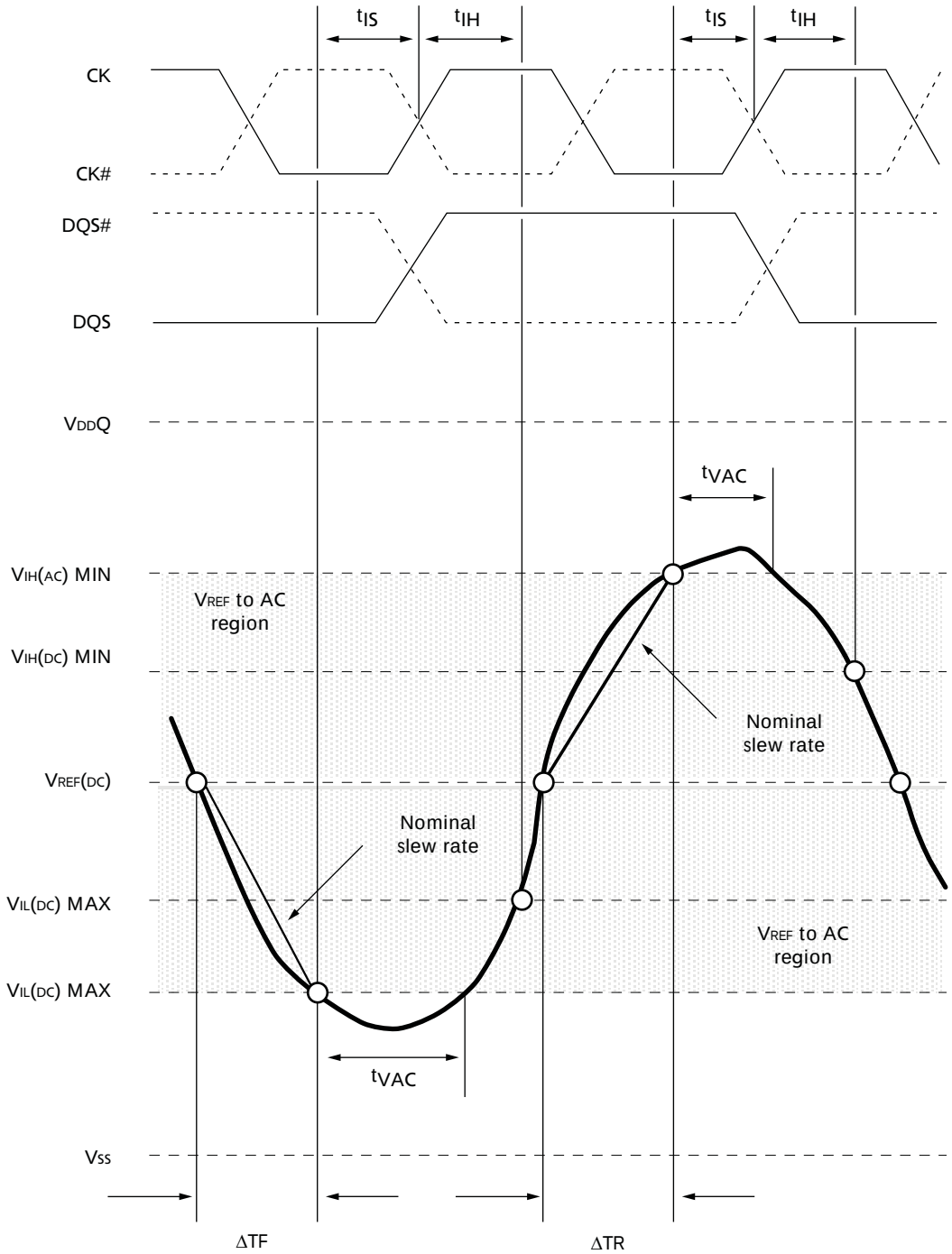
Figure 35: Nominal Slew Rate and ^{t}VAC for ^{t}IS (Command and Address – Clock)



$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)}\ MAX}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{V_{IH(AC)}\ MIN - V_{REF(DC)}}{\Delta TR}$$

Notes: 1. Both the clock and the strobe are drawn on different time scales.

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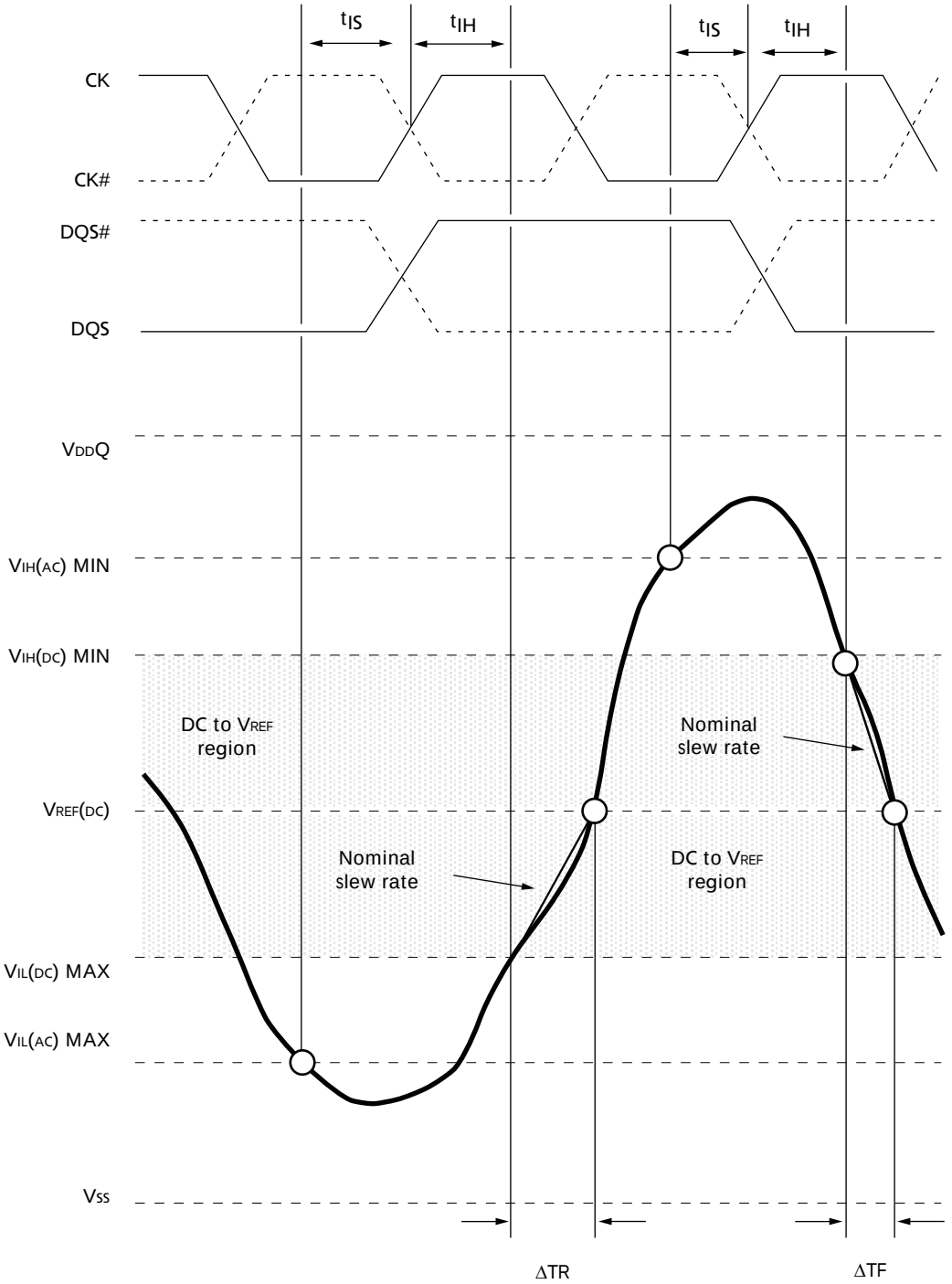
Figure 36: Nominal Slew Rate for ^{t}IH (Command and Address – Clock)



$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)}\ \text{MAX}}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)}\ \text{MIN} - V_{REF(DC)}}{\Delta TF}$$

Notes: 1. Both the clock and the strobe are drawn on different time scales.

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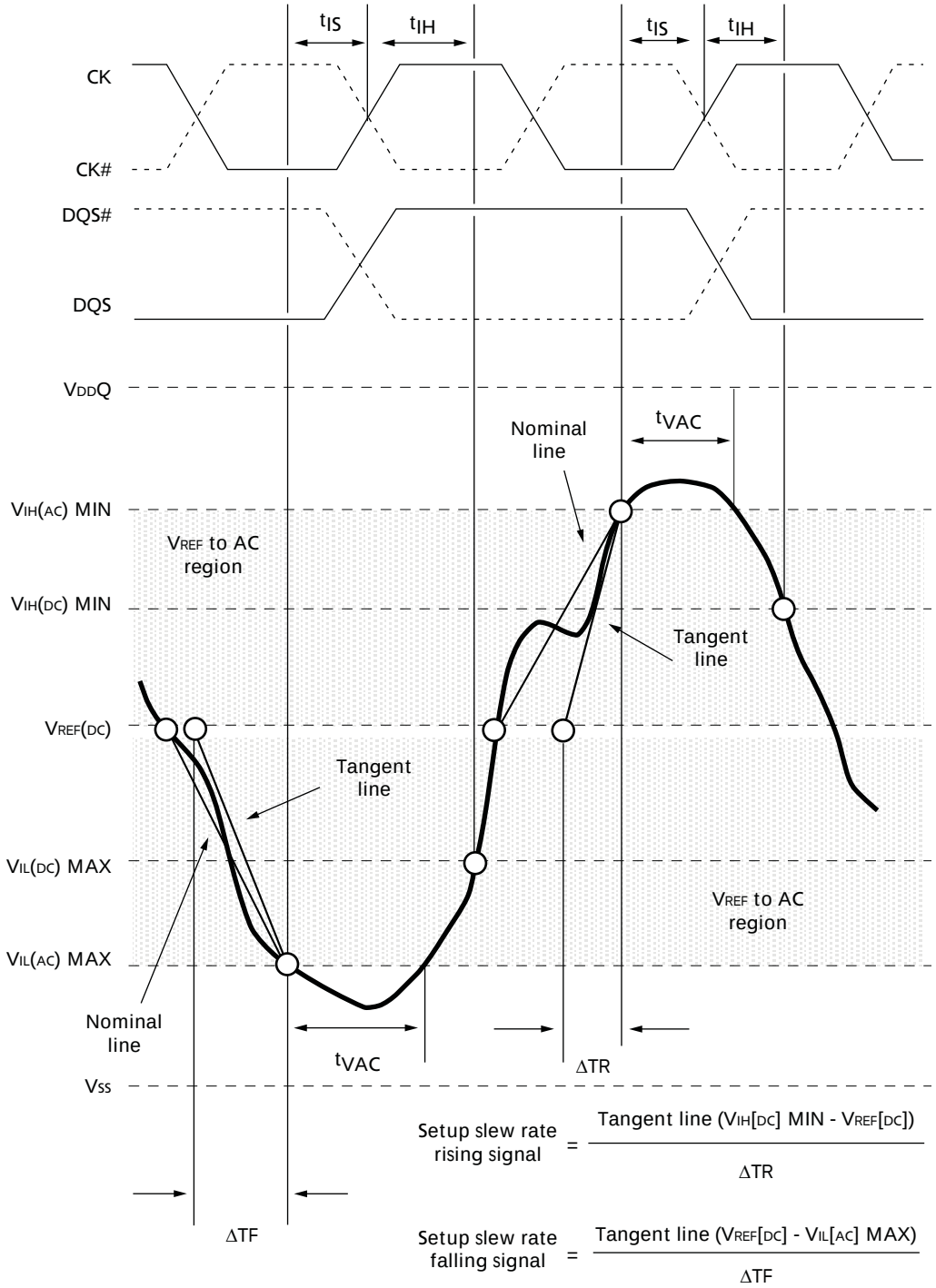
Figure 37: Tangent Line for ^{t}IS (Command and Address – Clock)



Notes: 1. Both the clock and the strobe are drawn on different time scales.

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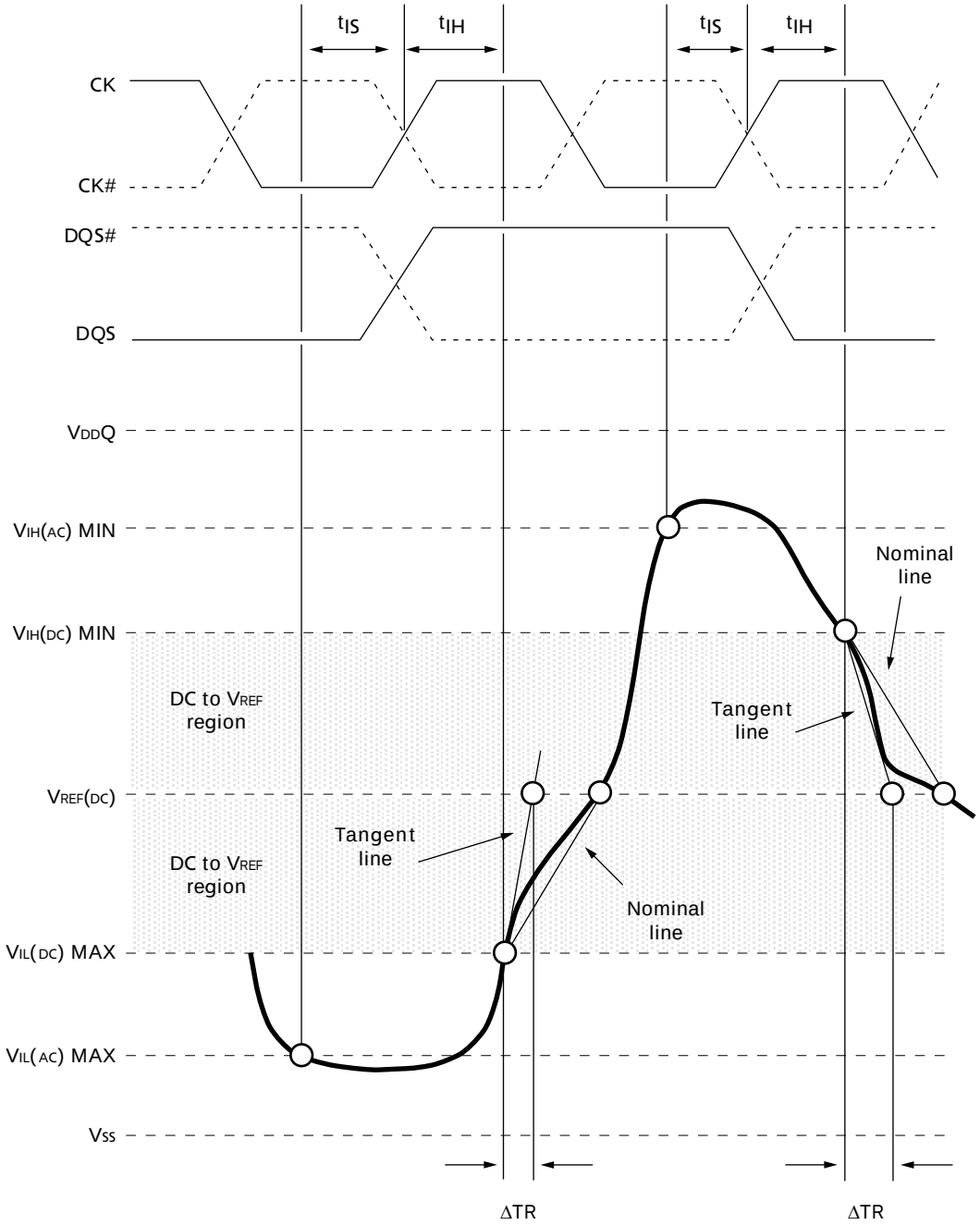
Figure 38: Tangent Line for ^{t}IH (Command and Address – Clock)



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF}[DC] - V_{IL}[DC]\ MAX)}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH}[DC]\ MIN - V_{REF}[DC])}{\Delta TF}$$

Notes: 1. Both the clock and the strobe are drawn on different time scales.

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Data Setup, Hold, and Derating

The total ^{t}DS (setup time) and ^{t}DH (hold time) required is calculated by adding the data sheet ^{t}DS (base) and ^{t}DH (base) values (see Table 58; values come from Table 53 on page 67) to the Δ^{t}DS and Δ^{t}DH derating values (see Table 59 on page 85), respectively. Example: ^{t}DS (total setup time) = ^{t}DS (base) + Δ^{t}DS. For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for some time ^{t}VAC (see Table 61 on page 86).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH[AC]/VIL[AC]) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH/VIL(AC). For slew rates which fall between the values listed in Table 59 on page 85, the derating values may obtained by linear interpolation.

Setup (^{t}DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC) MIN. Setup (^{t}DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC) MAX. If the actual signal is always earlier than the nominal slew rate line between the shaded "VREF(DC)-to-AC region," use the nominal slew rate for derating value (see Figure 39 on page 87). If the actual signal is later than the nominal slew rate line anywhere between the shaded "VREF(DC)-to-AC region," the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 41 on page 89).

Hold (^{t}DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC) MAX and the first crossing of VREF(DC). Hold (^{t}DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC) MIN and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between the shaded "DC-to-VREF(DC) region," use the nominal slew rate for derating value (see Figure 40 on page 88). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded "DC-to-VREF(DC) region," the slew rate of a tangent line to the actual signal from the "DC-to-VREF(DC) region" is used for derating value (see Figure 42 on page 90).

Table 58: Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based

Symbol	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units	Reference
^{t}DS AC175 (base)	75	25	–	–	ps	VIH(AC)/VIL(AC)
^{t}DH AC175 (base)	150	100	–	–	ps	VIH(DC)/VIL(DC)
^{t}DS AC150 (base)	–	–	30	10	ps	VIH(AC)/VIL(AC)
^{t}DH AC150 (base)	–	–	65	45	ps	VIH(DC)/VIL(DC)

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Table 59: DDR3-800, DDR3-1066, DDR3-1333, and DDR3-1600 Derating Values for ^{t}DS/^{t}DH – AC/DC-Based

AC175 threshold; shaded cells indicate slew rate combinations not supported

Δ^{t}DS, Δ^{t}DH Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
2.0	88	50	88	50	88	50										
1.5	59	34	59	34	59	34	67	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			–2	–4	–2	–4	6	4	14	12	22	20				
0.8					–6	–10	2	–2	10	6	18	14	26	24		
0.7							–3	–8	5	0	13	8	21	18	29	34
0.6									–1	–10	7	–2	15	8	23	24
0.5											–11	–16	–2	–6	5	10
0.4													–30	–26	–22	–10

Table 60: DDR3-1333and DDR3-1600 Derating Values for ^{t}DS/^{t}DH – AC/DC-Based

AC150 threshold; shaded cells indicate slew rate combinations not supported

Δ^{t}DS, Δ^{t}DH Derating (ps) – AC/DC-Based																
CMD/ ADDR Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IH	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
2.0	75	50	75	50	75	50										
1.5	50	34	50	34	50	34	58	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			0	–4	0	–4	8	4	16	12	24	20				
0.8					0	–10	8	–2	16	6	24	14	32	24		
0.7							8	–8	16	0	24	8	32	18	40	34
0.6									15	–10	23	–2	31	8	39	24
0.5											14	–16	22	–6	30	10
0.4													7	–26	15	–10

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Table 61: Required Time ^{t}VAC Above V_{IH}(AC) (Below V_{IL}[AC]) for Valid Transition

Slew Rate (V/ns)	^{t}VAC at 175mV (ps)	^{t}VAC at 150mV (ps)
	Min	Min
>2.0	75	175
2.0	57	170
1.5	50	167
1.0	38	163
0.9	34	162
0.8	29	161
0.7	22	159
0.6	13	155
0.5	0	150
<0.5	0	150

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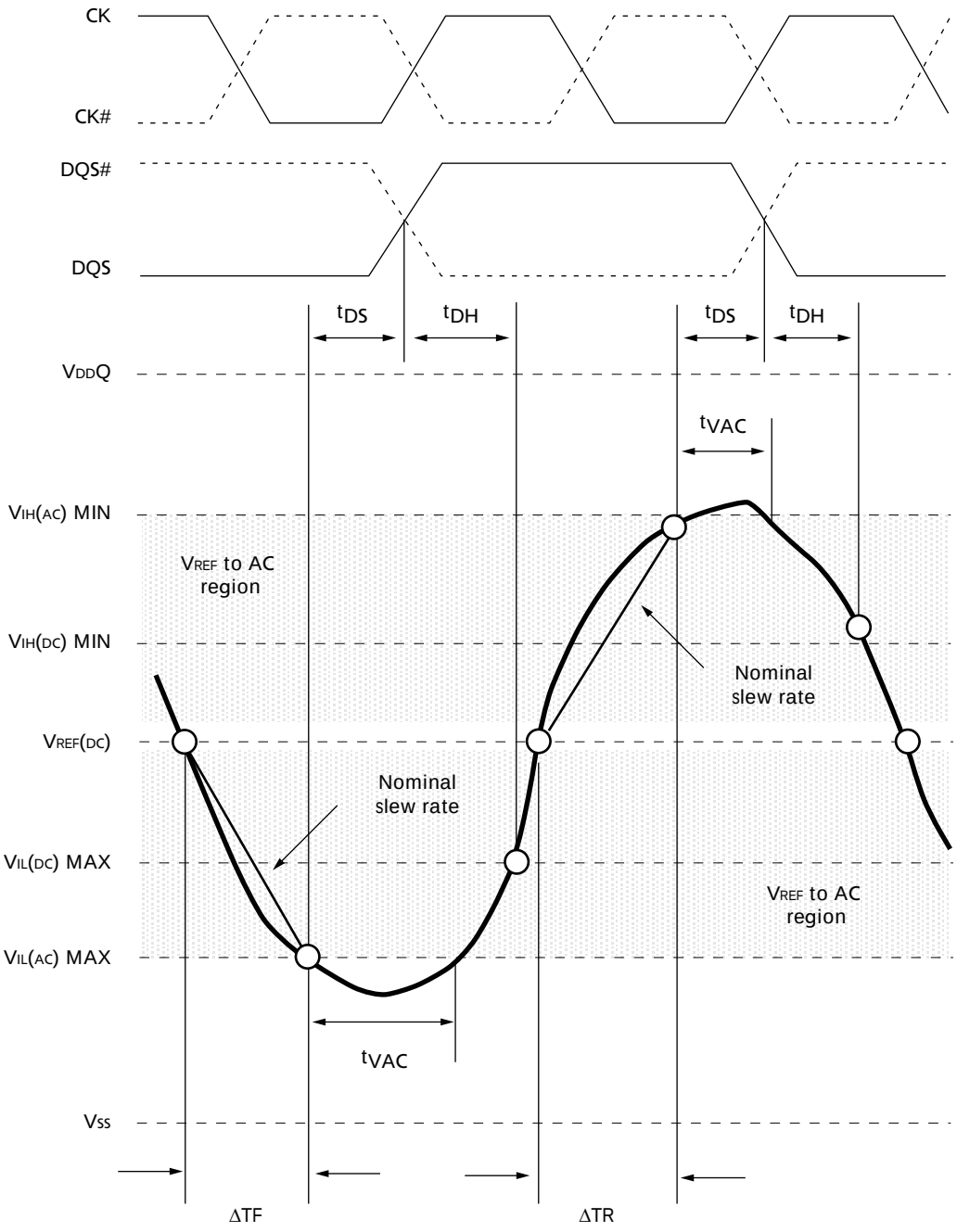
Figure 39: Nominal Slew Rate and ^{t}VAC for ^{t}DS (DQ – Strobe)



$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)}\ MAX}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{V_{IH(AC)}\ MIN - V_{REF(DC)}}{\Delta TR}$$

Notes: 1. Both the clock and the strobe are drawn on different time scales.

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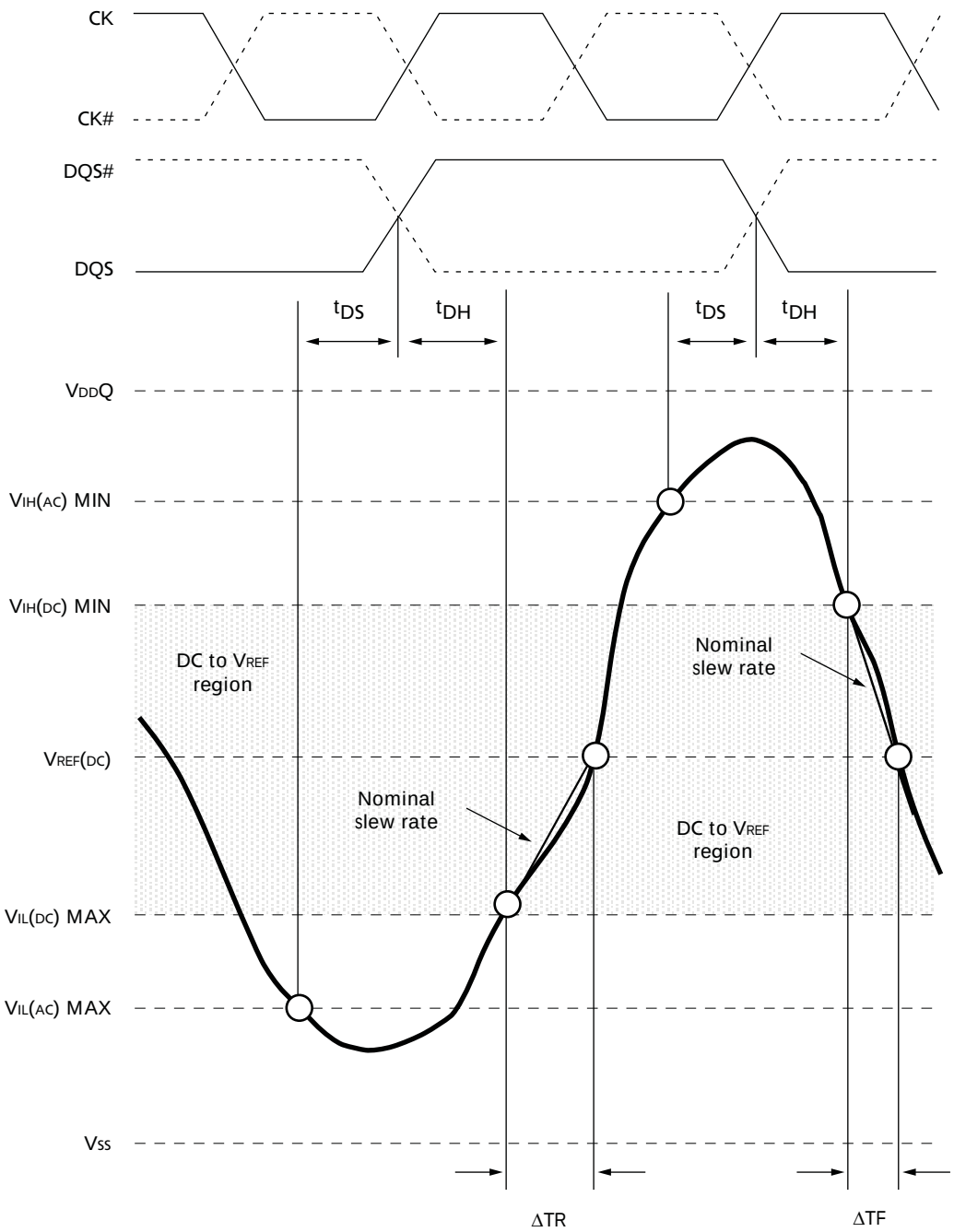
Figure 40: Nominal Slew Rate for ^{t}DH (DQ – Strobe)



$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)}\ MAX}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)}\ MIN - V_{REF(DC)}}{\Delta TF}$$

Notes: 1. Both the clock and the strobe are drawn on different time scales.

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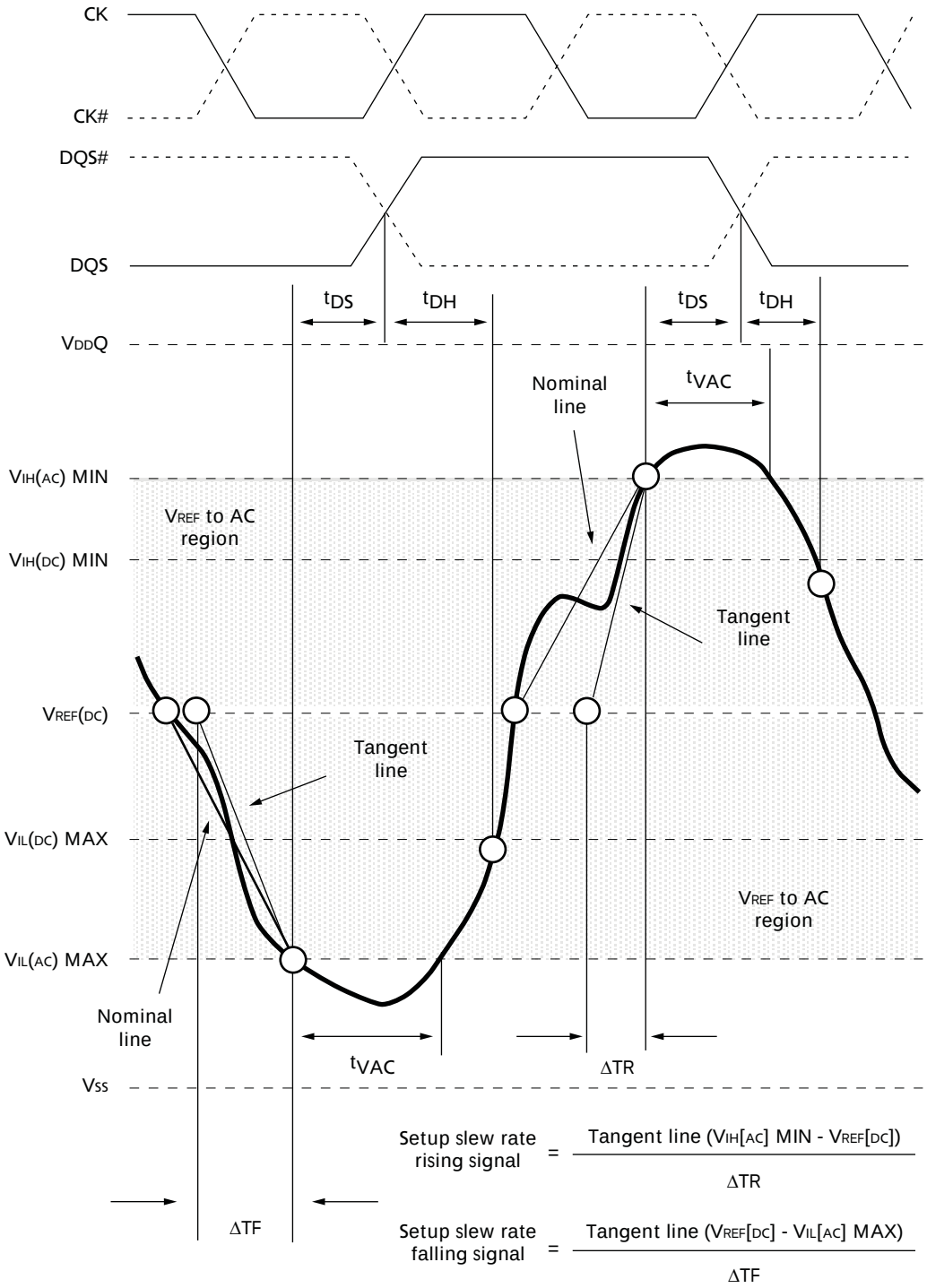
Figure 41: Tangent Line for ^{t}DS (DQ – Strobe)



Notes: 1. Both the clock and the strobe are drawn on different time scales.

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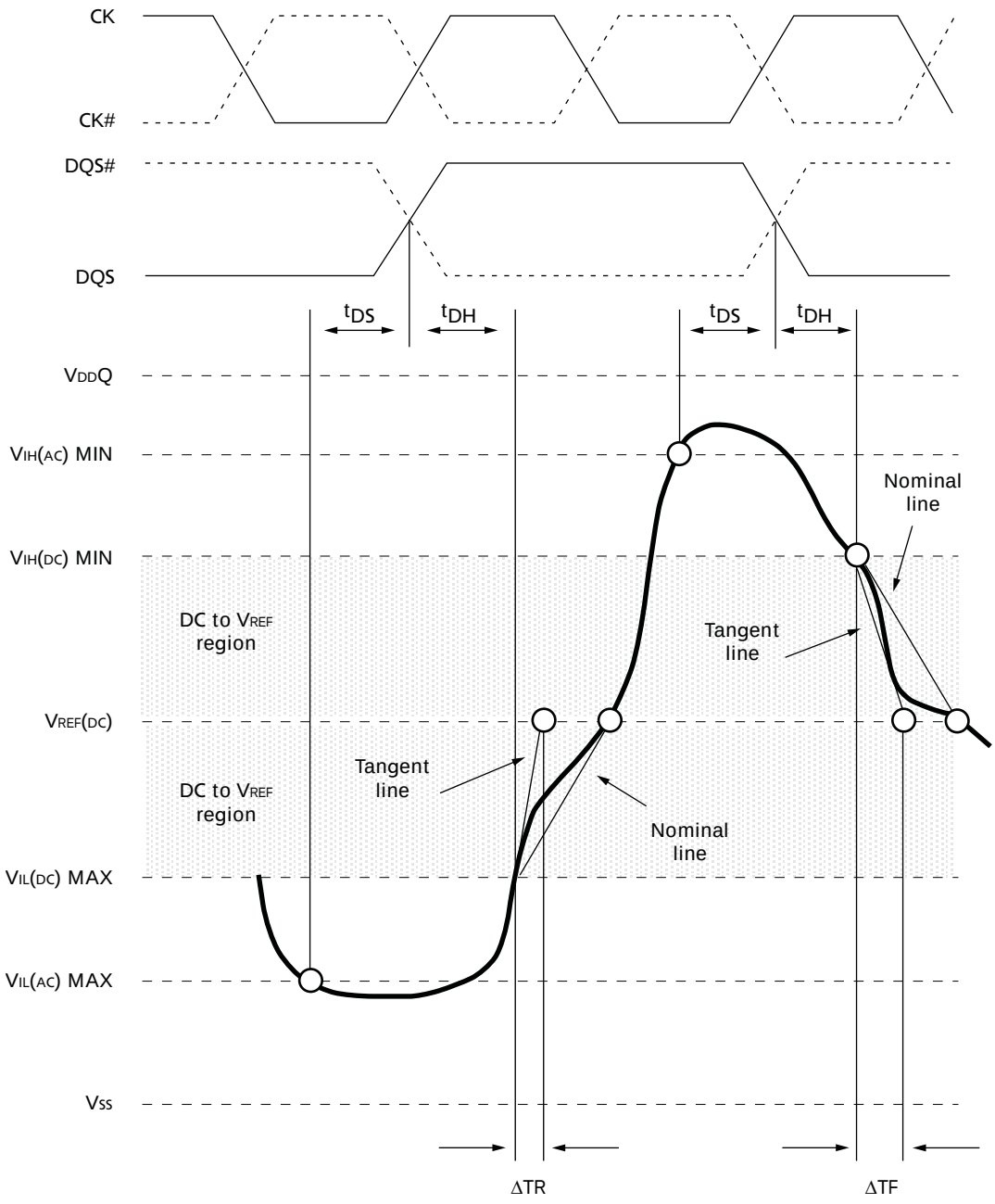
Figure 42: Tangent Line for ^{t}DH (DQ – Strobe)



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF}[DC] - V_{IL}[DC]\ MAX)}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH}[DC]\ MIN - V_{REF}[DC])}{\Delta TF}$$

Notes: 1. Both the clock and the strobe are drawn on different time scales.

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Commands

Truth Tables

Table 62: Truth Table – Command
Notes 1–5 apply to the entire table

Function		Symbol	CKE Prev Cycle	CKE Next Cycle	CS#	RAS#	CAS#	WE#	BA [2:0]	*An*	A12	A10	A[11, 9:0]	Notes
MODE REGISTER SET		MRS	H	H	L	L	L	L	BA	OP code				
REFRESH		REF	H	H	L	L	L	H	V	V	V	V	V	
Self refresh entry		SRE	H	L	L	L	L	H	V	V	V	V	V	6
Self refresh exit		SRX	L	H	H	V	V	V	V	V	V	V	V	6, 7
					L	H	H	H						
Single-bank PRECHARGE		PRE	H	H	L	L	H	L	BA	V	V	L	V	
PRECHARGE all banks		PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank ACTIVATE		ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE	BL8MRS, BC4MRS	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	8
	BC4OTF	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	8
	BL8OTF	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	8
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H	H	L	H	L	L	BA	RFU	V	H	CA	8
	BC4OTF	WRAPS4	H	H	L	H	L	L	BA	RFU	L	H	CA	8
	BL8OTF	WRAPS8	H	H	L	H	L	L	BA	RFU	H	H	CA	8
READ	BL8MRS, BC4MRS	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	8
	BC4OTF	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	8
	BL8OTF	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	8
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H	H	L	H	L	H	BA	RFU	V	H	CA	8
	BC4OTF	RDAPS4	H	H	L	H	L	H	BA	RFU	L	H	CA	8
	BL8OTF	RDAPS8	H	H	L	H	L	H	BA	RFU	H	H	CA	8
NO OPERATION		NOP	H	H	L	H	H	H	V	V	V	V	V	9
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	10
Power-down entry		PDE	H	L	L	H	H	H	V	V	V	V	V	6
					H	V	V	V						
Power-down exit		PDX	L	H	L	H	H	H	V	V	V	V	V	6, 11
					H	V	V	V						
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	L	X	X	X	H	X	12
ZQ CALIBRATION SHORT		ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:
1. Commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-density and configuration-dependent.
2. RESET# is LOW enabled and used only for asynchronous reset. Thus, RESET# must be held HIGH during any normal operation.
3. The state of ODT does not affect the states described in this table.

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4. Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.
5. "V" means "H" or "L" (a defined logic level), and "X" means "Don't Care."
6. See Table 63 for additional information on CKE transition.
7. Self refresh exit is asynchronous.
8. Burst READs or WRITEs cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.
9. The purpose of the NOP command is to prevent the DRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.
10. The DES and NOP commands perform similarly.
11. The power-down mode does not perform any REFRESH operations.
12. ZQ CALIBRATION LONG is used for either ZQINIT (first ZQCL command during initialization) or ZQOPER (ZQCL command after initialization).

Table 63: Truth Table – CKE

Notes 1–2 apply to the entire table; see Table 62 on page 91 for additional command details

Current State[3]	CKE		Command[5] (RAS#, CAS#, WE#, CS#)	Action[5]	Notes
	Previous Cycle[4] (*n* - 1)	Present Cycle[4] (*n*)			
Power-down	L	L	"Don't Care"	Maintain power-down	
	L	H	DES or NOP	Power-down exit	
Self refresh	L	L	"Don't Care"	Maintain self refresh	
	L	H	DES or NOP	Self refresh exit	
Bank(s) active	H	L	DES or NOP	Active power-down entry	
Reading	H	L	DES or NOP	Power-down entry	
Writing	H	L	DES or NOP	Power-down entry	
Precharging	H	L	DES or NOP	Power-down entry	
Refreshing	H	L	DES or NOP	Precharge power-down entry	
All banks idle	H	L	DES or NOP	Precharge power-down entry	6
	H	L	REFRESH	Self refresh	

Notes:
1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
2. ^{t}CKE (MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + ^{t}CKE (MIN) + ^{t}IH.
3. Current state = The state of the DRAM immediately prior to clock edge *n*.
4. CKE (*n*) is the logic state of CKE at clock edge *n*; CKE (*n* - 1) was the state of CKE at the previous clock edge.
5. COMMAND is the command registered at the clock edge (must be a legal command as defined in Table 62 on page 91). Action is a result of COMMAND. ODT does not affect the states described in this table and is not listed.
6. Idle state = All banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied. All self refresh exit and power-down exit parameters are also satisfied.

DESELECT (DES)

The DES command (CS# HIGH) prevents new commands from being executed by the DRAM. Operations already in progress are not affected.

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NO OPERATION (NOP)

The NOP command (CS# LOW) prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

ZQ CALIBRATION

ZQ CALIBRATION LONG (ZQCL)

The ZQCL command is used to perform the initial calibration during a power-up initialization and reset sequence (see Figure 51 on page 107). This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the DRAM I/O, which are reflected as updated R_{ON} and ODT values.

The DRAM is allowed a timing window defined by either $^{t}ZQ_{INIT}$ or $^{t}ZQ_{OPER}$ to perform the full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter $^{t}ZQ_{INIT}$ must be satisfied. When initialization is complete, subsequent ZQCL commands require the timing parameter $^{t}ZQ_{OPER}$ to be satisfied.

ZQ CALIBRATION SHORT (ZQCS)

The ZQCS command is used to perform periodic calibrations to account for small voltage and temperature variations. The shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter $^{t}ZQCS$. A ZQCS command can effectively correct a minimum of 0.5 percent R_{ON} and R_{TT} impedance error within 64 clock cycles, assuming the maximum sensitivities specified in Table 40 on page 56 and Table 41 on page 57.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[*n*:0] selects the row. This row remains open (or active) for accesses until a PRECHARGE command is issued to that bank.

A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The address provided on inputs A[2:0] selects the starting column address depending on the burst length and burst type selected (see Table 68 on page 111 for additional information). The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. The value on input A12 (if enabled in the mode register) when the READ command is issued determines whether BC4 (chop) or BL8 is used. After a READ command is issued, the READ burst may not be interrupted. A summary of READ commands is shown in Table 64 on page 94.

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Table 64: READ Command Summary

Function		Symbol	CKE Previous Cycle	CKE Next Cycle	CS#	RAS#	CAS#	WE#	BA [3:0]	A*n*	A12	A10	A[11, 9:0]
READ	BL8MRS, BC4MRS	RD	H		L	H	L	H	BA	RFU	V	L	CA
	BC4OTF	RDS4	H		L	H	L	H	BA	RFU	L	L	CA
	BL8OTF	RDS8	H		L	H	L	H	BA	RFU	H	L	CA
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H		L	H	L	H	BA	RFU	V	H	CA
	BC4OTF	RDAPS4	H		L	H	L	H	BA	RFU	L	H	CA
	BL8OTF	RDAPS8	H		L	H	L	H	BA	RFU	H	H	CA

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA[2:0] inputs selects the bank. The value on input A10 determines whether or not auto precharge is used. The value on input A12 (if enabled in the MR) when the WRITE command is issued determines whether BC4 (chop) or BL8 is used. The WRITE command summary is shown in Table 65.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored and a WRITE will not be executed to that byte/column location.

Table 65: WRITE Command Summary

Function		Symbol	CKE Prev Cycle	CKE Next Cycle	CS#	RAS#	CAS#	WE#	BA [3:0]	A*n*	A12	A10	A[11, 9:0]
WRITE	BL8MRS, BC4MRS	WR	H		L	H	L	L	BA	RFU	V	L	CA
	BC4OTF	WRS4	H		L	H	L	L	BA	RFU	L	L	CA
	BL8OTF	WRS8	H		L	H	L	L	BA	RFU	H	L	CA
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H		L	H	L	L	BA	RFU	V	H	CA
	BC4OTF	WRAPS4	H		L	H	L	L	BA	RFU	L	H	CA
	BL8OTF	WRAPS8	H		L	H	L	L	BA	RFU	H	H	CA

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or in all banks. The bank(s) are available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge. A READ or WRITE command to a different bank is allowed during concurrent auto precharge as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are precharged. In the case where only one bank is precharged, inputs BA[2:0] select the bank; otherwise, BA[2:0] are treated as “Don’t Care.” After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is treated as a NOP if

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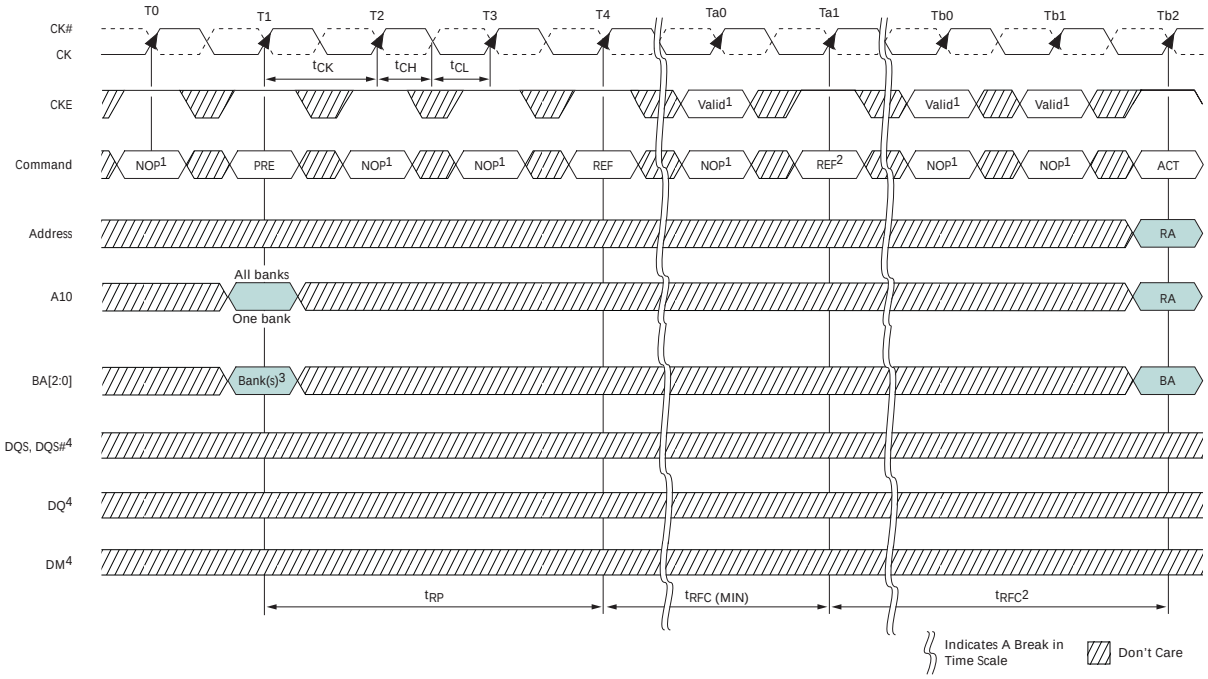
there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period is determined by the last PRECHARGE command issued to the bank.

REFRESH

REFRESH is used during normal operation of the DRAM and is analogous to CAS#-before-RAS# (CBR) refresh or auto refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during a REFRESH command. The DRAM requires REFRESH cycles at an average interval of 7.8µs (maximum when $T_C \leq$ 85°C or 3.9µs MAX when $T_C \leq$ 95°C). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to any given DRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is nine times the maximum average interval refresh rate. The REFRESH period begins when the REFRESH command is registered and ends ^{t}RFC (MIN) later.

Figure 43: Refresh Mode



Notes:
1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during the PRECHARGE, ACTIVATE, and REFRESH commands, but may be inactive at other times (see "Power-Down Mode" on page 151).
2. The second REFRESH is not required but depicts two back-to-back REFRESH commands.
3. "Don't Care" if A10 is HIGH at this point; however, A10 must be HIGH if more than one bank is active (must precharge all active banks).
4. For operations shown, DM, DQ, and DQS signals are all "Don't Care"/High-Z.

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SELF REFRESH

The SELF REFRESH command is used to retain data in the DRAM, even if the rest of the system is powered down. When in the self refresh mode, the DRAM retains data without external clocking. The self refresh mode is also a convenient method used to enable/disable the DLL (see "DLL Disable Mode" on page 96) as well as to change the clock frequency within the allowed synchronous operating range (see "Input Clock Frequency Change" on page 99). All power supply inputs (including VREFCA and VREFDQ) must be maintained at valid levels upon entry/exit and during SELF REFRESH operation.

DLL Disable Mode

If the DLL is disabled by the mode register (MR1[0] can be switched during initialization or later), the DRAM is targeted, but not guaranteed, to operate similarly to the normal mode with a few notable exceptions:

- The DRAM supports only one value of CAS latency (CL = 6) and one value of CAS WRITE latency (CWL = 6).
- DLL disable mode affects the read data clock-to-data strobe relationship (^{t}DQSCK), but not the read data-to-data strobe relationship (^{t}DQSQ, ^{t}QH). Special attention is needed to line the read data up with the controller time domain when the DLL is disabled.
- In normal operation (DLL on), ^{t}DQSCK starts from the rising clock edge AL + CL cycles after the READ command. In DLL disable mode, ^{t}DQSCK starts AL + CL - 1 cycles after the READ command. Additionally, with the DLL disabled, the value of ^{t}DQSCK could be larger than ^{t}CK.

The ODT feature is not supported during DLL disable mode (including dynamic ODT). The ODT resistors must be disabled by continuously registering the ODT ball LOW by programming RTT_NOM MR1[9, 6, 2] and RTT_WR MR2[10, 9] to "0" while in the DLL disable mode.

Specific steps must be followed to switch between the DLL enable and DLL disable modes due to a gap in the allowed clock rates between the two modes (^{t}CK [AVG] MAX and ^{t}CK [DLL disable] MIN, respectively). The only time the clock is allowed to cross this clock rate gap is during self refresh mode. Thus, the required procedure for switching from the DLL enable mode to the DLL disable mode is to change frequency during self refresh (see Figure 44 on page 97):

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and RTT_NOM and RTT_WR are High-Z), set MR1[0] to "1" to disable the DLL.
2. Enter self refresh mode after ^{t}MOD has been satisfied.
3. After ^{t}CKSRE is satisfied, change the frequency to the desired clock rate.
4. Self refresh may be exited when the clock is stable with the new frequency for ^{t}CKSRX. After ^{t}XS is satisfied, update the mode registers with appropriate values.
5. The DRAM will be ready for its next command in the DLL disable mode after the greater of ^{t}MRD or ^{t}MOD has been satisfied. A ZQCL command should be issued with appropriate timings met as well.

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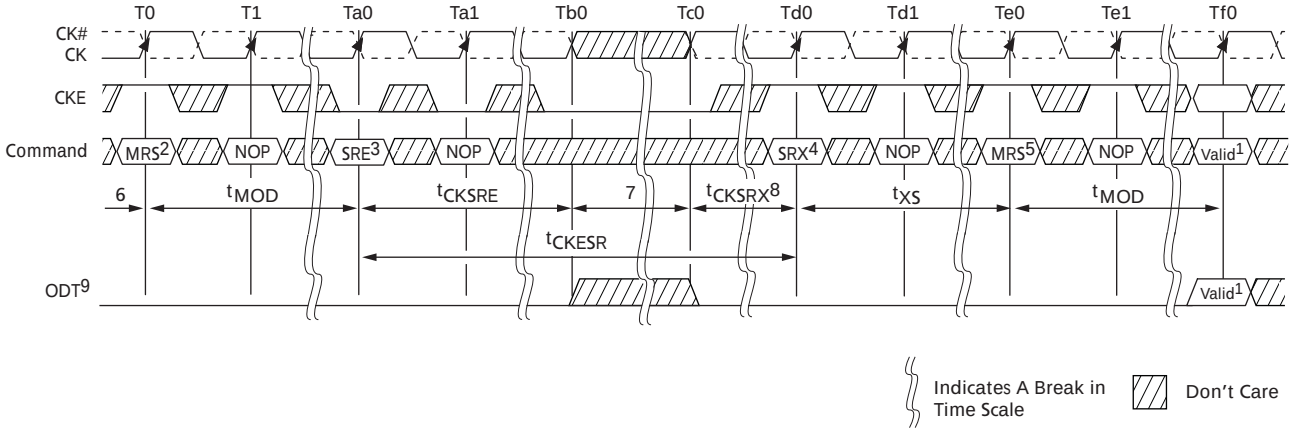
Figure 44: DLL Enable Mode to DLL Disable Mode



Notes:
1. Any valid command.
2. Disable DLL by setting MR1[0] to "1."
3. Enter SELF REFRESH.
4. Exit SELF REFRESH.
5. Update the mode registers with the DLL disable parameters setting.
6. Starting with the idle state, RTT is in the High-Z state.
7. Change frequency.
8. Clock must be stable ^{t}CKSRX.
9. Static LOW in case RTT_NOM or RTT_WR is enabled; otherwise, static LOW or HIGH.

A similar procedure is required for switching from the DLL disable mode back to the DLL enable mode. This also requires changing the frequency during self refresh mode (see Figure 45 on page 98).

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and RTT_NOM and RTT_WR are High-Z), enter self refresh mode.
2. After ^{t}CKSRE is satisfied, change the frequency to the new clock rate.
3. Self refresh may be exited when the clock is stable with the new frequency for ^{t}CKSRX. After ^{t}XS is satisfied, update the mode registers with the appropriate values. At a minimum, set MR1[0] to "0" to enable the DLL. Wait ^{t}MRD, then set MR0[8] to "1" to enable DLL RESET.
4. After another ^{t}MRD delay is satisfied, then update the remaining mode registers with the appropriate values.
5. The DRAM will be ready for its next command in the DLL enable mode after the greater of ^{t}MRD or ^{t}MOD has been satisfied. However, before applying any command or function requiring a locked DLL, a delay of ^{t}DLLK after DLL RESET must be satisfied. A ZQCL command should be issued with the appropriate timings met as well.

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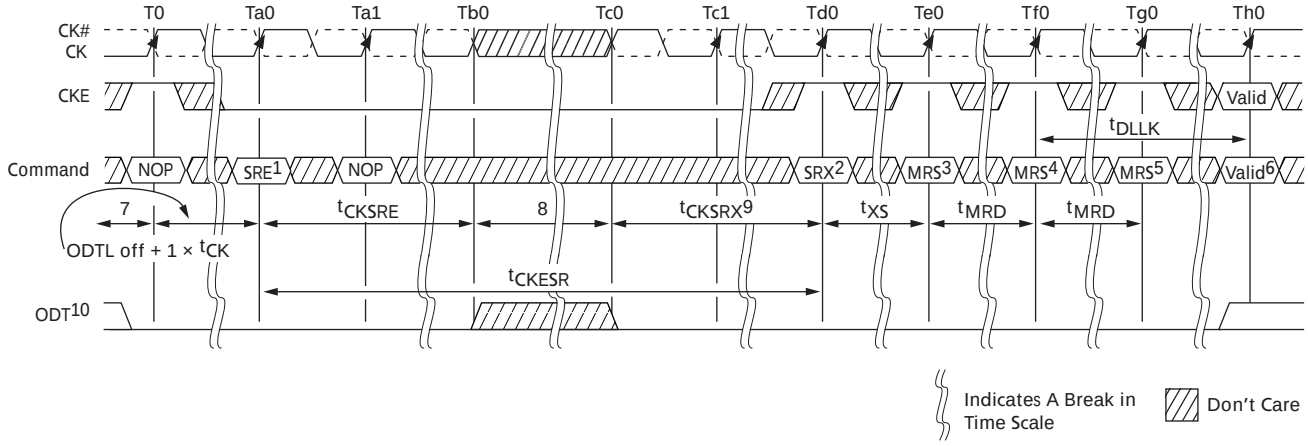
Figure 45: DLL Disable Mode to DLL Enable Mode



Notes:
1. Enter SELF REFRESH.
2. Exit SELF REFRESH.
3. Wait ^{t}XS, then set MR1[0] to "0" to enable DLL.
4. Wait ^{t}MRD, then set MR0[8] to "1" to begin DLL RESET.
5. Wait ^{t}MRD, update registers (CL, CWL, and write recovery may be necessary).
6. Wait ^{t}MOD, any valid command.
7. Starting with the idle state.
8. Change frequency.
9. Clock must be stable at least ^{t}CKSRX.
10. Static LOW in case RTT_NOM or RTT_WR is enabled; otherwise, static LOW or HIGH.

The clock frequency range for the DLL disable mode is specified by the parameter ^{t}CKDLL_DIS. Due to latency counter and timing restrictions, only CL = 6 and CWL = 6 are supported.

DLL disable mode will affect the read data clock to data strobe relationship (^{t}DQSCK) but not the data strobe to data relationship (^{t}DQSQ, ^{t}QH). Special attention is needed to line up read data to the controller time domain.

Compared to the DLL on mode where ^{t}DQSCK starts from the rising clock edge AL + CL cycles after the READ command, the DLL disable mode ^{t}DQSCK starts AL + CL - 1 cycles after the READ command (see Figure 46 on page 99).

WRITE operations function similarly between the DLL enable and DLL disable modes; however, ODT functionality is not allowed with DLL disable mode.

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Figure 46: DLL Disable ^{t}DQSCK Timing

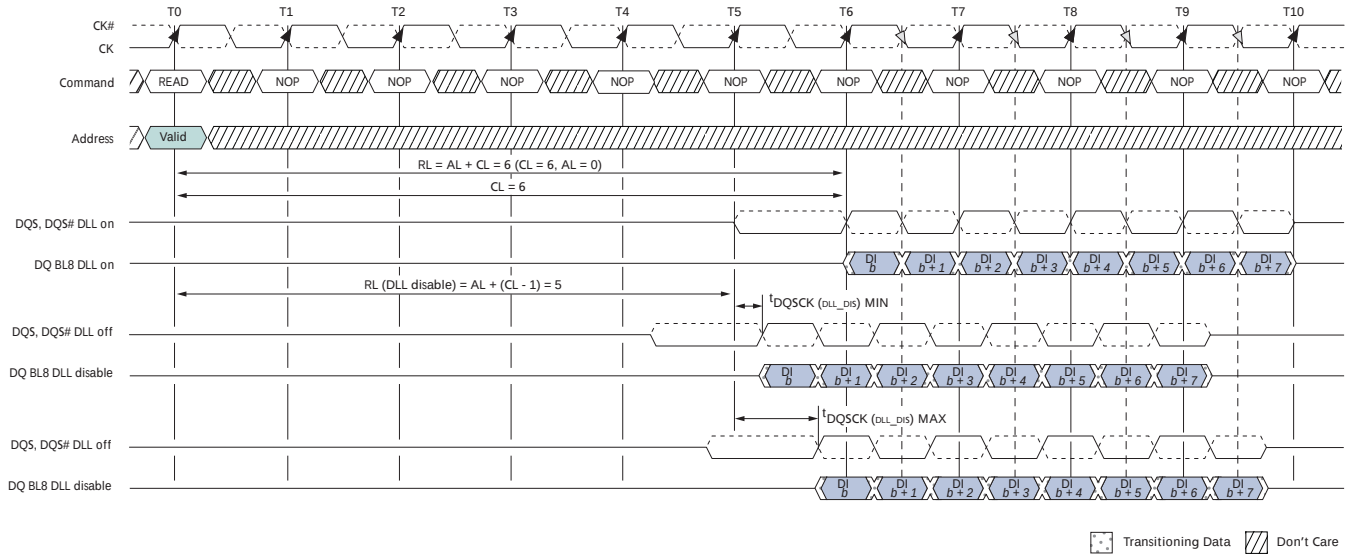

Table 66: READ Electrical Characteristics, DLL Disable Mode

Parameter	Symbol	Min	Max	Units
Access window of DQS from CK, CK#	^{t}DQSCK (DLL_DIS)	1	10	ns

Input Clock Frequency Change

When the DDR3 SDRAM is initialized, it requires the clock to be stable during most normal states of operation. This means that after the clock frequency has been set to the stable state, the clock period is not allowed to deviate except what is allowed for by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another under two conditions: self refresh mode and precharge power-down mode. Outside of these two modes, it is illegal to change the clock frequency. For the self refresh mode condition, when the DDR3 SDRAM has been successfully placed into self refresh mode and ^{t}CKSRE has been satisfied, the state of the clock becomes a "Don't Care." When the clock becomes a "Don't Care," changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^{t}CKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met.

The precharge power-down mode condition is when the DDR3 SDRAM is in precharge power-down mode (either fast exit mode or slow exit mode). Either ODT must be at a logic LOW or RTT_NOM and RTT_WR must be disabled via MR1 and MR2. This ensures RTT_NOM and RTT_WR are in an off state prior to entering precharge power-down mode, and CKE must be at a logic LOW. A minimum of ^{t}CKSRE must occur after CKE goes LOW before the clock frequency can change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade (^{t}CK [AVG] MIN to ^{t}CK [AVG] MAX). During the input clock frequency change, CKE must be held at a stable LOW level. When the input clock frequency is changed, a stable clock must be provided to the DRAM ^{t}CKSRX before precharge power-down may be exited. After precharge power-down is exited and ^{t}XP has

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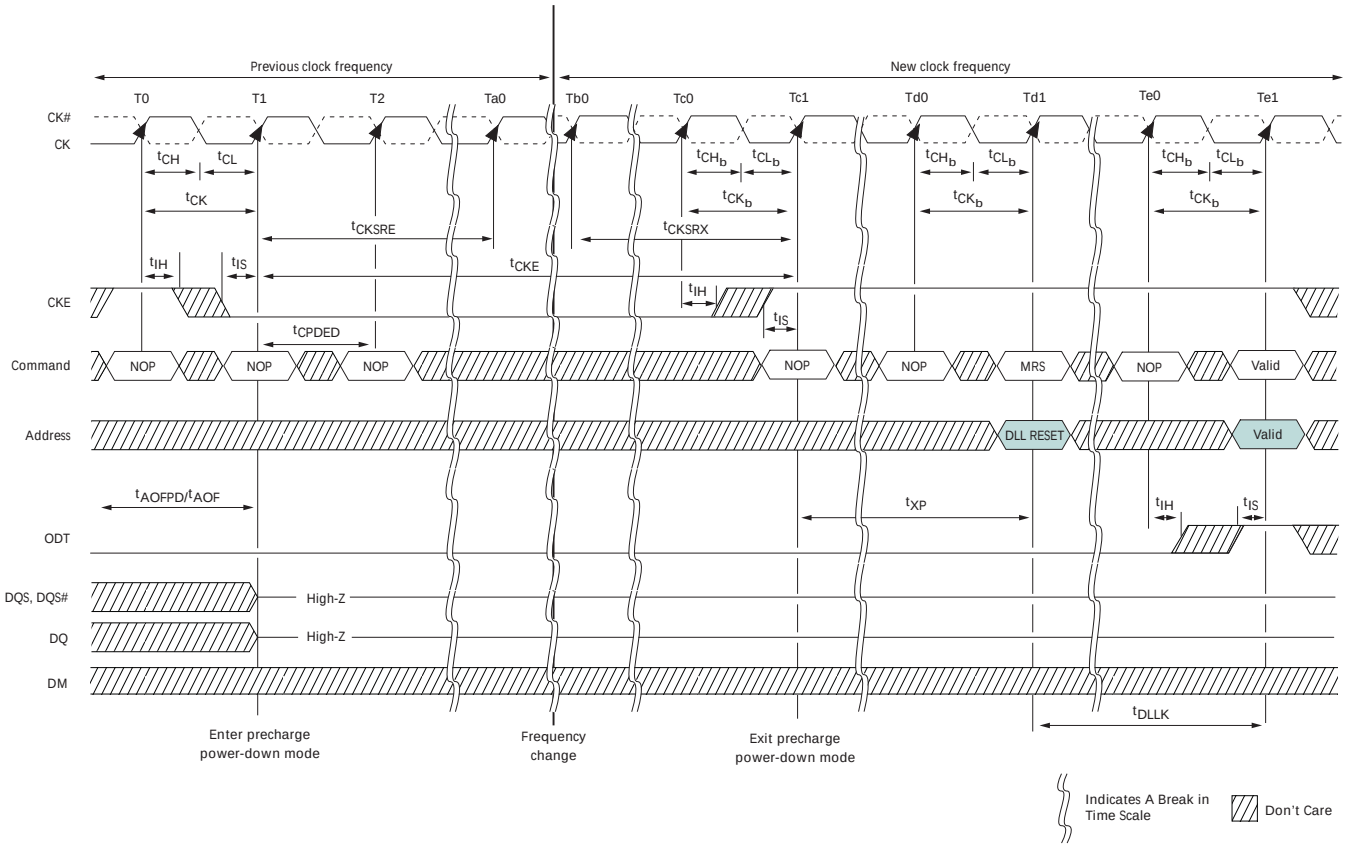
been satisfied, the DLL must be reset via the MRS. Depending on the new clock frequency, additional MRS commands may need to be issued. During the DLL lock time, RTT_NOM and RTT_WR must remain in an off state. After the DLL lock time, the DRAM is ready to operate with a new clock frequency. This process is depicted in Figure 47.

Figure 47: Change Frequency During Precharge Power-Down



Notes:
1. Applicable for both slow-exit and fast-exit precharge power-down modes.
2. ^{t}AOFPD and ^{t}AOF must be satisfied and outputs High-Z prior to T1 (see "On-Die Termination (ODT)" on page 160 for exact requirements).
3. If the RTT_NOM feature was enabled in the mode register prior to entering precharge power-down mode, the ODT signal must be continuously registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering precharge power-down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

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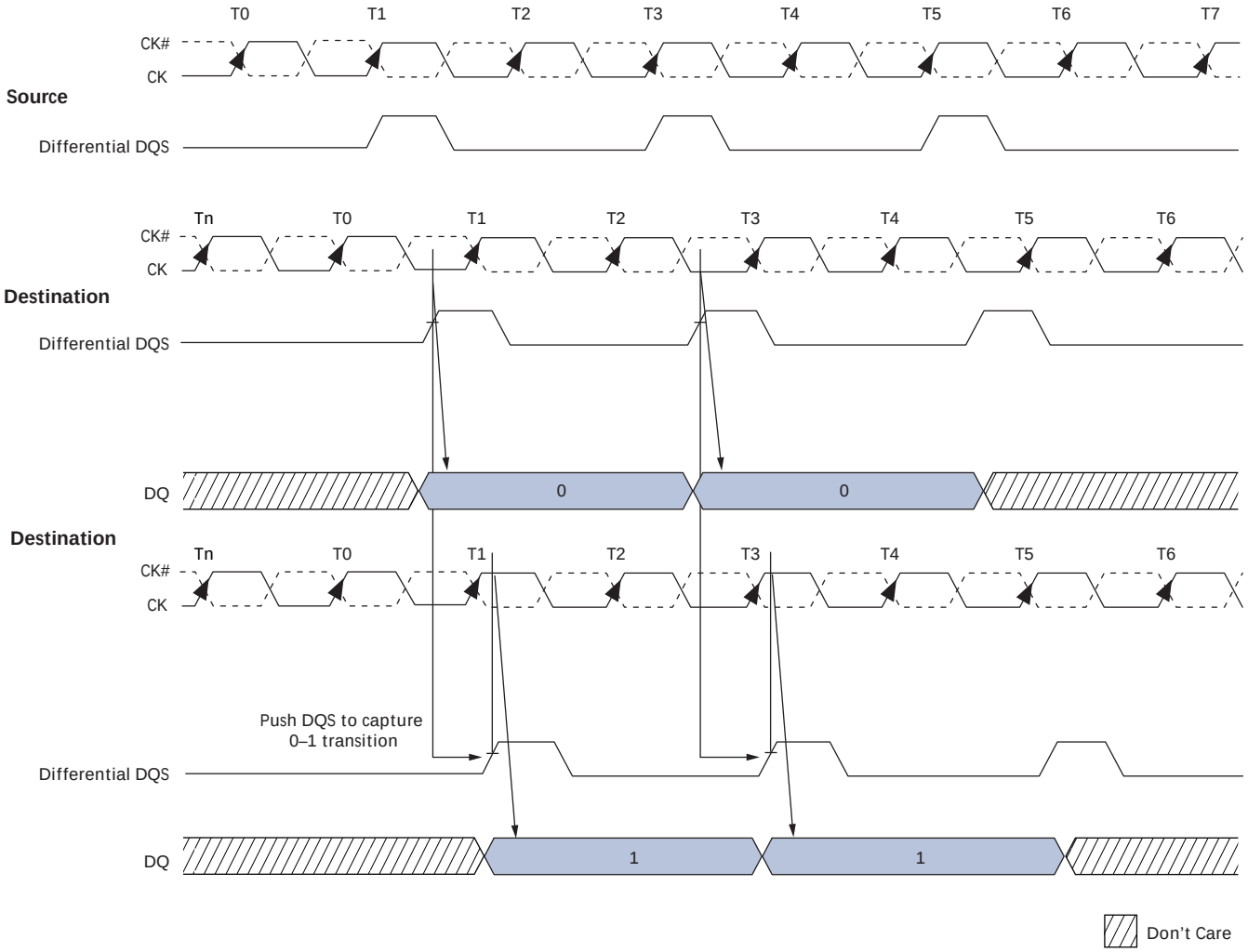
Write Leveling

For better signal integrity, DDR3 SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks. Write leveling is a scheme for the memory controller to adjust or deskew the DQS strobe (DQS, DQS#) to CK relationship at the DRAM with a simple feedback feature provided by the DRAM. Write leveling is generally used as part of the initialization process, if required. For normal DRAM operation, this feature must be disabled. This is the only DRAM operation where the DQS functions as an input (to capture the incoming clock) and the DQ function as outputs (to report the state of the clock). Note that nonstandard ODT schemes are required.

The memory controller using the write leveling procedure must have adjustable delay settings on its DQS strobe to align the rising edge of DQS to the clock at the DRAM pins. This is accomplished when the DRAM asynchronously feeds back the CK status via the DQ bus and samples with the rising edge of DQS. The controller repeatedly delays the DQS strobe until a CK transition from “0” to “1” is detected. The DQS delay established through this procedure helps ensure ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications in systems that use fly-by topology by deskewing the trace length mismatch. A conceptual timing of this procedure is shown in Figure 48.

Figure 48: Write Leveling Concept



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When write leveling is enabled, the rising edge of DQS samples CK, and the prime DQ outputs the sampled CK's status. The prime DQ for a x4 or x8 configuration is DQ0 with all other DQ (DQ[7:1]) driving LOW. The prime DQ for a x16 configuration is DQ0 for the lower byte and DQ8 for the upper byte. It outputs the status of CK sampled by LDQS and UDQS. All other DQ (DQ[7:1], DQ[15:9]) continue to drive LOW. Two prime DQ on a x16 enable each byte lane to be leveled independently.

The write leveling mode register interacts with other mode registers to correctly configure the write leveling functionality. Besides using MR1[7] to disable/enable write leveling, MR1[12] must be used to enable/disable the output buffers. The ODT value, burst length, and so forth need to be selected as well. This interaction is shown in Table 67. It should also be noted that when the outputs are enabled during write leveling mode, the DQS buffers are set as inputs, and the DQ are set as outputs. Additionally, during write leveling mode, only the DQS strobe terminations are activated and deactivated via the ODT ball. The DQ remain disabled and are not affected by the ODT ball (see Table 67).

Table 67: Write Leveling Matrix
Note 1 applies to the entire table

MR1[7]	MR1[12]	MR1[3, 6, 9]		DRAM R_{TT_NOM}				
Write Leveling	**Output Buffers**	**R_{TT_NOM} Value**	**DRAM ODT Ball**	**DQS**	**DQ**	**DRAM State**	**Case**	**Notes**
Disabled	See normal operations					Write leveling not enabled	0	
Enabled (1)	Disabled (1)	n/a	Low	Off	Off	DQS not receiving: not terminated Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	1	2
		20Ω, 30Ω, 40Ω, 60Ω, or 120Ω	High	On		DQS not receiving: terminated by R_{TT} Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	2	
	Enabled (0)	n/a	Low	Off		DQS receiving: not terminated Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	3	3
		40Ω, 60Ω, or 120Ω	High	On		DQS receiving: terminated by R_{TT} Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	4	

Notes:
1. Expected usage if used during write leveling: Case 1 may be used when DRAM are on a dual-rank module and on the rank not being levelized or on any rank of a module not being levelized on a multislotted system. Case 2 may be used when DRAM are on any rank of a module not being levelized on a multislotted system. Case 3 is generally not used. Case 4 is generally used when DRAM are on the rank that is being leveled.
2. Since the DRAM DQS is not being driven (MR1[12] = 1), DQS ignores the input strobe, and all R_{TT_NOM} values are allowed. This simulates a normal standby state to DQS.
3. Since the DRAM DQS is being driven (MR1[12] = 0), DQS captures the input strobe, and only some R_{TT_NOM} values are allowed. This simulates a normal write state to DQS.

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Write Leveling Procedure

A memory controller initiates the DRAM write leveling mode by setting MR1[7] to a "1," assuming the other programable features (MR0, MR1, MR2, and MR3) are first set and the DLL is fully reset and locked. The DQ balls enter the write leveling mode going from a High-Z state to an undefined driving state, so the DQ bus should not be driven. During write leveling mode, only the NOP or DES commands are allowed. The memory controller should attempt to level only one rank at a time; thus, the outputs of other ranks should be disabled by setting MR1[12] to a "1" in the other ranks. The memory controller may assert ODT after a ^{t}MOD delay as the DRAM will be ready to process the ODT transition. ODT should be turned on prior to DQS being driven LOW by at least ODTL on delay (WL - 2 ^{t}CK), provided it does not violate the aforementioned ^{t}MOD delay requirement.

The memory controller may drive DQS LOW and DQS# HIGH after ^{t}WLDQSEN has been satisfied. The controller may begin to toggle DQS after ^{t}WLMRD (one DQS toggle is DQS transitioning from a LOW state to a HIGH state with DQS# transitioning from a HIGH state to a LOW state, then both transition back to their original states). At a minimum, ODTL on and ^{t}AON must be satisfied at least one clock prior to DQS toggling.

After ^{t}WLMRD and a DQS LOW preamble (^{t}WPRE) have been satisfied, the memory controller may provide either a single DQS toggle or multiple DQS toggles to sample CK for a given DQS-to-CK skew. Each DQS toggle must not violate ^{t}DQSL (MIN) and ^{t}DQSH (MIN) specifications. ^{t}DQSL (MAX) and ^{t}DQSH (MAX) specifications are not applicable during write leveling mode. The DQS must be able to distinguish the CK's rising edge within ^{t}WLS and ^{t}WLH. The prime DQ will output the CK's status asynchronously from the associated DQS rising edge CK capture within ^{t}WLO. The remaining DQ that always drive LOW when DQS is toggling must be LOW within ^{t}WLOE after the first ^{t}WLO is satisfied (the prime DQ going LOW). As previously noted, DQS is an input and not an output during this process. Figure 49 on page 104 depicts the basic timing parameters for the overall write leveling procedure.

The memory controller will likely sample each applicable prime DQ state and determine whether to increment or decrement its DQS delay setting. After the memory controller performs enough DQS toggles to detect the CK's "0-to-1" transition, the memory controller should lock the DQS delay setting for that DRAM. After locking the DQS setting, leveling for the rank will have been achieved, and the write leveling mode for the rank should be disabled or reprogrammed (if write leveling of another rank follows).

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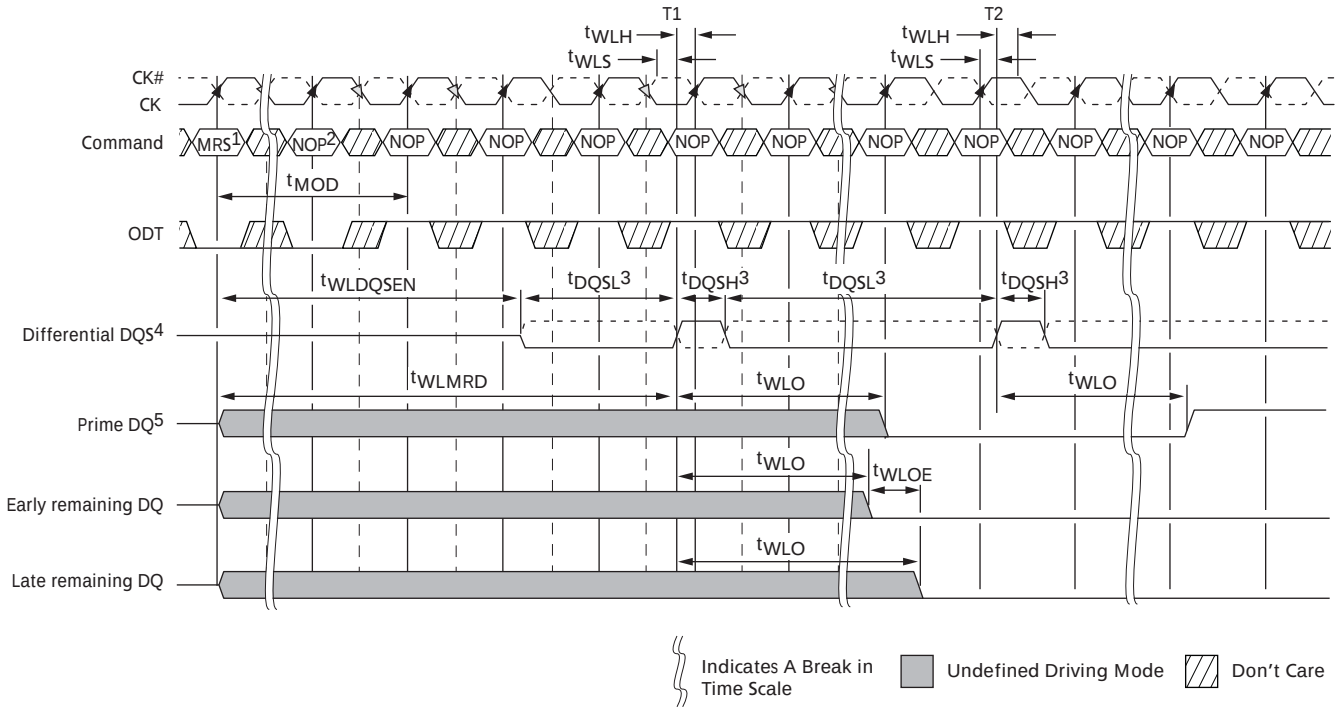
Figure 49: Write Leveling Sequence



Notes:
1. MRS: Load MR1 to enter write leveling mode.
2. NOP: NOP or DES.
3. DQS, DQS# needs to fulfill minimum pulse width requirements ^{t}DQSH (MIN) and ^{t}DQSL (MIN) as defined for regular writes. The maximum pulse width is system-dependent.
4. Differential DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. The solid line represents DQS; the dotted line represents DQS#.
5. DRAM drives leveling feedback on a prime DQ (DQ0 for x4 and x8). The remaining DQ are driven low and remain in this state throughout the leveling procedure.

Write Leveling Mode Exit Procedure

After the DRAM are leveled, they must exit from write leveling mode before the normal mode can be used. Figure 50 on page 105 depicts a general procedure in exiting write leveling mode. After the last rising DQS (capturing a "1" at T0), the memory controller should stop driving the DQS signals after ^{t}WLO (MAX) delay plus enough delay to enable the memory controller to capture the applicable prime DQ state (at ~Tb0). The DQ balls become undefined when DQS no longer remains LOW, and they remain undefined until ^{t}MOD after the MRS command (at Te1).

The ODT input should be deasserted LOW such that ODTL off (MIN) expires after the DQS is no longer driving LOW. When ODT LOW satisfies ^{t}IS, ODT must be kept LOW (at ~Tb0) until the DRAM is ready for either another rank to be leveled or until the normal mode can be used. After DQS termination is switched off, write level mode should be disabled via the MRS command (at Tc2). After ^{t}MOD is satisfied (at Te1), any valid command may be registered by the DRAM. Some MRS commands may be issued after ^{t}MRD (at Td1).

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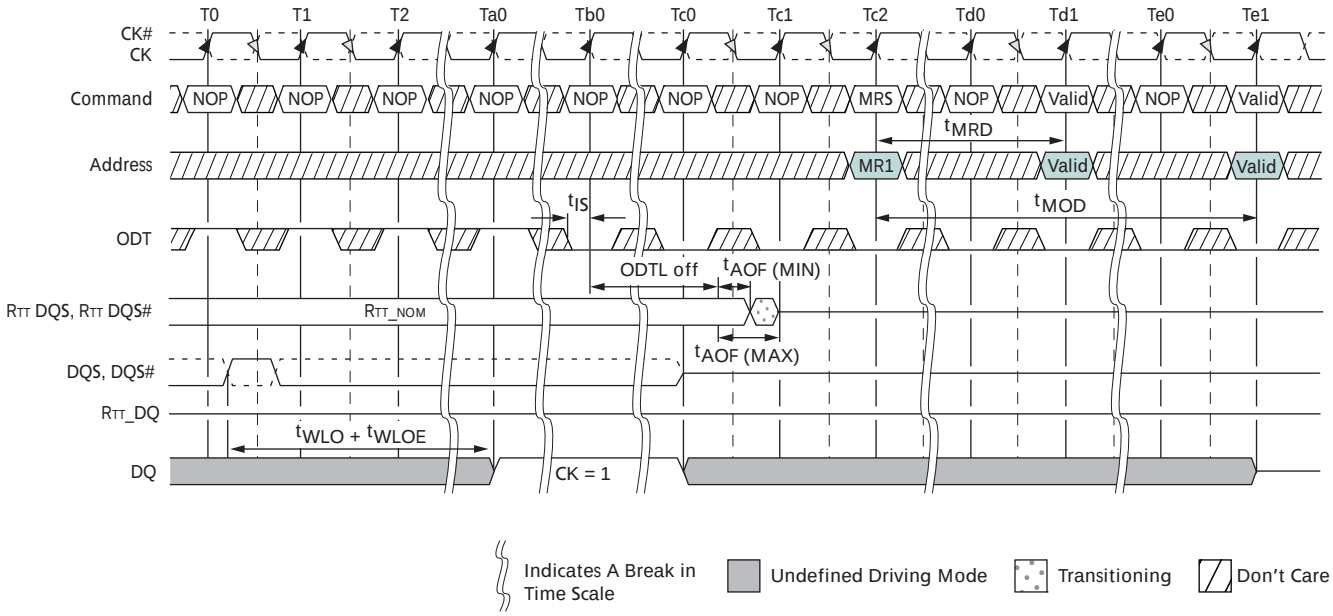
Figure 50: Exit Write Leveling



Notes: 1. The DQ result, "= 1," between Ta0 and Tc0, is a result of the DQS, DQS# signals capturing CK HIGH just after the T0 state.

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Operations

Initialization

The following sequence is required for power up and initialization, as shown in Figure 51 on page 107:

1. Apply power. RESET# is recommended to be below 0.2 × V_{DDQ} during power ramp to ensure the outputs remain disabled (High-Z) and ODT off (R_{TT} is also High-Z). All other inputs, including ODT, may be undefined.

During power up, either of the following conditions may exist and must be met:

- Condition A:
  - V_{DD} and V_{DDQ} are driven from a single-power converter output and are ramped with a maximum delta voltage between them of $\Delta V \leq 300mV$. Slope reversal of any power supply signal is allowed. The voltage levels on all balls other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side, and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.
  - Both V_{DD} and V_{DDQ} power supplies ramp to V_{DD} (MIN) and V_{DDQ} (MIN) within $^{t}V_{DDPR}$ = 200ms.
  - V_{REF}DQ tracks V_{DD} × 0.5, V_{REF}CA tracks V_{DD} × 0.5.
  - V_{TT} is limited to 0.95V when the power ramp is complete and is not applied directly to the device; however, ^{t}VTD should be greater than or equal to zero to avoid device latchup.
- Condition B:
  - V_{DD} may be applied before or at the same time as V_{DDQ}.
  - V_{DDQ} may be applied before or at the same time as V_{TT}, V_{REF}DQ, and V_{REF}CA.
  - No slope reversals are allowed in the power supply ramp for this condition.

2. Until stable power, maintain RESET# LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RESET# must be LOW for at least 200µs to begin the initialization process. ODT will remain in the High-Z state while RESET# is LOW and until CKE is registered HIGH.
3. CKE must be LOW 10ns prior to RESET# transitioning HIGH.
4. After RESET# transitions HIGH, wait 500µs (minus one clock) with CKE LOW.
5. After this CKE LOW time, CKE may be brought HIGH (synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns (and a minimum of five clocks) and ODT must be driven LOW at least ^{t}IS prior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.
6. After CKE is registered HIGH and after ^{t}XPR has been satisfied, MRS commands may be issued. Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).
7. Issue an MRS command to MR3 with the applicable settings.
8. Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring ODT.
9. Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. ^{t}DLLK (512) cycles of clock input are required to lock the DLL.
10. Issue a ZQCL command to calibrate R_{TT} and R_{ON} values for the process voltage temperature (PVT). Prior to normal operation, $^{t}ZQ_{INIT}$ must be satisfied.
11. When ^{t}DLLK and $^{t}ZQ_{INIT}$ have been satisfied, the DDR3 SDRAM will be ready for normal operation.

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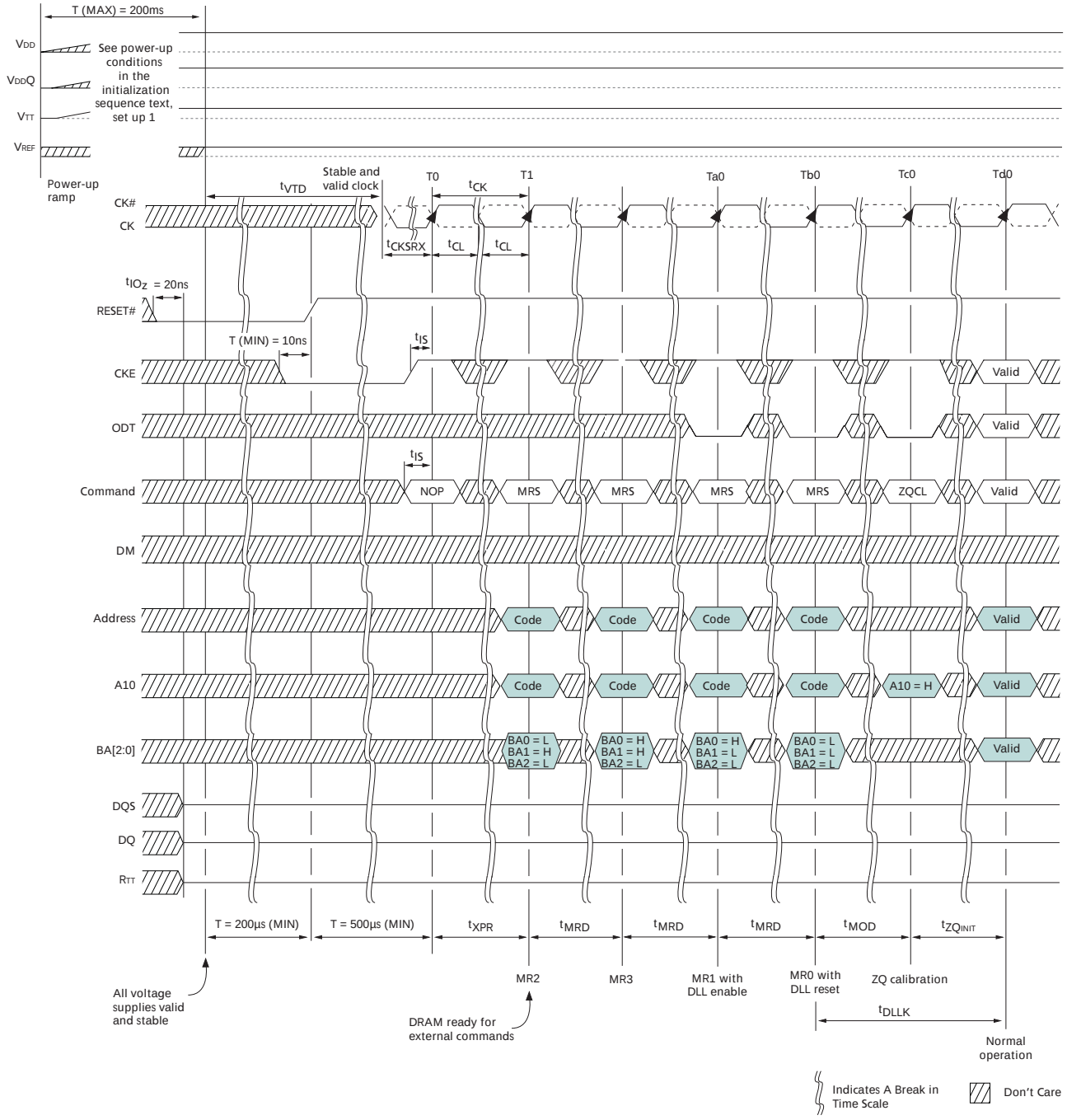
Figure 51: Initialization Sequence



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Mode Registers

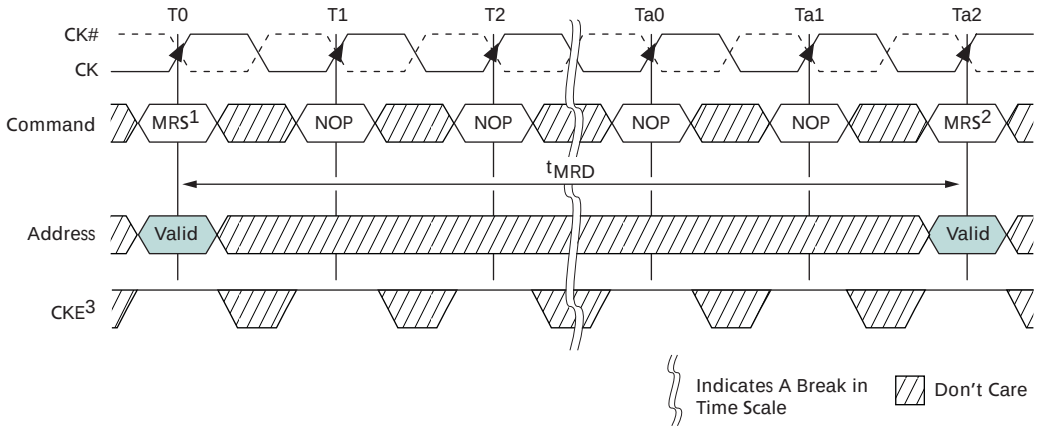
Mode registers (MR0–MR3) are used to define various modes of programmable operations of the DDR3 SDRAM. A mode register is programmed via the MODE REGISTER SET (MRS) command during initialization, and it retains the stored information (except for MR0[8] which is self-clearing) until it is either reprogrammed, RESET# goes LOW, or until the device loses power.

Contents of a mode register can be altered by reexecuting the MRS command. If the user chooses to modify only a subset of the mode register's variables, all variables must be programmed when the MRS command is issued. Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The MRS command can only be issued (or reissued) when all banks are idle and in the precharged state (^{t}RP is satisfied and no data bursts are in progress). After an MRS command has been issued, two parameters must be satisfied: ^{t}MRD and ^{t}MOD.

The controller must wait ^{t}MRD before initiating any subsequent MRS commands (see Figure 52).

Figure 52: MRS-to-MRS Command Timing (^{t}MRD)



Notes:
1. Prior to issuing the MRS command, all banks must be idle and precharged, ^{t}RP (MIN) must be satisfied, and no data bursts can be in progress.
2. ^{t}MRD specifies the MRS-to-MRS command minimum cycle time.
3. CKE must be registered HIGH from the MRS command until ^{t}MRSPDEN (MIN) (see "Power-Down Mode" on page 151).
4. For a CAS latency change, ^{t}XPDLL timing must be met before any nonMRS command.

The controller must also wait ^{t}MOD before initiating any nonMRS commands (excluding NOP and DES), as shown in Figure 53 on page 109. The DRAM requires ^{t}MOD in order to update the requested features, with the exception of DLL RESET, which requires additional time. Until ^{t}MOD has been satisfied, the updated features are to be assumed unavailable.

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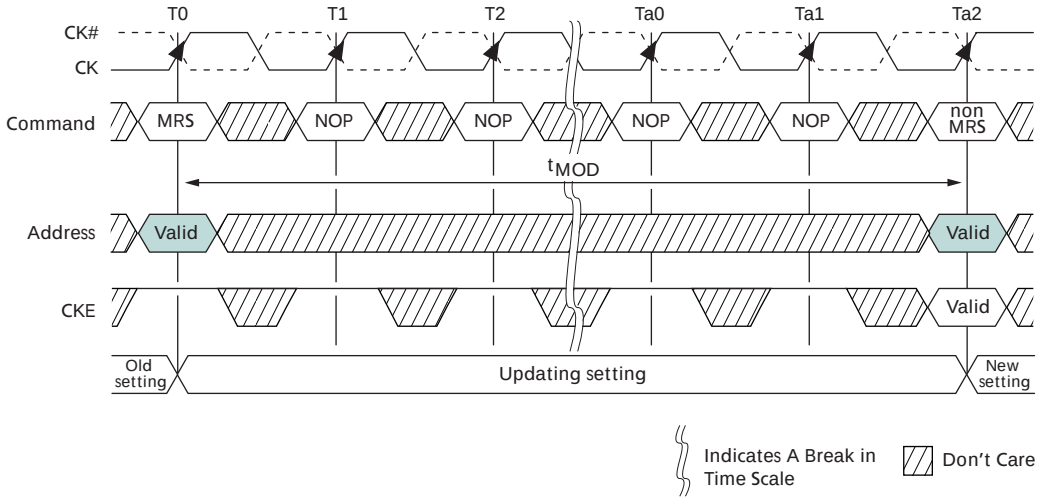
Figure 53: MRS-to-nonMRS Command Timing (^{t}MOD)



Notes:
1. Prior to issuing the MRS command, all banks must be idle (they must be precharged, ^{t}RP must be satisfied, and no data bursts can be in progress).
2. Prior to Ta2 when ^{t}MOD (MIN) is being satisfied, no commands (except NOP/DES) may be issued.
3. If RTT was previously enabled, ODT must be registered LOW at T0 so that ODTL is satisfied prior to Ta1. ODT must also be registered LOW at each rising CK edge from T0 until ^{t}MOD (MIN) is satisfied at Ta2.
4. CKE must be registered HIGH from the MRS command until ^{t}MRSPDEN (MIN), at which time power-down may occur (see "Power-Down Mode" on page 151).

Mode Register 0 (MR0)

The base register, MR0, is used to define various DDR3 SDRAM modes of operation. These definitions include the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and precharge power-down mode, as shown in Figure 54 on page 110.

Burst Length

Burst length is defined by MR0[1: 0] (see Figure 54 on page 110). Read and write accesses to the DDR3 SDRAM are burst-oriented, with the burst length being programmable to "4" (chop mode), "8" (fixed), or selectable using A12 during a READ/WRITE command (on-the-fly). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When MR0[1:0] is set to "01" during a READ/WRITE command, if A12 = 0, then BC4 (chop) mode is selected. If A12 = 1, then BL8 mode is selected. Specific timing diagrams, and turnaround between READ/WRITE, are shown in the READ/WRITE sections of this document.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[*i*:2] when the burst length is set to "4" and by A[*i*:3] when the burst length is set to "8" (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

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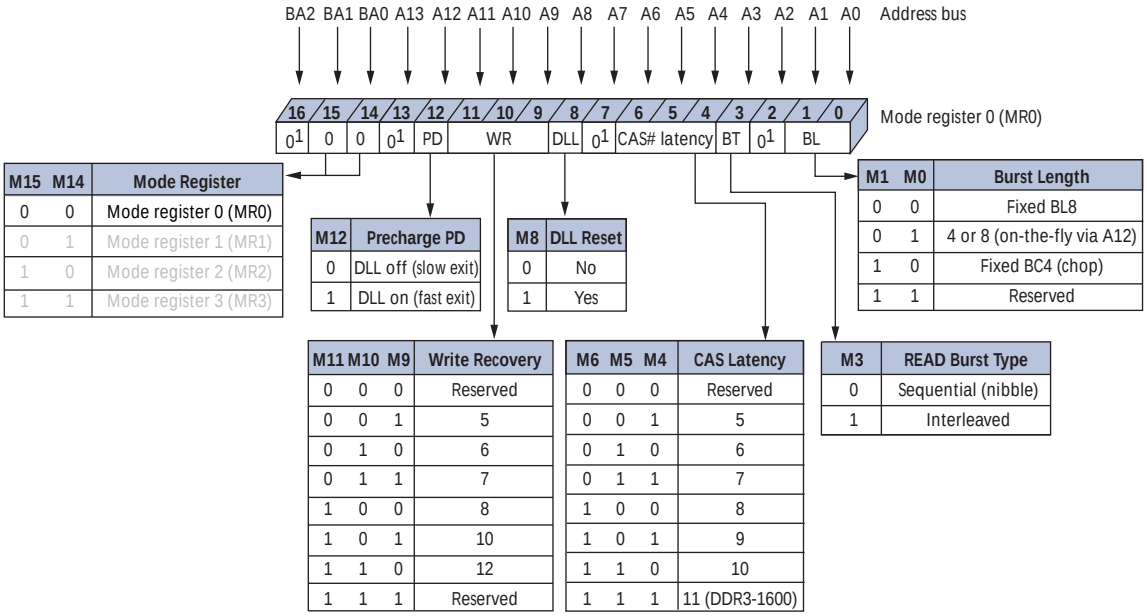
Figure 54: Mode Register 0 (MR0) Definitions



M15	M14	Mode Register
0	0	Mode register 0 (MR0)
0	1	Mode register 1 (MR1)
1	0	Mode register 2 (MR2)
1	1	Mode register 3 (MR3)

M12	Precharge PD
0	DLL off (slow exit)
1	DLL on (fast exit)

M8	DLL Reset
0	No
1	Yes

M1	M0	Burst Length
0	0	Fixed BL8
0	1	4 or 8 (on-the-fly via A12)
1	0	Fixed BC4 (chop)
1	1	Reserved

M11	M10	M9	Write Recovery
0	0	0	Reserved
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	Reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11 (DDR3-1600)

M3	READ Burst Type
0	Sequential (nibble)
1	Interleaved

Notes: 1. MR0[16, 13, 7, 2] are reserved for future use and must be programmed to “0.”

Burst Type

Accesses within a given burst may be programmed to either a sequential or an interleaved order. The burst type is selected via MR0[3], as shown in Figure 54. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 68 on page 111. DDR3 only supports 4-bit burst chop and 8-bit burst access modes. Full interleave address ordering is supported for READs, while WRITEs are restricted to nibble (BC4) or word (BL8) boundaries.

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Table 68: Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
4 chop	READ	0 0 0	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, Z, Z, Z, Z	1, 2
		0 0 1	1, 2, 3, 0, Z, Z, Z, Z	1, 0, 3, 2, Z, Z, Z, Z	1, 2
		0 1 0	2, 3, 0, 1, Z, Z, Z, Z	2, 3, 0, 1, Z, Z, Z, Z	1, 2
		0 1 1	3, 0, 1, 2, Z, Z, Z, Z	3, 2, 1, 0, Z, Z, Z, Z	1, 2
		1 0 0	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, Z, Z, Z, Z	1, 2
		1 0 1	5, 6, 7, 4, Z, Z, Z, Z	5, 4, 7, 6, Z, Z, Z, Z	1, 2
		1 1 0	6, 7, 4, 5, Z, Z, Z, Z	6, 7, 4, 5, Z, Z, Z, Z	1, 2
		1 1 1	7, 4, 5, 6, Z, Z, Z, Z	7, 6, 5, 4, Z, Z, Z, Z	1, 2
	WRITE	0 V V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 3, 4
		1 V V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	1, 3, 4
8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	1
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	1
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	1
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	1
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	1
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	1
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	1
	WRITE	V V V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1, 3

Notes:
1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
2. Z = Data and strobe output drivers are in tristate.
3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.
4. X = "Don't Care."

DLL RESET

DLL RESET is defined by MR0[8] (see Figure 54 on page 110). Programming MR0[8] to "1" activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of "0" after the DLL RESET function has been initiated.

Anytime the DLL RESET function is initiated, CKE must be HIGH and the clock held stable for 512 (^{t}DLLK) clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in invalid output timing specifications, such as ^{t}DQSCK timings.

Write Recovery

WRITE recovery time is defined by MR0[11:9] (see Figure 54 on page 110). Write recovery values of 5, 6, 7, 8, 10, or 12 may be used by programming MR0[11:9]. The user is required to program the correct value of write recovery and is calculated by dividing ^{t}WR (ns) by ^{t}CK (ns) and rounding up a noninteger value to the next integer: WR (cycles) = roundup (^{t}WR [ns]/^{t}CK [ns]).

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Precharge Power-Down (Precharge PD)

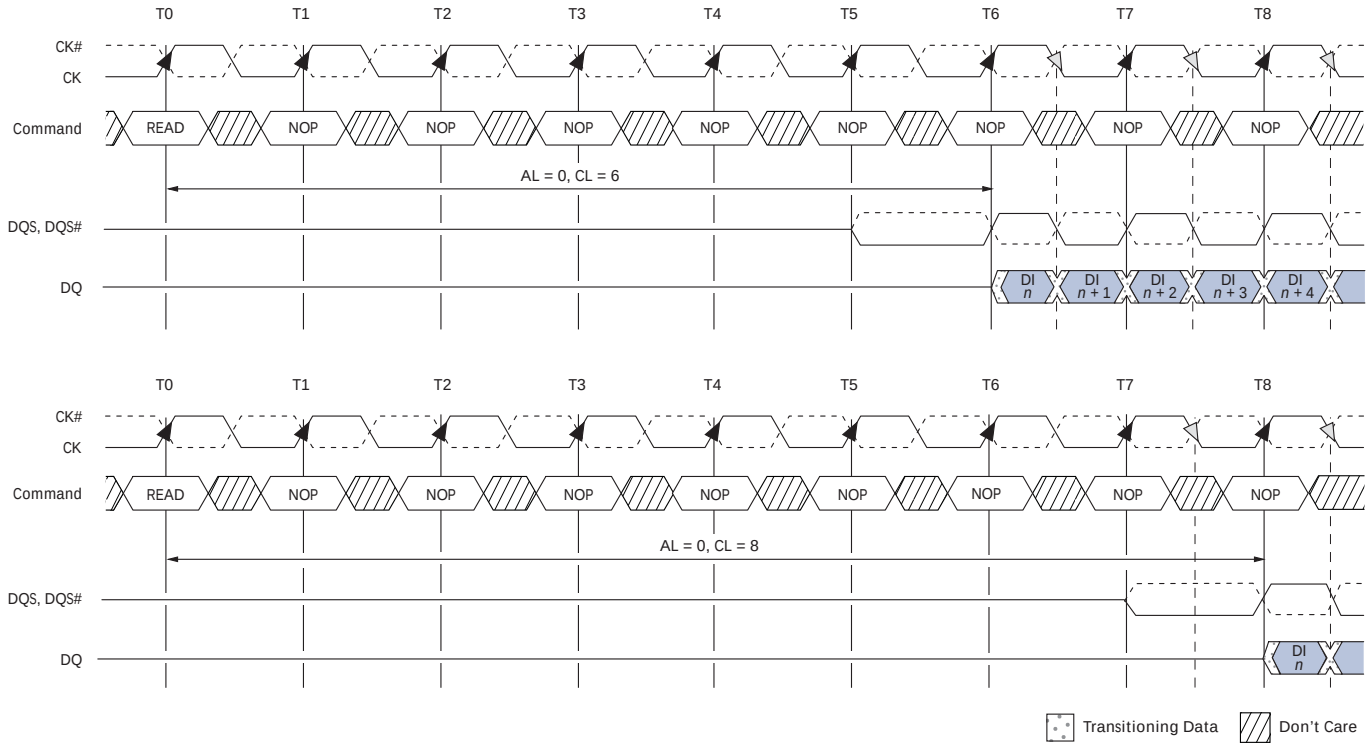
The precharge PD bit applies only when precharge power-down mode is being used. When MR0[12] is set to “0,” the DLL is off during precharge power-down providing a lower standby current mode; however, ^{t}XPDLL must be satisfied when exiting. When MR0[12] is set to “1,” the DLL continues to run during precharge power-down mode to enable a faster exit of precharge power-down mode; however, ^{t}XP must be satisfied when exiting (see "Power-Down Mode" on page 151).

CAS Latency (CL)

The CL is defined by MR0[6:4], as shown in Figure 54 on page 110. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The CL can be set to 5, 6, 7, 8, 9, or 10. DDR3 SDRAM do not support half-clock latencies.

Examples of CL = 6 and CL = 8 are shown in Figure 55. If an internal READ command is registered at clock edge *n*, and the CAS latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 49 on page 63 through Table 51 on page 65 indicate the CLs supported at various operating frequencies.

Figure 55: READ Latency



Notes: 1. For illustration purposes, only CL = 6 and CL = 8 are shown. Other CL values are possible.
2. Shown with nominal ^{t}DQSCK and nominal ^{t}DSDQ.

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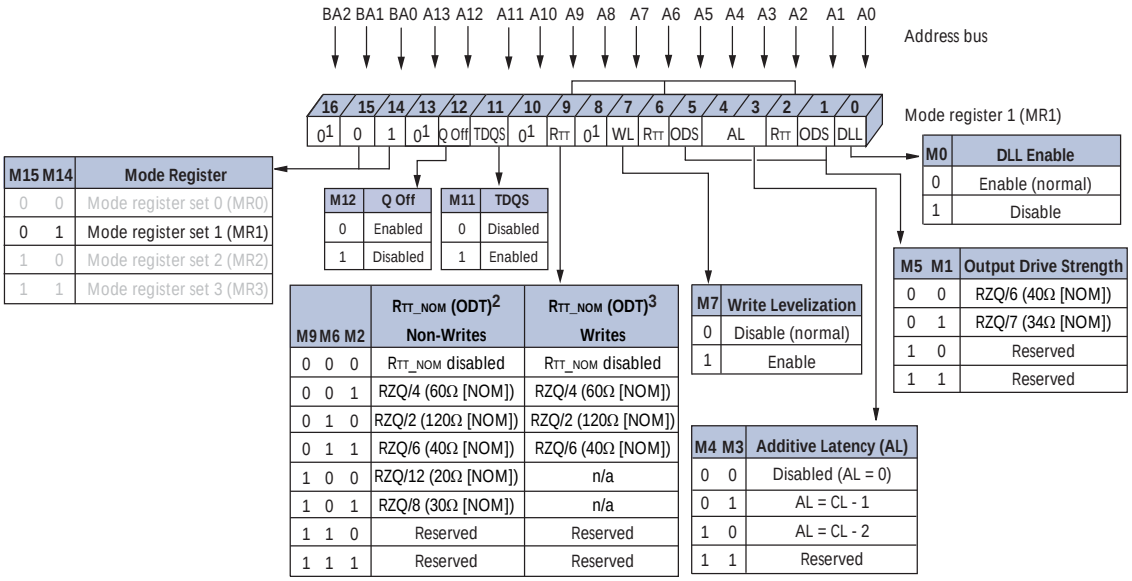
Mode Register 1 (MR1)

The mode register 1 (MR1) controls additional functions and features not available in the other mode registers: Q OFF (OUTPUT DISABLE), TDQS (for the x8 configuration only), DLL ENABLE/DLL DISABLE, RTT_NOM value (ODT), WRITE LEVELING, POSTED CAS ADDITIVE latency, and OUTPUT DRIVE STRENGTH. These functions are controlled via the bits shown in Figure 56. The MR1 register is programmed via the MRS command and retains the stored information until it is reprogrammed, until RESET# goes LOW, or until the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided it is performed correctly.

The MR1 register must be loaded when all banks are idle and no bursts are in progress. The controller must satisfy the specified timing parameters ^{t}MRD and ^{t}MOD before initiating a subsequent operation.

Figure 56: Mode Register 1 (MR1) Definition



Notes:
1. MR1[16, 13, 10, 8] are reserved for future use and must be programmed to "0."
2. During write leveling, if MR1[7] and MR1[12] are "1" then all RTT_NOM values are available for use.
3. During write leveling, if MR1[7] is a "1," but MR1[12] is a "0," then only RTT_NOM write values are available for use.

DLL Enable/DLL Disable

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command, as shown in Figure 56. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering self refresh mode, the DLL is automatically disabled when entering SELF REFRESH operation and is automatically reenabled and reset upon exit of SELF REFRESH operation. If the DLL is disabled prior to entering self refresh mode, the DLL remains disabled even upon exit of SELF REFRESH operation until it is reenabled and reset.

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The DRAM is not tested to check—nor does Micron warrant compliance with—normal mode timings or functionality when the DLL is disabled. An attempt has been made to have the DRAM operate in the normal mode where reasonably possible when the DLL has been disabled; however, by industry standard, a few known exceptions are defined:

1. ODT is not allowed to be used.
2. The output data is no longer edge-aligned to the clock.
3. CL and CWL can only be six clocks.

When the DLL is disabled, timing and functionality can vary from the normal operation specifications when the DLL is enabled (see "DLL Disable Mode" on page 96). Disabling the DLL also implies the need to change the clock frequency (see "Input Clock Frequency Change" on page 99).

Output Drive Strength

The DDR3 SDRAM uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5, 1]. RZQ/7 (34Ω [NOM]) is the primary output driver impedance setting for DDR3 SDRAM devices. To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and $V_{SS}Q$. The value of the resistor must be 240Ω ±1 percent.

The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation, and all data sheet timings and current specifications are met during an update.

To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up, the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined by MR1[12], as shown in Figure 56 on page 113. When enabled (MR1[12] = 0), all outputs (DQ, DQS, DQS#) function when in the normal mode of operation. When disabled (MR1[12] = 1), all DDR3 SDRAM outputs (DQ and DQS, DQS#) are tristated. The output disable feature is intended to be used during I_{DD} characterization of the READ current and during ^{t}DQSS margining (write leveling) only.

TDQS Enable

Termination data strobe (TDQS) is a feature of the x8 DDR3 SDRAM configuration, which provides termination resistance (R_{TT}), that may be useful in some system configurations. TDQS is not supported in x4 or x16 configurations. When enabled via the mode register (MR1[11]), the R_{TT} that is applied to DQS and DQS# is also applied to TDQS and TDQS#. In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance R_{TT} only. The OUTPUT DATA STROBE function of RDQS is not provided by TDQS; thus, R_{ON} does not apply to TDQS and TDQS#. The TDQS and DM functions share the same ball. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided, and the TDQS# ball is not used. The TDQS function is available in the x8 DDR3 SDRAM configuration only and must be disabled via the mode register for the x4 and x16 configurations.

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On-Die Termination

ODT resistance R_{TT_NOM} is defined by MR1[9, 6, 2] (see Figure 56 on page 113). The R_{TT} termination value applies to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls. DDR3 supports multiple R_{TT} termination values based on RZQ/*n* where *n* can be 2, 4, 6, 8, or 12 and RZQ is 240Ω.

Unlike DDR2, DDR3 ODT must be turned off prior to reading data out and must remain off during a READ burst. R_{TT_NOM} termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access, or when it is not in self refresh mode. Additionally, write accesses with dynamic ODT enabled (R_{TT_WR}) temporarily replaces R_{TT_NOM} with R_{TT_WR}.

The actual effective termination, R_{TT_EFF}, may be different from the R_{TT} targeted due to nonlinearity of the termination. For R_{TT_EFF} values and calculations (see "On-Die Termination (ODT)" on page 160).

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on/off ODT for any or all devices. The ODT input control pin is used to determine when R_{TT} is turned on (ODTL on) and off (ODTL off), assuming ODT has been enabled via MR1[9, 6, 2].

Timings for ODT are detailed in "On-Die Termination (ODT)" on page 160.

WRITE LEVELING

The WRITE LEVELING function is enabled by MR1[7], as shown in Figure 56 on page 113. Write leveling is used (during initialization) to deskew the DQS strobe to clock offset as a result of fly-by topology designs. For better signal integrity, DDR3 SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks.

The fly-by topology benefits from a reduced number of stubs and their lengths. However, fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM on the DIMM. Controllers will have a difficult time maintaining ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications without supporting write leveling in systems which use fly-by topology-based modules. Write leveling timing and detailed operation information is provided in “Write Leveling” on page 101.

POSTED CAS ADDITIVE Latency (AL)

AL is supported to make the command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. MR1[4, 3] define the value of AL as shown in Figure 57 on page 116. MR1[4, 3] enable the user to program the DDR3 SDRAM with an AL = 0, CL - 1, or CL - 2.

With this feature, the DDR3 SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank prior to ^{t}RCD (MIN). The only restriction is ACTIVATE to READ or WRITE + AL ≥ ^{t}RCD (MIN) must be satisfied. Assuming ^{t}RCD (MIN) = CL, a typical application using this feature sets AL = CL - 1^{t}CK = ^{t}RCD (MIN) - 1 ^{t}CK. The READ or WRITE command is held for the time of the AL before it is released internally to the DDR3 SDRAM device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL), RL = AL + CL. WRITE latency (WL) is the sum of CAS WRITE latency and AL, WL = AL + CWL (see "Mode Register 2 (MR2)" on page 116). Examples of READ and WRITE latencies are shown in Figure 57 on page 116 and Figure 59 on page 117.

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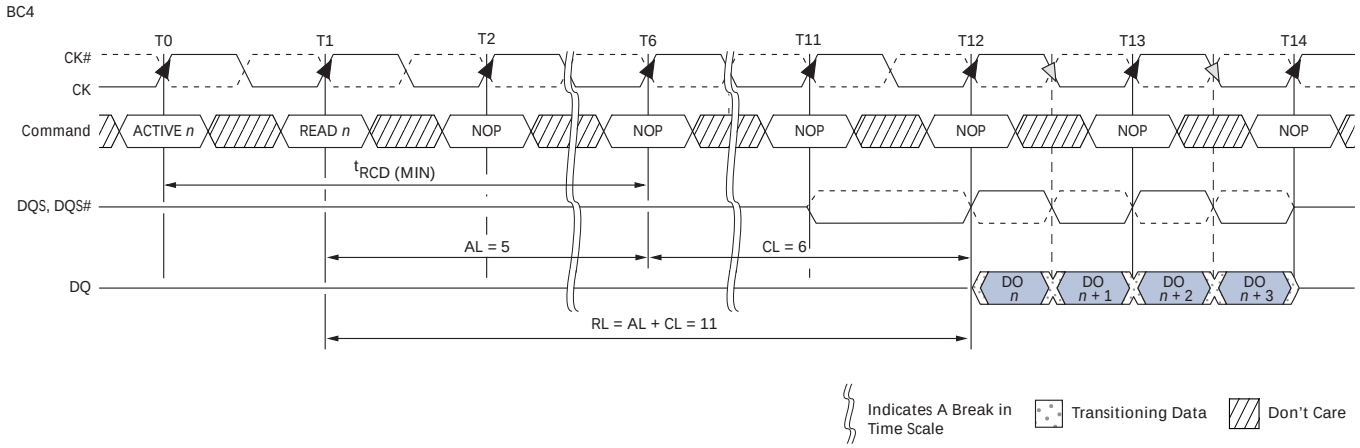
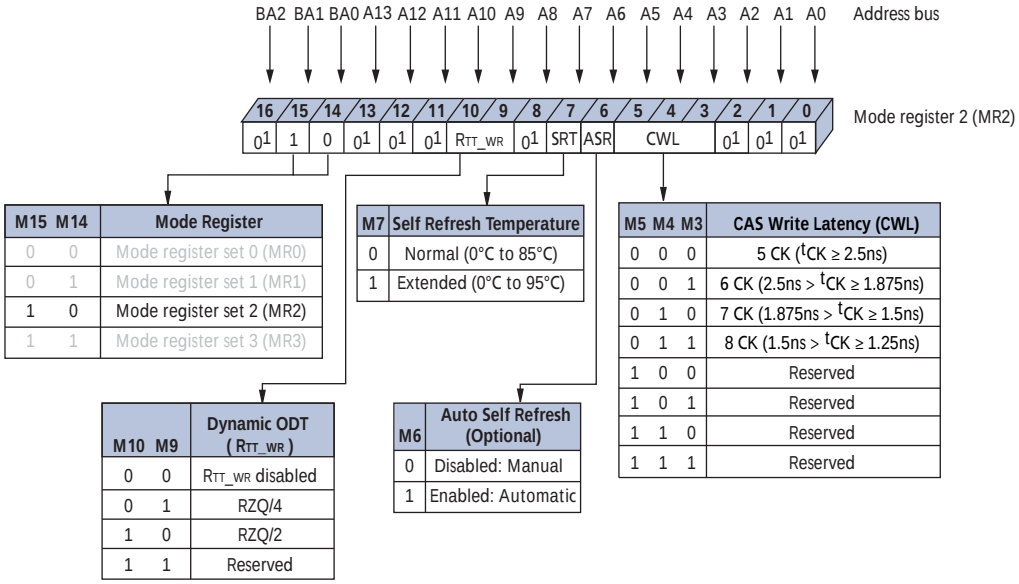
Figure 57: READ Latency (AL = 5, CL = 6)



Mode Register 2 (MR2)

The mode register 2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT), and DYNAMIC ODT (RTT_WR). These functions are controlled via the bits shown in Figure 58. The MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is performed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time ^{t}MRD and ^{t}MOD before initiating a subsequent operation.

Figure 58: Mode Register 2 (MR2) Definition



M15	M14	Mode Register
0	0	Mode register set 0 (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M7	Self Refresh Temperature
0	Normal (0°C to 85°C)
1	Extended (0°C to 95°C)

M5	M4	M3	CAS Write Latency (CWL)
0	0	0	5 CK (^{t}CK ≥ 2.5ns)
0	0	1	6 CK (2.5ns > ^{t}CK ≥ 1.875ns)
0	1	0	7 CK (1.875ns > ^{t}CK ≥ 1.5ns)
0	1	1	8 CK (1.5ns > ^{t}CK ≥ 1.25ns)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M10	M9	Dynamic ODT (RTT_WR)
0	0	RTT_WR disabled
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

M6	Auto Self Refresh (Optional)
0	Disabled: Manual
1	Enabled: Automatic

Notes: 1. MR2[16, 13:11, 8, and 2:0] are reserved for future use and must all be programmed to "0."

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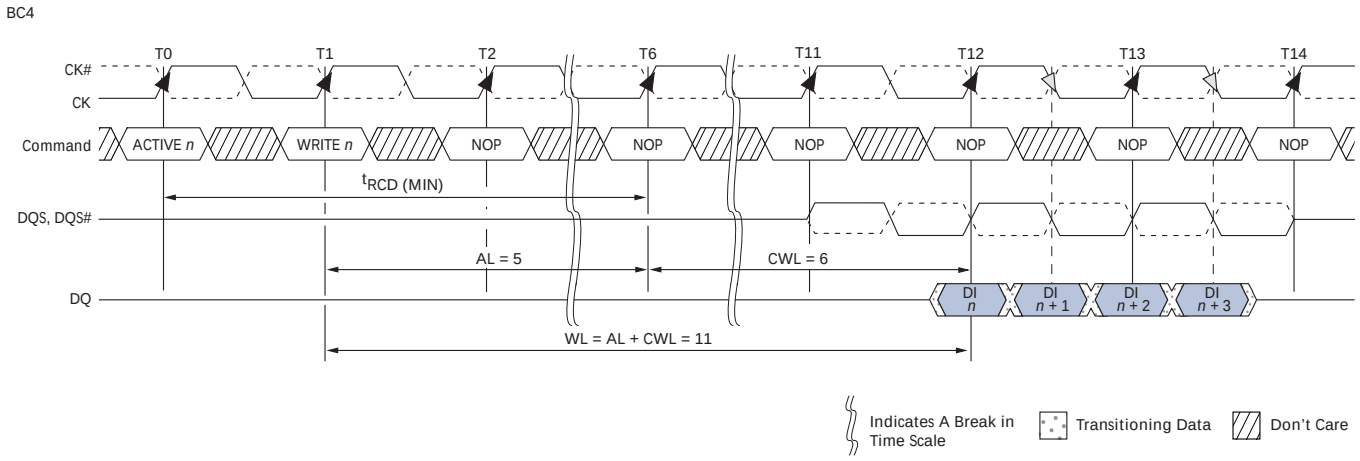
CAS Write Latency (CWL)

CWL is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal write to the latching of the first data in. CWL must be correctly set to the corresponding operating clock frequency (see Figure 58 on page 116). The overall WRITE latency (WL) is equal to CWL + AL (Figure 56 on page 113), as shown in Figure 59.

Figure 59: CAS Write Latency



AUTO SELF REFRESH (ASR)

Mode register MR2[6] is used to disable/enable the ASR function.

When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1X refresh rate). In the disabled mode, ASR requires the user to ensure the DRAM never exceeds a T_C of 85°C while in self refresh unless the user enables the SRT feature listed below when the T_C is between 85°C and 95°C.

Enabling ASR assumes the DRAM self refresh rate is changed automatically from 1X to 2X when the case temperature exceeds 85°C. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode.

The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if ASR is enabled, the standard self refresh current specifications do not apply (see "Extended Temperature Usage" on page 150).

SELF REFRESH TEMPERATURE (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1X refresh rate). In the disabled mode, SRT requires the user to ensure the DRAM never exceeds a T_C of 85°C while in self refresh mode unless the user enables ASR.

When SRT is enabled, the DRAM self refresh is changed internally from 1X to 2X, regardless of the case temperature. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode. The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if SRT is enabled, the standard self refresh current specifications do not apply (see "Extended Temperature Usage" on page 150).

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SRT vs. ASR

If the normal case temperature limit of 85°C is not exceeded, then neither SRT nor ASR is required, and both can be disabled throughout operation. However, if the extended temperature option of 95°C is needed, the user is required to provide a 2X refresh rate during (manual) refresh and to enable either the SRT or the ASR to ensure self refresh is performed at the 2X rate.

SRT forces the DRAM to switch the internal self refresh rate from 1X to 2X. Self refresh is performed at the 2X refresh rate regardless of the case temperature.

ASR automatically switches the DRAM's internal self refresh rate from 1X to 2X. However, while in self refresh mode, ASR enables the refresh rate to automatically adjust between 1X to 2X over the supported temperature range. One other disadvantage with ASR is the DRAM cannot always switch from a 1X to a 2X refresh rate at an exact case temperature of 85°C. Although the DRAM will support data integrity when it switches from a 1X to a 2X refresh rate, it may switch at a lower temperature than 85°C.

Since only one mode is neccesary, SRT and ASR cannot be enabled at the same time.

DYNAMIC ODT

The dynamic ODT (R_{TT_WR}) feature is defined by MR2[10, 9]. Dynamic ODT is enabled when a value is selected. This new DDR3 SDRAM feature enables the ODT termination value to change without issuing an MRS command, essentially changing the ODT termination "on-the-fly."

With dynamic ODT (R_{TT_WR}) enabled, the DRAM switches from normal ODT (R_{TT_NOM}) to dynamic ODT (R_{TT_WR}) when beginning a WRITE burst and subsequently switches back to ODT (R_{TT_NOM}) at the completion of the WRITE burst. If R_{TT_NOM} is disabled, the R_{TT_NOM} value will be High-Z. Special timing parameters must be adhered to when dynamic ODT (R_{TT_WR}) is enabled: $ODTL_{CNW}$, $ODTL_{CNW}4$, $ODTL_{CNW}8$, ODTH4, ODTH8, and ^{t}ADC.

Dynamic ODT is only applicable during WRITE cycles. If ODT (R_{TT_NOM}) is disabled, dynamic ODT (R_{TT_WR}) is still permitted. R_{TT_NOM} and R_{TT_WR} can be used independent of one other. Dynamic ODT is not available during write leveling mode, regardless of the state of ODT (R_{TT_NOM}). For details on dynamic ODT operation, refer to "On-Die Termination (ODT)" on page 160.

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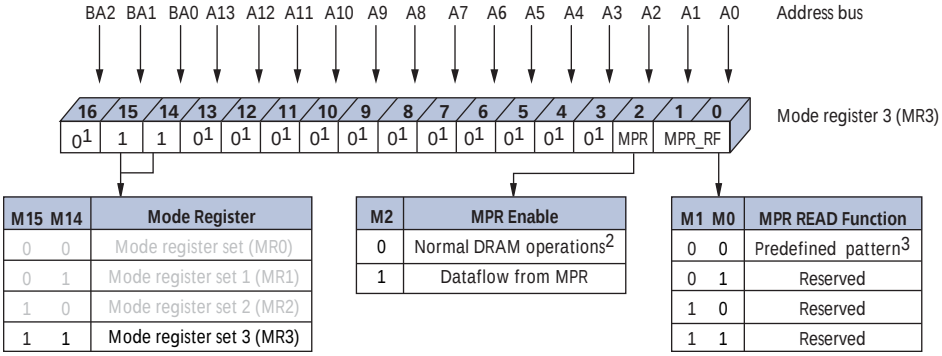
Mode Register 3 (MR3)

The mode register 3 (MR3) controls additional functions and features not available in the other mode registers. Currently defined is the MULTIPURPOSE REGISTER (MPR). This function is controlled via the bits shown in Figure 60. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed again or until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided it is performed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time ^{t}MRD and ^{t}MOD before initiating a subsequent operation.

Figure 60: Mode Register 3 (MR3) Definition



M15	M14	Mode Register
0	0	Mode register set (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M2	MPR Enable
0	Normal DRAM operations[2]
1	Dataflow from MPR

M1	M0	MPR READ Function
0	0	Predefined pattern[3]
0	1	Reserved
1	0	Reserved
1	1	Reserved

Notes:
1. MR3[16 and 13:4] are reserved for future use and must all be programmed to "0."
2. When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
3. Intended to be used for READ synchronization.

MULTIPURPOSE REGISTER (MPR)

The MULTIPURPOSE REGISTER function is used to output a predefined system timing calibration bit sequence. Bit 2 is the master bit that enables or disables access to the MPR register, and bits 1 and 0 determine which mode the MPR is placed in. The basic concept of the multipurpose register is shown in Figure 61 on page 120.

If MR3[2] is a "0," then the MPR access is disabled, and the DRAM operates in normal mode. However, if MR3[2] is a "1," then the DRAM no longer outputs normal read data but outputs MPR data as defined by MR3[0, 1]. If MR3[0, 1] is equal to "00," then a predefined read pattern for system calibration is selected.

To enable the MPR, the MRS command is issued to MR3, and MR3[2] = 1 (see Table 69 on page 120). Prior to issuing the MRS command, all banks must be in the idle state (all banks are precharged, and ^{t}RP is met). When the MPR is enabled, any subsequent READ or RDAP commands are redirected to the multipurpose register. The resulting operation when either a READ or a RDAP command is issued, is defined by MR3[1:0] when the MPR is enabled (see Table 70 on page 121). When the MPR is enabled, only READ or RDAP commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3[2] = 0). Power-down mode, self refresh, and any other nonREAD/RDAP command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

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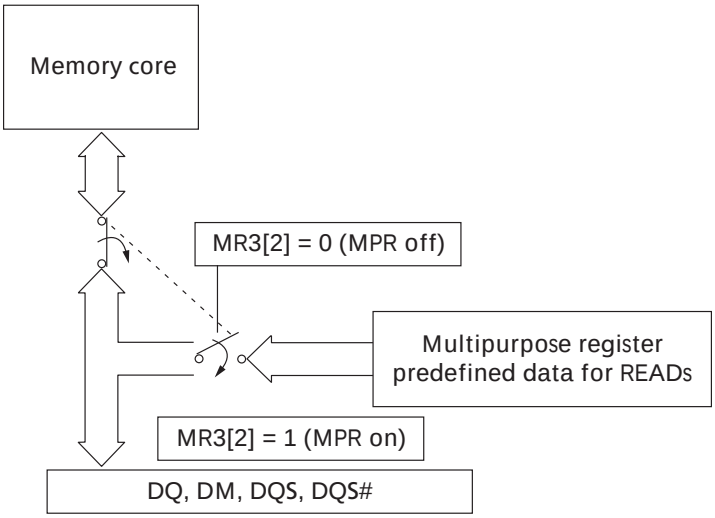
Figure 61: Multipurpose Register (MPR) Block Diagram



Notes: 1. A predefined data pattern can be read out of the MPR with an external READ command.
2. MR3[2] defines whether the data flow comes from the memory core or the MPR. When the data flow is defined, the MPR contents can be read out continuously with a regular READ or RDAP command.

Table 69: MPR Functional Description of MR3 Bits

MR3[2]	MR3[1:0]	
MPR	**MPR READ Function**	**Function**
0	"Don't Care"	Normal operation, no MPR transaction All subsequent READs come from the DRAM memory array All subsequent WRITEs go to the DRAM memory array
1	A[1:0] (see Table 70 on page 121)	Enable MPR mode, subsequent READ/RDAP commands defined by bits 1 and 2

MPR Functional Description

The MPR JEDEC definition allows for either a prime DQ (DQ0 on a x4 and a x8; on a x16, DQ0 = lower byte and DQ8 = upper byte) to output the MPR data with the remaining DQ driven LOW or for all DQ to output the MPR data. The MPR readout supports fixed READ burst and READ burst chop (MRS and OTF via A12/BC#) with regular READ latencies and AC timings applicable, provided the DLL is locked as required.

MPR addressing for a valid MPR read is as follows:

- A[1:0] must be set to "00" as the burst order is fixed per nibble
- A2 selects the burst order:
  - BL8, A2 is set to "0," and the burst order is fixed to 0, 1, 2, 3, 4, 5, 6, 7
- For burst chop 4 cases, the burst order is switched on the nibble base and:
  - A2 = 0; burst order = 0, 1, 2, 3
  - A2 = 1; burst order = 4, 5, 6, 7
- Burst order bit 0 (the first bit) is assigned to LSB, and burst order bit 7 (the last bit) is assigned to MSB
- A[9:3] are a "Don't Care"
- A10 is a "Don't Care"

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- A11 is a “Don’t Care”
- A12: Selects burst chop mode on-the-fly, if enabled within MR0
- A13 is a “Don’t Care”
- BA[2:0] are a “Don’t Care”

MPR Register Address Definitions and Bursting Order

The MPR currently supports a single data format. This data format is a predefined read pattern for system calibration. The predefined pattern is always a repeating 0–1 bit pattern.

Examples of the different types of predefined READ pattern bursts are shown in Figure 62 on page 122, Figure 63 on page 123, Figure 64 on page 124, and Figure 65 on page 125.

Table 70: MPR Readouts and Burst Order Bit Mapping

MR3[2]	MR3[1:0]	Function	Burst Length	Read A[2:0]	Burst Order and Data Pattern
1	00	READ predefined pattern for system calibration	BL8	000	Burst order: 0, 1, 2, 3, 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1, 0, 1, 0, 1
			BC4	000	Burst order: 0, 1, 2, 3 Predefined pattern: 0, 1, 0, 1
			BC4	100	Burst order: 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1
1	01	RFU	n/a	n/a	n/a
			n/a	n/a	n/a
			n/a	n/a	n/a
1	10	RFU	n/a	n/a	n/a
			n/a	n/a	n/a
			n/a	n/a	n/a
1	11	RFU	n/a	n/a	n/a
			n/a	n/a	n/a
			n/a	n/a	n/a

Notes: 1. Burst order bit 0 is assigned to LSB, and burst order bit 7 is assigned to MSB of the selected MPR agent.

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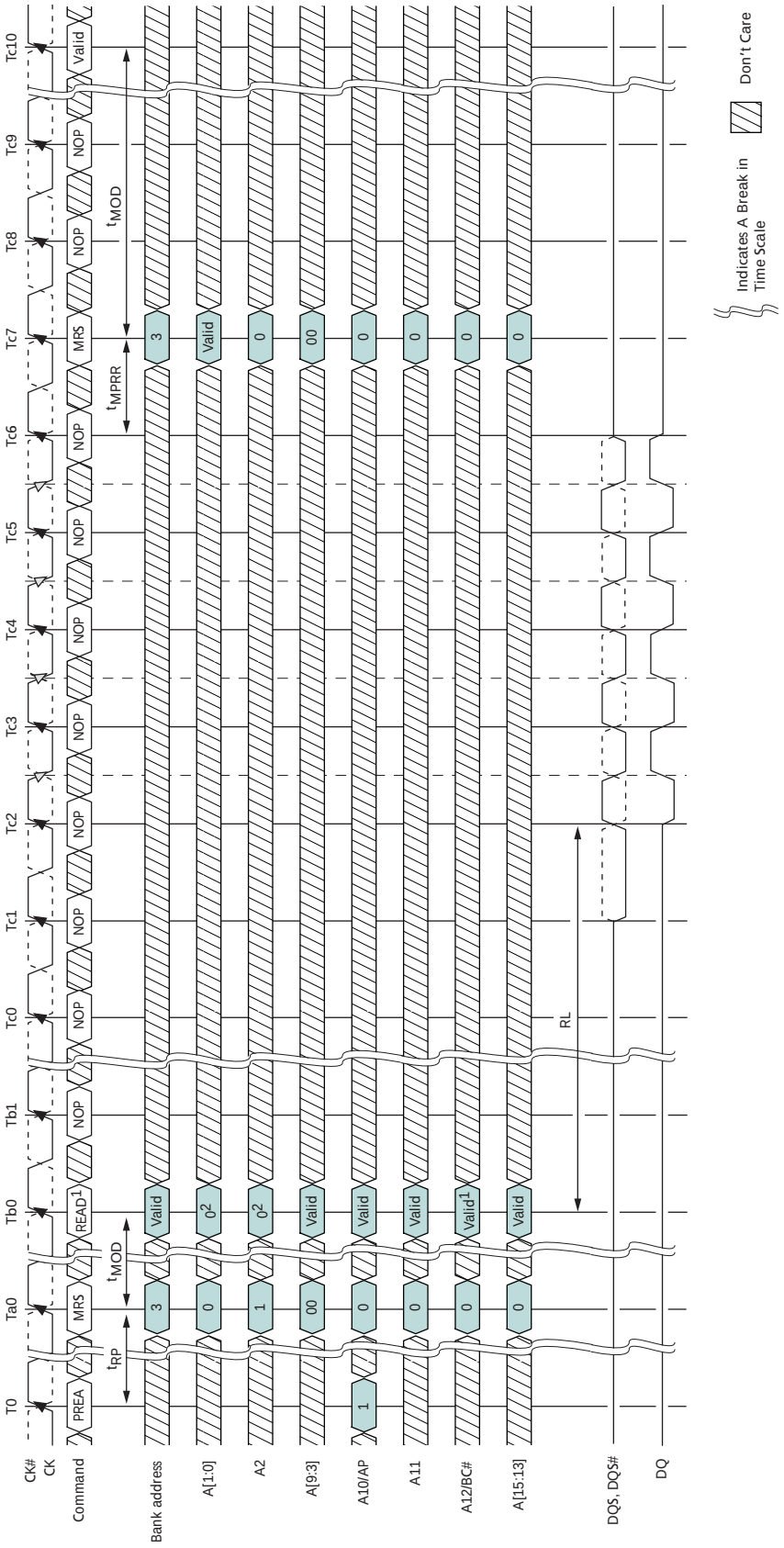
Figure 62: MPR System Read Calibration with BL8: Fixed Burst Order Single Readout



Notes:
1. READ with BL8 either by MRS or OTF.
2. Memory controller must drive 0 on A[2:0].

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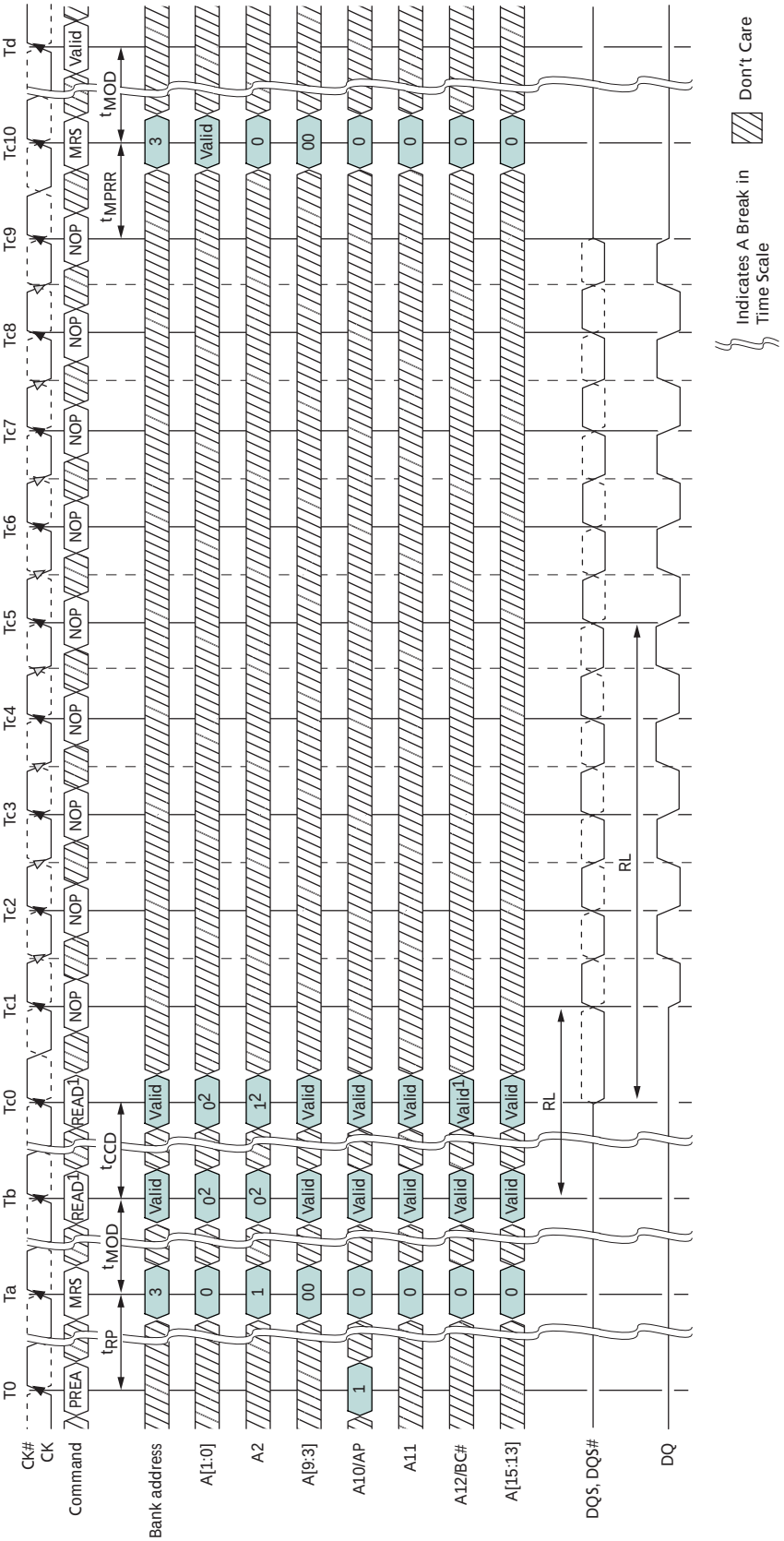
Figure 63: MPR System Read Calibration with BL8: Fixed Burst Order, Back-to-Back Readout



Notes:
1. READ with BL8 either by MRS or OTF.
2. Memory controller must drive 0 on A[2:0].

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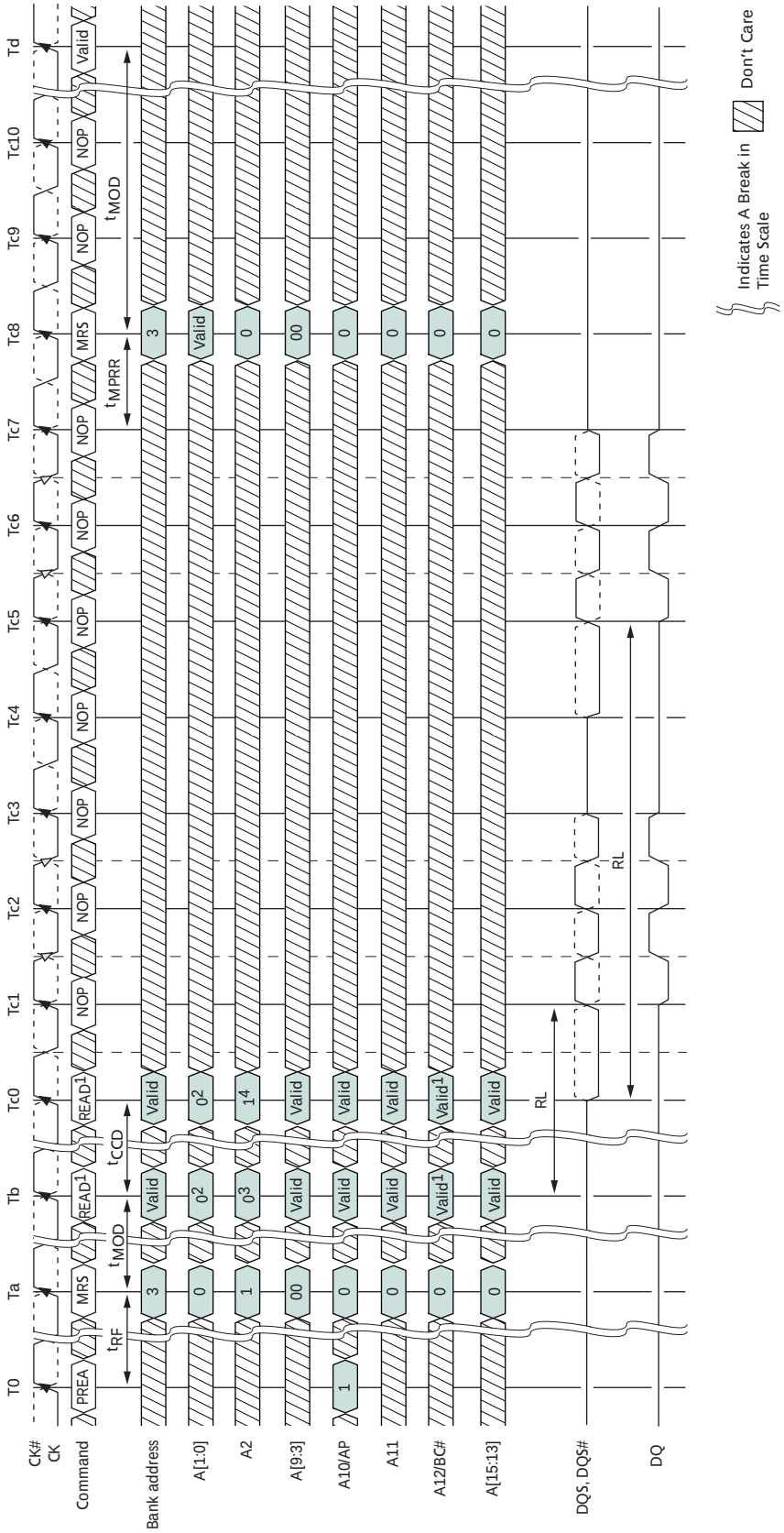
Figure 64: MPR System Read Calibration with BC4: Lower Nibble, Then Upper Nibble



Notes:
1. READ with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0].
3. A2 = 0 selects lower 4 nibble bits 0 . . . 3.
4. A2 = 1 selects upper 4 nibble bits 4 . . . 7.

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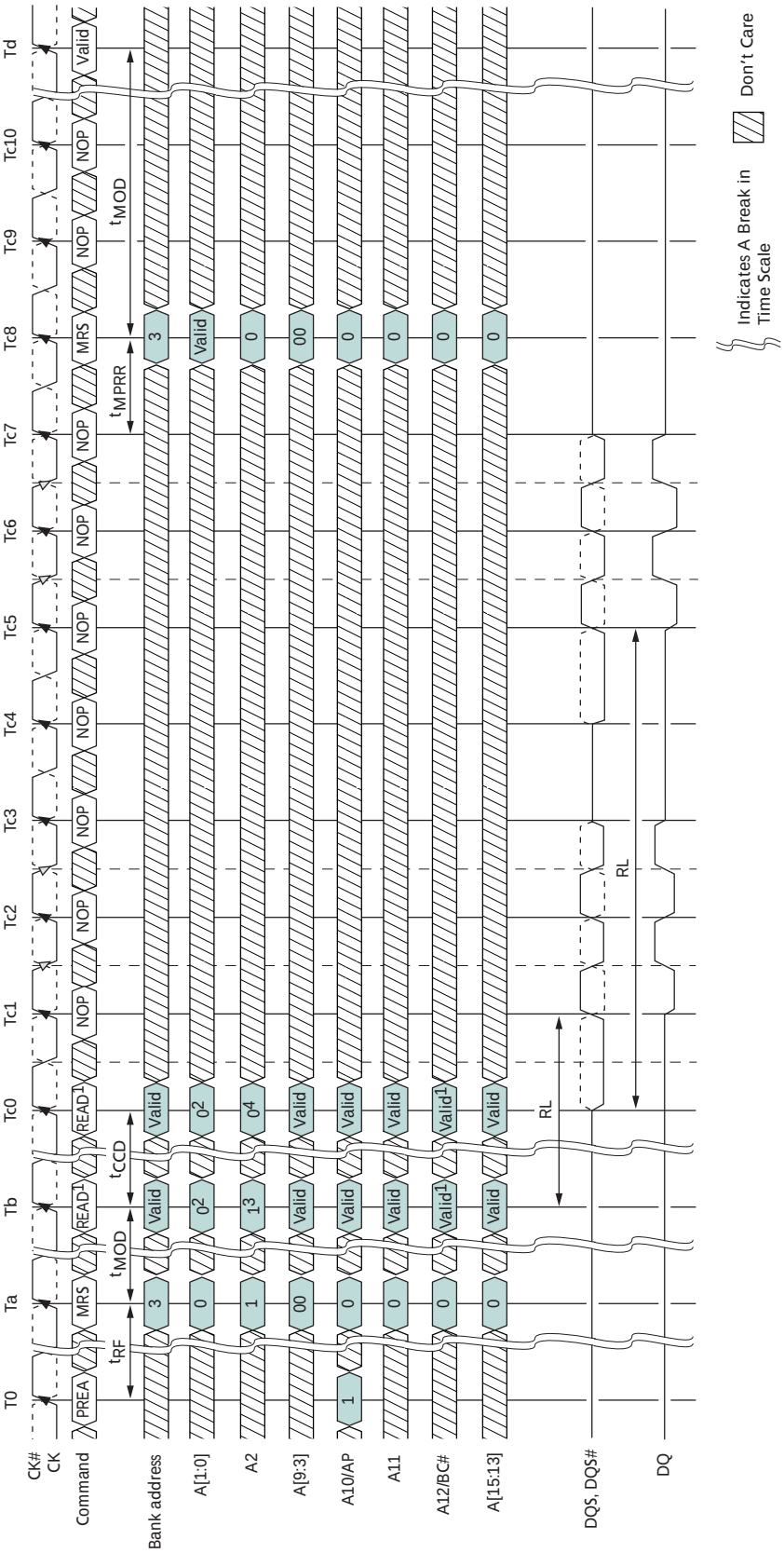
Figure 65: MPR System Read Calibration with BC4: Upper Nibble, Then Lower Nibble



Notes:
1. READ with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0].
3. A2 = 1 selects upper 4 nibble bits 4 . . . 7.
4. A2 = 0 selects lower 4 nibble bits 0 . . . 3.

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MPR Read Predefined Pattern

The predetermined read calibration pattern is a fixed pattern of 0, 1, 0, 1, 0, 1, 0, 1. The following is an example of using the read out predetermined read calibration pattern. The example is to perform multiple reads from the multipurpose register in order to do system level read timing calibration based on the predetermined and standardized pattern.

The following protocol outlines the steps used to perform the read calibration:

- Precharge all banks
- After ^{t}RP is satisfied, set MRS, MR3[2] = 1 and MR3[1:0] = 00. This redirects all subsequent reads and loads the predefined pattern into the MPR. As soon as ^{t}MRD and ^{t}MOD are satisfied, the MPR is available
- Data WRITE operations are not allowed until the MPR returns to the normal DRAM state
- Issue a read with burst order information (all other address pins are "Don't Care"):
  - A[1:0] = 00 (data burst order is fixed starting at nibble)
  - A2 = 0 (for BL8, burst order is fixed as 0, 1, 2, 3, 4, 5, 6, 7)
  - A12 = 1 (use BL8)
- After RL = AL + CL, the DRAM bursts out the predefined read calibration pattern (0, 1, 0, 1, 0, 1, 0, 1)
- The memory controller repeats the calibration reads until read data capture at memory controller is optimized
- After the last MPR READ burst and after ^{t}MPRR has been satisfied, issue MRS, MR3[2] = 0, and MR3[1:0] = "Don't Care" to the normal DRAM state. All subsequent read and write accesses will be regular reads and writes from/to the DRAM array
- When ^{t}MRD and ^{t}MOD are satisfied from the last MRS, the regular DRAM commands (such as activate a memory bank for regular read or write access) are permitted

MODE REGISTER SET (MRS)

The mode registers are loaded via inputs BA[2:0], A[13:0]. BA[2:0] determine which mode register is programmed:

- BA2 = 0, BA1 = 0, BA0 = 0 for MR0
- BA2 = 0, BA1 = 0, BA0 = 1 for MR1
- BA2 = 0, BA1 = 1, BA0 = 0 for MR2
- BA2 = 0, BA1 = 1, BA0 = 1 for MR3

The MRS command can only be issued (or reissued) when all banks are idle and in the precharged state (^{t}RP is satisfied and no data bursts are in progress). The controller must wait the specified time ^{t}MRD before initiating a subsequent operation such as an ACTIVATE command (see Figure 52 on page 108). There is also a restriction after issuing an MRS command with regard to when the updated functions become available. This parameter is specified by ^{t}MOD. Both ^{t}MRD and ^{t}MOD parameters are shown in Figure 52 on page 108 and Figure 53 on page 109. Violating either of these requirements will result in unspecified operation.

ZQ CALIBRATION

The ZQ CALIBRATION command is used to calibrate the DRAM output drivers (R_{ON}) and ODT values (R_{TT}) over process, voltage, and temperature, provided a dedicated 240Ω (±1 percent) external resistor is connected from the DRAM's ZQ ball to $V_{SS}Q$.

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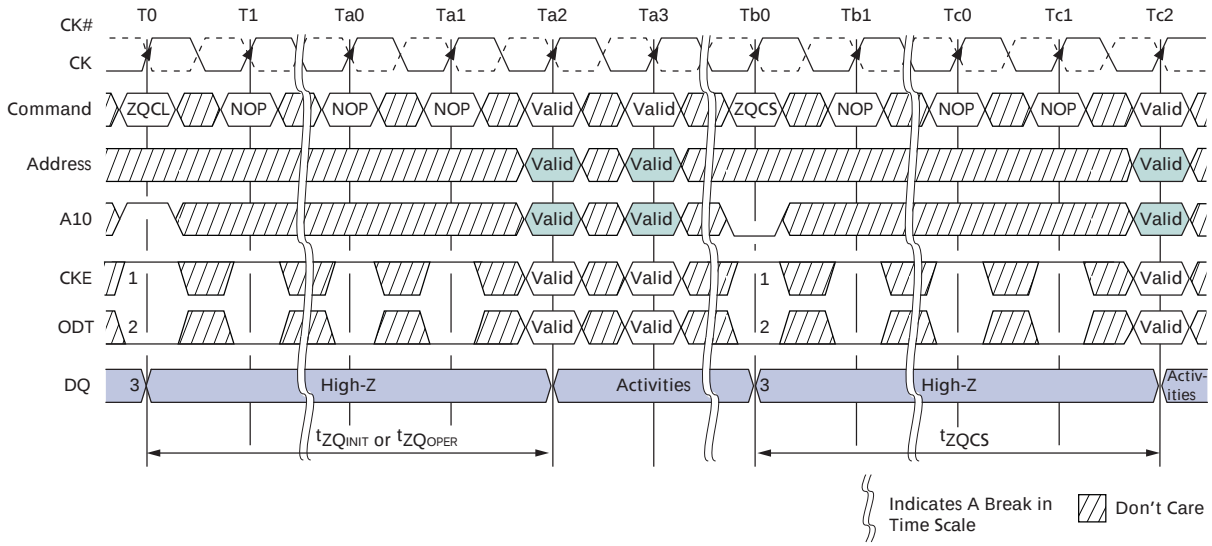
DDR3 SDRAM need a longer time to calibrate RON and ODT at power-up initialization and self refresh exit and a relatively shorter time to perform periodic calibrations. DDR3 SDRAM defines two ZQ CALIBRATION commands: ZQ CALIBRATION LONG (ZQCL) and ZQ CALIBRATION SHORT (ZQCS). An example of ZQ calibration timing is shown in Figure 66.

All banks must be precharged and ^{t}RP must be met before ZQCL or ZQCS commands can be issued to the DRAM. No other activities (other than another ZQCL or ZQCS command may be issued to another DRAM) can be performed on the DRAM channel by the controller for the duration of ^{t}ZQINIT or ^{t}ZQOPER . The quiet time on the DRAM channel helps accurately calibrate RON and ODT. After DRAM calibration is achieved, the DRAM should disable the ZQ ball's current consumption path to reduce power.

ZQ CALIBRATION commands can be issued in parallel to DLL RESET and locking time. Upon self refresh exit, an explicit ZQCL is required if ZQ calibration is desired.

In dual-rank systems that share the ZQ resistor between devices, the controller must not allow overlap of ^{t}ZQINIT, ^{t}ZQOPER, or ^{t}ZQCS between ranks.

Figure 66: ZQ Calibration Timing (ZQCL and ZQCS)



Notes:
1. CKE must be continuously registered HIGH during the calibration procedure.
2. ODT must be disabled via the ODT signal or the MRS during the calibration procedure.
3. All devices connected to the DQ bus should be High-Z during calibration.

ACTIVATE

Before any READ or WRITE commands can be issued to a bank within the DRAM, a row in that bank must be opened (activated). This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. However, if the additive latency is programmed correctly, a READ or WRITE command may be issued prior to ^{t}RCD (MIN). In this operation, the DRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank, but prior to ^{t}RCD (MIN) with the requirement that (ACTIVATE-to-READ/WRITE) + AL ≥ ^{t}RCD (MIN) (see "POSTED CAS ADDITIVE Latency (AL)" on page 115). ^{t}RCD (MIN) should be divided by the clock period and rounded up to

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the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles.

When at least one bank is open, any READ-to-READ command delay or WRITE-to-WRITE command delay is restricted to ^{t}CCD (MIN).

A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by ^{t}RRD. No more than four bank ACTIVATE commands may be issued in a given ^{t}FAW (MIN) period, and the ^{t}RRD (MIN) restriction still applies. The ^{t}FAW (MIN) parameter applies, regardless of the number of banks already opened or closed.

Figure 67: Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN)

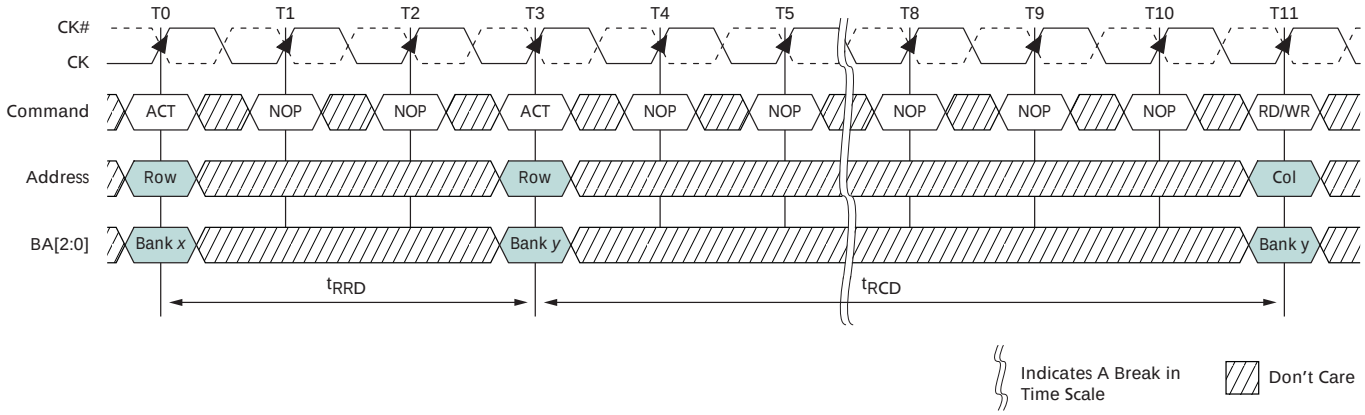
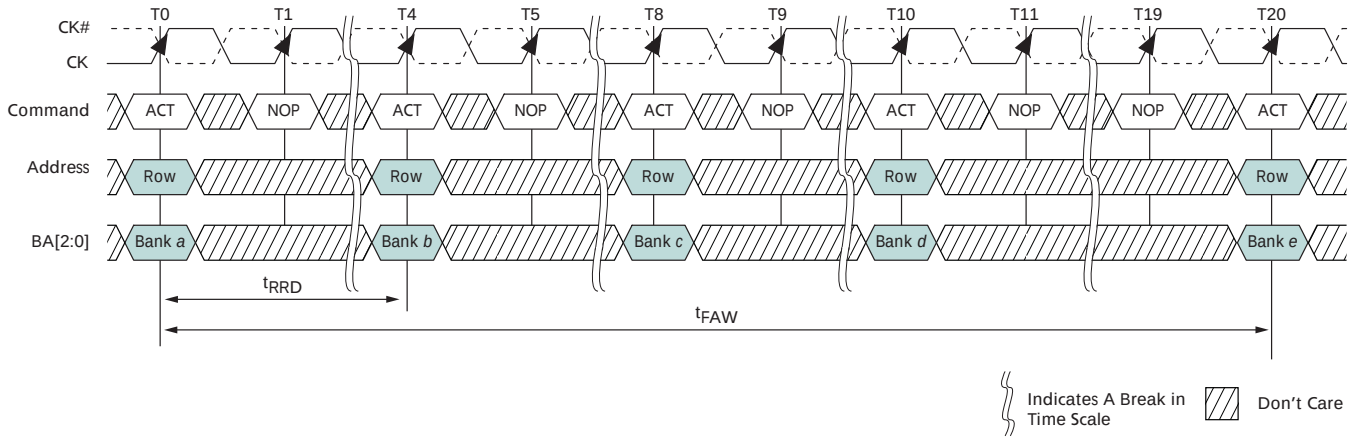


Figure 68: Example: ^{t}FAW



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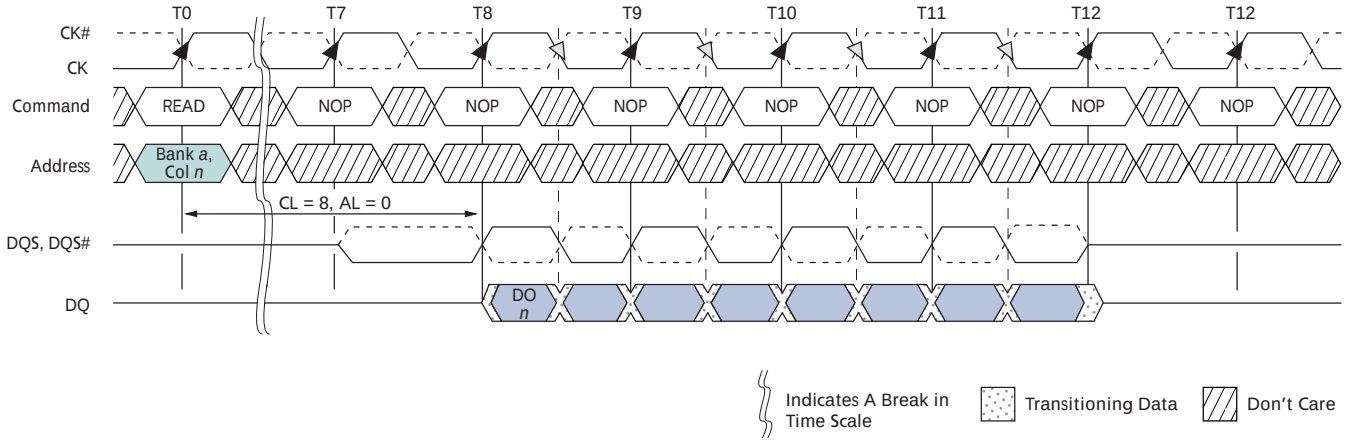
READ

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address is available READ latency (RL) clocks later. RL is defined as the sum of POSTED CAS ADDITIVE latency (AL) and CAS latency (CL) (RL = AL + CL). The value of AL and CL is programmable in the mode register via the MRS command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK#). Figure 69 shows an example of RL based on a CL setting of 8 and an AL setting of 0.

Figure 69: READ Latency



Notes: 1. DO *n* = data-out from column *n*.
2. Subsequent elements of data-out appear in the programmed order following DO *n*.

DQS, DQS# is driven by the DRAM along with the output data. The initial low state on DQS and HIGH state on DQS# is known as the READ preamble (^{t}RPRE). The low state on DQS and the HIGH state on DQS#, coincident with the last data-out element, is known as the READ postamble (^{t}RPST). Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), and the valid data window are depicted in Figure 80 on page 137. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) is also depicted in Figure 80 on page 137.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued ^{t}CCD cycles after the first READ command. This is shown for BL8 in Figure 70 on page 131. If BC4 is enabled, ^{t}CCD must still be met which will cause a gap in the data output, as shown in Figure 71 on page 131. Nonconsecutive read data is reflected in Figure 72 on page 132. DDR3 SDRAM do not allow interrupting or truncating any READ burst.

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Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst for BL8 is shown in Figure 73 on page 132 (BC4 is shown in Figure 74 on page 133). To ensure the read data is completed before the write data is on the bus, the minimum READ-to-WRITE timing is RL + ^{t}CCD - WL + 2^{t}CK.

A READ burst may be followed by a PRECHARGE command to the same bank provided auto precharge is not activated. The minimum READ-to-PRECHARGE command spacing to the same bank is four clocks and must also satisfy a minimum analog time from the READ command. This time is called ^{t}RTP (READ-to-PRECHARGE). ^{t}RTP starts AL cycles later than the READ command. Examples for BL8 are shown in Figure 75 on page 133 and BC4 in Figure 76 on page 134. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. The PRECHARGE command followed by another PRECHARGE command to the same bank is allowed. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

If A10 is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The DRAM starts an auto precharge operation on the rising edge which is AL + ^{t}RTP cycles after the READ command. DRAM support a ^{t}RAS lockout feature (see Figure 78 on page 134). If ^{t}RAS (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until ^{t}RAS (MIN) is satisfied. If ^{t}RTP (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until ^{t}RTP (MIN) is satisfied. In case the internal precharge is pushed out by ^{t}RTP, ^{t}RP starts at the point at which the internal precharge happens (not at the next rising clock edge after this event). The time from READ with auto precharge to the next ACTIVATE command to the same bank is AL + (^{t}RTP + ^{t}RP)*, where "*" means rounded up to the next integer. In any event, internal precharge does not start earlier than four clocks after the last 8*n*-bit prefetch.

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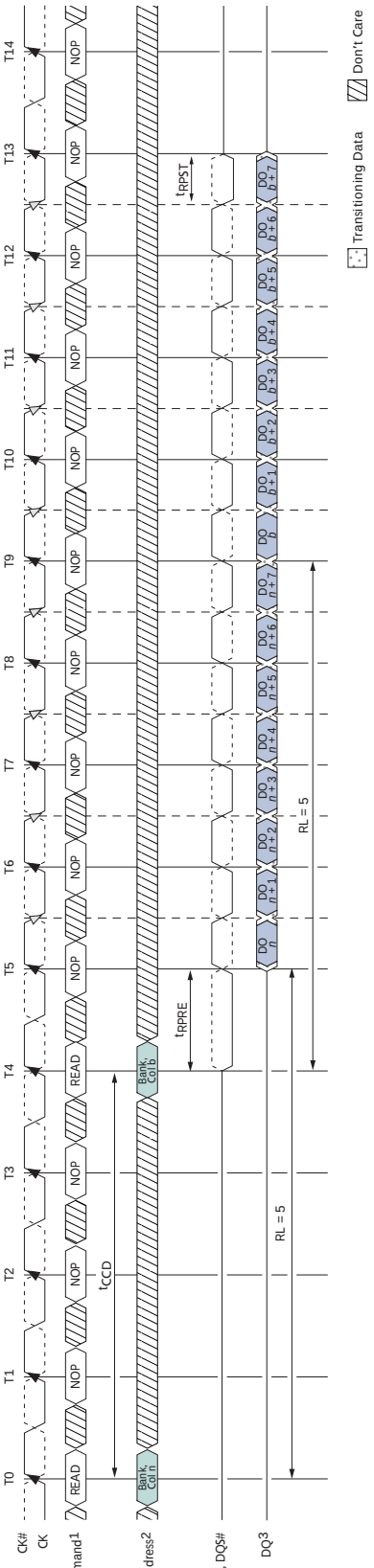
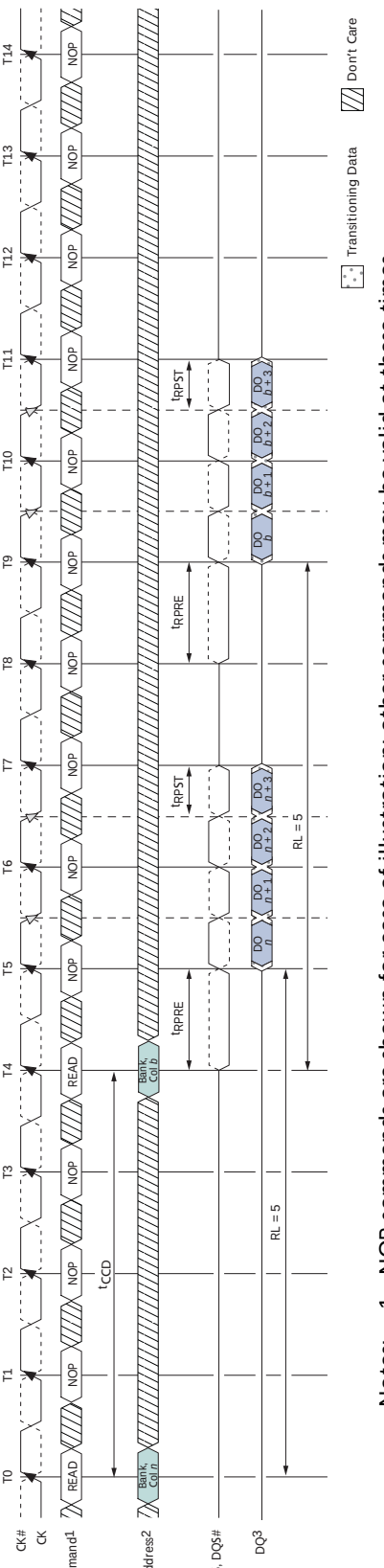
Figure 70: Consecutive READ Bursts (BL8)



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0 and T4.
3. DO *n* (or *b*) = data-out from column *n* (or column *b*).
4. BL8, RL = 5 (CL = 5, AL = 0).

Figure 71: Consecutive READ Bursts (BC4)



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 setting is activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ command at T0 and T4.
3. DO *n* (or *b*) = data-out from column *n* (or column *b*).
4. BC4, RL = 5 (CL = 5, AL = 0).

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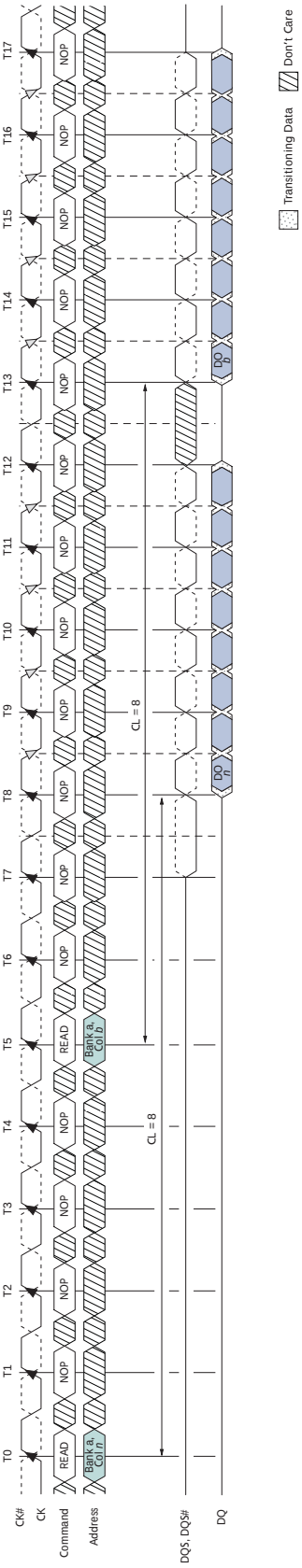
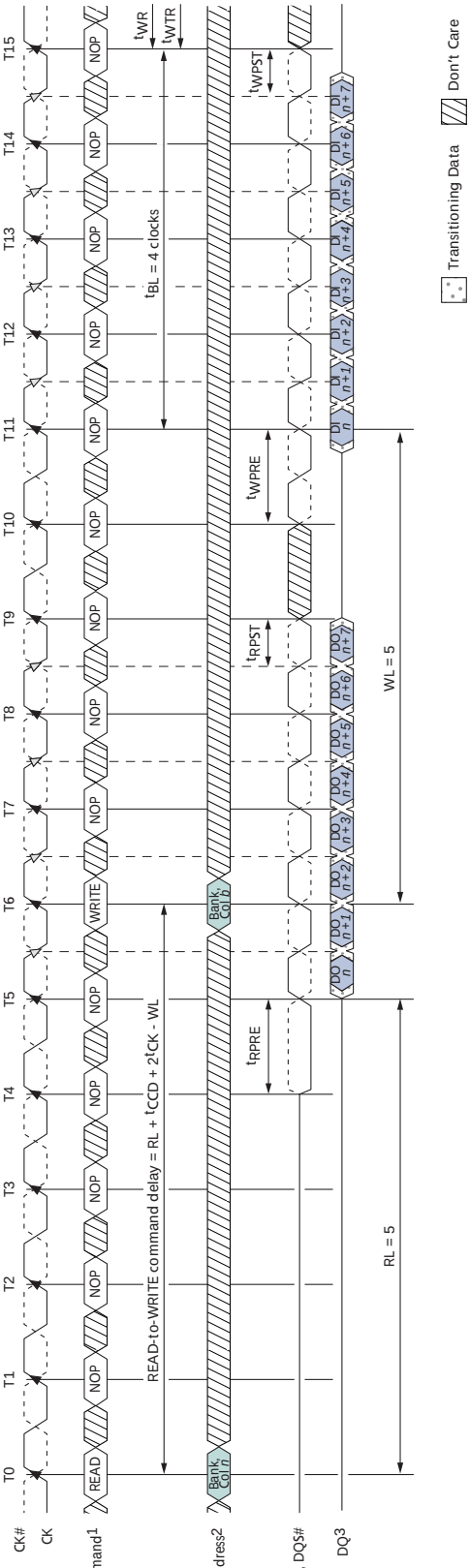
Figure 72: Nonconsecutive READ Bursts



Notes:
1. AL = 0, RL = 8.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. Seven subsequent elements of data-out appear in the programmed order following DO *n*.
4. Seven subsequent elements of data-out appear in the programmed order following DO *b*.

Figure 73: READ (BL8) to WRITE (BL8)



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the READ command at T0, and the WRITE command at T6.
3. DO *n* = data-out from column, DI *b* = data-in for column *b*.
4. BL8, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

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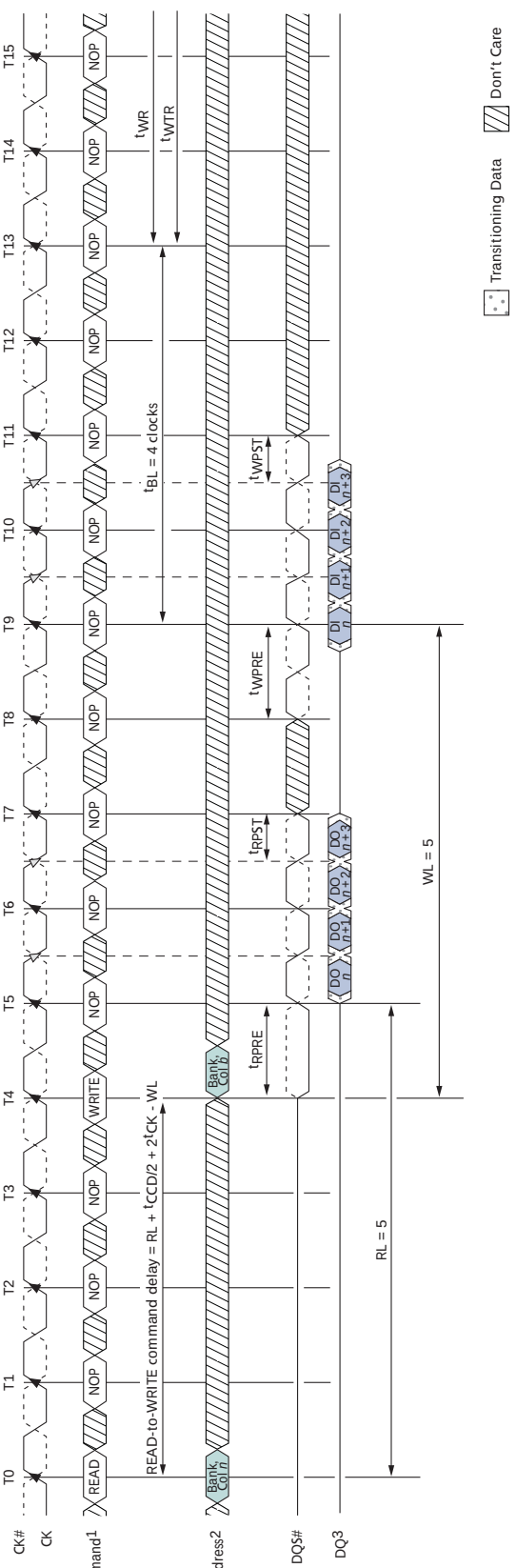
Figure 74: READ (BC4) to WRITE (BC4) OTF



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 OTF setting is activated by MR0[1:0] and A12 = 0 during READ command at T0 and WRITE command at T4.
3. DO *n* = data-out from column *n*; DI *n* = data-in from column *b*.
4. BC4, RL = 5 (AL - 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

Figure 75: READ to PRECHARGE (BL8)

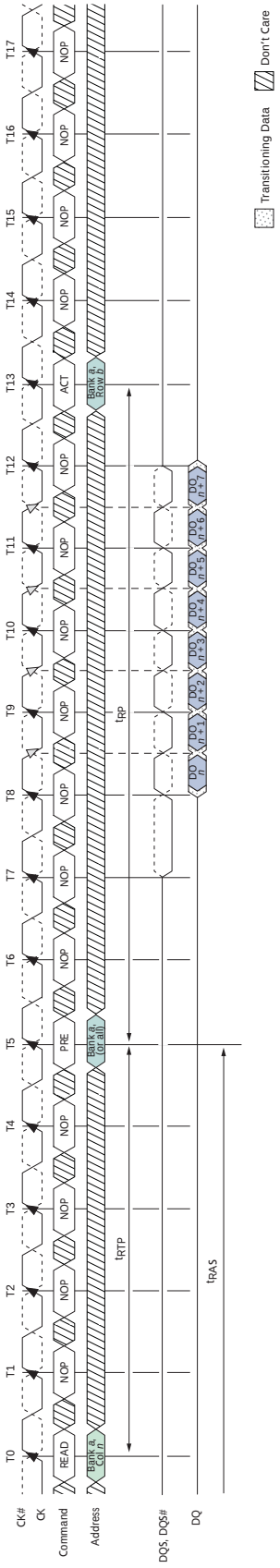


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Figure 76: READ to PRECHARGE (BC4)

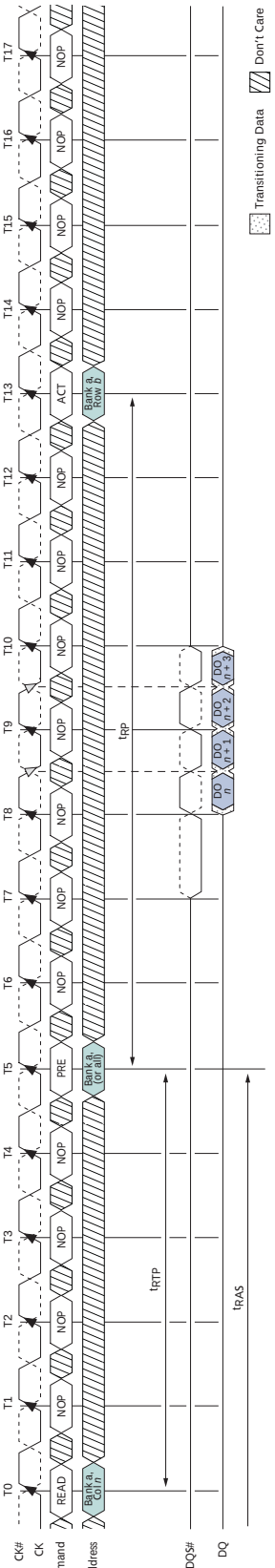


Figure 77: READ to PRECHARGE (AL = 5, CL = 6)

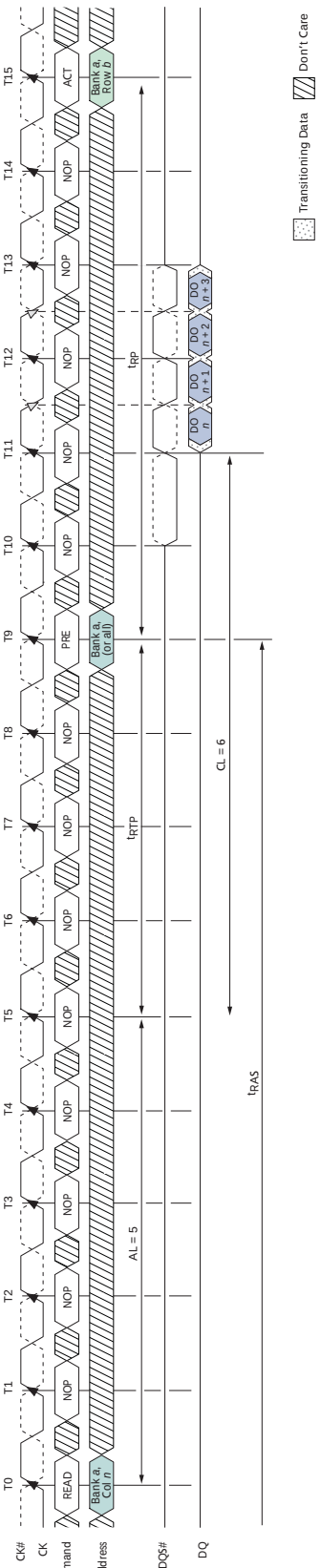
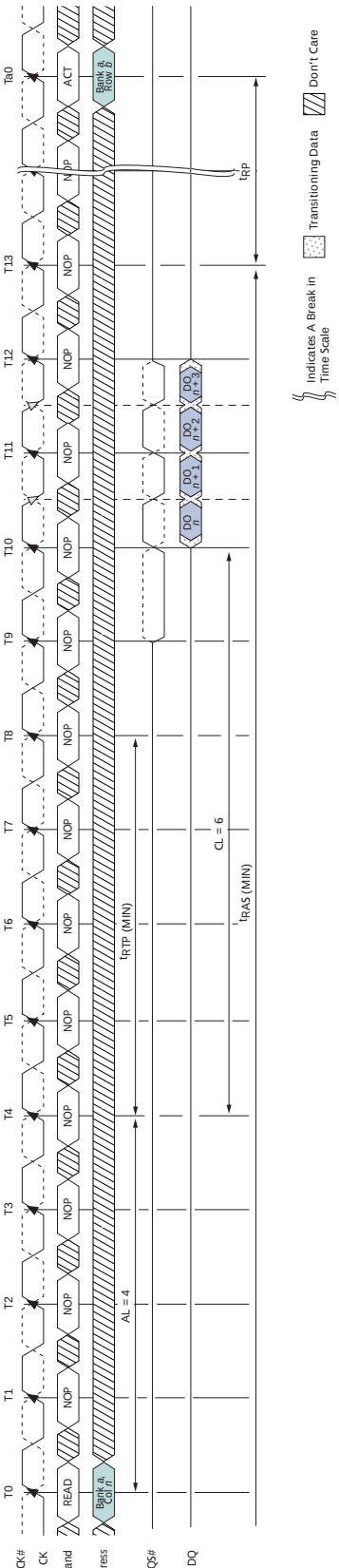


Figure 78: READ with Auto Precharge (AL = 4, CL = 6)



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A DQS to DQ output timing is shown in Figure 79 on page 136. The DQ transitions between valid data outputs must be within ^{t}DQSQ of the crossing point of DQS, DQS#. DQS must also maintain a minimum HIGH and LOW time of ^{t}QSH and ^{t}QSL. Prior to the READ preamble, the DQ balls will either be floating or terminated depending on the status of the ODT signal.

Figure 80 on page 137 shows the strobe-to-clock timing during a READ. The crossing point DQS, DQS# must transition within ±^{t}DQSCK of the clock crossing point. The data out has no timing relationship to clock, only to DQS, as shown in Figure 80 on page 137.

Figure 80 on page 137 also shows the READ preamble and postamble. Normally, both DQS and DQS# are High-Z to save power ($V_{DD}Q$). Prior to data output from the DRAM, DQS is driven LOW and DQS# is HIGH for ^{t}RPRE. This is known as the READ preamble.

The READ postamble, ^{t}RPST, is one half clock from the last DQS, DQS# transition. During the READ postamble, DQS is driven LOW and DQS# is HIGH. When complete, the DQ will either be disabled or will continue terminating depending on the state of the ODT signal. Figure 85 on page 140 demonstrates how to measure ^{t}RPST.

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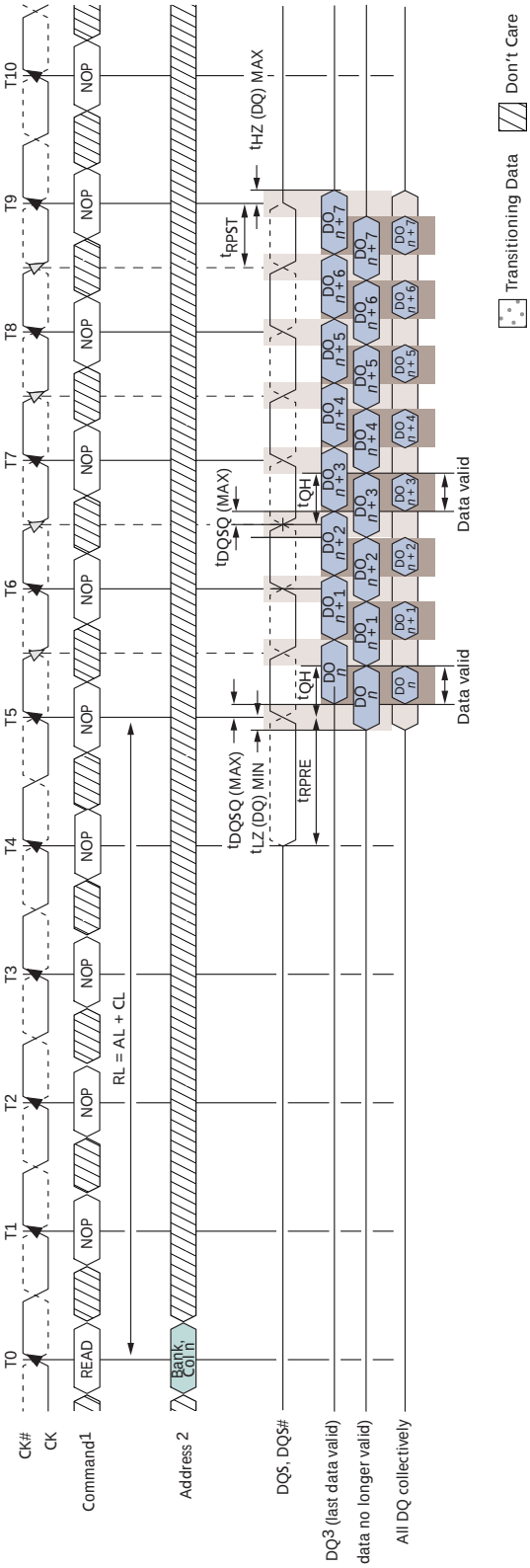
Figure 79: Data Output Timing – ^{t}DQSQ and Data Valid Window



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1, 0] = 0, 0 or MR0[0, 1] = 0, 1 and A12 = 1 during READ command at T0.
3. DO *n* = data-out from column *n*.
4. BL8, RL = 5 (AL = 0, CL = 5).
5. Output timings are referenced to V_{DDQ}/2 and DLL on and locked.
6. ^{t}DQSQ defines the skew between DQS, DQS# to data and does not define DQS, DQS# to clock.
7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

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^{t}HZ and ^{t}LZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving ^{t}HZ (DQS) and ^{t}HZ (DQ) or begins driving ^{t}LZ (DQS), ^{t}LZ (DQ). Figure 81 shows a method to calculate the point when the device is no longer driving ^{t}HZ (DQS) and ^{t}HZ (DQ) or begins driving ^{t}LZ (DQS), ^{t}LZ (DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters ^{t}LZ (DQS), ^{t}LZ (DQ), ^{t}HZ (DQS), and ^{t}HZ (DQ) are defined as single-ended.

Figure 80: Data Strobe Timing – READs

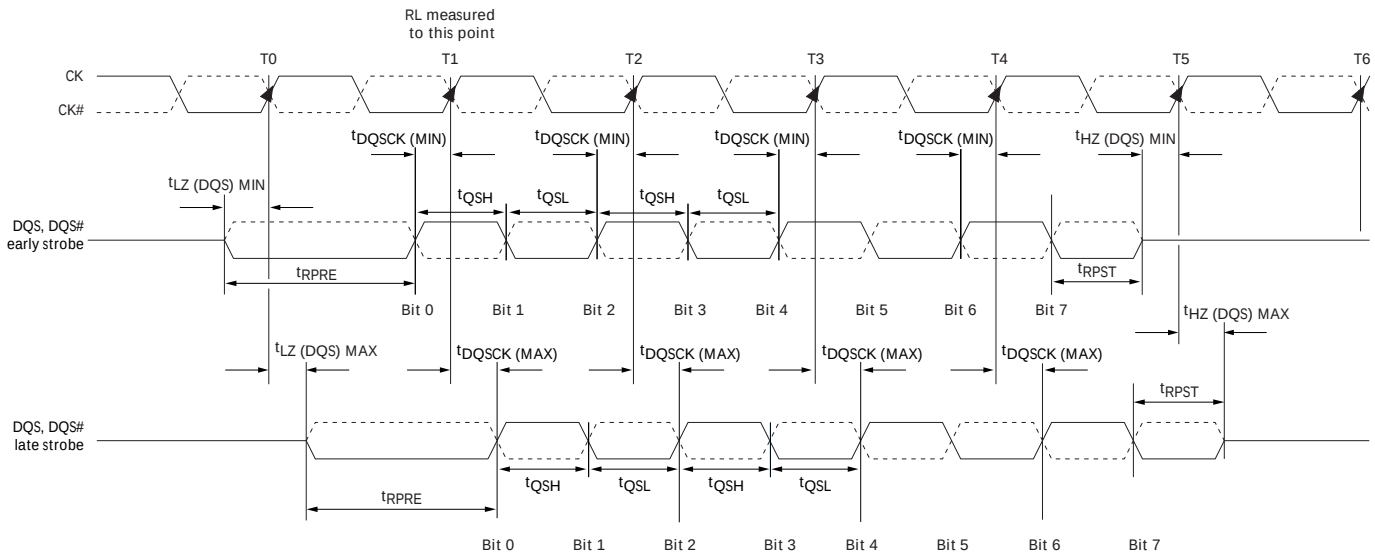
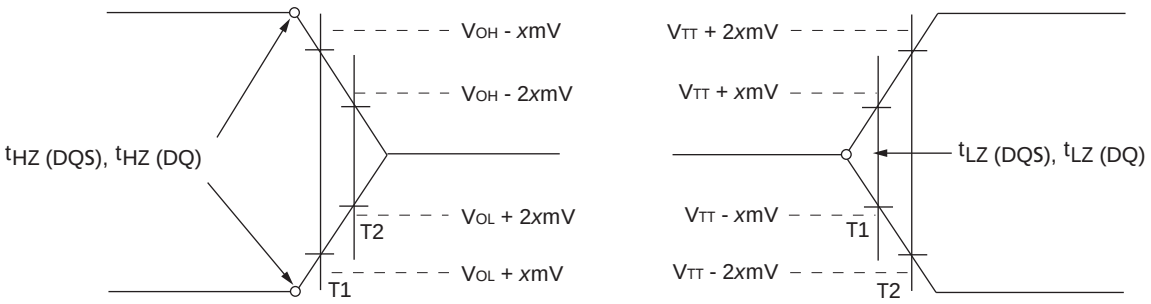


Figure 81: Method for Calculating ^{t}LZ and ^{t}HZ



^{t}HZ (DQS), ^{t}HZ (DQ) end point = 2 × T1 - T2

^{t}LZ (DQS), ^{t}LZ (DQ) begin point = 2 × T1 - T2

Notes:
1. Within a burst, the rising strobe edge is not necessarily fixed at ^{t}DQSCK (MIN) or ^{t}DQSCK (MAX). Instead, the rising strobe edge can vary between ^{t}DQSCK (MIN) and ^{t}DQSCK (MAX).
2. The DQS high pulse width is defined by ^{t}QSH, and the DQS low pulse width is defined by ^{t}QSL. Likewise, ^{t}LZ (DQS) MIN and ^{t}HZ (DQS) MIN are not tied to ^{t}DQSCK (MIN) (early strobe case) and ^{t}LZ (DQS) MAX and ^{t}HZ (DQS) MAX are not tied to ^{t}DQSCK (MAX) (late strobe case); however, they tend to track one another.
3. The minimum pulse width of the READ preamble is defined by ^{t}RPRE (MIN). The minimum pulse width of the READ postamble is defined by ^{t}RPST (MIN).

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Figure 82: ^{t}RPRE Timing

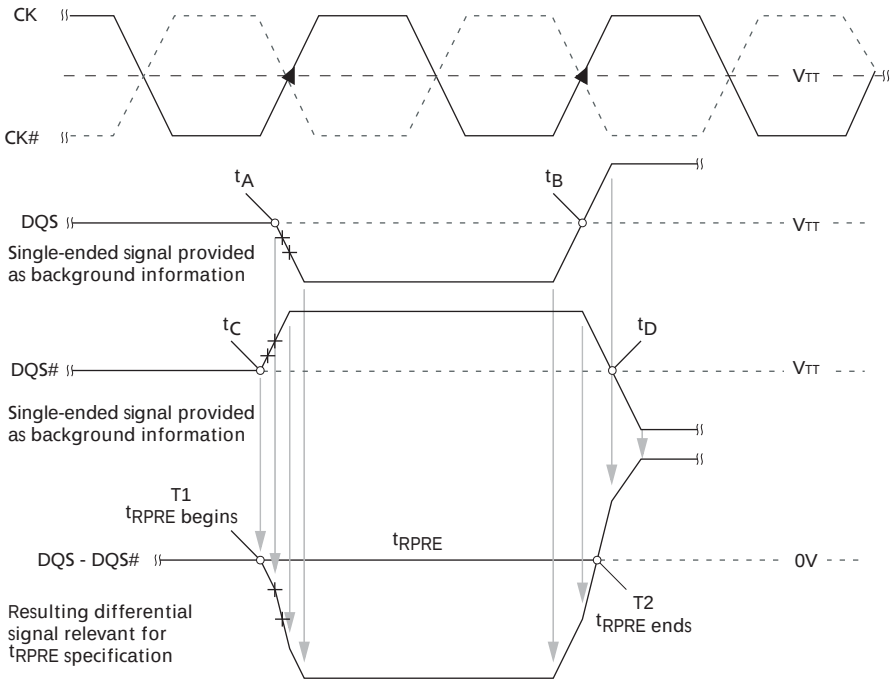
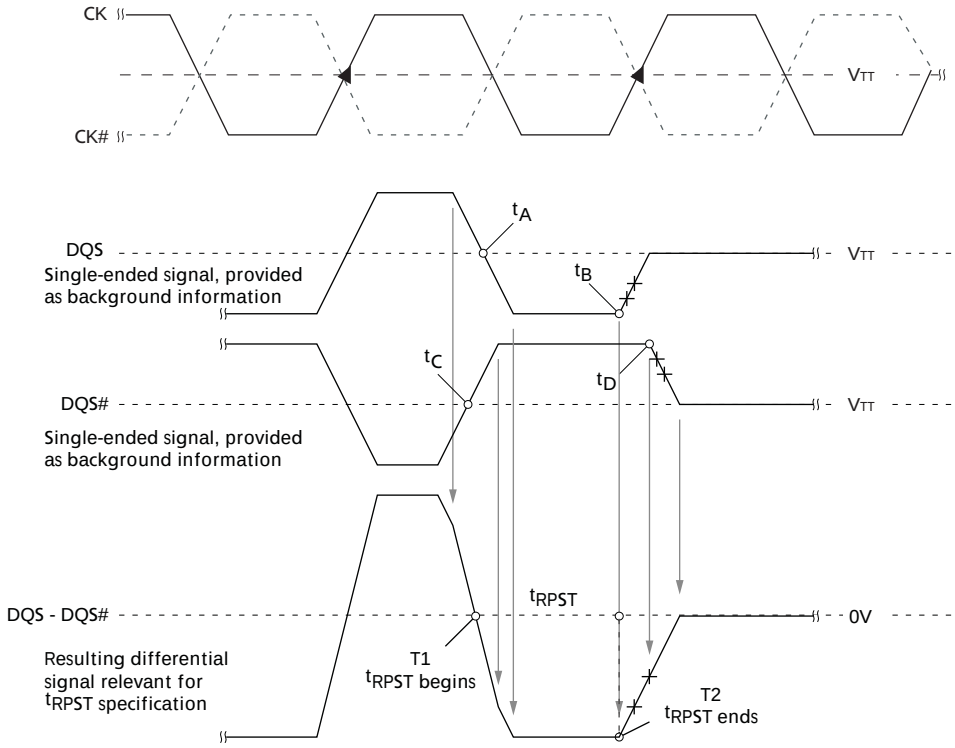


Figure 83: ^{t}RPST Timing



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WRITE

WRITE bursts are initiated with a WRITE command. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst. If auto precharge is not selected, the row will remain open for subsequent accesses. After a WRITE command has been issued, the WRITE burst may not be interrupted. For the generic WRITE commands used in Figure 86 on page 141 through Figure 94 on page 146, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered on a rising edge of DQS following the WRITE latency (WL) clocks later and subsequent data elements will be registered on successive edges of DQS. WRITE latency (WL) is defined as the sum of POSTED CAS ADDITIVE latency (AL) and CAS WRITE latency (CWL): WL = AL + CWL. The values of AL and CWL are programmed in the MR0 and MR2 registers, respectively. Prior to the first valid DQS edge, a full cycle is needed (including a dummy crossover of DQS, DQS#) and specified as the WRITE preamble shown in Figure 86 on page 141. The half cycle on DQS following the last data-in element is known as the WRITE postamble.

The time between the WRITE command and the first valid edge of DQS is WL clocks $\pm^{t}$DQSS. Figure 87 on page 142 through Figure 94 on page 146 show the nominal case where ^{t}DQSS = 0ns; however, Figure 86 on page 141 includes ^{t}DQSS (MIN) and ^{t}DQSS (MAX) cases.

Data may be masked from completing a WRITE using data mask. The mask occurs on the DM ball aligned to the write data. If DM is LOW, the write completes normally. If DM is HIGH, that bit of data is masked.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z, and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide a continuous flow of input data. The new WRITE command can be ^{t}CCD clocks following the previous WRITE command. The first data element from the new burst is applied after the last element of a completed burst. Figures 87 and 88 on page 142 show concatenated bursts. An example of nonconsecutive WRITEs is shown in Figure 89 on page 143.

Data for any WRITE burst may be followed by a subsequent READ command after ^{t}WTR has been met (see Figures 90 and 91 on page 144 and Figure 92 on page 145).

Data for any WRITE burst may be followed by a subsequent PRECHARGE command providing ^{t}WR has been met, as shown in Figure 93 on page 146 and Figure 94 on page 146.

Both ^{t}WTR and ^{t}WR starting time may vary depending on the mode register settings (fixed BC4, BL8 vs. OTF).

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Figure 84: ^{t}WPRE Timing

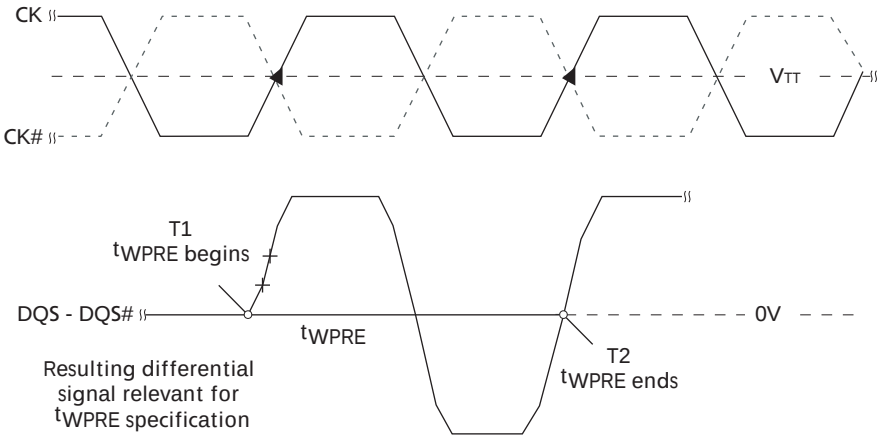

Figure 85: ^{t}WPST Timing

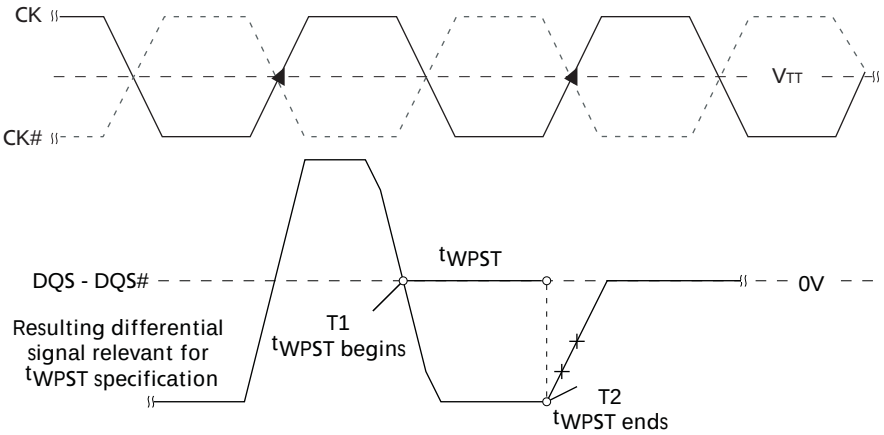

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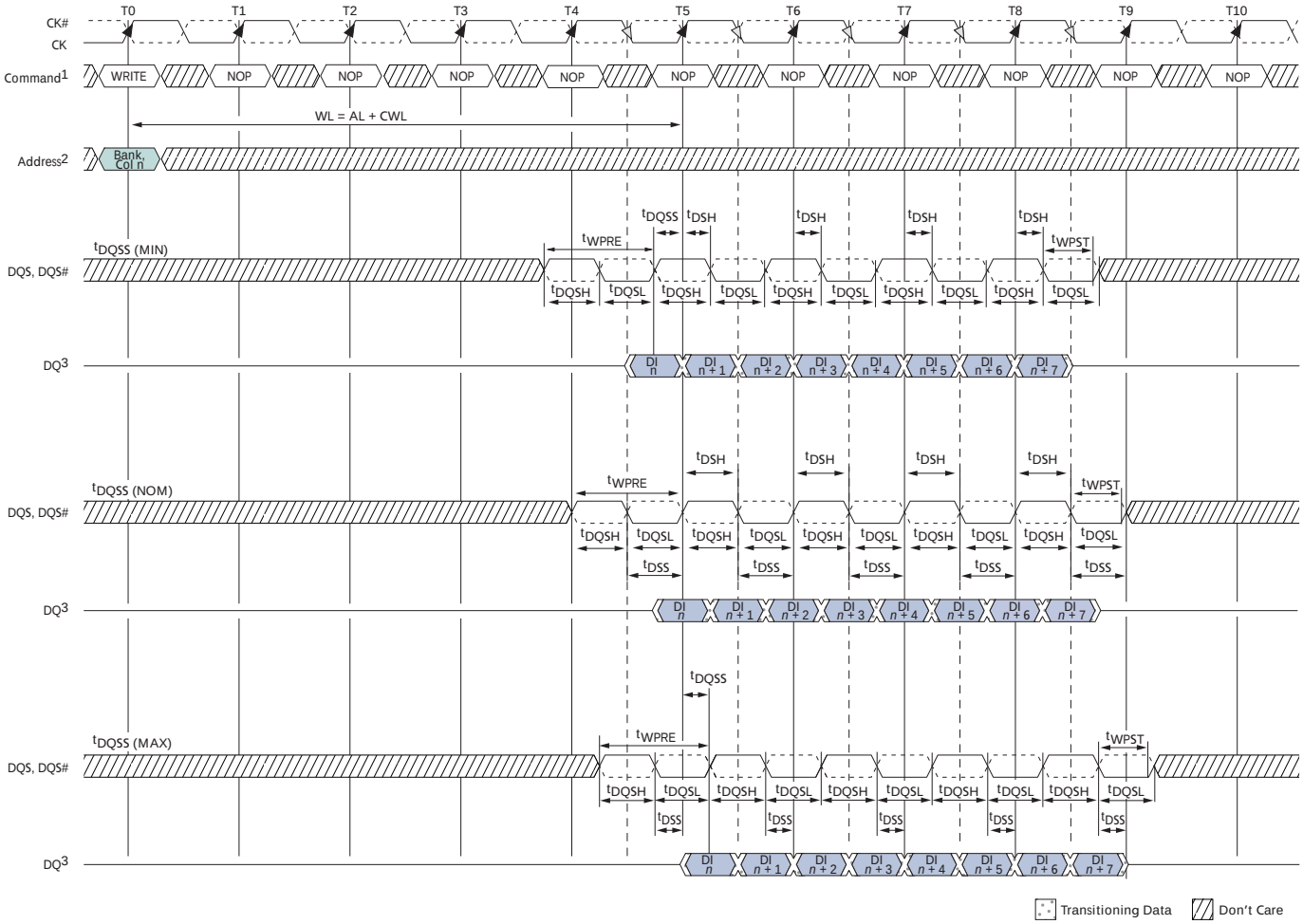
Figure 86: Write Burst



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE command at T0.
3. DI *n* = data-in for column *n*.
4. BL8, WL = 5 (AL = 0, CWL = 5).
5. ^{t}DQSS must be met at each rising clock edge.
6. ^{t}WPST is usually depicted as ending at the crossing of DQS, DQS#; however, ^{t}WPST actually ends when DQS no longer drives LOW and DQS# no longer drives HIGH.

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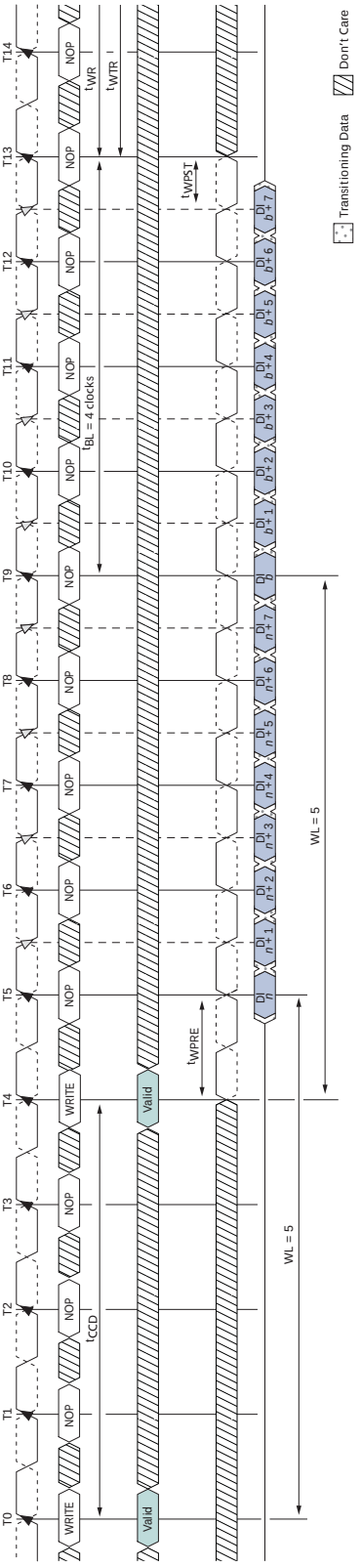
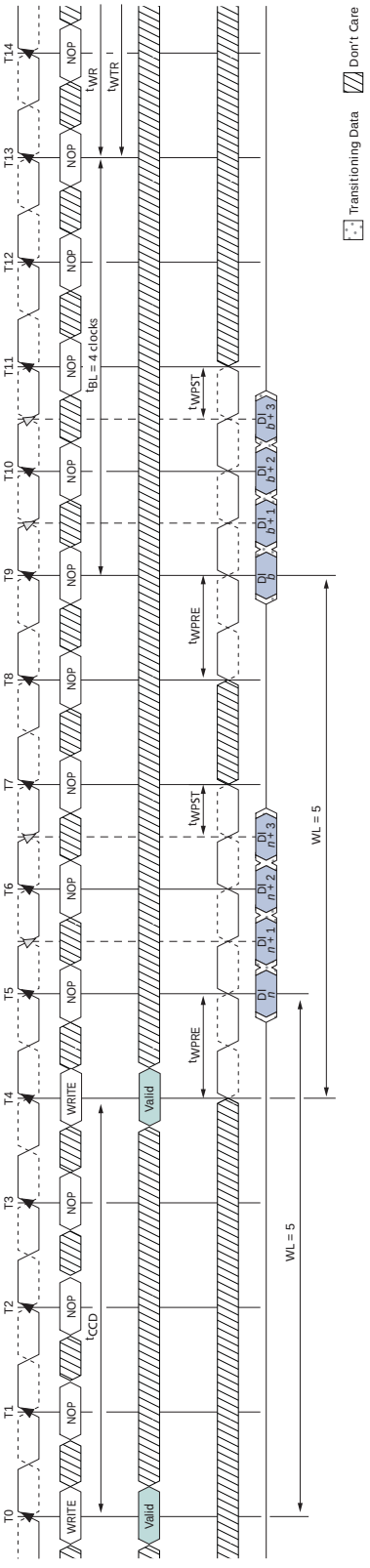
Figure 87: Consecutive WRITE (BL8) to WRITE (BL8)



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE commands at T0 and T4.
3. DI *n* (or *b*) = data-in for column *n* (or column *b*).
4. BL8, WL = 5 (AL = 0, CWL = 5).

Figure 88: Consecutive WRITE (BC4) to WRITE (BC4) via MRS or OTF



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BC4, WL = 5 (AL = 0, CWL = 5).
3. DI *n* (or *b*) = data-in for column *n* (or column *b*).
4. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and T4.

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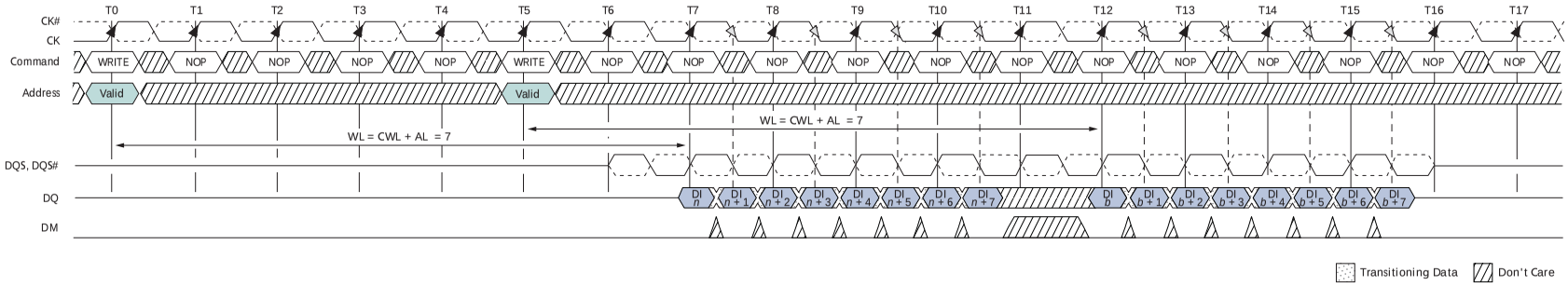
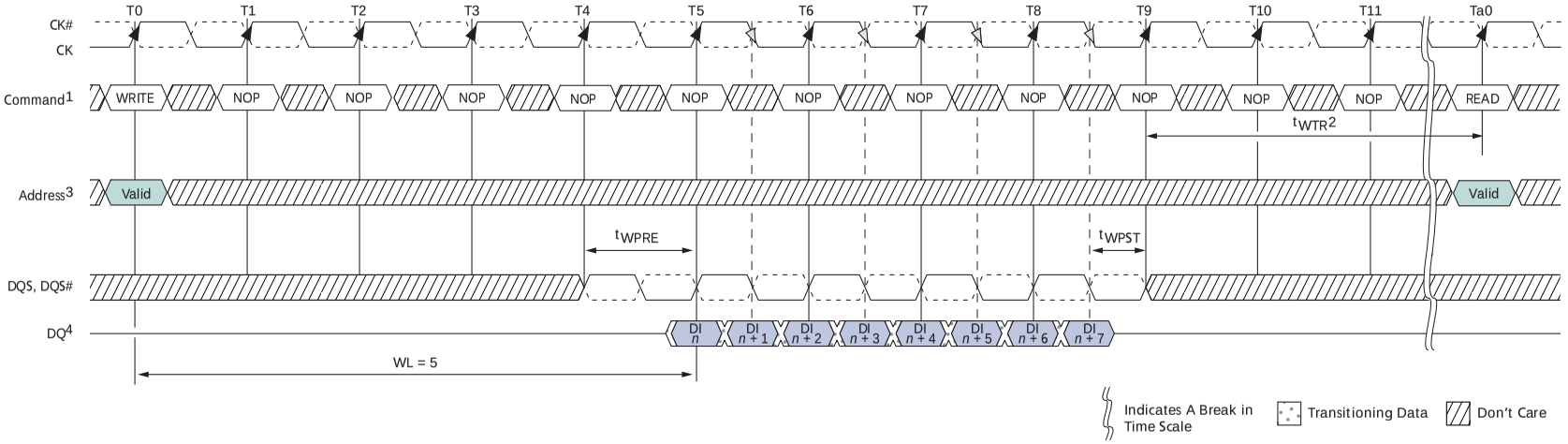
Figure 89: Nonconsecutive WRITE to WRITE



Notes:
1. DI *n* (or *b*) = data-in for column *n* (or column *b*).
2. Seven subsequent elements of data-in are applied in the programmed order following DO *n*.
3. Each WRITE command may be to any bank.
4. Shown for WL = 7 (CWL = 7, AL = 0).

Figure 90: WRITE (BL8) to READ (BL8)



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. ^{t}WTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T9.
3. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and MR0[12] = 1 during the WRITE command at T0. The READ command at Ta0 can be either BC4 or BL8, depending on MR0[1:0] and the A12 status at Ta0.
4. DI *n* = data-in for column *n*.
5. RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

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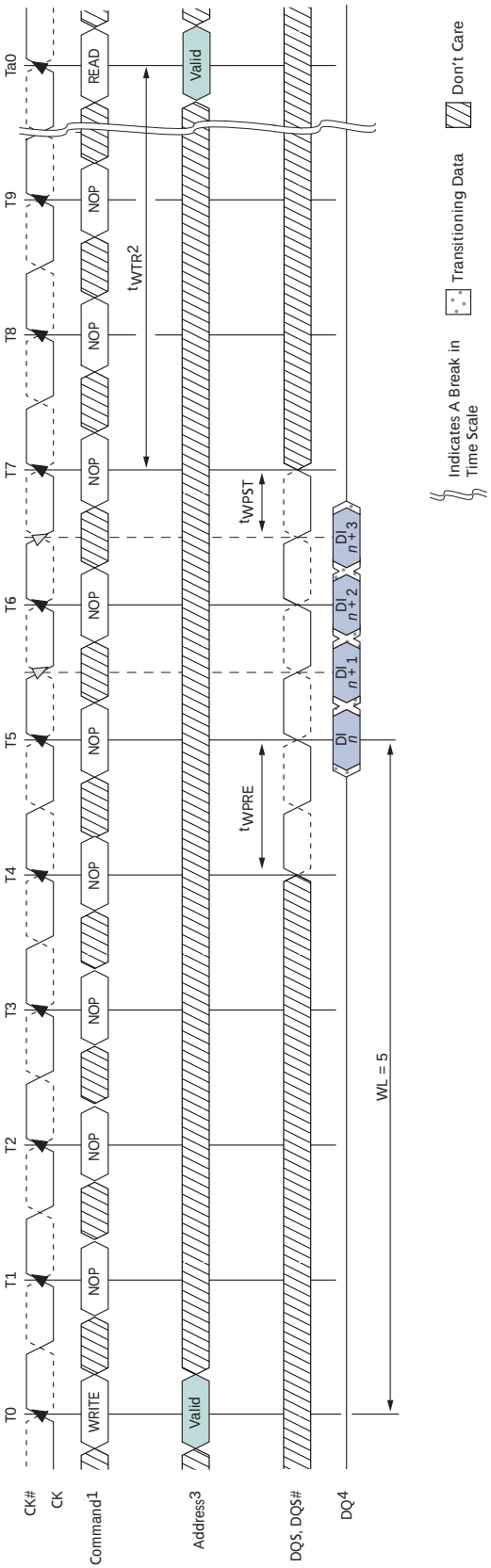
Figure 91: WRITE to READ (BC4 Mode Register Setting)



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. ^{t}WTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T7.
3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0 and the READ command at Ta0.
4. DI *n* = data-in for column *n*.
5. BC4 (fixed), WL = 5 (AL = 0, CWL = 5), RL = 5 (AL = 0, CL = 5).

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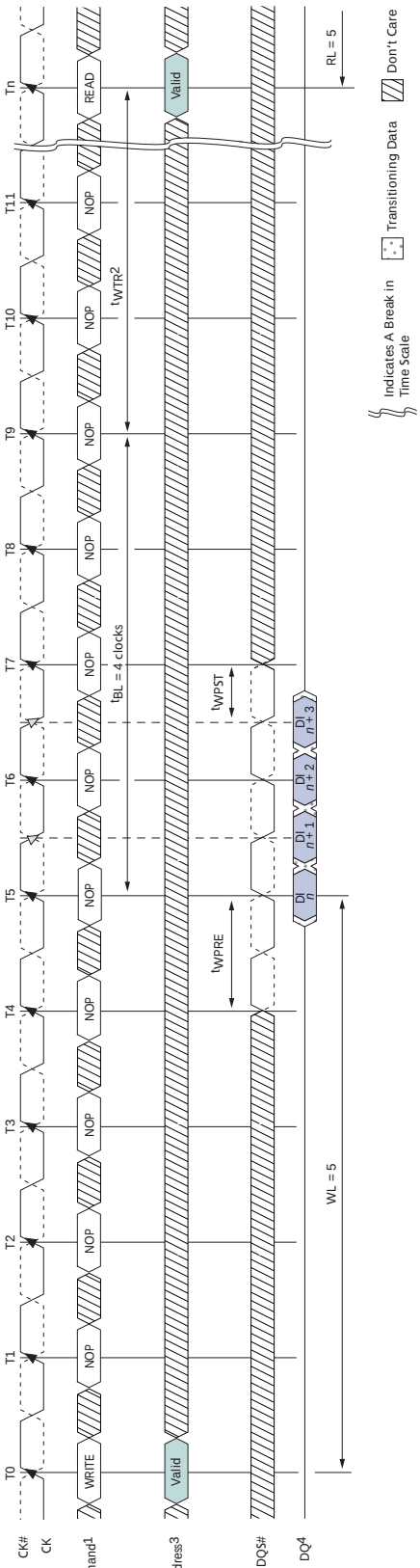
Figure 92: WRITE (BC4 OTF) to READ (BC4 OTF)



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. ^{t}WTR controls the WRITE-to-READ delay to the same device and starts after ^{t}BL.
3. The BC4 OTF setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and the READ command at T*n*.
4. DI *n* = data-in for column *n*.
5. BC4, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

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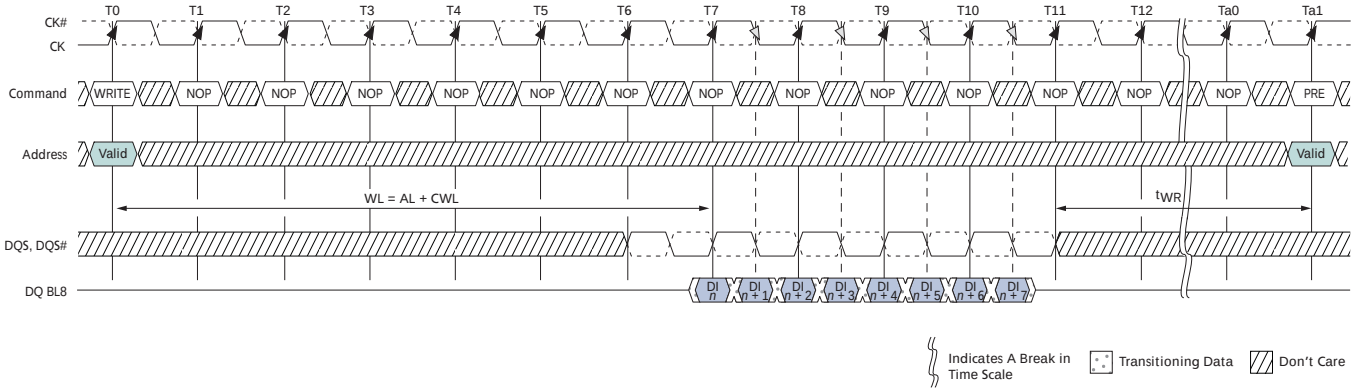
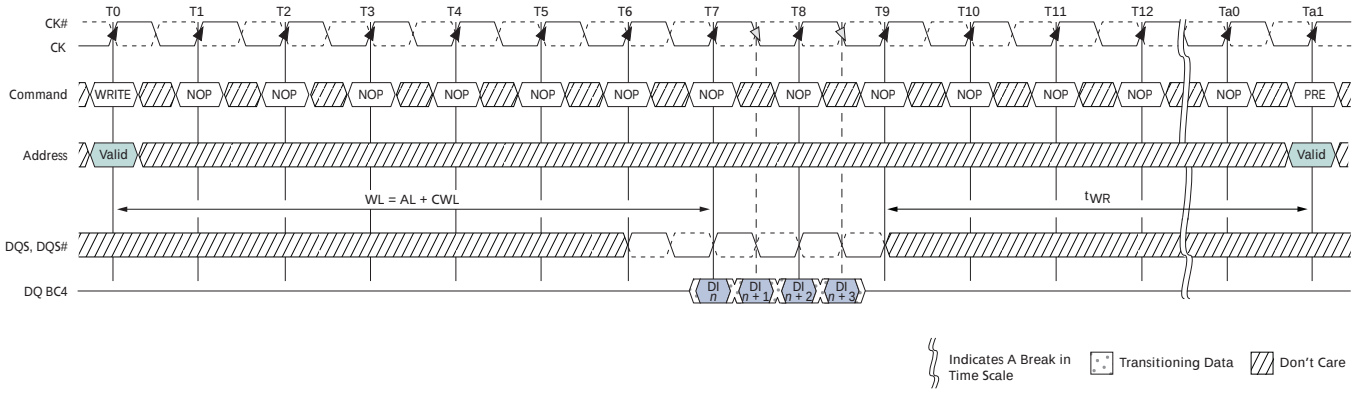
Figure 93: WRITE (BL8) to PRECHARGE



Notes:
1. DI *n* = data-in from column *n*.
2. Seven subsequent elements of data-in are applied in the programmed order following DO *n*.
3. Shown for WL = 7 (AL = 0, CWL = 7).

Figure 94: WRITE (BC4 Mode Register Setting) to PRECHARGE



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The write recovery time (^{t}WR) is referenced from the first rising clock edge after the last write data is shown at T7. ^{t}WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0.
4. DI *n* = data-in for column *n*.
5. BC4 (fixed), WL = 5, RL = 5.

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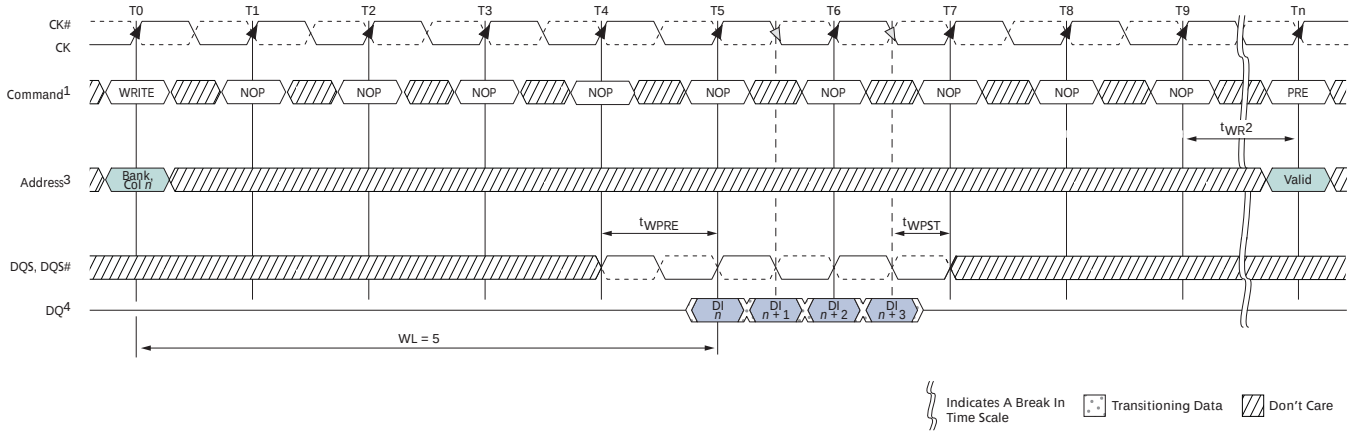
Figure 95: WRITE (BC4 OTF) to PRECHARGE



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The write recovery time (^{t}WR) is referenced from the rising clock edge at T9. ^{t}WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0.
4. DI *n* = data-in for column *n*.
5. BC4 (OTF), WL = 5, RL = 5.

DQ Input Timing

Figure 86 on page 141 shows the strobe to clock timing during a WRITE. DQS, DQS# must transition within 0.25^{t}CK of the clock transitions as limited by ^{t}DQSS. All data and data mask setup and hold timings are measured relative to the DQS, DQS# crossing, not the clock crossing.

The WRITE preamble and postamble are also shown. One clock prior to data input to the DRAM, DQS must be HIGH and DQS# must be LOW. Then for a half clock, DQS is driven LOW (DQS# is driven HIGH) during the WRITE preamble, ^{t}WPRE. Likewise, DQS must be kept LOW by the controller after the last data is written to the DRAM during the WRITE postamble, ^{t}WPST.

Data setup and hold times are shown in Figure 96 on page 148. All setup and hold times are measured from the crossing points of DQS and DQS#. These setup and hold values pertain to data input and data mask input.

Additionally, the half period of the data input strobe is specified by ^{t}DQSH and ^{t}DQSL.

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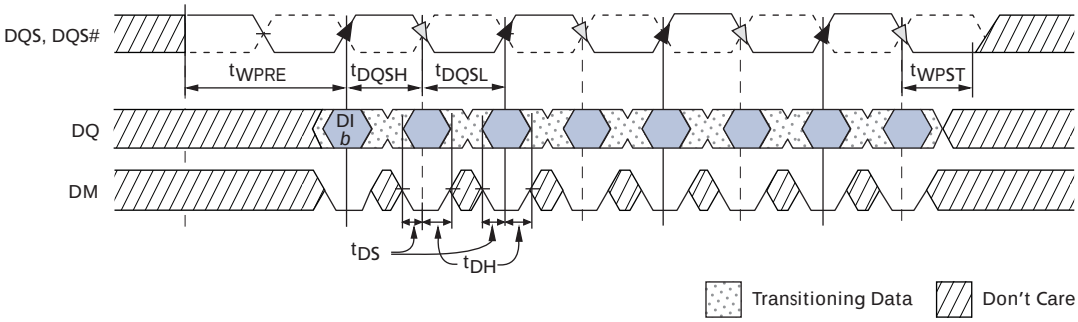
Figure 96: Data Input Timing



PRECHARGE

Input A10 determines whether one bank or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA[2:0] select the bank.

When all banks are to be precharged, inputs BA[2:0] are treated as "Don't Care." After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued.

SELF REFRESH

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH.

The DRAM must be idle with all banks in the precharge state (^{t}RP is satisfied and no bursts are in progress) before a self refresh entry command can be issued. ODT must also be turned off before self refresh entry by registering the ODT ball LOW prior to the self refresh entry command (see "On-Die Termination (ODT)" on page 160 for timing requirements). If RTT_NOM and RTT_WR are disabled in the mode registers, ODT can be a "Don't Care." After the self refresh entry command is registered, CKE must be held LOW to keep the DRAM in self refresh mode.

After the DRAM has entered self refresh mode, all external control signals, except CKE and RESET#, become "Don't Care." The DRAM initiates a minimum of one REFRESH command internally within the ^{t}CKE period when it enters self refresh mode.

The requirements for entering and exiting self refresh mode depend on the state of the clock during self refresh mode. First and foremost, the clock must be stable (meeting ^{t}CK specifications) when self refresh mode is entered. If the clock remains stable and the frequency is not altered while in self refresh mode, then the DRAM is allowed to exit self refresh mode after ^{t}CKESR is satisfied (CKE is allowed to transition HIGH ^{t}CKESR later than when CKE was registered LOW). Since the clock remains stable in self refresh mode (no frequency change), ^{t}CKSRE and ^{t}CKSRX are not required. However, if the clock is altered during self refresh mode (turned-off or frequency change), then ^{t}CKSRE and ^{t}CKSRX must be satisfied. When entering self refresh mode, ^{t}CKSRE must be satisfied prior to altering the clock's frequency. Prior to exiting self refresh mode, ^{t}CKSRX must be satisfied prior to registering CKE HIGH.

When CKE is HIGH during self refresh exit, NOP or DES must be issued for ^{t}XS time. ^{t}XS is required for the completion of any internal refresh that is already in progress and must be satisfied before a valid command not requiring a locked DLL can be issued to the device. ^{t}XS is also the earliest time self refresh reentry may occur (see Figure 97 on

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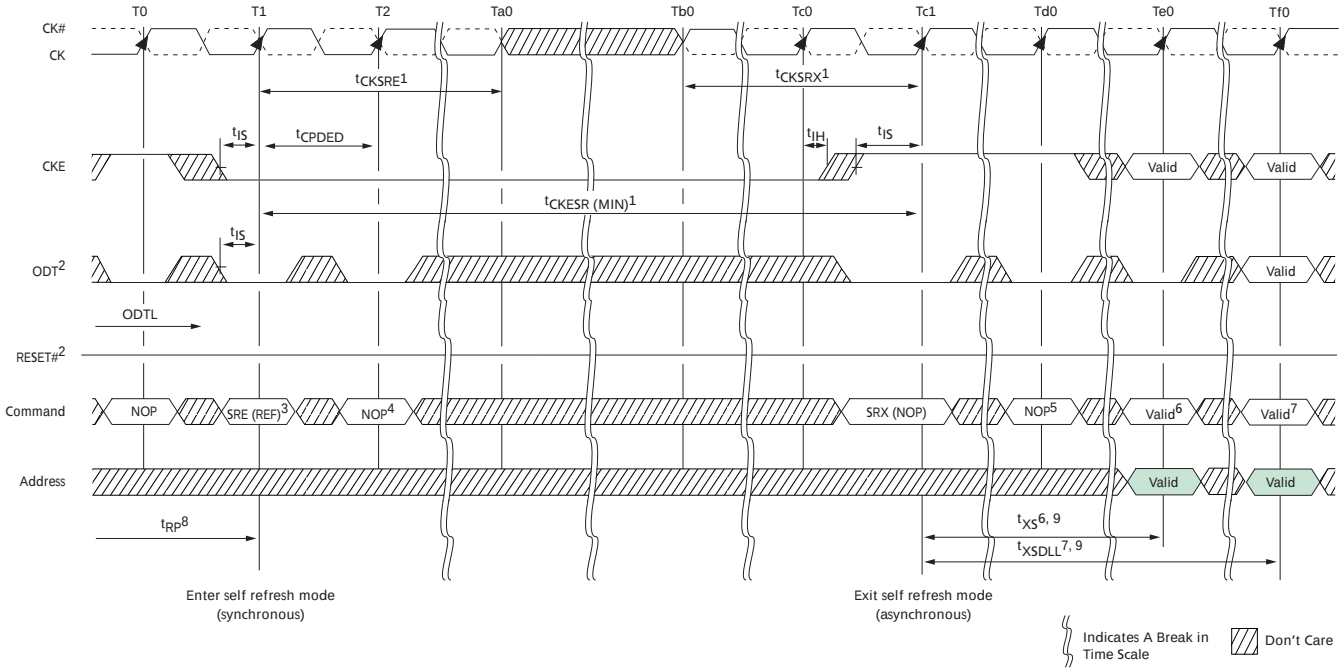
page 149). Before a command requiring a locked DLL can be applied, a ZQCL command must be issued, ^{t}ZQOPER timing must be met, and ^{t}XSDLL must be satisfied. ODT must be off during ^{t}XSDLL.

Figure 97: Self Refresh Entry/Exit Timing



Notes:

1. The clock must be valid and stable meeting ^{t}CK specifications at least ^{t}CKSRE after entering self refresh mode, and at least ^{t}CKSRX prior to exiting self refresh mode, if the clock is stopped or altered between states Ta0 and Tb0. If the clock remains valid and unchanged from entry and during self refresh mode, then ^{t}CKSRE and ^{t}CKSRX do not apply; however, ^{t}CKESR must be satisfied prior to exiting at SRX.
2. ODT must be disabled and RTT off prior to entering self refresh at state T1. If both RTT_NOM and RTT_WR are disabled in the mode registers, ODT can be a "Don't Care."
3. Self refresh entry (SRE) is synchronous via a REFRESH command with CKE LOW.
4. A NOP or DES command is required at T2 after the SRE command is issued prior to the inputs becoming "Don't Care."
5. NOP or DES commands are required prior to exiting self refresh mode until state Te0.
6. ^{t}XS is required before any commands not requiring a locked DLL.
7. ^{t}XSDLL is required before any commands requiring a locked DLL.
8. The device must be in the all banks idle state prior to entering self refresh mode. For example, all banks must be precharged, ^{t}RP must be met, and no data bursts can be in progress.
9. Self refresh exit is asynchronous; however, ^{t}XS and ^{t}XSDLL timings start at the first rising clock edge where CKE HIGH satisfies ^{t}ISXR at Tc1. ^{t}CKSRX timing is also measured so that ^{t}ISXR is satisfied at Tc1.

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Extended Temperature Usage

Micron's DDR3 SDRAM support the optional extended temperature range of 0°C to 95°C, T_C. Thus, the SRT and ASR options must be used at a minimum.

The extended temperature range DRAM must be refreshed externally at 2X (double refresh) anytime the case temperature is above 85°C (and does not exceed 95°C). The external refreshing requirement is accomplished by reducing the refresh period from 64ms to 32ms. However, self refresh mode requires either ASR or SRT to support the extended temperature. Thus either ASR or SRT must be enabled when T_C is above 85°C or self refresh cannot be used until the case temperature is at or below 85°C. Table 71 summarizes the two extended temperature options and Table 72 summarizes how the two extended temperature options relate to one another.

Table 71: Self Refresh Temperature and Auto Self Refresh Description

Field	MR2 Bits	Description
Self Refresh Temperature (SRT)		
SRT	7	If ASR is disabled (MR2[6] = 0), SRT must be programmed to indicate T_{OPER} during self refresh: *MR2[7] = 0: Normal operating temperature range (0°C to 85°C) *MR2[7] = 1: Extended operating temperature range (0°C to 95°C) If ASR is enabled (MR2[7] = 1), SRT must be set to 0, even if the extended temperature range is supported *MR2[7] = 0: SRT is disabled
Auto Self Refresh (ASR)		
ASR	6	When ASR is enabled, the DRAM automatically provides SELF REFRESH power management functions, (refresh rate for all supported operating temperature values) * MR2[6] = 1: ASR is enabled (M7 must = 0) When ASR is not enabled, the SRT bit must be programmed to indicate T_{OPER} during SELF REFRESH operation * MR2[6] = 0: ASR is disabled, must use manual self refresh temperature (SRT)

Table 72: Self Refresh Mode Summary

MR2[6] (ASR)	MR2[7] (SRT)	SELF REFRESH Operation	Permitted Operating Temperature Range for Self Refresh Mode
0	0	Self refresh mode is supported in the normal temperature range	Normal (0°C to 85°C)
0	1	Self refresh mode is supported in normal and extended temperature ranges; When SRT is enabled, it increases self refresh power consumption	Normal and extended (0°C to 95°C)
1	0	Self refresh mode is supported in normal and extended temperature ranges; Self refresh power consumption may be temperature-dependent	Normal and extended (0°C to 95°C)
1	1	Illegal	

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Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while either an MRS, MPR, ZQCAL, READ, or WRITE operation is in progress. CKE is allowed to go LOW while any of the other legal operations (such as ROW ACTIVATION, PRECHARGE, auto precharge, or REFRESH) are in progress. However, the power-down IDD specifications are not applicable until such operations have been completed. Depending on the previous DRAM state and the command issued prior to CKE going LOW, certain timing constraints must be satisfied (as noted in Table 73). Timing diagrams detailing the different power-down mode entry and exits are shown in Figure 98 on page 152 through Figure 107 on page 157.

Table 73: Command to Power-Down Entry Parameters

DRAM Status	Last Command Prior to CKE LOW[1]	Parameter (Min)	Parameter Value	Figure
Idle or active	ACTIVATE	^{t}ACTPDEN	1^{t}CK	Figure 105 on page 156
Idle or active	PRECHARGE	^{t}PRPDEN	1^{t}CK	Figure 106 on page 156
Active	READ or READAP	^{t}RDPDEN	RL + 4^{t}CK + 1^{t}CK	Figure 101 on page 154
Active	WRITE: BL8OTF, BL8MRS, BC4OTF	^{t}WRPDEN	WL + 4^{t}CK + ^{t}WR/^{t}CK	Figure 102 on page 154
Active	WRITE: BC4MRS		WL + 2^{t}CK + ^{t}WR/^{t}CK	Figure 102 on page 154
Active	WRITEAP: BL8OTF, BL8MRS, BC4OTF	^{t}WRAPDEN	WL + 4^{t}CK + WR + 1^{t}CK	Figure 103 on page 155
Active	WRITEAP: BC4MRS		WL + 2^{t}CK + WR + 1^{t}CK	Figure 103 on page 155
Idle	REFRESH	^{t}REFPDEN	1^{t}CK	Figure 104 on page 155
Power-down	REFRESH	^{t}XPDLL	Greater of 10^{t}CK or 24ns	Figure 108 on page 157
Idle	MODE REGISTER SET	^{t}MRSPDEN	^{t}MOD	Figure 107 on page 157

Notes: 1. If slow-exit mode precharge power-down is enabled and entered, ODT becomes asynchronous ^{t}ANPD prior to CKE going LOW and remains asynchronous until ^{t}ANPD + ^{t}XPDLL after CKE goes HIGH.

Entering power-down disables the input and output buffers, excluding CK, CK#, ODT, CKE, and RESET#. NOP or DES commands are required until ^{t}CPDED has been satisfied, at which time all specified input/output buffers will be disabled. The DLL should be in a locked state when power-down is entered for the fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation as well as synchronous ODT operation.

During power-down entry, if any bank remains open after all in-progress commands are complete, the DRAM will be in active power-down mode. If all banks are closed after all in-progress commands are complete, the DRAM will be in precharge power-down mode. Precharge power-down mode must be programmed to exit with either a slow exit mode or a fast exit mode. When entering precharge power-down mode, the DLL is turned off in slow exit mode or kept on in fast exit mode.

The DLL remains on when entering active power-down as well. ODT has special timing constraints when slow exit mode precharge power-down is enabled and entered. Refer to "Asynchronous ODT Mode" on page 172 for detailed ODT usage requirements in slow exit mode precharge power-down. A summary of the two power-down modes is listed in Table 74 on page 152.

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While in either power-down state, CKE is held LOW, RESET# is held HIGH, and a stable clock signal must be maintained. ODT must be in a valid state but all other input signals are a "Don't Care." If RESET# goes LOW during power-down, the DRAM will switch out of power-down mode and go into the reset state. After CKE is registered LOW, CKE must remain LOW until ^{t}PD (MIN) has been satisfied. The maximum time allowed for power-down duration is ^{t}PD (MAX) (9 × ^{t}REFI).

The power-down states are synchronously exited when CKE is registered HIGH (with a required NOP or DES command). CKE must be maintained HIGH until ^{t}CKE has been satisfied. A valid, executable command may be applied after power-down exit latency, ^{t}XP ^{t}XPDLL have been satisfied. A summary of the power-down modes is listed in Table 74.

For certain CKE-intensive operations, for example, repeating a power-down exit to refresh to power-down entry sequence, the number of clock cycles between power-down exit and power-down entry may not be sufficient enough to keep the DLL properly updated. In addition to meeting ^{t}PD when the REFRESH command is used in between power-down exit and power-down entry, two other conditions must be met. First, ^{t}XP must be satisfied before issuing the REFRESH command. Second, ^{t}XPDLL must be satisfied before the next power-down may be entered. An example is shown in Figure 108 on page 157.

Table 74: Power-Down Modes

DRAM State	MR1[12]	DLL State	Power-Down Exit	Relevant Parameters
Active (any bank open)	"Don't Care"	On	Fast	^{t}XP to any other valid command
Precharged (all banks precharged)	1	On	Fast	^{t}XP to any other valid command
	0	Off	Slow	^{t}XPDLL to commands that require the DLL to be locked (READ, RDAP, or ODT on) ^{t}XP to any other valid command

Figure 98: Active Power-Down Entry and Exit

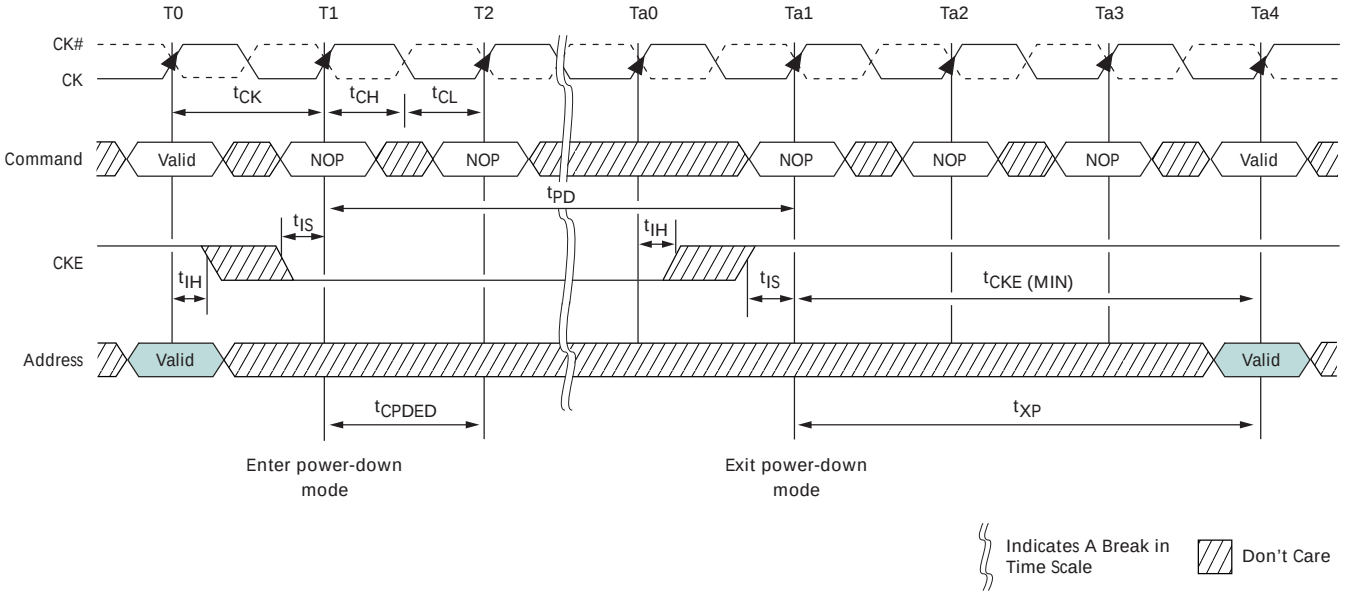

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Figure 99: Precharge Power-Down (Fast-Exit Mode) Entry and Exit

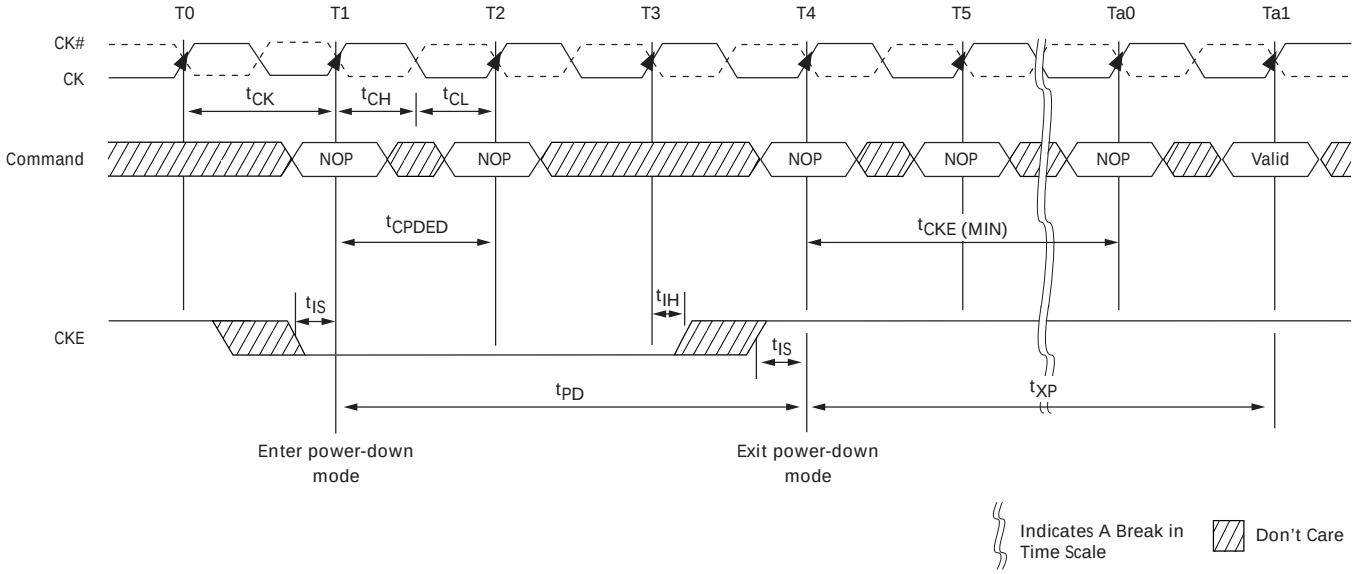
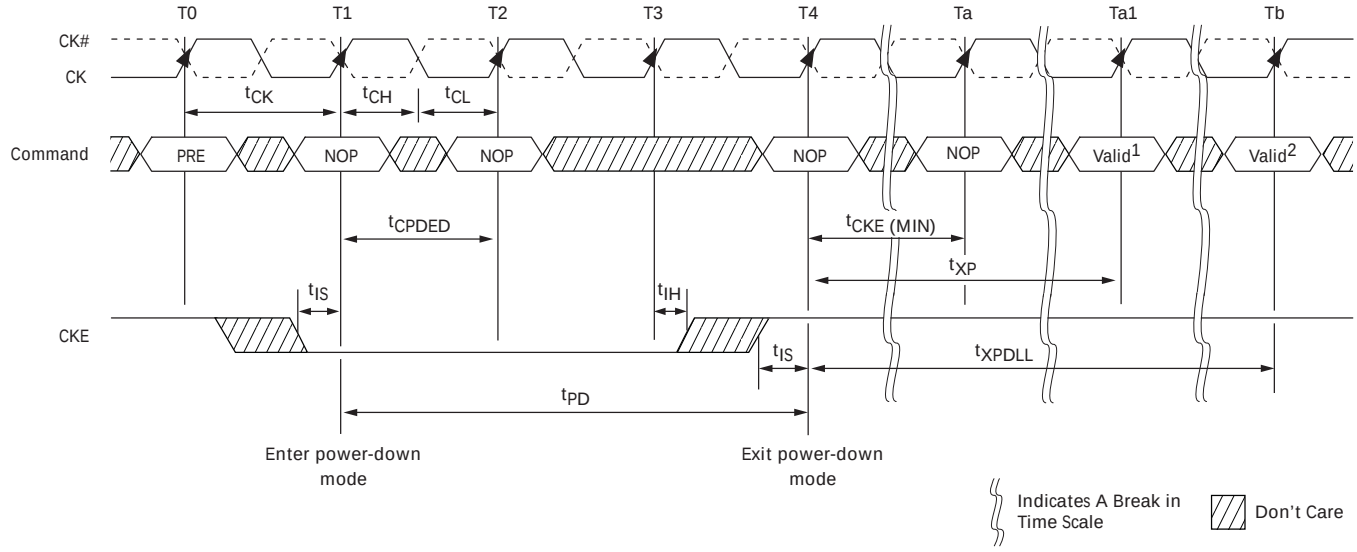


Figure 100: Precharge Power-Down (Slow-Exit Mode) Entry and Exit



Notes: 1. Any valid command not requiring a locked DLL.
2. Any valid command requiring a locked DLL.

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Figure 101: Power-Down Entry After READ or READ with Auto Precharge (RDAP)

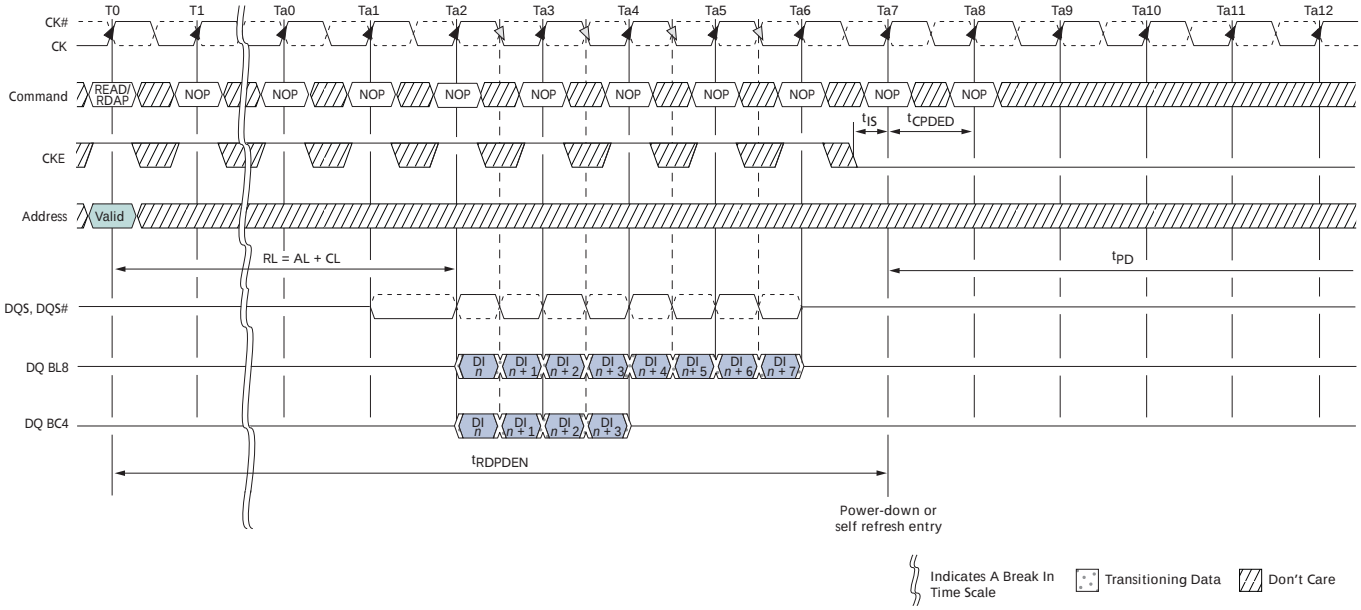
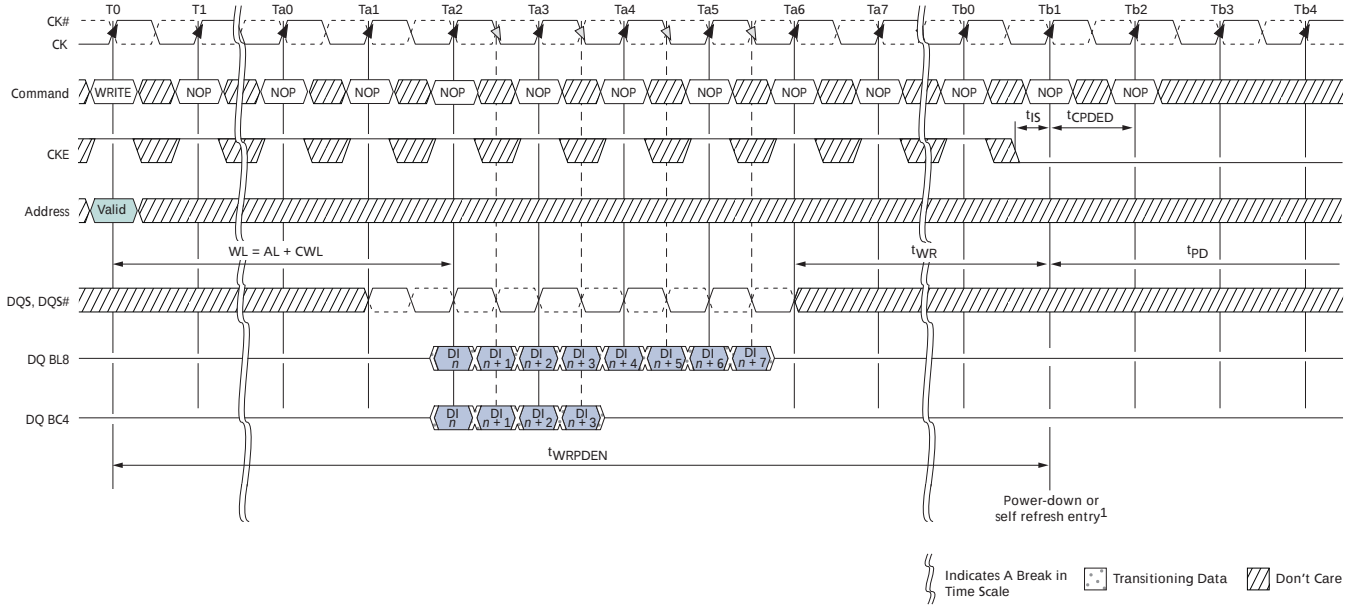


Figure 102: Power-Down Entry After WRITE



Notes: 1. CKE can go LOW 2tCK earlier if BC4MRS.

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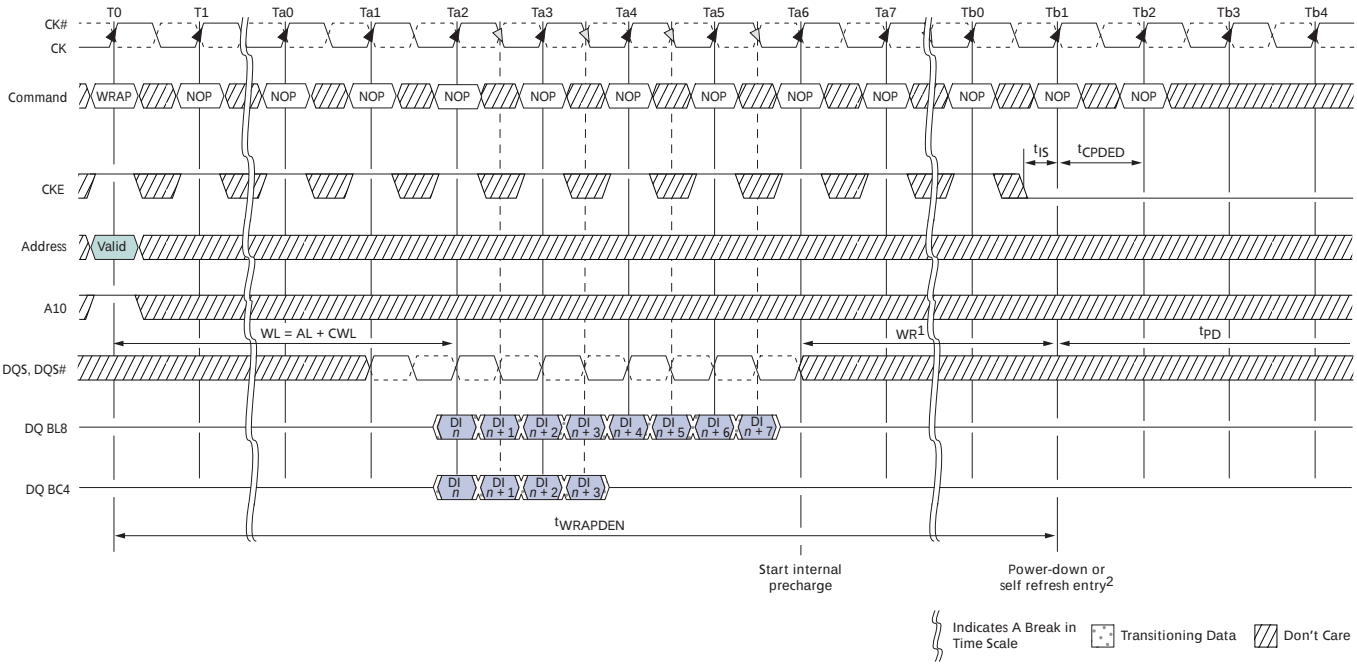
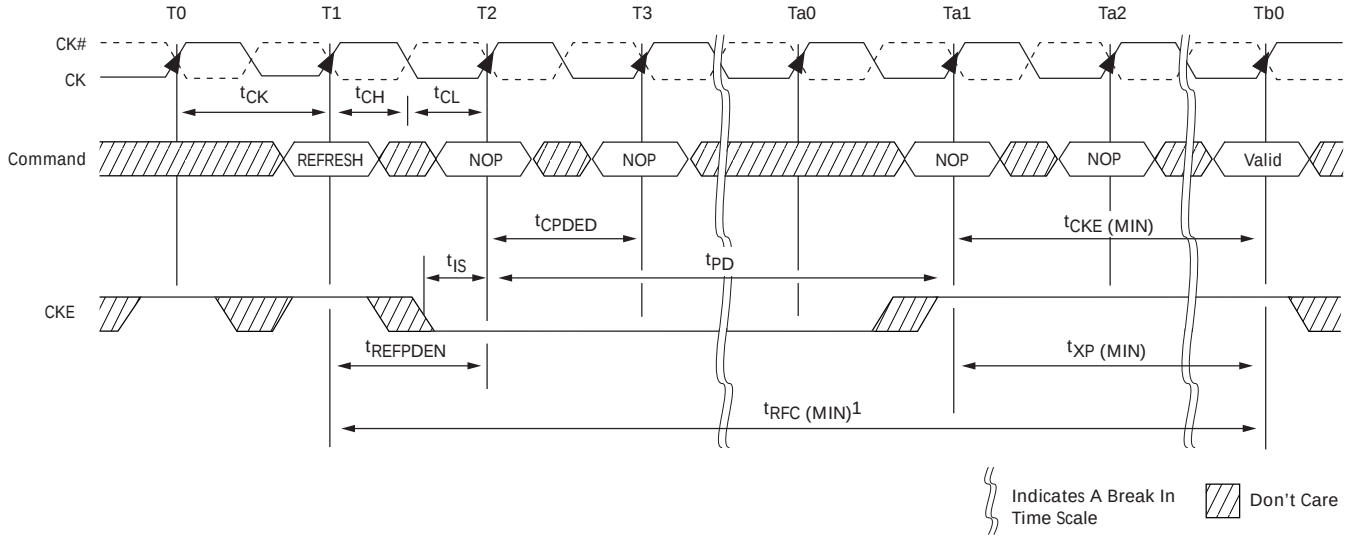
Figure 103: Power-Down Entry After WRITE with Auto Precharge (WRAP)



Notes: 1. ^{t}WR is programmed through MR0[11:9] and represents ^{t}WR (MIN)ns/^{t}CK rounded up to the next integer ^{t}CK.
2. CKE can go LOW 2^{t}CK earlier if BC4MRS.

Figure 104: REFRESH to Power-Down Entry



Notes: 1. After CKE goes HIGH during ^{t}RFC, CKE must remain HIGH until ^{t}RFC is satisfied.

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Figure 105: ACTIVATE to Power-Down Entry

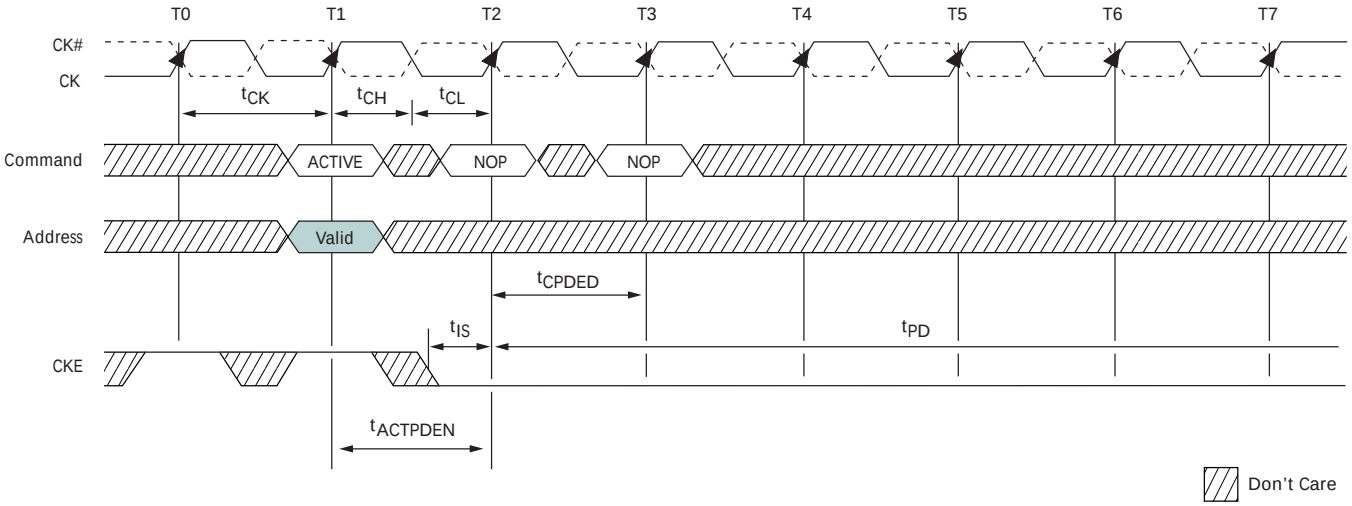

Figure 106: PRECHARGE to Power-Down Entry

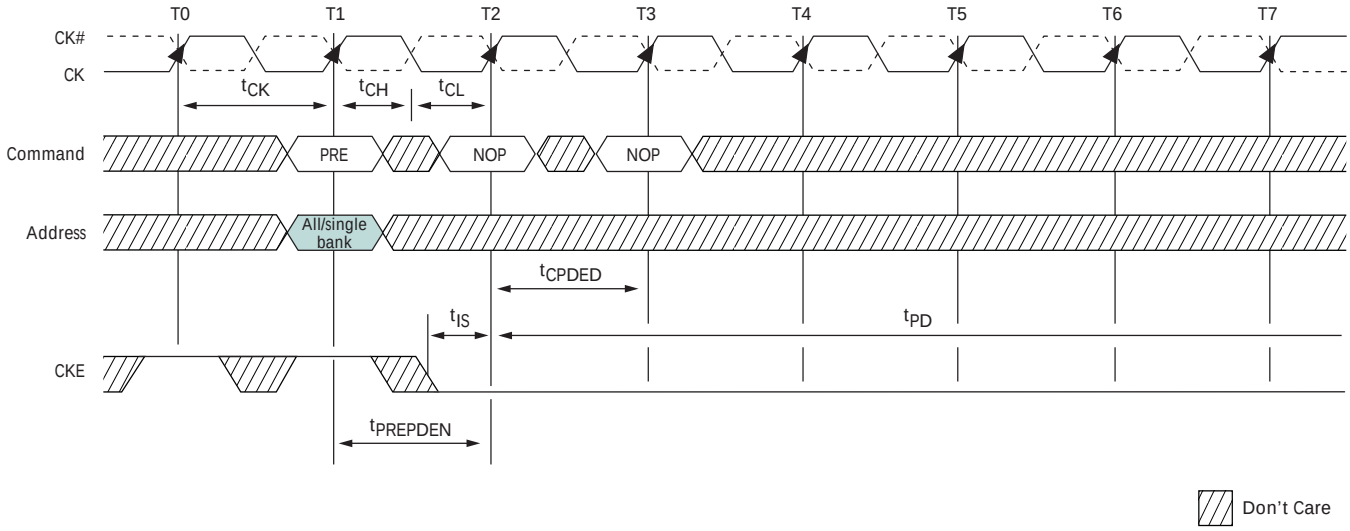

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Figure 107: MRS Command to Power-Down Entry

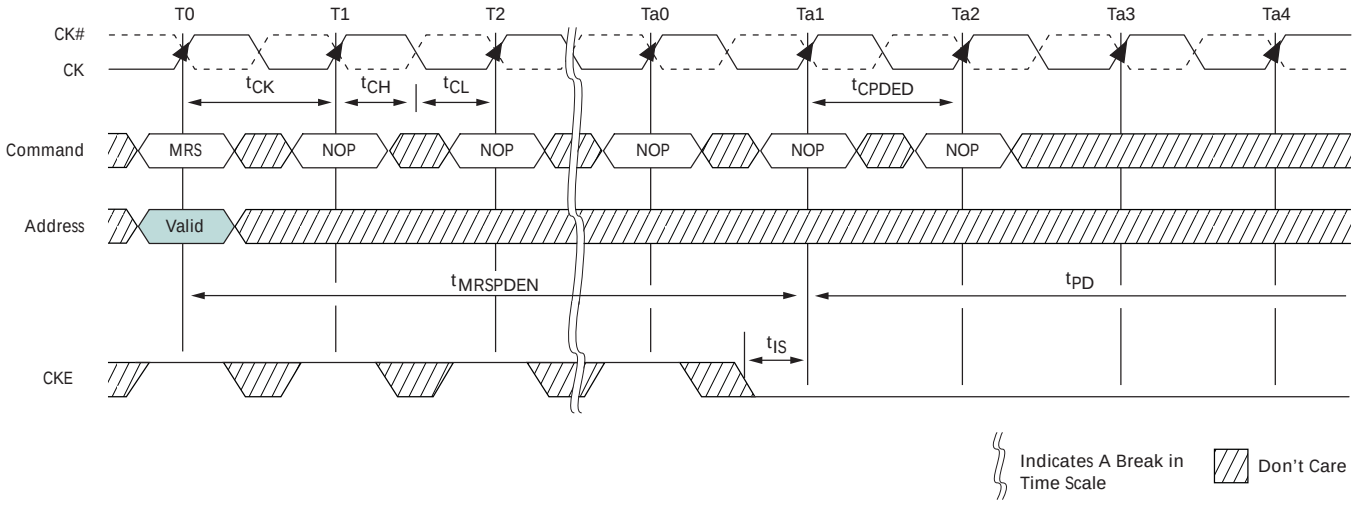
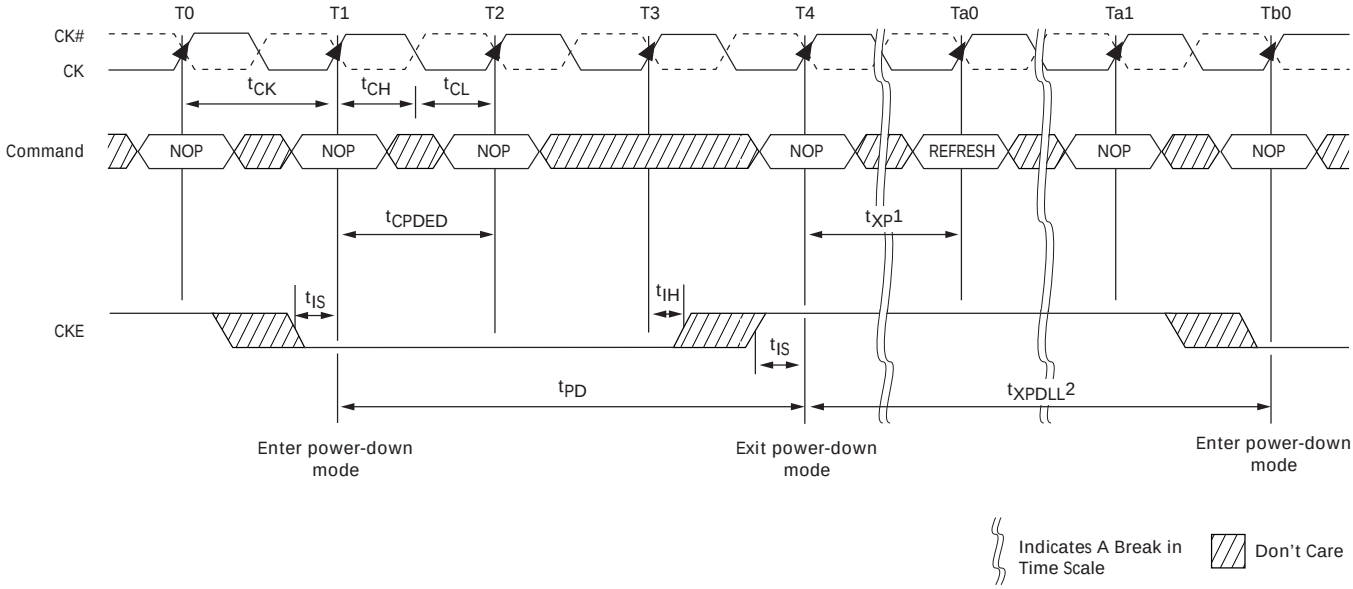


Figure 108: Power-Down Exit to Refresh to Power-Down Entry



Notes: 1. t_{XP} must be satisfied before issuing the command.
2. t_{XPDLL} must be satisfied (referenced to the registration of power-down exit) before the next power-down can be entered.

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RESET

The RESET signal (RESET#) is an asynchronous signal that triggers any time it drops LOW, and there are no restrictions about when it can go LOW. After RESET# goes LOW, it must remain LOW for 100ns. During this time, the outputs are disabled, ODT (R_{TT}) turns off (High-Z), and the DRAM resets itself. CKE should be brought LOW prior to RESET# being driven HIGH. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power up were executed (see Figure 109 on page 159). All refresh counters on the DRAM are reset, and data stored in the DRAM is assumed unknown after RESET# has gone LOW.

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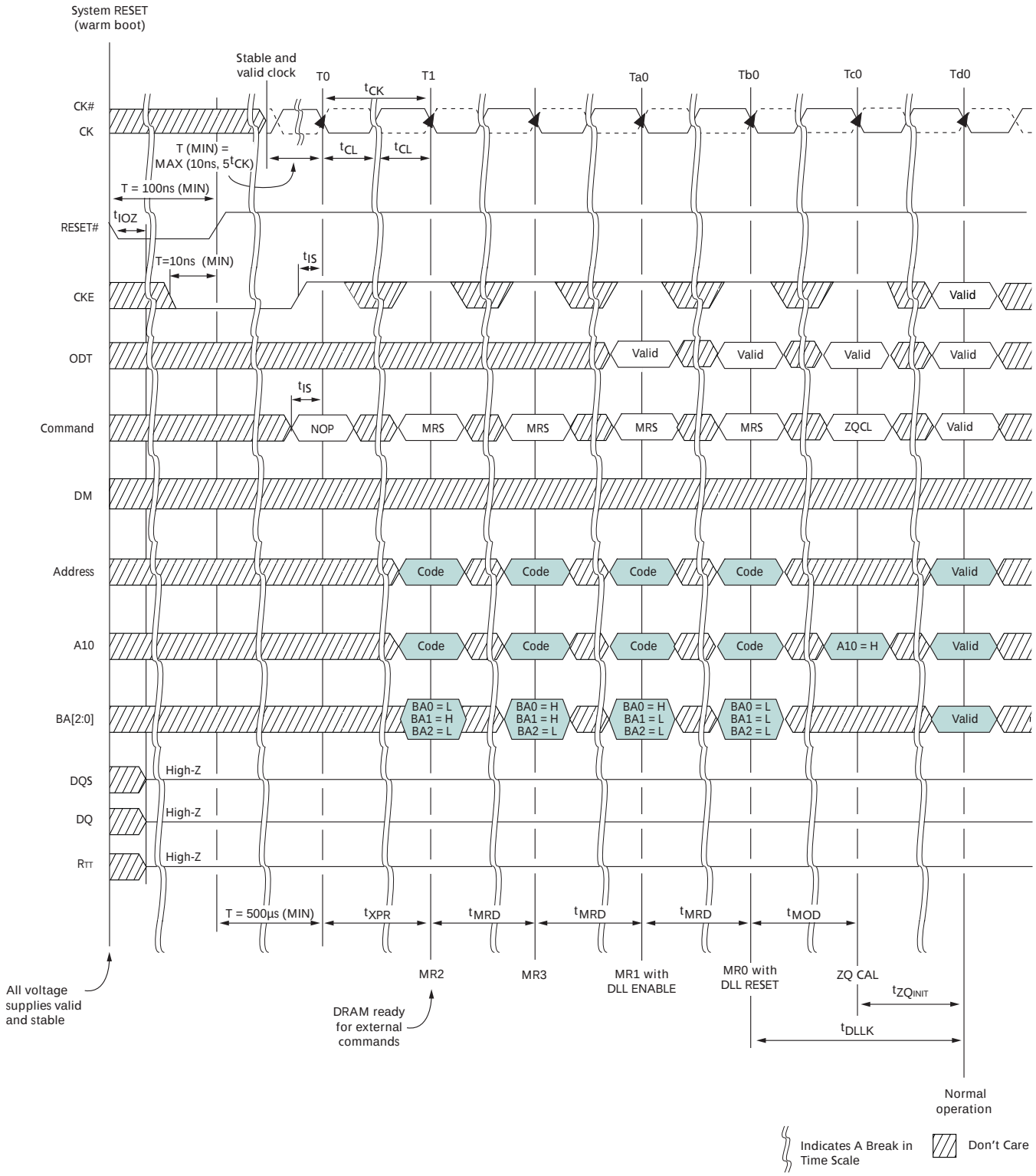
Figure 109: RESET Sequence



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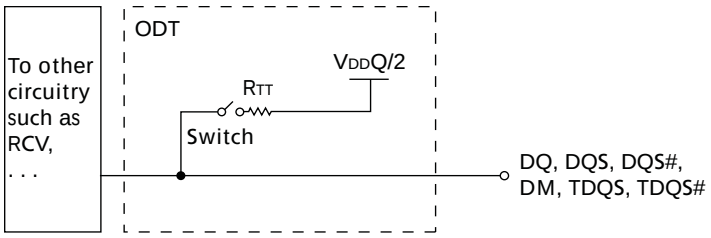
On-Die Termination (ODT)

ODT is a feature that enables the DRAM to enable/disable and turn on/off termination resistance for each DQ, DQS, DQS#, and DM for the x4 and x8 configurations (and TDQS, TDQS# for the x8 configuration, when enabled). ODT is applied to each DQ, UDQS, UDQS#, LDQS, LDQS#, UDM, and LDM signal for the x16 configuration.

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DRAM controller to independently turn on/off the DRAM's internal termination resistance for any grouping of DRAM devices. The ODT feature is not supported during DLL disable mode. A simple functional representation of the DRAM ODT feature is shown in Figure 110. The switch is enabled by the internal ODT control logic, which uses the external ODT ball and other control information.

Figure 110: On-Die Termination



Functional Representation of ODT

The value of R_{TT} (ODT termination value) is determined by the settings of several mode register bits (see Table 78 on page 163). The ODT ball is ignored while in self refresh mode (must be turned off prior to self refresh entry) or if mode registers MR1 and MR2 are programmed to disable ODT. ODT is comprised of nominal ODT and dynamic ODT modes and either of these can function in synchronous or asynchronous mode (when the DLL is off during precharge power-down or when the DLL is synchronizing). Nominal ODT is the base termination and is used in any allowable ODT state. Dynamic ODT is applied only during writes and provides OTF switching from no R_{TT} or R_{TT_NOM} to R_{TT_WR}.

The actual effective termination, R_{TT_EFF}, may be different from the R_{TT} targeted due to nonlinearity of the termination. For R_{TT_EFF} values and calculations, see "ODT Characteristics" on page 49.

Nominal ODT

ODT (NOM) is the base termination resistance for each applicable ball, it is enabled or disabled via MR1[9, 6, 2] (see Figure 47 on page 61), and it is turned on or off via the ODT ball (see Table 75 on page 161).

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Table 75: Truth Table – ODT (Nominal)
Note 1 applies to the entire table

MR1[9, 6, 2]	ODT Pin	DRAM Termination State	DRAM State	Notes
000	0	R_{TT_NOM} disabled, ODT off	Any valid	2
000	1	R_{TT_NOM} disabled, ODT on	Any valid except self refresh, read	3
000–101	0	R_{TT_NOM} enabled, ODT off	Any valid	2
000–101	1	R_{TT_NOM} enabled, ODT on	Any valid except self refresh, read	3
110 and 111	X	R_{TT_NOM} reserved, ODT on or off	Illegal	

Notes:
1. Assumes dynamic ODT is disabled (see "Dynamic ODT" on page 162 when enabled).
2. ODT is enabled and active during most writes for proper termination, but it is not illegal to have it off during writes.
3. ODT must be disabled during reads. The R_{TT_NOM} value is restricted during writes. Dynamic ODT is applicable if enabled.

Nominal ODT resistance R_{TT_NOM} is defined by MR1[9, 6, 2], as shown in Figure 47 on page 61. The R_{TT_NOM} termination value applies to the output pins previously mentioned. DDR3 SDRAM supports multiple R_{TT_NOM} values based on RZQ/*n* where *n* can be 2, 4, 6, 8, or 12 and RZQ is 240Ω. R_{TT_NOM} termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access or when it is not in self refresh mode.

Write accesses use R_{TT_NOM} if dynamic ODT (R_{TT_WR}) is disabled. If R_{TT_NOM} is used during writes, only RZQ/2, RZQ/4, and RZQ/6 are allowed (see Table 78 on page 163). ODT timings are summarized in Table 76, as well as listed in Table 53 on page 67.

Examples of nominal ODT timing are shown in conjunction with the synchronous mode of operation in "Synchronous ODT Mode" on page 167.

Table 76: ODT Parameter

Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Units
ODTL on	ODT synchronous turn on delay	ODT registered HIGH	R_{TT_ON} ±^{t}AON	CWL + AL - 2	^{t}CK
ODTL off	ODT synchronous turn off delay	ODT registered HIGH	R_{TT_OFF} ±^{t}AOF	CWL + AL - 2	^{t}CK
^{t}AONPD	ODT asynchronous turn on delay	ODT registered HIGH	R_{TT_ON}	1–9	ns
^{t}AOFPD	ODT asynchronous turn off delay	ODT registered HIGH	R_{TT_OFF}	1–9	ns
ODTH4	ODT minimum HIGH time after ODT assertion or write (BC4)	ODT registered HIGH or write registration with ODT HIGH	ODT registered LOW	4^{t}CK	^{t}CK
ODTH8	ODT minimum HIGH time after write (BL8)	Write registration with ODT HIGH	ODT registered LOW	6^{t}CK	^{t}CK
^{t}AON	ODT turn-on relative to ODTL on completion	Completion of ODTL on	R_{TT_ON}	See Table 53 on page 67	ps
^{t}AOF	ODT turn-off relative to ODTL off completion	Completion of ODTL off	R_{TT_OFF}	0.5^{t}CK ± 0.2^{t}CK	^{t}CK

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Dynamic ODT

In certain application cases, and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command, essentially changing the ODT termination on the fly. With dynamic ODT (R_{TT_WR}) enabled, the DRAM switches from nominal ODT (R_{TT_NOM}) to dynamic ODT (R_{TT_WR}) when beginning a WRITE burst and subsequently switches back to nominal ODT (R_{TT_NOM}) at the completion of the WRITE burst. This requirement is supported by the dynamic ODT feature, as described below:

Functional Description

The dynamic ODT mode is enabled if either MR2[9] or MR2[10] is set to "1." Dynamic ODT is not supported during DLL disable mode so R_{TT_WR} must be disabled. The dynamic ODT function is described, as follows:

- Two R_{TT} values are available—R_{TT_NOM} and R_{TT_WR}:
  - The value for R_{TT_NOM} is preselected via MR1[9, 6, 2]
  - The value for R_{TT_WR} is preselected via MR2[10, 9]
- During DRAM operation without READ or WRITE commands, the termination is controlled as follows:
  - Nominal termination strength R_{TT_NOM} is used
  - Termination on/off timing is controlled via the ODT ball and latencies ODTL on and ODTL off
- When a WRITE command (WR, WRAP, WRS4, WRS8, WRAPS4, WRAPS8) is registered, and if dynamic ODT is enabled, the ODT termination is controlled as follows:
  - A latency of $ODTL_{CNW}$ after the WRITE command: termination strength R_{TT_NOM} switches to R_{TT_WR}
  - A latency of $ODTL_{CWN8}$ (for BL8, fixed or OTF) or $ODTL_{CWN4}$ (for BC4, fixed or OTF) after the WRITE command: termination strength R_{TT_WR} switches back to R_{TT_NOM}
  - On/off termination timing is controlled via the ODT ball and determined by ODTL on, ODTL off, ODTH4, and ODTH8
  - During the ^{t}ADC transition window, the value of R_{TT} is undefined

ODT is constrained during writes and when dynamic ODT is enabled (see Table 77). ODT timings listed in Table 76 on page 161 also apply to dynamic ODT mode.

Table 77: Dynamic ODT Specific Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Units
$ODTL_{CNW}$	Change from R_{TT_NOM} to R_{TT_WR}	Write registration	R_{TT} switched from R_{TT_NOM} to R_{TT_WR}	WL - 2	^{t}CK
$ODTL_{CWN4}$	Change from R_{TT_WR} to R_{TT_NOM} (BC4)	Write registration	R_{TT} switched from R_{TT_WR} to R_{TT_NOM}	$4^{t}CK$ + ODTL off	^{t}CK
$ODTL_{CWN8}$	Change from R_{TT_WR} to R_{TT_NOM} (BL8)	Write registration	R_{TT} switched from R_{TT_WR} to R_{TT_NOM}	$6^{t}CK$ + ODTL off	^{t}CK
^{t}ADC	R_{TT} change skew	$ODTL_{CNW}$ completed	R_{TT} transition complete	$0.5^{t}CK \pm 0.2^{t}CK$	tCK

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Table 78: Mode Registers for RTT_NOM

MR1 (RTT_NOM)			RTT_NOM (RZQ)	RTT_NOM (Ohms)	RTT_NOM Mode Restriction
M9	M6	M2			
0	0	0	Off	Off	n/a
0	0	1	RZQ/4	60	Self refresh
0	1	0	RZQ/2	120	
0	1	1	RZQ/6	40	
1	0	0	RZQ/12	20	Self refresh, write
1	0	1	RZQ/8	30	
1	1	0	Reserved	Reserved	n/a
1	1	1	Reserved	Reserved	n/a

Notes: 1. RZQ = 240Ω. If RTT_NOM is used during WRITEs, only RZQ/2, RZQ/4, RZQ/6 are allowed.

Table 79: Mode Registers for RTT_WR

MR2 (RTT_WR)		RTT_WR (RZQ)	RTT_WR (Ohms)
M10	M9		
0	0	Dynamic ODT off: WRITE does not affect RTT_NOM	
0	1	RZQ/4	60
1	0	RZQ/2	120
1	1	Reserved	Reserved
n/a	n/a	n/a	n/a
n/a	n/a	n/a	n/a
n/a	n/a	n/a	n/a
n/a	n/a	n/a	n/a

Table 80: Timing Diagrams for Dynamic ODT

Figure and Page	Title
Figure 111 on page 164	Dynamic ODT: ODT Asserted Before and After the WRITE, BC4
Figure 112 on page 164	Dynamic ODT: Without WRITE Command
Figure 113 on page 165	Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8
Figure 114 on page 166	Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4
Figure 115 on page 166	Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4

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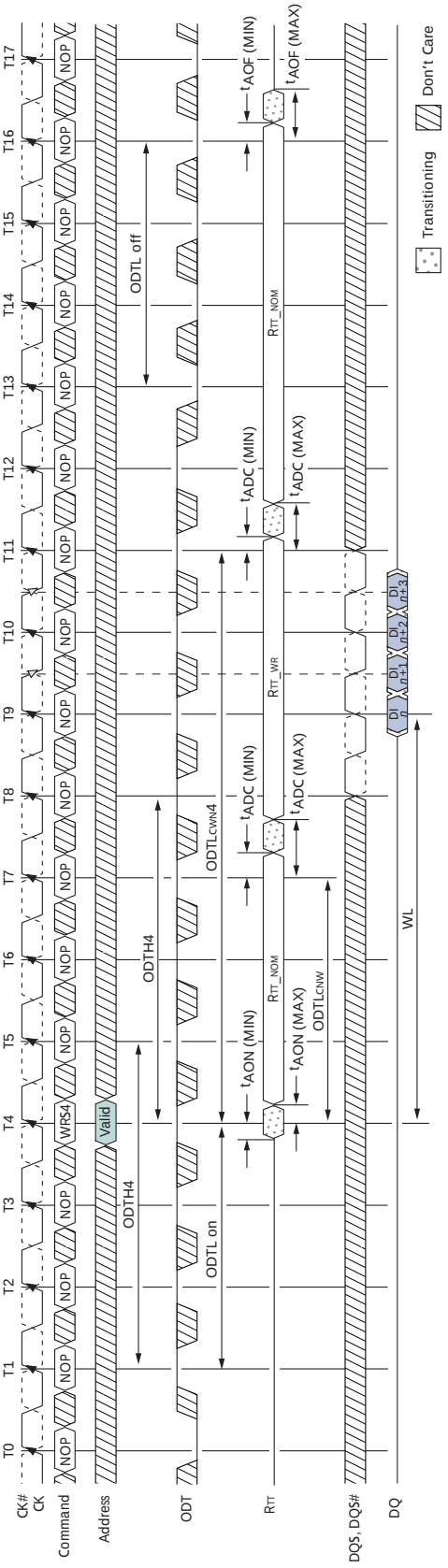
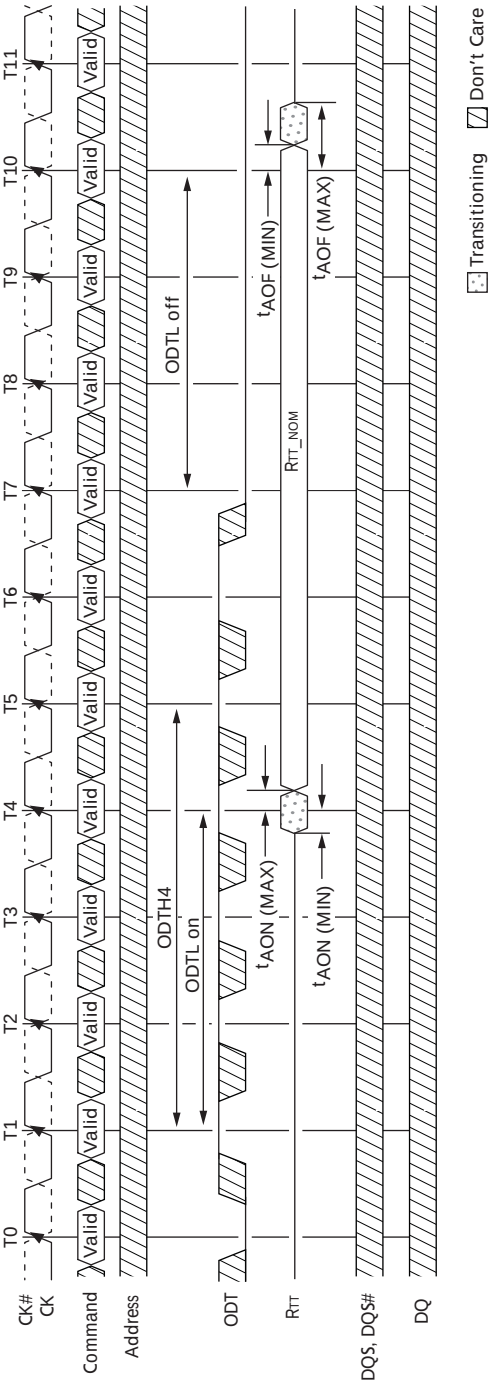
Figure 111: Dynamic ODT: ODT Asserted Before and After the WRITE, BC4



Notes:
1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM and RTT_WR are enabled.
2. ODTH4 applies to first registering ODT HIGH and then to the registration of the WRITE command. In this example, ODTH4 is satisfied if ODT goes LOW at T8 (four clocks after the WRITE command).

Figure 112: Dynamic ODT: Without WRITE Command



Notes:
1. AL = 0, CWL = 5. RTT_NOM is enabled and RTT_WR is either enabled or disabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW; in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

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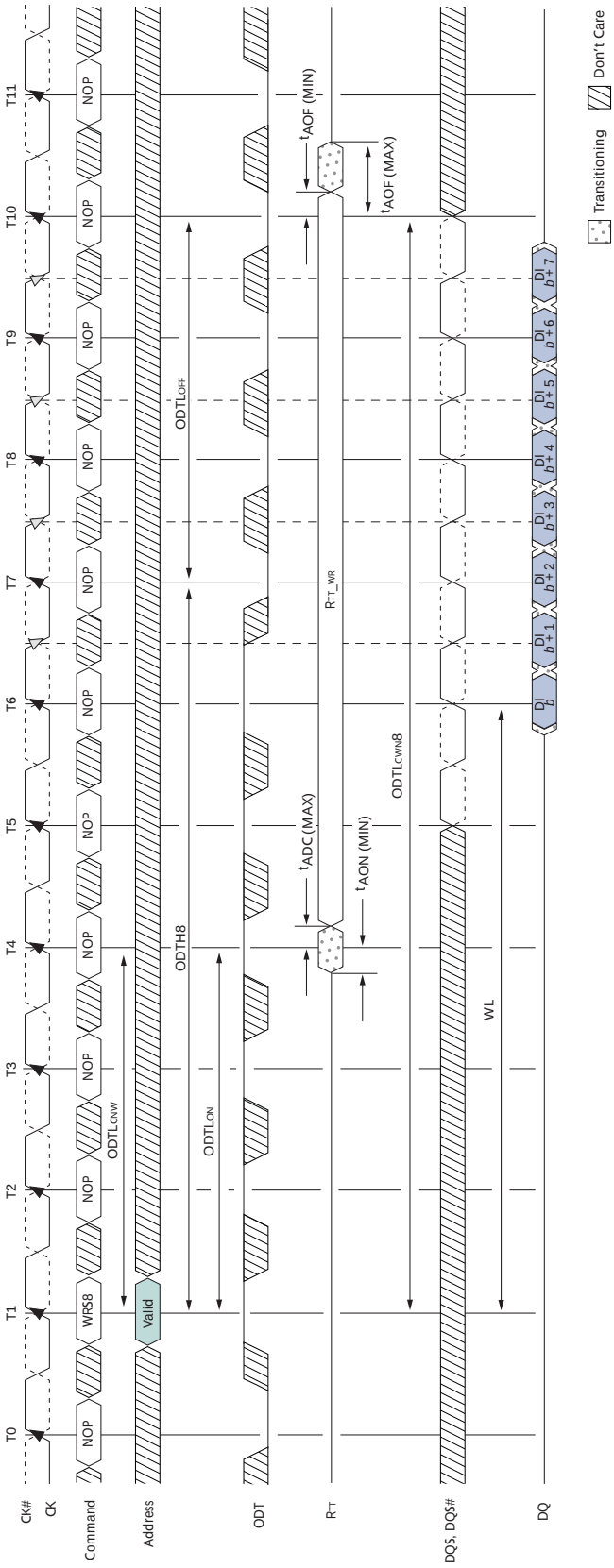
Figure 113: Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8



Notes:
1. Via MRS or OTF; AL = 0, CWL = 5. If RTT_NOM can be either enabled or disabled, ODT can be HIGH. RTT_WR is enabled.
2. In this example, ODTH8 = 6 is satisfied exactly.

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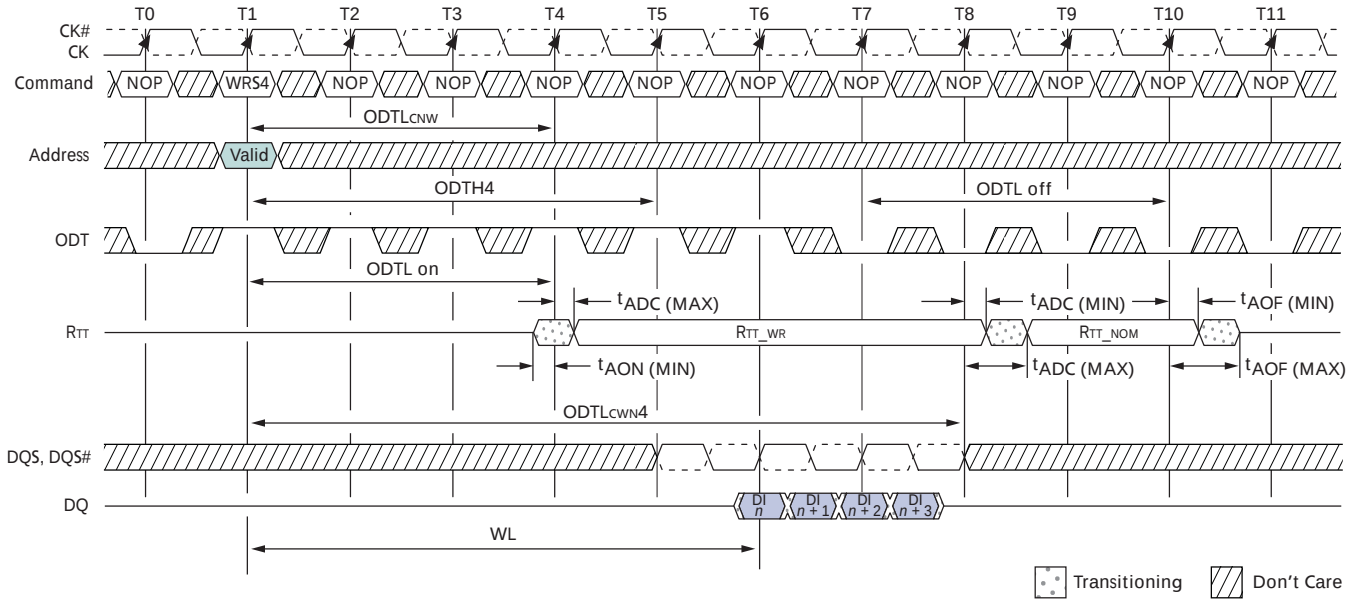
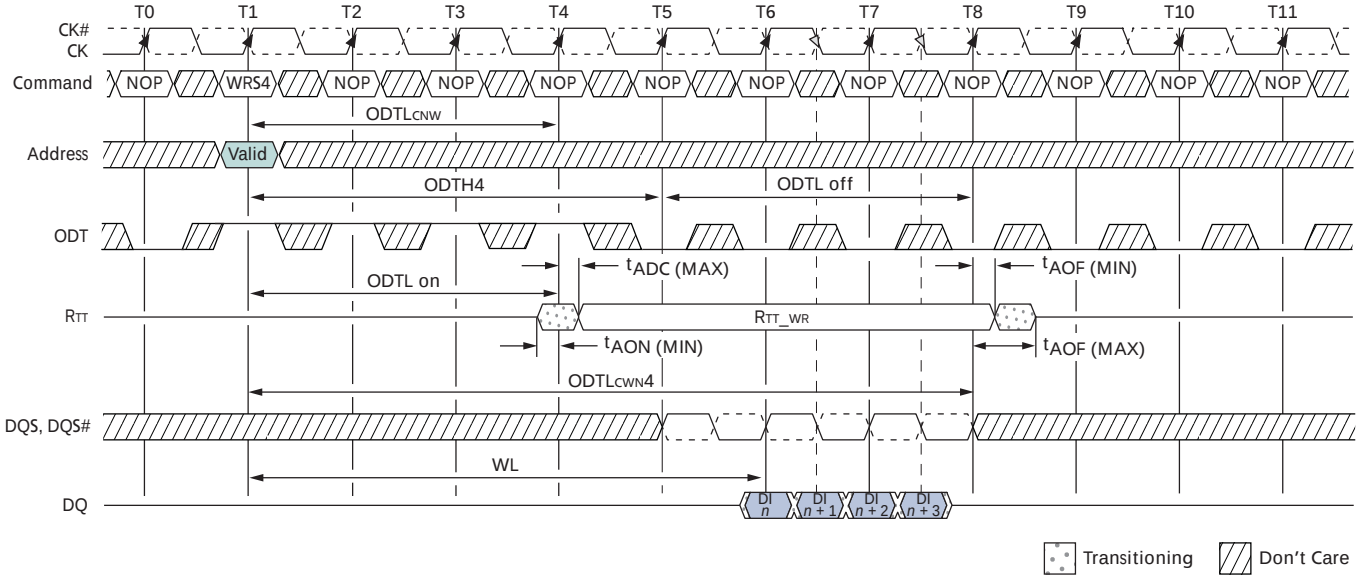
Figure 114: Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4



Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM and RTT_WR are enabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW, so in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

Figure 115: Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4



Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM can be either enabled or disabled. If disabled, ODT can remain HIGH. RTT_WR is enabled.
2. In this example ODTH4 = 4 is satisfied exactly.

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Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked and when either RTT_NOM or RTT_WR is enabled. Based on the power-down definition, these modes are:

- Any bank active with CKE HIGH
- Refresh mode with CKE HIGH
- Idle mode with CKE HIGH
- Active power-down mode (regardless of MR0[12])
- Precharge power-down mode if DLL is enabled during precharge power-down by MR0[12]

ODT Latency and Posted ODT

In synchronous ODT mode, RTT turns on ODTL on clock cycles after ODT is sampled HIGH by a rising clock edge and turns off ODTL off clock cycles after ODT is registered LOW by a rising clock edge. The actual on/off times varies by ^{t}AON and ^{t}AOF around each clock edge (see Table 81 on page 168). The ODT latency is tied to the WRITE latency (WL) by ODTL on = WL - 2 and ODTL off = WL - 2.

Since write latency is made up of CAS WRITE latency (CWL) and ADDITIVE latency (AL), the AL programmed into the mode register (MR1[4, 3]) also applies to the ODT signal. The DRAM's internal ODT signal is delayed a number of clock cycles defined by the AL relative to the external ODT signal. Thus ODTL on = CWL + AL - 2 and ODTL off = CWL + AL - 2.

Timing Parameters

Synchronous ODT mode uses the following timing parameters: ODTL on, ODTL off, ODTH4, ODTH8, ^{t}AON, and ^{t}AOF (see Table 81 and Figure 116 on page 168). The minimum RTT turn-on time (^{t}AON [MIN]) is the point at which the device leaves High-Z and ODT resistance begins to turn on. Maximum RTT turn-on time (^{t}AON [MAX]) is the point at which ODT resistance is fully on. Both are measured relative to ODTL on. The minimum RTT turn-off time (^{t}AOF [MIN]) is the point at which the device starts to turn off ODT resistance. Maximum RTT turn off time (^{t}AOF [MAX]) is the point at which ODT has reached High-Z. Both are measured from ODTL off.

When ODT is asserted, it must remain HIGH until ODTH4 is satisfied. If a WRITE command is registered by the DRAM with ODT HIGH, then ODT must remain HIGH until ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (see Figure 117 on page 169). ODTH4 and ODTH8 are measured from ODT registered HIGH to ODT registered LOW or from the registration of a WRITE command until ODT is registered LOW.

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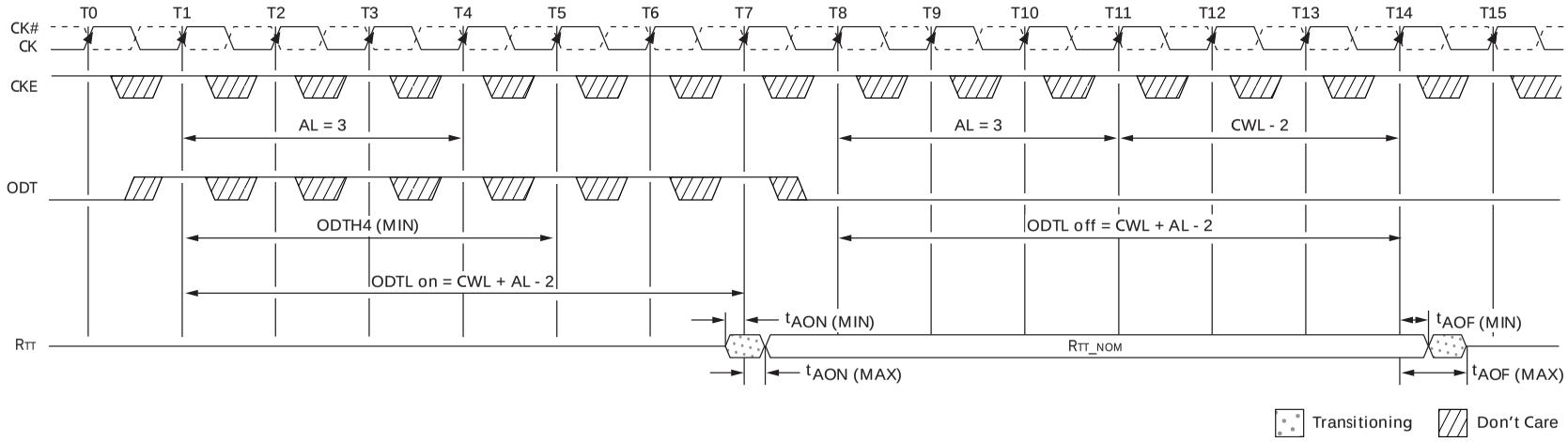
Table 81: Synchronous ODT Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Units
ODTL on	ODT synchronous turn-on delay	ODT registered HIGH	R_{TT_ON} ±^{t}AON	CWL + AL - 2	^{t}CK
ODTL off	ODT synchronous turn-off delay	ODT registered HIGH	R_{TT_OFF} ±^{t}AOF	CWL + AL - 2	^{t}CK
ODTH4	ODT minimum HIGH time after ODT assertion or WRITE (BC4)	ODT registered HIGH, or write registration with ODT HIGH	ODT registered LOW	4^{t}CK	^{t}CK
ODTH8	ODT minimum HIGH time after WRITE (BL8)	Write registration with ODT HIGH	ODT registered LOW	6^{t}CK	^{t}CK
^{t}AON	ODT turn-on relative to ODTL on completion	Completion of ODTL on	R_{TT_ON}	See Table 53 on page 67	ps
^{t}AOF	ODT turn-off relative to ODTL off completion	Completion of ODTL off	R_{TT_OFF}	0.5^{t}CK ± 0.2^{t}CK	tCK

Figure 116: Synchronous ODT



Notes: 1. AL = 3; CWL = 5; ODTL on = WL = 6.0; ODTL off = WL - 2 = 6. R_{TT_NOM} is enabled.

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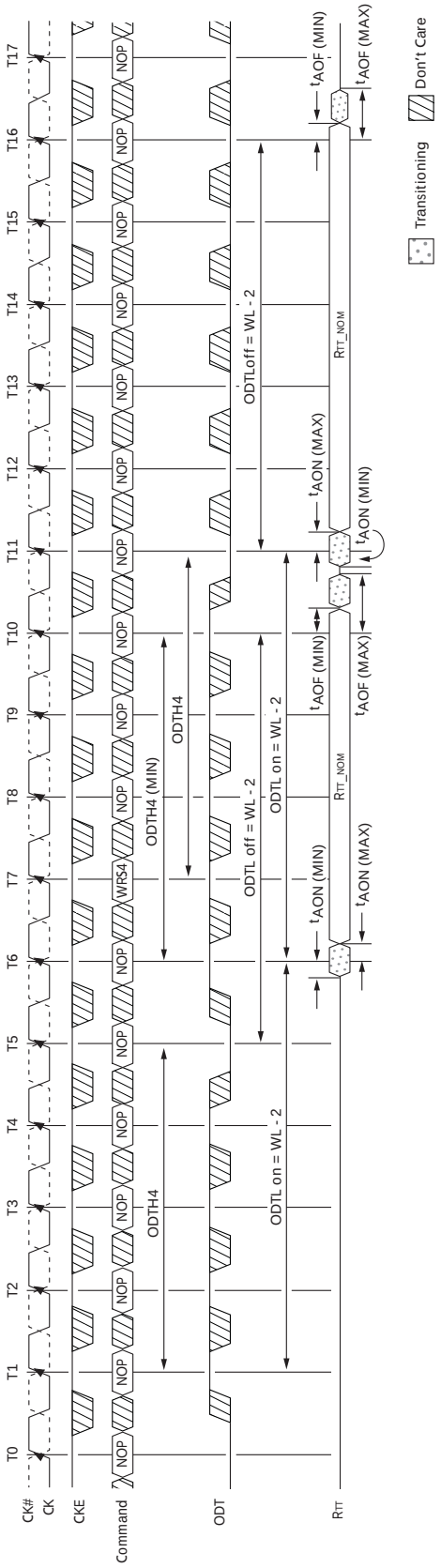
Figure 117: Synchronous ODT (BC4)



Notes:
1. WL = 7. RTT_NOM is enabled. RTT_WR is disabled.
2. ODT must be held HIGH for at least ODTH4 after assertion (T1).
3. ODT must be kept HIGH ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (T7).
4. ODTH is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of the WRITE command with ODT HIGH to ODT registered LOW.
5. Although ODTH4 is satisfied from ODT registered HIGH at T6, ODT must not go LOW before T11 as ODTH4 must also be satisfied from the registration of the WRITE command at T7.

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ODT Off During READs

As the DDR3 SDRAM cannot terminate and drive at the same time, R_{TT} must be disabled at least one-half clock cycle before the READ preamble by driving the ODT ball LOW (if either R_{TT_NOM} or R_{TT_WR} is enabled). R_{TT} may not be enabled until the end of the post-amble as shown in the example in Figure 118 on page 171.

Note: ODT may be disabled earlier and enabled later than shown in Figure 118 on page 171.

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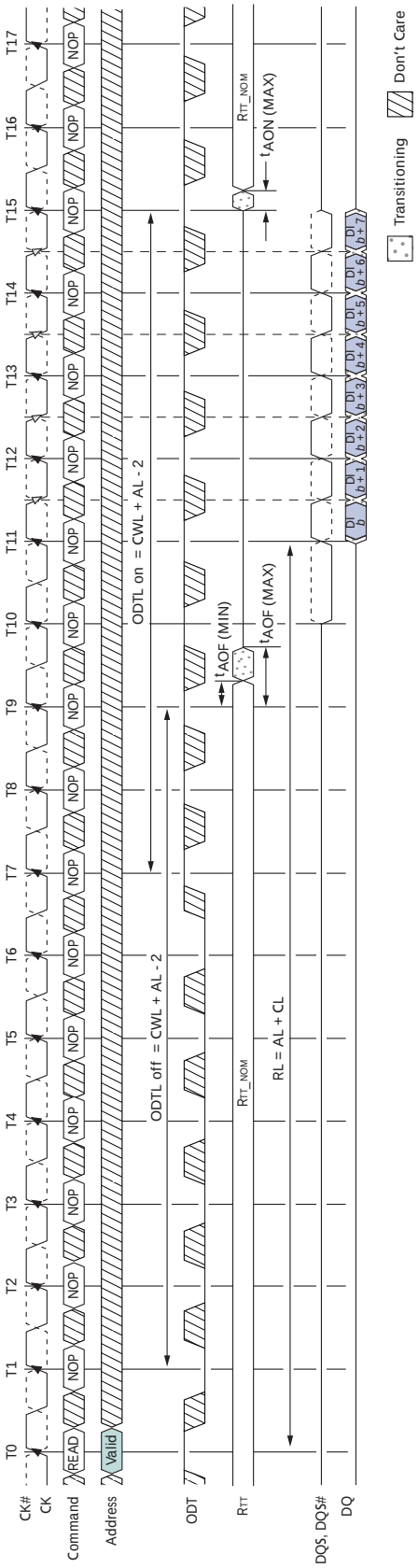
Figure 118: ODT During READs



Notes: 1. ODT must be disabled externally during READs by driving ODT LOW. For example, CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTL on = CWL + AL - 2 = 8; ODTL off = CWL + AL - 2 = 8. RTT_NOM is enabled. RTT_WR is a "Don't Care."

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Asynchronous ODT Mode

Asynchronous ODT mode is available when the DRAM runs in DLL on mode and when either R_{TT_NOM} or R_{TT_WR} is enabled; however, the DLL is temporarily turned off in precharged power-down standby (via MR0[12]). Additionally, ODT operates asynchronously when the DLL is synchronizing after being reset. See "Power-Down Mode" on page 151 for definition and guidance over power-down details.

In asynchronous ODT timing mode, the internal ODT command is not delayed by AL relative to the external ODT command. In asynchronous ODT mode, ODT controls R_{TT} by analog time. The timing parameters ^{t}AONPD and ^{t}AOFPD (see Table 82 on page 173) replace ODTL on/^{t}AON and ODTL off/^{t}AOF, respectively, when ODT operates asynchronously (see Figure 119 on page 173).

The minimum R_{TT} turn-on time (^{t}AONPD [MIN]) is the point at which the device termination circuit leaves High-Z and ODT resistance begins to turn on. Maximum R_{TT} turn-on time (^{t}AONPD [MAX]) is the point at which ODT resistance is fully on. ^{t}AONPD (MIN) and ^{t}AONPD (MAX) are measured from ODT being sampled HIGH.

The minimum R_{TT} turn-off time (^{t}AOFPD [MIN]) is the point at which the device termination circuit starts to turn off ODT resistance. Maximum R_{TT} turn-off time (^{t}AOFPD [MAX]) is the point at which ODT has reached High-Z. ^{t}AOFPD (MIN) and ^{t}AOFPD (MAX) are measured from ODT being sampled LOW.

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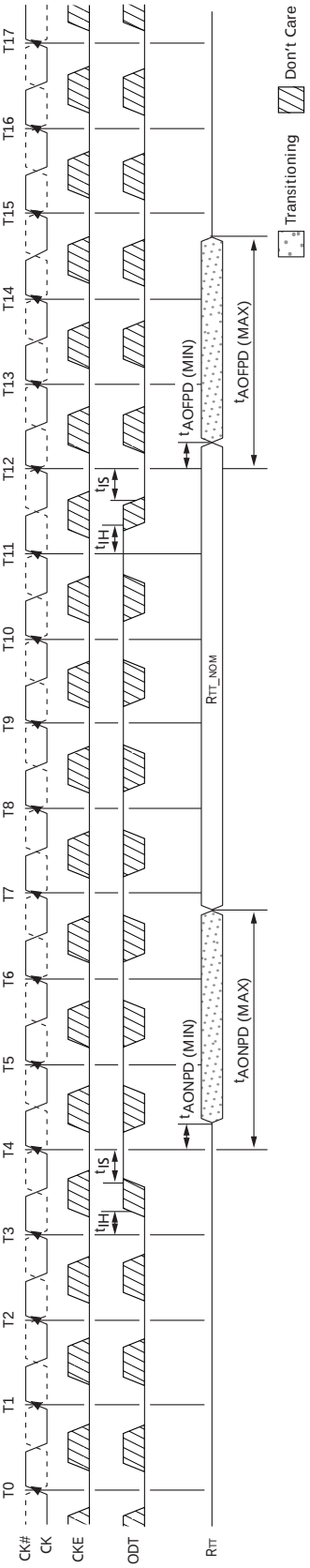
Figure 119: Asynchronous ODT Timing with Fast ODT Transition



Notes: 1. AL is ignored.

Table 82: Asynchronous ODT Timing Parameters for All Speed Bins

Symbol	Description	Min	Max	Units
t_{AONPD}	Asynchronous RTT turn-on delay (power-down with DLL off)	1	9	ns
t_{AOFPD}	Asynchronous RTT turn-off delay (power-down with DLL off)	1	9	ns

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Synchronous to Asynchronous ODT Mode Transition (Power-Down Entry)

There is a transition period around power-down entry (PDE) where the DRAM's ODT may exhibit either synchronous or asynchronous behavior. This transition period occurs if the DLL is selected to be off when in precharge power-down mode by the setting MR0[12] = 0. Power-down entry begins ^{t}ANPD prior to CKE first being registered LOW, and it ends when CKE is first registered LOW. ^{t}ANPD is equal to the greater of ODTL off + 1^{t}CK or ODTL on + 1^{t}CK. If a REFRESH command has been issued, and it is in progress when CKE goes LOW, power-down entry will end ^{t}RFC after the REFRESH command rather than when CKE is first registered LOW. Power-down entry will then become the greater of ^{t}ANPD and ^{t}RFC - REFRESH command to CKE registered LOW.

ODT assertion during power-down entry results in an RTT change as early as the lesser of ^{t}AONPD (MIN) and ODTL on × ^{t}CK + ^{t}AON (MIN) or as late as the greater of ^{t}AONPD (MAX) and ODTL on × ^{t}CK + ^{t}AON (MAX). ODT de-assertion during power-down entry may result in an RTT change as early as the lesser of ^{t}AOFPD (MIN) and ODTL off × ^{t}CK + ^{t}AOF (MIN) or as late as the greater of ^{t}AOFPD (MAX) and ODTL off × ^{t}CK + ^{t}AOF (MAX). Table 83 on page 175 summarizes these parameters.

If the AL has a large value, the uncertainty of the state of RTT becomes quite large. This is because ODTL on and ODTL off are derived from the WL and WL is equal to CWL + AL. Figure 120 on page 175 shows three different cases:

- ODT_A: Synchronous behavior before ^{t}ANPD
- ODT_B: ODT state changes during the transition period with ^{t}AONPD (MIN) less than ODTL on × ^{t}CK + ^{t}AON (MIN) and ^{t}AONPD (MAX) greater than ODTL on × ^{t}CK + ^{t}AON (MAX)
- ODT_C: ODT state changes after the transition period with asynchronous behavior

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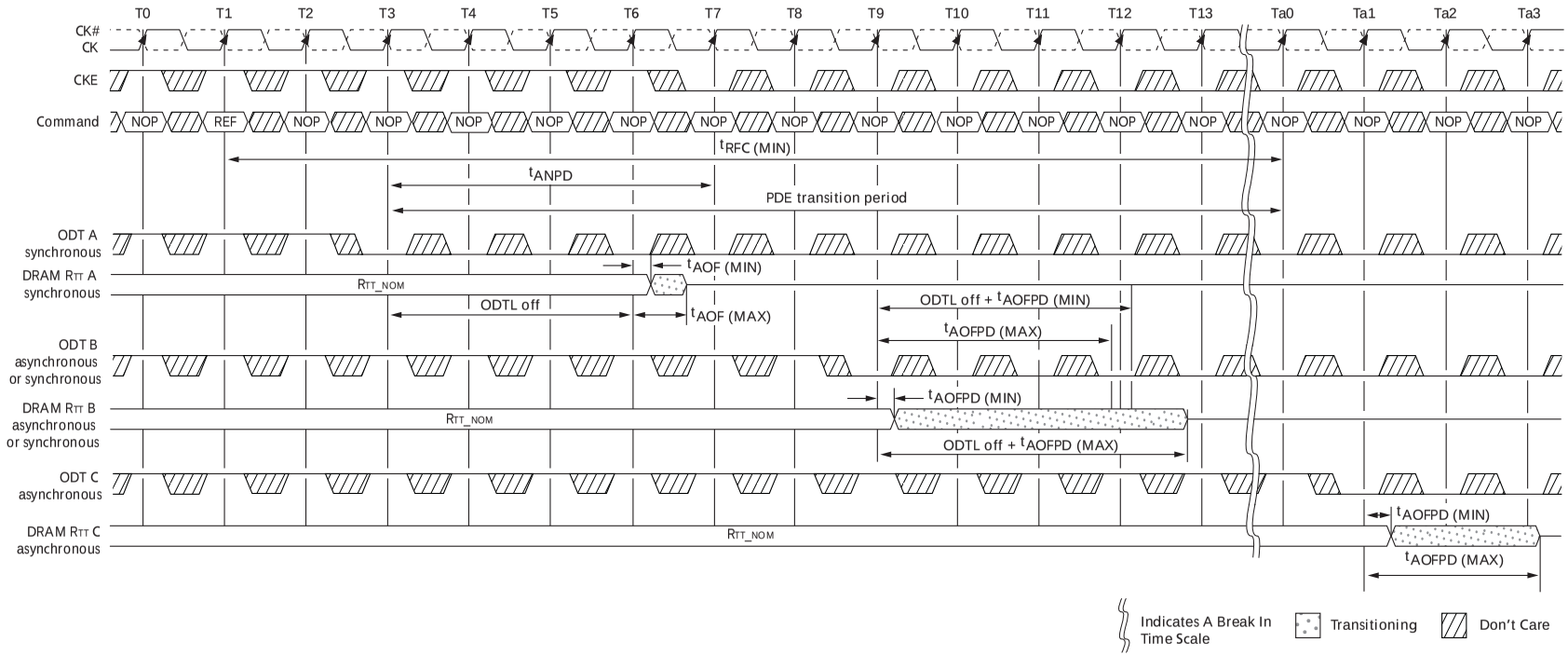
Table 83: ODT Parameters for Power-Down (DLL Off) Entry and Exit Transition Period

Description	Min	Max
Power-down entry transition period (power-down entry)	Greater of: ^{t}ANPD or ^{t}RFC - refresh to CKE LOW	
Power-down exit transition period (power-down exit)	^{t}ANPD + ^{t}XPDLL	
ODT to RTT turn-on delay (ODTL on = WL - 2)	Lesser of: ^{t}AONPD (MIN) (1ns) or ODTL on × ^{t}CK + ^{t}AON (MIN)	Greater of: ^{t}AONPD (MAX) (9ns) or ODTL on × ^{t}CK + ^{t}AON (MAX)
ODT to RTT turn-off delay (ODTL off = WL - 2)	Lesser of: ^{t}AOFPD (MIN) (1ns) or ODTL off × ^{t}CK + ^{t}AOF (MIN)	Greater of: ^{t}AOFPD (MAX) (9ns) or ODTL off × ^{t}CK + ^{t}AOF (MAX)
^{t}ANPD	WL - 1 (greater of ODTL off + 1 or ODTL on + 1)	

Figure 120: Synchronous to Asynchronous Transition During Precharge Power-Down (DLL Off) Entry



Notes: 1. AL = 0; CWL = 5; ODTL off = WL - 2 = 3.

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Asynchronous to Synchronous ODT Mode Transition (Power-Down Exit)

The DRAM's ODT may exhibit either asynchronous or synchronous behavior during power-down exit (PDX). This transition period occurs if the DLL is selected to be off when in precharge power-down mode by setting MR0[12] to "0." Power-down exit begins ^{t}ANPD prior to CKE first being registered HIGH, and it ends ^{t}XPDLL after CKE is first registered HIGH. ^{t}ANPD is equal to the greater of ODTL off + 1^{t}CK or ODTL on + 1^{t}CK. The transition period is ^{t}ANPD plus ^{t}XPDLL.

ODT assertion during power-down exit results in an RTT change as early as the lesser of ^{t}AONPD (MIN) and ODTL on × ^{t}CK + ^{t}AON (MIN) or as late as the greater of ^{t}AONPD (MAX) and ODTL on × ^{t}CK + ^{t}AON (MAX). ODT de-assertion during power-down exit may result in an RTT change as early as the lesser of ^{t}AOFPD (MIN) and ODTL off × ^{t}CK + ^{t}AOF (MIN) or as late as the greater of ^{t}AOFPD (MAX) and ODTL off × ^{t}CK + ^{t}AOF (MAX). Table 83 on page 175 summarizes these parameters.

If the AL has a large value, the uncertainty of the RTT state becomes quite large. This is because ODTL on and ODTL off are derived from the WL, and WL is equal to CWL + AL. Figure 121 on page 177 shows three different cases:

- ODT C: asynchronous behavior before ^{t}ANPD
- ODT B: ODT state changes during the transition period, with ^{t}AOFPD (MIN) less than ODTL off × ^{t}CK + ^{t}AOF (MIN) and ODTL off × ^{t}CK + ^{t}AOF (MAX) greater than ^{t}AOFPD (MAX)
- ODT A: ODT state changes after the transition period with synchronous response

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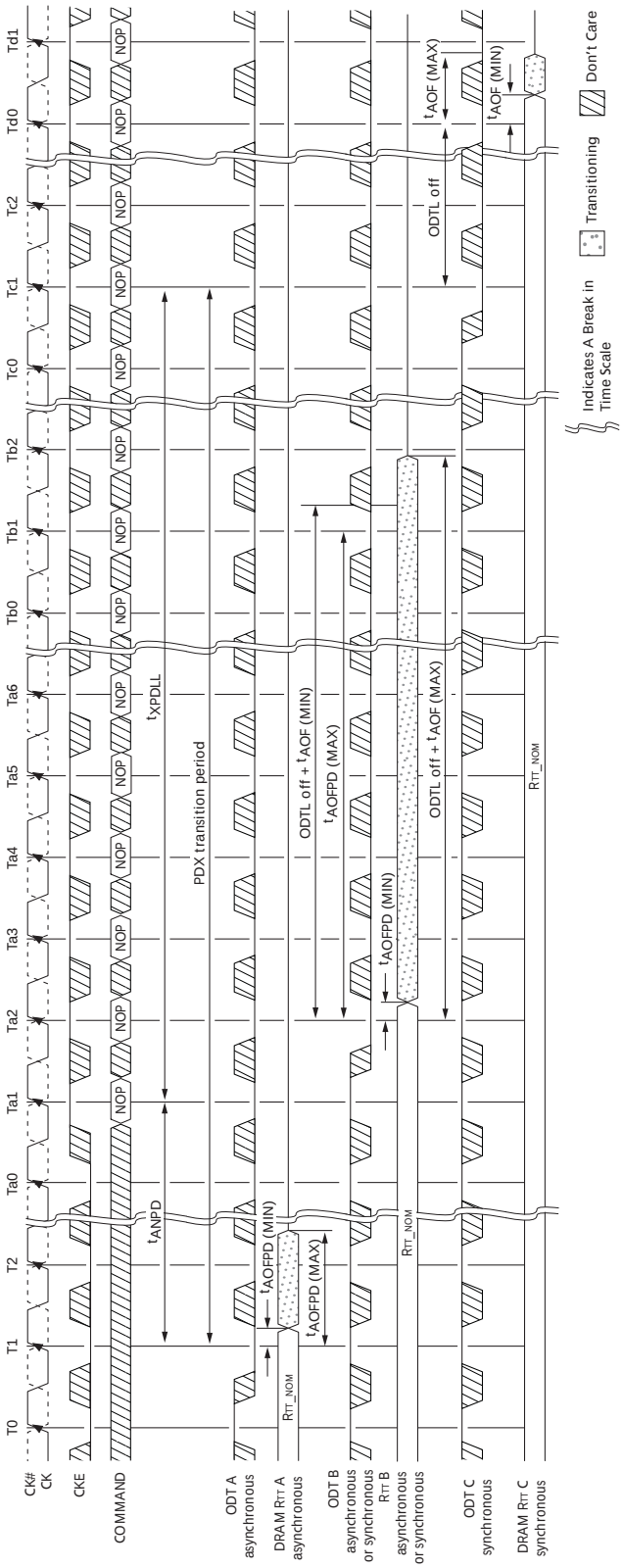
Figure 121: Asynchronous to Synchronous Transition During Precharge Power-Down (DLL Off) Exit



Notes: 1. CL = 6; AL = CL - 1; CWL = 5; ODTL off = WL - 2 = 8.

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Asynchronous to Synchronous ODT Mode Transition (Short CKE Pulse)

If the time in the precharge power down or idle states is very short (short CKE LOW pulse), the power-down entry and power-down exit transition periods will overlap. When overlap occurs, the response of the DRAM's RTT to a change in the ODT state may be synchronous or asynchronous from the start of the power-down entry transition period to the end of the power-down exit transition period even if the entry period ends later than the exit period (see Figure 122 on page 179).

If the time in the idle state is very short (short CKE HIGH pulse), the power-down exit and power-down entry transition periods overlap. When this overlap occurs, the response of the DRAM's RTT to a change in the ODT state may be synchronous or asynchronous from the start of power-down exit transition period to the end of the power-down entry transition period (see Figure 122 on page 179).

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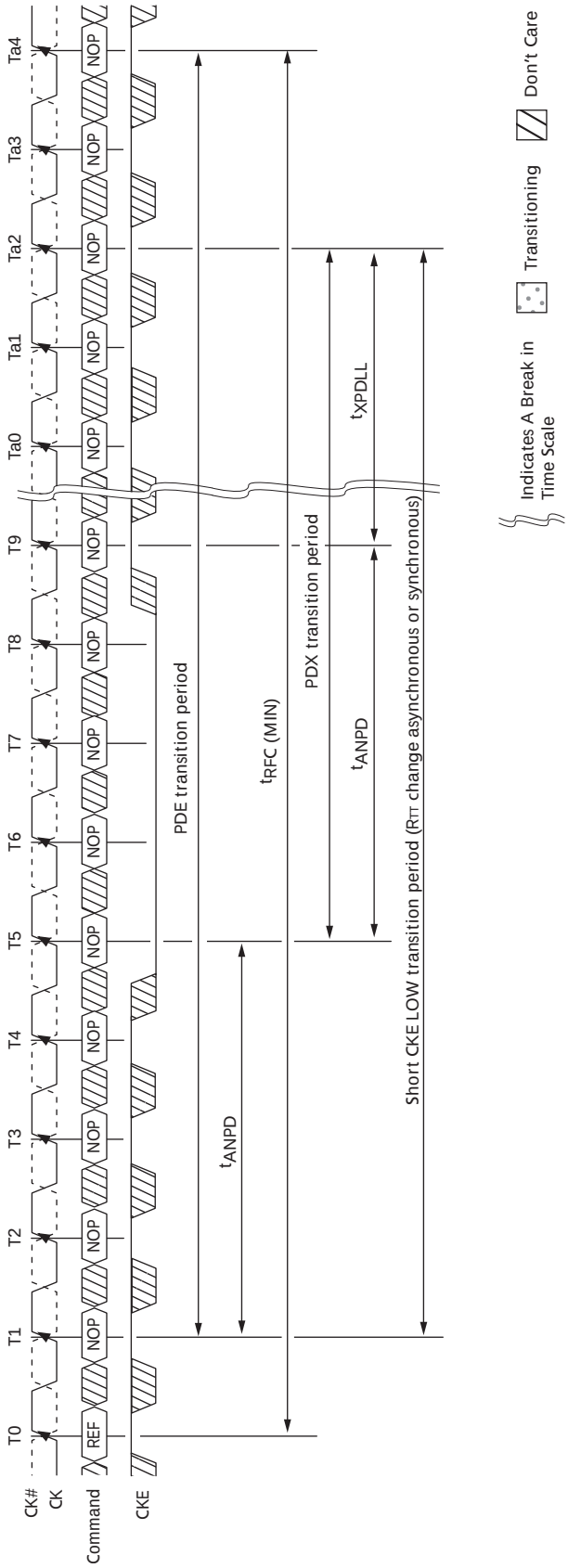
Figure 122: Transition Period for Short CKE LOW Cycles with Entry and Exit Period Overlapping



Notes: 1. AL = 0, WL = 5, ^{t}ANPD = 4.

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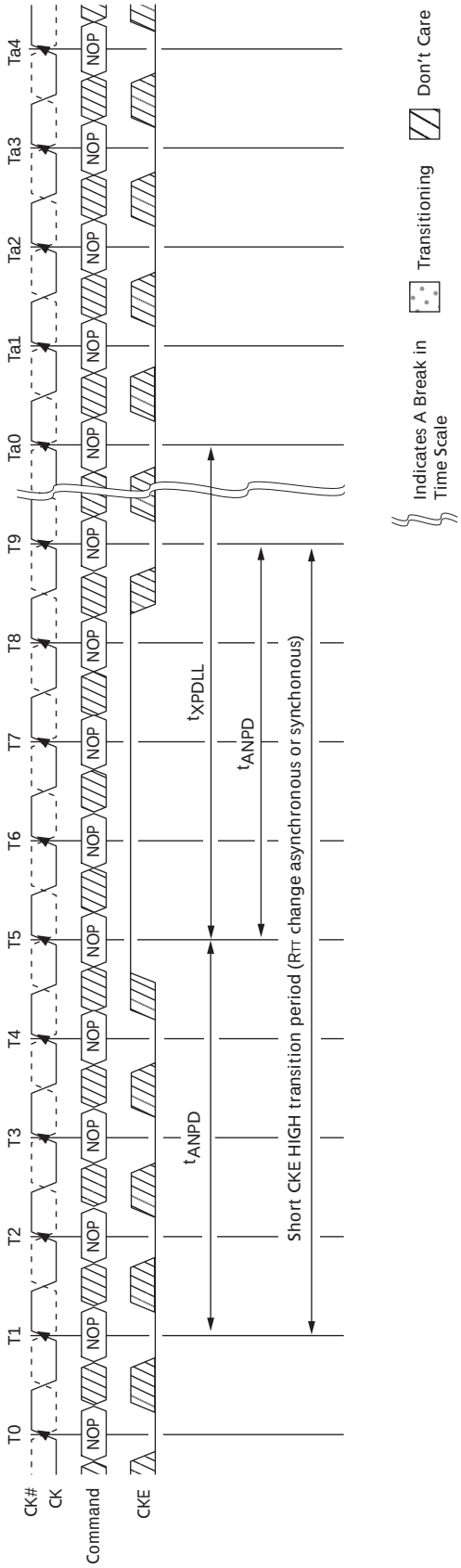
Figure 123: Transition Period for Short CKE HIGH Cycles with Entry and Exit Period Overlapping



Notes: 1. AL = 0, WL = 5, ^{t}ANPD = 4.

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