

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Yuan et al.
U.S. Patent No.: 10,998,017 Attorney Docket No.: 50095-0277IP1
Issue Date: May 4, 2021
Appl. Serial No.: 16/151,347
Filing Date: October 4, 2018
Title: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN
EMBEDDED DISPLAY PORT

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PETITION FOR *INTER PARTES* REVIEW
OF UNITED STATES PATENT NO. 10,998,017

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	REQUIREMENTS FOR IPR—37 C.F.R. §42.104.....	1
	A. Grounds for Standing.....	1
	B. Challenge and Relief Requested.....	1
	C. Claim Construction	4
III.	THE '017 PATENT.....	6
	A. Summary	6
	1. DRAM	6
	2. Embedded Display Port.....	8
	B. Prosecution History.....	10
IV.	LEVEL OF ORDINARY SKILL	10
V.	THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	11
	A. GROUND 1A: Takahashi anticipates and renders obvious claims 1-2 .11	
	1. Takahashi.....	11
	2. Analysis of claims	14
	B. GROUND 1B: Takahashi and Endo render obvious claims 1-2.....	35
	1. Endo.....	35
	2. Claims 1-2	36
	C. GROUND 1C: Takahashi, Tsern, and Schuette render obvious claims 1-2	38
	1. Tsern	38
	2. Schuette	39
	3. Combination of Takahashi, Tsern, and Schuette	40
	4. Analysis of claims	53
	D. GROUND 1D: Takahashi, Endo, Tsern, and Schuette render obvious claims 1-2.....	61
	E. GROUNDS 2A and 2A.1: Dono and Goto render obvious claims 1-2; and Dono, Goto, and Youn render obvious claims 1-2	61
	1. Dono	61
	2. Goto	62
	3. Youn	64
	4. Analysis of claims	66
	F. Grounds 2B and 2B.1: Dono, Goto, and Endo render obvious claims 1-2; and Dono, Goto, Endo, and Youn render obvious claims 1-2.....	87
	1. Claims 1-2	87

VI.	FEES	87
VII.	MANDATORY NOTICES—37 C.F.R § 42.8(a)(1)	87
	A. Real Party-In-Interest—37 C.F.R. § 42.8(b)(1).....	87
	B. Related Matters—37 C.F.R. § 42.8(b)(2)	87
	C. Lead And Back-Up Counsel—37 C.F.R. § 42.8(b)(3).....	88
	D. Service Information	89

LIST OF EXHIBITS

EX1001	U.S. Patent No. 10,998,017 to Yuan et al. (“the ’017 Patent”)
EX1002	Prosecution History of the ’017 Patent (“the Prosecution History”)
EX1003	Declaration and Curriculum Vitae of Dr. David Liu
EX1004	U.S. Patent Application Publication No. 2010/0290300 (“Takahashi”)
EX1005	U.S. Patent Application Publication No. 2012/0327726 (“Tsern”)
EX1006	U.S. Patent Application Publication No. 2010/0142247 (“Schuette”)
EX1007	U.S. Patent Application Publication No. 2012/0327062 (“Endo”)
EX1008	U.S. Patent Application Publication No. 2011/0063927 (“Dono”)
EX1009	U.S. Patent Application Publication No. 2012/0140578 (“Goto”)
EX1010	U.S. Patent No. 7,738,311 (“Youn”)
EX1011	Nakagome et al., “Review and future prospects of low-voltage RAM circuits,” IBM Journal of Research and Development, vol. 47, no. 5.6, p. 525-552 (2003)
EX1012	Keeth et al., <i>DRAM Circuit Design: Fundamental and High-Speed Topics</i> , IEEE Press (2008)
EX1013	“Low Power Double Data Rate 3 (LPDDR3),” JESD209-3, JEDEC Solid State Technology Association (May 2012)
EX1014	VESA Embedded DisplayPort Standard Version 1.3, Video Electronics Standards Association (2011)

EX1015	Craig Wiley, “The New Generation Digital Display Interface for Embedded Applications,” DisplayPort Developer Conference (2010)
EX1016	RESERVED
EX1017	Excerpts from Daintith et al., <i>A Dictionary of Computing, Sixth Edition</i> , Oxford University Press (2008)
EX1018	Excerpts from Harry Newton, <i>Newton’s Telecom Dictionary, 24th Edition</i> , Flatiron Publishing (2008)
EX1019	Excerpts from Downing et al., <i>Dictionary of Computer and Internet Terms, Tenth Edition</i> , Barron’s Educational Series, Inc. (2009)
EX1020	Itoh, <i>VLSI Memory Chip Design</i> , Springer Series in Advanced Microelectronics, Springer-Verlag Berlin Heidelberg New York (2001)
EX1021	Oct. 7, 2025 Complaint, <i>WeCrevention, Inc. v. Apple Inc.</i> , Civil Action No. 7:25-CV-458 (W.D. Tex)
EX1022	Micron Electronics, Inc., “DDR3 SDRAM” (2006)
EX1023	U.S. Patent No. 6,271,679
EX1024	“DDR2 SDRAM Specification,” JESD79-2F, JEDEC Solid State Technology Association (November 2009)
EX1025	U.S. Patent Application Publication No. 2010/0061165
EX1026	Jacob et al., <i>Memory Systems: Cache, DRAM, Disk</i> , Morgan Kaufmann Publishers (2008)
EX1027	RESERVED

EX1028	RESERVED
EX1029	Fairchild Semiconductor 74VCXH162244 datasheet (2005)
EX1030	Texas Instruments SN74AUP1G07 datasheet (2012)
EX1031	Wayne Wolf, <i>Modern VLSI Design: IP-Based Design, Fourth Edition</i> , Prentice Hall (2009)
EX1032	Barth et al., “A 45 nm SOI Embedded DRAM Macro for the POWER™ Processor 32 MByte On-Chip L3 Cache,” in <i>IEEE Journal of Solid-State Circuits</i> , vol. 46, no. 1, pp. 64-75, Jan. 2011
EX1033	J. Barth, “eDRAM to the Rescue,” SRC eDRAM (2009)
EX1034	U.S. Patent No. 7,626,883
EX1035	U.S. Patent No. 6,847,578
EX1036	U.S. Patent No. 8,901,009
EX1037	U.S. Patent No. 8,471,362
EX1038	U.S. Patent No. 7,829,410
EX1039	U.S. Patent No. 7,892,943
EX1040	U.S. Patent No. 8,148,763
EX1041	U.S. Patent No. 7,736,987
EX1042	RESERVED
EX1043	The International Technology Roadmap for Semiconductors - Overall Roadmap Technology Characteristics (2003)

- EX1044 Lee et al., “Tiered-latency DRAM: A low latency and low cost DRAM architecture,” 2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA)
- EX1045 Harvard et al., “A scalable I/O architecture for wide I/O DRAM,” 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)
- EX1046 RESERVED
- EX1047 “VESA Publishes Embedded DisplayPort Standard Version 1.5,” <https://www.prnewswire.com/news-releases/vesa-publishes-embedded-displayport-standard-version-1-5--301410053.html/> (accessed Dec. 24, 2025)
- EX1048 Gillingham, “Unleashing the Power of Embedded DRAM” (2005)
- EX1049 AP Memory, AD351216F-x 512Mb LPDDR3, “512Mb LPDDR3 Specification” (2022)
- EX1050 U.S. Patent Application Publication No. 2009/0080234
- EX1051 Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2025) | United States Courts (uscourts.gov), available at: [fcms_na_distprofile1231.2025.pdf](#)

LISTING OF CLAIMS

Claim 1	
[1.1]	A dynamic random access memory (DRAM), comprising:
[1.2]	a DRAM core cell,
[1.3]	wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and
[1.4]	the DRAM core cell is a volatile memory cell,
[1.5]	wherein the first voltage is lower than 1.1V; and
[1.6]	a peripheral circuit electrically connected to the DRAM core cell,
[1.7]	wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage,
[1.8]	wherein the second voltage is lower than 1.1V, and
[1.9]	wherein the DRAM core cell and the peripheral circuit are formed on a single chip,
[1.10]	and the peripheral circuit is external to the DRAM core cell;
[1.11]	wherein the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP).
Claim 2	
[2.1]	The dynamic random access memory of claim 1, further comprising: an input/output unit electrically connected to the peripheral circuit and the DRAM core cell
[2.2]	for operating in a third voltage,
[2.3]	wherein the third voltage is lower than 1.1V.

I. INTRODUCTION

Apple Inc. (“Petitioner” or “Apple”) petitions for IPR of claims 1 and 2 of U.S. Patent No. 10,998,017 (“the ’017 Patent”) assigned to WeCrevention, Inc. (“Patent Owner”/“PO”). Compelling evidence presented in this Petition demonstrates at least a reasonable likelihood that Apple will prevail with respect to at least one of the Challenged Claims. Accordingly, Apple respectfully submits that an IPR should be instituted, and that the Challenged Claims should be canceled as unpatentable.

II. REQUIREMENTS FOR IPR—37 C.F.R. §42.104

A. Grounds for Standing

Petitioner certifies that the ’017 Patent is available for IPR, and that Petitioner is not barred or estopped from requesting an IPR of the Challenged Claims on the below-identified grounds.

B. Challenge and Relief Requested

Petitioner requests an IPR of the Challenged Claims on the grounds set forth in the table below, and requests that each of the Challenged Claims be found unpatentable for the reasons described within the Petition in EX1003, the Declaration of Dr. David Liu (“Expert Declaration”). EX1003, 1-234.

Asserted Grounds		
GROUND	Claims	Prior Art Basis
1A	1-2	§102/103: Takahashi (US2010/0290300)
1B	1-2	§103: Takahashi+Endo (US2012/0327062)
1C	1-2	§103: Takahashi+Tsern (US2012/0327726)+Schuette (US2010/0142247)
1D	1-2	§103: Takahashi+Endo+Tsern+Schuette
2A [2A.1]	1-2	§103: Dono (US2011/0063927)+Goto (US2012/0140578) [§103: Dono+Goto+Youn (US7738311)]
2B [2B.1]	1-2	§103: Dono+Goto+Endo [§103: Dono+Goto+Endo+Youn]

The '017 patent was filed on 10/4/18 and claims priority from several previously-filed applications, the earliest of which was filed on 7/17/12. Each of the references asserted in this Petition qualifies as prior art even if the 7/17/12 date (hereinafter “Critical Date”)¹ is used as the '017 Patent's earliest possible priority date.

Reference	Filing/Publication dates	Prior art under ²
Takahashi	(F) 4/28/2010;	§102(a), (b), (e)

¹ Petitioner does not concede that Challenged Claims are entitled to the 7/17/12 date.

² Petitioner assesses the '017 Patent under pre-AIA 35 U.S.C. If the effective filing date is taken as 6/19/2013 (the filing date of Application No. 13/922,242),

Reference	Filing/Publication dates	Prior art under ²
	(P) 11/18/2010	
Dono	(F) 9/10/2010; (P) 3/17/2011	§102(a), (b), (e)
Endo	(F) 4/5/2012; (P) 12/27/2012	§102(e)
Schuette	(F) 12/7/2009; (P) 6/10/2010	§102(a), (b), (e)
Tsern	(F) 2/23/2010 (provisional); 12/1/2010 (PCT); (P) 12/27/2012	§102(e)
Goto	(F) 11/28/2011; (P) 6/7/2012	§102(a), (e)
Youn	(F) 11/6/2007; (P) 6/15/2010	§102(a), (b), (e)

All cited references are analogous art at least insofar as they are from the same field of endeavor (e.g., DRAM) as the '017 Patent, and are pertinent to the problems the '017 Patent was trying to solve. EX1001, 2:18-34, 4:40-61, 6:9-10; EX1004,

the '017 Patent is subject to post-AIA 35 U.S.C, and the applied references applied are also prior art.

[0018], [0045], [0082]-[0083]; EX1005, [0005], [0019]; EX1006, [0003], [0014], [0029]; EX1007, [0034]-[0035]; EX1008, [0005]-[0007], [0024]; EX1009, [0022], [0027]; EX1010, 5:49-67; EX1003, 46.

C. Claim Construction

The recited “input/output unit” should be construed as a §112(f) means-plus-function limitation. Based on its name, the input/output unit is a unit that performs input and/or output functions with respect to a memory. EX1001, 6:15-17 (“The dynamic random access memory of claim 1, further comprising: an input/output unit”).

The Specification’s most detailed description of corresponding structure is provided at 2:50-65 in relation to the “Input/output unit” 106 that is depicted in the Specification’s sole “FIGURE” as one box connected to two other boxes (respectively labeled “Memory core unit” 102 and “Peripheral circuit unit” 104). At 2:49-64, the Specification notes without further explanation that “the dynamic random access memory **100** includes a memory core unit **102**, a peripheral circuit unit **104**, and an input/output unit **106**, where the peripheral circuit unit **104** is electrically connected to the memory core unit **102**, and the input/output unit **106** is electrically connected to the peripheral circuit unit **104** and the memory core unit **102**.” EX1001, 2:49-64; *see also* Abstract, 1:64-2:34.

As explained in detail in Section V., *infra*, the prior art cited and applied in this Petition discloses the claimed input/output functions and at least as much structure as the '017 Patent's Specification with respect to the applied input/output units; in doing so, the applied prior art anticipates or renders obvious the Challenged Claims, regardless of whether "input/output unit" is construed as a §112(f) means-plus-function limitation. EX1003, 104-106.

All other claim terms should be construed according to their ordinary and customary meaning under the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. Petitioner submits that no other claim terms need be construed to resolve issues of controversy in the present Petition, but reserves the right to respond to construction issues raised by Patent Owner. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Petitioner is not conceding that each challenged claim satisfies all statutory requirements (for example, that the '017 Patent provides adequate structure for the "input/output unit"), nor waiving arguments/grounds that cannot be raised in this proceeding.

III. THE '017 PATENT

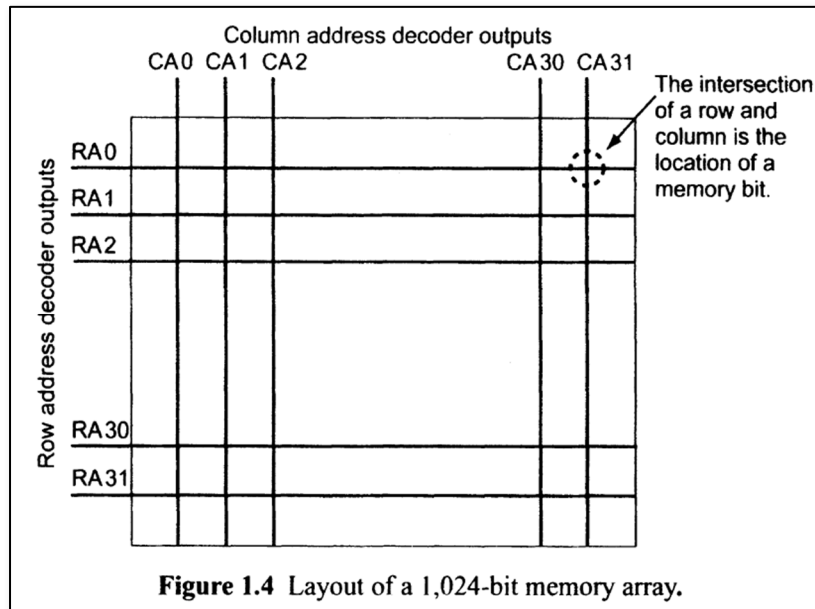
A. Summary

The '017 Patent relates to two technologies: dynamic random access memory (DRAM) and embedded display port interfaces. EX1003, 29-30.

1. DRAM

DRAM is a type of random access memory typically used as the primary memory of computing devices. EX1003, 31. In a DRAM device, memory cells are organized in an array. Each memory cell has a “row” position and a “column” position with which the memory cell can be addressed. EX1012, 16-18; EX1003, 31.

Voltages can be applied to “wordlines” (corresponding to a row) and “bitlines” (corresponding to a column) to store a 0 or 1 in a target memory cell, or to read out stored data. EX1012, 17-24; EX1003, 32. DRAM is referred to as “dynamic” because, once stored in a cell, charge (representing data) will “leak off over time.” EX1012, 20; EX1003, 33. To prevent loss of data, a “refresh” operation is performed periodically. EX1012, 19; EX1003, 33.



EX1012, FIG. 1.4

A DRAM device is provided with one or more external voltages, which may be converted to internal voltages supplied to various circuits of the device. EX1003, 34. The Low Power Double Data Rate 3 (LPDDR3) standard, published in May 2012 by the Joint Electron Device Engineering Council (JEDEC), defines several external voltages, including V_{DD1} (used for the memory cell array), V_{DD2} (used for peripheral circuitry), and V_{DDQ} (used for the input/output (I/O) circuit). EX1013, 83; EX1003, 34.

The '017 Patent purports to improve DRAMs by specifying lower voltages for memory circuitry. EX1001, 4:62-65; EX1003, 35. Specifically, the '017 Patent describes that DRAMs can have “operation voltages” of “<1.1 V” for each of a “memory core unit,” a “peripheral circuit unit,” and an “input/output unit.” EX1001,

Table II. These voltages, which are slightly lower than the external voltages specified by the LPDDR3 standard, result in “power consumption [that]...is much lower than power consumption of the [DRAM] operating in the operation voltages specified by the [JEDEC].” EX1001, 4:6-10; EX1003, 35.

The '017 Patent provides no technical detail on how DRAM using these low voltages might be achieved. EX1003, 36.

The desire for low voltage DRAM operation was not new and, unlike the '017 Patent, the prior art applied in this Petition provides not only *disclosure* of low DRAM voltages, but also details on *how the low voltages may be successfully used in real DRAM circuits*. EX1003, 36. Indeed, voltages within the ranges recited by the '017 Patent had been a subject of research for decades, and low-voltage DRAM circuits had been successfully manufactured and publicized. EX1011; EX1043; EX1003, 37.

2. Embedded Display Port

The embedded display port (eDP) standard “defines requirements and options of a standardized display panel interface for embedded display applications.” EX1014, 12. Version 1.3 of the eDP standard, published in 2011, introduces a “panel self-refresh” (PSR) feature. EX1014, 12, 21, 65; EX1003, 38.

According to eDP 1.3, a display device’s “timing controller” (TCON) includes a “remote frame buffer” (RFB). EX1014, 27, 65; EX1015, 24; EX1003, 39.

The RFB “can maintain [a] display image without receiving video data from [the] GPU [graphical processing unit].” EX1015, 25. This means that, when an eDP 1.3 display is showing a still image, the GPU can “enter a low power state...[a]llowing the GPU to power down between display updates.” EX1015, 25; EX1003, 39. Instead of using the GPU, the display can draw the static image from the RFB, reducing power consumption. EX1015, 26; EX1003, 39-40.

The '017 Patent states that “power consumption of the timing controller is increased due to operation of the frame buffer,” and therefore seeks “to design the frame buffer to reduce the power consumption.” EX1001, 1:56-59; EX1003, 41. According to the '017 Patent, “the operation voltages specified by [JEDEC] can not satisfy requirements (that is, the lower operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3.” EX1001, 3:22-27.

The '017 Patent does not describe what these “requirements” are, and, as discussed below in §V.A.2(a) ([1.11]), the eDP 1.3 standard in fact includes no such power requirements. EX1003, 42.

Despite that, the '017 Patent asserts that “power consumption of the [DRAM] of the present invention is much lower than power consumption of a [DRAM] operating in the operation voltages specified by [JEDEC],” and that “when the [DRAM] of the present invention is applied to an embedded display port, the present

invention can make system power consumption...be significantly reduced.”
EX1001, 4:65-5:7; EX1003, 43.

B. Prosecution History

The '017 Patent was issued on May 4, 2021 after rejections over references including “Mohammad” (US 2009/0122620) and/or Takahashi (EX1004), and the final rejection was over Takahashi alone. EX1002, 37-43, 84-91, 120-129, 159-166, 188-195. The claims were allowed after the applicant amended the sole independent claim to recite that “the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP),” and the Examiner also cited this feature in the Reasons for Allowance. EX1002, 12, 28. Despite the “eDP” feature being the apparent reason for allowance of the '017 Patent, the record is silent as to what voltages would be “capable of making the DRAM be applied to an embedded display port (eDP).” EX1003, 44-45. In fact, the eDP 1.3 standard cited by the '017 Patent includes no voltage or power requirements for a memory applied to an eDP. EX1003, 45. *See* §V.A.2(a) ([1.11]). As discussed below, the cited DRAMs—including Takahashi’s—were entirely “capable of being applied to an [eDP].” EX1003, 45.

IV. LEVEL OF ORDINARY SKILL

The range of qualifications for a POSITA would have included at least a master’s degree in electrical engineering, or a comparable field, and at least two

years of professional experience working with semiconductor memory, including DRAM. EX1003, 27-28. Additional years of experience could substitute for an advanced-level degree (and vice versa). *Id.*

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A: Takahashi anticipates and renders obvious claims 1-2

1. Takahashi

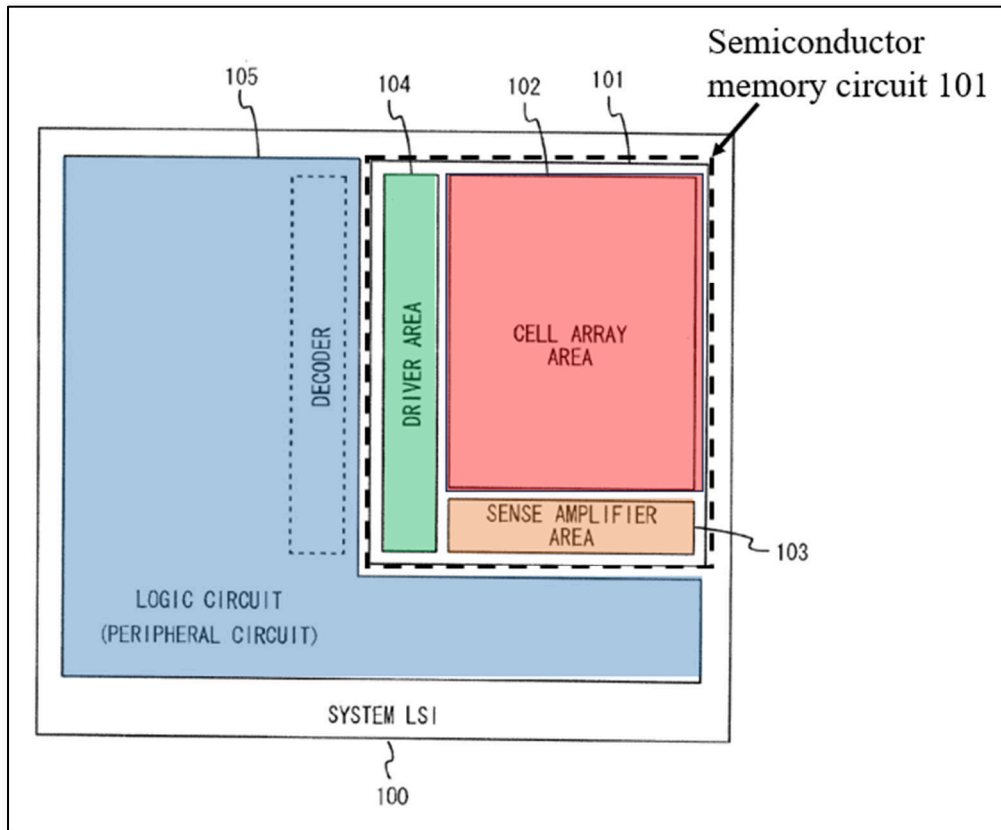
Takahashi describes a “built-in DRAM” that can provide “higher speed operation.” EX1004, [0021], [0047]; EX1003, 47.³

As shown in implementations of Takahashi depicted, e.g., in FIG. 1, Takahashi’s “device 100” includes a “semiconductor memory circuit 101” and a “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit.” EX1004, [0047], [0078]; EX1003, 48.⁴ Memory circuit 101 includes “a cell

³ This discussion of Takahashi is incorporated further into Grounds 1B-1D. Similarly, discussion of other references is incorporated into all grounds advancing the same.

⁴ In below addressing invalidity of the Challenged Claims over the teachings of the cited references, Petitioner relies on the teachings of those references as would have

array area 102, a sense amplifier area 103, and a driver area 104.” EX1004, [0047]; EX1003, 48.

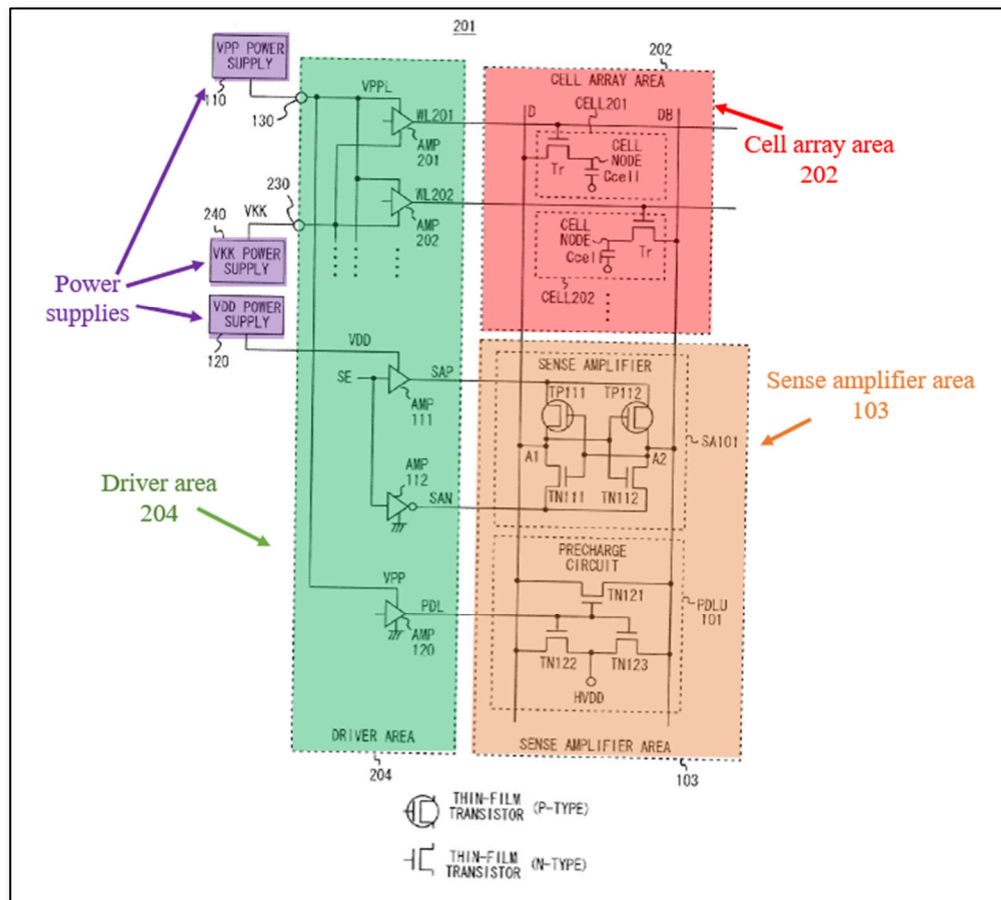


Takahashi, FIG. 1

Takahashi’s FIG. 7 (reproduced below) shows a configuration of a memory circuit 201 similar to that of FIG. 1. EX1004, [0077]-[0079]; EX1003, 49. Power to a cell array area 202, a sense amplifier area 103, and a driver area 204 is supplied by a VPP power supply 110, a VKK power supply 240, and a VDD power supply 120.

been understood by a POSITA, without necessarily relying upon incorporation of each or any of the disclosed or referenced exemplary details.

EX1004, [0081]-[0083], FIG. 7; EX1003, 49. These power supplies output voltages VPPL, VKK, and VDD, respectively. EX1004, [0081]-[0083], FIG. 7; EX1003, 50. VDD is also provided to the logic circuit 105. EX1004, [0045]-[0046]; EX1003, 50.



Takahashi, FIG. 7

Takahashi provides specific values for these voltages: “the power supply voltage VDD is 0.8 V, the voltage VPPL is 1.0 V, and the voltage VKK is -0.3 V.” EX1004, [0084]; EX1003, 51.

2. Analysis of claims

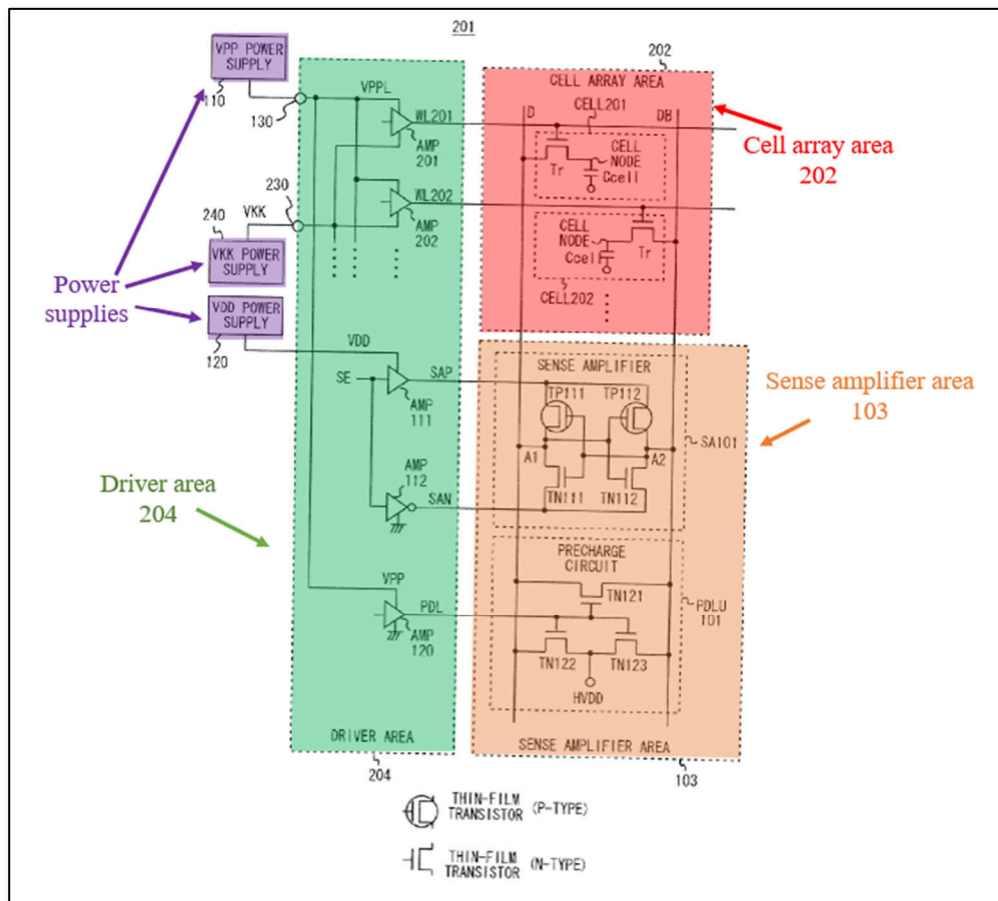
(a) Claim 1

*[1.1]: A dynamic random access memory (DRAM), comprising:*⁵

Takahashi's "semiconductor memory circuit 201 is a built-in DRAM of a system LSI." EX1004, [0078]; EX1003, 53.

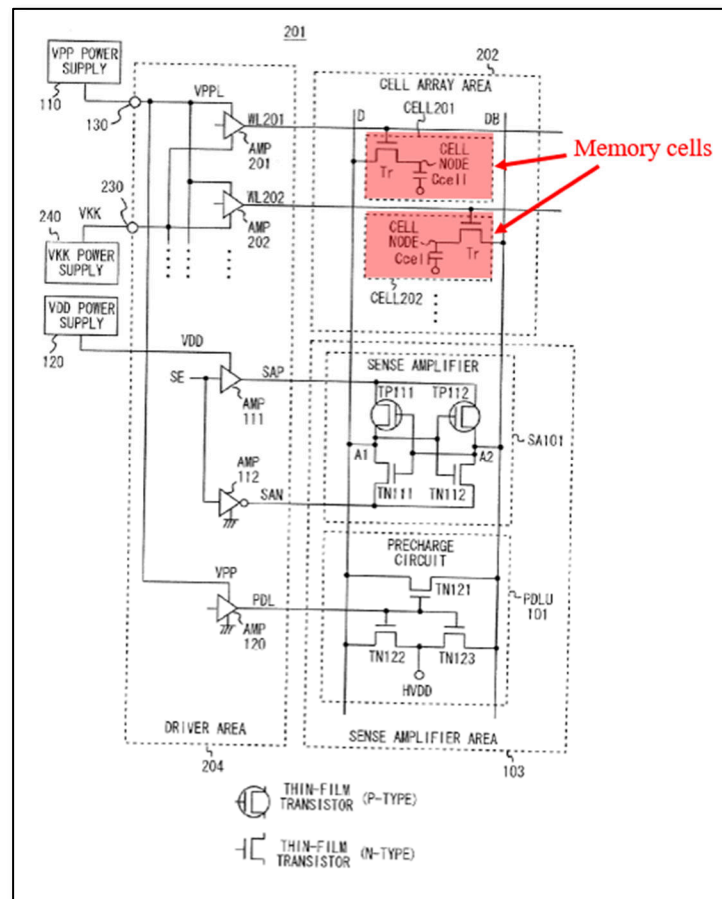
In more detail, and as shown in Takahashi's FIG. 7 (reproduced below), Takahashi's DRAM semiconductor memory circuit 201 includes a sense amplifier area 103, a driver area 204, and a cell array area 202 that includes memory cells. EX1004, [0077]-[0083], FIG. 7; EX1003, 54. Cell array area 202 is supplied by a VPP power supply 110 and a VKK power supply 240, while sense amplifier area 103 and driver area 204 are supplied by a VDD power supply 120. EX1004, [0081]-[0083], FIG. 7; EX1003, 54.

⁵ Petitioner does not concede that this preamble is limiting.



[1.2]: a DRAM core cell,

The “memory cells” in Takahashi’s DRAM are DRAM core cells. EX1004, [0079]-[0080]; EX1003, 55. For example, Takahashi discloses that the “semiconductor memory circuit 201 includes a cell array area 202... The cell array area 202 includes multiple memory cells CELLS.” EX1004, [0079]-[0080]; EX1003, 55.

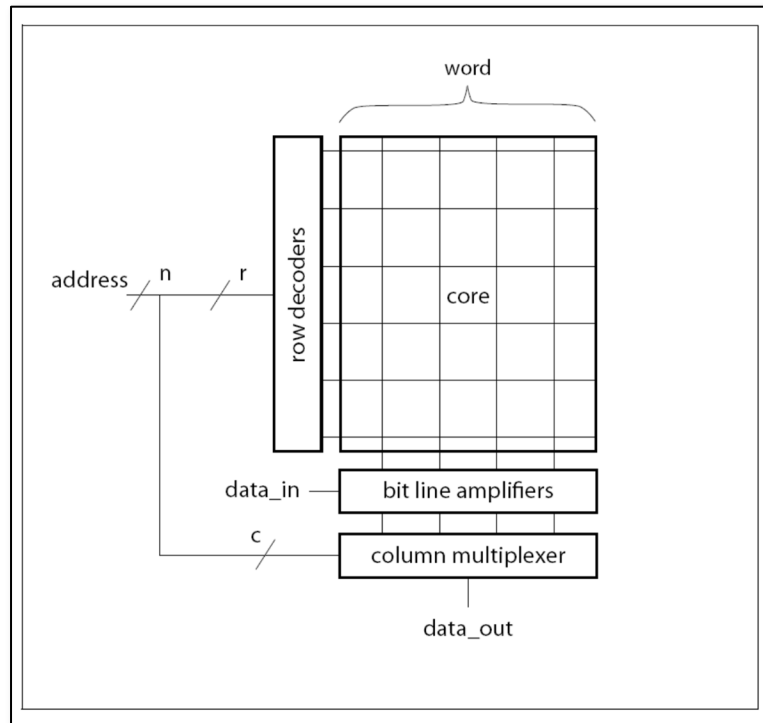


Takahashi, FIG. 7

A POSITA would have understood that these DRAM memory cells are each a “DRAM core cell.” EX1003, 56. As Dr. Liu explains, the “core” in “DRAM core cell” refers to, or at least encompasses, the cell array of a memory, which performs the memory’s data storage function. EX1003, 56. Thus, DRAM memory cells are “DRAM core cell[s].” EX1003, 56.

For example, the textbook *Modern VLSI Design: IP-Based Design* provides the below diagram in which the memory cell array is labeled as a “core.” EX1031, 385; EX1003, 57. The same textbook also refers to the “memory core” and refers to

a DRAM data storage cell as a “RAM core cell.” EX1031, 385, 391-392; EX1003, 57-58.

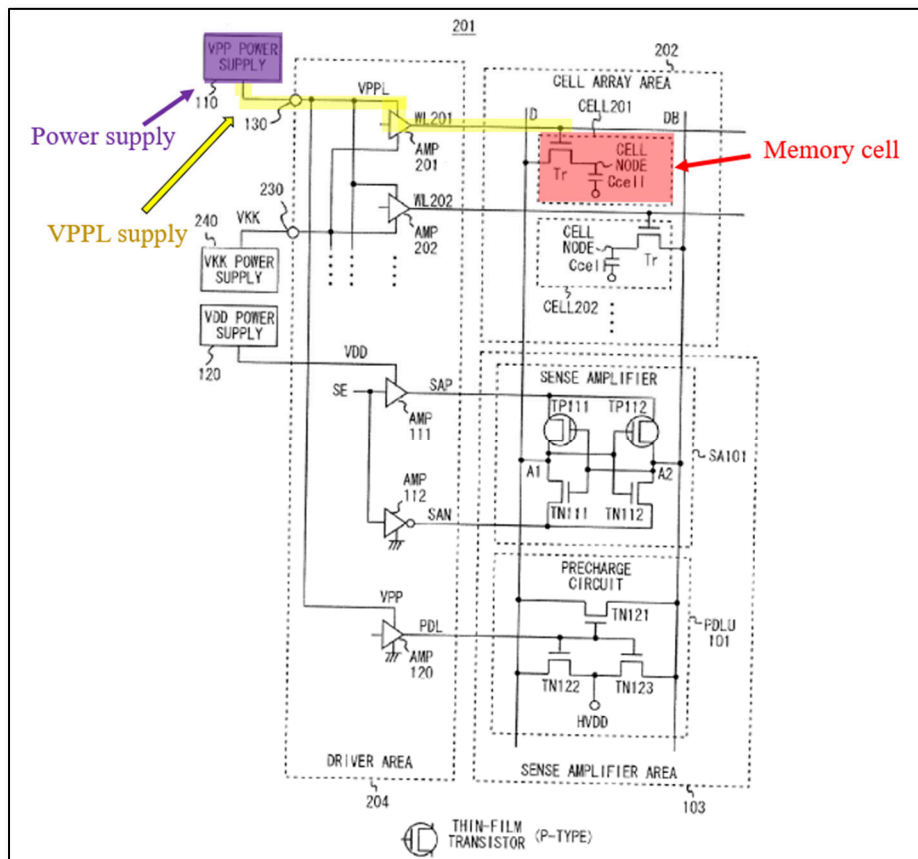


EX1031, Figure 6-16

[1.3]: wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and

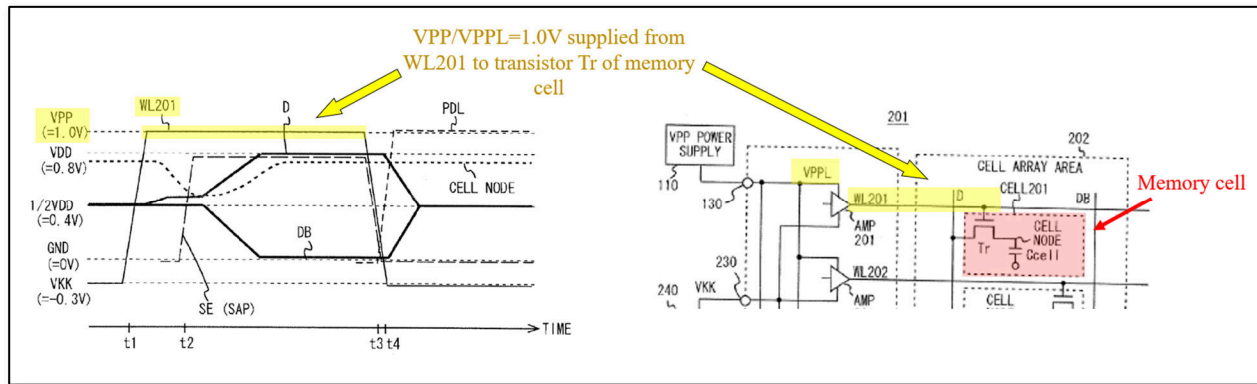
Takahashi's memory cells are supplied with a **first voltage VPPL**⁶ to make those cells operate at that voltage. EX1003, 59. As Takahashi explains, “the memory cells ...use a voltage VPPL, which is supplied from the VPP power supply 110.” EX1004, [0081]; EX1003, 59. Supply of VPPL to memory cells is performed through the transmission path shown below. EX1004, FIG. 7; EX1003, 60.

⁶ Emphasis is added throughout, except where noted otherwise.



Takahashi, FIG. 7

Supply of the first voltage VPPL (sometimes also referred to as VPP in the context of FIGS. 7-8) to a memory cell is shown explicitly in Takahashi FIG. 8. EX1003, 60-61. As shown, “at the time t1, the word signal WL201 rises to the voltage VPP [=1.0 V].” EX1004, [0084]-[0085], FIG. 8; EX1003, 61. The wordline 201 is connected to a gate of the transistor Tr, such that a first voltage of 1.0 V is supplied to memory cell 201. EX1004, [0083]-[0085], FIG. 8; EX1003, 61.



Left: Takahashi, FIG. 8; Right: Takahashi, FIG. 7 (partial)

The memory cell “use[s],” or operates at, the “voltage VPPL.” EX1004, [0081]; EX1003, 62. For example, based on provision of VPPL to the memory cell, “CELL 201 is turned on.” EX1004, [0085]; EX1003, 62.

Claim 1 recites that the first voltage is “within a first voltage range,” but none of the Challenged Claims limit the “first voltage range,” or even refer to it again. The “first voltage range” is therefore any range that includes the claimed “first voltage” that is “lower than 1.1V,” for example, 0.5-1.5 V. EX1001, 5:21-6:3. Takahashi’s disclosed VPPL=1.0V is “within” any such range. EX1003, 63-64.

Further, a POSITA would have understood that the voltage VPPL is “within a first voltage range” due to standard voltage variation. EX1003, 65. Dr. Liu describes that in practice “every voltage is defined or provided within a range...attributable to non-idealities such as temperature dependence, device-to-device variation, load dependence, and the like.” EX1003, 65. For example, Takahashi refers to VPPL as being “reduced to about 1.0V,” where “about” might

refer to a small level of expected variation. EX1004, [0083]; EX1003, 65. This small variation would have been understood by a POSITA as a “first range” that the first voltage VPPL is within. EX1003, 65.

[1.4]: the DRAM core cell is a volatile memory cell,

A POSITA would have understood that Takahashi’s DRAM (dynamic random access memory) core cell is, by definition, a volatile memory cell. EX1003, 66. For example, *A Dictionary of Computing* describes “dynamic memory” as a “form of **volatile** semiconductor memory in which stored information is degraded with time. The **most common example is dynamic RAM** (usually abbreviated to **DRAM**).” EX1017, 4-5. *See also* EX1018, 4-5; EX1019, 3-4; EX1003, 66-67.

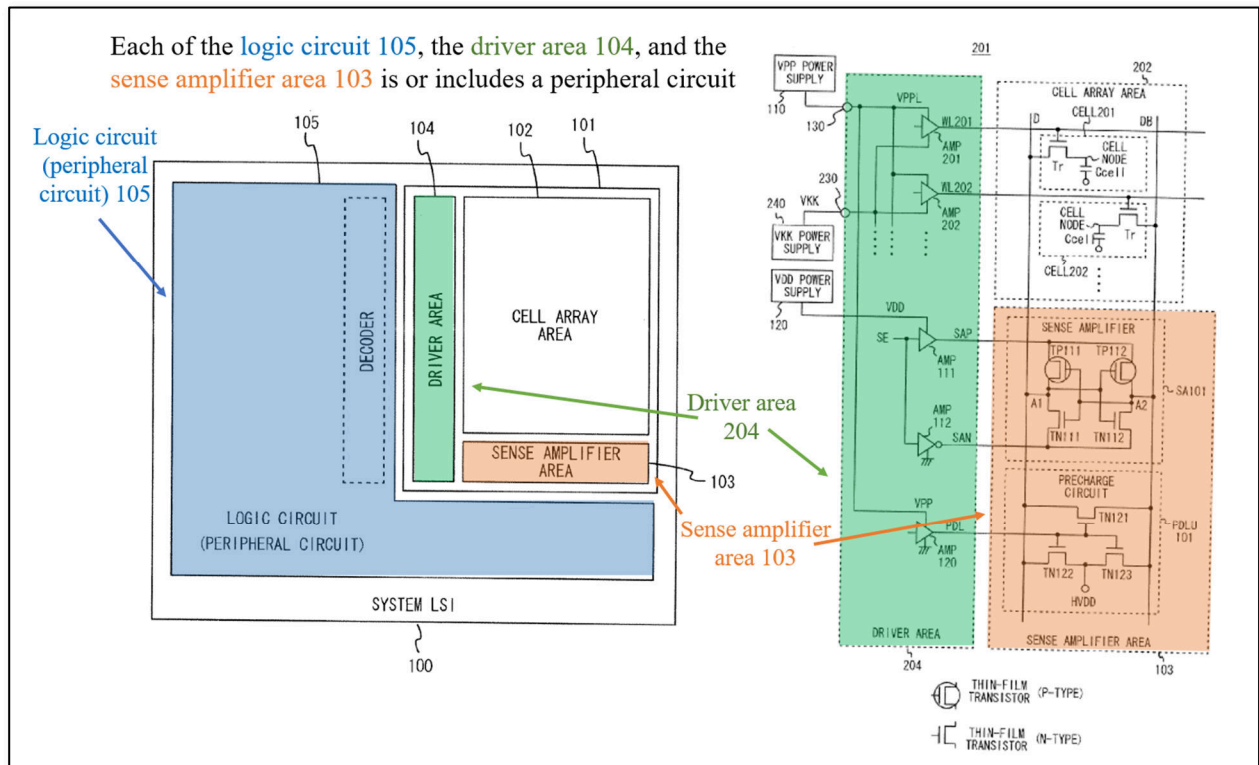
[1.5]: wherein the first voltage is lower than 1.1V; and

Takahashi discloses that the first voltage VPPL is **1.0 V**, which is lower than 1.1 V. EX1003, 68. *See* Takahashi [0083] (“the voltage VPPL supplied from the VPP power supply 110 can be reduced to about 1.0V”), FIG. 8. EX1004, [0083]-[0084], FIG. 8; EX1003, 68.

[1.6]: a peripheral circuit electrically connected to the DRAM core cell,

Takahashi discloses a peripheral circuit electrically connected to the DRAM core cell. EX1003, 69. According to the applicant’s proposed definition of “peripheral circuit” in the context of Takahashi, peripheral circuits electrically connected to the DRAM core cell include the “sense amplifier area 103” (e.g., “sense

amplifier SA101”), the “driver area 204” (e.g., driver amplifier AMP111), and at least a portion of the “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201.” EX1004, [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7; EX1003, 69.



Left: Takahashi, FIG. 1; Right: Takahashi, FIG. 7

⁷ FIG. 1 of Takahashi depicts a “semiconductor integrated device 100” of Takahashi’s “First Exemplary Embodiment,” whereas FIGS. 7 and 8 relate to a “semiconductor integrated device 200” of a “Second Exemplary Embodiment.” EX1004, [0026], [0034], [0043], [0077]; EX1003, 82. However, a POSITA would

have understood that the device 200 (which is not illustrated with a view similar to that of FIG. 1) has the same overall configuration as the device 100. EX1003, 82. Accordingly, this Petition utilizes FIG. 1 in connection with the device 200.

For example, Takahashi describes that “the semiconductor integrated device 200 of the second exemplary embodiment has a configuration in which the semiconductor memory circuit 101 of the semiconductor integrated device 100 shown in FIG. 1 is replaced with the semiconductor memory circuit 201.” EX1004, [0077]. From this and other disclosure (as further elaborated by Dr. Liu), a POSITA would have understood unambiguously, and found obvious, that the device 200 of FIGS. 7-8 includes substantially similar elements, arranged in substantially the same way, as the device 100 of FIG. 1. EX1003, 83.

For example, although the logic circuit 105 is illustrated only in FIG. 1, a POSITA would have understood that the second embodiment also includes the logic circuit 105. EX1004, [0026], [0034], FIG. 1; EX1003, 84. Similarly, a POSITA would have understood that the driver area 204, cell area 202, and sense amplifier 103 shown in FIG. 7 have a configuration substantially similar to that of the driver area, cell array area 102, and sense amplifier area 103 shown in FIG. 1. EX1003, 85.

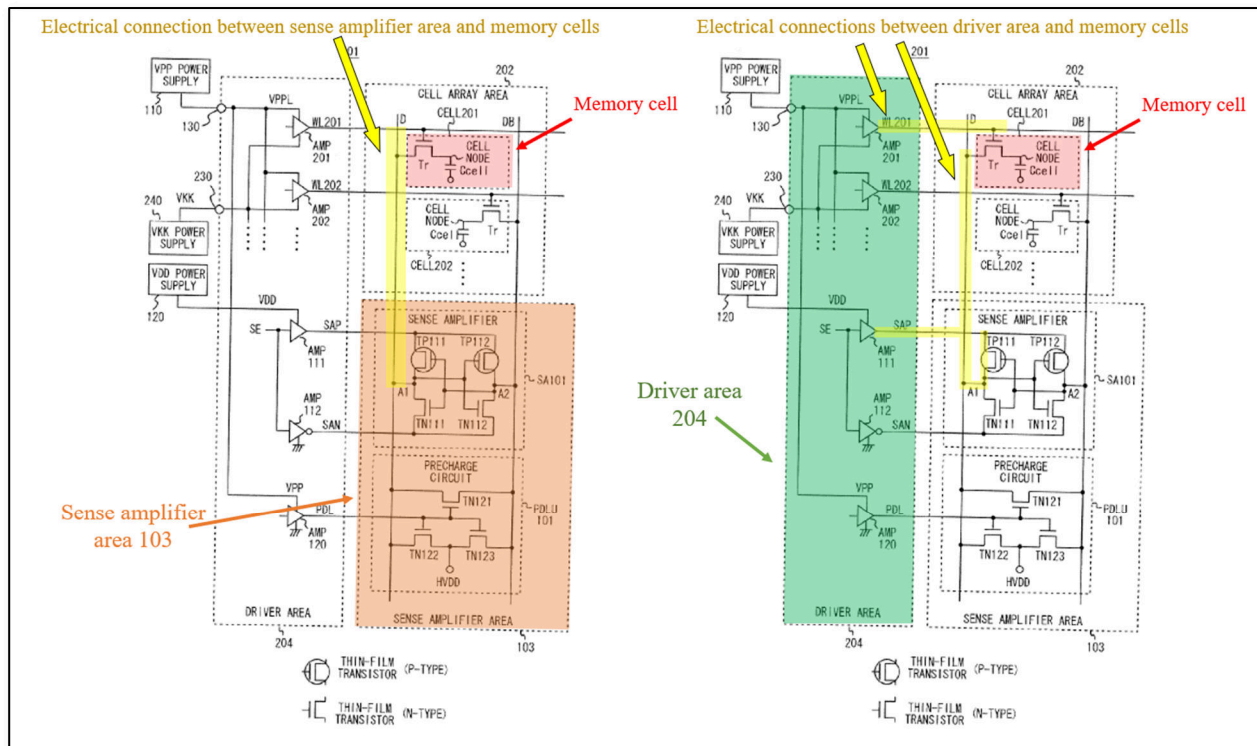
During prosecution of the '017 Patent, the applicant *explicitly* argued that drivers, sense amplifiers, and decoders are “peripheral circuits.” EX1003, 70-71. Specifically, while attempting to distinguish Takahashi’s logic circuit 105 from the claimed peripheral circuit, the applicant argued as follows:

storage cell of the reference figure can be just referred to the memory core unit of the present invention, and **row decoder, sense amplifiers/drivers, and column decoder of the reference figure can be just referred to the peripheral circuit unit 104 of the present invention.** Therefore, according to the reference figure, although paragraph [0078] of Takahashi discloses “the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201”, it is obvious that **the logic circuit 105 is not row decoder, sense amplifiers/drivers, and column decoder (shown in the reference figure) in the array-structured memory, so according to the reference figure, the logic circuit 105 of Takahashi still cannot be referred to the peripheral circuit** of the present invention.

EX1002, 72-73 (emphasis added).

Thus, by the applicant’s own definition, the circuitry of Takahashi’s driver area 204 (e.g., amplifier AMP111) and the sense amplifier area 103 (e.g., sense amplifier SA101) are each peripheral circuits. *See* EX1002, 70-74; EX1003, 72. The mapping of Takahashi to claim 1 in this ground is consistent with that understanding.

Further, these circuits are electrically connected to the DRAM core cell (memory cells). EX1003, 74. As shown in FIG. 7, the sense amplifier area 103 is electrically connected to the memory cells through, e.g., a bitline D, and the driver area 204 is electrically connected to the memory cells through, e.g., wordline WL201, sense amplifier control line SAP, sense amplifier SA101, and bitline D. EX1004, [0007], [0009], [0081], [0086], FIG. 7; EX1003, 74.



Takahashi, FIG. 7

At least a portion of the “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201” is also a peripheral circuit. EX1004, [0078]; EX1003, 75. Takahashi *explicitly* denotes it as such, and the ’017 Patent includes no definition of “peripheral circuit” that would exclude it. EX1003, 75. Although the

applicant argued against this interpretation (*see, e.g.,* EX1002, 72-74), the Examiner continued applying the “logic circuit (peripheral circuit)” as a peripheral circuit throughout prosecution, never conceding to the applicant’s position (*see, e.g.,* EX1002, 15, 62; EX1002, 40, 42). EX1003, 76.

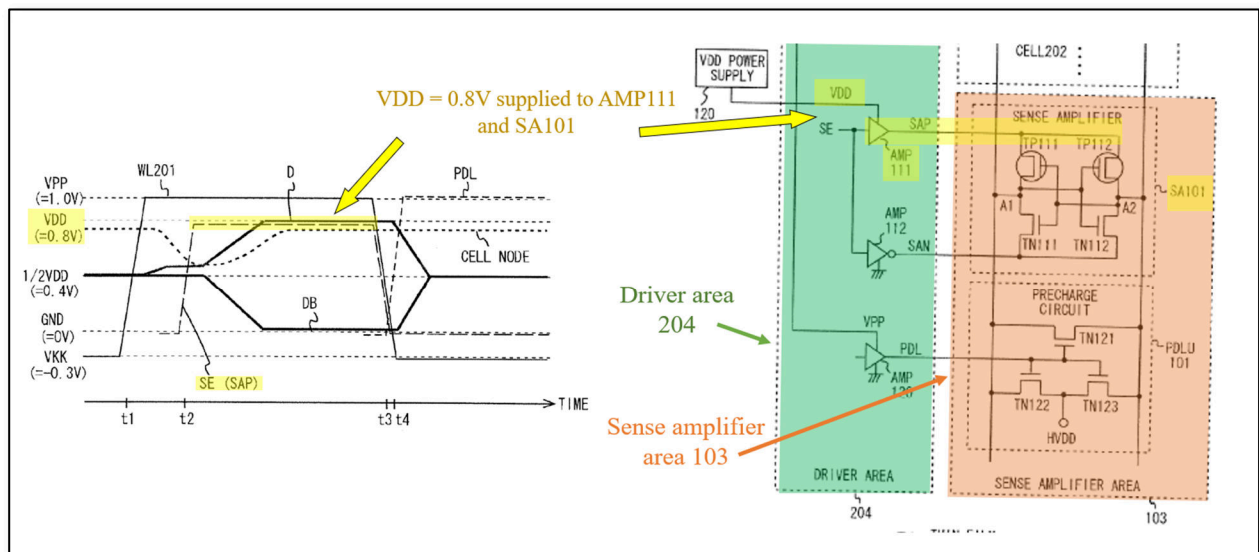
Indeed, in the block quote above, the applicant explicitly defined a “decoder” as a peripheral circuit, and Takahashi describes that the logic circuit includes “an address decoder of the semiconductor memory circuit.” EX1004, [0044], FIG. 1; EX1003, 77. As such, by the applicant’s own argument, at least a portion of the logic circuit 105 (*e.g.,* the address decoder thereof) is a peripheral circuit. EX1003, 77-78.

A POSITA would have understood that the logic circuit 105 is electrically connected to the memory cells, for example, through its “address decoder,” and though connections for obtaining “data...to be processed in the logic circuit” from the memory cells. EX1004, [0044], [0047]; EX1003, 79-80. Alternatively, a POSITA would have found it obvious to electrically connect the logic circuit 105 (*e.g.,* the address decoder) to the memory cells, so that the logic circuit 105 would be able to provide data to, and receive data from, the memory cells. EX1003, 81.

[1.7]: wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage,

Takahashi's peripheral circuits noted above (the sense amplifier area 103, the driver area 204, and the logic circuit 105) are each supplied with a **second voltage VDD**. EX1003, 86. VDD is a “power supply voltage [] of the logic circuit.” EX1004, [0045]. VDD is supplied to the sense amplifier area 103 when “the sense amplifier control signal SAP becomes equal to the power supply voltage VDD.” EX1004, [0086]; EX1003, 86. Further, VDD is supplied to the driver area 204 when “[a] power supply voltage [VDD] of the driver amplifier AMP111 is supplied from a VDD power supply 120.” EX1004, [0055]; EX1003, 86.

The supply of the second voltage VDD from VDD power supply 120 to the driver area 204, and to the sense amplifier area 103 on the sense amplifier control line SAP, is shown in Takahashi FIGS. 7 and 8, below. EX1003, 87.



Left: Takahashi, FIG. 8; Right: Takahashi, FIG. 7 (partial)

The logic circuit 105 operates at its “power supply voltage” VDD. EX1004,

[0045]; EX1003, 88-89. The sense amplifier area 103 operates at VDD when VDD is supplied to transistors TP111 and TP112 of the sense amplifier SA101 through the sense amplifier control line SAP. EX1004, [0052], [0056], [0086]; EX1003, 88. For example, the sense amplifier area 103 operates at VDD when, based on receiving the sense amplifier control signal at VDD, “[t]he sense amplifier SA101 amplifies the small potential difference between the pair of bit lines D and DB to the power supply voltage VDD and to the ground voltage GND.” EX1004, [0086]; EX1003, 88. The driver area 204 operates at VDD when the driver amplifier AMP111 receives VDD as its power supply voltage. EX1004, [0056]; EX1003, 88.

For the reasons discussed for [1.3], the recitation that the second voltage VDD be “within a second voltage range” is satisfied by any range that encompasses the claimed “second voltage...lower than 1.1V,” including the range around Takahashi’s disclosed nominal value of VDD=0.8V. EX1004, [0084]; EX1003, 90. More, and again as discussed for [1.3], the second voltage VDD is also within a small second voltage range around its nominal value of 0.8V due to expected non-idealities in voltage generation and provision. EX1003, 90.

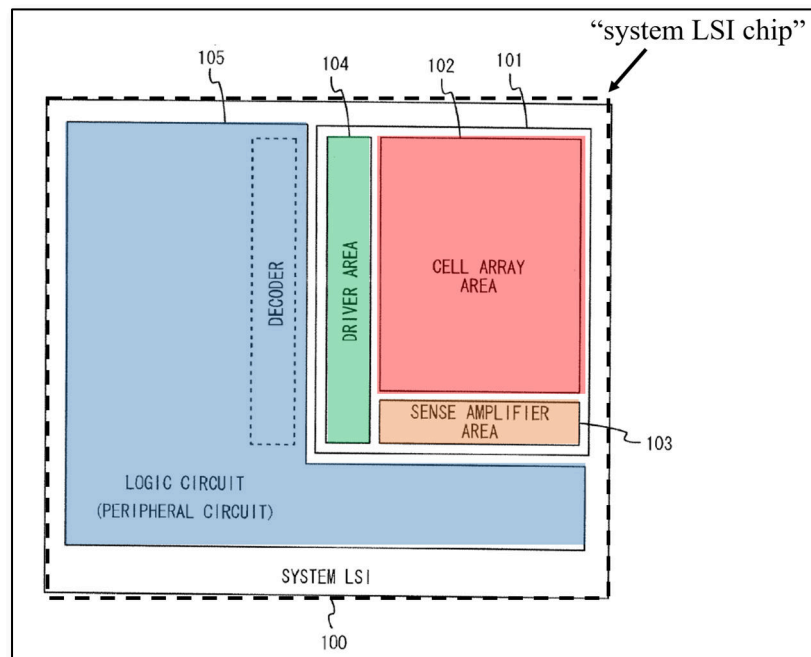
[1.8]: wherein the second voltage is lower than 1.1V, and

Takahashi’s second voltage, VDD, is 0.8 V, which is lower than 1.1 V. EX1003, 91. *See, e.g.,* Takahashi [0078] (“VDD is 0.8V or lower”), [0084] (“the

power supply voltage VDD is 0.8 V”), and FIG. 8, which shows “VDD (=0.8V).”
EX1004, [0078], [0084], FIG. 8; EX1003, 91.

*[1.9]: wherein the DRAM core cell and the peripheral circuit are formed on
a single chip,*

Takahashi describes “a system LSI chip” that includes the cell array area 102 (202 in the FIG. 7-10B embodiment), the sense amplifier area 103, the driver area 104 (204), and the logic circuit 105, thereby forming the DRAM core cell (cells of the cell array area) and the peripheral circuit (the sense amplifier area 103, the driver area 204, and/or the logic circuit 105) on a single chip. EX1004, [0043], FIG. 1; EX1003, 92.

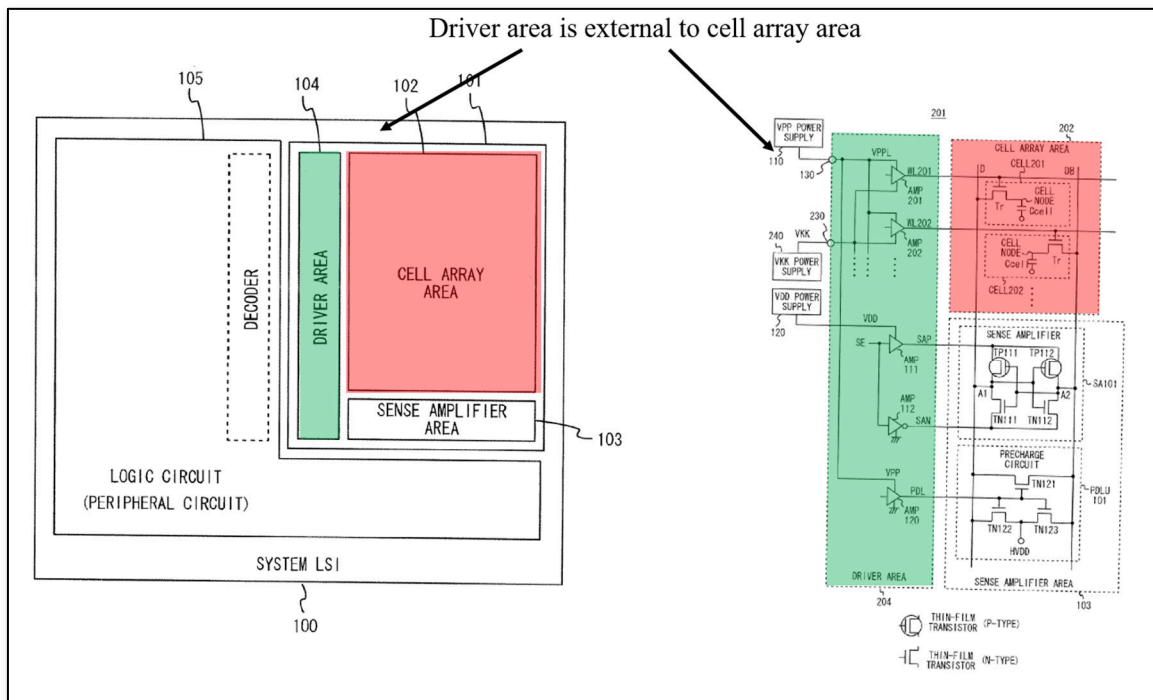


Takahashi, FIG. 1

Takahashi also describes that a “semiconductor memory circuit 1,” a prior art device similar to the semiconductor memory circuit 201, is “integrated into one chip,” and a POSITA would have understood that the semiconductor memory circuit 201 shares this same configuration. EX1004, [0005], [0018], FIG. 12; EX1003, 93. For example, the semiconductor memory circuit 1 is illustrated in FIG. 12 in a manner matching the illustrations of circuits 101, 201, suggesting matching device structures. EX1004, FIGS. 2, 7, 12; EX1003, 93. And Dr. Liu explains how Takahashi’s comparison of transistor designs between the logic circuit 105, the cell array area 202, and the sense amplifier area 103 would have informed a POSITA that these circuits were formed as an integrated circuit in a single chip. EX1004, [0014], [0044]-[0046], [0078]-[0083], FIG. 7; EX1003, 94.

[1.10]: and the peripheral circuit is external to the DRAM core cell;

Takahashi’s logic circuit 105, driver area 204, and sense amplifier area 103 are external to the cell array area 202, e.g., as shown in FIGS. 1 and 7. EX1004, FIGS. 1, 7; EX1003, 95-96.



Takahashi, FIG. 1

[1.11]: wherein the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP).

As discussed in §III.A.2, the '017 Patent describes use of its DRAM as a “frame buffer of a timing controller” of the eDP 1.3 standard. EX1001, 1:28-53, 2:49-54; EX1003, 97. The frame buffer holds static image data for presentation on a display. EX1001, 1:28-53; EX1015, 25.

A POSITA would have understood that the voltages of Takahashi’s DRAM (e.g., VPPL and VDD cited above) are “capable of making the DRAM be applied to an embedded display port (eDP),” for example, as a frame buffer. EX1003, 98.

Although the '017 Patent states that existing JEDEC “operation voltages...can not satisfy requirements (that is, the low operating power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3,” the eDP 1.3 standard includes no voltage or power consumption requirements for the frame buffer. EX1001, 3:22-27; EX1003, 99. The eDP 1.3 standard describes that the frame buffer (“RFB”) is included in the display panel. EX1014, FIG. 4-1; EX1003, 99. The RFB “stores a static image,” and the image is “display[ed] from” the RFB. EX1014, 65; EX1003, 99. The eDP 1.3 standard also describes protocols for configuring a “[s]etup time” of the RFB, indicating an RFB error, and otherwise enabling/disabling use of the RFB. EX1014, 43, 45, 48, 50, 65-77; EX1003, 99. But the eDP 1.3 standard requires no particular voltages or power consumption limits for the RFB; the '017 Patent’s description of these “requirements” is incorrect. EX1003, 99.

In view of the eDP 1.3 standard’s lack of those requirements, a POSITA would have understood that the voltages of a conventional memory, including Takahashi’s, would be “capable of making the [memory] be applied” to an eDP 1.3 frame buffer, at least because of the conventional memory’s ability to store and provide data representing a static image, consistent with the eDP 1.3 standard. EX1003, 100.

Notably, “capable of” is a very broad term—broader, for example, than “configured to” or “adapted to.” *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1349 (Fed. Cir. 2012); *In re Giannelli*, 739 F.3d 1375, 1379 (Fed. Cir. 2014). A POSITA would have recognized Takahashi’s memory, which is described as “hold[ing] data” and providing “high-speed operation,” as satisfying this relatively low bar for being applicable as a frame buffer, based on the voltages VPPL and VDD which power its operation. EX1004, [0047], [0082]; EX1003, 100.

It would also have been obvious to try applying a DRAM (e.g., Takahashi’s DRAM) as an eDP 1.3 frame buffer, because DRAM was one of a small number of memory types, along with, for example, static RAM (SRAM) and flash memory. EX1031, 381-394; EX1003, 101. A POSITA selecting a memory to use as a frame buffer would have naturally considered DRAM, such as Takahashi’s, as one of only several possibilities. EX1003, 102. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007). And, in making the obvious selection of Takahashi’s DRAM, a POSITA would have recognized that Takahashi’s voltages, which are capable of powering its data writing and reading operations, are equally “capable of making the DRAM be applied to an [eDP].” EX1003, 100.

Further, to the extent the ’017 Patent erroneously links voltages “capable of making the DRAM be applied to an embedded display port (eDP)” to those voltages being sufficiently low, then Takahashi’s first (VPPL) and second (VDD) voltages,

which satisfy the “< 1.1 V” condition of the ’017 Patent, would be equally as capable of making the DRAM be applied to an eDP as the ’017 Patent’s voltages. EX1001, 4:62-5:10, Table III; EX1003, 103. That is, if (as implied by the ’017 Patent) voltages <1.1V are capable of making a DRAM be applied to an eDP, then Takahashi necessarily satisfies [1.11], because Takahashi’s voltages are <1.1V. EX1003, 103.

(b) Claim 2

*[2.1]: The dynamic random access memory of claim 1, further comprising:
an input/output unit electrically connected to the peripheral circuit and the DRAM
core cell*

In addressing claim 1 above, consistent with applicant’s statements during prosecution, Takahashi’s driver area 204 is applied as a peripheral circuit. EX1003, 104. As Dr. Liu explains, however, in the context of embedded DRAMs like Takahashi’s, a POSITA would have also understood that the driver area 204 constitutes an input/output unit. EX1003, 107.

This is because, in an embedded DRAM which may lack off-chip I/O circuitry, the driver area 204 performs the function of receiving external inputs used to write to and read from the memory cell array. EX1003, 108-110. For example, to perform a data readout operation, the amplifier 111 of the driver area 204 receives, as input from outside the semiconductor memory circuit 201, a “control signal SE”

that causes voltage amplification and data output. EX1004, [0084]-[0086], FIGS. 7-8; EX1003, 111. Thus, the driver area 204 performs the function of receiving external inputs and translating those inputs into internal signals of the semiconductor memory circuit 201—that is, it performs the function of an input/output unit. EX1003, 111.

The driver area 204 thus performs the claimed input/output function and, as shown in FIG. 7, Takahashi discloses a level of structural detail exceeding that of the input/output unit 106 of the '017 Patent. EX1004, FIG. 7; EX1001, FIGURE; EX1003, 111.

Thus, in the context of an embedded DRAM like Takahashi's, the driver area 204 would be understood by a POSITA as a peripheral circuit *or* as an input/output unit. EX1003, 112. Consistent with this understanding, in addressing claim 2 in this ground, Petitioner provides an alternative approach that applies the driver area 204 as an input/output unit. EX1003, 112. Both this understanding and the understanding of the driver area 204 as a peripheral circuit are consistent with the understanding of a POSITA. EX1003, 112.

As discussed for [1.6] in §V.A.2(a), and as illustrated in FIG. 7, the driver area 204 is electrically connected to the memory cells and the peripheral circuit (e.g., the sense amplifier SA101) through, e.g., wordline WL201, sense amplifier control

lines SAN, SAP, precharge control line PDL, sense amplifier SA101, and/or bitline D. EX1004, [0007], [0009], [0081], [0086], FIG. 7; EX1003, 113-114.

[2.2]: for operating in a third voltage,

As discussed for [1.7] in §V.A.2(a), the driver area 204 (here applied as the input/output unit) operates in (or at/with) a voltage VDD. EX1004, [0055], FIG. 7; EX1003, 115-116. The **voltage VDD is a third voltage**. EX1003, 115. For example, VDD is supplied to the driver area 204 when “[a] power supply voltage [VDD] of the driver amplifier AMP111 is supplied from a VDD power supply 120,” and the driver amplifier AMP111 of the driver area 204 correspondingly operates at VDD. EX1004, [0055]; EX1003, 115-117.

[2.3]: wherein the third voltage is lower than 1.1V.

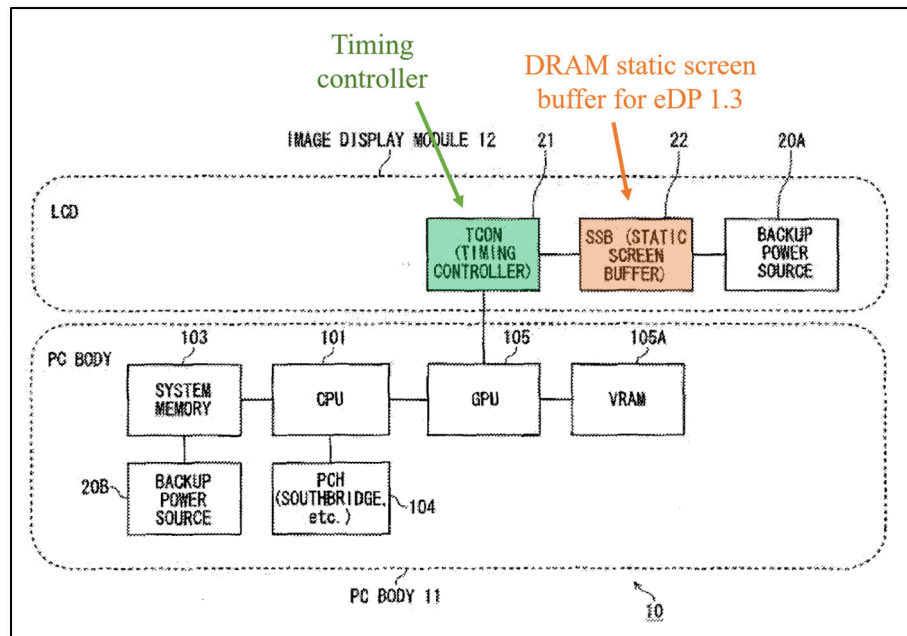
As discussed for [1.8] in §V.A.2(a), Takahashi’s third voltage, VDD, is 0.8 V, which is lower than 1.1 V. EX1004, [0078], [0084], FIG. 8; EX1003, 118.

B. GROUND 1B: Takahashi and Endo render obvious claims 1-2

1. Endo

Endo is directed to electronic devices with displays, such as laptops and phones. EX1007, [0020]-[0022], FIG. 1; EX1003, 119. Implementations described by Endo include FIG. 3, which illustrates an electronic apparatus 10 that includes an image display module 12. EX1007, [0023], FIG. 3; EX1003, 120. The image display module 12 includes a timing controller (TCON) and a static screen buffer (SSB).

EX1007, [0029], FIG. 3; EX1003, 120. Endo describes that the “static screen buffer (SSB) 22 is a memory defined as Embedded DisplayPort (eDP) version 1.3” and that the “SSB 22 is constituted by, for example, dynamic random access memory (DRAMs).” EX1007, [0034]-[0035]; EX1003, 120. A POSITA would have understood that this “static screen buffer” is the same as the “remote frame buffer” of the eDP 1.3 standard and the “frame buffer” of the ’017 Patent. EX1003, 120.



Endo, FIG. 3

2. Claims 1-2

As discussed in §V.A.2, Takahashi anticipates, or at least renders obvious, claims 1-2. Claim 1 is further obvious over Takahashi in view of Endo’s teachings, which further demonstrate that it would have been obvious for the voltages of

Takahashi's DRAM to be "capable of making the DRAM be applied to an embedded display port (eDP)," as recited in claim 1. EX1003, 121.

Specifically, Endo explicitly teaches the use of "DRAMs" as the frame buffer of eDP 1.3 devices. EX1007, [0034]-[0035]; EX1003, 122. Endo also describes how an apparatus in which the frame buffer is a DRAM can be specially configured to facilitate the DRAM: the apparatus can include a backup power source 20A that maintains storage of data in the volatile DRAM, even when the device is switched to a standby power state. EX1007, [0035], [0038], FIG. 3; EX1003, 122. This would have reinforced a POSITA's expectation of success in using Takahashi's DRAM as the frame buffer. EX1003, 122.

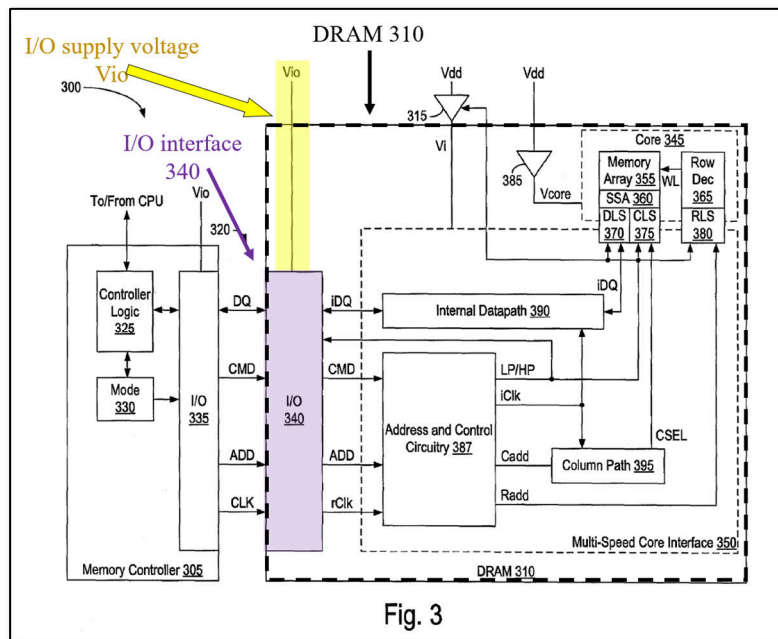
In view of Endo, a POSITA would have further found it obvious that the voltages of Takahashi's DRAM are capable of making the DRAM be applied to an eDP, would have been further motivated to apply that DRAM to an eDP to obtain the benefits of eDP operation, and would have reasonably expected success in doing so. EX1003, 123. Indeed, Endo discloses the use of a DRAM for that purpose, without disclosing any specific requirements or characteristics of the DRAM. EX1007, [0034]-[0035]; EX1003, 123. The Takahashi device is a DRAM. EX1004, [0078]; EX1003, 123. Thus, based on Endo, it would further have been obvious to a POSITA to apply Takahashi's DRAM to an eDP, e.g., as the frame buffer. EX1003, 123.

C. GROUND 1C: Takahashi, Tsern, and Schuette render obvious claims 1-2

1. Tsern

Tsern relates to DRAM having “dynamic scaling of power and performance.” EX1005, [0005]; EX1003, 124-125. Tsern discloses memories switchable between a “low-power mode” in which a “relatively low supply voltage V_i ” is supplied to a core interface, and a “high-performance mode” in which a “relatively high supply voltage V_i ” is provided. EX1005, [0018]; EX1003, 124. As noted by Tsern, “DRAM memory devices...typically include a variety of core voltages selected for optimal performance.” EX1005, [0032]; EX1003, 125.

As shown in implementations of Tsern depicted, e.g., in FIG. 3, Tsern describes a “memory system 300” including a “DRAM 310.” EX1005, [0034]; EX1003, 126. The DRAM 310 includes an “I/O [input/output] interface 340” that communicates with a memory controller. EX1005, [0037]; EX1003, 126. The I/O interface 340 “rel[ies] upon a supply voltage V_{io} ” that can be constant or scaled between different performance modes. EX1005, [0043], FIG. 3; EX1003, 126. Tsern describes that V_{io} can be “reduced in the low-power mode for increased power savings.” EX1005, [0070]; EX1003, 126.



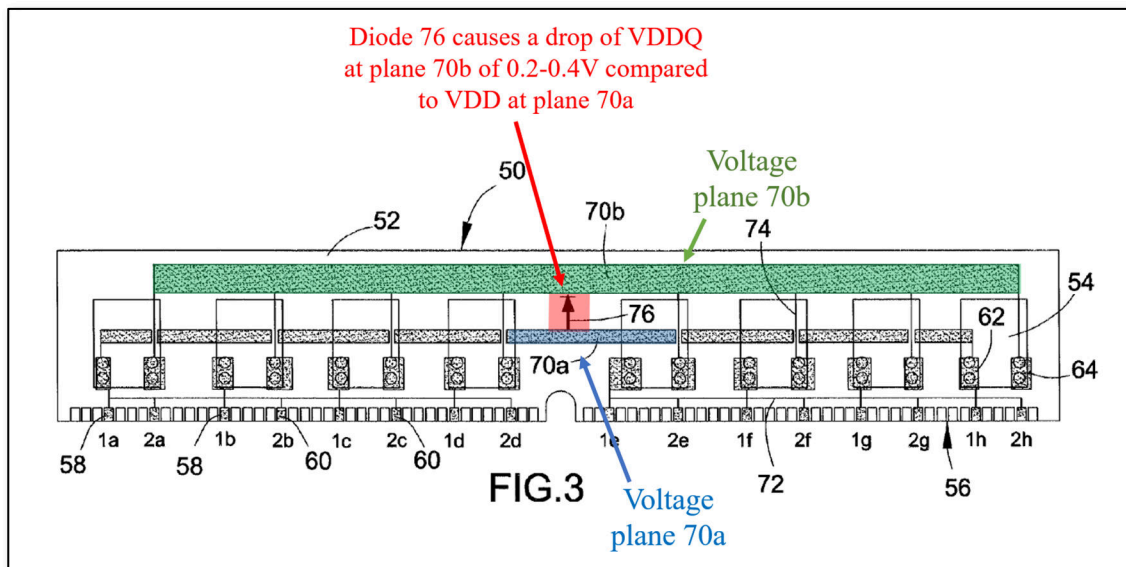
Tsern, FIG. 3

2. Schuette

Schuette describes “memory modules adapted...to generate different voltage for core supply (VDD) and input/output supply (VDDQ) inputs to memory components.” EX1006, Abstract; EX1003, 127. Schuette describes advantages (such as reliability improvement and improved memory performance) associated with separate provision of VDD and VDDQ in DRAMs. EX1006, [0005]-[0006], [0014]; EX1003, 127.

Schuette describes implementations including a memory module 50 in which “VDDQ input pins 64...are directly connected with lines 74 to the secondary voltage plane 70b, which is connected to the primary voltage plane 70a through a diode 76. With this approach, a reduction in VDDQ...is accomplished relative to the voltage

level at the VDD and VDDQ input pins.” EX1006, [0025]; EX1003, 128. Specifically, the diode 76 provides “a consistent voltage drop across all levels of load and power draw” for the I/O supply voltage VDDQ in comparison to the core supply voltage VDD. EX1006, [0021], [0029]; EX1003, 128. “[A] linear regulator circuit of a known type in the art could be employed in place of the diode 76 to achieve an equivalent reduction in VDDQ voltage.” EX1006, [0029]. “[V]oltage differentials of about 0.2 to about 0.4 volts can be achieved... depend[ing] in part on the default voltage of the memory subsystem.” EX1006, [0029]; EX1003, 128.



Schuette, FIG. 3

3. Combination of Takahashi, Tsern, and Schuette

It would have been obvious to a POSITA to modify Takahashi’s memory device in view of Tsern, to obtain a DRAM having an I/O interface supplied with a voltage V_{io} as described by Tsern. EX1003, 129. It would also have been obvious

to a POSITA to reduce Vio by 0.2-0.4 V compared to the core voltage, as taught by Schuette. EX1003, 129.

(a) Combination with Tsern

In §V.A.2(b), a POSITA would have understood that Takahashi's driver area 204 is an "input/output unit," because it serves an input/output function in the context of embedded DRAM. EX1003, 130. According to an alternative interpretation, however, the driver area 204 may be considered peripheral circuitry. EX1003, 130. For example, as discussed in §V.A.2(a), the applicant explicitly referred to "drivers" as peripheral circuitry during prosecution. EX1002, 72-73; EX1003, 130.

Thus, following the applicant's interpretation, this ground presents an alternative mapping in which the driver area 204 is considered a peripheral circuit and is not considered an input/output unit. EX1003, 131.

In the alternative mapping in which Takahashi's driver area 204 is not interpreted as an input/output unit, it would have been obvious to incorporate an input/output unit into Takahashi's semiconductor memory circuit 201, in two distinct ways and for at least two distinct reasons. EX1003, 132.

(i) **Obvious to include input/output unit for data readout from Takahashi's cell array 202 to logic circuit 105**

Takahashi relates to an “embedded” DRAM in which the memory and processors are integrated on the same chip. EX1003, 133. Correspondingly, Takahashi discloses that data stored in the cell array 202 is read out on the bit lines and utilized by the logic circuit 105. EX1004, [0060]; EX1003, 133-134. For example, Takahashi describes that the “amplifie[d] potential difference between the pair of bit lines D and DB is read out as high-level readout data...by an external circuit and is used for data processing and the like of the logic circuit 105.” EX1004, [0086].

Takahashi does not, however, describe details of the “external circuit” that reads out the data, and does not describe how data on the bit lines D and DB is transferred to “data processing” elements of the logic circuit 105. EX1003, 135. As Dr. Liu explains, “Takahashi has a ‘missing link’ [] between the bit lines and the data processing elements of the logic circuit 105: an ‘external circuit’ is used for data readout, but Takahashi provides no details on its structure.” EX1003, 135-136.

In view of Tsern's disclosure, a POSITA would have been motivated and would have found it obvious to provide Takahashi's semiconductor memory circuit 201 with an input/output unit, powered by a supply voltage Vio, as the “external circuit” that reads out data from Takahashi's bitlines and facilitates communication

with the logic circuit 105, performing a data output function with respect to Takahashi's memory. EX1003, 137-138. This is the function of Tsern's I/O interface 340, which receives "data iDQ" and transfers it out of the DRAM 310 for use. EX1003, 137. For example, Tsern describes that "[i]nternal datapath 390 then conveys the read data to I/O interface 340, and hence to controller 305 [distinct from the DRAM 310]." EX1005, [0042]; EX1003, 137. Consistent with this function, it would have been obvious to include an I/O interface (or circuit) in Takahashi, connected to Takahashi's bitlines, such that data read from Takahashi's memory cells would be "convey[ed]...to [the] I/O interface [], and hence to" the logic circuit 105 to provide output of stored data to the logic circuit 105. EX1005, [0042]; EX1003, 137. The I/O circuit would also obviously be configured to provide data input for storage in Takahashi's memory cells, consistent with the well-understood purpose and operation of bitlines and memory cells. EX1003, 137.

Dr. Liu explains that "the I/O unit incorporated into Takahashi's memory device as the 'external circuit' would obviously include, for example, input buffers, output buffers, level-shifters, and/or other circuit elements that facilitate useful transfer of data from their form in Takahashi (voltages on the pair of bitlines D and DB) to a form useful for circuit elements of the logic circuit 105." EX1004, [0086]; EX1003, 139. It would have been within the skill of a POSITA to select suitable circuit elements to perform this function with a reasonable expectation of success,

motivated by Tsern's disclosure of an I/O interface and guided by Tsern's disclosure that the I/O unit should be powered by a voltage V_{io} . EX1003, 140.⁸ For example, a POSITA would have been guided by Takahashi description that the "external circuit" "read[s] out" "the amplifie[d] potential difference between the pair of bit lines D and DB," and would correspondingly have had a reasonable expectation of success based on configuring the I/O unit to perform this function. EX1004, [0086]; EX1003, 140.

Further, a POSITA would have known that it was conventional to include I/O circuitry even in embedded DRAMs (like Takahashi's), to provide for data input and output between an embedded DRAM and processors. EX1003, 141. Dr. Liu notes, for example, the "IOBLOCK," an "interface between the [memory] arrays and the processor core" in the embedded DRAM of a 2011 IBM publication. EX1032, 2-3; EX1003, 142. An I/O unit is also illustrated in a die diagram of an embedded DRAM.

⁸Notably, the '017 Patent provides no structure for the input/output unit more specific than the "unit" of the FIGURE, and it would have been within the skill of a POSITA to select a structure for the I/O unit that, per Tsern's teachings, would have been electrically connected to Takahashi's peripheral circuits and core memory cells. EX1003, 137.

EX1033; EX1003, 143. *See also* EX1034, EX1035; EX1003, 144-145. In short, whether data was being transferred to/from a DRAM to another die or to a processor on the same die, an I/O unit of some form was conventional and necessary to facilitate the transfer. EX1003, 146. Providing Takahashi's DRAM with an I/O unit would have filled this vital function and been obvious to a POSITA. EX1003, 146.

Tsern motivates not only the inclusion of an I/O unit as the "external circuit" but also the use of a supply voltage *Vio* to power the I/O unit. EX1003, 147. Tsern describes, for example, that the I/O interface "can use [a] scaled supply voltage" *Vio*, such that *Vio* "can be reduced in the low-power mode for increased power savings." EX1005, [0043], [0070]; EX1003, 147. It would have been obvious to provide a supply voltage *Vio* to the I/O unit to achieve these power savings. Further, even in the absence of a low-power mode, a POSITA would have recognized the necessity of powering the I/O unit to allow the unit to operate. EX1003, 147.

(ii) **Obvious to add Tsern's input/output interface to Takahashi to facilitate off-chip data transfer**

As a second obvious modification of Takahashi (distinct from the first modification discussed immediately above), it would have been obvious to provide Takahashi's semiconductor memory circuit 201 with Tsern's I/O interface 340, or a substantially similar circuit, to allow Takahashi's semiconductor memory circuit 201 to receive data from, and transfer data to, off-chip elements. EX1003, 148.

A POSITA would have recognized several clear benefits from this modification. EX1003, 149. First, the addition of Tsern's I/O interface 340, or a substantially similar circuit, would have greatly expanded the versatility of Takahashi's memory, allowing it to not only exchange data with on-chip processing elements of the logic circuit 105, but also to exchange data with external devices, e.g., generic computing devices. EX1003, 149. For example, Tsern describes that the I/O interface 340 exchanges data with a memory controller 305, and that the memory controller 305 exchanges the data with a central processing unit, a configuration Tsern describes as "conventional." EX1005, [0034]-[0035], FIG. 5; EX1003, 149. Thus, while Takahashi's disclosed DRAM is limited to on-chip communication and use of the logic circuit 105's processor, the additional inclusion of Tsern's memory interface 340 would also permit off-chip communication with generic off-chip devices and processors, improving Takahashi's functionality. EX1003, 149.

Further, the inclusion of Tsern's I/O interface 340, or a substantially similar circuit, would have made Takahashi's DRAM compatible with DRAM standards, which assume the presence of an I/O unit for off-chip communication. EX1003, 150. For example, the LPDDR3 DRAM standard required an I/O data bus (e.g., "I/O pins") and supply of an I/O power supply voltage V_{DDQ} , for connecting to and powering an I/O unit of the memory. EX1013, 12-13, 83; EX1003, 150. A POSITA

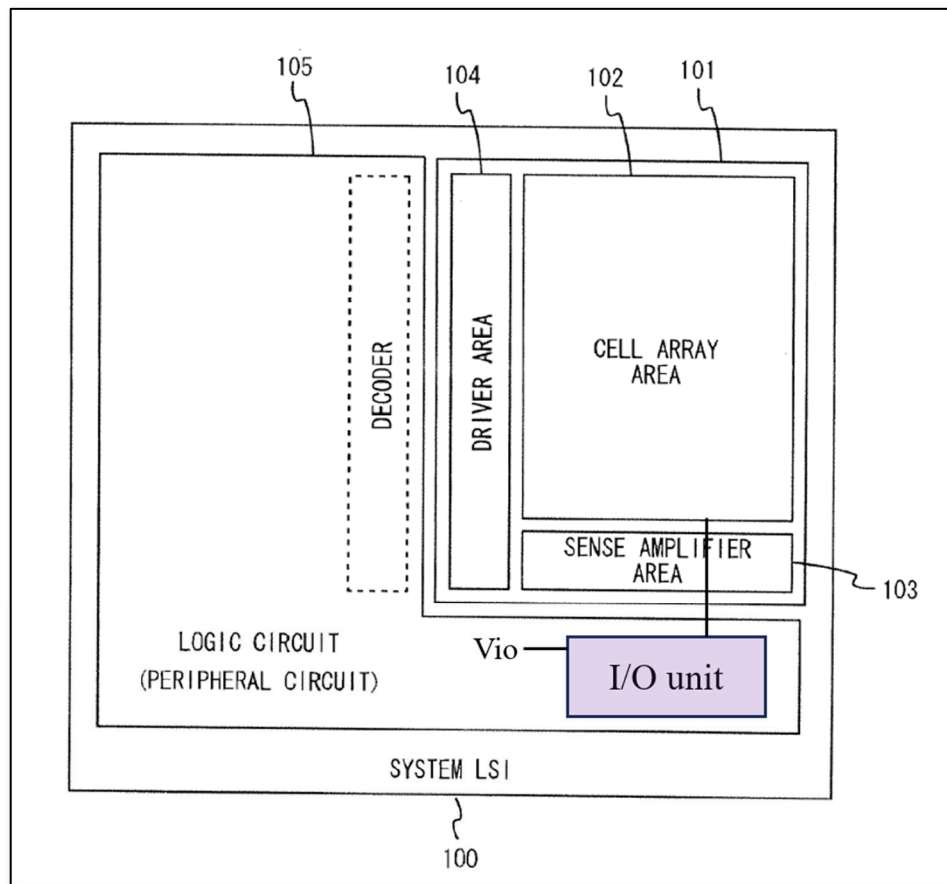
would have recognized that modifying Takahashi to conform to this and similar standards would have improved the interoperability of Takahashi's device and expanded its utility. EX1003, 150.

A POSITA would have had a reasonable expectation of success in making this modification. EX1003, 151. Takahashi's and Tsern's devices are DRAMs with similar architectures, each including, for example, a memory array, a sense amplifier circuit, precharge circuitry, drive circuitry, and address/decode circuitry. EX1004, [0044], [0048], [0051], [0079], FIGS. 1, 7; EX1005, [0020]-[0021], [0037], FIG. 3; EX1003, 151. And both Takahashi and Tsern employ multiple different voltages that are provided to different components (e.g., VPPL, VKK, and VDD in Takahashi, and Vio, Vi, and Vcore in Tsern). EX1004, [0084], FIG. 7; EX1005, [0026], [0043], FIG. 3; EX1003, 151.

Thus, in making this modification, a POSITA would have been modifying one device to have the configuration of a substantially similar device, in an entirely conventional way. EX1003, 152. Dr. Liu explains that "I/O circuitry was standard in memory devices to permit reception and transmission of signals representing data." EX1003, 152. That is, the inclusion of I/O units in DRAM was entirely standard. EX1005, [0035]; EX1003, 152. In that regard, incorporating an I/O unit into Takahashi would have involved nothing more than the combination of known elements (DRAM memory and peripheral circuitry, and DRAM I/O circuitry) to

yield predictable results, or the application of a known technique (I/O circuitry) to a piece of prior art (Takahashi's DRAM) ready for the improvement. *KSR* at 416-417 (2007). EX1003, 152-154.

Takahashi's system LSI 100, modified to include an I/O unit, is shown below. EX1003, 155. Although the I/O unit is illustrated as part of the logic circuit 105, the I/O unit can equally be included in the semiconductor memory circuit 201 (represented as 101 in the drawing below). EX1003, 155. In the case where Takahashi is modified as discussed in §V.C.3(a)(i), the I/O unit is the "external circuit" of Takahashi, configured for communication between Takahashi's embedded DRAM cell array and on-chip processing elements of the logic circuit 105. EX1003, 155. In the case where Takahashi is modified as discussed in §V.C.3(a)(ii), the I/O unit is, or is substantially similar to, Tsern's I/O interface 340 and is configured for communication between Takahashi's DRAM and off-chip elements. EX1003, 155. In either case, it would have been obvious to provide the I/O unit with a power supply voltage V_{io} for the reasons discussed in §V.C.3(a)(i). EX1003, 155.



Takahashi-Tsern device

(b) Combination with Schuette

While Tsern discloses provision of a “supply voltage V_{io} ” to the I/O interface and describes that V_{io} is preferably “reduced...for increased power savings,” Tsern does not provide a specific value for V_{io} . EX1005, [0043], [0070]; EX1003, 156. To determine an effective value, achieve Tsern’s power savings, and maintain effective device performance, a POSITA would have been motivated and would have found it obvious to follow Schuette’s teachings and configure V_{io} to be “about 0.2 to about 0.4 volts” lower than the core voltage, which a POSITA would have

recognized as either VPPL or VDD in Takahashi. EX1004, FIGS. 7-8; EX1006, [0029]; EX1003, 156.

As discussed in §V.A.2(a) for [1.2], the “core” refers to, or at least encompasses, the cell array of a memory. EX1003, 157. In the case of Takahashi, the cell array area receives both VPPL and VDD. EX1003, 157. Accordingly, either VPPL or VDD would have been interpreted as a core voltage compared to which the I/O voltage is dropped. EX1003, 157.

For example, a POSITA would have found it obvious to use a “diode” or a “linear regulator circuit of a known type in the art” to lower Takahashi’s VPPL (=1.0V) or VDD (=0.8V) by 0.2 to 0.4 V as described by Schuette, to obtain a Vio in a range from 0.6 to 0.8 V in comparison to VPPL, or in a range from 0.4 to 0.6 in comparison to VDD. EX1004, [0084]; EX1006, [0029]; EX1003, 158.

Schuette describes that this “more precise” approach “maintain[s] a consistent voltage drop across all levels of load and power draw,” such that a POSITA would have had a reasonable expectation of success in obtaining Vio from VPPL or VDD. EX1006, [0029]; EX1003, 159. Indeed, incorporating a “diode” or a “linear regulator circuit of a known type in the art” to lower Takahashi’s VPPL or VDD by 0.2 to 0.4 V as described by Schuette would have involved nothing more than the combination of known elements to yield predictable results, or the application of a known technique to a piece of prior art ready for the improvement. *KSR* at 416-417.

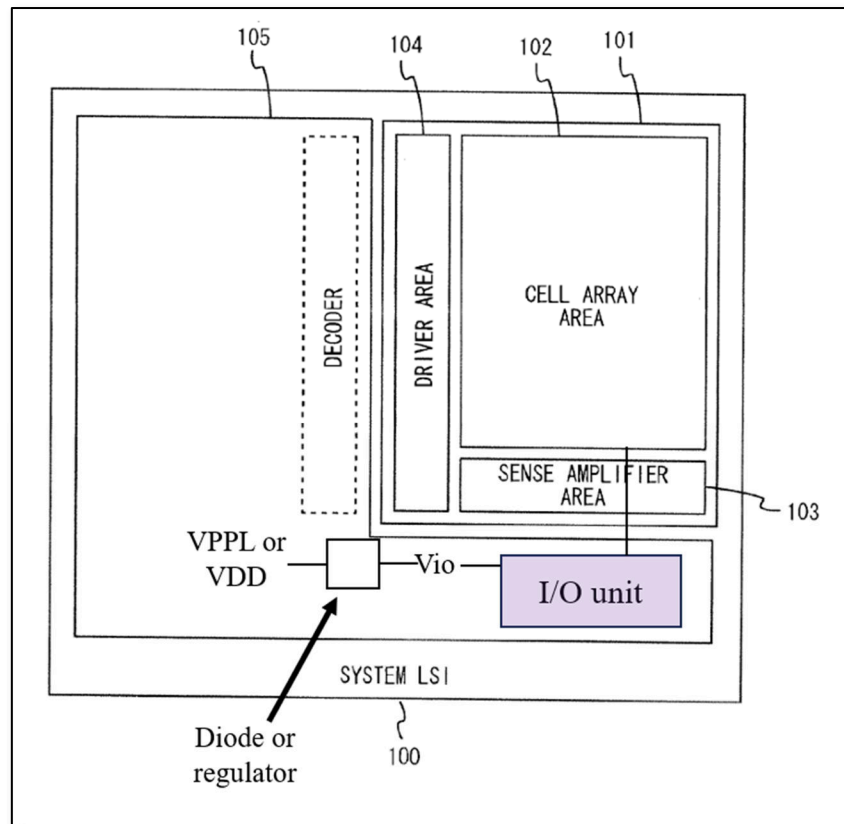
EX1003, 159. Moreover, the use of a regulator circuit to generate Vio would have been in full agreement with Tsern's existing disclosure, which describes "a collection of regulators that develops these and other necessary or desired core voltages from an externally supplied voltage Vdd." EX1005, [0032]; EX1003, 159.

Additionally, this modification would have been consistent with Takahashi's existing design, which already incorporates three power supplies providing three distinct voltages to different circuitry. EX1004, [0084]; EX1003, 160. The use of another voltage Vio to power the I/O unit, as taught by Tsern, would have constituted a minor change, especially since Schuette provides a simple and reliable circuit configuration for obtaining Vio from an existing core voltage. EX1003, 160.

Obviousness is further supported through comparison of Vio to Takahashi's VDD. EX1003, 161. Vio in a range from 0.6 to 0.8V (resulting from Schuette's disclosed voltage drop in comparison to Takahashi's VPPL=1.0V) would have resulted in a Vio matching, or similar to, Takashi's VDD=0.8, which powers Takahashi's logic circuit 105, driver area 204, and sense amplifier area 103. EX1004, [0045], FIG. 7; EX1003, 161. Thus, the modification of Takahashi based on Tsern and Schuette would have entailed providing an I/O unit with a voltage Vio matching, or close to, the voltage *already disclosed as being provided* to components of Takahashi. EX1003, 161. Indeed, one especially obvious choice for Vio would

have been $V_{io}=V_{DD}=0.8V$, in which case V_{DD} could be directly applied as the power supply voltage for the I/O unit. EX1003, 161.

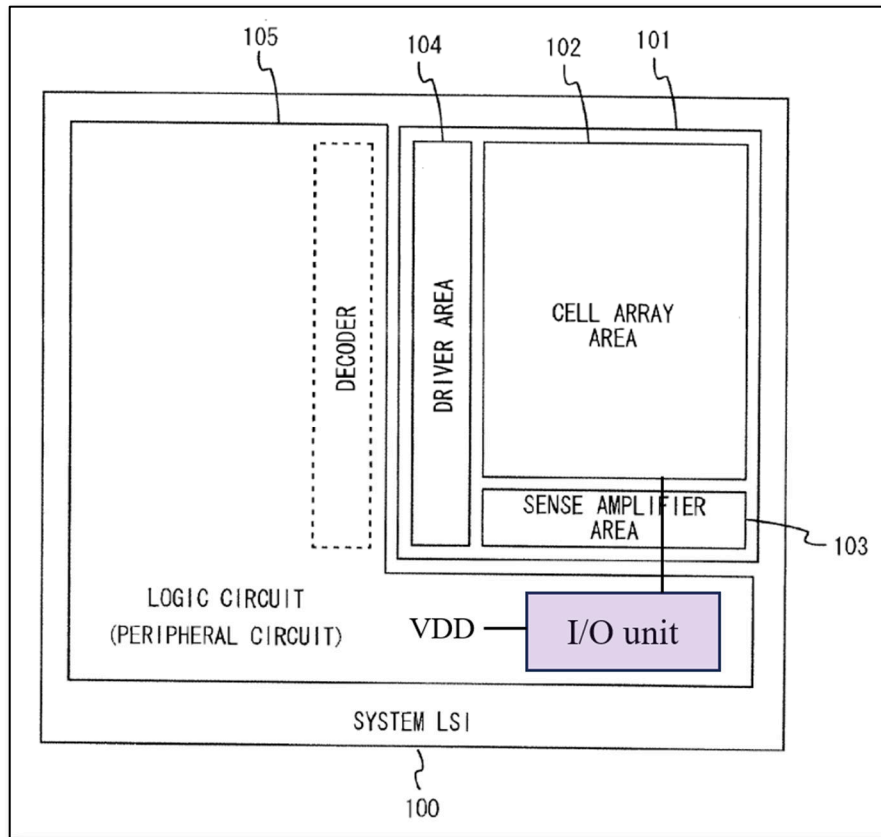
As a result of this obvious modification of Takahashi, a POSITA would have arrived at the Takahashi-Tsern-Schuette device shown below, in which $VPPL$ or V_{DD} is lowered by a diode or regulator and supplied to the I/O unit as V_{io} . EX1003, 162.



Takahashi-Tsern-Schuette device

In the specific case where V_{DD} is used as V_{io} (in accordance with Schuette's disclosure of a suitable voltage drop for an I/O circuit voltage in comparison to a

core voltage), the Takahashi-Tsern-Schuette device can be represented as shown below. EX1003, 163.



Takahashi-Tsern-Schuette device

4. Analysis of claims

(a) Claim 1

Takahashi, Tsern, and Schuette render obvious claim 1 for the reasons Takahashi anticipates and renders obvious claim 1, as discussed in §V.A.2(a). EX1003, 164.

Further, with respect to [1.11], based on the obvious inclusion of an I/O unit as discussed in §V.C.3(a)(ii), the Takahashi-Tsern-Schuette device is further

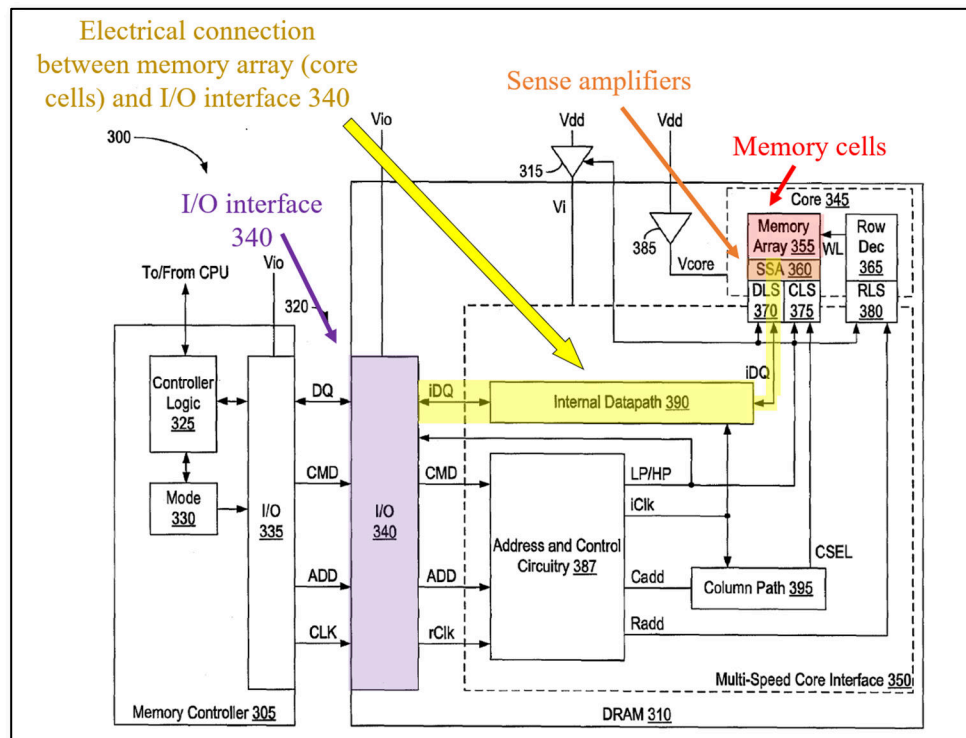
configured to receive data from and transmit data to off-chip devices, enhancing its applicability as a frame buffer in an eDP configuration. EX1003, 165.

(b) Claim 2

*[2.1]: The dynamic random access memory of claim 1, further comprising:
an input/output unit electrically connected to the peripheral circuit and the DRAM
core cell*

As discussed in §V.C.3, the Takahashi-Tsern-Schuette device includes an input/output unit, which can be configured to perform an input/output function for data exchange with the processing elements of the logic circuit 105 (§V.C.3(a)(i)) or for data exchange with an off-chip device (§V.C.3(a)(ii)). EX1003, 166.

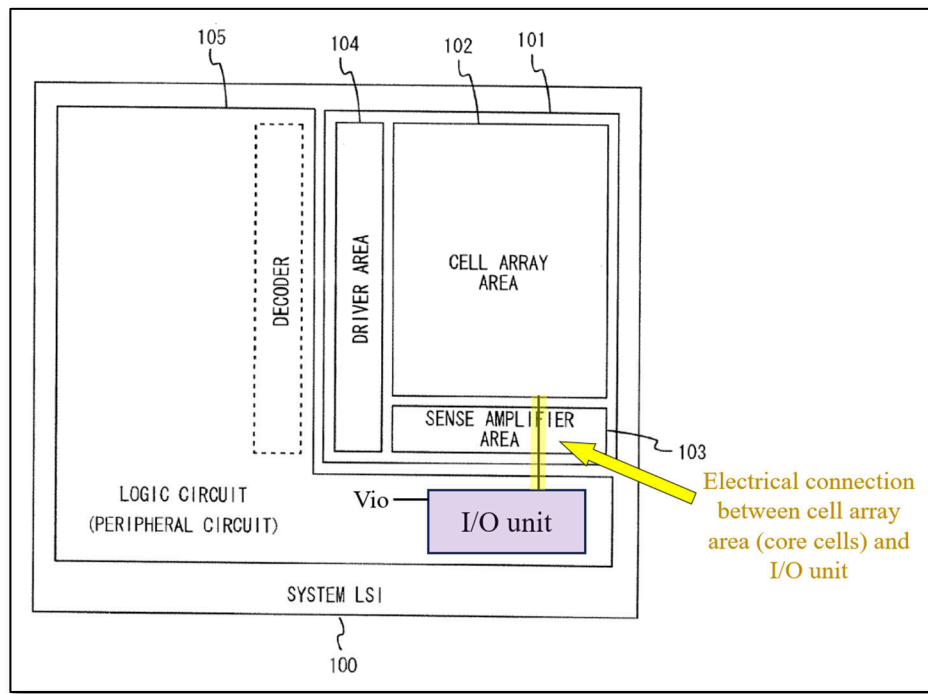
The I/O unit is electrically connected to the DRAM core cell (memory cell of the cell array area 202) so as to provide for, as Tsern describes, “the flow of signals between I/O interface 340 and memory core 345.” EX1005, [0037]; EX1003, 166. For example, Tsern describes an “[i]nternal datapath 390 [that] conveys the read data [stored in memory cells] to I/O interface 340.” EX1005, [0042]; EX1003, 166.



Tsern, FIG. 3

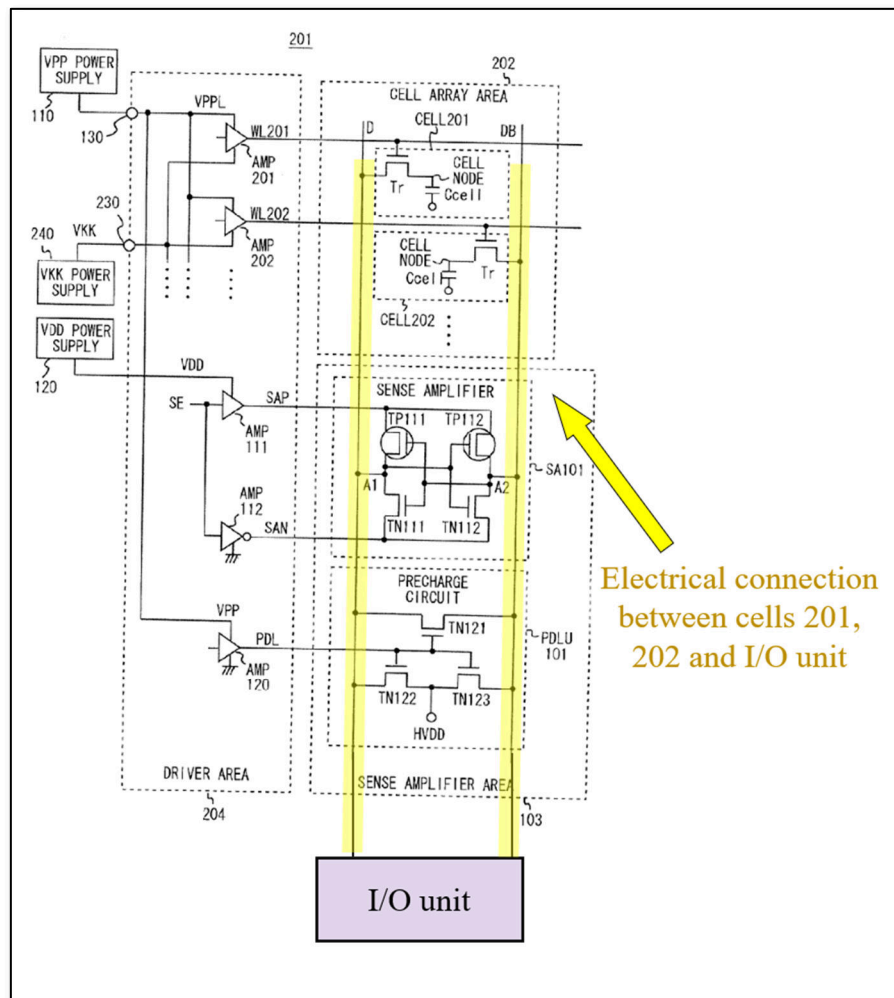
This internal datapath, which extends from the memory array 355, through sense amplifiers (SSA) 360, and to the I/O interface, is an electrical connection between the memory cells and the I/O interface. EX1003, 167.

For the Takahashi-Tsern-Schuette device, it would have been obvious for a POSITA to provide a similar electrical connection between the I/O unit and the cell array area 202 through the sense amplifier area 103, as shown below, to permit data readout/writing. EX1003, 168, 170. This configuration would have been consistent with the well-understood, standard configuration of DRAM devices, which near-universally included electrical connections from memory cells, through sense amplifiers, and to I/O circuitry to permit data readout/writing. EX1003, 168.



Takahashi-Tsern-Schuette device

For example, Takahashi describes that, in a data read process, “the amplifie[d] potential difference between the pair of bit lines D and DB is read out as high-level readout data of the semiconductor memory circuit 201 by an external circuit, and is used for data processing and the like of the logic circuit 105.” EX1004, [0086]; EX1003, 169. That is, data is output on the bitlines, and the “external circuit” reads out the data. EX1003, 169. Thus, one obvious configuration of the I/O unit would have been to electrically connect the I/O unit to the memory cells through the bitlines D and DB, as shown below:

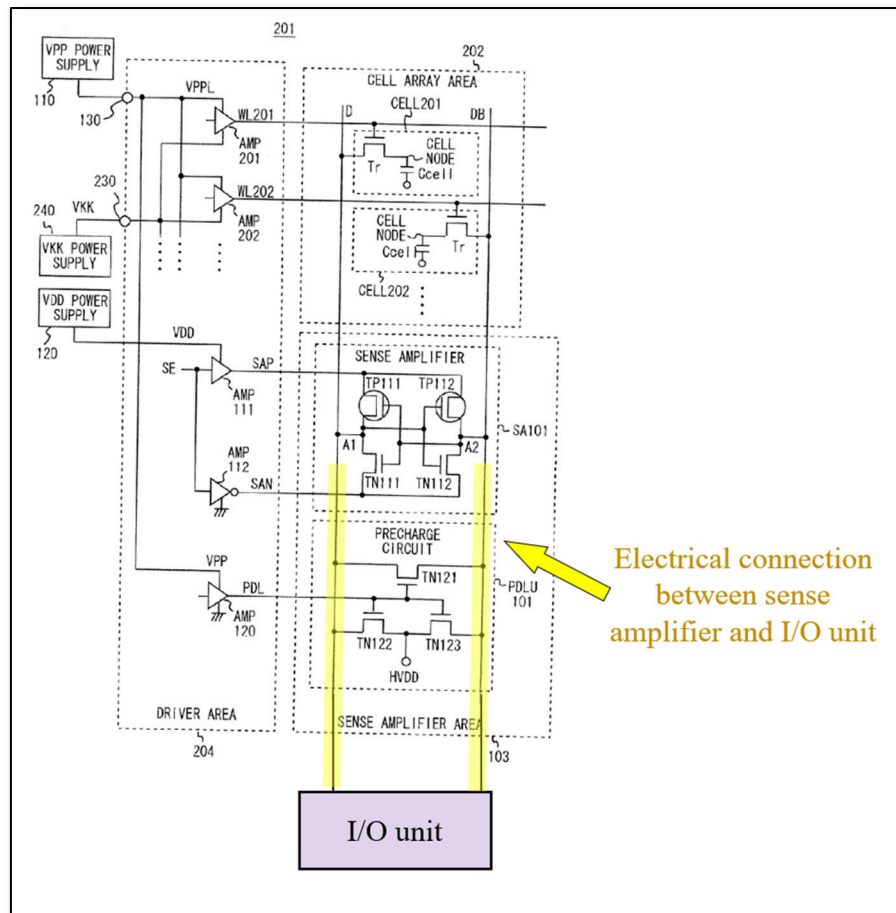


Electrical connection
between cells 201,
202 and I/O unit

Takahashi-Tsern-Schuette device

The input/output unit of the Takahashi-Tsern-Schuette device is electrically connected not only to the memory but also to the peripheral circuitry. EX1003, 171. For example, as shown in Tsern FIG. 3 above, Tsern's I/O interface 340 is electrically connected to sense amplifiers 360 through the internal datapath 390. EX1005, [0042]; EX1003, 171. A POSITA would have found it obvious to similarly configure the I/O unit of the Takahashi-Tsern-Schuette device to be electrically connected to the sense amplifier SA101 in Takahashi's sense amplifier area 103,

such that “sense amplifiers [] sense the addressed row of memory cells and present a selected column of the sensed memory-cell contents to datapath 390 [which] conveys the read data to I/O interface 340,” providing data readout. EX1004, FIG. 7; EX1005, [0042]; EX1003, 172. Indeed, in the obvious connection configuration discussed above, the I/O unit of the Takahashi-Tsern-Schuette device is electrically connected to the sense amplifier area 103 through bitlines D and DB. EX1003, 173.



Takahashi-Tsern-Schuette device

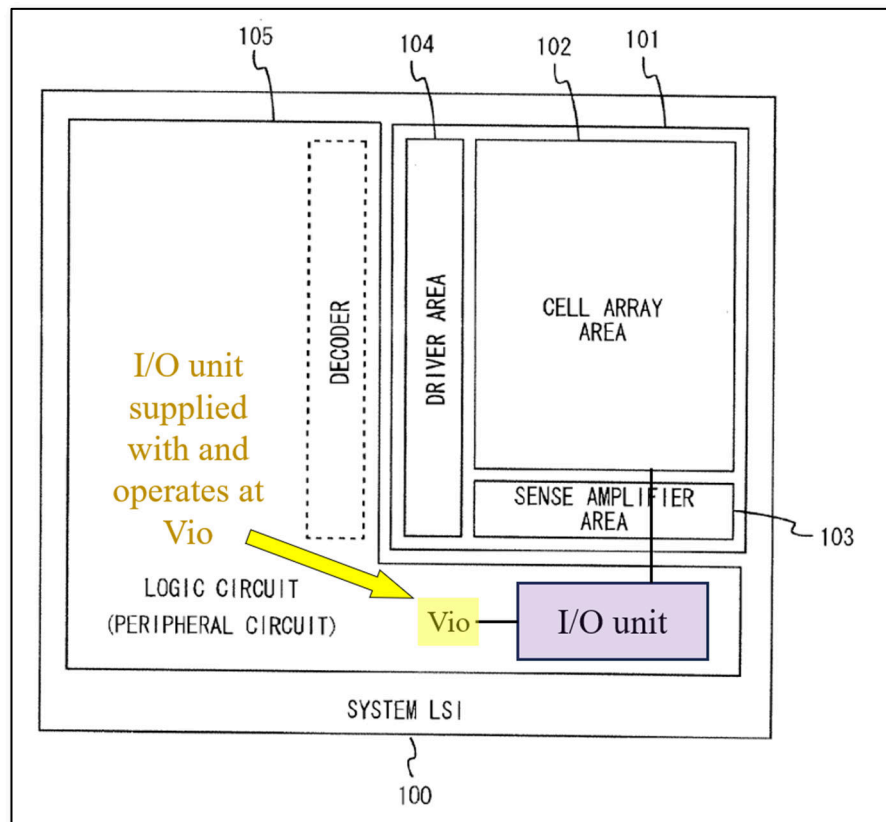
Because Takahashi's sense amplifier is a peripheral circuit (*see* [1.6] in §V.A.2(a)), this is an electrical connection between the input/output unit and the

peripheral circuit of the Takahashi-Tsern-Schuette device, as recited in claim 2. EX1003, 174.

Accordingly, the Takahashi-Tsern-Schuette device, which is a DRAM device, includes an input/output unit electrically connected to the DRAM core cell (memory cell of cell array area 202) and to the peripheral circuit. EX1003, 174-175.

[2.2]: for operating in a third voltage,

As discussed in §V.C.3, the I/O unit of the Takahashi-Tsern-Schuette device operates in (or at/with), **a third voltage Vio**. EX1005, [0043], [0070]; EX1003, 176. For example, Tsern describes that the I/O interface 340 “rel[ies] upon a supply voltage Vio.” EX1005, [0043].



Takahashi-Tsern-Schuette device

[2.3]: wherein the third voltage is lower than 1.1V.

As discussed in §V.C.3, Vio has a drop of “about 0.2 to about 0.4 volts” compared to the core voltage, which is VPPL or VDD in the Takahashi-Tsern-Schuette device. EX1006, [0029]; EX1003, 177. VPPL is 1.0 V, and VDD is 0.8V. EX1004, [0084]; EX1003, 177. Therefore, Vio is in a range from about 0.6 V to about 0.8 V, or from about 0.4 V to 0.6 V, lower than 1.1 V. EX1003, 177.

**D. GROUND 1D: Takahashi, Endo, Tsern, and Schuette
render obvious claims 1-2**

Endo is applied here as discussed for Ground 1B in §V.B.2. As discussed in §V.A.2(a), Takahashi anticipates or renders obvious that the first voltage and the second voltage are capable of making the DRAM be applied to an eDP. EX1003, 178. Endo further demonstrates that it would have been obvious for the voltages of the Takahashi-Tsern-Schuette DRAM to be capable of making the DRAM be applied to an eDP, e.g., as the frame buffer. EX1003, 178. *See* §V.B.2. EX1003, 178.

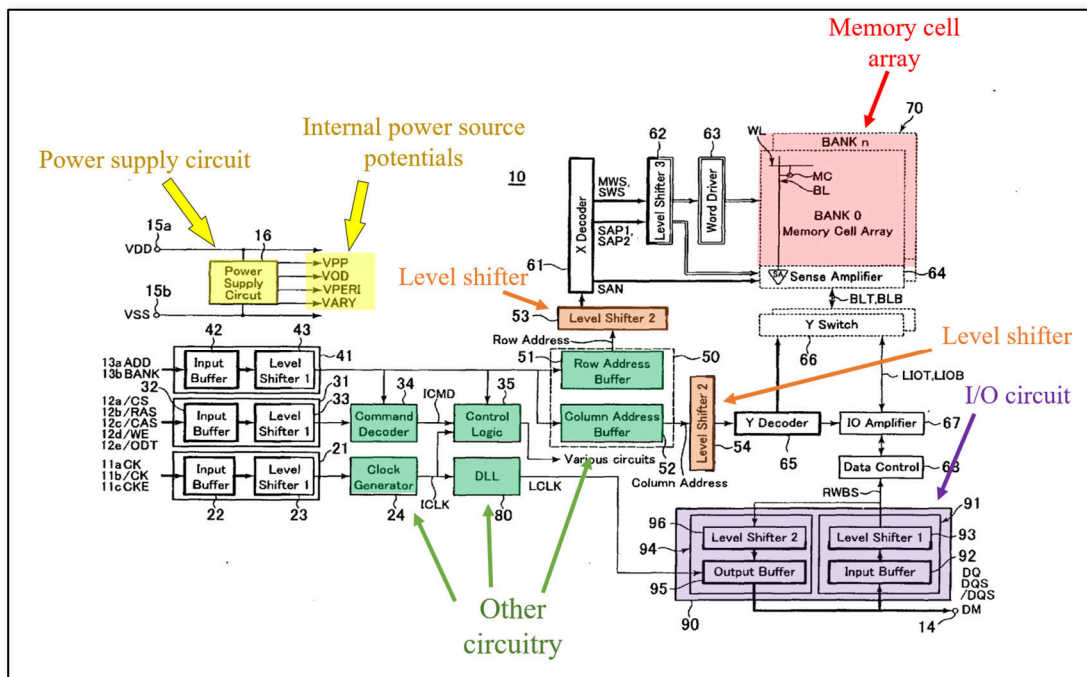
**E. GROUNDS 2A and 2A.1: Dono and Goto render obvious
claims 1-2; and Dono, Goto, and Youn render obvious
claims 1-2**

1. Dono

Dono is directed to “SDRAM” (synchronous dynamic random-access memory), a type of DRAM. EX1008, [0024]; EX1003, 179. As shown in implementations of Dono depicted, e.g., in FIG. 1, a DRAM includes elements such as a memory cell array 70, a sense circuit 64 including sense amplifiers, a data I/O circuit 90, an address controller 50, a delay-locked loop (DLL) circuit 80, and a control logic 35. EX1008, [0027], [0030], [0032], [0035], [0040], FIG. 1; EX1003, 179.

To power internal components, Dono’s DRAM receives an externally-supplied voltage VDD at a power supply circuit 16, which “generates internal power

source potentials VPP, VOD, VPERI, and VARY. These potentials have a size relationship of $VPP > VDD > VOD > VPERI \cong VARY > VSS$.” EX1008, [0042]; EX1003, 180. The outlines of circuit blocks of FIG. 1 (“thick line,” “normal line,” “double line,” and “broken line”) indicate which voltage is used (“handle[d]”) by each component. EX1008, [0043], FIG. 1; EX1003, 180. Some blocks (e.g., the first level shifters 23, 33, 43, 93) are drawn with multiple outlines to indicate that they receive multiple power supply voltages. EX1008, [0043]; EX1003, 180.



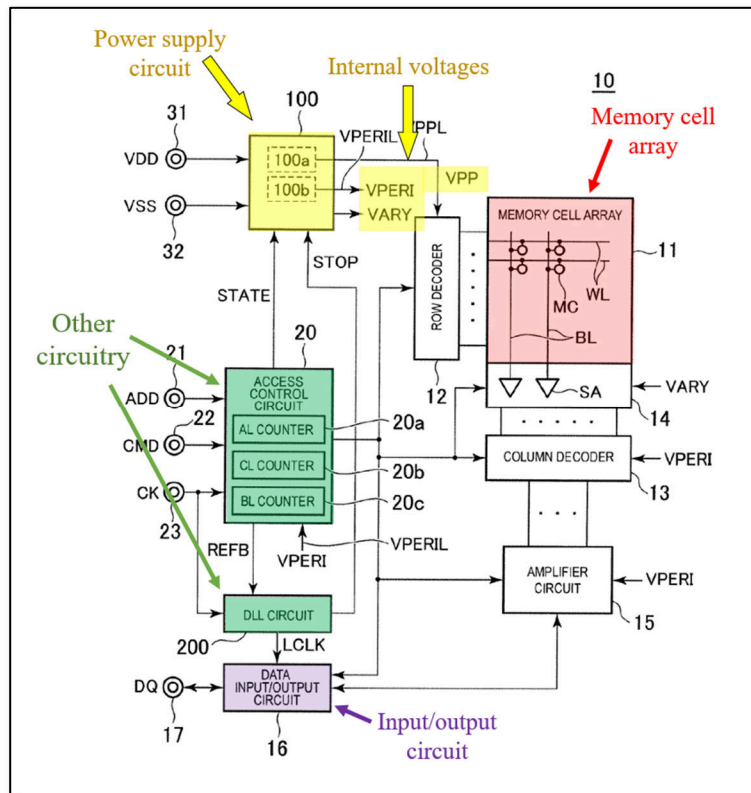
Dono, FIG. 1

2. Goto

Goto is a filing by the same applicant as Dono and, like Dono, relates to DRAM circuits. EX1009, [0022]; EX1003, 181. Implementations disclosed by Goto include, e.g., a FIG. 2 DRAM that has a structure similar to Dono’s FIG. 1 DRAM

shown above, including a memory cell array 11, a data input/output circuit 16, a DLL circuit 200, an address control circuit 20. EX1009, [0022], FIG. 2; EX1003, 181.

Also similar to Dono's circuit, Goto's DRAM includes a power supply circuit 100 that "generates internal voltages VPP, VPERI, [and] VARY." EX1009, [0026]; EX1003, 182. These voltages have the same relative relationship as in Dono: " $VPP > VDD > VPERI \approx VARY$." EX1009, [0026]; EX1003, 182.



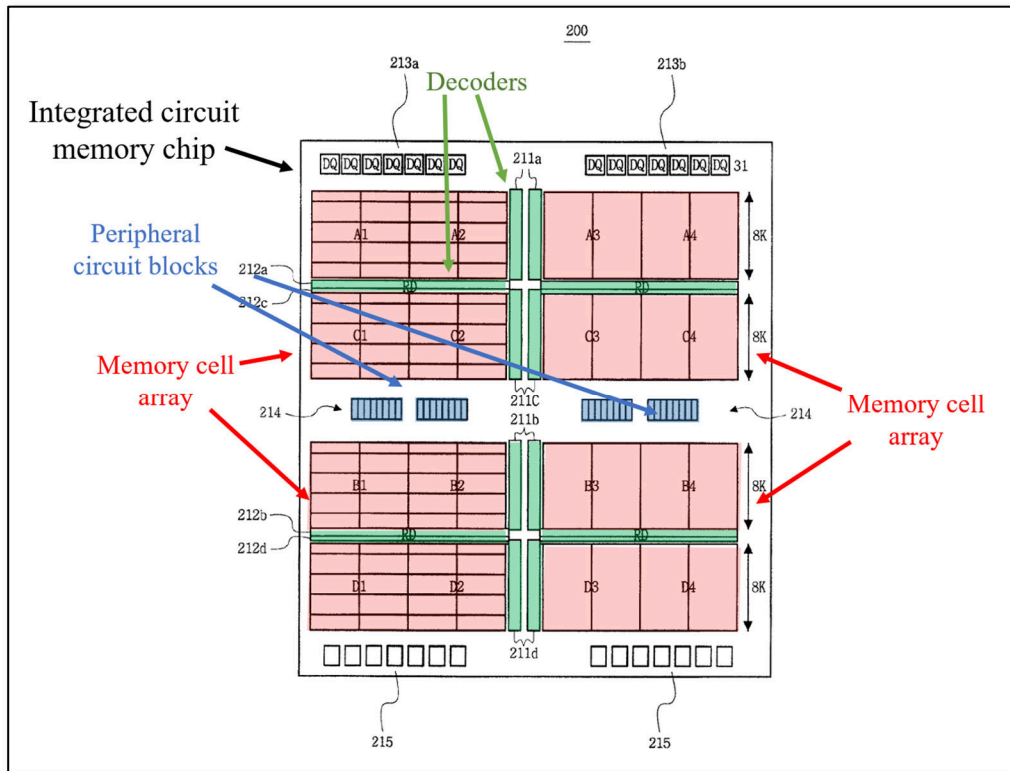
Goto, FIG. 2

3. Youn

Youn is directed to “[m]ulti-bank semiconductor memory devices...having optimized memory block layouts and data line routing to enable chip size reduction and increase operating memory access speed.” EX1010, Abstract; EX1003, 183. In addition to diagrammatic representations of memory devices, some implementations of Youn provide illustrations of physical memory chip layouts. EX1010, FIGS. 1A, 6; EX1003, 183. For example, FIG. 1A illustrates “a semiconductor memory device having a conventional hierarchical memory bank architecture” in the form of “a semiconductor integrated circuit memory chip.” EX1010, 1:48-52; EX1003, 183. The memory device can be a DRAM. EX1010, 2:26-27, 2:40-44; 5:51-59; EX1003, 183.

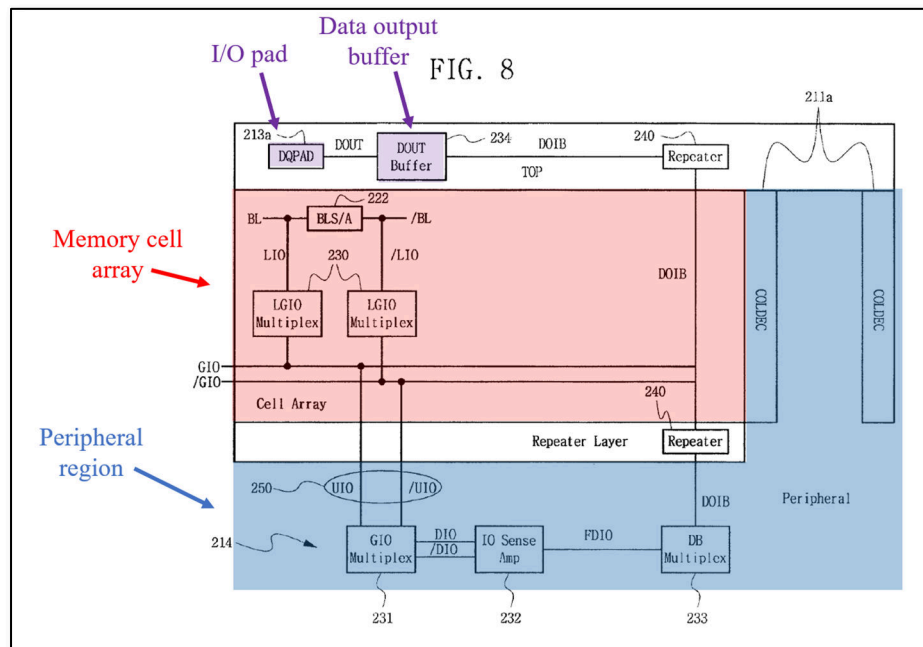
FIG. 6 “depicts an exemplary embodiment of the memory device of FIG. 1,” with a “more uniform layout” and a “shorten[ed] data path.” EX1010, 6:22-27; EX1003, 184. As shown in annotated FIG. 6 below, “a semiconductor integrated circuit memory chip (200)” includes a “memory cell array...divided into a plurality of memory banks.” EX1010, 5:59-62; EX1003, 184. The integrated circuit memory chip 200 also includes column decoders 211 and row decoders 212, along with “peripheral circuit blocks 214, and peripheral pads including I/O pads (213a, 213b) [and] control/address signal pads 215.” EX1010, 63-67; EX1003, 184. The row/column decoders are included in the peripheral circuits, and the peripheral

circuits can also include “other I/O circuitry for outputting/inputting data via peripheral data I/O pads.” EX1010, 1:57-59; EX1003, 184.



Youn, FIG. 6

FIG. 8 “illustrates an exemplary layout of the I/O circuitry and bus lines of the semiconductor device” 200 of FIG. 6. EX1010, 6:43-44; EX1003, 185. The I/O circuitry includes an “I/O pad” 213a and “DOUT [data output] buffer” 234. EX1010, 3:20, 7:1-2, FIG. 8; EX1003, 185. FIG. 8 also illustrates the memory cell array and a “peripheral region.” EX1010, 6:48-51, FIG. 8; EX1003, 182. Further illustration of I/O circuitry is provided in FIGS. 3 and 4. EX1003, 186.



Youn, FIG. 8

4. Analysis of claims

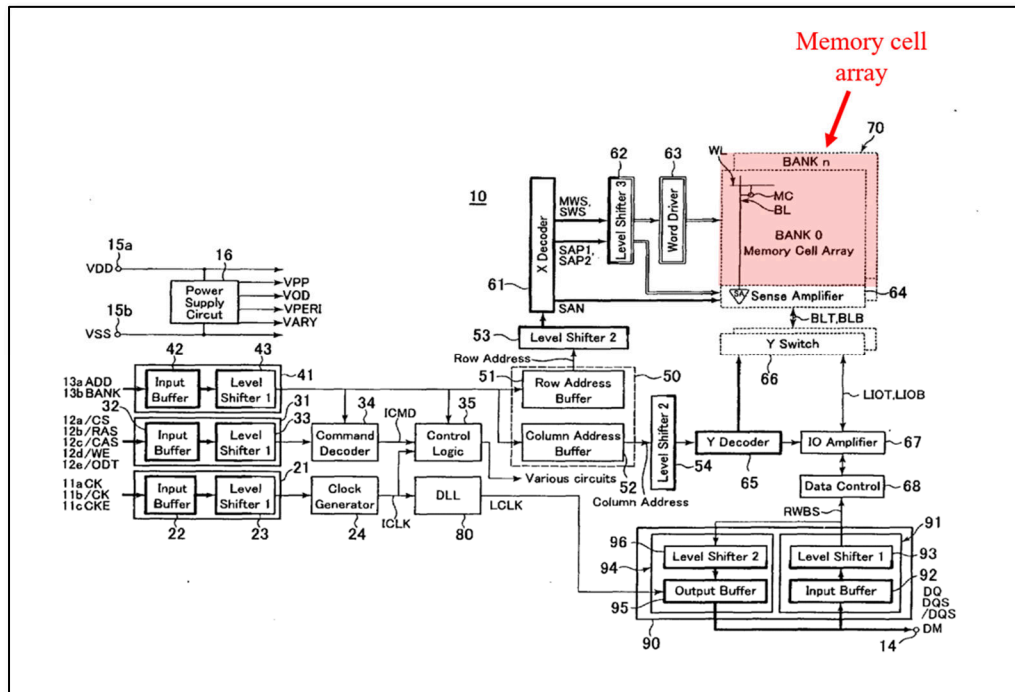
(a) Claim 1

[1.1]: A dynamic random access memory (DRAM), comprising:

Dono's "semiconductor device 10" shown in FIG. 1 "is a DDR SDRAM," i.e., a DRAM. EX1008, [0024], FIG. 1; EX1003, 187.

[1.2]: a DRAM core cell,

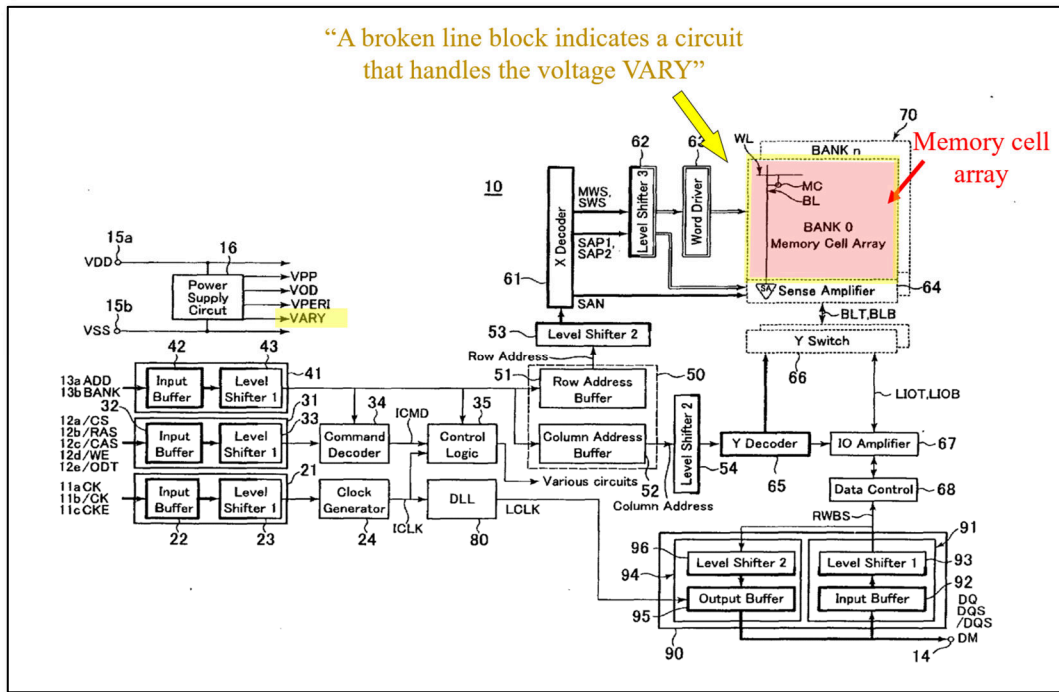
Dono's DRAM includes a "memory cell array 70 [that] includes dynamic memory cells MC arranged in a matrix." EX1008, [0037], FIG. 1; EX1003, 188. These DRAM memory cells are each a DRAM core cell. EX1003, 188. See [1.2] in §V.A.2(a) for discussion of why a POSITA would have understood a DRAM memory cell to be a "core" cell. EX1003, 188.



Dono, FIG. 1

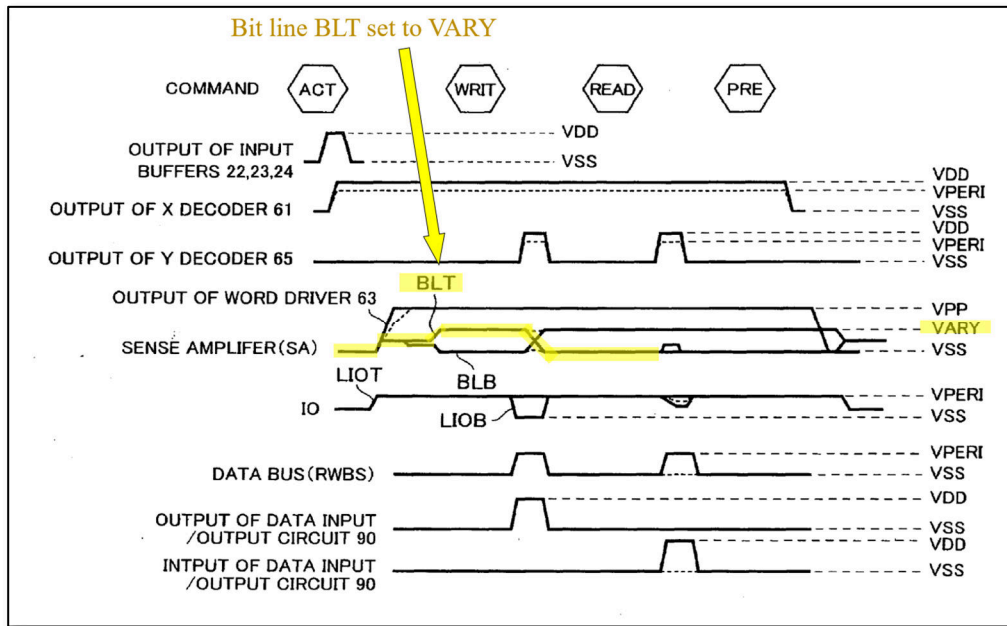
[1.3]: wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and

Dono's memory cells are supplied with, and operate at, **a first voltage VARY**. EX1003, 189, 192. Dono describes VARY as an "array-system circuit voltage," in reference to the "array" of memory cells MC, to denote that this is the voltage at which the cells of the array operate. EX1008, [0005]; EX1003, 189. The "broken line" around the memory cell array 70 in FIG. 1 also illustrates that the memory cell array is powered by VARY. EX1008, [0043], FIG. 1; EX1003, 189.



Dono, FIG. 1

FIGS. 2 and 7 illustrate operation of a memory cell at VARY in the context of “read/writing timings.” EX1008, [0078]; EX1003, 190. Based on a “write command WRIT,” a “bit line [] BLT” is driven to VARY as shown in FIG. 7, and “the data is written into the cell capacitor C1 of the memory cell MC.” EX1008, [0083]-[0084], FIG. 7; EX1003, 190. FIG. 2 illustrates the direct connection of the bit line BLT to a memory cell MC1; when the bit line BLT is set to VARY as shown in FIG. 7, VARY is set across a capacitor C1 of the memory cell MC1 to write data to the memory cell MC1. EX1008, FIG. 2; EX1003, 190. Thus, the memory cell operates at VARY. EX1003, 190.



Dono, FIG. 7

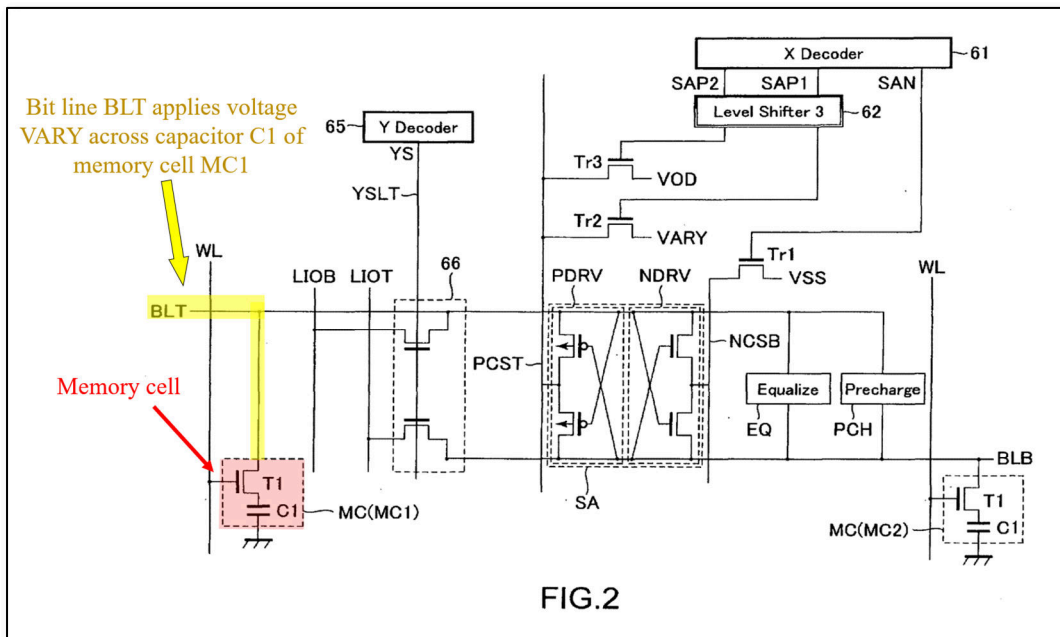


FIG.2

Dono, FIG. 2

For the reasons discussed for [1.3] in §V.A.2(a), the recitation that the first voltage VARY be “within a first voltage range” is satisfied by any arbitrary range

that encompasses the disclosed value of VARY=1.0V (discussed in further detail below). EX1008, [0005], [0049]; EX1003, 191. The first voltage VARY is also within a small first voltage range around its nominal value of 1.0V due to expected non-idealities in voltage generation and provision. EX1003, 191.

[1.4]: the DRAM core cell is a volatile memory cell,

See [1.4] at §V.A.2(a). The memory cells of Dono's DRAM are, by definition, volatile memory cells. EX1003, 193.

[1.5] wherein the first voltage is lower than 1.1V; and

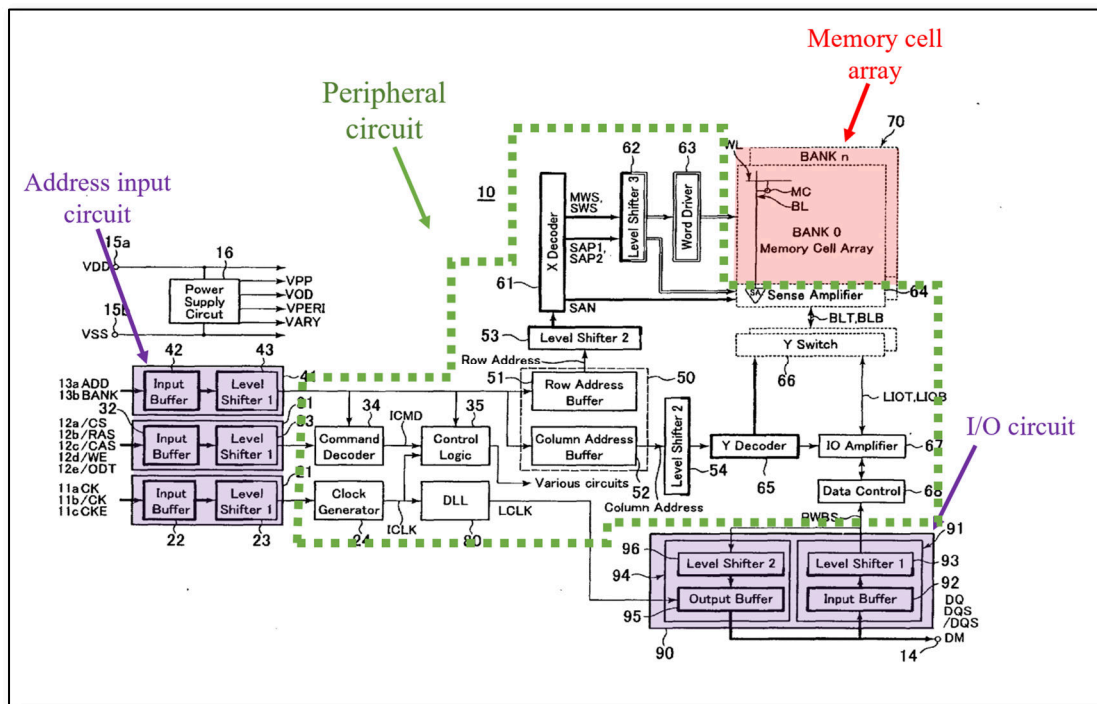
The first voltage VARY of Dono is "1.0 V," which is lower than 1.1 V. EX1008, [0005], [0049], [0105]; EX1003, 194.

[1.6] a peripheral circuit electrically connected to the DRAM core cell,

Dono discloses several peripheral circuits electrically connected to the DRAM core cell. EX1003, 195. These peripheral circuits include the command decoder 34, the control logic 35, the clock generator 24, the row address buffer 51, the column address buffer 52, the I/O amplifier 67, and/or the data control circuit 68. EX1003, 195. A POSITA would have understood that these peripheral circuits could also be collectively referred to as "a" peripheral circuit. EX1003, 195.

The textbook *VLSI Memory Chip Design* explains that "[a] memory chip is composed of three blocks[]: a memory cell array, a peripheral circuit, and an input/output (I/O) interface circuit." EX1020, 15; EX1003, 196. The peripheral

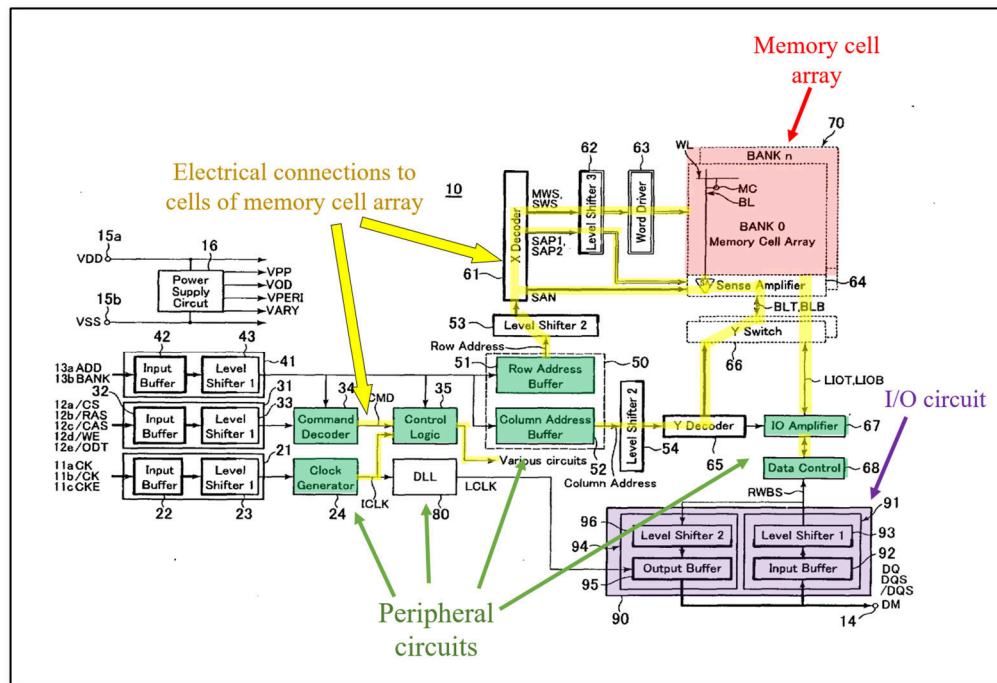
circuit “bridges between the memory array and the I/O interface circuit so that they can communicate with each other.” EX1020, 17; EX1003, 196. In Dono’s DRAM, this “bridg[ing]” peripheral circuit between the memory cell array 70 and the data I/O circuit 90/address input circuit 41 is outlined in green below. EX1003, 196.



Dono, FIG. 1

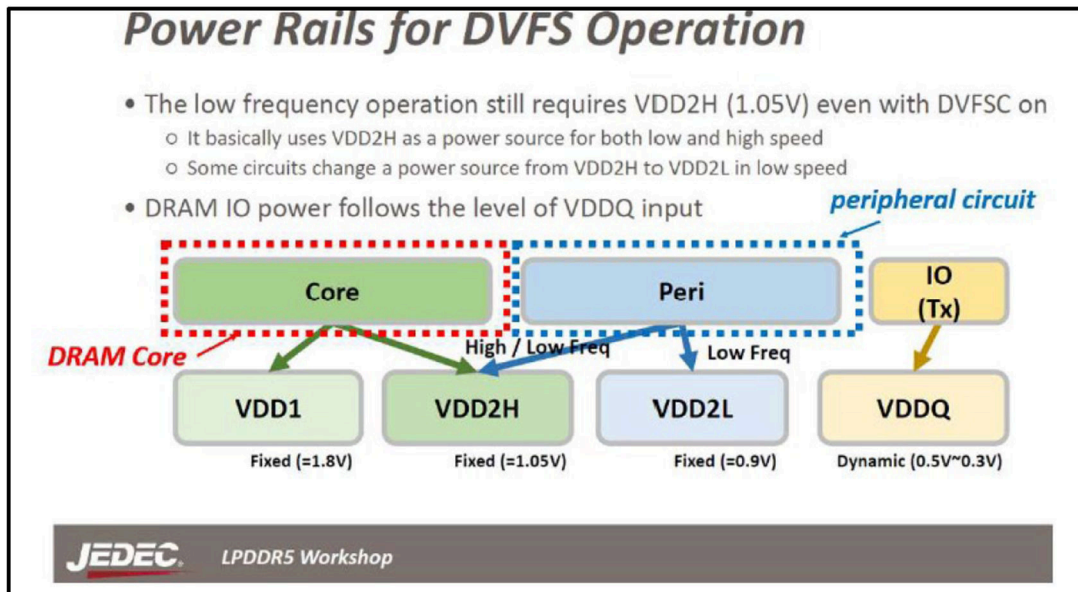
Based on this definition, Dono’s peripheral circuits include at least the command decoder 34, the control logic 35, the clock generator 24, the row address buffer 51, the column address buffer 52, the I/O amplifier 67, and the data control circuit 68. EX1003, 197. That these circuits are “peripheral” circuits is supported by the fact that each receives the “peripheral circuit voltage VPERI,” as indicated by their “normal line” outlines. EX1008, [0005], [0043]; EX1003, 197.

Each of these circuits is electrically connected to the DRAM core cells (cells of the memory cell array 70) through electrical connections illustrated below. EX1003, 198.



Dono, FIG. 1

WeCrevention's Complaint corroborates that these circuits are a "peripheral circuit [] electrically connected to the DRAM core cell." EX1021, 21; EX1003, 199. In discussing the products accused in the parallel litigation, WeCrevention provided the below annotated diagram to define "peripheral circuit." EX1021, 21; EX1003, 199. According to this diagram, DRAM elements besides the core and I/O unit—similar to the above-cited elements of Dono's DRAM—are categorized as peripheral circuits. EX1003, 199.



EX1021, 21 (annotations in original)

The WeCrevention Complaint also states that “the LPDDR5 DRAM includes buffers and other data path circuits (*i.e.*, peripheral circuits) connected to the DRAM core cell.” EX1021, 21. Most of the circuits of Dono cited above for the “peripheral circuit [] electrically connected to the DRAM core cell” either *are* buffers (the row address buffer 51 and the column address buffer 52) or are on a data path with the buffers (the command decoder 34, the control logic 35, the I/O amplifier 67, and the data control circuit 68), further indicating that they are peripheral circuits. EX1003, 200.

Thus, based both on the plain and ordinary meaning of “peripheral circuit [] electrically connected to the DRAM core cell” and on WeCrevention’s statements, Dono’s command decoder 34, control logic 35, clock generator 24, row address

buffer 51, column address buffer 52, I/O amplifier 67, and data control circuit 68 are peripheral circuits electrically connected to the DRAM core cell. EX1003, 201.

[1.7]: wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage,

Dono's command decoder 34, control logic 35, clock generator 24, row address buffer 51, column address buffer 52, I/O amplifier 67, and data control circuit 68 are each supplied with, and operate at, a **second voltage VPERI**. EX1003, 202. VPERI is the "peripheral circuit voltage." EX1008, [0005]; EX1003, 202. The "normal line" outlines of these circuits in FIG. 1 indicates that they "handle" VPERI. EX1008, [0043]; EX1003, 202. From this description, a POSITA would have understood that these circuits are supplied with VPERI. EX1003, 202. VPERI is also referred to as an "internal **operation** voltage," indicating that the circuit elements "handl[ing]" VPERI operate at VPERI. EX1008, [0007]; EX1003, 202.

Goto corroborates, and would have further made obvious to a POSITA, that the circuits described as "handl[ing]" VPERI are supplied with and operate at VPERI. EX1003, 203. Goto (which, as noted above, shares an applicant and overall DRAM structure with Dono) describes that "[t]he internal voltage **VPERI** is **supplied to most of the peripheral circuits**...The internal voltage **VPERI** is the **operating voltage** of such peripheral circuits." EX1009, [0027]; EX1003, 203. Indeed, Goto explicitly shows "VPERI" being supplied to the amplifier circuit 15,

corresponding to the I/O amplifier 67 of Dono. EX1003, 203. By reference to Goto, a POSITA would have understood that the indicated peripheral circuits of Dono operate at VPERI, and would have found it obvious to configure the peripheral circuits of Dono to operate at VPERI to ensure their correct operation. EX1003, 203.

For the reasons discussed for [1.3] in §V.A.2(a), the recitation that the second voltage VPERI be “within a second voltage range” is satisfied by any arbitrary range that encompasses the disclosed value of VPERI as equal to, or approximately, 1.0V (discussed in further detail below). EX1008, [0042], [0105]; EX1003, 204. The second voltage VPERI is also within a small second range around its nominal value of approximately 1.0V due to expected non-idealities in voltage generation and provision. EX1003, 204.

[1.8]: wherein the second voltage is lower than 1.1V, and

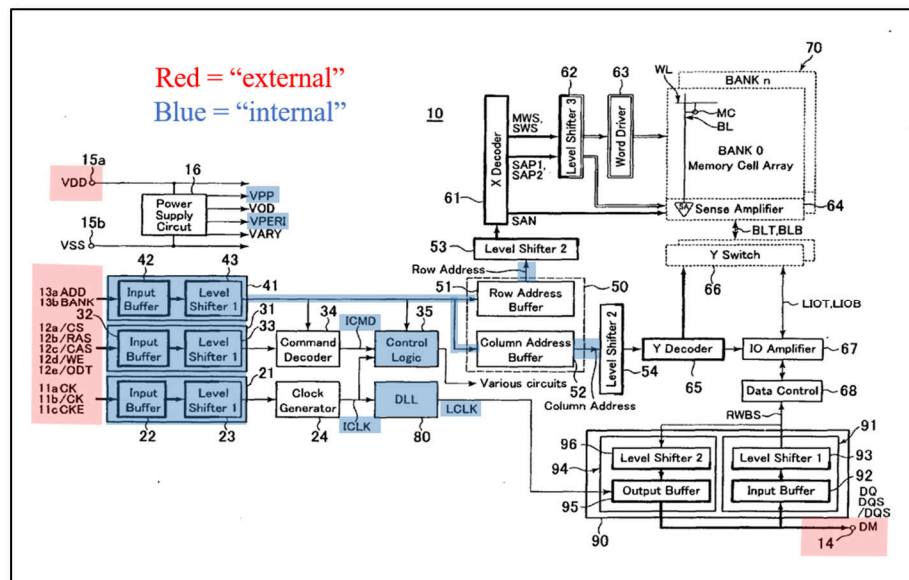
As noted above, “VARY is 1.0 V,” and Dono also describes that “VPERI $\cong$ VARY.” EX1008, [0042], [0105]; EX1003, 205. Dono also provides a specific value of VPERI as “VPERI=1.0 V.” EX1008, [0105]; EX1003, 205. Accordingly, Dono discloses that the second voltage VPERI is lower than 1.1 V. EX1003, 205.

[1.9]: wherein the DRAM core cell and the peripheral circuit are formed on a single chip,

Dono's DRAM core cells and peripheral circuits are formed on a single chip. EX1003, 206. A POSITA would have understood this for several reasons. EX1003, 206. **First**, Dono's DRAM receives a "chip select signal /CS" at a "command terminal" 12a. EX1008, [0024], [0028]; EX1003, 207. As a POSITA would have understood, the chip select signal is used to enable or disable a particular memory chip among multiple chips. EX1003, 207. For example, Micron Technology's "DDR3 SDRAM" datasheet describes that the chip select signal "enables [] and disables [] the command decoder. All commands are masked [i.e., ignored] when [the chip select signal] is registered HIGH." EX1022, 17; EX1003, 207. Correspondingly, in Dono's DRAM, the memory cell array 70 would be accessed by selecting the common single chip having both the memory cell array 70 and the peripheral circuits. EX1003, 207.

Second, Dono describes various "**external** terminals" of the "semiconductor device 10" of FIG. 1, such as terminals 11-14, in contrast to "**internal**" signals and circuits. EX1008, [0024], [0026]; EX1003, 208-209. In the annotated FIG. 1 below, elements described as "external" are highlighted in red, and elements described as "internal" are highlighted in blue. EX1003, 208. A POSITA would have understood that the "external terminals" are used for communicating with a separate chip (such as the "data processor 220" shown in FIG. 11), and that "internal" refers to signals and components on a common single chip. EX1008, [0103]; EX1003, 208. In

contrast to communication with external devices, Dono does not describe any external terminals, pins, bumps, pads, or the like for communicating between the peripheral circuits and the memory cell array 70. EX1008; EX1003, 208. As a POSITA would have understood, this is because the peripheral circuits and the memory cell array 70 are formed on a common single chip. EX1003, 208.



Dono, FIG. 1

Third, as Dr. Liu explains, DRAM circuitry—including memory cell arrays, peripheral circuitry, and I/O circuitry—was conventionally integrated in a single chip, and a POSITA would have understood that Dono’s device, lacking disclosure otherwise and conforming to conventional DRAM design, had this conventional configuration. EX1003, 210. For example, the LPDDR3 standard illustrates pad arrangements for a single DRAM chip, corresponding to a configuration (so well-understood that it did not have to be explicitly articulated) in which DRAM circuitry

would be formed as an integrated circuit in a single chip. EX1013, 6-12; EX1003, 210-211. In addition, a POSITA would have found this configuration obvious to apply to Dono's device. EX1003, 211.

Corroboration of the conventionality of forming DRAM circuitry on a single chip is provided, for example, in EX1036 (illustrating a memory cell array and peripheral circuitry, including an I/O circuit, formed in a single semiconductor substrate), EX1037 (illustrating a physical layout of a DRAM chip including a memory cell array, peripheral circuitry, and I/O circuitry), and EX1038 (describing a semiconductor substrate as having a "memory array region" and a "peripheral region" with integrated circuitry formed therein), among many other references. EX1036, 5:53-6:25, 7:34-39, FIGS. 1, 4; EX1037, 2:44-51, 6:34-8:36, FIGS. 3-4; EX1038, 2:25-31, FIG. 1; EX1039, 2:50-59, 5:63-7:3, FIGS. 1, 2A; EX1040, 1:36-37, 2:16-21, FIG. 20; EX1041, 4:41-44; EX1044, 2; EX1045, FIG. 6; EX1003, 211-212.

(i) **Ground 2A.1: In view of Youn, it would have been obvious to form Dono's semiconductor device on a single chip**

To the extent Dono and Goto alone are not considered to render obvious [1.9] (that "the DRAM core cell and the peripheral circuit are formed on a single chip"), a POSITA would in view of Youn have further found it obvious to form Dono's

semiconductor device 10—including the memory cell array and peripheral circuit—on a single chip. EX1003, 213.

Youn describes “market demands for semiconductor memory devices providing...higher integration density,” where “higher integration density” corresponds to dense integration of circuitry on a single chip. EX1010, 1:25-28; EX1003, 214. To satisfy these “market demands” while achieving high performance, Youn describes a layout of a “semiconductor integrated circuit memory chip (200)” that provides “a more uniform layout for data path lengths” and a “shorten[ed] data path, which reduces the differences in access times for read operations, for a memory device such as a [SDRAM] where timing of data signals is critical.” EX1010, 5:51-59, FIG. 6; EX1003, 214. The semiconductor integrated circuit memory chip 200 advantageously has a layout that is “capable of keeping the sensing efficiency of a data line sense amplifier uniform.” EX1010, 6:27-29; EX1003, 214.

To obtain these advantages, it would have been obvious to form Dono’s semiconductor device 10 on a single chip, e.g., conforming to the layouts illustrated by Youn, which have the memory cell array, peripheral circuit, and I/O circuit on a single chip. EX1003, 215. *See* §V.E.3. This implementation would have been obvious as the application of a known technique (DRAM circuit integration) to a piece of prior art (Dono’s DRAM device) ready for the improvement. *KSR* at 416-417. EX1003, 216.

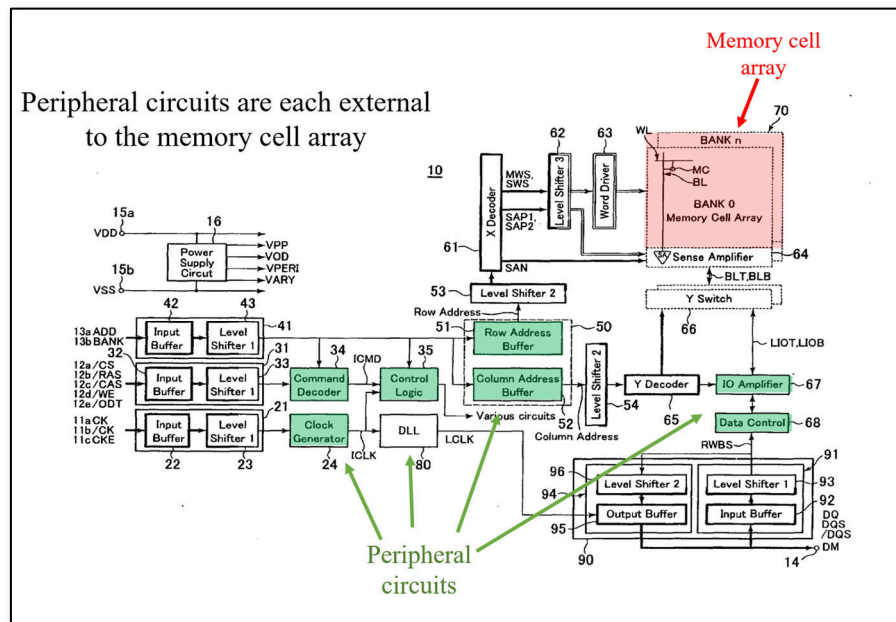
A POSITA would have had a reasonable expectation of success in forming Dono's semiconductor device 10 on a single chip. Dono's and Youn's devices are both DRAMs that include the same or similar components, including memory cell arrays, decoders, peripheral circuitry, and I/O circuitry including buffers and terminals/pads. EX1008, [0005], [0024], [0040], FIG. 1; EX1010, 3:20, 5:57-67, 7:1-2, FIGS. 6, 8; EX1003, 216. Given this similarity in DRAM architecture, a POSITA would have expected Youn's configurations to be directly applicable to Dono's device. EX1003, 216. Further, Youn discloses not merely the *goal* of integration in a single chip but also *specific physical chip layouts* for achieving effective integration, such that a POSITA would have had a clear roadmap for obtaining single-chip integration. EX1010, FIGS. 3, 6, 8; EX1003, 216. Thus, a POSITA would have had a reasonable expectation that forming Dono's semiconductor device 10 on a single chip would be successful. EX1003, 216.

Forming Dono's semiconductor device 10 on a single chip would also have been obvious for obtaining the well-known advantages of device integration common to all semiconductor integrated circuit devices, such as manufacturing efficiency, size reduction, and interconnect simplification. EX1003, 217. Youn's explicit DRAM chip layouts would have provided a POSITA with an obvious way to achieve these and other advantages of integration. EX1003, 217.

With Dono's semiconductor device 10 implemented so as to be formed on a single chip, Dono's DRAM core cell (cells of the memory cell array 70) and Dono's peripheral circuit (for example, the command decoder 34, the control logic 35, the clock generator 24, the row address buffer 51, the column address buffer 52, the I/O amplifier 67, and/or the data control circuit 68) would be formed on the single chip. EX1003, 218.

[1.10]: and the peripheral circuit is external to the DRAM core cell;

The peripheral circuits of Dono's DRAM are external to the core cells of the memory cell array 70, e.g., as shown in FIG. 1. EX1008, FIG. 1; EX1003, 219.



Dono, FIG. 1

[1.11]: wherein the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP).

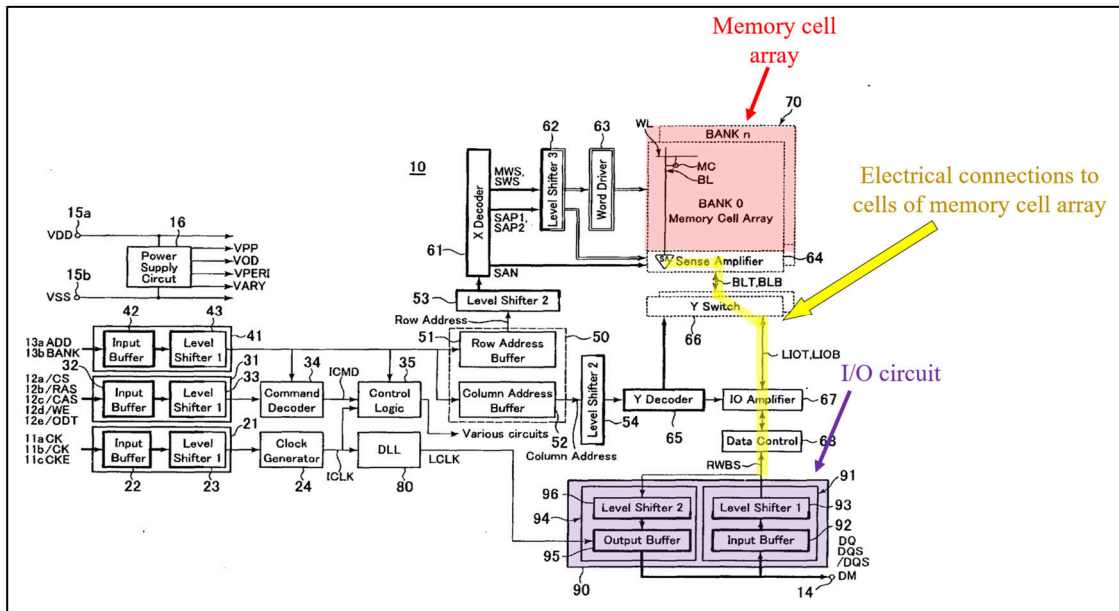
For the reasons discussed in §V.A.2(a) for Ground 1A, a POSITA would have understood that the first voltage VARY and the second voltage VPERI of Dono's DRAM are capable of making the DRAM be applied to an eDP. EX1003, 220. That is, Dono's memory is a working, conventional DRAM that, based on operation at VARY and VPERI, is capable of satisfying the requirements of the eDP 1.3 standard, which do not include any voltage or power requirements. EX1014; EX1003, 220. The eDP 1.3 standard requires that the frame buffer store and provide data representing a static image. EX1014; EX1003, 220. Dono's DRAM, which stores data, supports read and write operations, and provides "high-speed data transfer," is more than capable of fulfilling these requirements. EX1008, [0009], [0040]; EX1003, 220.

Further, to the extent the '017 Patent erroneously links "capable of making the DRAM be applied to an embedded display port (eDP)" to low-voltage operation, then Dono's DRAM, which has first (VARY) and second (VPERI) voltages that satisfy the "< 1.1 V" condition of the '017 Patent, would be equally as capable of being applied to an eDP as the '017 Patent's devices. EX1001, 4:62-5:10, Table III; EX1003, 221.

(b) Claim 2

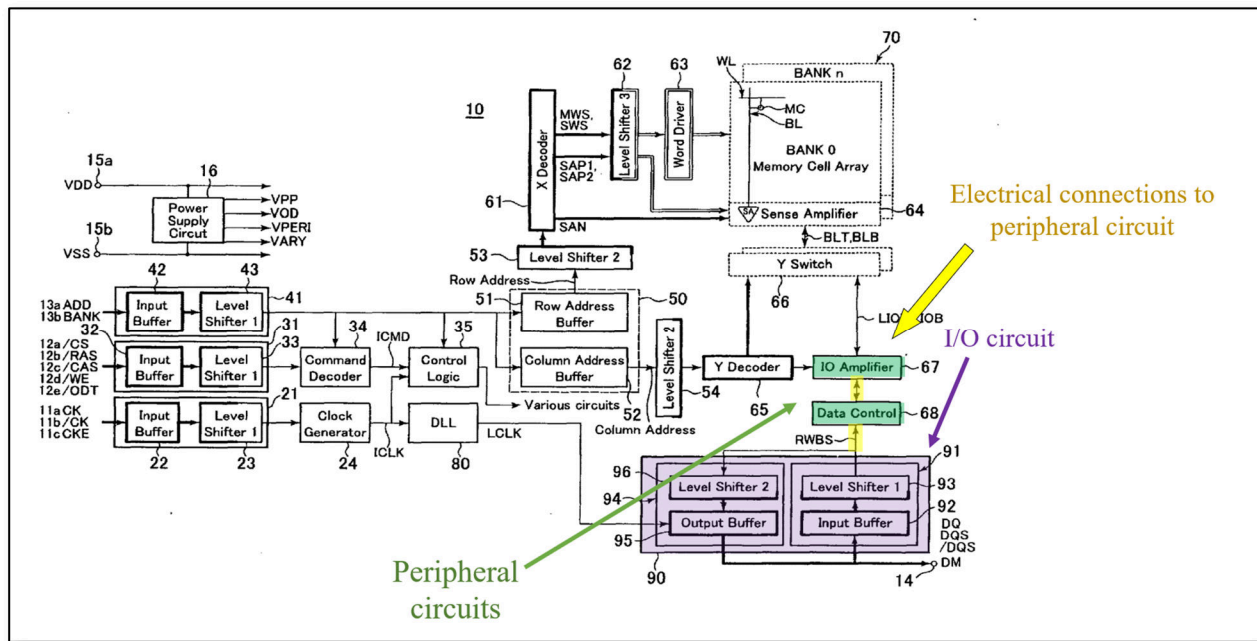
*[2.1]: The dynamic random access memory of claim 1, further comprising:
an input/output unit electrically connected to the peripheral circuit and the DRAM
core cell*

Dono's DRAM includes an "I/O circuit 90" (I/O unit) that is electrically connected both the peripheral circuitry and to the cells of the memory cell array 70 and to the peripheral circuit. EX1008, [0041], FIG. 1; EX1003, 222. For example, as shown below, the I/O circuit 90 is electrically connected to the memory cell array 70 through sense amplifier 64, I/O amplifier 67, and data control circuit 68. EX1008, [0039], FIG. 1; EX1003, 222. The I/O circuit 90 performs the claimed input/output function with respect to Dono's DRAM, and Dono discloses at least as much structure as is disclosed for the input/output unit 106 of the '017 Patent. EX1008, [0040], FIGS. 1, 7; EX1003, 222.



Dono, FIG. 1

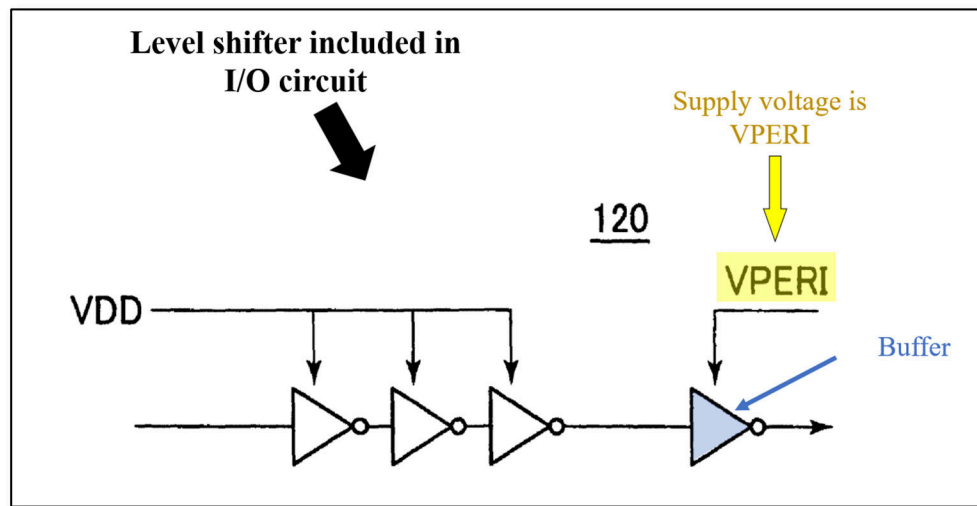
The I/O circuit 90 is also electrically connected to the peripheral circuit, e.g., to at least the I/O amplifier 67 and the data control circuit 68, as shown below. EX1003, 223.



Dono, FIG. 1

[2.2]: for operating in a third voltage,

Dono's I/O circuit 90 operates in (or at/with) the third voltage VPERI. EX1003, 224. For example, the I/O circuit 90 includes a "first level shifter 93." EX1008, [0040]; EX1003, 224. FIG. 6 illustrates a level shifter 120 that "is preferably used for the level shifter...93 shown in FIG. 1." EX1008, [0076]. **"VPERI is supplied to a power source terminal of the fourth buffer"** of the level shifter 93/120. EX1008, [0077]; EX1003, 224. As indicated by the half-"normal line" outline of the level shifter 93 in FIG. 1, the level shifter 93/120 "handle[s]" the third voltage VPERI at its "output side," in agreement with FIG. 6. EX1008, [0043]; EX1003, 224.



Dono, FIG. 6

A POSITA would have understood that the fourth buffer operates at VPERI because VPERI is its power supply voltage. EX1003, 225. As Dr. Liu explains, a POSITA would have understood that a circuit such as a buffer operates at its supply

voltage. EX1003, 225. For example, the datasheet for the Fairchild Semiconductor 74VCXH162244 buffer describes “operation” at its “1.4V to 3.6V V_{CC} supply [voltage].” EX1029, 1, 3; EX1003, 225. Similarly, the datasheet for the Texas Instruments SN74AUP1G07 buffer/driver describes its “**Operating** V_{CC} Range,” where V_{CC} is its supply voltage. EX1030, 1, 3; EX1003, 225.

Indeed, Dono describes V_{PERI} as “the internal **operation voltage**,” suggesting that circuits supplied with V_{PERI} (such as the fourth buffer and the I/O circuit 90) operate at V_{PERI} . EX1008, [0026]; EX1003, 226.

Thus, the fourth buffer of the first level shifter 93 of the I/O circuit 90 operates at V_{PERI} , meaning that the I/O circuit 90 operates in the third voltage V_{PERI} . EX1003, 227.

[2.3]: wherein the third voltage is lower than 1.1V.

As discussed for [2.2], the third voltage is V_{PERI} . EX1003, 228. V_{PERI} is equal to 1.0V or approximately 1.0V, and therefore is lower than 1.1V. EX1008, [0005], [0026], [0049], [0105]; EX1003, 228.

F. Grounds 2B and 2B.1: Dono, Goto, and Endo render obvious claims 1-2; and Dono, Goto, Endo, and Youn render obvious claims 1-2

1. Claims 1-2

Endo is applied here as discussed for Ground 1B in §V.A.2(b). As discussed in §V.E, Dono and Goto (and alternatively/additionally Dono and Goto and Youn) render obvious claims 1-2. In view of Endo's explicit disclosure of using a DRAM as the frame buffer in an eDP 1.3 device, a POSITA would have further found it obvious that Dono's DRAM is capable of being applied to an eDP, and would have been further motivated to apply that DRAM to an eDP to obtain the benefits of eDP operation, and would have reasonably expected success in doing so. EX1007, [0034]-[0035]; EX1003, 229.

VI. FEES

Petitioner authorizes the Patent and Trademark Office to charge any fees to Deposit Account No. 06-1050.

VII. MANDATORY NOTICES—37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest—37 C.F.R. § 42.8(b)(1)

Petitioner, Apple Inc. is the real party-in-interest.

B. Related Matters—37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the '017 Patent. The '017 Patent is the subject

of civil action: *WeCrevention, Inc. v. Dell Inc. et al*, 2-25-cv-01040 (EDTX) dated Oct. 10, 2025; *WeCrevention, Inc. v. Apple Inc.*, 7-25-cv-00458 (WDTX), dated Oct. 07, 2025; *WeCrevention Inc. v. Lenovo Group Limited et al*, 2-25-cv-01008 (EDTX), dated Oct. 03, 2025; *WeCrevention, Inc. v. Apple Inc.*, 2-25-cv-00951 (EDTX) dated Sep. 16, 2025.

C. Lead And Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
W. Karl Renner, Reg. No. 41,265 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR50095-0277IP1@fr.com	Andrew B. Patrick, Reg. No. 63,471 Alexander Berg, Reg. No. 79,866 Hyun Jin In, Reg. No. 70,014 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 IPR50095-0277IP1@fr.com

D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0277IP1@fr.com.

Respectfully submitted,

Dated: February 13, 2026

/W. Karl Renner/
W. Karl Renner, Reg. No. 41,265
Andrew B. Patrick, Reg. No. 63,471
Alexander Berg, Reg. No. 79,866
Hyun Jin In, Reg. No. 70,014
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

(Control No. IPR2026-00241)

Counsel for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,975 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 13, 2026

/W. Karl Renner/

W. Karl Renner, Reg. No. 41,265
Andrew B. Patrick, Reg. No. 63,471
Alexander Berg, Reg. No. 79,866
Hyun Jin In, Reg. No. 70,014
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 13, 2026, a complete and entire copy of this Petition for *Inter partes* Review, Power of Attorney, and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City 234645
TAIWAN
+886-2-8923-7350

/Crena Pacheco/
Crena Pacheco
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
pacheco@fr.com