IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

WECREVENTION, INC., Plaintiff, v. APPLE INC., Defendant.	Civil Action No. 7:25-cv-00458-ADA JURY TRIAL DEMANDED

DEFENDANT'S PRELIMINARY INVALIDITY CONTENTIONS

Exhibits

Exhibits A-00 – A-30	Motivations to Combine and Invalidity claim charts for U.S. No. 10,998,017
Exhibits B-00 – B-30	Motivations to Combine and Invalidity claim charts for U.S. No. 11,894,098
Exhibits C-00 – C-30	Motivations to Combine and Invalidity claim charts for U.S. No. 12,154,652
Exhibits D-00 – D-32	Motivations to Combine and Invalidity claim charts for U.S. No. 9,164,942
Exhibits E-00 – E-29	Motivations to Combine and Invalidity claim charts for U.S. No. 9,201,834

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I. INTRODUCTION

Pursuant to the March 5, 2025, Standing Order Governing Proceedings (OGP)—Patent Cases of the Western District of Texas (hereinafter "OGP") and the Court's Scheduling Order,[1] Defendant Apple Inc. ("Apple") provides its Preliminary Invalidity Contentions concerning U.S. Patent Nos. 10,998,017 ("the '017 Patent"), 11,894,098 ("the '098 Patent"), 12,154,652 ("the '652 Patent"), 9,164,942 ("the '942 Patent"), and 9,201,834 ("the '834 Patent") (collectively, "the Asserted Patents"). Defendant contends that each of the claims asserted by Plaintiff is invalid under one or more of 35 U.S.C. §§ 101, 102, 103, and 112.[2]

II. ASSERTED PATENT AND CLAIMS

Plaintiff served its Disclosures of Asserted Claims and Preliminary Infringement Contentions ("Infringement Contentions") on January 20, 2026. The following 32 claims remain asserted (with independent claims identified in **bold**):

Patent	Asserted Claims
10,998,017	**1,** 2
11,894,098	**1**, **2**, **3**, 4, 5, **6**, 7, 8, 9
12,154,652	**1**, **2**, **3**, 4, 5, 6
9,164,942	**1**, 5, 6, 7, 8, 9, **19**, 23, 25, 26
9,201,834	**1**, 2, 4, **21**, 23

For purposes of these contentions, Defendant only addresses those claims specifically asserted by Plaintiff. Defendant reserves the right to amend or supplement this disclosure as necessary in light of any changes or amendments made, for any reason, to WeCrevention's infringement theories, Infringement Contentions, or asserted claims.

[1] The Court's Scheduling Order is pending. *See* Dkt. 35.1 (Proposed Order on Joint MOTION for Entry of Scheduling Order Deadlines by APPLE INC).

[2] Defendants apply pre-AIA 35 U.S.C. §§ 101, 102, 103, and 112 here. However, to the extent that any other form of the patent statute (e.g., post-AIA) regarding invalidity for anticipation, obviousness, indefiniteness, non-enablement, or lack of written description applies, Defendants' Preliminary Invalidity Contentions and analysis apply just the same.

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III. RESERVATION OF RIGHTS

These Preliminary Invalidity Contentions are based on Defendant's current knowledge of the Asserted Patents and prior art, along with Defendant's understanding of Plaintiff's infringement allegations set forth in its Infringement Contentions. Defendant's investigation of the prior art is ongoing, and Defendant expressly reserves the right to supplement these Preliminary Invalidity Contentions as the case proceeds.

Nothing in these Preliminary Invalidity Contentions is intended, nor should be construed, as a waiver of any claim construction argument or non-infringement position. Defendant's statements herein (including the accompanying claim charts) reflect Defendant's present understanding of the purported potential scope of the claims that Plaintiff appears to be advocating by way of its Infringement Contentions. They are not to be seen as any acquiescence to Plaintiff's interpretation of any claims. Defendant disagrees that any such claim scope is proper. Defendant reserves the right to supplement these contentions to address any supplemental infringement contentions. For purposes of these Preliminary Invalidity Contentions, Defendant identifies prior art references and provides element-by-element claim charts based on the apparent constructions of the Asserted Claims advanced by Plaintiff in its Infringement Contentions. Nothing herein shall be interpreted as an admission that: (1) the Asserted Claims are infringed by any of Defendant's products, conduct, or instrumentalities, (2) any particular feature or aspect of any of the accused instrumentalities practices any limitation of the Asserted Claims, (3) there is 35 U.S.C. § 112 support for any limitation of the Asserted Claims, or (4) any of Plaintiff's proposed or implied constructions are supportable or proper.

Consistent with the OGP, the Court's Scheduling Order, and the Federal Rules of Civil Procedure, Defendant reserves the right to amend these Preliminary Invalidity Contentions. The

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information and documents that Defendant produces are provisional and subject to further revision as follows. Defendant expressly reserves the right to amend its disclosures and document production referenced herein should Plaintiff provide any information that it failed to provide in its Preliminary Invalidity Contentions or should Plaintiff amend its Preliminary Invalidity Contentions in any way, whether explicitly or implicitly. Further, because discovery has only recently begun and because Defendant has not yet completed its search for and analysis of relevant prior art, Defendant reserves the right to amend the information provided herein. Such amendments include, for example, identifying and relying on additional references should Defendant's further search and analysis yield additional information or references, consistent with the Patent Rules or the Federal Rules of Civil Procedure. Defendant reserves the right to supplement these contentions in light of any additional prior art of which Plaintiff is aware and later discloses to Defendant in fact discovery. Also, Defendant may issue additional subpoenas to third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed herein and/or additional prior art. These third parties include, but are not limited to, JEDEC Solid State Technology Association; NVIDIA Corporation; Texas Instruments Incorporated; Micron Technology, Inc.; Intel Corporation; Freescale Semiconductor, Inc.; HyperTransport Consortium, Inc.; Samsung Electronics Co., Ltd.; DDRdrive, LLC; Rambus, Inc.; Video Electronics Standards Association; Transmeta Corporation; Parade Technologies, Ltd.; SK hynix Inc; Winbond Electronics Corporation; the authors, employers of authors, inventors, assignees, or former or current employee of assignees, of the references identified or the Asserted Patents. Defendant reserves the right to supplement these contentions in light of any newly discovered information produced by these or other companies from which Defendant may seek discovery.

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Moreover, Defendant reserves the right to revise its ultimate contentions concerning the invalidity of the claims of the Asserted Patents based upon the Court's construction of the Asserted Claims, any findings as to the priority dates of the Asserted Claims, and/or positions that Plaintiff, Defendant, or any expert witness may take concerning claim interpretation, infringement, and/or invalidity issues. Defendant also reserves the right to revise its contentions in accordance with the Scheduling Order in the case, which specifies a later date for Final Invalidity Contentions.

Prior art not included in this disclosure, whether known or not known to Defendant, may become relevant. In particular, Defendant is currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Defendant. To the extent that such an issue arises, Defendant reserves the right to identify other references that would have made the addition of the allegedly missing limitation to the disclosed device or method obvious or show that the allegedly missing limitation would have been known or readily apparent to one of ordinary skill in the art at the time of the alleged invention in light of the disclosure of the prior art at issue.

Defendant's claim charts in Exhibits A-01 to A-30, B-01 to B-30, C-01 to C-30, D-01 to D-32, and E-01 to E-29 cite to or reference particular teachings and disclosures of the prior art as applied to features of the Asserted Claims, but persons having ordinary skill in the art generally may view an item of prior art in the context of other publications, literature, products, and understanding. As such, the cited portions are only examples, and Defendant reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation. Defendant further reserves the

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right to rely on uncited portions of the prior art references, other publications, and testimony to establish reasons for combining certain cited references that render the Asserted Claims obvious.

The references discussed in the claim charts in Exhibits A–E may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame.

Depending on the Court's construction of the claims of the Asserted Patents, and/or positions that Plaintiff, Defendant, or any expert witness may take concerning claim interpretation, infringement, and/or invalidity issues, one or more of the charted prior art references may be of greater or lesser relevance and different combinations of these references may be implicated. Given this uncertainty, the charts may reflect alternative applications of the prior art against the Asserted Claims.

Defendant's Preliminary Invalidity Contentions are based at least in part on the claimed priority dates that appear on the face of the Asserted Patents. Defendant reserves the right to challenge these dates and any different priority date that Plaintiff alleges is appropriate.

Discovery is ongoing, and Defendant reserves the right to assert invalidity under 35 U.S.C. §§ 101 and 102(a)-(g) to the extent that discovery or further investigation yield additional information forming the basis for such claims. Defendant reserves the right to assert that any Asserted Claim is invalid under 35 U.S.C. § 102(f) in the event Defendant obtains evidence that the named inventors of the Asserted Patents did not invent the subject matter claimed in the Asserted Patents. Should Defendant obtain such evidence, it will provide the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived.

Pursuant to the Court's Scheduling Order, Defendant has provided disclosures and related

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documents pertaining only to the Asserted Claims as identified by Plaintiff in its Infringement Contentions. Defendant reserves the right to modify, amend, or supplement these Preliminary Invalidity Contentions to show the invalidity of any additional claims that the Court may allow Plaintiff to later assert. Defendant further reserves the right to supplement its document production should it later find additional, responsive documents.

IV. CLAIM CONSTRUCTION

To the extent that these Preliminary Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Defendant is not proposing any such constructions as proper constructions of those terms or phrases at this time. The Court established separate deadlines for the parties' proposed claim constructions, and Defendant will disclose its proposed constructions accordingly. For purposes of these Preliminary Invalidity Contentions, Defendant may adopt alternative claim construction positions. In particular, portions of these Preliminary Invalidity Contentions, including the claim charts attached as Exhibits, may be based on the underlying claim constructions and/or interpretations as understood from Plaintiff's Infringement Contentions. Defendant, however, does not concede that Plaintiff's apparent constructions are proper, and expressly reserves the right to contest any such constructions. In addition, to the extent that these Preliminary Invalidity Contentions rely on or otherwise embody a particular order in which the steps of method claims are performed, Defendant does not necessarily propose that the method claims must be limited to such order, although Defendant reserves the right to propose such an order. Moreover, nothing disclosed herein is an admission or acknowledgement that any Accused Instrumentality, or any of Defendant's other products or services, infringes any of the Asserted Claims. Defendant reserves the right to supplement, modify, or otherwise amend these Preliminary Invalidity Contentions,

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including based on the Court's claim construction ruling and/or arguments or positions taken during the claim construction process.

Throughout the attached Exhibits, Defendant provides examples of where references disclose subject matter recited in preambles, without regard to whether the preambles are properly considered to be limitations of the Asserted Claims. Defendant reserves the right to argue, at the appropriate stage of this case, that the preambles are or are not limitations.

Moreover, Defendant reserves the right to argue that certain claim elements of the Asserted Claims do not in fact limit the scope of the Asserted Claims when determining invalidity, *e.g.*, the "process" portion of product-by-process claims. (*See, e.g., Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1369-70 (Fed. Cir. 2009)).

V. RELEVANT LEGAL PRINCIPLES

A. Lack of Written Description

The first paragraph of 35 U.S.C. § 112 requires a patent specification to contain "a written description of the invention." The written description must "reasonably convey[] to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1350 (Fed. Cir. 2010) (en banc) (citation omitted). Establishing possession as of the filing date is crucial as "[t]he purpose of the written description requirement is to prevent an applicant from later asserting that he invented that which he did not; the applicant for a patent is therefore required to 'recount his invention in such detail that his future claims can be determined to be encompassed within his original creation.'" *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003). For example, a written description is inadequate where the claim in question exceeds the scope of what the patent discloses by omitting an attribute of the described invention from the limitations, thereby over-extending the reach of the claim. *ICU Med., Inc. v. Alaris Med. Sys.,*

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Inc., 558 F.3d 1368, 1377-78 (Fed. Cir. 2009). It is also insufficient that one of ordinary skill in the art might recognize that the disclosure could be modified in light of the prior art to arrive at the claimed subject matter. *Id.* at 1378-79 (citing *Eli Lilly*, 119 F.3d at 1566-67 (explaining that "an applicant complies with the written description requirement by describing the invention, with all its claimed limitations, not that which makes it obvious.") (internal quotation marks omitted)).

B. Indefiniteness

The second paragraph of 35 U.S.C. § 112 requires the patentee to particularly point out and distinctly claim the subject matter regarded as the invention. A patent is invalid for indefiniteness if its claims, read in light of the specification of the patent, and the prosecution history, fail to inform, with reasonable certainty, those of ordinary skill in the art about the scope of the invention. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2130, 189 L. Ed. 2d 37 (2014).

VI. PRIORITY AND CONCEPTION DATES FOR THE ASSERTED CLAIMS[3]

A. U.S. Patent No. 10,998,017

In its infringement contentions, Plaintiff asserts that Claims 1 and 2 of the '017 Patent "claim priority to provisional application No. 61/672,287 (the "'287 Provisional"), filed on Jul. 17, 2012, and provisional application No. 61/768,406 (the "'406 Provisional"), filed on Feb. 23, 2013. The '017 Patent is a continuation of application No. 13/922,242, filed on Jun. 19, 2013."

To the extent Plaintiff is asserting that the priority date of Claims 1 and 2 of the '017 Patent is earlier than June 19, 2013, Defendant disputes that these claims are entitled to priority from either the '287 Provisional Application or '406 Provisional Application. The sole

[3] Notwithstanding Defendant's analysis of alleged priority for one or more Asserted Claims in this Section, Defendant reserves the right to argue that any one or more of the Asserted Claims are invalid under 35 U.S.C. § 112, as discussed in Section XI.

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independent claim, Claim 1, of the ’017 Patent claims “a DRAM core cell … supplied with a first voltage … lower than 1.1V,” “a peripheral circuit … supplied with a second voltage … lower than 1.1V,” “the DRAM core cell and the peripheral circuit are formed on a single chip,” and “the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP).”

Support for the above limitations is not found in the ’287 Provisional. The ’287 Provisional does not disclose voltages lower than 1.1V used for a DRAM core cell or peripheral circuit. (*See* ’287 Provisional at 11-15). Instead, the ’287 Provisional teaches that the “memory core power level” and the “memory peripheral power level” are at “1.8V-3.3V.” (*See* ’287 Provisional at 11-13). While draft claims 3, 7, and 11 recited that “the first voltage is between 0.9V~1.8V,” the antecedent for “the first voltage” is the “logic circuit operated under a first operation voltage” in the preambles of the respective independent draft claims, which only vaguely recited “a memory core unit … operated under a second voltage” and “a peripheral circuit unit … operated under a third voltage.” (*See* ’287 Provisional at 14-15).

The ’287 Provisional also does support the limitation that “the DRAM core cell and the peripheral circuit are formed on a single chip.” While the ’287 Provisional explains that “[i]n a conventional chipset, logic power, memory peripheral power, memory I/O power and memory core power are usually independent (separate),” there is no teaching that these components are formed on the same chip. (*See* ’287 Provisional at 11-13).

Finally, the ’287 Provisional does not support the limitation that “the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP).” The ’287 Provisional does not mention any displays, much less an embedded display, nor what voltages are capable of making the DRAM be applied to an embedded display port.

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(*See* ’287 Provisional at 11-15).

As to the ’406 Provisional, this Provisional Application does not support the limitations that “the DRAM core cell and the peripheral circuit are formed on a single chip.” The ’406 Provisional neither shows nor describes DRAM core cells and peripheral circuits on a single chip. (*See* ’406 Provisional at 11-15).

The priority date of the Asserted Claims of the ’017 patent should be no earlier than June 19, 2013, when U.S. Patent Application No. 13/922,242 was filed.

B. U.S. Patent No. 11,894,098

In its infringement contentions, Plaintiff asserts that “[e]ach of the Asserted Claims of the ’098 Patent claim priority similarly to the ’017 Patent, as the ’098 Patent is a continuation of the ’017 Patent.”

To the extent Plaintiff is asserting that the priority dates of Claims 1-9 of the ’098 Patent are earlier than June 19, 2013, Defendant disputes that these claims are entitled to priority from the ’287 Provisional Application and/or ’406 Provisional Application.

As to Claims 1 and 2 of the ’098 Patent, each recites “a DRAM core cell … supplied with a first voltage … lower than 1.1V” and “a peripheral circuit … supplied with a second voltage … lower than 1.1V.” As discussed in regard to the ’017 Patent priority above, the ’287 Provisional does not support these limitations. Moreover, Claims 1 and 2 of the ’098 further recite that “the first voltage is [different from | greater than] the second voltage.” Again, there is no support in the ’287 Provisional for this limitation. While the ’287 Provisional discloses that the “memory core power level” and the “memory peripheral power level” are at “1.8V-3.3V” (*see* ’287 Provisional at 11-13), it does not disclose that the power levels are ever “different” or that one is “greater” than the other. (*See* ’287 Provisional at 11-15).

The priority date of Claims 1 and 2 of the ’098 patent should be no earlier than February

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23, 2013, when the ’406 Provisional was filed.

As to Claim 3-5 of the ’098 Patent, independent Claim 3 recites “an input/output circuit … supplied with a third voltage … lower than 1.1V,” “a peripheral circuit … supplied with a second voltage … lower than 1.1V,” and “DRAM core cell and the input/output circuit are formed on a single chip.” Support for these limitations is not found in the ’287 Provisional.

The ’287 Provisional does not disclose voltages lower than 1.1V used for an input/output circuit or a peripheral circuit. (*See* ’287 Provisional at 11-15). While the draft claims 3, 7, and 11 recited that “the first voltage is between 0.9V~1.8V,” the antecedent for “the first voltage” is the “logic circuit operated under a first operation voltage” in the preambles of the respective independent draft claims. The draft claims recited that “a peripheral circuit unit … operated under a third voltage” and “an input and output circuit … operated under a fourth voltage.” (*See* ’287 Provisional at 14-15). The ’287 Provisional also does support the limitation that “DRAM core cell and the input/output circuit are formed on a single chip.” While the ’287 explains that “[i]n a conventional chipset, logic power, memory peripheral power, memory I/O power and memory core power are usually independent (separate),” there is no teaching that these components are formed on the same chip. (*See* ’287 Provisional at 11-13).

The ’406 Provisional also does not support the limitations that the “DRAM core cell and the input/output circuit are formed on a single chip.” The ’406 Provisional neither shows nor describes DRAM core cells and input/output circuits on a single chip. (*See* ’406 Provisional at 11-15).

The priority date of Claims 3-5 of the ’098 patent should be no earlier than June 19, 2013, when U.S. Patent Application No. 13/922,242 was filed.

As to Claims 6-9 of the ’098 Patent, independent Claim 6 recites “an input/output circuit

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… supplied with a third voltage … lower than 1.1V," "a DRAM core cell … supplied with a first voltage … greater than the third voltage," and "DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP)." Support for these limitations is not found in the '287 Provisional.

As discussed above, the '287 Provisional does not disclose voltage lower than 1.1V supplied to an input/output circuit. Nor does the '287 Provisional mention any displays, much less an embedded display, nor what voltages are capable of making the DRAM be applied to an embedded display port. (*See* '287 Provisional at 11-15). Lastly, there is no support in the '287 Provisional for supplying a greater voltage to the DRAM core cell than the input/output circuit. While the '287 Provisional discloses that the "memory core power level" and the "Memory I/O Power" are at "1.8V-3.3V" (*see* '287 Provisional at 11-13), it does not disclose that the one is "greater" than the other. (*See* '287 Provisional at 11-15).

The priority date of Claims 1 and 2 of the '098 patent should be no earlier than February 23, 2013, when the '406 Provisional was filed.

C. U.S. Patent No. 12,154,652

In its infringement contentions, Plaintiff asserts that "[e]ach of the Asserted Claims of the '652 Patent claim priority similarly to the '098 Patent, as the '652 Patent is a continuation of the '098 Patent."

To the extent Plaintiff is asserting that the priority dates of Claims 1-6 of the '652 Patent are earlier than June 19, 2013, Defendant disputes that these claims are entitled to priority from the '287 Provisional Application and/or '406 Provisional Application.

Each of independent Claims 1-3 recites "a DRAM core cell … supplied with a first voltage … lower than 1.1V," "an input/output circuit … supplied with a third voltage … lower than 1.1V," and that the "first voltage is [different from | greater than] the third voltage." For the

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reasons provided *supra* regarding Claims 6-9 of the '098 Patent, the '287 Provisional does not support these limitations. Claim 3 of the '652 Patent further recites that "the DRAM is capable to be applied to an embedded display port (eDP)." As previously discussed, the '287 Provisional does not disclose using DRAM with a display port, much less an embedded display port.

The priority date of Claims 3-6 of the '652 Patent should be no earlier than February 23, 2013, when the '406 Provisional was filed.

As to Claims 1-2 of the '652 Patent, Claims 1 and 2 further recite "wherein the DRAM core cell and the input/output circuit are formed on a single chip." The '406 Provisional does not support this limitations. The '406 Provisional neither shows nor describes DRAM core cells and input/output circuits on a single chip. (*See* '406 Provisional at 11-15).

The priority date of Claims 1-2 of the '652 Patent should be no earlier than June 19, 2013, when U.S. Patent Application No. 13/922,242 was filed.

D. U.S. Patent No. 9,164,942

In its infringement contentions, Plaintiff asserts that "[e]ach of the Asserted Claims of the '942 Patent claim priority to provisional application No. 61/546,039 [the "'039 Provisional"], filed on Oct. 11, 2011."

To the extent Plaintiff is asserting that the priority dates of Claims 1, 5-9, 19, 23, and 25-26 of the '942 Patent are earlier than October 11, 2012, Defendant disputes that these claims are entitled to priority from the '039 Provisional Application.

For example, independent Claim 1 of the '942 Patent recites "wherein the logic unit corresponds to a second MOSFET process, the second MOSFET process corresponds to a second MOSFET gate length, and the first MOSFET gate length is longer than the second MOSFET gate length." The '039 Provisional does not disclose this limitation. Accordingly, Claim 1 and asserted dependent Claims 5-9 are not entitled to the priority date of the '039

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Provisional.

As to independent Claim 19, it recites "wherein the ASIC processor executes a predetermined function corresponding to the second set of parallel data." The '039 Provisional does not disclose this limitation. Accordingly, Claim 19 and asserted dependent Claims 23 and 25-26 are not entitled to the priority date of the '039 Provisional.

The '039 Provisional also does not support additional limitations of the dependent claims. For example, Claim 6 recites "wherein the second transmission bus is a bus comprising the protocol of Universal Serial Bus (USB), a Serial Advanced Technology Attachment (SATA) bus, a Universal Flash Storage (UFS) bus, a mobile industry processor interface (MIPI) bus, or a Peripheral Component Interconnect Express (PCIE) bus." The '039 Provisional does not disclose the full scope of this limitation.

Moreover, claims directed to different transmitted and received signal properties on the same bus are not supported by the '039 Provisional. For example, Claims 7 and 23 recite "a signal swing of data transmitted through the first transmission bus and a signal swing of data received through the first transmission bus are different," Claim 8 recites "a signal swing of data transmitted through the second transmission bus and a signal swing of data received through the second transmission bus are different," Claims 9 and 25 recite "a transmitting data rate of the first transmission bus and a receiving data rate of the first transmission bus are different," and Claim 26 recites "a transmitting data rate of the second transmission bus and a receiving data rate of the second transmission bus are different"; none of these limitations are disclosed by the '039 Provisional.

The priority date of Claims 1, 5-9, 19, 23, and 25-26 of the '942 Patent should be no earlier than October 11, 2012, when U.S. Application No. 13/649,131 was filed.

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E. U.S. Patent No. 9,201,834

In its infringement contentions, Plaintiff asserts that: "Each of the Asserted Claims of the '834 Patent claim priority to provisional application No. 61/546,039, filed on Oct. 11, 2011, and Provisional application No. 61/555,468, filed on Nov. 3, 2011. The '834 Patent is a Continuation-in-part of application No. 13/649,131, filed on Oct. 11, 2012."

To the extent Plaintiff is asserting that the priority dates of Claims 1, 2, 4, 21 and 23 of the '834 Patent are earlier than November 2, 2012, Defendant disputes that these claims are entitled to priority from the '039 Provisional.

Independent Claims 1 and 21 recite "a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing" and "a second transmission bus coupled to the logic unit [and the ASIC processor] having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing." The '039 Provisional does not disclose these limitations.

The priority date of the Asserted Claims of the '834 patent should be no earlier than November 3, 2011, when Provisional Application No. 61/555,468 was filed.

VII. STATE OF THE ART

This section describes the general state of the art surrounding the claimed inventions at the time of the alleged invention and identifies a number of prior art references providing additional background, detail, and context, on which Defendant may rely. Defendant also intends to rely on each of the prior art references discussed in these Preliminary Invalidity Contentions, and exhibits thereto, for purposes of demonstrating the state of the art for the Asserted Patents. Defendant also reserves the right to rely on the discussions of the state of the art and prior art in each of the Asserted Patents and their file histories including explanations of the state of the art

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and the correspondence of prior art references with the claims of the Asserted Patents. Defendant further expressly reserves the right to supplement its summary of the state of the art, including for example, by information from any of the authors of or named inventors on any of the prior art references, by personnel familiar with systems based on any of the prior art, or by technical experts retained on behalf of any party.

As shown below, the features later claimed in the Asserted Patents were known and discussed in the prior art at the time of the alleged invention. The references cited in this section demonstrate that these features were part of the existing technological landscape, including in commercially available memory devices and systems.

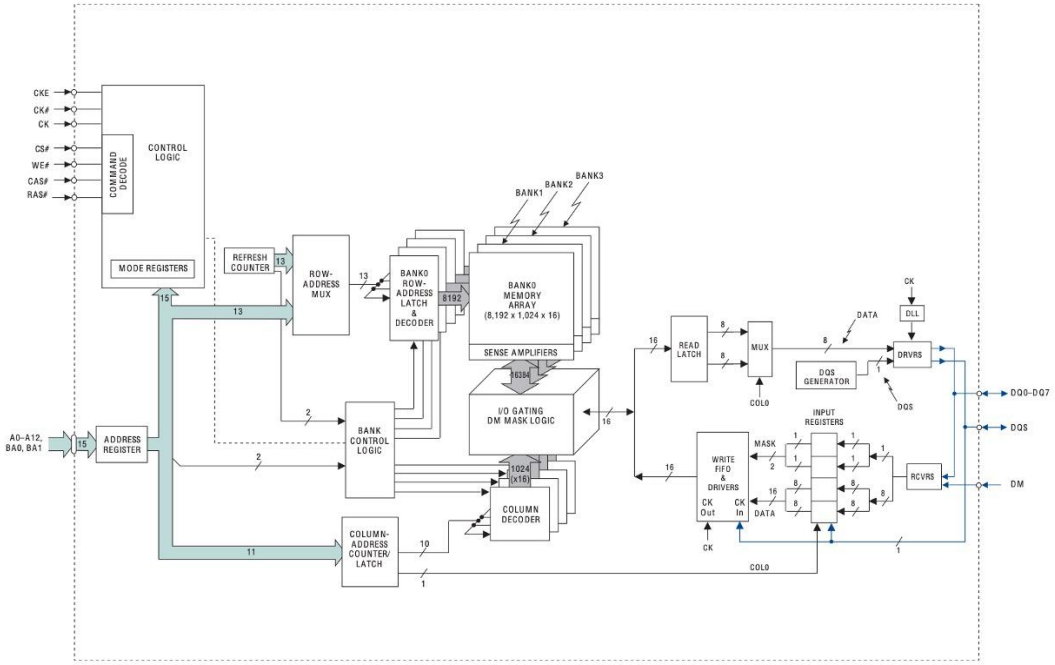
1. Configuration and Operation of DRAM

Dynamic Random-Access Memory (DRAM) is a type of volatile semiconductor memory often used as the main working memory in computers and other electronic devices. DRAM stores each bit of data in a memory cell that consists of one capacitor and one or more transistors. These memory cells must be periodically refreshed because the stored charge gradually leaks away. DRAM provides high memory density and relatively low cost per bit, but it is slower than on-chip cache memory and loses its contents when power is removed. DRAM technology has been in use since at least the late 1960s. For example, the widely used one-transistor DRAM cell was disclosed by Robert H. Dennard in 1966 and described in U.S. Patent No. 3,387,286, issued June 4, 1968, which predates the patents-in-suit by more than 40 years. (*See* U.S. Patent No. 3,387,286).

The memory cells of the DRAMs are organized in an array, wherein the rows and columns are selected by a combination of row and column address bits. Data is stored or retrieved by first opening a wide row of data. As an example, the functional block diagram of a 512 Mb DRAM below has four memory arrays (“Banks”), where each array has a row width of

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16K total bits (16 x 1024):



(*See* "*Micron MT46V128M4,_64M8,_32M16 Double Data Rate (DDR) SDRAM Datasheet*," at Fig. 3). Access begins by activating a row (wordline) to connect its cells to corresponding columns (bitlines). Sense amplifiers detect the presence or absence of the charge on the capacitor in the selected cell on the bitline. This allows the data to be read (and written) through the column selection circuitry. The row access is relatively slow due to the long row lines and large parasitic capacitance of the access transistors across all the columns. (*See* J. Poulton, "*An Embedded DRAM for CMOS ASICs*," at 2). Once the row is "open," the data bits are latched into a sense amp. (*Id.*). Typical device data widths are 4, 8, or 16 bits. (*See* X. Li, "*A Realistic Evaluation of Memory Hardware Errors and Software Systems Susceptibility*," at § 2.2). The column address is used to select data bits from the sense amp and I/O gating circuitry for output to the data buffers. The sense amp latches are essentially an addressable multiplexer allowing the data to be serialized for the output.

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2. Integration of the DRAM Core, Peripheral, and I/O Circuits

Simply put, DRAMs either store data into a memory array or retrieve data from the array, and the DRAM component must provide all the necessary circuits to realize these functions. Itoh describes the memory chip as having three blocks, "[a] memory chip is composed of three blocks []: a memory cell array, a peripheral circuit, and an input/output (I/O) interface circuit, as shown in Fig. 1.4":

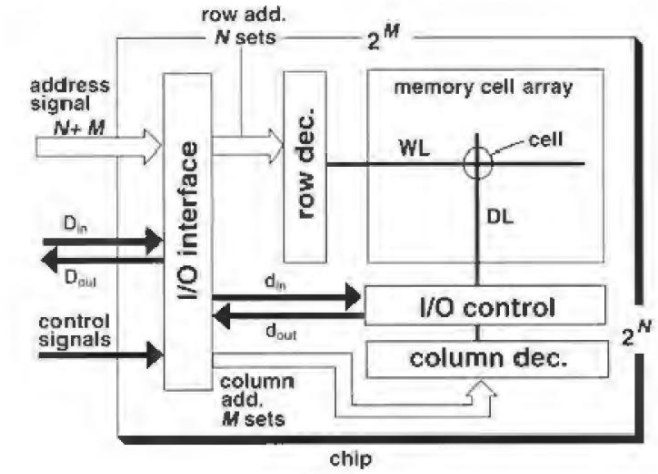


Fig. 1.4. The memory chip configuration

(K. Itoh, "*VLSI Memory Chip Design*" (hereinafter "*Itoh 2001*"), at 3-6, Fig. 1.4). The integration of these blocks into a single chip has always been the case for JEDEC specified DRAMs, and this was known at the time of the alleged invention. (*See, e.g.*, "*JESD209-2E Low Power Double Data Rate 2*" (hereinafter "*LPDDR2 Specification*"), at § 2 (illustrating ballout and pad configurations of an SDRAM chip including connections for power supplies for the core cell array, peripheral circuitry, and data input/output circuitry); "*JESD209-3 Low Power Double Data Rate 3*" (hereinafter "*LPDDR3 Specification*"), at § 2 (disclosing the same)).

3. The Trend to Integrate More Devices on a Single Chip

Evolutionary improvements in photolithography and process technology enable higher levels of integration on a single chip. "The fact that silicon integrated circuit technology is

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scalable was observed and described in 1965 by Intel founder Gordon Moore. His observations are now referred to as Moore's law and state that the number of devices on a chip will double every 18 to 24 months." (J. Baker, "*CMOS Circuit Design, Layout, and Simulation*" (hereinafter "*Baker*"), at xxxi). This paradigm results in a roadmap, which over time brings increases in processor complexity, increases of integration complexity with more functions on a chip, and increases in bit density for memory chips. (*See, e.g.*, G. Linden, "*System-on-a-Chip Integration in the Semiconductor Industry, Industry Structure and Firm Strategies*" (hereinafter "*Linden*"), at 1 ("Ever-advancing miniaturization continues to increase the number of design elements that can be placed on an integrated circuit (IC), creating the opportunity to build large-scale electronic systems on a single chip. This 'system-on-a-chip' (SOC) movement is engendering a marked shift in the approach towards creating, reusing and licensing designs for ICs."), 3 ("An SOC incorporates at least one processor, memory and any number of other functions, such as protocol converters, signal processors, and input and output controllers. While the semiconductor industry has witnessed various levels of on-chip functional integration in the past, the recent focus on SOC promises significant improvements in cost, portability and functionality of electronic end-products.")). By 2001, embedded DRAMs were proving to be viable options for custom memories. (*See, e.g.*, *Itoh 2001* at 340 ("[E]mbedded DRAMs are emerging architectures that boost the performance of standard DRAMs. … [S]tate-of the art DRAM miniaturization technology has at last progressed to the point at which embedded DRAMs are becoming attractive in terms of cost.")). A notable milestone in the development of system-on-a-chip technology was IBM's Power Processor 7 which, in 2009, replaced SRAM L3 cache of earlier generations with 32MB on-chip embedded DRAM. (*See* J. Barth, "*eDRAM to the Rescue*," at 6, 9).

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4. Memory Modules Wherein the Logic Interfaced with Memory and the Logic Gate Length Was Shorter than the Memory Gate Length

One of the challenges with embedded DRAM has always been disparate goals of a logic process versus a memory process. Any attempt to merge the two processes involves power, density, and speed compromises. It was conventional as of the purported invention dates of the Asserted Patents that for a given process generation, the gate length of memory (e.g., DRAM) transistors was longer than the gate length of logic transistors, given different performance criteria for the two types of devices. Logic scaling is focused on transistor switching speeds and energy efficiency, and accordingly, had short gate lengths, thin gate oxides, and no substrate reverse bias; while memory (e.g., DRAM) transistors were designed for low leakage, high density in the array core, and reliability, which accordingly had longer gate lengths, thicker gate oxides, and a reversed biased substrate. (*See, e.g.*, U.S. Patent No. 7,645,692 at 6:32-39; U.S. Patent No. 5,844,853 at 1:26-32, 1:45-52, 2:3-20; U.S. Patent No. 8,174,868 at 4:6-8; U.S. Patent No. 6,949,951 at 3:28-3; *see also, e.g.*, The International Technology Roadmap for Semiconductors, "*Overall Roadmap Technology Characteristics*" (hereinafter "*ITRS 2003*"), at 6).

It was also conventional as of the purported invention dates to use different gate material and topologies in the logic transistors than in DRAM. Specifically, in logic processes it was convention to use high-K metal gate (HKMG) transistors to reduce effective gate lengths; and in DRAMs, it was conventional to use recessed channel array transistors (RCAT) to increase effective gate lengths and reduce leakage current. One example of where these two processes were implemented is in the Intel Moorestown Platform SoC mobile processor, produced in 2010. This SoC used a 45-nm HKMG process and supported LPDDR1 devices. (*See, e.g.,* C. Mangano, "*Intel's Next-Generation Handheld Platform (codenamed 'Moorestown')*," at 1). The effective

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gate length was reported as 28 nm. (*See, e.g.,* C. Jan *et al*., "*A 45nm low power system-on-chip technology with dual gate (logic and I/O) high-k/metal gate strained silicon transistors*," at 1). Another example is the TI OMAP 3 processor, which was also produced in 2010 on a 45-nm logic process and coupled to LPDDR1 DRAMs. (*See, e.g.,* "*OMAP™ 3 Family of Multimedia Applications*," at 1, 3). Intel's HKMG 45-nm process during this timeframe had a reported 35-nm effective gate length. (*See, e.g.,* D. Scansen "*Under the Hood: 45 nm: What Intel didn't tell you*"). At a similar timeframe, the LPDDR devices were produced on 90-nm to 70-nm RCAT processes or spherical RCAT (S-RCAT) processes to increase the transistor effective gate length. (*See, e.g.,* J. Kim, "*S-RCAT (Sphere-Shaped-Recess-Channel-Array Transistor) Technology for 70nm DRAM Feature Size and Beyond*," at ¶2, Table 1). For the 90-nm process, an effective gate length of 350 nm was reported. (*See, e.g.,* D. James, "*Recent Innovations in DRAM Manufacturing*," at 2).

To achieve high circuit density and integration complexity, rather than attempt to fabricate the logic and memory on a single die, it was conventional to use 3D packaging to integrate logic chips (using one MOSFET process) and one or more DRAM chips (using a different MOSFET process). In mobile applications, package-on-package (POP) was a common packaging technique. In POP devices, DRAMs and processors were initially packaged in separate packages, and then the DRAMs were placed on top of the processor package with interconnections between the two:

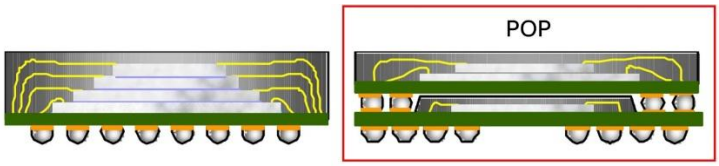


Figure 1: Structure of SCSP and PoP

("*Amkor Joint PoP*," at Fig. 1). The result was a high-performance logic device (with shorter

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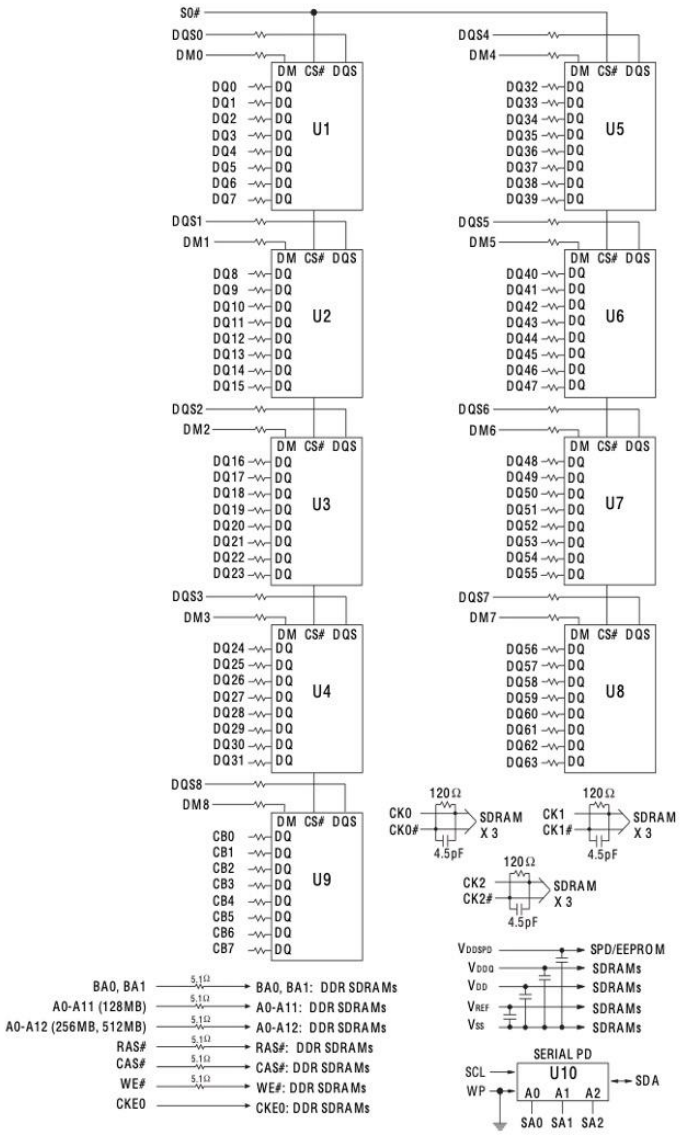
gate lengths) on the bottom and high density, low leakage DRAM chips on top (with longer gate lengths).

5. Memory Chip Modules with Bus Widths Greater than the Memory I/O Bus Width for Individual Memory Arrays

Also conventional at the time were memory modules known as Dual In Line Memory (DIMMs). DIMMs were printed circuit boards that contained a plurality of DRAM chips organized in ranks to provide a wider memory interface and greater bandwidth to a connected logic device. As shown in the exemplary functional block diagram below, a typical DIMM module consisted of eight 8-bit wide DRAMs (one rank) to form a 64-bit data bus; the entire rank of 8 DRAMs (each connected by individual 8-bit I/O bus) is accessed simultaneously over the 64-bit bus (DQ0-DQ63):

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Figure 3: Functional Block Diagram



("*Micron MT9VDDT3272AY-40BG4 DDR SDRAM Unbuffered DIMM datasheet*" at Fig. 3).[4]

B. DRAM Power Management

1. Using Separate Power Supply Voltages for DRAM Core Cells, Peripheral Circuits, and Input/Output Circuits

At the time of the alleged invention of the Asserted Patents, using separate power supply voltages for DRAM core cells, peripheral circuits, and input/output (I/O) circuits was well

[4] A ninth DRAM in the figure is provided for error correction and has a separate 8-bit bus (CB0-CB7).

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known. The specification of the '017 Patent discloses this fact: "Table I illustrates operation voltages (specified by the Joint Electron Device Engineering Council (JEDEC)) of a dynamic random access memory operating in the DDR I specification, a low power DDR I specification, the DDR II specification, and a low power DDR II specification." ('017 Patent, 2:65-3:2).[5] For example, in Table 1 for the "Low Power DDRII" (LPDDR2) row, the applicant of the '017 Patent family identified the following voltage ranges: 1.7v-1.95v for the "memory core unit 102," 1.14v-1.30v for the "peripheral circuit unit 104," and 1.14-1.3v for the "input/output unit 106":

TABLE I

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
DDR I	3.3 V ± 0.3 V or 2.5 V ± 0.2 V	3.3 V ± 0.3 V or 2.5 V ± 0.2 V	3.3 V ± 0.3 V or 2.5 V ± 0.2 V
Low Power DDR I	1.8 V ± 0.1 V	1.8 V ± 0.1 V	1.8 V ± 0.1 V
DDR II	1.8 V ± 0.1 V	1.8 V ± 0.1 V	1.8 V ± 0.1 V
Low Power DDR II	1.7 V~1.95 V	1.14 V~1.30 V	1.14 V~1.30 V

('017 Patent, Table I). While the patent specification does not detail the scope of these circuits or voltage domains, the applicant identified, in the admitted prior art, three voltages supplied to the memory core, peripheral circuit, and input/output unit, respectively.

At the time of the purported invention, it was common practice to use multiple voltage supplies within a DRAM to minimize power and optimize performance. For example, U.S. Patent No. 10,998,017 (hereinafter "Yamauchi"), which was filed in 2003, states in its Description of Background Art that "in a DRAM, a plurality of kinds of voltages of different voltage levels are used," (Yamauchi at 2:11-12), and further explained that the "general

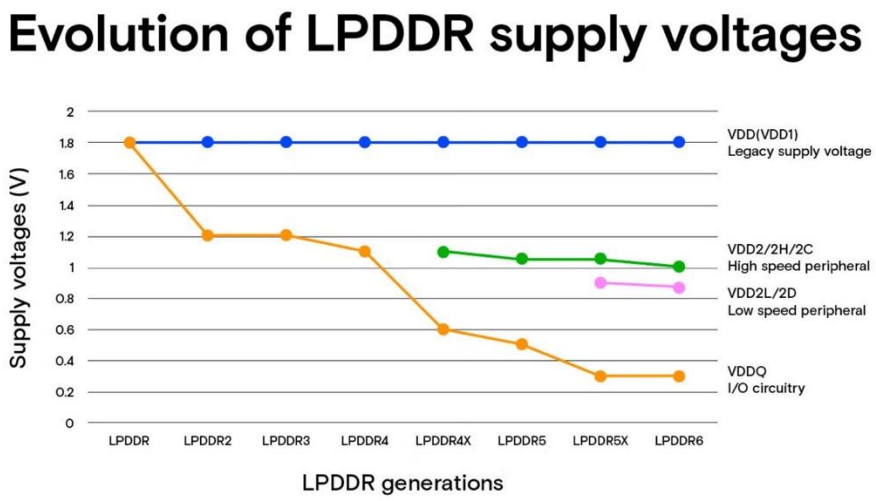
[5] The '017, '098, and '652 Patents share the same specification. It should be understood that herein and throughout, where applicable, citations to the '017 Patent are also representative of the same or similar citations to the '098 and '652 Patents.

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configuration of the conventional semiconductor memory device," (as illustrated in Fig. 37), includes "an internal voltage generating circuit 900 for generating various internal voltages Vpp, Vbb, Vbl, Vcp, Vdds, and Vddp in accordance with an external power supply voltage EXVDD" (Yamauchi at 2:39-42). Yamauchi also describes the use of these voltages, specifically, "[a] high voltage Vpp from internal voltage generating circuit 900 is also applied to row selecting circuit 906," and "[t]o column selecting circuit 910, usually, peripheral power supply voltage Vddp is applied as an operation power supply voltage," and that "VIH and VIL are set to, for example, 0.8VDDQ and 0.2VDDQ on the basis of an output power supply voltage VDDQ." (Yamauchi at 2:45-47, 2:61-63, 3-65:67).

In earlier DRAM technologies, one external power supply voltage was used, and the various voltage supplies were generated internally. (*See, e.g.*, Yamauchi at 2:39-42). As package pin pitch decreased, it became feasible to use more pins for external power supplies which allowed reductions in die size and on-chip power dissipation by eliminating some on-chip voltage regulators. (*See, e.g.*, Yamauchi at 2:16-19 ("In the DRAM as well, since the number of power supply pin terminals increases, the size of the package becomes large. Therefore, generally, the plurality of kinds of voltages are generated within a DRAM.")). Accordingly, the number of different power supply voltages supplied externally increased over time, as can be seen in Figure 2 below:

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(*See* R. Zhou, "*How does voltage scaling enable LPDDR5X to deliver efficient AI user experiences?*," at 2).

For example, KR Patent Publication KR015601B1 (hereinafter "Tomishima"), published Dec. 1, 1998, used three power supply voltages to provide power to the memory core, peripheral circuits, and input/output, "memory blocks in the first group to receive and operate a power supply voltage from the first pad 6. A data input / output pad unit (3c, 3d) installed corresponding to the memory block of the second group operating by receiving a power supply voltage from the input / output pad unit (3a, 3b) and the second pad (5); Peripheral circuit unit 4 which receives and operates a power supply voltage from the third pad 7." (Tomishima at Claim 18). Whether the supplies were generated internally or externally, using multiple internal DRAM power supply voltages was well-known at the time of the alleged invention. (*See, e.g.*, Tomishima at Fig. 1).

2. The Planned Use of DRAMs with Power Supply Voltages of Less Than 1.1v

Efforts to reduce power consumption have long been a driving consideration in the design of integrated circuits. (*See, e.g.*, Yamauchi at 3:9-14 ("In a semiconductor device, as the system scale increases, to prevent heat generation and the like, low power consumption is more

strongly required. Particularly, in applications of portable equipment using a battery as a power source, current consumption has to be reduced from the viewpoint of battery's life as well."); *Itoh 2001* at 434 ("The reduction of the operating voltage is essential not only to reduce power dissipation, but also to ensure reliability for miniaturized devices. Further reduction of the supply voltage allows users to design ultra-low-power systems or battery-based mobile equipment. One target is 0.9V, the minimum voltage of a NiCd cell.")). Predictably, DRAMs operating at 0.9V had been developed and demonstrated before the purported invention. (*See, e.g.*, S. Shukuri, "*A Complementary Gain Cell Technology for sub-1 V Supply DRAMs*," at 1 ("The test CG memory cell operation is successfully demonstrated at a supply voltage below 1V. … Table 1 compares the CG cell features with a 1T-cell assuming a supply voltage of 0.9V."); T. Oashi, "*16Mb DRAMS01 Technologies for Sub-1V Operation*," at 4 ("The operating voltage of 16Mb DRAM/SOI ranges from 0.9V to 2.0V as shown in Table 2")). Well before the time of the alleged invention, DRAMs with operating voltages of less than 1.1v had been demonstrated and published in papers.

3. DRAM Using Higher Core Cell Voltages Than Peripheral Circuit and I/O Circuit Voltages

The applicant of the '017 Patent family was aware of DRAMs in production that used higher voltage supplies for the core cell versus the peripheral and I/O circuits at the time of the alleged invention. ('017 Patent, 2:65-3:2, Table 1). In Table 1, for each of the three DRAMs of the admitted prior art, the applicant identified voltages supplied to the memory core unit that are different and greater than the voltages supplied to the peripheral circuit unit and input/output unit. ('017 Patent, Table 1). Indeed, this is confirmed by the JEDEC LPDDR2 specification, which was released in 2009:

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Table 69 — Recommended LPDDR2-S2 DC Operating Conditions

Symbol	LPDDR2-S2A			LPDDR2-S2B			DRAM	Unit
	Min	Typ	Max	Min	Typ	Max		
VDD1	1.70	1.80	1.95	1.70	1.80	1.95	Core Power1	V
VDD2	N/A	N/A	N/A	1.14	1.20	1.3	Core Power2	V
VDDCA	1.14	1.20	1.3	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	1.14	1.20	1.3	I/O Buffer Power	V

(LPDDR2 at Table 69). VDD1 is the core power supply with a typical value of 1.8v, while both VDD2 (which drives the core and peripheral circuits) and VDDQ (which is the I/O buffer power) are typically 1.2v. The use of a core voltage higher than that of the peripheral and I/O circuits continued even as voltage scaling progressed. (*See infra*, Section VII.B.1; R. Zhou, "*How does voltage scaling enable LPDDR5X to deliver efficient AI user experiences?,*" at 2). Using higher core cell voltages than peripheral circuit and I/O circuit voltages in DRAM was well-known at the time of the alleged invention.

4. Programmable Data Rates and Frequency Scaling

a) Programmable Data Rates and Frequency Scaling in Memory

In 2006, the roadmap for main memory bifurcated at JEDEC with the release of the JESD209 Low Power DDR (LPDDR, also referred to as LPDDR1 or Mobile DRAM) specification. (*See generally* JEDEC, "*JESD209B Low Power Double Data Rate SDRAM Standard*" (hereinafter "*LPDDR Specification*")). The low power specifications focused on short bus or point-to-point applications, lower power, and/or battery-operated applications. Several power saving features were added relative to the DDR standards, such as reducing the operating supply voltage (VDD) and the I/O power supply (VDDQ) from 2.5v to 1.8v, temperature compensated refresh, partial array refresh, deep power down mode, and clock stop mode. (*See, e.g.*, *LPDDR Specification* at 12).

LPDDR2 was subsequently standardized in 2009 with added power savings features. (*See*

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generally LPDDR2 Specification at Tables 2, 61). The core array supply voltage VDD1 remained at 1.8v, but the input/output supply voltage VDDQ was reduced to 1.2v. (*See LPDDR2 Specification* at Tables 2, 69, 70). In addition, two new supplies were also added: VDD2 = 1.2v, which supplied the peripheral logic and parts of the core, and VDDCA = 1.2v, which provided power to the input buffers. (*LPDDR2 Specification* at Tables 2, 69, 70). LPDDR2 also introduced the input clock stop and frequency change feature which allowed the input clock frequency to be changed, and therefore the data rate, under certain preconditions. (*See LPDDR2 Specification* at § 5.16). LPDDR2 supported a wide range of clock frequencies, 100 MHz to 533 MHz (*see LPDDR2 Specification* at Table 103), which allowed frequency scaling using the frequency change feature to reduce power dissipation during lighter transaction loads. Since it is a double data rate device, this allowed data rates to be changed from 200 MT/s to 1066 MT/s. DDR3 devices also support an input clock frequency mode and variable data rates, but with a narrower range than LPDDR2. (*See* JEDEC, "*JESD79-3E DDR3 SDRAM Specification*" (hereinafter "*DDR3 Specification*"), at § 4.7).

DRAM devices are ubiquitous, and the underlying specifications must support a wide variety of applications. Numerous features, modes, and mode registers have been included in the specifications to accommodate the usage models of different hardware applications. (*See, e.g.*, *LPDDR2 Specification* at Notice (setting forth objectives of JEDEC standards, including "eliminating misunderstandings between manufacturers and purchasers, [and] facilitating interchangeability and improvement of products")). For example, using the data mask function, the received data rates of Write data can be downscaled without affecting the data rates of the transmitted Read data output (e.g., providing a single data rate write with double data rate reads). (*See, e.g.*, *LPDDR2 Specification* at Table 2, § 5.7). This feature can provide a benefit to an

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application where the write bandwidth requirements are less than the read bandwidth requirements. Using the data mask function to provide asymmetric write/read bandwidth reduces the power dissipation without needing to change clock frequencies between reads and writes. This allows a faster turn-around time between read and write transactions.

b) Dynamic Frequency and Voltage Scaling in Processors

Dynamic Frequency and Voltage Scaling, DVFS, was introduced to processors to reduce power dissipation. Voltage and frequency were altered dynamically in selected processor logic blocks to reduce power in low activity and increase power in high activity. For example, the Crusoe processor, released by Transmeta Corp. in 2000, was one of the earliest uses of processor DVFS, which it referred to as LongRun Dynamic Power Management. (*See, e.g.*, Transmeta, "*Crusoe Processor Model TM5800*," at 6 ("LongRun achieves this dynamic power reduction by varying the CPU clock and core power supply voltage in response to adaptive power management protocols …."); M Fleischmann, "*LongRun(TM) Power Management - Dynamic Power Managmeent for Crusoe(TM) Processors*" (hereinafter "Fleischmann"), at 6, 10). The Crusoe processor allowed programmability of the main memory bus frequency at boot time by changing the memory clock ratio. DVFS was used in mobile processors by 2010 where the processors could take advantage of LPDDR2 power saving features and dynamically change memory bus frequency and data rates. In this timeframe, voltage scaling was also proposed for DDRx devices. (*See, e.g., generally*, H. David, "*Memory Power Management via Dynamic Voltage/Frequency Scaling*").

c) Dynamic Frequency and Voltage Scaling in Both Processors and Memory

The TI OMAP 4430, released in 2010, provides a good example of applying many of these power savings techniques. The OMAP 4430 is a System-on-Chip (SoC) designed for

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mobile applications, and it supported two channels of LPDDR2 memory. (*See, e.g.*, D. Witt, "*OMAP 4430 Architecture and Development*" (hereinafter "*Witt*"), at 3, 8-9, 14). To optimize power dissipation, it used multiple voltage domains throughout the chip and programmable voltage regulators to source the different supply domains with multiple operating performance points (OPPs), which define allowable frequency and voltage pairs for different domains. (*See, e.g.*, K. Morris, "*Software Thermal Management with TI OMAP Processors*" (hereinafter "*Morris*"), at 5). The TI OMAP 4430 generated frequency alterable clocks using a Digital PLL with programmable divider ratios. (*Morris* at 4). If the memory workload was low and the memory clock frequency could be lowered, the TI OMAP 4430 would use the input clock stop and frequency change mode of the LPDDR2 devices to change the clock frequency and, thereby, change the memory bus data rate. (*Morris* at 6; *Witt* at 8). Linux software drivers controlled the settings through hardware configuration registers within the SoC. Similar control over the host bus was also exercised. (Texas Instruments, "*OMAP4430 Multimedia Device Technical Reference Manual*" (hereinafter "*OMAP4430 Manual*"), at §§ 3.1.2.2 (describing Dynamic Voltage and Frequency Scaling (DVFS)), 3.8.6 (same)). The OMAP 4430 supported two channels of 32-bit LPDDR2 memory through a dynamic memory controller, but the narrow mode configuration register was also used to alter the channel to a 16-bit data width. (*See OMAP4430 Manual* at 3010, Table 15-130; *Witt* at 3, 8-9, 14).

Another SoC that had similar power saving features was the Transmeta TM8600 Efficeon Processor. (*See* "*Transmeta UPC Solutions Manual*," at 6). Released in 2004, the TM8600 Efficeon Processor integrated the northbridge on the processor and supported both DDR memory devices and a HyperTransport Mode interface. (*See, e.g.*, *id.* at 13, 16). The HyperTransport was a "low[] latency, highest-performance, fully scalable, packet-based interconnect technology"

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with "asymmetric Low Voltage Differential Signaling (LVDS) links." (*See* E. Powelson, "*ATI Endorses AMD's HyperTransport™ Technology*"). The TM8600 Efficeon Processor also supported Transmeta's LongRun power management technology which featured DVFS and memory frequency scaling. (*See Fleischmann* at 6-7).

Another example mobile processor is the NVIDIA Tegra 2, which was released in 2010. The Tegra 2 supported LPDDR, LPDDR2, and DDR2 memory and DVFS for both processor and memory. (*See* M. Toksvig, "*NVIDIA Tegra*" at 21; NVIDIA, "*Technical Reference Manual: NVIDIA TEGRA 2 Family*" (hereinafter "*Tegra 2 Manual*"), at 8, 298, 498-499, § 5.0, § 9.2, Fig. 1, Fig.15). Operating points were programmed to change the clock frequencies and voltages of different blocks. (*See Tegra 2 Manual* at § 9.2). The data rates on the high-speed AXI and AHB buses were also programmable via firmware in the processor. (*See Tegra 2 Manual* at § 10).

Yet another mobile processor that used power management features was the Freescale i.MX53, which went in production in the first quarter of 2011. The Freescale i.MX53 processor supported LPDDR2, DDR2, and DDR3 memories with 16- or 32-bit interfaces. (*See iMX53 Multimedia* at 189). The i.MX53 implemented processor DVFS bus frequency scaling, (*see iMX53 Sabre,* Sec.16.1,18.1), and memory frequency scaling, (*see* "*i.MX53 Multimedia Applications Processor Reference Manual*" (hereinafter "*i.MX53 Manual*"), at 1212). The AXI width can be configured to an x32 or x64 width via the AXI port gasket, (*see i.MX53 Manual* at 3460), and the AXI and memory data rates are independently programmable. The DDRx memory bus write transmit voltage swings are programmable via the IOMUX configuration registers, (*see i.MX53 Manual* at 1861), while the read receive voltage swings are programmable via the Phy control register ODT settings (*see i.MX53 Manual* at 1269).

5. Programmable High-Speed Buses

a) Peripheral Component Interconnect Express (PCIe)

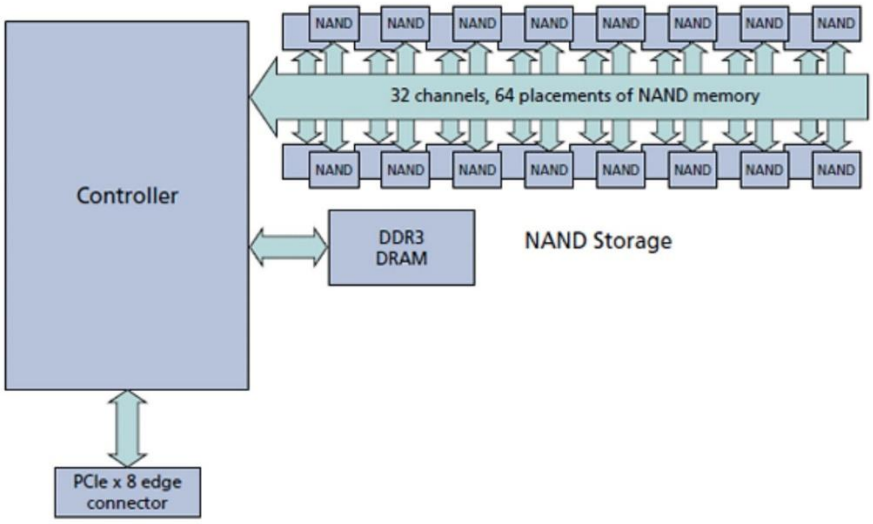
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A conventional interconnect bus at the time of the alleged invention was Peripheral Component Interconnect Express (PCIe). PCIe was standardized in 2002 and commonly used in computers as a high-speed interconnect bus in the early 2000s. PCIe provided high data rates with narrow bus widths. The number of lanes (bus width), the lane speed, and the voltage swing on the PCIe bus were all programmable. For example, the link width can be reduced when run in a "degraded mode." (*See, e.g.*, "*Intel(R) 5520 Chipset and Intel (R) 5500 Chipset Datasheet*" (hereinafter "*Intel 5520 Datasheet*"), at 49). The link data rate can further be set by a register. (*See* "*PCI Express Base Specification, Rev. 3.0*" (hereinafter "*PCIe 3.0 Specification*"), at 660-662 (disclosing a "Link Control 2 Register")). And the voltage swings in a PCIe bus can be set to either a full swing or reduced swing. (*See PCIe 3.0 Specification* at 333, 354). The PCIe interface was commonly included in logic chips such as northbridges, southbridges, PCIe controllers, other ASICs, and general-purpose processors.

PCIe was also used to attach storage appliances within the computer. An early example of a memory device using a PCIe bus to connect to a computer was Violin Memory Inc.'s solid-state drive (SSD) using DRAM. (*See, e.g.*, "*Violin Scalable Memory Products page*"; "Violin 1010 Memory Appliance page"; "*StorageSearch August 2007 entry*"). The Violin drive used a controller logic chip to interface the PCIe bus to a wide DRAM bus on the card.

Another example is the Micron P320H SSD, illustrated below:

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(D. Altavilla, "*Micron RealSSD P320h PCI Express SSD Review*," at 6). The PCIe interface provided the programmability of a high-speed bus with a wide DRAM bus on the other side of the controller.

b) HyperTransport Mode Bus

The HyperTransport Mode (HTM) bus, originally called Lightning Data Transport, debuted in 2001. (*See* "*HyperTransport™ Consortium - 2006 Press Release*"). The high-speed link was intended for intra-computer communications and featured two unidirectional links to and from a logic device. The link supported independent data transfer rates and bus widths for each direction. The data rate of each direction is software programmed via the Link Frequency Register, while the link width of each direction is programmed via the Link Configuration Register. (*See, e.g.*, "*AMD-8132TM HyperTransport™ PCI-X® 2.0 Tunnel Product Brief*," at 1; *"HyperTransport(TM) IO Link Specification 1.03*," at 88-92).

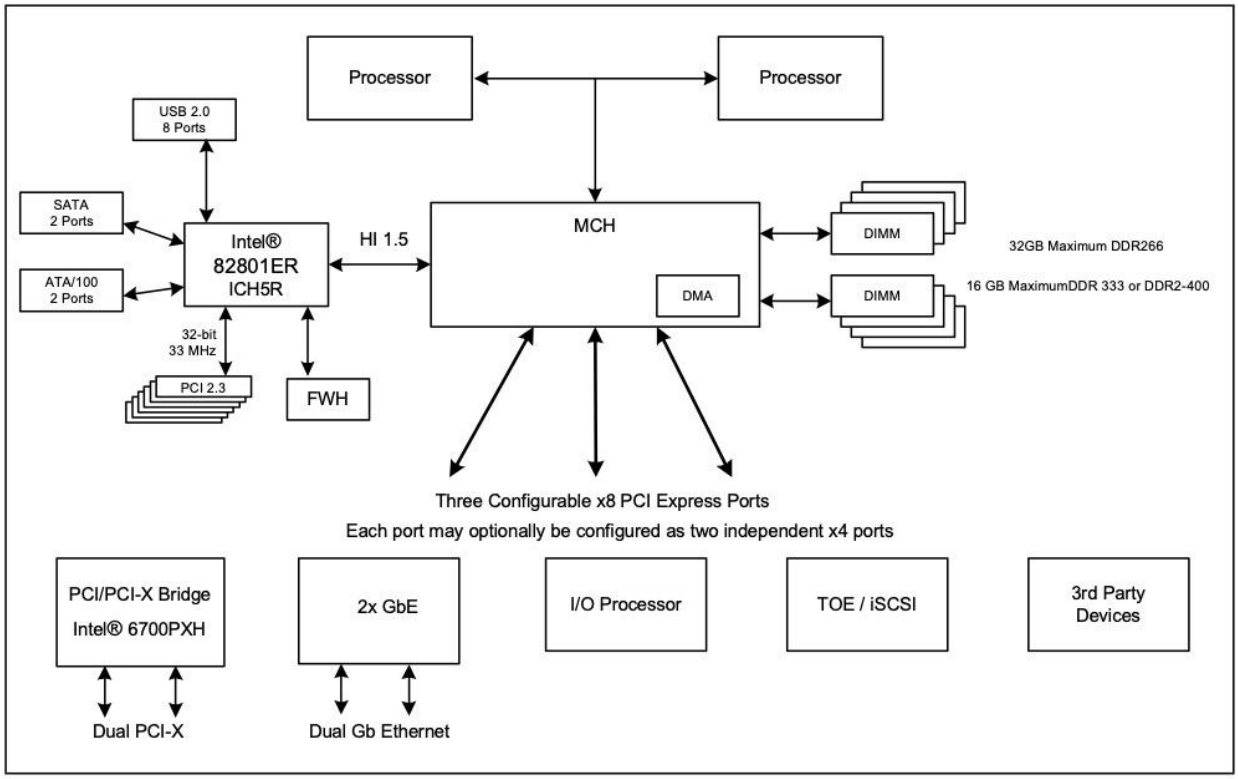
C. Converting Data Rates, Data Widths, and Voltage Swings Between Memory Buses and High-Speed Buses

Computer architectures in the early 2000s typically connected the processor to memory through a northbridge logic chip. The northbridge, sometimes called a memory controller hub

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(MCH), provided an interface to the processor bus, memory bus, and a high-speed link. The northbridge communicated via the different data rates, voltage swings, and data widths required by the various bus types. For example, the Intel E7520 MCH supported three different types of buses: a 64-bit system bus at 800 MT/s (Mega-transfers per second), a 128-bit memory data bus at 400 MT/s, and an x8 PCIe bus at 2.5 GT/s:

Figure 1-1. System Block Diagram

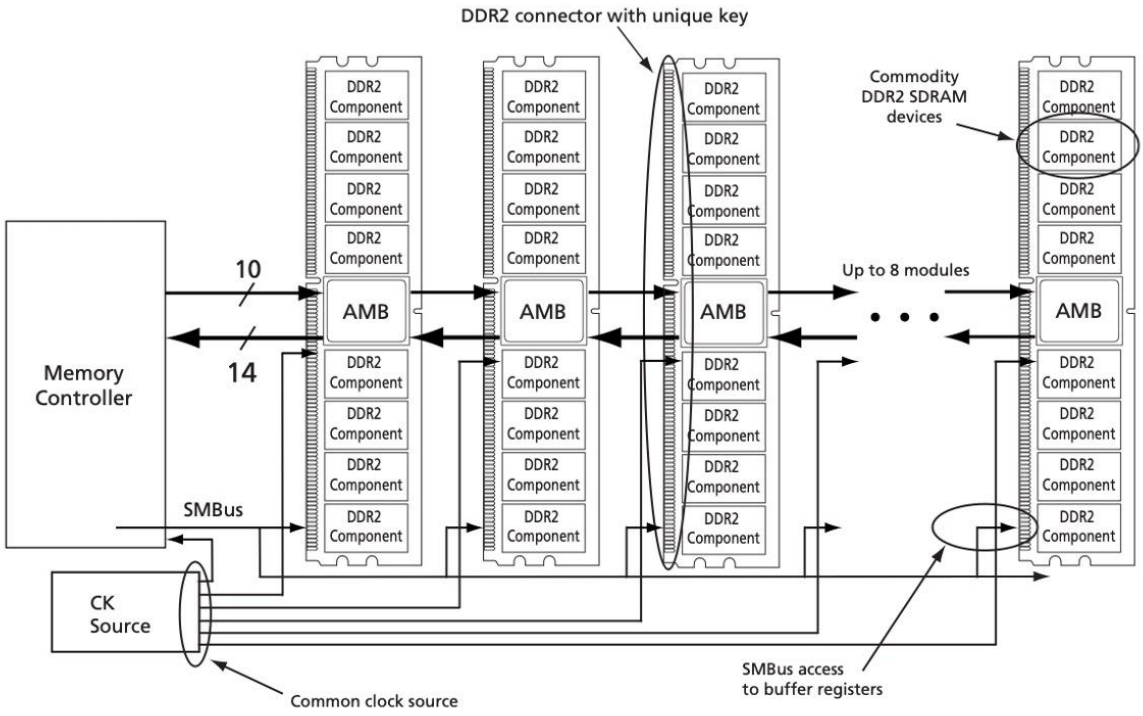


("*Intel® e7520 Memory Controller Hub Datasheet*" (hereinafter "*Intel e7520*"), at Fig. 1-1). To maintain the aggregate bandwidth, the MCH performed a 2:1 serialization from the memory bus to system bus and a 1:2 deserialization of the system bus to memory bus (64b * 800 = 128 * 400). All three buses on the MCH used different voltage swings. (*See, e.g.*, *Intel e7520* at 262-263).

With DDR2, the DIMM architecture changed to Fully Buffered DIMMs (FBDIMMs). FBDIMMs included a logic chip called an AMB (Advanced Memory Buffer) on the DIMM. As

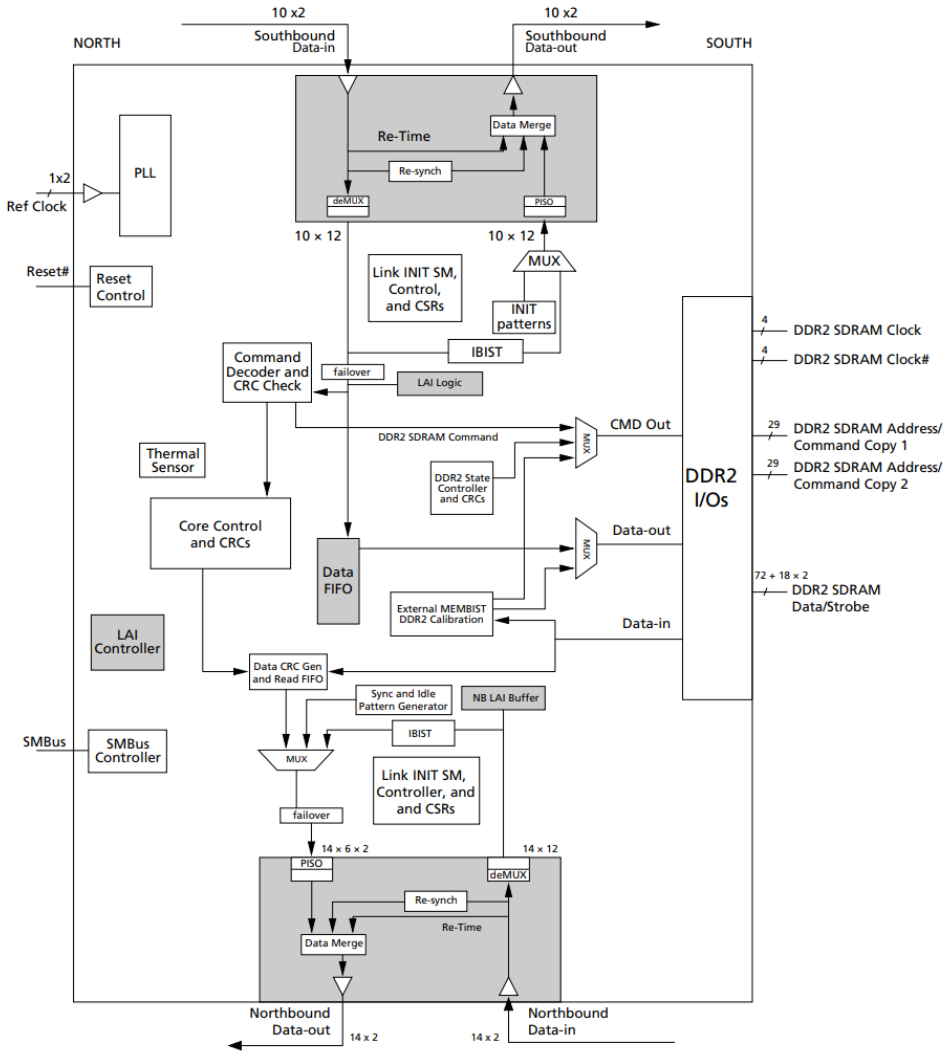
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illustrated in the example below, the AMB received a high-speed link from the northbridge and translated the data signals to a slower data rate and wider width for the 64-bit on-module data bus:



("*Micron MT36HTS51272F-4GB DDR2 SDRAM FBDIMM Datasheet*" (hereinafter "*Micron MT36HTS51272F Datasheet*"), at Fig. 2).

Figure 4: AMB Functional Block Diagram



(*Micron MT36HTS51272F Datasheet* at Fig. 4).

Serialization and deserialization were performed by the Read FIFOs and Write Data FIFOs within the AMB to maintain the same aggregate bandwidth of the two different busses, which also used different voltage swings. (*See, e.g.*, "*JESD205 FBDIMM Specification_DDR2 SDRAM Fully Buffered*," at 83; "*JESD83-20 FBDIMM Advanced Memory Buffer*," at 2, 19, 44). The voltage swings of the high-speed link were programmable by setting a configuration parameter in the AMB for large, regular, or small swings, and the transmitter voltage swings on the controller could be different than the swings on the FBDIMM AMB. (*See, e.g.*, *Micron*

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MT36HTS51272F Datasheet at 23; "*Intel® 6400/6402 Advanced Memory Buffer*" (hereinafter "*Intel AMB*"), at 20). The link frequency could also be changed through the link frequency configuration parameter. (*See Intel AMB* at 20). The voltage swings of the DDR2 DRAMs could be changed to a half-strength driver through a mode register setting, or the full-strength drive could be changed by a 4-bit code in Off-Chip Driver (OCD) adjust mode. (*See, e.g.*, "*JESD79-2F DDR2 SDRAM Specification*," at 21, 25). The AMB's DDR2 memory bus has the same independent capability.

The addition of the buffer on the module advantageously decoupled the memory's parasitic capacitance from the higher speed communication bus and added flexibility to the module. The buffer serialized and deserialized and provided physical layer conversion of the two busses to accommodate programmable data rates, voltage swings, and data widths of the two busses. (*See, e.g.,* U.S. Patent Publication No. 2004/0260864, [0021], Fig.2; U.S. Patent No. 6,882,082, 6:60-7:22, Claims 39-48; U.S. Patent No. 6,553,450, Fig.4, Claims 13-19; U.S. Patent No. 7,366,864, 3:53-4:7; U.S. Patent Publication No. 2010/0091537, [0043], [0051], Fig.7A,7B). The AMB, in particular, featured a programable high-speed bus width and voltage swing in addition to the voltage swings of the DRAM bus.

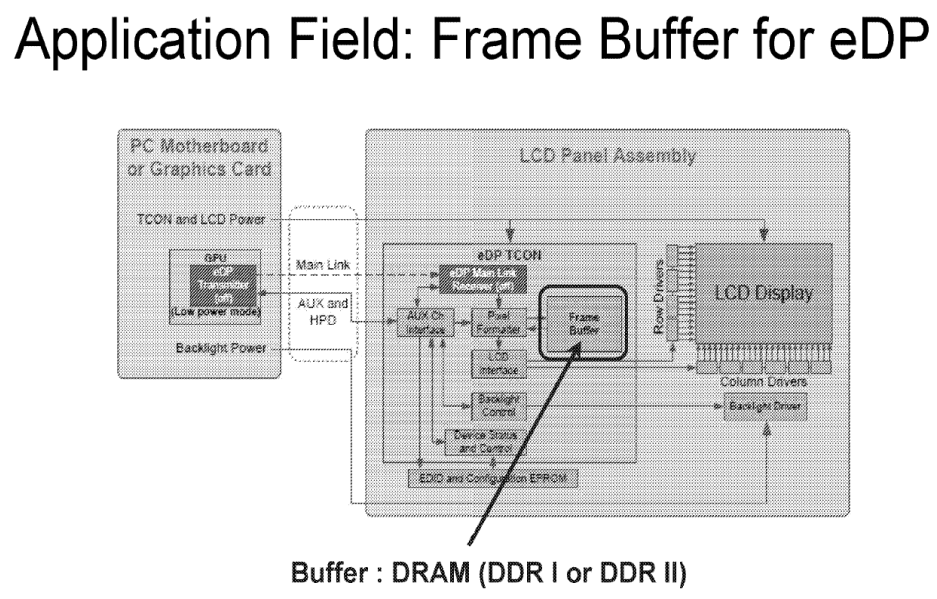
D. DRAM Capable of Being Applied to an Embedded DisplayPort

The Embedded DisplayPort (eDP) standard 1.3 was known at the time of the alleged invention and is the focus of the '017 Patent's Description of the Prior Art. (*See* '017 at 1:28-60). eDP evolved from DisplayPort, which was first standardized by VESA (Video Electronics Standards Association) in 2006. (*See* "*Embedded DisplayPort™ The New Generation Digital Display Interface for Embedded Applications*" (hereinafter "*Wiley*"), at 3). Embedded DisplayPort was standardized in 2008 and "was developed to be used specifically in embedded display applications." (*See Wiley* at 3, 17). eDP is based on the VESA DisplayPort Standard,

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shares the same electrical interface, and can share the same video port on the graphics processing unit (GPU). Specifically, eDP has the "same basic digital protocol" as the DisplayPort standard, "but with some differences added for eDP." (*See Wiley* at 3).

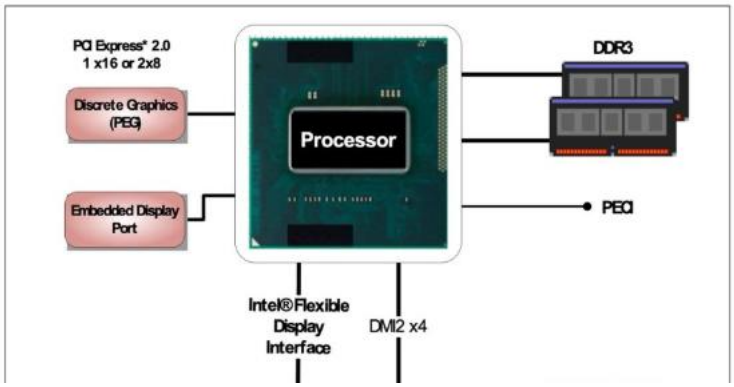
The specification of the '017 Patent presents the eDP 1.3 standard in its "Description of Prior Art," focusing on the addition of the "panel self refresh (PSR) function." ('017 Patent, 1:28-41). The '017 Patent explains that this function can reduce power consumption by "mak[ing] a graphic processing unit (GPU) turn off connection between the graphic processing unit and a liquid crystal panel when a frame displayed on the liquid crystal panel is frozen." (*Id.*). The '017 Patent further explains that this known feature of the admitted prior art includes a frame buffer in the display timing controller of the liquid crystal display. (*Id.*, 1:42-53). The applicant then describes the problem his alleged invention attempts to solve as increased power consumption due to the design of the "frame buffer." (*Id.*, 1:54-60). The frame buffer in the timing controller is illustrated in the '406 Provisional from which the '017 Patent family claims priority:



('406 Provisional at 12). As shown in the figure above, existing DRAM at the time ("DDR I or

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DDR II") was capable of being applied in LCD Panel Assemblies with eDP. Moreover, the '406 Provisional makes clear that, while the existing DRAMs were perhaps "not suitable" because they "[did] not save much power for EDP," DDR I, Low Power DDR I, DDR II, and Low Power DDR II were capable of being applied to eDP. ('406 Provisional at 13). Moreover, existing systems, such as the Sandy Bridge Mobile Processor and Samsung's Exynos 5 Dual RISC Microprocessor, available at the time, used both DDR3 DRAM and an Embedded Display Port:



("*Intel 2nd Generation Core Processor Family Mobile Datasheet Volume 1*," at 12; *see also, e.g.*, "*Samsung Exynos 5 Dual (Exynos 5250) RISC Microprocessor User Manual*," at § 1.1 ("Exynos 5250 supports not only low power eDP but also Panel-Self-Refresh (PSR) to make a low power system. … Exynos 5250 lowers the Bill of Materials by integrating … DDR3/LPDDR3 interfaces.")).

In sum, by the time of the alleged inventions, the technologies and architectural concepts implicated by the Asserted Patents were well understood and widely implemented in the field. As reflected in contemporaneous JEDEC standards, academic publications, technical textbooks, and commercial products, designers of memory devices and systems routinely employed multi-voltage DRAM architectures, separate core, peripheral, and I/O circuitry, programmable data rates and bus widths, voltage and frequency scaling, and logic-memory interfacing techniques to manage power, performance, and bandwidth. These features were not isolated

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innovations, but rather part of a mature and evolving design ecosystem driven by well-known constraints and objectives in semiconductor manufacturing and system integration.

The prior art further demonstrates that engineers of ordinary skill had ample motivation and ability to combine these known techniques in predictable ways to address power consumption, performance scaling, and interoperability across memory and high-speed interfaces. Against this backdrop, the Asserted Patents did not arise in a technological vacuum but instead were developed in view of an established state of the art in which the claimed concepts were already disclosed, practiced, or rendered obvious by existing knowledge and design practices.

Attached as Appendix A, by way of non-limiting example only, are certain background references to explain the state of the art as of the effective filing date of the Asserted Patents.

VIII. INVALIDITY UNDER 35 U.S.C. §§ 102 AND 103

Defendant contends that each Asserted Claim is invalid at least under 35 U.S.C. § 102, including pre-AIA subsections 102(a), 102(b), 102(e), and 102(g), and/or under 35 U.S.C. § 103. Pursuant to the Scheduling Order and the Local Rules, Defendant's contentions as to how each identified prior art reference either anticipates or renders obvious the Asserted Claims are attached as Exhibits. For each Asserted Patent, the Exhibits contain a separate chart for each anticipating and/or obviousness reference detailing where that reference teaches each limitation of the Asserted Claims.

Defendant also reserves the right to rely on other references disclosed or incorporated by reference in these Preliminary Invalidity Contentions, in prior art references identified or charted in these contentions, in the Asserted Patents, any patents or applications related to the Asserted Patents, in the file history of the Asserted Patents or any related patents or applications, and in

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the attached Exhibits. When a separate prior art reference is cited within an excerpt included in the Exhibits, that separate prior art reference is incorporated by reference.

Defendant's claim charts may disclose multiple theories of invalidity in a single chart. Each chart directed to an anticipatory product/system may also describe that the product/system alone, in view of the knowledge and skill in the art, or in view of one or more other prior art references, renders each Asserted Claim obvious.

Where Defendant cites a particular figure in a prior art reference, the citation should be understood to encompass the caption and description of the figure as well as any text relating to the figure in addition to the figure itself. Conversely, where a cited portion of text refers to a figure, the citation should be understood to include the figure as well. Furthermore, while Defendant has generally identified at least one citation per limitation present in a reference or combination, every disclosure of the same or similar limitation in the same reference or combination is not necessarily identified. To focus the issues, Defendant cites particularly pertinent portions of identified references, even where a reference or combination may contain additional support for a particular claim element. Thus, Defendant may rely on uncited portions of the prior art references for additional support or context for a particular element. Defendant may rely upon other prior art identified in future supplements, corroborating references, documentation, source code, products, and testimony, including materials obtained through further investigation and third-party discovery of the prior art identified herein, that demonstrates the invalidating functionality identified in these Preliminary Invalidity Contentions or that show the state of the art in the relevant time period (irrespective of whether such references themselves qualify as prior art to an Asserted Patent), and expert testimony to provide context to or aid in understanding the cited portions of the identified prior art. Similarly, where there are multiple

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references relating to a single prior art product or system, Defendant may cite only to a single reference for a particular limitation, even though other references may also contain similar teachings. Thus, Defendant may rely on uncited references relating to a particular prior art document or system for additional support for a particular element. Any prior art disclosed as anticipating a limitation also renders that limitation obvious.

Additionally, persons of ordinary skill in the art at the time of the alleged inventions generally read a prior art reference as a whole and in the context of other publications and literature. Numerous prior art references, including those identified herein and in the attached exhibits, reflect common knowledge and the state, scope, and content of the prior art before the priority date of the Asserted Claims of the Asserted Patents. Defendant may rely on uncited portions of the prior art references and on other publications and expert testimony to provide context and as aids to understanding and interpreting the portions that are cited.

In general, a claimed invention is invalid due to obviousness "if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art." 35 U.S.C. § 103; *Graham v. John Deere Co.*, 383 U.S. 1, 13-14 (1966). The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: "(1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art at the time of invention; and (4) objective evidence of nonobviousness." *Miles Labs., Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 (Fed. Cir. 1993); *see Graham*, 383 U.S. at 17-18. The U.S. Supreme Court decision in *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1739 (2007) reaffirmed *Graham*, but further held that a claimed invention can be obvious even if there is no explicit

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teaching, suggestion, or motivation for combining the prior art to produce that invention.

To the extent that any claim limitation is not anticipated pursuant to 35 U.S.C. § 102, Defendant contends that any purported differences are such that the claimed subject matter as a whole would have been obvious under 35 U.S.C. § 103 to one skilled in the art at the time of the alleged inventions, in view of the state of the art and knowledge of those skilled in the art. Each Asserted Claim would have been obvious in view of each reference cited in the attached Exhibits either alone or combined with the knowledge that was possessed by one of ordinary skill in the art. Additionally, each Asserted Claim would have been obvious to one of ordinary skill in the art in view of the combination of any one of the prior art references identified in the attached Exhibits with one or more of the other references identified or discussed in the same Exhibits.

In particular, those of ordinary skill in the art at the time of the alleged inventions of the Asserted Patents would have been motivated to modify or combine the prior art references because, for example: (a) the references in general deal with the same or related subject matter; (b) one of ordinary skill in the art would have been motivated by the problem that the inventor was attempting to solve, or with other problems that would have been faced in reaching a solution, and would have looked to references that concerned similar issues or taught how to overcome the problems faced; (c) the combinations were obvious to try and would have operated in their known and expected way; (d) the combinations were within the technical skill and understanding of a person of ordinary skill in the art; (e) the combinations would have been motivated by the developments in technology; and (f) the combinations reflect various design choices that would have been known to one of ordinary skill in the art and within that person's technical capability to implement (i.e., technically feasible).

The various motivations described above provide a basis for combining or modifying

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references, as detailed below, to render each of the Asserted Claims obvious. In addition, the Court can consider the inferences and creative steps a person of ordinary skill in the art would employ in making such combinations. *See KSR*, 127 S. Ct. at 1741 ("a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ").

Additional motivations to combine references may be found in the discussion of the state of the art, above, and in the discussion of invalidity with respect to each Asserted Patent, below.

If, and to the extent, Plaintiff challenges the correspondence of the references in the Exhibits with respect to particular limitations of the Asserted Claims of the Asserted Patents, Defendant reserves the right to supplement these Preliminary Invalidity Contentions to identify additional combinations, motivations to modify, or explanations for particular references with additional particularity.

Additionally, Defendant believes that certain non-parties and current or former employees thereof may have possession of relevant information and/or documents constituting prior art to the Asserted Patents. Defendant is continuing the investigation into these and other companies and their products. Defendant reserves the right to supplement these Preliminary Invalidity Contentions to identify additional references, combinations, motivations to modify, or explanations for particular references based on any information and/or documents provided by the former employees and/or successors-in-interests of companies or individuals who may possess relevant information and/or documents constituting prior art to the Asserted Patents. The concepts disclosed and claimed in each of the Asserted Patents are not new, and had been disclosed, used, offered for sale, sold, and practiced by others prior to the claimed priority date of the patents. The prior art identified herein and in the Exhibits, individually or in combination, invalidates the Asserted Claims under 35 U.S.C. §§ 102 (a), (b), (e), (g) and §103. Because

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discovery is ongoing, Defendant expects to gather additional information about the identified prior art, and other prior art, through third-party discovery or other discovery, and will thus amend and supplement these Preliminary Invalidity Contentions once they obtain that discovery and have meaningful and reasonable time to analyze it. The Asserted Claims may also be invalid under 35 U.S.C. §§ 101 and 112.

Moreover, Defendant reserves the right to rely on inventor admissions concerning the scope of the prior art relevant to the Asserted Patents found in, inter alia, the prosecution histories of the Asserted Patents or related patents and/or patent applications, any testimony or declarations of the named inventors concerning the Asserted Patents or related patents, and any papers or evidence submitted by Plaintiff in connection with this litigation, any other pending or future litigation brought by Plaintiff involving the Asserted Patents or related patents, or inter partes review proceedings involving the Asserted Patents or related patents. Defendant also may establish what was known to a person having ordinary skill in the art through references discussed above in connection with the state of the art and treatises, published industry standards, other publications, products, and/or testimony.

A. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the Asserted Claims. The attached claim charts in Exhibits A through E demonstrate where each limitation of the claims is found in, either expressly or inherently in the larger context of the passage, or rendered obvious by, certain of the references listed below, as understood by a person having ordinary skill in the art. The following patents, publications, products, and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e). To the extent Defendant identifies a patent publication as prior art, Defendant reserves the right to rely on the patent which issued from that publication, and vice-versa.

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1. Prior Art Patents and Patent Publications.

Reference No.	Filing Date	Issue/ Pub. Date	Title
US20070002636A1 ("Campbell '636")	7/1/2005	1/4/2007	Integrated circuit with separate supply voltage for memory that is different from logic circuit supply voltage
US20130100121A1 ("Cha '121")	4/20/2012	4/25/2013	Display driver and method of operating image data processing device
US20110063927A1 ("Dono '927")	9/10/2010	3/17/2011	Semiconductor device using plural internal operation voltages and data processing system using the same
US20120327062A1 ("Endo '062")	4/5/2012	12/27/2012	Electronic apparatus, control method of electronic apparatus, and non-transitory computer-readable medium storing computer executable control program of electronic apparatus
US5262999A ("Etoh '999")	3/24/1992	11/16/1993	Large scale integrated circuit for low voltage operation
US20120033506A1 ("Furutani '506")	8/5/2011	2/9/2012	Semiconductor device
US20110080797A1 ("Furutani '797")	10/4/2010	4/7/2011	Semiconductor device having sense amplifiers
US20100271289A1 ("Goodart '289")	4/22/2009	10/28/2010	System and method for authenticating a display panel in an information handling system
US20120140578A1 ("Goto '578")	11/28/2011	6/7/2012	Semiconductor device having plural internal voltage generating circuits and method of controlling the same
US20090003105A1 ("Itoh '105")	6/26/2007	1/1/2009	Semiconductor device
US6097641A ("Lu '641")	11/1/1999	8/1/2000	High performance dram structure employing multiple thickness gate oxide
US20080117700A1 ("Nakamura '700")	8/31/2007	5/22/2008	Dynamic semiconductor storage device and method for operating same
US20100245366A1 ("Nath '366")	3/29/2010	9/30/2010	Electronic device having switchable graphics processors
US20110310223A1 ("Pai '223")	4/13/2011	12/22/2011	Systems and methods for controlling a three dimensional (3d) compatible viewing device
US20020194425A1 ("Penchuk '425")	4/11/2002	12/19/2002	Method and apparatus for integrated circuit with DRAM
US20090067217A1 ("Sunwoo '217")	2/20/2008	3/12/2009	Methods for supplying power supply voltages in semiconductor memory devices and semiconductor memory devices using the same

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US20100290300A1 (“Takahashi ’300”)	4/28/2010	11/18/2010	Semiconductor integrated device
US20080186303A1 (“Takahashi ’303”)	1/9/2008	8/7/2008	Display driver IC having embedded DRAM
US20080291750A1 (“Takahashi ’750”)	5/23/2008	11/27/2008	Semiconductor device that uses a plurality of source voltages
US20120327726A1 (“Tsern ’726”)	12/1/2010	12/27/2012	Methods and circuits for dynamically scaling dram power and performance
US20120242671A1 (“Wyatt ’671”)	3/24/2011	9/27/2012	Method and apparatus to support a self-refreshing display device coupled to a graphics controller
US7738311B2 (“Youn ’311”)	11/6/2007	6/15/2010	Semiconductor memory devices having optimized memory block organization and data line routing for reducing chip size and increasing speed
US5187392A (“Allen ’392”)	7/31/1991	2/16/1993	Programmable logic device with limited signal swing
KR101533120B1 (“Best ’120 MT”)	12/13/2007	7/1/2015	Multi-die memory device
US20100091537A1 (“Best ’537”)	12/13/2007	4/15/2010	Multi-die memory device
US20100235554A1 (“Chang ’554”)	9/5/2008	9/16/2010	Reconfigurable point-to-point memory interface
US20100174858A1 (“Chen ’858”)	1/5/2009	7/8/2010	Extra high bandwidth memory die stack
US7647467B1 (“Hutsell ’467”)	12/19/2006	1/12/2010	Tuning DRAM I/O parameters on the fly
US7596675B2 (“Jobs ’675”)	3/7/2008	9/29/2009	Memory hub architecture having programmable lane widths
KR101213175B1 (“Kang ’175 MT”)	8/20/2007	12/18/2012	Semiconductor package having memory devices stacked on logic chip
US6807650B2 (“Lamb ’650”)	6/3/2002	10/19/2004	DDR-II driver impedance adjustment control algorithm and interface circuits
US8218347B1 (“Law ’347”)	10/12/2010	7/10/2012	Stacked memory device having a scalable bandwidth interface
US20040260864A1 (“Lee ’864”)	6/19/2003	12/23/2004	Reconfigurable memory module and method
US6754746B1 (“Leung ’746”)	3/23/2000	6/22/2004	Memory array with read/write methods
US5498990A (“Leung ’990”)	4/5/1995	3/12/1996	Reduced CMOS-swing clamping circuit for bus lines
US20010003836A1 (“Maclellan ’836”)	12/23/1997	6/14/2001	Plural bus data storage system
US7645692B2 (“Matsubara ’692”)	11/27/2007	1/12/2010	Semiconductor device and method of manufacturing the same
US20060262587A1	7/26/2006	11/23/2006	Memory module and memory system

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("Matsui '587")			
US7215561B2 ("Park '561")	8/21/2003	5/8/2007	Semiconductor memory system having multiple system data buses
US6889304B2 ("Perego '304")	11/22/2002	5/3/2005	Memory device supporting a dynamically configurable core organization
US7949817B1 ("Sakarda '817")	7/29/2008	5/24/2011	Adaptive bus profiler
US20020073274A1 ("Swaminathan '274")	12/4/2001	6/13/2002	Apparatus and method to precisely position packets for a queue based memory controller
US20100005214A1 ("Trombley '214")	7/1/2008	1/7/2010	Enhancing bus efficiency in a memory system
WO2008124503A1 ("Tsern '503")	4/3/2008	10/16/2008	Memory system topologies including a buffer device and an integrated circuit memory device
US20040158669A1 ("Weng '669")	3/24/2003	8/12/2004	Architecture for a serial ATA bus based flash memory apparatus
JP2010268006A ("Koichiro '006")	8/20/2010	11/25/2010	Semiconductor integrated circuit
US7167039B2 ("Garrett, Jr. '039")	8/29/1997	1/23/2007	Memory device having an adjustable voltage swing setting
JP2010268006A ("Ishibashi '006 MT")	8/20/2010	11/25/2010	Semiconductor integrated circuit

2. Prior Art Systems/Services and Non-Patent Publications to the Asserted Claims.

Publication / Sale Date	Title
Aug. 2009	A Sub-0.9V Logic-compatible Embedded DRAM with Boosted 3T Gain Cell, Regulated Bit-line Write Scheme and PVT-tracking Read Reference Bias ("Chun 2009")
Mar. 2006	Low-Voltage and Low-Power Logic, Memory, and Analog Circuit Techniques for SoCs Using 90 nm Technology and Beyond ("Ishibashi 2006")
2001	VLSI Memory Chip Design ("Itoh 2001")
Apr. 2011	JEDEC Standard JESD209-2E Low Power Double Data Rate 2 ("LPDDR2")
May 2012	JEDEC Standard JESD209-3 Low Power Double Data Rate 3 ("LPDDR3")
Feb. 1999	DRAM Design Overview ("Ogawa 1999")
	VESA Embedded DisplayPort Standard 1.3 ("eDP 1.3")
Dec. 2007	A Novel Capacitor-less 2-T SOI DRAM Cell ("Zhang 2007")
Jan. 2005	Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor ("Nakai 2005")

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2011	LPDDR2 compliant DRAM system
2012	LPDDR3 compliant DRAM system
2010	TI OMAP 4430 system
2007	The Intel Server System
2007	Intel® Server System SR1530SH Homepage ("Intel SR1530SH Homepage")
2010	Intel Server Board S3200SH_S3210SH Technical Product Specification ("Intel S3200SH/S3210SH Technical Specification")
Nov. 2008	Intel Server Boards S3210SH_S3200SH Tested Hardware and Operating System List ("Intel S3210SH/S3200SH Hardware and OS List")
Jan. 2008	Intel RAID Controller SRCSASPH16I Technical Product Specification ("Intel RAID Controller Specification")
Feb. 2005	Intel Server System - 3200-3210-chipset-memory-controller-hub-datasheet ("Intel 3200/3210 Memory Controller Datasheet")
Nov. 2009	JESD79-2F DDR2 SDRAM Specification ("DDR2 Specification")
Oct. 2006	The AMB System
Oct. 2006	Intel, "Intel 6400-6402 Advanced Memory Buffer Datasheet" ("Intel 6400-6402 AMB")
2005	Micron MT18HTF12872FDY-DDR2 SDRAM FBDIMM Datasheet ("Micron DDR2 SDRAM")
Jan. 2007	JESD206, FBDIMM Architecture and Protocol, 2007 ("FBDIMM")
May 2011	The i.MX53 System was publicly available as of at least May 2011, and is described by, e.g.:
Dec. 2011	freescale, "i.MX53 Multimedia Applications Processor Reference Manual" ("i.MX53 Processor Manual")
May 2011	freescale, "i.MX53 Sabre Tablet Linux Reference Manual" ("i.MX53 Sabre Reference")
Apr. 2011	JEDEC JESD209-2E Low Power Double Data Rate 2 Specification ("LPDDR2")
2008	The HyperTransport Mode Bus System
2005	HTM - 'AMD-8132TM HyperTransportTM PCI-X® 2.0 Tunnel Product Brief
Aug. 13, 2009	HTM - HC21.23.110.Duato-HTC-HT3
2006	HTM - HyperTransport Consortium - 2006 Press Release
Oct. 10, 2001	HTM - HyperTransport IO Link Specification 1.03
Apr. 21, 2006	HTM - HyperTransport IO Link Specification 3.0
2009	HTM - Litz - A HyperTransport 3 Physical Layer Interface for FPGAs
Sep. 2009	HTM - Renesas - Tsi308(TM) HyperTransport to PCI_X User Manual
Jan. 27, 2003	HTM - Sartori - 'Royalty-free HyperTransport makes good on chip-to-chip bandwidth
Feb. 2004	HTM - Wayback - HyperTransport 2.0 Specification
Apr. 2006	HTM - Wayback - HyperTransport 3.0 Specification
Aug. 18, 2008	HTM - Wayback - HyperTransport 3.1 Specification
Aug. 22, 2008	HTM - Wayback - HyperTransport Link Specifications
Oct. 23, 2006	"Celoxica Ships HyperTransport Solution," Embedded

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Nov. 1, 2007	R. Yasin, "HP delivers high-performance accelerators," Route Fifty
Nov. 2008	M. Aitkin, "A Reconfigurable Accelerator Card for High Performance Computing," Univeristy Cape Town Dissertation
2006	H. Froning, "The HTX-Board_ A Rapid Prototyping Station"
2005	The AMD K10 System
Mar. 2012	AMD - Revision Guide for AMD Family 10h Processors
Jan. 11, 2013	AMD - BIOS and Kernel Developer's Guide
2009	AMD - CPU World - AMD K10 processor families
Nov. 2009	JESD79-2F DDR2 SDRAM Specification

B. Claim Charts, Obviousness Combinations, and Motivations to Combine

The attached claim charts in Exhibits A-01—A-30, B-01—B-30, C-01—C-30, D-01—D-32, and E-01—E-29 demonstrate where each limitation of the claims is found in, either expressly or inherently in the larger context of the passage, or rendered obvious by, certain of the references listed below, as understood by a person having ordinary skill in the art. Exhibits A-00, B-00, C-00, D-00, and E-00 set forth exemplary anticipatory references and combinations that render obvious the Asserted Claims, along with exemplary motivations to combine prior art references where applicable. Defendant reserves the right to identify additional combinations and motivations to combine as discovery continues and in response to Plaintiff's subsequent contentions and proposed claim constructions.

IX. INVALIDITY UNDER 35 U.S.C. § 112

Pursuant to this Court's Scheduling Order and OGP, and subject to Defendant's reservation of rights, Defendant identifies below the grounds upon which it contends the Asserted Claims are invalid for lack of written description and/or enablement under 35 U.S.C. § 112, ¶ 1, and/or for failing to comply with the definiteness requirements of 35 U.S.C. § 112, ¶ 2. The disclosures below do not attempt to identify all recitations of a given term or phrase in each claim. Where Defendant has identified an instance of a term or limitation in a particular claim that renders the claim invalid under Section 112, Defendant contends that every instance of the

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challenged term or limitation, or similar term or limitation, in the claim renders the claim invalid for the same reasons.

The following contentions are subject to revision and amendment under Federal Rule of Civil Procedure 26(e) and the Orders of record in this matter where appropriate in light of further investigation and discovery regarding the defenses below, the Court's construction of the claims at issue, or the review and analysis of expert witnesses.

Subject to Defendant's reservation of rights, Defendant identifies the following written description, enablement, and indefiniteness grounds with respect to the following asserted claims. Where a particular claim term or limitation is identified, Defendant contends that the identified term or limitation, as well as the surrounding claim language in context as recited in the applicable claim, suffer from the identified Section 112 defect. Furthermore, where a particular claim term or limitation is identified with respect to one or more particular claims, Defendant contends that each other Asserted Claim that recites the same claim term or limitation, or similar claim term or limitation, is subject to the same Section 112 defect. Defendant also reserves the right to assert additional Section 112 defenses as discovery progresses.

The specifications of certain Asserted Patents do not provide adequate written description to support the scope of the claims asserted by Plaintiff in furtherance of its infringement theories or any reasonably understood scope of the claims.[6] 35 U.S.C. § 112 ¶ 1 requires the specification to contain "a written description of the invention." To fulfill the written description requirement, the specification "must clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed." *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (citation omitted). To satisfy the written description requirement, "the applicant

[6] This is also true of the original application(s) that gave rise to the Asserted Patents.

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must 'convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,' and demonstrate that by disclosure in the specification of the patent." *Carnegie Mellon Univ. v. Hoffmann-La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir. 2008) (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991)). Certain of the Asserted Patents do not meet that requirement for the reasons described below. Defendant reserves the right to amend this list.

Additionally, certain of the Asserted Patents do not enable the claim scope contended in Plaintiff's Infringement Contentions.[7] Title 35 U.S.C. § 112 ¶ 1 requires the specification to describe "the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains … to make and use the [invention]." The enablement requirement is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. This "requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003) (citation omitted); *see Wyeth & Cordis Corp. v. Abbott Labs.*, 720 F.3d 1380 (Fed. Cir. 2013). Certain of the Asserted Patents do not meet that requirement for the reasons described below. Defendant reserves the right to amend this list.

Certain of the Asserted Claims are invalid for failing to comply with the definiteness requirement of 35 U.S.C. § 112. Defendant notes that its charting of a prior art reference for a claim or limitation that Defendant contends is invalid for lack of definiteness in no way represents an admission or concession that the scope of the claim or limitation is definite or ascertainable. 35 U.S.C. § 112 ¶ 2 requires that a patent claim "particularly point[] out and

[7] This is also true of the original application(s) that gave rise to the Asserted Patents.

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distinctly claim[] the subject matter which the applicant regards as his invention." Claim terms that fail to inform those skilled in the art "with reasonable certainty . . . about the scope of the invention" fail the definiteness requirement of § 112 ¶ 2. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014). The patent laws of the United States prohibit claiming an invention through functional terms as way to capture every way of performing a function. Claim terms that recite an invention using functional terms are invalid as indefinite, except for those adequately claimed and supported in accordance with 35 U.S.C. § 112 ¶ 6. Under 35 U.S.C. § 112 ¶ 6, an element in a claim may be expressed as a "means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." "The standard [for determining whether § 112(6) applies] is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015). Although use of the word "means" in a claim creates a "presumption that § 112, ¶ 6 applies," "[w]hen a claim term lacks the word 'means,' the presumption can be overcome and § 112, para. 6 will apply if the challenger demonstrates that the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function." *Id*. (internal quotations omitted). Certain of the Asserted Claims are indefinite for at least the reasons described below. Defendant reserves the right to amend this list and may identify additional or different terms that are invalid under Section 112 in accordance with the schedule in this case for identifying terms for construction.

A. Indefiniteness

Defendant contends that the following claim limitations of the Asserted Claims are invalid as set forth below under 35 U.S.C. § 112, ¶ 2 for failing to particularly point out and

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distinctly claim the subject matter which the applicants regard as the alleged invention. The scope of the following claim terms is not reasonably certain, rendering the Asserted Claims in which they appear—and all claims that depend from such claims—invalid as indefinite.

Limitation	Asserted Claims	Basis for Indefiniteness
"input/output [unit/circuit]"	'017 (cl. 2) '098 (cls. 3, 6) '652 (cls. 1, 2, 3)	An "input/output [unit/circuit]" should be construed as a § 112, ¶ 6 means-plus-function limitation. Based on its name, the function is a unit/circuit that performs input and/or output functions with respect to memory. As set forth in the related *inter partes* reviews, the Specification's disclosure of this term's structure is limited to a box electrically connected to two other boxes. *See* IPR2026-00241 (Pap. 2) at 4-5 (citing '017, Abstract, 1:64-2:34, 2:49-65, Fig. 1); IPR2026-00242 (Pap. 2) at 4-5 (similar); IPR20206-000243 (Pap. 2) at 4-5 (similar). The Specification's minimal disclosure would not be understood by a person of ordinary skill to have a sufficiently definite meaning as the name for structure under § 112, ¶ 6. Further, (1) the specification does not disclose sufficient corresponding structure for that term, and/or (2) if a sufficient corresponding structure is disclosed, it is not adequate corresponding structure to achieve the claimed functions.

In view of the specifications and file histories of the Asserted Patents, the above terms—as well as any other similar terms in any of the Asserted Claims—fail to inform those skilled in the art about the scope of the invention with reasonable certainty. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014) (holding that "a patent is invalid for indefiniteness if its claims read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention"). As such, the Asserted Claims identified above are invalid as indefinite. *See id.* Defendant also reserves the right to seek a ruling of indefiniteness on any shorter terms or phrases within the

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items in the above list, or of longer terms or phrases.

B. Lack of Written Description and/or Enablement

The Asserted Claims are invalid for failure to comply with 35 U.S.C. Section 112's written description or enablement requirements. For instance, to the extent any Asserted Claim is interpreted to encompass any of the below concepts, the specifications of the Asserted Patents do not provide sufficient written description or enablement of such concept, rendering the Asserted Claims of the patents in which they appear invalid.

"embedded display port (eDP)" ('017 Patent, '098 Patent, '652 Patent). The specification of the '017, '098, and '652 Patents fails to provide sufficient written description or enablement for the "embedded display port (eDP)" limitations. Claim 1 of the '017 Patent recites that "the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP)." ('017 Patent, Cl. 1). Claim 6 of the '098 Patent recites that "the first voltage and the third voltage is capable of being applied to an embedded display port (eDP)." ('098 Patent, Cl. 6). And Claim 3 of the '652 Patent recites that "the DRAM is capable to be applied to an embedded display port (eDP)." ('652 Patent, Cl. 3). The shared specification of the '017, '098, and '652 Patents, however, provides insufficient guidance as to the scope of the "embedded display port" limitations.

"the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, … wherein the first voltage is lower than 1.1V" ('017 Patent, '098 Patent, '652 Patent). The specification of the '017, '098, and '652 Patents fails to provide sufficient written description or enablement for the "DRAM core cell is supplied with a first voltage … lower than 1.1V" limitations. Claim 1 of the '017 Patent recites that "a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the

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DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V." ('017 Patent, Cl. 1). Claims 1 and 2 of the '098 Patent and Claims 1 and 2 of the '652 Patent recite that "a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V." '098 Patent, Cls. 1, 2; ('652 Patent, Cls. 1, 2). And dependent Claims 4 and 7 of the '098 Patent and dependent Claim 4 of the '652 Patent recite that "the first voltage is lower than 1.1V." ('098 Patent, Cls. 4, 7; '652 Patent, Cl. 4). The shared specification of the '017, '098, and '652 Patents, however, provides insufficient guidance as to the meaning of the "embedded display port" limitations.

To the extent Plaintiff contends that these terms recited in the Asserted Claims are not described in the prior art, or that these terms that Plaintiff alleges are in the Accused Systems are not described in the prior art or meets these claim limitations, the claims are invalid for lacking sufficient written description and/or enablement. *See LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005). The Asserted Claims therefore do not meet the written description or enablement requirements of 35 U.S.C. § 112 for at least the reason that the patent specification does not provide support for the full scope of the claims to the extent Plaintiff asserts that the claims are broad enough to cover Defendant's products. *See id.* The patent specification, viewed in the context of Plaintiff's Infringement Contentions would not enable a person of ordinary skill in the art to practice the alleged invention without undue experimentation. Also, viewed in the context of Plaintiff's Infringement Contentions, a person of ordinary skill in the art would not understand the named inventor to be in possession of the purported invention. *See id.* Thus, the claims are invalid under the first paragraph of 35 U.S.C. §

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112 for lack of written description and lack of enablement. *See id.*; *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351-52 (Fed. Cir. 2010) (en banc); *Strick v. Dreamworks, LLC*, 516 F.3d 993, 999 (Fed. Cir. 2008).

X. KNOWLEDGE OF ONE OF ORDINARY SKILL IN THE ART

To the extent that Plaintiff contends that any particular feature or element of the Asserted Claims is a novel aspect of the claimed subject matter, Defendant reserves the right to illustrate that the particular feature was widely known, understood, and implemented by those of ordinary skill in the art at the time of the alleged invention, and that it would have been obvious to combine and/or modify the prior art identified throughout these Preliminary Invalidity Contentions with the knowledge of one of ordinary skill in the art. Defendant reserves the right to illustrate the knowledge of one of ordinary skill in the art using any of the prior art references identified throughout these Preliminary Invalidity Contentions, expert testimony, learned treatises, and/or testimony of prior art fact witnesses.

XI. ADDITIONAL INVALIDITY CONTENTIONS

Defendant incorporates by reference, in full and including supporting exhibits, the invalidity contentions served by defendants in Plaintiff's other proceedings involving any of the Asserted Patents, including but not limited to the invalidity contentions served in *WeCrevention Inc. v. Lenovo Group Limited et al.*, 2-25-cv-01008 (E.D. Tex.), *WeCrevention, Inc. v. Dell Inc. et al.*, 2-25-cv-01040 (E.D. Tex.).

Precise identification of all the bases upon which the Asserted Claims are invalid and/or unenforceable, including inequitable conduct, improper inventorship, and the judicially created non-statutory obviousness-type double patenting doctrine, are likely to be revealed only after further developments in the case, including fact and expert discovery. Defendant expressly

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reserves the right to amend or supplement these Preliminary Invalidity Contentions to address any additional invalidity arguments that become apparent in view of any relevant facts and information revealed during the course of discovery to the extent required by the Local Rules and the Scheduling Order.

XII. DOCUMENT PRODUCTION ACCOMPANYING PRELIMINARY INVALIDITY CONTENTIONS

Pursuant to the OGP and Scheduling Order and based on Defendant's investigation to date and understanding of Plaintiff's Infringement Contentions, Defendant is producing, concurrently with these Preliminary Invalidity Contentions, all prior art referenced in the Preliminary Invalidity Contentions.

Pursuant to the OGP and Scheduling Order and based on Defendant's investigation to date and understanding of Plaintiff's Infringement Contentions, Defendant is producing, concurrently with these Preliminary Invalidity Contentions, technical documents sufficient to show the operation of the accused products identified by Plaintiff's infringement contention charts. Defendant will continue to produce relevant non-privileged documents on a rolling basis as they are collected, consistent with the deadlines for such production in the Scheduling Order.

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Dated: March 17, 2026

/s/ Stephen Marshall

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CERTIFICATE OF SERVICE

I hereby certify that, on March 17, 2026, all counsel of record who have appeared in this case were served with a copy of the foregoing via electronic mail.

Dated: March 17, 2026 */s/ Stephen Marshall*

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APPENDIX A

1. Prior Art Patents and Patent Publications.

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2. Prior Art Systems/Services and Non-Patent Publications to the Asserted Claims, and Relevant Documents.

Publication Date	Title
Oct. 1, 2010	"Technology Development of Three-Dimensional Functional Integrated Circuits (Dream Chips)" Interim Evaluation Report
Feb. 16, 2013	[RFC 2_2] clk_ tegra20_ Use DT defines for CLK ID
1996	16 Mb DRAM SOI Technologies for Sub-1 V Operation
Mar. 15, 2012	2012 S-Series Richie 13.3" UMA/DIS Muxless Schematic
Mar. 2012	2G bits DDR2 Mobile RAM™ PoP Data Sheet
	3.6.5.4.4 Change Frequency During Self-Refresh Mode with Low-power DDR-SDRAM Devices
Oct. 13, 2009	3D DRAM Design and Application to 3D Multicore Systems
2011	3D Embedded Multi-core: Some Perspectives
Oct. 15, 2010	3D IC Using through Silicon via Technologies

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Dec. 19, 2010	3D Logic–Memory Integration for High-Performance Embedded Systems and Reconfigurable Computing
Dec. 2011	4G bits DDR2 Mobile RAM™ PoP (12mm × 12mm, 168-ball FBGA) EDB4432BAPA
Nov. 11, 2010	6-1 Image Memory (1) Semiconductor Memory
Oct. 2011	8-Output Regular Powers Applications Processors
2001	A 1.0V 230MHz Column-Access Embedded DRAM Macro for Portable MPEG Applications
June 18, 2010	A 1.1V, 667MHz Random Cycle, Asymmetric 2T Gain Cell Embedded DRAM with a 99.9 Percentile Retention Time of 110μsec
2012	A 1.2V 30nm 1.6 Gbspin 4Gb LPDDR3 SDRAM with Input Skew Calibration and Enhanced Control Scheme
2009	A 1.35V 4.3GB/s 1Gb LPDDR2 DRAM with Controllable Repeater and On-the-Fly Power-Cut Scheme for Low-Power and High-Speed Mobile Application
2011	A 1V Printed Organic DRAM Cell Based on Ion-Gel Gated Transistors with a Sub-10nW-per-Cell Refresh Power
2012	A 32nm High-k Metal Gate Application Processor with GHz Multi-Core CPU
Nov. 18, 2010	A 3D SoC Design for H.264 Application with On-Chip DRAM Stacking
June 2011	A 3T Gain Cell Embedded DRAM Utilizing Preferential Boosting for High Density and Low Power On-Die Caches
Jan. 1, 2009	A 3T Gain Cell Embedded DRAM Utilizing Preferential Boosting for High Density and Low Power On-Die Caches
	A 45nm low power system-on-chip technology
Sep. 29, 2007	A 65nm Low-Power 2T1D Embedded DRAM with Leakage Current Reduction
1999	A 800 MBs 72Mb SLDRAM with Digitally-Calibrated DLL
July, 21, 2020	A Better Way to Measure Progress in Semiconductors
	A Complementary Gain Cell Technology for Sub-1 V Supply DRAMs
Sep. 22, 2010	A Customized Design of DRAM Controller for On-Chip 3D DRAM Stacking
Mar. 27, 2006	A Design of Interface Module for Multiple Level MIL-STD-1553 Bus Topology
June 2004	A Design of SPI-4.2 Interface Core
	A HyperTransport 3 Physical Layer Interface for FPGAs
2012	A Low Power DDR SDRAM Controller Design
July 19, 1999	A New Architecture for Embedded Memory with Current Type CACHE
Dec. 2007	A Novel Capacitor-less 2-T SOI DRAM Cell (“Zhang 2007”)
2009	A Parallel Memory Test Structure for Testability of System-on-Chips
	A Realistic Evaluation of Memory Hardware Errors and Software

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	Systems Susceptibility
Nov. 2008	A Reconfigurable Accelerator Card for High Performance Computing
Nov. 1997	A Study on the Low Power Architecture of Multi-giga bit Synchronous DRAM's
June 2003	A Study on the SoC Design Using Programmable Logic Device
Aug. 2009	A Sub-0.9V Logic-compatible Embedded DRAM with Boosted 3T Gain Cell, Regulated Bit-line Write Scheme and PVT-tracking Read Reference Bias ("Chun 2009")
Sep. 10, 2006	Advanced DRAM and Post-DRAM Technology
Apr. 1, 2006	Advanced Memory Buffer for Fully Buffered DIMM Modules
Sep. 2007	AMD K10 Processor Families
	AMD-8132™ HyperTransportTM PCI-X® 2.0 Tunnel Product Brief
	An Embedded DRAM for CMOS ASICs
2009	An Optimized 3D-Stacked Memory Architecture by Exploiting Excessive, High-Density TSV Bandwidth
Jan. 2011	Annotated Intel Second Generation Core Processor Family Mobile
2003	Application Specific Integrated Circuits (ASICs)
Feb. 13, 2001	ATI Endorses AMD's HyperTransport™ Technology
Jan. 11, 2013	BIOS and Kernel Developer's Guide (BKDG) For AMD Famliy 10h Processors
Oct. 23, 2006	Celoxica Ships HyperTransport Solution
Aug. 1999	Channel Width Dependence of Hot-Carrier Induced Degradation in Shallow Trench Isolated PMOSFET's
2010	CMOS Circuit Design, Layout, and Simulation, Third Edition
July 5, 2001	Crusoe Processor Model TM5800
June 11, 2012	DDR Memory Trends and Design Considerations
June 11, 2012	DDR Memory Trends and Design Considerations
Jan. 2005	DDR2 SDRAM Specification
July 2010	DDR3 SDRAM Specification
Feb. 18, 2017	DDR4 SDRAM-History-circuit Board Pcb
May 5, 2009	DDRdrive Redefines Solid-State Storage - HotHardware
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Mar. 18, 2011	Design Space Exploration for 3D-stacked DRAMs
Feb. 2009	Designing for the Use Case: Using the OMAP™ 4 platform to overcome the challenges with integrating multiple applications
July 1, 2009	Development and Future Vision of Multi Chip Package for Combination between Logic Device and Stacked Memories with through Silicon Via
Feb. 2008	Development of 3D Stack Package Using Silicon Interposer for High-Power Application
June 2009	Disaggregated Memory for Expansion and Sharing in Blade Servers

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2012	DisplayPort
Feb. 11, 1999	DRAM Design Overview (“Ogawa 1999”)
Sep. 11, 2008	DRAM gets more exotic
Jan. 2005	Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor (“Nakai 2005”)
June 9, 2011	EDA tools pave path to 3-D ICs, part 1
2009	eDRAM to the Rescue
Dec. 1, 2019	Efficient Pipelined Broadcast with Monitoring Processing Node Status on a Multi-Core Processor
Nov. 24, 2011	Elpida Develops 1600 Mbps 4-gigabit DDR3 Mobile RAM (LPDDR3)
Dec. 6, 2010	Embedded DisplayPort™: The New Generation Digital Display Interface for Embedded Applications
2009	Embedded Memories for Nano-Scale VLSIs
Jan. 17, 2013	Empirical Analysis of Power Management Schemes for Multi-core Smartphones
2010	Evolution and Outlook of TSV and 3D IC/Si Integration
	External Memory Interface (EMIF)
Oct. 2012	Exynos 5 Dual User Manaul Public REV1
Feb. 3, 2012	Exynos Video Driver "exynos_dp_reg.h"
Jan. 2007	FBDIMM Architecture and Protocol
Nov. 16, 2012	Google Nexus 10 Take Apart First Look
2011	Heterogeneous Die Stacking of SRAM Row Cache and 3-D DRAM: An Empirical Design Evaluation
2005	High-Density Low-Power-Operating DRAM Device
Sep. 1, 2011	High-Frequency Transmission Characteristics of the Interconnects Stacked into the 3D IC Configuration
Aug. 4, 2011	HotChips 23 Hybrid Memory Cube
	How does voltage scaling enable LPDDR5X to deliver efficient AI user experiences
Nov. 1, 2007	HP Delivers High-Performance Accelerators
1997	HYB25SL64180V-400 SLDRAM Datasheet
2012	Hybrid Memory Cube New DRAM Architecture Increases Density and Performance
2012	Hybrid Memory Cube Specification 1.0
2012	HyperTransport 2.0 Specification
2011	HyperTransport 3.0 Specification
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2008	HyperTransport Link Specification
	HyperTransport™ Consortium Press Release
Oct. 10, 2001	HyperTransport™ IO Link Specification 1.03
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Dec. 2011	i.MX53 Multimedia Applications Processor Reference Manual
May 2011	i.MX53 Sabre Tablet Linux Reference Manual
Dec. 1, 2011	IBM to produce Micron's Hybrid Memory Cube with 3D CMOS
Aug. 21, 2008	IDF_ DDR4 als Hauptspeicher ab 2012
November 2007	Intel 3200 and 3210 Chipset Datashet
Oct. 2006	Intel 6400-6402 Advanced Memory Buffer Datasheet
Jan. 2011	Intel Second Generation Intel® Core™ Processor Family Mobile Datasheet - Volume 1
Mar. 2010	Intel® 4 Series Chipset Family Datasheet
Mar. 2009	Intel® 5520 Chipset and Intel® 5500 Chipset Datasheet
Sep. 2007	Intel® 7300 Chipset Memory Controller Hub Datasheet
Jan. 2010	Intel® Core™ i7-600, i5-500, i5-400 and i3-300 Mobile Processor Series
Feb. 2005	Intel® E7520 Memory Controller Hub Datasheet
Jan. 2008	Intel® RAID Controller SRCSASPH16I Technical Product Specification
May 2010	Intel® Server Board S3200SH/S3210SH Technical Product Specification
Nov. 2008	Intel® Server Boards S3210SH/S3200SH Tested Hardware and Operating System List
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Sep. 25, 2009	Interface Technology in 3D IC
Mar. 21, 2006	Interfacing a Low-voltage Processor with 3 V SD/SDIO or MMC Cards
Nov. 2008	Is 3D chip technology the next growth engine for performance improvement?
Feb. 10, 2005	ISSCC 2005 The CELL Microprocessor
Feb. 23, 2012	J11 MLB PIB Schematic
Apr. 2011	JEDEC Standard JESD209-2E Low Power Double Data Rate 2 (“LPDDR2”)
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Sep. 20, 2011	JEDEC Standards for 3D Stacked Integrated Circuits
Mar. 2007	JESD205 FBDIMM Specification_DDR2 SDRAM Fully Buffered
Apr. 2011	JESD209-2E Low Power Double Data Rate
May 2012	JESD209-3 Low Power Double Data Rate 3
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Nov. 2009	JESD79-2F DDR2 SDRAM Specification
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Jan. 17, 2001	LongRun™ Power Management - Dynamic Power Managmeent for Crusoe™ Processors
Mar. 2006	Low-Voltage and Low-Power Logic, Memory, and Analog Circuit Techniques for SoCs Using 90 nm Technology and Beyond ("Ishibashi 2006")
2011	LPDDR2 compliant DRAM system
2012	LPDDR3 compliant DRAM system
July 8, 2011	Memory for Exascale and Hybrid Memory Cube
2016	Memory Interface Design for Hybrid Memory Cube (HMC)
June 2011	Memory Power Management via Dynamic Voltage_Frequency Scaling
2011	Micron 4G: bx6, x32 Mobile LPDDR2 SDRAM S4 Data Sheet
Aug. 22, 2011	Micron Hybrid Memory Cube
2005	Micron MT18HTF12872FDY-DDR2 SDRAM FBDIMM Datasheet
2006	Micron MT36HTS51272F-DDR2 SDRAM FBDIMM Datasheet
2000	Micron MT46V128M4, 64M8, 32M16 Double Data Rate (DDR) SDRAM Datasheet
June 3, 2011	Micron RealSSD P320h can read 3GBps, write 2GBps, impress millions of geeks per second
Oct. 15, 2012	Micron RealSSD P320h PCI Express SSD Review
Jan. 24, 2003	MPEG2 HDTV Video decoder
Oct. 2012	Nanya 2Gb LPDDR2-S4 SDRAM Data Sheet
Mar. 2013	Nanya 512Mb LPDDR2-S4 SDRAM Data Sheet
	NVIDIA Tegra
	NVIDIA Tegra20 SoC External Memory Controller
2008	OMAP 4430 Architecture and Development
July 2010	OMAP4430 Multimedia Device Silicon Revision 2.0 Technical Reference Manual
2009	OMAP™ 3 Family of Multimedia Applications Processors
2003	Overall Roadmap Technology Characteristics
Apr. 29, 2002	PCI Express Base Specification v1.0
Nov. 10, 2010	PCI Express Base Specification, Rev. 3.0
Dec. 20, 2006	PCI Express® Base Specification Revision 2.0
Nov. 10, 2010	PCI Express® Base Specification Revision 3.0
June 2012	Product Manual - COM Express
2010	Recent Innovations in DRAM Manufacturing
Sep. 30, 2010	Renesas Electronics Introduces Next-Generation 1.1Gb Low-Latency, High-Speed Memory Devices with Low Power Consumption for Networking Equipment
Apr. 2001	Reviews and Proposals of Low-Voltage DRAM Circuit Design

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Mar. 2012	Revision Guide for AMD Family 10h Processors
Jan. 27, 2003	Royalty-Free HyperTransport Makes Good on Chip-to-Chip Bandwidth
Sep. 18, 2012	Samsung Announces Production of Industry's First 2GB LPDDR3 Mobile Memory Using 30nm-class Technology
Nov. 30, 2011	Samsung Exynos 5250 Experiencing the Cloud
June 2013	Samsung Mobile DRAM Brochure
Apr. 19, 2013	Samsung Nexus 10 GT-P8110 Tablet Teardown
Apr. 27, 2012	Samsung Officially Unveils the Quad Core Cortex A9 Exynos 4412
2012	Samsung Product Selection Guide Displays, Memory and Storage - 2H 2012
2011	Samsung Product Selection Guide LCD, Memory and Storage - 1H 2011
Feb. 2012	SEC Exynos4412 Users Manual Ver 1.00
1996	Semiconductor Device Fundamentals (excerpts)
2010	Sense Amplifier with Offset Mismatch Calibration for Sub 1-V DRAM Core Operation
Aug. 2, 2010	Software Thermal Management with TI OMAP Processors
July 8, 2011	Spartan-6 FPGA Block RAM Resources User Guide
2005	S-RCAT (Sphere-Shaped-Recess-Channel-Array Transistor) Technology for 70nm DRAM Feature Size and Beyond
	Start-Up DDRdrive Emerges From Stealth Mode
	StoarageSearch, August 2007 entry
July 2007	Sub-1.2-V 1-Gb Mobile DRAM with Ultra-low Leakage Current
2009	Sun Netra CP3220 Blade Server User's Guide - Chapter 5 Hardware Architecture
2003	System-on-a-Chip Integration in the Semiconductor Industry Industry Structure and Firm Strategies
Dec. 15, 2004	TC59YM916BKG MOS Digital Integrated Circuit Datasheet
	Technical Reference Manual NVIDIA TEGRA 2 Family
2003	The Breakthrough in Data Retention Time of DRAM
	The HTX-Board: A Rapid Prototyping Station
2011	The Second Genration Intel® Core™: a Highly Integrated High Performance Multi IA-Core and Processor Graphics Chip
Dec. 10, 2010	Three-Dimensional Integration of Stacked Memory and Logic Devices
Nov. 2011	Three-Dimensional Stacked Memory System for Defect Tolerance
2010	TI OMAP 4430 system
Oct. 1, 2008	Toshiba Shows off its SpursEngine
Sep. 2009	Tsi308™ HyperTransport to PCI X User Manual
2011	TSV based Silicon Interposer Technology for Wafer Level Fabrication of 3D SiP Modules
Jan. 21, 2008	Under the Hood 45 nm What Intel didn't tell you

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2003	UPC Solutions Manual
Jan. 11, 2008	VESA DisplayPort Standard - Version 1, Revision 1a
Jan. 5, 2010	VESA DisplayPort Standard - Version 1, Revision 2
Jan. 13, 2011	VESA DisplayPort Standard - Version 1.3
Aug. 8, 2011	VESA Embedded Display Port Standard 1.3
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	Violin 1010 Memory Appliance page
2008	Violin Scalable Memory Products page
2001	VLSI Memory Chip Design
2001	VLSI Memory Chip Design (“Itoh 2001”)
Aug. 22, 2011	Want to know more about the Micron Hybrid Memory Cube (HMC)
Feb. 18, 2005	World’s first USB to SATA bridge chip
Oct. 2011	ZIL Accelerator Random Write Revelation

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