

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Yuan et al.
U.S. Patent No.: 11,894,098 Attorney Docket No. 50095-0278IP1
Issue Date: February 6, 2024
Appl. Serial No.: 17/213,133
Filing Date: March 25, 2021
Title: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN
EMBEDDED DISPLAY PORT

DECLARATION OF DR. DAVID LIU

I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: February 10, 2026

By: 

David Liu, Ph.D.

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I, David Liu, Ph.D., declare that:

I. INTRODUCTION

1. I have been retained on behalf of Apple Inc. (“Apple”) to offer technical opinions related to U.S. Patent No. 11,894,098 (“the ’098 Patent”) (EX1001). I understand that Apple is requesting that the Patent Trial and Appeal Board (Board) institute an *Inter Partes* Review (IPR) proceeding of the ’098 Patent.

2. I have been asked to provide my independent analysis of the ’098 Patent in light of the prior art publications cited in this Declaration.

3. I am not and never have been an employee of Apple. I received no compensation for this Declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’098 Patent, the prior art publications cited below, and issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’098 Patent.

4. My analysis here is based on my years of education, research, and experience, as well as my investigation and study of relevant materials, including those cited in this Declaration.

5. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further,

I may consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

6. My analysis of the materials produced in this proceeding is ongoing, and I will continue to review any new material as it is provided. This Declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

7. My education and experience are described more fully in the attached curriculum vitae, attached as Appendix A to this declaration. For ease of reference, I have highlighted certain information below.

8. I am over the age of 18 and am competent to write this Declaration. I have personal knowledge or have developed knowledge—based upon education, training, or experience—of the technologies of the matters set forth herein.

9. My curriculum vitae (“CV”) is being filed concurrently as an appendix and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My CV also includes information about my expert witness experience, with case numbers where available.

10. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

11. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

12. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. ("TI"). At TI, my job responsibilities included process integration, device modeling, high-voltage complementary metal oxide semiconductor (CMOS) process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

13. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. ("AMD") where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5 μ m and 0.35 μ m Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology to accommodate x-decoder transistors and high-voltage transistors for negative gate erase operations. While at AMD, I was awarded a Spotlight Award for developing

a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

14. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

15. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

16. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm).

17. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

18. Since 2007, I have served as a technical consultant where I have provided expert advice regarding semiconductor memory technologies, including both DRAM and Flash memory technologies; CMOS process technology, and

semiconductor device physics. As part of this, I have considered, assessed, and assisted with the design of various different memory devices, both volatile memories and non-volatile memories, including NAND flash and monolithic 3D memory structures.

19. I hold over 99 U.S. patents, a vast majority of which are directly related to Nonvolatile memory device technology. For example, U.S. Patent No. 5,250,464 relates to use of sidewall layers of silicone dioxide and silicon nitride to form a sidewall anti-fuse structure.

20. In writing this Declaration, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- Prosecution History of the '098 Patent (EX1002)
- U.S. Patent Application Publication No. 2010/0290300 (“Takahashi”) (EX1004)
- U.S. Patent Application Publication No. 2012/0327726 (“Tsern”) (EX1005)
- U.S. Patent Application Publication No. 2010/0142247 (“Schuette”) (EX1006)
- U.S. Patent Application Publication No. 2012/0327062 (“Endo”) (EX1007)
- U.S. Patent Application Publication No. 2011/0063927 (“Dono”) (EX1008)
- U.S. Patent Application Publication No. 2012/0140578 (“Goto”) (EX1009)
- U.S. Patent No. 7,738,311 (“Youn”) (EX1010)

- Nakagome et al., “Review and future prospects of low-voltage RAM circuits,” IBM Journal of Research and Development, vol. 47, no. 5.6, p. 525-552 (2003) (EX1011)
- Keeth et al., DRAM Circuit Design: Fundamental and High-Speed Topics, IEEE Press (2008) (EX1012)
- “Low Power Double Data Rate 3 (LPDDR3),” JESD209-3, JEDEC Solid State Technology Association (May 2012) (EX1013)
- VESA Embedded DisplayPort Standard Version 1.3, Video Electronics Standards Association (January 2011) (EX1014)
- Craig Wiley, “The New Generation Digital Display Interface for Embedded Applications,” DisplayPort Developer Conference (2010) (EX1015)
- Prosecution History of U.S. Patent No. 10,998,017 (EX1016)
- Excerpts from Daintith et al., *A Dictionary of Computing, Sixth Edition*, Oxford University Press (2008) (EX1017)
- Excerpts from Harry Newton, *Newton’s Telecom Dictionary, 24th Edition*, Flatiron Publishing (2008) (EX1018)
- Excerpts from Downing et al., *Dictionary of Computer and Internet Terms, Tenth Edition*, Barron’s Educational Series, Inc. (2009) (EX1019)

- Itoh, *VLSI Memory Chip Design*, Springer Series in Advanced Microelectronics, Springer-Verlag Berlin Heidelberg New York (2001) (EX1020)
- Oct. 7, 2025 Complaint, *WeCrevention, Inc. v. Apple Inc.*, Civil Action No. 7:25-CV-458 (W.D. Tex) (EX1021)
- Micron Electronics, Inc., “DDR3 SDRAM” (2006) (EX1022)
- U.S. Patent No. 6,271,679 (EX1023)
- “DDR2 SDRAM Specification,” JESD79-2F, JEDEC Solid State Technology Association (November 2009) (EX1024)
- U.S. Patent Application Publication No. 2010/0061165 (EX1025)
- Jacob et al., *Memory Systems: Cache, DRAM, Disk*, Morgan Kaufmann Publishers (2008) (EX1026)
- Fairchild Semiconductor 74VCXH162244 datasheet (2005) (EX1029)
- Texas Instruments SN74AUP1G07 datasheet (2012) (EX1030)
- Wayne Wolf, *Modern VLSI Design: IP-Based Design*, Fourth Edition, Prentice Hall (2009) (EX1031)
- Barth et al., “A 45 nm SOI Embedded DRAM Macro for the POWER™ Processor 32 MByte On-Chip L3 Cache,” in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 64-75, Jan. 2011 (EX1032)
- J. Barth, “eDRAM to the Rescue,” SRC eDRAM (2009) (EX1033)

- U.S. Patent No. 7,626,883 (EX1034)
- U.S. Patent No. 6,847,578 (EX1035)
- U.S. Patent No. 8,901,009 (EX1036)
- U.S. Patent No. 8,471,362 (EX1037)
- U.S. Patent No. 7,829,410 (EX1038)
- U.S. Patent No. 7,892,943 (EX1039)
- U.S. Patent No. 8,148,763 (EX1040)
- U.S. Patent No. 7,736,987 (EX1041)
- The International Technology Roadmap for Semiconductors - Overall Roadmap Technology Characteristics (2003) (EX1043)
- Lee et al., “Tiered-latency DRAM: A low latency and low cost DRAM architecture,” 2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA) (EX1044)
- Harvard et al., “A scalable I/O architecture for wide I/O DRAM,” 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS) (EX1045)
- “VESA Publishes Embedded DisplayPort Standard Version 1.5,” <https://www.prnewswire.com/news-releases/vesa-publishes-embedded-displayport-standard-version-1-5--301410053.html/> (accessed Dec. 24, 2025) (EX1047)

- Gillingham, “Unleashing the Power of Embedded DRAM” (2005) (EX1048)
- AP Memory, AD351216F-x 512Mb LPDDR3, “512Mb LPDDR3 Specification” (2022) (EX1049)
- U.S. Patent Application Publication No. 2009/0080234 (EX1050)

21. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '098 Patent at the time of the earliest possible priority date of the '098 Patent, and I have done so during my review of these materials.

22. The '098 Patent has a filing date of March 25, 2021 and claims a priority date of July 17, 2012 (“the Critical Date”). Counsel has informed me that the Critical Date represents the earliest possible priority date to which the challenged claims of '098 Patent are entitled, and I have therefore used that Critical Date in my analysis below. I have not assessed whether the '098 Patent is entitled to the July 17, 2012 priority date.

23. I have no financial interest in the parties or in the outcome of this proceeding. I am being compensated for my work as an expert on an hourly basis. My compensation is not dependent on the outcome of these proceedings or the content of my opinions.

24. In writing this declaration, I have considered the following: my own knowledge and experience, including my work experience in electrical engineering

and memory development, and my experience in working with others involved in those fields. In addition, I have analyzed various publications and materials, in addition to other materials I cite in my declaration.

25. My opinions, as explained below, are based on my education, experience, and expertise in the fields relating to the '098 Patent. Unless otherwise stated, my testimony below refers to the knowledge of one of ordinary skill in the art as of the Critical Date, or before. Any figures that appear within this document have been prepared with the assistance of Counsel and reflect my understanding of the '098 Patent and the prior art discussed below.

III. SUMMARY OF CONCLUSIONS FORMED

26. This declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions, based upon my knowledge and experience and my review of the prior art publications listed above, I believe that:

- Claims 1-9 are anticipated by, and obvious in view of, Takahashi
- Claims 3-9 are obvious over Takahashi, Tsern, and Schuette
- Claims 6-9 are obvious over Takahashi and Endo
- Claims 6-9 are obvious over Takahashi, Tsern, Schuette, and Endo
- Claims 1-9 are obvious over Dono and Goto
- Claims 1-9 are obvious over Dono, Goto, and Youn
- Claims 6-9 are obvious over Dono, Goto, and Endo

- Claims 6-9 are obvious over Dono, Goto, Endo, and Youn

IV. LEVEL OF ORDINARY SKILL IN THE ART

27. In my opinion, a person of ordinary skill in the art as of the Critical Date of the '098 Patent (hereinafter a "POSITA") as of July 17, 2012 would have had at least a master's degree in electrical engineering, or a comparable field, and at least two years of professional experience working with semiconductor memory, including DRAM. Additional years of experience could substitute for an advanced-level degree (and vice versa).

28. Based on my experiences, I have a good understanding of the capabilities of one of ordinary skill. Indeed, I have worked closely with many such persons over the course of my career. From my industry experience, I am familiar with what a skilled person would have known and found predictable in the art. Furthermore, I possess those capabilities myself.

V. TECHNOLOGY BACKGROUND AND SUMMARY OF THE '098 PATENT

A. Technology Background

29. Dynamic random-access memory (DRAM) is the key memory component of modern computing systems, being "relatively large, relatively fast, and relatively cheap." EX1026, 38. While read-only memory (e.g., EEPROM) is used for firmware and other specialized tasks, non-volatile memory (e.g., flash memory) is used for long-term storage, and static random-access memory (SRAM)

is used for specialized memory tasks (e.g., cache memory), DRAM is used as the “main memory” workhorse. EX1026, 40. For example, DRAM is typically used to store data for currently-operating software.

30. The '098 Patent relates to both DRAM and to another technology: embedded display port interfaces.

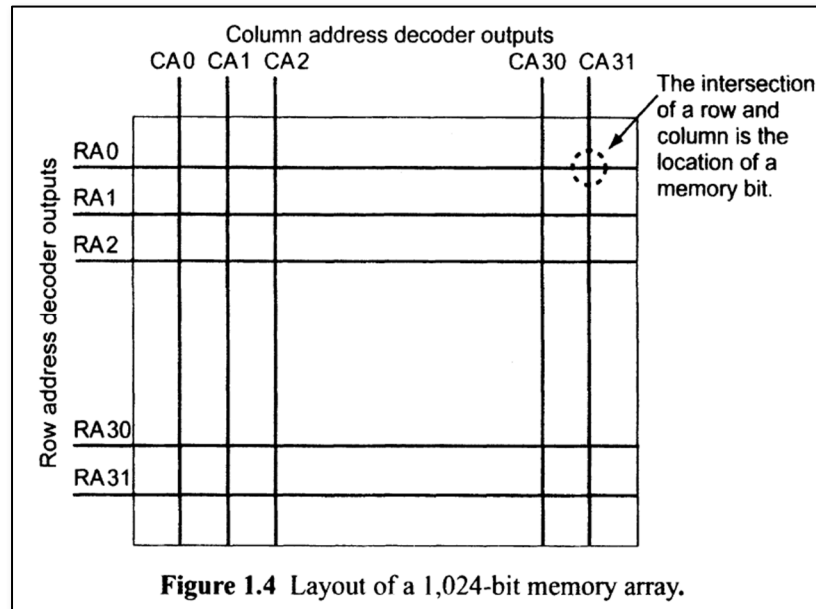
1. DRAM

31. As discussed above, DRAM is a type of random access memory typically used as the primary memory of computing devices. In a DRAM device, memory cells are organized in an array. Each memory cell has a “row” position and a “column” position with which the memory cell can be addressed. EX1012, 16-18. “By identifying the intersection of a row and a column (by specifying a row address and a column address to the DRAM), a memory controller can access an individual storage cell inside a DRAM chip so as to read or write the data held there.” EX1026, 352.

32. Voltages can be applied to “wordlines” (corresponding to a row) and “bitlines” (corresponding to a column) to store a 0 or 1 in a target memory cell, or to read out stored data. EX1012, 17-24. The 0 or 1 is represented by a charge stored (or not stored) on a capacitor in each cell. EX1026, 355.

33. DRAM is referred to as “dynamic” because, once stored in a cell, charge (representing data) will “leak off over time.” EX1012, 20. To prevent loss

of data, a “refresh” operation is performed periodically. EX1012, 19. That is, “capacitors storing electrons are not perfect devices, and their eventual leakage requires that, to retain information stored there, each capacitor in the DRAM must be periodically refreshed (i.e., read and rewritten).” EX1026, 351.



EX1012, FIG. 1.4

34. A DRAM device is provided with one or more external voltages, which may be converted to internal voltages supplied to various circuits of the device. The external voltages are typically supplied through pins, or solder balls, that connect a DRAM chip to a host device. EX1013, 6-10. The Low Power Double Data Rate 3 (LPDDR3) standard, published in May 2012 by the Joint Electron Device Engineering Council (JEDEC), defines several external voltages, including V_{DD1} , V_{DD2} , and V_{DDQ} . EX1013, 83; EX1049, 23. The DDR3/LPDDR3 standard was the most recent DDR SDRAM standard as of 2012, with DDR

synchronous dynamic random-access memory (SDRAM) itself being the dominant DRAM type. EX1026, 500, 506-512.

35. The '098 Patent states that it improves DRAMs by specifying lower voltages for memory circuitry. EX1001, 4:61-64. Specifically, the '098 Patent describes that DRAMs can have “operation voltages” of “<1.1 V” for each of a “memory core unit,” a “peripheral circuit unit,” and an “input/output unit.” EX1001, Table II. These voltages are slightly lower than the external voltages specified by the LPDDR3 standard: LPDDR3 describes minimum values of 1.7V for VDD1, 1.14V for VDD2, and 1.14V for VDDQ. EX1013, 83. According to the '098 Patent, this results in “power consumption [that]...is much lower than power consumption of the [DRAM] operating in the operation voltages specified by the [JEDEC].” EX1001, 4:6-10.

36. The '098 Patent provides no technical detail on how these low voltages might be achieved. For example, the '098 Patent does not discuss circuit design on a level lower than a “unit” (e.g., “memory core unit”), does not discuss circuit layouts or transistor types, does not discuss voltage conversion or generation, etc. EX1001. Based on my technical experience with memories, this is a glaring omission, to the extent that I cannot identify any technical contributions of the '098 Patent. The desire for low-voltage circuit operation, including for DRAM, was not new. Indeed, the move to lower and lower voltages was key to the

implementation of Moore's Law for decades from the 1970s to the 2010s: smaller and smaller transistors were able to switch faster and at lower voltages, enabling faster computation speeds and lower power consumption for a given number of transistors, and enabling more transistors overall. The challenge, and the focus of research, was to make low voltage operation feasible (e.g., through development of materials, transistor design, system design, fabrication methods, and the like), not to propose low voltage operation in the first place. Indeed, voltages within the ranges recited by the '098 Patent had been a subject of research for decades, and low-voltage DRAM circuits had been successfully manufactured and publicized. EX1011; EX1043. For example, 2003's "International Technology Roadmap For Semiconductors," an industry report predicting future semiconductor development, noted low-power V_{dd} (supply voltage) of 1.0 in 2003, predicted high-performance V_{dd} of 1.0V (lower than the '098 Patent's limits) by 2008, and targeted V_{dd} of 0.5V by 2016. EX1043, 22.

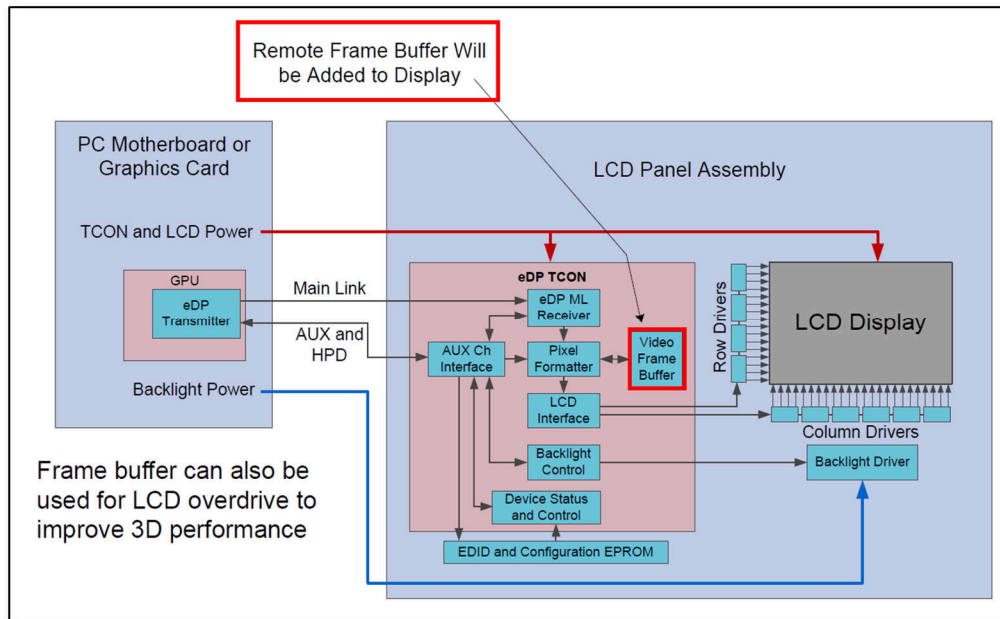
37. Unlike the '098 Patent, the prior art I have reviewed for preparation of this Declaration provides not only *disclosure* of low DRAM voltages, but also details on *how the low voltages may be successfully used in real DRAM circuits*, including discussion of specific circuit topologies, transistor types, DRAM layouts, and voltage generation and relative levels.

2. Embedded Display Port

38. The embedded display port (eDP) (or “Embedded DisplayPort”) standard “defines requirements and options of a standardized display panel interface for embedded display applications.” EX1014, 12. eDP interfaces are widely used in laptops, tablets, and other portable devices. EX1047.

39. Version 1.3 of the eDP standard, published in 2011, introduces a “panel self-refresh” (PSR) feature. EX1014, 12, 21, 65. According to eDP 1.3, a display device’s “timing controller” (TCON) includes a “remote frame buffer” (RFB). EX1014, 27, 65; EX1015, 24. The RFB is integrated into the “LCD Panel Assembly,” that is, into a display device. EX1015, 24. The RFB “can maintain [a] display image without receiving video data from [the] GPU [graphical processing unit].” EX1015, 25. This means that, when an eDP 1.3 display is showing a still (or static) image, the GPU can “enter a low power state...[a]llowing the GPU to power down between display updates.” EX1015, 25. Instead of using the GPU, the display can draw the static image from the RFB, reducing power consumption. EX1015, 26.

40. The below annotated figure from EX105 shows the remote frame buffer (“Video Frame Buffer”) in the eDP timing controller of an “LCD Panel Assembly.”



EX1015, 24

41. The '098 Patent states that “power consumption of the timing controller is increased due to operation of the frame buffer,” and therefore seeks “to design the frame buffer to reduce the power consumption.” EX1001, 1:58-61. According to the '098 Patent, “the operation voltages specified by [JEDEC] can not satisfy requirements (that is, the lower operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3.” EX1001, 3:22-27.

42. The '098 Patent does not describe what these “requirements” are. Based on my review, the eDP 1.3 standard in fact includes no such power requirements (e.g., “lower operation power consumption and the low standby power consumption”). Detailed discussion on this point is provided below in §VII.A.2(f).

43. Nevertheless, the '098 Patent asserts that “power consumption of the [DRAM] of the present invention is much lower than power consumption of a [DRAM] operating in the operation voltages specified by [JEDEC],” and that “when the [DRAM] of the present invention is applied to an embedded display port, the present invention can make system power consumption...be significantly reduced.” EX1001, 4:64-5:6.

B. Summary of the Prosecution History of the '098 Patent

44. The '098 Patent was issued on February 6, 2024 as a continuation of U.S. Patent No. 10,998,017 (“the '017 Patent”).

45. The parent '017 Patent received five rounds of rejections. EX1016, 37-43, 84-91, 120-129, 159-166, 188-195. Most of these rejections were over “Mohammad” (US 2009/0122620), in several cases in combination with Takahashi (EX1004). *Id.* The final rejection was over Takahashi, without requiring the additional citation of Mohammad. *Id.* The claims of the '017 Patent were allowed after the applicant amended the sole independent claim to recite that “the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP),” and the Examiner also cited this feature in the Reasons for Allowance. EX1016, 12, 28. A related claim element is found in independent claim 6 of the '098 Patent. The obvious inference is that the claims of the '017 Patent were allowed because of this “eDP” feature.

46. I have reviewed relevant portions of the prosecution history of the '017 Patent. EX1016. Despite the “eDP” feature being the apparent reason for allowance of the '017 Patent over Takahashi, the prosecution history does not clarify what voltages would be “capable of making the DRAM be applied to an embedded display port (eDP).” Nor does the prosecution history of the '098 Patent shed light on this feature. EX1002. For example, claim 6 of the '098 Patent recites that “the DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP),” but claim 6 does not require the first voltage to be lower than 1.1V (this feature is found in claim 7). In fact, the eDP 1.3 standard cited by the '017 and '098 Patents includes no voltage or power requirements for a memory applied to an eDP. *See* §VII.A.2(f). Thus, the cited DRAMs—including Takahashi’s, as discussed below—were entirely “capable of being applied to an [eDP].”

47. The '098 Patent was allowed over Takahashi and Mohammad after three office actions. EX1002, 10-17, 74-91, 130-138, 162-172. The allowance appears to have been based on a key oversight by the Examiner. Specifically, the Examiner cited Takahashi’s power supply voltage VDD for each of the “first voltage” and the “second voltage” of the claims, leading the Examiner to mistakenly conclude, in the Notice of Allowance, that the art did not teach “the second voltage...is different from the first voltage.” EX1002, 15, 79-80. The

Examiner appears to have overlooked Takahashi's *other* supply voltage, VPPL, which is different from VDD, is less than 1.1V, and is supplied to memory cells which operate based on VPPL, thereby teaching the "first voltage" of the claims. EX1004, [0083]-[0084], FIGS. 7-8. VPPL does not appear to have been discussed at any point during prosecution of the '098 Patent.

48. In Grounds 1A-1D below, Takahashi's VPPL is applied as the first voltage and VDD is applied as the second voltage. Based on my analysis, the Examiner should have recognized the relevance of VPPL and applied it in this manner.

49. The Examiner also suggested that the allowance was issued due to the recitation that the "third voltage is different from the first voltage." EX1002, 15. See claim 6, which recites a "first voltage [] greater than the third voltage," without reciting a "second voltage." EX1001, 6:25-41.

VI. SUMMARY OF THE PRIOR ART

50. In my opinion, claims 1-9 of the '098 Patent are anticipated and/or obvious in view of combinations of the references that I have listed above. All cited references are in the same field of endeavor (e.g., DRAM) as the '098 Patent. EX1001, 2:19-35; EX1004, [0018]; EX1005, [0005]; EX1006, [0003]; EX1007, [0035]; EX1008, [0024]; EX1009, [0022]; EX1010, 5:49-67. Further, the cited references are pertinent to problems the '098 Patent was trying to solve. For

example, like the '098 Patent, Endo addresses how to apply DRAM to eDP 1.3. EX1001, 2:19-35; EX1007, [0034]-[0035]. Like the '098 Patent, Takahashi, Tsern, Schuette, Dono, and Goto address voltage reduction and/or power reduction in DRAM. EX1001, 4:39-60; EX1004, [0045], [0082]-[0083]; EX1005, [0005], [0019]; EX1006, [0014], [0029]; EX1008, [0005]-[0007]; EX1009, [0027]. Like the '098 Patent, Youn addresses forming DRAM components on a single chip. EX1001, 5:32; EX1010, 5:49-67.

VII. PRIOR ART ANALYSIS

A. [Ground 1A] Takahashi Anticipates and Renders Obvious Claims 1-9

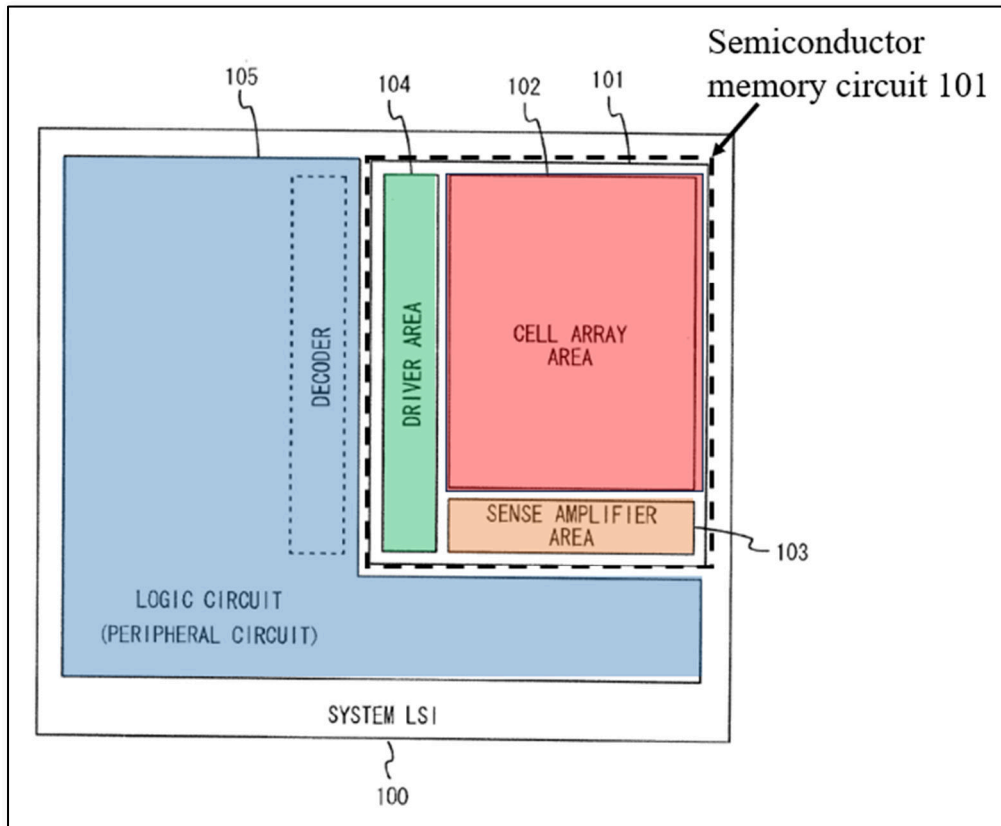
1. Takahashi

51. Takahashi describes a “built-in DRAM” that can provide “higher speed operation.” EX1004, [0021], [0047]. I interpret “built-in” as likely referring to an “embedded” DRAM, as discussed in further detail below in §VII.A.2(c).

52. As shown in Takahashi’s FIG. 1 (reproduced below), Takahashi’s “semiconductor integrated device 100” includes a “semiconductor memory circuit 101” and a “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit.” EX1004, [0047], [0078]. The semiconductor memory circuit 101 includes “a cell array area 102, a sense amplifier area 103, and a driver area 104.” EX1004, [0047]. Although Takahashi labels the logic circuit 105 separately from the “semiconductor memory circuit 101,” it was well-established that DRAM

peripheral circuitry—and, in particular, peripheral circuitry performing a specific memory function, such as a decoder—would be considered part of the DRAM.

This is discussed in more detail below for [1.6] in §VII.A.2(a).

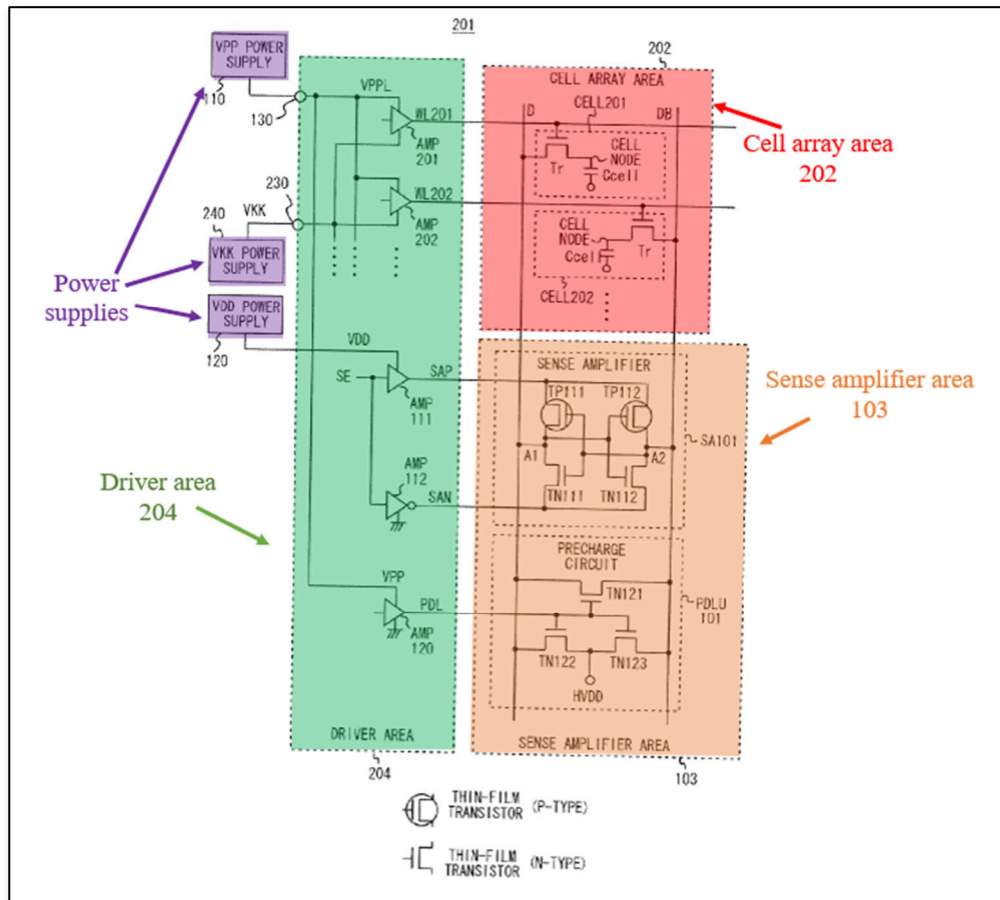


Takahashi, FIG. 1

53. Takahashi’s FIG. 7 (reproduced below) shows a circuit configuration of a semiconductor memory circuit 201 similar to that of FIG. 1. EX1004, [0077]-[0079]. FIG. 7 illustrates a “second exemplary embodiment” that “differs from the semiconductor device of the first exemplary embodiment [FIG. 1] in the configuration of a semiconductor memory circuit portion... the semiconductor

integrated device 200 of the second exemplary embodiment has a configuration in which the semiconductor memory circuit 101 of the semiconductor integrated device 100 shown in FIG. 1 is replaced with the semiconductor memory circuit 201.” EX1004, [0077]. That is, the second embodiment has the overall configuration shown in FIG. 1, with a different semiconductor memory circuit.

54. Power to a cell array area 202, a sense amplifier area 103, and a driver area 204 is supplied by a VPP power supply 110, a VKK power supply 240, and a VDD power supply 120. EX1004, [0081]-[0083], FIG. 7. These power supplies output voltages VPPL, VKK, and VDD, respectively. EX1004, [0081]-[0083], FIG. 7. VDD is also provided to the logic circuit 105 as the “power supply voltage VDD of the logic circuit 105.” EX1004, [0045]-[0046]. FIG. 8 illustrates that VDD is also supplied to the cell array area 202, on the bitline D. EX1004, FIGS. 7-8.



Takahashi, FIG. 7

55. In connection to the second embodiment of FIGS. 7 to 10B (which has an overall chip structure shown in FIG. 1), Takahashi provides specific values for these voltages: “the power supply voltage VDD is 0.8 V, the voltage VPPL is 1.0 V, and the voltage VKK is -0.3 V.” EX1004, [0084].

2. Analysis of claims

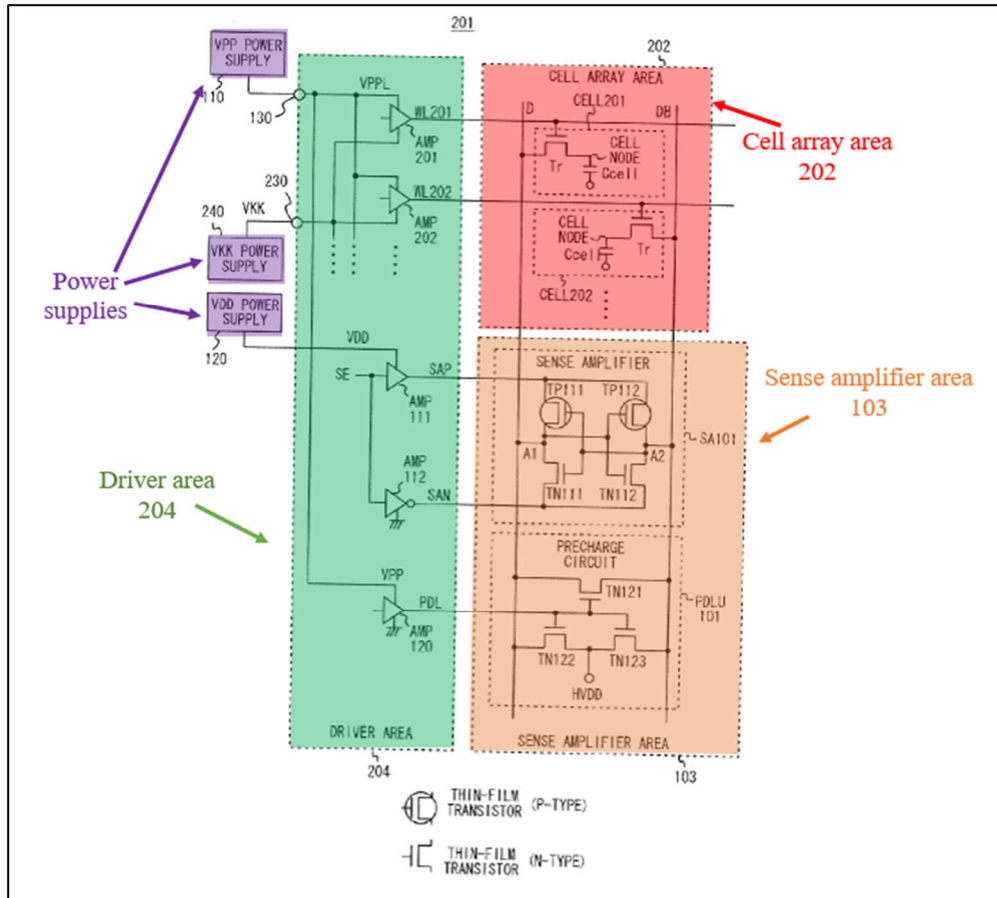
56. For the reasons below, claims 1-9 are anticipated by, or at least obvious over, Takahashi.

(a) *Claim 1*

[1.1]: A dynamic random access memory (DRAM), comprising:

57. Takahashi's "semiconductor memory circuit 201 is a built-in DRAM of a system LSI." EX1004, [0078]. Thus, Takahashi discloses a DRAM.

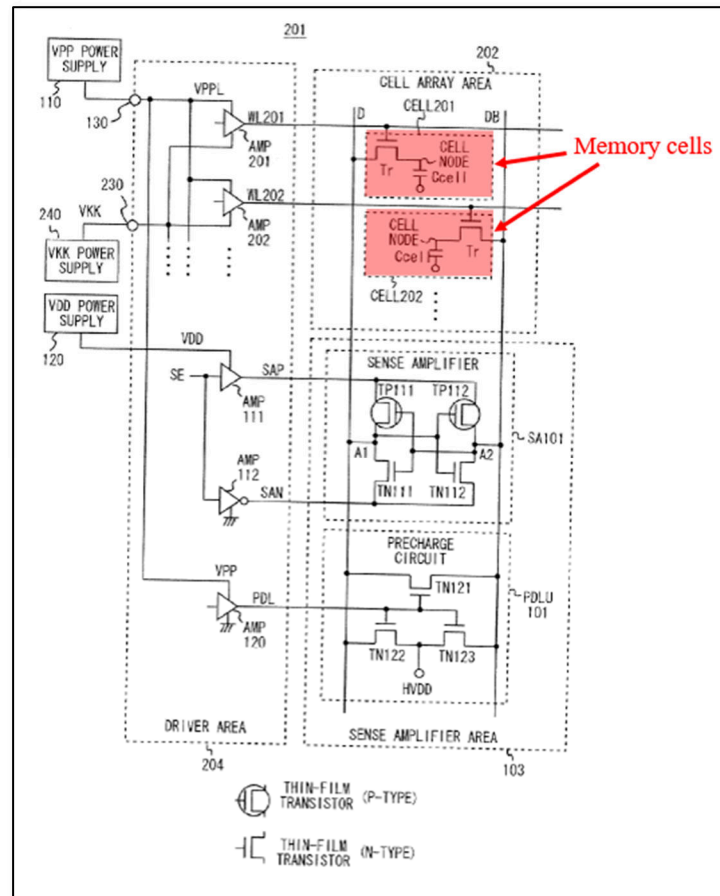
58. In more detail, and as shown in Takahashi's FIG. 7 (reproduced below), Takahashi's DRAM semiconductor memory circuit 201 includes a sense amplifier area 103, a driver area 204, and a cell array area 202 that includes memory cells. EX1004, [0077]-[0083], FIG. 7. Cell array area 202 is supplied by a VPP power supply 110, a VKK power supply 240, while sense amplifier area 103 and driver area 204 are supplied by a VDD power supply 120. EX1004, [0081]-[0083], FIG. 7. VDD is also supplied to the cell array area 202 through bitline D. EX1004, FIGS. 7-8.



Takahashi, FIG. 7

[1.2]: a DRAM core cell comprised in the DRAM,

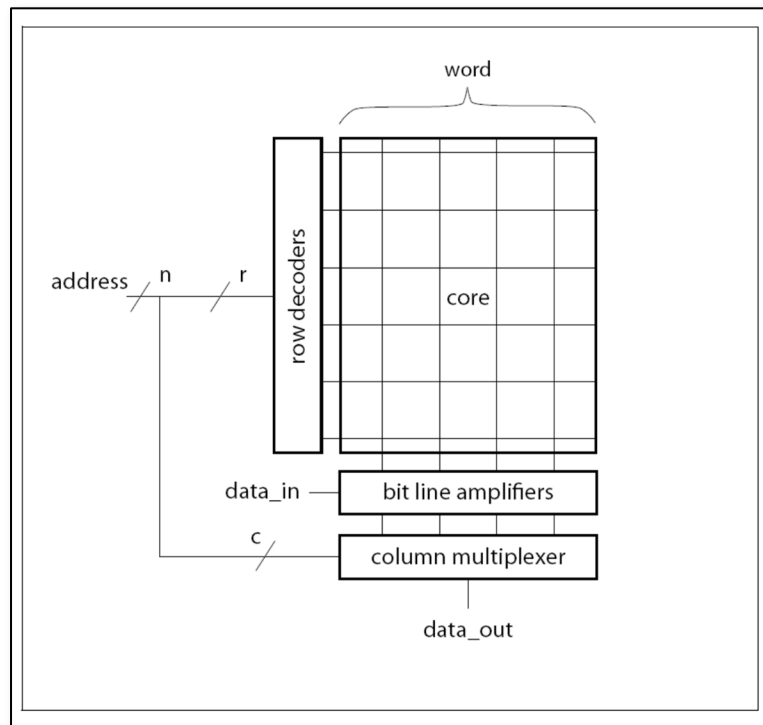
59. A POSITA would have understood and found obvious that the “memory cells” in Takahashi’s DRAM are DRAM core cells. EX1004, [0079]-[0080]. For example, Takahashi discloses that the “semiconductor memory circuit 201 includes a cell array area 202... The cell array area 202 includes multiple memory cells CELLS.” EX1004, [0079]-[0080].



Takahashi, FIG. 7

60. A POSITA would have understood that these DRAM memory cells are each a “DRAM core cell.” The “core” in “DRAM core cell” refers to, or at least encompasses, the cell array of a memory, which performs the memory’s data storage function. “Core” by itself can sometimes have a broader meaning, encompassing, in addition to the cells themselves, closely associated circuitry such as sense amplifiers and/or decoders. But a DRAM memory cell would be understood unambiguously as a DRAM core cell.

61. For example, the textbook *Modern VLSI Design: IP-Based Design* provides the below diagram in which the memory cell array (indicated by a grid) is labeled as a “core.” EX1031, 385. The same textbook also refers to the “memory core” and refers to a DRAM data storage cell as a “RAM core cell.” EX1031, 385, 391-392.



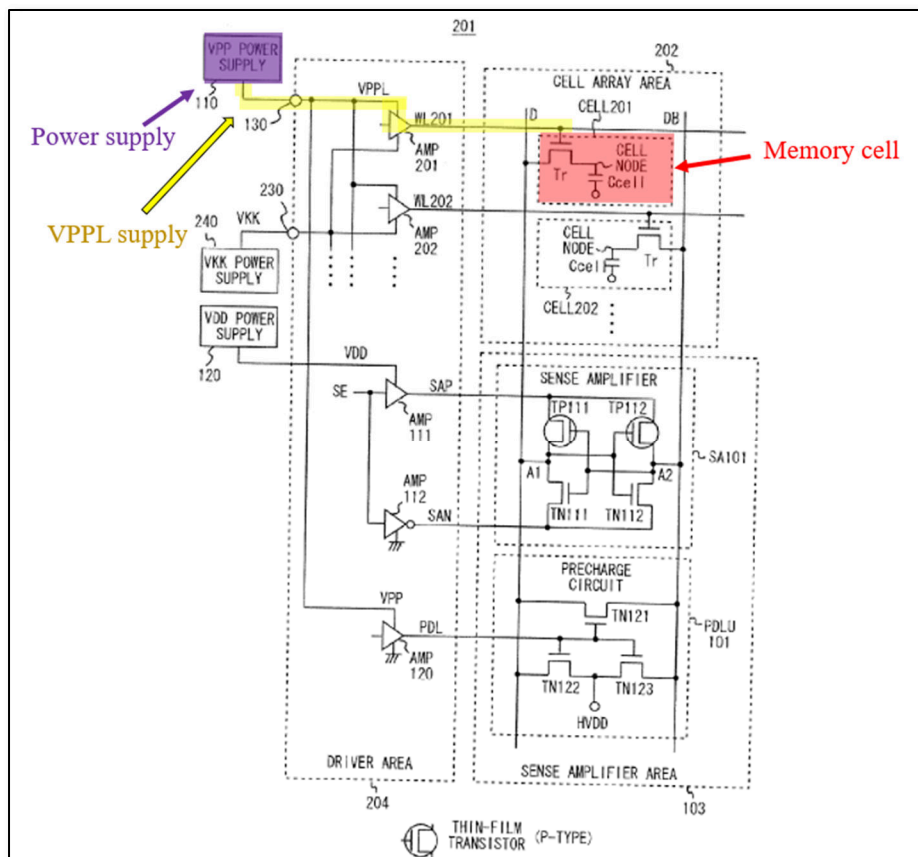
EX1031, Figure 6-16

62. As another example, a 2005 article on embedded DRAM refers to “core circuitry of a DRAM, including cells, sense amplifier, and datapath,” and the illustration of this “core circuitry” includes a “cell array” like that disclosed in Takahashi. EX1048, 2-3, FIG. 1.

[1.3]: wherein the DRAM core cell is supplied with a first voltage within a

first voltage range to make the DRAM core cell operate at the first voltage,

63. Takahashi's memory cells are supplied with a first voltage VPPL to make those cells operate at that voltage. Takahashi describes that "the memory cells ...use a voltage VPPL, which is supplied from the VPP power supply 110." EX1004, [0081. Supply of VPPL to memory cells is performed through the transmission path shown below. EX1004, FIG. 7. Specifically, VPPL is supplied from the VPP power supply 110, through a terminal 130 through an amplifier AMP201, and to a wordline WL201, which is connected to a gate of a transistor TR. EX1004, FIG. 7.

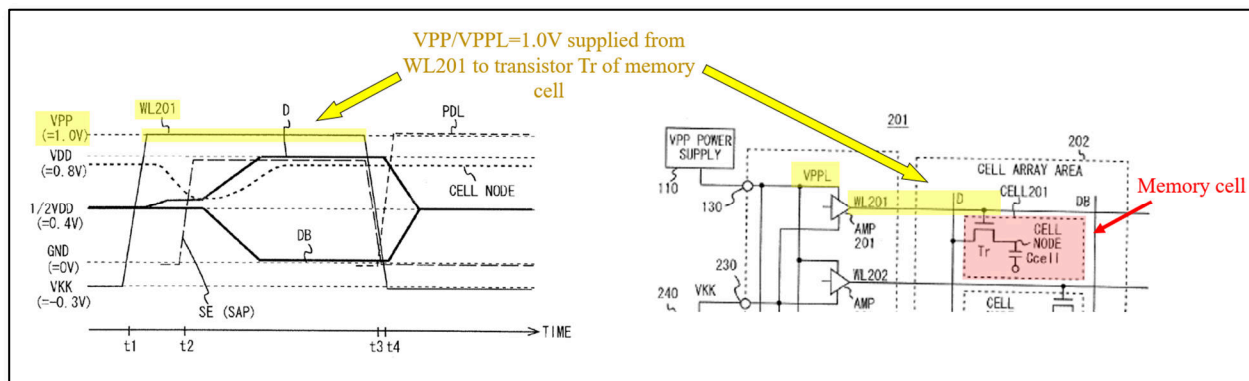


Takahashi, FIG. 7

64. In the context of FIGS. 7 to 10B (Takahashi's "second exemplary embodiment"), Takahashi sometimes refers to "VPP" instead of "VPPL." *See* [0085] and [0088], and FIG. 8. A POSITA would have recognized this as an error, and would have recognized that Takahashi intended to refer to "VPPL" only. Takahashi is clear that the "second exemplary embodiment" uses VPPL instead of VPP, as a lower-voltage version of VPP. *See*, e.g., [0081] ("Unlike the first exemplary embodiment, the memory cells of the second exemplary embodiment use a voltage VPPL"), [0082] ("the VPP power supply 110 supplies the voltage VPPL, which is lower than the voltage VPP of the first exemplary embodiment"), FIG. 7 (showing provision of only VPPL, not VPP) and FIG. 8 (showing a wordline WL201 driven to a value of "1.0V", matching with the disclosed value of VPPL, not the disclosed value of VPP). EX1004, [0084]. In view of this and other disclosure in Takahashi, and in agreement with my analysis below, a POSITA would have interpreted the erroneous references to "VPP" in the context of FIGS. 7 to 10B as referring to VPPL=1.0V.

65. Supply of the first voltage VPPL to a memory cell is shown explicitly in Takahashi FIG. 8. As shown below, "at the time t1, the word signal WL201 rises to the voltage VPP [=1.0 V]." EX1004, [0084]-[0085], FIG. 8. The wordline 201 is connected to a gate of the transistor Tr of the memory cell 201, such that a first voltage of 1.0 V is supplied to the memory cell. EX1004, [0083]-[0085], FIG. 8.

FIG. 7 illustrates the transistor gate as being connected directly to the wordline, such that the wordline voltage is supplied directly to the memory cell.



Left: Takahashi, FIG. 8; Right: Takahashi, FIG. 7 (partial)

66. Based on this provision of VPPL, a POSITA would have understood and found obvious that the memory cell “use[s],” or operates at, the “voltage VPPL.” EX1004, [0081]. For example, based on provision of VPPL to the memory cell, “the gate transistor of the memory cell CELL 201 is turned on.” EX1004, [0085]. That is, the memory cell operates at VPPL by receiving VPPL and switching its state (e.g., connected to the bitline or disconnected from the bitline) directly in response to VPPL. When the gate transistor is turned on, the capacitor “Ccell” of the memory cell becomes connected to the bitline D, such that data programming and readout can be performed.

67. Although claim 1 recites that the first voltage is “within a first voltage range,” neither this nor other claims place any limit on the “first voltage range,” or even refer to it again. The recitation of the “first voltage range” does not appear to

place any limits on the first voltage, and the first voltage range does not appear connected to any particular technical effect.

68. There are multiple possible interpretations of “within a first voltage range” (and other voltage ranges recited in the claims). One interpretation is that the “first voltage range” is any range that the first voltage must be within. According to this interpretation, a POSITA would have understood and found obvious that the “first voltage range” is any range that includes the disclosed $VPPL=1.0V$ value, for example, 0.5-1.5 V, or 0-20 V, because $VPPL=1.0V$ is “within” any such range.

69. Another interpretation is that the “first voltage range” refers to a range of possible variation in the first voltage. According to this interpretation, a POSITA would have understood and found obvious that the voltage $VPPL$ is “within a first voltage range” due to standard voltage variation. In practice, although practitioners in the art often refer to voltages as having a specific value, every voltage is defined or provided within a range. The range—which might be very small—is attributable to non-idealities such as temperature dependence, device-to-device variation, load dependence, and the like. Correspondingly, most devices are designed to tolerate variations in voltages, including power supply voltages. For example, Micron’s “DDR3 SDRAM” standard calls for VDD in a range from 1.425V to 1.575V. EX1022, 40. And Takahashi itself describes $VPPL$

as being “reduced to about 1.0V,” where “about” might refer to a small level of expected variation. EX1004, [0083]. This small variation—which a POSITA would have understood to exist for essentially any voltage—would have been understood by a POSITA as a “first range” that the first voltage VPPL is within.

[1.4]: *and the DRAM core cell is a volatile memory cell,*

70. A POSITA would have understood and found obvious that Takahashi’s DRAM (dynamic random access memory) core cell is, by definition, a volatile memory cell. That is, as a POSITA would have known, *all* DRAM memory cells are volatile memory cells, because all DRAM memory cells require power to maintain stored data, in contrast to non-volatile storage (e.g., flash storage) that can retain stored data even without power.

71. For example, *A Dictionary of Computing* describes “dynamic memory” as a “form of volatile semiconductor memory in which stored information is degraded with time. The most common example is dynamic RAM (usually abbreviated to DRAM).” EX1017, 4-5. *Newton’s Telecom Dictionary* states that “DRAM must be continually refresh to retain its data,” that “[d]ynamic memory requires a continuous electrical current,” and that “volatile storage” is “[c]omputer storage that is erased when power is turned off. RAM is volatile storage.” EX1018, 3-5. The *Dictionary of Computer and Internet Terms* states that “[t]he memory (RAM) of a computer is volatile” and defines DRAM as “a

computer memory that requires a refresh signal to be sent to it periodically,” i.e., because it is volatile. EX1019, 3-4.

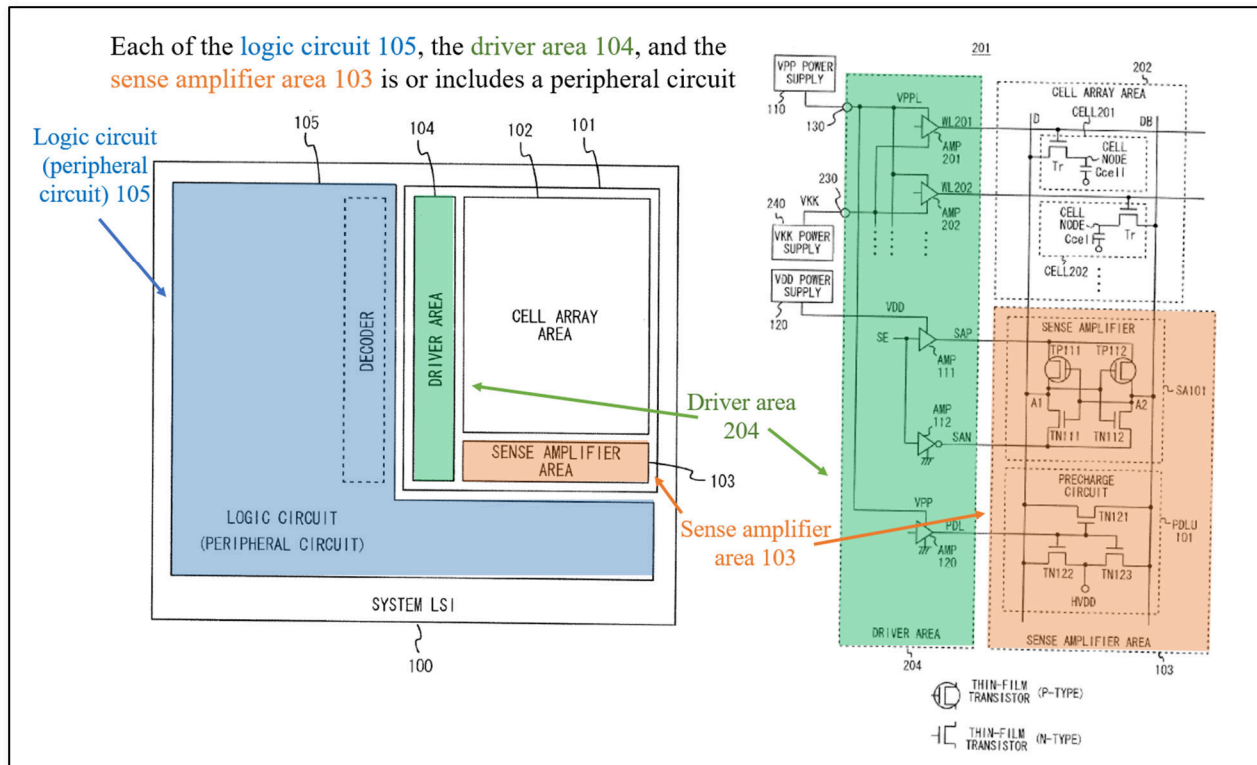
[1.5]: wherein the first voltage is lower than 1.1 V; and

72. Takahashi discloses that the first voltage VPPL is 1.0 V, which is lower than 1.1 V. *See* Takahashi [0083] (“the voltage VPPL supplied from the VPP power supply 110 can be reduced to about 1.0V”). EX1004, [0083]-[0084].

Takahashi FIG. 8 similarly shows the wordline WL201 being supplied with “1.0V.” EX1004, FIG. 8.

[1.6]: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell,

73. Takahashi discloses and renders obvious a peripheral circuit electrically connected to the DRAM core cell. According to the applicant’s proposed definition of “peripheral circuit” in the context of Takahashi, peripheral circuits electrically connected to the DRAM core cell include the “sense amplifier area 103” (e.g., “sense amplifier SA101”), the “driver area 204” (e.g., driver amplifier AMP111), and at least a portion of the “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201.” EX1004, [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7.



Left: Takahashi, FIG. 1; Right: Takahashi, FIG. 7

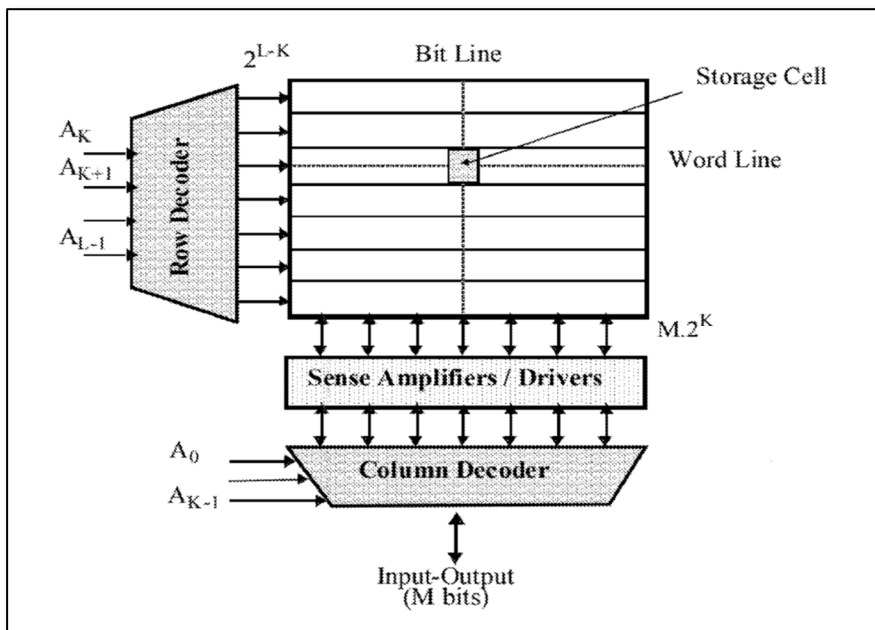
74. In determining that the sense amplifier area 103 and the driver area 204 are peripheral circuits, I am following examples provided by the applicant in reference to Takahashi. Specifically, during prosecution of Patent No. 10,998,017, the parent patent to the '098 Patent, the applicant argued to the examiner that drivers and sense amplifiers are “peripheral circuits.” These arguments were made while attempting to argue that Takahashi’s logic circuit 105 was not the claimed peripheral circuit. The applicant argued:

storage cell of the reference figure can be just referred to the memory core unit of the present invention, and **row decoder, sense amplifiers/drivers, and column decoder of the reference figure can be just referred to the peripheral circuit unit 104 of the present**

invention. Therefore, according to the reference figure, although paragraph [0078] of Takahashi discloses “the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201”, it is obvious that **the logic circuit 105 is not row decoder, sense amplifiers/drivers, and column decoder (shown in the reference figure) in the array-structured memory, so according to the reference figure, the logic circuit 105 of Takahashi still cannot be referred to the peripheral circuit** of the present invention.

EX1016, 72-73 (emphasis added).

75. The applicant also provided the following diagram (taken from a University of Utah webpage) which illustrates a “Row Decoder”, “Sense Amplifiers/Drivers” and a “Column Decoder.” EX1016, 73. The applicant suggested that, based on this diagram, these elements are peripheral circuits. EX1016, 72-73.



EX1016, 73 (taken from University of Utah webpage)

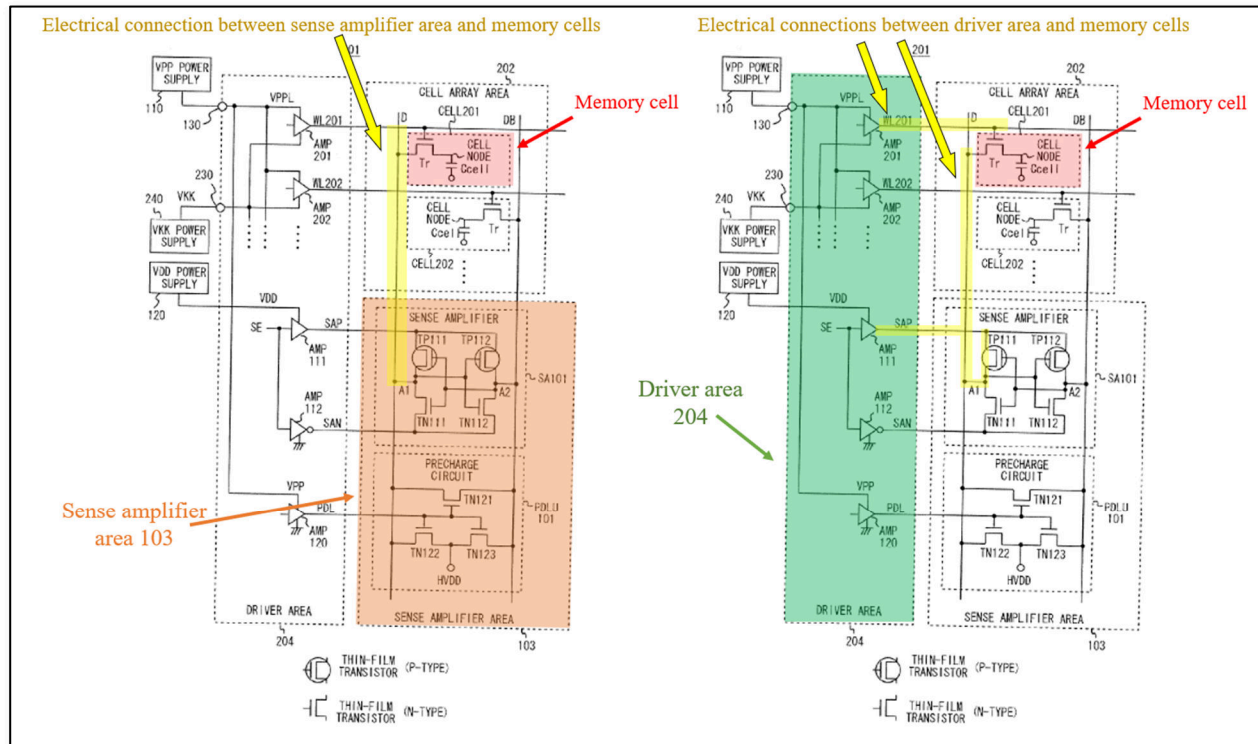
76. Thus, following the applicant’s own definition, a POSITA would have understood and found obvious that the circuitry of Takahashi’s driver area 204 (e.g., amplifier AMP111) and the sense amplifier area 103 (e.g., sense amplifier SA101) are peripheral circuits. *See* EX1016, 70-74. This understanding agrees with the plain and ordinary meaning of “peripheral circuit” as a POSITA would have understood it. *See*, e.g., the citation of EX1020 in §VII.E.4(a) below.

77. In addressing claims 1 and 2 in this ground (e.g., in mapping Takahashi to elements of the claims), I have followed the foregoing interpretation of Takahashi’s driver area 204 (e.g., amplifier AMP111) and the sense amplifier area 103 (e.g., sense amplifier SA101) as peripheral circuits.

78. Further, these circuits are electrically connected to the DRAM core cell (memory cells). As shown in FIG. 7, the sense amplifier area 103 is

electrically connected to the memory cells through, e.g., a bitline D, and the driver area 204 is electrically connected to the memory cells through, e.g., wordline WL201, sense amplifier control line SAP, sense amplifier SA101, and bitline D.

EX1004, [0007], [0009], [0081], [0086], FIG. 7.



Takahashi, FIG. 7

79. A POSITA would have also understood and found obvious that at least a portion of the “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201” is also a peripheral circuit. EX1004, [0078]. Takahashi explicitly denotes it as such, and the ’098 Patent includes no definition of “peripheral circuit” that would exclude it.

80. During prosecution of the '017 and '098 Patents, the applicant argued against any portion of the logic circuit 105 being interpreted as a peripheral circuit. EX1002, 39, 156-158; EX1016, 72-74. For example, the applicant argued that the DRAM of Takahashi is limited to the “semiconductor memory circuit 201,” such that the logic circuit 105, which is illustrated separately from the semiconductor memory circuit 201, could not be considered a “peripheral circuit comprised in the DRAM.” EX1016, 70-71. This reasoning is faulty for several reasons. First, as illustrated by Takahashi, the semiconductor memory circuit 201 includes only a cell array, a driver area, and a sense amplifier area. EX1004, FIGS. 1, 7. However, a POSITA would have understood that a DRAM would almost certainly include other circuits, such as buffers, decoders, control logic, and the like. More-complete DRAM diagrams are shown, for example, in Tsern FIG. 5 and Dono FIG. 1. EX1005, FIG. 5; EX1008, FIG. 1. The applicant’s attempted limiting of the “DRAM” of Takahashi to only the semiconductor memory circuit 201 (that is, to only the cell array, sense amplifiers, and drivers) would exclude all of these elements, an interpretation entirely incompatible with how a POSITA would have delimited a DRAM. *See, e.g.,* EX1005, FIG. 5; EX1008, FIG. 1; EX1009, FIG. 2; EX1010, FIG. 6; EX1012, Chapters 3-6. In line with this understanding, the Examiner properly continued applying the “logic circuit (peripheral circuit)” as a

peripheral circuit throughout prosecution, never conceding to the applicant's position (*see, e.g.,* EX1002, 15, 62; EX1016, 40, 42).

81. In addition, in the block quote above, the applicant explicitly defined a “decoder” as a peripheral circuit, and Takahashi describes that the logic circuit includes “an address decoder of the semiconductor memory circuit.” EX1004, [0044], FIG. 1. As such, by the applicant's own definition provided during prosecution with respect to Takahashi, at least a portion of the logic circuit 105 (e.g., the address decoder thereof) is a peripheral circuit. And this interpretation is consistent with what a POSITA would have understood and found obvious: decoders were considered part of the DRAM (i.e., its peripheral circuitry). *See, e.g.,* EX1005, FIG. 5; EX1008, FIG. 1; EX1009, FIG. 2; EX1010, FIG. 6; EX1012, Chapter 4.

82. Thus, a POSITA would have understood and found obvious that at least a portion of the “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201” (e.g., its decoder) is a peripheral circuit of the DRAM.

83. A POSITA would have understood and found obvious that the logic circuit 105 is electrically connected to the memory cells of the memory cell array. First, the logic circuit includes an “address decoder,” and a POSITA would have understood and found obvious that the address decoder is electrically connected to

the memory cells, because such an electrical connection is commonly provided so that the address decoder can select DRAM cells for reading/writing. For example, EX1012 (a DRAM textbook) shows a row address decoder being electrically connected to memory cells through a wordline, and a column address decoder being electrically connected to bitlines. EX1012, 18, 25. *See also* Tsern (showing row and column address decoders (“row decoder 365” and “column decoder 510) electrically connected to a memory array 355) and Dono (showing an X/row decoder and a Y/column decoder, which are also referred to as an “address decoder,” electrically connected to a memory cell array). EX1005, [0041], [0045], FIG. 5; EX1008, [0008], [0034]-[0039], FIGS. 1, 8.

84. Second, a POSITA would have understood and found obvious that the logic circuit 105 would be electrically connected to the memory cells of the memory cell array in order to obtain “data...to be processed in the logic circuit” from the memory cells. EX1004, [0044], [0047]. That is, Takahashi describes that data “read out” from the memory cell array is “used for data processing and the like of the logic circuit 105.” EX1004, [0060]. A POSITA would have understood and found obvious that, in order for the data to be obtained at the logic circuit for processing, an electrical connection would be provided between the logic circuit and the memory cells to transfer the data.

85. Alternatively, in order to provide the operations and connections discussed in the two foregoing paragraphs, a POSITA would have found it obvious to electrically connect the logic circuit 105 (e.g., the address decoder) to the memory cells, so that the logic circuit 105 would be able to provide data to, and receive data from, the memory cells, and control read/write operations on the memory cells (e.g., through row and column decoder operations).

86. In this declaration, when analyzing and discussing the circuits and operations discussed with respect to Takahashi FIGS. 7-10B, I sometimes refer to FIG. 1 and Takahashi's description of the elements shown in FIG. 1. FIG. 1 of Takahashi depicts a "semiconductor integrated device 100" of Takahashi's "First Exemplary Embodiment," whereas FIGS. 7 and 8 relate to a "semiconductor integrated device 200" of a "Second Exemplary Embodiment." EX1004, [0026], [0034], [0043], [0077]. However, a POSITA would have understood unambiguously, and found obvious, that the device 200 (which is not illustrated with a view similar to that of FIG. 1) has the same overall configuration as the device 100, and that the description provided for the device 100 can be applied to the device 200 except where Takahashi makes clear otherwise.

87. For example, Takahashi describes that the "second exemplary embodiment" "differs from the semiconductor device of the first exemplary embodiment [FIG. 1] in the configuration of a semiconductor memory circuit

portion... the semiconductor integrated device 200 of the second exemplary embodiment has a configuration in which the semiconductor memory circuit 101 of the semiconductor integrated device 100 shown in FIG. 1 is replaced with the semiconductor memory circuit 201.” EX1004, [0077]. That is, the second embodiment has the overall configuration shown in FIG. 1 (including the logic circuit 105), with a different semiconductor memory circuit, and a POSITA would have correspondingly understood and found obvious that the description provided for FIG. 1 correspondingly extends to the semiconductor integrated device 200.

88. As a specific example, a POSITA would have understood and found obvious that the that the logic circuit 105, as illustrated in FIG. 1, forms a part of the semiconductor integrated device 200 of FIGS. 7 to 10B. For example, Takahashi describes that “[t]he second exemplary embodiment assumes the case where transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201 are further reduced in film thickness...as compared with the first exemplary embodiment,” making clear that the logic circuit 105 is part of the second embodiment. EX1004, [0078]. Takahashi also describes that data read out from the memory in the second embodiment “is used for data processing and the like of the logic circuit 105.” EX1004, [0086]. Also, the logic circuit 105 includes the “address decoder” that is essentially required for DRAM operation, such that omitting the logic circuit 105 would prevent operation

of the semiconductor memory circuit 201. EX1004, [0044]. In addition, to the extent the logic circuit 105 does not already explicitly form a part of the semiconductor integrated device 200, a POSITA would have found it obvious to include the logic circuit 105 in the semiconductor integrated device 200, to permit the logic circuit 105 to perform the decoding and processing operations described for it in Takahashi. EX1004, [0044], [0047], [0060].

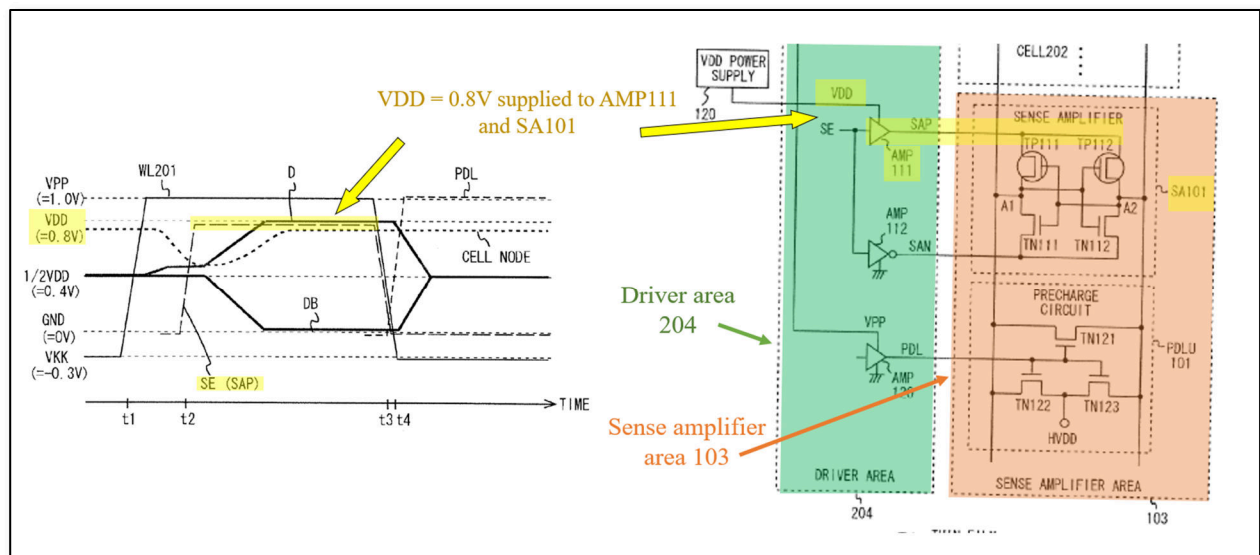
89. Similarly, a POSITA would have understood and found obvious that the driver area 204, cell area 202, and sense amplifier 103 shown in FIG. 7 have a configuration substantially similar to that of the driver area, cell array area 102, and sense amplifier area 103 shown in FIG. 1. This is made clear, for example, by their very similar illustration (compare FIGS. 2 and 7) and their similar operation (compare [0048]-[0065] to [0080]-[0088], and FIG. 3 to FIG. 8).

[1.7]: and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage,

90. Takahashi's peripheral circuits noted above (the sense amplifier area 103, the driver area 204, and at least a portion of the logic circuit 105) are each supplied with a second voltage VDD. VDD is a "power supply voltage [] of the logic circuit." EX1004, [0045]. VDD is supplied to the sense amplifier area 103 when "the sense amplifier control signal SAP becomes equal to the power supply voltage VDD." EX1004, [0086]. Note that the sense amplifier control signal SAP

is a voltage internal to the sense amplifier area 103 that is provided directly to transistors of the sense amplifier. EX1004, FIG. 7. Further, VDD is supplied to the driver area 204 when “[a] power supply voltage [VDD] of the driver amplifier AMP111 is supplied from a VDD power supply 120.” EX1004, [0055]. Takahashi FIG. 7 shows VDD on an internal line of the driver area and being provided directly to an amplifier of the driver area. EX1004, FIG. 7.

91. The supply of the second voltage VDD from VDD power supply 120 to the driver area 204, and to the sense amplifier area 103 on the sense amplifier control line SAP, is shown in Takahashi FIGS. 7 and 8, below.



Left: Takahashi, FIG. 8; Right: Takahashi, FIG. 7 (partial)

92. A POSITA would have understood and found obvious that the logic circuit 105 operates at its “power supply voltage” VDD. EX1004, [0045]. See discussion at §VII.E.4(c) below illustrating that power supply voltages are equated

to operation voltages. The sense amplifier area 103 operates at VDD at least when VDD is supplied to transistors TP111 and TP112 of the sense amplifier SA101 through the sense amplifier control line SAP. EX1004, [0052], [0056], [0086]. For example, the sense amplifier area 103 operates at VDD when, based on receiving the sense amplifier control signal at VDD, “[t]he sense amplifier SA101 amplifies the small potential difference between the pair of bit lines D and DB to the power supply voltage VDD and to the ground voltage GND.” EX1004, [0086]. The sense amplifier area 103 also operates at VDD when the bitline D (which is part of the sense amplifier area 103, as shown in FIG. 7) is set to VDD, as shown in FIG. 8. The driver area 204 operates at VDD at least when the driver amplifier AMP111 receives VDD as its power supply voltage. EX1004, [0056].

93. For further elaboration on why a POSITA would have understood and found obvious that that a circuit operates at its power supply voltage, *see* [3.6] in VII.E.4(c)

94. For the reasons discussed for [1.3], a POSITA would have understood the recitation that the second voltage VDD be “within a second voltage range” to be satisfied by any range that encompasses the disclosed value of VDD=0.8V (discussed in further detail below). EX1004, [0084]. More, and again as discussed for [1.3], the second voltage VDD is also within a small second voltage range around its nominal value of 0.8V due to expected non-idealities in voltage

generation and provision, for example, due to temperature effects, device-to-device variation, load conditions, etc.

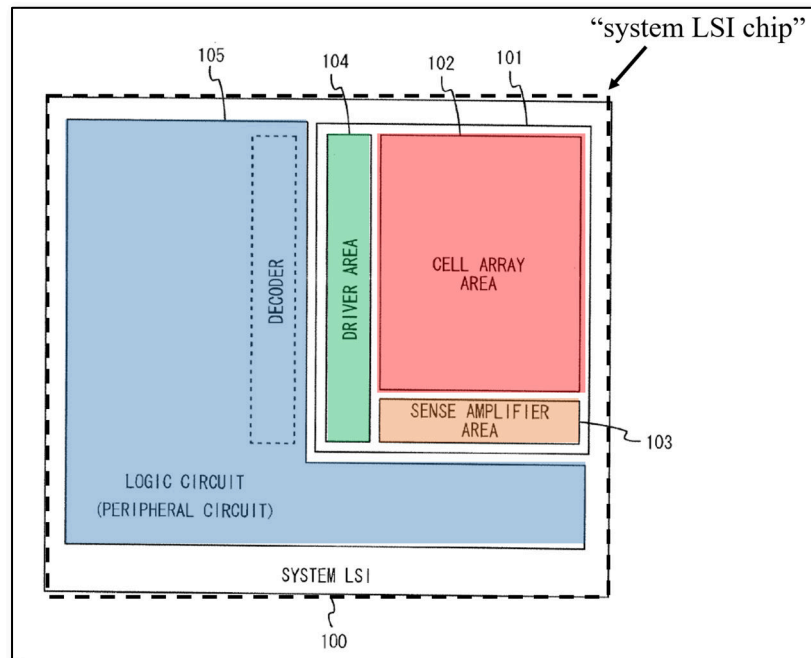
[1.8]: wherein the second voltage is lower than 1.1 V, and

95. Takahashi's second voltage, VDD, is 0.8 V, which is lower than 1.1 V. See, e.g., Takahashi [0078] ("VDD is 0.8V or lower"), [0084] ("the power supply voltage VDD is 0.8 V"), and FIG. 8, which shows "VDD (=0.8V)." EX1004, [0078], [0084], FIG. 8. Further, Takahashi FIGS. 9A and 10A state "VDD (=0.8V)."

[1.9]: wherein the DRAM core cell and the peripheral circuit are formed on a single chip,

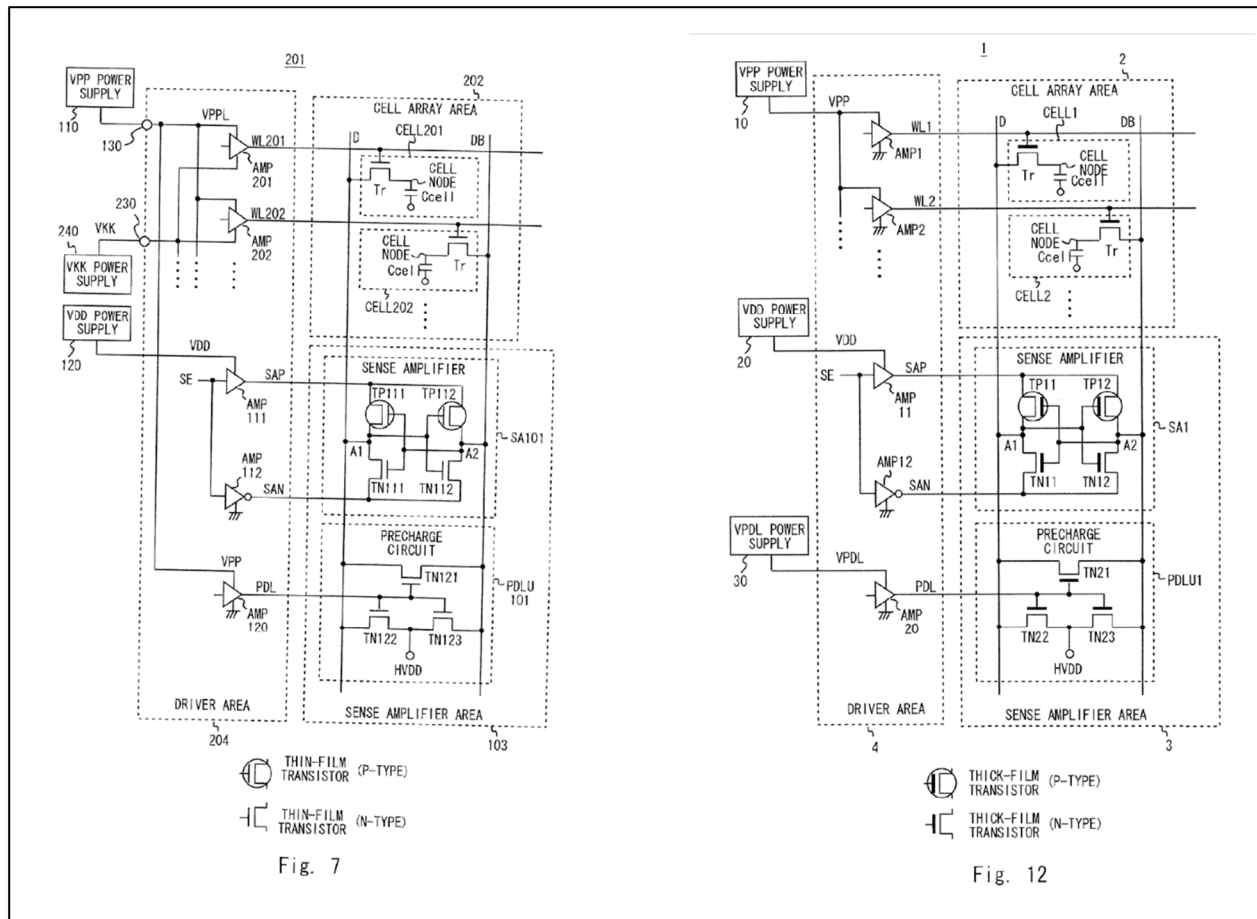
96. Takahashi describes "a system LSI chip" that includes the cell array area 102 (202 in the FIG. 7-10B embodiment), the sense amplifier area 103, the driver area 104 (204), and the logic circuit 105, thereby forming the DRAM core cell (cells of the cell array area) and the peripheral circuit (the sense amplifier area 103, the driver area 204, and/or the logic circuit 105) on a single chip. EX1004, [0043], FIG. 1. A POSITA would have understood and found obvious that these elements, all being included in the single "system LSI chip," are formed on the single system LSI chip. For example, the system LSI chip is also referred to as a "semiconductor integrated device 100," which a POSITA would have understood to mean that its circuitry is all "integrated" in the system LSI chip, i.e., formed on

the system LSI chip as an integrated circuit. EX1004, [0043]. Note that “integrated,” in the context of semiconductor chips, does not mean merely “combined” but refers to unified fabrication in a common semiconductor die.



Takahashi, FIG. 1

97. Takahashi also describes that a “semiconductor memory circuit 1,” a prior art device similar to the semiconductor memory circuit 201, is “integrated into one chip,” and a POSITA would have understood that the semiconductor memory circuit 201 shares this same configuration. EX1004, [0005], [0018], FIG. 12. For example, as shown below, the semiconductor memory circuit 1 is illustrated in FIG. 12 in a manner matching the illustrations of circuits 101, 201. EX1004, FIGS. 2, 7, 12. This parallel illustration would have been understood by a POSITA as disclosing matching device structures.



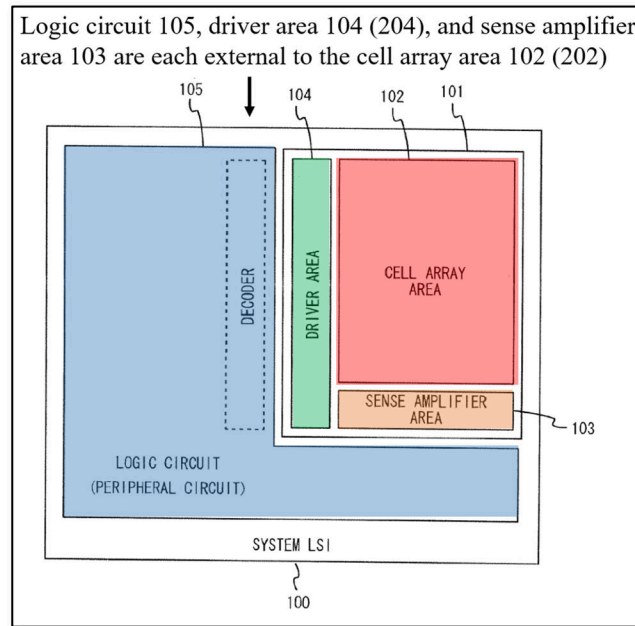
Takahashi, FIGS. 7 and 12

98. In addition, Takahashi's comparison of transistor designs between the logic circuit 105, the cell array area 202, and the sense amplifier area 103 would have informed a POSITA that these circuits were formed as an integrated circuit in a single chip. EX1004, [0014], [0044]-[0046], [0078]-[0083], FIG. 7. Takahashi describes use of two transistor types, "thick-film transistors" and "thin-film transistors," distinguished by their gate oxide thickness. EX1004, [0014]. Takahashi also describes that, in the second embodiment, "transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory

circuit 201 are further reduced in film thickness” and “the gate transistor Tr of each memory cell of the second exemplary embodiment is formed of a thin-film transistor similar to that of the logic circuit 105.” EX1004, [0078], [0080]. FIG. 7 further illustrates that the thin-film transistor is used in each of the cell array area 202 and the sense amplifier area 103. EX1004, FIG. 7. Takahashi also describes that “in the semiconductor memory circuit 201 of the second exemplary embodiment, the gate transistors Tr of the memory cells, the transistors of the sense amplifier SA101, and the transistors of the precharge circuit PDLU101 are each formed of a thin-film transistor similar to that used for the logic circuit 105 which is miniaturized and has a reduced power supply voltage. This eliminates the need to form thick gate oxide films and thin gate oxide films of transistors separately in the fabrication process of an LSI chip, which simplifies the fabrication process. The simplification of the fabrication process leads to a reduction in manufacturing cost and time.” EX1004, [0091]. This repeated discussion of matching transistor types, especially in reference in simplification of fabrication as discussed in [0091], would have made clear to a POSITA that the entirety of the Takahashi’s chip (including the logic circuit 105, the cell array area 202, the driver area 204, and the sense amplifier area 103) was formed in an integrated process in a single chip, because it is in such a fabrication process that matching transistor types would have been relevant.

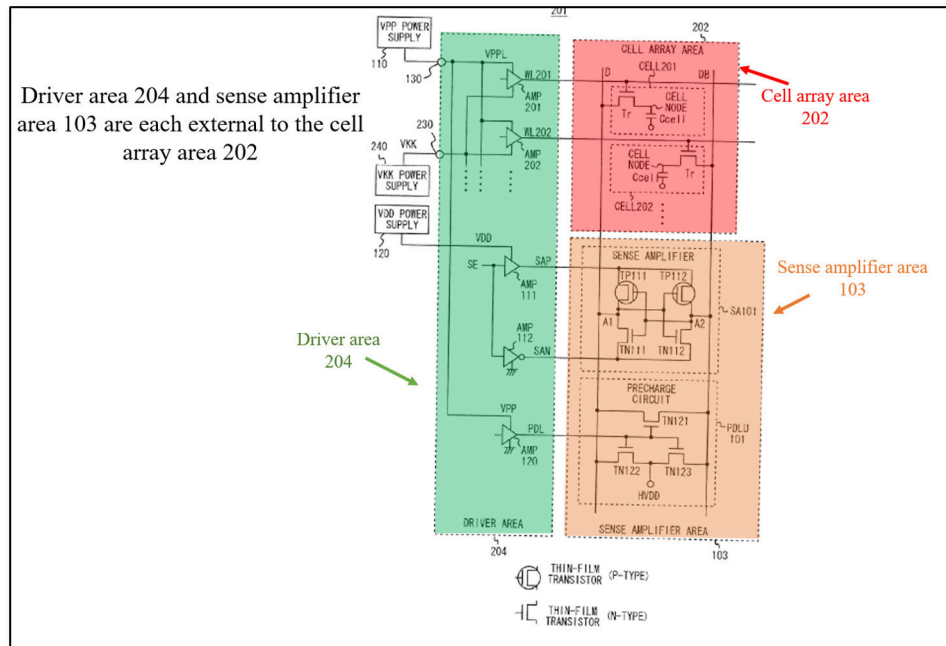
[1.10]: and the peripheral circuit is external to the DRAM core cell,

99. Takahashi's logic circuit 105, driver area 204, and sense amplifier area 103 are external to the cell array area 202 (which includes the DRAM core cells), e.g., as shown in FIG. 1. EX1004, FIG. 1.



Takahashi, FIG. 1

100. Takahashi FIG. 7 similarly shows that the driver area 204 and the sense amplifier area 103 are external to the cell array area 202.



Takahashi, FIG. 7

[1.11]: and wherein the first voltage is different from the second voltage.

101. See [1.5] and [1.8] above. Takahashi's first voltage VPPL is 1.0V, which is different from the 0.8V of Takahashi's second voltage VDD. EX1004, [0078], [0083]-[0084], FIG. 8.

(b) **Claim 2**

102. Claim 2's elements are found identically in claim 1, except for [2.9] discussed below. For [2.1]-[2.8], see [1.1]-[1.8], respectively.

[2.9]: wherein the first voltage is greater than the second voltage.

103. See [1.5] and [1.8]. Takahashi's first voltage VPPL is 1.0V, which is greater than the 0.8V of Takahashi's second voltage VDD. EX1004, [0078], [0083]-[0084], FIG. 8.

(c) **Claim 3**

[3.1]: A dynamic random access memory (DRAM), comprising:

104. *See [1.1] at §VII.A.2(a).*

[3.2]: a DRAM core cell comprised in the DRAM,

105. *See [1.2] at §VII.A.2(a).*

[3.3]: wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage,

106. *See [1.3] at §VII.A.2(a).* Takahashi discloses a first voltage, VPPL, supplied to the memory cells of the cell array area 202. EX1004, [0081], [0083], FIGS. 7-8.

[3.4]: and the DRAM core cell is a volatile memory cell;

107. *See [1.5] at §VII.A.2(a).*

[3.5]: an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell,

108. I have been informed by counsel that a “means-plus-function” interpretation can be appropriate when a claim term recites a function without reciting a definite structure for performing that function. The recited “input/output circuit” falls in that category, and I have therefore constructed the “input/output circuit” as a circuit that performs input and/or output functions with respect to a

memory, consistent with description in the '098 Patent. EX1001, 6:3-8 (“an input/output circuit comprised in the DRAM”).

109. I have also reviewed the '098 Patent's disclosure with respect to the input/output circuit. The Specification's most detailed description of this circuit is provided at 2:50-65 in relation to the “Input/output unit” 106 that is depicted in the Specification's sole “FIGURE” as one box connected to two other boxes (respectively labeled “Memory core unit” 102 and “Peripheral circuit unit” 104). At 2:50-65, the Specification notes that “the dynamic random access memory 100 includes a memory core unit 102, a peripheral circuit unit 104, and an input/output unit 106, where the peripheral circuit unit 104 is electrically connected to the memory core unit 102, and the input/output unit 106 is electrically connected to the peripheral circuit unit 104 and the memory core unit 102.” EX1001, 2:50-65. The '098 Patent also refers to “operation voltages of the input/output unit 106” and to “an input output unit.” EX1001, 1:66-2:35, Abstract.

110. Accordingly, in identifying an “input/output circuit” in prior art, I have identified circuits that perform the claimed input and/or output function. These circuits are also disclosed by the prior art with at least as much structure as the '098 Patent's Specification provides for the input/output circuit. The applied prior art anticipates or renders obvious the claims, regardless of whether the “input/output circuit” is construed as a means-plus-function limitation.

111. My analysis of claims 1 and 2 above was consistent with the applicant's statements during prosecution, in that Takahashi's driver area 204 was applied as a peripheral circuit. However, Takahashi's memory is an *embedded* DRAM, and, in this context, a POSITA would have also understood that the driver area 204 constitutes an input/output circuit.

112. A POSITA would have understood that Takahashi's DRAM is an "embedded DRAM" because Takahashi's LSI chip is an "integrated" chip in which "the semiconductor memory circuit [] and a logic circuit that operates at high speed are integrated into one chip." EX1004, [0018]. That is, the memory and the computer processor ("CPU") are integrated into the same die. EX1004, [0044]. The DRAM of such a chip is typically referred to as "embedded" DRAM, or eDRAM. In non-embedded DRAMs, the DRAM is typically in one die while the computer processor is in another die. For example, Tsern (which appears to disclose a non-embedded DRAM) describes that the memory controller is "typically separate from the DRAM" and discloses an example in which "memory controller 305 and DRAM 310 are on separate ICs." EX1005, [0035].

113. A POSITA would have analyzed the components of Takahashi's memory in view of the fact that the memory is an eDRAM. In particular, in labeling or demarcating the "input/output circuit," a POSITA would have differentiated between the eDRAM case and the non-embedded DRAM case. In the

case of a non-embedded DRAM memory chip, the I/O circuit is used to communicate with the outside world from the chip, and the I/O circuit performs the function of communicating with other chips. In this case, the peripheral circuits within the memory chip perform (among other functions) functions of facilitating this interfacing of the data in the memory with the I/O circuit.

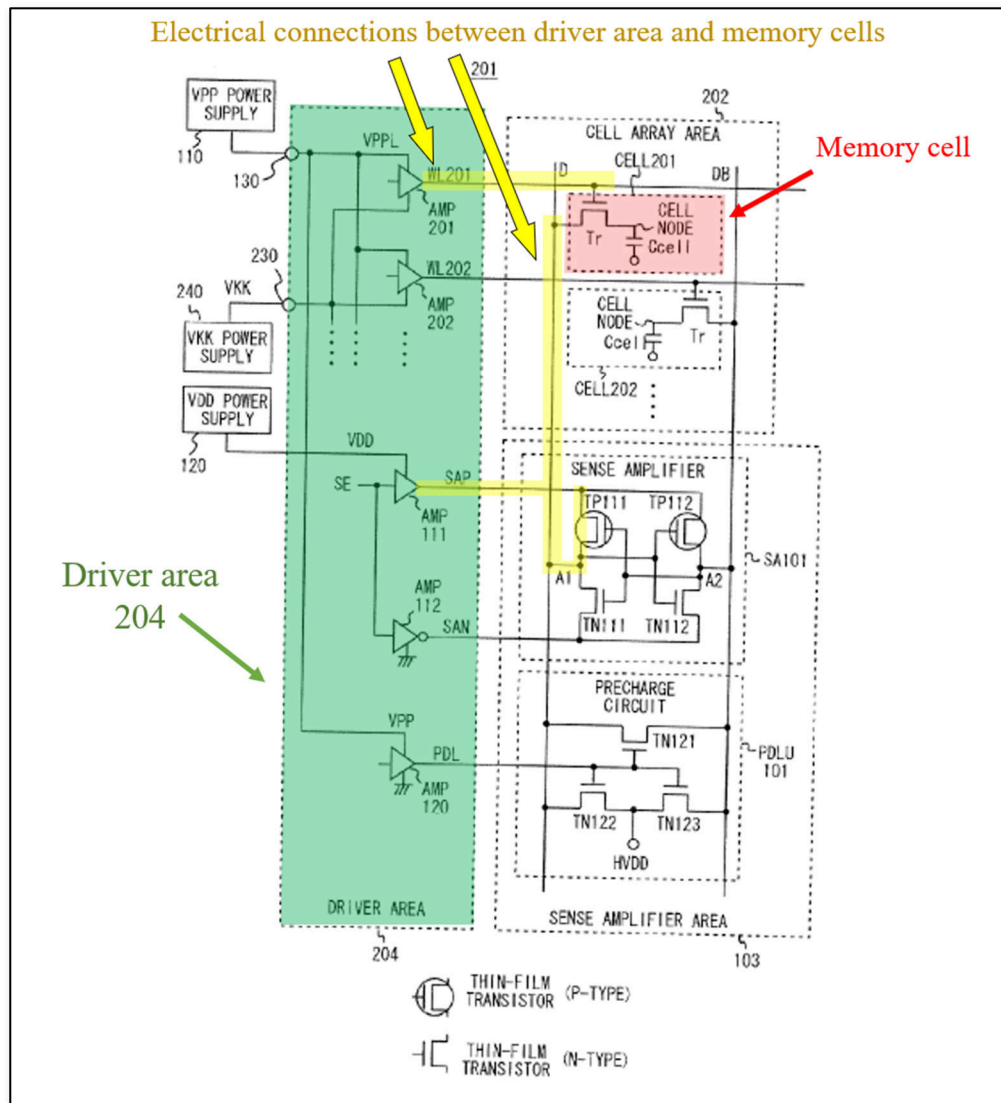
114. In an embedded DRAM, by contrast, communication is performed with other components on the same chip, and a POSITA would have understood and found obvious that the “input/output circuit” is the portion of the DRAM’s circuitry that performs the function of receiving external inputs used to write to, and read from, the memory cell array.

115. In Takahashi’s DRAM, this function is performed at least by the driver circuit 204. That is, the driver area 204 serves as interface circuitry between the cell array and other circuitry. For example, to perform a data readout operation, the amplifier 111 (AMP111) of the driver area 204 receives, as input from outside the semiconductor memory circuit 201, a “control signal SE” that causes voltage amplification and data output. EX1004, [0084]-[0086], FIGS. 7-8. In other words, the amplifier 111 (i) receives a control signal SE that represents, or indicates, a control signal provided from outside Takahashi’s eDRAM, and (ii) translates the control signal SE into a sense amplifier control signal SAN that controls operation of the sense amplifier SA101. EX1004, [0086]. The translation function is

performed, for example, by causing the sense amplifier control signal SAN to “become equal to the power supply voltage VDD” and thus suitable for controlling operation of the sense amplifier SA101. Thus, the driver area 204 performs the function of receiving external inputs and translating those inputs into internal signals of the semiconductor memory circuit 201, meaning that it performs the function of an input/output circuit. That is, the driver area 204 performs the claimed input and/or output function of the “input/output circuit.” Further, as shown in FIG. 7, Takahashi discloses a level of structural detail exceeding that of the input/output unit 106 of the ’098 Patent. EX1004, FIG. 7. For example, while the ’098 Patent shows the “Input/output unit 106” as a box, Takahashi illustrates and describes internal components and signals of the driver area 204 that are used to perform the claimed input and/or output function of an input/output circuit. EX1004, [0081]-[0088], FIGS. 7-8; EX1001, FIGURE.

116. Thus, in the context of an embedded DRAM like Takahashi’s, the driver area 204 would be understood by a POSITA as a peripheral circuit *or* as an input/output circuit. Consistent with this understanding, in addressing claims 3-9 in this ground, I follow an alternative approach that applies the driver area 204 as an input/output circuit. Both this understanding and the understanding of the driver area 204 as a peripheral circuit are consistent with what a POSITA would have understood and found obvious.

117. As discussed for [1.6] in §VII.A.2(a), the driver area 204 is electrically connected to the memory cells (DRAM core cell) through, e.g., wordline WL201, sense amplifier control line SAP, sense amplifier SA101, and bitline D. EX1004, [0007], [0009], [0081], [0086], FIG. 7. Examples of these electrical connections are shown below:



[3.6]: and the input/output circuit is supplied with a third voltage to make

the input/output circuit operate at the third voltage,

118. As discussed for [1.7] in §VII.A.2(a), the driver area 204 (here applied as the input/output circuit) is supplied with and operates at a voltage VDD. EX1004, [0055], FIG. 7. The voltage VDD is a third voltage. For example, VDD is supplied to the driver area 204 when “[a] power supply voltage [VDD] of the driver amplifier AMP111 is supplied from a VDD power supply 120,” and the driver amplifier AMP111 of the driver area 204 correspondingly operates at VDD when it operates using the power supply voltage VDD. EX1004, [0055].

[3.7]: wherein the third voltage is lower than 1.1V; and

119. As discussed for [1.8] in §VII.A.2(a), Takahashi’s third voltage, VDD, is 0.8 V, which is lower than 1.1 V. EX1004, [0078], [0084], FIG. 8.

[3.8]: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell,

120. See [1.6] at §VII.A.2(a). With Takahashi’s driver area 204 applied as the “input/output circuit,” Takahashi includes other circuits that, consistent with applicant’s statements during prosecution, a POSITA would have understood to constitute peripheral circuits electrically connected to the DRAM core cell. These circuits include the “sense amplifier area 103” (e.g., “sense amplifier SA101”) and/or at least a portion of the “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201” (e.g., the “address decoder of the

semiconductor memory circuit.”). EX1004, [0044], [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7. As discussed in §VII.A.2(f), during prosecution of the parent patent to the ’098 Patent, the applicant explicitly discussed the “row decoder,” “sense amplifiers,” and “column decoder” as peripheral circuits. EX1016, 72-73.

[3.9]: and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage,

121. See [1.7] at §VII.A.2(a). The sense amplifier area 103 and the logic circuit 105 (each of which is a peripheral circuit) are supplied with and operate at a second voltage VDD, which is provided to each of the sense amplifier area 103 and the logic circuit 105. EX1004, [0045], [0052], [0055]-[0056], [0086], FIGS. 7-8. For example, the sense amplifier area 103 operates at VDD when it amplifies a small potential difference to set a bitline voltage to VDD, and the logic circuit 105 operates at VDD because, being its power supply voltage, would have been understood as its operation voltage, as discussed in §VII.E.4(c) below.

[3.10]: wherein the second voltage is lower than 1.1 V and the first voltage is different from the second voltage;

122. See [1.8] at § VII.A.2(a). Takahashi discloses that the second voltage VDD (=0.8 V) is lower than 1.1 V and different from the first voltage VPPL (=1.0V). EX1004, [0078], [0084], FIG. 8.

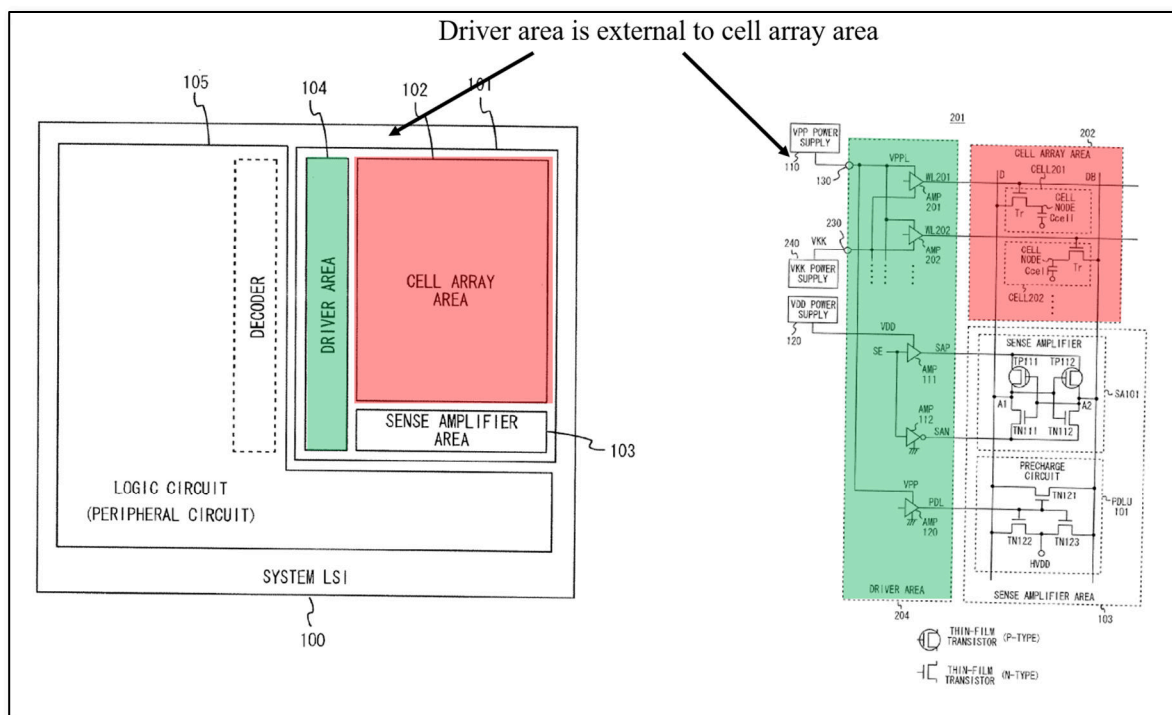
[3.11]: wherein the DRAM core cell and the input/output circuit are formed

on a single chip,

123. See [1.9] at §VII.A.2(a). Takahashi describes “a system LSI chip” that includes the cell array area 102 (202 in the FIG. 7-10B embodiment) and the driver area 104 (204 in the FIG. 7-10B embodiment), thereby forming the DRAM core cell (cells of the cell array area) and the input/output circuit (the driver area 204) on a single chip. EX1004, [0043], FIG. 1.

[3.12] and the input/output circuit is external to the DRAM core cell,

124. Takahashi’s driver area 204 (input/output circuit) is external to the cell array area 202, e.g., as shown in FIGS. 1 and 7. EX1004, FIGS. 1, 7.



Takahashi, FIGS. 1, 7

[3.13] and wherein the first voltage is different from the third voltage.

125. See [3.3] and [3.7]. The first voltage is VPPL=1.0 V. EX1004, [0084], FIGS. 7-8. The third voltage is VDD=0.8V, different from the first voltage. EX1004, [0078], [0084], FIG. 8.

(d) **Claim 4**

[4]: The dynamic random access memory of claim 3, wherein the first voltage is lower than 1.1V.

126. See [3.3] at §VII.A.2(c) and [1.3], [1.5] at §VII.A.2(a). Takahashi discloses a first voltage of VPPL = 1.0 V, lower than 1.1 V.

(e) **Claim 5**

[5]: The dynamic random access memory of claim 3, wherein the first voltage is different from the second voltage.

127. See [3.10] at §VII.A.2(c). This same claim element is recited in claim 3 and addressed above.

(f) **Claim 6**

[6.1]-[6.4]: See [1.1]-[1.4] at §VII.A.2(a).

[6.5]-[6.7]: See [3.5]-[3.7] at §VII.A.2(c).

[6.8]: wherein the first voltage is greater than the third voltage, and

128. See [3.13] at §VII.A.2(c). In Takahashi's device, the first voltage is VPPL=1.0V, and the third voltage is VDD=0.8V, lower than VPPL. EX1004, [0078], [0084], FIGS. 7-8.

[6.9]: the DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP).

129. As discussed in §V.A.2, the '098 Patent describes use of its DRAM as a “frame buffer of a timing controller” of the eDP 1.3 standard. EX1001, 1:30-55, 2:50-54. The frame buffer holds static image data for presentation on a display, reducing power consumption that would otherwise be used for GPU-based image display. EX1001, 1:30-55; EX1015, 25.

130. A POSITA would have understood and found obvious that Takahashi's DRAM is “capable of being applied to an embedded display port (eDP),” for example, as a frame buffer.

131. The '098 Patent states that existing JEDEC “operation voltages...can not satisfy requirements (that is, the low operating power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3.” EX1001, 3:23-27. To better understand the frame buffer and any requirements for its operation, I undertook a close review of the eDP 1.3 standard published by the JEDEC (EX1014). Based on my review, the eDP 1.3 standard includes no voltage or power consumption requirements for the frame buffer. The eDP 1.3 standard describes that the frame buffer (“RFB”) is included in the display panel. EX1014, FIG. 4-1. This requirement, though, does not impose any hard limits on voltage or power consumption. The RFB “stores a static image,” and the image is

“display[ed] from” the RFB. EX1014, 65. From this, a POSITA would have understood that the RFB should be a storage device capable of storing data representative of an image, but a POSITA would not have understood there to be any voltage or power limitations for operation of the RFB. The eDP 1.3 standard also describes protocols for configuring a “[s]etup time” of the RFB, indicating an RFB error, and otherwise enabling/disabling use of the RFB. EX1014, 43, 45, 48, 50, 65-77. Again, none of these operations necessitate any particular voltages or power consumption limits for the RFB. The ’098 Patent’s description of these “requirements” is inconsistent with the published and widely-available eDP 1.3 standard.

132. In view of the eDP 1.3 standard’s lack of those requirements, a POSITA would have understood that a conventional memory, including Takahashi’s, would be “capable of being applied” as an eDP 1.3 frame buffer, because of the conventional memory’s ability to store and provide data representing a static image, consistent with the eDP 1.3 standard. Counsel has informed me that, in patent claim interpretation, “capable of” is a very broad term, and does not necessitate that an element be specifically configured to perform a function or adapted to perform the function. Applying this interpretation, a POSITA would have recognized Takahashi’s memory, which is described as “hold[ing] data” and providing “high-speed operation,” as satisfying the relatively

low bar for being “capable of being applied” as a frame buffer. EX1004, [0047], [0082]. For example, a POSITA would have understood and found obvious that Takahashi’s DRAM is capable of holding data representative of an image, and of providing that data out for display. Indeed, a POSITA would have found it obvious to apply Takahashi’s DRAM as an eDP 1.3 frame buffer in order to conform to the eDP 1.3 standard, thereby gaining the commensurate power and commercial benefits of standard conformity.

133. It would also have been obvious to try applying a DRAM (e.g., Takahashi’s DRAM) as an eDP 1.3 frame buffer, because DRAM was one of a small number of potentially suitable memory types. A POSITA selecting a memory to use as a frame buffer would have been limited to only several options. Read-only memory would be excluded, because the RFB should be capable of receiving and storing new image data. The POSITA would have found it obvious to consider read-write memories such as, for example, static RAM (SRAM), DRAM, and flash memory. EX1031, 381-394.

134. From among those options, a POSITA with a basic knowledge in semiconductor memory at the critical date would recognize that DRAM is the most suitable choice amongst the read-write memory options for frame buffer application. DRAM has the cell size advantage, thus cost advantage, over SRAM; and has a speed advantage over flash memory, since flash memory has

prohibitively long latency delay in both programming time (write) and access time (read).

135. Further, to the extent the '098 Patent erroneously links “capable of being applied to an embedded display port (eDP)” to low-voltage operation, then Takahashi’s DRAM, which has first (VPPL) and third (VDD) voltages that satisfy the “< 1.1 V” condition of the '098 Patent, would be equally as capable of being applied to an eDP as the '098 Patent’s devices. EX1001, 4:61-5:9, Table III. That is, the '098 Patent appears to erroneously suggest that an RFB DRAM is required to have supply voltages less than 1.1V. By this reasoning, Takahashi’s DRAM, which has first and third voltages less than 1.1V, is capable of being applied to an eDP.

(g) **Claim 7**

[7]: The dynamic random access memory of claim 6, wherein the first voltage is lower than 1.1 V.

136. See [1.5] at §VII.A.2(a). Takahashi’s first voltage is VPPL=1.0 V, lower than 1.1 V. EX1004, [0083]-[0084], FIGS. 7-8.

(h) **Claim 8**

[8]: The dynamic random access memory of claim 6, further comprising: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied

with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1 V.

137. See [1.6]-[1.8] at §VII.A.2(a) and [3.8]-[3.10] at §VII.A.2(c). As applied in Ground 1A, peripheral circuits of Takahashi's device include the "sense amplifier area 103" (e.g., "sense amplifier SA101") and/or at least a portion of the "logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201" (e.g., the "address decoder of the semiconductor memory circuit."). EX1004, [0044], [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7. These circuits operate at a second voltage $V_{DD}=0.8$ V, which is lower than 1.1 V. EX1004, [0078], [0084], FIG. 8.

(i) **Claim 9**

[9]: The dynamic random access memory of claim 8, wherein the first voltage is different from the second voltage.

138. See [1.5], [1.8], and [1.11] at §VII.A.2(a), and [3.10] at §VII.A.2(c). Takahashi's second voltage V_{DD} ($=0.8$ V) is different from the first voltage V_{PPL} ($=1.0$ V). EX1004, [0078], [0084], FIG. 8.

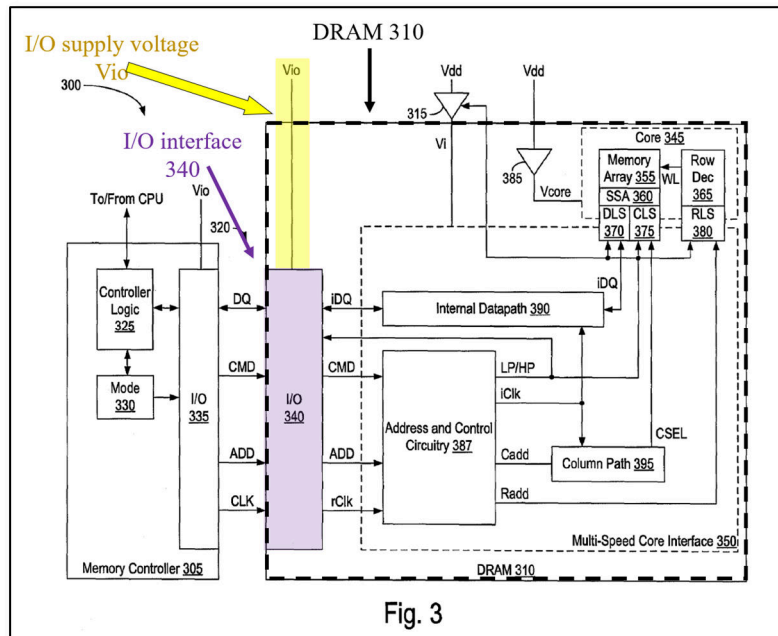
B. [Ground 1B] Takahashi, Tsern, and Schuette render obvious claims 3-9

1. Tsern

139. Tsern relates to DRAM having “dynamic scaling of power and performance.” EX1005, [0005]. The “dynamic scaling” refers to Tsern’s disclosure of memories switchable between a “low-power mode” in which a “relatively low supply voltage V_i ” is supplied to a core interface, and a “high-performance mode” in which a “relatively high supply voltage V_i ” is provided. EX1005, [0018]. “Peak performance is not always required, however, in which case lower supply voltages and reduced data rates can be used to save power.” EX1005, [0003]. Here, Tsern agrees with the widely-understood motivation in the art that lower supply voltages are advantageous in order to reduce power consumption.

140. Tsern also discusses the various voltages used in a DRAM. Tsern describes that “DRAM memory devices...typically include a variety of core voltages selected for optimal performance. These core voltages generally include the external supply voltage VCC, the internal voltage VINT, a boosted wordline voltage VPP, the bitline voltage VBL[,], a half-bitline-voltage $VBL/2$ as a reference for the bitline sense-amplifiers, and a substrate voltage VBB. These voltages can be provided using voltage regulators integrated with the memory core on the same integrated-circuit device, or one or more core voltage may be provided from external sources.” EX1005, [0032].

141. Tsern FIG. 3 illustrates a “memory system 300” including a “DRAM 310.” EX1005, [0034]. The DRAM 310 includes an “I/O [input/output] interface 340” that communicates with a memory controller. EX1005, [0037]. For example, the I/O interface 340 exchanges data DQ with the memory controller 305, and receives commands CMD, addresses ADD, and clock signals CLK from the memory controller 305. The I/O interface 340 “rel[ies] upon a supply voltage Vio” that can be constant or scaled between different performance modes. EX1005, [0043], FIG. 3. Specifically, in Tsern’s FIG. 9A-9D description, “[t]he data rates and supply voltage Vio do not change,” whereas, for FIGS. 11A and 11B, “the clock speed and supply voltage Vio of the I/O interfaces are reduced in the low-power mode.” EX1005, [0062], [0070]. Although Tsern does not provide a specific value for Vio, Tsern describes that Vio can be “reduced in the low-power mode for increased power savings.” EX1005, [0070].



Tsern, FIG. 3

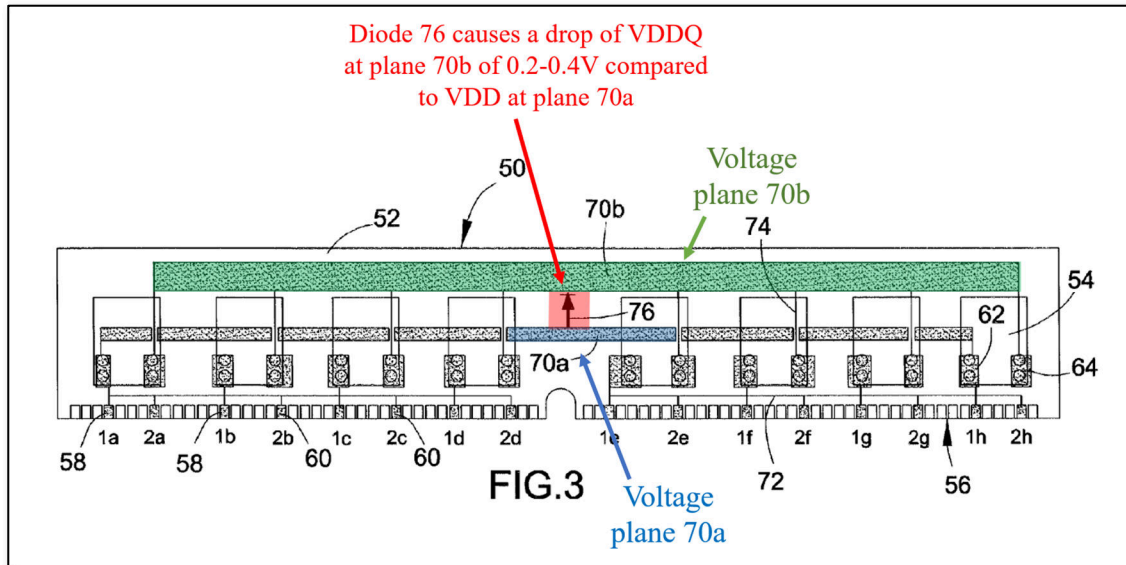
2. Schuette

142. Schuette is directed to “[m]ethods and memory modules adapted for use in computer systems to generate different voltage for core supply (VDD) and input/output supply (VDDQ) inputs to memory components.” EX1006, Abstract. VDDQ is also referred to as “ $V_{I/O}$.” EX1006, [0005]. Schuette describes that it can be useful to provide VDD and VDDQ separately. For example, Schuette states that, when VDD and VDDQ are the same voltage (i.e., when VDD and VDDQ voltage planes are tied together), “increasing the core supply (VDD) voltage of the memory chips 14 will also increase the I/O (VDDQ) voltage...Increasing the I/O voltage, however, can compromise the reliability of the memory controller.” EX1006, [0005]. Therefore, to obtain faster access times, “it is desirable to increase the memory core voltage [VDD]...while keeping the I/O voltage levels at

the standard system specification.” EX1006, [0006]. This configuration can provide “higher frequency and latency yield without compromising the memory controller that manages the flow of data to and from the module” while “avoid[ing] voltage level mismatch between the memory I/O and chipset I/O buffers.” EX1006, [0014].

143. To obtain these improvements, Schuette describes a memory module 50 in which “VDDQ input pins 64...are directly connected with lines 74 to the secondary voltage plane 70b, which is connected to the primary voltage plane 70a through a diode 76. With this approach, a reduction in VDDQ...is accomplished relative to the voltage level at the VDD and VDDQ input pins.” EX1006, [0025]. Specifically, the diode 76 provides “a consistent voltage drop across all levels of load and power draw” for the I/O supply voltage VDDQ in comparison to the core supply voltage VDD. EX1006, [0021], [0029]. As a POSITA would have recognized, this is because “on” diodes exhibit a relatively constant voltage drop. But Schuette is not limited to use of diodes. Rather, “a linear regulator circuit of a known type in the art could be employed in place of the diode 76 to achieve an equivalent reduction in VDDQ voltage.” EX1006, [0029]. “[V]oltage differentials of about 0.2 to about 0.4 volts can be achieved... depend[ing] in part on the default voltage of the memory subsystem.” EX1006, [0029]. This amount of voltage drop

agrees with typical voltage drops over Schottky diodes, a specific type of diode referenced in Schuette. EX1006, [0020].



Schuette, FIG. 3

3. Combination of Takahashi, Tsern, and Schuette

144. It would have been obvious to a POSITA to modify Takahashi's memory device in view of Tsern, to obtain a DRAM having an I/O circuit supplied with a voltage V_{io} as described by Tsern. It would also have been obvious to a POSITA to reduce V_{io} by 0.2-0.4 V compared to the core voltage, as taught by Schuette.

(a) *Combination with Tsern*

145. In addressing claims 3-9 for Ground 1A (*see* §VII.A.2(c)), I explained that Takahashi's driver area 204 would have been interpreted by a POSITA as an "input/output circuit," because it serves an input/output function in the context of

embedded DRAM, translating signals representative of external inputs into control signals that control data readout/writing (e.g., controlling the sense amplifier). According to an alternative interpretation, however, the driver area 204 may be considered peripheral circuitry. For example, as discussed in §VII.A.2(a), the applicant explicitly referred to “drivers” as peripheral circuitry during prosecution of the parent application to the ’098 Patent. EX1016, 72-73.

146. Thus, following the applicant’s interpretation and definition, this ground (Ground 1B) presents an alternative mapping for claims 3-9, in which the driver area 204 is considered a peripheral circuit and is not considered an input/output circuit.

147. In this alternative mapping, Takahashi is interpreted as not explicitly disclosing an input/output circuit. However, following this interpretation, it would have been obvious to incorporate an input/output circuit into Takahashi’s semiconductor memory circuit 201, in two distinct ways and for two distinct reasons.

(i) **Obvious to include input/output circuit for data readout from Takahashi’s cell array 202 to logic circuit 105**

148. As discussed above in §VII.A.2(c), Takahashi relates to an “embedded” DRAM in which the memory and processors are integrated on the same chip. In line with this configuration, Takahashi discloses that data stored in

the cell array 202 is read out on the bit lines and utilized by the logic circuit 105.

EX1004, [0060]. For example, Takahashi describes that the “amplifie[d] potential difference between the pair of bit lines D and DB is read out as high-level readout data...by an external circuit and is used for data processing and the like of the logic circuit 105.” EX1004, [0086]. In this description, a POSITA would have recognized that Takahashi’s original language of “amplifier potential difference” is a typographical error and that “amplified potential difference” is the correct interpretation. For example, Takahashi describes that the “sense amplifier SA101 amplifies the small potential difference,” thereby producing the “amplifie[d] potential difference.” EX1004, [0086].

149. For example, as a POSITA would have understood, a processing element of the logic circuit 105 (such as the “CPU”) would read out data stored in the cell array 202 and perform operations on the data. EX1004, [0044].

150. Takahashi does not, however, describe details of the “external circuit” that reads out the data, and does not describe how voltages on the bit lines D and DB are transferred, as “1”s and “0”s, to “data processing” elements of the logic circuit 105. That is, Takahashi has a “missing link,” or a missing interface, between the bit lines and the data processing elements of the logic circuit 105: an “external circuit” is used for data readout, but Takahashi provides no details on its structure. Indeed, Takahashi’s FIG. 7 does not illustrate what element(s) are

connected to the bottom of the bitlines D and DB, which would naturally have led a POSITA to inquire as to that connection and seek to provide a suitable “external circuit” connected to the bitlines.

151. For purposes of comparison, it is noteworthy that Takahashi illustrates and describes, at length, the driver area 204, which, as discussed in §VII.A.2(c) serves a function of translating control signals to internal control signals that control operation of Takahashi’s DRAM. As a POSITA would have recognized, however, the driver area’s operation is apparently limited to *control*: the driver area 204 does not appear to input or read out data values themselves. EX1004, [0079]-[0088]. An analogous circuit for the data values, and for voltages representative of the data values, is not explicitly disclosed by Takahashi, except for the brief mention of the “external circuit” that “read[s] out” the “amplifie[d] potential difference between the pair of bit lines” as “high-level data.” EX1004, [0086].

152. In view of Tsern’s disclosure, a POSITA would have been motivated and would have found it obvious to provide Takahashi’s semiconductor memory circuit 201 with an input/output circuit, powered by a supply voltage Vio, as the “external circuit” that reads out data from Takahashi’s bitlines and facilitates communication with the logic circuit 105, performing a data output function with respect to Takahashi’s memory. This is the function of Tsern’s I/O interface 340,

which receives “data iDQ” and transfers it out of the DRAM 310 for use. For example, Tsern describes that “[i]nternal datapath 390 then conveys the read data to I/O interface 340, and hence to controller 305 [distinct from the DRAM 310].” EX1005, [0042]. To provide this function (which a POSITA would have understood to be present in Takahashi’s DRAM, even if not discussed in detail), it would have been obvious to include an I/O interface (or circuit) in Takahashi, connected to Takahashi’s bitlines, such that data read from Takahashi’s memory cells would be “convey[ed]...to [the] I/O interface [], and hence to” the logic circuit 105 to provide output of stored data to the logic circuit 105. EX1005, [0042]. The I/O circuit would also obviously be configured to provide data input for storage in Takahashi’s memory cells, in line with the well-understood purpose and operation of bitlines and memory cells (voltages on bitlines are used to write data to memory cells by charging capacitors in the memory cells). It would be within the skill of a POSITA to select a suitable structure for the I/O circuit that, as Tsern describes, would have been electrically connected to Takahashi’s peripheral circuits and core memory cells (e.g., through the bitlines). The ’098 Patent provides no structure for the input/output circuit more detailed than the “unit” (box) of the FIGURE.

153. That Tsern appears directed to non-embedded DRAM, while Takahashi is focused on embedded DRAM, does not detract from the obviousness

of the inclusion of the I/O circuit. Regardless of this difference, Tsern would have made clear to a POSITA the usefulness of data I/O functionality, and would have motivated a POSITA to ensure that this functionality would be included in Takahashi's device. Tsern's *teaching*, not Tsern's physical I/O interface, is being applied to Takahashi.

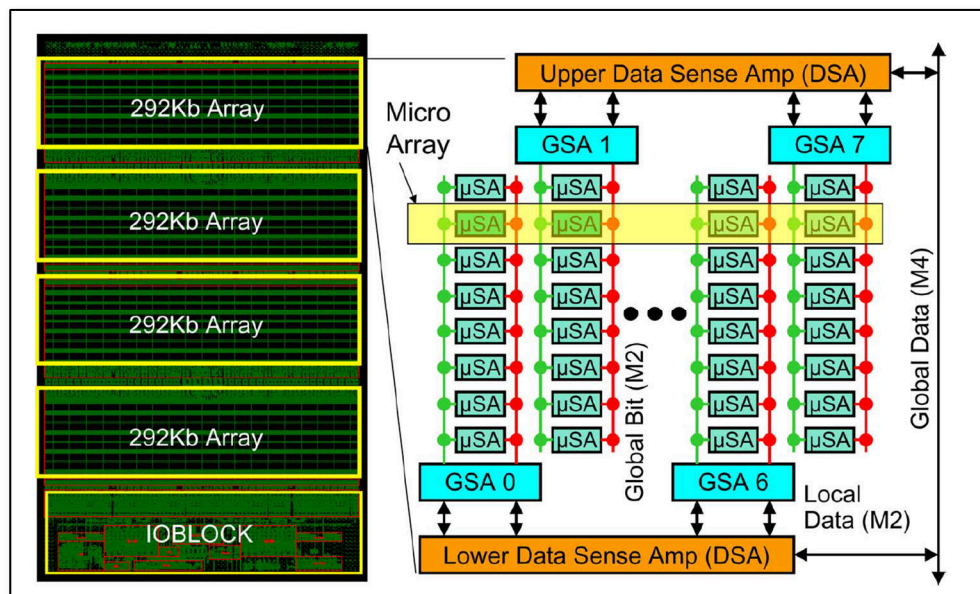
154. The exact form of the I/O circuit would not be particularly limited. The I/O circuit incorporated into Takahashi's memory device as the "external circuit" would obviously include, for example, input buffers, output buffers, level-shifters, and/or other circuit elements that facilitate useful transfer of data from their form in Takahashi (voltages on the pair of bitlines D and DB) to a form useful for circuit elements of the logic circuit 105. For example, the input buffer (e.g., in the form of inverters with suitably-designed channel width and length to provide targeted current) would be used to provide proper drive strength and threshold voltage to data signals. Likewise, the output buffer, similarly designed to targeted drive strength, would take the low-current data coming out of the sense amplifier area 103 and strengthen them onto the high capacitive load of the interconnect bus to be used by receiving devices of the logic circuit 105. Level shifters, in both directions, may be included to shift the signal levels to be compatible within the cell array area 202 and/or sense amplifier area 103 and the logic circuit, respectively.

155. It would have been within the skill of a POSITA to select suitable circuit elements to perform these and other input/output functions, motivated by Tsern's disclosure of an I/O interface and guided by Tsern's disclosure that the I/O circuit should be powered by a voltage V_{io} . For example, a POSITA would have been guided by Takahashi description that the "external circuit" "read[s] out" "the amplifie[d] potential difference between the pair of bit lines D and DB," and it would have been well within the skill of a POSITA to configure the I/O circuit to perform this function with a reasonable expectation of success, given that the circuit operations and functionalities in question were well-understood and predictable. For example, a POSITA would have been able to understand the interface requirements between the array/sense amplifier circuitry and the logic circuit 105, in terms of signal strengths, capacitive loading, and consequently voltage levels and drive current capabilities, to therefore be able to configure the I/O circuit to perform the I/O functions discussed above.

156. Further, a POSITA would have known that, like non-embedded DRAM, embedded DRAM also conventionally included I/O circuitry for data input and output between the DRAM and processor(s).

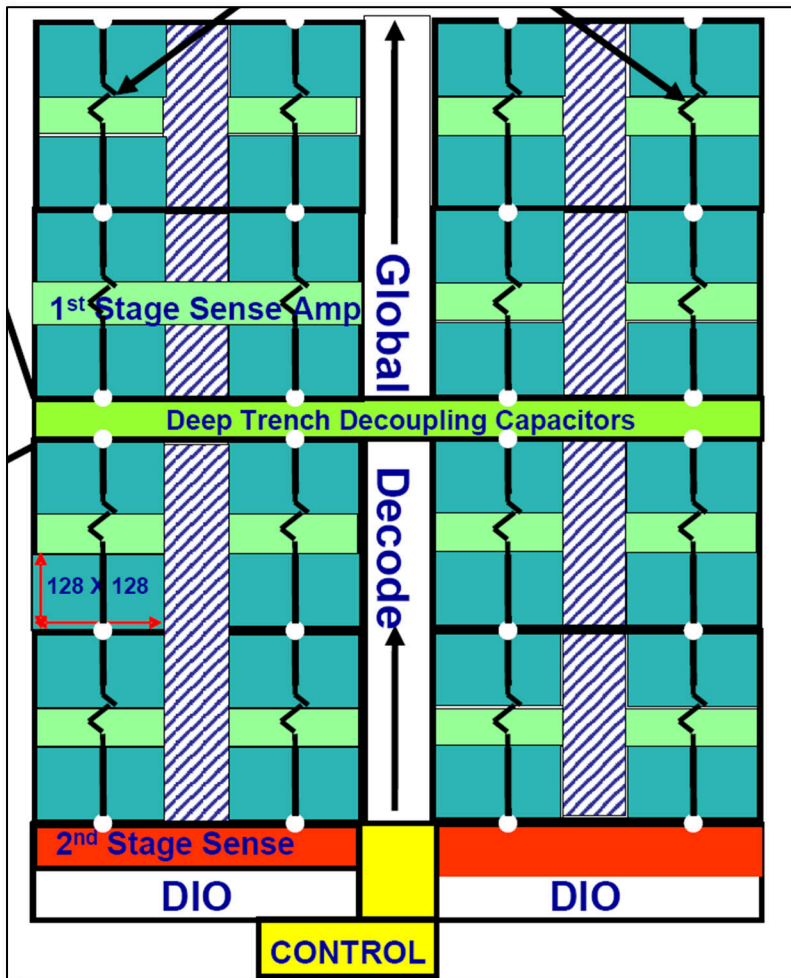
157. For example, a 2011 publication from IBM researchers entitled "A 45 nm SOI **Embedded DRAM** Macro..." discusses an "IOBLOCK," an "interface between the [memory] arrays and the processor core" in their embedded DRAM.

EX1032, 2. The IOBLOCK performs I/O functions for the eDRAM: for example, it “latches the commands and addresses, synchronizing with the processor clock, and generates sub-array selects, [and] global word-line signals. It also includes a concurrent refresh engine...and a refresh request protocol management scheme...to maximize the memory availability.” EX1032, 2. A POSITA would have understood that at least some of these functions could advantageously be performed by an I/O circuit included in Takahashi’s DRAM. The IOBLOCK is also shown in a diagram of the IBM eDRAM:



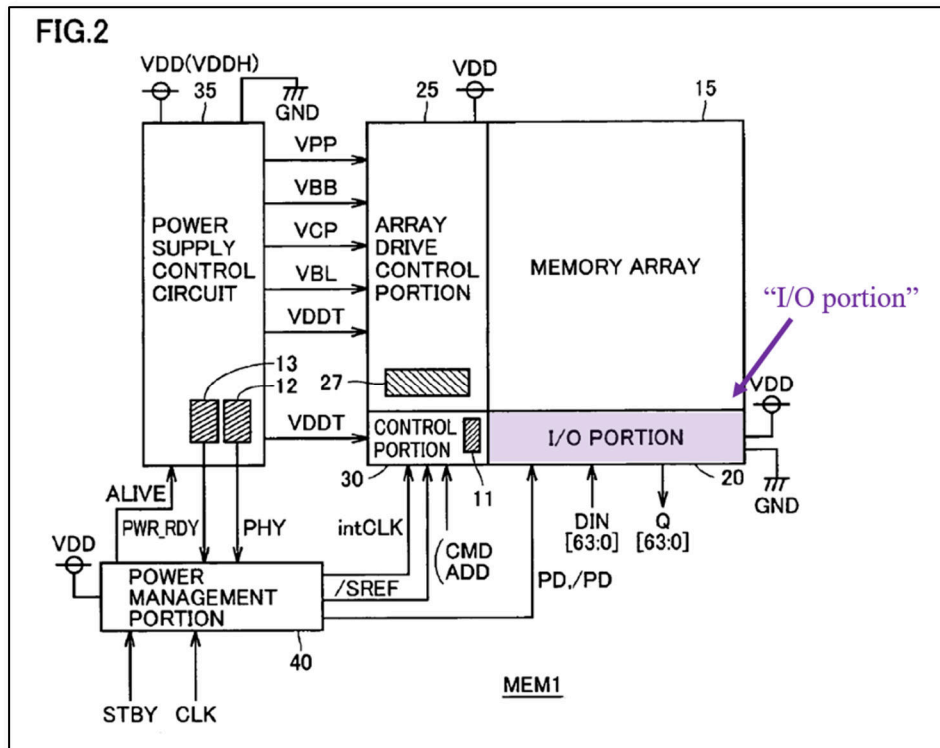
EX1032, FIG. 2

158. A presentation from 2009, “eDRAM to the Rescue,” includes a die diagram showing I/O circuitry (“DIO”) for communication between embedded DRAM and processor cores. EX1033, 10.



EX1033, 10.

159. A patent filing from 2008 (EX1034) relates “particularly to an embedded memory integrated on a single semiconductor chip together with a processing device such as logic,” for “an embedded DRAM.” EX1034, 1:6-14. EX1034 uses the same “system LSI” language as Takahashi and shows a “memory circuit” including “an I/O portion... transmitting and receiving data to and from [the] memory array.” EX1034, 1:6-20, 8:5-9, FIG. 2.



EX1034, FIG. 2

160. As another example, a patent filing from 2003 (EX1035) shows “a plurality of DRAM macro structures” “embedded” “in a system LSI.” EX1035, 19:18-19. A “memory 6” including multiple DRAM macros includes an “access optimizer” (i.e., an I/O circuit), where “[t]he DRAM macro structures 5Ma to 5Md input/output data from/to the access optimizer 4.” EX1034, 8:65-67.

161. In short, whether data was being transferred to/from a DRAM to another die or to a processor on the same die, I/O circuitry was conventional and necessary to facilitate the transfer. Providing Takahashi’s DRAM with an I/O circuit would have filled this vital function and been obvious to a POSITA.

162. Tsern motivates not only the inclusion of an I/O circuit as the “external circuit” but also the use of a supply voltage V_{io} to power the I/O circuit. For example, a POSITA would have been motivated to use the supply voltage V_{io} in order to reduce power consumption. Tsern describes, for example, that the I/O interface “can use [a] scaled supply voltage” V_{io} , such that V_{io} “can be reduced in the low-power mode for increased power savings.” EX1005, [0043], [0070]. It would have been obvious to provide a supply voltage V_{io} to the I/O circuit to achieve these power savings. Further, it would have been obvious to a POSITA that the I/O circuit would require a power supply voltage, as essentially all functional circuits do. In view of this requirement, it would have been obvious for a POSITA to follow Tsern’s clear teachings and power the I/O circuit with the supply voltage V_{io} . That is, even in the absence of a low-power mode, a POSITA would have recognized the necessity of powering the I/O circuit to allow the circuit to operate.

(ii) **Obvious to add Tsern’s input/output interface to Takahashi to facilitate off-chip data transfer**

163. As a second obvious modification of Takahashi (distinct from the first modification discussed immediately above), it would have been obvious to provide Takahashi’s semiconductor memory circuit 201 with Tsern’s I/O interface 340, or

a substantially similar circuit, to allow Takahashi's semiconductor memory circuit 201 to receive data from, and transfer data to, off-chip elements.

164. A POSITA would have recognized several clear benefits from this modification. First, the addition of Tsern's I/O interface 340, or a substantially similar circuit, would have greatly expanded the versatility of Takahashi's memory, allowing it to not only exchange data with on-chip processing elements of the logic circuit 105, but also to exchange data with external devices, e.g., generic computing devices. For example, Tsern describes that the I/O interface 340 exchanges data with a memory controller 305, and that the memory controller 305 exchanges the data with a central processing unit, a configuration Tsern describes as "conventional." EX1005, [0034]-[0035], FIG. 5. Thus, while Takahashi's disclosed DRAM is limited to on-chip communication and use of the logic circuit 105's processor, the additional inclusion of Tsern's memory interface 340 would also permit off-chip communication with generic off-chip devices and processors, improving Takahashi's functionality.

165. Further, the inclusion of Tsern's I/O interface 340, or a substantially similar circuit, would have made Takahashi's DRAM compatible with DRAM standards, which assume the presence of I/O circuitry for off-chip communication. For example, the LPDDR3 DRAM standard required an I/O data bus (e.g., "I/O pins") and supply of an I/O power supply voltage V_{DDQ} , for connecting to and

powering an I/O circuit of the memory. EX1013, 12-13, 83. The I/O power supply voltage V_{DDQ} , as a POSITA would have known, is used for—and therefore implies the presence of—inter-chip input/output circuitry of the DRAM. A POSITA would have recognized that modifying Takahashi to conform to this and similar standards would have improved the interoperability of Takahashi’s device and expanded its utility.

166. A POSITA would have had a reasonable expectation of success in making this modification. Takahashi’s and Tsern’s devices are DRAMs with similar architectures, each including, for example, a memory array, a sense amplifier circuit, precharge circuitry, drive circuitry, and address/decode circuitry. EX1004, [0044], [0048], [0051], [0079], FIGS. 1, 7; EX1005, [0020]-[0021], [0037], FIG. 3. And both Takahashi and Tsern employ multiple different voltages that are provided to different components (e.g., VPPL, VKK, and VDD in Takahashi, and Vio, Vi, and Vcore in Tsern). EX1004, [0084], FIG. 7; EX1005, [0026], [0043], FIG. 3.

167. Thus, in making this modification, a POSITA would have been modifying one device to have the configuration of a substantially similar device. I/O circuitry was standard in memory devices to permit reception and transmission of signals representing data. The typical DRAM configuration was for a DRAM chip to communicate with a separate chip for transmission of data, as reflected in

the DDR standards, such as the LPDDR3 DRAM standard. EX1013. That is, the inclusion of I/O interfaces in DRAM was entirely standard—so standard that Tsern elides the details of the I/O interface 340 and its off-chip communication, describing it as “conventional.” EX1005, [0035]. In that regard, incorporating an I/O interface (I/O circuit) into Takahashi would have involved nothing more than adding well-known DRAM I/O circuitry (from Tsern) to well-known DRAM cell array circuitry (from Takahashi), a combination that would have been within the skill of a POSITA to perform with a reasonable expectation of success, given the highly established and well-understood nature of DRAM operation.

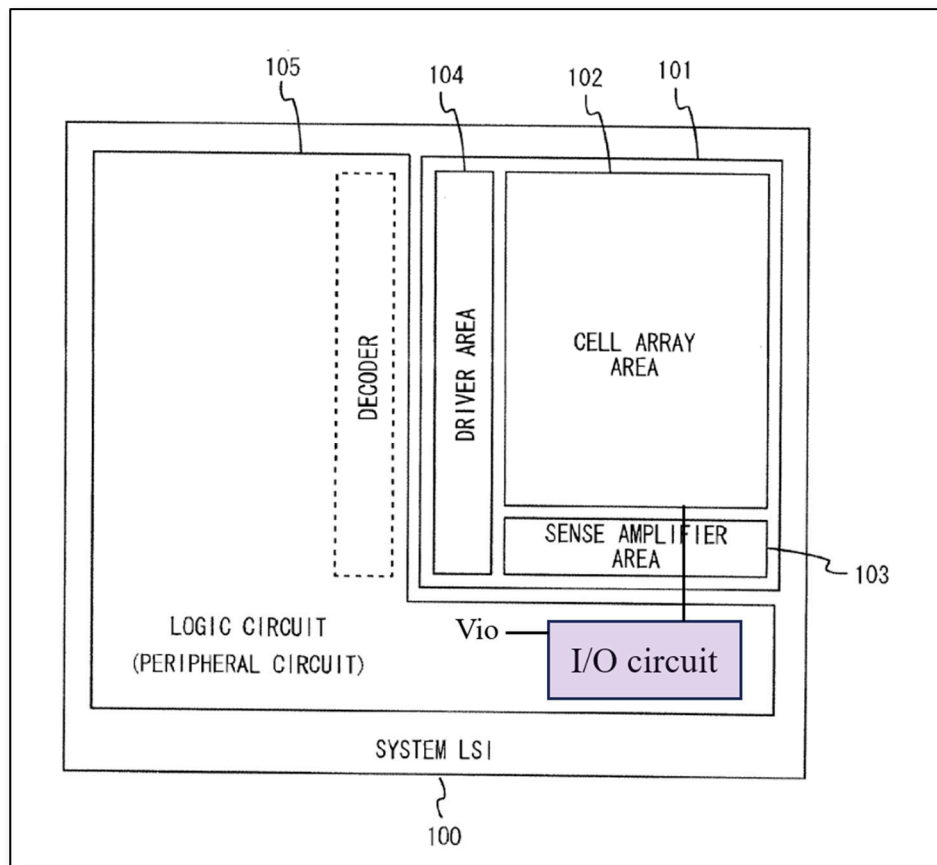
168. Put another way, the incorporation of an I/O interface into Takahashi would have entailed applying the known technique of I/O circuitry to Takahashi’s DRAM, which, by inputting and outputting data on bitlines, had an entirely standard bitline configuration that was ready for improvement through the addition of the I/O circuit. A POSITA would have had a reasonable expectation of success in making this modification by, for example, following the detailed circuit configuration shown in Tsern FIG. 5, and by taking advantage of well-known DRAM design principles.

169. The obviousness of this combination is reinforced by the fact that the inventor Takahashi himself, in another patent filing, disclosed a DRAM with a similar architecture to that of the applied Takahashi reference and having an I/O

circuit. In Takahashi '234 (EX1050), Takahashi described a “DRAM 10” that, like the DRAM of the applied Takahashi reference, included a memory array, sense amplifier, decoder, and power supply elements. EX1050, [0031]-[0034], FIGS. 1-2. Also like the DRAM of the applied Takahashi reference, Takahashi '234 describes output (reading) of data by generation of a potential difference on bitlines D and DB. EX1050, [0043]-[0044], FIG. 5. Further, however, Takahashi '234's DRAM includes, connected to the sense amplifier, an input/output circuit including I/O buffers and an I/O pin or pad, matching an obvious configuration for introduction of an I/O circuit into Takahashi, as discussed in this section. EX1050, [0033], FIG. 1. Thus, inventor Takahashi's own disclosures further demonstrate the conventionality of the I/O circuit and the reasonable expectation of success a POSITA would have had in introducing an I/O circuit (configured for off-chip communications) into Takahashi.

170. Takahashi's system LSI 100, modified to include an I/O circuit, is shown below. For convenience of illustration, the I/O circuit is illustrated as part of the logic circuit 105, but the I/O circuit can equally be considered part of the semiconductor memory circuit 201 (represented as 101 in the drawing below). In the case where Takahashi is modified as discussed in §VII.B.3(a)(i), the I/O circuit is the “external circuit” of Takahashi, configured for communication between Takahashi's embedded DRAM cell array and on-chip processing elements of the

logic circuit 105. In the case where Takahashi is modified as discussed in §VII.B.3(a)(ii), the I/O circuit is, or is substantially similar to, Tsern's I/O interface 340 and is configured for communication between Takahashi's DRAM and off-chip elements. In either case, it would have been obvious to provide the I/O circuit with a power supply voltage V_{io} for the reasons discussed in §VII.B.3(a)(i), e.g., to reduce power consumption and facilitate circuit operation through provision of a supply voltage.



Takahashi-Tsern device

(b) *Combination with Schuette*

171. While Tsern discloses provision of a “supply voltage Vio” to the I/O interface and describes that Vio is preferably “reduced...for increased power savings,” Tsern does not provide a specific value for Vio. EX1005, [0043], [0070]. A POSITA would have understood that incorporating an I/O circuit into Takahashi’s DRAM would involve selecting a suitable value for Vio. To determine an effective value, achieve Tsern’s power savings (which Tsern describes are directly linked to the value of Vio), and maintain effective device performance, a POSITA would have been motivated and would have found it obvious to follow Schuette’s teachings and configure Vio to be “about 0.2 to about 0.4 volts” lower than the core voltage, which a POSITA would have recognized as either VPPL or VDD in Takahashi. EX1004, FIGS. 7-8; EX1006, [0029].

172. As discussed in §VII.A.2(a) for [1.2], the “core” refers to, or at least encompasses, the cell array of a memory. In the case of Takahashi, the cell array area receives both VPPL and VDD. That is, VPPL is provided to the cell array on its wordlines, and VDD is provided to the cell array on its bitlines. EX1004, FIGS. 7-8. Accordingly, either VPPL or VDD would have been interpreted as a core voltage compared to which the I/O voltage is dropped.

173. Following Schuette’s teachings, a POSITA would have found it obvious to use a “diode” or a “linear regulator circuit of a known type in the art” to lower Takahashi’s VPPL (=1.0V) or VDD (=0.8V) by 0.2 to 0.4 V as described by

Schuette, to obtain a Vio in a range from 0.6 to 0.8 V in comparison to VPPL, or in a range from 0.4 to 0.6 in comparison to VDD. EX1004, [0084]; EX1006, [0029]. That is, a POSITA would have found it obvious to use the circuit elements disclosed by Schuette, in order to lower Vio by an amount disclosed by Schuette, in comparison to a core voltage disclosed by Schuette. In so doing, a POSITA would have been simply translating Schuette's teachings to the context of the Takahashi-Tsern device.

174. Schuette describes that this “more precise” approach “maintain[s] a consistent voltage drop across all levels of load and power draw,” such that a POSITA would have had a reasonable expectation of success in obtaining Vio from VPPL or VDD. EX1006, [0029]. Indeed, incorporating a “diode” or a “linear regulator circuit of a known type in the art” to lower Takahashi's VPPL or VDD by 0.2 to 0.4 V as described by Schuette would have involved nothing more than the combination of known elements (known circuit elements operating on known voltages in similar devices) to yield predictable results (a “consistent” voltage drop). EX1006, [0029]. Viewed another way, this modification would have constituted merely the application of a known technique—generation of VDDQ/Vio from a core voltage—to a piece of prior art (Takahashi-Tsern) that is ready for the improvement, in that Takahashi already discloses the generation of multiple different internal voltages for different circuit components, and in that

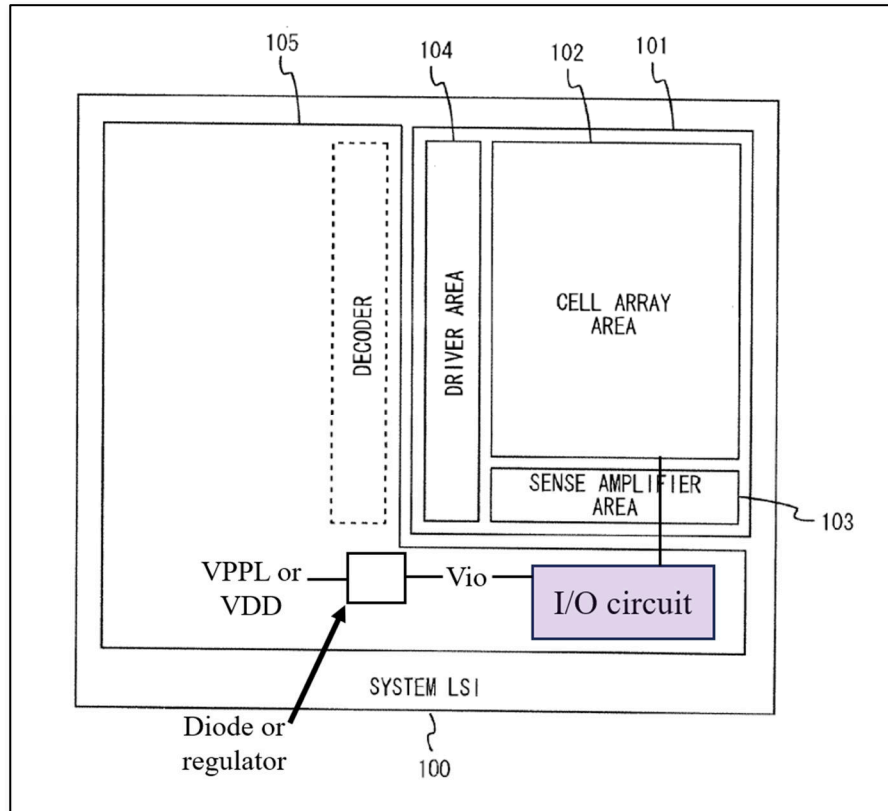
Tsern already discloses the use of a specific Vio for an I/O interface. Moreover, the use of a regulator circuit to generate Vio would have been in full agreement with Tsern's existing disclosure, which already describes "a collection of regulators that develops these and other necessary or desired core voltages from an externally supplied voltage Vdd." EX1005, [0032].

175. Additionally, this modification would have been consistent with Takahashi's existing design, which already incorporates three power supplies providing three distinct voltages to different circuitry. EX1004, [0084]. The use of another voltage Vio to power the I/O circuit, as taught by Tsern, would have constituted a minor change, especially since Schuette provides a simple and reliable circuit configuration (for example, the use of a diode or regulator) for "consistent[ly]...across all levels of load and power draw" obtaining Vio from an existing core voltage. EX1006, [0029].

176. A POSITA would have found this Vio even more obvious through comparison of Vio to Takahashi's VDD. Vio in a range from 0.6 to 0.8V (resulting from Schuette's disclosed voltage drop in comparison to Takahashi's VPPL=1.0V) would have resulted in a Vio matching, or similar to, Takashi's VDD=0.8V, which powers Takahashi's logic circuit 105, driver area 204, and sense amplifier area 103. EX1004, [0045], FIG. 7. Accordingly, the modification of Takahashi based on Tsern and Schuette would have entailed providing an I/O circuit with a voltage Vio

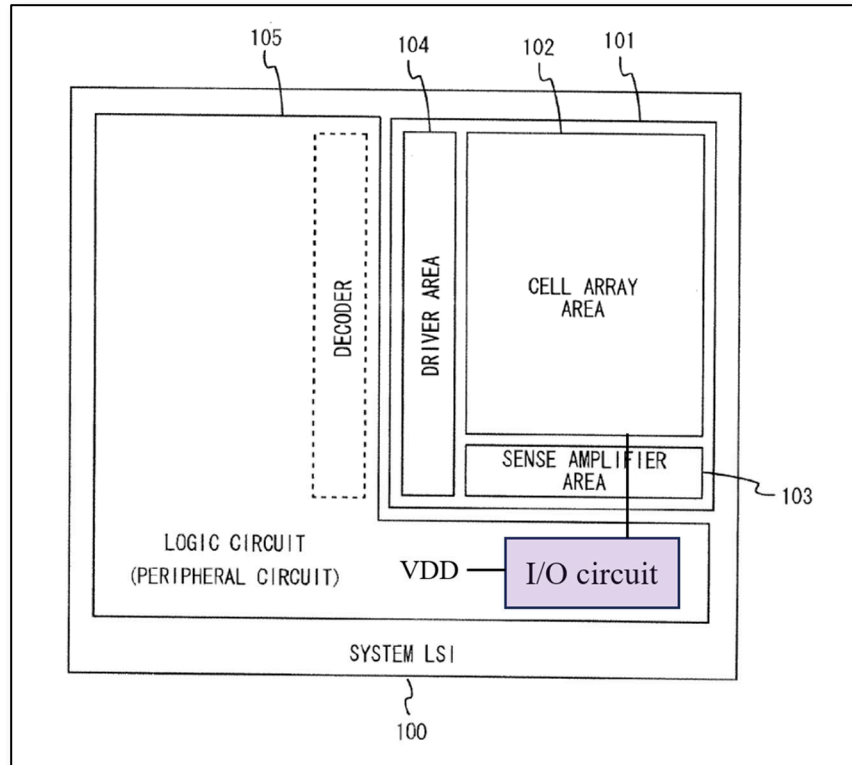
matching, or close to, the voltage already disclosed as being provided to components of Takahashi's DRAM. Indeed, a POSITA would have found it especially obvious to choose $V_{io}=V_{DD}=0.8V$, in which case V_{DD} could be directly applied as the power supply voltage for the I/O circuit, reducing the amount of circuit reconfiguration or modification required to include the input/output circuit.

177. As a result of this obvious modification of Takahashi, a POSITA would have arrived at the Takahashi-Tsern-Schuette device shown below, in which V_{PPL} or V_{DD} is lowered by a diode or regulator and supplied to the I/O circuit as V_{io} .



Takahashi-Tsern-Schuette device

178. In the specific case where VDD is used as Vio (following Schuette's disclosure of a suitable voltage drop, which gives a value of $V_{io}=0.8V$, matching Takahashi's disclosed $VDD=0.8V$), the Takahashi-Tsern-Schuette device can be represented as shown below.



Takahashi-Tsurn-Schuette device

4. Analysis of claims

(a) Claim 3

[3.1]: A dynamic random access memory (DRAM), comprising:

179. *See [1.1] at §VII.A.2(a).*

[3.2]: a DRAM core cell comprised in the DRAM,

180. *See [1.2] at §VII.A.2(a).*

[3.3]: wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage,

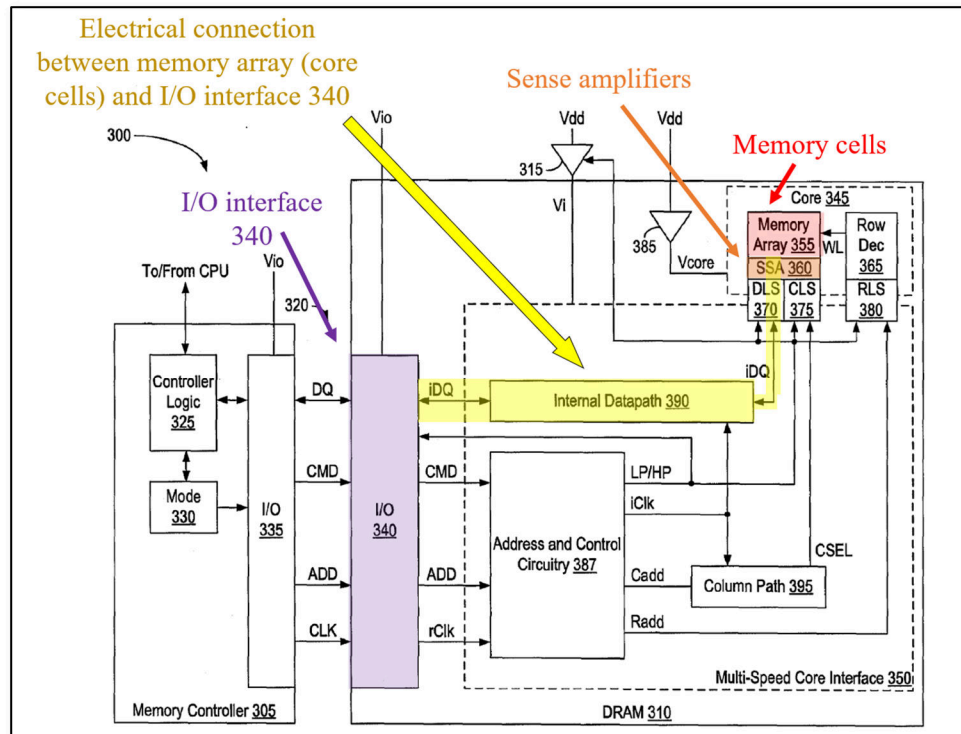
181. See [1.3] at §VII.A.2(a). Takahashi discloses a first voltage, VPPL, supplied to the memory cells of the cell array area 202. EX1004, [0081], [0083], FIGS. 7-8.

[3.4]: and the DRAM core cell is a volatile memory cell;

182. See [1.5] at §VII.A.2(a).

[3.5]: an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell,

183. As discussed in §VII.B.3(a), the Takahashi-Tsern-Schuette device includes an input/output circuit, which can be configured either for data exchange with the processing elements of the logic circuit 105 (§VII.B.3(a)(i)) or for data exchange with an off-chip device (§VII.B.3(a)(ii)). As a POSITA would have understood and found obvious, the I/O circuit is electrically connected to the DRAM core cell (memory cell of the cell array area 202) so as to provide for, as Tsern describes, “the flow of signals between I/O interface 340 and memory core 345.” EX1005, [0037]. For example, Tsern describes an “[i]nternal datapath 390 [that] conveys the read data [stored in memory cells] to I/O interface 340.” EX1005, [0042]. The input/output circuit performs an input and/or output function with respect to the cell array area 202, e.g., transferring data into and out of the cell array area 202 (e.g., from/to the logic circuit 105 or an off-chip device).

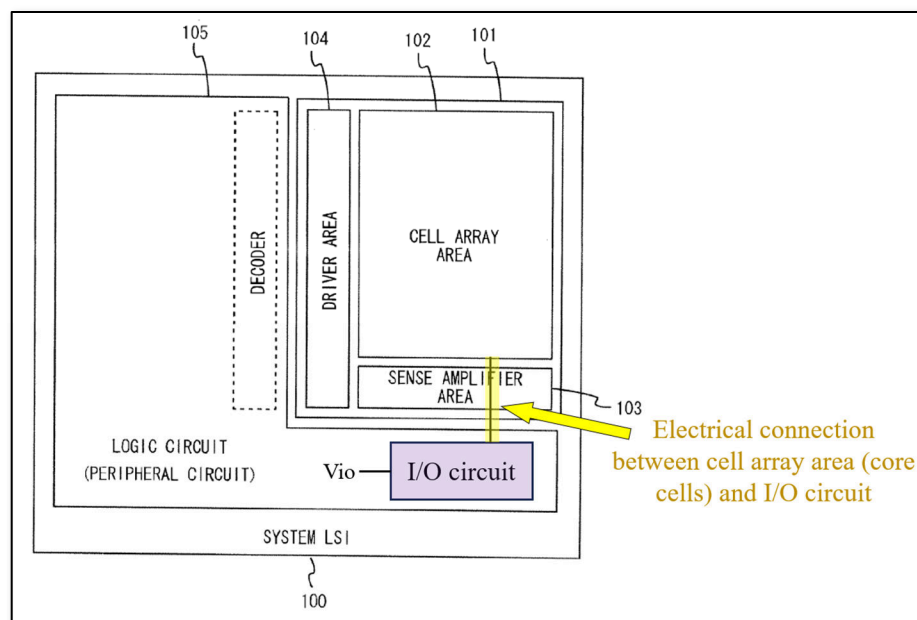


Tsern, FIG. 3

184. This internal datapath, which extends from the memory array 355, through sense amplifiers (SSA) 360, and to the I/O interface, is an electrical connection between the memory cells and the I/O interface. For example, data read from memory cells of the memory array 355 is sensed by the secondary sense amplifiers 360, level-shifted by a data level shifter 370, and provided out through the internal datapath 390 to the I/O interface 340. EX1005, [0037]-[0048], FIG. 3.

185. For the Takahashi-Tsern-Schuette device, it would have been obvious for a POSITA to provide a similar electrical connection between the I/O circuit and the cell array area 202 through the sense amplifier area 103, as shown below, to permit data readout/writing. This configuration would have been consistent with

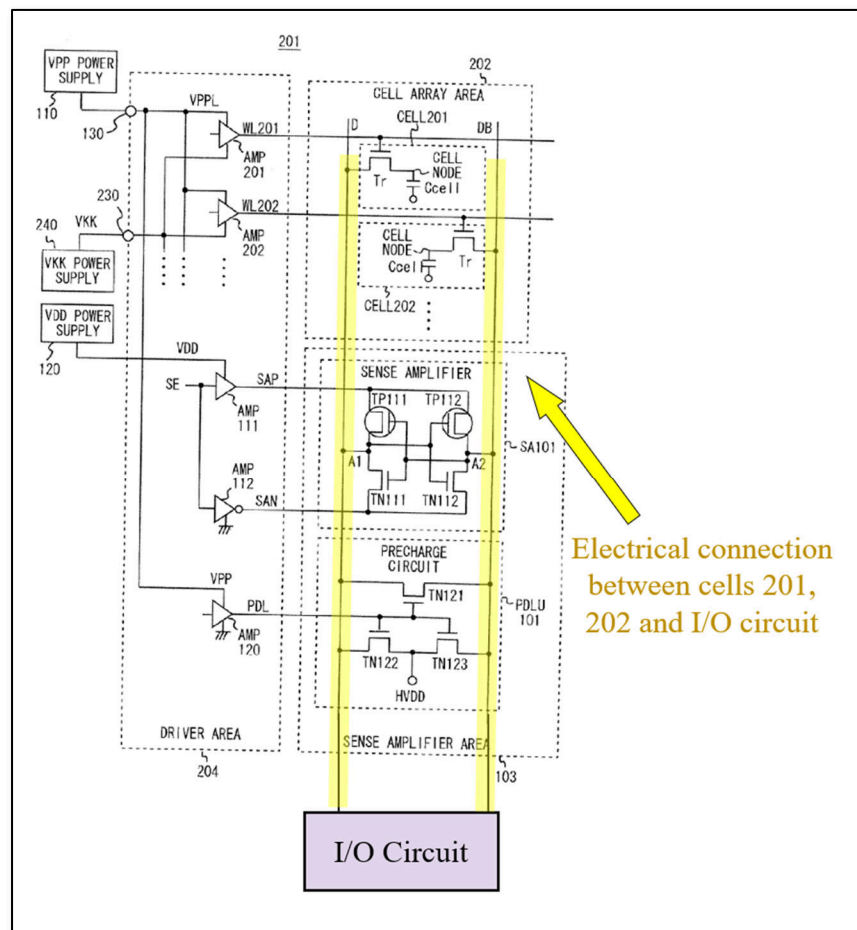
the well-understood, standard configuration of DRAM devices, which near-universally included electrical connections from memory cells, through sense amplifiers, and to I/O circuitry to permit data writing and readout. *See*, e.g., the textbook EX1012’s illustration of I/O circuitry (I/O buffers) electrically connected to the cell matrix in a “DRAM function diagram;” Dono’s illustration of an electrical connection between I/O circuit 90 and the memory cell array; and the illustrated electrical connection to “Input-Output” in the reference diagram supplied by the applicant during prosecution, as discussed in §VII.A.2(a). EX1012, FIG. 1.1; EX1008, FIG. 1; EX1016, 73.



Takahashi-Tsern-Schuette device

186. To provide a specific example, a POSITA would have found it obvious to connect the I/O circuit to the bitlines D and DB, which are themselves connected to the memory cell array. EX1004, FIG. 7. Takahashi describes that, in a

data read process, “the amplifie[d] potential difference between the pair of bit lines D and DB is read out as high-level readout data of the semiconductor memory circuit 201 by an external circuit, and is used for data processing and the like of the logic circuit 105.” EX1004, [0086]. That is, data is output on the bitlines, and the “external circuit” reads out the data. Thus, one obvious configuration of the I/O circuit would have been to electrically connect the I/O circuit to the memory cells through the bitlines D and DB, as shown below, so that the I/O circuit would have access to the data on the bitlines D and DB.



Takahashi-Tsern-Schuette device

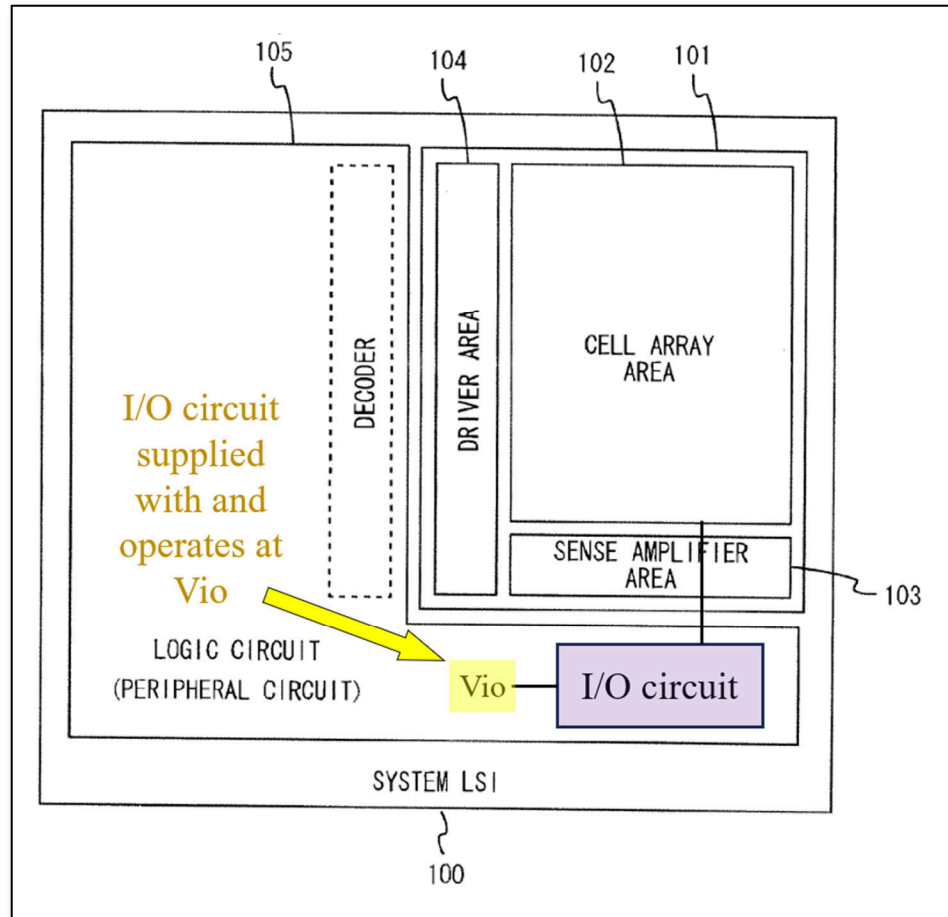
187. Accordingly, the Takahashi-Tsern-Schuette device, which is a DRAM device, includes an input/output circuit electrically connected to the DRAM core cell (memory cell of cell array area 202) and to the peripheral circuit (e.g., to the sense amplifier area 103 through the bitlines).

188. A POSITA would also have understood and found obvious that the I/O circuit of the Takahashi-Tsern-Schuette device is “comprised in the DRAM,” i.e., considered part of the DRAM. This comports with standard terminology and usage in the art, in which “a DRAM” includes not only the memory cells themselves but also peripheral and I/O circuitry. *See*, e.g., EX1005, FIG. 5 (showing a “DRAM 310” including “I/O interface 340”); EX1008, FIG. 1 (showing “a DDR SDRAM” 10 as including a “data I/O circuit 90”); EX1009, FIG. 2; EX1010, FIG. 6; EX1012, FIG. 1.1.

[3.6]: and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage,

189. As discussed in §VII.B.3, the input/output circuit of the Takahashi-Tsern-Schuette device is supplied with, and operates at, a third voltage V_{io} . EX1005, [0043], [0070]. For example, Tsern describes that the I/O interface 340 “rel[ies] upon a supply voltage V_{io} .” EX1005, [0043]. The reliance on V_{io} would have been understood by a POSITA as operation at V_{io} , because the I/O circuit

would operate in response or, or based on receiving, V_{io} , and would be powered by V_{io} .



Takahashi-Tsern-Schuette device

[3.7]: wherein the third voltage is lower than 1.1V; and

190. As discussed in §VII.B.3, V_{io} has a drop of “about 0.2 to about 0.4 volts” compared to the core voltage, which is VPPL or VDD in the Takahashi-Tsern-Schuette device. EX1006, [0029]. VPPL is 1.0V, and VDD is 0.8V. EX1004, [0084]. Therefore, V_{io} is in a range from about 0.6 V to about 0.8 V, or from about 0.4 V to 0.6 V, lower than 1.1 V.

[3.8]: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell,

191. See [1.6] at §VII.A.2(a). Like Takahashi's unmodified device, and following the interpretation provided by the applicant during prosecution, the Takahashi-Tsern-Schuette device includes several peripheral circuits electrically connected to the DRAM core cell, including the "sense amplifier area 103" (e.g., "sense amplifier SA101"), the "driver area 204" (e.g., driver amplifier AMP111), and/or at least a portion of the "logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201" (e.g., the "address decoder of the semiconductor memory circuit."). EX1004, [0044], [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7. The inclusion of the I/O circuit in the Takahashi-Tsern-Schuette device would have been entirely compatible with the retention of these circuits, as DRAMs conventionally included I/O circuitry along with sense amplifiers, drivers, and logic circuits (e.g., decoders).

[3.9]: and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage,

192. See [1.7] at §VII.A.2(a). The peripheral circuit of the Takahashi-Tsern-Schuette device is supplied with and operates at a second voltage VDD, which is provided to each of the peripheral circuits: sense amplifier area 103,

driver area 204, and logic circuit 105 (e.g., the decoder thereof). EX1004, [0045], [0052], [0055]-[0056], [0086], FIGS. 7-8.

[3.10]: wherein the second voltage is lower than 1.1 V and the first voltage is different from the second voltage;

193. See [1.8] at §VII.A.2(a). Takahashi discloses that the second voltage VDD (=0.8 V) is lower than 1.1 V and different from the first voltage VPPL (=1.0V). EX1004, [0078], [0084], FIG. 8.

[3.11]: wherein the DRAM core cell and the input/output circuit are formed on a single chip,

194. See [1.9] at §VII.A.2(a). As discussed in detail in that section, Takahashi describes an integrated device, formed on a single chip, that includes the cell array area 102 (202 in the FIG. 7-10B embodiment), the sense amplifier area 103, the driver area 104 (204), and the logic circuit 105. For example, Takahashi describes that a “semiconductor memory circuit...and a logic circuit...are integrated into one chip.” EX1004, [0018]. When an I/O circuit is incorporated into the Takahashi-Tsern-Schuette device, the I/O circuit is formed on a single chip with the DRAM core cell (memory cell of cell array area 202), because these elements are on a common “LSI chip” and are “integrated into one chip.” EX1004, [0018], [0043], FIG. 1.

195. Further, forming the I/O circuit on a single chip with the DRAM core cell would have been the most obvious configuration of the I/O circuit.

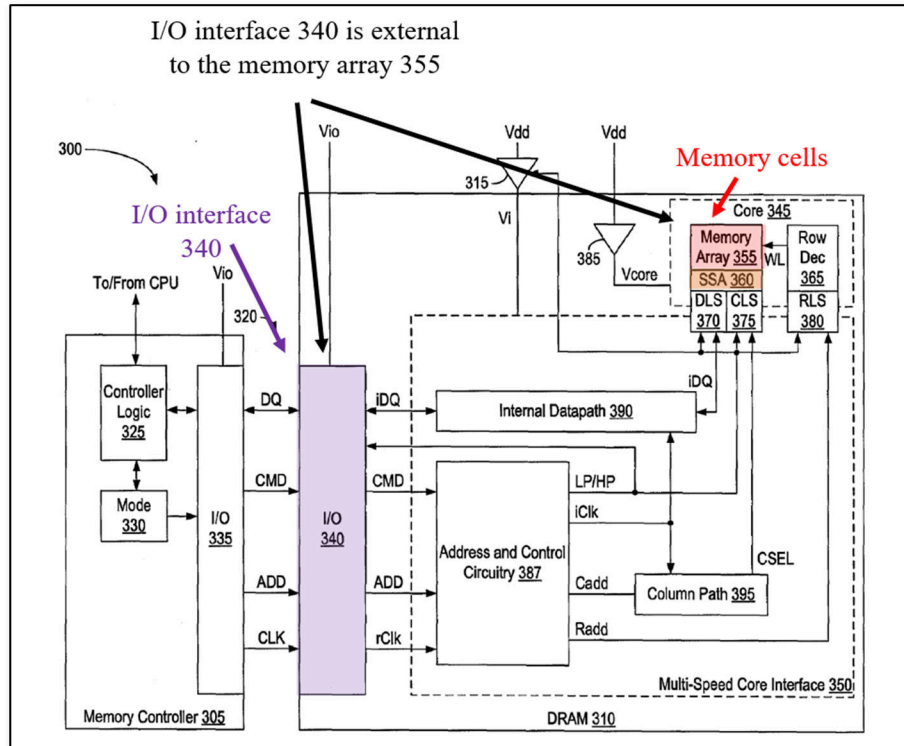
Takahashi's memory cells and processing elements of the logic circuit 105 are formed on the same chip, so an I/O circuit configured for data exchange between these elements would naturally also be formed on that same chip. As another example, in the case where the I/O circuit is configured for off-chip communication, the I/O circuit would, by definition, be formed on the same chip as the memory cells.

196. It also would have been obvious to a POSITA to form the I/O circuit on a single chip with the DRAM core cell because this configuration is described for the I/O interface 340 in Tsern and was associated with well-known advantages. For example, Tsern describes that "memory controller 305 and DRAM 310 are on separate ICs [integrated circuits]," and that the I/O interface 340 and the memory core 345 (which includes memory array 355) are in the DRAM 310. EX1005, [0034]-[0035], FIG. 3. A POSITA, from this description, would have understood and found obvious that the memory core 345 and the I/O interface 340 are formed on a single chip. It would have been obvious to apply this configuration to the Takahashi-Tsern-Schuetz device (i) as the most obvious choice of placement of the I/O circuit, because it matches the placement of the corresponding circuit in Tsern, and (ii) to achieve the well-known benefits of integration on a single chip.

Such benefits included, for example, lower loss associated with inter-chip signal transmission, manufacturing simplicity and economy, and signal delay reduction. Indeed, Takahashi describes that “there is a demand for higher levels of integration,” i.e., forming more components together on a single chip. EX1004, [0018]. To meet this demand, and following the descriptions of Takahashi and Tsern, it would have been obvious to a POSITA to form the I/O circuit of the Takahashi-Tsern-Schuette device on a single chip.

[3.12] and the input/output circuit is external to the DRAM core cell,

197. A POSITA would have found it obvious to have the I/O circuit of the Takahashi-Tsern-Schuette device be external to the DRAM core cell (memory cell of cell array area 202). First, this matches the configuration described by Tsern, in which the I/O interface 340 is external to the memory array 355, as shown below. EX1005, FIG. 3. A POSITA seeking to incorporate I/O circuitry into Takahashi’s device would have found it obvious to use the configuration described by Tsern, in view of its apparent and disclosed success in Tsern’s DRAM.

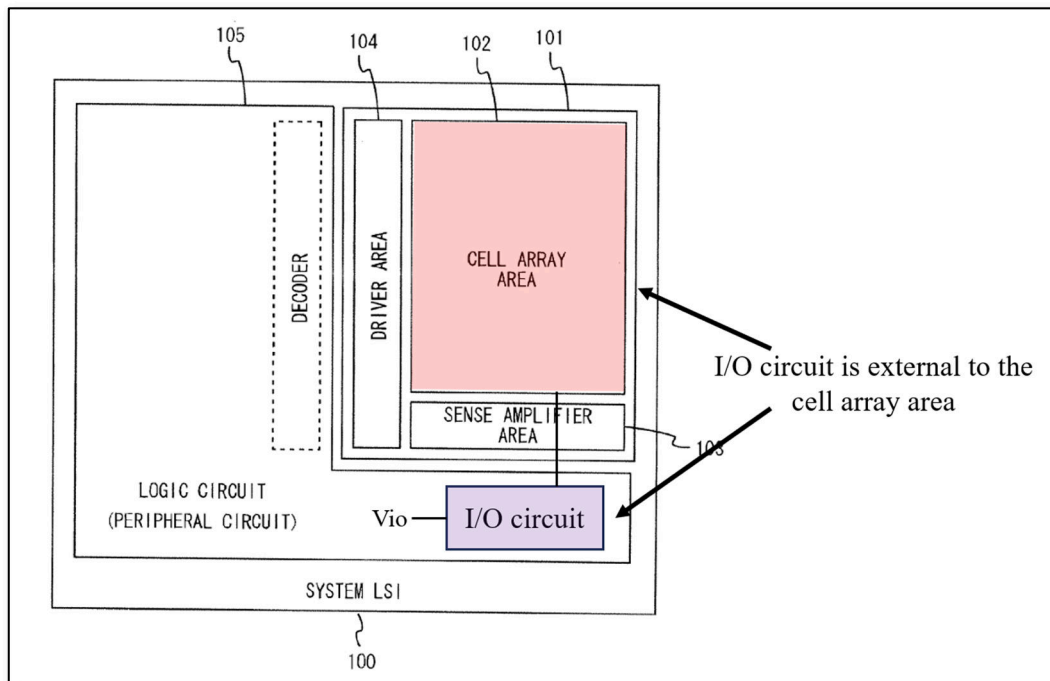


Tsern, FIG. 3

198. This configuration also matches the configuration of the “external circuit” that is an example of an I/O circuit of the Takahashi-Tsern-Schuette device. EX1004, [0086]. The “external circuit” would have been understood by a POSITA as external to the cell array area 202.

199. Moreover, a POSITA would have understood that I/O circuitry of a DRAM is essentially always external to the core memory cells that store data. To maximize data storage capacity, DRAM memory cells are arranged in dense arrays with rows of wordlines and columns of bitlines. Providing I/O circuitry *internal* to a DRAM core cell would interfere with that dense arrangement and reduce storage capacity. Further, each DRAM core cell is a relatively small, simple circuit (for

example, one transistor and one capacitor in the example of Takahashi), and providing an I/O circuit internal to that simple structure would have been a very unlikely arrangement for a POSITA incorporating the I/O circuit into a DRAM. EX1004, FIG. 7. It would have been obvious to apply this essentially universal configuration in the Takahashi-Tsern-Schuette device, as shown below:



Takahashi-Tsern-Schuette device

[3.13] and wherein the first voltage is different from the third voltage.

200. See [3.3] and [3.7]. The first voltage is $VPPL=1.0$ V. EX1004, [0084], FIGS. 7-8. The third voltage is V_{io} , which is reduced compared to the core voltage ($VPPL$ or VDD) by “about 0.2 to about 0.4 volts.” EX1006, [0029]. Thus, V_{io} is in a range from about 0.6 to about 0.8 V, or from about 0.4 to about 0.6 V, different from the first voltage $VPPL=1.0$ V.

(b) **Claim 4**

[4]: The dynamic random access memory of claim 3, wherein the first voltage is lower than 1.1V.

201. See [3.3] at §VII.B.4(a) and [1.3], [1.5] at §VII.A.2(a). Takahashi discloses a first voltage of VPPL = 1.0 V, lower than 1.1 V.

(c) **Claim 5**

[5]: The dynamic random access memory of claim 3, wherein the first voltage is different from the second voltage.

202. See [3.10] at §VII.B.4(a). This element is recited identically in claim 3 and addressed above.

(d) **Claim 6**

[6.1]-[6.4]: See [1.1]-[1.4] at §VII.A.2(a).

[6.5]-[6.7]: See [3.5]-[3.7] at §VII.B.4(a).

[6.8]: wherein the first voltage is greater than the third voltage, and

203. See [3.13] at §VII.B.4(a). In the Takahashi-Tsern-Schuette device, the first voltage is VPPL=1.0 V. EX1004, [0084], FIGS. 7-8. The third voltage is Vio, which is reduced compared to the core voltage (VPPL or VDD) by “about 0.2 to about 0.4 volts.” EX1006, [0029]. Thus, Vio is in a range from about 0.6 to about 0.8 V, or from about 0.4 to about 0.6 V, lower than the first voltage VPPL=1.0V.

[6.9]: the DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP).

204. For the reasons discussed in §VII.A.2(f) for Ground 1A, a POSITA would have understood and found obvious that the Takahashi-Tsern-Schuette device, operating with the first voltage VPPL and the third voltage Vio, is capable of being applied to an eDP. The Takahashi-Tsern-Schuette device is “capable” of being applied in this way because it is a working, conventional DRAM that is capable of satisfying the requirements of the eDP 1.3 standard, which do not include any voltage or power requirements. EX1014. The eDP 1.3 standard requires that the frame buffer store and provide data representing a static image. EX1014. The Takahashi-Tsern-Schuette DRAM, which stores data and supports read and write operations, is more than capable of fulfilling these requirements. EX1004, [0086].

205. Further, based on the obvious inclusion of an I/O circuit as discussed in §VII.B.3(a)(ii), the Takahashi-Tsern-Schuette device is configured to receive data from and transmit data to off-chip devices, enhancing its applicability as a frame buffer in an eDP configuration. For example, the Takahashi-Tsern-Schuette device, operating with VPPL and Vio, would be capable of receiving frame data through the I/O circuit from an off-chip memory controller, storing the frame data in memory cells, and outputting the frame data from the memory cells through the I/O circuit to the off-chip memory controller, for presentation on a display.

206. In addition, to the extent the '098 Patent erroneously links “capable of being applied to an embedded display port (eDP)” to low-voltage operation, then the Takahashi-Tsern-Schuette device, which has first (VPPL) and third (Vio) voltages that satisfy the “< 1.1 V” condition of the '098 Patent, would be equally as capable of being applied to an eDP as the '098 Patent's devices. EX1001, 4:61-5:9, Table III. *See* discussion for [6.8], which describes VPPL and Vio values.

(e) **Claim 7**

[7]: The dynamic random access memory of claim 6, wherein the first voltage is lower than 1.1 V.

207. *See* [1.5] at §VII.A.2(a). The first voltage of the Takahashi-Tsern-Schuette device is VPPL=1.0 V, lower than 1.1 V. EX1004, [0083]-[0084], FIGS. 7-8.

(f) **Claim 8**

[8]: The dynamic random access memory of claim 6, further comprising: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1 V.

208. *See* [1.6]-[1.8] at §VII.A.2(a) and [3.8]-[3.10] at §VII.B.4(a). Peripheral circuits of the Takahashi-Tsern-Schuette device include the “sense

amplifier area 103” (e.g., “sense amplifier SA101”), the “driver area 204” (e.g., driver amplifier AMP111), and/or at least a portion of the “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201” (e.g., the “address decoder of the semiconductor memory circuit.”). EX1004, [0044], [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7. These circuits operate at a second voltage $V_{DD}=0.8$ V, which is lower than 1.1 V. EX1004, [0078], [0084], FIG. 8. Further, these peripheral circuits are electrically connected to the DRAM core cell, as discussed for [1.6] in §VII.A.2(a).

(g) **Claim 9**

[9]: The dynamic random access memory of claim 8, wherein the first voltage is different from the second voltage.

209. See [1.5], [1.8], and [1.11] at §VII.A.2(a), and [3.10] at §VII.B.4(a). In the Takahashi-Tsern-Schuetz device, the second voltage V_{DD} ($=0.8$ V) is different from the first voltage V_{PPL} ($=1.0$ V). EX1004, [0078], [0084], FIG. 8.

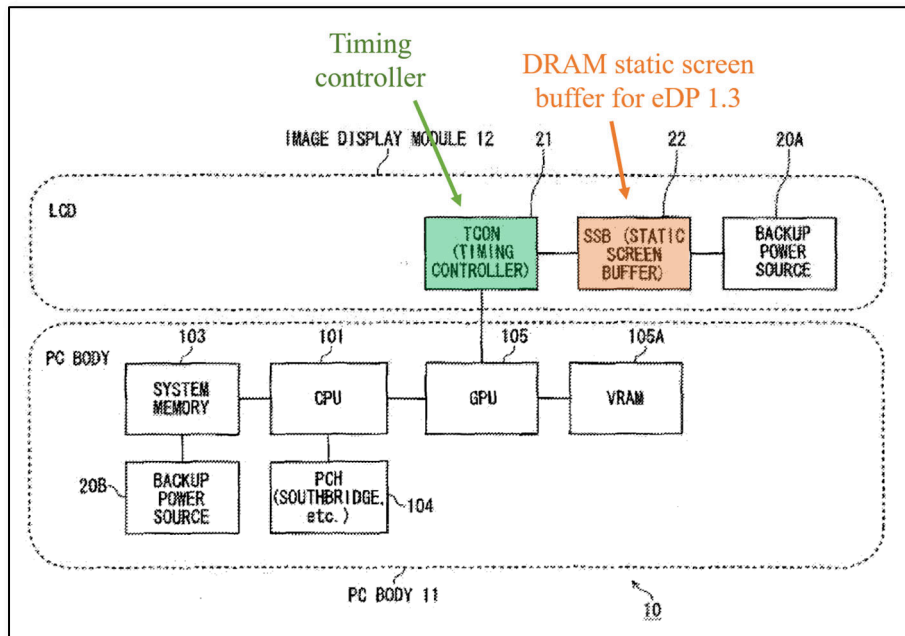
C. [Ground 1C] Takahashi and Endo render obvious claims 6-9

1. Endo

210. Endo is directed to electronic devices with displays, such as laptops and phones. EX1007, [0020]-[0022], FIG. 1. Endo identifies that “an issue having been challenged in the related art is to decrease the time required when the electronic apparatus is returned to the active state after being resumed.” EX1007,

[0004]. Thus, Endo provides configurations that “decrease the time...required for [] resume processing.” EX1007, [0077].

211. FIG. 3 of Endo illustrates an electronic apparatus 10 that includes an image display module 12. EX1007, [0023], FIG. 3. The image display module 12 includes a timing controller (TCON) and a static screen buffer (SSB). EX1007, [0029], FIG. 3. Endo describes that the “static screen buffer (SSB) 22 is a memory defined as Embedded DisplayPort (eDP) version 1.3” and that the “SSB 22 is constituted by, for example, dynamic random access memory (DRAMs).” EX1007, [0034]-[0035]. A POSITA would have understood and found obvious that this “static screen buffer” is the same as the “remote frame buffer” of the eDP 1.3 standard and the “frame buffer” of the '098 Patent. For example, the frame buffer handles a “still video image,” i.e., a “static” display screen. EX1015, 25. Further, Endo describes that the static screen buffer “is a memory defined as [eDP] 1.3,” and the eDP 1.3 standard does not describe any other display(panel)-located buffers that Endo might be attempting to refer to, besides the remote frame buffer. EX1007, [0034]; EX1014.



Endo, FIG. 3

2. Obviousness of claims 6-9

212. As discussed in §VII.A.2, Takahashi anticipates and renders obvious claims 6-9. Those claims are further obvious over Takahashi in view of Endo’s teachings, which further demonstrate that it would have been obvious for Takahashi’s device to be “capable of being applied to an embedded display port (eDP),” as recited in claim 6.

213. Specifically, Endo explicitly teaches the use of “DRAMs” as the frame buffer of eDP 1.3 devices. EX1007, [0034]-[0035]. Endo also describes how an apparatus in which the frame buffer is a DRAM can be specially configured to facilitate the DRAM: the apparatus can include a backup power source 20A that maintains storage of data in the volatile DRAM, even when the device is switched to a standby power state. EX1007, [0035], [0038], FIG. 3. A POSITA would have

known that DRAM, as a volatile memory, requires a power source in order to retain stored data, e.g., to support refresh operations. Endo specifically accounts for this DRAM characteristic, describing that “since the power is continuously supplied from, for example, a backup power source...even through the electronic apparatus 10 is in a standby state, it is possible to maintain data of, for example, displayed information of the image display module 12.” EX1007, [0035]. Note that the backup power source 20A is connected specifically to the static screen buffer 22, making clear that the DRAM static screen buffer is the recipient of the backup power. EX1007, FIG. 3. In view of this specific power configuration suited specifically for DRAM memory, a POSITA would have had a reasonable expectation of success in using Takahashi’s DRAM as the frame buffer.

214. In view of Endo, a POSITA would have further found it obvious that Takahashi’s DRAM is capable of being applied to an eDP, would have been further motivated to apply that DRAM to an eDP to obtain the benefits discussed above (e.g., the power reduction benefits provided by the RFB of the eDP 1.3 standard, the benefits of conforming to the eDP 1.3 standard, and the benefits provided by the use of DRAM as discussed in §VII.A.2(f)), and would have reasonably expected success in doing so. Indeed, Endo discloses the use of a DRAM for that purpose, without disclosing any specific requirements or characteristics of the DRAM. EX1007, [0034]-[0035]. That is, Endo describes the

use of a DRAM as an eDP 1.3 frame buffer, without specifying, or suggesting in any way, that the DRAM must satisfy the low-voltage or low-power requirements incorrectly described by the '098 Patent. Takahashi's memory is a DRAM. Thus, based on Endo, it would further have been obvious to a POSITA to apply a DRAM, such as Takahashi's, to an eDP, e.g., as the frame buffer.

D. [Ground 1D] Takahashi, Tsern, Schuette, and Endo render obvious claims 6-9

1. Obviousness of claims 6-9

215. Endo is applied here as discussed for Ground 1C in §VII.C.2. As discussed in §VII.B, Takahashi, Tsern, and Schuette render obvious claims 6-9. In view of Endo's explicit disclosure of using a DRAM as the frame buffer in an eDP 1.3 device, a POSITA would have further found it obvious that the Takahashi-Tsern-Schuette DRAM is capable of being applied to an eDP, would have been further motivated to apply that DRAM to an eDP to obtain the benefits discussed above, and would have reasonably expected success in doing so. EX1007, [0034]-[0035].

E. [GROUNDS 2A and 2A.1] Dono and Goto render obvious claims 1-9; and Dono, Goto, and Youn render obvious claims 1-9

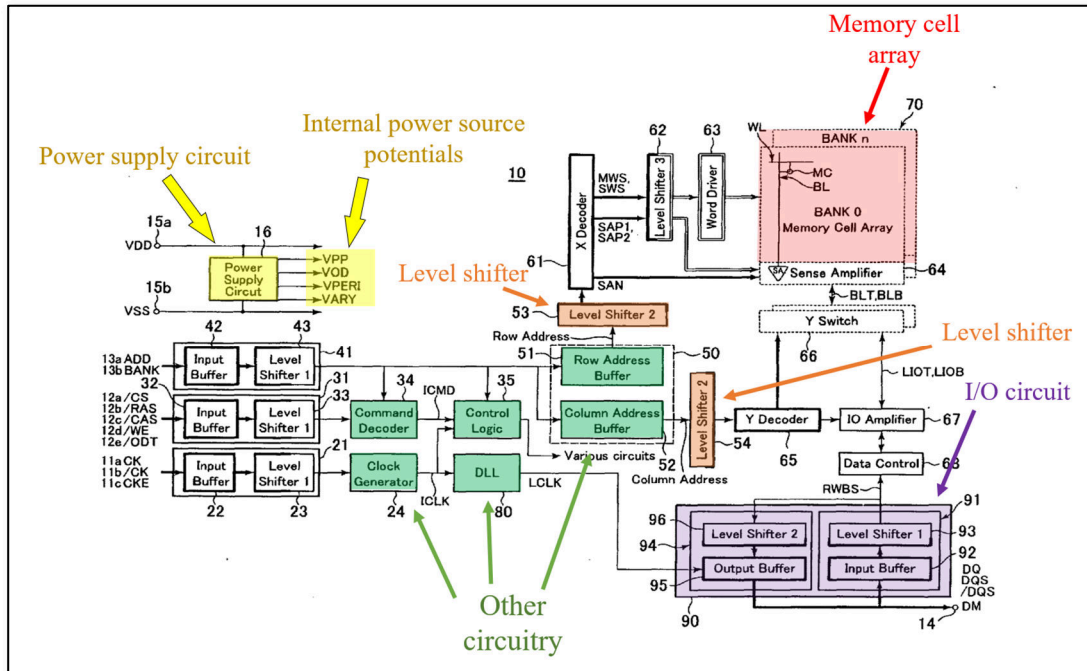
1. Dono

216. Dono is directed to “SDRAM” (synchronous dynamic random-access memory), a type of DRAM. EX1008, [0024]. The common double data rate (DDR) DRAM type referred to by the ’098 Patent is an example of an SDRAM, which incorporates a synchronous interface that syncs operations to master clock signal. EX1012, 29-30. The DRAM of FIG. 1 includes conventional elements such as a memory cell array 70, a sense circuit 64 including sense amplifiers, a data I/O circuit 90, an address controller 50, a delay-locked loop (DLL) circuit 80, and a control logic 35. EX1008, [0027], [0030], [0032], [0035], [0040], FIG. 1. These elements perform DRAM operations. For example, the address controller 50 includes buffers 51, 52 that latch rows and columns for cell addressing. EX1008, [0033], FIG. 1. Delay-locked loops are commonly used in DDR SDRAMs; the DLL circuit 80 “generates a phase-controlled internal clock LCLK” that is supplied to the I/O circuit 90. EX1012, 149; EX1008, [0027]. The control logic 35 includes a mode register and a refresh controller. EX1008, [0030].

217. To power internal components, Dono’s DRAM receives an externally-supplied voltage VDD at a power supply circuit 16, which “generates internal power source potentials VPP, VOD, VPERI, and VARY. These potentials have a size relationship of $VPP > VDD > VOD > VPERI \cong VARY > VSS$.” EX1008, [0042].

The outlines of circuit blocks of FIG. 1 (“thick line,” “normal line,” “double line,” and “broken line”) indicate which voltage is used (“handle[d]”) by each component. EX1008, [0043], FIG. 1. Some blocks (e.g., the first level shifters 23, 33, 43, 93) are drawn with multiple outlines to indicate that they receive multiple power supply voltages. EX1008, [0043]. For example, the level shifter 93 is illustrated with half-thick and half-normal lines, indicating that it receives both VDD and VPERI power supply voltages. EX1008, [0043], FIG. 1.

Correspondingly, FIG. 6 illustrates a level shifter that “is preferably used for the level shifters...93” and which receives each of VDD and VPERI at different power supply terminals. EX1008, [0076]-[0077], FIG. 6.

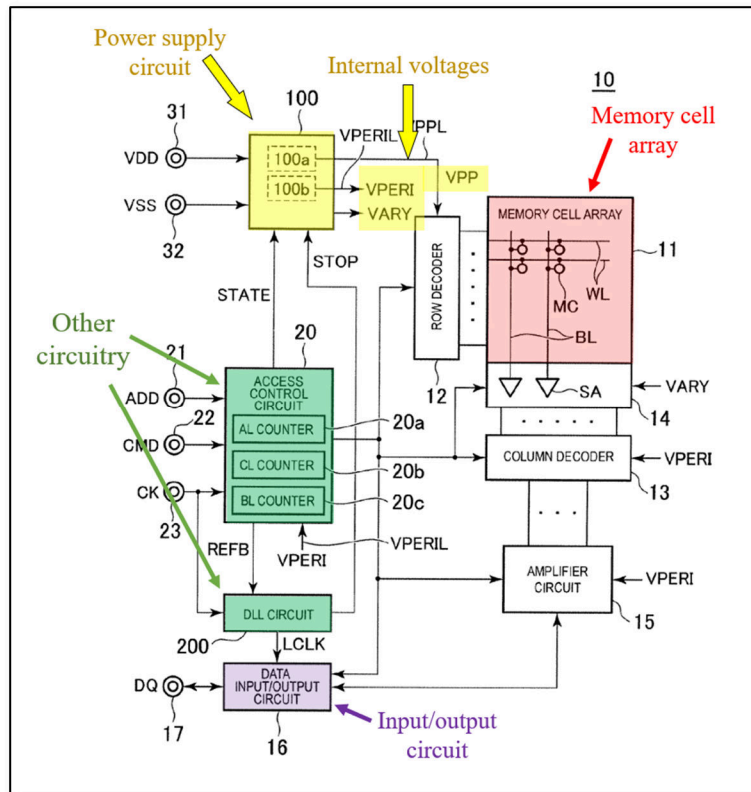


Dono, FIG. 1

2. Goto

218. Goto is a filing by the same applicant (“Elpida Memory, Inc.”) as Dono and, like Dono, relates to DRAM circuits. EX1009, [0022]. Goto’s FIG. 2 DRAM has a structure similar to Dono’s FIG. 1 DRAM shown above, including a memory cell array 11, a data input/output circuit 16, a DLL circuit 200, and an address control circuit 20. EX1009, [0022], FIG. 2. Both Dono and Goto illustrate an amplifier circuit, that receives V_{PERI} , connected between the I/O circuit and the memory cell array. EX1008, FIG. 1; EX1009, FIG. 2.

219. Also similar to Dono’s circuit, Goto’s DRAM includes a power supply circuit 100 that “generates internal voltages V_{PP} , V_{PERI} , [and] V_{ARY} .” EX1009, [0026]. These voltages have the same relative relationship as in Dono: “ $V_{PP} > V_{DD} > V_{PERI} \approx V_{ARY}$.” EX1009, [0026].



Goto, FIG. 2

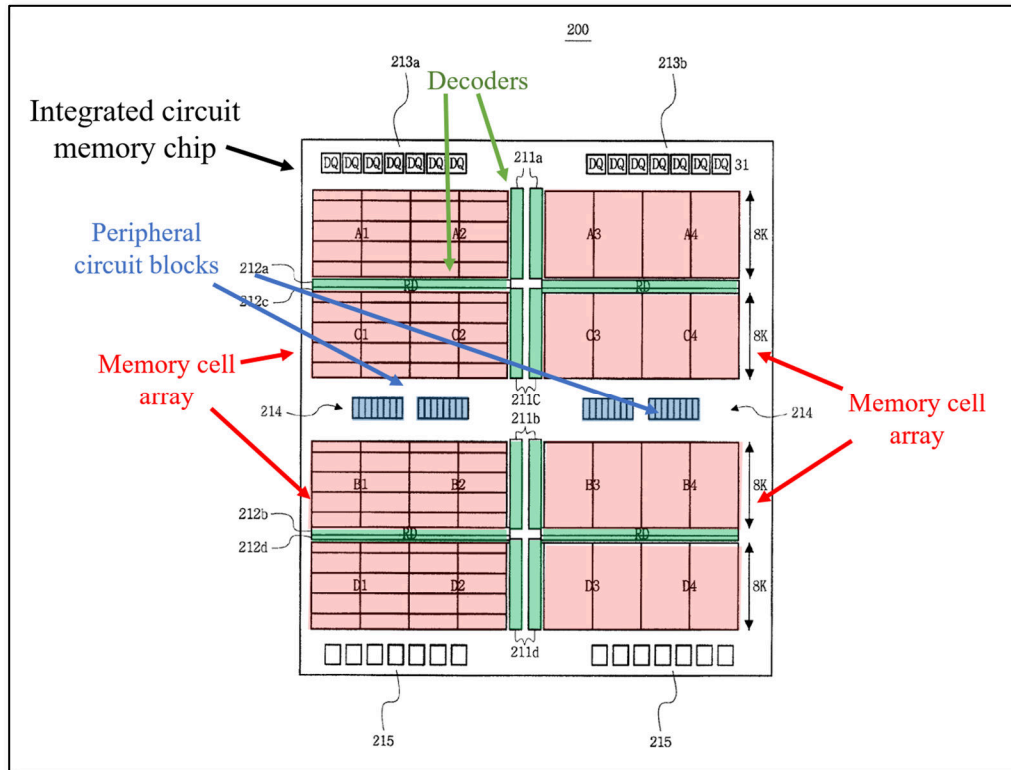
3. Youn

220. Youn is directed to “[m]ulti-bank semiconductor memory devices...having optimized memory block layouts and data line routing to enable chip size reduction and increase operating memory access speed.” EX1010, Abstract. In addition to diagrammatic representations of memory devices, Youn provides illustrations of physical memory chip layouts. EX1010, FIGS. 1A, 6. For example, FIG. 1A illustrates “a semiconductor memory device having a conventional hierarchical memory bank architecture” in the form of “a semiconductor integrated circuit memory chip.” EX1010, 1:48-52. The memory device can be a DRAM. EX1010, 2:26-27, 2:40-44; 5:51-59. A POSITA would

have understood and found obvious that this and other “semiconductor integrated circuit memory chip[s]” disclosed in Young are formed on a single chip, e.g., due to their use of the term “integrated,” the use of the singular “chip,” and the physical memory chip layouts showing specific locations of different components in each chip.

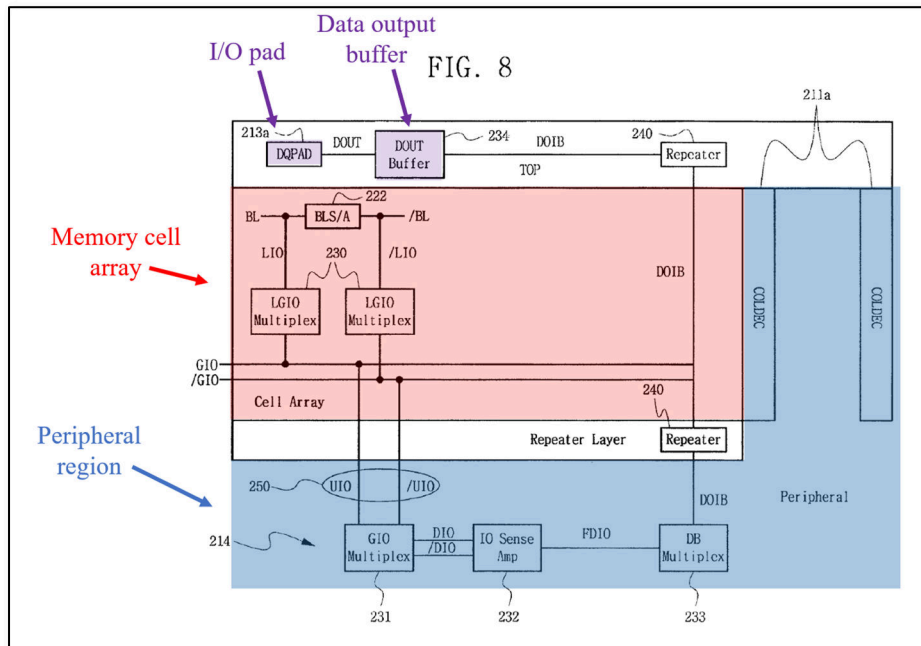
221. FIG. 6 “depicts an exemplary embodiment of the memory device of FIG. 1,” with a “more uniform layout” and a “shorten[ed] data path.” EX1010, 6:22-27. The reference to the shortened data path ties into well-understood advantages of integration that I note herein and that would have been understood by a POSITA as of the critical date: integration of different circuits on the same chip was generally desirable and advantageous because the on-chip data paths of such circuits were shorter and more efficient than inter-chip data paths, e.g., exhibiting shorter signal transmission delays, lower resistance, etc. As shown in annotated FIG. 6 below, “a semiconductor integrated circuit memory chip (200)” includes a “memory cell array...divided into a plurality of memory banks, Bank A, B, C and D.” EX1010, 5:59-62. The integrated circuit memory chip 200 also includes column decoders 211 and row decoders 212, along with “peripheral circuit blocks 214, and peripheral pads including I/O pads (213a, 213b) [and] control/address signal pads 215.” EX1010, 63-67. The row/column decoders are included in the peripheral circuits (note Youn’s disclosure that memory banks are

“operated with associated peripheral circuits including column decoders [] and row decoders”), and the peripheral circuits can also include “other I/O circuitry for outputting/inputting data via peripheral data I/O pads.” EX1010, 1:55-59.



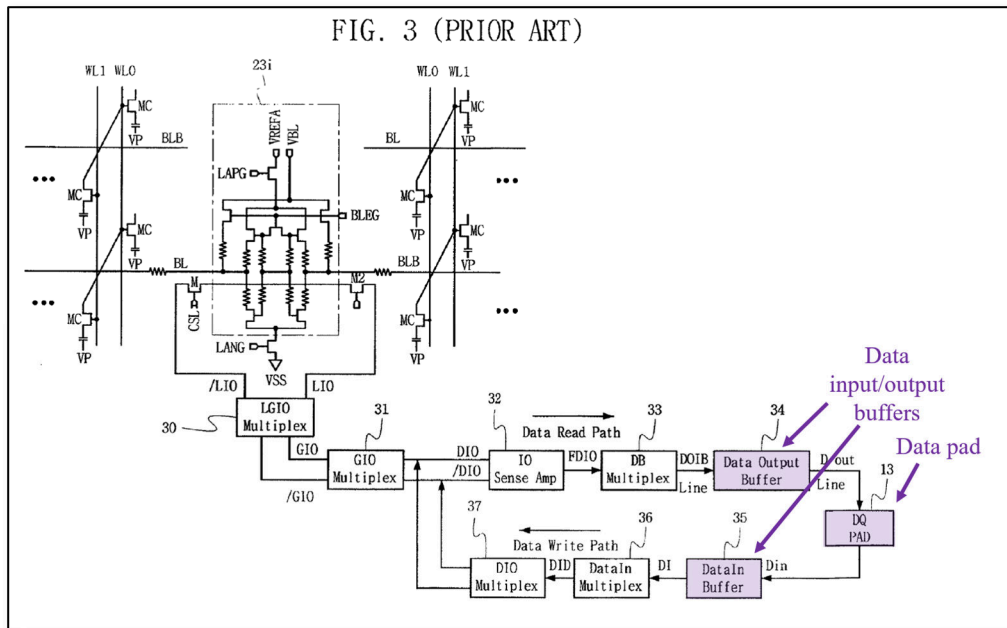
Youn, FIG. 6

222. FIG. 8 “illustrates an exemplary layout of the I/O circuitry and bus lines of the semiconductor device” 200 of FIG. 6. EX1010, 6:43-44. The I/O circuitry includes an “I/O pad” 213a and “DOUT [data output] buffer” 234. EX1010, 3:20, 7:1-2, FIG. 8. FIG. 8 also illustrates the memory cell array and a “peripheral region.” EX1010, 6:48-51, FIG. 8.



Youn, FIG. 8

223. Further illustration of I/O circuitry is provided in FIGS. 3 and 4. EX1010, 2:38-46. FIG. 3, for example, shows the DQ pad connected to I/O circuitry including a data output buffer 34 and a data input buffer 35, matching the configuration of Dono's I/O circuit 90. EX1008, FIG. 1; EX1010, FIG. 3.



Youn, FIG. 3

4. Analysis of claims

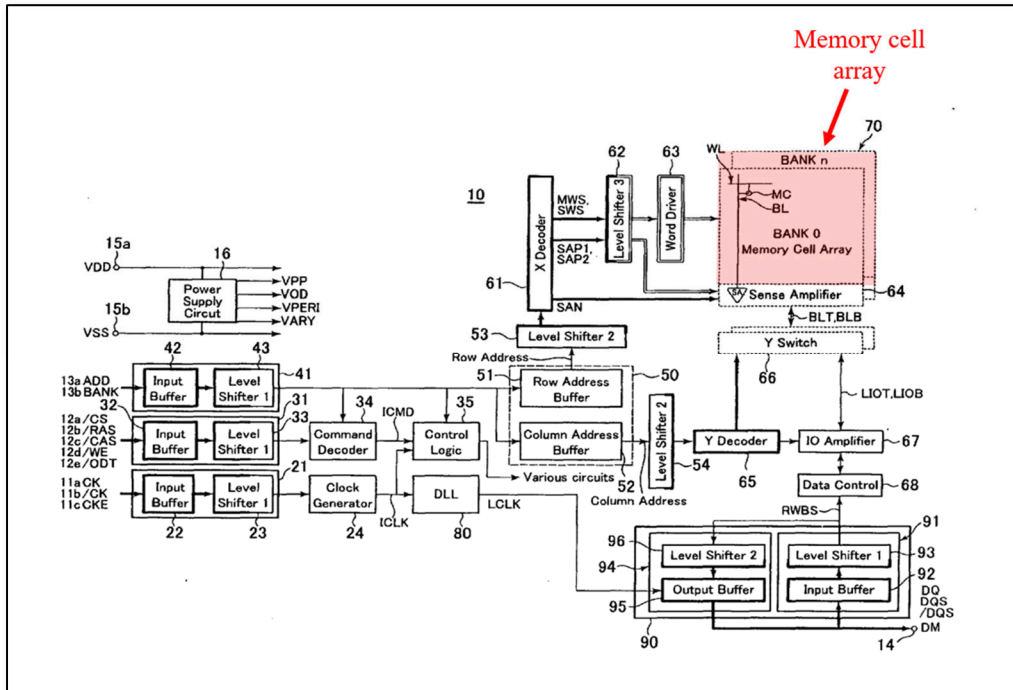
(a) Claim 1

[1.1]: A dynamic random access memory (DRAM), comprising:

224. Dono’s “semiconductor device 10” shown in FIG. 1 “is a DDR SDRAM,” i.e., a DRAM. EX1008, [0024], FIG. 1.

[1.2]: a DRAM core cell comprised in the DRAM,

225. Dono’s DRAM includes a “memory cell array 70 [that] includes dynamic memory cells MC arranged in a matrix.” EX1008, [0037], FIG. 1. These DRAM memory cells are each a DRAM core cell. *See* [1.2] in §VII.A.2(a) for discussion of why a POSITA would have understood and found obvious that a DRAM memory cell is a “core” cell.



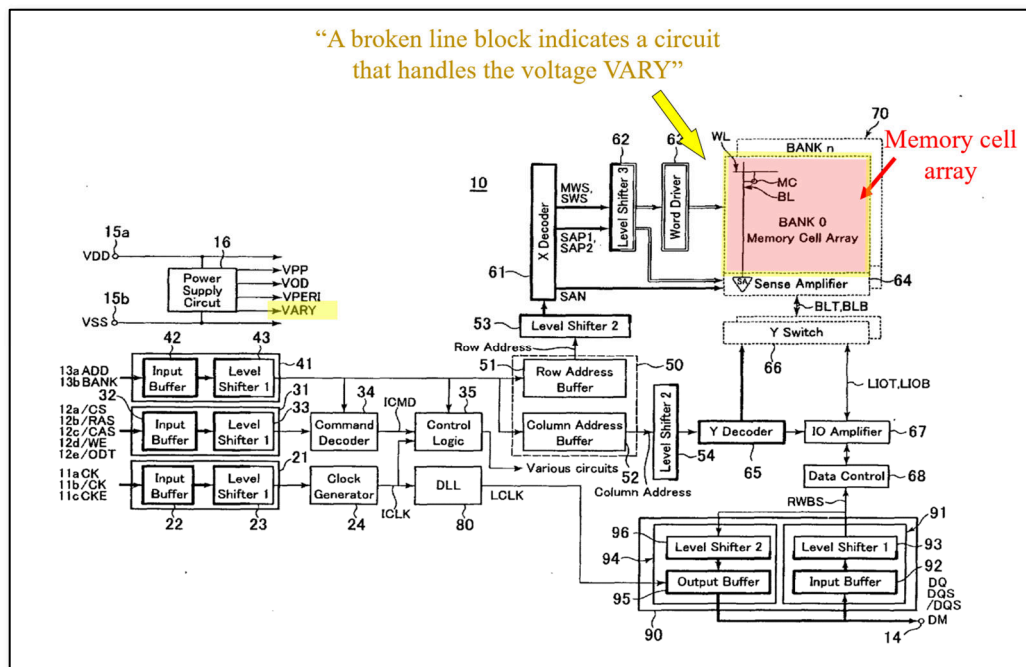
Dono, FIG. 1

[1.3]: wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage,

226. Dono's memory cells are supplied with, and operate at, a first voltage VARY. Dono describes VARY as an "array-system circuit voltage," in reference to the "array" of memory cells MC, to denote that this is the voltage at which the cells of the array operate. EX1008, [0005]. Further, Dono associates selection of VARY with "physical constants of memory cells, such as a memory cell capacitance," making clear that the memory cells themselves receive and operate at VARY. EX1008, [0005]. The "broken line" around the memory cell array 70 in FIG. 1 also illustrates that the memory cell array is powered by VARY: "a broken

line block indicates a circuit that handles the voltage VARY.” EX1008, [0043],

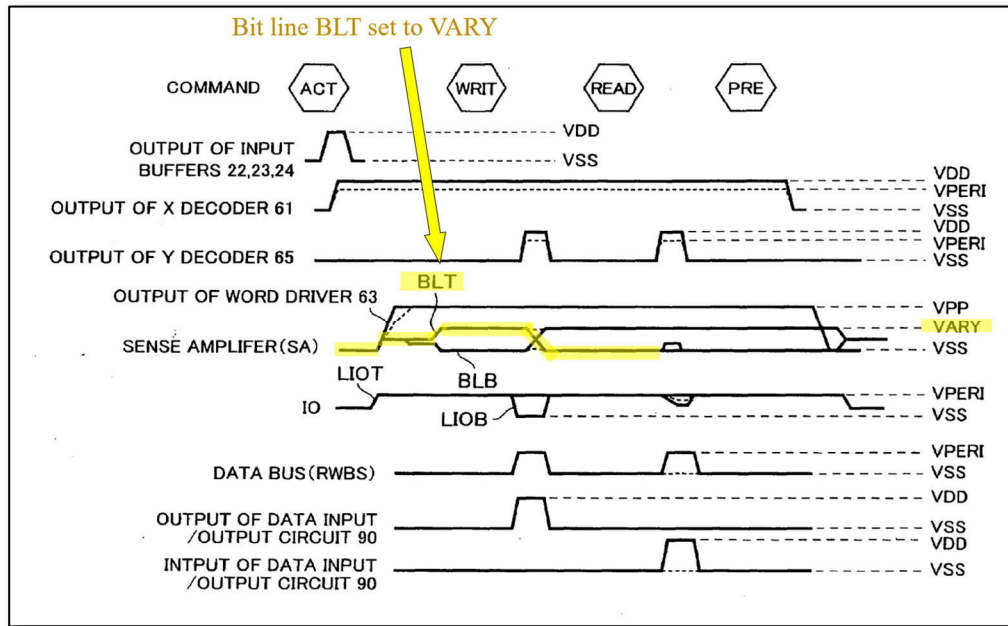
FIG. 1.



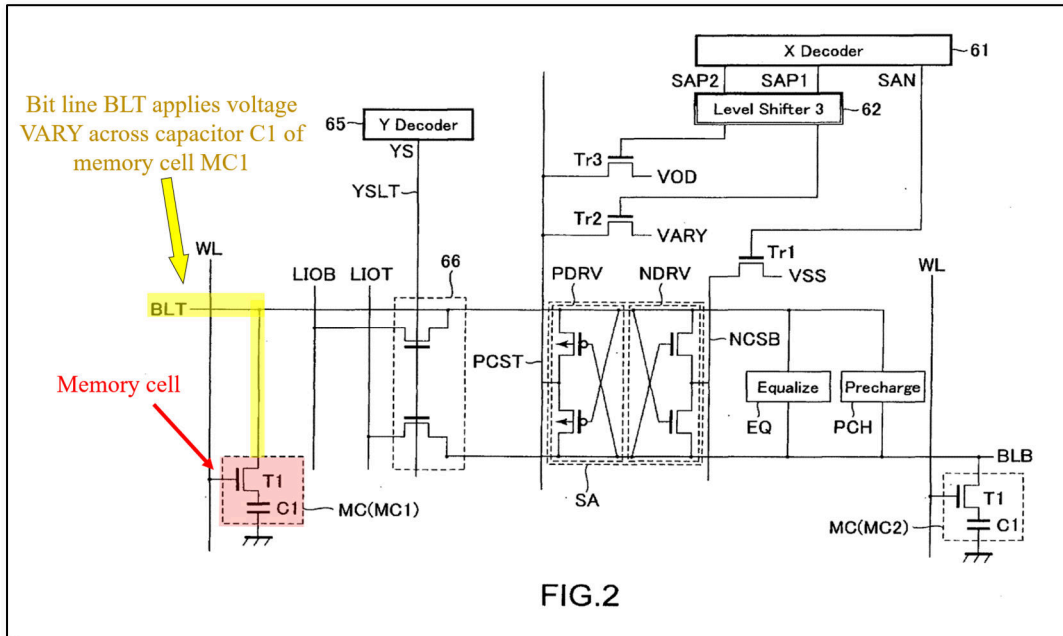
Dono, FIG. 1

227. FIGS. 2 and 7 illustrate operation of a memory cell at VARY in the context of “read/writing timings.” EX1008, [0078]. FIG. 2 is a detailed circuit diagram illustrating a memory cell “MC1” and closely associated circuitry, and FIG. 7 illustrates voltages of various circuit lines and elements as a function of time. Based on a “write command WRIT,” a “bit line [] BLT” is driven to VARY as shown in FIG. 7, and “the data is written into the cell capacitor C1 of the memory cell MC.” EX1008, [0083]-[0084], FIG. 7. This corresponds to a “WRIT” timing illustrated in FIG. 7. FIG. 2 illustrates the direct connection of the bit line BLT to a memory cell MC1; when the bit line BLT is set to VARY as shown in

FIG. 7, VARY is set across a capacitor C1 of the memory cell MC1 (transmitted through an activated transistor T1) to write data to the memory cell MC1. EX1008, FIG. 2. Thus, the memory cell operates at VARY. For example, a memory cell MC1 storing a “1” would have a voltage VARY across its capacitor C1.



Dono, FIG. 7



Dono, FIG. 2

228. For the reasons discussed for [1.3] in §VII.A.2(a), a POSITA would have understood and found obvious that the first voltage VARY is “within a first voltage range” that is, for example, any range that encompasses the disclosed value of VARY=1.0V (this value being discussed in further detail below). EX1008, [0005], [0049]. A POSITA would have also understood and found obvious that the first voltage VARY is within a small first voltage range around its nominal value of 1.0V due to expected non-idealities in voltage generation and provision, e.g., due to temperature effects, load effects, and device variation.

229. Note that Dono’s memory cells are also supplied with, and operate at, VPP, which is supplied to the wordlines (e.g., as the output of word driver 63). EX1008, [0007], [0035], [0059], FIG. 7.

[1.4]: and the DRAM core cell is a volatile memory cell,

230. See [1.4] at §VII.A.2(a). The memory cells of Dono's DRAM ("DDR SDRAM") are, by definition, volatile memory cells. EX1008, [0024].

[1.5]: wherein the first voltage is lower than 1.1 V; and

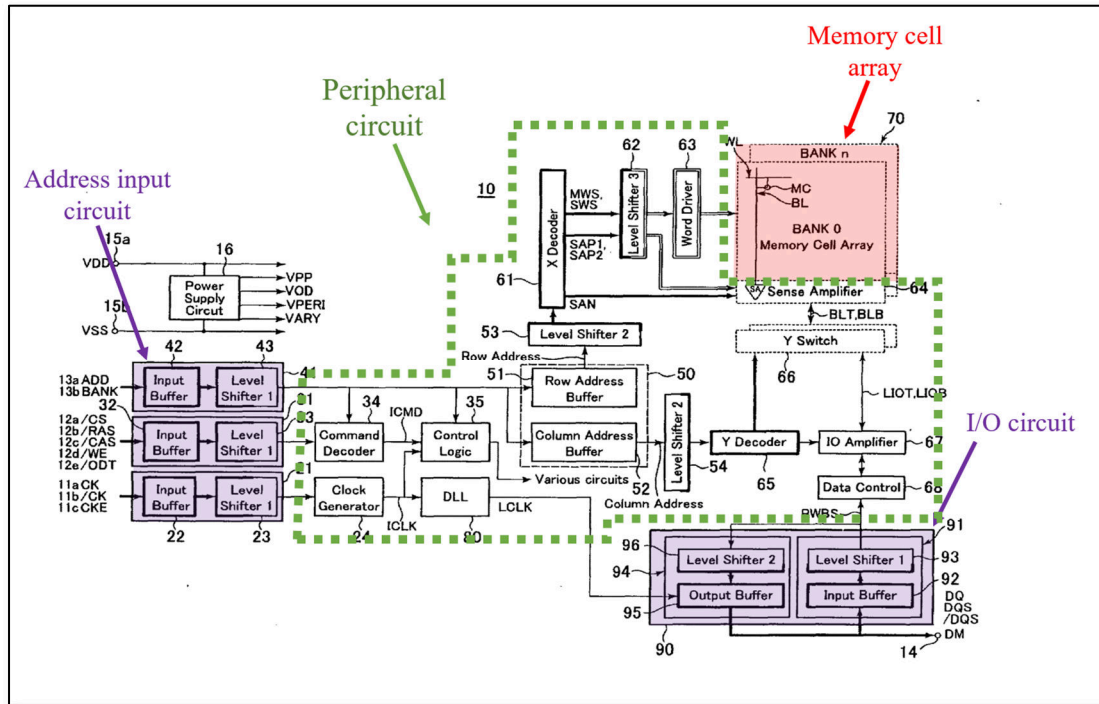
231. The first voltage VARY of Dono is "1.0 V," which is lower than 1.1 V. EX1008, [0005], [0049], [0105].

[1.6]: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell,

232. Dono discloses several peripheral circuits electrically connected to the DRAM core cell. These peripheral circuits include the command decoder 34, the control logic 35, the clock generator 24, the row address buffer 51, the column address buffer 52, the I/O amplifier 67, and/or the data control circuit 68. A POSITA would have understood that these and other peripheral circuits disclosed by Dono could also be collectively referred to as "a" peripheral circuit. See, e.g., EX1020, 15.

233. The textbook *VLSI Memory Chip Design* explains that "[a] memory chip is composed of three blocks[]: a memory cell array, a peripheral circuit, and an input/output (I/O) interface circuit." EX1020, 15. The peripheral circuit "bridges between the memory array and the I/O interface circuit so that they can communicate with each other." EX1020, 17. In Dono's DRAM, this "bridg[ing]"

peripheral circuit between the memory cell array 70 and the data I/O circuit 90/address input circuit 41 is outlined in green below.

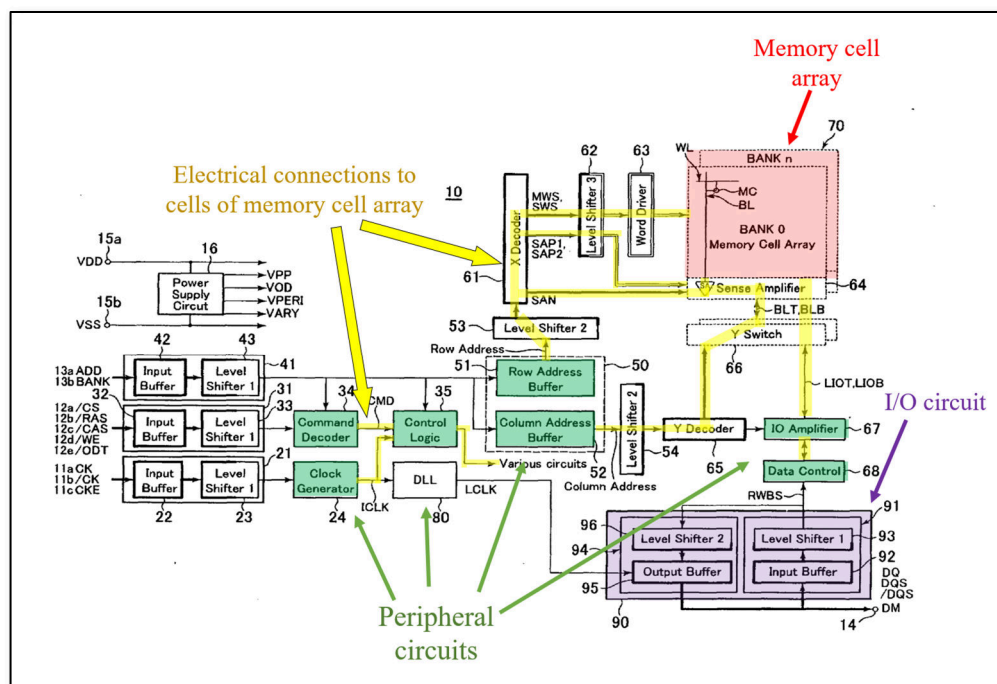


Dono, FIG. 1

234. Based on this definition, Dono’s peripheral circuits include at least the command decoder 34, the control logic 35, the clock generator 24, the row address buffer 51, the column address buffer 52, the I/O amplifier 67, and the data control circuit 68: none of these elements are part of the I/O circuit 90 (or the address input circuit 41, which also has external connections) or the memory cell array, and all of them are connected between those circuits. That the indicated circuits are “peripheral” circuits is supported by the fact that each receives the “peripheral circuit voltage VPERI,” as indicated by their “normal line” outlines. EX1008, [0005], [0043]. I note, however, that just because a circuit does *not* receive VPERI

does not mean it is not a peripheral circuit. For example, the X and Y decoders in Dono FIG. 1 are not illustrated as operating at VPERI, but a POSITA would still have understood and found obvious that they are peripheral circuits. EX1008, FIG. 1. Further, just because a circuit receives VPERI does not mean that it is *necessarily* a peripheral circuit. For example, Dono's I/O circuit 90, which is categorized as an I/O circuit, receives and operates at VPERI (along with VDD).

235. Each of the indicated circuits is electrically connected to the DRAM core cells (cells of the memory cell array 70) through electrical connections illustrated below.

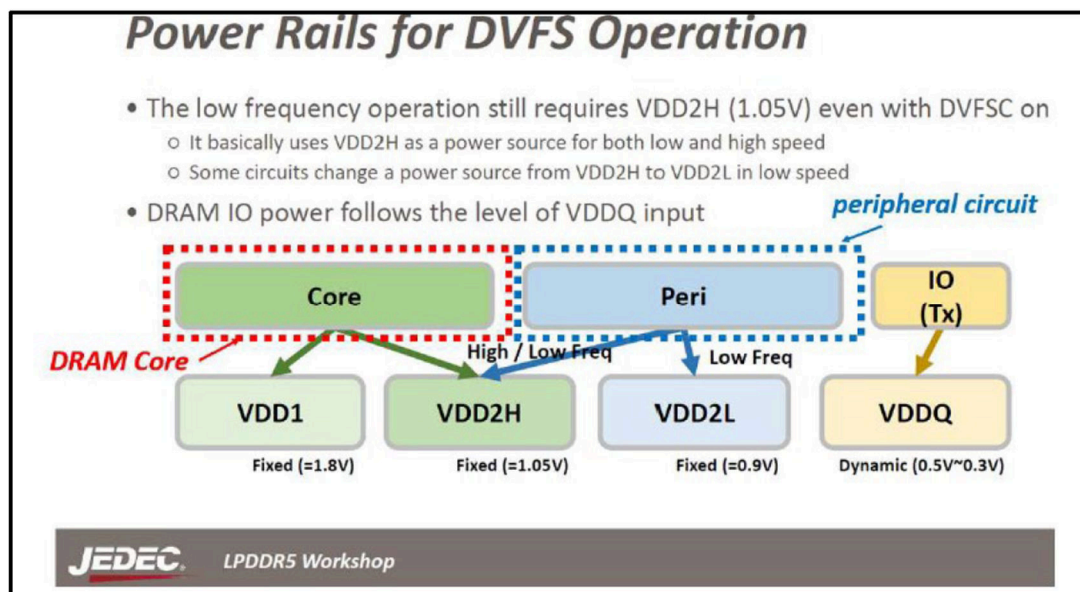


Dono, FIG. 1

236. WeCrevention's Complaint corroborates that these circuits are a "peripheral circuit [] electrically connected to the DRAM core cell." EX1021, 21.

In discussing the products accused in parallel litigation, WeCrevention provided the below annotated diagram to define “peripheral circuit.” EX1021, 21.

WeCrevention’s diagram divides the DRAM into three circuits: core, peri (peripheral), and IO. EX1021, 21. Thus, according to this diagram, DRAM elements besides the core and I/O circuitry—such as the above-cited elements of Dono’s DRAM—are categorized as peripheral circuits.



EX1021, 21 (annotations in original)

237. The WeCrevention Complaint also states that “the LPDDR5 DRAM includes buffers and other data path circuits (*i.e.*, peripheral circuits) connected to the DRAM core cell.” EX1021, 21. Most of the circuits of Dono cited above for the “peripheral circuit [] electrically connected to the DRAM core cell” either *are* buffers (the row address buffer 51 and the column address buffer 52) or are on a data path with the buffers (the command decoder 34, the control logic 35, the I/O

amplifier 67, and the data control circuit 68), meaning that they are peripheral circuits by WeCrevention's own definition. *See* Dono FIG. 1.

238. Thus, based both on the plain and ordinary meaning of “peripheral circuit [] electrically connected to the DRAM core cell” as a POSITA would have understood that term, and on WeCrevention's statements, Dono's command decoder 34, control logic 35, clock generator 24, row address buffer 51, column address buffer 52, I/O amplifier 67, and data control circuit 68 are peripheral circuits electrically connected to the DRAM core cell.

[1.7]: and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage,

239. A POSITA would have understood and found obvious that Dono's command decoder 34, control logic 35, clock generator 24, row address buffer 51, column address buffer 52, I/O amplifier 67, and data control circuit 68 are each supplied with, and operate at, a second voltage VPERI. VPERI is the “peripheral circuit voltage.” EX1008, [0005]. The “normal line” outlines of these circuits in FIG. 1 indicates that they “handle” VPERI. EX1008, [0043], FIG. 1. From this description, a POSITA would have understood that these circuits are supplied with VPERI. VPERI is also referred to as an “internal **operation** voltage,” indicating that the circuit elements “handl[ing]” VPERI operate at VPERI. EX1008, [0007].

240. Goto corroborates, and would have further made obvious to a POSITA, that the circuits described as “handl[ing]” VPERI are supplied with and operate at VPERI. Because Goto shares an applicant and overall structure with Dono, a POSITA would naturally have found Goto relevant for interpreting and applying Dono. Goto describes that “[t]he internal voltage VPERI is supplied to most of the peripheral circuits...The internal voltage VPERI is the operating voltage of such peripheral circuits.” EX1009, [0027]. This mirrors the language of claim 1 that “the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage,” including both the “suppl[y]” and “operate” aspects. Indeed, Goto explicitly shows “VPERI” being supplied to the amplifier circuit 15, corresponding to the I/O amplifier 67 of Dono. By reference to Goto, a POSITA would have understood that the indicated peripheral circuits of Dono operate at VPERI, and would have found it obvious to configure the peripheral circuits of Dono to operate at VPERI to ensure their correct operation.

241. For the reasons discussed for [1.3] in §VII.A.2(a), the recitation that the second voltage VPERI be “within a second voltage range” is satisfied by any range that encompasses the disclosed value of VPERI as equal to, or approximately, 1.0V (discussed in further detail below). EX1008, [0042], [0105]. The second voltage VPERI is also within a small second range around its nominal

value of approximately 1.0V due to expected non-idealities in voltage generation and provision.

[1.8]: wherein the second voltage is lower than 1.1 V, and

242. As noted above, “VARY is 1.0 V,” and Dono also describes that “VPERI $\cong$ VARY.” EX1008, [0042], [0105]. Dono also provides a specific value of VPERI as “VPERI=1.0 V.” EX1008, [0105]. Accordingly, Dono discloses that the second voltage VPERI is lower than 1.1 V.

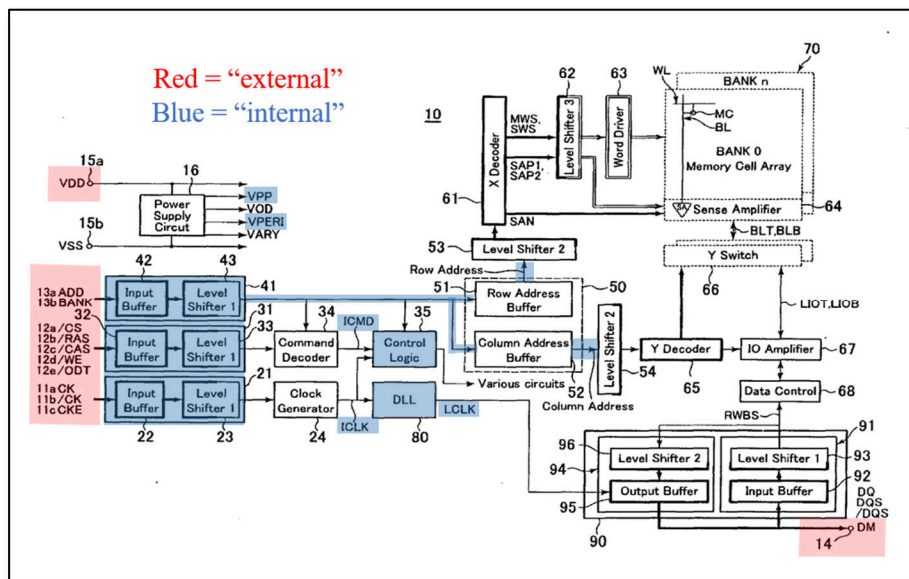
[1.9]: wherein the DRAM core cell and the peripheral circuit are formed on a single chip,

243. A POSITA would have understood and found obvious, for several reasons, that Dono’s DRAM core cells and peripheral circuits are formed on a single chip. **First**, Dono’s DRAM receives a “chip select signal /CS” at a “command terminal” 12a. EX1008, [0024], [0028]. As a POSITA would have known, the chip select signal is used to enable or disable a particular memory chip among multiple chips. For example, Micron Technology’s “DDR3 SDRAM” datasheet describes that the chip select signal “enables [] and disables [] the command decoder. All commands are masked [i.e., ignored] when [the chip select signal] is registered HIGH.” EX1022, 17. Correspondingly, in Dono’s DRAM, the memory cell array 70 would be accessed by selecting the common single chip on which both the memory cell array 70 and the peripheral circuits are formed.

244. *Second*, Dono describes various “*external* terminals” of the “semiconductor device 10” of FIG. 1, such as terminals 11-14, in contrast to “*internal*” signals and circuits. EX1008, [0024], [0026]. In the annotated FIG. 1 below, elements described as “external” are highlighted in red, and elements described as “internal” are highlighted in blue. VDD is “an external voltage.” EX1008, [0004]. Terminals 11a, 11b, 12a to 12e, 13a, 13b, 14, 15a, and 15b are “external terminals.” EX1008, [0024]. VPERI is an “internal operation voltage.” EX1008, [0026]. ICLK and LCLK are “internal clock” signals. EX1008, [0027]. ICMD is “internal commands,” which are supplied to the control logic 35. EX1008, [0030]. VPP is an “internal power source potential.” EX1008, [0042]. The address input circuit 41 is an “internal address circuit,” and its output is an “internal address signal.” EX1008, claim 8.

245. A POSITA would have understood and found obvious that the “external terminals” are used for communicating with a separate chip (such as the “data processor 220” shown in FIG. 11), and that “internal” refers to signals and components on a common single chip. EX1008, [0103]. Dono is explicit about communication with external chips, illustrating the “external terminals” used for that communication. EX1008, [0024]. In contrast to communication with external devices, Dono does not describe any external terminals, pins, bumps, pads, or the like for communicating between the peripheral circuits and the memory cell array

70. EX1008. As a POSITA would have understood, this is because the peripheral circuits and the memory cell array 70 are formed on a common single chip.



Dono, FIG. 1

246. *Third*, the recited “formed on a single chip” configuration for memory cells and peripheral circuitry was entirely conventional and standard. DRAM circuitry—including memory cell arrays, peripheral circuitry, and I/O circuitry—was conventionally integrated in a single chip, and a POSITA would have understood that Dono’s device, lacking disclosure otherwise and conforming to conventional DRAM design, had this conventional configuration. For example, the LPDDR3 standard illustrates pad arrangements for a single DRAM chip, corresponding to a configuration (so well-understood that it did not have to be explicitly articulated) in which DRAM circuitry would be formed as an integrated circuit in a single chip. EX1013, 6-12. A POSITA would have known that, if Dono

intended to depart from the standard configuration, Dono would have discussed some architecture and/or interface circuitry used to communicate between the separate chips hosting the memory cells and the peripheral circuit. Dono does not include any such discussion, and a POSITA would have understood this to mean that, like standard DRAMs, Dono's DRAM was formed on a single chip.

247. The single-chip configuration was the result of applying well-known circuit design principles to DRAM. A POSITA would have known that the most economical and highest-performance implementation would be to integrate all DRAM elements on a single chip, for example, to reduce fabrication and packaging costs, and to reduce signal delays. This understanding of a POSITA is corroborated by the trend of implementing embedded DRAM, in which the DRAM, in addition to being formed on a single chip, is formed on the single chip with *other* components, such as a processor. To the extent the "formed on a single chip" element may not have been directly understood based on Dono, it would have been obvious to a POSITA to form Dono's DRAM (including the memory cell array and peripheral circuits) on a single chip. This configuration would have been obvious as the most common DRAM configuration and in order to realize the well-known advantages of integration, discussed below in reference to Ground 2A.1. To the extent the "formed on a single chip" element may not have been directly understood based on Dono, it would have been obvious to a POSITA to

form Dono's DRAM (including the memory cell array and peripheral circuits) on a single chip. This configuration would have been obvious as the most common DRAM configuration and in order to realize the well-known advantages of integration, discussed below in reference to Ground 2A.1.

248. Further corroboration of the conventionality of forming DRAM circuitry on a single chip is provided, for example, in EX1036 (illustrating a memory cell array and peripheral circuitry, including an I/O circuit, formed in a single semiconductor substrate), EX1037 (illustrating a physical layout of a DRAM chip including a memory cell array, peripheral circuitry, and I/O circuitry), EX1038 (describing a semiconductor substrate as having a "memory array region" and a "peripheral region" with integrated circuitry formed therein), EX1039 (describing an "integrated circuit memory device" that "includes an array of memory cells 104 and a region peripheral to memory array 104," with all components being "formed" on the same "substrate 200"), EX1040 (describing a memory device including a "substrate [that] includes a cell array region...and a peripheral region on which a peripheral circuit is disposed"), EX1041 (describing that "[i]n typical processing, a semiconductor wafer will have one region corresponding to a memory array, and another region peripheral to the memory array in which logic or other circuitry is to be formed"), EX1044 (describing that "a DRAM chip is the set of all cells on the same silicon die, along with the I/O

circuitry which allows the cells to be accessed from outside the chip”), and EX1045 (illustrating I/O routing, sense amplifiers, and cell arrays on the same die). EX1036, 5:53-6:25, 7:34-39, FIGS. 1, 4; EX1037, 2:44-51, 6:34-8:36, FIGS. 3-4; EX1038, 2:25-31, FIG. 1; EX1039, 2:50-59, 5:63-7:3, FIGS. 1, 2A; EX1040, 1:36-37, 2:16-21, FIG. 20; EX1041, 4:41-44; EX1044, 2; EX1045, FIG. 6.

(i) **Ground 2A.1: In view of Youn, it would have been obvious to form Dono’s semiconductor device on a single chip**

249. To the extent Dono and Goto alone are not considered to render obvious [1.9] (that “the DRAM core cell and the peripheral circuit are formed on a single chip”), a POSITA would in view of Youn have further found it obvious to form Dono’s semiconductor device 10—including the memory cell array, peripheral circuits, and I/O circuit—on a single chip.

250. Youn describes “market demands for semiconductor memory devices providing...higher integration density,” where “higher integration density” corresponds to dense integration of circuitry on a single chip. EX1010, 1:25-28. To satisfy these “market demands” while achieving high performance, Youn describes a layout of a “semiconductor integrated circuit memory chip (200)” that provides “a more uniform layout for data path lengths” and a “shorten[ed] data path, which reduces the differences in access times for read operations, for a memory device such as a [SDRAM] where timing of data signals is critical.” EX1010, 5:51-59, FIG. 6. The semiconductor integrated circuit memory chip 200 advantageously has

a layout that is “capable of keeping the sensing efficiency of a data line sense amplifier uniform.” EX1010, 6:27-29. In addition to these specific advantages discussed by Youn, a POSITA would have been aware of the other well-known advantages of integration in general, as discussed in this section.

251. To obtain these advantages, a POSITA would have found it obvious to form Dono’s semiconductor device 10 on a single chip, e.g., conforming to the layouts illustrated by Youn, which have the memory cell array, peripheral circuits, and I/O circuit formed on a single chip. *See* §VII.E.3 and Youn FIGS. 3, 5A, 6, and 8. This implementation would have been obvious as the application of a known technique (DRAM circuit integration) to a piece of prior art (Dono’s DRAM device) ready for the improvements provided by integration generally and by Youn’s advantageous layout specifically.

252. A POSITA would have had a reasonable expectation of success in forming Dono’s semiconductor device 10 on a single chip. Dono’s and Youn’s devices are both DRAMs that include the same or similar components, including memory cell arrays, decoders, peripheral circuitry, and I/O circuitry including input and output buffers and terminals/pads. EX1008, [0005], [0024], [0040], FIG. 1; EX1010, 3:20, 5:57-67, 7:1-2, FIGS. 6, 8. Given this similarity in DRAM architecture (which, I note, is an entirely conventional architecture), a POSITA would have expected Youn’s configurations and layouts to be directly applicable to

Dono's device. Further, Youn discloses not merely the *goal* of integration in a single chip but also *specific physical chip layouts* for achieving effective integration, such that a POSITA would have had a clear roadmap for obtaining single-chip integration. EX1010, FIGS. 3, 6, 8. That is, in addition to motivating forming the DRAM components on a single chip, Youn also teaches a POSITA *how* the DRAM components can be formed on a single chip. Thus, a POSITA would have had a reasonable expectation that forming Dono's semiconductor device 10 on a single chip would be successful.

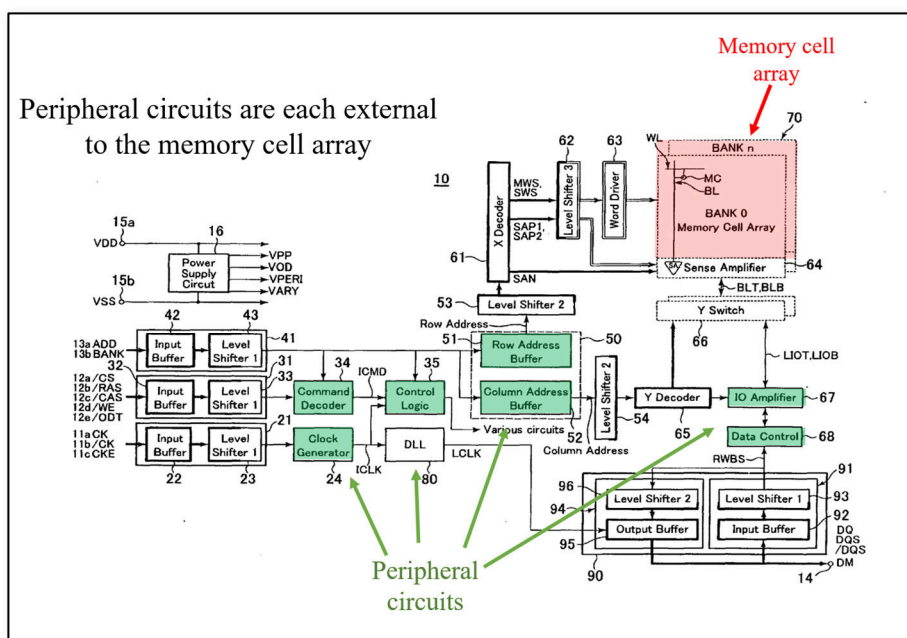
253. Forming Dono's semiconductor device 10 on a single chip would also have been obvious for obtaining the well-known advantages of device integration common to all semiconductor integrated circuit devices, such as manufacturing efficiency, size reduction, and interconnect simplification. This would lead to significant reduction in the cost of both manufacturing and packaging the integrated circuit, while obtaining higher performance due to a significant reduction in energy by eliminating the need to drive key components off-chip. Youn's explicit DRAM chip layouts would have provided a POSITA with an obvious way to achieve these and other well-known advantages of integration.

254. With Dono's semiconductor device 10 implemented so as to be formed on a single chip, Dono's DRAM core cell (cells of the memory cell array 70) and Dono's peripheral circuit (for example, the command decoder 34, the

control logic 35, the clock generator 24, the row address buffer 51, the column address buffer 52, the I/O amplifier 67, and/or the data control circuit 68) would be formed on the single chip.

[1.10]: and the peripheral circuit is external to the DRAM core cell,

255. The peripheral circuits of Dono's DRAM are external to the core cells of the memory cell array 70, e.g., as shown in FIG. 1. EX1008, FIG. 1.



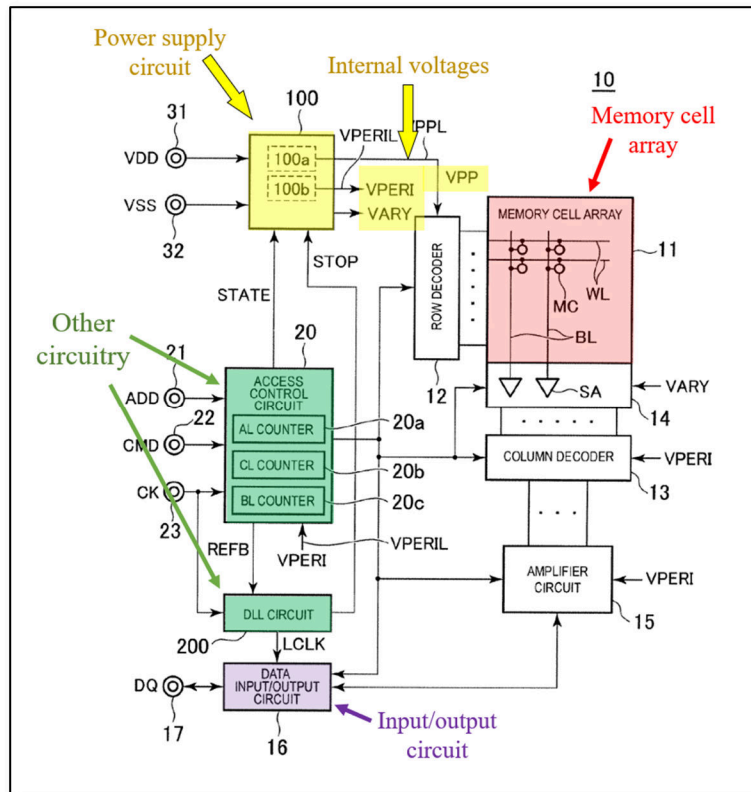
Dono, FIG. 1

[1.11]: and wherein the first voltage is different from the second voltage.

256. Dono discloses, or at least renders obvious to a POSITA, that the first voltage VARY is different from the second voltage VPERI. Dono describes that $VPERI \cong VARY$, meaning that VPERI is *approximately* VARY. EX1008, [0042]. A POSITA would have understood the “ $\cong$ ” to mean that there are, or at least

obviously can be, a difference between VPERI and VARY; otherwise, Dono would have simply used the equal sign (“=”). Further, a POSITA would have understood the language of [1.11] to encompass any “differen[ce]” between the first voltage and the second voltage, such that any deviation between VARY and VPERI (as disclosed by the use of “ $\cong$ ” instead of “=”) satisfies claim 1. Thus, Dono discloses that the first voltage VARY is different from the second voltage VPERI.

257. Goto reinforces that “ $VPERI \cong VARY$ ” is substantively different from “ $VPERI = VARY$,” suggests a difference between VPERI and VARY, and would have motivated a POSITA to provide a difference between VPERI and VARY. As noted in §VII.E.2, Goto shares its applicant with Dono and discloses a similar internal voltage configuration, including the generation of both VPERI and VARY from an external voltage VDD, as shown below. Thus, a POSITA would have found Goto’s disclosures regarding VARY and VPERI highly relevant to interpreting Dono.



Goto, FIG. 2

258. Goto describes that “[w]hether $V_{PERI}=V_{ARY}$ or $V_{PERI}\approx V_{ARY}$ is appropriately determined depending on the intended targets of the respective corresponding plurality of circuits.” EX1009, [0027]. That is, Goto explicitly differentiates between V_{PERI} being *equal to* V_{ARY} and V_{PERI} being *approximately* V_{ARY} . A POSITA would have interpreted this as reinforcing that Dono’s disclosure of “ $V_{PERI}\cong V_{ARY}$ ” is materially different from “ $V_{PERI}=V_{ARY}$ ” and encompasses and suggests differences therebetween. In view of this similar disclosure from the same applicant, it would have been obvious to a POSITA that V_{PERI} and V_{ARY} are, or obviously should be, different from one another, satisfying claim 1.

259. Further, in view of Goto’s disclosure that “[w]hether $V_{PERI}=V_{ARY}$ or $V_{PERI}\approx V_{ARY}$ is appropriately determined depending on the intended targets of the respective corresponding plurality of circuits,” it would have been obvious to “appropriately” make V_{PERI} approximately equal to, but different from, V_{ARY} in order to satisfy “the intended targets of the respective corresponding plurality of circuits [i.e., the peripheral circuits].” EX1009, [0027]. For example, in configuring Dono’s DRAM in view of Goto, a POSITA would have found it obvious to tune V_{PERI} in a small range around V_{ARY} (e.g., a range corresponding to approximately V_{ARY}) to identify the value(s) that provide improved operation of the peripheral circuits. And, in doing so, it would have been obvious to arrive at V_{PERI} being different from V_{ARY} , within the “ $V_{PERI}\cong V_{ARY}$ ” range disclosed by Dono. This would have constituted mere optimization of a variable (V_{PERI}), which was recognized in the art to affect peripheral circuit operation, within the range disclosed in the art (V_{PERI} approximately V_{ARY}), to achieve the recognized result of making V_{PERI} “appropriate” for the peripheral circuits. EX1009, [0027].

(b) ***Claim 2***

260. Claim 2’s elements are found identically in claim 1, except for [2.9] discussed below. For [2.1]-[2.8], *see* [1.1]-[1.8] in §VII.E.4(a), respectively.

[2.9]: wherein the first voltage is greater than the second voltage.

261. See [1.5] and [1.8] in §VII.E.4(a). Dono’s disclosure that “ $V_{PERI} \cong V_{ARY}$ ” explicitly encompasses small differences between the first voltage V_{ARY} and the second voltage V_{PERI} . EX1008, [0042]. Counsel has informed me that a claimed range (here, the first voltage being greater than the second voltage) overlapping with or lying inside a range disclosed by the prior art (here, the second voltage being slightly-greater-than to slightly-less-than the first voltage (i.e., approximately the first voltage)) is obvious, absent countervailing evidence such as unexpected results. I am not aware of, and a POSITA would not have had any reason to believe, that there would be unexpected results here.

262. Goto provides further motivation to make V_{ARY} greater than V_{PERI} . Goto describes that “[w]hether $V_{PERI} = V_{ARY}$ or $V_{PERI} \approx V_{ARY}$ is appropriately determined depending on the intended targets of the [peripheral circuits receiving V_{PERI}].” EX1009, [0027]. It would have been obvious to vary V_{PERI} around V_{ARY} —including making $V_{ARY} > V_{PERI}$, satisfying claim 2—in order to better match V_{PERI} to peripheral circuit(s) for which a V_{PERI} differing from V_{ARY} is more “appropriate.” EX1009, [0027]. For example, in performing the obvious tuning of V_{PERI} that I referred to above, a POSITA would naturally try V_{PERI} not only slightly greater than V_{ARY} but also slightly less than V_{ARY} , satisfying claim 2.

263. In addition, Goto describes that “[u]sing the internal voltage VPERI lower than VDD as the operating voltage of the peripheral circuits reduces the power consumption of the peripheral circuits.” EX1009, [0027]. This disclosure would have provided a POSITA with a motivation to reduce VPERI in order to reduce power consumption, thereby arriving at VARY greater than VPERI through this voltage and power optimization.

(c) **Claim 3**

[3.1]: A dynamic random access memory (DRAM), comprising:

264. *See [1.1].*

[3.2]: a DRAM core cell comprised in the DRAM,

265. *See [1.2].*

[3.3]: wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage,

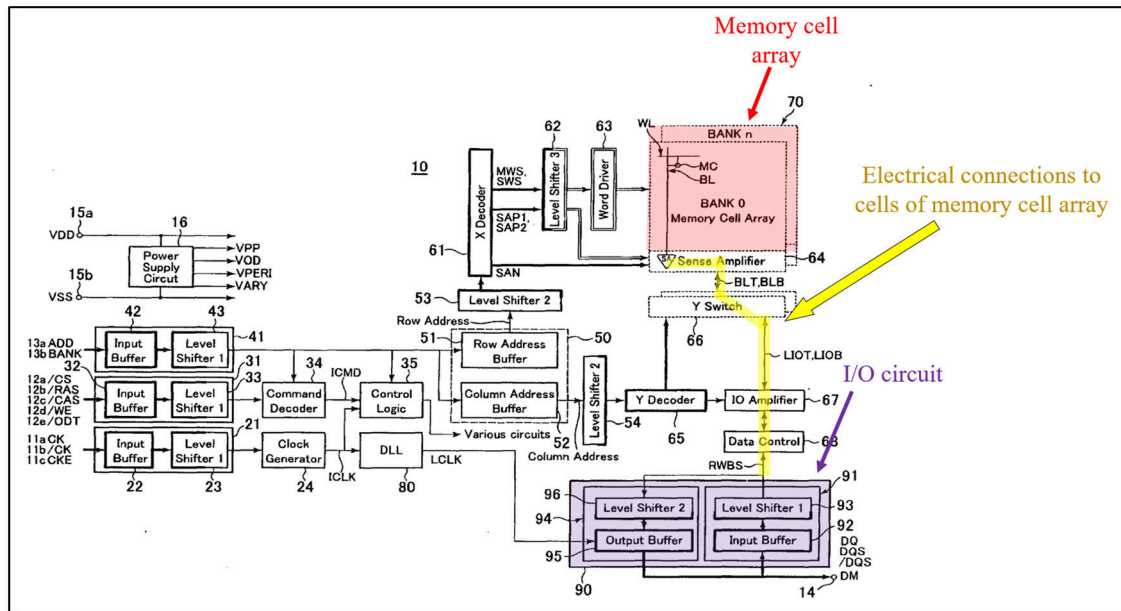
266. *See [1.3].* Dono discloses a first voltage, VARY, supplied to the memory cells of the memory cell array 70. EX1008, [0043], [0078], [0083]-[0084], FIGS. 1-2, 7.

[3.4]: and the DRAM core cell is a volatile memory cell;

267. *See [1.5].*

[3.5]: an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell,

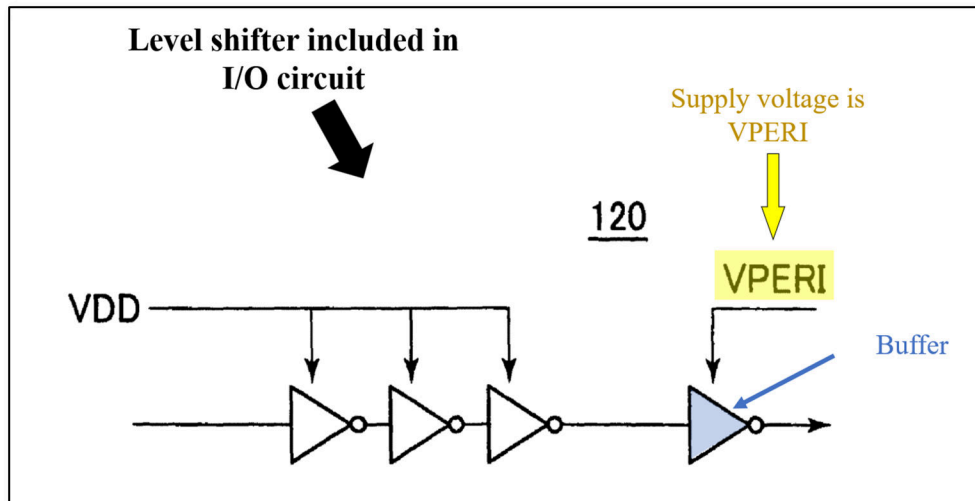
268. Dono's DRAM includes an "I/O circuit 90" that is electrically connected to the cells of the memory cell array 70. EX1008, [0041], FIG. 1. For example, as shown below, the I/O circuit 90 is electrically connected to the memory cell array 70 through sense amplifier 64, IO amplifier 67, and data control circuit 68. EX1008, [0039], FIG. 1. The I/O circuit 90 is also electrically connected to the peripheral circuit, e.g., to the I/O amplifier 67 and the data control circuit 68. EX1008, FIG. 1. The I/O circuit 90 performs the claimed input and/or output function of the "input/output circuit" with respect to Dono's DRAM (as disclosed, for example, through its connection to a "read/write bus RWBS"), and Dono discloses at least as much structure for the I/O circuit 90 as is disclosed for the input/output unit 106 of the '098 Patent (additionally disclosing, for example, the inclusion of level shifters and buffers, and illustrating a further connection to a data system terminal 14). EX1008, [0024], [0040]-[0041], FIGS. 1, 7.



Dono, FIG. 1

[3.6]: and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage,

269. Dono's I/O circuit 90 is supplied with a third voltage VPERI that makes the I/O circuit 90 operate at the third voltage VPERI. For example, the I/O circuit 90 includes a "first level shifter 93." EX1008, [0040]. FIG. 6 illustrates a level shifter 120 that "is preferably used for the level shifter...93 shown in FIG. 1." EX1008, [0076]. "**VPERI is supplied** to a power source terminal of the fourth buffer" of the level shifter 93/120. EX1008, [0077]. As indicated by the half-"normal line" outline of the level shifter 93 in FIG. 1, the level shifter 93/120 "handle[s]" the third voltage VPERI at its "output side," in agreement with FIG. 6. EX1008, [0043].



Dono, FIG. 6

270. A POSITA would have understood and found obvious that the fourth buffer “operates at” VPERI because VPERI is its power supply voltage. A POSITA would have understood that a circuit such as a buffer “operates at” its supply voltage. For example, a POSITA would have understood and found obvious that standard CMOS buffers employing a common push-pull inverter would output between VPERI and 0V at the output of the fourth buffer, even if the third buffer is operated at VDD. The fourth buffer would have the function of dropping the VDD to the VPERI level for its operation. For example, the datasheet for the Fairchild Semiconductor 74VCXH162244 buffer describes “operation” at its “1.4V to 3.6V V_{CC} supply [voltage].” EX1029, 1, 3. Similarly, the datasheet for the Texas Instruments SN74AUP1G07 buffer/driver describes its “**Operating V_{CC} Range,**” where V_{CC} is its supply voltage. EX1030, 1, 3.

271. Corroborating this, Dono describes VPERI as “the internal **operation voltage**,” indicating that circuits supplied with VPERI (such as the fourth buffer and the I/O circuit 90) “operate” at VPERI. EX1008, [0026].

272. Thus, the fourth buffer of the first level shifter 93 of the I/O circuit 90 is supplied with and operates at VPERI, meaning that the I/O circuit 90 is supplied with and operates at the third voltage VPERI.

[3.7]: wherein the third voltage is lower than 1.1V; and

273. As discussed for [3.6], the third voltage is VPERI. VPERI is equal to 1.0V or approximately 1.0V, and therefore is lower than 1.1V. EX1008, [0005], [0026], [0049], [0105].

[3.8]: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell,

274. See [1.6]. Dono discloses several peripheral circuits electrically connected to the DRAM core cell. These peripheral circuits include the command decoder 34, the control logic 35, the clock generator 24, the row address buffer 51, the column address buffer 52, the I/O amplifier 67, and/or the data control circuit 68.

[3.9]: and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage,

275. See [1.7]. Dono's peripheral circuits are supplied with and operate at a second voltage VPERI.

[3.10]: wherein the second voltage is lower than 1.1 V and the first voltage is different from the second voltage;

276. See [1.8] and detailed discussion at [2.9]. Dono discloses that the second voltage VPERI is approximately the first voltage VARY ("VPERI $\cong$ VARY"), where "VARY is 1.0 V." EX1008, [0042], [0105] Thus, the second voltage VPERI is lower than 1.1 V. Further, Dono's use of " $\cong$," in conjunction with Goto's explicit distinction between "VPERI=VARY" and "VPERI $\approx$ VARY" and Goto's disclosed motivations to (i) optimize VPERI for target circuit operation and (ii) reduce VPERI to reduce power consumption, would have disclosed or at least rendered obvious to a POSITA that the first voltage VARY is different from the second voltage VPERI. EX1009, [0027].

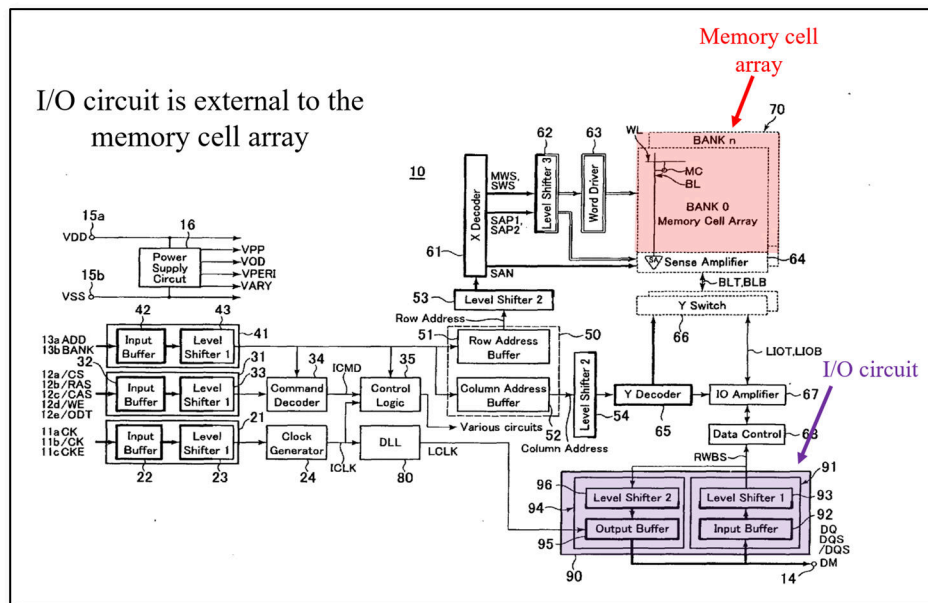
[3.11]: wherein the DRAM core cell and the input/output circuit are formed on a single chip,

277. See [1.9]. Under Ground 2A, for analogous reasons to those discussed for the peripheral circuit, a POSITA would have understood that the memory cell array 70 and the I/O circuit 90 of Dono are formed on a single chip, in keeping with conventional DRAM integration. Alternatively, under Ground 2A.1, in view of YOUN, it would have been obvious to form the memory cell array 70 and the I/O

circuit 90 on a single chip, for the reasons discussed for [1.9], in order to achieve, with a reasonable expectation of success, both the widely-understood advantages of DRAM integration and the particular advantages described for Youn's single-chip integrated layout.

[3.12] and the input/output circuit is external to the DRAM core cell,

278. Dono's I/O circuit 90 is external to the memory cell array 70, as shown in FIG. 1. EX1008, FIG. 1.



Dono, FIG. 1

[3.13] and wherein the first voltage is different from the third voltage.

279. See [3.3], [3.7], and [3.10], and detailed discussion at [2.9]. The first voltage is VARY=1.0 V. EX1008, [0105]. The third voltage is VPERI, which Dono and Goto disclose, or at least render obvious, is different from VARY. Therefore, the first voltage VARY is different from the third voltage VPERI.

(d) **Claim 4**

[4]: The dynamic random access memory of claim 3, wherein the first voltage is lower than 1.1V.

280. See [1.3], [1.5], and [3.3]. The first voltage is VARY=1.0V, which is lower than 1.1V. EX1008, [0026], [0049], [0105].

(e) **Claim 5**

[5]: The dynamic random access memory of claim 3, wherein the first voltage is different from the second voltage.

281. See [3.10]. This element is recited identically in claim 3 and addressed above.

(f) **Claim 6**

[6.1]-[6.4]:

282. See [1.1]-[1.4].

[6.5]-[6.7]:

283. See [3.5]-[3.7].

[6.8]: wherein the first voltage is greater than the third voltage, and

284. See [3.3], [3.7], [3.10], [3.13] and detailed discussion at [2.9]. The first voltage is VARY=1.0 V. EX1008, [0105]. The third voltage is VPERI(“ $\cong$ VARY”). EX1008, [0105]. Dono’s use of “ $\cong$,” in conjunction with Goto’s explicit distinction between “VPERI=VARY” and “VPERI $\approx$ VARY” and

Goto's disclosed motivations to (i) optimize VPERI for target circuit operation and (ii) reduce VPERI to reduce power consumption, would have disclosed or at least rendered obvious to a POSITA that the first voltage VARY is greater than the third voltage VPERI. EX1009, [0027].

[6.9]: the DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP).

285. For the reasons discussed in §VII.A.2(f) for Ground 1A, a POSITA would have understood that Dono's DRAM, operating with the first voltage VARY and the third voltage VPERI, is capable of being applied to an eDP. This is because Dono's memory is a working, conventional DRAM that, when operating with Dono's disclosed voltages VARY and VPERI, is capable of satisfying the requirements of the eDP 1.3 standard, which do not include any voltage or power requirements. EX1014. As I discussed in §VII.A.2(f), the eDP 1.3 standard provided by JEDEC (EX1014) can simply be read to learn that the standard's requirements for the frame buffer are quite limited. The standard requires, in essence, that the frame buffer store and provide data representing a static image. EX1014. Dono's DRAM, which stores data, supports read and write operations, and provides "high-speed data transfer," is more than capable of fulfilling these requirements. EX1008, [0009], [0040].

286. Further, to the extent the '098 Patent erroneously links “capable of being applied to an embedded display port (eDP)” to low-voltage operation, then Dono’s DRAM, which has first (VARY) and third (VPERI) voltages that satisfy the “< 1.1 V” condition of the '098 Patent, would be equally as capable of being applied to an eDP as the '098 Patent’s devices. EX1001, 4:61-5:9, Table III.

(g) **Claim 7**

[7]: The dynamic random access memory of claim 6, wherein the first voltage is lower than 1.1 V.

287. See [1.5]. The first voltage of Dono’s DRAM is VARY=1.0V, lower than 1.1 V. EX1008, [0105].

(h) **Claim 8**

[8]: The dynamic random access memory of claim 6, further comprising: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1 V.

288. See [1.7]-[1.8] and [3.8]-[3.10]. Peripheral circuits of Dono’s DRAM include Dono’s command decoder 34, control logic 35, clock generator 24, row address buffer 51, column address buffer 52, I/O amplifier 67, and/or data control circuit 68, each of which is supplied with, and operates at, a second voltage

VPERI. EX1008, [0007], [0043], FIG. 1; EX1009, [0027]. VPERI is approximately 1.0V, lower than 1.1V. EX1008, [0105].

(i) **Claim 9**

[9]: The dynamic random access memory of claim 8, wherein the first voltage is different from the second voltage.

289. See [1.5], [1.8], [1.11], and [3.10]. For the reasons discussed there, in Dono's DRAM, a POSITA would have found it obvious to make the second voltage VPERI different from the first voltage VARY.

F. [Grounds 2B and 2B.1] Dono, Goto, and Endo render obvious claims 6-9; and Dono, Goto, Endo, and Youn render obvious claims 6-9

1. Obviousness of claims 6-9

290. Endo is applied here as discussed for Ground 1C in §VII.C. As discussed in §VII.D, Dono and Goto (and alternatively/additionally Dono and Goto and Youn) render obvious claims 6-9. In view of Endo's explicit disclosure of using a DRAM as the frame buffer in an eDP 1.3 device, a POSITA would have further found it obvious that Dono's DRAM is capable of being applied to an eDP, would have been further motivated to apply that DRAM to an eDP to obtain the benefits discussed above (e.g., the power reduction benefits provided by the RFB of the eDP 1.3 standard, and the benefits of conforming to the eDP 1.3 standard), and would have reasonably expected success in doing so. EX1007, [0034]-[0035].

VIII. LEGAL PRINCIPLES

A. Anticipation

291. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.

292. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date).

B. Obviousness

293. I have been informed that a patent claim is invalid as “obvious” under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a POSITA, taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii)

commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others. For purposes of my analysis above and because I know of no indication from the patent owner or others to the contrary, I have applied a date of July 17, 2012, as the date of invention in my obviousness analyses, although in many cases the same analysis would hold true even at an earlier time than July 17, 2012.

294. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason to modify the single prior art reference, or combine two or more references, in order to achieve the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or “common sense” of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

295. I have also been informed of the Supreme Court decision *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), which I am informed guides obviousness

analyses. Under *KSR*, the mere application of a known technique to a piece of prior art ready for the improvement is obvious. In addition, the selection of one of a finite number of identified, predictable solutions to achieve a predictable result is obvious. Further, the simple substitution of one known element for another to obtain a predictable result is obvious.

APPENDIX A

DAVID KUAN-YU LIU, Ph.D.

2055 15TH St. N, #2007, VA 22201 • (510) 579-5029
davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 18 years of experience serving as expert consultant.
 - Named inventor on 99 US patents.
- Consultant and expert witness for past 18 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

EXPERT WITNESS WORK - CASE EXPERIENCE:

Case: **Advanced Memory Technologies, Inc. v. Micron Technology, Inc.**
Jurisdiction: Civil Action No. 1:25-cv-01036 (W.D. Tex.)
Work Product: Expert consulting work relating to Booster Circuit. Patent analysis and prior art review toward preparation of EPR petition support and draft of declaration.
Nature of Case: EPR.
Counsel: Retained by Fish & Richardson (Contact: Tim Riffe)
Date: 11/25 – Present

Case: **Apple v. WeCrevention, Inc.**
Jurisdiction: Post-Grant Patent Matters Adverse to WeCrevention, Inc.
Work Product: Expert consulting work relating to High Speed Chip Memory Module. Patent analysis and prior art review toward preparation of IPR petition support and draft of declaration.
Nature of Case: IPR.
Counsel: Retained by Fish & Richardson (Contact: Dr. Hyun Jin In)
Date: 11/25 – Present

Case: **Monterey Research LLC v. Renesas Electronics Corp.**
Jurisdiction: Civil Action No. 2:24-cv-00238-JRG (E.D. Tex.)
Work Product: Expert consulting work relating to Charge Trapping Nonvolatile Memory. Patent analysis and prior art review toward preparation of IPR petition support and draft of declaration.
Nature of Case: Civil action and IPR.
Counsel: Retained by Morrison Foerster (Contact: Yuka Teraguchi)
Date: 03/25 – Present

Case: **Palisade Techs., LLP v. Micron Tech., Inc.**
Jurisdiction: Civil Action N.D. Cal, No. 7:24-cv-00262 (W.D. Tex.)
Work Product: Expert consulting work relating to 3D NAND Flash Memory Technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 2 patents.
Nature of Case: Civil action and IPR.
Counsel: Retained by O'Melveny & Myers LLP (Contact: John Kappos)
Date: 12/24 – 01/26

Case: **Yangtze Memory Technologies Company, Ltd. vs. Micron Technology, Inc.**
Jurisdiction: Civil Action N.D. Cal, No. 3:223-cv-05792-RFL
Easter District of Texas
Work Product: Expert consulting work relating to 3D NAND Flash Memory Technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents. ***Deposed on 3 petitions that have been instituted.***
Nature of Case: Civil action and IPR.
Counsel: Retained by Orrick, Herrington & Sutcliffe (Contact: Jason Lang)
Date: 03/24 – Present

Case: **Force MOS Technology Co., Ltd. vs. Inergy Technology, Inc.**
Jurisdiction: Civil Action E.D. TX, No. 2:22-cv-00460-JRG
Easter District of Texas
Work Product: Expert consulting work relating to Vertical Trench DMOS process technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 2 patents. Declaration for claim construction on 3 patents. ***Deposed on Claim Construction Declaration, and deposed on declarations for IPR petitions, and deposed on reply declaration.*** Continuing work on claim construction and technical consulting.
Nature of Case: Civil action and IPR.
Counsel: Retained by Baker McKenzie (Contact: McKenzie Martin)
Date: 10/23 – 10/25

Case: **GlobalFoundries U.S. vs. International Business Machines**
Jurisdiction: 03348-KMK-AEK (S.D.N.Y. 2023)
Work Product: Expert consulting work relating to trade secrets involving advanced CMOS process and device technology (Nanosheet technology). Reviewed evidence and summarized findings.
Nature of Case: Civil action.
Counsel: Retained by Latham & Watkins (Contact: Sami Al-Marzoog)
Date: 10/23 – 2/25

Case: **Element Capital. vs. Beijing BOE Display Technology Co., Ltd.**
Jurisdiction: Civil Action No. 2:22-cv-00118-JRG
Eastern District of Texas
Work Product: Expert consulting work relating to OLED technology. Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 3 patents.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Linhong Zhang)
Date: 4/23 – 12/23

Case: **Sonrai Memory Ltd. vs. Micron Technology, Inc.,**
Jurisdiction: Civil Action No. 6:22-cv-000855-FB
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration resulting in institution of
the petition and ***deposed on supplemental declaration.***
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Tim Riffe)
Date: 12/22 – 7/24

Case: **Daedalus Prime LLC vs. Samsung Electronics Co.,**
Jurisdiction: Civil Action E.D. TX, Marshall Div., No. 2:22-cv-353
Eastern District of Texas, Marshall Div., and
Investigation No. 337-TA-1336
Work Product: Expert consulting work relating to FINFET process technology.
Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration on 2 patents. Source code
database viewing (GDS layout and process flow documents) for
supporting of non-infringement position.
Nature of Case: Civil action and ITC Investigation on Certain Semiconductor Devices,
Mobile Devices Containing the Same and Components Thereof..
Counsel: Retained by Fish & Richardson (Contact: Kevin Su)
Date: 10/22 – 4/23

Case: **Netlist, Inc. vs. Samsung Electronics Co. Ltd. et al.,**
Jurisdiction: Civil Action No. 2:21-cv-00463
Eastern District of Texas
Work Product: Expert consulting work relating to memory modules.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Tony Nguyen)
Date: 8/22 – 12/22

Case: **Vervain, LLC vs. Micron Technology & related IPR Petition**
Jurisdiction: Action No. 6:21-cv-00487-ADA
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR
petition material and draft of declaration on 4 patents, all 4 petitions
instituted, and ***deposed on both initial declaration and reply
declaration on all 4 patents.***
Counsel: Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared
Bobrow)
Date: 8/21 – 2/23

Case: **Monterey Research vs. Qualcomm PTAB Matter**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Jones Day (Contact: David Cochran)
Date: 12/21 – 2/22

Case: **Semiconductor Energy Laboratory Co., OLED Patent Matters**
Jurisdiction: Action No. 8:21-cv-00554-JAK-ADS
Central District of California
Work Product: Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Bryan Basso)
Date: 9/21 – 4/22

Case: **Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Erise IP (Contact: Paul Hart)
Date: 8/21 – 9/21

Case: **Texas Instruments IPR Petition**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Josh Griswold)
Date: 9/20 – 4/21

Case: **Micron Technology vs. UMC/JinHua**
Jurisdiction: Case No. 4:17-CV-06932-MMC
United States District Court for the Northern District of California
Work Product: Testifying expert, trade secret documents review, and declaration submission.
Nature of Case: Trade secret contention of Micron confidential documents.
Counsel: Retained by Jones Day (Contact: Randy Kay)
Date: 3/17 – 12/23

Case: **SK Hynix vs. BitMicro**
Jurisdiction: Investigation No. 337-TA-1097
United States International Trade Commission
Work Product: Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, **deposition taken**, issued witness statement.
Nature of Case: ITC infringement case concerning module stacking of SDRAM.
Counsel: Retained by Fish Richardson (Contact: Joseph Colaianni)
Date: 11/18 – 4/19

Case: ***Rohm Company IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Matt Colvin)
Date: 4/18 – 8/18

Case: ***Apple Inc., vs. Qualcomm Incorporated***
Jurisdiction: Case No. 3:17-CV-02402
United States District Court for the Southern District of California
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, ***2 depositions taken.***
Counsel: Fish & Richardson (Contact: Tony Nguyen)
Date: 1/18 – 5/19

Case: ***Macronix vs. Toshiba***
Jurisdiction: Investigation No. 337-TA-1046
United States International Trade Commission
Work Product: Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, ***deposition taken for 2 patents,*** issued witness statement and rebuttal witness statement, ***testified in ITC court on both infringement and invalidity.***
Nature of Case: ITC infringement case concerning advanced NAND Flash memory.
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 4/17 – 10/18

Case: ***Novatek Microelectronics Corp. IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date: 2/17 – 4/17

Case: ***Taiwan Semiconductor Manufacturing Company IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: John Goetz)
Date: 7/15 – 4/17

Case: **Triune Systems, LLC vs. Wayne Chen, et al.,**
Jurisdiction: Case No. 296-03209-2013,
District Court of Collin County, TX
Work Product: Testifying expert, database viewing, expert report, ***video-taped testimony***
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: **Macronix vs. Spansion**
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial,
database viewing for evidence gathering, expert report, expert
rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: **Macronix vs. Spansion**
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content
of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: **Keranos, LLC v. Analog Devices et. al.**
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: **Silicon Storage Technology, Inc. v. Xicor, LLC**
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the
process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Testifying expert: issuing expert report, declarations, and
deposition taken.
Nature of Case: Patent infringement case concerning minimizing source current
during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

PROFESSIONAL EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 12 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35 μ m and 0.18 μ m CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00

Programmable Silicon Solutions, Sunnyvale, California

Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98

AMIC Technology, Santa Clara, California

Director of Flash Technology. Responsible for developing 0.35 μ m ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97

Altera Corp., San Jose, California

Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35 μ m generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96

Information Storage Devices, San Jose, California

Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95

Advanced Micro Devices, Sunnyvale, California

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5 μ m and 0.35 μ m flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K.-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.
8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.
9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994
10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.
11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.
12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.
13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.
14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.
15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.

16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.
17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.
18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.
19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.
20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.
21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.
22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.
23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.
24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.
25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997
26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.
27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.
28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.
29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998
30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.
31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.
32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.

33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.
34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.
35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.
36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.
37. U.S. Patent 6,026,017, "Compact nonvolatile memory," Issued February 15, 2000.
38. U.S. Patent 6,027,974, "Nonvolatile memory," Issued February 22, 2000.
39. U.S. Patent 6,088,263, "Non-volatile memory using substrate electrons," Issued July 11, 2000.
40. U.S. Patent 6,091,636, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued July 18, 2000.
41. U.S. Patent 6,127,225, "Memory cell having implanted region formed between select and sense transistors," Issued October 3, 2000.
42. U.S. Patent 6,159,800, "Method of forming memory cell," Issued December 12, 2000.
43. U.S. Patent 6,188,604, "Flash memory cell & array with improved pre-program and erase characteristics," Issued February 13, 2001.
44. U.S. Patent 6,185,133, "Flash EPROM using junction hot hole injection for erase," Issued February 6, 2001.
45. U.S. Patent 6,252,799, "Device with embedded Flash and EERPOM memories," Issued June 26, 2001.
46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.
47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.
48. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode," Issued November 12, 2002.
49. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," Issued January 28, 2003.
50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.

51. U.S. Patent 6,624,026, "Nonvolatile Memory," Issued September 23, 2003.
52. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process," Issued January 20, 2004.
53. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same," Issued February 3, 2004.
54. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic," Issued February 17, 2004.
55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.
56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.
57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.
58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.
59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.
60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.
61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.
62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.
63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.
64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.
65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.
66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.
67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.

68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.
69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010
70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.
72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010
73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.
74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010
75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011
76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011
77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011
78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012
79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012
80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012
81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012
82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.

83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.
84. U.S. Patent 8,582,342, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued November 12, 2013.
85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.
86. U.S. Patent 8,705,263, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.
87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.
88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.
89. U.S. Patent 9,224,739, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued December 29, 2015.
90. U.S. Patent 9,305,931, "Zero Cost NVM Cell Using High Voltage Devices in Analog Process," Issued April 5, 2016.
91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.
92. U.S. Patent 9,558,813, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued January 31, 2017.
93. U.S. Patent 9,570,161, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
95. U.S. Patent 10,061,738, "Ephemeral Peripheral Device," Issued August 28, 2018.
96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.
97. U.S. Patent 10,198,889, "Automatic Valid Vote Count Storage Using Secure Embedded Non-Volatile Memory," Issued February 5, 2019
98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.
99. U.S. Patent 10,629,607, "Semiconductor CMOS Non-Volatile Memory Device," Issued April 21, 2020

PUBLICATIONS

1. S.D. Leeke, D. K. Y. Liu and J. P. McVittie, "Plasma mode trench etching with direct hydrocarbon injection," *Materials Research Society Symposium Proceedings*, Vol. 68, pp. 21-27, 1986.
2. D. K. Y. Liu and J. D. Plummer, "A novel trench-injector power device with low ON-resistance and high switching speed," *IEEE Electron Device Letters*, Vol. 9, No. 7, pp. 321-323, 1988.
3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
6. M. Wong, D. K. Y. Liu, M. M. Moslehi and D. W. Reed, "Preoxidation treatment using HCl/HF vapor," *IEEE Electron Device Letters*, Vol. 12, No. 8, pp. 425-426, 1991.
7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
8. K.-L. Chen, D. K. Y. Liu, G. Misium, W. M. Gosney, S.-J. Wang, J. Camp and H. Tigelaar, "A sublithographic antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 53-55, 1992.
9. K. T. San, C. Kaya, D. K. Y. Liu, T. P. Ma, and P. Shah, "A new technique for determining capacitive coupling coefficients in flash EPROMs," *IEEE Electron Device Letters*, Vol. 13, No. 6, pp. 328-331, 1992.
10. C. Kaya, D. K. Y. Liu, J. Paterson and P. Shah, "Buried source-side injection (BSSI) for flash EPROM programming," *IEEE Electron Device Letters*, Vol. 13, No. 9, pp. 465-467, 1992.
11. M. Wong, D. K. Y. Liu and S. S.-W. Huang, "Analysis of the subthreshold slope and the linear transconductance techniques for the extraction of the capacitance coupling coefficients of floating-gate devices," *IEEE Electron Device Letters*, Vol. 13, No. 11, pp. 566-568, 1992.
12. D. K. Y. Liu and J. D. Plummer, "Design and analysis of a new conductivity-modulated power MOSFET," *IEEE Transactions on Electron Devices*, Vol. 40, No. 2, pp. 428-438, 1993.
13. J. Z. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, B. Ho, Y. Sun, D. Liu, Y. Tang, J. Hsu, S. Luan, J. Lien, "Flash EPROM endurance simulation using physics-based models," In *International Electron Devices Meeting Technical Digest*, pp. 295-298, 1994.

14. J. Chen, J. Hsu, S. Luan, Y. Tang, D. Liu, S. Haddad, C. Chang, S. Longcor, J. Lien, "Short Channel enhanced degradation during discharge of Flash EEPROM memory Cell," *International Electron Devices Meeting Technical Digest*, pp. 331-334, 1995.
15. V. H. Chan and D. Liu, "An Enhanced Erase Mechanism During Channel Fowler-Nordheim Tunneling in Flash EPROM Memory Devices," *IEEE Electron Devices Letters*, Vol. 20, No. 3, pp. 140-142, 1999.