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VESA Embedded DisplayPort[®] 1.3 Errata

Errata Version 1

August 8, 2011

Purpose

The purpose of this document is to clarify and/or add known errors/omissions to the Embedded DisplayPort (eDP) 1.3 standard published in January 2011.

Corrections to eDP 1.3 will be shown in red text and will be published under the original section number in numerical order within this document.

Following each changed section will typically be Notes that will describe the benefits and impact of the changes.

Any changes to Intellectual Property (IP) will be shown in the standard IP section of this document

The revision history will track sections affected and the date of errata publication.

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Preface

Intellectual Property

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Revision History

August 8, 2011

Errata 1

3.4 eDP AUX Link Services

In the case of using the AUX channel to set display backlight brightness, a change has been made regarding the required state of other DPCD control bits.

In eDP v1.3, backlight brightness can be set using the Sink's EDP_BACKLIGHT_BRIGHTNESS_MSB and/or EDP_BACKLIGHT_BRIGHTNESS_LSB registers (if the ability to use these registers is enabled in the Sink). In eDP v1.3, writing to these registers is ignored if the BACKLIGHT_ENABLE bit is set to 0.

This errata removes the state requirement of the BACKLIGHT_ENABLE bit. Writing to EDP_BACKLIGHT_BRIGHTNESS_MSB and DP_BACKLIGHT_BRIGHTNESS_LSB is no longer dependent on the state of the BACKLIGHT_ENABLE bit.

4.3.3.1.1 Source Transmitter Off

In the case of PSR exit when No Link Training is used (and only in this case), a new requirement is added for the Source device. In eDP 1.3, if the Main Link is Off, Main Link activity is resumed only after the Source receives an ACK from the Sink. This errata stipulates that the Source begins Main Link activity by the end of the wake request to the Sink, instead of waiting for ACK from the Sink.

Summary of the Proposed Change(s)

In the case of using the AUX channel to set display backlight brightness, a change has been made regarding the required state of other DPCD control bits.

In eDP v1.3, backlight brightness can be set using the Sink's EDP_BACKLIGHT_BRIGHTNESS_MSB and/or EDP_BACKLIGHT_BRIGHTNESS_LSB registers (if the ability to use these registers is enabled in the Sink). In eDP v1.3, writing to these registers is ignored if the BACKLIGHT_ENABLE bit is set to 0.

This errata removes the state requirement of the BACKLIGHT_ENABLE bit. Writing to EDP_BACKLIGHT_BRIGHTNESS_MSB and EDP_BACKLIGHT_BRIGHTNESS_LSB is no longer dependent on the state of the BACKLIGHT_ENABLE bit.

3 Embedded DisplayPort Implementation

3.4 eDP AUX Link Services

Table 3-5: Display Control DPCD Registers Listed as Reserved within DisplayPort v1.2

DisplayPort Address	Definition	Read/Write over AUX Channel
00722h	EDP_BACKLIGHT_BRIGHTNESS_MSB Bits 7:0 = Display backlight brightness control, most significant bits. Applies when BACKLIGHT_BRIGHTNESS_CONTROL_MODE = 10 or 11 (register 00721h). When BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 1 (register 00702h), this register provides the most significant 8 bits out of 16 possible bits that can be assigned for setting the display backlight brightness level. When BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 0, this register provides up to 8 bits for setting the display backlight brightness level. The actual number of assigned bits for the backlight brightness PWM generator is set by bits 4:0 of EDP_PWMGEN_BIT_COUNT (register 00724h). If bits 4:0 of EDP_PWMGEN_BIT_COUNT represent a value of more than 8 and BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 0, then only the 8 MSB bits of the brightness control value can be controlled. Note 1 below applies. Assigned bits are allocated to the MSB bits of the enabled register combination. Writes ignored if BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE = 0; (register 00702h), ~~or if BACKLIGHT_ENABLE = 0 (register 00721h)~~, or if TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 0 (register 00701h) Note: The quantity of assigned or controllable bits will have the ability to provide full brightness control. Examples: For 10 bit operation 00h = 0% brightness, and 3FFh = 100% brightness For 8 bit operation, 00h = 0% brightness, and FFh = 100% brightness	Read/Write
00723h	EDP_BACKLIGHT_BRIGHTNESS_LSB	Read/Write

DisplayPort Address	Definition	Read/Write over AUX Channel
	Bits 7:0 = Display backlight brightness control, least significant bits. When BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 1 (register 00702h), this register provides the least significant 8 bits (out of 16 possible bits) that can be assigned for setting the display backlight brightness level. Refer to register 00722h for more information. Writes ignored if BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 0 (register 00702h) BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE = 0 (register 00702h), ~~or if~~ ~~BACKLIGHT_ENABLE = 0 (register 00721h),~~ or if TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 0 (register 00701h)	

Benefits as a Result of the Changes

There is no known reason to prevent the writing of EDP_BACKLIGHT_BRIGHTNESS_MSB and EDP_BACKLIGHT_BRIGHTNESS_LSB when the BACKLIGHT_ENABLE bit is set to 0. What's more, this requirement presents unnecessary system application challenges. The reason for this requirement in eDP v1.3 is unknown and is being removed.

With this modification, the backlight brightness can now always be programmed prior to enabling the backlight, including when the BACKLIGHT_ENABLE bit is used for backlight control. In addition, the backlight brightness can now be programmed when using the eDP connector BL_ENABLE pin, since dependence is removed on the BACKLIGHT_ENABLE bit, which is the alternate mechanism for backlight control.

Assessment of the Impact

Should not impact existing systems, but will allow more flexibility in the future.

Analysis of the Device Hardware Implication

No hardware changes needed, except for new capability that can be added.

Analysis of the Device Software Implications

Software modifications needed only to take advantage of the change.

Analysis of the Compliance Test & Interop Implications

No eDP compliance testing exists at this time. Source devices taking advantage of this modification to eDP 1.3 may not work properly with Sink devices that do not incorporate these changes. One may want to test backlight brightness setting capability is using the EDP_BACKLIGHT_BRIGHTNESS_MSB and/or EDP_BACKLIGHT_BRIGHTNESS_LSB registers.

End of this section

Summary of the Proposed Change(s)

In the case of PSR exit when No Link Training is used (and only in this case), a new requirement is added for the Source device. In eDP 1.3, if the Main Link is Off, Main Link activity is resumed only after the Source receives an ACK from the Sink. This errata stipulates that the Source begins Main Link activity by the end of the wake request to the Sink, instead of waiting for ACK from the Sink.

4 Panel Self Refresh (PSR)

4.3.3.1.1 Source Transmitter Off

If the Source Main Link transmitter is off, upon detecting conditions for PSR exit, a Source must wake the Sink by writing “01h” to DPCD address 600h of the Sink device via the AUX channel. The Sink must send an ACK after powering up its Main Link RX and prepare for link training. Link training is optional and the Sink declares if it is required in the “link training requirement of Sink on PSR exit” field in the DPCD PSR capability registers as described in Section 3.4.

If link training is not required, **upon receiving an ACK from the Sink**, the Source may omit the training phase of link bring up, and move directly to transmission of Idle Patterns. The Source must generate at least 5 Idle Patterns prior to the first valid data (SDP, MSA/VBID/MVID/MAUD or active video frame) sent. The first Idle Pattern sent may start with either a BS or SR sequence. After a minimum of 5 Idle Patterns have been sent, prior to sending the first valid data, the Source is required to send an SR sequence and thereafter maintain the “every 512th BS sequence must be replaced by SR sequence” policy as described in Section 2.2.1.2 of DP v1.2. The Sink must perform clock recovery and symbol lock within five Idle Patterns, instead of using training patterns. The Sink must perform scrambler synchronization after receiving the SR sequence to correctly receive the first valid data.

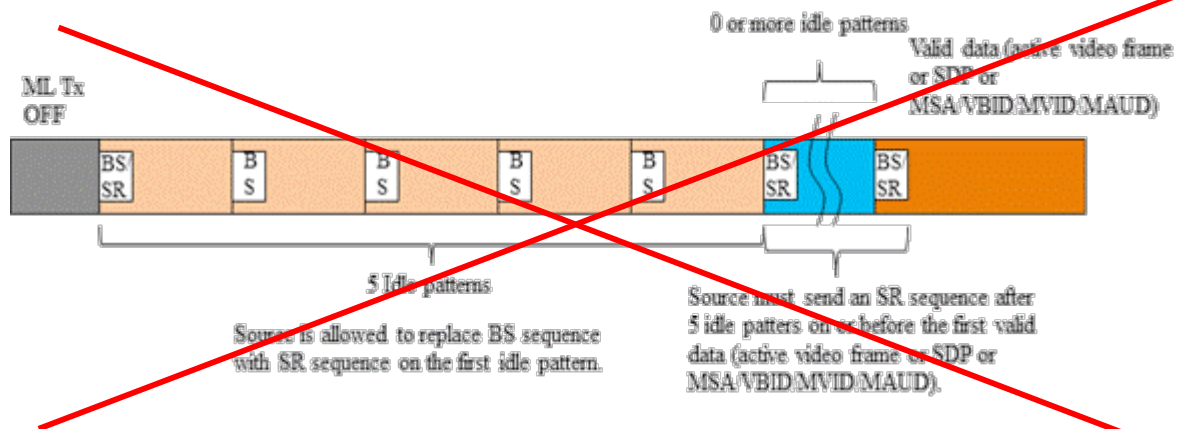


Figure 4-8: PSR Exit Link Management with No Link Training

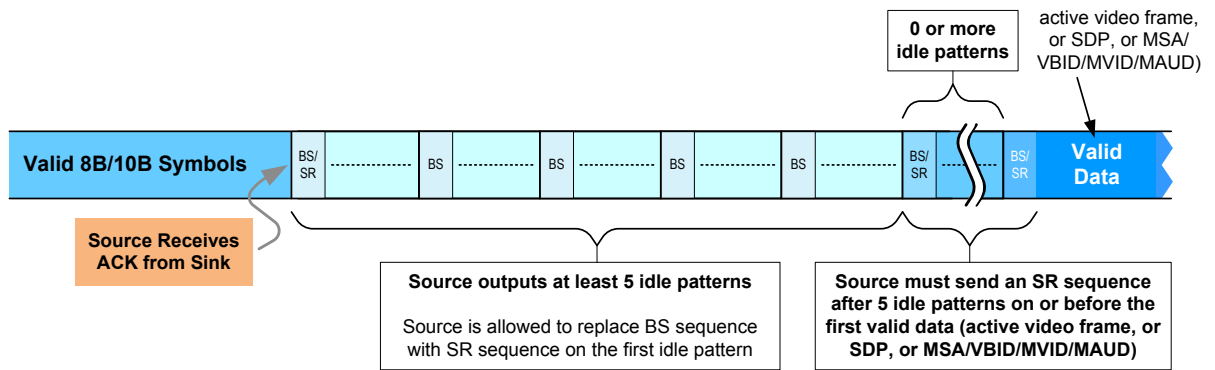


Figure 4-8: PSR Exit Link Management with No Link Training

If link training is not required, the Source must begin transmitting data on the Main Link no later than the end of the wake AUX command which writes “01h” to DPCD address 600h of the Sink. This transmitted data must be a valid 8B/10B symbol sequence. (In addition to normal video content, valid 8B/10B symbol sequences include the idle pattern as well as the D10.2 clock pattern which is Training Pattern 1 used in Link Training).

If link training is needed, a Source initiates link training after receiving an ACK from the Sink, and after satisfying the Main Link common mode pre charge time. **As an option, the Source may begin transmitting data on the Main Link before an ACK is received from the Sink.** This transmitted data may be any valid 8B/10B symbol sequence such as the idle pattern or the D10.2 clock pattern.

In both of the above cases, if the Source doesn’t receive a valid ACK from the Sink after writing “01h” to DPCD address 600h, the Source must retry the AUX write until a 1ms wake up time out period expires, before taking corrective action in an implementation dependent manner. The 1ms wake up time out restriction is applied only to PSR Sinks when the PSR function is enabled.

The Sink must properly handle an SR sequence received after link training is completed.

Note that the Source is not required to write “02h” into register 600h when turning off the Main Link upon PSR entry.

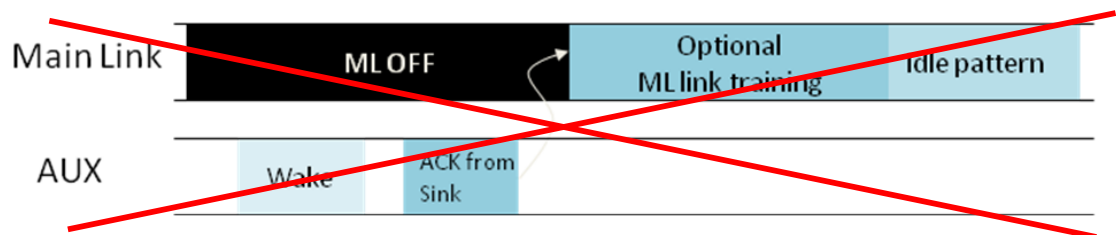


Figure 4-9: PSR Exit Link Management

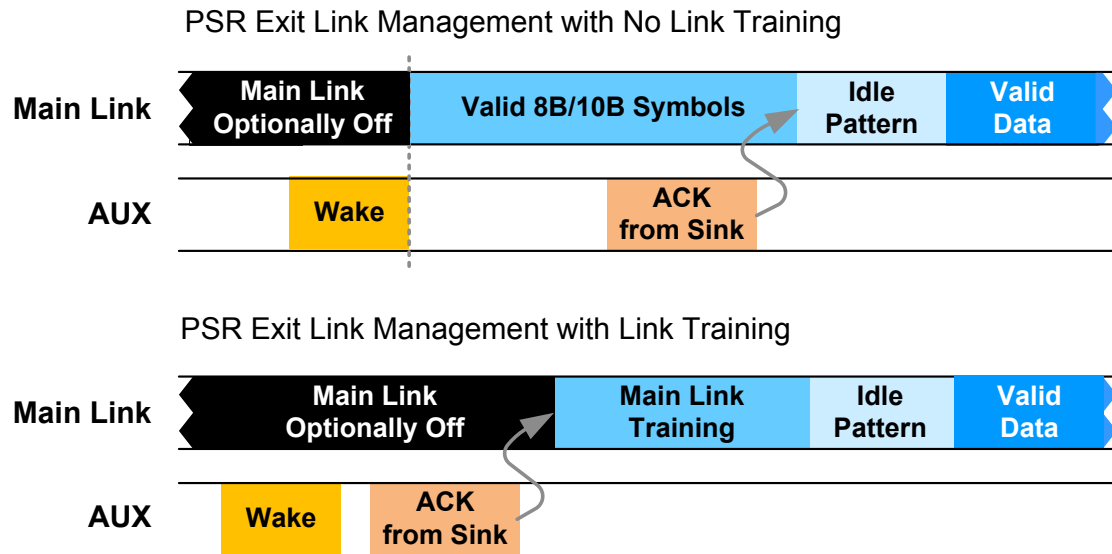


Figure 4-9: PSR Exit Link Management

Benefits as a Result of the Changes

The reason for the proposed change is to allow the Sink CDR (clock-data recovery) unit to begin relocking to the Main Link as soon as the request is received, and while it is replying with an ACK to the Source. This provides additional margin for the Sink's receiver to lock to the Main Link prior to receiving the first video data packets.

This change will also prevent the Sink from attempting to lock to a disabled Main Link signal. In eDP 1.3, the Sink cannot predict when the Source will enable the Main Link output after it receives the ACK from the Sink. Attempting to lock to a disabled Main Link can put the CDR into a state that will lengthen lock time when the Main Link is activated. This additional lock time may prevent the Sink from properly receiving the first valid video packets from the Source.

Assessment of the Impact

May require change in Source device behavior for PSR exit when no link training is used.

Analysis of the Compliance Test & Interop Implications

As PSR Compliance Test development has not yet been initiated, there is no impact.

When using a Source device that does not meet these requirements, PSR with No Link Training should be thoroughly tested with the eDP Panel. PSR exit with Fast Link Training or normal Link Training is not affected.

End of this section



eDP™

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VESA Embedded DisplayPort Standard

Version 1.3

13 January 2011

Purpose

This standard defines requirements and options of a standardized display panel interface for embedded display applications. It is based on the VESA DisplayPort Standard Version 1.2 and includes implementation options recommended for consideration by the system integrator.

Summary

DisplayPort 1.2 is a scalable and extendable video data interface developed for use in both embedded (internal) and external (box-to-box) applications. While DisplayPort™ does reference embedded applications; it is primarily oriented toward external applications with emphasis on interoperability between system vendors and interconnect cables. This standard defines a feature set of an embedded version of DisplayPort for applications including, but not limited to, notebook PCs and all-in-one PCs.

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Preface

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Revision History

December 2008

Initial release of the standard

October 2009

Version 1.1

In Table 3-1, specified requirement for IRQ HPD pulse from Sink HPD connector pin to indicate Sink status change.

Expanded description of Section 3.4 including the definition of applicable Sink DPCD control bits in Table 3-5; removed method 3C; modified description for methods 2, 3a, and 3b as “display authentication”, vs. “content protection” that now only applies to Method 1; added text describing that Method 1 is normally not expected in an eDP Sink.

In the titles for Tables 5-1, 5-2, 5-3, and 5-4, replaced “Connector” with “Pin Assignment” for clarity.

Modified table 5-4 to increase the number of LCD_VDD pins from 2 to 4, and number of LCD_GND pins from 2 to 4, in order to better facilitate LCD logic and driver power demand through the connector and cable.

Updated contributor list for this version

May 2010

Version 1.2

Updated reference from DisplayPort Standard Version 1.1a to Version 1.2, as well as other reference document version updates.

Added 5.4Gbps link rate as an implementation option

Made fast link training mandatory for the Sink

In Table 3-5:

- Added DPCD register to the Sink for Black Video control through the AUX channel
- Added optional DPCD registers to the Sink to control backlight brightness, PWM frequency adjustment, backlight enable, and test mode enable.
- Added optional DPCD registers to the Sink to control new optional display functions including dynamic backlight control, color engine, dithering and FRC.
- Added DPCD register to indicate if LCD panel includes the LCD overdrive function.
- Added DPCD register to indicate if SET_POWER DPCD register 00600h has effect on the Sink
- Added Section 3.8 to explain backlight brightness and PWM frequency control options

In Table 3-6, for Method 3a, added capability to enable and disable ASSR during normal operation along with mandated requirements for the Sink and Source during such operation.

In Table 4-1:

- For item T7, added that Sink will set SINK_STATUS
- For item T9, added that Sink will reset the SINK_STATUS bit

In Tables 5-3 and 5-4, signals BL_ENABLE and BL_PWM_DIM were made optional, since these controls are now possible through the AUX channels as per Table 3-5.

January 2011

Version 1.3

Added support for Panel Self Refresh (PSR) by adding PSR register descriptions to Section 3.4, adding Section 3.5 to describe a Secondary Data Packet to support PSR, & adding Section 4, describing PSR support

Updated Table 3-1 to include PSR. Updated Section 4.2 (PSR configuration section) to simplify the flow.

Clarified Section 4.3.3.1 about when to send SR sequence when no link training option is used. Updated Figure 5-1 to include PSR as well as active video.

Clarified in Table 3-1 that secondary packet support is required for PSR support. Updated Table 3-3 to include columns for 5.4Gbps and row for WQXGA.

Updated description of VBLANK_BACKLIGHT_UPDATE_ENABLE, bit 7 of DPCD 720h to indicate new backlight settings will be applied at start of vertical blank.

Reduced size of SINK SELF REFRESH STATUS field in DPCD 2008h to 3 bits. Added 1 bit to both fields in DEBUG REGISTER 0, DPCD 2009h, and defined value of 8h = more than 8 lines.

In Section 3.9 clarified that 27MHz clock in Figure 3-9 is an internal signal and is generated in an implementation-specific manner.

In Table 3-1 changed Enhanced framing from optional to recommended.

Section 4.3.6 updated to indicate SDP timing requirements after the initial single frame update for burst single frame updates.

1 Overview

1.1 Background

This document describes a standardized set of DisplayPort interface features for use in an embedded display application. This embedded interface is known as eDP™ (Embedded DisplayPort) and is the electrical transport for video and auxiliary data between the system motherboard (graphics hardware) and the display panel. eDP applications include notebook PCs, all-in-one PCs, and other systems that incorporate the display panel with the video or graphics processor.

The DisplayPort Standard Version 1.2 primarily addresses external box-to-box interfaces. The external interface must interoperate with any connected compliant system over a variety of compliant cables. Link training is used to determine the number of lanes supported, link rate, link voltage swing, and pre-emphasis needed to send raw data at the target bit-error-rate floor of 10^{-9} , over a given cable to a given Sink device.

eDP is based on the DisplayPort Standard v1.2 and provides an interoperability guideline for system integrators and panel makers. It is the responsibility of the system integrator to determine the appropriate eDP feature set for a given platform, based on platform requirements and component capability.

1.2 Acronyms

Acronym	Stands for:
AAC	Advanced Audio Coding
AACS	Advanced Access Content System
ASSR	Alternate Scrambler Seed Reset
AUX, or AUX Channel	DisplayPort Auxiliary Channel
bpc	Bits Per Component
bpp	Bits Per Pixel
BE	Blanking End
BS	Blanking Start
CDR	Clock and Data Recovery
CRC	Cyclic Redundancy Check
DBC	Dynamic Backlight Control
CSS	Content Scramble System
DDC/CI	Display Data Channel/Command Interface (VESA)
DP	DisplayPort (VESA)
DPCD	DisplayPort Configuration Data
EDID	Extended Display Identification Data (VESA)
eDP	Embedded DisplayPort (VESA)
FRC	Frame Rate Control
GPU	Graphics Processing Unit
HBR	High Bit Rate (2.7Gbps per lane)
HBR2	High Bit Rate 2 (5.4Gbps per lane)
HDCP	High-bandwidth Digital Content Protection
HPD	Hot Plug Detect
LCD	Liquid Crystal Display
LCDVCC	Liquid Crystal Display Voltage Charge Connection
MAUD	M value for audio
MCCS	Monitor Control Command Set (VESA)
MSA	DisplayPort Main Stream Attribute
MVID	M value for video
OSD	On Screen Display
OUI	Organization Unique ID
PCB	Printed Circuit Board
PSR	Panel Self Refresh
PWM	Pulse Width Modulation
RBR	Reduced Bit Rate (1.62Gbps per lane)
RFB	Remote Frame Buffer
SDP	Secondary Data Packet
SR	Scrambler Reset
SSC	Spread Spectrum Clock
TCON	Timing Controller
VB-ID	Vertical Blanking ID
VESA	Video Electronics Standards Association
VSC	Video Stream Configuration

1.3 Glossary

Terminology	Definition
Active Frame	Active frame indicates active pixel data in a video frame.
Active stream	Stream from the Source on the Main Link carrying a main video stream.
AUX or AUX Channel	A half-duplex, bidirectional channel within the DisplayPort interface; short for “Auxiliary Channel”. Consists of one differential pair transporting self-clocked data. Used to transport data between the Source and Sink device (such as EDID information, link status, and MCCS data). The DisplayPort AUX Channel supports a bandwidth of 1Mbps. The DisplayPort Source is the master (also referred to as AUX Channel Requester) that initiates an AUX Channel transaction. The DisplayPort Sink is the slave (also referred to as AUX Channel Replier) that replies to the AUX Channel transaction initiated by the Requester. The AUX Channel is used by the Source to read and write data from and to the DisplayPort Configuration Data (DPCD) register in the Sink device.
Color Engine	Circuitry within an eDP TCON that is designed to create more vivid and/or more accurate colors on the display. Implementation is panel specific and the visual effect may differ between panel models.
DisplayPort receiver	Circuitry that receives the incoming DisplayPort Main Link data. Also contains the transceiver circuit for AUX Channel. Located in Sink device and in the receiving port upstream port of any Intermediate device.
DisplayPort transmitter	Circuitry that transmits the DisplayPort Main Link data. Also contains the transceiver circuit for AUX Channel. Located in Source Device and in the transmitting port of any Intermediate Device.
Dynamic Backlight Control	Circuitry within an eDP TCON that can reduce total panel power dissipation by automatically adjusting the backlight brightness and pixel values based on the characteristics of the displayed image. Implementation is panel-specific and the visual effect may differ between panel models.
Frame Rate Control	A term used to describe temporal dithering of the component value of a single pixel that is employed to emulate color resolution beyond the native ability of a given display.
LCDVCC	LCD main power
Link layer	Server providing services as instructed or requested by the stream-/link-policy maker
Main Link	High-speed, unidirectional data channel within the DisplayPort interface used for channel data transport from DisplayPort Source to DisplayPort Sink. Used to transport video and other stream data. Can also transport audio. The Main Link can consist of one, two, or four lanes; each lane is a differential signal pair. One of three bit rates can be used: 5.4Gb/s per lane (referred to as “High Bit Rate 2”), 2.7Gb/s per lane (referred to as “High Bit Rate”) or 1.62Gb/s per lane (referred to as “Reduced Bit Rate”).
PSR active	Indicates Panel Self Refresh state in Source and Sink. <u>Source PSR active:</u> Indicates that Source is in one of the panel self refresh active states. Refer to section 4.3.1.1 for details of Source PSR states. <u>Sink PSR active:</u> Indicates that Sink is in one of PSR active states. Refer to section 4.3.1.2 for details of Sink PSR states.
PSR inactive	Indicates inactive Panel Self Refresh state in Source and Sink. <u>Source PSR inactive:</u> Indicates that Source is not in a PSR active state. <u>Sink PSR inactive:</u> Indicates that Sink is not in a PSR active state and is not displaying from the Remote Frame Buffer.
PSR entry event/indication	Source PSR state transition from inactive to active
PSR exit event/indication	Source PSR state transition from active to inactive
Pulse Width Modulation	The modulation of the duty cycle of a periodic digital signal to produce the effect of a variable signal level when subjected to the integration of a low pass filter or human perception capability.

Sink Device	Within this eDP standard, the Sink device refers to the eDP panel. Within the overall context of DisplayPort, a Sink device contains one Sink function and at least one rendering function, and is a Leaf device in a DisplayPort tree topology. A Sink receives an AV stream for video display and/or sound reproduction.
Static Image/Static frame	Image/frame that is to be locally displayed from the Remote Frame Buffer (RFB).
Source Device	Within this eDP standard, a Source device normally refers to the GPU or integrated graphics on the system motherboard. Within the overall context of DisplayPort, a Source is the originating device of an isochronous AV stream.
Video frame	A Video frame includes the vertical and horizontal blanking periods and active pixel data. It spans from the first BS sequence at the start of vertical blank to the last active pixel of the last active line.

1.4 References

Table 1-1: Reference Documents

Document	Version / Revision	Date
VESA Policy 200 Intellectual Property Rights	Version B	February 2005
VESA Enhanced Extended Display Identification Standard (E-EDID)	Rel. A/ Rev. 2	September 2006
VESA Coordinated Video Timings (CVT)	Version 1.1	September 2003
VESA DisplayPort Standard	Version 1.2	January 2010
VESA DisplayPort Link Layer Compliance Test Specification	Version 1.1a	October 2009
VESA DisplayPort PHY Compliance Test Specification	Version 1.1a	October 2009
VESA Display ID Data Structure Standard (DisplayID)	Version 1.1	March 2009
VESA Monitor Control Command Set (MCCS)	Version 2.2	January 2009

2 eDP System Architecture

2.1 eDP System Application

The typical system application of eDP is shown in Figure 2-1, below. The eDP Source function is typically integrated into the video/graphics processor circuit, such as in the GPU of a notebook PC. The eDP Sink function is normally integrated into the display processor, such as in the LCD timing controller (TCON) of a notebook PC.

The cable used for the eDP interconnect will be chosen by the system integrator to consider cost, signal integrity, EMI performance, mechanical space, etc. Typically a 20- or 30-pin connector will be used for one and two-lane implementations.

In a system application using an LCD display panel, the display panel will typically include the TCON, gate (row) and column drivers, and backlight control. An EPROM will normally be connected to the TCON containing EDID information for the particular panel, and it may also contain configuration registers for TCON operation.

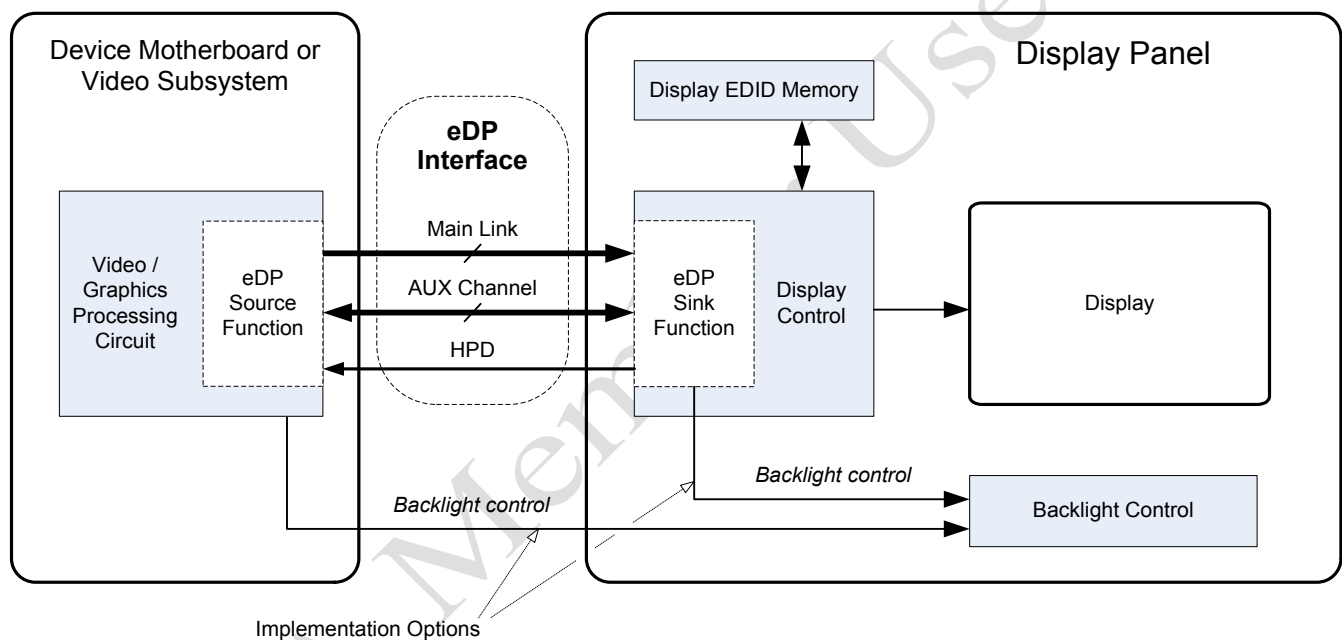


Figure 2-1: Typical System Implementation of eDP

2.2 eDP Support by Source and Sink Components

Except where otherwise described in this document, an eDP Source and Sink device must be fully compatible with the DisplayPort 1.2 Standard. Typically only one or two Main Link lanes will be needed due to the limited panel resolution normal for embedded application. The eDP Sink device must support Fast Link Training, and support of Fast Link Training by the Source device is an implementation option.

3 Embedded DisplayPort Implementation

3.1 Background

Embedded DisplayPort, or eDP, is based on the VESA DisplayPort Standard v1.2. Some features specified with DisplayPort v1.2 are optional with eDP v1.2 devices, as itemized in Table 3-1. It is up to the system integrator to determine which set of options are needed.

3.2 eDP Feature Requirements and Recommendations

Table 3-1, below, provides a list of eDP features, some of which are optional as noted. For further description of any feature items, refer to DP v1.2.

Table 3-1: eDP Features and Recommended Configurations

eDP Feature	Recommended Configuration	Note
Audio	Optional	Dependent on usage requirements
Backlight Control via TCON	Optional	Backlight control by the Source can be provided directly via separate control signals from the system control function. Two methods available include use of the BL_PWM_DIM pin listed in Tables 5-3 and 5-4, and AUX Channel control as described in Sections 3.4 and 3.9.
Bit Depth	6 or 8 bpc	Video component bit depth is implementation specific and is not limited to 6 or 8 bits per color (bpc)
Display Authentication / Content Protection	Recommended	See Section 3.6 below. Support of methods 3a and 3b are recommended for Sink devices.
Display Control Registers	Optional	DisplayPort DPCD registers 00700h-007FFh are reserved for eDP display control use and are described in Sections 3.4 and 3.9. As an implementation option, MCCS can also be used for display control if supported by the Source and Sink.
DPCD Revision	DPCD Rev 1.2 or later	The DPCD revision number is specified at DPCD address 0000h.
EDID	Yes	EDID support simplifies the use of different panels with one system board. EDID 1.4 must be supported. Use of VESA DisplayID is an implementation option.
Enhanced Framing	Yes	Enhanced Framing provides increased robustness over Basic Framing.
HPD Pin on Sink	Yes	The HPD pin is required on the Sink, and the HPD pin will support all functions required for the HPD (Hot Plug Detect) pin defined in the DisplayPort 1.2 standard, including the IRQ HPD pulse used for Sink device status change notification including link failure notification. Use of the HPD signal by the Source is optional. The HPD conductor in the connector cable can be omitted if HPD is not used by the Source. To replace the HPD interrupt function asserted by the Sink, the Source can instead use Sink polling. Support for polling by the Source devices is optional. To monitor integrity of the Main Link, the Source will poll the Sink at regular intervals. Use of HPD is generally preferred over polling by the Source as Source polling may increase system power dissipation.
LCD Panel Self-Test	Optional	See Section 3.10. Provides a system diagnostics tool.
LCDVCC	Single Supply	See Section 3.7. Use of a single power rail is an implementation option, as is the supply voltage level.
Link Rate	1.62 or 2.7Gbps	The link rate that minimizes the number of lanes should be used. 5.4Gbps is an implementation option.

eDP Feature	Recommended Configuration	Note
Link Training	Full Link Training	The eDP device (Source and Sink) must be capable of supporting full link training. Fast link training is mandatory on the Sink, and is an implementation option on the Source.
Main Stream Attribute (MSA) Data	Option to ignore certain Data Fields	See Section 3.8.
MCCS Support	Optional	Can be used for display control and host-based software OSD, including, for example, backlight control. The Display Control Registers listed in Table 3-5 can alternately be used for display control.
Number of Main Link Lanes	Fewest lanes possible	See Section 3.3. The preference is to minimize the number of lanes. Table 3-3 provides the number of lanes for common eDP configurations.
Panel Self Refresh	Optional	Must be supported by both Source and Sink to implement this feature
Safe Mode (640x480 or other default video resolution)	No	The panel will always be driven at native resolution.
Secondary- Data Packet	Optional	Dependent on usage requirements. Required for the optional Panel Self Refresh support.
Source Detection via AUX Channel	Not required	Pull-up and pull-down resistors are not required on the Source AUX Channel pin for Source detection. Likewise, the Sink is not required to perform Source detection via the AUX Channel. Refer to the Recommended eDP AUX Channel Topology in Figure 3-1 below.

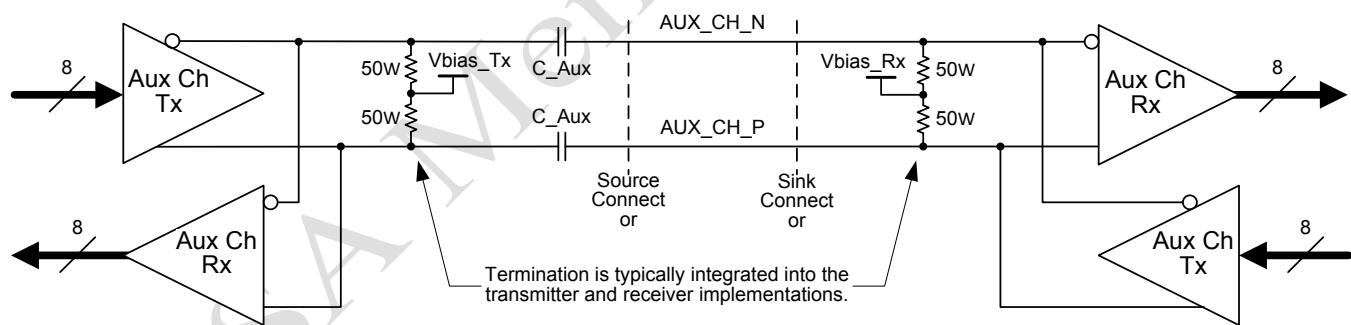


Figure 3-1: Recommended eDP AUX Channel Topology

3.3 Number of Main Link Lanes vs. Video Mode Support (Informative)

The number of Main Link lanes required in the eDP interface will depend on the panel display resolution and color depth. For example, most notebook PC applications will only require one or two Main Link lanes. It is recommended that the minimum number of lanes be used, using the minimum link rate allowed for that lane configuration. This section explains the relationship between the panel video mode and the required number of Main Link lanes and link rate.

The bit rate for a given Main Link configuration can be calculated as follows:

$$\text{Bit Rate Capacity} = (\text{Link Rate}) * (\text{Number of Lanes}) * (0.8 \text{ for } 8B/10B \text{ coding overhead})$$

So for example, 2 lanes at 2.7GHz link rate would have the following capacity:

$$\text{Bit Rate Capacity} = (2) * (2.7\text{Gbps}) * 0.8 = 4.32\text{Gbps}$$

Bit rate capacities for all possible Main Link configurations are shown in Table 3-2 below.

Table 3-2: Bit Rate Capacity for Possible eDP Main Link Configurations (Informative)

Lane Count	1 Lane			2 Lanes			4 Lanes		
Lane Rate (Gbps)	1.62	2.7	5.4	1.62	2.7	5.4	1.62	2.7	5.4
Max Data Capacity (Gbps)	1.296	2.16	4.32	2.592	4.32	8.64	5.184	8.64	17.28

The bit rate *requirements* for a given video mode can be calculated as follows:

$$\text{Bit Rate Requirement} = (\text{Pixel Clock Rate}) * (\text{bits-per-pixel, or bpp})$$

Note: This calculation assumes one video stream.

The WSXGA+ mode (1680x1050 pixels), using reduced blanking has a pixel clock of 119MHz. When displayed at 18bpp:

$$\text{Bit Rate Requirement} = (119\text{MHz}) * (18) = 2.142\text{Gbps}$$

Thus, WSXGA+ can be transported using just 1 Main Link lane at the 2.7Gbps rate. This configuration is preferred over two lanes at the reduced bit rate.

Table 3-3 below shows the preferred and optional Main Link lane counts for common display formats using common eDP Main Link configurations. The preferred configuration, as indicated by “P”, is based on the minimum lane count configuration, using the lowest link rate that supports that lane count, using link rates of 2.7Gbps (HBR) and 1.62Gbps (RBR) only. The 5.4Gbps link rate is included for reference for those systems that optionally implement 5.4Gbps.

Table 3-3: Supported Video Mode Examples for Common eDP Configurations (Informative)

Common Video Mode Name	VESA Timing Name (Horizontal x Vertical @ Frame Rate)	Pixel clock Rate (MHz)	18 bits per pixel				24 bits per pixel			
			Stream Bit Rate (Gbps)	Required Number of Main Link Lanes			Stream Bit Rate (Gbps)	Required Number of Main Link Lanes		
				@ 1.62 Gbps	@ 2.7 Gbps	@ 5.4 Gbps (1)		@ 1.62 Gbps	@ 2.7 Gbps	@ 5.4 Gbps (1)
XGA	1024x768 @ 60Hz CVT (Reduced Blanking)	56	1.01	1 (P)	1	1	1.34	2	1 (P)	1
WXGA	1280x768 @ 60Hz CVT (Reduced Blanking)	68.25	1.23	1 (P)	1	1	1.64	2	1 (P)	1
WXGA	1280x800 @ 60Hz CVT (Reduced Blanking)	71	1.28	1 (P)	1	1	1.70	2	1 (P)	1
HD	1366x768 @ 60Hz	85.5	1.54	2	1 (P)	1	2.05	2	1 (P)	1
WXGA+	1440x900 @ 60Hz CVT (Reduced Blanking)	88.75	1.60	2	1 (P)	1	2.13	2	1 (P)	1
SXGA+	1400x1050 @ 60Hz CVT (Reduced Blanking)	101	1.82	2	1 (P)	1	2.42	2 (P)	2	1
HD+	1600x900 @ 60Hz (Reduced Blanking)	108	1.94	2	1 (P)	1	2.59	4	2 (P)	1
WSXGA+	1680x1050 @ 60Hz CVT (Reduced Blanking)	119	2.12	2	1 (P)	1	2.86	4	2 (P)	1
UXGA	1600x1200 @ 60Hz CVT (Reduced Blanking)	130.25	2.34	2 (P)	2	1	3.13	4	2 (P)	1
FHD	1920x1080 @ 60Hz	148.5	2.67	4	2 (P)	1	3.56	4	2 (P)	1
WUXGA	1920x1200 @ 60Hz CVT (Reduced Blanking)	154	2.77	4	2 (P)	1	3.70	4	2 (P)	1
WQXGA	2560x1600 @ 60Hz CVT (Reduced Blanking)	268.5	4.83	4 (P)	4	2	6.44	N/A	4	2

Notes: Use of 5.4 Gbps Main Link rate is an implementation option. (P) denotes the *preferred* eDP Configuration, when not using the optional 5.4 Gbps Main Link rate. Modes with packing ratios near 99% or higher may oversubscribe if the video stream clock is generated asynchronous to the link clock within the Source, especially when SSC is enabled. In such cases, a main link configuration with a bit rate higher than the denoted ‘preferred’ configuration may be considered.

3.4 eDP AUX Link Services

For eDP, the use of AUX Channel is the same as described by the DisplayPort Standard, but with the following exceptions:

- The use of HPD is not required by the Source. When HPD is not used, polling by the Source would replace the HPD interrupt function.
- This eDP Standard defines certain DPCD registers and register bits that are otherwise identified as “reserved” within the DP 1.2 Standard. This includes bit 3 of register address 0000Dh in Table 3-4 below, and the display control DPCD registers 00700h-007FFh as shown in Table 3-5, below. It also includes DPCD registers to support the optional Panel Self Refresh feature, as defined in tables 3-5 through 3-8.

For eDP, enhanced display control capability has been added through the definition of new DisplayPort DPCD registers. These registers are located in the DPCD register address field 00700h-007FFh, which is defined as “RESERVED for eDP” in the current DP 1.2 Standard. These display control registers provide ability for the Source to control display characteristics such as backlight brightness and backlight PWM modulation frequency, and the ability to enable and disable certain display features such as dynamic backlight control, color engine, FRC, and other attributes. As with other the DPCD registers, these new control registers will only exist in the Sink device, and will be read and/or written to by the Source device. The “Read Only” registers allow the Sink device to convey capability information to the Source device. The “Write/Read” registers are used by the Source to set characteristics within the Sink. It is the responsibility of the Source to first read the Sink capability before attempting to set Sink characteristics through the control registers. It is anticipated that additional registers within the 00700h-007FFh field will be defined in future versions of the eDP Standard to further enhance display control capability.

To allow Source devices to easily identify panels that utilize these 00700h-007FFh address field control registers, bit 3 of DPCD register 0000Dh has been assigned to indicate this capability. In the DisplayPort 1.2 standard, bit 3 of register 0000Dh is listed as RESERVED. For eDP 1.2 or higher this bit has been assigned as described in Table 3-4.

Table 3-4: Assignment of DPCD Register 0000Dh Bit 3 within eDP v1.2

DisplayPort Address	Definition	Read/Write over AUX Channel
<i>Within Receiver Capability Field</i>		
0000Dh	eDP_CONFIGURATION_CAP Always reads 00h for external receivers. For Embedded DisplayPort (eDP) receivers: Bit 0 = ALTERNATE_SCRAMBLER_RESET_CAPABLE A setting of 1 indicates that this is an eDP device that can use the eDP alternate scrambler reset value of FFFEh. Bit 1 = FRAMING_CHANGE_CAPABLE A setting of 1 indicates that this is an eDP device that uses only Enhanced Framing, independently of the setting by the Source of ENHANCED_FRAME_EN	Read Only

DisplayPort Address	Definition	Read/Write over AUX Channel
	Bit 2 = RESERVED for eDP. Read 0s. Bit 3 = DPCD_DISPLAY_CONTROL_CAPABLE A setting of 1 indicates that display control registers starting at address 00700h are enabled. Bits 7:4 = RESERVED for eDP. Read all 0s.	

Table 3-5 provides the list of registers defined by the eDP Standard within the DPCD register address field 00700h-007FFh (this address field is listed as “RESERVED” within DP v1.2). The address field begins with an eDP revision (or version) identifier. Those displays reporting eDP version 1.1 or lower (indicated by a value of 00h) will have 00h values in registers 00701h-007FFh since no enhanced display control capability will be supported. For eDP version 1.2 and higher, the Source will read the eDP capability registers starting at address 00701h. Through the use of read/write registers 00720h-007FFh, the Source will be able to control certain aspects of the display, based on the capabilities reported in address 00701h-0071Fh.

To enable the function of the backlight control registers, it is necessary for the backlight controller to be located on the panel, and for the TCON to interface with the backlight controller. See Section 3.9 for more information on this topic.

Below is a summary of display control capability added by eDP v1.2 through the definition of new DPCD registers within the 00700h-007FF address field, as listed in Table 3-5.

- Backlight brightness control
 - A variable bit-width brightness control option is allowed to provide the option to eliminate the wire for the eDP connector pin BL_PWM_PIN in tables 5-3 and 5-4.
- Backlight enable
 - The addition of a backlight enable control bit provides the option to eliminate the wire for the eDP connector pin BL_ENABLE in tables 5-3 and 5-4.
- Backlight brightness control through the PWM input and DPCD register value combination
 - Brightness can be controlled by the product of the PWM input pin and DPCD register value. This can facilitate dynamic backlight control by the GPU.
- Backlight PWM frequency control
 - The PWM frequency provided by the TCON can be established through register setting.
- Dynamic Backlight Control (DBC)
 - A bit has been assigned to enable/disable the dynamic backlight control (DBC) feature in panels that include this capability. DBC can reduce total panel power dissipation by automatically adjusting the backlight brightness and LCD values based on the characteristics of the displayed image. While the function of the DBC control bit is defined in this specification, DBC implementation specifics are not defined, including the interaction with other DPCD register settings. The DBC implementation, visual performance, and power savings characteristics may differ between specific panels.
- Color Engine Enable (CEE)

- A bit has been assigned to enable/disable the color engine feature in panels that include this capability. The color engine feature is designed to create more vivid and/or more accurate colors on the display. As with DBC, this specification defines the function of the CEE control bit but not the specific color engine implementation or the interaction with other DPCD register settings. Color engine implementation and visual performance may differ between specific panels.
- Dithering and FRC (Frame Rate Control)
 - A bit has been assigned to enable/disable the FRC function, when provided. The FRC function applies temporal dithering of the pixel color value to provide the subjective appearance of color resolution beyond the native color resolution of the display. Typically the FRC function will add 2 virtual bits of color depth, however implementation may vary between panel vendors. For a 2 bit FRC, a 6bpc panel would accept 8bpc pixel data and would dither the 6 bit pixel value accordingly; an 8 bit panel would accept 10bpc and dither the 8 bit pixel value. FRC implementation and visual performance may vary between specific panels.
- Black Video control
 - Through the use of an assigned control bit, manual control for the generation of Black Video is provided.
- LCD Overdrive indication by the Sink
 - LCD Overdrive functionality within the display is reported by the Sink, allowing video data processing adjustments to be made by the Source if needed.

Table 3-5 defines the DPCD registers that use the 00700h-007FFh address fields, which are defined as “Reserved for eDP” in DP v1.2.

Table 3-5: Display Control DPCD Registers Listed as Reserved within DisplayPort v1.2

DisplayPort Address	Definition	Read/Write over AUX Channel
<i>Within Sink Control Field</i>		
00700h	EDP_REV 00h = eDP v1.1 or lower 01h = eDP v1.2 02h = eDP v1.3 If DPCD_DISPLAY_CONTROL_CAPABLE = 1 in DPCD register 0000Dh, then register must contain a value of 01h or higher	Read Only
00701h	EDP_GENERAL_CAPABILITY_REGISTER_1 Bit 0 = TCON_BACKLIGHT_ADJUSTMENT_CAPABLE A setting of 1 indicates the TCON has brightness and/or PWM frequency control capabilities for the backlight. Refer to EDP_BACKLIGHT_ADJUSTMENT_CAPABILITIES_REGISTER for a complete description of backlight control capabilities. A setting of 0 indicates the BL_PWM_DIM pin of the eDP connector controls the backlight controller directly (the TCON is bypassed). Refer to Section 3.9 for further information. Bit 1 = BACKLIGHT_PIN_ENABLE_CAPABLE A setting of 1 indicates the Sink supports the BL_ENABLE pin on the eDP	Read Only

DisplayPort Address	Definition	Read/Write over AUX Channel
	connector. Must be set to 1 if BACKLIGHT_AUX_ENABLE_CAPABLE = 0 Bit 2 = BACKLIGHT_AUX_ENABLE_CAPABLE A setting of 1 indicates the Sink supports display backlight enable through the BACKLIGHT_ENABLE control bit (register 00720h). Must be set to 1 if BACKLIGHT_PIN_ENABLE_CAPABLE = 0 Bit 3 = PANEL_SELF_TEST_PIN_ENABLE_CAPABLE A setting of 1 indicates the panel supports the LCD_Self_Test pin on the eDP connector as described in Section 3.10. Bit 4 = PANEL_SELF_TEST_AUX_ENABLE_CAPABLE A setting of 1 indicates the panel supports the PANEL_SELF_TEST_ENABLE bit in DPCD register 0010Ah (refer to the DisplayPort Standard). Bit 5 = FRC_ENABLE_CAPABLE A setting of 1 indicates the panel supports the FRC_ENABLE control bit (register 00720h). Bit 6 = COLOR_ENGINE_CAPABLE A setting of 1 indicates the Sink includes color engine capability which is controlled by the COLOR_ENGINE_ENABLE bit (register 00720h). Bit 7 = SET_POWER_CAPABLE A setting of 1 indicates that the panel power state can be controlled through SET_POWER DPCD register 00600h. A setting of 0 indicates that the SET_POWER DPCD register 00600h has no effect on the panel. This bit must have a value of 1 if PSR is supported, as indicated by the PANEL_SELF_REFRESH_CAPABILITY_SUPPORTED_AND_VERSION DPCD field (register 00070h).	
00702h	EDP_BACKLIGHT_ADJUSTMENT_CAPABILITY_REGISTER When TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 1, these register bits describe backlight control capability. When TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 0, these register bits have no meaning (any of the bits might read 0 or 1). Bit 0 = BACKLIGHT_BRIGHTNESS_PWM_PIN_CAPABLE A setting of 1 indicates the Sink supports backlight brightness adjustment through the BL_PWM_DIM pin of the eDP connector. Must be set to 1 if BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE = 0 Bit 1 = BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE A setting of 1 indicates the Sink supports backlight adjustment through DPCD control registers EDP_BACKLIGHT_BRIGHTNESS_MSB or EDP_BACKLIGHT_BRIGHTNESS_MSB and	Read Only

DisplayPort Address	Definition	Read/Write over AUX Channel
	EDP_BACKLIGHT_BRIGHTNESS_LSB (registers 00722h and 00723h). Must be set to 1 if BACKLIGHT_BRIGHTNESS_PWM_PIN_CAPABLE = 0 Bit 2 = BACKLIGHT_BRIGHTNESS_BYTE_COUNT A setting of 1 indicates the Sink supports two bytes for the backlight brightness setting value using EDP_BACKLIGHT_BRIGHTNESS_MSB and EDP_BACKLIGHT_BRIGHTNESS_LSB (registers 00722h and 00723h). A setting of 0 indicates the Sink supports only one byte for backlight brightness setting value using EDP_BACKLIGHT_BRIGHTNESS_MSB. Only valid if BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE = 1. Bit 3 = BACKLIGHT_AUX-PWM_PRODUCT_CAPABLE A setting of 1 indicates the Source can combine the backlight brightness levels set through AUX and the BL_PWM_DIM pin of the eDP connector (through the setting of register 00721h bits 1,00 to 11). This mode of operation uses the product of the two values to set the panel brightness, Must be 0 if BACKLIGHT_BRIGHTNESS_PWM_PIN_CAPABLE = 0 or BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE = 0. See section 3.9 for more information. Bit 4 = BACKLIGHT_FREQ_PWM_PIN_PASS-THRU_CAPABLE A setting of 1 indicates the ability to directly pass the PWM frequency applied to the BL_PWM_DIM pin to the backlight current source. This operation is enabled with the BACKLIGHT_FREQ_PWM_PIN_PASS-THRU_ENABLE bit (register 00721h). Must be 0 if BACKLIGHT_BRIGHTNESS_PWM_PIN_CAPABLE = 0 Bit 5 = BACKLIGHT_FREQ_AUX_SET_CAPABLE A setting of 1 indicates the Source can set the PWM frequency of the backlight current source through the EDP_BACKLIGHT_FREQ_SET register (register 00728h). Bit 6 = DYNAMIC_BACKLIGHT_CAPABLE A setting of 1 indicates the Sink includes dynamic backlight control capability through the assertion of the DYNAMIC_BACKLIGHT_ENABLE bit (register 00721h). Bit 7 = VBLANK_BACKLIGHT_UPDATE_CAPABLE A setting of 1 indicates the panel supports the application of all new backlight settings to the next vertical blanking period, as controlled by the VBLANK_BACKLIGHT_UPDATE_ENABLE bit (register 00720h). A setting of 0 indicates that the panel can only apply new settings immediately.	
00703h	EDP_GENERAL_CAPABILITY_REGISTER_2 Bit 0 = OVERDRIVE_ENGINE_ENABLED A setting of 1 indicates the Sink includes LCD Overdrive functionality. Bits 1-7: RESERVED. Read all 0s.	Read Only
00704h-	RESERVED for future eDP capabilities registers	Read all 0s

DisplayPort Address	Definition	Read/Write over AUX Channel
0071Fh		
00720h	EDP_DISPLAY_CONTROL_REGISTER Bit 0 = BACKLIGHT_ENABLE Source sets to 1 to enable the display backlight. This bit has no effect on other display functions. Writes ignored if BACKLIGHT_AUX_ENABLE_CAPABLE = 0 (register 00701h) Power-on default value = 0 Use of this control bit by the panel is optional if TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 0 (register 00701h) Bit 1 = BLACK_VIDEO_ENABLE Source sets to 1 to enable Black Video on display (input video data is overwritten) Power-on default value = 0 (Black Video automatically enabled/disabled only, refer to Section 5.) Bit 2 = FRC_ENABLE Source sets to 1 to enable 2 bit Frame Rate Control from TCON output that drives column drivers. Writes ignored if FRC_ENABLE_CAPABLE = 0 (register 00701h) Power-on default value = 0 (no FRC enabled) Bit 3 = COLOR_ENGINE_ENABLE Source sets to 1 to enable color engine feature in Sink. Writes ignored if COLOR_ENGINE_CAPABLE = 0 (register 00701h) Power-on default value = 0 (no color engine enabled) Bits 6:4 Reserved. Read all 0s. Bit 7 = VBLANK_BACKLIGHT_UPDATE_ENABLE Source set to 1 to enable the panel to apply all new backlight settings at the start of the next vertical blanking interval. Writes ignored if VBLANK_BACKLIGHT_UPDATE_CAPABLE = 0 (register 00702h). Power-on default value = 0 (panel will update any new backlight settings immediately)	Read/Write
00721h	EDP_BACKLIGHT_MODE_SET_REGISTER When TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 1, (register 00701h) the availability of these control modes are declared by EDP_BACKLIGHT_ADJUSTMENT_CAPABILITIES_REGISTER (register 00702h). When TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 0, writes to these register bits will be ignored. (Refer to Section 3.9 for more information)	Read/Write

DisplayPort Address	Definition	Read/Write over AUX Channel
	Bits 1,0 = BACKLIGHT_BRIGHTNESS_CONTROL_MODE 00 = Backlight controlled by BL_PWM_DIM pin on eDP connector 01 = Backlight brightness pre-set level (panel default level) 10 = Backlight controlled by DPCD registers 00722h and 00723h 11 = Backlight controlled by product of BL_PWM_DIM and registers 00722h and 00723h If BACKLIGHT_BRIGHTNESS_PWM_PIN_CAPABLE = 1 (register 00702h), Power-on default = 00. If BACKLIGHT_BRIGHTNESS_PWM_PIN_CAPABLE = 0, Power-on default = 01 Bit 2 = BACKLIGHT_FREQ_PWM_PIN_PASS-THRU_ENABLE When BACKLIGHT_BRIGHTNESS_CONTROL_MODE = 00, Source sets to 1 to enable the display backlight frequency to be controlled by BL_PWM_DIM pin. Does not apply when BACKLIGHT_BRIGHTNESS_CONTROL_MODE is = 01, 10, or 11. Writes ignored when BACKLIGHT_FREQ_PWM_PASS-THRU_CAPABLE = 0 (register 00702h), or when EDP_BACKLIGHT_FREQ_AUX_SET_ENABLE = 1. Power-on default value = 0 (Backlight frequency set either by panel default value or by EDP_BACKLIGHT_FREQ_SET, register 00728h, enabled by bit 3 below). Bit 3 = BACKLIGHT_FREQ_AUX_SET_ENABLE Source set to 1 to control backlight frequency with EDP_BACKLIGHT_FREQ_SET (register 00728h). Over-rides BACKLIGHT_FREQ_PWM_PIN_PASS-THRU_ENABLE. Writes ignored when BACKLIGHT_FREQ_AUX_SET_CAPABLE = 0 (register 00702h) Power-on default value = 0 (Backlight frequency uses panel pre-set value) Bit 4 = DYNAMIC_BACKLIGHT_ENABLE Source sets to 1 to enable dynamic backlight feature in Sink. Backlight brightness range is set by the EDP_DBC_MINIMUM_BRIGHTNESS_SET and EDP_DBC_MAXIMUM_BRIGHTNESS_SET registers (registers 00732h and 00733h). Writes ignored if DYNAMIC_BACKLIGHT_CAPABLE = 0 (register 00702h). Power-on default value = 0 (no dynamic backlight enabled). Bits 7:5 = RESERVED. Read all 0s	
00722h	EDP_BACKLIGHT_BRIGHTNESS_MSB Bits 7:0 = Display backlight brightness control, most significant bits. Applies when BACKLIGHT_BRIGHTNESS_CONTROL MODE = 10 or 11 (register 00721h). When BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 1 (register 00702h), this register provides the most significant 8 bits out of 16 possible bits that can be assigned for setting the display backlight brightness level.	Read/Write

DisplayPort Address	Definition	Read/Write over AUX Channel
	When BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 0, this register provides up to 8 bits for setting the display backlight brightness level. The actual number of assigned bits for the backlight brightness PWM generator is set by bits 4:0 of EDP_PWMGEN_BIT_COUNT (register 00724h). If bits 4:0 of EDP_PWMGEN_BIT_COUNT represent a value of more than 8 and BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 0, then only the 8 MSB bits of the brightness control value can be controlled. Note 1 below applies. Assigned bits are allocated to the MSB bits of the enabled register combination. Writes ignored if BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE = 0, (register 00702h), or if BACKLIGHT_ENABLE = 0 (register 00721h), or if TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 0 (register 00701h) Note: The quantity of assigned or controllable bits will have the ability to provide full brightness control. Examples: For 10 bit operation 00h = 0% brightness, and 3FFh = 100% brightness For 8 bit operation, 00h = 0% brightness, and FFh = 100% brightness	
00723h	EDP_BACKLIGHT_BRIGHTNESS_LSB Bits 7:0 = Display backlight brightness control, least significant bits. When BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 1 (register 00702h), this register provides the least significant 8 bits (out of 16 possible bits) that can be assigned for setting the display backlight brightness level. Refer to register 00722h for more information. Writes ignored if BACKLIGHT_BRIGHTNESS_BYTE_COUNT = 0 (register 00702h) BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE = 0 (register 00702h), or if BACKLIGHT_ENABLE = 0 (register 00721h), or if TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 0 (register 00701h)	Read/Write
00724h	EDP_PWMGEN_BIT_COUNT Bits 4:0 are used to program the number of active control bits for EDP_BACKLIGHT_BRIGHTNESS_MSB/LSB. If the value of bits 4:0 is less than bits 4:0 of EDP_PWMGEN_BIT_COUNT_CAP_MIN (register 00725h), the value of that register will apply. If the value of bits 4:0 is more than bits 4:0 of EDP_PWMGEN_BIT_COUNT_CAP_MAX (register 00726h), the value of that register will apply. Bits 7:5 = RESERVED. Read all 0s.	Read/Write
00725h	EDP_PWMGEN_BIT_COUNT_CAP_MIN Bits 4:0 = the minimum allowed value for bits 4:0 of EDP_PWMGEN_BIT_COUNT (register 00724h). This value is set by the Sink and must have a value of 1 or greater. Bits 7:5 = RESERVED. Read all 0s.	Read Only

DisplayPort Address	Definition	Read/Write over AUX Channel
00726h	EDP_PWMGEN_BIT_COUNT_CAP_MAX Bits 4:0 = the maximum allowed value for bits 4:0 of EDP_PWMGEN_BIT_COUNT (register 00724h). This value is set by the Sink and must have a value greater than or equal to EDP_PWMGEN_BIT_COUNT_CAP_MIN. Bits 7:5 = RESERVED. Read all 0s	Read Only
00727h	EDP_BACKLIGHT_CONTROL_STATUS Bit 0 = Fault condition A setting of 1 indicates a backlight fault condition that prevents proper operation of the backlight. The exact nature of the fault condition is implementation specific. Once this bit is set to 1, it may remain 1 until the panel is power cycled through the removal and reapplication of panel power (LCD_VCC and BL_PWR). An IRQ_HPD is not generated by a backlight fault condition. A setting of 0 indicates normal operation Bits 7:1 = RESERVED. Read all 0s	Read Only
00728h	EDP_BACKLIGHT_FREQ_SET Bit 7:0 = Display backlight PWM frequency control value. Refer to document Section 3.9 for more information. Backlight PWM frequency = $(27 \text{ MHz}) / (F * P)$ Where F = The PWM Frequency Pre-Divider value set by bits 7:0 Where $P = 2^{P_n}$, where P_n is the value set by Bits 4:0 of EDP_PWMGEN_BIT_COUNT (Register 00724h) (F * P) represents total divider value for the backlight frequency generator The (F * P) minimum value is defined by the 18 bit value defined by this set of registers: Bits 7:0 of EDP_BACKLIGHT_FREQ_CAP_MIN_MSB (Register 0072Ah) Bits 7:0 of EDP_BACKLIGHT_FREQ_CAP_MIN_MID (Register 0072Bh) Bits 1:0 of EDP_BACKLIGHT_FREQ_CAP_MIN_LSB (Register 0072Ch) If the value of (F * P) is less than the minimum value defined by EDP_BACKLIGHT_FREQ_CAP_MIN_MSB/MID/LSB, then the value of EDP_BACKLIGHT_FREQ_CAP_MIN_MSB/MID/LSB will apply. The (F * P) maximum value is defined by the 18 bit value defined by this set of registers: Bits 7:0 of EDP_BACKLIGHT_FREQ_CAP_MAX_MSB (Register 0072Dh) Bits 7:0 of EDP_BACKLIGHT_FREQ_CAP_MAX_MID (Register	Read/Write

DisplayPort Address	Definition	Read/Write over AUX Channel
	0072Eh) Bits 1:0 of EDP_BACKLIGHT_FREQ_CAP_MAX_LSB (Register 0072Fh) If the value of (F * P) is more than the maximum value defined by EDP_BACKLIGHT_FREQ_CAP_MAX_MSB/MID/LSB, then the value of EDP_BACKLIGHT_FREQ_CAP_MAX_MSB/MID/LSB will apply. Writes ignored if BACKLIGHT_FREQ_AUX_SET_CAPABLE = 0 (register 00702h), or BACKLIGHT_FREQ_AUX_SET_ENABLE = 0 (register 00721h), or TCON_BACKLIGHT_ADJUSTMENT_CAPABLE = 0 (register 00701h)	
00729h	RESERVED	
0072Ah	EDP_BACKLIGHT_FREQ_CAP_MIN_MSB Bit 7:0 = Most significant bits (bits 17-10) of minimum value allowed for (F * P) as defined in register 00728h. When BACKLIGHT_FREQ_SET_CAPABLE = 0, this register has no meaning.	Read
0072Bh	EDP_BACKLIGHT_FREQ_CAP_MIN_MID Bit 7:0 = Middle bits (bits 9-2) of minimum value allowed for (F * P) as defined in register 00728h. When BACKLIGHT_FREQ_SET_CAPABLE = 0, this register has no meaning.	Read
0072Ch	EDP_BACKLIGHT_FREQ_CAP_MIN_LSB Bit 1:0 = Least significant bits (bits 1-0) of minimum value allowed for (F * P) as defined in register 00728h. The value of the 18 bit number defined by EDP_BACKLIGHT_FREQ_CAP_MIN_MSB/MID/LSB must be 1 or greater. When BACKLIGHT_FREQ_SET_CAPABLE = 0, this register has no meaning. Bits 7:2 = RESERVED. Read all 0s	Read
0072Dh	EDP_BACKLIGHT_FREQ_CAP_MAX_MSB Bit 7:0 = Most significant bits (bits 17-10) of maximum value allowed for (F * P) as defined in register 00728h. When BACKLIGHT_FREQ_SET_CAPABLE = 0, this register has no meaning.	Read
0072Eh	EDP_BACKLIGHT_FREQ_CAP_MAX_MID Bit 7:0 = Middle bits (bits 2-9) of maximum value allowed for (F * P) as defined in register 00728h. When BACKLIGHT_FREQ_SET_CAPABLE = 0, this register has no meaning.	Read
0072Fh	EDP_BACKLIGHT_FREQ_CAP_MAX_LSB Bit 1:0 = Least significant bits (bits 1-0) of maximum value allowed for (F * P) as defined in register 00728h. The value of the 18 bit number defined by EDP_BACKLIGHT_FREQ_CAP_MAX_MSB/MID/LSB must be greater than or equal to the 18 bit number defined by EDP_BACKLIGHT_FREQ_CAP_MIN_MSB/MID/LSB. When BACKLIGHT_FREQ_SET_CAPABLE = 0, this register has no meaning. Bits 7:2 = RESERVED. Read all 0s	Read
00730h-00731h	RESERVED	

DisplayPort Address	Definition	Read/Write over AUX Channel
00732h	EDP_DBC_MINIMUM_BRIGHTNESS_SET Bits 4:0 = the minimum backlight brightness level when DYNAMIC_BACKLIGHT_ENABLE = 1 (register 00721h). The minimum brightness is expressed as the percentage of normal brightness established by BACKLIGHT_BRIGHTNESS_CONTROL_MODE (register 00721h). The percentage value = (bits 4:0) x 5% (up to 100% maximum) Example: Bits 4:0 = 00100, percentage value is 20%. Bits 7:5 = RESERVED. Read all 0s	Read/Write
00733h	EDP_DBC_MAXIMUM_BRIGHTNESS_SET Bits 4:0 = the maximum backlight brightness level when DYNAMIC_BACKLIGHT_ENABLE = 1 (register 00721h). The maximum brightness is expressed as the percentage of normal brightness established by BACKLIGHT_BRIGHTNESS_CONTROL_MODE (register 00721h). The percentage value = (bits 4:0) x 5% (up to 100% maximum) Example: Bits 4:0 = 10100, percentage value is 100%. EDP_DBC_MINIMUM_BRIGHTNESS_SET must be less than or equal to EDP_DBC_MAXIMUM_BRIGHTNESS_SET Bits 7:5 = RESERVED. Read all 0s	Read/Write
00734h-007FF	RESERVED for future use	Read all 0s

In order to support the optional Panel Self Refresh feature, DPCD registers have been assigned for capability, configuration and status. These registers reside within existing DP 1.2 register address space and do not reside within the address space reserved exclusively for eDP. Tables 3-6 through 3-8 provide a definition of these registers.

Table 3-6: DPCD – Sink PSR Capability Field

DisplayPort Address	Definition	Read/Write over AUX Channel
00070h	PANEL SELF REFRESH CAPABILITY SUPPORTED AND VERSION Bits 7:0 = PSR support and version 00h = Panel Self Refresh Capability not supported: Default. 01h = Panel Self Refresh Capability supported and PSR version is 01h The PSR DPCD registers defined in this section and the PSR function described in section 4 are supported. If PSR is supported, the SET_POWER_CAPABLE bit (bit 7 of DPCD register 00701h) must be set to 1. All other values are reserved for future versions of PSR	Read/Write Receiver, Read Only Source
00071h	PANEL SELF REFRESH CAPABILITIES Bit 0 = Link training requirement of Sink on PSR exit when Main Link is off. 0: Needs training on PSR exit when Main Link is off. Default. 1: No link training is needed on PSR exit when Main Link is off. The Sink must be able to lock within 5 Idle Patterns after the Main Link is turned on. Bits 3:1 = PSR Setup time. The Source must allow a time period greater than or equal to the value specified in this field between an SDP indicating PSR entry and the start of the active frame to be captured in the RFB. The Sink must be capable of decoding the SDP, powering up PSR related resources, and start capturing a static frame, including any implementation dependent timing margins, within the specified setup time in this field. By default, this field is set to 330µs. 0h = 330µs. Default. 1h = 275µs 2h = 220µs 3h = 165µs 4h = 110µs 5h = 55µs 6h = 0µs 7h = RESERVED Bits 7:4 = RESERVED. Read all 0s	Read/Write Receiver Read Only Source

Table 3-7: DPCD – Sink PSR Configuration Field

DisplayPort Address	Definition	Read/Write over AUX Channel
00170h	PANEL SELF REFRESH ENABLE AND CONFIGURATION Bit 0 = Source Enables Self Refresh Feature in Sink 0 = Disable. Default. 1 = Enable. The Sink will honor the PSR fields of the Video Stream Configuration (VSC) packet. Setting this bit does not automatically force the Sink into PSR active mode. PANEL SELF REFRESH CONFIGURATION Bit 1 = Source transmitter state in PSR active 0 = The Source may shut down the Main Link transmitters after BS of 9th line after the end of the static frame transmitted to the Sink with entry into PSR active. Default. 1 = The Main Link transmitters remain active during PSR active Bit 2 = CRC verification in PSR active 0 = CRC verification performed by the Source. The Sink must calculate CRC but is not required to compare. The Source will not send CRCs to the Sink. Default. 1 = The Sink must perform CRC verification. Bit 3 = Frame capture indication 0 = The Sink must capture the first active frame after the PSR entry indication. Default. 1 = The Sink must capture the second active frame after PSR entry indication. The Sink may use the additional time for powering up the RFB. Bits 7:4 = RESERVED. Read all 0s	Read/Write Source Read only for Receiver

Table 3-8: DPCD – Sink PSR Status Field

DisplayPort Address	Definition	Read/Write over AUX Channel
2006h	ERROR STATUS If either bit 0 or bit 1 is set to 1 by the Sink, the Sink generates an IRQ_HPD. Bit 0 = LINK CRC ERROR. Sticky bit. Write 1 clears register bit. 0 = No CRC error 1 = CRC mismatch or CRC not received from Source Bit 1 = RFB STORAGE ERROR. Sticky bit. Write 1 clears register bit. 0 = No internal error 1 = Internal Error Bits 7:2 = RESERVED. Read all 0s	Read/Write Source Write 1 clears Read/Write for Sink
2007h	PSR EVENT STATUS INDICATOR (PSR ESI) Bit 0 = SINK PSR CAPABILITY CHANGE. Sticky bit. Write 1 clears register bit. 0 = No PSR capability change. 1 = Sink requested PSR capability change. Bits 7:1 = RESERVED. Read all 0s	Read/Write Source Write 1 clears Read/Write for Sink

DisplayPort Address	Definition	Read/Write over AUX Channel
2008h	SINK PANEL SELF REFRESH STATUS Bits 2:0 = SINK SELF REFRESH STATUS 0h = PSR_State 0: Sink PSR inactive state. Default. 1h = PSR_State 1: Sink PSR active capture and display on Source timing 2h = PSR_State 2: Sink PSR active display from RFB 3h = PSR_State 3: Sink PSR active Capture and display on Sink timing 4h = PSR_State 4: Sink PSR active Capture and display, timing resync 5h = Reserved 6h = Reserved 7h = SINK INTERNAL ERROR. The Sink must generate an IRQ_HPD and must report “7” until the Source disables the PSR function. Bits 7:3 = RESERVED. Read all 0s	Read Only Source Read/Write for Sink

DisplayPort Address	Definition	Read/Write over AUX Channel
2009h	DEBUG REGISTER 0 SYNCHRONIZATION LATENCY IN SINK Number of frames upon PSR exit required for the Sink to synchronize to Source provided timing. Bits 3:0 = Maximum number of frames needed by the Sink for synchronizing to Source timing. This is static value field. 0h = Sink will synchronize by the first frame received after PSR exit. 1h = Sink will synchronize by the second frame received after PSR exit. 2h = Sink will synchronize by the third frame received after PSR exit. 3h = Sink will synchronize by the fourth frame received after PSR exit. ... 7h = Sink will synchronize by the eighth frame received after PSR exit. 8h = Maximum number of frames for Sink to synchronize is more than 8 frames. All other values for this field are reserved. LAST ACTUAL SYNCHRONIZATION LATENCY IN SINK Bits 7:4 = Number of frames that the Sink took to synchronize to Source timing on the last PSR exit. This field has to be updated before entering PSR_State 0. It is the number of frames measured between the PSR exit event received in the Sink and the Sink is completely synchronized to the Source timing. 0h = Sink has synchronized to the first frame received after PSR exit. 1h = Sink has synchronized to the second frame received after PSR exit. 2h = Sink has synchronized to the third frame received after PSR exit. 3h = Sink has synchronized to the fourth frame received after PSR exit. ... 7h = Sink has synchronized to the eighth frame received after PSR exit. 8h = Sink took more than 8 frames to synchronize. All other values for this field are reserved. This register provides information about the Sink PSR operation and a Source is not required to use this register.	Read Only Source Read/Write for Sink

DisplayPort Address	Definition	Read/Write over AUX Channel
200Ah	DEBUG REGISTER 1 LAST RECEIVED PSR SDP Bits 2:0 = Content of the last received PSR SDP DB1 field. Bit 0 = PSR State bit. Current value of the PSR state bit in the Sink. Bit 1 = Update RFB bit. Current value of the Update RFB bit in the Sink. Bit 2 = CRC Valid bit. Current value of the CRC Valid bit in the Sink. Bits 7:3 = RESERVED. Read all 0s This register provides information about the Sink PSR operation and a Source is not required to use this register.	Read Only Source Read/Write for Sink

3.5 PSR Secondary Data Packet Support

This section defines the secondary data packet format required to support Panel Self Refresh. Panel Self Refresh requirements are defined in Section 4.

A Source device indicates PSR entry/exit by in-band signaling using a Video Stream Configuration (VSC) secondary data packet.

- Table 3-9 defines the VSC packet with PSR feature support
- Table 3-10 defines changes in the packet header bytes related to the addition of PSR signaling
- Tables 3-11 through 3-14 define bit definitions of the VSC packet data payload

Table 3-9: Video Stream Configuration Packet

	7	6	5	4	3	2	1	0
HB0	Secondary Data Packet ID							
HB1	Secondary Data Packet Type							
HB2	Reserved = 0				Revision			
HB3	Reserved = 0				Number of Valid Payload Bytes			

DB0	Stereo Interface Method Specific Parameter				Stereo Interface Method Code			
DB1	PSR							
DB3 - DB2	CRC Value R or Cr component							
DB5 – DB4	CRC Value G or Y component							
DB7 – DB6	CRC Value B or Cb component							
DB31 – DB8	Reserved = 0							

Table 3-10: Video Stream Configuration Packet Header

Byte #	Content
HB0	Secondary Data Packet ID = 0
HB1	Secondary Data Packet Type = 07h
HB2	Bits 4:0 = Revision Number = 02h Bits 7:5 = RESERVED. Read all 0s
HB3	Bits 4:0 = Number of Valid Data Bytes = 08h Bits 7:5 = RESERVED. Read all 0s

Table 3-11: Video Stream Configuration Packet DB1

Byte #	Detailed Bit Definitions
DB1	Bit 0 = PSR State 0 = PSR Inactive (normal operation mode) 1 = PSR Active (indication to enter PSR)
	Bit 1 = Update RFB (If PSR State bit received in the previous VSC SDP is 0 or if PSR State in this VSC SDP is 0, ignore this bit) 0 = Do not update RFB. 1 = Update RFB: capture incoming frame into the RFB.
	Bit 2 = CRC Valid 0 = CRC values in DB7:2 are invalid 1 = CRC values in DB7:2 are valid
	Bits 7:3 = RESERVED. Read all 0s

Table 3-12: Video Stream Configuration Packet DB2-3

Byte #	Detailed Bit Definitions
DB2	Bits 7:0 = CRC value bits 7:0 of the R or Cr component
DB3	Bits 7:0 = CRC value bits 15:8 of the R or Cr component

Table 3-13: Video Stream Configuration Packet DB4-5

Byte #	Detailed Bit Definitions
DB4	Bits 7:0 = CRC value bits 7:0 of the G or Y component
DB5	Bits 7:0 = CRC value bits 15:8 of the G or Y component

Table 3-14: Video Stream Configuration Packet DB6-7

Byte #	Detailed Bit Definitions
DB6	Bits 7:0 = CRC value bits 7:0 of the B or Cb component
DB7	Bits 7:0 = CRC value bits 15:8 of the B or Cb component

3.6 Support for Display Authentication and Content Protection

Implementations of certain content protection schemes such as CSS, AACS and others require a trusted platform mechanism when outputting protected video content to an integrated display. Unless HDCP is

used for protecting content sent to the integrated display, which is not a usual system implementation, a mechanism must be employed to assure the protected content is being sent to the integrated display rather than to a non-HDCP external display or other Sink device. eDP can meet these mechanism requirements using any one of the alternatives listed in Table 3-15.

Table 3-15: Optional eDP Display Authentication and Content Protection Methods

eDP Display Authentication Method	eDP Display Authentication Method Approach
Method 1	Use HDCP for protecting content to an eDP panel. The Source and eDP Sink must have the capability to support HDCP to use this method. Similar to a typical non-eDP external DisplayPort Sink device, this method makes use of HDCP as a content protection mechanism over the eDP link. HDCP would typically be invoked by a content protection flag, as is typical for content protection implementations. Support of method 1 is normally not expected in an eDP Sink device.
Method 2	Ensure Source device can reliably determine and report usage of an internal connection to an eDP panel. Implementation of this method must ensure that the GPU or graphics driver can reliably determine and report that a given DisplayPort Source port is connected to an internal eDP Sink only. An example approach would be to use a dedicated video port and/or certain fixed GPU hardware features disabling the use of non-eDP Sinks. Support of method 2 is system implementation-specific.
Method 3a	Use an Alternative Scrambler Seed Reset (ASSR) for eDP panel communications. The Source and eDP Sink must have the capability to support ASSR to use this method. eDP panels report ASSR support capability through use of bit 4 in DPCD register 0000Dh (refer to the DisplayPort Standard). The Source enables the ASSR mode in the Sink by setting bit 0 of DPCD register 0010Ah (eDP_CONFIGURATION_SET) to 1. Non-eDP Sink devices (such as external Sink devices) must not support nor indicate support of this capability. When this method is used for display authentication, it can be enabled and disabled at any time by the Source writing into the eDP_CONFIGURATION_SET DPCD register. Upon changing the ASSR state, the Sink should wait for 5 SR patterns in the attempt to resynchronize to the Source's scrambler before triggering a link failure event. Since display noise may occur during re-synchronization, the Source must conceal such possible display noise by forcing Black Video during the ASSR state change using the BLACK_VIDEO_ENABLE bit (Bit 1 of DPCD register 00720h as listed in Table 3-5). In operation, the SR symbol resets the LFSRs in the Source and Sink to FFFEh, in place of the normal FFFFh value that is used on non-eDP (such as external) DisplayPort Sinks. Support of method 3a is recommended for eDP Sink devices.
Method 3b	Use Alternate Framing for eDP panel communications. The Source and eDP Sink must have the capability to support Alternate Framing to use this method. eDP panels report Alternate Framing support capability through use of bit 1 in DPCD register 0000Dh (refer to the DisplayPort Standard). The Source

eDP Display Authentication Method	eDP Display Authentication Method Approach
	enables the Alternate Framing mode in the Sink by setting bit 1 of DPCD register 0010Ah to 1. Non-eDP Sink devices (such as external Sink devices) must not support nor indicate support of this capability. When this method is used for display authentication, it is normally enabled upon link training and continues to be used until the display is powered off. When enabled, the eDP Sink must operate only in Enhanced Framing Mode. The Source must send only Enhanced Framing on the main link, and must only write a '0' to DPCD 00101h: LANE_COUNT_SET Bit 7: ENHANCED_FRAME_EN bit. Support of method 3b is recommended for eDP Sink devices.

Methods 3a and 3b in Table 3-15 are optional eDP features as described in DP v1.2. The capability of the eDP Sink to support these features, as well as the capability of the Source to enable them, is communicated through the Sink DPCD registers described in Table 3-4.

eDP display authentication methods 3a and 3b must not be enabled in non-embedded displays which includes external displays and other external Sink devices. This assures that video and audio content are deliverable to embedded displays only when these methods are used for display authentication. The specifics of how non-interoperability with external devices is achieved with these methods is beyond the scope of this standard.

Implementation of any one or more of these methods is optional for eDP devices. As with other eDP device features, the system integrator is responsible for ensuring interoperability between the eDP Source and eDP Sink chosen for a particular application.

It is recommended that eDP panels incorporate methods 3a and 3b to accommodate a variety of embedded Source device types. A given eDP panel product model may be used with a variety of Source types taking into account the manufacturing test requirements and GPU options available in a typical notebook PC. It is possible that a given eDP panel may be subjected to a diversity of Source device types over its life cycle as shown in the example of Figure 3-2.

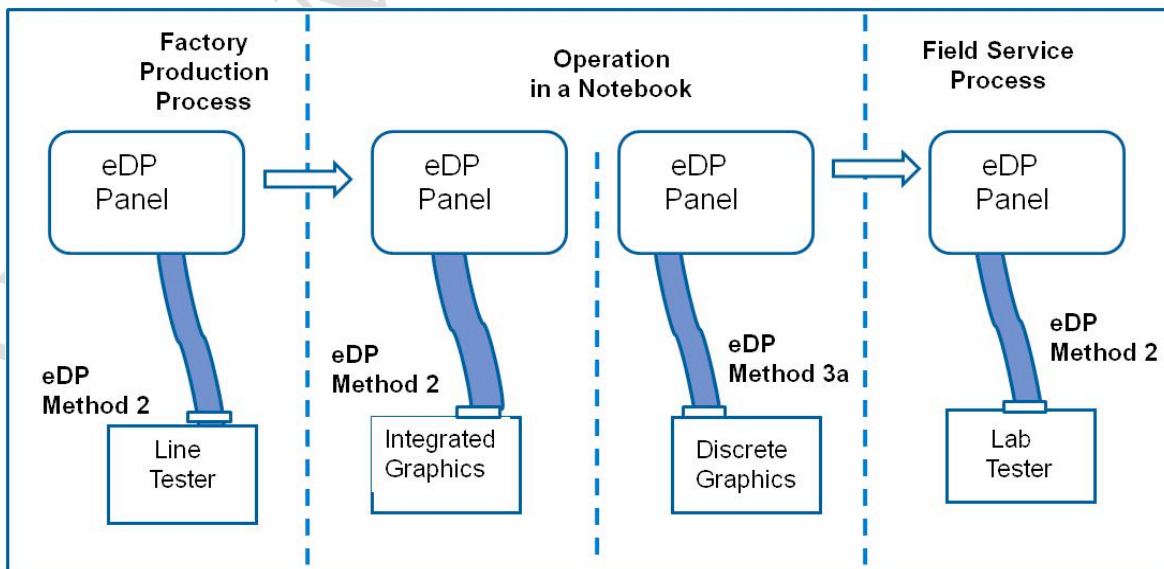


Figure 3-2: Example of a Single eDP Panel Supporting Multiple Source Display Authentication Methods

Figure 3-3 illustrates an example of eDP panel operation with Source devices that may be used in factory production line testing.

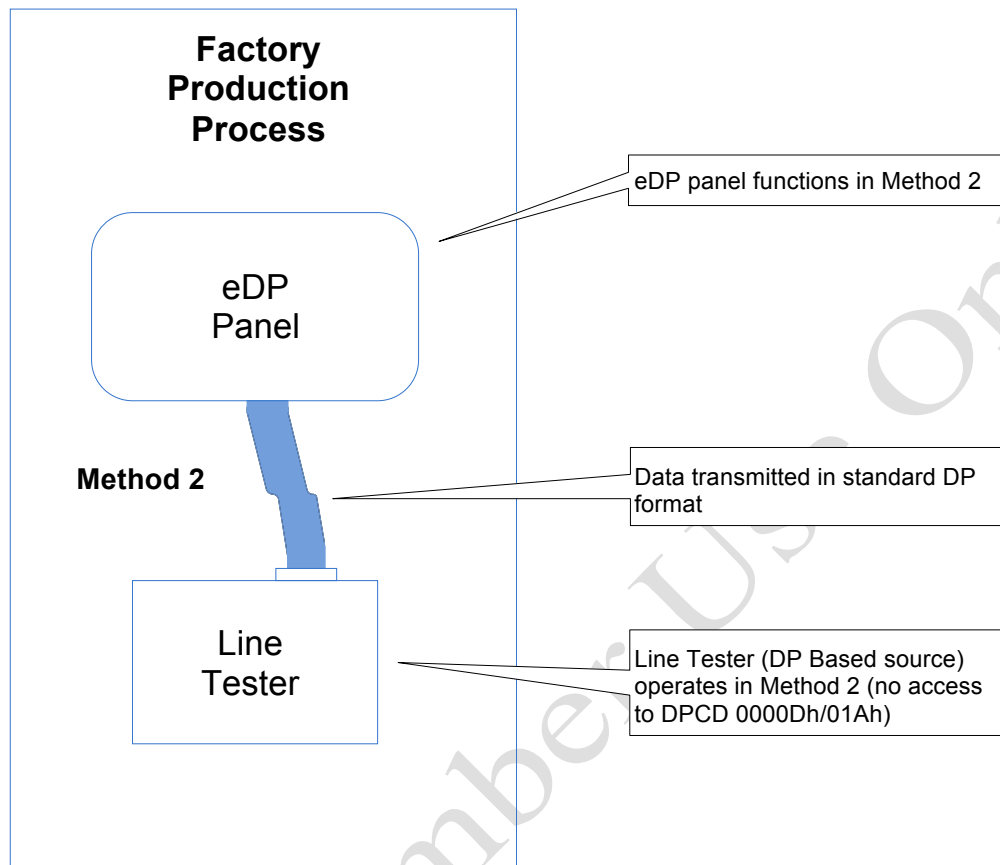


Figure 3-3: eDP Panel Factory Production Process Operational Example

Figure 3-4 illustrates eDP operation in a notebook PC scenario where a variety of chipsets, processors, or GPUs may be encountered.

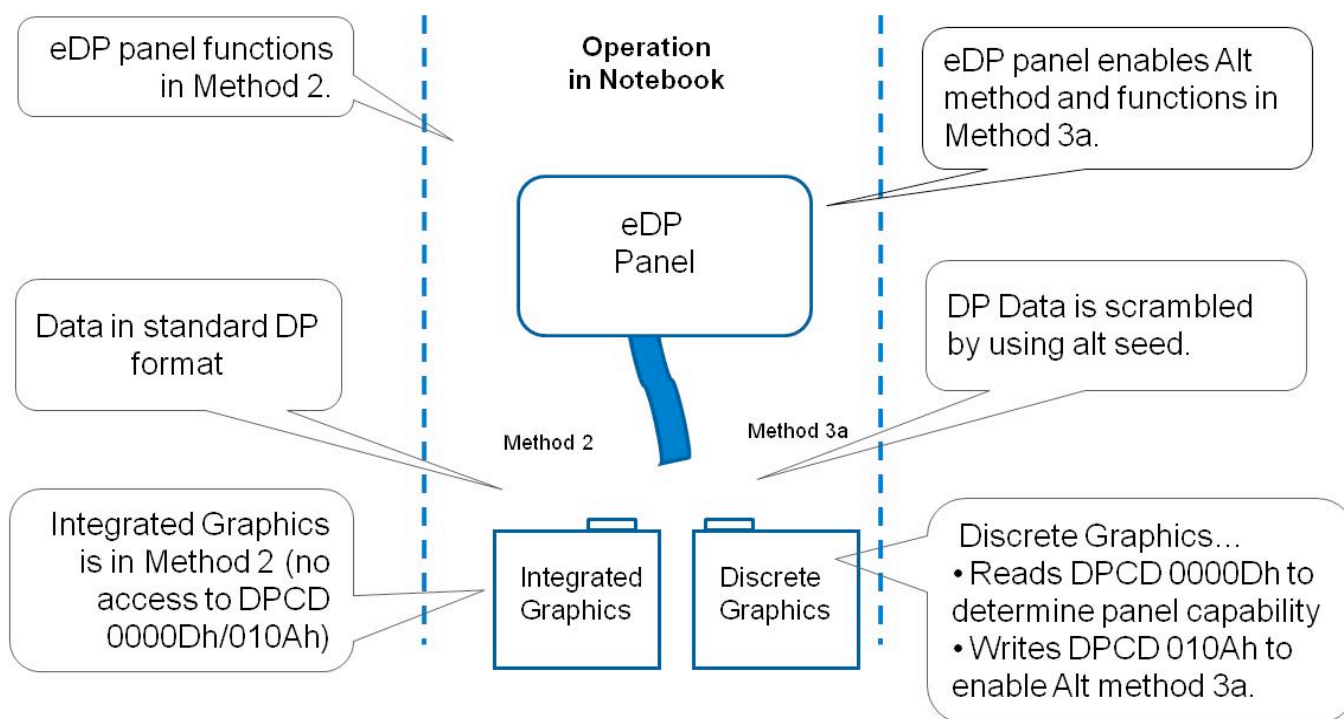


Figure 3-4: eDP Panel Embedded in Notebook PC Operational Example

Figure 3-5 illustrates eDP operation in a field service scenario where an eDP panel may need to be removed from a notebook for testing in lab environment with test equipment.

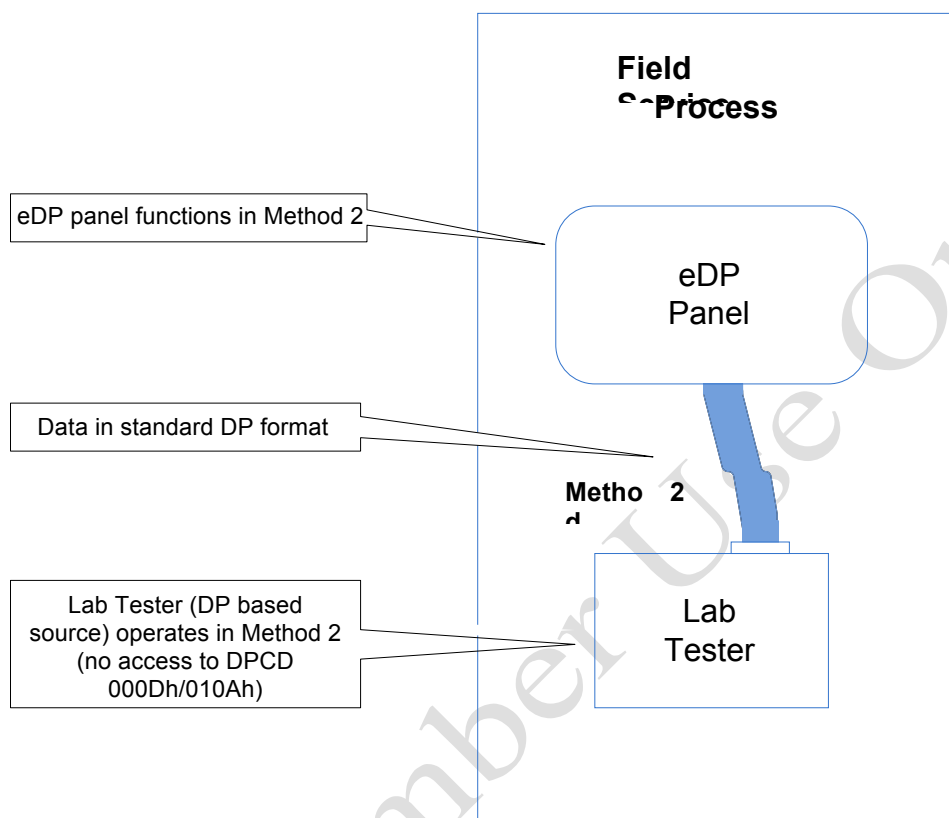


Figure 3-5: eDP Panel Field Service Process Operational Example

With regard to methods 3a and 3b, the Source will typically read the Sink's capability registers and then enable the preferred method during the link training sequence as illustrated in Figures 3-6 and Table 3-16 below.

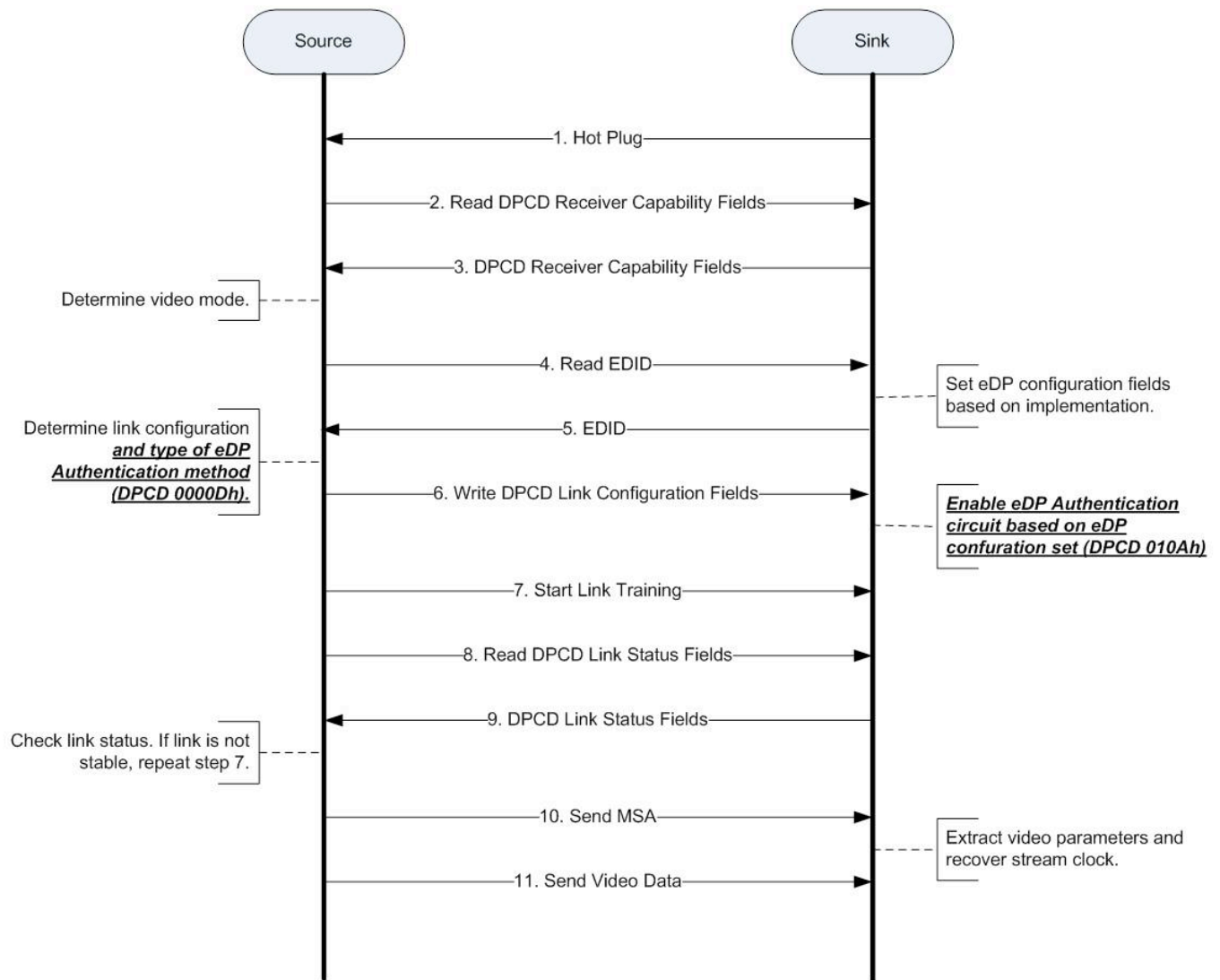


Figure 3-6: Method 3a or 3b Identification and Control During Link Training Process

Table 3-16: Expanded Description of Figure 3-6

Process Step	Source and Sink Behavior Action
1	Upon power-on Sink generates a hot plug detection pulse thru HPD
2	Source determines video mode by reading DPCD receiver capability field (DPCD 00000h to 0000Dh) <i>including eDP CP capability register (DPCD 0000Dh)</i>
3	Sink replies DPCD receiver capability field.
4	Source starts EDID read thru I ² C-over-AUX
5	Sink replies EDID thru I ² C-over-AUX
6	Source determines link configuration, such as MAX_LINK_RATE and MAX_LANE_COUNT. <i>Source also determines which type of eDP Authentication method to use and writes DPCD link configuration field (DPCD 00100h to 0010Ah) including eDP configuration set (DPCD 0010Ah).</i>
7	Source starts link training. Sink does clock recovery and equalization
8	Source reads DPCD link status field (DPCD 00200h to 0020Bh)
9	Sink replies DPCD link status field. If main link is not stable, Source repeats Step 7.
10	Source sends MSA (Main Stream Attribute) data. Sink extracts video parameters and recovers stream clock.
11	Source sends video data

3.7 Panel Input Power (LCDVCC)

It is recommended that the power supplied to the eDP/TCON device (LCDVCC) uses a single power rail. Any additional power rails should use the same power sequence and timing as defined for LCDVCC in Section 5 (Power Sequencing). All eDP functions including the Main Link and AUX Channel should be powered by LCDVCC. To read DPCD or EDID, the Source device must turn on LCDVCC.

3.8 Main Stream Attribute Data

The Source must be capable of correctly generating all of the MSA fields, and the Sink must be capable of correctly reading all MSA fields. However, to support particular video formats from the Source, the Sink can implement the option to ignore the set of MSA Timing Parameter listed in Table 3-17 below. The Sink must be able to indicate this capability through the means described in Table 3-18.

Table 3-17: Set of MSA Timing Parameters That May Be Ignored

HTotal[15:0]	HStart[15:0]	HSyncPolarity (HSP)	HSyncWidth[14:0] (HSW)
VTotall[15:0]	VStart[15:0]	VSynCPolary (VSP)	VSynWidth[14:0] (VSW)

Table 3-18: DPCD Register Bits That Determines Use of Parameters in Table 3-17

DPCD Address	Bit Name		Read/Write over AUX Channel
	Field Type	Description	
00007h Bit 6	MSA_TIMING_PAR_IGNORED		Read Only
	Sink Capability (set by the Sink)	0 = Sink device requires the MSA timing parameters listed in Table 3-17 to be sent by the Source device for rendering the incoming video stream. 1 = Sink device is capable of rendering incoming video stream without the MSA timing parameters listed in Table 3-17.	
00107h Bit 7	MSA_TIMING_PAR_IGNORE_EN		Read/Write
	Link Configuration (set by the Source)	0 = Source device will send valid data for the MSA Timing Parameters listed in Table 3-17. (The default value of this bit is 0, therefore the Source does not need to write this bit if it does not support modes where invalid MSA Timing Parameters will be sent.) 1 = Source device may send invalid data for the MSA Timing Parameters listed in Table 3-17. Sink must ignore these parameters and be able to regenerate the incoming video stream without depending on these parameters. (This bit can be set to 1 only if the MSA_TIMING_PAR_IGNORED bit in the Sink is set to 1.)	

3.9 Display Backlight Control Using DPCD Registers

The AUX channel display control capability introduced with eDP version 1.2 includes control of the display backlight. As per Table 3-5, DPCD registers are available in address fields 00721h-00731h to control brightness and PWM frequency, when these functions are supported by the panel (backlight adjustment capability is declared in register 00702h).

Figure 3-7 below shows a conceptual panel block diagram for implementations where the eDP TCON is used for display backlight adjustment. In this example, the backlight brightness can be controlled by the EDP_BACKLIGHT_BRIGHTNESS_MSB/LSB registers (registers 00722h and 00723h) and/or the BL_PWM_DIM connector pin (Tables 6-3 and 6-4). Table 3-19 summarizes the display brightness control modes available with eDP 1.2 or higher. The capability for the Source to adjust backlight characteristics in the panel using the Sink DPCD registers is indicated by reading the TCON_BACKLIGHT_ADJUSTMENT_CAPABLE bit as 1, as indicated in Table 3-5 (register 00701h).

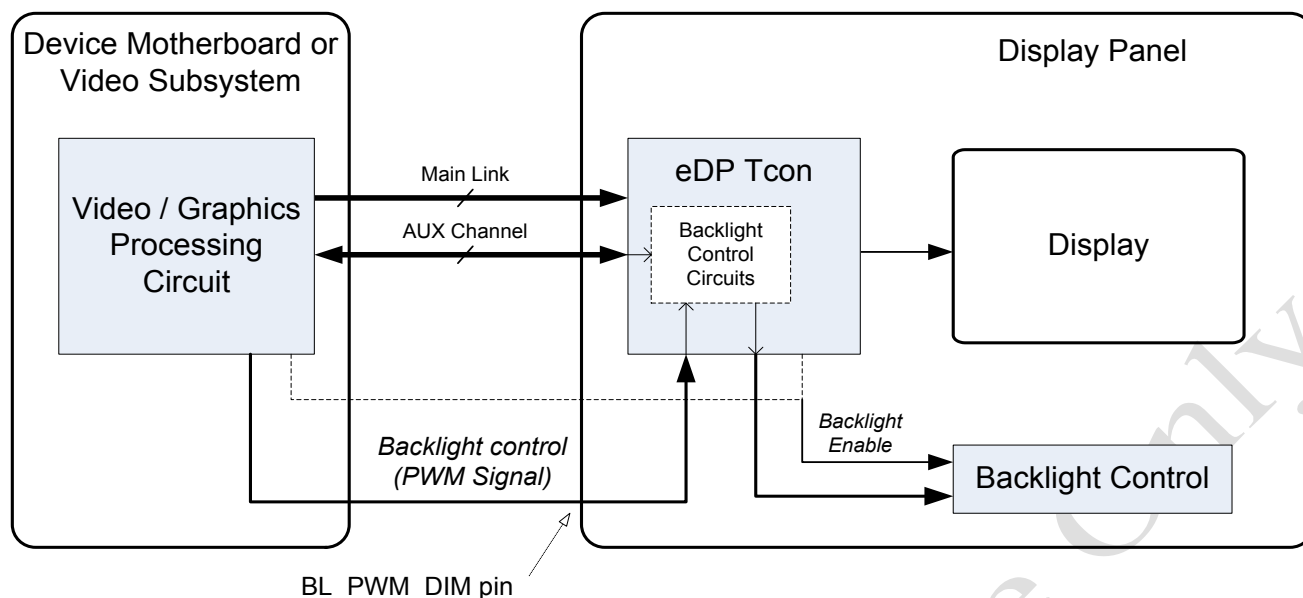


Figure 3-7: Control of Backlight via Timing Controller

Panels can also be configured for direct backlight control via the eDP connector pins, as shown in the example in Figure 3-8. This block diagram represents the typical panel configuration used for eDP 1.1 and below, and is an implementation option for eDP 1.2 or higher. For eDP 1.2 or higher panels, the TCON_BACKLIGHT_ADJUSTMENT_CAPABLE bit (register 00701h) must be cleared to 0 to indicate that the TCON is not capable of display backlight adjustment.

Both Figure 3-7 and Figure 3-8 indicate two options for Backlight Enable that controls the display backlight illumination. Backlight Enable control can originate from the eDP connector pin, or through AUX channel command. Capability for this function through the BL_ENABLE connector pin is indicated by BACKLIGHT_PIN_ENABLE_CAPABLE = 1 (register 00701h). Capability for this function through the AUX channel is indicated by BACKLIGHT_AUX_ENABLE_CAPABLE = 1 (register 00701h). When AUX capability is available, Backlight Enable is controlled by the BACKLIGHT_ENABLE bit (register 00720h). A Source sets this bit to 1 to enable (illuminate) the panel backlight. This bit does not affect other panel functions, such as the PWM logic.

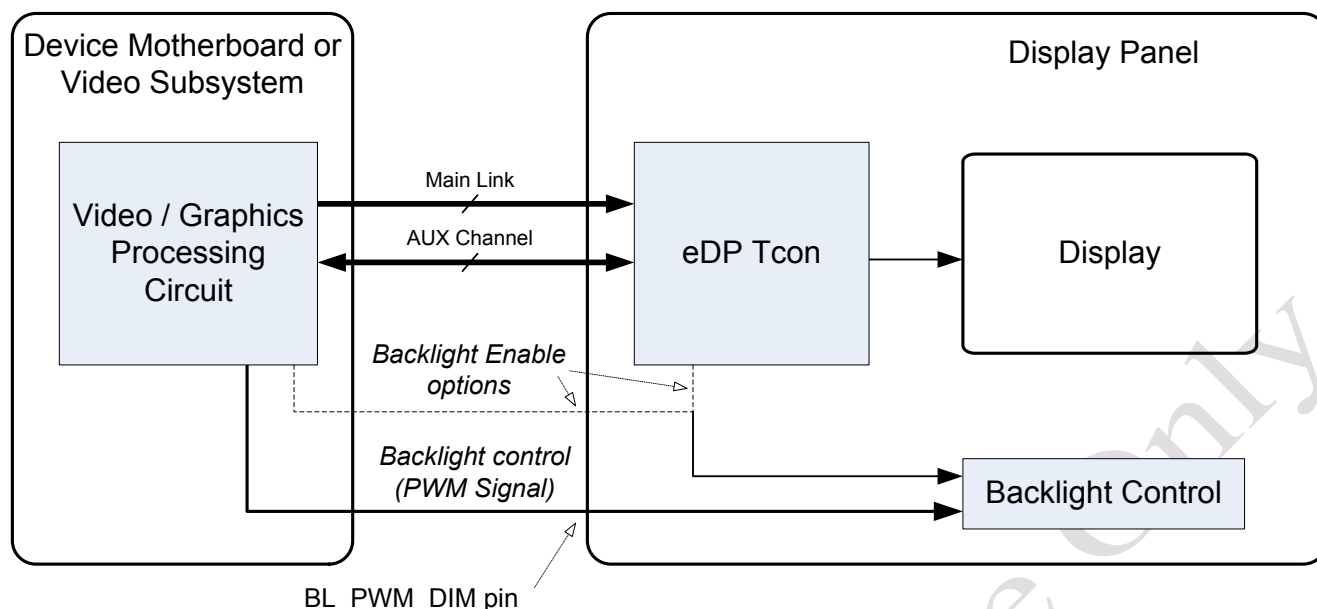


Figure 3-8: Control of Backlight via eDP Connector Interface

Table 3-19 summarizes the backlight adjustment modes that are available with eDP Version 1.2 or higher when the TCON is used for backlight adjustment (refer to Figure 3-7 above). Both backlight brightness and backlight PWM frequency control options are shown.

Note when BACKLIGHT_BRIGHTNESS_CONTROL_MODE is cleared to 00 (register 00721h, bits 1-0), the PWM input is passed through the TCON as shown in Figure 3-7, and does not bypass the TCON as shown in Figure 3-8. This means the Backlight frequency can also be modified as per the capability bits in register 00721h.

The Dynamic Backlight Control (DBC) and Color Engine modes are not listed in Table 3-19 because when they are available, they are available for any of the modes supported.

It should be noted that some panel implementations will allow the backlight brightness to be controlled by both the eDP connector PWM input (through the “BL_PWM_DIM” pin) and DPCD register(s) 00722h-00723h (see Table 3-5). This is sometimes known as the “product” function. When this capability is specified and the mode is set (see BACKLIGHT_BRIGHTNESS_CONTROL_MODE ‘11’ in Table 3-19), the backlight brightness level is the numeric product of the PWM input duty cycle and DPCD register value (registers 00722h and 00723h). So, for example, if the PWM input cycle is 50%, and the DPCD register 00722h is set to “10000000” or 80h (using 8 bit mode) which also represents a value of 50%, then the backlight brightness value will be 25%. This is determined by the equation (PWM duty cycle) * (DPCD register value) = (backlight value), or in this example $(0.5) * (0.5) = (0.25)$.

Table 3-19: Summary of Backlight Control Modes Using DPCD Registers in Table 3-5

Capability Registers in Sink (TCON)					Configuration Registers in Sink (TCON)				
Set by Sink (TCON) to indicate mode support, read by Source (GPU) R = TCON register is Read Only					Set by Source (GPU) to set contols modes Sink (TCON) R/W = TCON register is Read or Write				
R	R	R	R	R/W					
TCON_BACKLIGHT_ADJUSTMENT_CAPABLE (00701h, bit 0)	BACKLIGHT_BRIGHTNESS_PWM_PIN_CAPABLE (00702h, bit 0)	BACKLIGHT_BRIGHTNESS_AUX_SET_CAPABLE (00702h, bit 1)	BACKLIGHT_AUX-PWM_PRODUCT_CAPABLE (00702h, bit 3)	BACKLIGHT_BRIGHTNESS_CONTROL_MODE (00721h, bits 1-0)					

DC = Don't Care

The following provides an overview on how the LCD panel backlight frequency is programmed using DPCD registers listed in Table 3-5.

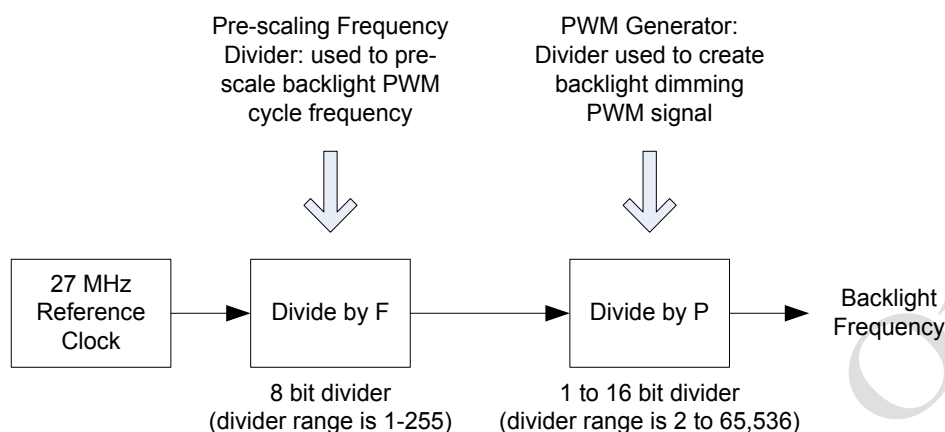


Figure 3-9: TCON Circuit Blocks the Determine Panel Backlight Frequency

Please refer to Figure 3-9. The mechanism used for backlight brightness control is the PWM (pulse width modulation) generator. For eDP v1.2 or higher, the number of bits that can be used to control the PWM generator is adjustable over a range of 1 to 16. For the purpose of simplifying this discussion, we will refer to this number of bits as the value ‘Pn’

In reference to Table 3-5:

Pn = Bits 4:0 of EDP_PWMGEN_BIT_COUNT (Register 00724h)

Min Pn = Bits 4:0 of EDP_PWMGEN_BIT_COUNT_CAP_MIN (Register 00725h)

Max Pn = Bits 4:0 of EDP_PWMGEN_BIT_COUNT_CAP_MAX (Register 00726h)

A larger Pn value (meaning more PWM generator control bits) will provide a finer backlight adjustment (increased granularity), but will also limit the maximum backlight frequency as will be described later below. The main points about setting Pn are:

- The number of dimming steps available for brightness control is 2^{Pn} . So for example, if Pn = 10, then the number of dimming steps available will be $2^{10} = 1024$.
- The divider ratio ‘P’ (referring to Figure 3-9) is also equal to 2^{Pn} . So again, if Pn = 10, the value of P will be 1024.

The Pre-scale divider shown in Figure 3-9 is used to set backlight frequency, in conjunction with the ‘P’ divider value described above. The actual backlight frequency is determined by the following equation:

$$\text{Backlight Frequency} = (27 \text{ MHz}) / (F * P)$$

Where F = the pre-scale divider ratio

P = the PWM Generator divider ratio.

The value (F * P) represents the total divider ratio that is applied to the 27MHz reference clock. The 27MHz reference clock is an internal signal for backlight PWM signal generation and is derived in an implementation specific manner.

An increase in the Pn value will decrease the maximum possible backlight frequency. Again for example, if Pn = 10, then P = 1024. The maximum backlight frequency that can be achieved is when F = 1. Therefore for this example, the maximum backlight frequency is

$$\text{Maximum Backlight Frequency} = (27 \text{ MHz}) / 1024 = 26.4 \text{ kHz.}$$

Allowing Pn to be adjustable provides the flexibility of backlight dimming granularity vs. maximum backlight frequency.

Referring back again to this definition: Backlight Frequency = (27MHz) / (F * P)

With P being fixed by the choice of Pn, the backlight frequency is then adjusted by F.

In reference to Table 3-5:

Pre-Divider value “F” is an 8 bit value defined by:

Bits 7:0 of EDP_BACKLIGHT_FREQ_SET (Register 00728h)

A given LCD panel will normally have a limited range of backlight frequency capability. To limit the programmable frequency range, limitations are placed on the allowable total divider ratio with the Sink device. The total divider ratio limits are with the Sink device expressed as follows:

The (F * P) minimum value is defined by the 18 bit value defined by this set of registers:

Bits 7:0 of EDP_BACKLIGHT_FREQ_CAP_MIN_MSB (Register 0072Ah)

Bits 7:0 of EDP_BACKLIGHT_FREQ_CAP_MIN_MID (Register 0072Bh)

Bits 1:0 of EDP_BACKLIGHT_FREQ_CAP_MIN_LSB (Register 0072Ch)

The (F * P) maximum value is defined by the 18 bit value defined by this set of registers:

Bits 7:0 of EDP_BACKLIGHT_FREQ_CAP_MAX_MSB (Register 0072Dh)

Bits 7:0 of EDP_BACKLIGHT_FREQ_CAP_MAX_MID (Register 0072Eh)

Bits 1:0 of EDP_BACKLIGHT_FREQ_CAP_MAX_LSB (Register 0072Fh)

3.10 LCD Panel Self-Test (Informative)

Many TCON devices will include an embedded LCD panel self-test mode. The self-test mode is designed to help the system integrator identify the root cause of abnormal display operation without the use of complicated debug tools. LCD video-related failure modes can usually be associated with major subsystem blocks including the GPU board, video cable/connector, and LCD components. In an eDP device, the LCD panel self-test is initiated through AUX Channel registers using OEM/ODM system diagnosis tools or via the LCD Self-Test pin on the connector.

A typical LCD test sequence consists of five sequencing color patterns during a two second interval as illustrated in Figure 3-10. Each color pattern should display the native screen size. Common color definition is shown in Table 3-20.

The self-test mode can be enabled in one of two ways:

1. If the LCD_Self_Test pin as listed in Table 6-1 through 6-4 is enabled with this function, as indicated by bit 3 in DPCD register 00701h (see Table 3-5), the self-test mode can be enabled by forcing this pin to logic level 1. If the LCD_Self_Test pin is not enabled or not used it can be left unconnected.
2. If the PANEL_SELF_TEST_AUX_ENABLE_CAPABLE bit of DPCD register 00701h is set to 1 (See Table 3-5), then the PANEL_SELF_TEST_ENABLE bit in DPCD register 0010Ah can be used to enable the self-test mode.

The use of either method (1) or (2) above will over-ride other video modes including normal video (when valid video data is received) or Black Video (which may be generated automatically when invalid video data is being received, or enabled through the BLACK_VIDEO_ENABLE bit of register 00720h listed in Table 3-5).

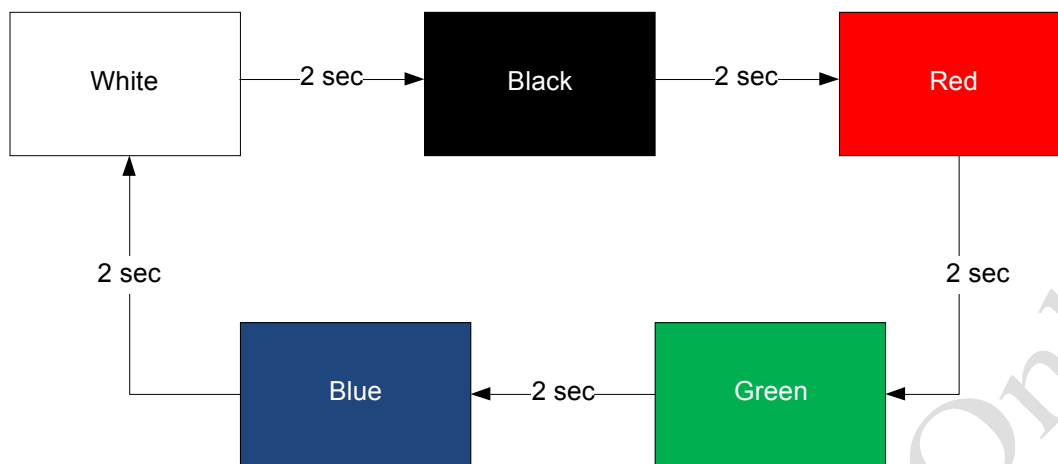


Figure 3-10: LCD Panel Self-Test Patterns

Table 3-20: LCD Self-Test Color Square Definition

Colorimetry	Dynamic Range		White Pattern	Black Pattern	Red Pattern	Green Pattern	Blue Pattern
18bpp RGB	VESA	R	63	0	63	0	0
		G	63	0	0	63	0
		B	63	0	0	0	63
24bpp RGB	VESA	R	255	0	255	0	0
		G	255	0	0	255	0
		B	255	0	0	0	255

4 Panel Self Refresh (PSR)

Panel Self Refresh (PSR) is an optional feature for both Sinks and Sources. To be implemented within a system, both Source and Sink must support PSR.

The Panel Self Refresh feature enables system-level power savings when the displayed image remains static for multiple display frames. The Sink stores a static image locally in the Remote Frame Buffer (RFB) within the Sink, and displays this image from the RFB, while the eDP Main Link may be turned off. Other Source functions may also be powered down for further power savings.

4.1 Architecture Overview

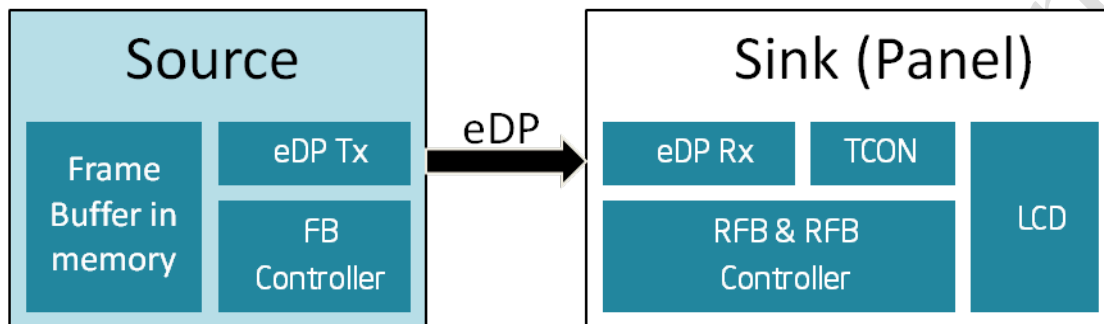


Figure 4-1: Panel Self Refresh System-level Diagram

In PSR system architecture, the eDP link and the Sink resident RFB state are considered to be independent resources. The Source is responsible for functional correctness. For example, while the Source may choose to enable the RFB for display refresh without turning the eDP Main Link off, the Source should not turn off the Main Link without first enabling the RFB for display refresh.

The terms active frame and video frame are used multiple times in this specification. Video frame as shown in Figure 4-2 constitutes vertical blank period, horizontal blank period and active pixel data. It spans from the first BS sequence of the vertical blank to the last active pixel of the last active line.

Active frame constitutes only active pixel data. It starts with the first pixel after the first BE at the end of the vertical blank period and continues to the last active pixel of the last active line excluding the horizontal blank period of each horizontal line. Horizontal blank period starts from the BS sequence and ends with BE, and includes the BS sequence and BE of each horizontal line.

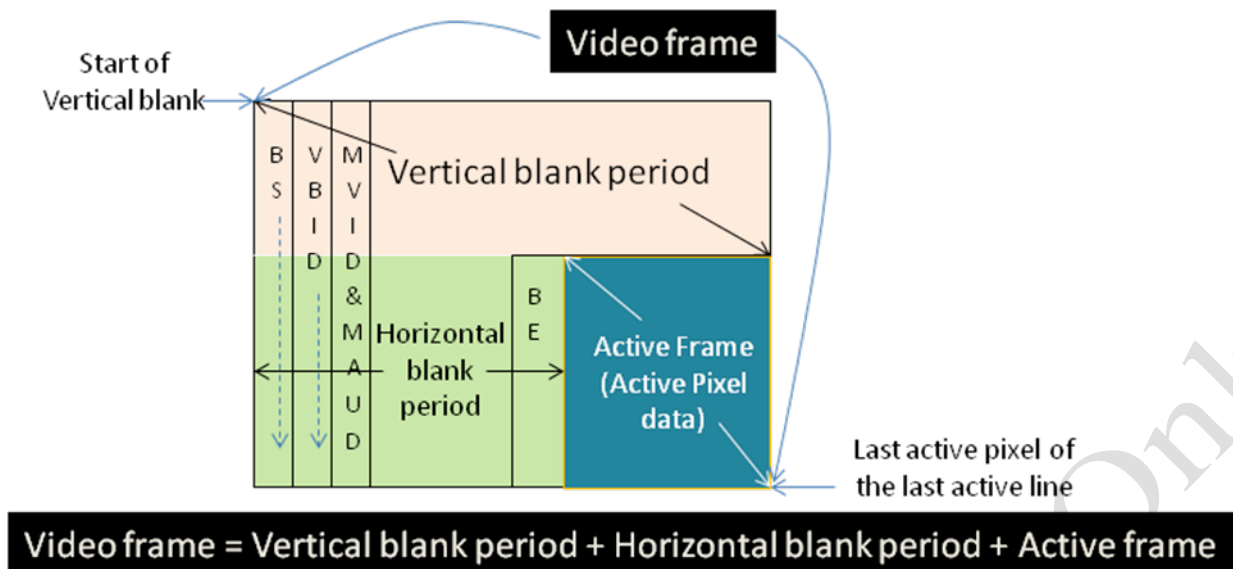


Figure 4-2: Pictorial Representation of Video Frame and Active Frame

4.1.1 Source Responsibilities

A Source device is responsible for determining when the displayed image is static, sending PSR Source state indication to the Sink. The Source sends PSR active state indication to the Sink, along with a complete active frame to capture.

The Source is responsible for sending the PSR state in a secondary data packet (SDP) for RFB management in the Sink. The SDP format used for PSR is defined in Section 3.5. The Source is also responsible for Source transmitter management. For additional power savings, the Source may turn its transmitter off while in Source PSR active state.

The Source should ensure that system responsiveness to a user input that affects display, such as cursor movement, is not perceptibly impacted by the PSR feature.

4.1.2 Sink Responsibilities

A Sink is responsible for declaring its capabilities, providing current status, calculating CRC for a captured static frame and generating interrupts for transmission or RFB errors to the Source.

The Sink is responsible for detecting PSR entry and exit events by tracking Source PSR state transitions. Upon detecting entry, the Sink must capture the entire static frame into the RFB and display from it until the Source indicates PSR inactive state. The Sink is responsible for switching from the active stream to the RFB and switching to locally generated timings on PSR entry without visual artifacts. The Sink is responsible for differentiating PSR entry from Main Link errors to provide correct event notification to the Source.

While in PSR active state, the Sink is responsible for generating video frame timings locally, and tracking the Source PSR state for RFB management. If the Sink receives PSR inactive state from the Source, the Sink is responsible for performing timing re-synchronization and switching from the RFB to the active stream without visual artifacts and no added latency.

Note that timing re-synchronization means the Sink is driving the display from locally generated video timings while in the process of synchronizing to the timings generated by the Source. Both the Source and Sink are expected to be in frame timing synchronization at the end of timing re-synchronization.

4.2 Configuration

A Sink declares its PSR capability in the “Sink PSR capability” DPCD registers. The default state of these registers is described in Section 3.4. The Source must read the Sink PSR capability registers to confirm it is a PSR capable device. After confirming the Sink’s PSR capability, a Source may update the Sink PSR configuration registers such as “Source transmitter state in PSR active”, “CRC verification in PSR active” and “Frame capture indication” if it chooses to change their default settings and then enable the PSR function. Default settings for Sink PSR configuration registers are described in Section 3.4.

A Sink must be ready to correctly process the first SDP with Video Stream Configuration (VSC) packet revision #2 received after it has ACKed a PSR function enable. VSC packet revision #2 contains PSR control data. It will be referred to as a PSR control packet in the rest of this document, and the SDP with PSR control packet will be referred to as a PSR SDP. Refer to Section 3.5 for a description of the VSC packet revision #2. The Source must not send an SDP with PSR control packet until it has received an ACK from the Sink for the PSR function enable AUX write.

Note that this configuration happens through AUX channel read/write commands. This may be done while the Sink is displaying active video, and the Sink must continue to correctly display video.

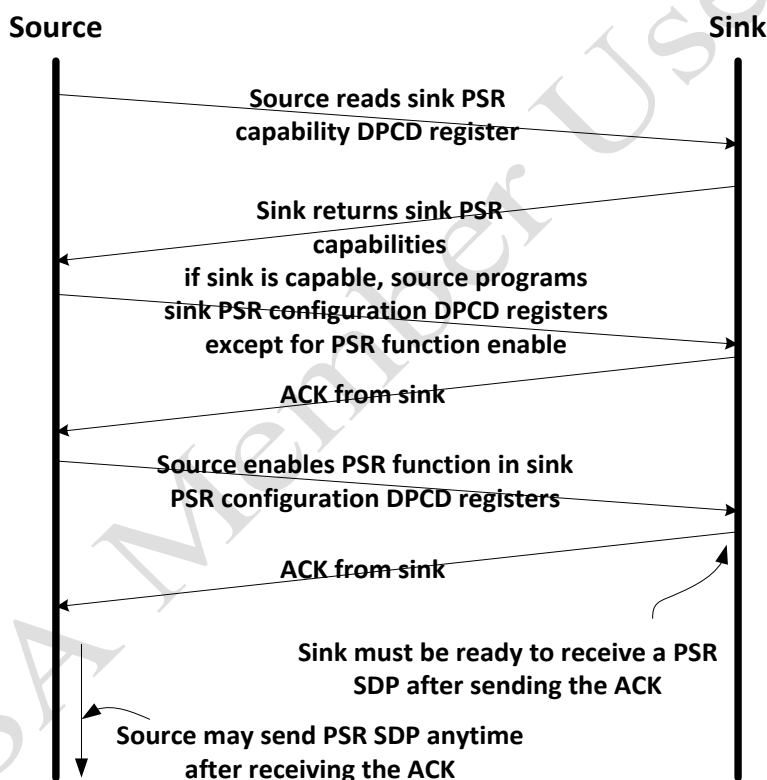


Figure 4-3: PSR Configuration

A Source may change the PSR configuration registers anytime while the PSR function is disabled. While the PSR function is enabled, if the Source chooses to change any PSR configuration registers, it must first disable the PSR function, change them and then re-enable the PSR function. If the Sink is not ready to process the PSR enable, it may NAK using the existing AUX policy. The PSR function may be disabled by the Source at any time.

If a Sink chooses to change any of its PSR capability registers, it may first update the PSR capability registers, and then notify the Source by setting the “Sink PSR capability change” PSR ESI register to “1” and generating an IRQ_HPD. The Source must clear the “Sink PSR capability change” PSR ESI register by writing “1” into this register. Sink PSR capability changes take effect only after the Source clears the “Sink PSR capability change” PSR ESI register. When the “Sink PSR capability change” PSR ESI register is set to “1”, the Sink must not update

any PSR capability registers until it is cleared by the Source. The PSR ESI register is described in Section 3.4 of this document.

Detailed steps for making Sink PSR capability changes:

- (1) For changing PSR capabilities in the Sink, a Sink must update the PSR capability registers, set the “Sink PSR capability change” bit to “1” in the PSR ESI register and make a PSR capability change notification to the Source by generating IRQ_HPD.
- (2) The Source must read the “Sink PSR capability change” bit in the PSR ESI register after receiving IRQ_HPD. The Source may complete any current AUX transaction before reading the PSR ESI or PSR capability registers. Note that the Source is allowed to read the PSR ESI register even without receiving an IRQ_HPD. If a Sink receives a read request of PSR capabilities from the Source, while it is making any changes to the PSR capability registers, it must not allow the read to complete until the changes are complete. A Sink may generate a NACK to keep the read from completing.
- (3) If the “Sink PSR capability change” bit in the PSR ESI register is set to 1, the Source must read the Sink PSR capability registers. The Source must exit the PSR active state if PSR is active and must disable the PSR function, if the PSR function is enabled. The Source must update the PSR configuration registers if they are impacted by the Sink PSR capability change, after disabling the PSR function. If there are no changes required in the Sink PSR configuration registers due to the Sink PSR capability changes, the Source may skip the update PSR configuration registers step and allow the Sink PSR capability changes to take effect as described in the following step.
- (4) The Source must clear the “Sink PSR capability change” bit in the PSR ESI register by writing “1” into the PSR ESI register to make the PSR capability changes effective. The Sink must not make any additional changes until the Source clears the PSR ESI register. The Sink should continue to function as it did before the ESI/IRQ_HPD with the current PSR configuration during this period of time, until the changes take effect.
- (5) The Source must enable the PSR function when it chooses to re-enter PSR.

4.3 PSR Entry/Exit Protocols

This section describes the protocols for PSR entry and exit events, and Main Link management during a PSR active state.

When a Source needs to send the PSR state indication SDP while it is transmitting an active stream, it must send the PSR SDP during the blanking period. The Sink must track the Source PSR state transitions to detect entry and exit events. A Source must not send more than one SDP with the same PSR state indication in a video frame. A Source may send a maximum of two PSR SDPs with different PSR state indications in a video frame. The usage of sending two different state indications will be discussed in Sections 4.3.4 and 4.3.5.

4.3.1 PSR States

Separate PSR states are defined for the Sink and Source.

4.3.1.1 Source PSR States

A Source supports six PSR states.

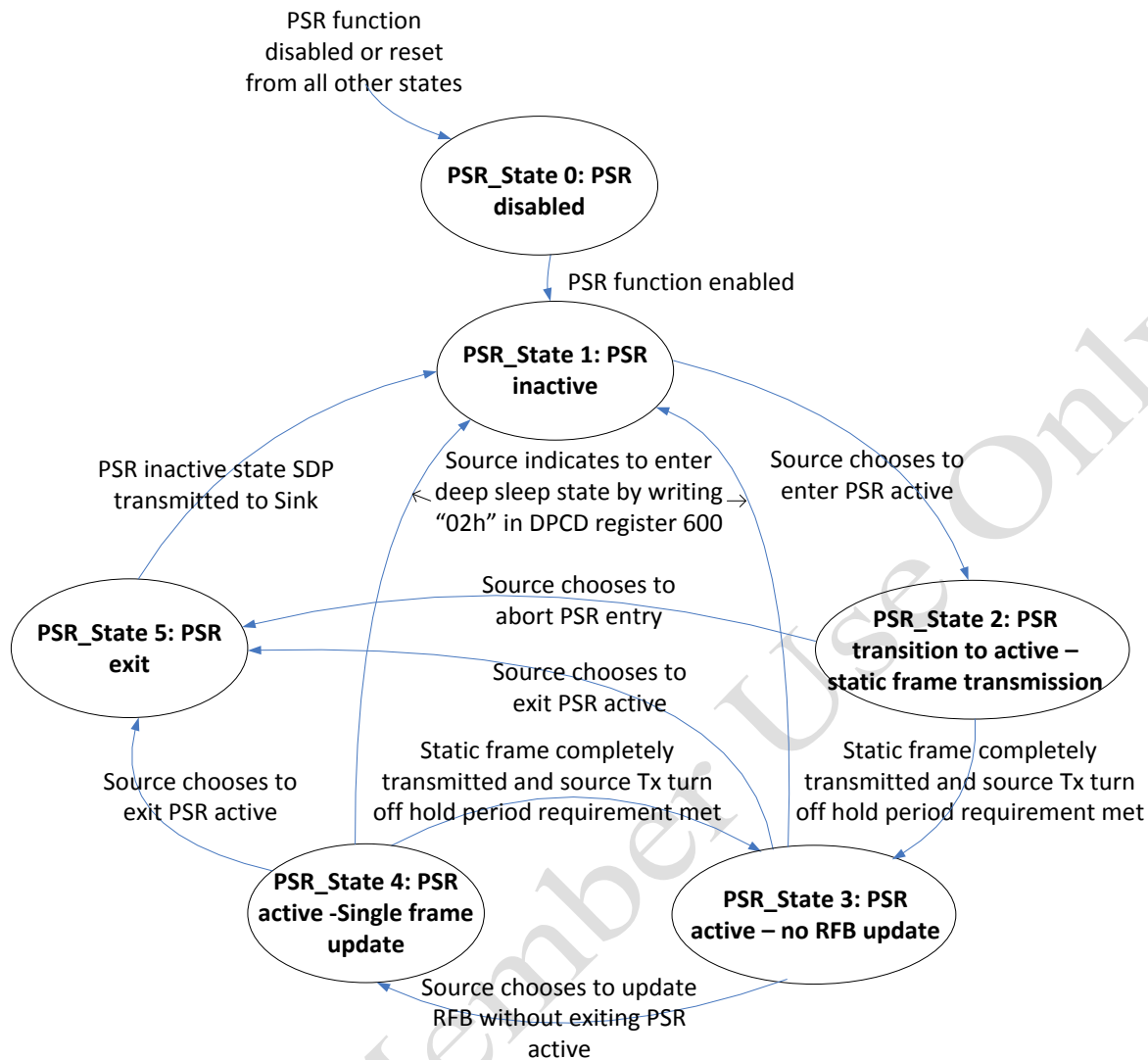


Figure 4-4: Source PSR States

- PSR disabled (PSR_State 0): Source operates in normal operation. A Source must stay in this state until the PSR function is enabled. A Source must return to this state if the PSR function is disabled while in any other PSR states. A Source must not send any SDP with PSR control packet in this state.
- PSR inactive (PSR_State 1): Source operates in normal operation. In this state, a Source may send a PSR SDP with PSR state set to inactive, and it must not send a PSR SDP with PSR state set to active. A Source stays in this state until it chooses to enter PSR active.
- PSR transition to active – static frame transmission (PSR_State 2): A Source must send an SDP with PSR state set to active along with a static frame to capture into the RFB by the Sink in this state. The Source must go to the “PSR active – no RFB update” state after completely transmitting a static frame and the Source TX turn off hold period requirement is met. Refer to section 4.3.2 for details on Source TX turn off hold period. If the Source chooses to abort entering the “PSR active – no RFB update” state it must go to the PSR exit state and generate a PSR SDP with PSR inactive state from the PSR exit state. Note that the abort described here is only for entering the “PSR active – no RFB update” state and the Source must not abort transmission of an active frame in the middle of a video frame.
- PSR active – no RFB update (PSR_State 3): A Source may turn off its transmitter or keep it active. Even when the transmitter is active, the Source may stop sending active pixels in this state. The Source must only send a PSR SDP with PSR active state when the transmitter is active and sending valid video frames.
- PSR active – single frame update (PSR_State 4): A Source must enter this state for transmitting a static frame to update the RFB without exiting PSR active. In addition to static frame transmission, the Source must send a

single frame update notification in the SDP to the Sink in this state. Single frame update notification is described in detail in section 4.3.5.

- PSR exit (PSR_State 5): When a Source chooses to exit PSR active from any PSR active states (states 3 and 4) or the PSR transition to active – static frame transmission state (state 2), it must enter the PSR exit state and generate a PSR SDP with PSR inactive state indication in a video frame. It must go to the PSR inactive state after transmitting the SDP with PSR inactive state indication to the Sink.

A Source chooses when to enter the “PSR transition to active – static frame transmission” state based on an implementation dependent algorithm. Determination of the exit condition from PSR active states is implementation specific and is out of scope for this spec. When this document refers to PSR active instead of actual state names it means the Source is in one of the two PSR active states (PSR_State 3 or PSR_State 4).

4.3.1.2 Sink PSR States

A Sink supports five PSR states. Sink PSR states are shown in figure 4-5.

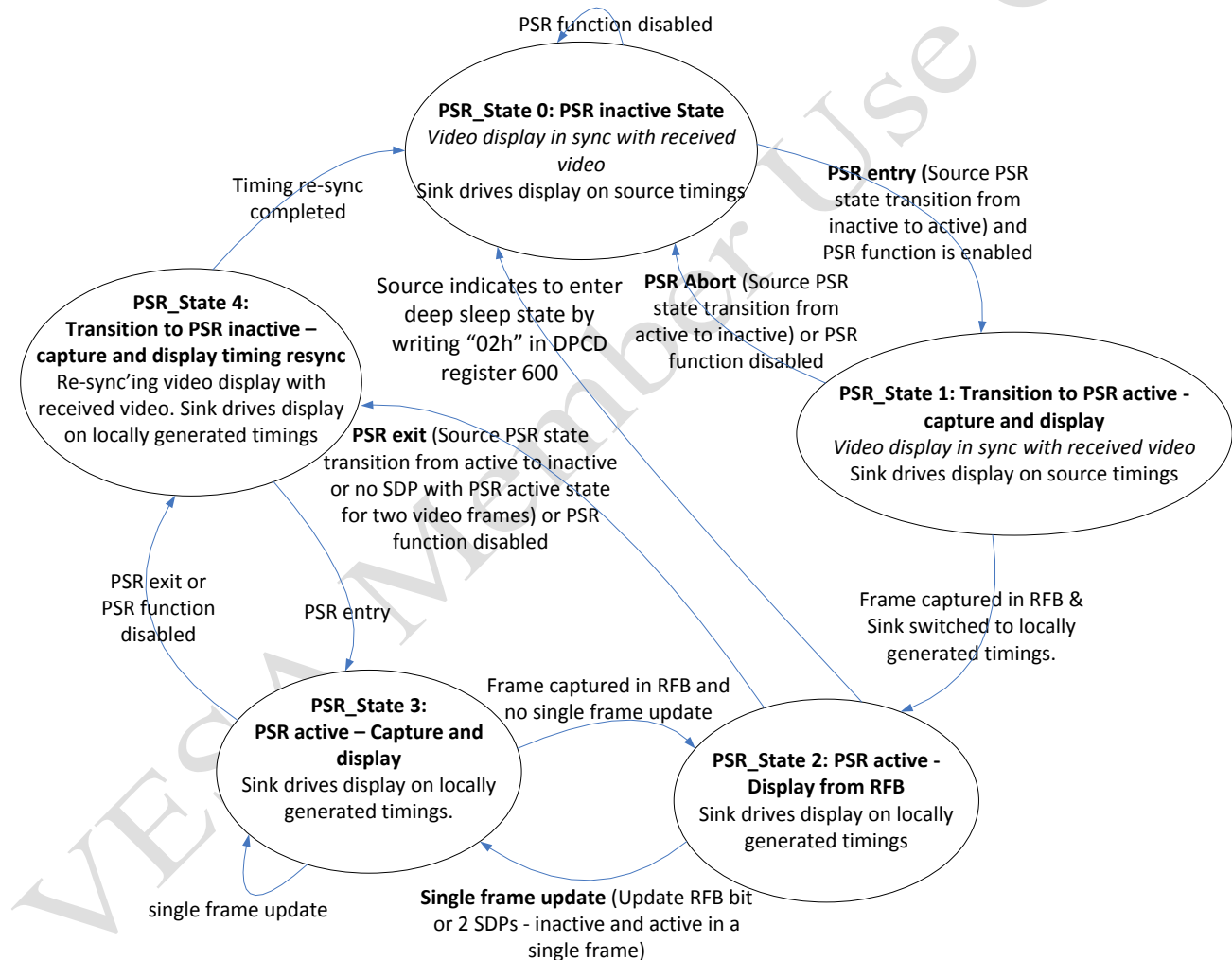


Figure 4-5: Sink PSR States

Sink PSR states:

- PSR inactive state (PSR_State 0): Sink is in normal operation. When an active stream is received from a Source, a Sink displays it and drives the display with Source timings. If the Source does not provide any video

data, the Sink is expected to display black video as described in section 5. A Sink remains in this state until the Source enables the PSR function in the Sink and sends a PSR SDP with PSR active state indication. While in Sink PSR_States 2, 3 or 4, if the PSR function is disabled, the Sink must return to this state through PSR_State 4. While in Sink PSR_State 1, if the PSR function is disabled, the Sink must return to this state directly.

- Transition to PSR active – capture and display (PSR_State 1): In this state, a Sink captures the static frame into the RFB while displaying it on Source timings. The Sink switches to locally generated timing before BS of the 9th line following the last line of the captured static frame, unless there is an abort.
- PSR active – display from RFB (PSR_State 2): A Sink displays the captured static frame in the RFB and drives the display with locally generated timings. The Sink discards pixel data from the Source, even if it is present, in this state.
- PSR active – capture and display; on Sink timings (PSR_State 3): In this state, a Sink captures a static frame into the RFB while displaying from the RFB. The Sink drives the display with locally generated timings in this state.
- Transition to PSR inactive – capture and display; timing re-synchronization (PSR_State 4): In this state, a Sink transitions from locally generated timing to the Source timing. The Sink must display the incoming active frames from the Source with no visible glitches/artifacts. If PSR active is signaled by the Source before the transition to Source timing is completed, the Sink enters PSR_State 3.

4.3.2 PSR Entry

To initiate PSR entry, a Source must send a PSR active state indication in a PSR SDP during the vertical blanking period. The Sink may have to power up resources to capture the active frame into the RFB upon receiving a PSR SDP with PSR active indication, if they are not powered up already. The time required for the Sink to power up the resources and be ready to capture an active frame into the RFB is referred to as the PSR entry setup time. The Sink must declare this in the “PSR setup time” field of the Sink PSR capability registers as described in Section 3.4. A Source must read this register during configuration and use it for determining if the Source is capable of sending a PSR SDP with PSR active state with a setup time before the active frame starts that meets the PSR entry setup time.

If the Source determines that a PSR SDP with PSR active state indication can be sent before the PSR entry set up time declared by the Sink, it must indicate to the Sink to capture the active frame of the video frame the SDP is sent in, as shown in Figure 4-6, by clearing the “Frame capture indication” field of the PSR configuration DPCD register in the Sink. The Source must clear this DPCD register before the PSR function is enabled in the Sink PSR configuration DPCD register, as described in Section 4.2. The “Frame capture indication” field of the Sink PSR configuration DPCD register is described in Section 3.4. When a Sink receives a PSR SDP with a PSR control packet, it must detect the Source PSR state transition from inactive to active and capture the following active frame within that video frame into the RFB. If the Source sends a PSR SDP with PSR inactive state before the end of the first horizontal line of frame “n+1”, the Sink must abort PSR entry and display from the video stream on the Main Link. Refer to Section 4.3.4 for more details about PSR entry abort.

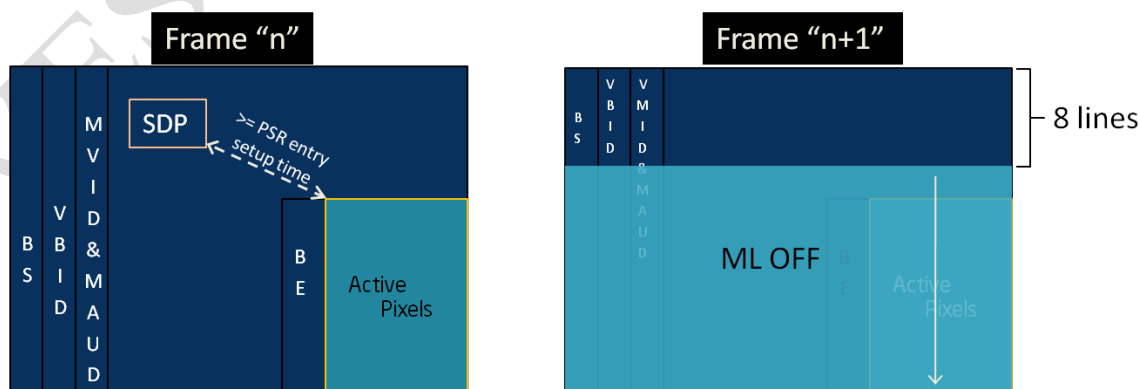


Figure 4-6: PSR Entry for Source TX Off Case

If the Source determines that a PSR SDP with PSR active state indication can't be sent before the PSR entry setup time, it must indicate to the Sink to capture active frame "n+1" instead of "n" by setting the "Frame capture indication" field of the Sink PSR Configuration DPCD register. A Source must program this DPCD register before the PSR function is enabled as described in Section 4.2. In this case the Source must send a PSR SDP with PSR active state in video frame "n" for capturing active frame "n+1" into the RFB.

When the frame capture indication field is set to 1, and a Sink receives a PSR SDP with PSR active state indication in video frame "n", the Sink must capture active frame "n+1". The Source must send a PSR SDP with PSR active state indication in video frame "n+1" also. If the Source sends a PSR inactive state indication before the end of the first horizontal line in frame n+2, the Sink must abort PSR entry and display from the video stream on the Main Link. PSR entry abort is described in detail in Section 4.3.4.

A Sink must switch to locally generated timings and display from the RFB after PSR entry is completed.

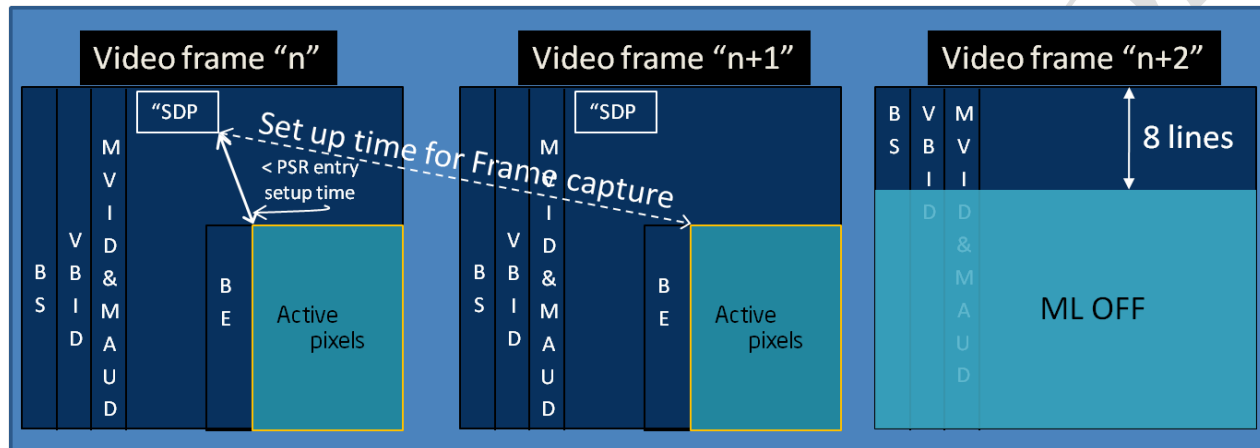


Figure 4-7: PSR Entry when Source can't Send PSR Active SDP before Setup Time

While a Sink is in a PSR active state, if the Source writes "02h" into DPCD register 600h, the Sink must enter power-save mode.

4.3.2.1 PSR Entry Link Management

A Source may keep its Main Link transmitter active or turn it off upon entering a PSR active state. A Source must indicate which option it chooses in the "Source transmitter state in PSR active" bit of the PSR configuration registers in the Sink DPCD registers described in section 3.4. By default this bit must be cleared to 0 (Source TX off). A Source must update the "Source transmitter state in PSR active" DPCD bit to 1 if it chooses to keep its Main Link transmitter active, before enabling the PSR function as described in Section 4.2.

4.3.2.1.1 Source Transmitter off

A Source may turn its transmitter off after the BS sequence of the 9th line of video frame "n+1" as shown in figure 4-6. If the "Frame capture indication" field of the DPCD registers is set by the Source, the Source may turn its Main Link transmitter off after the BS sequence of the 9th line in video frame "n+2" as shown in figure 4-7. This period is referred to as the "Source TX turn off hold period" within this document.

If the Main Link transmitter is turned off after the Source TX turn off hold period and the "Source transmitter state in PSR active" field in the DPCD registers is cleared to 0, the Sink must not generate a loss of sync IRQ_HPD to the Source, and the SINK_STATUS bit (bit 0 of DPCD register 00205h) must maintain its value of '1'. If the "Source transmitter state in PSR active" bit is set to 1, the Sink must generate a loss of sync IRQ_HPD as it would normally, and the SINK_STATUS bit must be reset to '0'. Upon receiving a loss of sync IRQ_HPD, a Source must take corrective action as described in DP1.2 section 2.9.3.5.

A Source may send a PSR SDP with PSR control data during the Source TX turn off hold period if the Source chooses to send any additional information such as CRCs to the Sink before the Source Main Link transmitter is turned off. The PSR state must be set to active in this SDP unless the Source chooses to abort PSR entry. PSR entry abort is described in section 4.3.4.

If a Source chooses the Sink to perform CRC check by setting the “CRC verification in PSR active” field of the Sink DPCD registers to “1” and if the Source CRCs for the static frame are not available until multiple video frames later, the Source must keep its Main Link transmitters active even after the Source TX turn off hold period. After the Sink receives all required data including CRCs for the static frame from the Source, it may turn its Main Link receiver off even before the Source TX turn off hold period requirement is met. Refer to Figure 4-13 and Figure 4-14 for the CRC SDP timing.

4.3.2.1.2 Source Transmitter Active

As described in the DP 1.2, section 5.2.5, a Source device may keep transmitting an Idle Pattern over the Main Link even when there is no video stream to transmit. The Source device may start the transmission of a video stream without initiating Link Training. Therefore, when the “Source transmitter state in PSR active” field in the DPCD registers is set to 1, the Sink device must keep its Main Link receiver active as long as it is receiving either a video stream or Idle Pattern and as long as it keeps the HPD signal asserted.

If the Source keeps the Main Link transmitter active and transmits valid video frames, it must send a PSR SDP with PSR state set to active on every video frame. The active frame data may be invalid. The Sink must ignore the active frame data and display from the RFB.

If the Source keeps the Main Link active and transmits an Idle Pattern, as described in DP1.2, section 2.2.1.1, the BS framing sequence must be periodically (every 2^{13} or 8,192 symbols) inserted for active links with no main video stream data to send. The Source must replace every 512th BS sequence with an SR (or CPSR). It is optional for the Source to send a PSR SDP while transmitting Idle Patterns. The Sink must ignore a PSR SDP while receiving an Idle Pattern. Refer to section 3.5 for details on the VSC packet revision number.

A Source must not switch to an Idle Pattern if it hasn't completely sent the required information to the Sink in a PSR SDP, such as CRCs when “CRC verification in PSR active” is set to 1.

4.3.3 PSR Exit

To exit from a PSR active state, a Source must send a PSR SDP with PSR inactive state indication to the Sink. The Sink must detect the Source PSR state transition from active to inactive to detect the PSR exit event and display active video from the eDP link. As shown in the state diagram in Figure 4-5, a Sink goes through the Sink “Transition PSR inactive - capture and display timing re-synchronization” state for switching to link timings. The Sink must support PSR re-entry during timing re-synchronization if the Source PSR state changes to active. The Sink must display the active frames received from the Source with no visible glitches/artifacts and no discernable loss of data on the display during timing re-synchronization.

A Sink must exit from a PSR active state when the Sink power management state machine transitions to the OFF state (power state 4) to handle cases such as a system crash. The Sink power management state machine is described in detail in Figure 5-2 of DP v1.2. If the Sink exits PSR active in this fashion, it must automatically reset the PSR enable control bit to a value of 0.

A PSR SDP that carries PSR state indicating inactive may be sent during the vertical or horizontal blanking periods.

A Sink may turn off the RFB and the associated functions such as PLLs, local timing generators, etc., after entering the PSR inactive state for power savings.

4.3.3.1 PSR Exit Link Management

When the Source is in a PSR active state, there are two cases to consider for PSR exit link management – (1) Source Main Link transmitters off and (2) Source Main Link transmitter active.

4.3.3.1.1 Source Transmitter Off

If the Source Main Link transmitter is off, upon detecting conditions for PSR exit, a Source must wake the Sink by writing “01h” to DPCD address 600h of the Sink device via the AUX channel. The Sink must send an ACK after powering up its Main Link RX and prepare for link training. Link training is optional and the Sink declares if it is required in the “link training requirement of Sink on PSR exit” field in the DPCD PSR capability registers as described in Section 3.4.

If link training is not required, the Source may omit the training phase of link bring up, and move directly to transmission of Idle Patterns. The Source must generate at least 5 Idle Patterns prior to the first valid data (SDP, MSA/VBID/MVID/MAUD or active video frame) sent. The first Idle Pattern sent may start with either a BS or SR sequence. After a minimum of 5 Idle Patterns have been sent, prior to sending the first valid data, the Source is required to send an SR sequence and thereafter maintain the “every 512th BS sequence must be replaced by SR sequence” policy as described in Section 2.2.1.2 of DP v1.2. The Sink must perform clock recovery and symbol lock within five Idle Patterns, instead of using training patterns. The Sink must perform scrambler synchronization after receiving the SR sequence to correctly receive the first valid data.

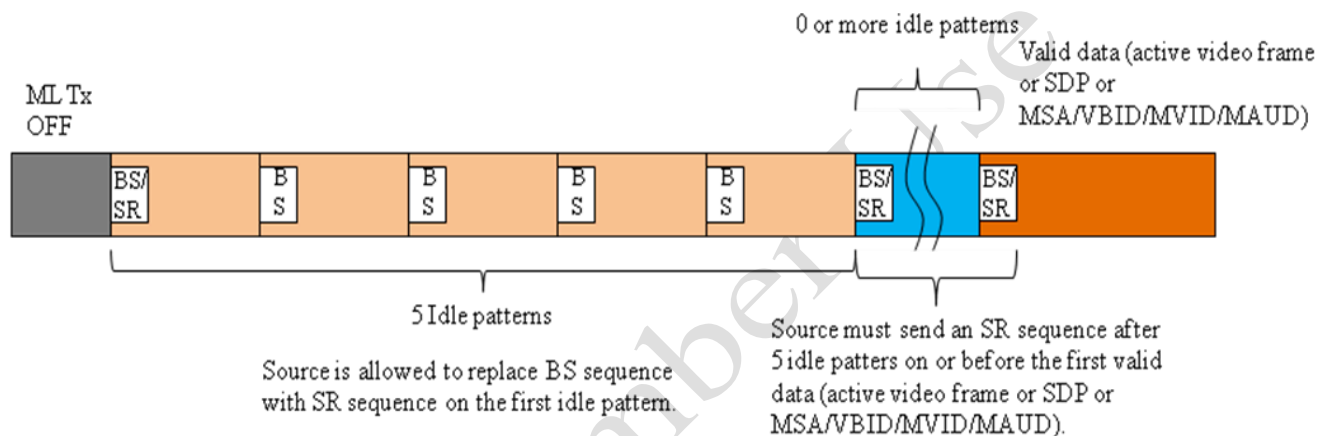


Figure 4-8: PSR Exit Link Management With No Link Training

If link training is needed, a Source initiates link training after receiving an ACK from the Sink, and after satisfying the Main Link common mode pre charge time.

In both of the above cases, if the Source doesn't receive a valid ACK from the Sink after writing “01h” to DPCD address 600h, the Source must retry the AUX write until a 1ms wake up time out period expires, before taking corrective action in an implementation dependent manner. The 1ms wake up time out restriction is applied only to PSR Sinks when the PSR function is enabled.

The Sink must properly handle an SR sequence received after link training is completed.

Note that the Source is not required to write “02h” into register 600h when turning off the Main Link upon PSR entry.

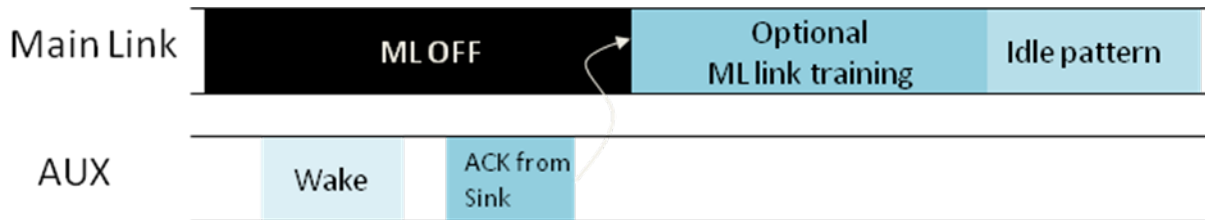


Figure 4-9: PSR Exit Link Management

As described in DP v1.2, Section 2.9.3.4, after Link Training is successfully completed (which means the DisplayPort receiver is synchronized to the incoming Main Link data) and before transport of a main video stream starts, the Source Main Link transmitter must send at least five Idle Patterns.

After link training and sending five Idle Patterns, a Source may take one of the following actions.

- (1) The Source may continue to send Idle Patterns. The Sink must continue to display from the RFB until it receives a Source PSR inactive state indication in a PSR SDP in a valid video frame. If the Sink receives a PSR SDP during an Idle Pattern, it must ignore the SDP. The Source must send a PSR SDP with PSR inactive state in a video frame to indicate PSR exit to the Sink. Upon receiving a Source PSR inactive state indication, the Sink must exit the “PSR active – display from RFB” state and display active frames from the Main Link.
- (2) The Source may send active video frames. There are three sub-options in this case
 - a. The Source may send a PSR SDP with PSR inactive state on the first video frame, telling the Sink to exit immediately from the “PSR active – display from RFB” state. This is the desired method for exiting PSR active. The Sink must exit the PSR active state and display active frames from the Main Link.
 - b. The Source may send a Source PSR active state indication in a PSR SDP in one or multiple video frames. In this case, the Sink must ignore the active frames received on the eDP Main Link and must continue to display the static frame from the RFB until the Source sends a PSR inactive state indication. When the Source PSR inactive indication is received from the Source, the Sink must exit the “PSR active – display from RFB” state and display active frames from the Main Link.
 - c. In recovering from an error, the Source may not send a PSR SDP with PSR active state in the vertical blank period of the first two frames. In this case, the Sink must exit the “PSR active – display from RFB” state after the vertical blank period of the second frame and display active frames from the Main Link. The Sink must not capture or display the active frames on the Main Link until it detects two frames with no PSR SDPs and exits from PSR active. This is an error case and is not a desired normal way to exit PSR active.

If a the Source supports modes of operation that are not PSR aware, it must always write 01h to DPCD register 600h before any mode set sequences in non-PSR aware modes of operation, to ensure PSR exit in the Sink.

4.3.3.1.2 Source Transmitter Active

If the Source Main Link transmitter remains active, the Source may send Idle Patterns or valid video frames with a PSR SDP that carries PSR state. The Sink must keep the Main Link receiver active as long as it is receiving either a video stream or Idle Pattern and as long as it keeps the HPD signal asserted.

When the Source is sending valid video frames, it must send a PSR SDP with PSR active state indication in every video frame. If the Source chooses to exit PSR active, it must send a PSR SDP with PSR inactive state indication. While receiving valid video frames, the Sink must monitor all PSR SDPs for Source PSR state transition from active to inactive in order to detect PSR exit. The Sink must also exit PSR active if it doesn't receive a PSR SDP for two consecutive video frames; this is an error case and should not be used in normal operation. Upon detecting PSR exit, the Sink must exit the "PSR active – display from RFB" state, and display active frames from the Main Link.

When the Source is sending Idle Patterns, it is optional for the Source to send a PSR SDP. The Sink must ignore all PSR SDPs while receiving an Idle Pattern. Refer to section 3.5 for details on the VSC packet revision number. To exit from PSR active, the Source must switch from Idle Patterns to a valid video frame and send a PSR SDP with PSR inactive state indication in that video frame as described in the previous paragraph.

4.3.4 PSR Entry Abort

If a Source chooses not to enter PSR active after sending a PSR SDP with PSR active state indication to the Sink, it may abort PSR entry, or enter PSR active and exit on the subsequent video frames.

To abort PSR entry, when "Source transmitter state in PSR active" is cleared to "0", the Source must send a PSR SDP with PSR inactive state before the end of the first horizontal line in video frame "n+1" as shown in figure 4-10 and continue to send active frames on the Main Link. When the "Frame capture indication field" is set to 1, the Source may abort before the end of the first horizontal line in frame "n+2". The Sink must return to the PSR inactive state from the "Transition to PSR active - capture and display" state and drive the display with the active stream received on the Main Link, using Source timings. The Sink may turn off the RFB and the associated functions such as PLLs, local timing generators, etc., after entering the PSR inactive state for power savings.

If the Source chooses to enter PSR active and then exit, it may exit PSR active as described in Section 4.3.3.1.

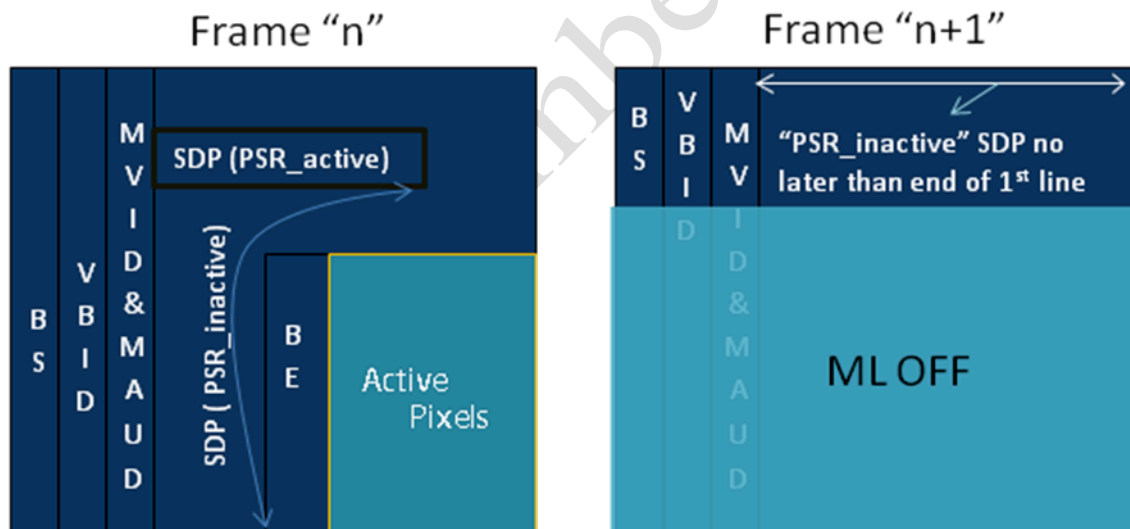


Figure 4-10: PSR Entry Abort for Source TX Off Case

When "Source transmitter state in PSR active" is cleared to "0" and the Source sends a PSR SDP with inactive state to abort PSR entry after the end of first horizontal line, it is an error condition and if the Sink detects it, it may send an IRQ_HPD to indicate the error.

When "Source transmitter state in PSR active" is set to "1", the Source may abort PSR entry by sending a PSR SDP with PSR inactive state in the same video frame as the static frame, or exit PSR active by sending a PSR SDP with PSR inactive on the following video frames.

4.3.5 Single Frame Updates

While the Sink is in a PSR active state, to update the RFB with a single static frame without exiting Sink PSR active, the Source may send a PSR SDP with Source PSR inactive and a second SDP with Source PSR active in the same video frame.

The Source may optionally set the “Update RFB” bit in the PSR SDP to indicate a single frame update instead of sending two SDPs in the same video frame. The Sink must ignore this bit if the Source PSR state is inactive or transitioning from PSR inactive to active state. If the Source PSR state is active and the Update RFB bit is set to 1, the Sink must capture the incoming static frame into the RFB, but should not perform timing re-synchronization. The following table describes the Sink actions for the Update RFB bit in the PSR SDP.

Source Previous PSR state	Source current PSR state	Update RFB	Sink action
Active (1)	Active (1)	Active (1)	Capture the incoming image into RFB, should not perform timing re-sync.
Active (1)	Active (1)	Inactive (0)	Must not capture incoming frame. Display from the RFB.
X	Inactive (0)	X	Ignore “Update RFB” indication
Inactive (0)	Active (1)	X	Capture the incoming image into RFB, should not perform timing re-sync. Ignore Update RFB indication

Table 4-1: Sink Action for Single Frame Update

When the Sink detects a single frame update notification from the Source, either through the Update RFB bit indication or PSR state inactive to active transition, it must only update the image in the RFB and should continue to run on locally generated timings. The Sink should not perform timing re-synchronization.

When a Source chooses to send a single frame update, the Source Main Link transmitter may be active or turned off. The Source must bring up the Main Link before sending the static frame to the Sink for updating the RFB. Both cases are described below.

A single frame update notification may be sent anytime during the vertical blanking period. For single frame updates, the Sink must ignore the “Frame capture indication” field of the Sink PSR configuration DPCD register, even if it is set to “1”, and capture active frame “n”.

4.3.5.1 Source Transmitter Off

For single frame updates when the Source transmitter is turned off, the Source must follow the steps described in Section 4.3.3 for bringing the Main Link up. After successful link training and sending Idle Patterns, the Source must send a single frame update notification to the Sink as described in section 4.3.5. The Sink must capture the active frame into the RFB and display from it. The Sink should not perform timing re-synchronization. The Source may turn its Main Link transmitter off after the Source TX turn off hold period (after the BS sequence of the 9th line of the next video frame).

4.3.5.2 Source Transmitter Active

As described above, when a Sink receives a single frame update notification from the Source, it must capture the active frame into the RFB and display from it. The Sink should not perform timing re-synchronization.

4.3.5.3 PSR Exit After Single Frame Update

If a Source wishes to exit PSR right after a single frame update, the Source must send a PSR SDP with PSR inactive state indication to the Sink before the end of the 1st line in vertical blank of the next frame.

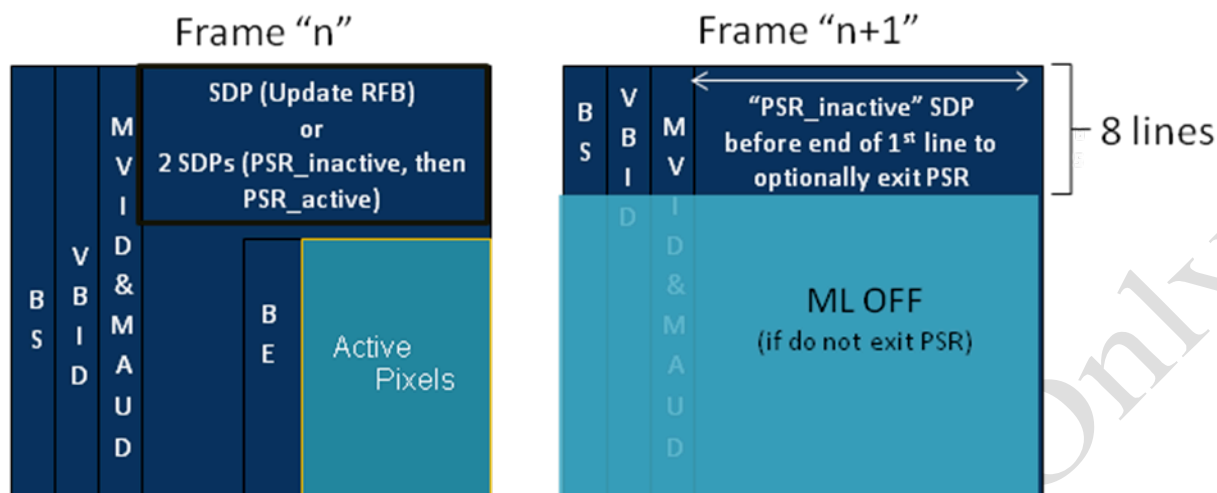


Figure 4-11: Single Frame Update Timing Shown with Optional SDP for PSR Exit

4.3.6 Burst Single Frame Updates

The single frame update mechanisms can be extended to multiple consecutive frames. A Source may send single frame updates for multiple consecutive frames to achieve burst single frame updates without exiting PSR active.

If a Source wishes to burst single frame updates, after the initial single frame update, the Source must send PSR SDPs indicating a single frame update, either through the Update RFB bit indication or PSR state inactive to active transition, to the Sink before the end of the 1st line in vertical blank of the next frame.

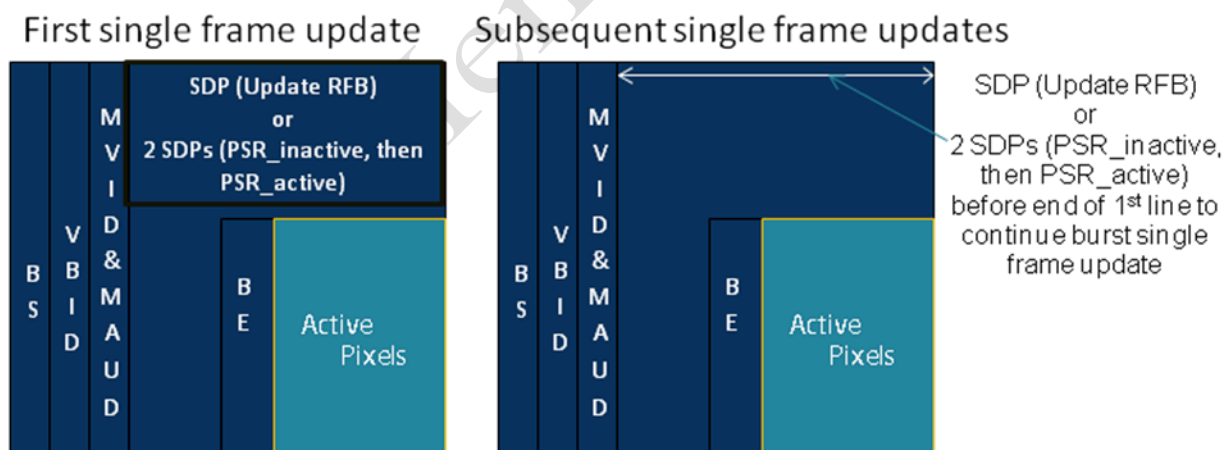


Figure 4-12: Burst Single Frame Update SDP Timing

4.4 Error Management/Recovery

This section describes the error reporting mechanism for three types of errors detected by the Sink. These are LINK CRC ERRORS, RFB STORAGE ERRORS and SINK INTERNAL ERRORS. CRC verification must be performed to identify transmission errors on the link. The Sink may verify the static image stored in the RFB for any storage errors. The Sink may use CRC verification for detecting storage errors in the RFB. RFB STORAGE

ERROR detection is implementation specific and is out of scope for this spec. Determination and detection of SINK INTERNAL ERROR is Sink implementation dependent and out of scope for this spec.

There are two functions related to CRCs (1) CRC generation and (2) CRC verification. It is mandatory for the Sink to generate CRCs upon receiving a static frame while in any of the Sink PSR active states regardless of what is programmed in TEST_SINK_START in the TEST_SINK DPCD register. TEST_SINK_START is a non-PSR DPCD register described in DP v1.2. This register is used to start CRC calculation in the Sink. CRC calculation is performed as described in DP v1.2. A 16 bit CRC is generated per color component, on active pixels only.

The Source must indicate whether verification for LINK CRC ERRORS must be performed by the Sink or not, by programming the “CRC verification in PSR active” bit in the Sink’s PSR configuration DPCD register. The “CRC verification in PSR active field” is described in section 3.4. It is optional for the Source to generate CRCs or perform CRC verification. The Sink must support CRC generation and verification methods as described below.

Notification for LINK CRC ERROR and RFB STORAGE ERROR are synchronous events. They are discussed in detail in Sections 4.4.1 and 4.4.2. SINK INTERNAL ERROR notification is asynchronous.

If Sink detects a “SINK INTERNAL ERROR”, it may indicate the error to the Source by reporting a value of “7” in the Sink panel self refresh status field of the Sink status DPCD register. If the Sink reports SINK INTERNAL ERROR, it must generate an IRQ_HPD to the Source. The Source may read the “Sink panel self refresh status” DPCD register and disable the PSR function to clear the SINK INTERNAL ERROR indication. The Sink must ensure that it doesn’t change the “Sink panel self refresh status” DPCD register from “7” until the PSR function is disabled by the Source. At this point the Source may take an action in an implementation dependent manner. Note that a state with encoding “7” is not shown in the Sink PSR state diagram in figure 4-5. Refer to section 3.4 for details on the “Sink panel self refresh status” field.

If a Source receives an IRQ_HPD, while in a PSR active state, and can’t identify the cause for the IRQ_HPD, based on sink status registers, the Source may take an implementation dependent action. One such action may be to exit PSR active and then re-enter PSR active.

4.4.1 CRC Verification Performed in Source

If a Source chooses to perform CRC verification in the Source, the “CRC verification in PSR active” bit of the Sink configuration DPCD register must be cleared to 0. The Sink must ignore any CRCs and the CRC Valid bit sent in a PSR SDP if the Source chooses to perform CRC verification in the Source.

When a Sink is in any of the PSR active states, the Sink must calculate CRCs for the static frame received on the link, update the DPCD registers TEST_CRC_R_Cr, TEST_CRC_G_Y and TEST_CRC_B_Cb, and indicate that CRCs for the received static frame are calculated and stored in the DPCD by incrementing TEST_CRC_COUNT in the TEST_SINK_MISC register. These registers and mechanism are described in the DP 1.2 spec. These registers are in the non-PSR DPCD range. If the Sink chooses to include RFB STORAGE ERROR completion to increment TEST_CRC_COUNT, it must wait for CRCs calculation and RFB STORAGE ERROR detection completion before incrementing TEST_CRC_COUNT.

The TEST_CRC_COUNT register must be reset on either one of these events:

- (1) PSR inactive to active transition – after receiving a PSR SDP with PSR active while the Sink is in a PSR inactive state
- (2) Single frame update notification as described in section 4.4.5.

A Sink must complete the CRC calculation and update the LINK CRC ERROR bit of the ERROR STATUS DPCD register before the end of video frame “n+1” after the static frame “n” is completely received on the link. Note that the Sink may update TEST_CRC_COUNT before the end of video frame “n+1” for early indication.

A Sink may verify the static image stored in the RFB for any errors in an implementation dependent manner. The Sink may update the RFB STORAGE ERROR bit of the ERROR STATUS DPCD register if it detects any errors before the end of video frame “n+1” after the static frame “n” is completely received on the link.

The Source may read the CRCs and the RFB STORAGE ERROR bit from the Sink after the Sink indicates the CRCs and RFB STORAGE ERROR bit are ready within one frame time by incrementing the TEST_CRC_COUNT or the Source may wait one video frame after completely transmitting the static frame and then read the CRCs and the RFB STORAGE ERROR bit. In either of these options, the Source may compare the CRCs received from the Sink against the CRCs of the static frame generated locally at the Source. If they do not match or the CRCs are not available after the end of one video frame after transmitting the static frame or RFB STORAGE ERROR bit is set to “1”, the Source may take corrective action in an implementation dependent manner.

4.4.2 CRC Verification Performed in Sink

If the Source chooses the Sink to perform CRC verification, the “CRC verification in PSR active” bit of the Sink configuration DPCD register must be set to 1 by the Source. The Sink will honor the CRC valid bit in the PSR SDP by using the corresponding CRCs in the PSR SDP to verify the CRCs generated for the static frame in the Sink. The Sink must compute the CRCs within 1 video frame time after the static frame is received from the Source.

A Source must send the CRCs of the static frame “n” after completely transmitting that video frame and, before the Source TX turn off hold period of video frame “n+2”. If the Sink doesn’t receive valid CRCs before the “Source TX turn off hold period” of video frame “n+2”, or if the CRCs received from the Source do not match with the CRCs locally generated in the Sink, the Sink must set the “LINK CRC ERROR” bit to “1”. The Sink may perform verification on the static image stored in the RFB and update the “RFB STORAGE ERROR” bit of the ERROR STATUS register. If LINK CRC ERROR or RFB STORAGE ERROR is set to “1”, the Sink must generate an IRQ_HPD to the Source. Upon receiving an IRQ_HPD for a CRC error, the Source may take an action in an implementation-dependent manner.

The Source must not send the CRCs of either the previous or current static frame to the Sink in the same video frame as the current static frame. If the Sink receives CRCs in the same video frame as a static frame, it is an error case and the Sink must ignore the CRCs.

If the Sink receives a new static frame from the Source before CRCs for the previous static frame are received, the Sink must ignore the CRCs generated internally for the previous static frame and must generate CRCs for the new static frame and compare them with the CRCs received from the Source for the new static frame. If the Source transmits a new static frame before sending CRCs of a previously transmitted static frame, it must not send the CRCs of the previously sent static frames and it must only send the CRCs corresponding to the latest static frame that is captured into the RFB.

If the Source sends burst single frame updates, it must not send CRCs until after the last static frame is sent.

A PSR inactive indication aborts the CRC generation and verification process in the Source and Sink.

The CRC SDP timing is shown in Figure 4-13 and Figure 4-14.

The “LINK CRC ERROR” and “RFB STORAGE ERROR” bits must be reset on either one of these events:

- (1) PSR inactive to active transition – after receiving a PSR SDP with PSR active while the Sink is in a PSR inactive state.
- (2) Single frame update notification as described in Section 4.3.5.

Frame capture indication = 0

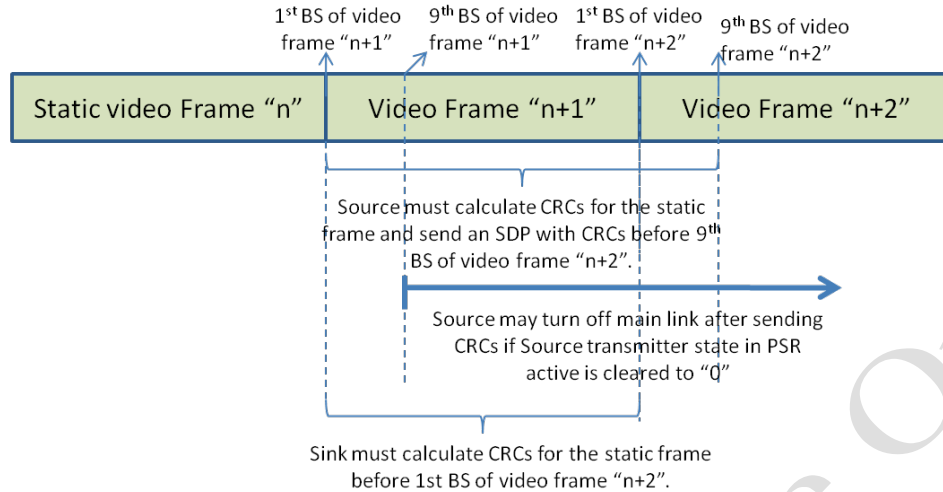


Figure 4-13: CRC SDP Timing with Frame Capture Indication = 0 and for Single Frame Update

Frame capture indication = 1

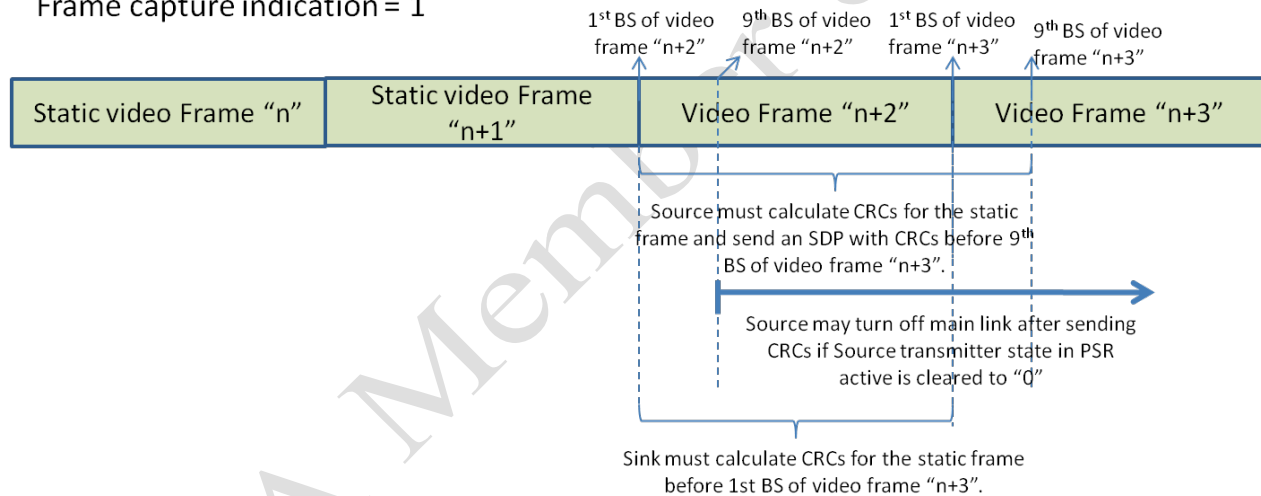
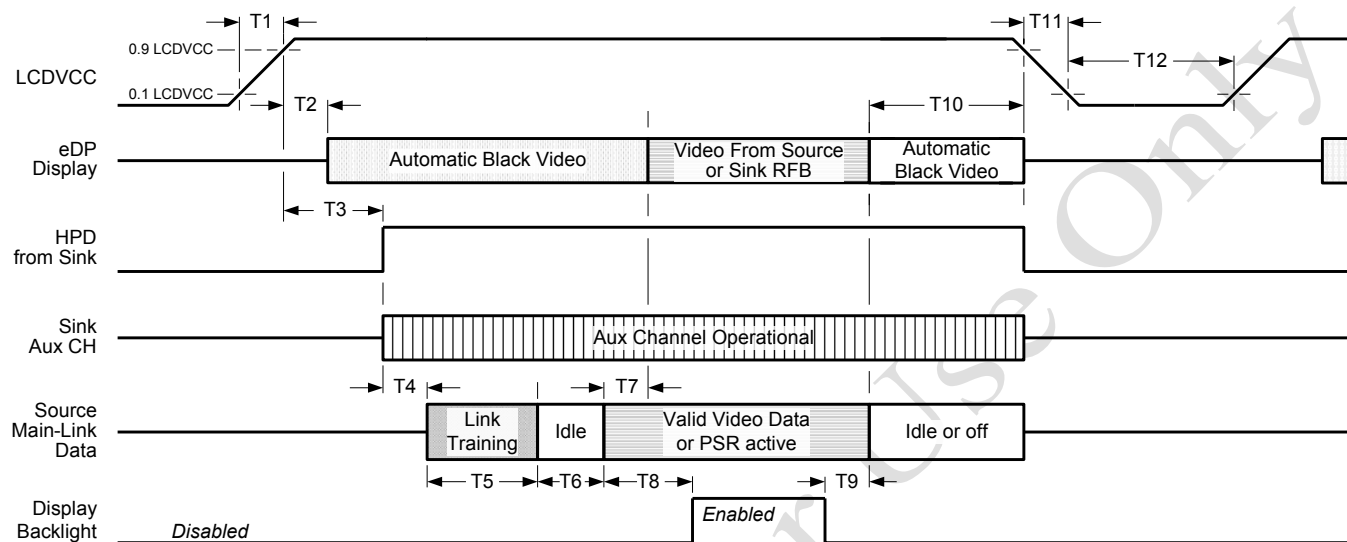


Figure 4-14: CRC SDP Timing with Frame Capture Indication = 1

5 Power Sequencing

The Power Up and Power Down Sequence is described in Figures 5-1 and 5-2, and Table 5-1. Figure 5-1 describes the Power Up/Down sequence for normal system operation. Figure 5-2 describes the Power Up/Down sequence when the Source executes an AUX Channel transaction only, without the display of video (which might be performed to read EDID, for example).



Note: Manual control of Black Video (using DPCD register 00720h, bit 1) is a system implementation option.

Figure 5-1: eDP Interface Power Up/Down Sequence, Normal System Operation

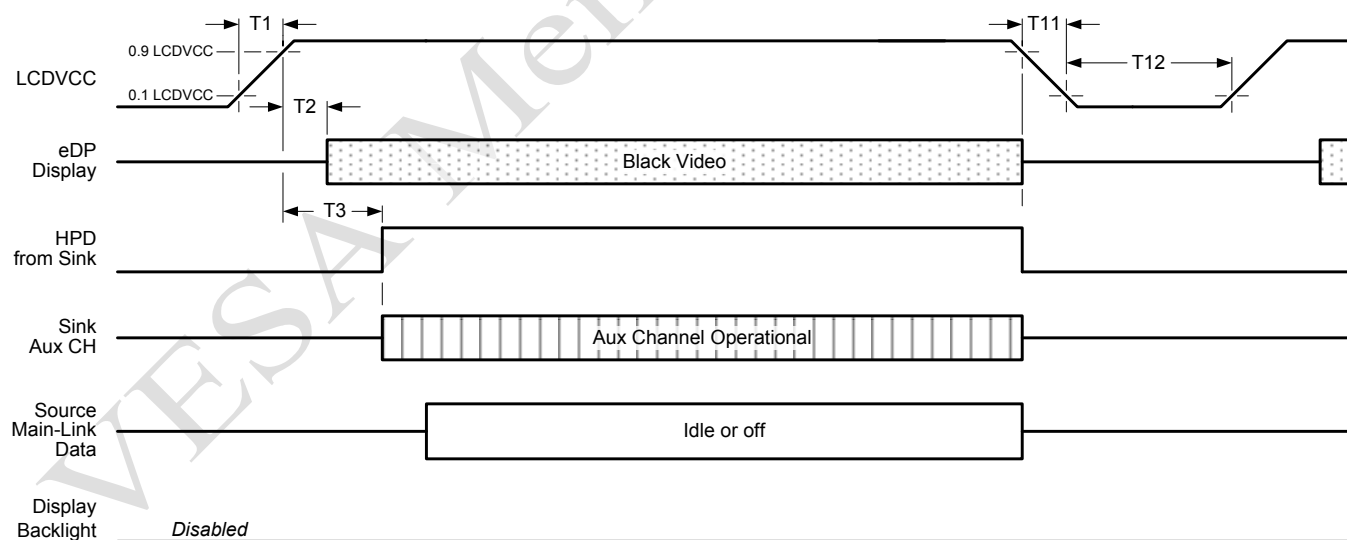


Figure 5-2: eDP Interface Power Up/Down Sequence, AUX Channel Transaction Only

Table 5-1: eDP Panel Power Sequence Timing Parameters

Timing Parameter	Description	Required By	Limits		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	
T2	Delay from LCDVCC to automatic Black Video generation	Sink	0ms	200ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes: 1 and 2 below)
T3	Delay from LCDVCC to HPD high	Sink	0ms	200ms	Sink AUX Channel must be operational upon HPD high (see Note: 3 below)
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for the Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on the Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle Pattern. Max allows for Source frame synchronization.
T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max value allows for the Sink to validate video data and timing. At the end of T7, the Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and the Sink will no longer generate automatic Black Video.
T8	Delay from valid video data from Source to backlight enable	Source	-	-	The Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	The Source must assure backlight is no longer illuminated. At the end of T9, the Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and the Sink will automatically display Black Video. (See Notes: 1 and 2 below)
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	
T11	Power rail fall time, 90% to 10%	Source	-	10ms	
T12	Power off time	Source	500ms	-	

Note 1: The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

Upon LCDVCC power-on (within T2 max)

When the “NoVideoStream_Flag” (VB-ID Bit 3) is received from the Source (at the end of T9)

When no Main Link data, or invalid video data, is received from the Source. Black Video must be displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The Sink may implement the ability to disable the automatic Black Video function, as described in Note 1, above, for system development and debugging purposes.

Note 3: The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to respond to an AUX Channel transaction with the time specified within T3 max.

VESA Member Use Only

6 eDP Connector Pin Assignments

Standardized pin assignments for eDP are provided in Tables 6-1, 6-2, 6-3, and 6-4. It is up to the manufacturer to select the eDP pin assignment appropriate for the panel configuration. This selection is primarily determined by the required number of Main Link lanes and the backlight configuration. The manufacturer will also select a connector type and connecting cable wire gauge appropriate for the panel's supply and ground current requirement. There are a variety of available connectors that have been qualified for eDP application.

When only a single lane is used on a connector that supports two lanes (Tables 6-1, 6-2, and 6-3), Lane 0 will be connected and Lane 1 will remain unconnected. When only two lanes are used on a connector that supports four lanes (Table 6-4), Lanes 0 and 1 will be connected while Lanes 2 and 3 will remain unconnected.

Table 6-1: 20-Pin eDP Pin Assignment for CCFL Backlight (1 or 2 Lane eDP)

Pin	Signal Name	Description
1	NC - RESERVED	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test or NC	LCD Panel Self Test Enable (optional)
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	NC - RESERVED	RESERVED for LCD manufacturer's use
19	NC - RESERVED	RESERVED for LCD manufacturer's use
20	NC - RESERVED	RESERVED for LCD manufacturer's use

Table 6-2: 30-Pin eDP Pin Assignment for LED Backlight w/o LED Driver on PCB (1 or 2 Lane eDP)

Pin	Signal Name	Description
1	NC - RESERVED	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test or NC	LCD Panel Self Test Enable (optional)
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	NC - RESERVED	RESERVED for LCD manufacturer's use
19	NC - RESERVED	RESERVED for LCD manufacturer's use
20	Vdc1	LED Cathode
21	Vdc2	LED Cathode
22	Vdc3	LED Cathode
23	Vdc4	LED Cathode
24	Vdc5	LED Cathode
25	Vdc6	LED Cathode
26	NC	
27	Vdc	LED Anode
28	Vdc	LED Anode
29	Vdc	LED Anode
30	NC - RESERVED	Reserved for LCD manufacturer's use

Table 6-3: 30-Pin eDP Pin Assignment for LED Backlight with LED Driver on PCB (1 or 2 Lane eDP)

Pin	Signal Name	Description
1	NC - RESERVED	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test or NC	LCD Panel Self-Test Enable (optional)
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_ENABLE or NC	Backlight On/Off (Optional)
23	BL_PWM_DIM or NC	System PWM signal input for dimming (optional)
24	NC - Reserved	Reserved for LCD manufacturer's use
25	NC - Reserved	Reserved for LCD manufacturer's use
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC - RESERVED	Reserved for LCD manufacturer's use

Table 6-4: 40-Pin eDP Pin Assignment for LED Backlight with LED Driver on PCB (up to 4 Lane eDP)

Pin	Signal Name	Description
1	NC - RESERVED	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE or NC	Backlight On/Off (Optional)
33	BL_PWM_DIM or NC	System PWM signal input for dimming (Optional)
34	NC - RESERVED	Reserved for LCD manufacturer's use
35	NC - RESERVED	Reserved for LCD manufacturer's use
36	BL_PWR	Backlight power
37	BL_PWR	Backlight power
38	BL_PWR	Backlight power
39	BL_PWR	Backlight power
40	NC - RESERVED	RESERVED for LCD manufacturer's use

7 Labeling for the eDP Interface

The system and display panel shall include an identification label, or engraving in the chassis, for the DisplayPort interface. Such a warning label or marking shall be located as close to the DisplayPort connector as practical. This will decrease the possibility of connecting an eDP Sink or Source to an LVDS Sink or Source, which may cause damage to either side of the interface.

Pin 1 should also be indicated to prevent inappropriate cable orientation.

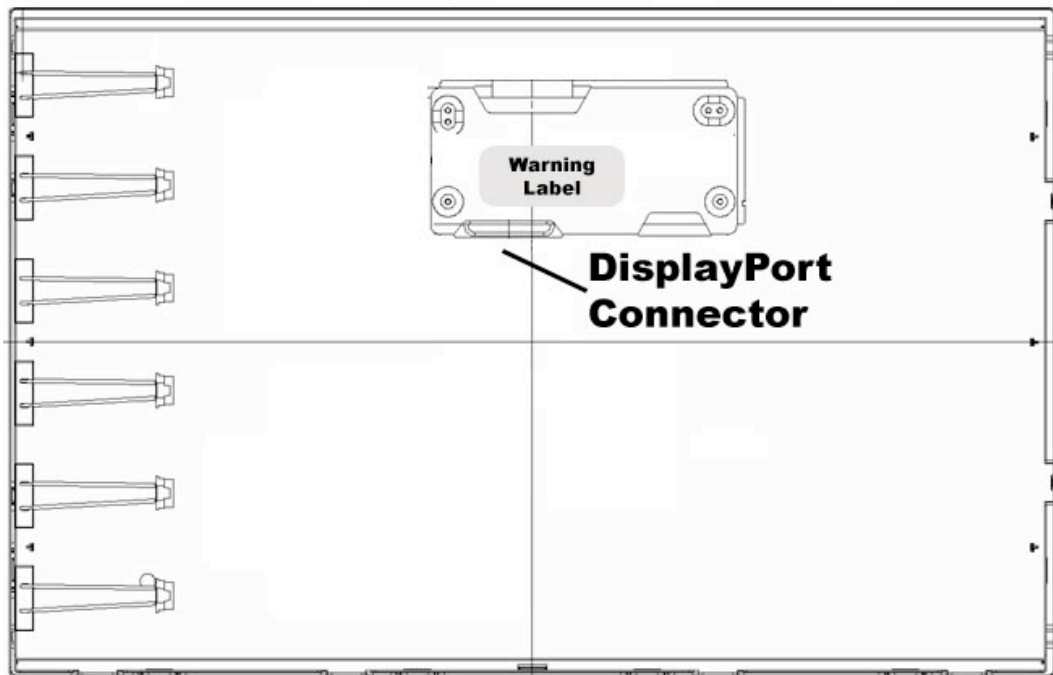


Figure 7-1: Example of VESA DisplayPort Panel Showing Warning Label Affixed Near Connector

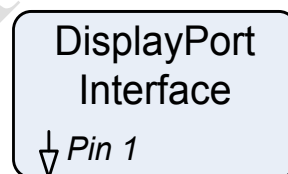


Figure 7-2: Example of a DisplayPort Panel Warning Label

8 Appendix A: Main Contribution History

Table 8-1: Main Contributors to Version 1

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