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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3	9765

27765 7590 02/06/2024
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2138	

NOTIFICATION DATE	DELIVERY MODE
02/06/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	ISSUE DATE	PATENT NO.
17/213,133	06-Feb-2024	11894098

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at https://patentcenter.uspto.gov

The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit https://www.uspto.gov/electronicgrants

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/213,133	02/06/2024	11894098	ETRP0395USA3	9765

27765 7590 01/17/2024

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at https://certifiedcopycenter.uspto.gov/index.html. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (https://patentcenter.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional inventors):

Der-Min Yuan, New Taipei City, TAIWAN;
Yen-An Chang, Miaoli County, TAIWAN;
Wei-Ming Huang, Hsinchu County, TAIWAN;

APPLICANT(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional applicants):

Etron Technology, Inc., Hsinchu, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

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PATENT AND TRADEMARK OFFICE

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/213,133	12/26/2023 08:34:02 PM Z ET	ETRP0395USA3

Title of Invention

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	9765	FILED BY	Anna Lu
PATENT CENTER #	63743502	AUTHORIZED BY	Winston Hsu
CUSTOMER #	27765	FILING DATE	03/25/2021
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Der-Min Yuan

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
DA / 503105	E2023BPK34487002	Anna Lu

PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY
503105	37 CFR 1.16 (National application filing, search, and examination fees); 37 CFR 1.17 (Patent application and reexamination processing fees); 37 CFR 1.19 (Document supply fees); 37 CFR 1.20 (Post Issuance fees); 37 CFR 1.21 (Miscellaneous fees and charges)

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2501	UTILITY ISSUE FEE	480.00	1	480.00
			TOTAL AMOUNT:	$480.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement

Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/213,133	**12/26/2023 08:34:02 PM Z ET**	**ETRP0395USA3**

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CONFIRMATION #	9765	FILED BY	Anna Lu
PATENT CENTER #	63743502	FILING DATE	03/25/2021
CUSTOMER #	27765	FIRST NAMED INVENTOR	Der-Min Yuan
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Winston Hsu

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
5143713.pdf	1	Issue Fee Payment (PTO-85B)	855 KB

Warning: The attached file contains comments or annotations. Comments are not recommended and may cause processing problems with the document.

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
5143713.pdf	61D47B6B7BA68881AFF1D69957CCCA9B4D7B1986F135E1FD B9BAAF1E407A1DD499185C1D4CC34A5254F3F7DD13B63F2A D60B30D391DCF366820EAB5EC76F8894

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New International Application Filed with the USPTO as a Receiving Office

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PART B – FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate ¡§FEE ADDRESS¡¨ for maintenance fee notifications. Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 11/22/2023

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.,
New Taipei City,
Taiwan

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Anna Lu	(Typed or printed name)
/Anna Lu/	(Signature)
12/26/2023	(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3	9765

TITLE OF INVENTION: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	02/22/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2138	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ " Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Winston Hsu
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE or COUNTRY)
Etron Technology, Inc.	Hsinchu, Taiwan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. Fees Submitted: ☑ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment (*Please first reapply any previously paid fee shown above*):

☑ Electronic Payment via Patent Center or EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-3105

5. Change of Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29. NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27. NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status. NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Winston Hsu/ Date 12/25/2023

Typed or printed name Winston Hsu Registration No. 41526

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 11/22/2023
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/22/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3	9765

TITLE OF INVENTION: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	02/22/2024

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

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(Typed or printed name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3	9765

TITLE OF INVENTION: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

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nonprovisional	SMALL	$480	$0.00	$0.00	$480	02/22/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2138	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via the USPTO patent electronic filing system ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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EXAMINER
FARROKH, HASHEM

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DATE MAILED: 11/22/2023

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/213,133	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to amendment filed 08/17/2023.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1,3-5 and 7-11 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION:

2. This office action is in response to the communication(s) filed on 08/17/2023. There are a total of 9 claims pending in the application. Claims 1, 3, 4-5, and 7-10 have been amended; claims 2 and 6 have been canceled; and no new claims have been added.

RESPONSE TO REMARKS:

3. Claims 1, 3-5 and 810 have amended to replace "not greater than" with "lower than" overcomes rejection of the claims under 35 USC § 112(a), first paragraph. In regard to rejection of the claim 1, Examiner respectfully disagree with the Applicant that TAKAHASHI does not teach Peripheral circuit (e.g., Fig. 1 shows the logic circuit includes peripheral circuit). Applicant also argues that TAKAHASHI doe not teach that the first voltage (e.g., core cell voltage) is lower 1.1 V. The Examiner respectfully disagrees, VDD is 1.0 V or lower, which is lower 1.1 V recited in the claim. Applicant make similar arguments regarding the other claims. However, the amendments: the first voltage (e.g., core cell circuit voltage) lower than 1.1 V, the second voltage (e.g., peripheral circuit voltage) lower than 1.1 V, and third voltage (e.g., Input/output circuit voltage) lower than 1.1 V; and the second voltage and third voltage is different from the first voltage overcome the prior art of record.

REASON FOR ALLOWANCE:

4. Claims 1, 3-5, and 7-11 are considered to be allowable.
The reason for allowance of the independent claims are the following: in interpreting the pending claim(s), in view of the specification, the Examiner finds the claimed invention to be patentably distinct from the prior art of record. The prior art of record neither anticipates , nor renders obvious the distinct features recited in the claim as describe below:

The invention directed to A dynamic random access memory (DRAM), comprising: the DRAM comprising a core memory circuit, a peripheral circuit, and an input/output circuit, wherein: the core memory cell circuit operate at a first voltage range lower than 1.1 V, the peripheral circuit operate at a second voltage range lower than 1.1 V, the input/output circuit operate at a third voltage range lower than 1.1 V, the second voltage different from the first voltage, and third voltage is different from the first voltage.

5. Dependent claims 5, 7, and 9-11 are allowable at least for the reasons indicated above including all the limitations of the allowable base claim upon which they depend.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

DIRECTION OF FUTURE CORRESPENDENCES:

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see htto://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	03/09/2022	HF
G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/00	05/15/2023	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE
711	105	03/09/2022	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF
PALM and EAST Inventor Search Updated	04/28/2020	HF
EAST Text Search Updated	04/28/2020	HF
Assignee/ Inventor Search Updated	11/20/2020	HF
EAST Text Search Updated	11/20/2020	HF
Inventor/Assignee Search	03/09/2022	HF
EAST Text Search	03/09/2022	HF
IP Search	03/09/2022	HF
Google Search	03/09/2022	HF
Inventor/Assignee Search Updated	11/07/2022	HF
EAST Text, CPC, Facet Search Updated	11/07/2022	HF
Inventor/Assignee Search Updated	05/15/2023	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

EAST Text, CPC, Facet Search Updated	05/15/2023	HF
Inventor/Assignee Search Updated	11/13/2023	HF
EAST Text, CPC, Facet Search Updated	11/13/2023	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G11C/71075	G11C7/00	11/13/2023	HF
G11C11/4074	G11C11/00	11/13/2023	HF
G06F12/0882	G06F12/00	11/13/2023	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

CPC						
Symbol					**Type**	**Version**
G11C	/	7	/	1075	F	2013-01-01
G11C	/	11	/	4074	I	2013-01-01
G06F	/	12	/	0882	A	2013-01-01
G06F	/	3	/	0653	A	2013-01-01
G06F	/	12	/	0238	A	2013-01-01
G06F	/	13	/	4278	A	2013-01-01
G06F	/	3	/	061	A	2013-01-01
G06F	/	3	/	0656	A	2013-01-01
G06F	/	12	/	0692	A	2013-01-01
G06F	/	12	/	063	A	2013-01-01
G06F	/	12	/	0866	A	2013-01-01
G06F	/	13	/	4221	A	2013-01-01
G11C	/	11	/	40615	A	2013-01-01
Y02D	/	10	/	00	A	2018-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 9	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138 (Primary Examiner)	13 November 2023 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office

Part of Paper No.: 20231113

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G11C	/	7	/	10

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
711	105

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 9	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138 (Primary Examiner)	13 November 2023 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office

Part of Paper No.: 20231113

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	8	10												
	2	9	11												
2	3														
3	4														
4	5														
	6														
5	7														
6	8														
7	9														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 9	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138 (Primary Examiner)	13 November 2023 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office Part of Paper No.: 20231113

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L116	490	(operation$2 near2 voltage) WITH ((lower OR less OR below OR smaller) near2 ("1.1" OR "1.0" OR "0.8" OR one))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 11:25 AM
L117	43	116 AND (DRAM OR DDR$2)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 11:27 AM
L118	17	117 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 11:27 AM
L119	284	116 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 11:43 AM
L120	106	119 AND (memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 11:44 AM
L121	12	(peripheral near2 voltage) WITH ((lower OR less OR below OR smaller OR equal) near2 ("1.1" OR "1.0" OR "0.8" OR one))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 12:03 PM
L122	11	121 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 12:03 PM
L123	7	(peripheral near2 voltage) WITH ((lower OR less OR below OR smaller OR equal) near2 ("1.1" OR "1.0" OR "0.8" OR (one ADJ volt)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 12:05 PM
L124	7	123 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 12:05 PM
L125	4	122 NOT 124	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/12 12:09 PM
L126	1176	((DRAM OR DDR$2 OR ((integrsted ADJ circuit)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/11/13 07:45 AM

		OR IC)) near2 (chip OR die)) WITH ((input$1output OR I$1O) near2 (circuit OR unit OR portion))	JPO; DERWENT; IBM_TDB)				
L127	2961	((DRAM OR DDR$2 OR ((integrsted ADJ circuit) OR IC)) near2 (chip OR die)) WITH ((peripheral) near2 (circuit OR unit OR portion))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 07:46 AM
L128	77	126 AND 127	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 07:46 AM
L129	52	128 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 07:52 AM
L130	432	((DRAM OR DDR$2) near2 (chip OR die OR ((integrsted ADJ circuit) OR IC))) WITH ((peripheral) near2 (circuit OR unit OR portion))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 07:59 AM
L131	256	((DRAM OR DDR$2) near2 (chip OR die OR ((integrsted ADJ circuit) OR IC))) WITH ((input$1output OR I$1O) near2 (circuit OR unit OR portion))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 08:01 AM
L132	32	130 AND 131	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 08:02 AM
L133	22	132 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 08:02 AM
L134	0	((DRAM OR DDR$2) near2 (chip OR die OR ((integrsted ADJ circuit) OR IC))) WITH ((peripheral) near2 (circuit OR unit OR portion)) WITH (voltage near5 ((lower OR less OR smaller OR below) adj2 ("1.1 v" OR (one ADJ volt))))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 12:44 PM
L135	58	((DRAM OR DDR$2) near2 (chip OR die OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/11/13 12:46 PM

		((integrsted ADJ circuit) OR IC))) SAME ((peripheral) near2 (circuit OR unit OR portion)) SAME ((input$1output OR I/$1O) ADJ circuit)	JPO; DERWENT; IBM_TDB)				
L136	1	(((DRAM OR DDR$2) near2 (chip OR die OR ((integrsted ADJ circuit) OR IC))) SAME ((peripheral) near2 (circuit OR unit OR portion)) SAME ((input$1output OR I/$1O) ADJ circuit)).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 12:46 PM
L138	4	135 AND ((Etron ADJ Technology).as.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 12:48 PM
L139	0	136 AND ("CHANG; YEN-AN".ine. OR "HUANG; WEI-MING".ine. OR "YUAN; DER-MIN".ine.)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 12:49 PM
L140	0	136 AND ("CHANG; YEN-AN".ine. OR "HUANG; WEI-MING".ine. OR "YUAN; DER-MIN".ine.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 12:49 PM
L141	7	135 AND ((G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/00).cpc. OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/11/13 12:57 PM

		711/105.ccls. OR (G11C11/4074 OR G11C7/10).ipc.)					

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Bibliographic Data

Application No: 17/213,133

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No | ☐ Met After Allowance

Verified and Acknowledged: /HASHEM FARROKH/ | Examiner's Signature | Initials

Title: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
03/25/2021 **RULE**	711	2138	ETRP0395USA3

APPLICANTS

Etron Technology, Inc., Hsinchu, TAIWAN

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Yen-An Chang, Miaoli County, TAIWAN

Wei-Ming Huang, Hsinchu County, TAIWAN

CONTINUING DATA

This application is a CON of 16151347 10/04/2018 PAT 10998017

16151347 is a CON of 13922242 06/19/2013ABN

13922242 has PRO of 61768406 02/23/2013

13922242 has PRO of 61672287 07/17/2012

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

04/01/2021

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FILING FEE RECEIVED

$830

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Appl. No.	: 17/213,133	Confirmation No.	9765
First Named Inventor	: Der-Min Yuan		
Filed	: March 25, 2021		
TC/A.U.	: 2138		
Examiner	: FARROKH, HASHEM		
Docket No.	: ETRP0395USA3		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of May 18, 2023, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is ~~not greater~~ lower than 1.1V, and

wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell, and wherein the first voltage is different from the second voltage.

2. (Deleted)

3. (currently amended): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is ~~not greater~~ lower than 1.1V;

wherein the first voltage is greater than the second voltage.

4. (currently amended): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell; ~~and~~

an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell, and the input/output circuit is supplied with a third voltage ~~w~~ to make the input/output circuit operate at the third voltage, wherein the third voltage is ~~not greater~~ lower than 1.1V; and

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1V and the first voltage is different from the second voltage;

wherein the DRAM core cell and the input/output circuit are formed on a single chip, and the input/output circuit is external to the DRAM core cell, and wherein the first voltage is different from the third voltage.

5. (currently amended): The dynamic random access memory of claim 4, wherein the first voltage is ~~not greater~~ lower than 1.1V.

6. (Deleted)

7. (currently amended): The dynamic random access memory of claim ~~6~~4, wherein the first voltage is different from the second voltage.

8. (currently amended): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is

supplied with a first voltage to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell; and

an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell, and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage, wherein the third voltage is ~~not greater~~ lower than 1.1V;

wherein the first voltage is greater than the third voltage, and the DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP).

9. (currently amended): The dynamic random access memory of claim 8, wherein the first voltage is ~~not greater~~ lower than 1.1V.

10. (currently amended): The dynamic random access memory of claim 8, further comprising:

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is ~~not greater~~ lower than 1.1V.

11. (previously presented): The dynamic random access memory of claim 10, wherein the first voltage is different from the second voltage.

Electronic Acknowledgement Receipt

EFS ID:	48457706
Application Number:	17213133
International Application Number:	
Confirmation Number:	9765
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Jessie Su
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0395USA3
Receipt Date:	17-AUG-2023
Filing Date:	25-MAR-2021
Time Stamp:	21:53:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	5012777.PDF	841382 91d4e1e3e63c53487d54cd9a7d2ff9e12df7e342	no	8

Warnings:

Information:					
2	Amendment/Request for Reconsideration-After Non-Final Rejection	5012776.PDF	118034 403398fe19bcccc2b60587a9a2cc9b7b004b6f52	no	1
Warnings:					
Information:					
3	Claims	5012775.PDF	124780 9118b9943972cf54c6e3f652cd682db4576eea8e	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	1084196		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Claim Rejections, 35 U.S.C. 112

Response:

After "**not greater than**" cited by the previously presented claims 1, 3-5, 8-10 are replaced with "**lower than**", the currently amended claims 1, 3-5, 8-10 should overcome 35 U.S.C 112(a), or pre-AIA 35 U.S.C. 112, first paragraph.

2. Amendment of Claims:

The previously amended claim 4 is amended according to the previously amended claims 1, 6, and the previously presented claim 6 is canceled and the previously presented claim 7 is amended accordingly. In addition, the previously amended claim 8 is amended according to Table II and paragraph [0015] of the present invention. No new matter is introduced. Allowance of the claim amendments is politely requested.

3. Rejections of claims under 35 U.S.C. 102 & 35 U.S.C. 103:

Response:

In regard to claim 1

35 U.S.C. 102(a)(1) states "A person shall be entitled to a patent unless— (1) the claimed invention **was patented**, **described in a printed publication**, or **in public use**, **on sale, or otherwise available to the public** before the effective filing date of the claimed invention", so according to the above-mentioned statement of 35 U.S.C. 102(a)(1), it is very clear that if the examiner wants to use TAKAHASHI(US20100290300) to reject the previously present claim 1 of the present invention, TAKAHASHI **needs to completely disclose the all technical features** of the previously present claim 1 of the present invention.

Next, please refer to paragraph [0046] of TAKAHASHI. Paragraph [0046] of TAKAHASHI discloses "it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower) **for use in the logic circuit 105**", so according to paragraph [0046] of TAKAHASHI, although TAKAHASHI states that the reduced power supply voltage (e.g., 1.0 V or lower) **can be used in the logic circuit 105** (wherein the examiner holds that **the logic circuit 105 <u>can be referred to</u> the peripheral circuit** of the present invention), TAKAHASHI **<u>does not explicitly state</u>** that the reduced power supply voltage **<u>needs to be lower than 1.0V</u>**. However, according to the above-mentioned statement of 35 U.S.C. 102(a)(1), it is very clear that if the examiner wants to use TAKAHASHI to reject the previously present claim 1 of the present invention, TAKAHASHI **<u>needs to completely disclose the all technical features</u>** of the previously present claim 1 of the present invention, but according to paragraph [0046] of TAKAHASHI, TAKAHASHI **<u>does not explicitly state</u>** that the reduced power supply voltage **<u>needs to be lower than 1.0V</u>**, so TAKAHASHI obviously **fails to** teach the technical feature "**the first voltage is different from the second voltage**" cited by the amended claim 1 of the present invention.

In addition, please refer to paragraph [0078] of TAKAHASHI. Paragraph [0078] of TAKAHASHI discloses "The second exemplary embodiment assumes the case where transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201 are further reduced in film thickness and the **<u>power supply voltage is also further reduced (e.g., VDD is 0.8 V or lower)</u>** as compared with the first exemplary embodiment", so according to paragraph [0078] of TAKAHASHI, TAKAHASHI **<u>only states</u>** that the **<u>power supply voltage is also further reduced (e.g., VDD is 0.8 V or lower)</u>**, but TAKAHASHI **<u>does not explicitly state</u>** that the reduced power supply voltage **(e.g., VDD is 0.8 V or lower) <u>is for only use</u> in the logic circuit 105**. That is, according to paragraph [0078] of TAKAHASHI, the reduced power supply voltage **(e.g., VDD is 0.8 V or lower) <u>can also be for use the cell</u>**

array area 102 (wherein the examiner holds that **the cell array area 102 can be referred to the DRAM core cell** of the present invention). That is, according to paragraph [0078] of TAKAHASHI, TAKAHASHI still **fails to** teach the technical feature "**the first voltage is different from the second voltage**" cited by the amended claim 1 of the present invention. Therefore, the currently amended claim 3 of the present invention **should be obviously patentable over** TAKAHASHI.

In regard to claim 3

According to paragraph [0046] of TAKAHASHI, it is very clear that TAKAHASHI **does not explicitly state** that the reduced power supply voltage **needs to be lower than 1.0V**. However, according to the above-mentioned statement of 35 U.S.C. 102(a)(1), it is very clear that if the examiner wants to use TAKAHASHI to reject the previously present claim 1 of the present invention, TAKAHASHI **needs to completely disclose the all technical features** of the previously present claim 1 of the present invention, but according to paragraph [0046] of TAKAHASHI, TAKAHASHI **does not explicitly state** that the reduced power supply voltage **needs to be lower than 1.0V**, so TAKAHASHI obviously **fails to** teach the technical feature "**the first voltage is greater than the second voltage**" cited by the amended claim 3 of the present invention.

In addition, according to paragraph [0078] of TAKAHASHI, TAKAHASHI **only states** that the **power supply voltage is also further reduced (e.g., VDD is 0.8 V or lower)**, but TAKAHASHI **does not explicitly state** that the reduced power supply voltage **(e.g., VDD is 0.8 V or lower) is for only use in the logic circuit 105**. That is, according to paragraph [0078] of TAKAHASHI, the reduced power supply voltage **(e.g., VDD is 0.8 V or lower) can also be for use the cell array area 102**. That is, according to paragraph [0078] of TAKAHASHI, TAKAHASHI still **fails to** teach the technical feature "**the first voltage is greater than the second voltage**" cited by the amended claim 3 of the present invention. Therefore, the currently amended claim 3 of the present invention **should be obviously patentable over** TAKAHASHI.

In regard to claim 4

According to the above-mentioned arguments of the claim 1, it is very clear that TAKAHASHI **fails to** teach the technical feature "**the first voltage is different from the second voltage**" cited by the amended claim 1 of the present invention. Therefore, after the previously presented claim 6 and the technical feature "**the first voltage is different from the second voltage**" cited by the amended claim 1 of the present invention are merged into the previously presented claim 4, the currently amended claim 4 of the present invention **should be obviously patentable over** TAKAHASHI.

In addition, because the examiner **does not use** Mohammad(US20090122620) to reject the previously presented claim 6, the applicant believes that the currently amended claim 4 of the present invention **should be also obviously patentable over** Mohammad.

In regard to claim 8

Please refer to Table I, Table II, and paragraphs [0011-0012], [0015] of the present invention. Paragraphs [0011-0012] of the present invention disclose "Please refer to the figure. The figure is a diagram illustrating a **<u>dynamic random access memory 100 applied to an embedded display port</u>** according to an embodiment … **Table I** illustrates **<u>operation voltages</u>** (specified by the Joint Electron Device Engineering Council (JEDEC)) of a dynamic random access memory operating in the DDR I specification, a low power DDR I specification, the DDR II specification, and a low power DDR II specification … But, **the operation voltages** specified by the Joint Electron Device Engineering Council (as shown in Table I) **<u>cannot satisfy requirements</u> (that is, <u>the low operation power consumption and the low standby power consumption)</u> of the embedded display port (eDP) version 1.3**", and paragraph [0015] of the present invention discloses "As shown in Table II, because **the operation voltages of <u>the memory core unit 102</u>** in the DDR I specification, the low power DDR I specification, the DDR II specification, and the low power DDR II specification **<u>are the first predetermined voltage</u>**, **the dynamic random access memory 100 <u>has lower memory core power consumption</u>**; because the **operation**

voltages of **the peripheral circuit unit 104** in the DDR I specification, the low power DDR I specification, the DDR II specification, and the low power DDR II specification **are the second predetermined voltage**, **the dynamic random access memory 100** **has lower access power consumption**…**so power consumption of the dynamic random access memory 100** **is much lower than** **power consumption of the dynamic random access memory operating in the operation voltages** specified by the Joint Electron Device Engineering Council", so according to Table I, Table II, and paragraphs [0011-0012], [0015] of the present invention, it is very obvious that **the DRAM 100** provided by the present invention is **only used for solving the problem that the operation voltages** (shown in Table I) **of a DRAM** specified by Joint Electron Device Engineering Council (JEDEC) **cannot satisfy the requirements of the embedded display port (eDP) version 1.3**. Therefore, Table II and paragraph [0015] of the present invention **obviously teach** the technical feature "**the DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP)**". Table I and Table II of the present invention are shown as follows:

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
DDR I	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V
Low Power DDR I	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
DDR II	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
Low Power DDR II	1.7V~1.95V	1.14V~1.30V	1.14V~1.30V

Table I

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	< 1.1V	< 1.1V	< 1.1V

Table II

However, please refer to paragraph [0004] of Mohammad (US20090122620). Paragraph [0004] of Mohammad discloses "**One problem with increased usage of SRAM in computing devices is that accesses to such memory incurs power usage that may affect the battery life of the computing device. One problem in decreasing power usage of the SRAM includes a decreased access success rate of the memory**", so according to paragraph [0004] of Mohammad, it is very obvious that Mohammad is **not used for providing a DRAM applied to the embedded display port (eDP) version 1.3**.

In addition, please refer to paragraph [0021] of TAKAHASHI. Paragraph [0021] of TAKAHASHI discloses "The present inventors have found **a problem as described below**. In the technique disclosed in Patent Document 1, a **thick-film transistor is used as a central transistor of a memory cell, and a thin-film transistor, which is used for a logic circuit, is used as a precharge MOS transistor and a sense amplifier**. Patent Document 1 discloses that a **high voltage is not applied to** the **precharge MOS transistor which is formed of a thin-film transistor**. However, unless a **voltage higher than** the power supply voltage as in the semiconductor memory circuit 1 is applied to the transistor for use in the precharge circuit, **the operation speed of the precharge circuit cannot be increased**. Accordingly, the present inventors have found **a problem** that the **semiconductor integrated device** fabricated using the technique as **disclosed in Patent Document 1 has a limitation in achieving a higher speed operation**", so according to paragraph [0021] of TAKAHASHI, TAKAHASHI is very obviously **used for solving a problem** of **Patent Document 1 having a limitation in achieving a higher speed operation**, that is, TAKAHASHI is **also not used for providing a DRAM applied to the embedded display port (eDP) version 1.3**.

Therefore, because according to paragraph [0004] of Mohammad, Mohammad is **not used for providing a DRAM applied to the embedded display port (eDP) version 1.3**, and according to paragraph [0021] of TAKAHASHI, TAKAHASHI **is also not used**

for providing a DRAM applied to the embedded display port (eDP) version 1.3, it is very obvious that both Mohammad and TAKAHASHI **obviously fail to teach** the technical feature "**the DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP)**" disclosed by Table II and paragraph [0015] of the present invention.

Therefore, because both Mohammad and TAKAHASHI obviously **fail to teach** the technical feature "**the DRAM operating with the first voltage and the third voltage is capable of being applied to an embedded display port (eDP)**" disclosed by Table II and paragraph [0015] of the present invention, the currently amended claim 8 of the present invention should be patentable over Mohammad and TAKAHASHI after the previously presented claim 8 of the present invention is amended according to the above-mentioned technical feature disclosed by Table II and paragraph [0015] of the present invention.

To sum up, allowance of the currently amended claims 1, 3-5, 7-10 and the previously presented claim 11 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Winston Hsu/ Date: 08/17/2023

Winston Hsu, Patent Agent No. 41,526
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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time and DST 12 hours behind.)

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/213,133	Filing Date 03/25/2021	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	08/17/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 9	Minus	** 20	= 0		x $40 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $192 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/DENISE HOPKINS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3	9765

27765 7590 05/26/2023
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2138	

NOTIFICATION DATE	DELIVERY MODE
05/26/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 17/213,133	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 04/14/2023.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 and 3-11 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 and 3-11 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 03/25/2021 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
17/213,133	03/25/2021	Yuan et al.	ETRP0395USA3

		EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION **5F., NO.389, FUHE RD., YONGHE DIST.** **NEW TAIPEI CITY,**		HASHEM FARROKH	
		ART UNIT	**PAPER**
		2138	20230522

DATE MAILED: _____

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The purpose of this communication is to inform the applicant that Office Action mailed on 05/18/2023 is a non-final office action. The Conclusion portion (e.g., pages 16-17) of the Office Action mailed is 05/18/2023 erroneously indicated that the Office Action is final, which is being corrected by this communication(s).

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

PTO-90C (Rev.04-03)

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/14/2023 has been entered.

3. This Office action is in response to the communication(s) filed on 04/14/2023. There are a total of 10 claims pending in the application. Claims 1 and 3 have been amended, claim 2 has been canceled; and claims 4-11 have been added.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*4. As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> *(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.*

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

1. Claims 1 and 3-11 rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

1.0 v

2. Claims 1, 3, 6, and 10 recite, in part, the limitation:

"wherein the second voltage is not greater than 1.1V"

The claimed specification does not appear to describe/define the above limitation as claimed. Claims 7 and 11 are rejected by virtue of their dependency from claims 6 and 10, respectively.

3. Claims 4 and 8 recite, in part, the limitation:

"wherein the third voltage is not greater than 1.1V"

The claimed specification does not appear to describe/define the above limitation as claimed. Claims 5-7 and 9-11 are rejected by virtue of their dependency from claims 4 and 8, respectively.

4. Claims 5 and 9 recite, in part, the limitation:

"wherein the first voltage is not greater than 1.1V"

The claimed specification does not appear to describe/define the above limitation as claimed.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.*

Claims 1 and 3 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by TAKAHASHI et al. "TAKAHASHI" (US 2010/0290300 A1).

4. In regard to claim 1 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100)**, comprising: a DRAM core cell comprised in the DRAM **(e.g., cell array 102 in Fig. 1)**, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V;" **(e.g., Fig. 2, ¶¶ 0048-0049; Figs. 2 and 3, ¶ 0046, it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower)}.** *Cell array area 102 (e.g., core) shows memory CELL101 and CELL 102, with drain each transistor in memory cells connected to bit-line D and DB, respectively. Fig. 4A shows the bit line D set at VDD power supply value 1.0V.*

"and a peripheral circuit comprised in the DRAM **(e.g., Abstract, provided is a semiconductor integrated device including a semiconductor memory circuit and a peripheral circuit of the semiconductor memory circuit; claim 7, the peripheral circuit is a logic circuit that includes an address decoder of the semiconductor memory circuit),** wherein the peripheral circuit is electrically connected to DRAM core cell **(e.g., ¶ 0081, in response to word signals WL201, WL202, . . . , the gate transistors Tr of the memory cells CELL201, CELL202, . . . are activated)**, and the

peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V," **[(e.g., ¶ 0078, the logic circuit 105 serving as a peripheral circuit… further reduced (e.g., VDD is 0.8 V or lower)].** *The logic circuit or peripheral 105, shown in Fig. 1, comprises decoder (e.g., address decoder), which is connected to the gate of transistors in cell array (e.g., DRAM core), see Fig. 2 of TAKAHASHI.*

"and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell," **(e.g., Fig. 1, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100. The semiconductor memory circuit 101 holds data or the like to be processed in the logic circuit 105).**

"and wherein the first voltage is different from the second voltage." **[e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, (e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1). The two voltages are different.*

5. In regard to claim 3 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100)**, comprising: a DRAM core cell comprised in the DRAM **(e.g., ell array 102 in Fig. 1)**, wherein the DRAM core cell is supplied with a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is volatile memory cell,

wherein the first voltage is lower than 1.1 V; " **(e.g., Fig. 2, ¶¶ 0048-0049; Figs. 2 and 3, ¶ 0046, it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower)).** *Cell array area 102 (e.g., core) shows memory CELL101 and CELL 102, with drain each transistor in memory cells connected to bit-line D and DB, respectively. Fig. 4A shows the bit line D set at VDD power supply value 1.0V.*

"and a peripheral circuit comprised in the DRAM **(e.g., Abstract, provided is a semiconductor integrated device including a semiconductor memory circuit and a peripheral circuit of the semiconductor memory circuit; claim 7, the peripheral circuit is a logic circuit that includes an address decoder of the semiconductor memory circuit)**, wherein the peripheral circuit electrically connected to the DRAM core cell **(e.g., ¶ 0081, in response to word signals WL201, WL202, . . . , the gate transistors Tr of the memory cells CELL201, CELL202…are activated),** and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1 V;" **[(e.g., ¶ 0078, the logic circuit 105 serving as a peripheral circuit… further reduced (e.g., VDD is 0.8 V or lower)].** *The logic circuit or peripheral 105, shown in Fig. 1, comprises decoder (e.g., address decoder), which is connected to the gate of transistors in cell array (e.g., DRAM core), see Fig. 2 of TAKAHASHI.*

"wherein the **first voltage is greater than the second voltage**." **[e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, (e.g., VDD is 0.8 V or lower)].** *The different supply voltage ranges (e.g., 1.0 V vs 0.8 V).*

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.*

Claims 4-11 are rejected under 35 U.S.C. 103 as being unpatentable over TAKAHASHI in view of Mohammad "Mohammad" (US 2009/0122620 A1).

6. In regard to claim 4 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100)**, comprising: a DRAM core cell comprised in the DRAM," **(e.g., cell array 102 in Fig. 1)**.

"wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell;" **[e.g., Fig.**

2, ¶¶ 0048-0049; Figs. 2 and 3, ¶ 0046, it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower)]. *Cell array area 102 (e.g., core) shows memory CELL101 and CELL 102, with drain each transistor in memory cells connected to bit-line D and DB, respectively. Fig. 4A shows the bit line D set at VDD power supply value 1.0V. However, TAKAHASHI does not expressly teach while Mohammad discloses:*

"an input/output circuit comprised in the DRAM **(e.g., Fig. 1, ¶ 0025, While the inventive concepts are described as being included in SRAM, the inventive concepts may be included in other types of memory including, but not limited to, SDRAM; Fig. 5, ¶ 0049, MUX/Demux Input/Output logic 516)** wherein the input/output circuit is electrically connected to the DRAM core cell **(e.g., memory cells 512 in Fig. 5 or 6 is electrically connected I/O logic 512)**, and the input/output circuit is supplied with a third voltage w to make the input/output circuit operate at the third voltage, wherein the third voltage is not greater than 1.1V;" **(e.g., Figs. 5-6, ¶ 0049, MUX/Demux Input/Output logic 516; ¶ 0051, a power rail to be received by logic 504 and 516 may be set to 0.8 v instead of 1.0 v).**

and wherein the DRAM core cell and the input/output circuit are formed on a single chip **(e.g., Fig. 6, ¶ 0051, on-chip components)**, and the input/output circuit is external to the DRAM core cell," **(e.g., Fig. 6, ¶ 0051).** *The block 516 comprising I/O logic 516, which is external to memory cells 502.*

"and wherein the first voltage is different from the third voltage." **(e.g., Fig. 1, ¶ 0025, the inventive concepts may be included in other types of memory including, but**

not limited to, SDRAM; Fig. 6, ¶ 0051, a power rail to be received by logic 504 and 516 may be set to 0.8 v instead of 1.0 v). *The first (e.g., core) voltage Vdd =1.0 v is reduced to 0.8 v for third (e.g., Input/Output logic) voltage. The two voltages are different.*

Disclosures by TAKAHASHI and Mohammad are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the Semiconductor Integrated Device taught by TAKAHASHI to include the Input/Output circuit disclosed by Mohammad.

The motivation for including the Input/Output circuit as taught by paragraph [0002] of Mohammad is to provide low power, high yield memory.

Therefore, it would have been obvious to combine teaching of Mohammad with TAKAHASHI to obtain the invention as specified in the claim.

7. In regard to claim 5 TAKAHASHI further teaches:

"wherein the first voltage is not greater than 1.1V." **(e.g., ¶ 0046; VDD power supply 1.0 V or lower).** *The VDD of 1.0 V for DRAM memory cells (e.g., core) is not greater than 1.1 V.*

8. In regard to claim 6 TAKAHASHI further teaches:

"a peripheral circuit comprised in the DRAM **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device**

100), wherein the peripheral circuit is electrically connected to the DRAM core cell (e.g., ¶ 0081, in response to **word signals WL201, WL202, . . . , the gate transistors Tr of the memory cells CELL201, CELL202…are activated)**, and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V." [e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, **(e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1) comprising peripheral circuit (e.g., the second voltage). The second voltage (e.g., peripheral circuit voltage of 0.8 V is not greater 1.1 V.*

9. In regard to claim 7 TAKAHASHI further teaches:

"wherein the first voltage is different from the second voltage." [e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, **(e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1). The two voltages are different.*

10. In regard to claim 8 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) (e.g., Figs. 1-2, ¶ 0047, **semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100**), comprising: a DRAM core cell comprised in the DRAM (e.g., ell array 102 in Fig. 1), wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell;" (e.g., Fig. 2, ¶ 00 47, **semiconductor memory circuit 101 is a built-in DRAM of the**

semiconductor integrated device 100; Fig. 2, ¶¶ 0048-0049; Figs. 2 and 3, ¶ 0046, **it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower)**).

However, TAKAHASHI does not expressly teach while Mohammad discloses:

"an input/output circuit comprised in the DRAM (e.g., Fig. 1, ¶ 0025, **While the inventive concepts are described as being included in SRAM, the inventive concepts may be included in other types of memory including, but not limited to, SDRAM;** Fig. 5, ¶ 0049, **MUX/Demux Input/Output logic 516)** wherein the input/output circuit is electrically connected to the DRAM core cell (e.g., I/O logic 516 electrically connected to memory cells 512 in Fig. 5), and the input/output circuit is supplied with a third voltage w to make the input/output circuit operate at the third voltage, wherein the third voltage is not greater than 1.1V;" (e.g., Figs. 5-6, ¶ 0049, **MUX/Demux Input/Output logic 516**; ¶ 0051, **a power rail to be received by logic 504 and 516 may be set to 0.8 v instead of 1.0 v).**

"wherein the first voltage is greater than the third voltage." (e.g., Figs. 5-6, ¶ 0049, **MUX/Demux Input/Output logic 516**; ¶ 0051, **a power rail to be received by logic 504 and 516 may be set to 0.8 v instead of 1.0 v)** *the VDD of 1.0 V for memory core (e.g., the first voltage) is reduced to 0.8 V for Input/Output logic (e.g., the third voltage). The first voltage (e.g., VDD=1.0 V) is greater than 0.8 V set for Input/Output logic. The motivation for combining is based on the same rational presented for rejection of claim 4.*

11. In regard to claim 9 TAKAHASHI further teaches:

"wherein the first voltage is not greater than 1.1V." **(e.g., ¶ 0046; VDD power supply 1.0 V or lower).** *The VDD of 1.0 V for DRAM memory cells (e.g., core) is not greater than 1.1 V.*

12. In regard to claim 10 TAKAHASHI further teaches:

"a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell **(e.g., ¶ 0081, in response to word signals WL201, WL202, . . . , the gate transistors Tr of the memory cells CELL201, CELL202…are activated)**, and the peripheral circuit is 15 supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V." **[e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, (e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1) comprising peripheral circuit (e.g., the second voltage). The second voltage (e.g., peripheral circuit voltage of 0.8 V is not greater 1.1 V.*

13. In regard to claim 11 TAKAHASHI further teaches:

"wherein the first voltage is different from the second voltage."." **[e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, (e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1). The two voltages are different.*

Response to Remarks

Applicant arguments have been fully considered but they are not persuasive. On page 4 of the Remarks, Applicant makes references to paragraph [0078] and Figs. 1 and 7 of TAKAHASHI and states:

"Therefore, according to FIG. 1 and paragraph [0078] of TAKAHASHI, because the logic circuit 105 is not included in the semiconductor memory circuit 101, **it is obvious that the logic circuit 105 of TAKAHASHI does not disclose the peripheral cir**cuit of the currently amended claim 1" *(emphasis added).*

TAKAHASHI teaches:

"[0078] The semiconductor integrated device 200 includes **the semiconductor memory circuit 201 and the logic circuit 105**. The semiconductor memory circuit 201 is a built-in DRAM of a system LSI, as with the first exemplary embodiment. The **second exemplary embodiment assumes the case where transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201** are further reduced in film thickness and the power supply voltage is also further reduced (e.g., VDD is 0.8 V or lower) as compared with the first exemplary embodiment." *(Emphasis added).*

Fig. 4 of TAKAHASHI discloses that the logic circuit 5, shown in Fig. 1 comprises decoder. TAKAHASHI further teaches the logic circuit 105 includes … logic gate for performing address decoder of the semiconductor memory circuit 1 (e.g., see paragraph 0044 of TAKAHASHI).

TAKAHASHI clearly teaches that transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory (e.g., circuit 101 in Fig. 2 or circuit 201 in Fig. 7 of TAKAHASHI).

Claim 1 of TAKAHASHI, in part recites:

"1. A semiconductor integrated device comprising: a semiconductor memory circuit; and **a peripheral circuit of the semiconductor memory circuit**…" *(Emphasis added).*

Furthermore, the Examiner notes, the instant specification do not describe what constitutes a peripheral circuit.

Paragraph [0047] of TAKAHASHI further teaches:

"[0047] **The semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100**. The semiconductor memory circuit 101 holds data or the like to be processed in the logic circuit 105. As shown in FIG. 1, the semiconductor memory circuit 101 includes a cell array area 102, a sense amplifier area 103, and a driver area 104. FIG. 2 shows an exemplary circuit configuration of the semiconductor memory circuit 101. In the first exemplary embodiment, the semiconductor memory circuit 101 shown in FIG. 2 is illustrated as a DRAM circuit including a pair of bit lines in order to simplify the drawings. **The semiconductor memory circuit 101 may have a configuration including** multiple pairs of bit lines, memory cells connected to the multiple pairs of bit lines, a **sense amplifier**, and a **precharge circuit**. Further, the semiconductor memory circuit 101 is not limited to a DRAM, but may be an SRAM, for example." *(Emphasis added).*

As shown in Fig. 2 of TAKAHASHI the sense amplifier SA101 and precharge circuit PDLU101 are included within the integrated memory device 101.

Therefore, the Examiner respectfully submits that TAKAHASHI teaches or anticipates all limitations recited in the independent claim 1. Accordingly, the Examiner maintains his position. Disclosure of Mohammad has been added to expressly teach that the logic circuit includes Input/Output logic or circuit of semiconductor memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

Monday, May 22, 2023

Notice of References Cited	Application/Control No. 17/213,133	Applicant(s)/Patent Under Reexamination Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20090122620-A1	05-2009	Mohammad; Baker	G11C5/14	365/189.11
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	03/09/2022	HF
G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/00	05/15/2023	HF

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE
711	105	03/09/2022	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

Search Notes		
Search Notes	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF
PALM and EAST Inventor Search Updated	04/28/2020	HF
EAST Text Search Updated	04/28/2020	HF
Assignee/ Inventor Search Updated	11/20/2020	HF
EAST Text Search Updated	11/20/2020	HF
Inventor/Assignee Search	03/09/2022	HF
EAST Text Search	03/09/2022	HF
IP Search	03/09/2022	HF
Google Search	03/09/2022	HF
Inventor/Assignee Search Updated	11/07/2022	HF
EAST Text, CPC, Facet Search Updated	11/07/2022	HF
Inventor/Assignee Search Updated	05/15/2023	HF
EAST Text, CPC, Facet Search Updated	EAST Text, CPC, Facet Search Updated	HF

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/09/2022	11/07/2022							
	1	✓	✓							
	2	✓	-							
	3	✓	✓							
	4		✓							
	5		✓							
	6		✓							
	7		✓							
	8		✓							
	9		✓							
	10		✓							
	11		✓							

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3	9765

27765 7590 05/18/2023
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EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2138	

NOTIFICATION DATE	DELIVERY MODE
05/18/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 17/213,133	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 04/14/2023.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 and 3-11 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 and 3-11 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 03/25/2021 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/14/2023 has been entered.

3. This Office action is in response to the communication(s) filed on 04/14/2023. There are a total of 10 claims pending in the application. Claims 1 and 3 have been amended, claim 2 has been canceled; and claims 4-11 have been added.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*4. As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by*

M.P.E.P. 707.05 *and* ***904*** *and as stated in* ***M.P.E.P. 2001.06(b),*** *no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> *(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.*

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

1. Claims 1 and 3-11 rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

1.0 v

2. Claims 1, 3, 6, and 10 recite, in part, the limitation:

"wherein the second voltage is not greater than 1.1V"

The claimed specification does not appear to describe/define the above limitation as claimed. Claims 7 and 11 are rejected by virtue of their dependency from claims 6 and 10, respectively.

3. Claims 4 and 8 recite, in part, the limitation:

"wherein the third voltage is not greater than 1.1V"

The claimed specification does not appear to describe/define the above limitation as claimed. Claims 5-7 and 9-11 are rejected by virtue of their dependency from claims 4 and 8, respectively.

4. Claims 5 and 9 recite, in part, the limitation:

"wherein the first voltage is not greater than 1.1V"

The claimed specification does not appear to describe/define the above limitation as claimed.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.*

Claims 1 and 3 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by TAKAHASHI et al. "TAKAHASHI" (US 2010/0290300 A1).

4. In regard to claim 1 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100)**, comprising: a DRAM core cell comprised in the DRAM **(e.g., cell array 102 in Fig. 1)**, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V;" **(e.g., Fig. 2, ¶¶ 0048-0049; Figs. 2 and 3, ¶ 0046, it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower)}.** *Cell array area 102 (e.g., core) shows memory CELL101 and CELL 102, with drain each transistor in memory cells connected to bit-line D and DB, respectively. Fig. 4A shows the bit line D set at VDD power supply value 1.0V.*

"and a peripheral circuit comprised in the DRAM **(e.g., Abstract, provided is a semiconductor integrated device including a semiconductor memory circuit and a peripheral circuit of the semiconductor memory circuit; claim 7, the peripheral circuit is a logic circuit that includes an address decoder of the semiconductor memory circuit),** wherein the peripheral circuit is electrically connected to DRAM core cell **(e.g., ¶ 0081, in response to word signals WL201, WL202, . . . , the gate transistors Tr of the memory cells CELL201, CELL202, . . . are activated)**, and the

peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V," **[(e.g., ¶ 0078, the logic circuit 105 serving as a peripheral circuit… further reduced (e.g., VDD is 0.8 V or lower)].** *The logic circuit or peripheral 105, shown in Fig. 1, comprises decoder (e.g., address decoder), which is connected to the gate of transistors in cell array (e.g., DRAM core), see Fig. 2 of TAKAHASHI.*

"and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell," **(e.g., Fig. 1, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100. The semiconductor memory circuit 101 holds data or the like to be processed in the logic circuit 105).**

"and wherein the first voltage is different from the second voltage." **[e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, (e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1). The two voltages are different.*

5. In regard to claim 3 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100)**, comprising: a DRAM core cell comprised in the DRAM **(e.g., ell array 102 in Fig. 1)**, wherein the DRAM core cell is supplied with a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is volatile memory cell,

wherein the first voltage is lower than 1.1 V; " **(e.g., Fig. 2, ¶¶ 0048-0049; Figs. 2 and 3, ¶ 0046, it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower)).** *Cell array area 102 (e.g., core) shows memory CELL101 and CELL 102, with drain each transistor in memory cells connected to bit-line D and DB, respectively. Fig. 4A shows the bit line D set at VDD power supply value 1.0V.*

"and a peripheral circuit comprised in the DRAM **(e.g., Abstract, provided is a semiconductor integrated device including a semiconductor memory circuit and a peripheral circuit of the semiconductor memory circuit; claim 7, the peripheral circuit is a logic circuit that includes an address decoder of the semiconductor memory circuit)**, wherein the peripheral circuit electrically connected to the DRAM core cell **(e.g., ¶ 0081, in response to word signals WL201, WL202, . . . , the gate transistors Tr of the memory cells CELL201, CELL202…are activated),** and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1 V;" **[(e.g., ¶ 0078, the logic circuit 105 serving as a peripheral circuit… further reduced (e.g., VDD is 0.8 V or lower)].** *The logic circuit or peripheral 105, shown in Fig. 1, comprises decoder (e.g., address decoder), which is connected to the gate of transistors in cell array (e.g., DRAM core), see Fig. 2 of TAKAHASHI.*

"wherein the **first voltage is greater than the second voltage**." **[e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, (e.g., VDD is 0.8 V or lower)].** *The different supply voltage ranges (e.g., 1.0 V vs 0.8 V).*

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.*

Claims 4-11 are rejected under 35 U.S.C. 103 as being unpatentable over TAKAHASHI in view of Mohammad "Mohammad" (US 2009/0122620 A1).

6. In regard to claim 4 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100)**, comprising: a DRAM core cell comprised in the DRAM," **(e.g., cell array 102 in Fig. 1)**.

"wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell;" **[e.g., Fig.**

2, ¶¶ 0048-0049; Figs. 2 and 3, ¶ 0046, it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower)]. *Cell array area 102 (e.g., core) shows memory CELL101 and CELL 102, with drain each transistor in memory cells connected to bit-line D and DB, respectively. Fig. 4A shows the bit line D set at VDD power supply value 1.0V. However, TAKAHASHI does not expressly teach while Mohammad discloses:*

"an input/output circuit comprised in the DRAM **(e.g., Fig. 1, ¶ 0025, While the inventive concepts are described as being included in SRAM, the inventive concepts may be included in other types of memory including, but not limited to, SDRAM; Fig. 5, ¶ 0049, MUX/Demux Input/Output logic 516)** wherein the input/output circuit is electrically connected to the DRAM core cell **(e.g., memory cells 512 in Fig. 5 or 6 is electrically connected I/O logic 512)**, and the input/output circuit is supplied with a third voltage w to make the input/output circuit operate at the third voltage, wherein the third voltage is not greater than 1.1V;" **(e.g., Figs. 5-6, ¶ 0049, MUX/Demux Input/Output logic 516; ¶ 0051, a power rail to be received by logic 504 and 516 may be set to 0.8 v instead of 1.0 v).**

and wherein the DRAM core cell and the input/output circuit are formed on a single chip **(e.g., Fig. 6, ¶ 0051, on-chip components)**, and the input/output circuit is external to the DRAM core cell," **(e.g., Fig. 6, ¶ 0051).** *The block 516 comprising I/O logic 516, which is external to memory cells 502.*

"and wherein the first voltage is different from the third voltage." **(e.g., Fig. 1, ¶ 0025, the inventive concepts may be included in other types of memory including, but**

not limited to, SDRAM; Fig. 6, ¶ 0051, a power rail to be received by logic 504 and 516 may be set to 0.8 v instead of 1.0 v). *The first (e.g., core) voltage Vdd =1.0 v is reduced to 0.8 v for third (e.g., Input/Output logic) voltage. The two voltages are different.*

Disclosures by TAKAHASHI and Mohammad are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the Semiconductor Integrated Device taught by TAKAHASHI to include the Input/Output circuit disclosed by Mohammad.

The motivation for including the Input/Output circuit as taught by paragraph [0002] of Mohammad is to provide low power, high yield memory.

Therefore, it would have been obvious to combine teaching of Mohammad with TAKAHASHI to obtain the invention as specified in the claim.

7. In regard to claim 5 TAKAHASHI further teaches:

"wherein the first voltage is not greater than 1.1V." **(e.g., ¶ 0046; VDD power supply 1.0 V or lower).** *The VDD of 1.0 V for DRAM memory cells (e.g., core) is not greater than 1.1 V.*

8. In regard to claim 6 TAKAHASHI further teaches:

"a peripheral circuit comprised in the DRAM **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device**

100), wherein the peripheral circuit is electrically connected to the DRAM core cell (e.g., ¶ 0081, in response to **word signals WL201, WL202, . . . , the gate transistors Tr of the memory cells CELL201, CELL202…are activated)**, and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V." [e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, **(e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1) comprising peripheral circuit (e.g., the second voltage). The second voltage (e.g., peripheral circuit voltage of 0.8 V is not greater 1.1 V.*

9. In regard to claim 7 TAKAHASHI further teaches:

"wherein the first voltage is different from the second voltage." [e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, **(e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1). The two voltages are different.*

10. In regard to claim 8 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) (e.g., Figs. 1-2, ¶ 0047, **semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100**), comprising: a DRAM core cell comprised in the DRAM (e.g., ell array 102 in Fig. 1), wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell;" (e.g., Fig. 2, ¶ 00 47, **semiconductor memory circuit 101 is a built-in DRAM of the**

semiconductor integrated device 100; Fig. 2, ¶¶ 0048-0049; Figs. 2 and 3, ¶ 0046, **it is assumed that the power supply voltage VDD according to the first exemplary embodiment is equal to a reduced power supply voltage (e.g., 1.0 V or lower)**).

However, TAKAHASHI does not expressly teach while Mohammad discloses:

"an input/output circuit comprised in the DRAM (e.g., Fig. 1, ¶ 0025, **While the inventive concepts are described as being included in SRAM, the inventive concepts may be included in other types of memory including, but not limited to, SDRAM;** Fig. 5, ¶ 0049, **MUX/Demux Input/Output logic 516)** wherein the input/output circuit is electrically connected to the DRAM core cell (e.g., I/O logic 516 electrically connected to memory cells 512 in Fig. 5), and the input/output circuit is supplied with a third voltage w to make the input/output circuit operate at the third voltage, wherein the third voltage is not greater than 1.1V;" (e.g., Figs. 5-6, ¶ 0049, **MUX/Demux Input/Output logic 516**; ¶ 0051, **a power rail to be received by logic 504 and 516 may be set to 0.8 v instead of 1.0 v).**

"wherein the first voltage is greater than the third voltage." (e.g., Figs. 5-6, ¶ 0049, **MUX/Demux Input/Output logic 516**; ¶ 0051, **a power rail to be received by logic 504 and 516 may be set to 0.8 v instead of 1.0 v)** *the VDD of 1.0 V for memory core (e.g., the first voltage) is reduced to 0.8 V for Input/Output logic (e.g., the third voltage). The first voltage (e.g., VDD=1.0 V) is greater than 0.8 V set for Input/Output logic. The motivation for combining is based on the same rational presented for rejection of claim 4.*

11. In regard to claim 9 TAKAHASHI further teaches:

"wherein the first voltage is not greater than 1.1V." **(e.g., ¶ 0046; VDD power supply 1.0 V or lower).** *The VDD of 1.0 V for DRAM memory cells (e.g., core) is not greater than 1.1 V.*

12. In regard to claim 10 TAKAHASHI further teaches:

"a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell **(e.g., ¶ 0081, in response to word signals WL201, WL202, . . . , the gate transistors Tr of the memory cells CELL201, CELL202…are activated)**, and the peripheral circuit is 15 supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V." **[e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, (e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1) comprising peripheral circuit (e.g., the second voltage). The second voltage (e.g., peripheral circuit voltage of 0.8 V is not greater 1.1 V.*

13. In regard to claim 11 TAKAHASHI further teaches:

"wherein the first voltage is different from the second voltage."." **[e.g., ¶ 0046, reduced power supply voltage VDD (e.g., 1.0 V or lower); ¶ 0078, (e.g., VDD is 0.8 V or lower)].** *The VDD supply of 1.0 V for memory cells (e.g., core) reduce to 0.8 V for logic circuit 105 (Fig. 1). The two voltages are different.*

Response to Remarks

Applicant arguments have been fully considered but they are not persuasive. On page 4 of the Remarks, Applicant makes references to paragraph [0078] and Figs. 1 and 7 of TAKAHASHI and states:

"Therefore, according to FIG. 1 and paragraph [0078] of TAKAHASHI, because the logic circuit 105 is not included in the semiconductor memory circuit 101, **it is obvious that the logic circuit 105 of TAKAHASHI does not disclose the peripheral cir**cuit of the currently amended claim 1" *(emphasis added).*

TAKAHASHI teaches:

"[0078] The semiconductor integrated device 200 includes **the semiconductor memory circuit 201 and the logic circuit 105**. The semiconductor memory circuit 201 is a built-in DRAM of a system LSI, as with the first exemplary embodiment. The **second exemplary embodiment assumes the case where transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201** are further reduced in film thickness and the power supply voltage is also further reduced (e.g., VDD is 0.8 V or lower) as compared with the first exemplary embodiment." *(Emphasis added).*

Fig. 4 of TAKAHASHI discloses that the logic circuit 5, shown in Fig. 1 comprises decoder. TAKAHASHI further teaches the logic circuit 105 includes … logic gate for performing address decoder of the semiconductor memory circuit 1 (e.g., see paragraph 0044 of TAKAHASHI).

TAKAHASHI clearly teaches that transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory (e.g., circuit 101 in Fig. 2 or circuit 201 in Fig. 7 of TAKAHASHI).

Claim 1 of TAKAHASHI, in part recites:

"1. A semiconductor integrated device comprising: a semiconductor memory circuit; and **a peripheral circuit of the semiconductor memory circuit**…" *(Emphasis added).*

Furthermore, the Examiner notes, the instant specification do not describe what constitutes a peripheral circuit.

Paragraph [0047] of TAKAHASHI further teaches:

"[0047] **The semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100**. The semiconductor memory circuit 101 holds data or the like to be processed in the logic circuit 105. As shown in FIG. 1, the semiconductor memory circuit 101 includes a cell array area 102, a sense amplifier area 103, and a driver area 104. FIG. 2 shows an exemplary circuit configuration of the semiconductor memory circuit 101. In the first exemplary embodiment, the semiconductor memory circuit 101 shown in FIG. 2 is illustrated as a DRAM circuit including a pair of bit lines in order to simplify the drawings. **The semiconductor memory circuit 101 may have a configuration including** multiple pairs of bit lines, memory cells connected to the multiple pairs of bit lines, a **sense amplifier**, and a **precharge circuit**. Further, the semiconductor memory circuit 101 is not limited to a DRAM, but may be an SRAM, for example." *(Emphasis added).*

As shown in Fig. 2 of TAKAHASHI the sense amplifier SA101 and precharge circuit PDLU101 are included within the integrated memory device 101.

Therefore, the Examiner respectfully submits that TAKAHASHI teaches or anticipates all limitations recited in the independent claim 1. Accordingly, the Examiner maintains his position. Disclosure of Mohammad has been added to expressly teach that the logic circuit includes Input/Output logic or circuit of semiconductor memory.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

Notice of References Cited	Application/Control No. 17/213,133	Applicant(s)/Patent Under Reexamination Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20090122620-A1	05-2009	Mohammad; Baker	G11C5/14	365/189.11
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/09/2022	11/07/2022							
	1	✓	✓							
	2	✓	-							
	3	✓	✓							
	4		✓							
	5		✓							
	6		✓							
	7		✓							
	8		✓							
	9		✓							
	10		✓							
	11		✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	HASHEM FARROKH	2138

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	03/09/2022	HF
G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/00	05/15/2023	HF

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE
711	105	03/09/2022	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

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Search Notes		
Search Notes	**Date**	**Examiner**

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PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF
PALM and EAST Inventor Search Updated	04/28/2020	HF
EAST Text Search Updated	04/28/2020	HF
Assignee/ Inventor Search Updated	11/20/2020	HF
EAST Text Search Updated	11/20/2020	HF
Inventor/Assignee Search	03/09/2022	HF
EAST Text Search	03/09/2022	HF
IP Search	03/09/2022	HF
Google Search	03/09/2022	HF
Inventor/Assignee Search Updated	11/07/2022	HF
EAST Text, CPC, Facet Search Updated	11/07/2022	HF
Inventor/Assignee Search Updated	05/15/2023	HF
EAST Text, CPC, Facet Search Updated	EAST Text, CPC, Facet Search Updated	HF

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	**Art Unit**
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Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L15	4	"13922242"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/08 08:59 AM
L16	4	(operating ADJ voltage) WITH DDR??	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 10:12 AM
L17	0	(dram OR DDR??) WITH (operat$3 near5 voltage) WITH "1.1$1v"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:00 PM
L18	6	(dram OR DDR??) WITH (operat$3 near5 voltage) WITH "1.1"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:00 PM
L19	4	18 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:01 PM
L20	387	((input$1output OR I$1O) driver) WITH ("1.1v" OR "1.1 v" OR ("1.1" ADJ volt))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:29 PM
L21	174	20 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:44 PM
L22	112	21 AND (voltage near2 range)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:45 PM
L23	4	(DRAM OR DDR??) WITH ((input$1output OR I$1O) driver) WITH ("1.1v" OR "1.1 v" OR ("1.1" ADJ volt))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:47 PM

L24	0	23 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:48 PM
L25	0	(DRAM OR DDR??) AND (((input$1output OR I$1O) near2 driver) WITH ("1.1v" OR "1.1 v" OR ("1.1" ADJ volt)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 12:49 PM
L27	3	("20060012038").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 01:47 PM
L28	3	("20060120138").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 01:49 PM
L29	3	("20090122620").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 02:10 PM
L30	6	(DRAM OR DDR??) WITH ((input$1output OR I$1O) driver OR logic OR peripheral) WITH ("1.1v" OR "1.1 v" OR ("1.1" ADJ volt))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:06 PM
L32	1	30 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:07 PM
L36	36	(DRAM OR DDR??) WITH (operat$5 near5 voltage) WITH ("1.1v" OR "1.1 v")	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:18 PM
L37	4	(DRAM OR DDR??) WITH (operat$5 near5 voltage) WITH range WITH 1.1v	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV,	OR	ON	ON	2023/05/09 04:18 PM

			MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L38	36	(DRAM OR DDR??) WITH (operat$5 near5 voltage) WITH ("1.1v" OR "1.1 v")	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:19 PM
L39	2	(DRAM OR DDR??) WITH (operat$5 near5 voltage) WITH range WITH 1.1v	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:19 PM
L40	0	37 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:21 PM
L41	7	38 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:21 PM
L42	19	(operat$5 near5 voltage) WITH range WITH (lower OR less OR smaller OR below) WITH 1.1v	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:31 PM
L43	32	(operat$5 near5 voltage) WITH range WITH (lower OR less OR smaller OR below) WITH (1.1v OR "1.1 v")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:32 PM
L44	623670	((dynamic adj4 memory) OR ??dram OR DDR??)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:34 PM
L45	3	44 SAME 43	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:35 PM

L46	7	44 AND 43	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:36 PM
L47	0	46 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:36 PM
L48	276	(operat$5 near5 voltage) WITH (lower OR less OR smaller OR below) WITH (1.1v OR "1.1 v")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:38 PM
L49	37	44 AND 48	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:38 PM
L50	6	49 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:38 PM
L51	153	DDR?? near5 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:53 PM
L52	6	50 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:54 PM
L53	58	51 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 04:56 PM
L54	7	53 AND (operat$5 near2 voltage)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/09 05:01 PM
L55	5072	DDR near5 (specication OR standard)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/10 01:17 PM
L56	329	(?DRAM OR DDR$3) WITH (LOW$4 NEAR2 operat$4 near2 voltage)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	ON	ON	2023/05/11 09:57 AM

			VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L57	100	56 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 09:58 AM
L58	2	(?DRAM OR DDR$3) WITH ((LOW$4 NEAR2 operat$4 near2 voltage) near5 range)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 09:58 AM
L59	145	(?DRAM OR DDR$3) WITH (LOW$4 NEAR2 operat$4 near2 voltage)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:07 AM
L60	100	59 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:08 AM
L61	24	(??DRAM OR ??DDR$3) WITH (LOW$4 NEAR2 operat$4 near2 voltage)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:16 AM
L62	17	61 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:22 AM
L63	2103	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (LOW$4 NEAR2 operat$4 near2 (voltage OR POWER))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:28 AM
L64	1433	63 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:29 AM
L65	26	64 AND (("1.1" ADJ volt) OR "1.1v" OR "1.1 v")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:30 AM
L66	4	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (LOW$4 NEAR2 operat$4 near2 (voltage OR POWER)) WITH ("1.1v" OR "1.1 v" OR ("1.1" ADJ volt))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:46 AM
L67	2	66 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:46 AM

L68	282	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (("1.1" ADJ volt) OR "1.1v" OR "1.1 v")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:48 AM
L69	38	68 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 10:48 AM
L70	232	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (("1.0" ADJ volt) OR "1.0v" OR "1.0 v")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 11:19 AM
L71	156	70 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 11:19 AM
L72	107	71 AND (peripheral OR (Input$1Output OR I$1O))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 11:21 AM
L73	0	sub$1.1v near5 dram	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 02:20 PM
L76	10	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (memory near2 (core OR cells)) WITH ((lower OR less OR smaller OR below) near5 (("1.1" ADJ volt) OR "1.1v" OR "1.1 v" OR "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 03:21 PM
L77	2	76 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 03:21 PM
L78	0	(sub$1one ADJ volt) WITH (DRAM OR ??DRAM OR DDR$3 OR LPDDR$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 03:35 PM
L79	0	(sub$1one ADJ volt) WITH VDD WITH (DRAM OR ??DRAM OR DDR$3 OR LPDDR$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 03:37 PM
L80	160	64 AND (("1.1" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 03:40 PM

L81	36	64 AND ((less OR lower OR smaller OR below OR sub) WITH (("1.1" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 03:41 PM
L82	36	81 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 03:41 PM
L83	4	63 WITH ((less OR lower OR smaller OR below OR sub) WITH (("1.1" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:04 PM
L84	2	83 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:04 PM
L85	0	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (vdd near2 voltage) near5 (one ADJ volt)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:08 PM
L86	0	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (vdd near2 (voltage OR power)) WITH ((lower OR less OR smaller) near5 (one ADJ volt))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:10 PM
L87	2	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (vdd near2 (voltage OR power)) WITH ((lower OR less OR smaller) near5 (("1.0" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:11 PM
L88	19	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (operat$5 near2 (voltage OR power)) WITH ((lower OR less OR smaller) near5 (("1.0" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:18 PM
L89	10	88 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:18 PM

L90	25	("7243254" "6218817" "7888966" "20020149959" "6466472" "20080253214" "20040133758" "20060077744" "20040004893" "20060291318").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:47 PM
L91	17	90 AND (DRAM OR ??DRAM OR DDR$3 OR LPDDR$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:48 PM
L92	17	91 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/11 04:49 PM
L93	38	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (core OR voltage) WITH ((lower OR less OR smaller) near5 (("1.0" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 08:42 AM
L94	16	93 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 08:43 AM
L95	0	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (core ADJ voltage) WITH ((lower OR less OR smaller) near5 (("1.0" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 08:47 AM
L96	6	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH (supply ADJ voltage) WITH ((lower OR less OR smaller) near5 (("1.0" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 08:48 AM
L97	26	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) WITH ((supply OR core OR operat$5) near2 voltage) WITH ((lower OR less OR smaller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 08:51 AM

		near5 (("1.0" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))					
L98	56	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) SAME ((supply OR core OR operat$5) near2 voltage) SAME ((lower OR less OR smaller) near5 (("1.0" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v"))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 08:54 AM
L99	30	98 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 08:54 AM
L100	62	(DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) SAME ((supply OR core OR operat$5 OR bit$1line OR (bit ADJ line)) near5 voltage) SAME ((lower OR less OR smaller) near5 (("1.0" ADJ volt) OR "1.1v" OR "1.1 v" "1.0v" OR "1.0 v" OR (one ADJ volt)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 10:16 AM
L101	31	100 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 10:17 AM
L102	1	101 NOT 99	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 10:17 AM
L103	152	(?DRAM OR ??DRAM OR DDR$3 OR LPDDR$3) SAME ((supply OR core OR operat$5 OR bit$1line OR (bit ADJ line)) near5 voltage) SAME table	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 10:25 AM
L104	56	103 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/12 10:26 AM
L105	5	(((dynamic ADJ random ADJ access ADJ memory) OR DRAM OR ?DRAM OR DDR$4 OR LPDDR) SAME voltage SAME ((less OR lower OR smaller OR below	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:06 PM

		OR under) near5 ("1.1V" OR "1.1 V" OR ("1.1" ADJ volt)))).clm.					
L106	9	(((dynamic ADJ random ADJ access ADJ memory) OR DRAM OR ?DRAM OR DDR$4 OR LPDDR) SAME ("1.1V" OR "1.1 V" OR ("1.1" ADJ volt))).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:08 PM
L107	452937	(G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/00).cpc. OR 711/105.ccls. OR (G11C11/4074 OR G11C7/10).ipc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:18 PM
L108	11	106 AND 107	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:19 PM
L109	0	108 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:19 PM
L110	200	("CHANG; YEN-AN".ine. OR "HUANG; WEI-MING".ine. OR "YUAN; DER-MIN".ine.)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL,	OR	ON	ON	2023/05/15 02:32 PM

			NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L112	4	106 AND 110	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:35 PM
L113	821	(Etron ADJ Technology).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:36 PM
L114	387	(((dynamic ADJ random ADJ access ADJ memory) OR DRAM OR ?DRAM OR DDR$4 OR LPDDR) SAME ("1.1V" OR "1.1 V" OR ("1.1" ADJ volt)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:36 PM
L115	6	113 AND 114	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/05/15 02:36 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

PTO/SB/30EFS (01-22)
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	17/213,133	Filing Date	2021-03-25	Docket Number (if applicable)	ETRP0395USA3	Art Unit	2135
First Named Inventor	Der-Min Yuan			Examiner Name	FARROKH, HASHEM		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☒ Other Extension of time

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503105

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Signature of Registered U.S. Patent Practitioner			
Signature	/Roger Chen/	Date (YYYY-MM-DD)	2023-04-14
Name	Roger Chen	Registration Number	67314

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/22 (10-20)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): ETRP0395USA3

Application Number: 17/213,133

Filed: 03/25/2021

For: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Art Unit: 2135

Examiner: FARROKH, HASHEM

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	Micro Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$220	$88	$44	$
☑	Two months (37 CFR 1.17(a)(2))	$640	$256	$128	$ 256.00
☐	Three months (37 CFR 1.17(a)(3))	$1,480	$592	$296	$
☐	Four months (37 CFR 1.17(a)(4))	$2,320	$928	$464	$
☐	Five months (37 CFR 1.17(a)(5))	$3,160	$1,264	$632	$

☑ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☑ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-3105.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 67314.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Roger Chen/	04/14/2023
Signature	Date
Roger Chen	3027291562
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Electronic Patent Application Fee Transmittal

Application Number:	17213133
Filing Date:	25-Mar-2021
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Filer:	Roger Gwan-Jye Chen/Anna Lu
Attorney Docket Number:	ETRP0395USA3

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
INDEPENDENT CLAIMS IN EXCESS OF 3	2201	1	192	192
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Extension - 2 months with $0 paid	2252	1	256	256
Miscellaneous:				
RCE- 1ST REQUEST	2801	1	544	544
		Total in USD ($)		**992**

Electronic Acknowledgement Receipt

EFS ID:	47841726
Application Number:	17213133
International Application Number:	
Confirmation Number:	9765
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Anna Lu
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0395USA3
Receipt Date:	14-APR-2023
Filing Date:	25-MAR-2021
Time Stamp:	02:53:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$992
RAM confirmation Number	E20234D353597502
Deposit Account	503105
Authorized User	Anna Lu

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	4883124.PDF	848138 8ff8587951ad95888aa86ad318cc952b0c9ff1d8	no	4
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of Continued Prosecution Application (CPA)/Request for Continued Examination(RCE)	4883123.PDF	118093 bf5d32f999e65687963f4f2869f26a1bb08013d8	no	1
Warnings:					
Information:					
3	Claims	4883122.PDF	124267 de2aa39b72013b8378dc001d4f95c65564685a5b	no	3
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	4882804.pdf	616609 9be4a638f23eb56d7cbf483c8a36fa522afbe104	no	3
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
5	Extension of Time	4882802.PDF	965043 95cc69b8f2aeba2ffe5022b4cc48cde465bec473	no	1
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	42954 788612954dfcec0d212a47caf7786546ad7086e3	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	2715104

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Amendment of Claims:

The previously presented claim 1 is amended by merging the original claim 2, the original claim 3 is amended according to the previously presented claim 1, and the original claim 2 is canceled accordingly. In addition, the new claims 4, 8 are introduced according to the previously presented claim 1 of the present invention and Figure, paragraph [0017], and Table Ⅲ of the present invention, the new claims 5, 6, 9, 10 are introduced according to the previously presented claim 1, and the new claims 7, 11 are introduced according to the original claim 2. No new matter is introduced. Allowance of the claim amendments is politely requested.

2. Rejections of claims under 35 U.S.C. 102(a)(1) & 35 U.S.C. 103:

Response:

In regard to claim 1

The amended claim 1 adds the limitation of the original claim 2.

Please refer to paragraph [0016] of the present invention. Paragraph [0016] of the present invention discloses "Please refer to Table Ⅲ. **Table Ⅲ** illustrates **operation voltage ranges** … **according to another embodiment**", so according to paragraph [0016] of the present invention, it is very obvious that **Table Ⅲ** is the **operation voltage**

solution proposed by the present invention to solve the shortcomings of the prior art, **rather than AAPA**. That is, that the examiner holds that **Table Ⅲ** teaches the technical feature **"the first voltage is different from the second voltage**" of the original claim 2 of the present invention **is not proper** because **Table Ⅲ** is **not AAPA** of the present invention. Therefore, **AAPA** obviously **fails to** teach the technical feature "**the first voltage is different from the second voltage**" of the amended claim 1.

In regard to claim 3

Please refer to paragraph [0016] of the present invention. Paragraph [0016] of the present invention discloses "Please refer to Table Ⅲ. **Table Ⅲ** illustrates **operation voltage ranges** … **according to another embodiment**", so according to paragraph [0016] of the present invention, it is very obvious that **Table Ⅲ** is the **operation voltage solution proposed by the present invention** to solve the shortcomings of the prior art, **rather than AAPA**. That is, that the examiner holds that **Table Ⅲ** teaches the technical feature "**the first voltage is greater than the second voltage**" of the original claim 3 of the present invention **is not proper** because **Table Ⅲ** is **not AAPA** of the present invention. Therefore, **AAPA** obviously **fails to** teach the technical feature "**the first voltage is greater than the second voltage**" of the original claim 3.

In addition, because the examiner **does not utilize TAKAHASHI to reject** the technical feature "**the first voltage is greater than the second voltage**" of the original claim 3, TAKAHASHI also obviously **fails to** teach the technical feature "**the first voltage is greater than the second voltage**" of the original claim 3. Therefore, because both AAPA and TAKAHASHI **fail to** teach the technical feature "**the first voltage is greater than the second voltage**" of the original claim 3, the currently amended claim 3 (including the technical feature "**the first voltage is greater than the second voltage**" of the original claim 3) should be patentable over AAPA and TAKAHASHI.

In regard to claims 4, 8

Please refer to Figure, paragraph [0017], and Table Ⅲ of the present invention. Paragraph [0017] of the present invention discloses "**operation voltages** of **the input/output unit 106** in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification **are a third predetermined voltage**, where **the third predetermined voltage is lower than 1.1V**", so Figure, paragraph [0017], and Table Ⅲ of the present invention obviously teach the technical features "**an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell, and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage, wherein the third voltage is not greater than 1.1V; wherein the first voltage is greater than the third voltage**", but it is very obvious that neither AAPA nor TAKAHASHI **disclose any technical features corresponding to the input/output unit of the dynamic random access memory**.

Therefore, after the new claims 4, 8 of the present invention are introduced according to the previously presented claim 1 of the present invention and the above-mentioned technical features disclosed by Figure, paragraph [0017], and Table Ⅲ of the present invention, the new claims 4, 8 of the present invention **are obviously patentable over** AAPA and TAKAHASHI.

To sum up, allowance of the currently amended claims 1 and 3 and the new claims 4-11, is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Roger Chen/ Date: 04/14/2023

Roger Chen, Patent Agent No. 67,314
5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan
Voice Mail: 302-729-1562
e-mail : RogerChen@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time and DST 12 hours behind.)

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Appl. No.	: 17/213,133	Confirmation No.	:	9765
First Named Inventor	: Der-Min Yuan			
Filed	: March 25, 2021			
TC/A.U.	: 2135			
Examiner	: FARROKH, HASHEM			
Docket No.	: ETRP0395USA3			
Customer No.	: 27765			

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

In response to the Office action of November 14, 2022, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V, and

wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell<u>, and wherein the first voltage is different from the second voltage</u>.

2. (Deleted)

3. (currently amended): ~~The dynamic random access memory of claim 1,~~ <u>A dynamic random access memory (DRAM), comprising:</u>

<u>a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and</u>

<u>a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the</u>

peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V;

wherein the first voltage is greater than the second voltage.

4. (new): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell; and

an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell, and the input/output circuit is supplied with a third voltage w to make the input/output circuit operate at the third voltage, wherein the third voltage is not greater than 1.1V; and

wherein the DRAM core cell and the input/output circuit are formed on a single chip, and the input/output circuit is external to the DRAM core cell, and wherein the first voltage is different from the third voltage.

5. (new): The dynamic random access memory of claim 4, wherein the first voltage is not greater than 1.1V.

6. (new): The dynamic random access memory of claim 4, further comprising:

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V.

7. (new): The dynamic random access memory of claim 6, wherein the first voltage is different from the second voltage.

8. (new): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is

supplied with a first voltage to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell; and

an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell, and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage, wherein the third voltage is not greater than 1.1V;

wherein the first voltage is greater than the third voltage.

9. (new): The dynamic random access memory of claim 8, wherein the first voltage is not greater than 1.1V.

10. (new): The dynamic random access memory of claim 8, further comprising:

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V.

11. (new): The dynamic random access memory of claim 10, wherein the first voltage is different from the second voltage.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/213,133	Filing Date 03/25/2021	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	04/14/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0		x $40 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 3	= 1		x $192 =	192
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	192

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/BRENDA V HARRISON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3	9765

27765 7590 11/14/2022
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
11/14/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 17/213,133	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 08/12/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-3 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-3 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 03/25/2021 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This Office action is in response to the communication(s) filed on 08/12/2022. There are a total of 3 claims pending in the application. Claim 1 has been amended, no claims have been added or canceled.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

Terminal Disclaimer

The terminal disclaimer filed on 08/12/2022 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of Application 16/151,347 has been reviewed and is accepted. The terminal disclaimer has been recorded.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.*

Claim 1 is rejected under 35 U.S.C. 102(a)(1) as being anticipated by TAKAHASHI et al. "TAKAHASHI" (US 2010/0290300 A1).

4. In regard to claim 1 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., Figs. 1-2, ¶ 0047, semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100)**, comprising: a DRAM core cell comprised in the DRAM **(e.g., cell array 102 in Fig. 1)**, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V;" **(e.g., ¶ 0084, Fig. 8).** *The VDD of bit line (e.g., VDD applied to memory cells is 0.8 v.*

"and a peripheral circuit comprised in the DRAM **(e.g., Fig. 2, ¶ 00 47, The semiconductor memory circuit 101 may have a configuration including multiple pairs of bit lines, memory cells connected to the multiple pairs of bit lines, a sense amplifier, and a precharge circuit; Figs. 1 and 7. ¶ 0078,, The second exemplary embodiment assumes the case where transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201)**, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater than 1.1V, and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell." **[(e.g., ¶ 0078, the logic circuit 105 serving as a peripheral circuit… further reduced (e.g., VDD is 08 V or lower)].**

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have*

> *been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.*

Claim 2-3 are rejected under 35 U.S.C. 103 as being unpatentable over TAKAHASHI in view Applicant Prior Art Admission (APAA – DDR Specification).

5. In regard to claims 2 TAKAHASHI further teaches:

"wherein the first voltage is different from the second voltage." **(e.g., ¶ 0016 and TABLE III on page 2 of instant specification – APAA).** *Table III specify the voltage of memory core (e.g., first voltage) as 1.8 V +/- 0.1 V and the voltage of peripheral circuit (e.g., second voltage) as <1.1 V. The two voltages are different.*

Paragraph [0016] of the claimed specification recites:

"[0016] Please refer to Table III. **Table III illustrates operation voltage ranges** of the dynamic random-access memory 100 operating in the **DDR I specification, the low power DDR I specification, the DDR II specification, and the low power DDR II specification** according to another embodiment."

6. In regard to claim 3 TAKAHASHI further teaches:

"wherein the first voltage is greater than the second voltage." **(e.g., ¶ 0016 and TABLE III on page 2 of instant specification – APAA).** *Table III specify the voltage of memory core (e.g., first voltage) as 1.8 V +/- 0.1 V and the voltage of peripheral circuit (e.g., second voltage) as <1.1 V. The two voltages are different. The first voltage 1.8 V is greater than second voltage < 1.1 V*

Response to Remarks

Applicant arguments have been fully considered but they are not persuasive. On page 4 of the Remarks, Applicant make reference to paragraph [0078] and Figs. 1 and 7 of TAKAHASHI and states:

"Therefore, according to FIG. 1 and paragraph [0078] of TAKAHASHI, because the logic circuit 105 is not included in the semiconductor memory circuit 101, **it is obvious that the logic circuit 105 of TAKAHASHI does not disclose the peripheral cir**cuit of the currently amended claim 1" *(emphasis added).*

TAKAHASHI teaches:

"[0078] The semiconductor integrated device 200 includes **the semiconductor memory circuit 201 and the logic circuit 105**. The semiconductor memory circuit 201 is a built-in DRAM of a system LSI, as with the first exemplary embodiment. The **second exemplary embodiment assumes the case where transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201** are further reduced in film thickness and the power supply voltage is also further reduced (e.g., VDD is 0.8 V or lower) as compared with the first exemplary embodiment." *(Emphasis added).*

TAKAHASHI clearly teaches that transistors constituting the logic circuit 105 serving as a peripheral circuit of the semiconductor memory (e.g., circuit 101 in Fig. 2 or circuit 201 in Fig. 7 of TAKAHASHI).

Claim 1 of TAKAHASHI, in part recites:

"1. A semiconductor integrated device comprising: a semiconductor memory circuit; and **a peripheral circuit of the semiconductor memory circuit**..." *(Emphasis added).*

Furthermore, the Examiner notes, the instant specification do not describe what constitutes a peripheral circuit.

Paragraph [0047] of TAKAHASHI further teaches:

"[0047] **The semiconductor memory circuit 101 is a built-in DRAM of the semiconductor integrated device 100**. The semiconductor memory circuit 101 holds data or the like to be processed in the logic circuit 105. As shown in FIG. 1, the semiconductor memory circuit 101 includes a cell array area 102, a sense amplifier area 103, and a driver area 104. FIG. 2 shows an exemplary circuit configuration of the semiconductor memory circuit 101. In the first exemplary embodiment, the

semiconductor memory circuit 101 shown in FIG. 2 is illustrated as a DRAM circuit including a pair of bit lines in order to simplify the drawings. **The semiconductor memory circuit 101 may have a configuration including** multiple pairs of bit lines, memory cells connected to the multiple pairs of bit lines, a **sense amplifier**, and a **precharge circuit**. Further, the semiconductor memory circuit 101 is not limited to a DRAM, but may be an SRAM, for example." *(Emphasis added).*

As shown in Fig. 2 of TAKAHASHI the sense amplifier SA101 and precharge circuit PDLU101 are included within the integrated memory device 101.

Therefore, the Examiner respectfully submits that TAKAHASHI teaches or anticipates all limitations recited in the independent claim 1. Accordingly, the Examiner maintains his position.

Conclusion

THIS ACTION IS MADE FINAL. *Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is

(571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2131

November 8, 2022

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/09/2022	11/07/2022							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	03/09/2022	HF

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE
711	105	03/09/2022	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF
PALM and EAST Inventor Search Updated	04/28/2020	HF
EAST Text Search Updated	04/28/2020	HF
Assignee/ Inventor Search Updated	11/20/2020	HF
EAST Text Search Updated	11/20/2020	HF
Inventor/Assignee Search	03/09/2022	HF
EAST Text Search	03/09/2022	HF
IP Search	03/09/2022	HF
Google Search	03/09/2022	HF
Inventor/Assignee Search Updated	11/07/2022	HF
EAST Text, CPC, Facet Search Updated	11/07/2022	HF

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	1	"17213133"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/05 12:20 PM
L2	22	((dynamic ADJ random ADJ access ADJ memory) OR DRAM OR ?DRAM) SAME voltage SAME ((less OR lower OR smaller OR below OR under) near5 ("1.1V" OR "1.1 V" OR ("1.1" ADJ volt)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 09:31 AM
L3	5	(((dynamic ADJ random ADJ access ADJ memory) OR DRAM OR ?DRAM) SAME voltage SAME ((less OR lower OR smaller OR below OR under) near5 ("1.1V" OR "1.1 V" OR ("1.1" ADJ volt)))).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 09:32 AM
L4	198	("CHANG; YEN-AN".ine. OR "HUANG; WEI-MING".ine. OR "YUAN; DER-MIN".ine.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 09:33 AM
L5	309896	(G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/00).cpc. OR 711/105.ccls. OR (G11C11/4074 OR G11C7/10).ipc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 09:38 AM
L6	10	2 AND 5	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 09:39 AM
L8	83198787	"12" AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/11/07 09:43 AM

			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L10	12	2 AND (@ad<"20130223")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 09:44 AM
L11	7	((dynamic ADJ random ADJ access ADJ memory) OR DRAM OR ?DRAM) SAME voltage adj2 ((less OR lower OR smaller OR below OR under) near5 ("1.1V" OR "1.1 V" OR ("1.1" ADJ volt)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 09:51 AM
L12	10	("20100290300" "20090122620" "20090067217" "20050133852").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 10:16 AM
L13	810	(Etron ADJ Technology).as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 05:07 PM
L14	2	13 AND 2	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/11/07 05:07 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Appl. No.	: 17/213,133	Confirmation No.	9765
First Named Inventor	: Der-Min Yuan		
Filed	: March 25, 2021		
TC/A.U.	: 2135		
Examiner	: FARROKH, HASHEM		
Docket No.	: ETRP0395USA3		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of March 14, 2022, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended): A dynamic random access memory (DRAM), comprising:

a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and

a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater ~~lower~~ than 1.1V, and

wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell.

2. (original): The dynamic random access memory of claim 1, wherein the first voltage is different from the second voltage.

3. (original): The dynamic random access memory of claim 1, wherein the first voltage is greater than the second voltage.

PTO/AIA/26 (04-13)
Approved for use through 04/30/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) ETRP0395USA3

In re Application of: Der-Min Yuan et al.

Application No.: 17/213,133

Filed: 03/25/2021

For: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

The applicant, Etron Technology, Inc., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,998,017 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for any during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 67314

/Roger Chen/ — Signature
08/12/2022 — Date

Roger Chen — Typed or printed name

Agent of Record — Title
Voice Mail:3027291562 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included. USD 170.00

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/22 (10-20)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) ETRP0395USA3
Application Number 17/213,133	Filed 03/25/2021
For DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	
Art Unit 2135	Examiner FARROKH, HASHEM

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	Micro Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$220	$110	$55	$
☑	Two months (37 CFR 1.17(a)(2))	$640	$320	$160	$ 320.00
☐	Three months (37 CFR 1.17(a)(3))	$1,480	$740	$370	$
☐	Four months (37 CFR 1.17(a)(4))	$2,320	$1,160	$580	$
☐	Five months (37 CFR 1.17(a)(5))	$3,160	$1,580	$790	$

☑ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☑ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-3105.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 67314.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Roger Chen/	08/12/2022
Signature	Date
Roger Chen	3027291562
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Electronic Patent Application Fee Transmittal

Application Number:	17213133
Filing Date:	25-Mar-2021
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Filer:	Roger Gwan-Jye Chen/Anna Lu
Attorney Docket Number:	ETRP0395USA3

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	2252	1	320	320
Miscellaneous:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	170	170
		Total in USD ($)		**490**

Electronic Acknowledgement Receipt

EFS ID:	46397530
Application Number:	17213133
International Application Number:	
Confirmation Number:	9765
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Anna Lu
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	ETRP0395USA3
Receipt Date:	12-AUG-2022
Filing Date:	25-MAR-2021
Time Stamp:	03:33:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$490
RAM confirmation Number	E20228B434180225
Deposit Account	503105
Authorized User	Anna Lu

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	4656518.PDF	850966 f58e0d88eaea72959058a301ffdddef5d1ab1088	no	4
Warnings:					
Information:					
2	Amendment/Request for Reconsideration-After Non-Final Rejection	4656517.PDF	114571 30a4f2f1b2cb6a83164580603e20c5ef15ce75d9	no	1
Warnings:					
Information:					
3	Claims	4656516.PDF	115405 7f6d914d158a906ce258420dbf6c830e1da1a116	no	1
Warnings:					
Information:					
4	Terminal Disclaimer Filed	4656450.PDF	969048 e0ebfce86d23fd065c86865ba2030c5ab7c38461	no	1
Warnings:					
Information:					
5	Extension of Time	4656443.PDF	965198 5a669cd10b5e266d1e9fe6a1cd4a495365bc5676	no	1
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	40582 31eb2db753fb8d8d93221bdd670ed0391ecef418	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	3055770

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Claim Objections

After "**wherein the second voltage is not greater lower than 1.1V**" recited in claim 1 is replaced with "**wherein the second voltage is not greater than 1.1V**", the currently amended claim 1 should overcome claim objection.

2. Double Patenting

Claim 1 of the present invention is rejected on the ground of nonstatutory double patenting as being unpatenable over claim 1 of U.S. Patent No. US 10998017.

Response:

To overcome the rejection based on nonstatutory double patenting, the applicant wishes to submit a terminal disclaimer of the instant application in compliance with 37 CFR 1.321(c) or 1.321(d) without disclaimer as to the merits of the claims filed in the present invention. In light of this, acceptance of the terminal disclaimer is therefore respectfully requested, and the applicant respectfully requests reconsideration of the rejection under double patenting of claim 1 of the present invention.

3. Rejections of claims under 35 U.S.C. 102(a)(1) & 35 U.S.C. 103:

Response:

Please refer to FIG. 1 and paragraph [0078] of TAKAHASHI (US20100290300). Paragraph [0078] of TAKAHASHI discloses "The **semiconductor integrated device 200** **<u>includes</u>** the **<u>semiconductor memory circuit 201</u>** and the **<u>logic circuit 105</u>**. The **<u>semiconductor memory circuit 201 is a built-in DRAM</u>** of a system LSI". Because

paragraph [0078] of TAKAHASHI discloses "The **semiconductor memory circuit 201** **is a built-in DRAM** of a system LSI", it is obvious that the **semiconductor memory circuit 201** (the **semiconductor memory circuit 101**) **can be referred to** **dynamic random access memory (DRAM)** of the currently amended claim 1 of the present invention. In addition, as shown in FIG. 1 of TAKAHASHI, it is very obvious that the **logic circuit 105** (the examiner holds that the **logic circuit 105** **can be referred to** **peripheral circuit** of the currently amended claim 1 of the present invention) **is not included in** **the semiconductor memory circuit 101** (the **semiconductor memory circuit 101** **can be referred to** **dynamic random access memory (DRAM)** of the currently amended claim 1 of the present invention). Therefore, according to FIG. 1 and paragraph [0078] of TAKAHASHI, because the **logic circuit 105** **is not included in** **the semiconductor memory circuit 101**, it is obvious that the **logic circuit 105** of TAKAHASHI **does not disclose** **the peripheral circuit** of the currently amended claim 1 of the present invention. That is, TAKAHASHI **fails to** teach **the peripheral circuit** of the currently amended claim 1 of the present invention. FIG. 1 of TAKAHASHI is shown as follows:

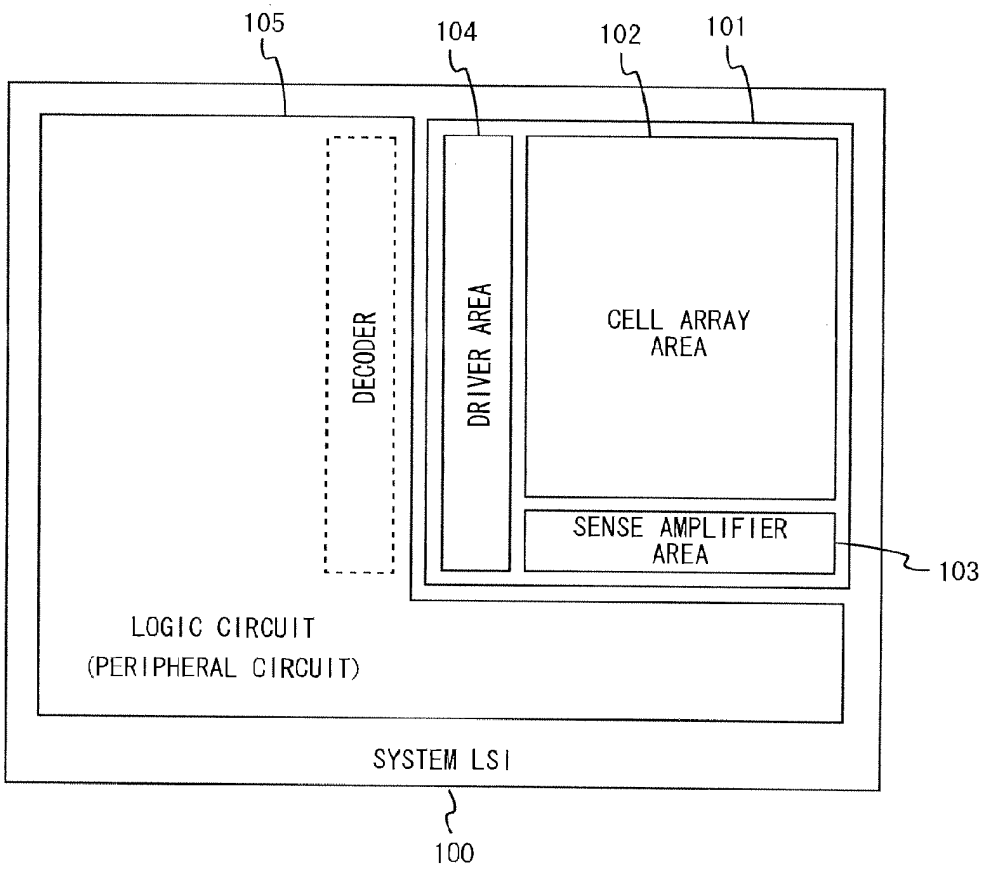

Fig. 1

Therefore, because, according to FIG. 1 and paragraph [0078] of TAKAHASHI, TAKAHASHI obviously **fails to** teach **the peripheral circuit** of the currently amended claim 1 of the present invention, the currently amended claim 1 should be patentable over TAKAHASHI.

To sum up, allowance of the currently amended claim 1 and the original claims 2, 3 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Roger Chen/ Date: 08/12/2022

Roger Chen, Patent Agent No. 67,314
5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan
Voice Mail: 302-729-1562
e-mail : RogerChen@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time and DST 12 hours behind.)

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
* 17/213,133 *	17/213,133	Yuan et al.	
	Examiner FARROKH, HASHEM	Art Unit 2135	

Document Code - DISQ	Internal Document - DO NOT MAIL

TERMINAL DISCLAIMER	☑ APPROVED	☐ DISAPPROVED
Date Filed: 12 August 2022	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

/LAWANA R HIXON/

Technology Center: OPLC

Telephone: (571)272-6074

_____

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/213,133	Filing Date 03/25/2021	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	08/12/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 3	Minus	** 20	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/LAVINIA D JOHNSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3	9765

27765 7590 03/14/2022
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
03/14/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 17/213,133	Applicant(s) Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 03/25/2021.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-3 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-3 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 03/25/2021 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 06/25/2021.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This Office action is in response to the communication(s) filed on 03/05/2021. There are a total of 3 claims pending in the application. Claim 1 is independent and claim 2-3 are dependent.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.

INFORMATION CONCERNING IDS:

The information disclosure statement (IDS) submitted on 06/25/2021 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

INFORMATION CONCERNING CLAIMS:

Claim Interpretation

Claim limitations in this application do not use the word "means" (or "step"), thus, they are not being interpreted under 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph.

INFORMATION CONCERNING CLAIMS:

Claim Objections

Claim 1 is objected to because of the following informalities:

1. The independent claim 1 in lines 11-12 recites the limitation:

"wherein the second voltage **is not greater lower** than 1.1V" *(emphasis added).*

It is not clear what "greater lower" *means. For rejection and the prior art search, the Examiner has assumed the limitation meant to recite* ""wherein the second voltage **is lower** than 1.1V"

Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, *140 F.3d 1428, 46*

USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, *11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993);* In re Longi, *759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985);* In re Van Ornum, *686 F.2d 937, 214 USPQ 761 (CCPA 1982);* In re Vogel, *422 F.2d 438, 164 USPQ 619 (CCPA 1970);* In re Thorington, *418 F.2d 528, 163 USPQ 644 (CCPA 1969).*

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 et seq. *for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).*

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

2. Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 of U.S. Patent No. 10,998,017. Although the claims at issue

*are not identical, they are not patentably distinct from each other because the slight differences in claim language does not make the claims patentably distinct from each other. For example, the claim 1 of the instant application additionally recites the limitation "*a peripheral circuit comprised in the DRAM". *However, the preamble and the further limitations in body of claims indicate the memory cell array and the peripheral circuits are parts of the DRAM.*

3. Claim 1 of instant application (Application No. 17/213,133) is compared to claim 1 of Patent No. 10,998,017 B2 in the following table:

Patent No. 10,998,017 B2	***Application No. 17/213,133***
Claim 1: 1. A dynamic random access memory (DRAM), comprising: a DRAM core cell, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V;	**Claim 1:** 1. A dynamic random access memory (DRAM), comprising: a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and a peripheral circuit comprised in the DRAM,

and a peripheral circuit electrically connected to the DRAM core cell,	wherein the peripheral circuit is electrically connected to the DRAM core cell,
wherein the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is lower than 1.1V, and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell;	and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater lower than 1.1V, and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell.
wherein the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP).	

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.*

Claim 1 is rejected under 35 U.S.C. 102(a)(1) as being anticipated by TAKAHASHI et al. "TAKAHASHI" (US 2010/0290300 A1).

4. In regard to claim 1 TAKAHASHI teaches:

"A dynamic random access memory (DRAM) **(e.g., ¶ 0047; Figs. 1-2)**, comprising: a DRAM core cell comprised in the DRAM **(e.g., ell array 102 in Fig. 1)**, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V;" **(e.g., ¶ 0084, Fig. 8)**. *The VDD of bit line (e.g., VDD applied to memory cells is 0.8 v.*

"and a peripheral circuit comprised in the DRAM **(e.g., ¶ 0078; Figs. 1-2)**, wherein the peripheral circuit is electrically connected to the DRAM core cell **[e.g., logic circuit (peripheral circuit) 105 in Fig. 1)**, and the peripheral circuit is supplied with a second

voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage **is not greater lower** than 1.1V, and wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell." **[(e.g., ¶ 0078, the logic circuit 105 serving as a peripheral circuit… further reduced (e.g., VDD is 08 V or lower)].**

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.*

Claim 2-3 are rejected under 35 U.S.C. 103 as being unpatentable over TAKAHASHI in view Applicant Prior Art Admission (APAA – DDR Specification).

5. In regard to claims 2 TAKAHASHI further teaches:

"wherein the first voltage is different from the second voltage." **(e.g., ¶ 0016 and TABLE III on page 2 of instant specification -- APAA).** *Table III specify the voltage of*

memory core (e.g., first voltage) as 1.8 V +/- 0.1 V and the voltage of peripheral circuit (e.g., second voltage) as <1.1 V. The two voltages are different.

Paragraph [0016] of the claimed specification recites:

"[0016] Please refer to Table III. **Table III illustrates operation voltage ranges** of the dynamic random access memory 100 operating in the **DDR I specification, the low power DDR I specification, the DDR II specification, and the low power DDR II specification** according to another embodiment."

6. In regard to claim 3 TAKAHASHI further teaches:

"wherein the first voltage is greater than the second voltage." **(e.g., ¶ 0016 and TABLE III on page 2 of instant specification -- APAA).** *Table III specify the voltage of memory core (e.g., first voltage) as 1.8 V +/- 0.1 V and the voltage of peripheral circuit (e.g., second voltage) as <1.1 V. The two voltages are different. The first voltage 1.8 V is greater than second voltage < 1.1 V*

Conclusion

The prior art made of record and not relied upon are as follows:

1. Mohammad (US 20090122620 A1).

2. Sunwoo et al. (US 20090067217 A1).

3. Shau (US 20050133852 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2131

March 9, 2022

Notice of References Cited	Application/Control No. 17/213,133	Applicant(s)/Patent Under Reexamination Yuan et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20100290300-A1	11-2010	TAKAHASHI; Hiroyuki	G11C11/4094	365/207
*	B	US-20090122620-A1	05-2009	Mohammad; Baker	G11C5/14	365/189.11
*	C	US-20090067217-A1	03-2009	Sunwoo; Jung	G11C7/1069	365/230.06
*	D	US-20050133852-A1	06-2005	Shau, Jeng-Jye	G11C11/4087	257/E21.639
	E					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/09/2022								
	1	✓								
	2	✓								
	3	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 3/061	5/17/2015	RIE
G06F 3/0628	5/17/2015	RIE
G06F 3/0653	5/17/2015	RIE
G06F 3/0656	5/17/2015	RIE
G06F 12/0238	5/17/2015	RIE
G06F 12/063	5/17/2015	RIE
G06F 12/0692	5/17/2015	RIE
G06F 12/0866	5/17/2015	RIE
G06F 12/0882	5/17/2015	RIE
G06F 13/4221	5/17/2015	RIE
g06F 13/4278	5/17/2015	RIE
Search Updated	11/16/2015	RIE
Search Updated	5/15/2016	RIE
Search Updated	10/1/2016	RIE
Search Updated	5/14/2017	RIE
Search Updated	9/18/2017	RIE
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	5/28/2018	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0866; G06F12/0882; G06F13/4221; G06F3/061; G06F3/0653; G06F3/0656; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	11/11/2019	HF
G06F12/0238; G06F12/063; G06F12/0692; G06F12/0882; G06F13/4221; G06F13/4278; G06F3/061; G06F3/0653; G06F3/0656; G11C11/40615; G11C11/4074; G11C7/1075; Y02D10/14; Y02D10/151	03/09/2022	HF

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	105	5/17/2015	RIE
	111	5/17/2015	RIE
	154	5/17/2015	RIE
710	7	5/17/2015	RIE
	21	5/17/2015	RIE
	34	5/17/2015	RIE
	52	5/17/2015	RIE
712	16	5/17/2015	RIE
	209	5/17/2015	RIE
	214	5/17/2015	RIE
	245	5/17/2015	RIE
Search	Updated	11/16/2015	RIE
Search	Updated	5/15/2016	RIE
365	51	5/15/2016	RIE
	59	5/15/2016	RIE
	143	5/15/2016	RIE
	205	5/15/2016	RIE
	226	5/15/2016	RIE
	189	5/15/2016	RIE
	189.09	5/15/2016	RIE
Search	Updated	10/1/2016	RIE
Search	Updated	5/14/2017	RIE
Search	Updated	9/18/2017	RIE
711	105	03/09/2022	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

Search Notes		
Search Notes	**Date**	**Examiner**
PLUS Search	5/17/2015	RIE
PALM Inventor Search	5/17/2015	RIE
EAST Text Search	5/17/2015	RIE
EAST Text Search Updated	11/16/2015	RIE
EAST Text Search Updated	5/15/2016	RIE
EAST Text Search Updated	10/1/2016	RIE
EAST Text Search Updated	5/14/2017	RIE
EAST Text Search Updated	9/18/2017	RIE
EAST Text Search Updated	5/28/2018	HF
PALM Inventor Search Updated	01/21/2019	HF
EAST Text Search Updated	01/21/2019	HF
PALM and EAST Inventor Search Updated	07/01/2019	HF
EAST Text Search Updated	07/01/2019	HF
PALM and EAST Inventor Search Updated	11/11/2019	HF
EAST Text Search Updated	11/11/2019	HF
PALM and EAST Inventor Search Updated	04/28/2020	HF
EAST Text Search Updated	04/28/2020	HF
Assignee/ Inventor Search Updated	11/20/2020	HF
EAST Text Search Updated	11/20/2020	HF
Inventor/Assignee Search	03/09/2022	HF
EAST Text Search	03/09/2022	HF
IP Search	03/09/2022	HF
Google Search	03/09/2022	HF

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/213,133	Yuan et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
Search	History	5/15/2016	RIE

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	886	(ETRON adj TECHNOLOGY).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:17
L13	2	L7 and (L8 or L9 or L10)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:22
L14	26	((((volatile adj memory) or SRAM or ??RAM) near2 (chip or die or ASIC or ((integrated adj circuit) or IC))) with (peripheral near2 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:26
L15	58	Yuan-Der-Min.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:26
L16	59	Chang-Yen-An.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:26
L17	122	Huang-Wei-Ming.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:26
L18	0	L14 and (L15 or L16 or L17)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:26

L19	94	(((Dynamic adj random adj access adj memory) or DRAM) and (cell adj array) and (peripheral near2 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:30
L20	0	L19 and (L15 or L16 or L17)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:31
L21	17	(((Dynamic adj random adj access adj memory) or DRAM) and (cell near2 core) and (peripheral near2 (circuits or unit or section))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:33
L22	3	L21 and (L15 or L16 or L17)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:34
L23	1	6 and 21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:35
L24	451	(((Dynamic adj random adj access adj memory) or DRAM) and (cell near2 core) and (peripheral near2 (circuits or unit or section)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:35
L25	2	6 and 24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:36
L26	5	((dynamic adj random adj access adj memory) or DRAM) with ((compatible or appl$4 or used or utiliz$4) near5 ((embedded adj display adj port) or eDP))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:40

L27	5	L26 AND ((G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0866 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/00 OR Y02D10/14 OR Y02D10/151).CPC. OR (711/105).CCLS. OR (G11C7/10 OR G11C11/4074).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:40
L28	92	("7295036" "6551896" "6097070" "6570787" "6363014" "5928336" "7894294" "7692979" "7594129" "20110292448" "20060259679" "20110252253" "20060192282" "20030031043" "20060120138" "20060140004" "20050010746" "20130135955" "20110069562" "20100095137" "20100074043" "20100005439" "20090122620" "20060047985" "20120182076" "20100008172" "20130046941" "20130132660" "20050133852" "20090067217" "20080117700" "20100290300").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:54
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L30	14	L29 AND ((G06F12/0238 OR G06F12/063 OR G06F12/0692 OR G06F12/0882 OR G06F13/4221 OR G06F13/4278 OR G06F3/061 OR G06F3/0653 OR G06F3/0656 OR G11C11/40615 OR G11C11/4074 OR G11C7/1075 OR Y02D10/14 OR Y02D10/151).CPC. OR (711/105).CCLS. OR (G11C7/10).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 13:57
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S231	6	"16151347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2022/03/09 09:17

			DERWENT; IBM_TDB			
S232	1	"17213133"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/03/09 09:31

3/9/2022 2:15:28 PM
C:\Users\hfarrokh\Documents\EAST\Workspaces\13922242.wsp

Visuals

1 - 50

DRAM and manufacturing method thereof

A 16 megabit (224) or greater density single deposition layer metal Dynamic Random Access Memory (DRAM) part is described which allows for a die that fits within an industry-standard 300 mi wide SOJ (Small Outline J-wing) package or a TSOP (Thin, Small Outline Package) with little or no speed loss...

ROUND ROCK RSCH LLC

JP3790853B2 : Japan Patents : 2006-06-28 : 5

Semiconductor chip manufacturing process for integrating logic circuitry, embedded dram and embedded non-volatile ferroelectric random access memory (feram) on a same semiconductor die

An apparatus is described. The apparatus includes a semiconductor chip that includes logic circuitry, embedded dynamic random access memory (DRAM) cells and embedded ferroelectric random access memory (FeRAM) cells.

INTEL CORP

US20190279697 : US Applications : 2019-09-12 : 5

Semiconductor chip manufacturing process for integrating logic circuitry, embedded dram and embedded non-volatile ferroelectric random access memory (feram) on a same semiconductor die

An apparatus is described. The apparatus includes a semiconductor chip that includes logic circuitry, embedded dynamic random access memory (DRAM) cells and embedded ferroelectric random access memory (FeRAM) cells.

INTEL CORP

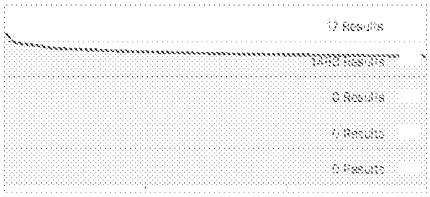
WO2018063375A1 : WIPO Applications : 2018-04-05 : 5

Semiconductor chip manufacturing process for integrating logic circuitry, embedded DRAM and embedded non-volatile ferroelectric random access memory (FERAM) on a same semiconductor die

An apparatus is described. The apparatus includes a semiconductor chip that includes logic circuitry, embedded dynamic random access memory (DRAM) cells and embedded ferroelectric random access memory (FeRAM) cells.

INTEL CORP

Relevance



Publication Date

First Cur Assignees by Relevance

ROUND ROCK RSCH LLC **(87)**
INTEL CORP **(146)**
MICRON TECH INC **(443)**
YANGTZE MEMORY TEC... **(72)**
KEPLER COMPUTING **(1)**
EMPIRE TECH DEV LLC **(4)**

More Visuals

Result 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17213133
	Filing Date	2021-03-25
	First Named Inventor	Der-Min Yuan
	Art Unit	2135
	Examiner Name	~~N/A~~ Hashem Farrokh
	Attorney Docket Number	ETRP0395USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7295036	B1	2007-11-13	Zaveri	
	2	6551896	B2	2003-04-22	Hosoda	
	3	6097070	A	2000-08-01	Mandelman	
	4	6570787	B1	2003-05-27	Wang	
	5	6363014	B1	2002-03-26	Fastow	
	6	5928336	A	1999-07-27	Takeuchi	
	7	7894294	B2	2011-02-22	Pyeon	
	8	7692979	B2	2010-04-06	Fuji	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17213133
	Filing Date	2021-03-25
	First Named Inventor	Der-Min Yuan
	Art Unit	2135
	Examiner Name	N/A
	Attorney Docket Number	ETRP0395USA3

	9	7594129	B2	2009-09-22	Otani	
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110292448	A1	2011-12-01	OHASHI	
	2	20060259679	A1	2006-11-16	Schumann	
	3	20110252253	A1	2011-10-13	RUI	
	4	20060192282	A1	2006-08-31	Suwa	
	5	20030031043	A1	2003-02-13	Pochmuller	
	6	20060120138	A1	2006-06-08	Liaw	
	7	20060140004	A1	2006-06-29	Shukuri	
	8	20050010746	A1	2005-01-13	Chen	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17213133
	Filing Date	2021-03-25
	First Named Inventor	Der-Min Yuan
	Art Unit	2135
	Examiner Name	N/A
	Attorney Docket Number	ETRP0395USA3

	9	20130135955	A1	2013-05-30	McCombs	
	10	20110069562	A1	2011-03-24	Conte	
	11	20100095137	A1	2010-04-15	Bieswanger	
	12	20100074043	A1	2010-03-25	Kang	
	13	20100005439	A1	2010-01-07	SHIKATA	
	14	20090122620	A1	2009-05-14	Mohammad	
	15	20060047985	A1	2006-03-02	Otani	
	16	20120182076	A1	2012-07-19	Kim	
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	18	20130046941	A1	2013-02-21	Ma	
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	First Named Inventor	Der-Min Yuan
	Art Unit	2135
	Examiner Name	N/A
	Attorney Docket Number	ETRP0395USA3

	20	20050133852	A1	2005-06-23	Shau	
	21	20090067217	A1	2009-03-12	Sunwoo	
	22	20080117700	A1	2008-05-22	Nakamura	
	23	20100290300	A1	2010-11-18	TAKAHASHI	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	102187323	CN	A	2011-09-14			Abstract
	2	201123198	TW		2011-07-01			Abstract

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1	Iyer, S.S.; IBM Corp., East Fishkill, NY, USA; Kalter, H.L., "Embedded DRAM technology: opportunities and challenges", Spectrum, IEEE (Volume: 36, Issue: 4), Apr. 1999, IEEE, pages 56-64.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17213133
	Filing Date	2021-03-25
	First Named Inventor	Der-Min Yuan
	Art Unit	2135
	Examiner Name	N/A
	Attorney Docket Number	ETRP0395USA3

EXAMINER SIGNATURE			
Examiner Signature	/HASHEM FARROKH/	Date Considered	03/09/2022
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17213133
	Filing Date	2021-03-25
	First Named Inventor	Der-Min Yuan
	Art Unit	2135
	Examiner Name	N/A
	Attorney Docket Number	ETRP0395USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ See attached certification statement.

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☒ None

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2021-06-24
Name/Print	Winston Hsu	Registration Number	41526

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/213,133	03/25/2021	Der-Min Yuan	ETRP0395USA3

CONFIRMATION NO. 9765

PUBLICATION NOTICE

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27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

Title:DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Publication No.US-2021-0217451-A1
Publication Date:07/15/2021

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	1	102187323	CN	A	2011-09-14			Abstract
	2	201123198	TW		2011-07-01			Abstract

NON-PATENT LITERATURE DOCUMENTS

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	1	Iyer, S.S.; IBM Corp., East Fishkill, NY, USA; Kalter, H.L., "Embedded DRAM technology: opportunities and challenges", Spectrum, IEEE (Volume: 36, Issue: 4), Apr. 1999, IEEE, pages 56-64.	

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Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2021-06-24
Name/Print	Winston Hsu	Registration Number	41526

Abstract of CN102187323

Dynamic utilization of power-down modes in multi-core memory modules

ABST:

Various embodiments of the present invention are directed to methods that enable a memory controller to choose a particular operation mode for virtual memory devices of a memory module based on dynamic program behavior. In one embodiment, a method for determining an operation mode for each virtual memory device of a memory module includes selecting a metric

(1001) that provides a standard by which performance and/or energy efficiency of the memory module is optimized during execution of one or more applications on a multicore processor. For each virtual memory device (1005), the method also includes collecting usage information (1006) associated with the virtual memory device over a period of time, determining an operation mode (1007) for the virtual memory device based on the metric and usage information, and entering the virtual memory device into the operation mode

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代理人 李娜 王洪斌

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G06F 12/08 (2006.01)
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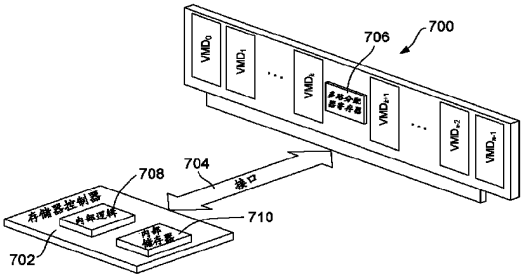
权利要求书 2 页 说明书 11 页 附图 16 页

(54) 发明名称

多核存储器模块中的功率下降模式的动态利用

(57) 摘要

本发明的各个实施例涉及使得存储器控制器能够基于动态程序行为针对存储器模块的虚拟存储器设备选择特定操作模式的方法。在一个实施例中，用于确定存储器模块的每个虚拟存储器设备的操作模式的方法包括选择提供标准的度量(1001)，按照该标准优化存储器模块的性能和/或能量效率。对于每个虚拟存储器设备(1005)，该方法还包括在一定的时间段内收集与虚拟存储器设备相关的使用信息(1006)，基于度量和使用信息确定虚拟存储器设备的操作模式(1007)，以及使得虚拟存储器设备进入该操作模式。



CN 102187323 A

1. 一种确定用于存储器模块的每个虚拟存储器设备的操作模式的方法，包含：

选择提供标准的度量（1001），按照该标准在多核处理器上的一个或多个应用的执行过程中优化所述存储器模块的性能和／或能量效率；以及

对于每个虚拟存储器设备（1005）：

在一定的时间段内收集与所述虚拟存储器设备相关的使用信息（1006）；

基于所述度量和使用信息确定所述虚拟存储器设备的操作模式（1007）；以及

使得所述虚拟存储器设备进入所述操作模式（1103，1105，1107，1108）。

2. 根据权利要求 1 所述的方法，其中该度量还包含最小总执行时间、最小总能量消耗、最小能量延迟乘积或者能够按照其来优化存储器模块的性能和／或能量效率的另一合适标准。

3. 根据权利要求 1 所述的方法，其中选择度量为最小总执行还包含对于不同时间段重复权利要求 1 的步骤。

4. 根据权利要求 1 所述的方法，还包含：

在所述一个或多个应用的执行过程中改变度量；以及

运行时系统，其配置成接收与所述一个或多个应用的存储器访问模式或所需存储量有关的特性信息和所述度量，解释该度量和特性信息，且指导存储器控制器使得每个虚拟存储器设备进入合适的操作模式。

5. 根据权利要求 1 所述的方法，其中该使用信息还包含确定以下项中的一个或多个：

当存储器控制器在该时间段内接收足够数目的存储器请求时存储器请求的频率；

在该时间段内的存储器请求的数目与执行的指令数目的比率；

分配给优于另一操作模式而选择一个操作模式的惩罚；

编译器向存储器控制器提供的与应用相关的存储器访问的频率；以及

应用在运行时确定的且发送到存储器控制器的存储器访问的频率。

6. 根据权利要求 1 所述的方法，其中选择度量还包含以下项之一：

计算机系统操作员选择度量；

一个或多个应用被编程为选择度量；

操作系统选择度量；以及

系统管理程序或运行时系统的其他元件调度、监控且支持运行时应用。

7. 根据权利要求 1 所述的方法，其中收集使用信息还包含存储器控制器（702）存储在该时间段内访问虚拟存储器设备的次数。

8. 根据权利要求 1 所述的方法，其中确定用于虚拟存储器设备的操作模式还包含：

基于度量确定至少一个阈值（1101）；以及

将使用信息与所述至少一个阈值进行比较（1102，1104，1106），其中当使用信息大于所述至少一个阈值时，使得该虚拟存储器设备进入待机模式（1108），否则使得该虚拟存储器设备进入节能模式（1103，1105，1107）。

9. 根据权利要求 8 所述的方法，其中当节能模式还包含至少一个功率下降模式时，每个功率下降模式与所述至少一个阈值之一相关。

10. 根据权利要求 9 所述的方法，其中当使用信息大于第一阈值且小于第二阈值时，使得虚拟存储器设备进入与第二阈值相关的功率下降模式。

11. 根据权利要求 1 所述的方法，其中该操作模式还包含当虚拟存储器设备不处理存储器请求且存储器模块的性能的优先级高于节省能量时的待机模式。

12. 一种系统，包含：

存储器控制器；以及

存储器模块，其包含至少一个虚拟存储器设备和连接到每个虚拟存储器设备和存储器控制器的多路分配器寄存器，其中该存储器控制器基于在一定的时间段内收集的使用信息的水平和度量使得至少一个虚拟存储器设备进入操作模式。

13. 根据权利要求 13 所述的系统，其中该虚拟存储器设备还包含一个或多个存储器芯片。

14. 根据权利要求 13 所述的系统，其中该度量还包含最小总执行时间、最小总能量消耗、最小能量延迟乘积或者能够按照其来优化存储器模块的性能和 / 或能量效率的另一合适标准。

15. 根据权利要求 13 所述的系统，其中操作模式还包含以下之一：

节能模式；以及

待机模式。

多核存储器模块中的功率下降模式的动态利用

技术领域

[0001] 本发明的实施例涉及存储器模块，且具体而言，涉及基于程序的动态操作使得存储器模块的独立虚拟存储器设备进入不同操作模式的方法。

背景技术

[0002] 在现代计算机系统中，对于存储器容量和带宽的需求保持增长。微处理器的近来的性能扩展取决于增加每芯片内核的数量，并且多核和很多内核的单芯片多处理器（“CMP”）通过每处理器多个存储器控制器而要求甚至更高的存储器带宽和容量。因此，主存储器模块的功率预算变得与当前计算机系统中的处理器的功率预算相似，或者甚至高于当前计算机系统中的处理器的功率预算。

[0003] 然而，典型的存储器模块是能量低效的。例如，当多个存储器模块连接到处理器的存储器控制器时，存储器模块的待机能量是总的主存储器能量使用的重要部分。当存储器模块并不积极响应于存储器请求时，大多数存储器模块是空闲的，在它们等待下一次存储器请求的同时使用待机能量，这是能量的低效使用。在很多当前存储器芯片中提供多种功率下降（power-down）模式以节省待机能量，且系统软件和硬件均使用这些功率下降模式来节省待机能量。然而，节省的功率量有限，因为相同的功率下降模式必须应用于模块中的所有存储器芯片。

[0004] 希望使得能够对存储在存储器系统中的信息进行访问的存储器系统和方法，所述存储器系统节省能量而不明显牺牲系统性能。

发明内容

[0005] 本发明的各个实施例涉及使得存储器控制器能够基于动态程序行为针对存储器模块的虚拟存储器设备选择特定操作模式的方法。在一个实施例中，用于确定存储器模块的每个虚拟存储器设备的操作模式的方法包括选择提供标准的度量，按照该标准，在多核处理器上的一个或多个应用的执行过程中，优化存储器模块的性能和／或能量效率。对于每个虚拟存储器设备，该方法还包括在一定的时间段内收集与虚拟存储器设备相关的使用信息，基于所述度量和使用信息确定虚拟存储器设备的操作模式，以及使得虚拟存储器设备进入该操作模式。

附图说明

[0006] 图 1A 示出具有八个存储器芯片的存储器模块的等距视图。

[0007] 图 1B 示出电路板上安装的存储器模块和存储器控制器的等距视图。

[0008] 图 2 示出构成存储器芯片的八个存储体（bank）的示意性表示。

[0009] 图 3A 示出传统存储器模块的示意性表示。

[0010] 图 3B 示出将命令广播到传统存储器模块的所有存储器芯片的示例。

[0011] 图 4A 示出根据本发明实施例配置的单个多核存储器模块的等距视图。

[0012] 图 4B 示出根据本发明实施例的电路板上安装的多核存储器模块和存储器控制器的等距视图。

[0013] 图 5A-5D 示出根据本发明的实施例配置的多核、双列直插存储器模块的一般示意性表示。

[0014] 图 6 示出根据本发明的实施例配置的示例性多核、双列直插存储器模块的示意性表示。

[0015] 图 7 示出根据本发明的实施例的电子地连接到存储器控制器的多核双列直插存储器模块。

[0016] 图 8A 示出条形图，该条形图呈现针对根据本发明的实施例的图 7 中示出的多核双列直插存储器模块的每个虚拟存储器设备的使用信息。

[0017] 图 8B 示出根据本发明的实施例的处于不同节能模式的图 7 中示出的多核双列直插存储器模块的三个虚拟存储器设备。

[0018] 图 9A 示出图 8A 中示出的条形图，其中根据优化根据本发明实施例的图 7 中示出的多核双列直插存储器模块的总执行时间来调节阈值。

[0019] 图 9B 示出根据本发明的实施例的处于节能模式的图 7 中示出的多核双列直插存储器模块的一个虚拟存储器设备。

[0020] 图 10 示出根据本发明的实施例的用于使得存储器模块的虚拟存储器设备动态地进入功率下降模式的方法的控制流程图。

[0021] 图 11 示出根据本发明的实施例的图 10A 的方法的子例程的控制流程图。

具体实施方式

[0022] 本发明的各种实施例涉及使得存储器控制器能够基于动态程序行为针对存储器模块的存储器芯片选择特定操作模式的方法。例如，存储器控制器可以配置成使得在一定的时间段内接收许多存储器请求的某些存储器芯片进入待机模式，从而当这些存储器芯片不在使用中时，它们可以快速地对存储器请求做出响应。与之对照，存储器控制器还可以使得在相同时间段内经历相对较低活动的其他存储器芯片进入许多节能模式之一。方法实施例是灵活的，因为系统性能可以与能量效率均衡。术语“性能”表示在一定的时间段内存储器系统执行的工作量。等待时间、响应时间和带宽是可用于比较在对存储器系统或其他存储器系统进行改变之前和之后的存储器系统的性能的度量。方法实施例允许给性能赋予比能量效率更高的优先级，方式是通过指导存储器控制器以与当给能量效率赋予比性能更高的优先级时存储器控制器将使得进入节能模式的存储器芯片相比，使得更少的存储器芯片进入节能模式。

[0023] 本发明的方法实施例可以应用于传统存储器模块和多核存储器模块，其被设计为改善存储器系统的能量效率而对系统性能具有小的影响。多核存储器模块包括存储器芯片，所述存储器芯片被划分成称为“虚拟存储器设备”（“VMD”）的一个或多个存储器芯片的组。存储器芯片可以是动态随机存取存储器（“DRAM”）芯片。

[0024] 详细描述按以下方式组织。在第一小节中描述传统存储器模块的一般性说明。在第二小节中描述多核存储器模块的说明。在第三小节中描述本发明的方法实施例。

[0025] <u>存储器模块</u>

存储器模块典型地包括形成被称为“双列直插存储器模块”（“DIMM”）的存储单元的印制电路板上安装的若干 DRAM 芯片。图 1A 示出包括八个 DRAM 芯片的单个 DIMM 的等距视图。然后在电路板上安装一个或多个 DIMM，并且由存储器控制器控制该一个或多个 DIMM。图 1B 示出电路板 106 上安装的存储器 102 和存储器控制器 104 的等距视图。存储器 102 由插入四个 DIMM 插槽 112-115 的四个 DIMM 108-111 组成。存储器控制器 104 是计算机芯片或多核微处理器芯片的部分，其管理发送到 DIMM 108-111 以及从 DIMM 108-111 发送的命令和数据流，并且将存储器 102 与计算机系统的其他主要组件（例如中央处理单元）对接。每一 DIMM 经由接口 118 与存储器控制器 104 进行电通信。接口 118 是载送从存储器控制器 104 到存储器 102 的时钟信号和命令以及 DIMM 108-111 与存储器控制器 104 之间的数据信号的总线。数据信号在 DIMM 108-111 中的 DRAM 芯片与存储器控制器 104 之间并行地发送。接口 118 可以支持单数据率（“SDR”）、双数据率（“DDR”）以及更高的数据率传送。SDR 指的是每时钟周期发送数据一次，以及 DDR 指的是在计算机系统时钟信号的上升沿和下降沿都发送数据。存储器控制器 104 和 DIMM 108-111 可以被配置为：根据 SDR 和 DDR 发送并且接收数据。在 DDR 中通过使用时钟的两个沿，数据信号在相同的极限频率操作，相比单数据率传输使得数据传输率加倍。

[0026] DRAM 芯片将比特存储在由晶体管和电容器组成的被称为 DRAM 存储器单元的结构中。单个 DRAM 芯片中存在数十亿个单元，以及可以以被称为“存储体”的许多二维阵列的二维布置组织这些单元。图 2 示出构成 DRAM 芯片 200 的标为 0-7 的八个存储体的示意性表示。如图 2 的示例中所示，每一存储体经由交叉信号线连接到行解码器、感测放大器以及列解码器。例如，存储体 0 经由与 x 轴平行走线的信号线（例如信号线 204）连接到行解码器 202。存储体 0 还经由与 y 轴平行走线的信号线（例如信号线 210）连接到感测放大器 206 和列解码器 208。存储器单元位于信号线交点处。例如，存储器单元 212 位于信号 204 和 210 交叉的点处。

[0027] 从存储器控制器 104 发送到存储器 102 的命令包括 READ（读）、WRITE（写）、ACTIVATE（激活）、REFRESH（刷新）和 PRECHARGE（预充电）。命令由控制信号和地址信号组成。控制信号表示命令执行的操作，以及地址信号标识在其执行命令的 DRAM 芯片中的存储体地址和行地址或列地址。例如，ACTIVATE 命令由激活控制信号和标识在 DRAM 芯片内的哪个存储体和行执行 ACTIVATE 命令的存储体地址和行地址组成。READ 和 WRITE 命令由读取和写入控制信号以及标识在 DRAM 芯片中的哪个存储体和列执行 READ 和 WRITE 命令的存储体地址和列地址组成。

[0028] 在两个步骤中访问 DRAM 芯片 200 的存储体中存储的数据。首先，存储器控制器（未示出）发送指定 DRAM 芯片 200 的行地址和存储体地址的 ACTIVATE 命令。将典型地是存储体的 8K 比特或 16K 比特的行中的所有比特激活到存储体内的感测放大器中。其次，发送指定存储体地址和列地址的一个或多个 READ/WRITE 命令。数据总线的大小和突发长度确定每 READ/WRITE 事务传送的比特的数量。突发长度是控制在数据块的单个突发事务或高速传输中执行的 READ/WRITE 操作的数量的常见的存储器有关的基本输入／输出系统设置。典型地，将突发长度设置为 4 或 8。当 DRAM 芯片接收到例如存储器 READ 请求时，芯片通过跨接口 118 的信号线提供数据来进行响应。突发长度确定响应于存储器 READ 请求发送的数据块的大小。具有 64 比特宽的数据总线（即 64 个单端信号线或 128 个差分信号线）和被配

置为支持 4 的突发长度的 DRAM 芯片的存储器模块响应于来自存储器控制器的单个 READ 请求发送 32 字节(4x64 比特 =32 字节)的数据块。另一方面,具有 64 比特宽的数据总线和被配置为支持 8 的突发长度的 DRAM 芯片的存储器模块响应于来自存储器控制器的单个 READ 请求发送 64 字节(8x64 比特 =64 字节)的数据块。

[0029] 当在 DRAM 芯片的同一存储体中的两个不同行中读取数据时,在可以读取第二行中的数据之前,必须写回第一行,对位线充电,以及通过 PRECHARGE 命令以及 ACTIVATE 命令锁存第二行。PRECHARGE 命令将该行写回到 DRAM 存储体,因为 ACTIVATE 命令破坏性地读取,所以这是必须的。在 READ 命令、WRITE 命令、ACTIVATE 命令和 PRECHARGE 命令中,存储体地址由小数量的比特给出。在同一存储体中,在第一 ACTIVATE 和第二 ACTIVATE 命令之间,这些命令操作一般花费大约 50ns。因此,除非 ACTIVATE 命令与 PRECHARGE 命令之间存在很多 READ/WRITE 命令,否则命令 / 地址 / 数据总线经常保持空闲。然而,如果在不同存储体中读取数据,则因为两个不同存储体之间的 ACTIVATE 至 ACTIVATE 时间短了大约 8ns,所以可以流水线化到不同存储体的命令。因此,通过交错不同存储体中的请求可以实现更高的吞吐量,当 ACTIVATE 和 PRECHARGE 命令对之间不存在很多 READ/WRITE 命令时尤其如此。

[0030] 图 3A 示出包括其中每一个具有 8 比特数据总线的 8 个 DRAM 芯片的传统 DIMM 300 的示意性表示。方向箭头 302 表示从存储器控制器(未示出)发送到称为寄存器 304 的可选设备的命令的分送。寄存器 304 位于存储器控制器与 DRAM 芯片之间的总线上。寄存器 304 锁存来自存储器控制器的命令信号,然后以更好的信号质量和定时裕度将它们转发到每一 DRAM 芯片,以减少存储器控制器上的电负载并且保持命令信号的稳定性。寄存器 304 也可以缓冲命令,并且将时钟信号广播到 DRAM 芯片,以在每存储器控制器具有多个 DIMM 的系统中促进对不同 DIMM 的交叠访问。寄存器 304 通过总线将命令广播到所有 8 个 DRAM 芯片,如通过分支方向箭头 306 和 308 指示的那样。在其它传统存储器模块中,将命令广播到 DRAM 芯片而不用寄存器 304。

[0031] 图 3B 示出传统 DIMM 操作的示例。如图 3B 的示例中所示,DIMM 300 内的所有 DRAM 芯片从存储器控制器接收相同命令,并且激活阴影区域 310 表示的每一 DRAM 芯片中的相同行。结果,DIMM 300 内的所有 DRAM 芯片充当具有更宽数据路径和更大行的单个 DRAM 芯片。

[0032] 如上参照图 2 描述的那样,DRAM 芯片行的大小典型地是 8 (或 16K 比特)。为了读取缓存线或者将缓存线写入 DIMM,将 READ/WRITE 命令广播到所有 DRAM 芯片,并且每一 DRAM 芯片激活相同行。换句话说,在由 8 个 DRAM 芯片组成的典型 DIMM 中,每一 DRAM 芯片激活包括 8K 比特的相同行地址。因而,一次激活 DIMM 的 DRAM 单元的 8×8Kbit 或 64Kbit,这大于待读取或写入的缓存线的大小。典型的缓存线处于 64 字节或 512 比特的量级。因为典型地以缓存线粒度读取或写入 READ/WRITE 命令 DIMM,所以对于单个 READ 或 WRITE 事务,超过 99% 的被激活的 DRAM 单元不被使用,这是能量的低效使用。

[0033] <u>多核存储器模块</u>

多核存储器模块包含安装在印刷电路板上的分组成 VMD 的存储器芯片以及用于从存储器控制器接收命令的多路分配器寄存器(“多路分配器寄存器”)。在某些实施例中,存储器芯片可以是 DRAM 芯片。图 4A 示出根据本发明的实施例的包含布置在电路板 412 上的 8 个 DRAM 芯片 401-408 和多路分配器寄存器 410 的单个多核双列直插存储器模块 400 的等

距视图。DRAM 芯片 410-408 可以分组成包含一个或多个 DRAM 芯片的 VMD，其示例在下面更详细地描述。

[0034] 与传统 DIMM 一样，一个或多个 MCDIMM 可以安装在电路板上且通过存储器控制器控制。图 4B 示出根据本发明的实施例的安装在电路板 424 上的存储器 420 和存储器控制器 422 的等距视图。存储器 420 包含分别插入 DIMM 插槽 430-433 的 MCDIMM 426-429。MCDIMM 400 具有存储器控制器 422 和存储器模块 426-429 的多路分配器寄存器之间的接口 434。接口 434 包括从存储器控制器 422 到存储器 420 载送命令信号的总线以及在存储器控制器 422 和存储器 420 之间载送数据信号的数据总线。在该架构中，存储器控制器 422 发送的命令并不广播到存储器 420 的 DRAM 芯片。而是，存储器控制器 420 向 MCDIMM 426-429 的多路分配器寄存器发送命令。MCDIMM 426-429 中的每一个包括使得多路分配器寄存器能够直接向 VMD 发送命令的命令总线。

[0035] MCDIMM 与多核处理器兼容。例如，多个应用可以在多核处理器中并发地运行，其中每个内核运行一个多线程应用，且多核处理器中的存储器控制器服务于仅仅一个应用的请求。

[0036] 图 5A 示出根据本发明的实施例配置的 MCDIMM 500 的一般示意性表示。MCDIMM 500 包括 n 个 VMD，其中 n 是代表 MCDIMM 500 中的 VMD 的数目的整数。8 个 VMD 在图 5A 中示出且由 VMD_k 表示，其中下标 k 是范围从 1 到 n 的整数。MCDIMM 500 配置成使得每个 VMD 经由信号线的分离集合连接到多路分配器寄存器 502。下面参考图 5B 和 5C 描述多路分配器寄存器 502 的两个不同实施例。例如，VMD_0、VMD_1、VMD_k、VMD_{k-1}、VMD_{n-2} 和 VMD_{n-1} 经由信号线集合 504-509 连接到多路分配器寄存器 502。将 VMD 连接到多路分配器寄存器 502 的信号线的组合集合被称为“命令总线”。每个 VMD 可以由一个或多个存储器芯片（诸如 DRAM 芯片）组成。从存储器控制器（未示出）发送到 MCDIMM 500 的命令通过称为“命令路径”的信号线集合 510 到达多路分配器寄存器 502。每个 VMD 在通过双头箭头（诸如双头箭头 511）在图 5A 中标识的分离数据总线上与存储器控制器交换数据。

[0037] 图 5B 示出根据本发明的实施例配置的第一多路分配器寄存器 525 的示意性表示。多路分配器寄存器 525 由寄存器 512 和多路分配器 514 组成。多路分配器寄存器 525 经由图 5A 的命令路径 510 从存储器控制器接收命令。命令是时分复用的。换句话说，每个命令被编码在比特流中，所述比特流在固定的持续时间时隙中从存储器控制器发送到多路分配器寄存器 525。在图 5B 中，时分复用的命令的时隙由一系列矩形 515-520 表示。图 5B 中表示的每个命令包括意欲接收该命令的图 5A 中的 VMD 的索引。命令被发送到多路分配器寄存器 525 的顺序由存储器控制器确定。因而，在图 5B 中，命令以该顺序出现。嵌入在命令中的是标识待执行的特定种类的操作的控制信号、标识存储体、行或列的地址信号以及标识由存储器控制器分配为接收命令的特定 VMD 的 VMD 地址。例如，当命令要被发送到特定 VMD 时，存储器控制器创建包括标识该 VMD 的 VMD 地址的命令。一般而言，VMD 地址是包含 $\log_2 n$ 个比特的比特串。

[0038] 寄存器 512 是接收且临时存储命令的缓冲器。多路分配器 514 包括两个输入。如方向箭头 522 和 524 所表示的，寄存器向一个输入发送命令且向另一输入发送 VMD 地址。多路分配器 514 使用 VMD 地址来选择通向由 VMD 地址标识的 VMD 的命令总线的信号线的适当集合。在图 5B 中，命令总线的信号线的 n 个集合中的 6 个通过对应于信号线集合 504-509

的方向箭头 504-509 表示，且使用图 5A 中示出的相关 VMD 的索引进行标记。注意，在处理后续命令之前，每个命令在特定时间间隔内被多路分配器寄存器 525 单独处理。

[0039] 例如参考图 5A-5B，考虑存储器控制器向 VMD_k 发送命令 k+1 519。在图 5A 中，命令 k+1 519 沿着命令路径 510 被发送到多路分配器寄存器 525。如图 5B 所示，寄存器 512 接收且临时存储命令 k+1 519，且 VMD 地址和命令被发送到多路分配器 514，其然后选择信号线的适当集合 506 来向图 5A 中的 VMD_{k+1} 发送命令 k+1 519。在发送命令 k+1 519 之后，下一命令 1 518 以类似的方式被处理。

[0040] 如图 5B 所示，多路分配器寄存器 525 可选地包括与每个信号线集合相关的计数器。当 VMD 的 DRAM 芯片不能支持与缓存线的 READ 或 WRITE 事务相关的长突发长度时，可能需要计数器。多路分配器寄存器将缓存线划分为缓存线片段且将命令转换为多个命令，每个命令对应于缓存线片段。因而，由计数器发送的对应命令在发送到 VMD 的每个缓存线片段之前。例如，当不能将 VMD 的一个或多个 DRAM 芯片的突发长度设置得足够长以覆盖缓存线时，计数器将列级别命令（例如 READ 或 WRITE）转换为用于每一缓存线片段的若干 READ/WRITE 命令，从而可以分离地读取每一缓存线片段或将每一缓存线片段写入到 DRAM 芯片。每一计数器包括跟踪为划分的缓存线生成的命令的数量的计数设备。计数器执行的转换节省了来自存储器控制器的命令带宽。

[0041] 图 5C 示出根据本发明的实施例配置的第二多路分配器寄存器 527 的示意性表示。多路分配器寄存器 527 包含标为 0 至 n-1 的 n 个命令选择器以及广播总线 528，对于图 5A 中示出的 n 个 VMD 中的每一个都有一个命令选择器。如上面参考图 5B 所描述的，存储器控制器在命令路径 510 上向多路分配器寄存器 527 发送时分复用命令 515-520。命令选择器经由支路 529-534 电子地连接到广播总线 528，且每个命令选择器经由命令总线中的某个信号线集合连接到 VMD 之一。在图 5C 中，命令总线中的信号线的 n 个集合中的 6 个由对应于信号线集合 504-509 的方向箭头 504-509 表示且使用图 5A 示出的相关 VMD 的索引进行标记。如图 5C 所示，每个命令被广播到所有的 n 个命令选择器。每个命令选择器配置成提取嵌入在命令中的 VMD 地址以确定命令是否要被转发到对应的 VMD 或命令是否被寻址到不同 VMD，在命令被寻址到不同 VMD 的情况下，命令被丢弃。因而，对于广播到所有 n 个命令选择器的每个命令而言，该命令仅被命令选择器之一发送到对应的 VMD。例如，多路分配器寄存器 527 接收命令 n-2 520 且将其广播到所有 n 个命令选择器 0 至 n-1。然而，因为命令 n-2 520 包括 VMD_{n-2} 的地址，所以命令选择器 n-2 通过信号线集合 508 将命令 n-2 520 发送到 VMD_{n-2} 且其他命令选择器丢弃命令 n-2 520。注意，在处理后续命令之前，每个命令在特定时间间隔内被多路分配器寄存器 527 单独处理。

[0042] 图 5D 示出根据本发明的实施例配置的示例性命令选择器 n-2 的示意性表示。其他的 n-1 个命令选择器被类似配置。命令选择器 n-2 包含 AND（与）门 530、寄存器 / 计数器 532 以及随机存取存储器（“RAM”）定时控制 534。命令在支路 533 上被输入到命令选择器 n-1。AND 门 530 提取嵌入在每个命令中的 VMD 地址且接收系统时钟信号。AND 门 530 配置成在提取的 VMD 地址匹配对应的 VMD_{n-2} 的地址时向寄存器 / 计数器 532 发送选择信号。AND 门 530 接收时钟信号以确定寄存器 / 计数器何时锁存命令，且 AND 门 530 可以配置成在每个上升和 / 或下降时钟沿发送选择信号。寄存器 / 计数器 532 是在从 AND 门 530 接收到选择信号时临时存储命令且向对应的 VMD_{n-2} 发送命令的缓冲器。寄存器 / 计数器 532 还包

括如上面参考图 5B 所描述的执行缓存线和命令划分的计数器。RAM 定时控制 534 控制寄存器 / 计数器 532 的计数器部分。

[0043] 一般而言，AND 门在所有输入信号对应于比特“1”时输出对应于比特“1”的信号且在输入信号中的至少一个对应于比特“0”时输出对应于比特“0”的信号，其中比特“1”和“0”可以分别代表信号的高和低电压。命令选择器 0 至 n-1 的 AND 门可以包括某些输入信号线上的反相器。反相器将与比特“0”相关的信号转变成与比特“1”相关的信号且反之亦然。AND 门包括某些输入信号线上的反相器以将代表对应 VMD 的 VMD 地址转变成包含全“1”比特的比特流。AND 门然后向寄存器 / 计数器 532 输出对应于比特“1”的选择信号。例如，假设 VMD_{n-2} 的 VMD 地址包含比特流 11…1101。AND 门 530 包括反相器 536，其反转在线 538 上进入 AND 门 530 的信号的电压。因而，如图 5D 所示，当嵌入在命令中的 VMD 地址匹配地址 11…1101 时，地址被转变成 11…1111，且 AND 门 530 与时钟信号结合地向寄存器 / 计数器 532 输出代表比特“1”的选择信号，寄存器 / 计数器 532 锁存命令到信号线集合 508 上。对于其他地址，进入 AND 门 530 的比特流包括至少一个“0”比特，且 AND 门 530 不输出信号或者输出对应于比特“0”的低信号。因而，寄存器 / 计数器 532 不锁存命令到信号线集合 508 上。

[0044] 图 6A 示出根据本发明的实施例配置的 MCDIMM 600 的示意性表示。MCDIMM 600 包括由 VMD_k 标识的 4 个 VMD 以及多路分配器寄存器 602，其中 k 是范围从 0 到 3 的整数。每个 VMD 包含两个 DRAM 芯片，且多路分配器寄存器 602 可以如上面参考图 5B-5D 描述的那样被配置和操作。命令总线 MCDIMM 600 包含将每个 VMD 的 DRAM 芯片连接到多路分配器寄存器 602 的四个信号线集合 604-607。命令沿着命令路径 608 从存储器控制器(未示出)发送到多路分配器寄存器 602。根据 $\log_2 n$，其中 n 等于 4，VMD 可以被分配两比特 VMD 地址 00、01、10 和 11 之一，所述地址包括在命令中以标识意欲接收该命令的 VMD。每个 VMD 通过命令总线接收不同的命令且经由双头箭头(诸如双头箭头 610)所表示的其自己的数据总线独立于其他 VMD 传输数据。

[0045] 在图 6A-6B 的示例性 MCDIMM 600 中，每个存储器请求涉及两个 DRAM 芯片。DRAM 芯片对的等同阴影区域表示与不同命令相关的不同独立存储器请求。每个 VMD 通过命令总线接收命令且使用其自己的数据总线独立传输数据。因而，通过比传统 DIMM (见伴随图 3 的描述)激活更少的比特来节省能量。然而，与传统 DIMM 相比，因为数据总线大小小于传统 DIMM 中的数据总线大小，可能需要更多的时间来传送数据。例如，数据可以被划分成较小的串行化数据部分，其中每个部分通过 VMD 总线单独被发送到存储器控制器。以这种方式串行化数据增加了使用传统 DIMM 发送数据所需的时间量。该附加串行化等待时间问题可能对系统性能具有负面影响。

[0046] <u>本发明的方法实施例</u>

下面参考动态地改变 MCDIMM 的各个 VMD 的能量消耗描述本发明的方法实施例。存储器芯片可以进入若干不同的操作模式。例如，存储器芯片可以响应于存储器请求而进入活动(active)模式。当存储器芯片不再处理存储器请求时，存储器芯片可以进入待机模式，其中存储器芯片被提供以待机能量，该待机能量低于活动地处理存储器请求所需的能量，但是高得足以维持内部存储器芯片组件的操作，使得存储器芯片能够快速响应于另一存储器请求。然而，当每存储器通道存在多个存储器模块时，处于待机模式中的存储器芯片消耗

发送给存储器模块的总能量的显著部分。

[0047] 通过使得临时不在使用中的存储器芯片进入节能模式可以节省待机能量。处于节能模式中的存储器芯片必须被加电(power up),这增加了响应时间。例如,功率下降模式是通过关闭很多内部存储器芯片组件来节省能量的一种节能模式,然而,存在与该模式相关的很多性能限制。当存储器芯片处于功率下降模式时,正常的存储器芯片访问是不可能的,且存储器芯片必须被加电,因此进入和退出功率下降模式比进入和退出待机模式花费更多的时间。结果,使用功率下降模式典型地节省能量,但是导致较低的存储器系统性能。为了减小对存储器芯片加电所需的时间,很多存储器芯片还可以配置成具有多个功率下降模式。每个功率下降模式提供不同递增级别的能量节省。然而,能量节省的每个递增增加对应于对存储器芯片加电所需的更长的时间量。

[0048] 本发明的方法实施例对于运行在多核处理器上的一个或多个应用可以是透明的,因为挑选操作模式的决策可以完全由硬件做出,其还具有在运行时期间由编译器或一个或多个应用修改的灵活性。图 7 示出根据本发明的实施例的经由接口 704 电子地连接到存储器控制器 702 的 MCDIMM 700。MCDIMM 700 包含如上参考图 5A 描述的那样配置的多路分配器寄存器 706 和 n 个 VMD。如图 7 所示,存储器控制器 702 配置有内部逻辑 708 和内部储存器 710。关于每个 VMD 的使用的信息可以存储在内部储存器 710 中,且本发明的方法可以完全由存储器控制器内部逻辑 708 执行。

[0049] 方法实施例包括在运行在多核处理器上的一个或多个应用的运行时期间优化存储器模块的性能和/或能量效率。计算机系统操作员、一个或多个应用或者操作系统选择提供标准的度量,按照该标准优化存储器模块的性能和/或能量效率。该度量可以是最小总执行时间(“TET”)、最小总能量消耗(“TEC”)、最小能量延迟乘积(“EDP”)或可以按照其来优化存储器模块的性能和/或能量效率的任意其他合适标准。设置度量以最小化一个或多个应用的 TET 允许所述应用几乎全带宽地访问存储器模块提供的存储容量。换句话说,当存储器芯片并不活动地处理存储器请求时,不是使得存储器芯片进入功率下降模式,而是使得存储器芯片进入待机模式,从而存储器芯片能够快速响应于下一存储器请求。因而,TET 是性能度量。另一方面,设置度量为 TEC 通过以下方式减小了针对每个存储器请求的容易可用的存储器芯片的数目:使得这些存储器芯片进入节能模式,这减小了带宽且延迟了存储器响应时间但是提供了优于设置度量为 TET 的能量节省。设置度量为最小化 EDP 提供了 TET 和 TEC 之间的折衷。EDP 度量被定义为与存储器请求相关的能量和延迟的乘积。EDP 可用于在给定性能水平提供最小能量,或者针对相同的能量提供更多的性能。

[0050] 一旦选择了度量,就确定在一个或多个应用的运行期间与每个 VMD 的使用有关的信息。使用信息被收集且存储在存储器控制器 702 中且可以包括以下项中的一个或多个:(1)当存储器控制器在一定的时间段内接收足够数量的存储器请求时每 VMD 的存储器请求的频率的记录;(2)在一定时间段内的存储器请求的数目与执行的指令数目的比率;(3)分配给优于另一操作模式而选择一个操作模式的惩罚;(4)编译器可以向存储器控制器 702 提供关于与它处理的一个或多个应用相关的每 VMD 的存储器访问的频率的信息;以及(5)运行时的一个或多个应用可以向存储器控制器 702 提供每 VMD 的存储器访问的频率的历史。

[0051] 存储器控制器将用于每个 VMD 的使用信息与一个或多个阈值进行比较且通过向

VMD 发送适当的命令而使得 VMD 进入对应的操作模式。例如，当与 VMD 相关的使用信息小于阈值时，存储器控制器使得 VMD 进入对应的功率下降模式，且当与 VMD 相关的使用信息大于阈值时，存储器控制器使得 VMD 进入待机模式。根据被选择用于优化存储器模块的使用的度量选择所述阈值。例如，本发明的实施例包括当度量设置为 TET 时，节能模式可以被绕过或者阈值可以被设置为低，使得很少的 VMD 进入节能模式。另一方面，通过设置度量为 TEC 或 EDP，阈值比与 TET 相关的阈值相对更高，使得若干 VMD 能够进入节能模式。

[0052] 本发明的实施例还包括运行在多核处理器上的一个或多个应用或者编译器向存储器控制器提供关于一个或多个应用的存储器访问模式或所需的存储器量的特性信息。特性信息和度量经由诸如操作系统或者虚拟机的运行时系统被发送到存储器控制器，所述虚拟机是类似于真实计算机的执行一个或多个应用的计算机的软件实现。运行时系统为存储器控制器解释度量和特性信息且可以指导存储器控制器选择用于应用的适当操作模式。例如，假设系统操作员在多个应用并发地运行在多核处理器的内核中的情况下选择 EDP 度量，其中应用作者或编译器提供的特性信息将大多数应用标识为频繁存储器访问应用。结果，运行时系统可以指导存储器控制器将 MCDIMM 配置为不使用功率下降模式，而不收集关于存储器访问的数目的统计信息。而且，调度、监控和支持运行应用的运行时系统的其他元件或系统管理程序可以指导存储器控制器配置 MCDIMM。

[0053] 图 8A 示出呈现根据本发明的实施例的 MCDIMM 700 的每个 VMD 的使用信息的条形图 800。图 800 的每一条可以代表在一定的时间段内访问 MCDIMM 700 的 VMD 的频率或次数。图 800 包括分别代表阈值 T_1、T_2 和 T_{max} 的三个虚线 801-803。所述阈值也与三个不同的功率下降模式 PDM_1、PDM_2 和 PDM_{max} 相关。PDM_{max} 通过关闭最大数量的内部存储器芯片组件比 PDM_1 和 PDM_2 节省更多的功率，但是要求最长的延迟时间来加电；PDM_1 通过关闭最少的内部存储器芯片组件提供最少的能量节省，但是要求最短的延迟时间来加电；且 PDM_2 提供 PDM_{max} 和 PDM_1 之间的能量节省且要求中间的延迟时间来加电。

[0054] 图 8A 中示出的阈值 T_1、T_2 和 T_{max} 801-803 可以代表通过设置度量为 TEC 或 EDP 确定的阈值。阈值代表可接受性能和能量效率之间的均衡。例如，条形图 800 揭示 VMD_0、VMD_2、VMD_k、VMD_{k+1}、和 VMD_{k-2} 全都具有超过阈值 T_1 的使用信息。换句话说，存储器控制器在一个或多个应用运行的时候经常使用这些 VMD。因而，不是使得这些 VMD 进入节能模式之一，当它们不活动地处理存储器请求时，存储器控制器使其进入待机模式。另一方面，如图 8B 所示，与 VMD_1 相关的使用信息小于 T_{max}，与 VMD_{n-3} 相关的使用信息大于 T_{max} 且小于 T_2，且与 VMD_{n-1} 相关的使用信息大于 T_2 且小于 T_1。因而，为了节省能量，存储器控制器使得 VMD_1 进入 PDM_{max}，使得 VMD_{n-3} 进入 PDM_2，且使得 VMD_{n-1} 进入 PDM_1，直到 VMD_1、VMD_{n-3} 和 VMD_{n-1} 被加电以响应于存储器请求为止。

[0055] 图 9A 示出条形图 800，其表示图 8A 中示出的 MCDIMM 700 的每个 VMD 的使用信息，但是阈值根据设置度量为 TET 而改变。注意表示与每个 VMD 相关的使用信息的条并未与图 8A 中示出的条有所不同。然而，因为度量变为 TET，图 8A 中表示的阈值 T_1、T_2 和 T_{max} 变为在图 9A 中由虚线 901-903 表示的阈值 T'_1、T'_2 和 T'_{max}。在该特定示例中，性能比能量效率更重要。因而，图 9A 揭示出仅一个 VMD 落在阈值之下。具体而言，与 VMD_1 相关的使用信息大于阈值 T'_2 且小于阈值 T'_1。存储器控制器使得 VMD_1 进入功率下降模式 PDM_1 达一定的时间段，直到 VMD_1 被加电以用于存储器请求为止。当剩余 VMD 不活动地处理存储器请求时，

存储器控制器使得这些 VMD 进入待机模式。

[0056] 在某些实施例中，存储器控制器可以选择使用哪个操作模式。在某些实施例中，当存储器被很频繁地使用或者性能更关键时，存储器控制器不使用节能模式。

[0057] 方法实施例是动态的，因为使用信息可以由存储器控制器定期地收集且与每个 VMD 相关的使用信息在一个或多个应用运行的时候被更新。结果，基于当前使用信息，VMD 可以在一个或多个应用运行的时候被定期地切换到不同操作模式，而不禁用存储器访问。另外，在某些实施例中，度量还可以在一个或多个应用运行的时候由计算机系统操作员改变。

[0058] 图 10 示出根据本发明的实施例的用于动态地使得存储器模块的 VMD 进入操作模式的方法的控制流程图。在步骤 1001，度量（诸如度量 TET、TEC 或 EDP）被选择以优化与运行一个或多个应用相关的存储器性能和 / 或能量消耗。如上所述，度量可以由计算机系统操作员、一个或多个应用或者操作系统选择。在步骤 1002，执行一个或多个应用。在步骤 1003，操作系统选择一个或多个内核来处理一个或多个应用。在步骤 1004，基于一个或多个应用的存储器要求，操作系统选择 MCDIMM 的一个或多个 VMD。在步骤 1005，根据度量和 / 或应用本身提供的特性信息，运行时系统可以指导存储器控制器到步骤 1006 且进入步骤 1006-1009 中实施的方法的节能部分。否则，运行时系统可以指导存储器控制器跳过方法的节能部分。例如，当一个或多个应用提供的特性信息将所述应用标识为频繁存储器访问应用时，运行时系统可以指导存储器控制器跳过步骤 1006-1009 中实施的方法的节能部分。在步骤 1006 的 for 循环中，针对存储器模块的每个 VMD 执行步骤 1007-1008。在步骤 1007，如上面参考图 7 所描述的，存储器控制器在一定的时间段内收集和存储 VMD 使用信息。在步骤 1008，存储器控制器基于度量和使用信息使得 VMD 进入操作模式，如下面在图 11 的控制流程图中描述的。例如，当 VMD 不活动地处理存储器请求时，存储器控制器可以使得 VMD 进入待机模式或者很多节能模式之一，如上面参考图 8-9 所述的。在步骤 1009，当所有 VMD 都进入操作模式时，前进到 1010，否则针对另一 VMD 重复步骤 1007 和 1008。在步骤 1010 中，当一个或多个应用的运行没有结束时，本发明的实施例可以可选地包括步骤 1011，否则当一个或多个应用结束运行时，前进到步骤 1012，其中针对不同组的一个或多个应用或者相同组的一个或多个应用的后续运行，重复步骤 1001-1009。在步骤 1011，在一个或多个应用仍在运行的时候，计算机系统操作员可以改变度量。例如，计算机系统操作员可以在步骤 1001 中初始设置度量为 TET，且稍后在一个或多个应用运行的时候改变度量为 TEC。

[0059] 图 11 示出根据本发明的实施例的用于动态地使得 VMD 进入功率下降模式的方法的控制流程图。在该实施例中，如参考图 8-9 所述，假设存储器芯片具有在步骤 1103、1105 和 1107 中表示的三个节能功率下降模式。在步骤 1101，如上面参考图 8-9 所述，基于图 10 的步骤 1001 中选择的度量确定对应于三个功率下降模式的阈值。存储器控制器使用在图 10 的步骤 1006 中收集和存储的使用信息在步骤 1102-1107 中选择一个或三个功率下降模式。功率下降模式是上面参考图 8A 所述的 PDM_1、PDM_2 和 PDM_{max}。在步骤 1102，当使用信息小于阈值 T_{max} 时，前进到步骤 1103，否则前进到步骤 1104。在步骤 1103，存储器控制器使得 VMD 进入 PDM_{max}。在步骤 1104，当使用信息小于阈值 T_2 时，前进到步骤 1105，否则前进到步骤 1106。在步骤 1105，存储器控制器使得 VMD 进入 PDM_2。在步骤 1106，当使用信息小于阈值 T_1 时，前进到步骤 1107，否则前进到步骤 1108。在步骤 1107，存储器控制器使得 VMD 进

入 PDM_1。在步骤 1108，存储器控制器使得 VMD 进入待机模式。在其他实施例中，存储器芯片可以配置有一个、两个或四个或更多不同的功率下降模式。

[0060] 为了解释的目的，前面的描述使用特定词汇来提供本发明的透彻理解。然而，本领域技术人员显而易见的是，为了实践本发明，并不需要具体细节。给出本发明具体实施例的前面描述，目的是进行说明和描述。它们并非意欲穷尽本发明或者将其限制为所公开的精确形式。显然，根据以上教导，很多修改和变化是可能的。示出并且描述实施例，以最佳地解释本发明的原理及其实际应用，由此使得本领域其他技术人员能够最佳地利用本发明以及具有适于所考虑的特定使用的各个修改的各个实施例。本发明的范围意欲由所附权利要求及其等同物所定义。

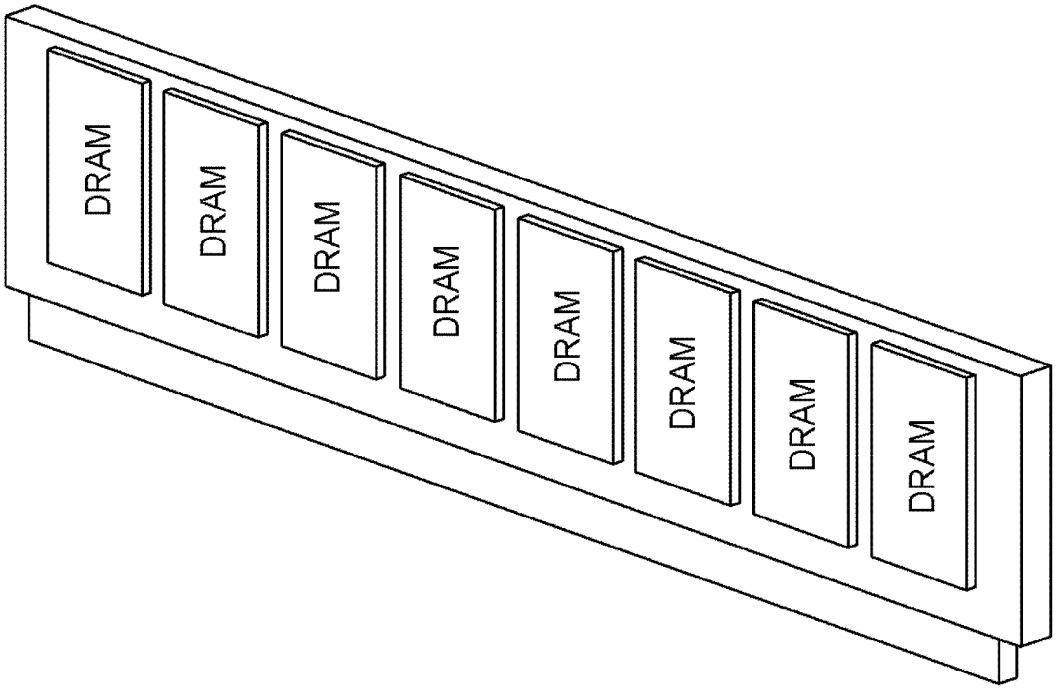


图 1A

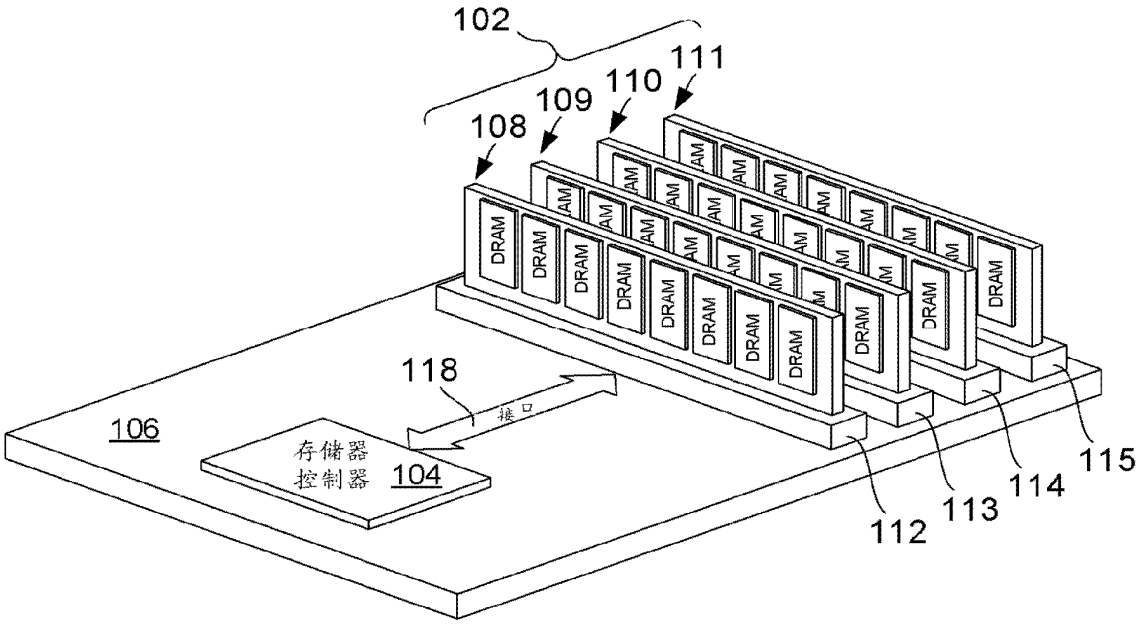


图 1B

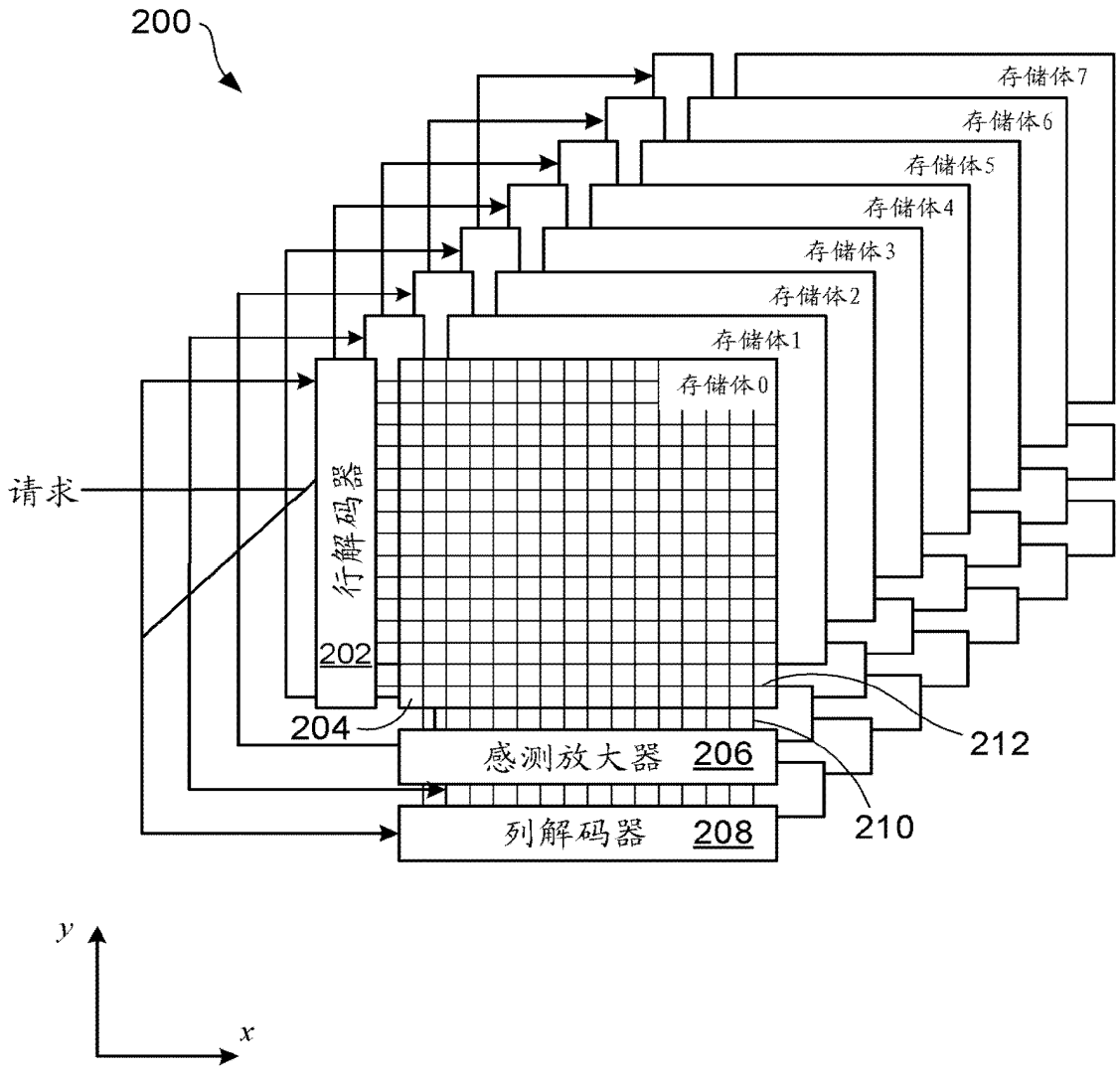

200
存储体7
存储体6
存储体5
存储体4
存储体3
存储体2
存储体1
存储体0
请求
行解码器
202
204
212
感测放大器 206
210
列解码器 208
y
x

图 2

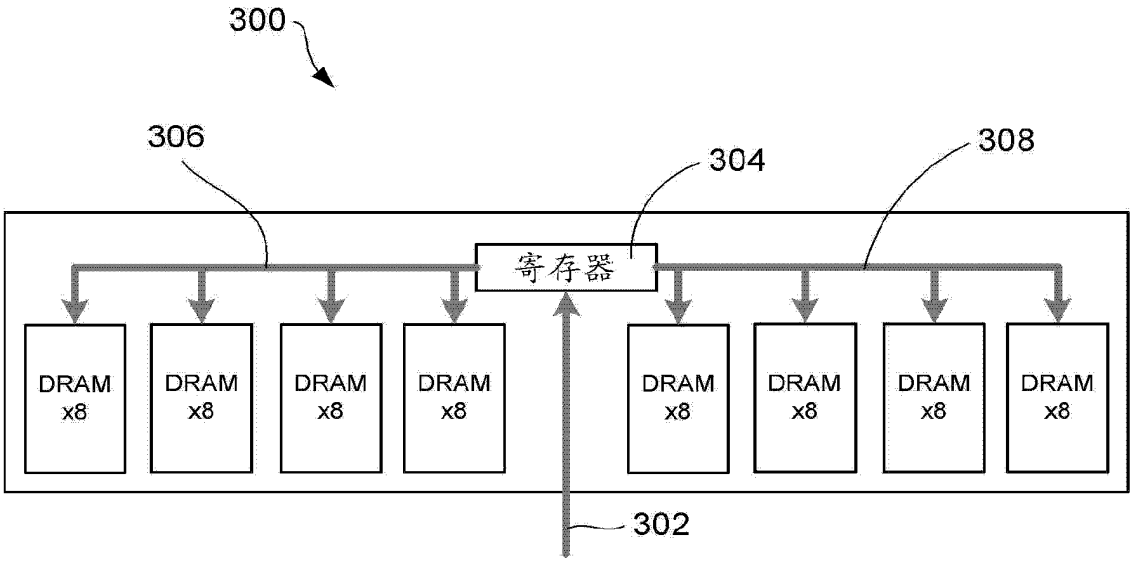

300
306
304
308
寄存器
DRAM x8
DRAM x8
DRAM x8
DRAM x8
DRAM x8
DRAM x8
DRAM x8
DRAM x8
302

图 3A

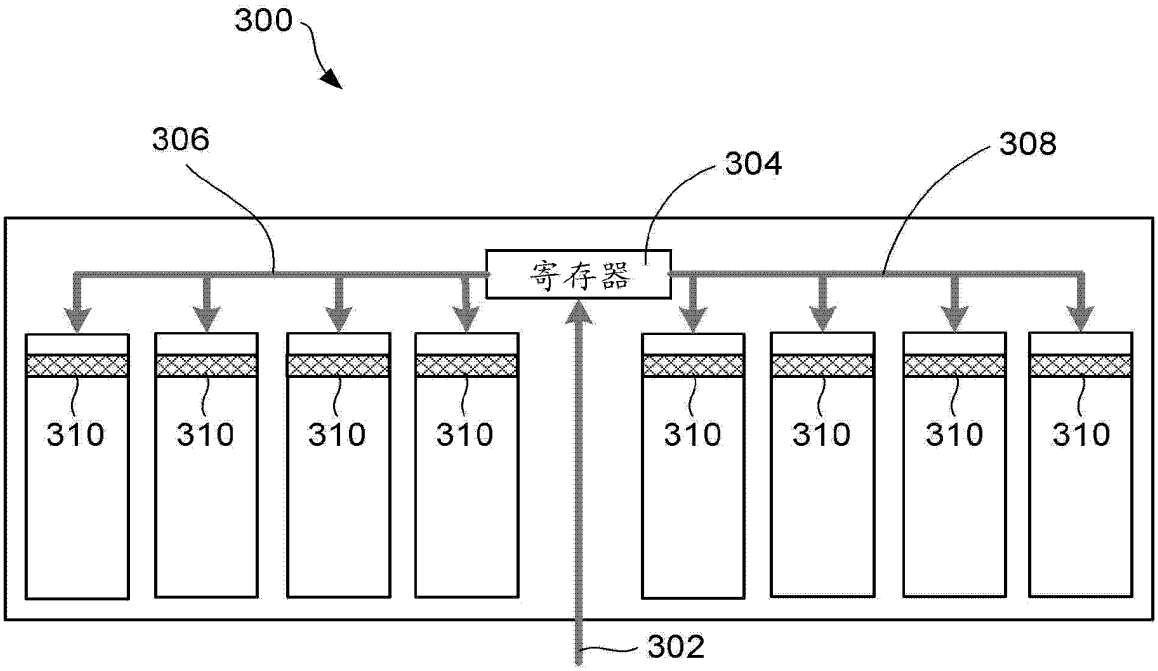

300
306
304
308
寄存器
310
310
310
310
310
310
310
310
302

图 3B

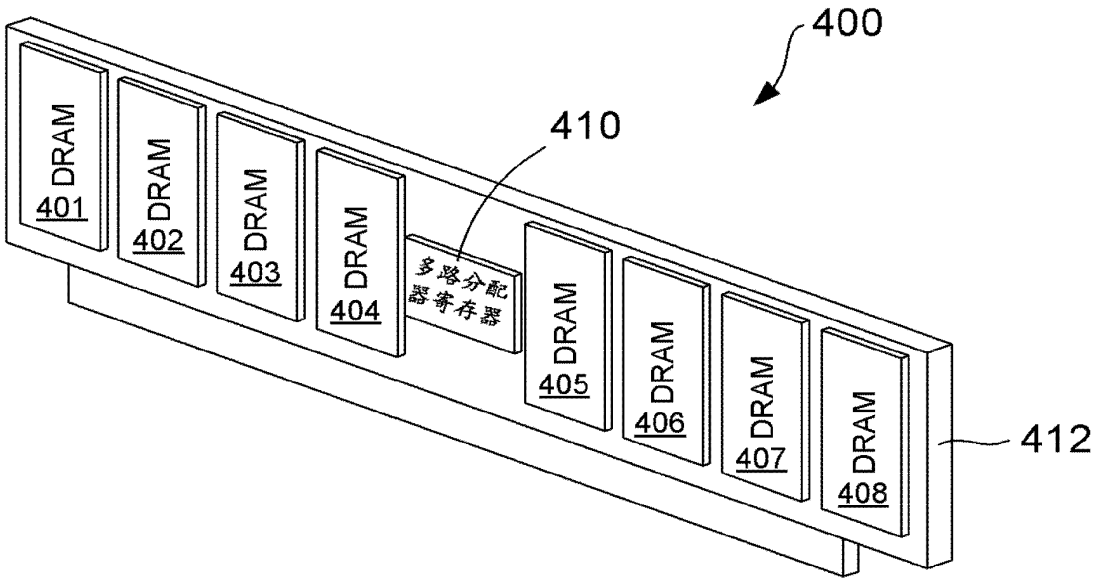

400
410
DRAM
401
DRAM
402
DRAM
403
DRAM
404
多路分配器寄存器
DRAM
405
DRAM
406
DRAM
407
DRAM
408
412

图 4A

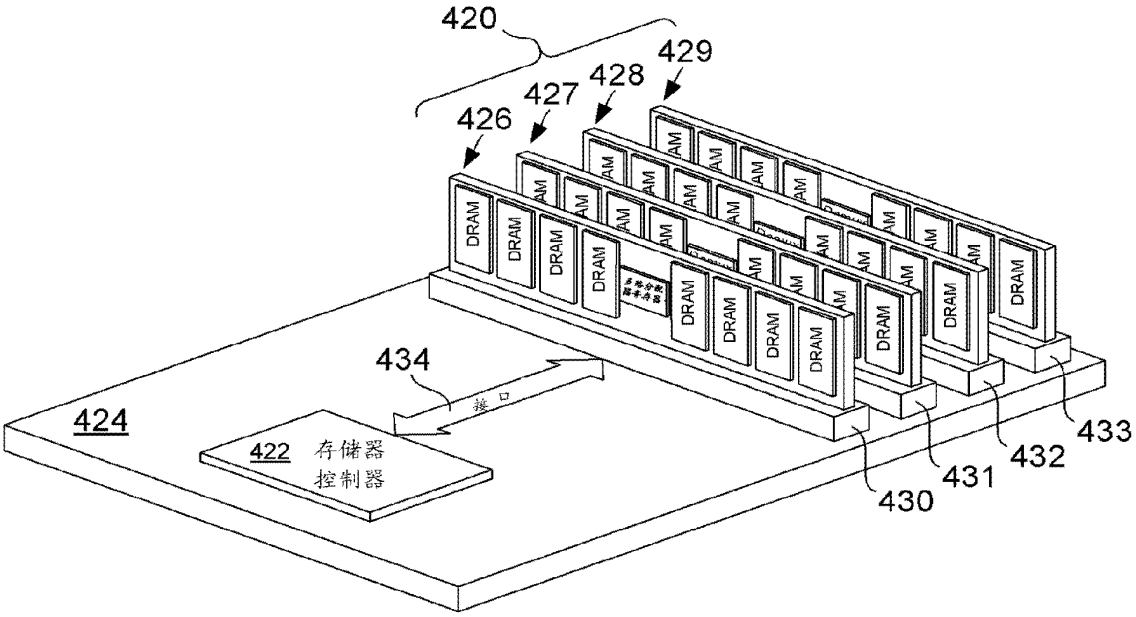

420
429
428
427
426
DRAM
AM
434
接口
424
422
存储器
控制器
430
431
432
433

图 4B

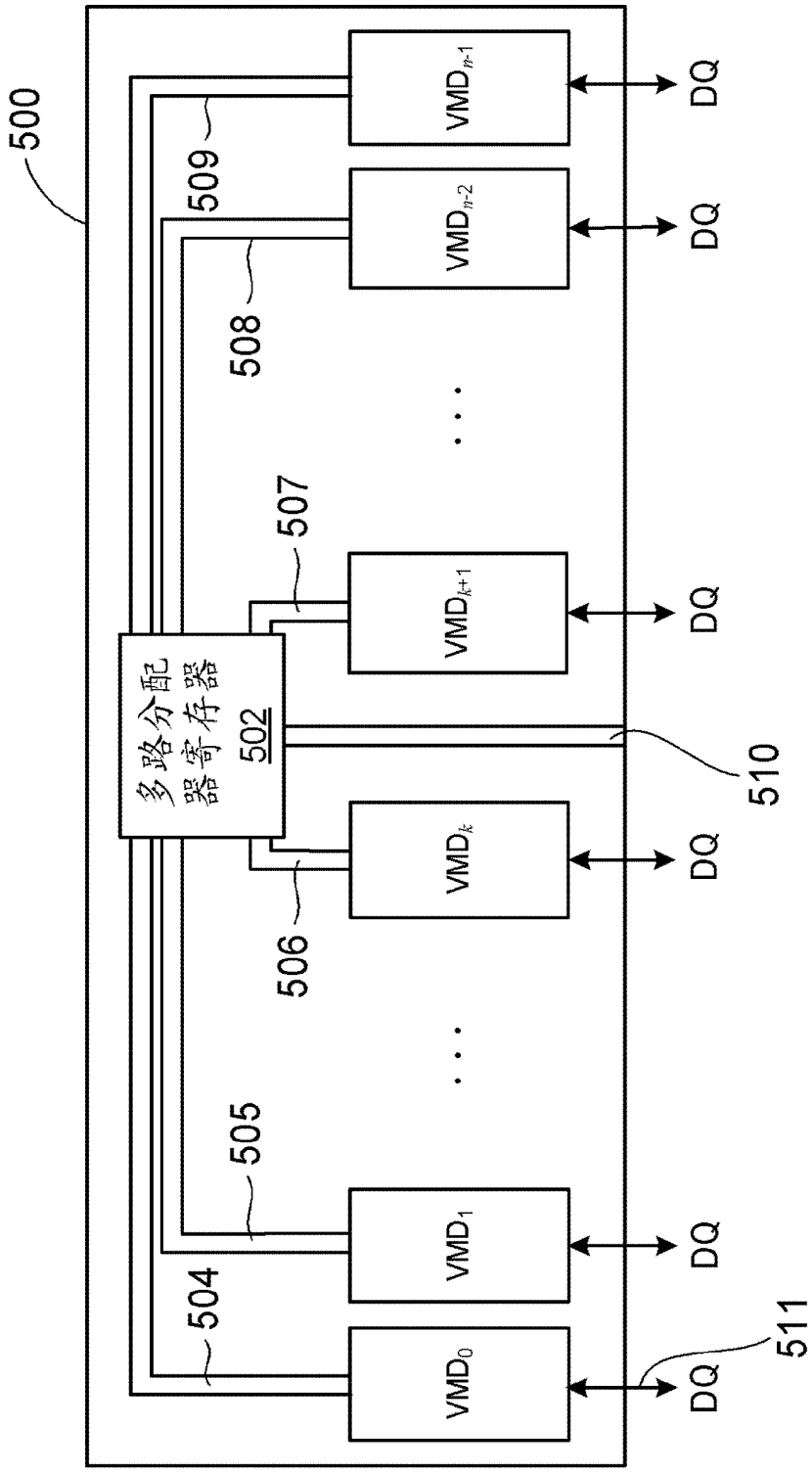

500
多路分配器寄存器
502
509
508
507
506
505
504
510
511
VMD0
VMD1
VMDk
VMDk+1
VMDn-2
VMDn-1
DQ
DQ
DQ
DQ
DQ
DQ

图 5A

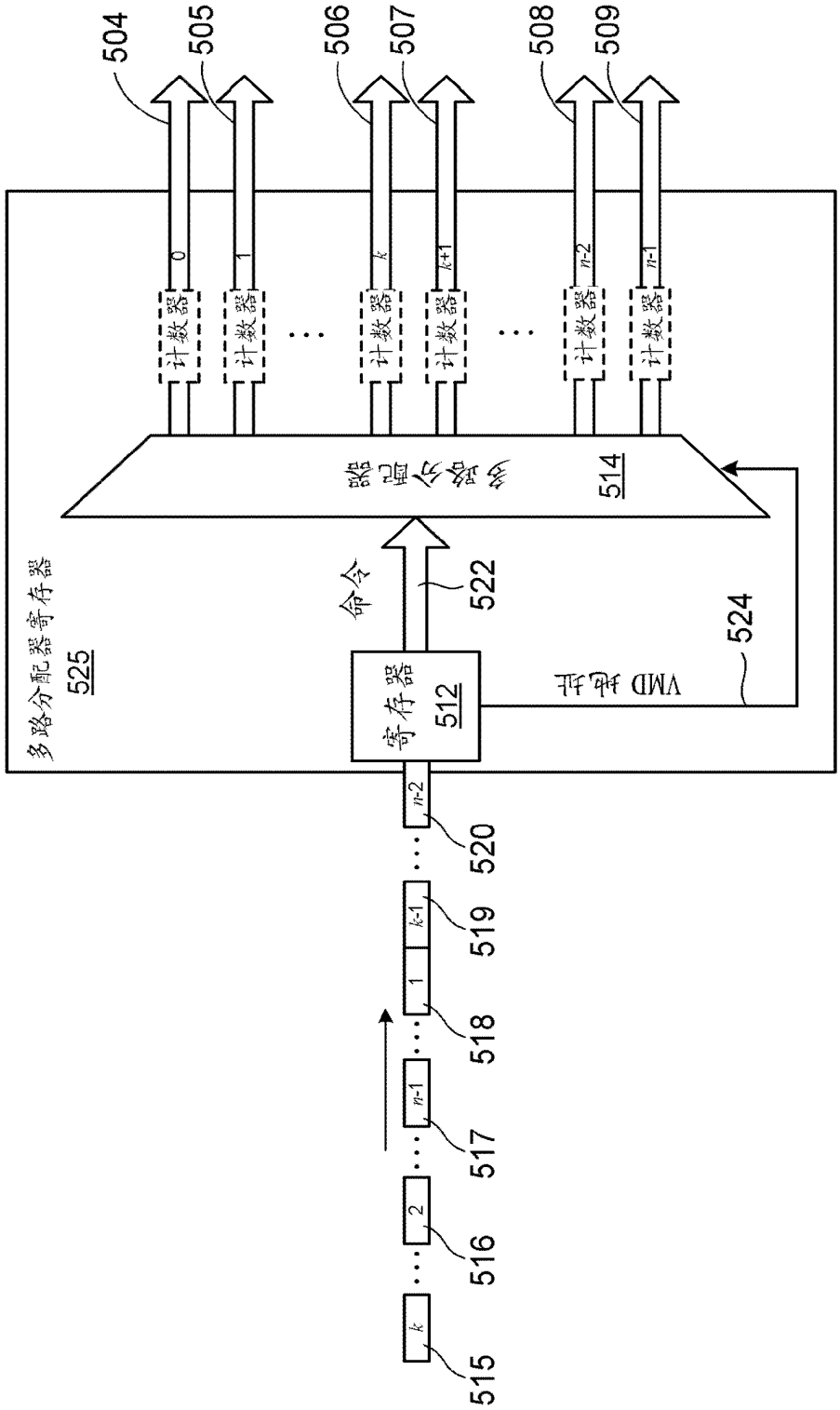

504
505
506
507
508
509
计数器
计数器
计数器
计数器
计数器
计数器
0
1
k
k+1
n-2
n-1
多路分配器
514
命令
522
524
多路分配器寄存器
525
寄存器
512
VMD 地址
n-2
520
k-1
519
1
518
n-1
517
2
516
k
515

图 5B

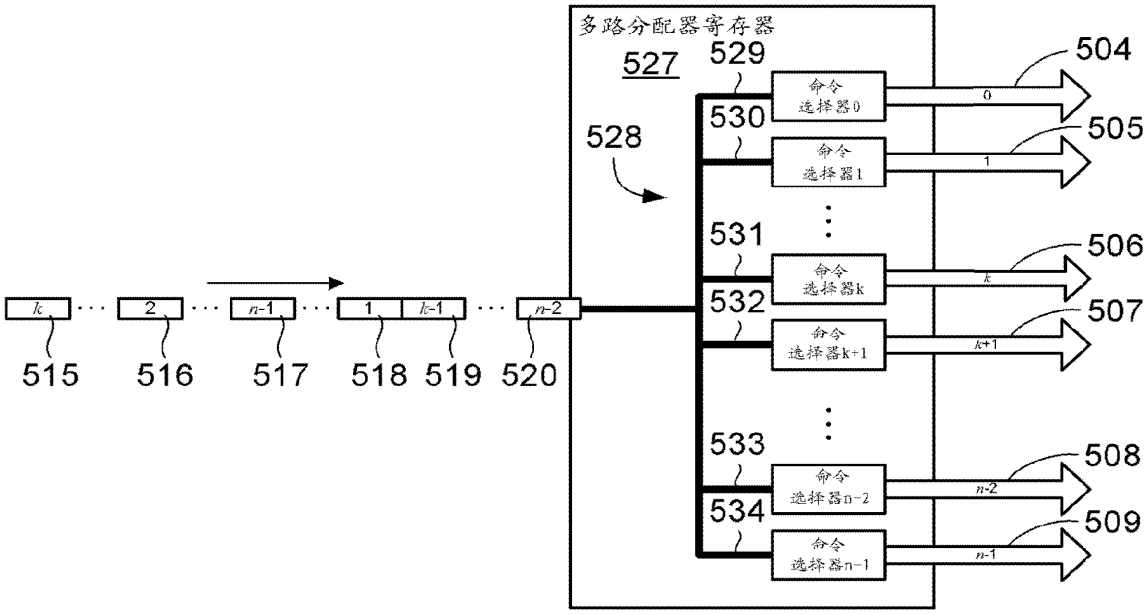
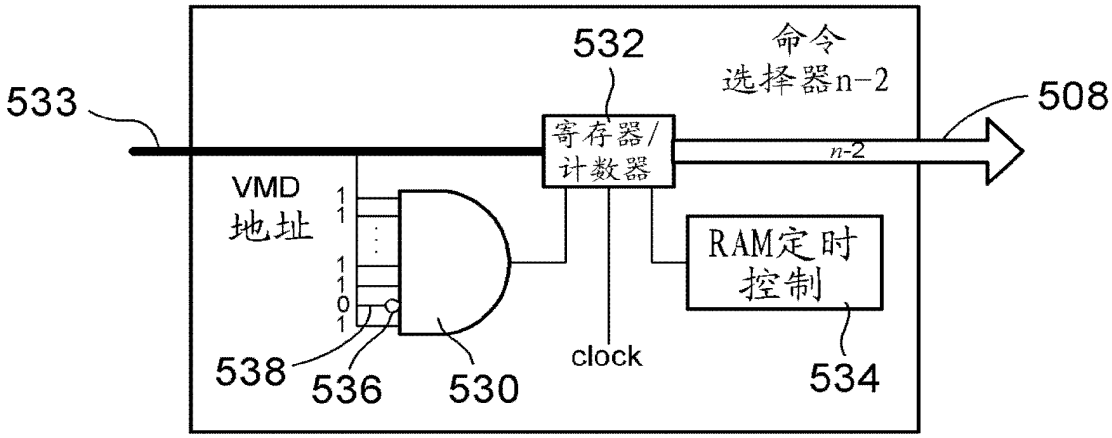


图 5C



VMD_{n-2} 地址 = 11 . . . 1101

图 5D

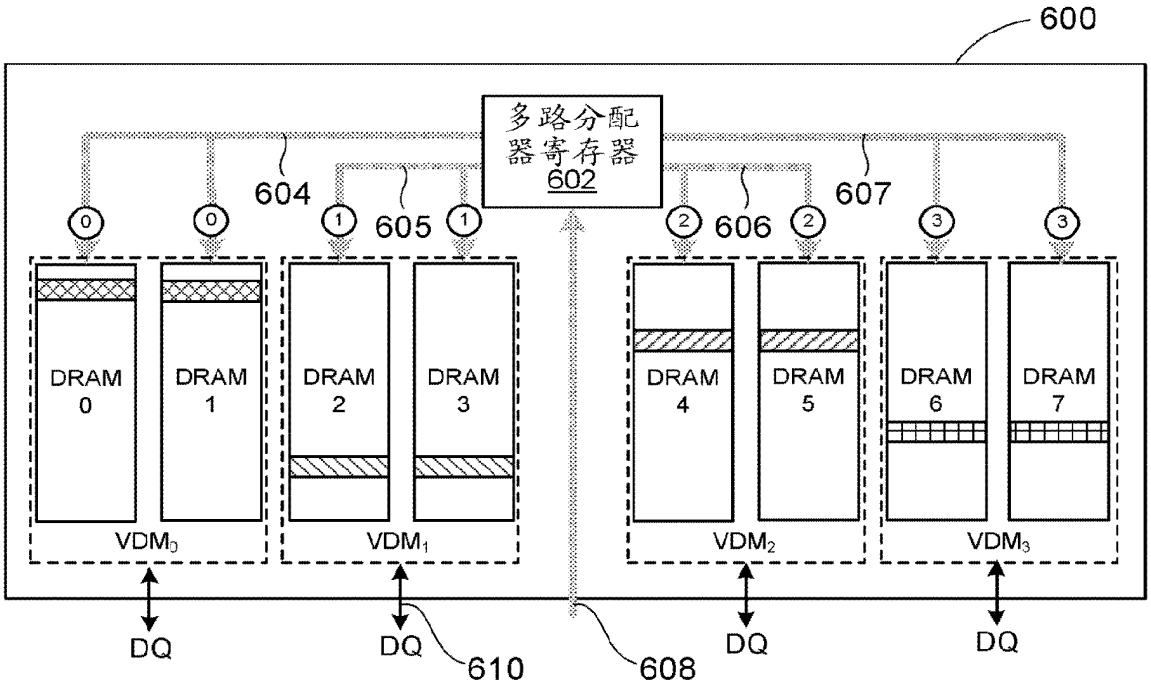

600
多路分配器寄存器
602
604
605
606
607
0
0
1
1
2
2
3
3
DRAM 0
DRAM 1
DRAM 2
DRAM 3
DRAM 4
DRAM 5
DRAM 6
DRAM 7
VDM0
VDM1
VDM2
VDM3
DQ
DQ
DQ
DQ
610
608

图 6

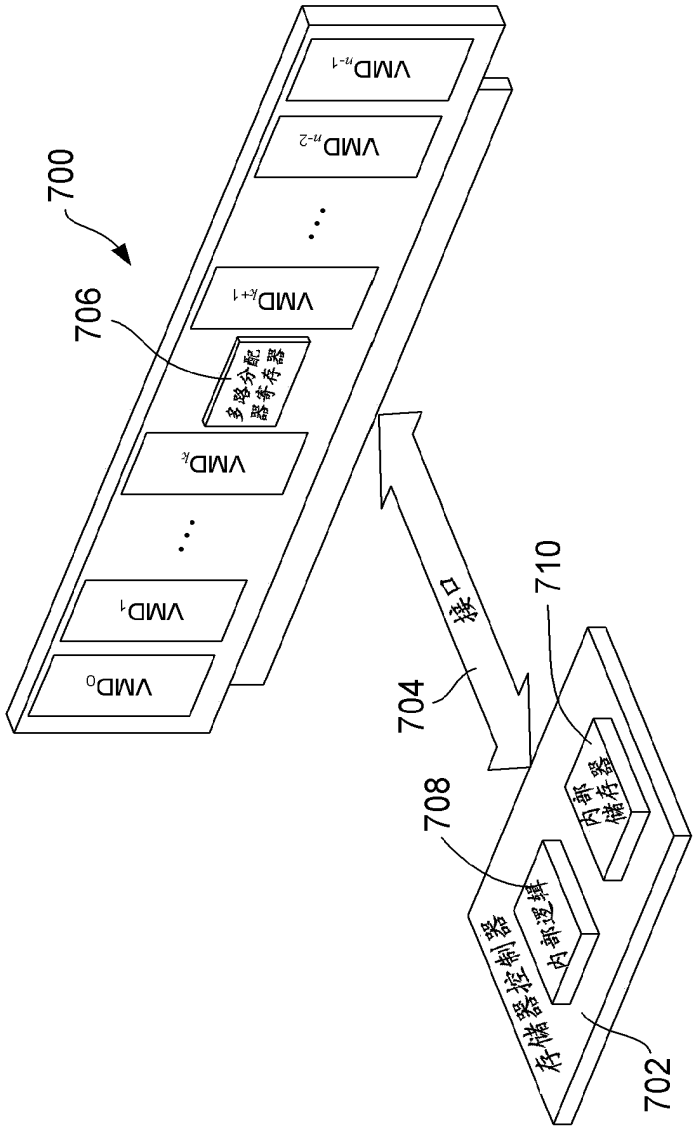

700
706
多路分配器寄存器
VMD$_0$
VMD$_1$
VMD$_k$
VMD$_{k+1}$
VMD$_{n-2}$
VMD$_{n-1}$
接口
704
710
708
内部储存器
内部逻辑
存储器控制器
702

图 7

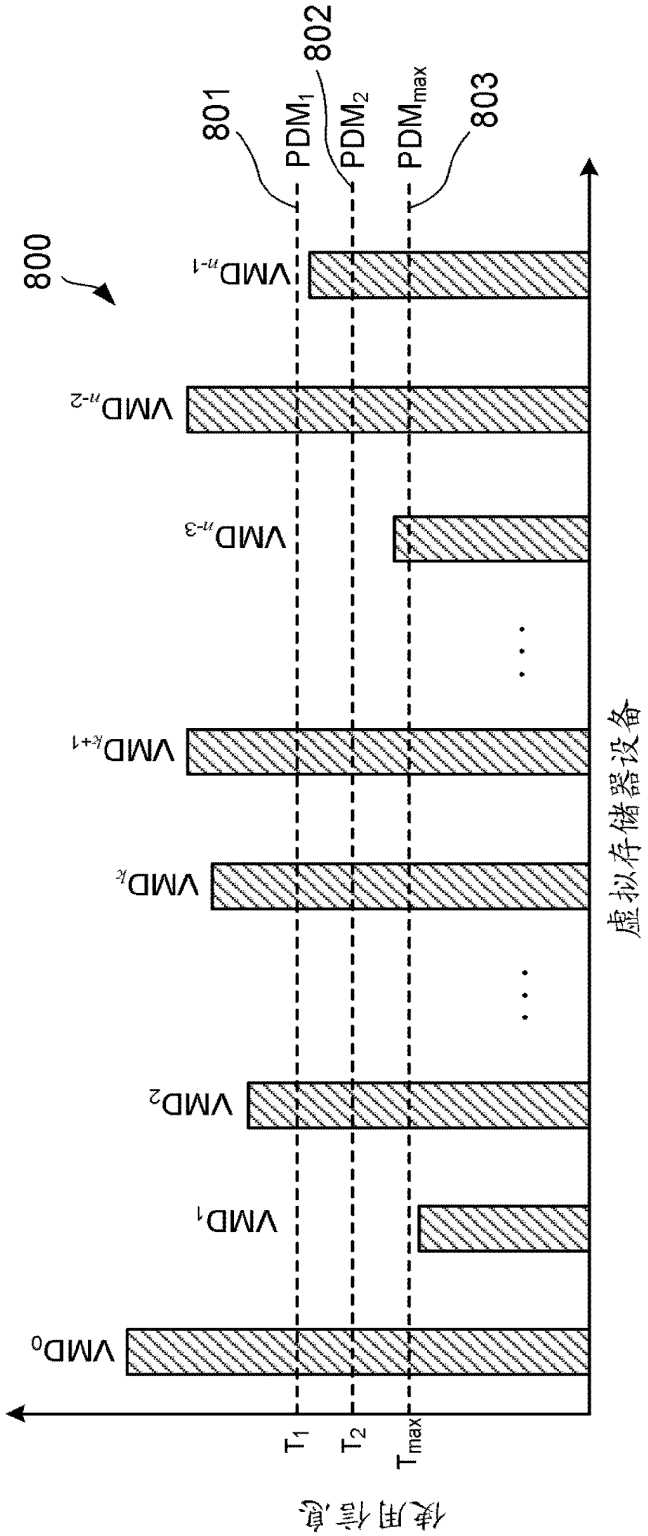

800
801
802
803
PDM1
PDM2
PDMmax
VMD0
VMD1
VMD2
VMDk
VMDk+1
VMDn-3
VMDn-2
VMDn-1
虚拟存储器设备
T1
T2
Tmax
使用信息

图 8A

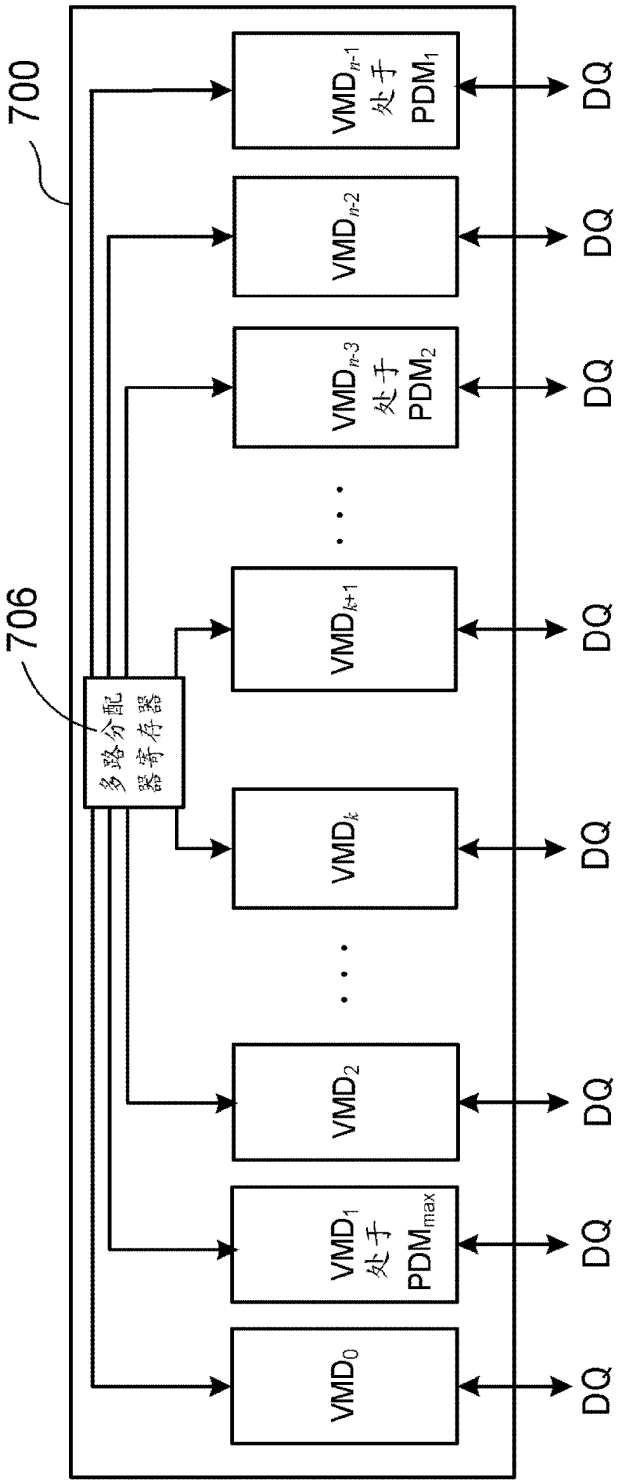

700
706
多路分配器寄存器
VMD0
VMD1 处于 PDMmax
VMD2
VMDk
VMDk+1
VMDn-3 处于 PDM2
VMDn-2
VMDn-1 处于 PDM1
DQ

图 8B

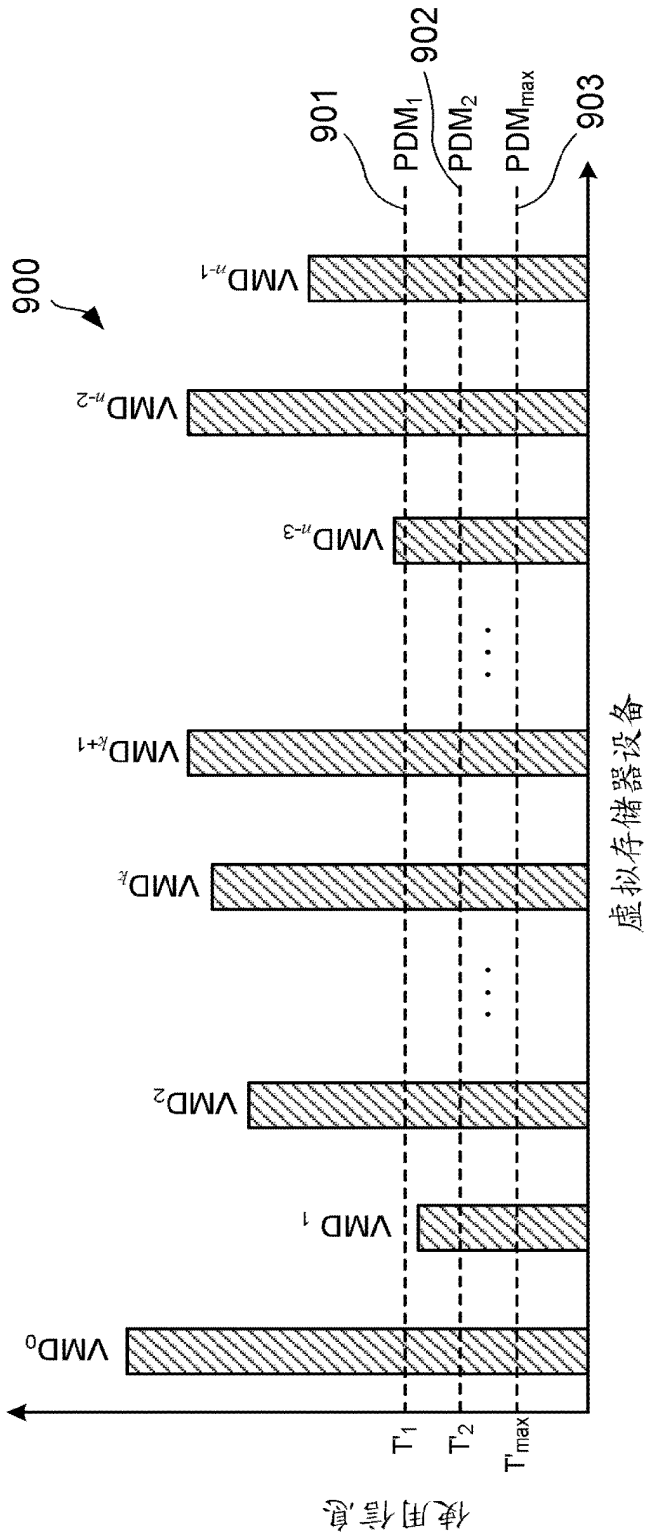

使用信息
T'1
T'2
T'max
VMD0
VMD 1
VMD2
VMDk
VMDk+1
VMDn-3
VMDn-2
VMDn-1
900
901
PDM1
902
PDM2
PDMmax
903
虚拟存储器设备

图 9A

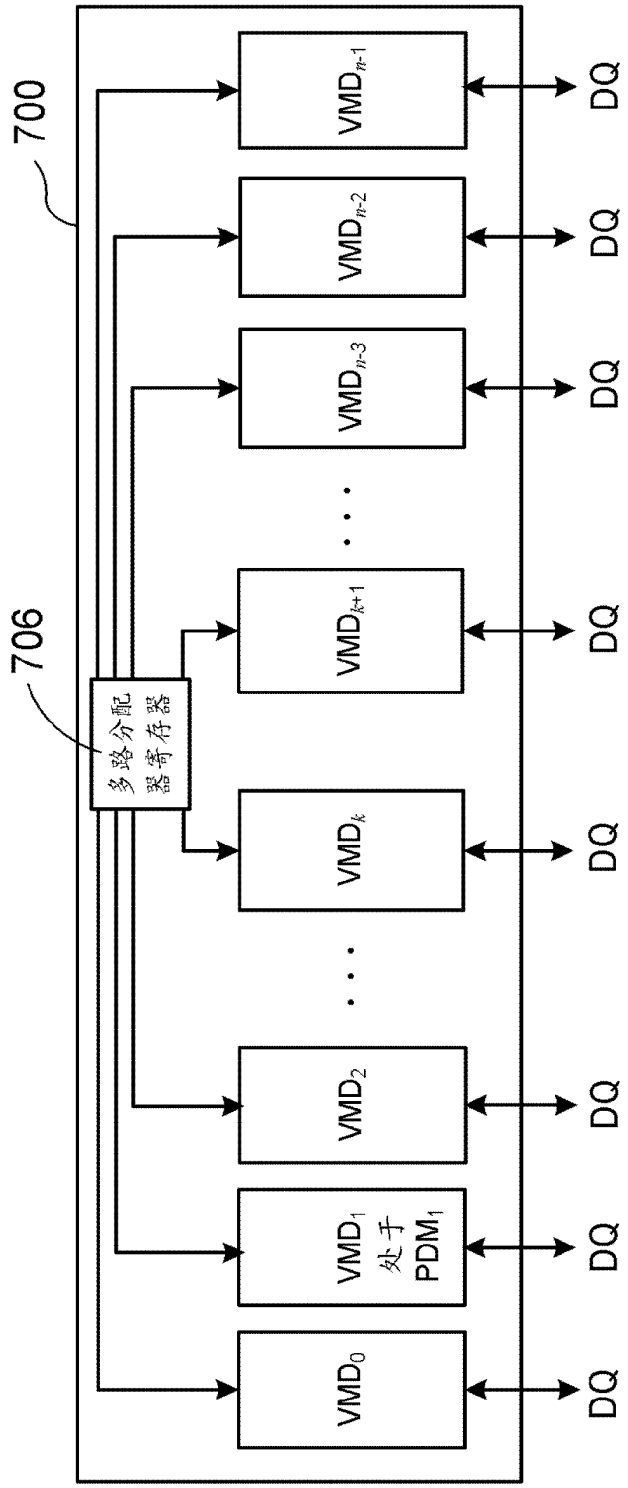

700
706
多路分配器寄存器
VMD0
VMD1 处于 PDM1
VMD2
VMDk
VMDk+1
VMDn-3
VMDn-2
VMDn-1
DQ
DQ
DQ
DQ
DQ
DQ
DQ

图 9B

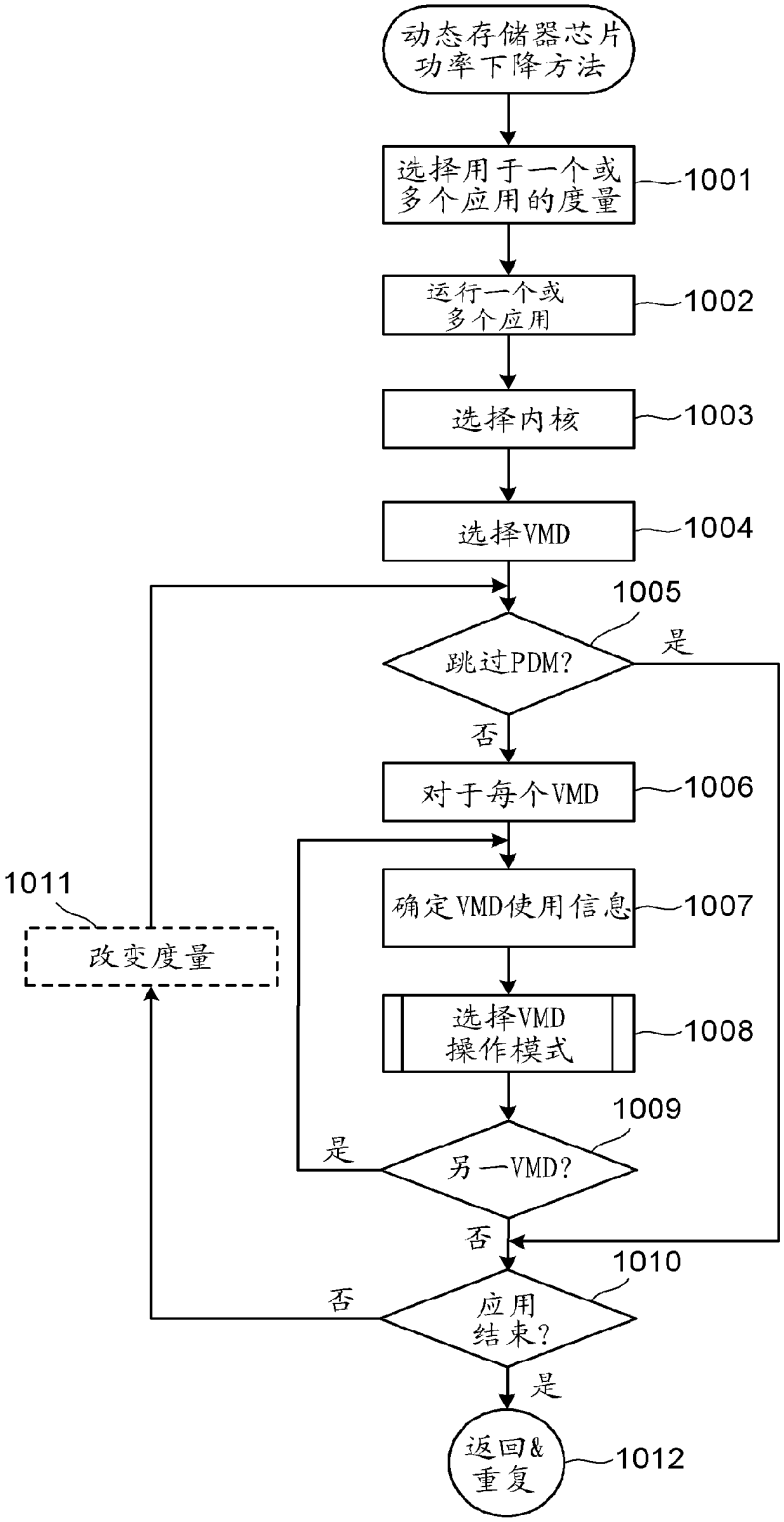

动态存储器芯片功率下降方法
选择用于一个或多个应用的度量
1001
运行一个或多个应用
1002
选择内核
1003
选择VMD
1004
1005
跳过PDM?
是
否
对于每个VMD
1006
1011
改变度量
确定VMD使用信息
1007
选择VMD操作模式
1008
1009
是
另一VMD?
否
1010
否
应用结束?
是
返回&重复
1012

图 10

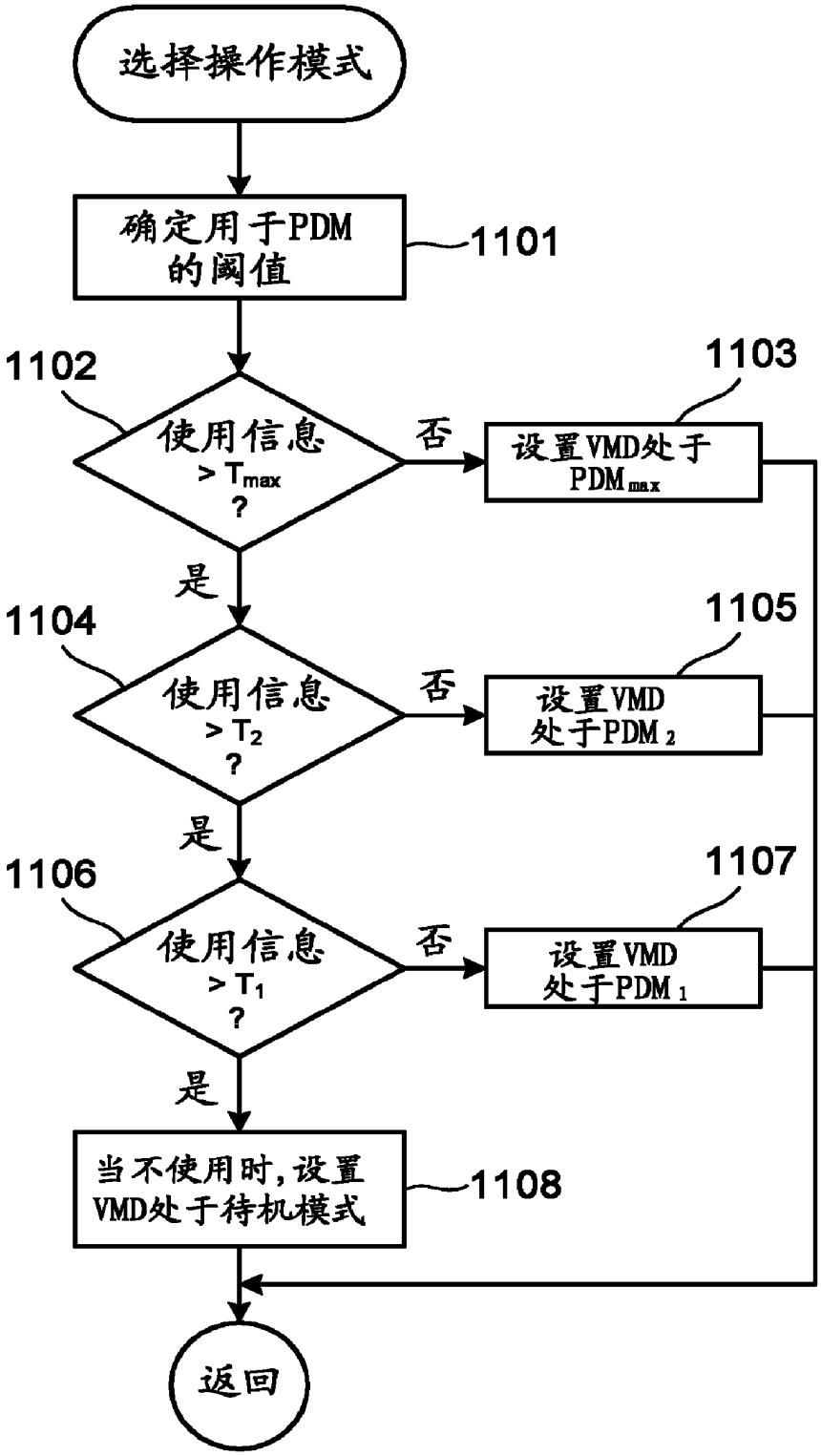

选择操作模式
确定用于PDM的阈值
1101
1102
使用信息 > T_{max} ?
否
1103
设置VMD处于 PDM_{max}
是
1104
使用信息 > T_2 ?
否
1105
设置VMD处于 PDM_2
是
1106
使用信息 > T_1 ?
否
1107
设置VMD处于 PDM_1
是
当不使用时,设置VMD处于待机模式
1108
返回

图 11

Abstract of TW201123198

Memory power supply circuit

ABST:
A memory power supply circuit includes a single-phase PWM signal controller, a first transistor and a second transistor, a first a field-effect transistor (FET) and a second FET. The first and the second transistors receive an enable signal and control the PWM signal controller to alternately output a high level voltage and a low level voltage via a high pass driving pin and a low pass driving pin thereof, to alternately control the first and the second FETs to be turned on and turned off. At the same time, a phase pin of the PWM signal controller outputs a PWM signal and receives a power supply via a capacitor and a resistor, and then outputs a power voltage to a memory.

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(43)公開日： 中華民國 100 (2011) 年 07 月 01 日

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(51)Int. Cl.： *G11C5/14 (2006.01)*
(71)申請人：鴻海精密工業股份有限公司 (中華民國) HON HAI PRECISION INDUSTRY CO., LTD. (TW)
新北市土城區自由街 2 號
(72)發明人：周海清 ZHOU, HAI-QING (CN)
申請實體審查：無 申請專利範圍項數：10 項 圖式數：1 共 14 頁

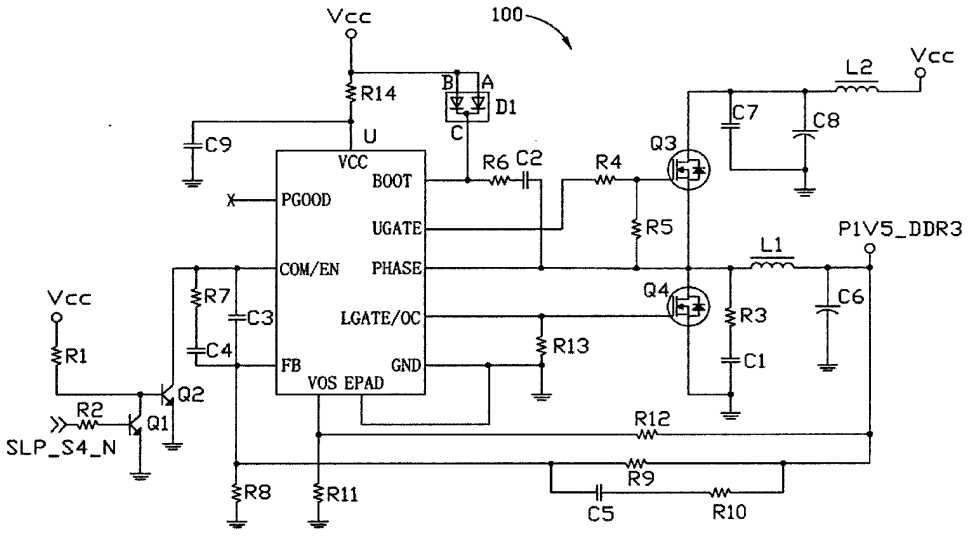
(54)名稱

記憶體供電電路

MEMORY POWER SUPPLY CIRCUIT

(57)摘要

一種記憶體供電電路，包括一單相脈寬調製訊號控制器、一第一及一第二電晶體、一第一及一第二場效應電晶體，該第一及第二電晶體接收一使能控制訊號並在該使能訊號輸入時控制該單相脈寬調製訊號控制器工作，以使該單相脈寬調製訊號控制器的高通驅動引腳及低通驅動引腳交替輸出高低電平以交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊號並透過一電容及一電阻接收電源，再透過一電感輸出一供電電壓給記憶體。



100：記憶體供電電路
C1-C9：電容
D1：二極體元件
L1：電感
L2：電感
Q1：電晶體
Q2：電晶體
Q3：場效應電晶體
Q4：場效應電晶體
R1-R14：電阻
U：單相脈寬調製訊號控制器
Vcc：5V 電源

專利案號：098143494

智專收字第0982074484-0

DTD版本：1.0.0

日期：98年12月18日

發明專利說明書

※申請案號：098143494　※ＩＰＣ分類：G11C 5/14 (2006.01)

※申請日：98.12.18

一、發明名稱：

記憶體供電電路

Memory Power Supply Circuit

二、中文發明摘要：

一種記憶體供電電路，包括一單相脈寬調製訊號控制器、一第一及一第二電晶體、一第一及一第二場效應電晶體，該第一及第二電晶體接收一使能控制訊號並在該使能訊號輸入時控制該單相脈寬調製訊號控制器工作，以使該單相脈寬調製訊號控制器的高通驅動引腳及低通驅動引腳交替輸出高低電平以交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊號並透過一電容及一電阻接收電源，再透過一電感輸出一供電電壓給記憶體。

三、英文發明摘要：

A memory power supply circuit includes a single-phase PWM signal controller, a first transistor and a second transistor, a first a field-effect transistor (FET) and a second FET. The first and the second transistors receive an enable signal and control the PWM signal controller to alternately output a high level voltage and a low level voltage via a high pass driving pin and a low pass driving pin thereof, to alternately control the first and the second FETs to be turned on and turned off. At the same time, a phase pin of the PWM signal controller outputs a PWM signal and receives a power supply via a capacitor and a resistor, and

then outputs a power voltage to a memory.

四、指定代表圖：

(一)本案指定代表圖為：第（1）圖

(二)本代表圖之元件符號簡單說明：

記憶體供電電路：100

單相脈寬調製訊號控制器：U

5V電源：Vcc

電晶體：Q1、Q2

場效應電晶體：Q3、Q4

電感：L1、L2

二極體元件：D1

電阻：R1-R14

電容：C1-C9

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

六、發明說明：

【發明所屬之技術領域】

[0001] 本發明係關於一種供電電路，尤指一種用於給記憶體提供電壓的供電電路。

【先前技術】

[0002] 隨著電子技術迅速發展，低壓大電流設計成為主流，因為電路設計中，電壓愈低，，電路消耗功率愈小。電源設計人員所面臨的最大挑戰是如何滿足更大的功率、更小的電壓容限以及更快的瞬態回應，並降低電源的總成本。隨著CPU電流和功率增大，記憶體電流也要求愈來愈大，並且記憶體供電電壓也愈來愈小。我們知道，最初DRAM記憶體的供電電壓是5V，SDRAM記憶體的供電電壓是3.3V，DDR記憶體的供電電壓是2.5V，DDR2記憶體的供電電壓是1.8V，DDR3記憶體的供電電壓則降為1.5V（其中DRAM、SDRAM、DDR、DDR2、DDR3為不同時期記憶體的不同標準）。同時記憶體頻率也愈來愈高，回應速度愈來愈快，當然消耗功率也愈來愈大，因此如何設計出大電流、低功耗的穩定電路是業界需要解決的問題。

【發明內容】

[0003] 鑒於上述內容，有必要提供一種大電流、低功耗的記憶體供電電路。

[0004] 一種記憶體供電電路，包括一單相脈寬調製訊號控制器、一第一及一第二電晶體、一第一及一第二場效應電晶體及一第一及一第二電感，該單相脈寬調製訊號控制器的使能引腳連接至該第二電晶體的集極，該第二電晶體

的射極接地，基極連接該第一電晶體的集極並透過一第一電阻連接至一電源，該第一電晶體的射極接地，基極透過一第二電阻接收一使能控制訊號，該單相脈寬調製訊號控制器的相位引腳透過該第一電感連接至一電壓輸出引腳以提供電壓給記憶體，還依次透過一第三電阻及一第一電容接地，該單相脈寬調製訊號控制器的高通驅動引腳透過一第四電阻連接至該第一場效應電晶體的閘極，該第一場效應電晶體汲極透過該第二電感連接至該電源，該第一場效應電晶體的源極連接至該第二場效應電晶體的汲極，該第一場效應電晶體的閘極還透過一第五電阻連接至該第二場效應電晶體的汲極，該單相脈寬調製訊號控制器的低通驅動引腳連接至該第二場效應電晶體的閘極，該第二場效應電晶體的源極接地，當該使能控制訊號輸入時，該第一電晶體導通，該第二電晶體截止，該單相脈寬調製訊號控制器的高通驅動引腳及低通驅動引腳交替輸出高低電平以交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊號並透過一第二電容及一第六電阻接收該電源，再透過該第一電感及該電壓輸出引腳輸出一供電電壓給該記憶體。

[0005] 上述記憶體供電電路透過該第一及第二電晶體接收該使能控制訊號，並在該使能訊號輸入時控制該單相脈寬調製訊號控制器工作，以使該單相脈寬調製訊號控制器交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊

號並透過一第二電容及一第六電阻接收該電源，再透過該第一電感及該電壓輸出引腳輸出一大電流、低功耗且穩定的供電電壓給該記憶體。

【實施方式】

[0006] 請參照圖1，本發明記憶體供電電路100的較佳實施方式包括一單相脈寬調製訊號控制器U、兩電晶體Q1及Q2、兩場效應電晶體Q3及Q4、十四個電阻R1-R14、九個電容C1-C9、兩電感L1及L2、一由兩並聯的二極體組成的二極體元件D1及一5V電源Vcc。本實施方式中，該單相脈寬調製訊號控制器U的型號為ISL6341CRZ，該二極體組件D1的型號為BAT54C，其他實施方式中也可根據需要選取其他型號。

[0007] 該單相脈寬調製訊號控制器U的使能引腳COM/EN連接至該電晶體Q2的集極，該電晶體Q2的射極接地，基極連接該電晶體Q1的集極並透過該電阻R1連接至該5V電源Vcc，該電晶體Q1的射極接地，基極透過該電阻R2接收一使能控制訊號SLP_S4_N。該單相脈寬調製訊號控制器U的使能引腳COM/EN透過該電容C3連接至其上的回饋引腳FB，還依次透過該電阻R7及電容C4連接至該回饋引腳FB。該回饋引腳FB透過該電阻R8接地，還透過該電阻R9連接一電壓輸出引腳P1V5_DDR3。該單相脈寬調製訊號控制器U的偵測引腳VOS透過該電阻R11接地，還透過該電阻R12連接該電壓輸出引腳P1V5_DDR3，該電容C5與電阻R10串聯後再與該電阻R9並聯，該電容C6連接在該電壓輸出引腳P1V5_DDR3與地之間，該電壓輸出引腳P1V5_DDR3連

接至一DDR3記憶體（未示出）的電源端，以提供1.5V電壓給該DDR3記憶體。

[0008] 該單相脈寬調製訊號控制器U的電源引腳VCC透過該電阻R14連接至該5V電源Vcc並透過該電容C9接地。該單相脈寬調製訊號控制器U的自舉引腳BOOT連接至該二極體元件D1的陰極C，該二極體元件D1的陽極A、B連接至該5V電源Vcc，該自舉引腳BOOT還依次透過該電阻R6及C2連接至該單相脈寬調製訊號控制器U的相位引腳PHASE，該相位引腳PHASE透過該電感L1連接至該電壓輸出引腳P1V5_DDR3，還依次透過該電阻R3及電容C1接地。該單相脈寬調製訊號控制器U的高通驅動引腳UGATE透過該電阻R4連接至該場效應電晶體Q3的閘極，該場效應電晶體Q3的汲極透過該電感L2連接至該5V電源Vcc，該兩電容C7及C8分別連接在該場效應電晶體Q3的汲極與地之間。

[0009] 該場效應電晶體Q3的源極連接至該場效應電晶體Q4的汲極，該場效應電晶體Q3的閘極還透過電阻R5連接至該場效應電晶體Q4的汲極，該單相脈寬調製訊號控制器U的低通驅動引腳LGATE/OC連接至該場效應電晶體Q4的閘極，該場效應電晶體Q4的源極接地。該低通驅動引腳LGATE/OC還透過該電阻R13接地，該單相脈寬調製訊號控制器U的接地引腳GND接地，該單相脈寬調製訊號控制器U的引腳EPAD接地，該單相脈寬調製訊號控制器U的引腳PGOOD空接。

[0010] 工作時，該使能控制訊號SLP_S4_N為低電平有效，即當該使能控制訊號SLP_S4_N為低電平時，系統進入S4狀態

（此狀態記憶體、硬碟均不工作），該電晶體Q1截止，該電晶體Q2導通，該單相脈寬調製訊號控制器U不工作。

[0011] 當該使能控制訊號SLP_S4_N變為低電平時，系統退出S4狀態，該電晶體Q1導通，該電晶體Q2截止，該單相脈寬調製訊號控制器U開始工作，該單相脈寬調製訊號控制器U的高通驅動引腳UGATE及低通驅動引腳LGATE/OC交替輸出高低電平以交替控制該兩場效應電晶體Q3及Q4導通及截止，同時該單相脈寬調製訊號控制器U的相位引腳PHASE輸出一脈寬調製訊號並透過該電容C2、電阻R6及二極體元件D1接收該5V電源Vcc，然後再透過該電感L1輸出一1.5V電壓給該記憶體。該1.5V電壓還透過電阻R9及電阻R8回饋至該單相脈寬調製訊號控制器U的回饋引腳FB，以調節該高通驅動引腳UGATE、低通驅動引腳LGATE/OC及相位引腳PHASE的輸出訊號，從而產生穩定該電壓輸出引腳P1V5_DDR3輸出電壓的作用，上述電路結構可使該電壓輸出引腳P1V5_DDR3輸出大電流、低功耗且穩定的供電訊號給該記憶體。

[0012] 其中，該二極體元件D1產生隔離電壓的作用，該單相脈寬調製訊號控制器U的偵測引腳VOS用於偵測該電壓輸出引腳P1V5_DDR3輸出的電壓是否正常。該電阻R7、電容C4、電阻R10及電容C5組成輸出補償回路，採用此電路架構可明顯提高輸出電壓與輸出電流的精度。該電感L2產生濾波整流的作用，電路中的其他電容元件產生濾波的作用，以提高電路的整體性能，也可根據需要增加或減少上述各元件。

[0013] 綜上所述，本發明符合發明專利要件，爰依法提出專利申請。惟，以上所述者僅為本發明之較佳實施例，舉凡熟悉本案技藝之人士，在爰依本發明精神所作之等效修飾或變化，皆應涵蓋於以下之申請專利範圍內。

【圖式簡單說明】

[0014] 圖1係本發明記憶體供電電路較佳實施方式的電路圖。

【主要元件符號說明】

[0015] 記憶體供電電路：100

[0016] 單相脈寬調製訊號控制器：U

[0017] 5V電源：Vcc

[0018] 電晶體：Q1、Q2

[0019] 場效應電晶體：Q3、Q4

[0020] 電感：L1、L2

[0021] 二極體元件：D1

[0022] 電阻：R1-R14

[0023] 電容：C1-C9

七、申請專利範圍：

1．一種記憶體供電電路，包括一單相脈寬調製訊號控制器、一第一及一第二電晶體、一第一及一第二場效應電晶體及一第一及一第二電感，該單相脈寬調製訊號控制器的使能引腳連接至該第二電晶體的集極，該第二電晶體的射極接地，基極連接該第一電晶體的集極並透過一第一電阻連接至一電源，該第一電晶體的射極接地，基極透過一第二電阻接收一使能控制訊號，該單相脈寬調製訊號控制器的相位引腳透過該第一電感連接至一電壓輸出引腳以提供電壓給記憶體，還依次透過一第三電阻及一第一電容接地，該單相脈寬調製訊號控制器的高通驅動引腳透過一第四電阻連接至該第一場效應電晶體的閘極，該第一場效應電晶體汲極透過該第二電感連接至該電源，該第一場效應電晶體的源極連接至該第二場效應電晶體的汲極，該第一場效應電晶體的閘極還透過一第五電阻連接至該第二場效應電晶體的汲極，該單相脈寬調製訊號控制器的低通驅動引腳連接至該第二場效應電晶體的閘極，該第二場效應電晶體的源極接地，當該使能控制訊號輸入時，該第一電晶體導通，該第二電晶體截止，該單相脈寬調製訊號控制器的高通驅動引腳及低通驅動引腳交替輸出高低電平以交替控制該第一及第二場效應電晶體導通及截止，同時該單相脈寬調製訊號控制器的相位引腳輸出一脈寬調製訊號並透過一第二電容及一第六電阻接收該電源，再透過該第一電感及該電壓輸出引腳輸出一供電電壓給該記憶體。

2．如申請專利範圍第1項所述之記憶體供電電路，其中該單

相脈寬調製訊號控制器的使能引腳還透過一第三電容連接至其上的回饋引腳，還依次透過一第七電阻及一第四電容連接至該回饋引腳，該回饋引腳透過一第八電阻接地，還透過一第九電阻連接該電壓輸出引腳，一第五電容與一第十電阻串聯後再與該第九電阻並聯。

3．如申請專利範圍第2項所述之記憶體供電電路，其中該單相脈寬調製訊號控制器的偵測引腳透過一第十一電阻接地，還透過一第十二電阻連接該電壓輸出引腳，一第六電容連接在該電壓輸出引腳與地之間。

4．如申請專利範圍第3項所述之記憶體供電電路，其中該單相脈寬調製訊號控制器的自舉引腳依次透過該第六電阻及第二電容連接至該單相脈寬調製訊號控制器的相位引腳。

5．如申請專利範圍第4項所述之記憶體供電電路，其中該第六電阻與該電源之間還連接一二極體元件，該二極體元件的陰極連接該第六電阻的一端，該二極體元件的陽極連接至該電源。

6．如申請專利範圍第5項所述之記憶體供電電路，其中一第七及一第八電容分別連接在該第二場效應電晶體的汲極與地之間。

7．如申請專利範圍第6項所述之記憶體供電電路，其中該單相脈寬調製訊號控制器的低通驅動引腳還透過一第十三電阻連接至該單相脈寬調製訊號控制器的接地引腳並接地。

8．如申請專利範圍第7項所述之記憶體供電電路，其中該單相脈寬調製訊號控制器的電源引腳透過一第十四電阻連接該電源，還透過一第九電容接地。

9．如申請專利範圍第1項所述之記憶體供電電路，其中該記

憶體為DDR3記憶體。

10．如申請專利範圍第1項所述之記憶體供電電路，其中該電源為5V電源。

八、圖式：

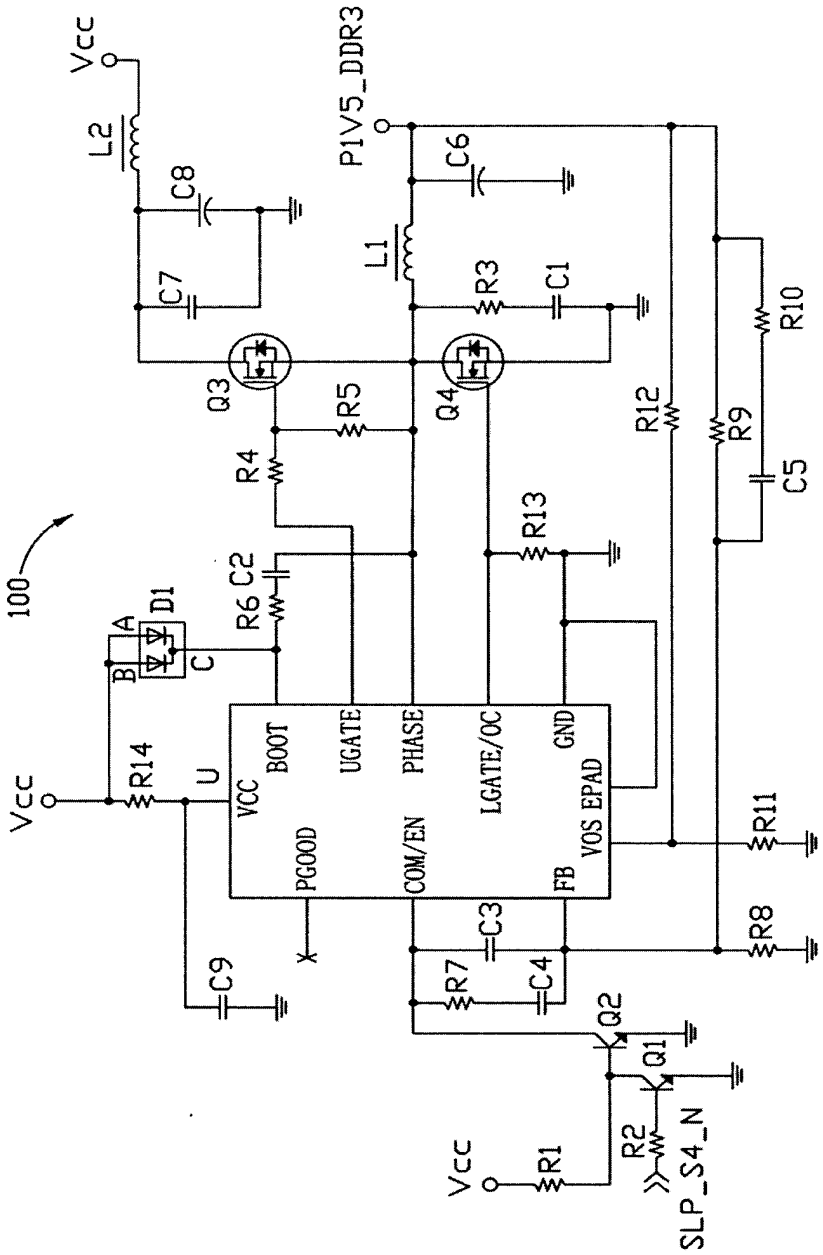

Vcc
L2
C8
C7
P1V5_DDR3
C6
L1
R3
C1
R10
Q3
R5
Q4
R12
R9
C5
R4
R13
100
C2
R6
D1
A
B
C
R14
U
VCC
BOOT
UGATE
PHASE
LGATE/OC
GND
PGOOD
COM/EN
FB
VOS EPAD
R11
R8
C3
C9
R7
C4
Q2
Q1
R2
R1
SLP_S4_N

圖 1

Electronic Acknowledgement Receipt

EFS ID:	43086530
Application Number:	17213133
International Application Number:	
Confirmation Number:	9765
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Edie Hung
Filer Authorized By:	Roger Gwan-Jye Chen
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Receipt Date:	25-JUN-2021
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	4252688.PDF	33358 d269c0c6addd4d46c982c17971c404bb4aa05f68	no	6

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/213,133	03/25/2021	2827	830	ETRP0395USA3	3	1

CONFIRMATION NO. 9765

FILING RECEIPT

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHE DIST.
NEW TAIPEI CITY,
TAIWAN

Date Mailed: 04/05/2021

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Inventor(s)

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Applicant(s)

Etron Technology, Inc., Hsinchu, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This application is a CON of 16/151,347 10/04/2018
which is a CON of 13/922,242 06/19/2013 ABN
which claims benefit of 61/672,287 07/17/2012
and claims benefit of 61/768,406 02/23/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/213,133**

Projected Publication Date: 07/15/2021

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
17/213,133

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	80		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	350		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	400		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	3 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*	x 240 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	830		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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Application Number	N/A
Filing Date	N/A
First Named Inventor	Der-Min Yuan
Title	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	ETRP0395USA3

SIGNATURE of Applicant or Patent Practitioner

Signature	/Roger Chen/	Date (Optional)	03/25/2021
Name	Roger Chen	Registration Number	67314
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

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Doc Code: PA..
Document Description: Power of Attorney

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Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Etron Technology, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

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SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	DEC 22 2017
Name	Tony Wang		
Title	Associate Vice President		

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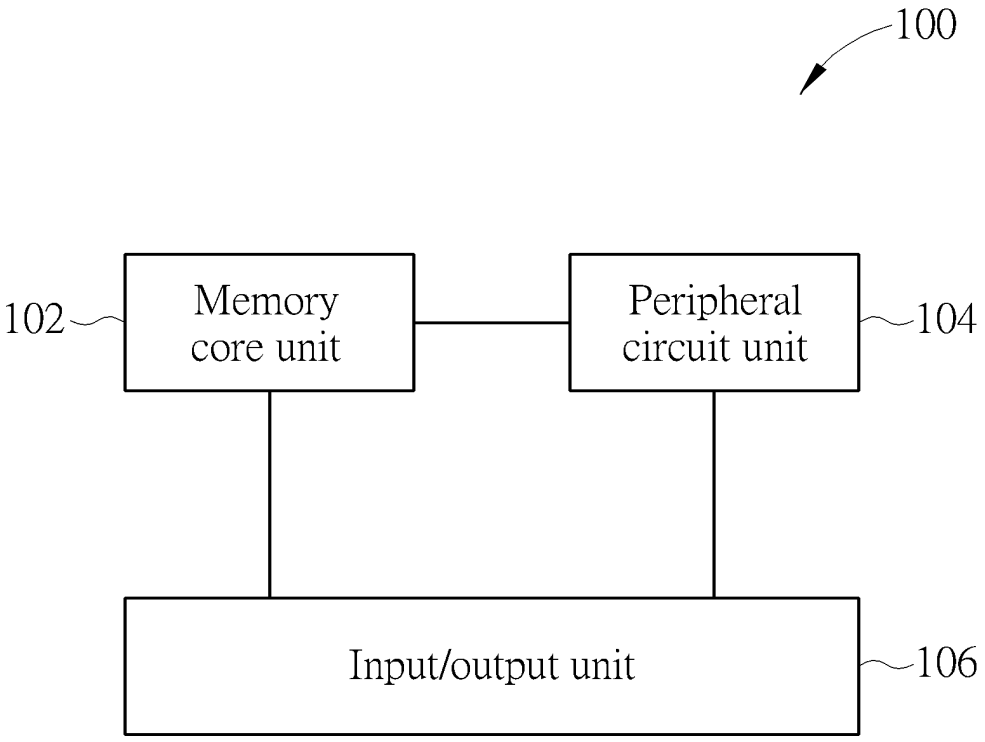
100
102
Memory core unit
Peripheral circuit unit
104
Input/output unit
106

Figure

Abstract of Disclosure

A dynamic random access memory applied to an embedded display port includes a memory core unit, a peripheral circuit unit, and an input/output unit. The memory core unit is used for operating in a first predetermined voltage. The peripheral circuit unit is electrically connected to the memory core unit for operating in a second predetermined voltage, where the second predetermined voltage is lower than 1.1V. The input/output unit is electrically connected to the memory core unit and the peripheral circuit unit for operating in a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.

Claims

What is claimed is:

1. A dynamic random access memory (DRAM), comprising:

   a DRAM core cell comprised in the DRAM, wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage, and the DRAM core cell is a volatile memory cell, wherein the first voltage is lower than 1.1V; and

   a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell, and the peripheral circuit is supplied with a second voltage within a second voltage range to make the peripheral circuit operate at the second voltage, wherein the second voltage is not greater lower than 1.1V, and

   wherein the DRAM core cell and the peripheral circuit are formed on a single chip, and the peripheral circuit is external to the DRAM core cell.

2. The dynamic random access memory of claim 1, wherein the first voltage is different from the second voltage.

3. The dynamic random access memory of claim 1, wherein the first voltage is greater than the second voltage.

Title

DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

Cross Reference To Related Applications

[0001] This is a continuation application of U.S. Patent Application No. 16/151,347, filed on Oct. 4, 2018, which is a continuation application of U.S. Patent Application No. 13/922,242, filed on June 19, 2013, which claims the benefit of U.S. Provisional Application No. 61/672,287, filed on July 17, 2012 and entitled "Flexible Memory Power Supply Architecture," and the benefit of U.S. Provisional Application No. 61/768,406, filed on February 23, 2013 and entitled "Mixed-Low-Voltage DRAM For Embedded Display Port." The above-mentioned applications are incorporated herein by reference.

Background of the Invention

1. Field of the Invention

[0002] The present invention relates to a dynamic random access memory, and particularly to a dynamic random access memory applied to an embedded display port.

2. Description of the Prior Art

[0003] An embedded display port (eDP) published by the Video Electronics Standards Association (VESA) is used for acting as a standard display panel interface to connect external devices. For example, the embedded display port can act as an interface between a video card and a notebook panel. In addition, the embedded display port version 1.3 published by the Video Electronics Standards Association adds a panel self refresh (PSR) function, where the panel self refresh function can make a graphic processing unit (GPU) turn off connection between the graphic processing unit and a liquid crystal panel when a frame displayed on the liquid crystal panel is frozen. Thus, power consumption of the graphic processing unit can be significantly reduced and battery endurance ability can be extended.

[0004] In addition, a timing controller supporting the panel self refresh function of the liquid crystal display needs to include a frame buffer (e.g. a dynamic random access memory). When the graphic processing unit turns off the connection between the graphic processing unit and the liquid crystal panel, the frame buffer needs to store a last frame before the graphic processing unit turns off the connection between the graphic processing unit and the liquid crystal panel. Therefore, when no data transmission exists between the graphic processing unit and the liquid crystal panel, the timing controller can directly output the last frame stored in the frame buffer.

[0005] Although the panel self refresh function can make power consumption of the graphic processing unit be significantly reduced, power consumption of the timing controller is increased due to operation of the frame buffer. Therefore, how to design the frame buffer to reduce the power consumption of the timing controller becomes an important issue of memory manufacturers.

Summary of the Invention

[0006] An embodiment provides a dynamic random access memory applied to an embedded display port. The dynamic random access memory includes a memory core unit and a peripheral circuit unit. The memory core unit is used for operating in a first predetermined voltage. The peripheral circuit unit is electrically connected to the memory core unit for operating in a second predetermined voltage, where the second predetermined voltage is lower than 1.1V.

[0007] Another embodiment provides a dynamic random access memory applied to an embedded display port. The dynamic random access memory includes a memory core unit, a peripheral circuit unit, and an input/output unit. The memory core unit is used for operating in a first predetermined voltage. The peripheral circuit unit is electrically connected to the memory core unit for operating in a second predetermined voltage, where the second predetermined voltage

is lower than 1.1V. The input/output unit is electrically connected to the peripheral circuit unit and the memory core unit for operating in a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.

[0008] The present invention provides a dynamic random access memory applied to an embedded display port. The dynamic random access memory makes a memory core unit, a peripheral circuit unit, and an input/output unit thereof operate in lower voltages. Compared to the prior art, power consumption of the dynamic random access memory of the present invention is much lower than power consumption of a dynamic random access memory operating in operation voltages specified by the Joint Electron Device Engineering Council. Thus, when the dynamic random access memory of the present invention is applied to an embedded display port, the present invention can make system power consumption (e.g. power consumption of a graphic processing unit) be significantly reduced, not make power consumption of a timing controller be increased due to operation of a frame buffer, and extend battery endurance ability of a portable device.

[0009] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0010] The figure is a diagram illustrating a dynamic random access memory 100 applied to embedded display port according to an embodiment.

Detailed Description

[0011] Please refer to the figure. The figure is a diagram illustrating a dynamic random access memory 100 applied to an embedded display port according to an embodiment, where the dynamic random access memory 100 acts as a frame buffer of a timing controller of a liquid

crystal display, and the dynamic random access memory 100 is compatible with a single data rate (SDR) specification, a double data rate (DDR Ⅰ) specification, a double data rate two (DDR Ⅱ) specification, or a double data rate three (DDR Ⅲ) specification. As shown in the figure, the dynamic random access memory 100 includes a memory core unit 102, a peripheral circuit unit 104, and an input/output unit 106, where the peripheral circuit unit 104 is electrically connected to the memory core unit 102, and the input/output unit 106 is electrically connected to the peripheral circuit unit 104 and the memory core unit 102. Please refer to Table Ⅰ. Table Ⅰ illustrates operation voltages (specified by the Joint Electron Device Engineering Council (JEDEC)) of a dynamic random access memory operating in the DDR Ⅰ specification, a low power DDR Ⅰ specification, the DDR Ⅱ specification, and a low power DDR Ⅱ specification.

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
DDR Ⅰ	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V	3.3V±0.3V or 2.5V±0.2V
Low Power DDR Ⅰ	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
DDR Ⅱ	1.8V±0.1V	1.8V±0.1V	1.8V±0.1V
Low Power DDR Ⅱ	1.7V~1.95V	1.14V~1.30V	1.14V~1.30V

Table Ⅰ

[0012] If the dynamic random access memory 100 is designed to have low power consumption to reduce power consumption of the timing controller, the dynamic random access memory 100 needs to have low operation power consumption (e.g. power consumption for the dynamic random access memory 100 outputting storage frames to the timing controller) and low standby power consumption. But, the operation voltages specified by the Joint Electron Device Engineering Council

(as shown in Table Ⅰ) can not satisfy requirements (that is, the low operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3.

[0013] Please refer to Table Ⅱ. Table Ⅱ illustrates operation voltage ranges of the dynamic random access memory 100 operating in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification according to an embodiment.

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	< 1.1V	< 1.1V	< 1.1V

Table Ⅱ

[0014] As shown in Table Ⅱ, operation voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a first predetermined voltage, where the first predetermined voltage is lower than 1.1V; operation voltages of the peripheral circuit unit 104 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a second predetermined voltage, where the second predetermined voltage is lower than 1.1V; and operation voltages of the input/output unit 106 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.

[0015] As shown in Table Ⅱ, because the operation voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR

Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the first predetermined voltage, the dynamic random access memory 100 has lower memory core power consumption; because the operation voltages of the peripheral circuit unit 104 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the second predetermined voltage, the dynamic random access memory 100 has lower access power consumption; and the operation voltages of the input/output unit 106 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the third predetermined voltage, the dynamic random access memory 100 has lower input/output power consumption. In addition, the input/output unit 106 is compatible with an interface provided by the prior art, so power consumption of the dynamic random access memory 100 is much lower than power consumption of the dynamic random access memory operating in the operation voltages specified by the Joint Electron Device Engineering Council.

[0016] Please refer to Table Ⅲ. Table Ⅲ illustrates operation voltage ranges of the dynamic random access memory 100 operating in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification according to another embodiment.

	memory core unit 102	peripheral circuit unit 104	input/output unit 106
operation voltage ranges	1.8V±0.1V	< 1.1V	< 1.1V

Table Ⅲ

[0017] As shown in Table Ⅲ, operation voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR Ⅰ

specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a first predetermined voltage, where the first predetermined voltage is equal to 1.8V±0.1V; operation voltages of the peripheral circuit unit 104 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a second predetermined voltage, where the second predetermined voltage is lower than 1.1V; and operation voltages of the input/output unit 106 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are a third predetermined voltage, where the third predetermined voltage is lower than 1.1V.

[0018] As shown in Table Ⅲ, because the operation voltages of the memory core unit 102 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the first predetermined voltage, the dynamic random access memory 100 has higher charge pump efficiency; because the operation voltages of the peripheral circuit unit 104 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the second predetermined voltage, the dynamic random access memory 100 has lower access power consumption; and the operation voltages of the input/output unit 106 in the DDR Ⅰ specification, the low power DDR Ⅰ specification, the DDR Ⅱ specification, and the low power DDR Ⅱ specification are the third predetermined voltage, the dynamic random access memory 100 has lower input/output power consumption. In addition, the input/output unit 106 is also compatible with an interface provided by the prior art, so power consumption of the dynamic random access memory 100 is much lower than power consumption of the dynamic random access memory operating in the operation voltages specified by the Joint Electron Device Engineering Council.

[0019] To sum up, the dynamic random access memory applied to an

embedded display port makes the memory core unit, the peripheral circuit unit, and the input/output unit operate in lower voltages. Compared to the prior art, power consumption of the dynamic random access memory of the present invention is much lower than power consumption of a dynamic random access memory operating in the operation voltages specified by the Joint Electron Device Engineering Council. Thus, when the dynamic random access memory of the present invention is applied to an embedded display port, the present invention can make system power consumption (e.g. power consumption of a graphic processing unit) be significantly reduced, not make power consumption of the timing controller be increased due to operation of the frame buffer, and extend battery endurance ability of a portable device.

[0020] Although the present invention has been illustrated and described with reference to the embodiments, it is to be understood that the invention is not to be limited to the disclosed embodiments, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0395USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Der-Min		Yuan	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	New Taipei City	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	No.2, Lane 10, Jhongsing St., Xinzhuang Dist.		
Address 2			
City	New Taipei City	State/Province	
Postal Code		Country i	TW

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yen-An		Chang	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

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Mailing Address of Inventor:

Address 1	No.26, Bade 2nd Rd., Toufen City		
Address 2			
City	Miaoli County	State/Province	
Postal Code		Country i	TW

Inventor 3 Remove

Legal Name

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0395USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Wei-Ming		Huang	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

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Mailing Address of Inventor:

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Address 2			
City	Hsinchu County	**State/Province**	
Postal Code		**Country** i	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	27765		
Email Address	rogerchen@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT		
Attorney Docket Number	ETRP0395USA3	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	1	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0395USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16151347	2018-10-04
Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16151347	Continuation of	13922242	2013-06-19
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13922242	Claims benefit of provisional	61672287	2012-07-17

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0395USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13922242	Claims benefit of provisional	61768406	2013-02-23
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0395USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0395USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Etron Technology, Inc.		
Mailing Address Information For Applicant:			
Address 1	No. 6, Technology Road 5		
Address 2			
City	Hsinchu	**State/Province**	
Country	TW	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0395USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

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Signature:

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NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Roger Chen/			Date (YYYY-MM-DD)	2021-03-25
First Name	Roger	Last Name	Chen	Registration Number	67314

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	ETRP0395USA3
	Application Number	
Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Filer:	Winston Hsu/Joy Lai
Attorney Docket Number:	ETRP0395USA3

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	80	80
UTILITY SEARCH FEE	2111	1	350	350
UTILITY EXAMINATION FEE	2311	1	400	400
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**830**

Electronic Acknowledgement Receipt

EFS ID:	42276569
Application Number:	17213133
International Application Number:	
Confirmation Number:	9765
Title of Invention:	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT
First Named Inventor/Applicant Name:	Der-Min Yuan
Customer Number:	27765
Filer:	Winston Hsu/Sibyl Yu
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	ETRP0395USA3
Receipt Date:	25-MAR-2021
Filing Date:	
Time Stamp:	21:06:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$830
RAM confirmation Number	E20213OL07170927
Deposit Account	503105
Authorized User	Sibyl Yu

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Internet Communications Authorized	4160811.PDF	415390 750f02c4b3d72b81d15d27f4e36681d0dbce92aa	no	2
Warnings:					
Information:					
2	Oath or Declaration filed	4160810.PDF	241773 16f8ee034e35795458f9ee511fc10063bc38e42c	no	3
Warnings:					
Information:					
3	Power of Attorney	4160809.PDF	394266 1f51a711b79fb6cb179c4c3b3e5a5e6101aca58a	no	2
Warnings:					
Information:					
4	Drawings-only black and white line drawings	4160446.PDF	21815 2e55a9c6a051ca6bff28f2bf7c9f3fd546e62734	no	1
Warnings:					
Information:					
5	Abstract	4160445.PDF	24325 935e91c4cdc29990c474104a5a6957cd7485402b	no	1
Warnings:					
Information:					
6	Claims	4160444.PDF	25670 e244dc9e5ad89933f6a421b5fd9914d7edea8c85	no	1
Warnings:					
Information:					

7	Specification	4160443.PDF	85875 c4ed2f9eb7a8d87c1be978a806431dafd2fa2d72	no	8
Warnings:					
Information:					
8	Application Data Sheet	4162455.PDF	1771970 8776482b5b9c15ccb208e3e9a656d425947a58ef	no	9
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	35003 a3ccc04aa63c4155d72a5f66724303d86149653b	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	3016087	

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorized/Internet Communications Authorization Withdrawn

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS		
	Application No.	N/A
	Filing Date	N/A
	First Named Inventor	Der-Min Yuan
	Art Unit	N/A
	Examiner Name	N/A
	Practitioner Docket No.	ETRP0395USA3

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. To authorize permission for Internet Communications.

☑ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

II. To withdraw authorization for Internet Communications.

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 67314.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Roger Chen/	03/25/2021
Signature	Date
Roger Chen	3027291562
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/01 (06-12)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN EMBEDDED DISPLAY PORT

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [✓] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Der-Min Yuan Date (Optional) : _____

Signature: Der-Min Yuan

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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This declaration is directed to:

☑ The attached application, or

☐ United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Yen-An Chang Date (Optional) : _____

Signature: Yen-An Chang

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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LEGAL NAME OF INVENTOR

Inventor: Wei-Ming Huang Date (Optional) : _____

Signature: Wei Ming Huang.

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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