

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Yuan et al.
U.S. Patent No.: 12,154,652 Attorney Docket No.: 50095-0279IP1
Issue Date: November 26, 2024
Appl. Serial No.: 18/540,888
Filing Date: December 15, 2023
Title: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN
EMBEDDED DISPLAY PORT

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PETITION FOR *INTER PARTES* REVIEW
OF UNITED STATES PATENT NO. 12,154,652

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LIST OF EXHIBITS

EX1001	U.S. Patent No. 12,154,652 to Yuan et al. (“the ’652 Patent”)
EX1002	Prosecution History of the ’652 Patent (“the Prosecution History”)
EX1003	Declaration and Curriculum Vitae of Dr. David Liu
EX1004	U.S. Patent Application Publication No. 2010/0290300 (“Takahashi”)
EX1005	U.S. Patent Application Publication No. 2012/0327726 (“Tsern”)
EX1006	U.S. Patent Application Publication No. 2010/0142247 (“Schuette”)
EX1007	U.S. Patent Application Publication No. 2012/0327062 (“Endo”)
EX1008	U.S. Patent Application Publication No. 2011/0063927 (“Dono”)
EX1009	U.S. Patent Application Publication No. 2012/0140578 (“Goto”)
EX1010	U.S. Patent No. 7,738,311 (“Youn”)
EX1011	Nakagome et al., “Review and future prospects of low-voltage RAM circuits,” IBM Journal of Research and Development, vol. 47, no. 5.6, p. 525-552 (2003)
EX1012	Keeth et al., <i>DRAM Circuit Design: Fundamental and High-Speed Topics</i> , IEEE Press (2008)
EX1013	“Low Power Double Data Rate 3 (LPDDR3),” JESD209-3, JEDEC Solid State Technology Association (May 2012)

EX1014	VESA Embedded DisplayPort Standard Version 1.3, Video Electronics Standards Association (2011)
EX1015	Craig Wiley, “The New Generation Digital Display Interface for Embedded Applications,” DisplayPort Developer Conference (2010)
EX1016	Prosecution History of U.S. Patent No. 10,998,017
EX1017	Excerpts from Daintith et al., <i>A Dictionary of Computing, Sixth Edition</i> , Oxford University Press (2008)
EX1018	Excerpts from Harry Newton, <i>Newton’s Telecom Dictionary, 24th Edition</i> , Flatiron Publishing (2008)
EX1019	Excerpts from Downing et al., <i>Dictionary of Computer and Internet Terms, Tenth Edition</i> , Barron’s Educational Series, Inc. (2009)
EX1020	Itoh, <i>VLSI Memory Chip Design</i> , Springer Series in Advanced Microelectronics, Springer-Verlag Berlin Heidelberg New York (2001)
EX1021	Oct. 7, 2025 Complaint, <i>WeCrevention, Inc. v. Apple Inc.</i> , Civil Action No. 7:25-CV-458 (W.D. Tex)
EX1022	Micron Electronics, Inc., “DDR3 SDRAM” (2006)
EX1023	U.S. Patent No. 6,271,679
EX1024	“DDR2 SDRAM Specification,” JESD79-2F, JEDEC Solid State Technology Association (November 2009)
EX1025	U.S. Patent Application Publication No. 2010/0061165
EX1026	Jacob et al., <i>Memory Systems: Cache, DRAM, Disk</i> , Morgan Kaufmann Publishers (2008)

EX1027	RESERVED
EX1028	RESERVED
EX1029	Fairchild Semiconductor 74VCXH162244 datasheet (2005)
EX1030	Texas Instruments SN74AUP1G07 datasheet (2012)
EX1031	Wayne Wolf, <i>Modern VLSI Design: IP-Based Design, Fourth Edition</i> , Prentice Hall (2009)
EX1032	Barth et al., “A 45 nm SOI Embedded DRAM Macro for the POWER™ Processor 32 MByte On-Chip L3 Cache,” in <i>IEEE Journal of Solid-State Circuits</i> , vol. 46, no. 1, pp. 64-75, Jan. 2011
EX1033	J. Barth, “eDRAM to the Rescue,” SRC eDRAM (2009)
EX1034	U.S. Patent No. 7,626,883
EX1035	U.S. Patent No. 6,847,578
EX1036	U.S. Patent No. 8,901,009
EX1037	U.S. Patent No. 8,471,362
EX1038	U.S. Patent No. 7,829,410
EX1039	U.S. Patent No. 7,892,943
EX1040	U.S. Patent No. 8,148,763
EX1041	U.S. Patent No. 7,736,987
EX1042	RESERVED

- EX1043 The International Technology Roadmap for Semiconductors - Overall Roadmap Technology Characteristics (2003)
- EX1044 Lee et al., “Tiered-latency DRAM: A low latency and low cost DRAM architecture,” 2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA)
- EX1045 Harvard et al., “A scalable I/O architecture for wide I/O DRAM,” 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)
- EX1046 Prosecution History of U.S. Patent No. 11,894,098
- EX1047 “VESA Publishes Embedded DisplayPort Standard Version 1.5,” <https://www.prnewswire.com/news-releases/vesa-publishes-embedded-displayport-standard-version-1-5--301410053.html/> (accessed Dec. 24, 2025)
- EX1048 Gillingham, “Unleashing the Power of Embedded DRAM” (2005)
- EX1049 AP Memory, AD351216F-x 512Mb LPDDR3, “512Mb LPDDR3 Specification” (2022)
- EX1050 U.S. Patent Application Publication No. 2009/0080234
- EX1051 Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2025) | United States Courts (uscourts.gov), available at: [fcms_na_distprofile1231.2025.pdf](#)

LISTING OF CLAIMS

Claim 1	
[1.1]	A dynamic random access memory (DRAM), comprising:
[1.2]	a DRAM core cell comprised in the DRAM,
[1.3]	wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage,
[1.4]	and the DRAM core cell is a volatile memory cell,
[1.5]	wherein the first voltage is lower than 1.1V; and
[1.6]	an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell,
[1.7]	and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage,
[1.8]	wherein the third voltage is lower than 1.1V, and
[1.9]	wherein the DRAM core cell and the input/output circuit are formed on a single chip,
[1.10]	the input/output circuit is external to the DRAM core cell, and
[1.11]	the first voltage is different from the third voltage.
Claim 2	
[2.1]	A dynamic random access memory (DRAM), comprising:
[2.2]	a DRAM core cell comprised in the DRAM,
[2.3]	wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage,
[2.4]	and the DRAM core cell is a volatile memory cell,

[2.5]	wherein the first voltage is lower than 1.1V; and
[2.6]	an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell,
[2.7]	and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage,
[2.8]	wherein the third voltage is lower than 1.1V;
[2.9]	wherein the DRAM core cell and the input/output circuit are formed on a single chip,
[2.10]	the input/output circuit is external to the DRAM core cell, and
[2.11]	the first voltage is greater than the third voltage.
Claim 3	
[3.1]	A dynamic random access memory (DRAM), comprising:
[3.2]	a DRAM core cell comprised in the DRAM,
[3.3]	wherein the DRAM core cell is supplied with a first voltage to make the DRAM core cell operate at the first voltage,
[3.4]	and the DRAM core cell is a volatile memory cell; and
[3.5]	an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell,
[3.6]	and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage,
[3.7]	wherein the third voltage is lower than 1.1V;
[3.8]	wherein the first voltage is greater than the third voltage, and
[3.9]	the DRAM is capable to be applied to an embedded display port (eDP).

Claim 4	
[4]	The dynamic random access memory of claim 3, wherein the first voltage is lower than 1.1V.
Claim 5	
[5.1]	The dynamic random access memory of claim 3, further comprising: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell,
[5.2]	and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage,
[5.3]	wherein the second voltage is lower than 1.1 V.
Claim 6	
[6]	The dynamic random access memory of claim 5, wherein the first voltage is different from the second voltage.

I. INTRODUCTION

Apple Inc. (“Petitioner”) petitions for IPR of claims 1-6 of U.S. Patent No. 12,154,652 (“the ’652 Patent”) assigned to WeCrevention, Inc. (“Patent Owner”/“PO”). Compelling evidence presented in this Petition demonstrates at least a reasonable likelihood that Apple will prevail with respect to at least one of the Challenged Claims. Accordingly, Apple respectfully submits that an IPR should be instituted, and that the Challenged Claims should be canceled as unpatentable.

II. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’652 Patent is available for IPR. Petitioner is not barred or estopped from requesting an IPR of the Challenged Claims.

B. Challenge and Relief Requested

Petitioner requests an IPR of the Challenged Claims on the grounds set forth in the table below, and requests that each of the Challenged Claims be found unpatentable for the reasons described within the Petition and in EX1003, the Declaration of Dr. David Liu (“Expert Declaration”). EX1003, 1-267.

Asserted Grounds		
GROUND	Claims	Prior Art Basis
1A	1-6	§102/103: Takahashi (US2010/0290300)

Asserted Grounds		
GROUND	Claims	Prior Art Basis
1B	1-6	§103: Takahashi+Tsern (US2012/0327726)+Schuette (US2010/0142247)
1C	3-6	§102/103: Takahashi+Endo (US2012/0327062)
1D	3-6	§103: Takahashi+Tsern+Schuette+Endo
2A [2A.1]	1-6	§103: Dono (US2011/0063927)+Goto (US2012/0140578) [§103: Dono+Goto+Youn (US7738311)]
2B [2B.1]	3-6	§103: Dono+Goto+Endo [§103: Dono+Goto+Youn+Endo)]

The '652 Patent was filed on 12/15/23 and claims priority from several previously-filed applications, the earliest of which was filed on 7/17/12. Each of the references asserted in this Petition qualifies as prior art even if the 7/17/12 date (hereinafter “Critical Date”)¹ is used as the '652 Patent's earliest possible priority date.

Reference	Filing/Publication dates	Prior art under ²
Takahashi	(F) 4/28/2010;	§102(a), (b), (e)

¹ Petitioner does not concede that the Challenged Claims are entitled to the 7/17/12 date.

² Petitioner assesses the '652 Patent under pre-AIA 35 U.S.C. If the effective filing date is taken as 6/19/2013 (the filing date of Application No. 13/922,242),

Reference	Filing/Publication dates	Prior art under ²
	(P) 11/18/2010	
Dono	(F) 9/10/2010; (P) 3/17/2011	§102(a), (b), (e)
Endo	(F) 4/5/2012; (P) 12/27/2012	§102(e)
Schuette	(F) 12/7/2009; (P) 6/10/2010	§102(a), (b), (e)
Tsern	(F) 2/23/2010 (provisional); 12/1/2010 (PCT); (P) 12/27/2012	§102(e)
Goto	(F) 11/28/2011; (P) 6/7/2012	§102(a), (e)
Youn	(F) 11/6/2007; (P) 6/15/2010	§102(a), (b), (e)

All cited references are analogous art at least insofar as they are from the same field of endeavor (e.g., DRAM) as the '652 Patent, and are pertinent to the problems the '652 Patent was trying to solve. EX1001, 2:18-34, 4:40-61, 5:33; EX1004, [0018], [0045], [0082]-[0083]; EX1005, [0005], [0019]; EX1006, [0003], [0014],

the '652 Patent is subject to post-AIA 35 U.S.C, and the applied references are also prior art.

[0029]; EX1007, [0034]-[0035]; EX1008, [0005]-[0007], [0024]; EX1009, [0022], [0027]; EX1010, 5:49-67; EX1003, 50.

C. Claim Construction

The recited “input/output circuit” should be construed as a §112(f) means-plus-function limitation. Based on its name, the input/output circuit is a circuit that performs input and/or output functions with respect to a memory. EX1001, 5:26 (“an input/output circuit comprised in the DRAM”).

The Specification’s most detailed description of corresponding structure is provided at 2:49-64 in relation to the “Input/output unit” 106 that is depicted in the Specification’s sole “FIGURE” as one box connected to two other boxes (respectively labeled “Memory core unit” 102 and “Peripheral circuit unit” 104). At 2:49-64, the Specification notes without further explanation that “the dynamic random access memory **100** includes a memory core unit **102**, a peripheral circuit unit **104**, and an input/output unit **106**, where the peripheral circuit unit **104** is electrically connected to the memory core unit **102**, and the input/output unit **106** is electrically connected to the peripheral circuit unit **104** and the memory core unit **102**.” EX1001, 2:49-64; *see also* Abstract, 1:65-2:34.

As explained in detail in Section V., *infra*, the prior art cited and applied in this Petition discloses the claimed input/output functions and at least as much structure as the ’652 Patent’s Specification with respect to the applied input/output

circuits; in doing so, the applied prior art anticipates or renders obvious the Challenged Claims, regardless of whether “input/output circuit” is construed as a §112(f) means-plus-function limitation. EX1003, 73-76.

All other claim terms should be construed according to their ordinary and customary meaning under the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. Petitioner submits that no other claim terms need be construed to resolve issues of controversy in the present Petition, but reserves the right to respond to construction issues raised by Patent Owner. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Petitioner is not conceding that each challenged claim satisfies all statutory requirements (for example, that the ’652 Patent provides adequate structure for the “input/output circuit”), nor waiving arguments/grounds that cannot be raised in this proceeding.

III. THE ’652 PATENT

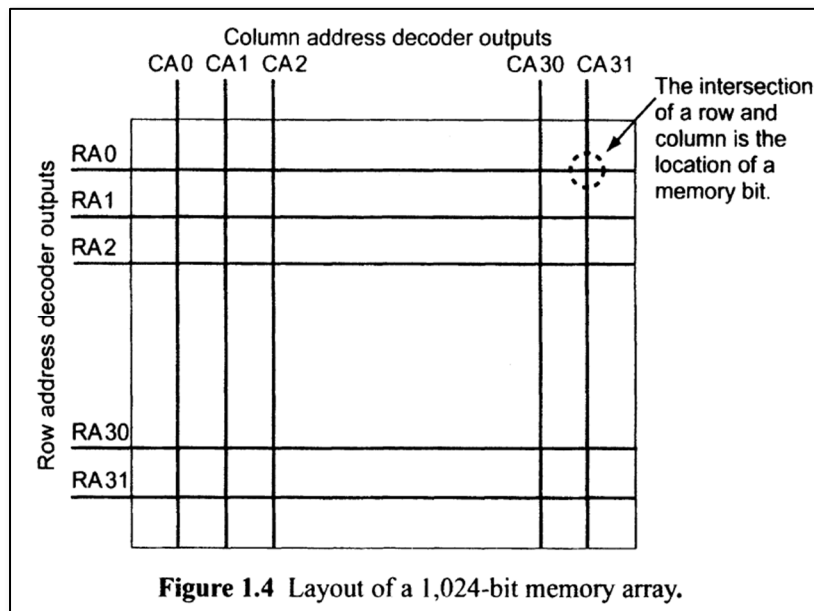
A. Summary

The ’652 Patent relates to two technologies: dynamic random access memory (DRAM) and embedded display port interfaces. EX1003, 29-30.

1. DRAM

DRAM is a type of random access memory typically used as the primary memory of computing devices. EX1003, 31. In a DRAM device, memory cells are organized in an array. Each memory cell has a “row” position and a “column” position with which the memory cell can be addressed. EX1012, 16-18; EX1003, 31.

Voltages can be applied to “wordlines” (corresponding to a row) and “bitlines” (corresponding to a column) to store a 0 or 1 in a target memory cell, or to read out stored data. EX1012, 17-24; EX1003, 32. DRAM is referred to as “dynamic” because, once stored in a cell, charge (representing data) will “leak off over time.” EX1012, 20; EX1003, 32. To prevent loss of data, a “refresh” operation is performed periodically. EX1012, 19; EX1003, 32.



EX1012, FIG. 1.4

A DRAM device is provided with one or more external voltages, which may be converted to internal voltages supplied to various circuits of the device. EX1003, 34. The Low Power Double Data Rate 3 (LPDDR3) standard, published in May 2012 by the Joint Electron Device Engineering Council (JEDEC), defines several external voltages. EX1013, 83; EX1003, 34.

The '652 Patent purports to improve DRAMs by specifying lower voltages for memory circuitry. EX1001, 4:62-65; EX1003, 35. Specifically, the '652 Patent describes that DRAMs can have “operation voltages” of “<1.1 V” for each of a “memory core unit,” a “peripheral circuit unit,” and an “input/output unit.” EX1001, Table II. These voltages allegedly result in “power consumption [that]...is much

lower than power consumption of the [DRAM] operating in the operation voltages specified by the [JEDEC].” EX1001, 4:6-11; EX1003, 35.

The ’652 Patent provides no technical detail on how DRAM using these low voltages might be achieved. EX1003, 36.

The desire for low voltage DRAM operation was not new and, unlike the ’652 Patent, the prior art applied in this Petition provides not only *disclosure* of low DRAM voltages, but also details on *how the low voltages may be successfully used in real DRAM circuits*. EX1003, 37. Indeed, voltages within the ranges recited by the ’652 Patent had been a subject of research for decades, and low-voltage DRAM circuits had been successfully manufactured and publicized. EX1011; EX1043; EX1003, 36.

2. Embedded Display Port

The embedded display port (eDP) standard “defines requirements and options of a standardized display panel interface for embedded display applications.” EX1014, 12. Version 1.3 of the eDP standard, published in 2011, introduces a “panel self-refresh” (PSR) feature. EX1014, 12, 21, 65; EX1003, 38-39.

According to eDP 1.3, a display device’s “timing controller” (TCON) includes a “remote frame buffer” (RFB). EX1014, 27, 65; EX1015, 24; EX1003, 39. The RFB “can maintain [a] display image without receiving video data from [the] GPU [graphical processing unit].” EX1015, 25. This means that, when an eDP 1.3

display is showing a still image, the GPU can “enter a low power state...[a]llowing the GPU to power down between display updates.” EX1015, 25; EX1003, 39. Instead of using the GPU, the display can draw the static image from the RFB, reducing power consumption. EX1015, 26; EX1003, 39-40.

The '652 Patent states that “power consumption of the timing controller is increased due to operation of the frame buffer,” and therefore seeks “to design the frame buffer to reduce the power consumption.” EX1001, 1:57-60. According to the '652 Patent, “the operation voltages specified by [JEDEC] can not satisfy requirements (that is, the lower operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3.” EX1001, 3:22-27; EX1003, 41.

The '652 Patent does not describe what these “requirements” are, and, as discussed below in §V.A.2(c) ([3.9]), the eDP 1.3 standard in fact includes no such power requirements. EX1003, 42.

Despite that, the '652 Patent asserts that “power consumption of the [DRAM] of the present invention is much lower than power consumption of a [DRAM] operating in the operation voltages specified by [JEDEC],” and that “when the [DRAM] of the present invention is applied to an embedded display port, the present invention can make system power consumption...be significantly reduced.” EX1001, 4:65-5:7; EX1003, 43.

B. Prosecution History

The '652 Patent was issued on November 26, 2024 as a continuation of U.S. Patent No. 11,894,098 (“the '098 Patent”), which was itself a continuation of U.S. Patent No. 10,998,017 (“the '017 Patent”).

The grandparent '017 Patent received rejections over references including “Mohammad” (US 2009/0122620) and/or Takahashi (EX1004), and the final rejection was over Takahashi. EX1016, 37-43, 84-91, 120-129, 159-166, 188-195. The claims of the '017 Patent were allowed after the applicant amended the sole independent claim to recite that “the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP),” and the Examiner also cited this feature in the Reasons for Allowance. EX1016, 12, 28. The '652 patent's independent claim 3 recites a similar element. EX1003, 44-45.

Despite the “eDP” feature being the apparent reason for allowance of the '017 Patent, the record is silent as to what voltages would be “capable of making the DRAM be applied to an embedded display port (eDP).” In fact, the eDP 1.3 standard cited by the '017 and '652 Patents includes no voltage or power requirements for a memory applied to an eDP. EX1003, 46. *See* §V.A.2(c) ([3.9]). As discussed below, the cited DRAMs—including Takahashi's—were entirely capable of being applied to an eDP. EX1003, 46.

The parent '098 patent was allowed over Takahashi and Mohammad based on an additional oversight by the Examiner. EX1046, 10-17, 74-91, 130-138, 162-172. The Examiner cited Takahashi's power supply voltage VDD for each of the "first voltage" and the "second voltage" of the claims, and therefore erroneously concluded in the Notice of Allowance that the art did not teach "the second voltage...is different from the first voltage." EX1046, 15, 79-80; EX1003, 47. The Examiner apparently overlooked Takahashi's *other* supply voltage, VPPL, which is different from VDD, is less than 1.1V, and is supplied to memory cells, thereby teaching the "first voltage" of the claims. EX1004, [0083]-[0084], FIGS. 7-8; EX1003, 47.

In Grounds 1A-1D below, Takahashi's VPPL is applied as the first voltage and VDD is applied as the second voltage, remedying the Examiner's error. EX1003, 48.

The '652 Patent was allowed without receiving prior art rejections. EX1002, 15-21, 46-52. The "Reason for Allowance" referred generically to "combination [of] features or limitations recited in the independent claims 1, 2, and 3," without providing substantive reasons for allowance. EX1002, 20. EX1003, 49.

IV. LEVEL OF ORDINARY SKILL

The range of qualifications for a POSITA would have included at least a master's degree in electrical engineering, or a comparable field, and at least two

years of professional experience working with semiconductor memory, including DRAM. EX1003, 27-28. Additional years of experience could substitute for an advanced-level degree (and vice versa). *Id.*

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A: §102/103: Takahashi anticipates and renders obvious claims 1-6

1. Takahashi

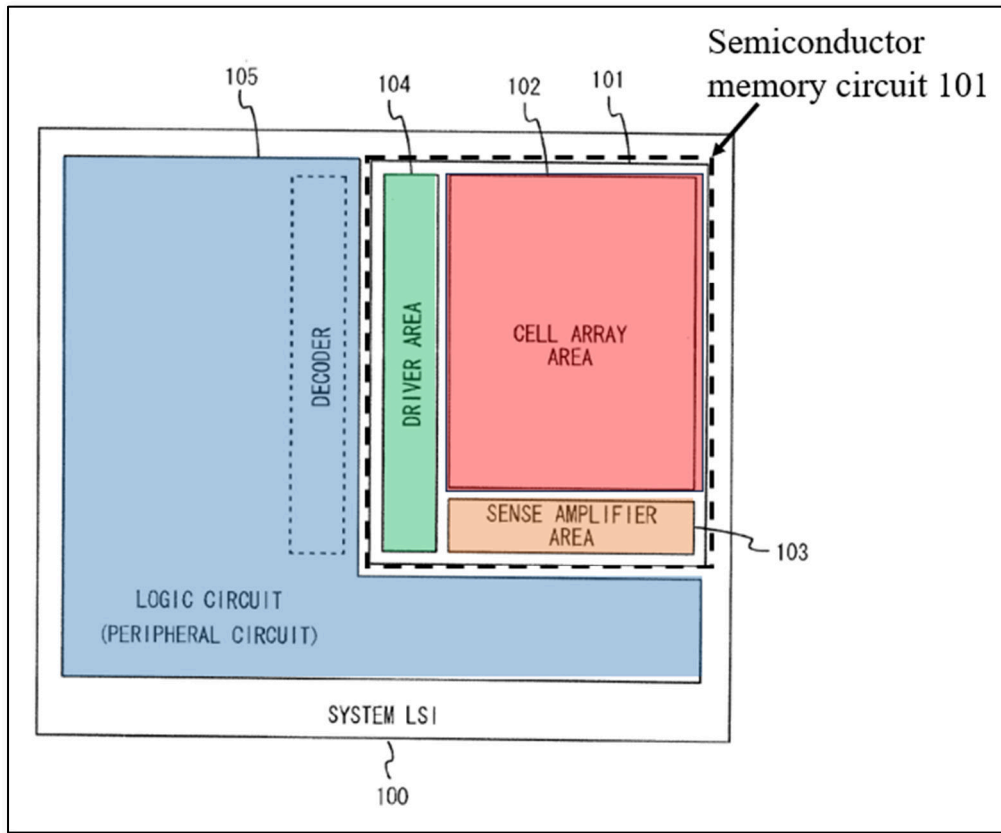
Takahashi describes a “built-in DRAM” that can provide “higher speed operation.” EX1004, [0021], [0047]; EX1003, 51.³

As shown in implementations of Takahashi depicted, e.g., in FIG. 1, Takahashi’s “device 100” includes a “semiconductor memory circuit 101” and a “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit.”⁴ EX1004, [0047], [0078]; EX1003, 52. Memory circuit 101 includes “a cell

³ This discussion of Takahashi is incorporated further into Grounds 1B-1D. Similarly, discussion of other references is incorporated into all grounds advancing the same.

⁴ In below addressing invalidity of the Challenged Claims over the teachings of the cited references, Petitioner relies on the teachings of those references as would have

array area 102, a sense amplifier area 103, and a driver area 104.” EX1004, [0047]; EX1003, 52.

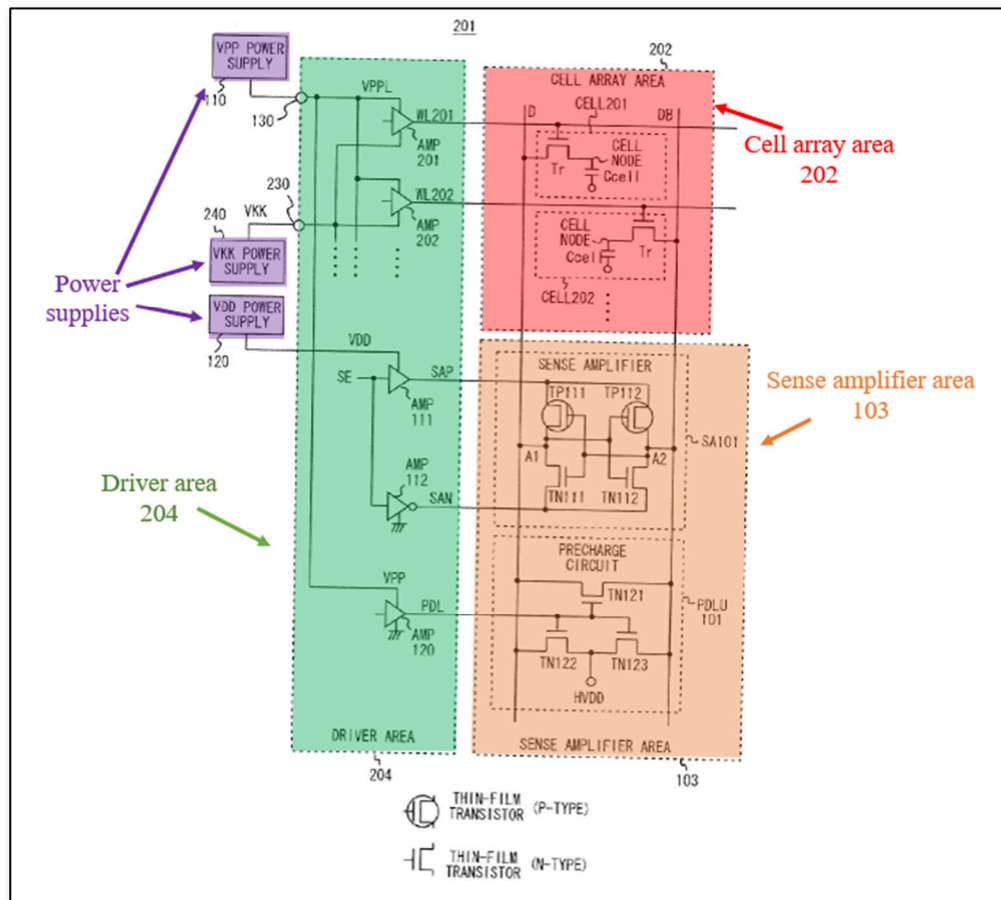


Takahashi, FIG. 1

Takahashi’s FIG. 7 (reproduced below) shows a configuration of a memory circuit 201 similar to that of FIG. 1. EX1004, [0077]-[0079]; EX1003, 53. Power to a cell array area 202, a sense amplifier area 103, and a driver area 204 is supplied by a VPP power supply 110, a VKK power supply 240, and a VDD power supply 120.

been understood by a POSITA, without necessarily relying upon incorporation of each or any of the disclosed or referenced exemplary details.

EX1004, [0081]-[0083], FIG. 7; EX1003, 54. These power supplies output voltages VPPL, VKK, and VDD, respectively. EX1004, [0081]-[0083], FIG. 7; EX1003, 54. VDD is also provided to the logic circuit 105. EX1004, [0045]-[0046]; EX1003, 54.



Takahashi, FIG. 7

Takahashi provides specific values for these voltages: “the power supply voltage VDD is 0.8 V, the voltage VPPL is 1.0 V, and the voltage VKK is -0.3 V.” EX1004, [0084]; EX1003, 55.

2. Analysis of claims

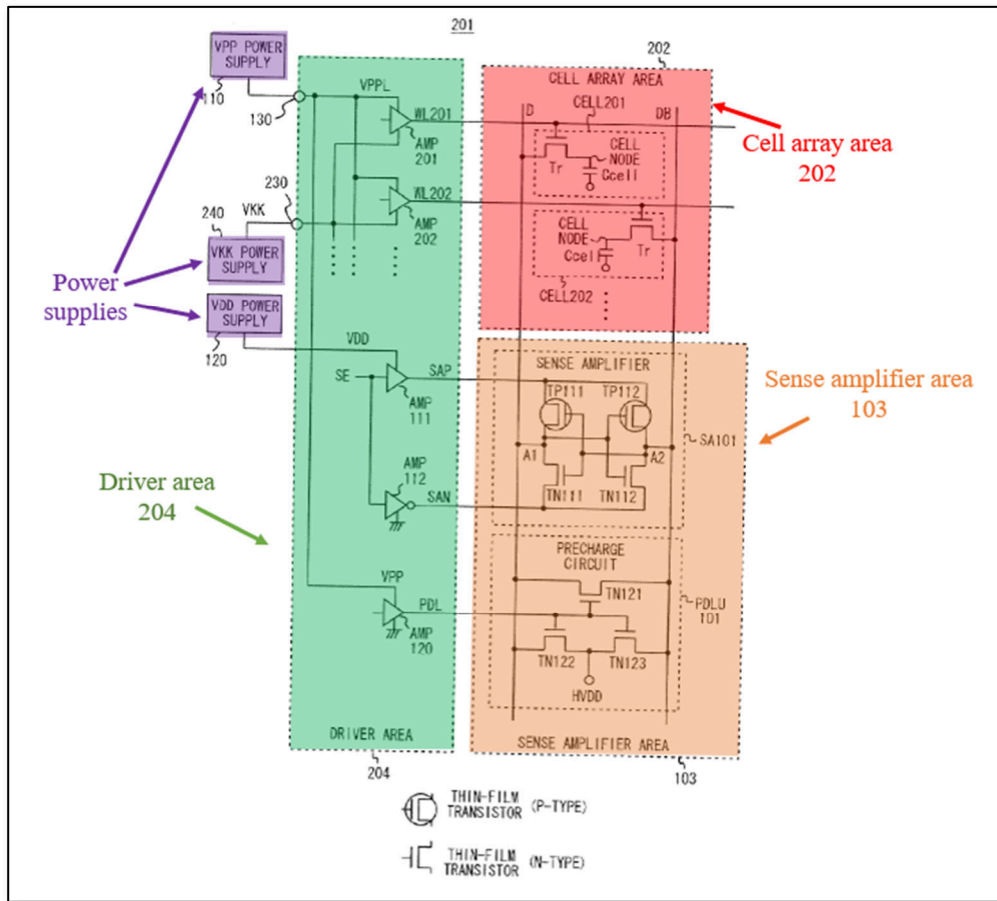
(a) Claim 1

*[1.1]: A dynamic random access memory (DRAM), comprising:*⁵

Takahashi's "semiconductor memory circuit 201 is a built-in DRAM of a system LSI." EX1004, [0078]; EX1003, 57.

In more detail, and as shown in Takahashi's FIG. 7 (reproduced below), Takahashi's DRAM semiconductor memory circuit 201 includes a sense amplifier area 103, a driver area 204, and a cell array area 202 that includes memory cells. EX1004, [0077]-[0083], FIG. 7; EX1003, 58. Cell array area 202 is supplied with VPP and VKK, while sense amplifier area 103 and driver area 204 are supplied with VDD. EX1004, [0081]-[0083], FIG. 7; EX1003, 58.

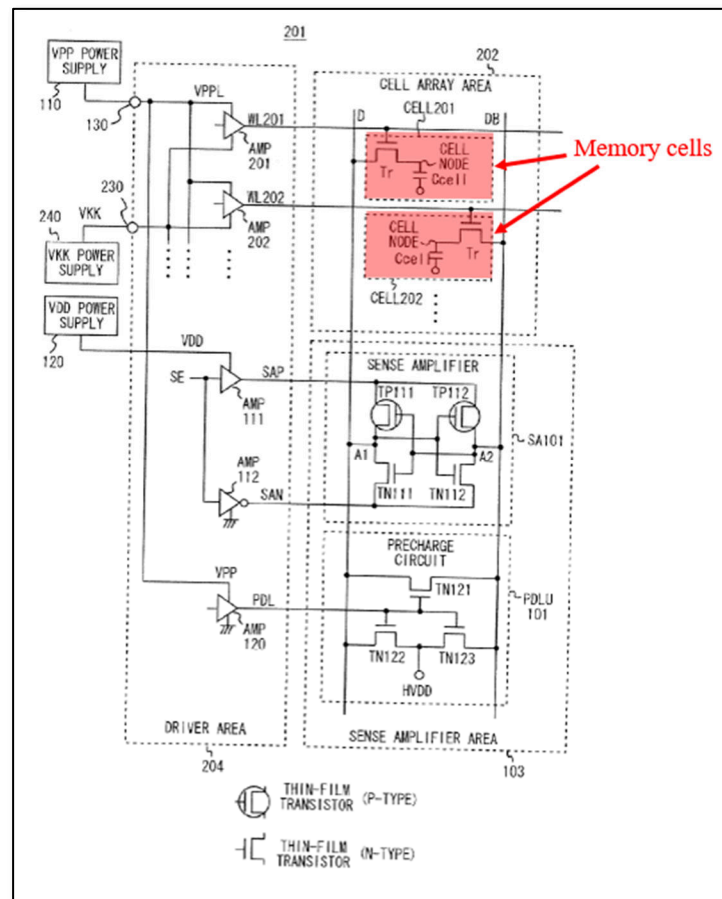
⁵ Petitioner does not concede that this preamble or other preambles are limiting.



Takahashi, FIG. 7

[1.2]: a DRAM core cell comprised in the DRAM,

The “memory cells” in Takahashi’s DRAM are DRAM core cells. EX1004, [0079]-[0080]; EX1003, 59. For example, Takahashi discloses that the “semiconductor memory circuit 201 includes a cell array area 202... The cell array area 202 includes multiple memory cells CELLS.” EX1004, [0079]-[0080]; EX1003, 59.

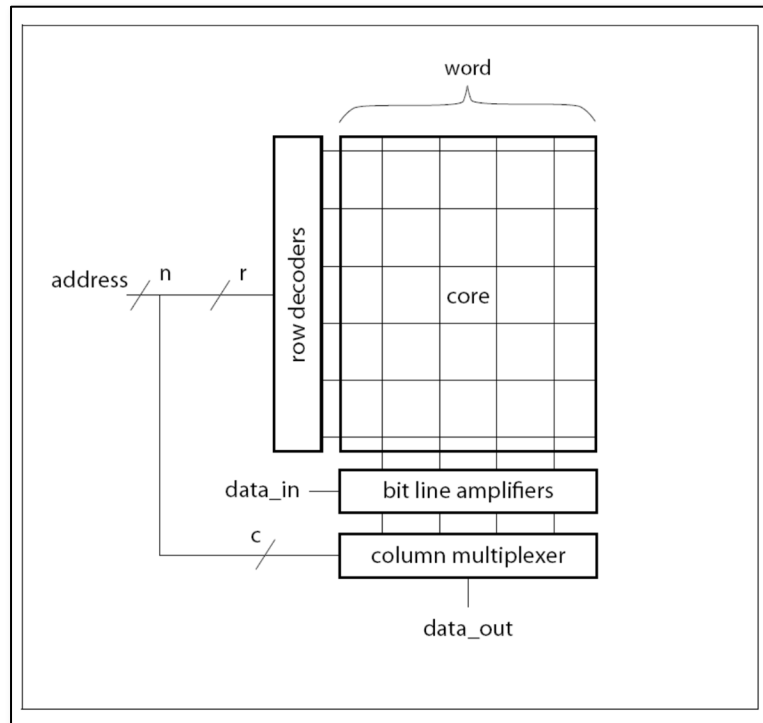


Takahashi, FIG. 7

A POSITA would have understood that these DRAM memory cells are each a “DRAM core cell.” EX1003, 60. As Dr. Liu explains, the “core” in “DRAM core cell” refers to, or at least encompasses, the cell array of a memory, which performs the memory’s data storage function. EX1003, 60-62. Thus, DRAM memory cells are “DRAM core cell[s].” EX1003, 60.

For example, the textbook *Modern VLSI Design: IP-Based Design* provides the below diagram in which the memory cell array is labeled as a “core.” EX1031, 385; EX1003, 61. The same textbook also refers to the “memory core” and refers to

a DRAM data storage cell as a “RAM core cell.” EX1031, 385, 391-392; EX1003, 61.

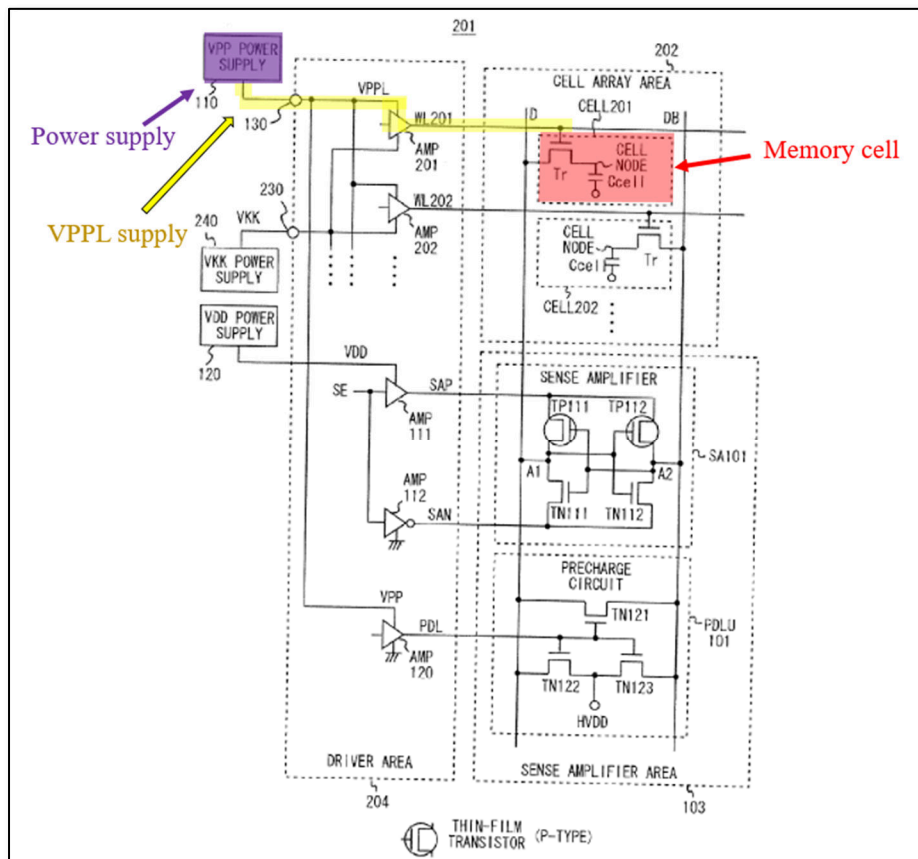


EX1031, Figure 6-16

[1.3]: wherein the DRAM core cell is supplied with a first voltage within a first voltage range to make the DRAM core cell operate at the first voltage,

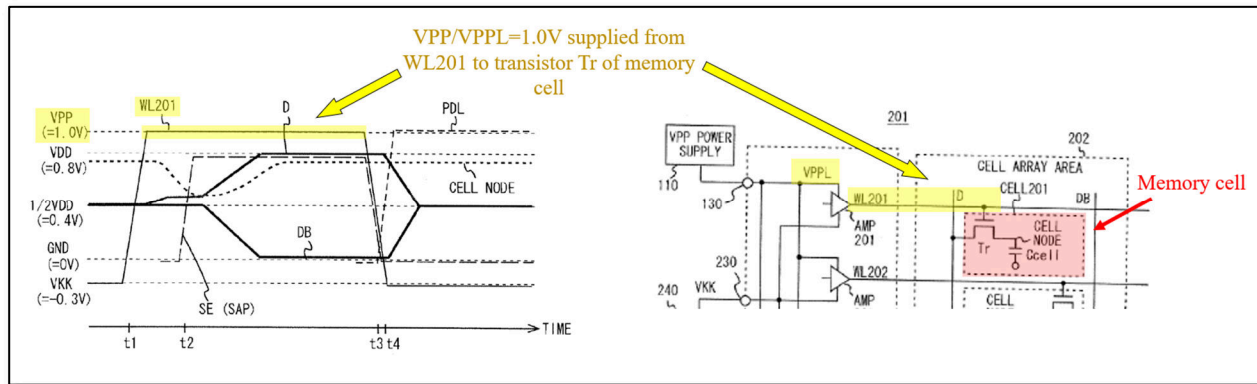
Takahashi’s memory cells are supplied with a **first voltage VPPL**⁶ to make those cells operate at that voltage. EX1003, 63-64. As Takahashi explains, “the memory cells ...use a voltage VPPL.” EX1004, [0081]; EX1003, 63. Supply of VPPL to memory cells is shown below. EX1004, FIG. 7; EX1003, 63.

⁶ Emphasis is added throughout, except where noted otherwise.



Takahashi, FIG. 7

Supply of the first voltage VPPL/VPP to a memory cell is shown explicitly in Takahashi FIG. 8. EX1003, 65. As shown, “at the time t1, the word signal WL201 rises to the voltage VPP [=1.0 V].” EX1004, [0084]-[0085], FIG. 8; EX1003, 65. The wordline 201 is connected to a gate of the transistor Tr, such that a first voltage of 1.0 V is supplied to memory cell 201. EX1004, [0083]-[0085], FIG. 8; EX1003, 65.



Left: Takahashi, FIG. 8; Right: Takahashi, FIG. 7 (partial)

The memory cell “use[s],” or operates at, the “voltage VPPL.” EX1004, [0081]; EX1003, 66. For example, based on provision of VPPL to the memory cell, “CELL 201 is turned on.” EX1004, [0085]; EX1003, 66.

Claim 1 recites that the first voltage is “within a first voltage range,” but none of the Challenged Claims limit the “first voltage range,” or even refer to it again. The “first voltage range” is therefore any range that includes the claimed “first voltage” that is “lower than 1.1V,” for example, 0.5-1.5 V. EX1001, 5:21-5:25. Takahashi’s disclosed VPPL=1.0V is “within” any such range. EX1003, 67-68.

Further, a POSITA would have understood that the voltage VPPL is “within a first voltage range” due to standard voltage variation. EX1003, 69. Dr. Liu describes that in practice “every voltage is defined or provided within a range... attributable to non-idealities such as temperature dependence, device-to-device variation, load dependence, and the like.” EX1003, 69. For example, Takahashi refers to VPPL as being “reduced to about 1.0V,” where “about” might refer to a

small level of expected variation. EX1004, [0083]; EX1003, 69. This small variation would have been understood by a POSITA as a “first range” that the first voltage VPPL is within. EX1003, 69.

[1.4]: and the DRAM core cell is a volatile memory cell,

A POSITA would have understood that Takahashi’s DRAM (dynamic random access memory) core cell is, by definition, a volatile memory cell. EX1003, 70-71. For example, *A Dictionary of Computing* describes “dynamic memory” as a “form of **volatile** semiconductor memory,” adding that DRAM is the “most common example.” EX1017, 4-5. *See also* EX1018, 4-5; EX1019, 3-4; APPLE-1003, 71.

[1.5]: wherein the first voltage is lower than 1.1V; and

Takahashi discloses that the first voltage VPPL is **1.0 V**, which is lower than 1.1 V. EX1003, 72. *See* Takahashi [0083] (“the voltage VPPL...can be reduced to about 1.0V”), FIG. 8. EX1004, [0083]-[0084], FIG. 8; EX1003, 72.

[1.6]: an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell,

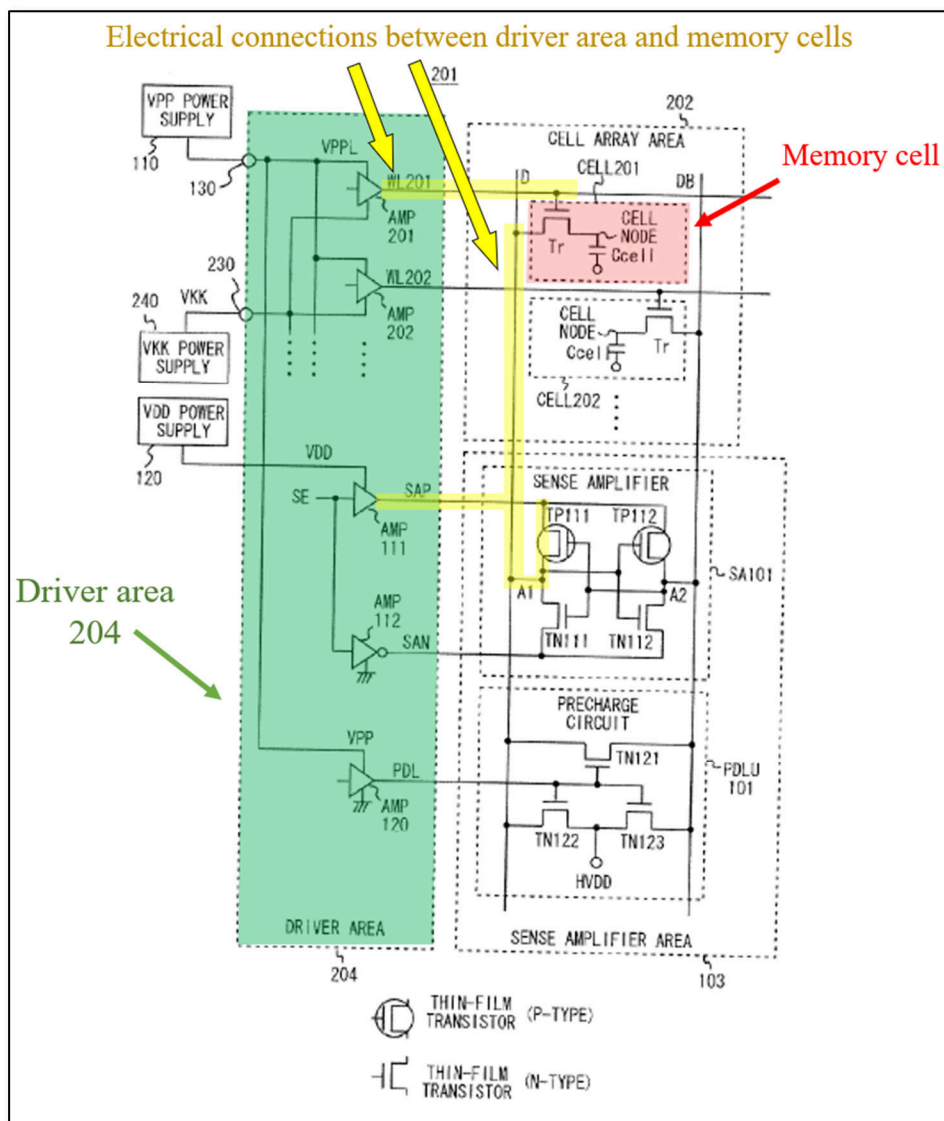
A POSITA would have understood and found obvious that, in the context of embedded DRAMs like Takahashi’s, the driver area 204 constitutes an input/output circuit. EX1003, 76. As Dr. Liu explains, this is because, in an embedded DRAM which may lack off-chip I/O circuitry, the driver area 204 performs the function of receiving external inputs used to write to and read from the memory cell array.

EX1003, 76-79. For example, to perform a data readout operation, the amplifier 111 of the driver area 204 receives, as input from outside the semiconductor memory circuit 201, a “control signal SE” that causes voltage amplification and data output. EX1004, [0084]-[0086], FIGS. 7-8; EX1003, 80. Thus, the driver area 204 performs the function of receiving external inputs and translating those inputs into internal signals of the semiconductor memory circuit 201—that is, it performs the function of an input/output circuit. EX1003, 80.

The driver area 204 thus performs the claimed input/output function and, as shown in FIG. 7, Takahashi discloses a level of structural detail exceeding that of the input/output unit 106 of the '652 Patent. EX1004, FIG. 7; EX1001, FIGURE; EX1003, 80.

As discussed below for [5.1] in §V.A.2(e), consistent with applicant's statements during prosecution, the driver area 204 would also have been understood by a POSITA to be a peripheral circuit. EX1003, 81. Thus, in the context of an embedded DRAM like Takahashi's, the driver area 204 would be understood by a POSITA as a peripheral circuit *or* as an input/output circuit. EX1003, 81. Consistent with this understanding, in Grounds 1A and 1C, Petitioner applies the driver area 204 as an input/output circuit. In Grounds 1B and 1D, Petitioner alternatively applies the driver area 204 as a peripheral circuit and not as an input/output circuit. Both understandings are consistent with the understanding of a POSITA. EX1003, 81.

Takahashi's input/output circuit (driver area 204) is electrically connected to the DRAM core cell (memory cells of cell area 202). EX1003, 82. For example, the driver area 204 is electrically connected to the memory cells through wordline WL201, sense amplifier control line SAP, sense amplifier SA101, and bitline D, as shown in FIG. 7. EX1004, [0007], [0009], [0081], [0086], FIG. 7; EX1003, 82.

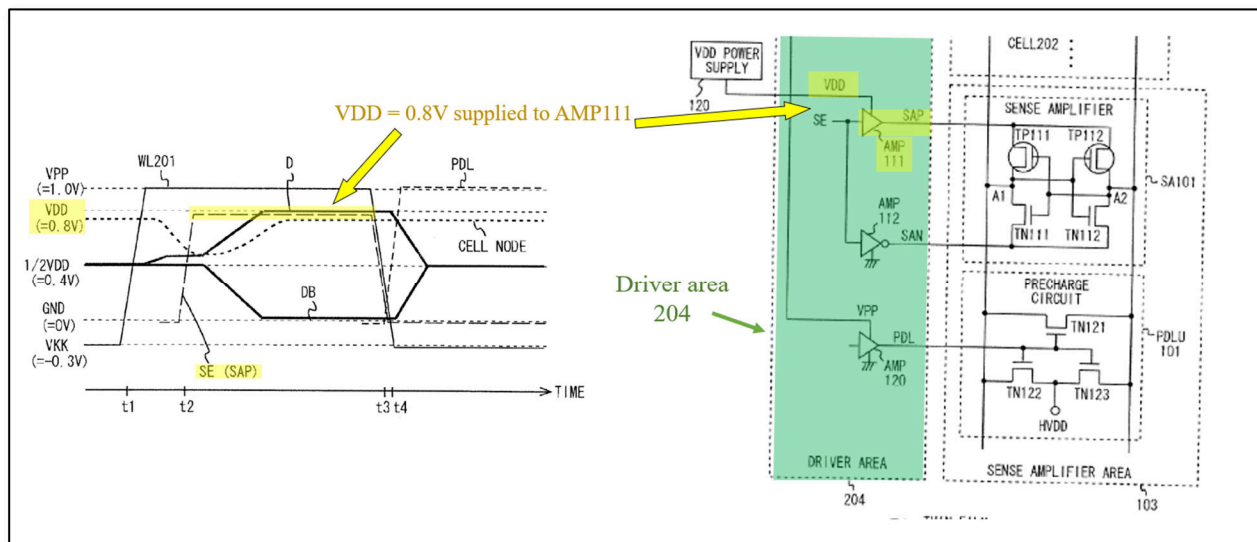


Takahashi, FIG. 7

[1.7]: and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage,

The driver area 204 (here applied as the input/output circuit) is supplied with and operates at a **third voltage VDD**. EX1004, [0055], FIG. 7; EX1003, 83. For example, VDD is supplied to the driver area 204 when “[a] power supply voltage [VDD] of the driver amplifier AMP111 is supplied from a VDD power supply 120,” and the driver amplifier AMP111 of the driver area 204 correspondingly operates at VDD. EX1004, [0055]; EX1003, 83, 85.

Supply of the third voltage VDD to the driver area 204 is shown in Takahashi FIGS. 7 and 8. EX1003, 84.



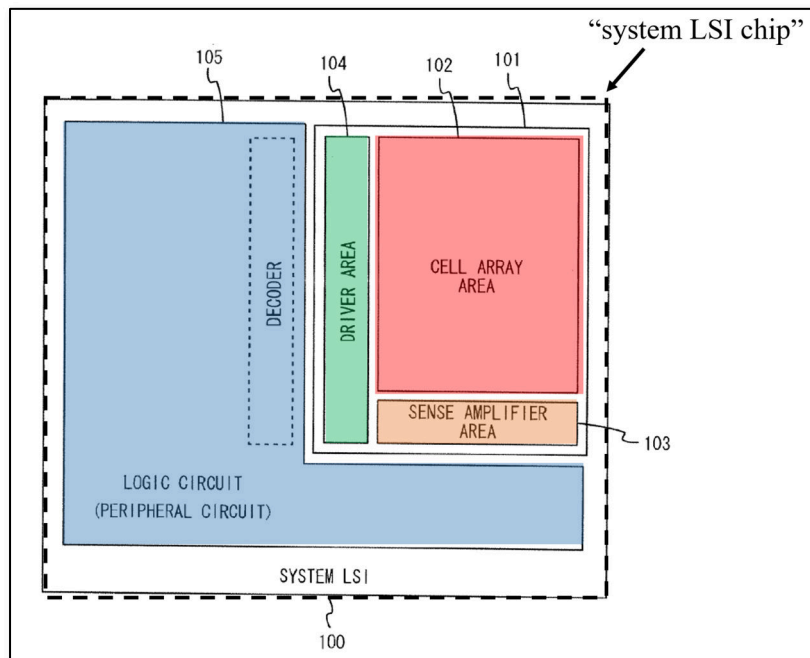
Left: Takahashi, FIG. 8; Right: Takahashi, FIG. 7 (partial)

[1.8]: wherein the third voltage is lower than 1.1V, and

Takahashi's third voltage, VDD, is 0.8 V, which is lower than 1.1 V. EX1003, 86. *See, e.g.,* Takahashi [0078] ("VDD is 0.8V or lower"), [0084] ("the power supply voltage VDD is 0.8 V"); FIG. 8 ("VDD (=0.8V)")." EX1004, [0078], [0084], FIG. 8; EX1003, 86.

[1.9]: wherein the DRAM core cell and the input/output circuit are formed on a single chip,

Takahashi describes "a system LSI chip" that includes the cell array area 102 (202 in FIGS. 7-10B) and the driver area 104 (204), and thereby discloses that the DRAM core cell and input/output circuit (driver area 204) are formed on a single chip. EX1004, [0043], FIG. 1; EX1003, 87.



Takahashi, FIG. 1⁷

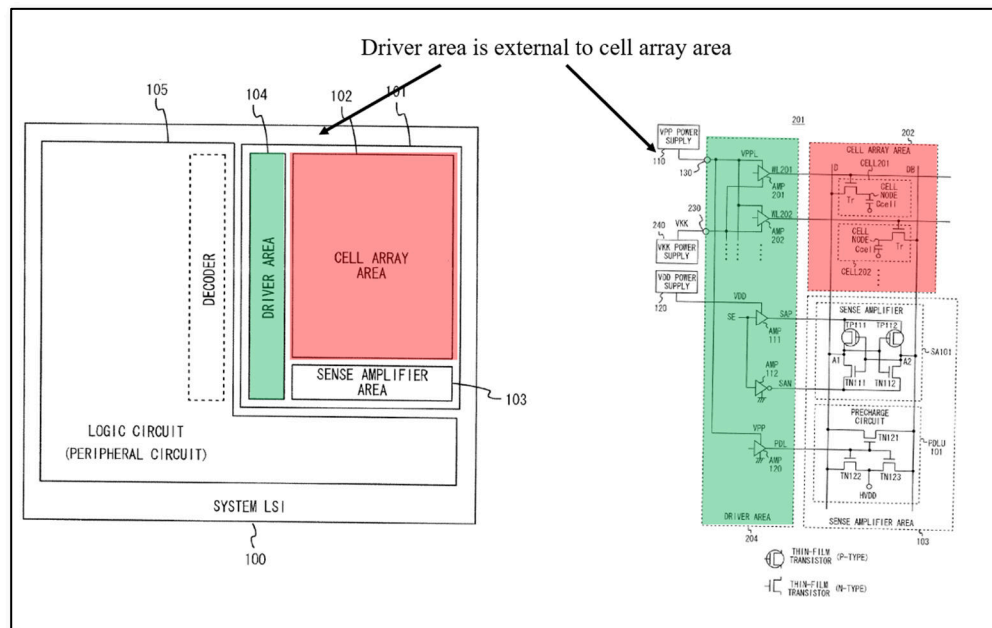
⁷ Takahashi's FIG. 1 depicts a "semiconductor integrated device 100" of Takahashi's "First Exemplary Embodiment," and FIGS. 7 and 8 relate to a "semiconductor integrated device 200" of a "Second Exemplary Embodiment." EX1004, [0026], [0034], [0043], [0077]; EX1003, 87. Takahashi explains that "the semiconductor integrated device 200 of the second exemplary embodiment has a configuration in which the semiconductor memory circuit 101 of the semiconductor integrated device 100 shown in FIG. 1 is replaced with the semiconductor memory circuit 201." EX1004, [0077]. From this and other disclosure, a POSITA would have understood that the device 200 includes substantially similar elements (including the

Takahashi further describes that a prior art “semiconductor memory circuit 1” is “integrated into one chip”; from this and related description, a POSITA would have understood that the semiconductor memory circuit 201 is similarly formed on a single chip. EX1004, [0005], [0014], [0018], [0044]-[0046], [0078]-[0083], FIGS. 2, 7, 12; EX1003, 88-89. For example, the semiconductor memory circuit 1 is illustrated in FIG. 12 in a manner matching the illustrations of circuits 101, 201. EX1003, 88.

[1.10]: the input/output circuit is external to the DRAM core cell, and

Takahashi’s driver area 204 (input/output circuit) is external to the cell array area 202, e.g., as shown in FIGS. 1 and 7. EX1004, FIGS. 1, 7; EX1003, 94.

logic circuit 105), arranged in substantially the same way, as the device 100 of FIG. 1. EX1003, 90-93. Accordingly, this Petition utilizes FIG. 1 in connection with the device 200.



Left: Takahashi, FIG. 1; Right: Takahashi, FIG. 7

[1.11]: the first voltage is different from the third voltage.

See [1.5] and [1.8] above. Takahashi's first voltage VPPL is 1.0V, which is different from the 0.8V of Takahashi's third voltage VDD. EX1004, [0078], [0083]-[0084], FIG. 8; EX1003, 95.

(b) Claim 2

Claim 2's elements are found identically in claim 1, except for [2.11] discussed below. For [2.1]-[2.10], see [1.1]-[1.10] in §V.A.2(a), respectively. EX1003, 96.

[2.11]: the first voltage is greater than the third voltage.

See [1.5] and [1.8] in §V.A.2(a). Takahashi's first voltage VPPL is 1.0V, which is greater than the 0.8V of Takahashi's third voltage VDD. EX1004, [0078], [0083]-[0084], FIG. 8; EX1003, 97.

(c) Claim 3

[3.1]-[3.7]: See [1.1]-[1.4] and [1.6]-[1.8] in in §V.A.2(a), respectively.

[3.8]: See [2.11] in §V.A.2(b).

[3.9]: the DRAM is capable to be applied to an embedded display port (eDP).

As discussed in §III.A.2, the '652 Patent describes use of its DRAM as a "frame buffer of a timing controller" of the eDP 1.3 standard. EX1001, 1:29-54, 2:49-53; EX1003, 100. The frame buffer holds static image data for presentation on a display. EX1001, 1:29-54; EX1015, 25; EX1003, 100.

A POSITA would have understood that Takahashi's device is "capable to be applied to an embedded display port (eDP)," for example, as a frame buffer. EX1003, 101.

Although the '652 Patent states that existing JEDEC "operation voltages...can not satisfy requirements (that is, the low operating power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3," the eDP 1.3 standard includes no voltage or power consumption requirements for the frame buffer. *See generally* EX1014; EX1001, 3:23-27; EX1003, 102.

More, a POSITA would have understood that a conventional memory, including Takahashi's, would be "capable to be applied" as an eDP 1.3 frame buffer, at least because of the conventional memory's ability to store and provide data representing a static image, consistent with the eDP 1.3 standard. EX1003, 103.

Notable, "capable [of]" is broader, for example, than "configured to" or "adapted to." *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1349 (Fed. Cir. 2012); *In re Giannelli*, 739 F.3d 1375, 1379 (Fed. Cir. 2014). A POSITA would have recognized Takahashi's memory, which is described as "hold[ing] data" and providing "high-speed operation," as satisfying this relatively low bar for being "capable to be applied" as a frame buffer. EX1004, [0047], [0082]; EX1003, 103.

It would also have been obvious to try applying Takahashi's DRAM as an eDP 1.3 frame buffer, because DRAM was one of a small number of memory types, along with, for example, static RAM (SRAM) and flash memory. EX1031, 381-394; EX1003, 104-105. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

Further, to the extent the '652 Patent erroneously links "capable to be applied to an embedded display port (eDP)" to low-voltage operation, then Takahashi's device which has first (VPPL) and third (VDD) voltages that satisfy the "< 1.1 V" condition of the '652 Patent, would be equally as capable of being applied to an eDP as the '652 Patent's devices. EX1001, 4:62-5:10, Table III; EX1003, 106.

(d) Claim 4

[4]: The dynamic random access memory of claim 3, wherein the first voltage is lower than 1.1V.

See [1.5] in §V.A.2(a). Takahashi discloses that the first voltage VPPL is **1.0 V**, which is lower than 1.1 V. EX1004, [0083]; EX1003, 107.

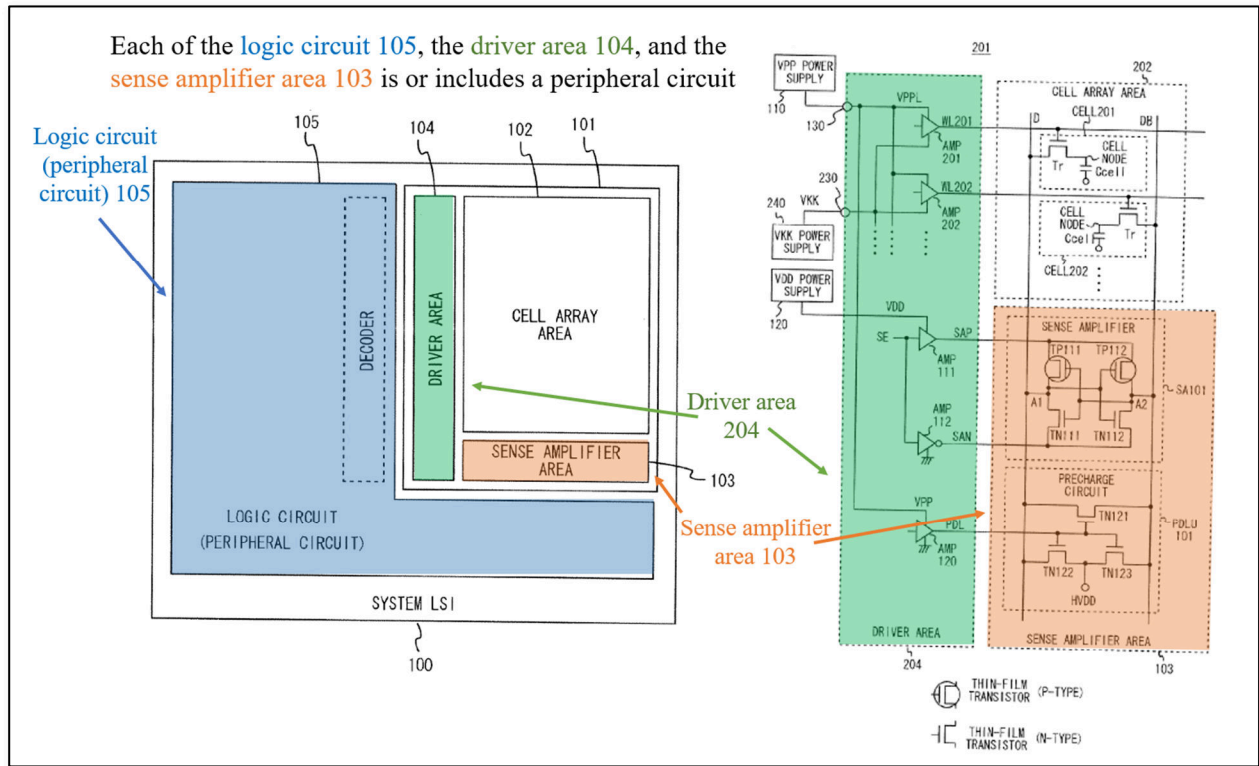
(e) Claim 5

[5.1]: The dynamic random access memory of claim 3, further comprising: a peripheral circuit comprised in the DRAM, wherein the peripheral circuit is electrically connected to the DRAM core cell,

Takahashi discloses a peripheral circuit electrically connected to the DRAM core cell. EX1003, 108. According to the applicant's proposed definition of "peripheral circuit" in the context of Takahashi, peripheral circuits electrically connected to the DRAM core cell include the "sense amplifier area 103" (e.g., "sense amplifier SA101"), the "driver area 204" (e.g., driver amplifier AMP111), and at least a portion of the "logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201." EX1004, [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7; EX1003, 109.

Note that, in Grounds 1A and 1C, the driver area 204 is applied as the input/output circuit, not as the peripheral circuit, pursuant to the discussion in §V.A.2(a). However, for the sake of efficiency and unified discussion, the driver

area 204 is discussed here as a peripheral circuit, together with the sense amplifier area 103 and the logic circuit 105. *See* Grounds 1B and 1D for mappings in which the driver area 204 is applied as a peripheral circuit. EX1003, 110.



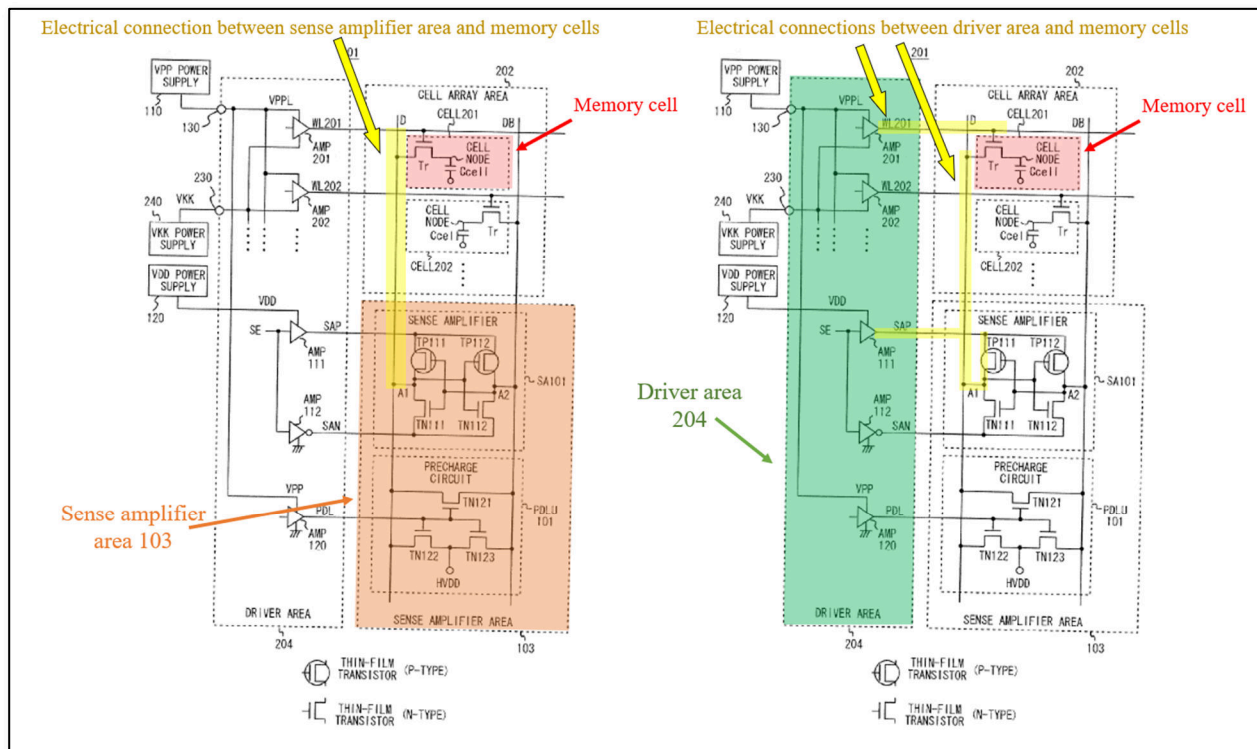
Left: Takahashi, FIG. 1; Right: Takahashi, FIG. 7

During prosecution of the parent '017 Patent, the applicant *explicitly* argued that drivers, sense amplifiers, and decoder are “peripheral circuits.” EX1003, 111. *See* EX1016, 72-82. Specifically, while attempting to distinguish Takahashi’s logic circuit 105 from the claimed peripheral circuit, the applicant argued that the “row decoder, sense amplifiers/drivers, and column decoder of the reference figure can be just referred to the peripheral circuit unit 104 of the present invention.” *Id.* Thus, by the applicant’s own argument, the circuitry of Takahashi’s driver area 204 (e.g.,

amplifier AMP111) and the sense amplifier area 103 (e.g., sense amplifier SA101) are each peripheral circuits. *See* EX1016, 70-74; EX1003, 112.

Consistent with applicant's argument, peripheral circuits electrically connected to Takahashi's DRAM core cell include the "sense amplifier area 103" (e.g., "sense amplifier SA101") and the "driver area 204" (e.g., driver amplifier AMP111); the peripheral circuits additionally include at least a portion of the "logic circuit 105," which includes "an address decoder," and which "serv[es] as a peripheral circuit of the semiconductor memory circuit 201." EX1004, [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7; *see also* EX1046, 15, 62; EX1016, 40, 42; EX1003, 113-119.

As shown in FIG. 7, these circuits are electrically connected to the DRAM core cell (memory cells). EX1003, 115, 120. For instance, the sense amplifier area 103 is electrically connected to the memory cells through, e.g., a bitline D, and the driver area 204 is electrically connected to the memory cells through, e.g., wordline WL201, sense amplifier control line SAP, sense amplifier SA101, and bitline D. EX1004, [0007], [0009], [0081], [0086], FIG. 7; EX1003, 115.



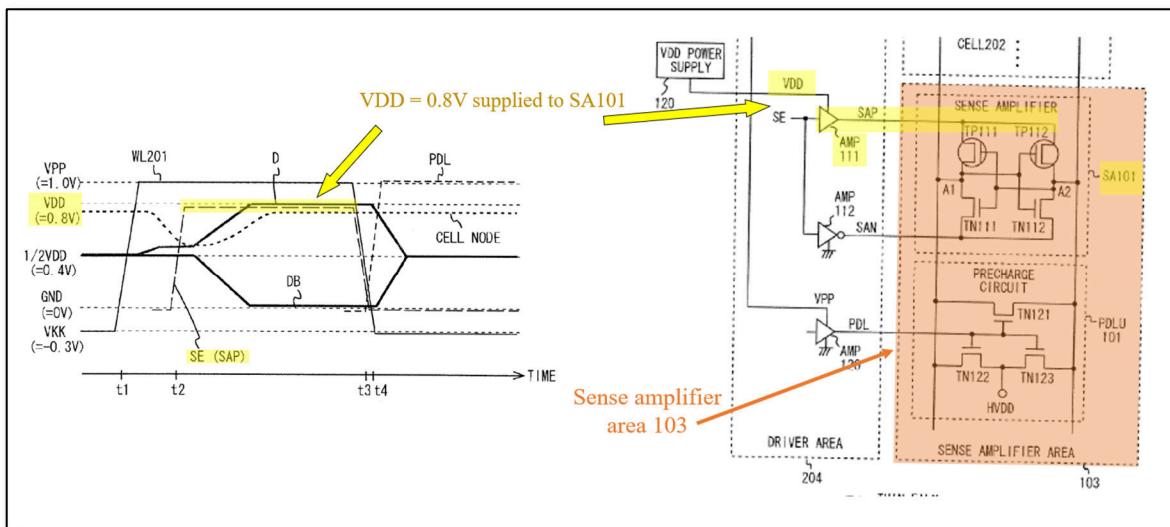
Takahashi, FIG. 7

Logic circuit 105 is also obviously electrically connected to the memory cells through its “address decoder,” and though connections for obtaining “data...to be processed in the logic circuit” from the memory cells. EX1004, [0044], [0047]; EX1003, 120-122.

[5.2]: and the peripheral circuit is supplied with a second voltage to make the peripheral circuit operate at the second voltage,

Takahashi’s peripheral circuits applied in this ground (the sense amplifier area 103 and the logic circuit 105) are each supplied with and operate at a **second voltage VDD**, which Takahashi describes as a “power supply voltage [] of the logic circuit.”

EX1004, [0045]; EX1003, 123. VDD is supplied to the sense amplifier area 103 when “the sense amplifier control signal SAP becomes equal to the power supply voltage VDD.” EX1004, [0086]; EX1003, 123-125. The supply of the second voltage VDD from VDD power supply 120 to the sense amplifier area 103 on the sense amplifier control line SAP is shown in Takahashi FIGS. 7 and 8. EX1003, 124.



Left: Takahashi, FIG. 8; Right: Takahashi, FIG. 7 (partial)

The logic circuit 105 operates at its “power supply voltage” VDD. EX1004, [0045]; EX1003, 126. The sense amplifier area 103 operates at VDD when VDD is supplied to transistors TP111 and TP112 of the sense amplifier SA101 through the sense amplifier control line SAP. EX1004, [0052], [0056], [0086]; EX1003, 125. For example, the sense amplifier area 103 operates at VDD when, based on receiving the sense amplifier control signal at VDD, “[t]he sense amplifier SA101 amplifies the small potential difference between the pair of bit lines D and DB to

the power supply voltage VDD and to the ground voltage GND.” EX1004, [0086]; EX1003, 125.

[5.3]: wherein the second voltage is lower than 1.1V.

Takahashi’s second voltage, VDD, is 0.8 V, which is lower than 1.1 V. EX1003, 127. *See, e.g.,* Takahashi [0078] (“VDD is 0.8V or lower”), [0084] (“the power supply voltage VDD is 0.8 V”), and FIG. 8, which shows “VDD (=0.8V).” EX1004, [0078], [0084], FIG. 8; EX1003, 127.

(f) Claim 6

[6]: The dynamic random access memory of claim 5, wherein the first voltage is different from the second voltage.

See [1.5] in §V.A.2(a), and [5.3] above. Takahashi’s first voltage VPPL is 1.0V, which is different from the 0.8V of Takahashi’s second voltage VDD. EX1004, [0078], [0083]-[0084], FIG. 8; EX1003, 128.

B. GROUND 1B: §103: Takahashi, Tsern, and Schuette render obvious claims 1-6

1. Tsern

Tsern discloses memories switchable between a “low-power mode” in which a “relatively low supply voltage Vi” is supplied to a core interface, and a “high-performance mode” in which a “relatively high supply voltage Vi” is provided. EX1005, [0018]; EX1003, 129-130.

As shown in implementations of Tsern depicted, e.g., in FIG. 3, Tsern describes a “memory system 300” including a “DRAM 310.” EX1005, [0034]; EX1003, 131. The DRAM 310 includes an “I/O [input/output] interface 340” that communicates with a memory controller. EX1005, [0037]; EX1003, 131. The I/O interface 340 “rel[ies] upon a supply voltage Vio” that can be constant or scaled between different performance modes. EX1005, [0043], FIG. 3; EX1003, 131. Vio can be “reduced in the low-power mode for increased power savings.” EX1005, [0070]; EX1003, 131.

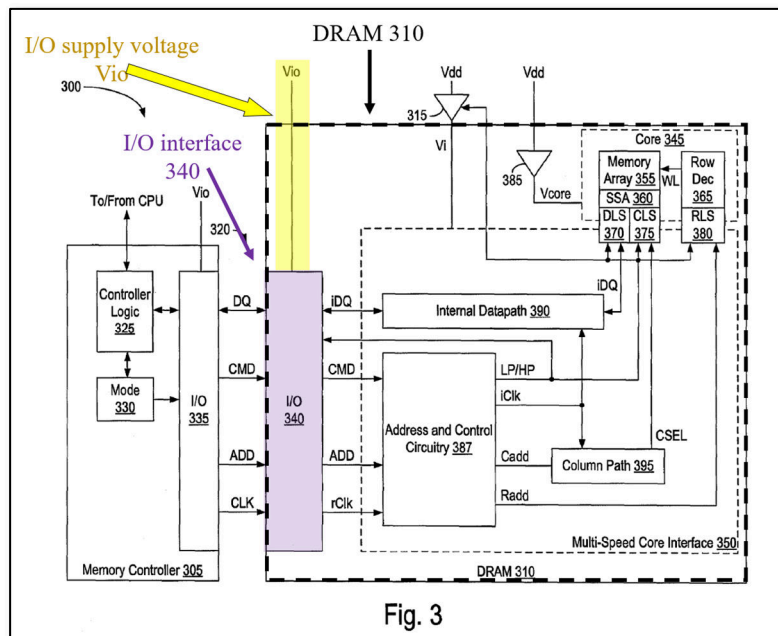


Fig. 3

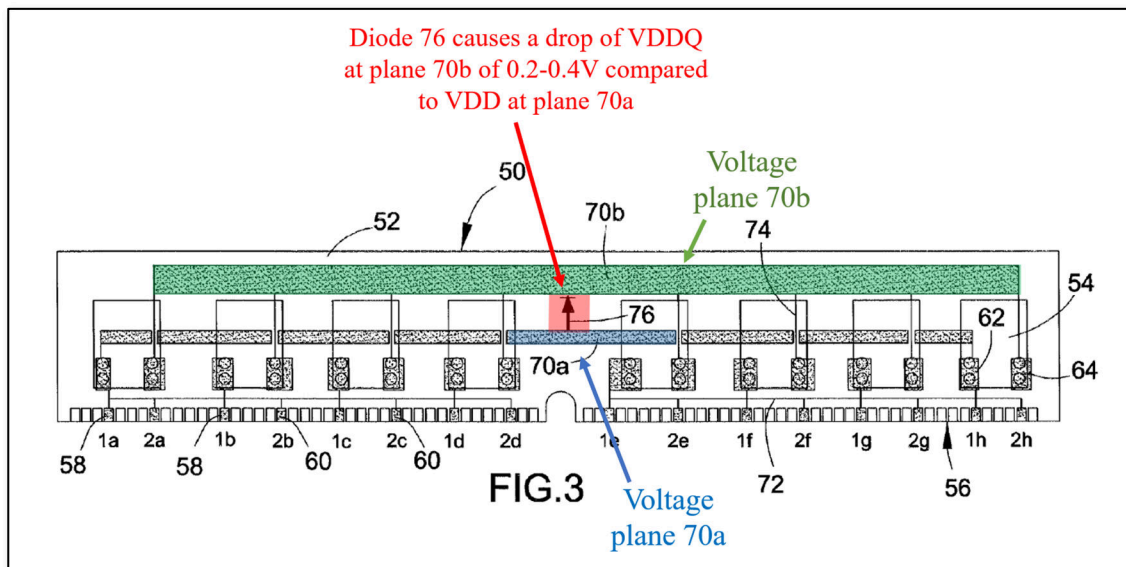
Tsern, FIG. 3

2. Schuette

Schuette describes “memory modules adapted...to generate different voltage for core supply (VDD) and input/output supply (VDDQ) inputs to memory

components.” EX1006, Abstract; EX1003, 132. Schuette describes advantages (such as reliability improvement and improved memory performance) associated with separate provision of VDD and VDDQ in DRAMs. EX1006, [0005]-[0006], [0014]; EX1003, 132.

Schuette describes implementations including a memory module in which “VDDQ input pins 64...are directly connected with lines 74 to the secondary voltage plane 70b, which is connected to the primary voltage plane 70a through a diode 76. With this approach, a reduction in VDDQ...is accomplished relative to the voltage level at the VDD and VDDQ input pins.” EX1006, [0025]; EX1003, 133. Specifically, the diode provides “a consistent voltage drop across all levels of load and power draw” for the I/O supply voltage VDDQ in comparison to the core supply voltage VDD. EX1006, [0021], [0029]; EX1003, 133. “[V]oltage differentials of about 0.2 to about 0.4 volts can be achieved.” EX1006, [0029]; EX1003, 133.



Schuette, FIG. 3

3. Combination of Takahashi, Tsern, and Schuette

It would have been obvious to a POSITA to advantageously modify Takahashi's memory device, to obtain a DRAM having an I/O circuit supplied with a voltage V_{io} as described by Tsern. EX1003, 134. It would also have been obvious to a POSITA to reduce V_{io} by 0.2-0.4 V compared to the core voltage, as taught by Schuette. EX1003, 134.

(a) Combination with Tsern

As discussed in §V.A.2(a), a POSITA would have understood that Takahashi's driver area 204 is an "input/output circuit," because it serves an input/output function in the context of embedded DRAM. EX1003, 135.

As discussed in §V.A.2(e) (claim 5), the driver area 204 can alternatively be considered peripheral circuitry, consistent with applicant's arguments. EX1016, 72-73; EX1003, 135.

In this alternative mapping in which Takahashi's driver area 204 is not interpreted as an input/output circuit, it would have been obvious to incorporate an input/output circuit into Takahashi's semiconductor memory circuit 201, in two distinct ways and for at least two distinct reasons. EX1003, 136-137.

(i) **Obvious to include input/output circuit for data readout from Takahashi's cell array 202 to logic circuit 105**

Takahashi relates to an "embedded" DRAM in which the memory and processors are integrated on the same chip. EX1003, 138. Correspondingly, Takahashi discloses that data stored in the cell array 202 is read out on the bit lines and utilized by the logic circuit 105. EX1004, [0060]; EX1003, 138-139. For example, Takahashi describes that the "amplifie[d] potential difference between the pair of bit lines D and DB is read out as high-level readout data...by an external circuit and is used for data processing and the like of the logic circuit 105." EX1004, [0086].

Takahashi does not, however, describe details of the "external circuit" that reads out the data, nor describe how data on the bit lines D and DB is transferred to "data processing" elements of the logic circuit 105. EX1003, 140-141.

In view of Tsern's disclosure, a POSITA would have been motivated and found it obvious to provide Takahashi's semiconductor memory circuit 201 with an input/output circuit, powered by a supply voltage V_{io} , as the "external circuit" that reads out data from Takahashi's bitlines and facilitates communication with the logic circuit 105, performing a data output function with respect to Takahashi's memory. EX1003, 142. This is the function of Tsern's I/O interface 340, which receives "data iDQ" and transfers it out of the DRAM 310 for use. EX1003, 142. For example, Tsern describes that "[i]nternal datapath 390 then conveys the read data to I/O interface 340, and hence to controller 305 [distinct from the DRAM 310]." EX1005, [0042]; EX1003, 142. Consistent with this function, it would have been obvious to include an I/O interface (or circuit) in Takahashi, connected to Takahashi's bitlines, such that data read from Takahashi's memory cells would be "convey[ed]...to [the] I/O interface [], and hence to" the logic circuit 105 to provide output of stored data to the logic circuit 105. EX1005, [0042]; EX1003, 142-143. The I/O circuit would also obviously be configured to provide data input for storage in Takahashi's memory cells, consistent with the well-understood purpose and operation of bitlines and memory cells. EX1003, 142.

Dr. Liu explains that "the I/O circuit incorporated into Takahashi's memory device as the 'external circuit' would obviously include, for example, input buffers, output buffers, level-shifters, and/or other circuit elements that facilitate useful

transfer of data from their form in Takahashi (voltages on the pair of bitlines D and DB) to a form useful for circuit elements of the logic circuit 105.” EX1004, [0086]; EX1003, 144. It would have been within the skill of a POSITA to, with a reasonable expectation of success, select suitable circuit elements to perform this function, motivated by Tsern’s disclosure of an I/O interface and guided by Tsern’s disclosure that the I/O circuit should be powered by a voltage V_{io} .⁸ EX1003, 145. For example, a POSITA would have been guided by Takahashi description that the “external circuit” “read[s] out” “the amplifie[d] potential difference between the pair of bit lines D and DB,” and would correspondingly have had a reasonable expectation of success based on configuring the I/O circuit to perform this function. EX1004, [0086]; EX1003, 145.

Further, a POSITA would have known that it was conventional to include I/O circuitry even in embedded DRAMs (like Takahashi’s), to provide for data input and

⁸ Notably, the ’652 Patent provides no structure for the input/output circuit more specific than the “unit” of the FIGURE, and it would have been within the skill of a POSITA to select a structure for the I/O circuit that, per Tsern’s teachings, would have been electrically connected to Takahashi’s peripheral circuits and core memory cells. EX1003, 142.

output between an embedded DRAM and processors. EX1032; EX1033; EX1034, EX1035; EX1003, 146-150. Whether data was being transferred to/from a DRAM to another die or to a processor on the same die, I/O circuitry of some form was conventional and necessary to facilitate the transfer. EX1003, 151. Providing Takahashi's DRAM with an I/O circuit would have filled this vital function and been obvious to a POSITA. EX1003, 151.

Tsern motivates not only the inclusion of an I/O circuit as the "external circuit" but also the use of a supply voltage Vio to power the I/O circuit. EX1003, 152. Tsern describes, for example, that the I/O interface "can use [a] scaled supply voltage" Vio, such that Vio "can be reduced in the low-power mode for increased power savings." EX1005, [0043], [0070]; EX1003, 152. It would have been obvious to provide a supply voltage Vio to the I/O circuit to achieve these power savings. Further, even in the absence of a low-power mode, a POSITA would have recognized the necessity of powering the I/O circuit to allow the circuit to operate. EX1003, 152.

(ii) **Obvious to add Tsern's input/output interface to Takahashi to facilitate off-chip data transfer**

As a second obvious modification of Takahashi (distinct from the first modification discussed immediately above), it would have been obvious to provide Takahashi's semiconductor memory circuit 201 with Tsern's I/O interface 340, or a

substantially similar circuit, to allow Takahashi's semiconductor memory circuit 201 to receive data from, and transfer data to, off-chip elements. EX1003, 153.

A POSITA would have recognized several clear benefits from this modification. EX1003, 154. First, the addition of Tsern's I/O interface 340, or a substantially similar circuit, would have greatly expanded the versatility of Takahashi's memory, allowing it to not only exchange data with on-chip processing elements of the logic circuit 105, but also to exchange data with external devices, thereby improving Takahashi's functionality. EX1003, 154. For example, Tsern describes that the I/O interface 340 exchanges data with a memory controller 305, and that the memory controller 305 exchanges the data with a central processing unit, a configuration Tsern describes as "conventional." EX1005, [0034]-[0035], FIG. 5; EX1003, 154.

Further, the inclusion of Tsern's I/O interface 340, or a substantially similar circuit, would have made Takahashi's DRAM compatible with DRAM standards, which assume the presence of I/O circuitry for off-chip communication, thereby improving interoperability and utility. EX1003, 155; EX1013, 12-13, 83.

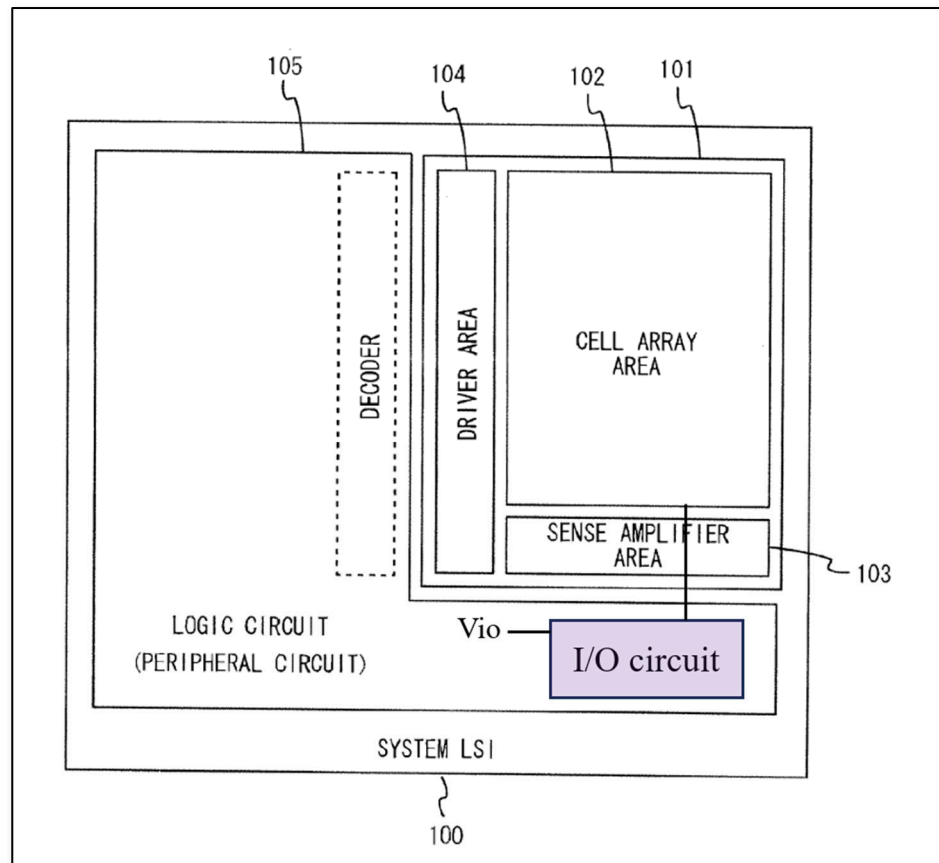
A POSITA would have had a reasonable expectation of success in making this modification. EX1003, 156. Takahashi's and Tsern's devices are DRAMs with similar architectures. EX1004, [0044], [0048], [0051], [0079], FIGS. 1, 7; EX1005, [0020]-[0021], [0037], FIG. 3; EX1003, 156. And both Takahashi and Tsern employ

multiple different voltages that are provided to different components. EX1004, [0084], FIG. 7; EX1005, [0026], [0043], FIG. 3; EX1003, 156.

Thus, in making this modification, a POSITA would have been modifying one device to have the configuration of a substantially similar device, in an entirely conventional way. EX1003, 157. Dr. Liu explains that “I/O circuitry was standard in memory devices to permit reception and transmission of signals representing data.” EX1003, 157; EX1005, [0035]. Thus, incorporating an I/O interface into Takahashi would have involved nothing more than the combination of known elements (DRAM memory and peripheral circuitry, and DRAM I/O circuitry) to yield predictable results, or the application of a known technique (I/O circuitry) to a piece of prior art (Takahashi’s DRAM) ready for the improvement. *KSR* at 416-417. EX1003, 157-159.

Takahashi’s system LSI 100, modified to include an I/O circuit, is shown below. EX1003, 160. Although the I/O circuit is illustrated as part of the logic circuit 105, the I/O circuit can equally be included in the semiconductor memory circuit 201 (represented as 101 in the drawing below). EX1003, 160. In the case where Takahashi is modified as discussed in §V.B.3(a)(i), the I/O circuit is the “external circuit” of Takahashi, configured for communication between Takahashi’s embedded DRAM cell array and on-chip processing elements of the logic circuit

105. EX1003, 160. In the case where Takahashi is modified as discussed in §V.B.3(a)(ii), the I/O circuit is, or is substantially similar to, Tsern's I/O interface 340 and is configured for communication between Takahashi's DRAM and off-chip elements. EX1003, 160. In either case, it would have been obvious to provide the I/O circuit with a power supply voltage V_{io} for the reasons discussed in §V.B.3(a)(i). EX1003, 160.



Takahashi-Tsern device

(b) Combination with Schuette

While Tsern discloses provision of a “supply voltage Vio” to the I/O interface and describes that Vio is preferably “reduced...for increased power savings,” Tsern does not provide a specific value for Vio. EX1005, [0043], [0070]; EX1003, 161. To determine an effective value, achieve Tsern’s power savings, and maintain effective device performance, a POSITA would have been motivated and would have found it obvious to follow Schuette’s teachings and configure Vio to be “about 0.2 to about 0.4 volts” lower than the core voltage. EX1004, FIGS. 7-8; EX1006, [0029]; EX1003, 161.

As discussed in §V.A.2(a) for [1.2], the “core” refers to, or at least encompasses, the cell array of a memory. EX1003, 162. In the case of Takahashi, the cell array area receives both VPPL and VDD. EX1003, 162. Accordingly, either VPPL or VDD would have been interpreted as a core voltage compared to which the I/O voltage is dropped. EX1003, 162.

For example, a POSITA would have found it obvious to use a “diode” or a “linear regulator circuit of a known type in the art” to lower Takahashi’s VPPL (=1.0V) or VDD (=0.8V) by 0.2 to 0.4 V as described by Schuette, to obtain a Vio in a range from 0.6 to 0.8 V in comparison to VPPL, or in a range from 0.4 to 0.6 in comparison to VDD. EX1004, [0084]; EX1006, [0029]; EX1003, 163.

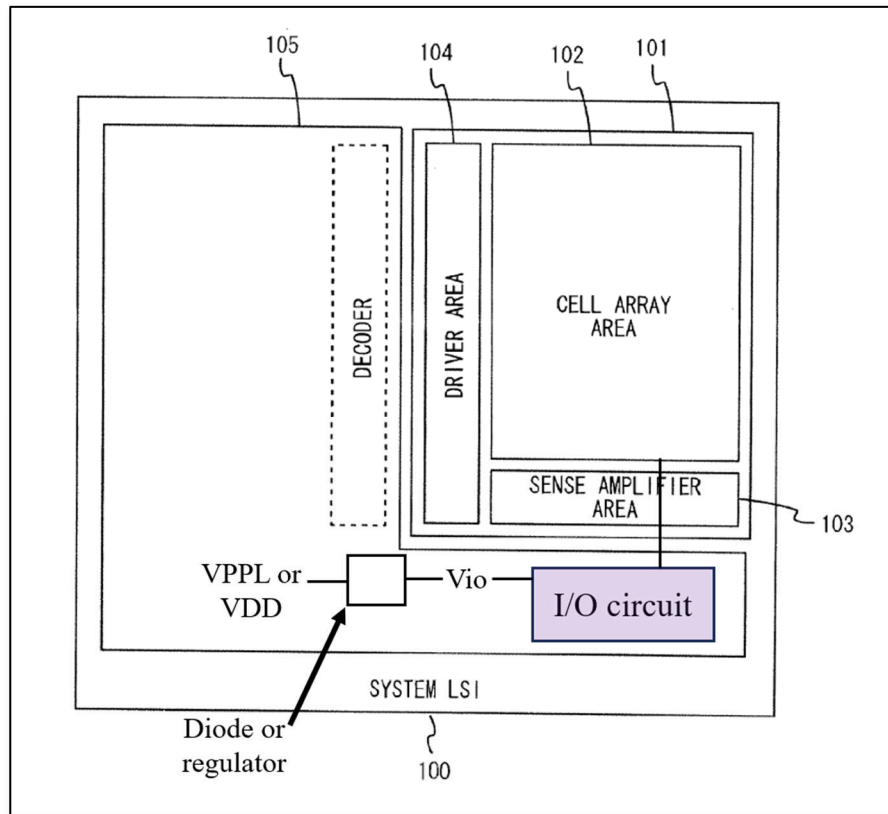
Schuette describes that this “more precise” approach “maintain[s] a consistent voltage drop across all levels of load and power draw,” such that a POSITA would have had a reasonable expectation of success in obtaining Vio from VPPL or VDD. EX1006, [0029]; EX1003, 164. Indeed, this would have involved nothing more than the combination of known elements to yield predictable results, or the application of a known technique to a piece of prior art ready for the improvement. *KSR* at 416-417. EX1003, 164. Moreover, the use of a regulator circuit to generate Vio would have been in full agreement with Tsern’s existing disclosure, which describes “a collection of regulators that develops these and other necessary or desired core voltages from an externally supplied voltage Vdd.” EX1005, [0032]; EX1003, 164.

Additionally, this modification would have been consistent with Takahashi’s existing design, which already incorporates three power supplies providing three distinct voltages to different circuitry. EX1004, [0084]; EX1003, 165. The use of another voltage Vio to power the I/O circuit, as taught by Tsern, would have constituted a minor change, especially since Schuette provides a simple and reliable circuit configuration for obtaining Vio from an existing core voltage. EX1003, 165.

Obviousness is further supported through comparison of Vio to Takahashi’s VDD. EX1003, 166. Vio in a range from 0.6 to 0.8V (resulting from Schuette’s disclosed voltage drop in comparison to Takahashi’s VPPL=1.0V) would have resulted in a Vio matching, or similar to, Takashi’s VDD=0.8, which powers

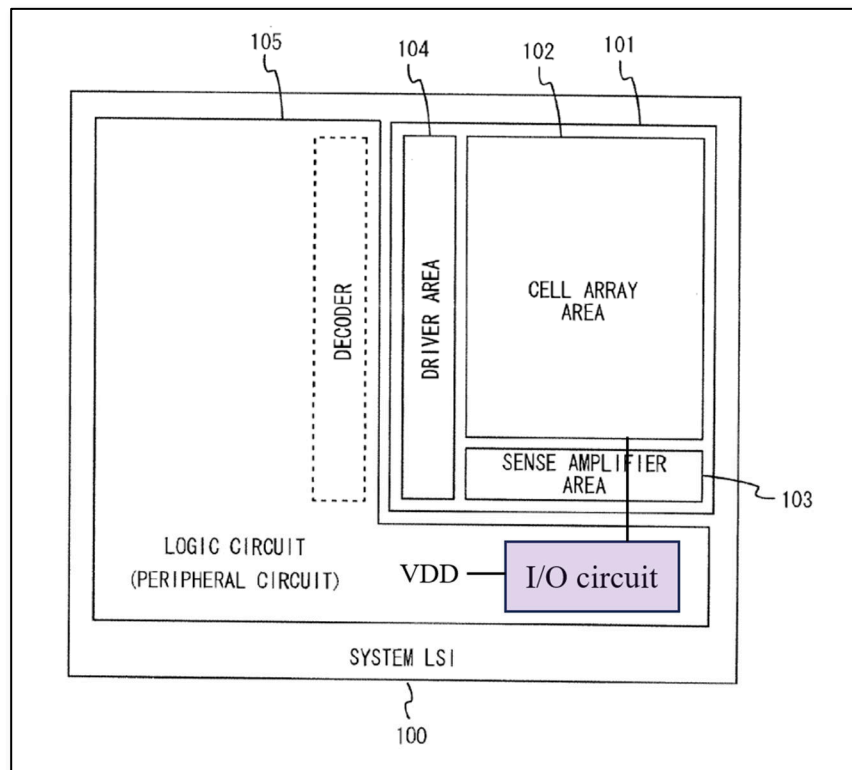
Takahashi's logic circuit 105, driver area 204, and sense amplifier area 103. EX1004, [0045], FIG. 7; EX1003, 166. Thus, the modification of Takahashi based on Tsern and Schuette would have entailed providing an I/O circuit with a voltage V_{io} matching, or close to, the voltage *already disclosed as being provided* to components of Takahashi. EX1003, 166. Indeed, one especially obvious choice for V_{io} would have been $V_{io}=VDD=0.8V$, in which case VDD could be directly applied as the power supply voltage for the I/O circuit. EX1003, 166.

As a result of this obvious modification of Takahashi, a POSITA would have arrived at the Takahashi-Tsern-Schuette device shown below, in which VPPL or VDD is lowered by a diode or regulator and supplied to the I/O circuit as V_{io} . EX1003, 167.



Takahashi-Tsern-Schuette device

In the specific case where VDD is used as Vio (in accordance with Schuette's disclosure of a suitable voltage drop for an I/O circuit voltage in comparison to a core voltage), the Takahashi-Tsern-Schuette device can be represented as shown below. EX1003, 168.



Takahashi-Tsern-Schuette device

4. Analysis of claims

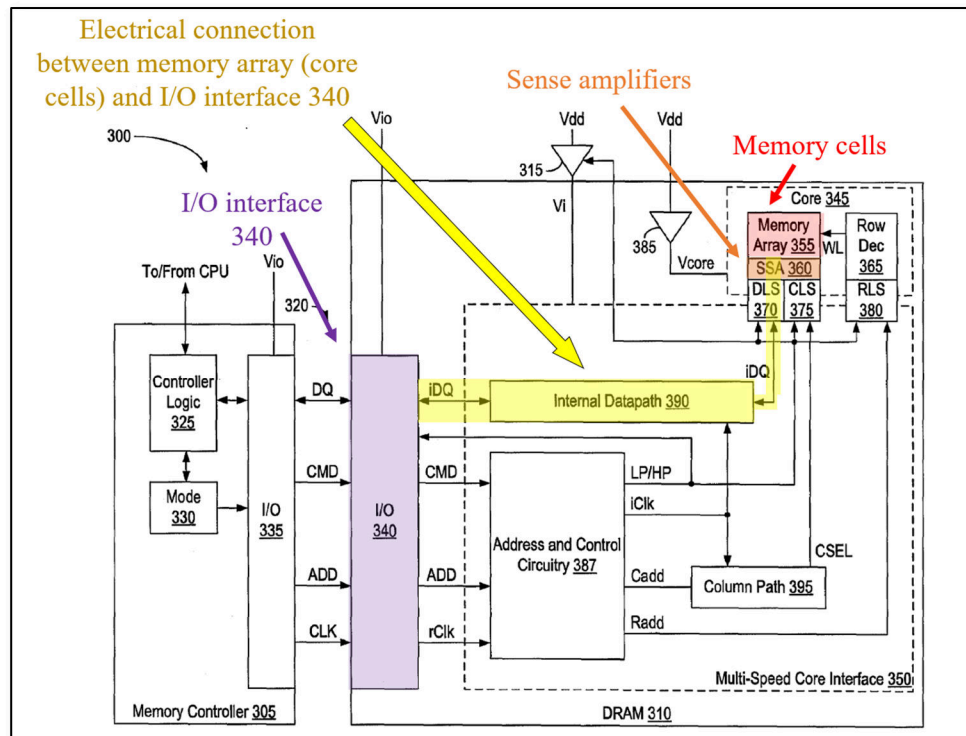
(a) Claim 1

[1.1]-[1.5]: See [1.1]-[1.5] in §V.A.2(a) (Ground 1A).

[1.6]: *an input/output circuit comprised in the DRAM, wherein the input/output circuit is electrically connected to the DRAM core cell,*

As discussed in §V.B.3, the Takahashi-Tsern-Schuette device includes an input/output circuit, which can be configured to perform an input/output function for data exchange with the processing elements of the logic circuit 105 (§V.B.3(a)(i)) or for data exchange with an off-chip device (§V.B.3(a)(ii)). EX1003, 170.

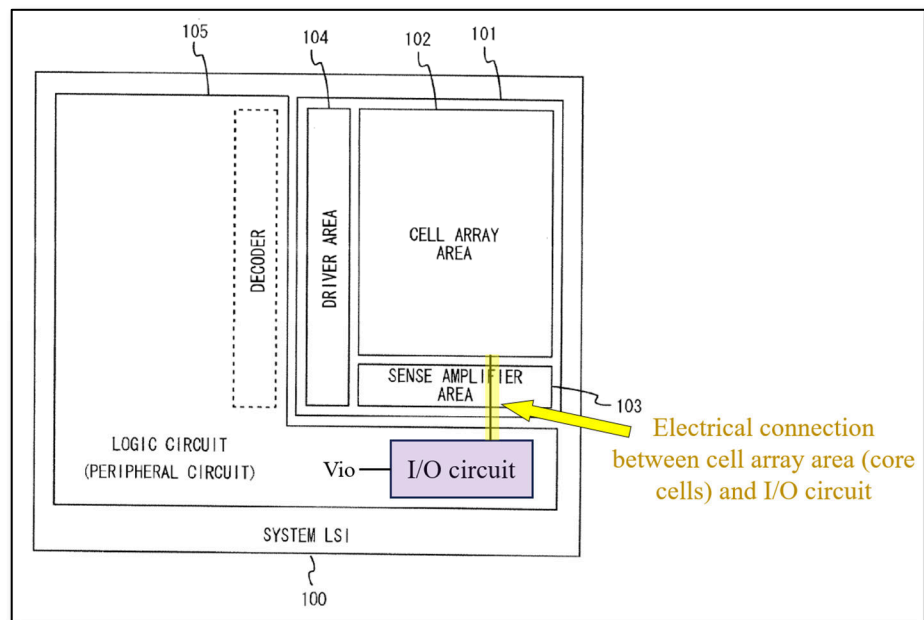
As a POSITA would have understood, the I/O circuit is electrically connected to the DRAM core cell (memory cell of the cell array area 202) so as to provide for, as Tsern describes, “the flow of signals between I/O interface 340 and memory core 345.” EX1005, [0037]; EX1003, 170. For example, Tsern describes an “[i]nternal datapath 390 [that] conveys the read data [stored in memory cells] to I/O interface 340.” EX1005, [0042]; EX1003, 170.



Tsern, FIG. 3

This internal datapath, which extends from the memory array 355, through sense amplifiers (SSA) 360, and to the I/O interface, is an electrical connection between the memory cells and the I/O interface. EX1003, 171.

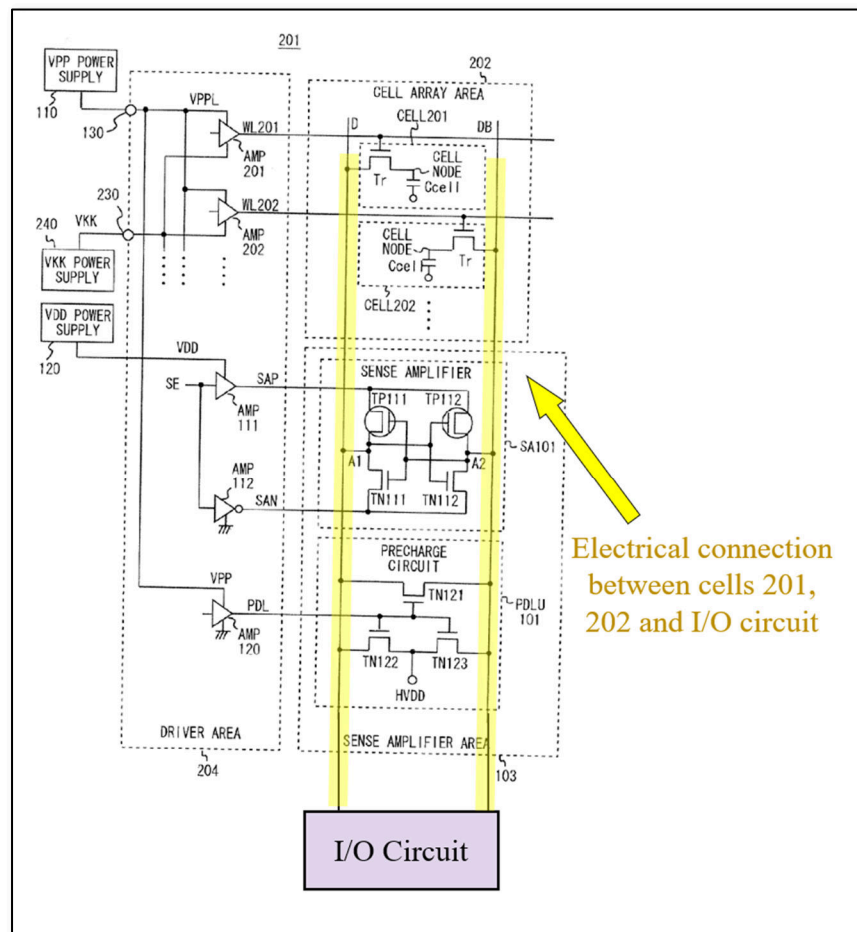
For the Takahashi-Tsern-Schuette device, it would have been obvious for a POSITA to provide a similar electrical connection between the I/O circuit and the cell array area 202 through the sense amplifier area 103, as shown below, to permit data readout/writing. EX1003, 172. This configuration would have been consistent with the well-understood, standard configuration of DRAM devices, which near-universally included electrical connections from memory cells, through sense amplifiers, and to I/O circuitry to permit data readout/writing. EX1003, 172.



Takahashi-Tsern-Schuette device

For example, Takahashi describes that, in a data read process, “the amplifie[d] potential difference between the pair of bit lines D and DB is read out as high-level readout data of the semiconductor memory circuit 201 by an external circuit, and is used for data processing and the like of the logic circuit 105.” EX1004, [0086];

EX1003, 173. That is, data is output on the bitlines, and the “external circuit” reads out the data. EX1003, 173. Thus, one obvious configuration of the I/O circuit would have been to electrically connect the I/O circuit to the memory cells through the bitlines D and DB, as shown below:

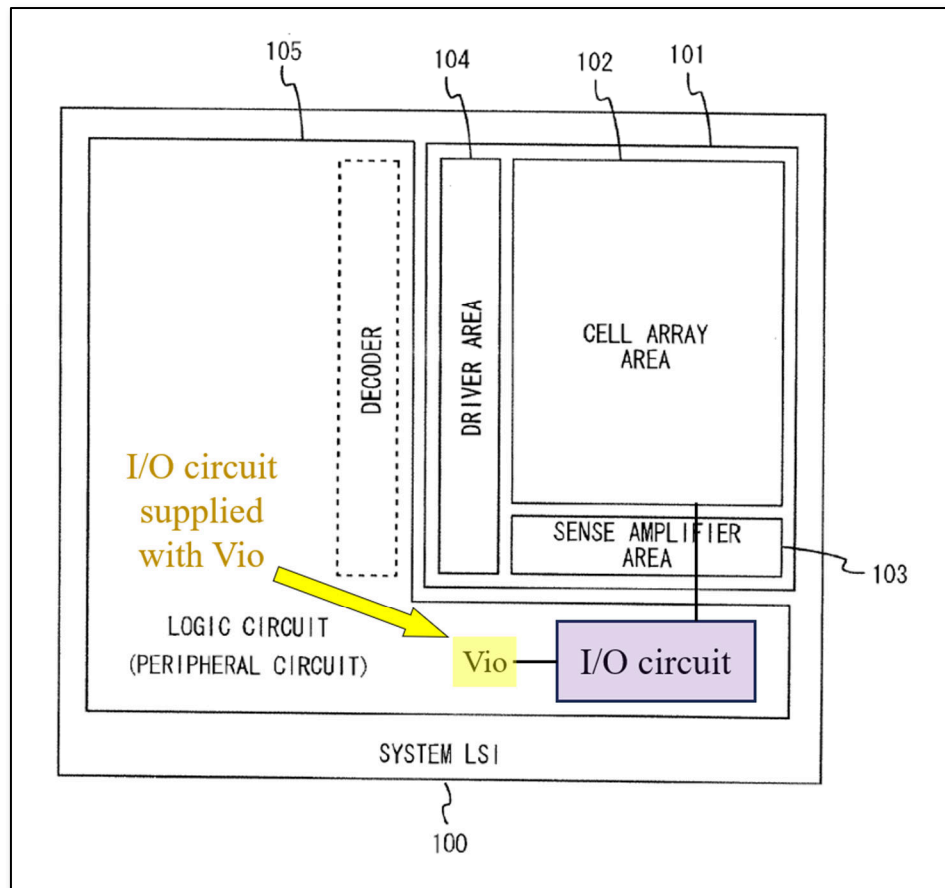


Takahashi-Tsern-Schuette device

Accordingly, the Takahashi-Tsern-Schuette device, which is a DRAM device, includes an input/output circuit (I/O circuit) that is electrically connected to the peripheral circuit and to the DRAM core cell (memory cell of cell array area 202). EX1003, 174-175.

[1.7]: and the input/output circuit is supplied with a third voltage to make the input/output circuit operate at the third voltage,

As discussed in §V.B.3, the input/output circuit of the Takahashi-Tsern-Schuette device is supplied with, and operates at, **a third voltage Vio**. EX1005, [0043], [0070]; EX1003, 176. For example, Tsern describes that the I/O interface 340 “rel[ies] upon a supply voltage Vio.” EX1005, [0043].



Takahashi-Tsern-Schuette device

[1.8]: wherein the third voltage is lower than 1.1V, and

As discussed in §V.B.3, Vio has a drop of “about 0.2 to about 0.4 volts” compared to the core voltage, which is VPPL or VDD in the Takahashi-Tsern-Schuette device. EX1006, [0029]; EX1003, 177. VPPL is 1.0V, and VDD is 0.8V. EX1004, [0084]; EX1003, 177. Therefore, Vio is in a range from about 0.6 V to about 0.8 V, or from about 0.4 V to 0.6 V, lower than 1.1 V. EX1003, 177.

[1.9]: wherein the DRAM core cell and the input/output circuit are formed on a single chip,

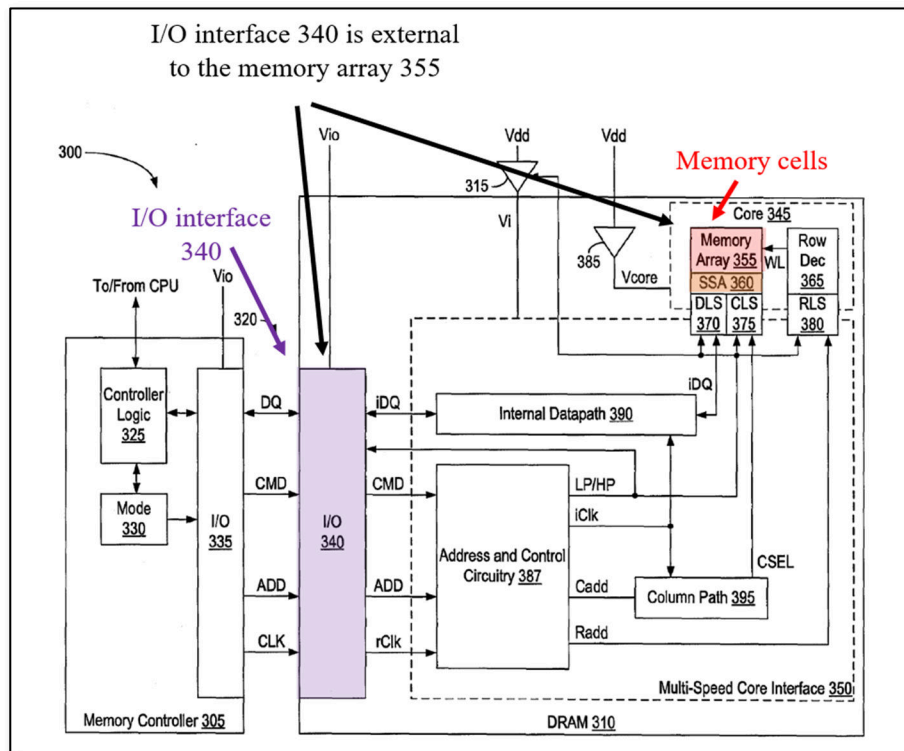
See [1.9] at §V.A.2(a). In Takahashi’s device, a “semiconductor memory circuit...and a logic circuit...are integrated into one chip.” EX1004, [0018]; EX1003, 178. When an I/O circuit is incorporated into the Takahashi-Tsern-Schuette device, the I/O circuit is formed on a single chip with the DRAM core cell (memory cell of cell array area 202), because these elements are on a common “LSI chip” and are “integrated into one chip.” EX1004, [0018], [0043], FIG. 1; EX1003, 178.

Further, it would have been obvious to form the I/O circuit on a single chip with the DRAM core cell, to facilitate its function, to achieve the well-known benefits of integration on a single chip, and because this configuration is described for Tsern’s I/O interface. EX1003, 179-180; EX1005, [0034]-[0035], FIG. 3.

[1.10]: the input/output circuit is external to the DRAM core cell, and

A POSITA would have found it obvious to have the I/O circuit of the Takahashi-Tsern-Schuette device be external to the DRAM core cell (memory cell

of cell array area 202). EX1003, 181. For example, this matches the configuration described by Tsern, in which the I/O interface 340 is external to the memory array 355, as shown below. EX1005, FIG. 3; EX1003, 181.

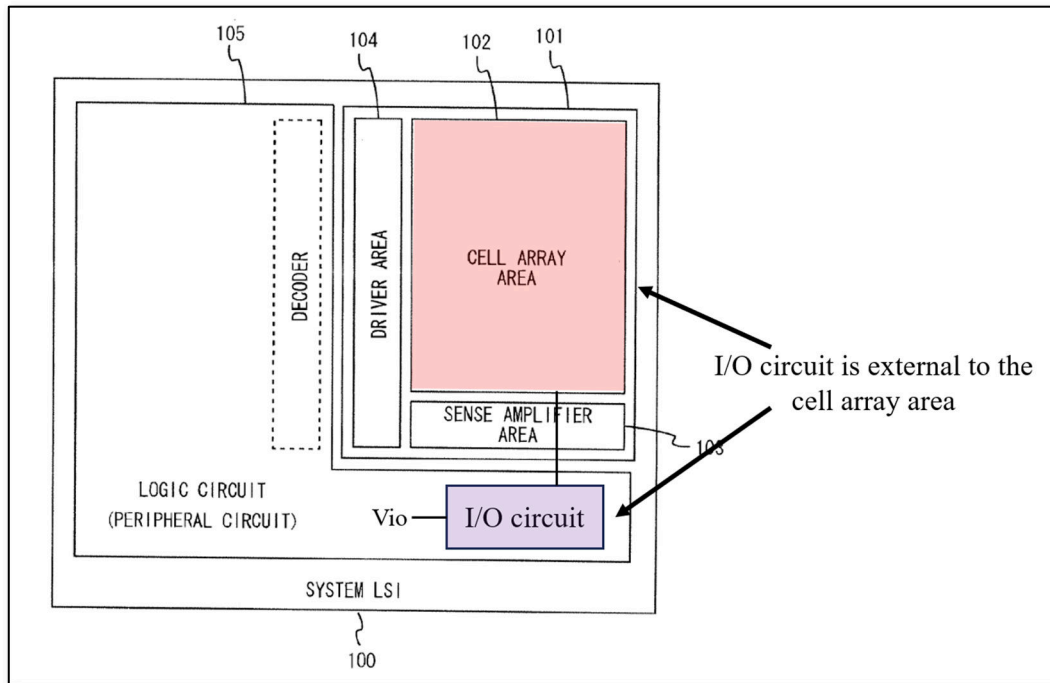


Tsern, FIG. 3

This configuration also matches the configuration of the “external circuit” that is the I/O circuit of the Takahashi-Tsern-Schuetz device: the “external circuit” is described separately from the cell array area 202 and would have been understood by a POSITA as external to the cell array area 202. EX1004, [0086]; EX1003, 182.

Moreover, as described by Dr. Liu, a POSITA would have understood that I/O circuitry of a DRAM is essentially always external to the core memory cells that store data. EX1003, 183.

It would have been obvious to apply this essentially universal configuration in the Takahashi-Tsern-Schuette device, as shown below. EX1003, 183.



Takahashi-Tsern-Schuette device

[1.11]: the first voltage is different from the third voltage.

See [1.5] in §V.A.2(a) and [1.8] in this section. The first voltage is VPPL=1.0 V. EX1004, [0084], FIGS. 7-8; EX1003, 184. The third voltage is Vio, which is reduced compared to the core voltage (VPPL or VDD) by “about 0.2 to about 0.4 volts.” EX1006, [0029]; EX1003, 184. Thus, the third voltage Vio is in a range from about 0.6 to about 0.8 V, or from about 0.4 to about 0.6 V, different from the first voltage VPPL=1.0V; EX1003, 184.

(b) Claim 2

Claim 2's elements are found identically in claim 1, except for [2.11] discussed below. For [2.1]-[2.10], *see* [1.1]-[1.10] in §V.B.4(a), respectively. EX1003, 185.

[2.11]: the first voltage is greater than the third voltage.

See [1.5] in §V.A.2(a) and [1.8] in this section. The first voltage is VPPL=1.0 V. EX1004, [0084], FIGS. 7-8; EX1003, 186. The third voltage is Vio, which is reduced compared to the core voltage (VPPL or VDD) by “about 0.2 to about 0.4 volts.” EX1006, [0029]; EX1003, 186. Thus, the third voltage Vio is in a range from about 0.6 to about 0.8 V, or from about 0.4 to about 0.6 V, less than the first voltage VPPL=1.0V; EX1003, 186.

(c) Claim 3

[3.1]-[3.7]: See [1.1]-[1.4] and [1.6]-[1.8] in §V.B.4(a), respectively.

[3.8]: See [2.11] in §V.B.4(b).

[3.9]: the DRAM is capable to be applied to an embedded display port (eDP).

For the reasons discussed in §V.A.2(c) for Ground 1A, a POSITA would have understood that the Takahashi-Tsern-Schuetz device, operating with the first voltage VPPL and the third voltage Vio, is capable of being applied to an eDP. EX1003, 189. That is, the Takahashi-Tsern-Schuetz device is a working,

conventional DRAM that is capable of satisfying the requirements of the eDP 1.3 standard, which do not include any voltage or power requirements. EX1014; EX1003, 189. Further, based on the obvious inclusion of an I/O circuit as discussed in §V.B.3(a)(ii), the Takahashi-Tsern-Schuette device is configured to receive data from and transmit data to off-chip devices, enhancing its applicability as a frame buffer in an eDP configuration. EX1003, 190.

To the extent the '652 Patent erroneously links “capable to be applied to an embedded display port (eDP)” to low-voltage operation, then the Takahashi-Tsern-Schuette device, which has first (VPPL) and third (Vio) voltages that satisfy the “< 1.1 V” condition of the '652 Patent, would be equally as capable of being applied to an eDP as the '652 Patent's devices. EX1001, 4:62-5:10, Table III; EX1003, 191.

(d) Claim 4

See [1.5] in §V.A.2(a). Takahashi discloses that the first voltage VPPL is **1.0 V**, which is lower than 1.1 V. EX1004, [0083]; EX1003, 192.

(e) Claim 5

[5.1]:

See [5.1] in §V.A.2(e). Peripheral circuits of the Takahashi-Tsern-Schuette device include the “sense amplifier area 103” (e.g., “sense amplifier SA101”), the “driver area 204” (e.g., driver amplifier AMP111), and/or at least a portion of the “logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit

201” (e.g., the “address decoder of the semiconductor memory circuit.”). EX1004, [0044], [0054], [0078]-[0079], [0086], [0088], FIGS. 1, 7; EX1003, 193. These circuits are electrically connected to the DRAM core cell (memory cells), as discussed in §V.A.2(e).

[5.2]:

For the reasons discussed for [1.7] in §V.A.2(a) and [5.2] in §V.A.2(e), Takahashi’s peripheral circuits noted above (the sense amplifier area 103, the driver area 204, and the logic circuit 105) are each supplied with, and operate at, **a second voltage VDD**. EX1003, 194.

[5.3]:

See [5.3] in §V.A.2(e). Takahashi’s second voltage, VDD, is 0.8 V<1.1 V. EX1004, [0078], [0084], FIG. 8; EX1003, 195.

(f) Claim 6

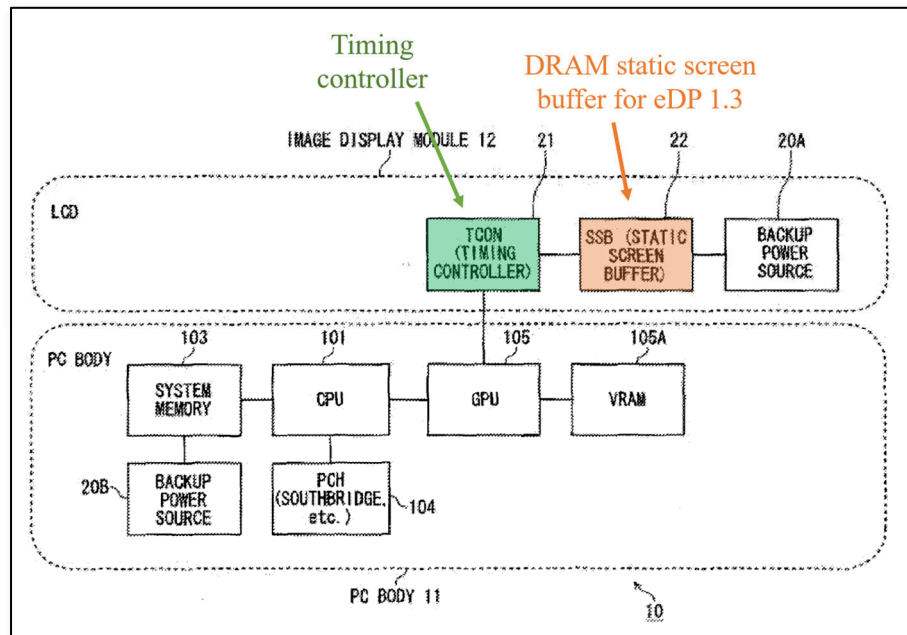
See [6] in §V.A.2(f).

C. Ground 1C: Takahashi and Endo render obvious claims 3-6

1. Endo

Endo is directed to electronic devices with displays. EX1007, [0020]-[0022], FIG. 1; EX1003, 197. Implementations described by Endo include FIG. 3, which illustrates an electronic apparatus 10 that includes an image display module 12. EX1007, [0023], FIG. 3; EX1003, 198. The image display module 12 includes a

timing controller (TCON) and a static screen buffer (SSB). EX1007, [0029], FIG. 3; EX1003, 198. Endo describes that the “static screen buffer (SSB) 22 is a memory defined as Embedded DisplayPort (eDP) version 1.3” and that the “SSB 22 is constituted by, for example, dynamic random access memory (DRAMs).” EX1007, [0034]-[0035]; EX1003, 198. This “static screen buffer” is the same as the “remote frame buffer” of the eDP 1.3 standard and the “frame buffer” of the ’652 patent. EX1003, 198.



Endo, FIG. 3

2. Obviousness of claims 3-6

As discussed in §V.A.2, Takahashi anticipates and renders obvious claims 3-6. Those claims are further obvious over Takahashi in view of Endo’s teachings, which further demonstrate that it would have been obvious for Takahashi’s DRAM

to be “*capable to be applied to an embedded display port (eDP)*” (claim 3). EX1003, 199.

Specifically, Endo explicitly teaches the use of “DRAMs” as the frame buffer of eDP 1.3 devices. EX1007, [0034]-[0035]; EX1003, 200. Endo also describes how an apparatus in which the frame buffer is a DRAM can be specially configured to facilitate the DRAM: a backup power source 20A can maintain storage of data in the volatile DRAM, even when the device is switched to a standby power state. EX1007, [0035], [0038], FIG. 3; EX1003, 200. This would have reinforced a POSITA’s expectation of success in using the Takahashi’s DRAM as the frame buffer. EX1003, 200.

In view of Endo, a POSITA would have further found it obvious that Takahashi’s DRAM is capable of being applied to an eDP, would have been further motivated to apply that DRAM to an eDP to obtain the benefits of eDP operation, and would have reasonably expected success in doing so. EX1003, 201. Indeed, Endo discloses the use of a DRAM for that purpose, without disclosing any specific requirements or characteristics of the DRAM. EX1007, [0034]-[0035]; EX1003, 201. Takahashi’s device 200 is a DRAM. EX1004, [0078]; EX1003, 201. Thus, based on Endo, it would further have been obvious to a POSITA to apply a DRAM, such as the Takahashi’s device 200, to an eDP, e.g., as the frame buffer. EX1003, 201.

D. Ground 1D: Takahashi, Tsern, Schuette, and Endo render obvious claims 3-6

1. Claims 3-6

Endo is applied here as discussed for Ground 1C in §V.C. As discussed in §V.B, Takahashi, Tsern, and Schuette render obvious claims 3-6. In view of Endo's explicit disclosure of using a DRAM as the frame buffer in an eDP 1.3 device, a POSITA would have further found it obvious that the Takahashi-Tsern-Schuette device is capable of being applied to an eDP, would have been further motivated to apply that DRAM to an eDP to obtain the benefits of eDP operation, and would have reasonably expected success in doing so. EX1007, [0034]-[0035] EX1003, 202. Further, based on the obvious inclusion of an I/O circuit as discussed in §V.B.3(a)(ii), the Takahashi-Tsern-Schuette device is configured to receive data from and transmit data to off-chip devices, enhancing its applicability as a frame buffer in an eDP configuration. EX1003, 202.

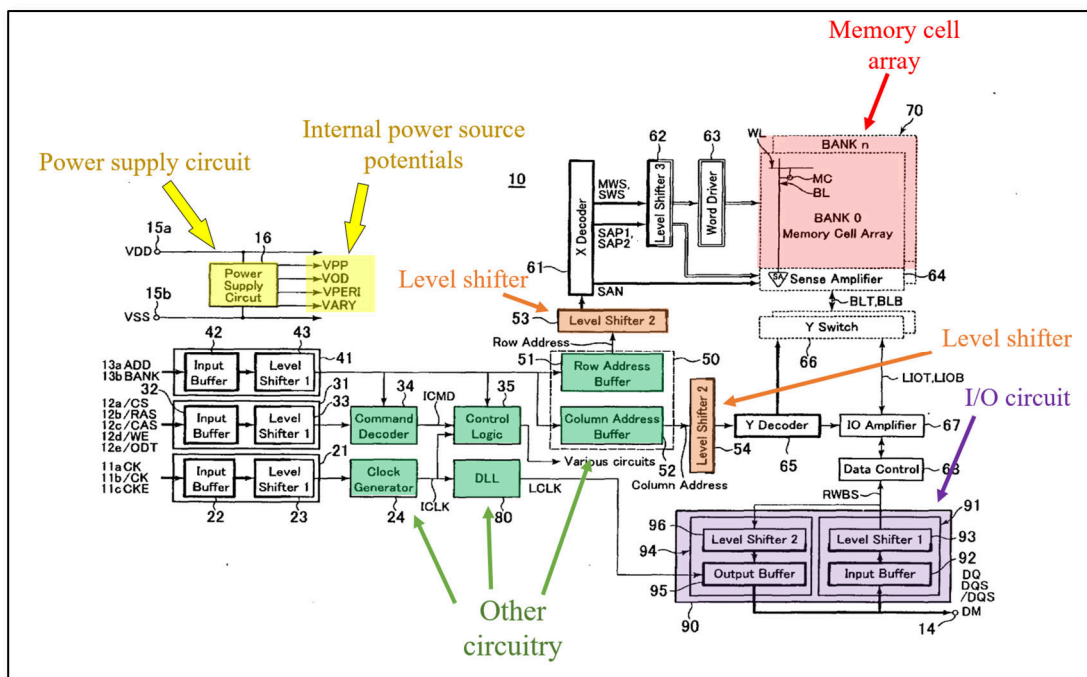
E. GROUNDS 2A and 2A.1: Dono and Goto render obvious claims 1-6; Dono, Goto, and Youn render obvious claims 1-6

1. Dono

Dono is directed to "SDRAM," a type of DRAM. EX1008, [0024]; EX1003, 203. As shown in implementations of Dono depicted, e.g., in FIG. 1, a DRAM includes elements such as a memory cell array 70, a sense circuit 64 including sense

amplifiers, and data I/O circuit 90. EX1008, [0027], [0030], [0032], [0035], [0040], FIG. 1; EX1003, 203.

To power internal components, Dono's DRAM receives an externally-supplied voltage VDD at a power supply circuit, which "generates internal power source potentials VPP, VOD, VPERI, and VARY. These potentials have a size relationship of $VPP > VDD > VOD > VPERI \cong VARY > VSS$." EX1008, [0042]; EX1003, 204. The outlines of circuit blocks of FIG. 1 ("thick line," "normal line," "double line," and "broken line") indicate which voltage is used ("handle[d]") by each component. EX1008, [0043], FIG. 1; EX1003, 204. Some blocks (e.g., the first level shifters 23, 33, 43, 93) are drawn with multiple outlines to indicate that they receive multiple power supply voltages. EX1008, [0043]; EX1003, 204.

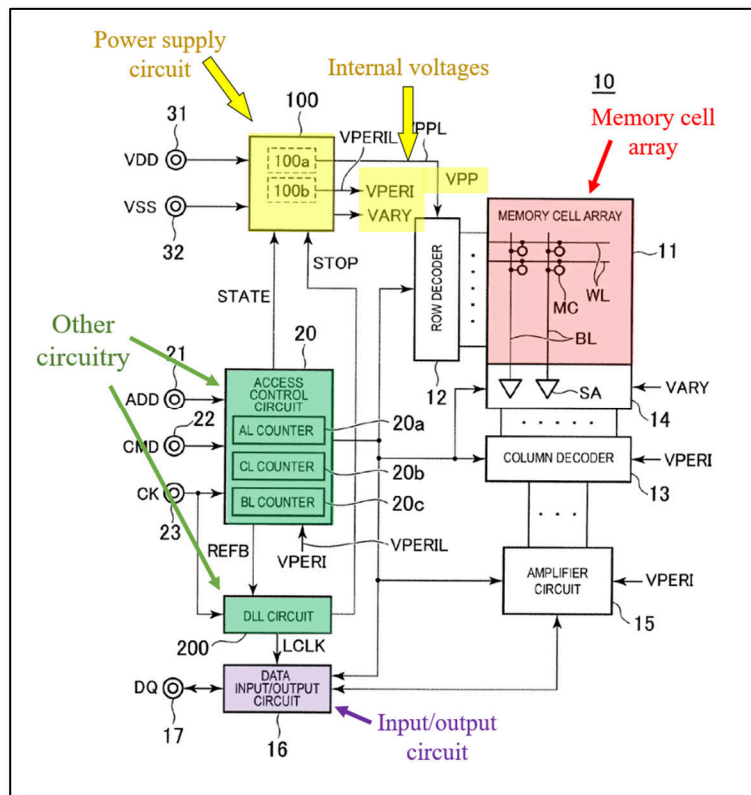


Dono, FIG. 1

2. Goto

Goto is a filing by the same applicant as Dono and, like Dono, relates to DRAM circuits. EX1009, [0022]; EX1003, 205. Implementations disclosed by Goto include, e.g., a FIG. 2 DRAM that has a structure similar to Dono's FIG. 1 DRAM, including a memory cell array 11, a data input/output circuit 16, and an address control circuit 20. EX1009, [0022], FIG. 2; EX1003, 205.

Similar to Dono's circuit, Goto's DRAM includes a power supply circuit 100 that "generates internal voltages V_{PP} , V_{PERI} , [and] V_{ARY} ." EX1009, [0026]; EX1003, 205. These voltages have the same relative relationship as in Dono: " $V_{PP} > V_{DD} > V_{PERI} \approx V_{ARY}$." EX1009, [0026]; EX1003, 206.



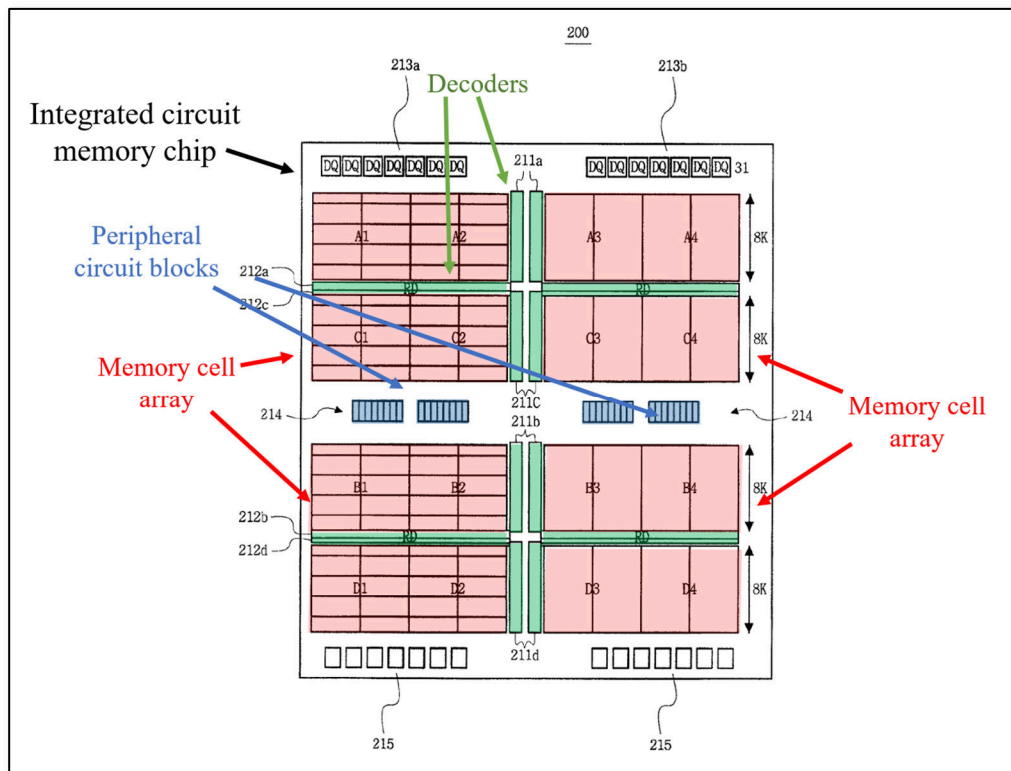
Goto, FIG. 2

3. Youn

Youn is directed to “[m]ulti-bank semiconductor memory devices...having optimized memory block layouts and data line routing to enable chip size reduction and increase operating memory access speed.” EX1010, Abstract; EX1003, 207. In addition to diagrammatic representations of memory devices, some implementations of Youn provide illustrations of physical memory chip layouts. EX1010, FIGS. 1A, 6; EX1003, 207. For example, FIG. 1A illustrates “a semiconductor memory device having a conventional hierarchical memory bank architecture” in the form of “a semiconductor integrated circuit memory chip.” EX1010, 1:48-52; EX1003, 207.

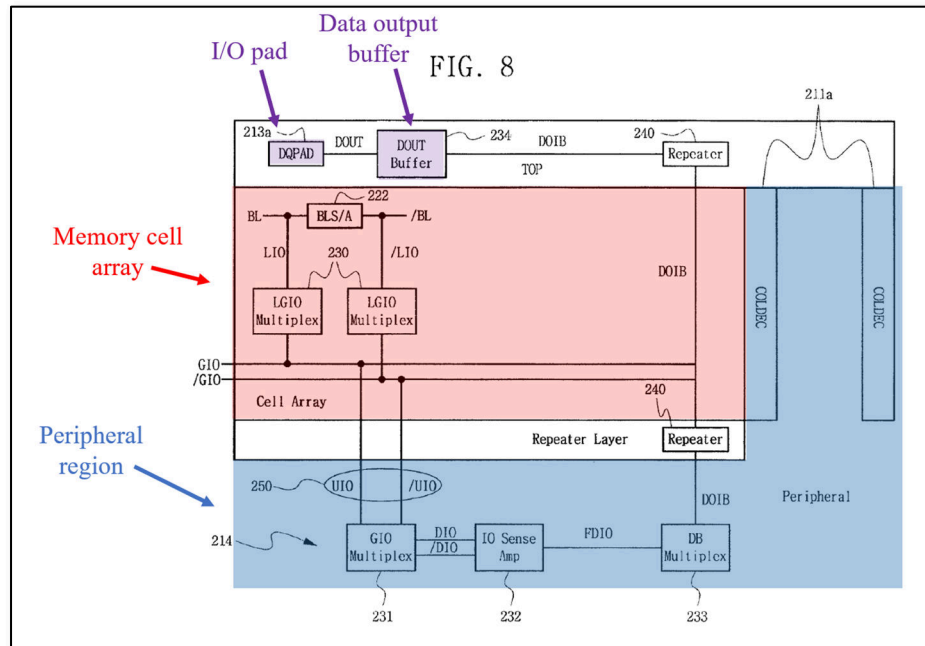
The memory device can be a DRAM. EX1010, 2:26-27, 2:40-44; 5:51-59; EX1003, 207.

FIG. 6 “depicts an exemplary embodiment of the memory device of FIG. 1,” with a “more uniform layout” and a “shorten[ed] data path.” EX1010, 6:22-27; EX1003, 208. “[A] semiconductor integrated circuit memory chip (200)” includes a “memory cell array.” EX1010, 5:59-62; EX1003, 208. The integrated circuit memory chip 200 also includes row/column decoders, peripheral circuit blocks, and I/O circuitry. EX1010, 1:57-67; EX1003, 208.



Youn, FIG. 6

FIG. 8 shows an integrated layout of I/O circuitry, the memory cell array, and a peripheral region. EX1010, 3:20, 7:1-2, 6:43-51, FIG. 8; EX1003, 209, 210.



Youn, FIG. 8

4. Analysis of claims

(a) Claim 1

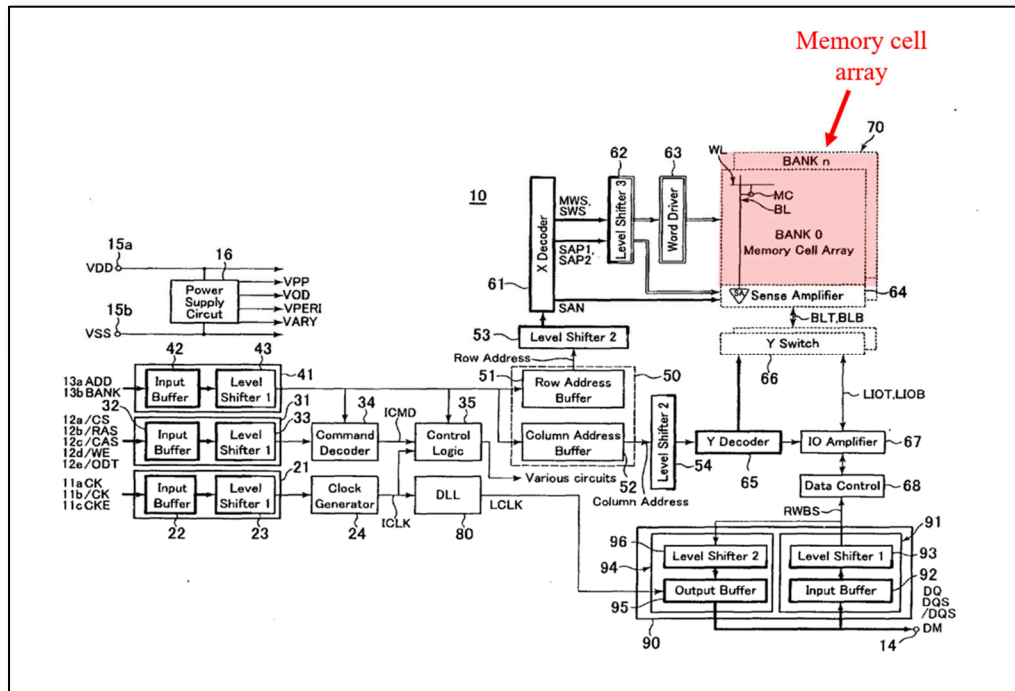
[1.1]:

Dono's "semiconductor device 10" shown in FIG. 1 "is a DDR SDRAM," i.e., a DRAM. EX1008, [0024], FIG. 1; EX1003, 211.

[1.2]:

Dono's DRAM includes a "memory cell array 70 [that] includes dynamic memory cells MC arranged in a matrix." EX1008, [0037], FIG. 1; EX1003, 212. These DRAM memory cells are each a DRAM core cell. EX1003, 212. *See* [1.2] in

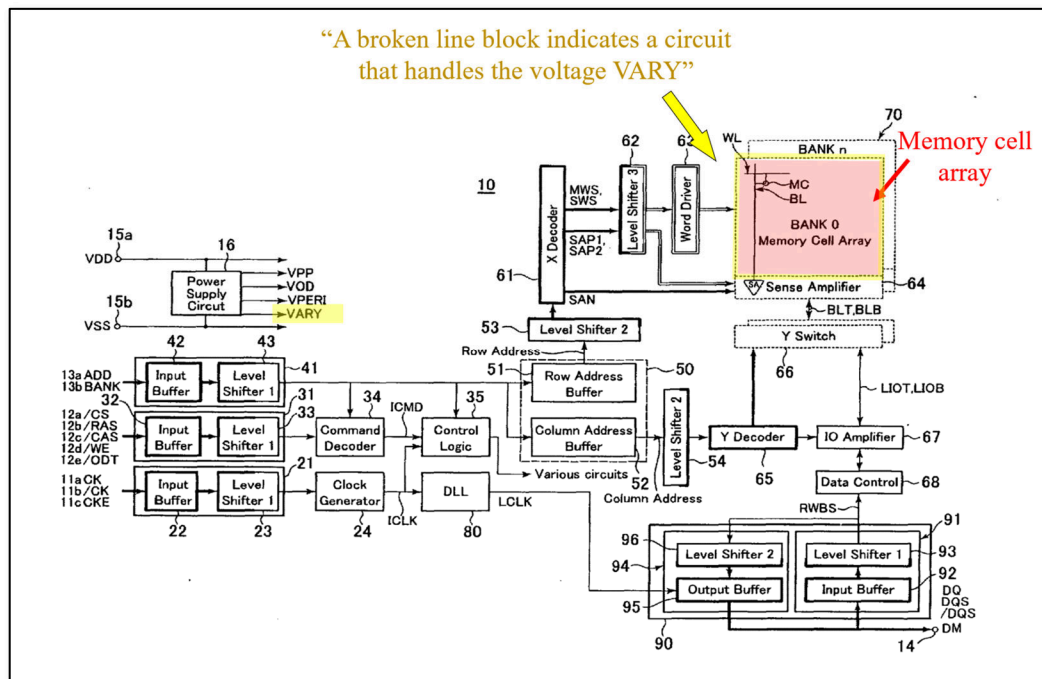
§V.A.2(a) for discussion of why a POSITA would have understood a DRAM memory cell to be a “core” cell. EX1003, 212.



Dono, FIG. 1

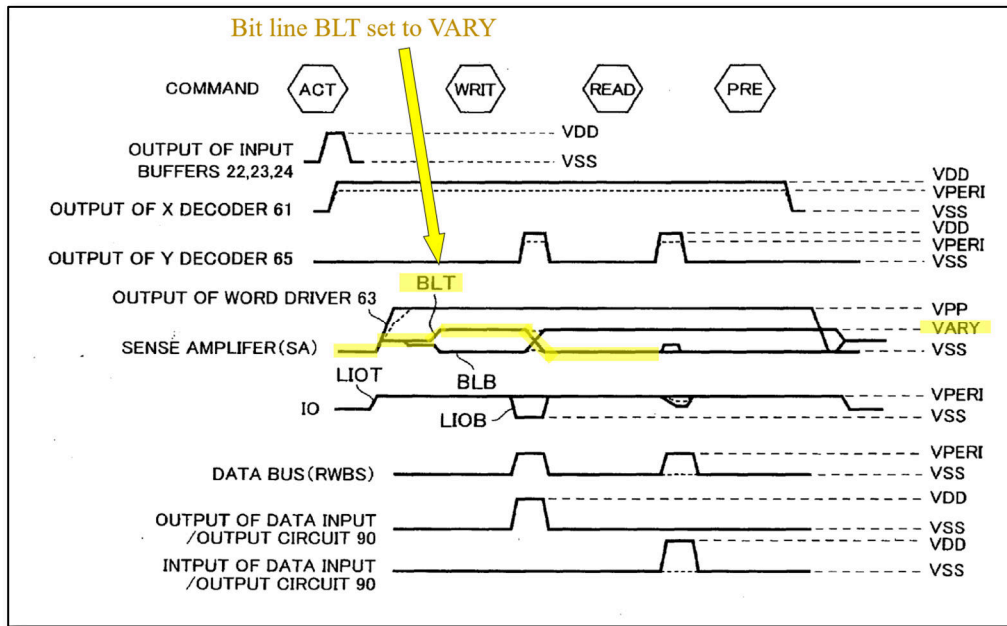
[1.3]:

Dono’s memory cells are supplied with, and operate at, a **first voltage VARY**. EX1003, 213, 216. Dono describes VARY as an “array-system circuit voltage,” in reference to the “array” of memory cells MC, to denote that this is the voltage at which the cells of the array operate. EX1008, [0005]; EX1003, 213. The “broken line” around the memory cell array 70 in FIG. 1 also illustrates that the memory cell array is powered by VARY. EX1008, [0043], FIG. 1; EX1003, 213.



Dono, FIG. 1

FIGS. 2 and 7 illustrate operation of a memory cell at VARY in the context of “read/writing timings.” EX1008, [0078]; EX1003, 214. Based on a “write command WRIT,” a “bit line [] BLT” is driven to VARY as shown in FIG. 7, and “the data is written into the cell capacitor C1 of the memory cell MC.” EX1008, [0083]-[0084], FIG. 7; EX1003, 214. FIG. 2 illustrates the direct connection of the bit line BLT to a memory cell MC1; when the bit line BLT is set to VARY as shown in FIG. 7, VARY is set across a capacitor C1 of the memory cell MC1 to write data to the memory cell MC1. EX1008, FIG. 2; EX1003, 214. Thus, the memory cell operates at VARY. EX1003, 214.



Dono, FIG. 7

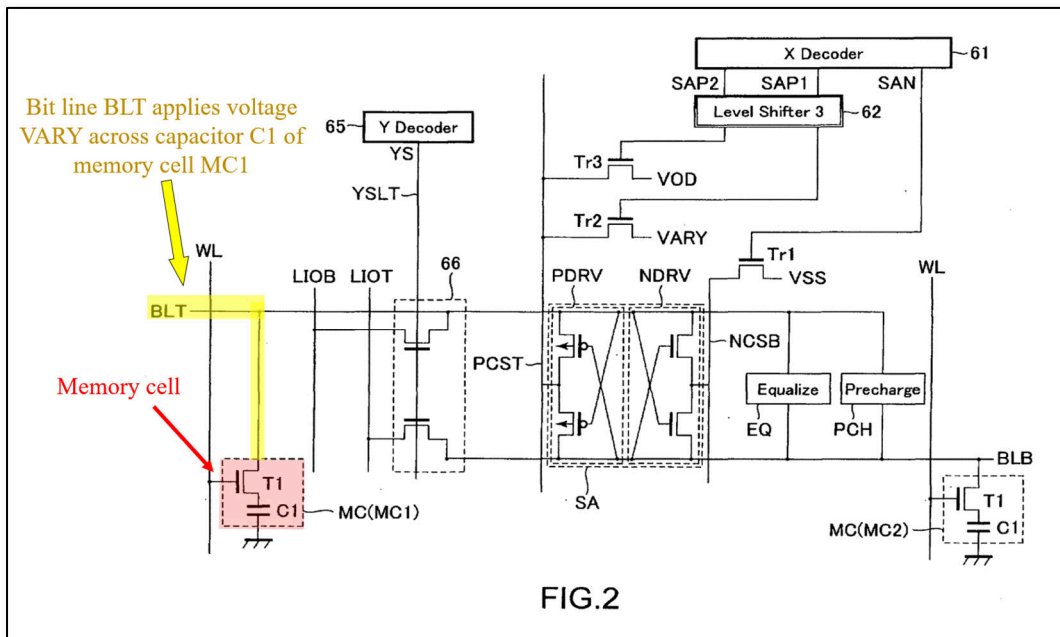


FIG.2

Dono, FIG. 2

For the reasons discussed for [1.3] in §V.A.2(a), the recitation that the first voltage VARY be “within a first voltage range” is satisfied by any range that

encompasses the disclosed value of VARY=1.0V. EX1008, [0005], [0049]; EX1003, 215. The first voltage VARY is also within a small first voltage range around its nominal value of 1.0V due to expected non-idealities in voltage generation and provision. EX1003, 215.

[1.4]:

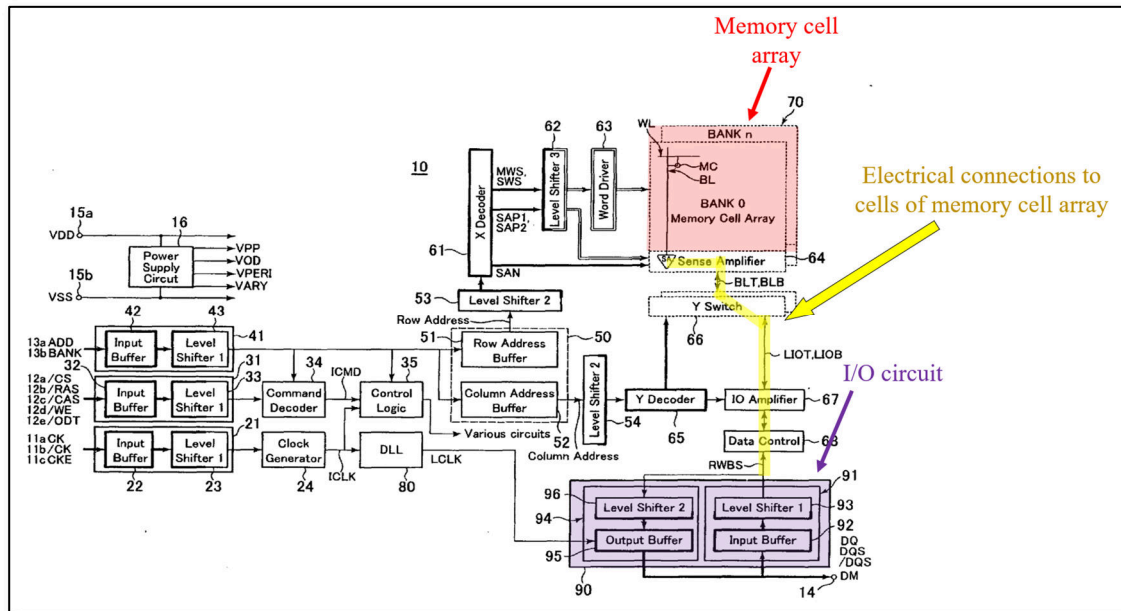
See [1.4] at §V.A.2(a). The memory cells of Dono's DRAM are, by definition, volatile memory cells. EX1003, 217.

[1.5]:

The first voltage VARY of Dono is "1.0 V," which is lower than 1.1 V. EX1008, [0005], [0049], [0105]; EX1003, 218.

[1.6]:

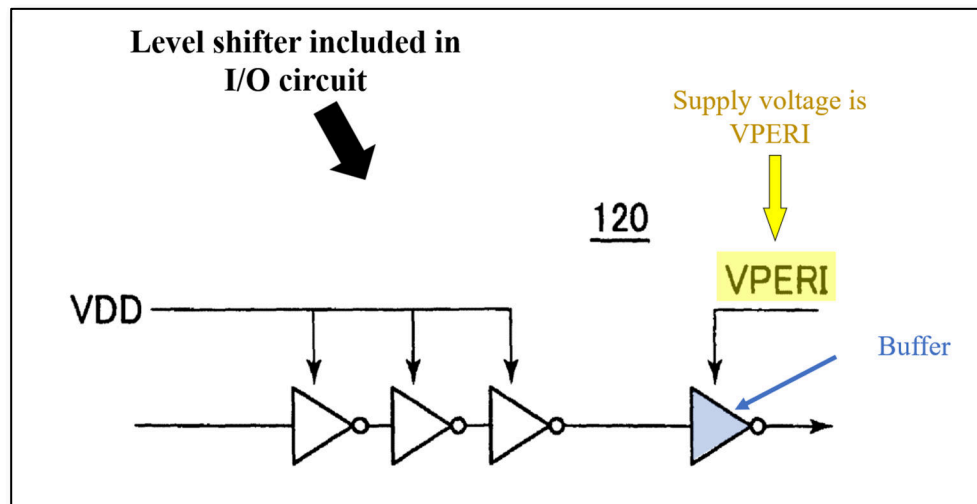
Dono's DRAM includes an "I/O circuit 90" that is electrically connected both to peripheral circuitry and to the cells of the memory cell array 70. EX1008, [0041], FIG. 1; EX1003, 218. For example, as shown below, the I/O circuit 90 is electrically connected to the memory cell array 70 through sense amplifier 64, IO amplifier 67, and data control circuit 68. EX1008, [0039], FIG. 1; EX1003, 216. The I/O circuit 90 performs the claimed input/output function with respect to Dono's DRAM, and Dono discloses at least as much structure as is disclosed for the input/output unit 106 of the '652 Patent. EX1008, [0040], FIGS. 1, 7; EX1003, 219.



Dono, FIG. 1

[1.7]:

Dono's I/O circuit 90 is supplied with a **third voltage VPERI** that makes the I/O circuit 90 operate at the third voltage VPERI. EX1003, 220. For example, the I/O circuit 90 includes a "first level shifter 93." EX1008, [0040]; EX1003, 220. FIG. 6 illustrates a level shifter 120 that "is preferably used for the level shifter...93 shown in FIG. 1." EX1008, [0076]. "**VPERI is supplied** to a power source terminal of the fourth buffer" of the level shifter 93/120. EX1008, [0077]; EX1003, 220. As indicated by the half-"normal line" outline of the level shifter 93 in FIG. 1, the level shifter 93/120 "handle[s]" the third voltage VPERI at its "output side," in agreement with FIG. 6. EX1008, [0043]; EX1003, 220.



Dono, FIG. 6

A POSITA would have understood that the fourth buffer “operates at” VPERI because VPERI is its power supply voltage. EX1003, 221. As Dr. Liu explains, a POSITA would have understood that a circuit such as a buffer “operates at” its supply voltage, e.g., as reflected in buffer datasheets. EX1003, 221; EX1029, 1, 3; EX1030, 1, 3.

Indeed, Dono describes VPERI as “the internal **operation voltage**,” suggesting that circuits supplied with VPERI (such as the fourth buffer and the I/O circuit 90) operate at VPERI. EX1008, [0026]; EX1003, 222.

Thus, the fourth buffer of the first level shifter 93 of the I/O circuit 90 is supplied with and operates at VPERI, meaning that the I/O circuit 90 is supplied with and operates at the third voltage VPERI. EX1003, 223.

[1.8]:

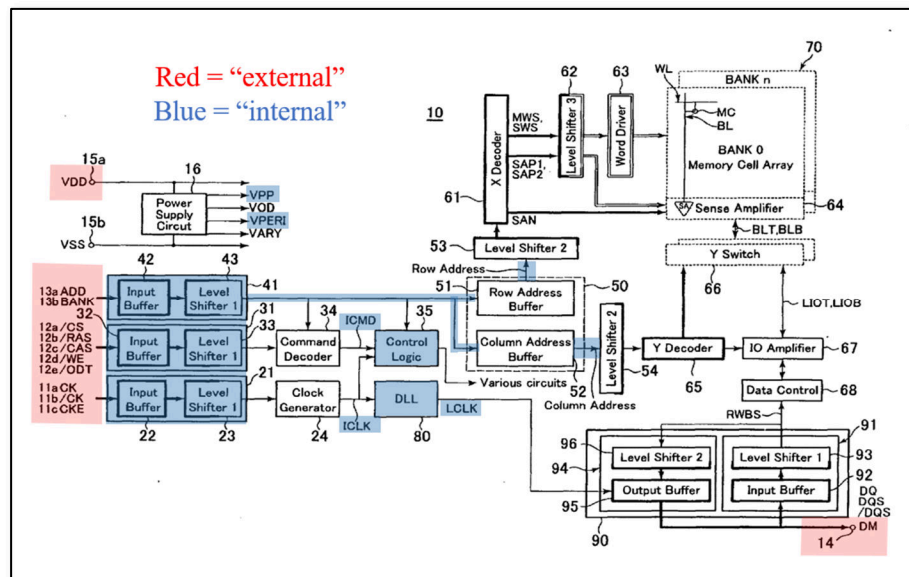
As discussed for [1.7], the third voltage is VPERI. EX1003, 224. VPERI is equal to 1.0V or approximately 1.0V, and therefore is lower than 1.1V. EX1008, [0005], [0026], [0049], [0105]; EX1003, 224.

[1.9]:

Dono's DRAM core cells and input/output circuit are formed on a single chip. EX1003, 225. A POSITA would have understood this for several reasons. **First**, Dono's DRAM receives a "chip select signal /CS" at a "command terminal" 12a. EX1008, [0024], [0028]; EX1003, 225. As a POSITA would have understood, the chip select signal is used to enable or disable a particular memory chip among multiple chips. EX1003, 225. For example, Micron Technology's "DDR3 SDRAM" datasheet describes that the chip select signal "enables [] and disables [] the command decoder. All commands are masked [i.e., ignored] when [the chip select signal] is registered HIGH." EX1022, 17; EX1003, 225. Correspondingly, in Dono's DRAM, the memory cell array 70 would be accessed by selecting the common single chip having both the memory cell array 70 and the I/O circuit 90. EX1003, 225.

Second, Dono describes various "**external** terminals" of the "semiconductor device 10" of FIG. 1, such as terminals 11-14, in contrast to "**internal**" signals and circuits. EX1008, [0024], [0026]; EX1003, 226. In the annotated FIG. 1 below, elements described as "external" are highlighted in red, and elements described as "internal" are highlighted in blue. EX1003, 226. A POSITA would have understood

that the “external terminals” are used for communicating with a separate chip (such as the “data processor 220” shown in FIG. 11), and that “internal” refers to signals and components on a common single chip. EX1008, [0103]; EX1003, 226. In contrast to communication with external devices, Dono does not describe any external terminals, pins, bumps, pads, or the like for communicating between the I/O circuit 90 and the memory cell array 70. EX1008; EX1003, 226. This is because the I/O circuit 90 and the memory cell array 70 are formed on a common single chip. EX1003, 227.



Dono, FIG. 1

Third, as Dr. Liu explains, DRAM circuitry—including memory cell arrays and I/O circuitry—was conventionally integrated in a single chip, and a POSITA would have understood that Dono’s device, lacking disclosure otherwise and conforming to conventional DRAM design, had this conventional configuration.

EX1003, 228. For example, the LPDDR3 standard illustrates pad arrangements for a single DRAM chip, corresponding to a configuration (so well-understood that it did not have to be explicitly articulated) in which DRAM circuitry would be formed as an integrated circuit in a single chip. EX1013, 6-12; EX1003, 228. Also, this configuration would have been obvious to apply to Dono's device. EX1003, 229.

Corroboration of the conventionality of forming DRAM circuitry on a single chip is provided, for example, in EX1036 (illustrating a memory cell array and peripheral circuitry, including an I/O circuit, formed in a single semiconductor substrate), EX1037 (illustrating a physical layout of a DRAM chip including a memory cell array, peripheral circuitry, and I/O circuitry) and EX1038 (describing a semiconductor substrate as having a "memory array region" and a "peripheral region" with integrated circuitry formed therein), among many other references. EX1036, 5:53-6:25, 7:34-39, FIGS. 1, 4; EX1037, 2:44-51, 6:34-8:36, FIGS. 3-4; EX1038, 2:25-31, FIG. 1; EX1039, 2:50-59, 5:63-7:3, FIGS. 1, 2A; EX1040, 1:36-37, 2:16-21, FIG. 20; EX1041, 4:41-44; EX1044, 2; EX1045, FIG. 6; EX1003, 229-230.

(i) **Ground 2A.1: In view of Youn, it would have been obvious to form Dono's semiconductor device on a single chip**

To the extent Dono and Goto alone are not considered to render obvious [1.9] (that "the DRAM core cell and the input/output circuit are formed on a single chip")

a POSITA would in view of Youn have further found it obvious to form Dono's semiconductor device 10—including the memory cell array and I/O circuit—on a single chip. EX1003, 231.

Youn describes “market demands for semiconductor memory devices providing...higher integration density,” where “higher integration density” corresponds to dense integration of circuitry on a single chip. EX1010, 1:25-28; EX1003, 232. To satisfy these “market demands” while achieving high performance, Youn describes a layout of a “semiconductor integrated circuit memory chip (200)” that provides “a more uniform layout for data path lengths” and a “shorten[ed] data path, which reduces the differences in access times for read operations, for a memory device such as a [SDRAM] where timing of data signals is critical.” EX1010, 5:51-59, FIG. 6; EX1003, 232. The semiconductor integrated circuit memory chip 200 advantageously has a layout that is “capable of keeping the sensing efficiency of a data line sense amplifier uniform.” EX1010, 6:27-29; EX1003, 232.

To obtain these advantages, it would have been obvious to form Dono's semiconductor device 10 on a single chip, e.g., conforming to the layouts illustrated by Youn, which have the memory cell array, peripheral circuits, and I/O circuit on a single chip. EX1003, 233. *See* §V.E.3. This implementation would have been obvious as the application of a known technique (DRAM circuit integration) to a

piece of prior art (Dono's DRAM device) ready for the improvement. *KSR* at 416-417. EX1003, 233.

A POSITA would have had a reasonable expectation of success in forming Dono's semiconductor device 10 on a single chip. Dono's and Youn's devices are both DRAMs that include the same or similar components, including memory cell arrays, decoders, peripheral circuitry, and I/O circuitry including buffers and terminals/pads. EX1008, [0005], [0024], [0040], FIG. 1; EX1010, 3:20, 5:57-67, 7:1-2, FIGS. 6, 8; EX1003, 234. Given this similarity in DRAM architecture, a POSITA would have expected Youn's configurations to be directly applicable to Dono's device. EX1003, 234. Further, Youn discloses not merely the *goal* of integration in a single chip but also *specific physical chip layouts* for achieving effective integration, such that a POSITA would have had a clear roadmap for obtaining single-chip integration. EX1010, FIGS. 3, 6, 8; EX1003, 234. Thus, a POSITA would have had a reasonable expectation that forming Dono's semiconductor device 10 on a single chip would be successful. EX1003, 234.

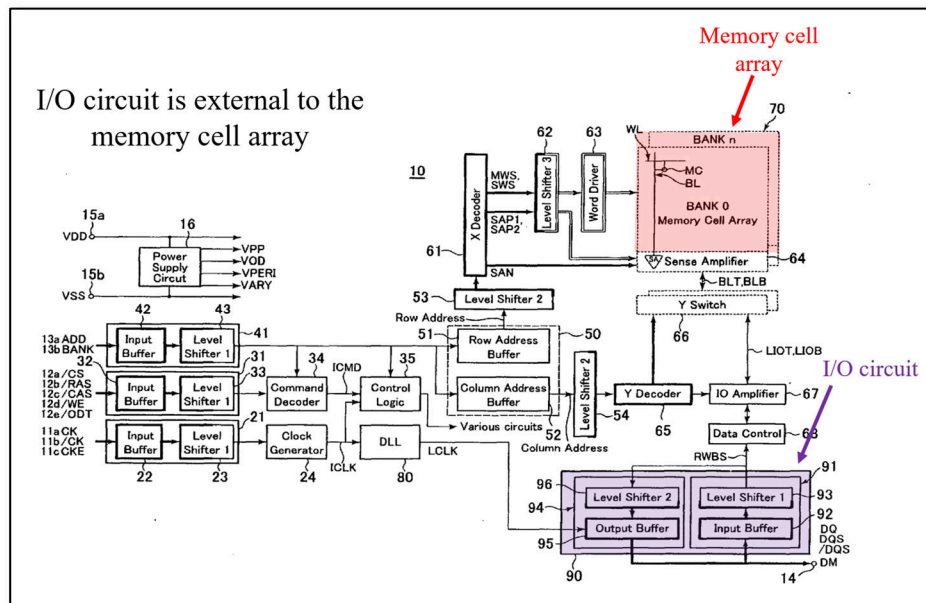
Forming Dono's semiconductor device 10 on a single chip would also have been obvious for obtaining the well-known advantages of device integration common to all semiconductor integrated circuit devices, such as manufacturing efficiency, size reduction, and interconnect simplification. EX1003, 235. Youn's

explicit DRAM chip layouts would have provided a POSITA with an obvious way to achieve these and other advantages of integration. EX1003, 235.

With Dono's semiconductor device 10 implemented so as to be formed on a single chip, Dono's DRAM core cell (cells of the memory cell array 70) and Dono's input/output circuit (I/O circuit 90) would be formed on the single chip. EX1003, 236.

[1.10]:

Dono's I/O circuit 90 is external to the memory cell array 70, as shown in FIG. 1. EX1008, FIG. 1; EX1003, 237.

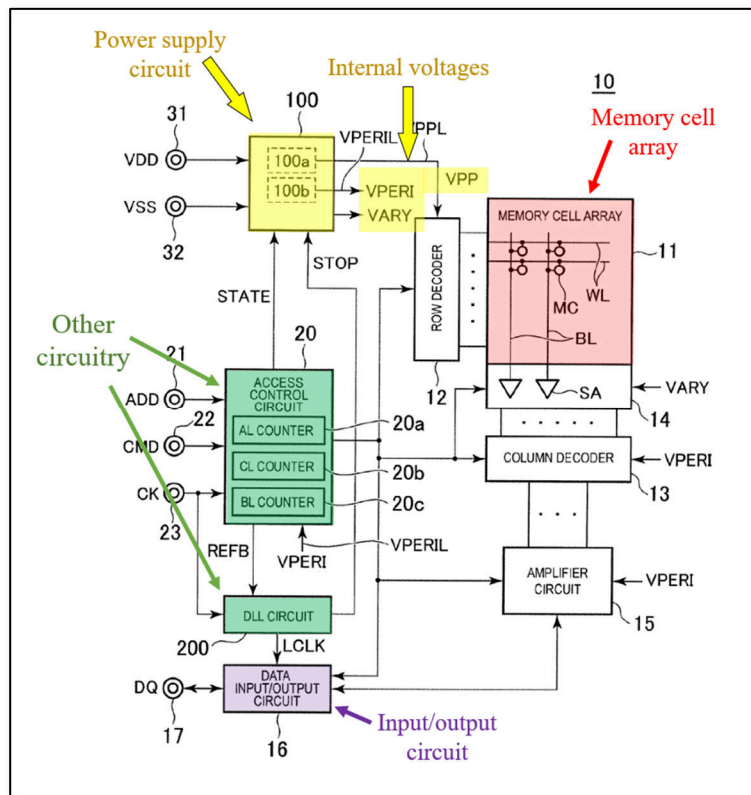


Dono, FIG. 1

[1.11]:

Dono discloses, or at least renders obvious, that the first voltage VARY is different from the third voltage VPERI. EX1003, 238. Dono describes that $VPERI \cong VARY$, meaning that VPERI is *approximately* VARY. EX1008, [0042]; EX1003, 238. The language of [1.11] encompasses any “differen[ce]” between the first voltage and the third voltage, such that any deviation between VARY and VPERI (as disclosed by the use of “ $\cong$ ” instead of “=”) satisfies claim 1. EX1003, 238. Thus, Dono discloses that the first voltage VARY is different from the third voltage VPERI. EX1003, 238.

Goto reinforces that “ $VPERI \cong VARY$ ” is substantively different from “ $VPERI = VARY$ ” and suggests a difference between VPERI and VARY. EX1003, 239. As noted in §V.E.2, Goto shares its applicant with Dono and discloses a similar internal voltage configuration, including the generation of both VPERI and VARY from an external voltage VDD, as shown below. EX1003, 239.



Goto, FIG. 2

Goto describes that “[w]hether $VPERI=VARY$ or $VPERI \approx VARY$ is appropriately determined depending on the intended targets of the respective corresponding plurality of circuits.” EX1009, [0027]. That is, Goto explicitly differentiates between $VPERI$ being *equal to* $VARY$ and $VPERI$ being *approximately* $VARY$. EX1003, 240. In view of this similar disclosure from the same applicant, it would have been obvious to a POSITA that $VPERI$ and $VARY$ are, or obviously should be, different from one another, satisfying claim 1. EX1003, 240.

For example, Goto describes that “[w]hether $V_{PERI}=V_{ARY}$ or $V_{PERI}\approx V_{ARY}$ is appropriately determined depending on the intended targets of the respective corresponding plurality of circuits.” EX1009, [0027]. It would have been obvious to “appropriately” make V_{PERI} approximately equal to, but different from, V_{ARY} in order to satisfy “the intended targets of the respective corresponding plurality of circuits [i.e., the peripheral circuits].” EX1009, [0027]; EX1003, 241. This would have constituted mere optimization of a result-effective variable (V_{PERI}), within the range disclosed in the art (V_{PERI} approximately V_{ARY}), to achieve the recognized result of making V_{PERI} “appropriate” for the peripheral circuits. EX1009, [0027]; EX1003, 241.

(b) Claim 2

Claim 2’s elements are found identically in claim 1, except for [2.11] discussed below. For [2.1]-[2.10], *see* [1.1]-[1.10] in §V.E.4(a), respectively. EX1003, 242.

[2.11]:

See [1.11] in §V.E.4(a). Dono’s disclosure that “ $V_{PERI}\cong V_{ARY}$ ” explicitly encompasses small differences between the first voltage V_{ARY} and the second voltage V_{PERI} . EX1008, [0042]; EX1003, 243. It is well-established that a recited range (here, the first voltage being greater than the third voltage) overlapping with or lying inside a range disclosed by the prior art (here, the third voltage being

slightly-greater-than to slightly-less-than the first voltage) is obvious, absent countervailing evidence such as unexpected results, which have not been alleged or evidenced here. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (C.C.P.A. 1976); *In re Geisler*, 116 F.3d 1465, 1469-71, 43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997); *In re Bergen*, 120 F.2d 329, 332, 49 USPQ 749, 751-52 (C.C.P.A. 1941).

Goto provides further motivation to make VARY greater than VPERI. Goto describes that “[w]hether $VPERI=VARY$ or $VPERI\approx VARY$ is appropriately determined depending on the intended targets of the [peripheral circuits receiving VPERI].” EX1009, [0027]; EX1003, 244. It would have been obvious to vary VPERI around VARY—including making $VARY>VPERI$, satisfying claim 2—in order to better match VPERI to peripheral circuit(s) for which a VPERI differing from VARY is more “appropriate.” EX1009, [0027]; EX1003, 244.

Further, Goto describes that “[u]sing the internal voltage VPERI lower than VDD as the operating voltage of the peripheral circuits reduces the power consumption of the peripheral circuits.” EX1009, [0027]; EX1003, 245. This disclosure would have provided a POSITA with a motivation to reduce VPERI in order to reduce power consumption, thereby arriving at VARY greater than VPERI through this voltage and power optimization. EX1003, 245.

(c) Claim 3

[3.1]-[3.7]: See [1.1]-[1.4] and [1.6]-[2.8] in in §V.E.4(a), respectively.

[3.8]: See [2.11] in §V.E.4(b).

[3.9]:

For the reasons discussed in §V.A.2(c) for Ground 1A, a POSITA would have understood that Dono's DRAM is capable of being applied to an eDP. EX1003, 248. That is, Dono's memory is a working, conventional DRAM that is capable of satisfying the requirements of the eDP 1.3 standard, which do not include any voltage or power requirements. EX1014; EX1003, 248. The eDP 1.3 standard requires that the frame buffer store and provide data representing a static image. EX1014; EX1003, 248. Dono's DRAM, which stores data, supports read and write operations, and provides "high-speed data transfer," is more than capable of fulfilling these requirements. EX1008, [0009], [0040]; EX1003, 248.

To the extent the '652 Patent erroneously links "capable to be applied to an embedded display port (eDP)" to low-voltage operation, then Dono's DRAM, which has first (VARY) and third (VPERI) voltages that satisfy the "< 1.1 V" condition of the '652 Patent, would be equally as capable of being applied to an eDP as the '652 Patent's devices. EX1001, 4:61-5:9, Table III; EX1003, 249.

(d) Claim 4

[4]:

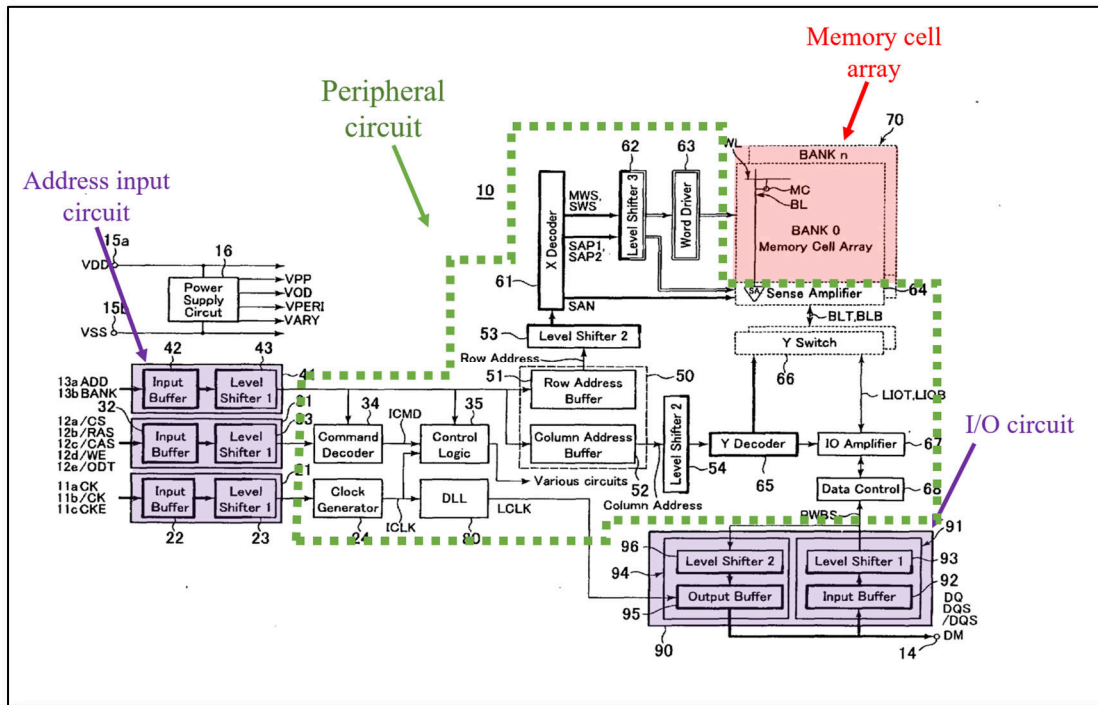
See [1.5] in §V.E.4(a). The first voltage VARY of Dono is "1.0 V," which is lower than 1.1 V. EX1008, [0005], [0049], [0105]; EX1003, 250.

(e) Claim 5

[5.1]:

Dono discloses several peripheral circuits electrically connected to the DRAM core cell, including the command decoder 34, the control logic 35, the clock generator 24, the row address buffer 51, the column address buffer 52, the I/O amplifier 67, and/or the data control circuit 68. EX1003, 251. A POSITA would have understood that these peripheral circuits could also be collectively referred to as “a” peripheral circuit. EX1003, 251.

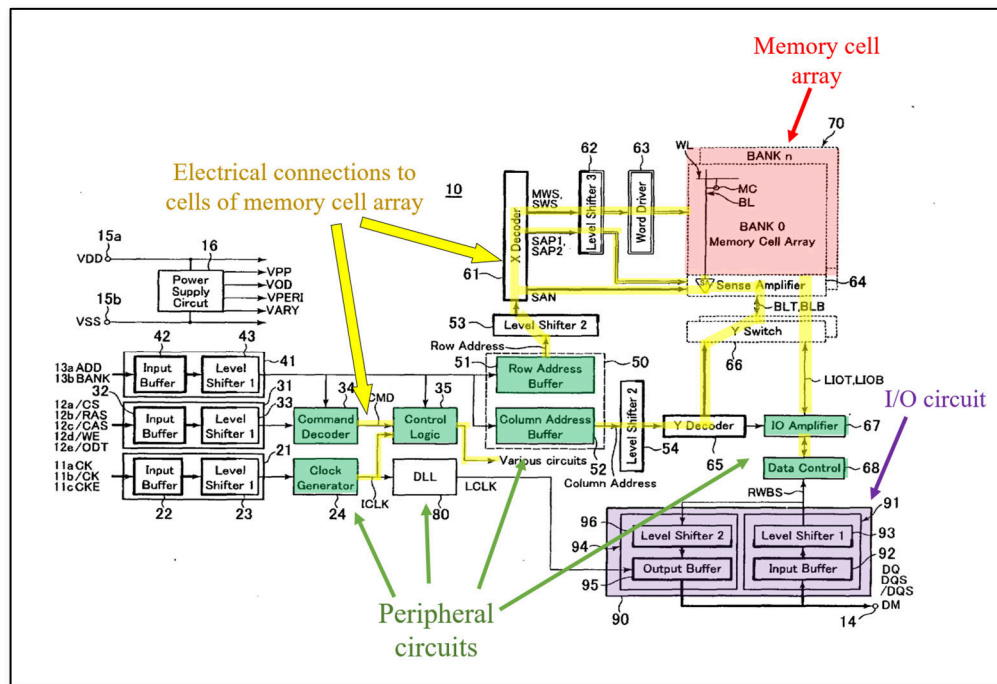
The textbook *VLSI Memory Chip Design* explains that “[a] memory chip is composed of three blocks[]: a memory cell array, a peripheral circuit, and an input/output (I/O) interface circuit.” EX1020, 15; EX1003, 252. The peripheral circuit “bridges between the memory array and the I/O interface circuit so that they can communicate with each other.” EX1020, 17; EX1003, 252. In Dono’s DRAM, this “bridg[ing]” peripheral circuit between the memory cell array 70 and the data I/O circuit 90/address input circuit 41 is outlined in green below. EX1003, 252.



Dono, FIG. 1

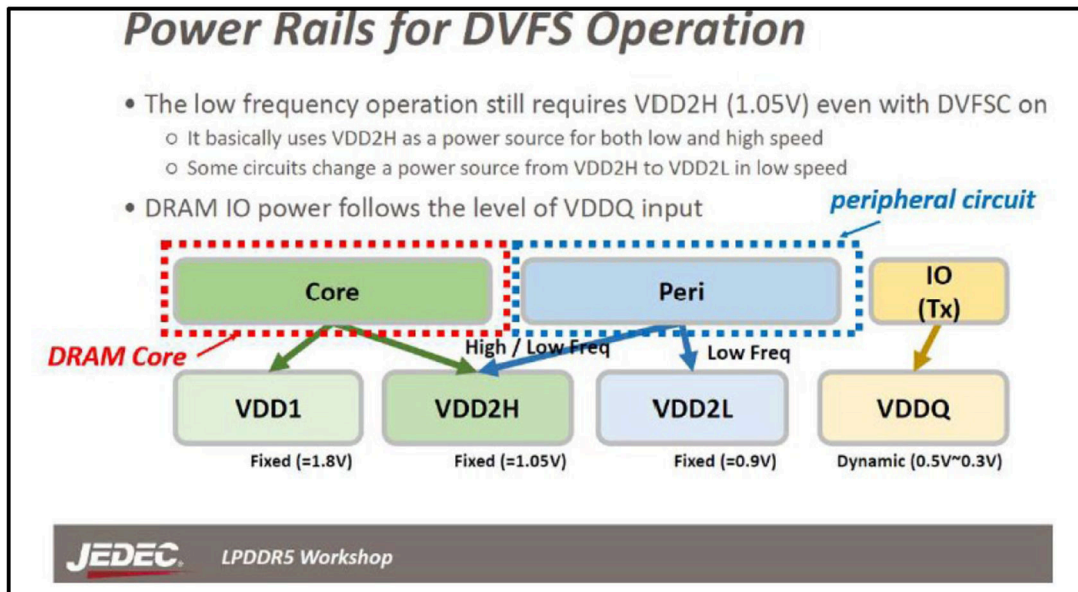
That these circuits are “peripheral” circuits is supported by the fact that each receives the “peripheral circuit voltage VPERI,” as indicated by their “normal line” outlines. EX1008, [0005], [0043]; EX1003, 253.

Each of these circuits is electrically connected to the DRAM core cells (cells of the memory cell array 70) as illustrated below. EX1003, 254.



Dono, FIG. 1

WeCrevention’s Complaint corroborates that these circuits are a “peripheral circuit [] electrically connected to the DRAM core cell.” EX1021, 21; EX1003, 255. In discussing the products accused in the parallel litigation, WeCrevention provided the below annotated diagram to define “peripheral circuit.” EX1021, 21; EX1003, 255. According to this diagram, DRAM elements besides the core and I/O circuitry—similar to the above-cited elements of Dono’s DRAM—are categorized as peripheral circuits. EX1003, 255.



EX1021, 21 (annotations in original)

The WeCrevention Complaint also states that “the LPDDR5 DRAM includes buffers and other data path circuits (*i.e.*, peripheral circuits) connected to the DRAM core cell.” EX1021, 21. Most of the circuits of Dono cited above for the “peripheral circuit” either *are* buffers (the row address buffer 51 and the column address buffer 52) or are on a data path with the buffers (the command decoder 34, the control logic 35, the I/O amplifier 67, and the data control circuit 68), further indicating that they are peripheral circuits. EX1003, 256-257.

[5.2]:

Dono’s command decoder 34, control logic 35, clock generator 24, row address buffer 51, column address buffer 52, I/O amplifier 67, and data control circuit 68 are each supplied with, and operate at, a **second voltage VPERI**. EX1003,

258. VPERI is the “peripheral circuit voltage.” EX1008, [0005]; EX1003, 258. The “normal line” outlines of these circuits in FIG. 1 indicates that they “handle” VPERI. EX1008, [0043]; EX1003, 258. From this description, a POSITA would have understood that these circuits are supplied with VPERI. EX1003, 258. VPERI is also referred to as an “internal **operation** voltage,” indicating that the circuit elements “handl[ing]” VPERI operate at VPERI. EX1008, [0007]; EX1003, 258.

Goto corroborates, and would have further made obvious to a POSITA, that the circuits described as “handl[ing]” VPERI are supplied with and operate at VPERI. EX1003, 259. Goto (which, as noted above, shares an applicant and overall DRAM structure with Dono) describes that “[t]he internal voltage **VPERI is supplied to most of the peripheral circuits...**The internal voltage **VPERI is the operating voltage** of such peripheral circuits.” EX1009, [0027]; EX1003, 259. By reference to Goto, a POSITA would have understood that the indicated peripheral circuits of Dono operate at VPERI, and would have found it obvious to configure the peripheral circuits of Dono to operate at VPERI to ensure their correct operation. EX1003, 259.

[5.3]:

As noted above, “VARY is 1.0 V,” and Dono also describes that “VPERI $\cong$ VARY.” EX1008, [0042], [0105]; EX1003, 260. Dono also provides a specific value of VPERI as “VPERI=1.0 V.” EX1008, [0105]; EX1003, 260.

Accordingly, Dono discloses that the second voltage VPERI is lower than 1.1 V. EX1003, 260.

(f) Claim 6

[6]:

See discussion at [1.11]. Dono discloses that the second voltage VPERI is approximately VARY (“VPERI $\cong$ VARY”), where “VARY is 1.0 V.” EX1008, [0042], [0105]; EX1003, 261. Dono’s use of “ $\cong$,” together with Goto’s explicit distinction between “VPERI=VARY” and “VPERI $\approx$ VARY” and Goto’s disclosed motivations to (i) optimize VPERI for target circuit operation and (ii) reduce VPERI to reduce power consumption, disclose or at least render obvious that the first voltage VARY is different from the second voltage VPERI. EX1009, [0027]; EX1003, 261.

F. Grounds 2B and 2B.1: Dono, Goto, and Endo render obvious claims 3-6; Dono, Goto, Youn, and Endo render obvious claims 3-6

1. Claims 3-6

Endo is applied here as discussed for Ground 1C in §V.C.2. As discussed in §V.E, Dono and Goto (or alternatively/additionally Dono, Goto, and Youn) render obvious claims 3-6. In view of Endo’s explicit disclosure of using a DRAM as the frame buffer in an eDP 1.3 device, a POSITA would have further found it obvious that Dono’s DRAM is capable of being applied to an eDP, would have been further motivated to apply that DRAM to an eDP to obtain the benefits of eDP operation,

and would have reasonably expected success in doing so. EX1007, [0034]-[0035]
EX1003, 262.

VI. FEES

Petitioner authorizes the Patent and Trademark Office to charge any fees to
Deposit Account No. 06-1050.

VII. MANDATORY NOTICES—37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest—37 C.F.R. § 42.8(b)(1)

Petitioner, Apple Inc. is the real party-in-interest.

B. Related Matters—37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or
petitions for inter partes review for the '652 Patent. The '652 Patent is the subject
of civil action: *WeCrevention, Inc. v. Dell Inc. et al*, 2-25-cv-01040 (EDTX) dated
Oct. 10, 2025; *WeCrevention, Inc. v. Apple Inc.*, 7-25-cv-00458 (WDTX), dated
Oct. 07, 2025; *WeCrevention Inc. v. Lenovo Group Limited et al*, 2-25-cv-
01008 (EDTX), dated Oct. 03, 2025; *WeCrevention, Inc. v. Apple Inc.*, 2-25-cv-
00951 (EDTX) dated Sep. 16, 2025.

C. Lead And Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
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D. Service Information

Please address all correspondence and service to the address listed above.

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Respectfully submitted,

Dated: February 13, 2026

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,984 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 13, 2026

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 13, 2026, a complete and entire copy of this Petition for *Inter partes* Review, Power of Attorney, and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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