

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,

Petitioner,

v.

WECREVENTION, INC.,

Patent Owner.

Patent No. 12,154,652

Filing Date: December 15, 2023

Issue Date: November 26, 2024

Inventors: Der-Min Yuan, Yen-An Chang, and Wei-Ming Huang
Title: DYNAMIC RANDOM ACCESS MEMORY APPLIED TO AN
EMBEDDED DISPLAY PORT

PATENT OWNER'S PRELIMINARY RESPONSE

Case No. IPR2026-00243

TABLE OF CONTENTS

	Page(s)
I. INTRODUCTION	1
II. CLAIM CONSTRUCTION	5
III. LEVEL OF ORDINARY SKILL IN THE ART	6
IV. PETITIONER HAS NOT DEMONSTRATED A REASONABLE LIKELIHOOD OF SUCCESS, AND THE PETITION SHOULD BE DENIED	6
A. The Petition Should Be Denied Because Petitioner Takes Inconsistent and Improper Claim-Construction Positions Without Explanation	8
1. Apple’s Inconsistent Positions Across the Two Forums	8
2. The Unexplained Inconsistency Warrants Denial Under Revvo, Tesla, and Cambridge, and Terumo	10
3. Apple’s Hedged Positions Independently Seek an Impermissible Advisory Opinion Under Samsung- Uniloc	13
4. Apple’s Attempted Equivalence Showing Is Inadequate Under Fresenius	14
5. The Board Should Deny Institution in View of Apple’s Claim Construction Positions	16
B. The Takahashi-Based Grounds (1A–1D) Fail Because Takahashi’s VPPL Is Not the Externally-Supplied Sub-1.1V Voltage the Claims Require	16
1. The ’652 Patent’s Operation Voltages (Including the “first voltage”) Are Externally-Supplied	17
2. Takahashi’s VPPL Voltage Is Internally Generated, Not Externally Supplied	19

3.	The Takahashi-Based Grounds Independently Fail Because Takahashi’s Voltages Are Not “Capable to Be Applied to an Embedded Display Port (eDP)” as Element [3.9] Requires	20
C.	The Takahashi-Based Grounds (1A–1D) Fail Independently Because Apple’s Mapping Requires Driver Area 204 to Function Simultaneously as Both the Separately Claimed “Peripheral Circuit” and “Input/Output Circuit”	23
1.	The Claims Require a Structurally Distinct “Peripheral Circuit” and “Input/Output Circuits”	23
2.	Apple’s Mapping of the “Peripheral Circuit” and “Input/Output Circuit” to Driver Area 204 Is Defective	24
D.	The Takahashi-Based Grounds Also Fail Because the Mapping for “Comprised in the DRAM” Excludes Takahashi’s Logic Circuit 105—Closing Apple’s Attempt to Avoid the Double-Mapping in § IV.C	26
E.	The Tsern, Schuette, and Endo Combinations (Grounds 1B–1D) Independently Fail.....	27
1.	Takahashi + Tsern + Schuette (Ground 1B) Cannot Place a Structurally Distinct I/O Circuit Within Takahashi’s DRAM and Transposes a Board-Level Architecture Onto an On-Chip One	27
2.	Takahashi + Endo (Ground 1C) Adds eDP Context Without Curing the Voltage Defects	28
3.	Takahashi + Tsern + Schuette + Endo (Ground 1D) Suffers from All of the Defects of Ground 1A-1C Combined	29
4.	Takahashi’s System-LSI Purpose Counsels Against the Combinations	30
F.	The Dono + Goto Grounds (2A and 2B and Their 2A.1 and 2B.1 Variants) Fail	30

1.	Apple’s Mapping Inverts the Voltage Relationship Required by Claims 2 and 3	30
2.	Dono’s VARY and VPERI Are Internal Voltages, Not Externally-Supplied Operation Voltages	32
3.	The Structural Defects Identified for Takahashi Apply Equally to Dono + Goto	32
V.	CONCLUSION.....	34

LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions in <i>WeCrevention, Inc. v. Apple Inc.</i> , Case No. 7:25-cv-00458-ADA (W.D. Tex.), dated January 20, 2026
2002	Defendant's Invalidity and Subject Matter Eligibility Contentions in <i>WeCrevention Inc. v. Apple Inc.</i> , Case No. 7:25-cv-00458-ADA (W.D. Tex.), dated March 17, 2026
2003	Federal Register, Vol. 90, No. 199, dated Friday, October 17, 2025
2004	Scheduling Order (Dkt. 32) in <i>WeCrevention, Inc. v. Apple Inc.</i> , Case No. 7:25-cv-00458-ADA (W.D. Tex.), dated January 21, 2026
2005	https://marketrealist.com/2019/12/will-china-still-be-second-home-apple/
2006	Appeal Statistics, Patent Trial and Appeal Board, dated October 31, 2025
2007	Patent Trial and Appeals Board (PTAB) data at a glance December 2025
2008	March 24, 2025 guidance memorandum from Chief Administrative Patent Judge Boalick
2009	Director Squires Memorandum, Additional Discretionary Institution Considerations — U.S. Manufacturing and Small Business Use of AIA Proceedings (Mar. 11, 2026)
2010	MacRumors / Financial Times, Apple Plans to Source All U.S.-Bound iPhones from India by End of 2026, Apr. 25, 2025
2011	Korea Economic Daily / MacRumors, Samsung Becomes Apple's Primary LPDDR5X Supplier for iPhone 17, Providing 60–70% of Memory, Dec. 22, 2025
2012	SK hynix Newsroom, <i>Semiconductor 101: SK hynix on Where Chips Are Made & Used</i> (Apr. 3, 2025)
2013	Apple Newsroom, Apple Increases U.S. Commitment to \$600 Billion, Announces American Manufacturing Program, Aug. 6, 2025, https://www.apple.com/newsroom/2025/08/apple-increases-us-commitment-to-600-billion-usd-announces-ambitious-program/

Exhibit No.	Description of Document
2014	Samsung Semiconductor Newsroom, <i>Samsung Begins Mass Production of 16Gb LPDDR5 DRAM at World's Largest Semiconductor Line</i> (Sept. 9, 2020)
2015	SK hynix Inc., <i>SK hynix Signs Investment Agreement of Advanced Chip Packaging with Indiana</i> (Apr. 3, 2024)
2016	Apple's Opening Claim Construction Brief in <i>WeCrevention, Inc. v. Apple Inc.</i> , Case No. 7:25-cv-00458-ADA (W.D. Tex.) Dkt., 40, dated May 6, 2026

I. INTRODUCTION

Apple’s Petition for *inter partes* review of the ’652 Patent should be denied. It fails for reasons that emerge from Apple’s own filings, from the prior-art references Apple selected, and from the prosecution history. Each of the independent defects identified below is, on its own, sufficient to defeat institution; taken together, they show a Petition that did not, and on the references Apple chose could not, demonstrate a reasonable likelihood of success on any Challenged Claim.

First, Apple’s claim-construction posture is irreconcilable. In the parallel district-court litigation¹, Apple has told the district court that the “*input/output [unit/circuit]*” terms—which pervade the Challenged Claims—invoke 35 U.S.C. § 112 ¶ 6 and that the ’652 Patent’s specification “[l]acks sufficient structure (indefinite).” Ex. 2016 at 12. In this Petition, Apple proceeds as though those same terms have adequate corresponding structure (identified by Apple as the input/output unit 106 in the specification of the ’652 Patent), and Apple applies prior art to that structure under a § 112(f) framework that Apple expressly reserves the right to disavow. Pet. at 4–5. Apple offers no explanation for the inconsistency. Under *Revvo*, *Tesla*, *Cambridge*, and *Terumo*—the framework the Director has now applied to deny institution multiple times—Apple’s unexplained inconsistency is,

¹ *WeCrevention, Inc. v. Apple Inc.*, Case No. 7-25-cv-00458 (W.D. Tex.)

standing alone, dispositive. And Apple’s “regardless of whether” § 112(f) applies hedge and its express “not conceding” reservation are the precise tactic the Board rejected in *Samsung-Uniloc* as an impermissible request for an advisory opinion from the Board on indefiniteness.

Second, Apple’s Takahashi-based Grounds fail on the face of the prior art Apple chose. The ’652 Patent’s operation voltages are externally supplied voltages (tracking exemplary JEDEC standards)—not internally-generated on-chip voltages downstream of them. ’652 Patent, 2:64–3:2, 4:6–11. Apple itself draws this exact distinction in the Petition: “A DRAM device is provided with one or more external voltages, which may be converted to internal voltages supplied to various circuits of the device.” Pet. 7. Apple’s ’652 Patent voltage candidate—Takahashi’s VPPL—is, on Takahashi’s express disclosure, an internal voltage because the DRAM of Takahashi is an embedded DRAM and Takahashi’s on-chip VPP power supply 110 supplies as the high-potential-side voltage of the wordline drivers in driver area 204, with a value of approximately 1.0V. EX1004, [0081], [0083]–[0084]. That is exactly the kind of internal voltage Apple’s own Petition framed as downstream of, not equivalent to, the externally-supplied operation voltage. The only Takahashi voltage that is externally supplied to Takahashi’s DRAM—VDD—was expressly considered, addressed, and overcome during prosecution of the ’652 Patent’s parents (the ’017 and ’098 Patents), and Apple does not map it.

Third, Apple’s structural mapping requires Takahashi’s driver area 204 to function simultaneously as two structurally distinct claimed circuits—the “*peripheral circuit*” and the “*input/output circuit*.” Apple itself describes its mapping as having the driver area 204 serve as the “peripheral circuit *or* as an input/output circuit” (Pet. 22) and concedes Takahashi’s embedded DRAM “may lack off-chip I/O circuitry” (Pet. 21). The claims do not recite either-or; they require both circuits, each as a structurally distinct element supplied with its own claimed operating voltage. Apple’s bifurcated approach—mapping driver area 204 as the input/output circuit in Grounds 1A/1C and as the peripheral circuit in Grounds 1B/1D, Pet. 22-23—is an admission, not a cure: no single Takahashi structure can fill the two structurally distinct claim limitations.

Fourth, the claims further require the “*peripheral circuit*” and “*input/output circuit*” to be “*comprised in the DRAM*”—a limitation Takahashi’s logic circuit 105 fails. Takahashi’s own text places the logic circuit 105 outside the semiconductor memory circuit 201 (which Apple maps to the claimed DRAM). Ex. 1004, [0078]. Once logic circuit 105 is excluded, the candidate Takahashi structures within the DRAM—sense amplifier area 103 and driver area 204—cannot satisfy the claims’ voltage-differentiation requirements: on Apple’s own mapping, both are supplied with VDD as the operating voltage. Apple cites to nothing inside the DRAM at a voltage distinct from VDD to fill the third-voltage role.

Fifth, Apple’s secondary references do not cure these defects. Tsern describes its I/O interface as the external interface between a memory controller and a memory device—a memory system level with distinct memory controller and memory chip. Schuette is a board-level memory module with discrete chips on a printed circuit board and discrete diode-based voltage drops between board-level voltage planes—structurally incompatible with Takahashi’s on-chip system-LSI. Endo provides eDP context but specifies no DRAM voltage levels. Each combination inherits, rather than cures, the defects of Ground 1A. Further, the four-reference Ground 1D compounds the problem by stacking borrowings that pull the resulting hypothetical device further from each reference’s actual disclosure.

Sixth, Apple’s alternative Dono + Goto family of Grounds fails for the same external-vs-internal voltage reason and for an additional reason. Dono’s VARY and VPERI are not externally-supplied voltages; they are on-chip outputs of an internal voltage generator supplied with an externally supplied 1.5V VDD in a DDR3 context, Ex. 1008, [0023]–[0026], [0042], [0105], FIG. 3—the same downstream-internal-voltage defect that defeats VPPL in Takahashi. Moreover, Claims 2 and 3 each require the “*first voltage*” (cell) to be greater than the “*third voltage*” (input/output). ’652 Patent, Cls. 2, 3. Apple maps the “*first voltage*” to VARY and the “*third voltage*” to VPERI. Pet. 82–86. But Dono and Goto both disclose $VPP > VDD > VPERI \cong VARY$, with VPERI listed first in the descending hierarchy, and

Dono’s embodiment expressly recites $V_{PERI} = V_{ARY} = 1.0\text{ V}$. Ex. 1008, [0042], [0105]; Ex. 1009, [0026]. Neither reference teaches that V_{ARY} is *greater* than V_{PERI} —which Apple is required to show. Apple’s argument that $V_{ARY} > V_{PERI}$ is rendered obvious by Dono’s “ $\cong$ ” symbol and Goto’s separate distinction between “=” and “ $\approx$ ” supplies no teaching—and the references’ actual ordering points the other way. Independently, Apple maps the same V_{PERI} as both the “*second voltage*” (peripheral) and the “*third voltage*” (I/O)—which is the same structural-redundancy defect that defeats Takahashi.

Any one of the foregoing—the claim-construction inconsistency, the externally-supplied operation-voltage requirement, the $VP_{PL} - VKK$ arithmetic, the failure to satisfy Claim 3’s eDP-capable element, the driver-area double-mapping, the “*comprised in the DRAM*” exclusion, the failed Tsern/Schuetz/Endo combinations, or the inverted Dono + Goto mapping—is, independently, a sufficient basis to deny institution. Together, they leave Apple far short of the reasonable-likelihood threshold. The Petition should be denied.

II. CLAIM CONSTRUCTION

Patent Owner’s position is that no claim term of the ’652 Patent requires construction and that 35 U.S.C. § 112 ¶ 6 does not govern any term of the Challenged Claims. Solely for purposes of this Preliminary Response, however, Patent Owner

applies the claim-construction positions adopted by Petitioner in the Petition, as discussed herein.

III. LEVEL OF ORDINARY SKILL IN THE ART

For the purposes of this Preliminary Response only, Patent Owner applies Petitioner's definition of a person of ordinary skill in the art (POSITA). Pet. at 11-12. Patent Owner reserves the right to advance an alternative definition in any subsequent filing should the Board institute review.

IV. PETITIONER HAS NOT DEMONSTRATED A REASONABLE LIKELIHOOD OF SUCCESS, AND THE PETITION SHOULD BE DENIED

Obviousness rests on factual determinations including the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question is whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983). Failure to identify the differences between the claimed subject matter and the prior art is fatal to an obviousness challenge. See *Apple, Inc. v. Contentguard Holdings, Inc.*, IPR2015-00355, Paper 9 at 9–10 (P.T.A.B. June 26, 2015).

The Board must support the conclusion that a POSITA not only could have made, but *would have* been motivated to combine the prior art references in the way

the claim recites and reasonably expected success. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016); *L.A. Biomedical Rsch. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly & Co.*, 849 F.3d 1049, 1067 (Fed. Cir. 2017). The combinability determination requires a plausible articulated rationale. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013). “Knowledge of a problem and motivation to solve it ***are entirely different from*** motivation to combine particular references.” *Innogenetics, N.V. v. Abbott Lab’ys*, 512 F.3d 1363, 1373 (Fed. Cir. 2008) (emphasis added).

35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.104(b) require the petition to identify “*with particularity*” each claim challenged, the grounds for the challenge, and how each claim element is found in the prior art. The Board may deny petitions that fail to comply. See July 31, 2025 Memorandum from Then-Acting Director Stewart Regarding Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4). Independently, the Board may deny institution under 35 U.S.C. § 314(a). *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016). The Director has held in a precedential decision that a petitioner advancing different claim-construction positions across forums “**should explain sufficiently why the different positions are warranted**” and that failure to do so warrants denial. *Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20 at 5 (Director Nov. 3,

2025) (*precedential*) (emphasis added).

A. The Petition Should Be Denied Because Petitioner Takes Inconsistent and Improper Claim-Construction Positions Without Explanation

After filing this Petition, Apple filed an Opening Claim Construction Brief in the parallel district court litigation, *WeCrevention, Inc. v. Apple Inc.*, Case No. 7:25-cv-00458-ADA (W.D. Tex. May 6, 2026) (Ex. 2016), taking a position on the corresponding structure for “input/output [unit/circuit]” that is irreconcilable with the position Apple takes here. The disparity is unexplained, and the manner in which Apple has structured its IPR position—identifying a candidate corresponding structure while expressly reserving the right to argue (in district court) that the same specification provides no adequate structure—seeks an impermissible advisory opinion the Board has no authority to issue. Either basis warrants denial of the Petition.

1. Apple’s Inconsistent Positions Across the Two Forums

Apple’s district-court position. Apple’s Opening Claim Construction Brief proposes that “input/output [unit/circuit]” “should be construed as a § 112, ¶ 6 means-plus-function limitation,” identifies the function as “performing input and/or output functions with respect to memory,” and identifies the structure as “[I]acks sufficient structure (indefinite).” Ex. 2016 at 12 (emphasis added). Apple’s

position in district court is express and unambiguous: “[t]he specification fails to disclose sufficient corresponding structure for performing input and output operations with respect to memory, much less for performing those operations within any particular voltage range.” *Id.* at 19. Indeed, Apple is emphatic: “‘input/output [unit/circuit]’ . . . merely describe[s] an operation . . . without reciting sufficient structure to achieve that operation. The patent specifications fail to offer any technical detail . . . beyond labeling a black box an ‘input/output unit.’” *Id.* at 1.

Apple’s IPR position. Apple’s Petition adopts the same § 112(f) framework and recites the same function—but here Apple identifies the corresponding structure as input/output unit 106. Pet. 4. Apple’s mapping of “input/output [unit/circuit]” to Takahashi’s driver area 204, for example, proceeds on the basis that input/output unit 106 is the corresponding structure. *See* Pet. 21.

Apple also includes two improper hedges in the Petition: (1) that the prior art applies “*regardless of whether* ‘input/output circuit’ is construed as a § 112(f) means-plus-function limitation,” and (ii) that “Petitioner is *not conceding* . . . that the ’652 Patent provides adequate structure for the ‘input/output circuit.’” Pet. at 5 (emphasis added). These hedges are the heart of Apple’s strategy: Apple asks the Board to apply prior art using “input/output unit 106” as the corresponding structure while simultaneously preserving Apple’s parallel-litigation position that no adequate corresponding structure exists in the specification.

The disparity is irreconcilable. Apple cannot simultaneously be right in both forums. To the extent § 112(f) governs, then either input/output unit 106 *is* sufficient corresponding structure (in which case Apple’s district-court indefiniteness argument fails), or it is not (in which case Apple’s IPR mapping relies on a structure Apple itself maintains is inadequate). Apple offers no explanation for this inconsistency. Apple’s express reservation that it is “***not conceding***” adequate structure (Pet. 5) is itself an admission that Apple knew, when it filed the Petition, that it was taking inconsistent positions across forums.

2. The Unexplained Inconsistency Warrants Denial Under *Revvo*, *Tesla*, and *Cambridge*, and *Terumo*

An unexplained inconsistency between a petitioner’s claim-construction positions in district court and at the Board warrants denial of institution. In *Revvo Techs., Inc.*, for example, the Director held: “**the petitioner should explain sufficiently why the different [claim construction] positions are warranted.**” See IPR2025-00632, Paper 20 at 4-5 (emphasis added). On remand, the Board again granted institution, and the Director subsequently *sua sponte* initiated review and again denied institution. *Id.*, Papers 30 (Jan. 14, 2026) and 36 (Director Jan. 26, 2026).

The Director applied *Revvo* in *Tesla, Inc. v. Intell. Ventures II LLC*, IPR2025-00340. The *Tesla* petitioner argued indefiniteness in district court but said in the IPR

that no claim term required express construction. The Director rejected the petitioner’s explanation that indefiniteness could not be raised in an IPR: “Petitioner’s statement that it cannot raise indefiniteness challenges in an *inter partes* review is not a sufficient explanation. Indeed, the statement amounts to an assertion that a petitioner should be permitted to raise inconsistent invalidity challenges in the two forums.” *Id.* Paper 18 at 3 (P.T.A.B. Nov. 5, 2025). Applying *Revvo*, the Director was express in denying institution in *Tesla*: “[a]llowing a petitioner to advance a claim construction before the Board when that petitioner has made inconsistent indefiniteness arguments in district court fails to further, but instead detracts from, the Office’s goal of ‘providing greater predictability and certainty in the patent system.’” *Id.* at 4 (citing *Revvo*, IPR2025-00632, Paper 20 at 4-5; 83 Fed. Reg. at 51,342–43; *see also Cambridge Mobile Telematics, Inc. v. Sfara, Inc.*, IPR2024-00952, Paper 12 at 8 (P.T.A.B. Dec. 13, 2024) (“[a]t a minimum, the Petition should have explained why the plain and ordinary meaning . . . should apply in this proceeding (why the inconsistent positions are warranted) or set forth an alternative means-plus-function claim construction.”)).

Indeed, just last week the Director reaffirmed the policy reasons why petitioners are precluded from taking inconsistent positions on claim construction in an IPR and in district court. In *Terumo BCT Inc. v. Haemonetics Corp.*, the petitioner argued that the claims “need no construction” and advanced a plain and ordinary

meaning for all claim terms, but then after institution, Petitioner argued in district court that certain claims of the each of the challenged patents are indefinite. IPR2025-0139, Paper 23 at 3-4 (P.T.A.B. May 12, 2026). The Director vacated institution in *Terumo*, and his reasoning was expressly clear: “Petitioner knew that, consistent with Board precedent, it cannot take different positions on claim construction in the district court and at the Board without an adequate explanation. Nonetheless, Petitioner did not heed that caution.” *Id.* at 3. Similarly here, Apple was required to “present a single construction and apply that construction consistently before the Board and the district court,” which Apple failed to do. *Id.* at 3-4 (citing *Infineon Techs. Am. Corp. v. Mosaid Techs. Corp.*, IPR2025-01456, Paper 27 at 3–4 (Director Mar. 17, 2026)). Apple’s conduct, like the petitioner in *Terumo*, “demonstrates that this dispute is less about a litigation alternative, as Congress intended, and more about inconsistent positions to gain an upper hand in the overall litigation. *Id.* at 4-5 (citing H.R. Rep. No. 112-98, at 48 (2011)).

Apple’s hedges are not a sufficient explanation. The “*regardless of whether*” § 112(f) governs hedge is a more elaborate version of the explanation *Tesla* rejected—it’s a refusal to engage the structure question disguised as alternative pleading. And Apple’s express reservation of indefiniteness rights is the opposite of an explanation: it is a candid admission that Apple is taking inconsistent positions and intends to maintain both. *Revvo* requires that Apple explain *why* the different

positions are warranted—but Apple has merely flagged the inconsistency. That is insufficient and merits denial of the Petition.

3. Apple’s Hedged Positions Independently Seek an Impermissible Advisory Opinion Under *Samsung-Uniloc*

Independent of the unexplained-inconsistency basis for denial, Apple’s structuring of its IPR position is the precise tactic the Board rejected as “improper” in *Samsung Elecs. Am., Inc. v. Uniloc 2017 LLC*. See IPR2020-00046, Paper 6 (P.T.A.B. Apr. 1, 2020). The petitioner there, like Apple here, advanced § 112(f) treatment, identified an “*assumed corresponding structure*” “in the event the Board believes the specification does disclose sufficient corresponding structure,” and applied the prior art using the “assumed” structure—while maintaining that the specification did not disclose adequate corresponding structure. The Board denied institution, holding the position “improper, because it, in effect, seeks an advisory opinion from the Board as to whether the challenged claims are indefinite under 35 U.S.C. § 112(b).” *Id.* at 6-8. As the Board explained: “[t]he purpose of a decision on institution is to make a threshold determination whether Petitioner has shown a reasonable likelihood of success on the statutory grounds set forth in § 311(a) (§§ 102 and 103), not to issue advisory opinions on how we might have ruled if given additional statutory authority.” *Id.* at 8. The Board noted that “the proper course for the Board to follow, if it cannot ascertain the scope of a claim with reasonable

certainty for purposes of assessing patentability, is to decline to institute the IPR.” *Id.* at 10 (citing *Samsung Elecs. Am., Inc. v. Prisia Eng’g Corp.*, 948 F.3d 1342, 1353 (Fed. Cir. 2020)).

Apple’s position here is materially identical. Apple identifies input/output unit 106 as the “most detailed description” of corresponding structure (Pet. 4)—pointedly not as a structure Apple concedes is sufficient. Apple’s reservation that it is “*not conceding* . . . that the ’652 Patent provides adequate structure” (Pet. 5) confirms that Apple, like the *Samsung-Uniloc* petitioner, is asking the Board to apply prior art using a structure Apple itself maintains is inadequate. And Apple’s “regardless of whether” hedge invites the advisory ruling *Samsung-Uniloc* held was improper. For this independent reason the Petition should be denied under *Samsung-Uniloc* and *Prisia*.

4. Apple’s Attempted Equivalence Showing Is Inadequate Under *Fresenius*

Independently, Apple’s prior-art mapping fails on the merits. For a means-plus-function limitation, “a challenger who seeks to demonstrate that a means-plus-function limitation was present in the prior art must prove that the corresponding structure—*or an equivalent*—was present in the prior art.” *Fresenius USA, Inc. v. Baxter Int’l, Inc.*, 582 F.3d 1288, 1299 (Fed. Cir. 2009) (emphasis added). “[U]nder § 112, ¶ 6 equivalence, functional identity is required. . . . Structural equivalence

under § 112, ¶ 6 is met only if . . . the assertedly equivalent structure performs the claimed function in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification.” *Odetics, Inc. v. Storage Tech. Corp.*, 185 F.3d 1259, 1267 (Fed. Cir. 1999); *see also Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1352 (Fed. Cir. 2015) (en banc).

Apple’s entire structural showing is a single conclusory sentence: “Takahashi discloses a level of structural detail exceeding that of the input/output unit 106 of the ’652 Patent.” Pet. 22. That is not a sufficient showing of equivalence. *Fresenius USA*, 582 F.3d at 1299. The test is whether the prior-art structure is structurally similar to the corresponding structure in substantial respects—not whether the prior-art structure purportedly has *more* detail. Apple offers no analysis of *how* Takahashi’s driver area 204 (a specific driver-amplifier circuit) is structurally similar to input/output unit 106; Apple identifies no overlapping structural features; and Apple addresses no structural differences as insubstantial. Instead, Apple’s assertion is conclusory and insufficient under the equivalence test.

The assertion is also in tension with Apple’s district-court position. Apple cannot simultaneously maintain (in district court) that input/output unit 106 is a “black box” with “no more than . . . a simple block diagram” (Ex. 2016 at 19) and rely (in this IPR) on Takahashi’s purportedly “exceeding” structural detail to supply the equivalence showing. Pet. 22. The equivalence inquiry requires structural

similarity to corresponding structure that is itself sufficient—not similarity to a structure Apple itself disclaims as a “black box.” *See Odetics*, 185 F.3d at 1267 (equivalent structure must perform the claimed function “in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification”). Apple has not made the required equivalence showing.

5. The Board Should Deny Institution in View of Apple’s Claim Construction Positions

Apple has placed itself in a corner. If Apple’s IPR position is correct (input/output unit 106 is sufficient structure), then Apple’s district-court indefiniteness argument fails and the inconsistency is unexplained. If Apple’s district-court position is correct (no adequate structure exists), then Apple’s IPR mapping uses a structure Apple itself believes is inadequate—the *Samsung-Uniloc* advisory-opinion problem. And under either position, Apple has failed to make the structural-equivalence showing *Fresenius* requires. The Board should deny institution.

B. The Takahashi-Based Grounds (1A–1D) Fail Because Takahashi’s VPPL Is Not the Externally-Supplied Sub-1.1V Voltage the Claims Require

Each Takahashi-based Ground requires Apple to identify a Takahashi voltage satisfying the requirement that the DRAM core cell be “*supplied with a first voltage*” that is “*lower than 1.1V.*” ’652 Patent, Cl. 1. Apple maps Takahashi’s VPPL—a

positive boosted voltage produced by Takahashi's on-chip VPP power supply 110. That mapping fails on the face of the '652 Patent and Takahashi: the operation voltage claimed in the '652 Patent is an externally-supplied (*e.g.*, the JEDEC voltages) at which a DRAM operates, and VPPL is not such a voltage because the DRAM of Takahashi is an embedded DRAM.

1. The '652 Patent's Operation Voltages (Including the “*first voltage*”) Are Externally-Supplied

The '652 Patent's disclosure of operation voltages is unambiguous. The specification introduces three exemplary tables—Tables I, II, and III—each described as showing “operation voltages (specified by the Joint Electron Device Engineering Council (JEDEC)) of a dynamic random access memory operating in” DDR I, DDR II, and DDR III. '652 Patent, 2:64–3:2 (Table I), 3:27–30 (Table II), 4:11–14 (Table III). Each table lists three voltages—cell, peripheral, and I/O—corresponding precisely to JEDEC's **externally-supplied** voltage rails. The patent frames its contribution against those JEDEC operation voltages: “power consumption of the dynamic random access memory of the present invention is much lower than power consumption of a dynamic random access memory operating in operation voltages specified by the Joint Electron Device Engineering Council.” *Id.*, 2:22-27. Critically, the claims recite that each circuit is “***supplied with***” its respective voltage, *id.*, Cl. 1—language that, in DRAM context, denotes voltage

provided to the chip from an external source. See, e.g., Ex. 1013 (JEDEC LPDDR3) at 83 (specifying specific VDD1, VDD2, VDDQ voltages provided to the device). The specification is “the single best guide to the meaning of a disputed term.” Phillips v. AWH Corp., 415 F.3d 1303, 1315 (Fed. Cir. 2005) (en banc) (citing Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996) (emphasis added)).

Apple adopts the same framing. Apple’s Petition opens its discussion of the patent at page 7 by anchoring “operation voltages” to the JEDEC baseline: Apple’s Petition describes JEDEC LPDDR3 as “defin[ing] several external voltages,” including VDD1, VDD2, and VDDQ for, respectively, the memory cell array, peripheral circuitry, and the I/O circuit, and then notes that the ’652 Patent’s claimed voltages purportedly “result in ‘power consumption [that]...is much lower than power consumption of the [DRAM] operating in the operation voltages specified by the [JEDEC].” Pet. 7–8 (citing ’652 Patent, 4:6–11). And Apple’s framing in the Petition is more explicit: **“A DRAM device is provided with one or more external voltages, which may be converted to internal voltages supplied to various circuits of the device.** The Low Power Double Data Rate 3 (LPDDR3) standard, published in May 2012 by the Joint Electron Device Engineering Council (JEDEC), defines several external voltages, including VDD1 (used for the memory cell array), VDD2 (used for peripheral circuitry), and VDDQ (used for the input/output (I/O)

circuit).” Pet. 7 (emphasis added). Thus, even Apple distinguishes *externally-supplied* JEDEC voltages from *internal* voltages produced from them on-chip. The ’652 Patent’s framing matches Apple’s framing, and thus renders Takahashi’s disclosures deficient.

2. Takahashi’s VPPL Voltage Is Internally Generated, Not Externally Supplied

VPPL is not an externally-supplied operation voltage because the DRAM of Takahashi is an embedded DRAM. Takahashi describes VPPL as an internal voltage that Takahashi’s own on-chip VPP power supply 110 supplies as the high-potential-side voltage of the wordline drivers in driver area 204, with a value of approximately 1.0V. Ex. 1004, [0081], [0083]–[0084], Figs. 1, 7. VPPL is therefore precisely the kind of **“internal voltage[] supplied to various circuits of the device”** that Apple’s own Pet. describes as *downstream* of the claimed operation voltage supplied to the DRAM. VPPL is not an externally-supplied operation voltage—it is the on-chip output of the operation voltage’s conversion to an internal voltage. The Examiner’s actions in the prosecution of the ’652 Patent and its parent patent’s applications confirm as much. The ’652 Patent is a continuation in the family that includes the ’017 and ’098 Patents, and the Examiner expressly invoked MPEP 2001.06(b) to confirm that “the examiner has reviewed the prior art cited in the earlier related application” such that “no separate citation of the same prior art need be made by

the applicants in the instant application.” Ex. 1002, 45 (Office Action mailed July 3, 2024). The Examiner then cited Takahashi on the record. *Id.*, 46 (Office Action mailed July 3, 2024). Yet the Examiner did not rely on Takahashi to reject any ’652 claim. *Id.*, 48 (Office Action mailed July 3, 2024); *id.*, 20 (Notice of Allowability mailed October 8, 2024). The Examiner allowed the ’652 claims with the express finding that “[t]he prior art of record does not teach or render obvious combination features or limitations recited in the independent claims 1, 2, and 3,” and identified the patentable architecture as “three distinct circuits (e.g., units) comprising a memory core unit, an I/O unit, and peripheral unit,” each “operat[ing] under distinct voltage range of less than 1.1 V.” *Id.*, 20 (Notice of Allowability mailed October 8, 2024). And in the parent ’017 and ’098 prosecutions—which are part of the ’652’s prior-art record—the Examiner expressly relied on the same Takahashi paragraphs Apple cites here for the sub-1.1 V voltage limitations. Apple’s IPR mapping does not cure that defect; it merely retries the same prior-art theory the Examiner already rejected as insufficient.

3. The Takahashi-Based Grounds Independently Fail Because Takahashi’s Voltages Are Not “*Capable to Be Applied to an Embedded Display Port (eDP)*” as Element [3.9] Requires

Element [3.9] of Claim 3 requires that “*the DRAM is capable to be applied to an embedded display port (eDP).*” ’652 Patent, Cl. 3. The eDP-capable requirement

of [3.9] traces directly to the prosecution of the '652 Patent's parents (the '017 and '098 Patents), where the claims were allowed only after the applicant amended the sole independent claim to recite an eDP-capable element and the Examiner expressly cited that element in the Reasons for Allowance. Ex. 2002 at 2–3; Ex. 2003 at 6–10; *see also* Pet. 11 (acknowledging that “[t]he claims of the '017 Patent were allowed after the applicant amended the sole independent claim to recite that ‘*the first voltage and the second voltage are capable of making the DRAM be applied to an embedded display port (eDP)*,’ and the Examiner also cited this feature in the Reasons for Allowance”) (emphasis added). Apple itself recognizes that the '652 Patent's Claim 3 “recites a similar element.” *Id.* Apple's [3.9] showing—that “a conventional memory, including Takahashi's, would be ‘capable to be applied’ as an eDP 1.3 frame buffer” (Pet. 30)—reads [3.9] out of the claim. Pet. 29–30. Apple's position, if accepted, would render the element trivially satisfied by any working DRAM, contradicting the fact that the eDP-capable element was the basis for allowance. That position cannot be correct.

The intrinsic record requires more than mere voltage compatibility. The '652 Patent's express purpose is to enable a DRAM applied to an eDP with “significantly reduced” system power consumption: “when the dynamic random access memory of the present invention is applied to an embedded display port, the present invention can make system power consumption (e.g., power consumption of a graphic

processing unit) be significantly reduced, not make power consumption of the timing controller be increased due to operation of the frame buffer, and extend battery endurance ability of a portable device.” ’652 Patent, 4:65–5:7. The applicant identified that “the operation voltages specified by [JEDEC] cannot satisfy requirements (that is, the low operation power consumption and the low standby power consumption) of the embedded display port (eDP) version 1.3.” *Id.*, 3:22–27. The “*capable to be applied*” language thus does not encompass any DRAM that happens to function; the intrinsic record ties the eDP-capable element to voltages that reduce system power consumption relative to older JEDEC operation voltages. Takahashi’s system-LSI architecture, optimized for high-speed operation, is designed for the opposite purpose. Ex. X1004, [0078], [0082].

Apple’s fallback—that voltages “< 1.1 V” are necessarily “capable” per the ’652 Patent’s own framing, such that Takahashi’s sub-1.1V voltages necessarily satisfy [3.9] (Pet. 30 (citing ’652 Patent, 4:62–5:10))—is circular. The ’652 Patent describes the inventor’s voltages as below 1.1V and as suitable for eDP; the ’652 Patent does not say that every sub-1.1V DRAM is necessarily eDP-capable. That converse does not follow from the spec. And as established in §§ IV.B.1–IV.B.3, Takahashi’s voltages are not externally supplied (VPPL is an internal voltage downstream of VDD, and is the only Takahashi voltage Apple maps as the “*first voltage*”). Apple’s reliance on *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672

F.3d 1335 (Fed. Cir. 2012), and *In re Giannelli*, 739 F.3d 1375 (Fed. Cir. 2014) (Pet. 30), is misplaced: both cases involved “capable of” constructions for very different technologies (*i.e.*, mechanical devices) and arose against entirely different prosecution contexts. Where—as here—an element traces to an amendment that was the basis for the Examiner’s allowance in the parent prosecution and that disclaimer is inherited by the continuation, the element must be given meaning. *See Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) (“claims are interpreted with an eye toward giving effect to all terms in the claim”). Apple’s reading impermissibly reads [3.9] out of the claim.

C. The Takahashi-Based Grounds (1A–1D) Fail Independently Because Apple’s Mapping Requires Driver Area 204 to Function Simultaneously as Both the Separately Claimed “Peripheral Circuit” and “Input/Output Circuit”

Apple’s Takahashi-based mapping fails for an additional, independent reason: it requires Takahashi’s driver area 204 to simultaneously perform both functions of two structurally distinct claimed circuits—*i.e.*, the “*peripheral circuit*” and the “*input/output circuit*.” The claims, the prosecution history (including that of the ’017 and ’098 parent Patents), and Apple’s own admissions foreclose that double-mapping.

1. The Claims Require a Structurally Distinct “Peripheral Circuit” and “Input/Output Circuits”

Claim 5, for example, which depends from Claim 3, recites both “*a peripheral*

circuit comprised in the DRAM” and “*an input/output circuit comprised in the DRAM,*” each “*supplied with*” and “*operating at*” its own separate voltage. ’652 Patent, Cls. 3, 5. The two circuits are recited as separate, structurally distinct claim elements. The claims further require the peripheral and I/O voltages to each be different from the cell voltage, and under the patent’s embodiments, the peripheral and I/O voltages are also different from each other. *See, e.g., id.*, Tables I–III; Ex. 1013 at 83. The ’652 Patent does not disclose the peripheral and input/output circuits as a single circuit “supplied with” and “operating at” two different voltages simultaneously.

2. Apple’s Mapping of the “Peripheral Circuit” and “Input/Output Circuit” to Driver Area 204 Is Defective

Apple’s mapping for Claim 5, for example, maps Takahashi’s driver area 204 to the input/output element (in Grounds 1A and 1C) and again to the peripheral element (in Grounds 1B and 1D). Pet. 21-23. In Grounds 1A and 1C, Apple maps driver area 204 to the input/output role: “in the context of embedded DRAMs like Takahashi’s, the driver area 204 constitutes an input/output circuit.” Pet. 21 (citing Ex. 1003, 76). Apple then concedes that “in an embedded DRAM which may lack off-chip I/O circuitry, the driver area 204 performs the function of receiving external inputs.” *Id.* For Claim 5 in Ground 1A, Apple then must locate a separate peripheral circuit; Apple identifies sense amplifier area 103, a portion of driver area 204, and

logic circuit 105 as candidate peripheral circuits. *Id.* 31–33. But Apple cannot have driver area 204 do double duty as both the claimed “*input/output circuit*” and as the claimed “*peripheral circuit*,” and logic circuit 105 is excluded from the DRAM (§ IV.D, *infra*), leaving only sense amplifier area 103 within the DRAM as a candidate peripheral structure—a structure that operates at the same VDD voltage as the I/O role Apple ascribes to driver area 204. *Id.* 24–25, 34–35; Ex. 1004, [0052], [0055]–[0056]. In Grounds 1B and 1D, Apple takes the opposite mapping—driver area 204 as peripheral, with Tsern’s external I/O interface imported to fill the input/output role (Pet. 22–23, 39–43)—but Tsern’s interface cannot be inserted into Takahashi’s DRAM without re-architecting Takahashi (§ IV.E.1, *infra*). Apple’s mapping is foreclosed by its own contention that: “the driver area 204 would be understood by a POSITA as a peripheral circuit *or* as an input/output circuit. EX1003, 81. Consistent with this understanding, in Grounds 1A and 1C, Petitioner applies the driver area 204 as an input/output circuit. In Grounds 1B and 1D, Petitioner alternatively applies the driver area 204 as a peripheral circuit and not as an input/output circuit.” Pet. 22. But the claims do not claim a “peripheral circuit” *or* an “*input/output circuit*”—the claims require **both** of those circuits. *See, e.g.*, Cls. 3 and 6. Thus, the Takahashi-based Grounds fail for this independent reason. Indeed, Apple’s own concession that Takahashi’s disclosures “**may lack off-chip I/O circuitry**” as a hedge (Pet. 21) confirm the fatal defect in Apple’s read. Thus, the

Takahashi-based Grounds 1A–1D should be denied for failure to identify Takahashi structures satisfying both the peripheral and I/O claim limitations of the '652 Patent.

D. The Takahashi-Based Grounds Also Fail Because the Mapping for “*Comprised in the DRAM*” Excludes Takahashi’s Logic Circuit 105—Closing Apple’s Attempt to Avoid the Double-Mapping in § IV.C

The '652 Patent’s claims require both the “*peripheral circuit*” and the “*input/output circuit*” to be “*comprised in the DRAM.*” '652 Patent, Cls. 3, 6. To escape the double-mapping defect identified in § IV.C, Apple alternatively reassigns Takahashi’s driver area 204 to the input/output element for Claim 3 and maps the peripheral element to “the ‘sense amplifier area 103’ . . . and/or at least a portion of the ‘logic circuit 105 serving as a peripheral circuit of the semiconductor memory circuit 201’ (e.g., the ‘address decoder of the semiconductor memory circuit’).” Pet. 60 ([5.1]). That mapping, however, fails because Takahashi structurally places logic circuit 105 **outside** its semiconductor memory circuit 201—Apple’s mapped DRAM—and does map to any other structures of Takahashi that purported perform the claimed peripheral functions.

Takahashi’s disclosure is express: “The semiconductor integrated device 200 includes the semiconductor memory circuit 201 *and* the logic circuit 105.” Ex. 1004, [0078] (emphasis added). Semiconductor memory circuit 201—Apple’s mapped DRAM—is itself defined to include only “a cell array area 202, the sense amplifier

area 103, and a driver area 204.” *Id.*, [0079]; Fig. 7. Logic circuit 105 is *not* among them; Takahashi enumerates it as a separate element of the broader semiconductor integrated device 200. *Id.*, [0078]. Under any reading of “*comprised in the DRAM*,” logic circuit 105 is excluded. Grounds 1A–1D should be denied for the additional independent reason that Apple has not identified, within the DRAM, a structure structurally distinct from the peripheral circuit and satisfying the third-voltage limitation distinct from the second.

E. The Tsern, Schuette, and Endo Combinations (Grounds 1B–1D) Independently Fail

1. Takahashi + Tsern + Schuette (Ground 1B) Cannot Place a Structurally Distinct I/O Circuit Within Takahashi’s DRAM and Transposes a Board-Level Architecture Onto an On-Chip One

Ground 1B is a three-reference combination offered by Apple to purportedly supply several of the missing disclosures in Takahashi. The combination fails for multiple reasons.

Apple invokes Tsern, for example, to purportedly supply the “*input/output circuit*” disclosures that are missing in Takahashi. Pet. 39–58. Tsern describes its I/O interface as the *external* interface between a memory controller and a memory device—between separate chips, not within a single embedded DRAM. Ex. 1005 at [0034]-[0042], Fig. 1. Inserting Tsern’s interface into Takahashi creates a structural impossibility: if Apple inserts Tsern’s interface inside Takahashi’s embedded

semiconductor memory circuit 201, the modification would re-architect Takahashi to add an I/O circuit where Apple argues no such circuit need exist (Pet. 21) (“may lack off-chip I/O circuitry”). If Apple instead places the interface outside semiconductor memory circuit 201—*e.g.*, in logic block 105—the resulting I/O circuit fails the “*comprised in the DRAM*” limitation as in § IV.D. Either way, Ground 1B fails.

Additionally, and separately, Schuette is a board-level memory module: discrete chips on a printed circuit board with discrete board-level voltage planes and diode-based voltage drops between them. Ex. 1006 at [0021], [0025], [0029], FIGS. 2–4. Takahashi is a single-chip system LSI. Ex. 1004, [0043], Fig. 1. Schuette’s voltage architecture is intrinsically board-level—physical separation between chips, physical voltage planes, discrete diode components. Applying it to Takahashi’s on-chip architecture would require either miniaturizing Schuette’s discrete components down to on-chip dimensions (a non-trivial step Apple does not address) or lifting Takahashi up to a multi-chip module (defeating Takahashi’s system-LSI purpose).

2. Takahashi + Endo (Ground 1C) Adds eDP Context Without Curing the Voltage Defects

Endo provides eDP context but specifies no DRAM voltage levels and no internal DRAM core, peripheral, or I/O voltages. Ex. 1007 at [0034]–[0035]. The voltage values come from Takahashi. The Takahashi + Endo combination therefore

inherits all the voltage defects of §§ IV.B and IV.D and adds nothing that cures them.

**3. Takahashi + Tsern + Schuette + Endo (Ground 1D)
Suffers from All of the Defects of Ground 1A-1C
Combined**

Ground 1D stacks Endo onto the same Takahashi + Tsern + Schuette combination addressed in Ground 1B. It therefore inherits every defect identified in §§ IV.B-D, and IV.E.1–IV.E.2—none of which is cured by the addition of a fourth reference. To the contrary, the four-reference combination compounds the problem. Apple now asks the Board to credit a hypothetical device that pulls (i) a high-speed system-LSI built-in DRAM (Takahashi), (ii) an external memory-controller-to-memory-device I/O interface (Tsern), (iii) a board-level multi-chip memory module with discrete diode-based voltage drops between board-level voltage planes (Schuette), and (iv) an eDP 1.3 frame-buffer application context (Endo) into a single architecture. Each reference’s architectural premise points away from the next, and Apple offers no integrated rationale to combine all four other than the institutional admission that no single reference (or three) supplies the claimed structure or voltage levels. Where, as here, the secondary references are mutually incompatible and each is offered to plug a different hole that Apple’s lead reference fails to fill, the combination is unsupported. *See KSR Int’l*, 550 U.S. at 418 (obviousness ground requires articulated reasoning with rational underpinnings); *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984) (combination that renders prior art “inoperable for its

intended purpose” is not obvious). For all of the reasons set forth above, Ground 1D should be denied.

4. Takahashi’s System-LSI Purpose Counsels Against the Combinations

Takahashi describes itself as “a built-in DRAM of a system LSI” (Ex. 1004, [0078]), optimized for “high-speed operation” (*id.*, [0082]), and with the negative-bias VKK voltage integral to that performance (*id.*, [0084]). By contrast, eDP frame buffers prioritize low standby power—the very design constraint motivating the ’652 Patent’s sub-1.1V limitations. ’652 Patent, 1:28–53. Takahashi’s commitment to high-speed operation, accomplished through additional voltage-supply machinery that costs power, teaches away from its use as an eDP frame buffer DRAM. *See In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004); *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009).

F. The Dono + Goto Grounds (2A and 2B and Their 2A.1 and 2B.1 Variants) Fail

1. Apple’s Mapping Inverts the Voltage Relationship Required by Claims 2 and 3

Claims 2 and 3, for example, each require the first voltage (cell) to be *greater than* the third voltage (input/output). ’652 Patent, Cls. 2, 3. Apple maps Dono’s VARY as the first voltage and VPERI as the third voltage. Pet. 73–75 ([1.7]) (mapping the “fourth buffer” of level shifter 93 inside I/O circuit 90 to the third voltage VPERI). Pet. 82–86 ([1.11], [2.11], [3.8]). But Dono and Goto themselves

disclose the opposite ordering. Dono expressly describes its internal voltage relationship as “VPP>VDD>VOD>VPERI $\cong$ VARY>VSS,” with VPERI listed *first* in that descending sequence. EX1008, [0042]. Goto’s parallel disclosure points the same direction: “VPP>VDD>VPERI $\approx$ VARY.” Ex. 1009, [0026]. Dono’s specific embodiment expressly recites a DDR3 generation in which “VPERI=1.0 V” and “VARY=1.0 V”—*i.e.*, VPERI is *equal to* VARY in the specific embodiment Apple relies on. Ex. 1008, [0105]. And the only directional disclosure of any VPERI–VARY differential anywhere in Dono is the background discussion of an earlier DDR2 generation in which “VPERI=1.3 V” and “VARY=1.2 V”—*i.e.*, VPERI *greater than* VARY, the opposite of what Apple must show. Ex. 1008, [0005]. Apple’s contrary argument rests on bootstrapping Dono’s “ $\cong$ ” symbol and Goto’s separate distinction between “VPERI=VARY” and “VPERI $\approx$ VARY” to argue that VARY > VPERI is rendered obvious. Pet. 84–85 ([2.11]) (citing Ex. 1009, [0027]). But neither reference teaches that direction. Dono’s “ $\cong$ ” connotes approximate equality, not a directional inequality; Goto’s “=”/“ $\approx$ ” distinction is silent on which side of approximate equality the small differential falls. These defects in Dono and Goto are textual—the Board need only read the claim and the references’ own voltage equations to deny Grounds 2A/2A.1 and 2B/2B.1 as to Claims 2 and 3 (and Claims 4, 5, and 6 which depend on Claim 3).

2. Dono’s VARY and VPERI Are Internal Voltages, Not Externally-Supplied Operation Voltages

The Dono + Goto Grounds also all fail for the same reason that Takahashi is defective—the mapped voltages are not externally-supplied. *See, supra* § IV.B. Dono’s VARY and VPERI are *internal* voltages—outputs of internal voltage generators, generated on-chip from external supply voltages. Ex. 1008, [0023]–[0026], FIG. 3; Ex. 1009, [0026]–[0029]. As shown in § IV.B, the ’652 Patent’s operation voltage is an externally-supplied voltage (*e.g.*, as prescribed by JEDEC), and Apple’s own framing in the Petition is that internal voltages are downstream of the operation voltage. Pet. 7. On the face of Dono, the externally-supplied voltage is VDD = 1.5V or higher in DDR3 context, Ex. 1008, [0042], [0105]—above the 1.1V ceiling for the “*peripheral circuit*” and “*input/output circuit*.”

3. The Structural Defects Identified for Takahashi Apply Equally to Dono + Goto

Dono is described in DDR3 context. Ex. 1008, [0005], [0105]. DDR3 specifies external VDDQ at 1.5V—above the 1.1V ceiling and incompatible with the eDP frame-buffer purpose motivating the ’652 Patent. Ex. 1013 at 83; ’652 Patent, 1:28–53. Independently, Apple’s Dono + Goto mapping has its own structural defect: Apple maps the same Dono voltage—VPERI—to both the “*second voltage*” (peripheral) and the “*third voltage*” (input/output). Compare Pet. 73–75 ([1.7]) (mapping the “fourth buffer” of level shifter 93 inside I/O circuit 90 as

supplied with “a third voltage VPERI”) *with* Pet. 87–91 ([5.1]–[5.2]) (mapping “Dono’s peripheral circuits” as “supplied with and operate at a second voltage VPERI”). The ’652 Patent recites separate “*second voltage*” and “*third voltage*” limitations precisely because the claimed invention differentiates a peripheral-circuit operating voltage from an input/output-circuit operating voltage. Indeed, the low-voltage-eDP advancement the ’652 Patent claims rests, *inter alia*, on the ability to operate distinct DRAM circuits at distinct sub-1.1V voltages. ’652 Patent, 4:6–11, Tables I–III. Apple’s collapse of those distinct voltages into a single VPERI eliminates the differentiation of the claimed voltages. Independently again, the eDP frame-buffer purpose described in the ’652 Patent’s sub-1.1V regime is incompatible with the DDR3 context in which Dono is described. Dono’s express embodiment recites an external supply voltage of VDD = 1.5 V (EX1008, [0105])—the standard DDR3 external rail, well above the 1.1 V ceiling of the ’652 Patent’s claims. DDR3’s external VDDQ at 1.5 V is similarly above the ceiling. Ex. 1013 at 83; Ex. 1001, 1:28–53. The two architectural premises do not coexist: a Dono-based DRAM cannot be both an externally-supplied 1.5 V DDR3 device and a sub-1.1 V eDP frame buffer. Apple’s combination with Endo (Grounds 2B/2B.1) does not cure that mismatch—Endo supplies an eDP context but no DRAM voltage levels (§ IV.E.2), and Dono’s internal VARY/VPERI remain downstream of the externally-supplied 1.5 V VDD (§ IV.B and § IV.F.2 above). For these additional reasons, Grounds 2A,

2A.1, 2B, and 2B.1 should be denied.

V. CONCLUSION

For each of the foregoing reasons—any one of which is independently sufficient—Patent Owner respectfully requests that the Board deny institution.

Respectfully submitted,

Dated: May 20, 2026

By: /Vincent J. Rubino, III/
Vincent J. Rubino, III (Reg. No. 68,594)
Lead Counsel for Patent Owner
Fabricant, Rubino & Lambrianakos LLP
411 Theodore Fremd Avenue,
Suite 206 South
Rye, New York 10580
Tel. 212-257-5797
Fax. 212-257-5796
Email: vrubino@frlip.com

CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S PRELIMINARY RESPONSE has 7,630 words in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

Respectfully submitted,

May 20, 2026

By: /Vincent J. Rubino, III/
Vincent J. Rubino, III (Reg. No. 68,594)
Lead Counsel for Patent Owner
Fabricant, Rubino & Lambrianakos LLP
411 Theodore Fremd Avenue,
Suite 206 South
Rye, New York 10580
Tel. 212-257-5797
Fax. 212-257-5796
Email: vrubino@frlip.com

CERTIFICATE OF SERVICE

A copy of the foregoing Patent Owner's Preliminary Response and Exhibit
2016 have been served on Petitioner's counsel of record as follows:

Email: IPR50095-0279IP1@fr.com
W. Karl Renner
Andrew B. Patrick
Alexander Berg
Hyun Jin In
FISH & RICHARDSON P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402

Attorneys for Apple Inc.

May 20, 2026

By: /Vincent J. Rubino, III/
Vincent J. Rubino, III (Reg. No. 68,594)
Lead Counsel for Patent Owner