IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

WECREVENTION, INC. Plaintiff v. APPLE INC. Defendant	CIVIL ACTION NO. 7:25-cv-00458-ADA **JURY TRIAL DEMANDED**

APPLE'S OPENING CLAIM CONSTRUCTION BRIEF

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A	U.S. Patent No. 9,164,942	’942 Patent
B	U.S. Patent No. 9,201,834	’834 Patent
C	U.S. Patent No. 10,998,017	’017 Patent
D	U.S. Patent No. 11,894,098	’098 Patent
E	U.S. Patent No. 12,154,652	’652 Patent
F	U.S. Provisional Patent Application No. 61/768,406 File Wrapper	’406 Provisional
G	U.S. Provisional Patent Application No. 61/672,287 File Wrapper	’287 Provisional
H	Expert Declaration of Dr. R. Jacob Baker	Baker Decl.
I	Excerpt of *Memory Systems: Cache, DRAM, Disk* (2008)	
J	Excerpt of *Wiley Electrical and Electronics Engineering Dictionary* (2004)	
K	Excerpt of *Collins English Dictionary* (7th ed. 2005)	
L	Excerpt of U.S. Patent Application No. 17/213,133 File Wrapper	

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I. INTRODUCTION

The parties dispute two terms—one from each group of asserted patents. The first group, U.S. Patent Nos. 9,164,942 ("the '942 Patent") and 9,201,834 ("the '834 Patent"), concerns an allegedly improved memory module. Although the patents focus entirely on the structure and benefits of the allegedly inventive module, Plaintiff WeCrevention seeks to eliminate that module requirement from the claims entirely by ignoring the necessary structural context of the preamble. Defendant Apple's construction instead reflects that the claim—including the preamble—is the patentee's complete claimed invention, a reading the intrinsic record unambiguously and repeatedly supports.

The second group of patents, U.S. Patent Nos. 10,998,017 ("the '017 Patent"), 11,894,098 ("the '098 Patent"), and 12,154,652 ("the '652 Patent"), are directed to a type of low-voltage memory. The terms "input/output [unit/circuit]" in these patents invoke the means-plus-function doctrine, as they merely describe an operation (performing input and output operations below a specific voltage) without reciting sufficient structure to achieve that operation. The patent specifications fail to offer any technical detail on how to accomplish that input/output function, beyond labeling a black box an "input/output unit." Means-plus-function claims of this type are precisely those that courts hold indefinite for violating the most fundamental aspect of a patentee's covenant: a patentee must describe *how* its invention accomplishes a claimed function.

II. BACKGROUND

Dynamic random access memory ("DRAM") is the most common form of computer memory, used in virtually every modern electronic device. At a high level, a DRAM chip stores data in arrays of cells comprising transistors and storage cells and relies on supporting circuitry to provide power, interface with other components, and conduct read and write operations in relation to the stored data. Different regions of the chip may operate at different voltages. An organization

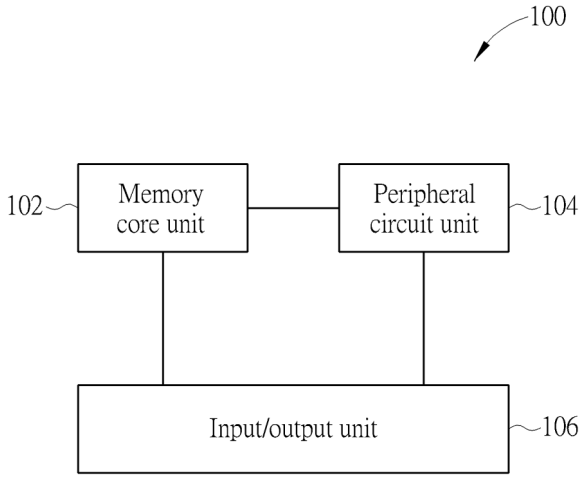
called the Joint Electron Device Engineering Council ("JEDEC") sets common industry standards regarding the design and operation of DRAM.

The Module Patents. The related '942 and '834 Patents are directed to "[reconfigurable] high speed memory chip module[s]" and electronic devices including the same. '834 Patent, cl. 1; '942 Patent, cl. 1. Both patents describe a purported invention in which multiple memory cell array integrated circuits ("ICs") are coupled to a logic unit within a memory chip module through a first transmission bus, where the logic unit converts data for transmission through a second transmission bus to an external processor. *See, e.g.*, '834 Patent, 1:60-2:6, Figs. 1, 7, 13; '942 Patent, 1:48-2:3, Figs. 1, 7, 13. These components are physically stacked in three-dimensional package structures using mechanisms such as flip-chip bonding, wire bonding, and through-silicon vias ("TSVs"). *See, e.g.*, '834 Patent, 7:9-24; '942 Patent, 4:53-67.

The Module Patents' alleged point of novelty is the inclusion of the logic unit within the unitary memory module. Accordingly, the patents frame the claimed invention in contradistinction to conventional "standard memory module[s] or chip[s]" which were interfaced with separate logic units, a configuration described as supposedly suffering from drawbacks including "poorer heat dissipation, higher power consumption and bad noise interference." '834 Patent, 1:34-57; '942 Patent, 1:26-44. The patents thus present the claimed "high speed memory chip module" as an improvement over standard memory modules, touting advantages such as "lower power consumption, lower effective greenhouse gas emission rate, higher data transmission efficiency, enhanced electromagnetic interference (EMI) shielding effect, better heat dissipation capability, and an external noise isolation function." '834 Patent, 1:25-33; '942 Patent, 1:15-25.

The Low Voltage Patents. The '017, '098, and '652 Patents are related via a sequence of continuation applications stemming from Provisional Patent Application Nos. 61/768,406 and 61/672,287. The three patents share the same substantive specification and claim DRAM including

a memory core unit, a peripheral unit, and/or an input/output unit operated at voltages below 1.1V. ’017 Patent, cls. 1-2; ’098 Patent cls. 1-9; ’652 Patent, cls. 1-6. While the purported innovation is operating these depicted units at voltages below 1.1V, *compare* ’017 Patent,[1] 3:4-14 *with* 3:34-40, 4:17-24, the disclosed structure of the input/output unit for achieving that purported innovation is no more than a block (106) in the following figure:



’017 Patent, Fig. 1. The claim construction dispute focuses on whether the patents have disclosed sufficient structure for the “input/output” units.

III. LEGAL STANDARDS

When construing claims, “[t]he construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.” *SimpleAir, Inc. v. Sony Ericsson Mobile Commc’ns AB*, 820 F.3d 419, 430 (Fed. Cir. 2016).

Limiting Preambles. “[T]erms appearing in a preamble may be deemed limitations of a claim when they give meaning to the claim and properly define the invention.” *In re Paulsen*, 30 F.3d 1475, 1479 (Fed. Cir. 1994). “Whether to treat a preamble term as a claim limitation is

[1] Because the specifications of the ’017, ’098, and ’652 Patents are substantively identical, Defendant cites to the specification of the ’017 Patent as representative of all three patents.

determined on the facts of each case in light of the claim as a whole and the invention described in the patent." *Am. Med. Sys., Inc. v. Biolitec, Inc.,* 618 F.3d 1354, 1358 (Fed. Cir. 2010). The determination of whether a preamble serves as a claim limitation is "resolved only on review of the entire[ ] . . . patent to gain an understanding of what the inventors actually invented and intended to encompass by the claim." *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257 (Fed. Cir. 1989).

While there is no "litmus test" that defines whether a preamble limits claim scope, a preamble generally limits an invention if it recites essential structure or steps or if it is "necessary to give life, meaning, and vitality" to a claim. *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002); *Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1357 (Fed. Cir. 2012) (quoting *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 128 F.3d 1298, 1305 (Fed. Cir. 1999)). Further, a preamble that is "essential to understand limitations or terms in the claim body" or that recites "additional structure or steps underscored as important by the specification" may limit claim scope. *Catalina*, 289 F.3d at 808.

Functional Claiming. By enacting 35 U.S.C. § 112 ¶ 6,[2] Congress allowed, but importantly limited, reciting generic structure for performing a function: "In enacting this provision, Congress struck a balance . . . by restricting the scope of coverage to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347-48 (Fed. Cir. 2015). Thus, by limiting the claim to structures disclosed in the patent and their equivalents, such claims would cover what an inventor contemplated as their invention without blocking innovation of new

[2] For each of the asserted claims, depending on the priority date conferred, either pre–AIA 35 U.S.C. § 112 ¶ 6 (before March 16, 2013) or AIA 35 U.S.C. §112(f) (on or after March 16, 2013) governs. Regardless, both provisions codify the same means-plus-function doctrine.

ways to perform the claimed function. Where the patentee fails to disclose any corresponding structure, this bargain fails entirely. Accordingly, "[i]f the patentee fails to disclose adequate corresponding structure, the claim is indefinite." *Id.* at 1352. Indeed, the Federal Circuit provides that "[i]f the specification is not clear as to the structure that the patentee intends to correspond to the claimed function, then the patentee has not paid the price but is attempting to claim in functional terms unbounded by any reference to structure in the specification." *Biomedino, LLC v. Waters Techs. Corp.*, 490 F.3d 946, 948 (Fed. Cir. 2007).

Williamson explains the legal framework that enforces this bargain. The first question is whether § 112 ¶ 6 applies, for which "[t]he standard is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Williamson*, 792 F.3d at 1349. When a claim term recites the word "means," there is a rebuttable presumption that § 112 ¶ 6 applies. *Id.* And, while a converse rebuttable presumption applies "[w]hen a claim term lacks the word 'means,' the presumption can be overcome and § 112, para. 6 will apply if the challenger demonstrates that the claim term fails to 'recite sufficiently definite structure' or else recites 'function without reciting sufficient structure for performing that function.'" *Id.* Importantly, "[t]he question is not whether a claim term recites any structure but whether it recites sufficient structure—a claim term is subject to § 112(f) if it recites function without reciting sufficient structure for performing that function." *Egenera, Inc. v. Cisco Sys., Inc.*, 972 F.3d 1367, 1374 (Fed. Cir. 2020).

If § 112 ¶ 6 applies, the term must be construed according to a two-step process. "The court must first identify the claimed function. Then, the court must determine what structure, if any, disclosed in the specification, corresponds to the claimed function . . . If the patentee fails to disclose adequate corresponding structure, the claim is indefinite." *Williamson*, 792 F.3d at 1351-52 (internal citations omitted).

IV. DISPUTED TERMS FOR CONSTRUCTION

A. "[reconfigurable] high speed memory chip module"

Terms/Claims	Plaintiff WeCrevention's Proposal	Defendant Apple's Proposal
"high speed memory chip module" '942 Patent, cls. 1, 5–9, and 19.	Plain and ordinary meaning; preamble is not limiting	Plain and ordinary meaning; preamble is limiting
"reconfigurable[3] high speed memory chip module" '834 Patent, cls. 1, 2, 4, and 21.	Plain and ordinary meaning; preamble is not limiting	Plain and ordinary meaning; preamble is limiting

The preamble of the claims of the Module Patents limits their scope to a "module." Claim 1 of the '834 Patent is representative:

> 1. A ***reconfigurable high speed memory chip module***, comprising
>
> a type of memory cell array group, wherein the type of memory cell array group comprises multiple memory cell array integrated circuits (ICs);
>
> a first transmission bus coupled to the type of memory cell array group having a first programmable transmitting or receiving data rate, a first programmable transmitting or receiving signal swing;
>
> a second transmission bus coupled to the logic unit having a second programmable transmitting or receiving data rate, a second programmable transmitting or receiving signal swing; and
>
> a logic unit coupled to the first transmission bus for accessing the type of memory cell array group through the first transmission bus, and further used for converting a first set of parallel data of the first transmission bus into a second set of parallel data through the second transmission bus.

[3] The preambles of the '834 Patent differ from those of the '942 Patent by adding the term "reconfigurable" to the "high speed memory chip module" term. Both versions of the preamble are limiting for the same reasons set forth *infra*.

’834 Patent, cl. 1 (emphasis added). Both intrinsic and extrinsic evidence confirm that the patentee deemed a high speed memory chip module to be the purported invention, and further that the chip module recited in the preamble is a structural element necessary to give proper context to the claim body. The Court should therefore construe the preamble as limiting.

1. The Specifications Demonstrate that a “[Reconfigurable] High Speed Memory Chip Module” is the Claimed Invention

Review of “the entirety of the patent” makes clear that the preamble phrase “high speed memory chip module” contains the core of what the inventors “actually invented and intended to encompass by the claims,” *Corning*, 868 F.2d at 1257, and so the preamble should be limiting.

The Module Patents’ descriptions of the prior art and the problems the inventors sought to solve are particularly relevant here. For example, the specifications present the Module Patents’ purported invention as an improvement over prior art “standard memory module[s] or chip[s],” which the patents disparage as having numerous undesirable attributes, such as “lower manufacturability,” “less flexibility,” “higher system migration cost,” “poorer heat dissipation,” “higher power consumption,” and “bad noise interference.” *See, e.g.*, ’942 Patent, 1:35-44; ’834 Patent, 1:43-57. The patents distinguish the alleged invention as a “high speed memory chip module” or an “electronics system device with a high speed memory chip module.” *See, e.g.*, ’942 Patent, 1:16-25; ’834 Patent, 1:25-33. The patents tout the benefits of these “high speed memory chip modules” in direct contrast to the qualities of standard memories; among other benefits, they have “lower cost, higher manufacturability, less technology migration effort, wider application ranges and higher overall performance.” ’834 Patent, 2:38-40; *see also* ’834 Patent, 1:35-39; 13:62-14:16; ’942 Patent, 1:27-31, 8:64-9:16. This distinction throughout the specification between “high speed” and “standard” memory chip modules makes clear that the “inventors were working on the particular problem [of high speed memory chip modules] and not general improvements to all [memory containing] systems.” *See Gen. Elec. Co. v. Nintendo Co.*, 179 F.3d

1350, 1361-62 (Fed. Cir. 1999) (limiting claim scope to a "raster scanned display device" rather than all display systems in view of specification's focus on the prior art problem of displaying binary data on a raster scan display device); *see also* Baker Decl. at ¶ 41. Put another way, without the preamble, the claims would fail to inform a POSA of the actual scope of the purported invention, which is an improvement to the specific field of memory chip modules in the form of a high speed memory chip module. S*ee Corning*, 868 F.2d at 1257 (in view of specification, limiting claim scope to "particular problem of an effective optical communication system not on general improvements in conventional optical fibers").

The importance of the preamble in defining the invention is further underscored by the patents' repeated and consistent use of the phrase "[reconfigurable] high speed memory chip module." The Federal Circuit has held terms in a preamble to be limiting where the use of the term throughout the specification makes clear that the inventor considered that language to be "an important characteristic of the claimed invention." *Poly-Am., L.P. v. GSE Lining Tech., Inc.*, 383 F.3d 1303, 1310 (Fed. Cir. 2004). In *Poly-America*, the preamble phrase "blown-film" was limiting because the "specification [was] replete with references to the invention as a 'blown-film' liner, including the title of the patent itself and the 'Summary of the Invention'" and the phrase was "used repeatedly to describe the preferred embodiments." *Id.* Here, the specifications' use of the preamble language shows that the inventors considered a "[reconfigurable] ***high speed memory chip module***" to be a critical and defining characteristic of the claimed invention in contrast with prior art modules. As in *Poly-America*, the specifications are similarly "replete" with the preamble term "[reconfigurable] high speed memory chip module," used throughout every facet of the patent including the titles, the abstracts, the field of the invention, and the body of the specifications in describing each of the embodiments. *See, e.g.*, '942 Patent, Title, Abstract, 1:17-25, 1:48-2:57, 3:36-37, 8:64-67; '834 Patent, Title, Abstract, 1:25-33, 1:61-2:54, 3:40-41, 5:59-63, 13:62-65. A

keyword search of the term "high speed memory chip module" reveals that the '942 Patent specification uses the term nearly fifty times.[4] Given such repeated emphasis, the preamble here "does not state a purpose or an intended use of the invention, but rather discloses a fundamental characteristic of the claimed invention that is properly construed as a limitation of the claim itself." *Poly-Am.*, 383 F.3d at 1310; *see also* Baker Decl. at ¶ 42.

2. The Preambles Supply Structural Context Missing from the Claims

The preambles are also limiting because the phrase "[reconfigurable] high speed memory chip module" supplies fundamental structure required by the body of the claims. In contrast to non-limiting preambles that do no more than "state a purpose or intended use" for an otherwise "structurally complete invention [defined] in the claim body," here the preamble describes a "fundamental characteristic of the claimed invention that informs one of skill in the art as to the structure required by the claim." *See Deere*, 703 F.3d at 1358 (quoting *Poly-Am.*, 383 F.3d at 1310). The claims are thus directed to a memory chip module (as recited in the preamble) comprising associated circuitry (recited in the claims), rather than a dissociated set of computing components.

Consistent with the plain and ordinary meaning of the claims when read as a whole, the Module Patents make clear that a memory chip module is—as the word "module" itself indicates—a self-contained unit including one or more memory chips and associated circuitry. Each of the patents' diagrams that include a "high speed memory chip module 100" depict that module as a

[4] The '834 Patent, which is a continuation-in-part of the '942 Patent, uses the term "high speed memory chip module" in the specification over sixty times. The applicant purposefully changed the patent's title to make clear that the purported invention is directed to a "reconfigurable high speed memory chip module," consistent with the preamble of every independent claim of the '834 Patent. '834 Patent at Cover, cls. 1-21.

standalone unit connected to the external ASIC or SOC processor 112 through a transmission bus 110:

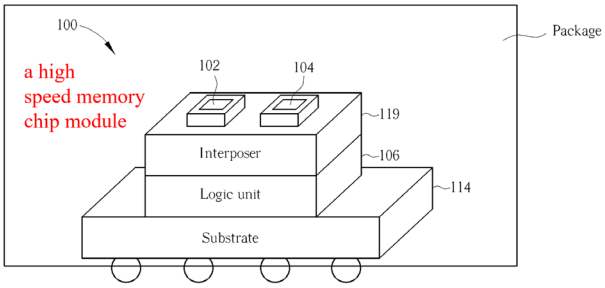


FIG. 6

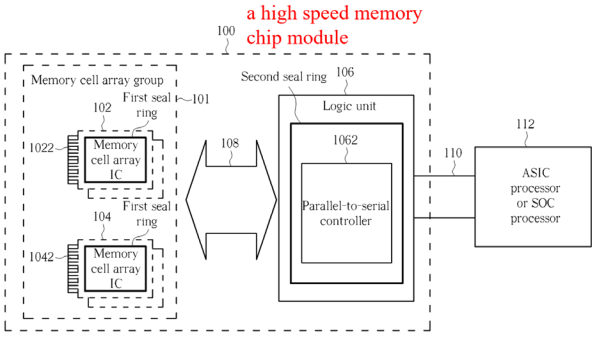


FIG. 7

’834 Patent, Figs. 6, 7 (annotated in red); *see also* ’834 Patent, Figs. 1-5, 13; ’942 Patent, Figs. 1-7, 13.

As the specifications of the Module Patents make clear, the characteristics flowing from the modularity of the invention are among the key aspects of the invention. For example, the specifications highlight “high manufacturability” and “less technology migration effort” as advantages of the invention and emphasize that the memory chip module can be used with “various ASIC processors.” *See, e.g.*, ’834 Patent, 2:23-42 (“The high speed memory chip module and the electronics system device have advantages at least as follows: . . . higher manufacturability, [and] less technology migration effort . . . . Those embodiments can be applied to various ASIC processors (or various SOC processors)”), 6:23-29 (“The high speed memory chip module 100 not only can be applied to various ASIC processors (or various SOC processors), but can also reduce cost of the high speed memory chip module 100 and enhance the performance of the high speed memory chip module 100 without bearing the unwanted inventory cost of different configuration of memory chip modules.”); *see also, e.g.*, ’942 Patent, 2:22-42, 6:23-39. As Apple’s expert Dr. Baker explains, a person of ordinary skill in the art would have understood that constructing a memory element as a self-contained and interchangeable unit (*i.e.*, a module) would lead to these

highlighted benefits and enable the invention to be readily incorporated into various systems for use with a variety of ASIC processors or SOCs. *See* Baker Decl. at ¶¶ 41, 43-44.

Extrinsic evidence further confirms that the term "module" imparts structural context to the rest of the claim. As Dr. Baker explains, a person of skill at the time would have understood "memory chip module" according to its plain and ordinary meaning as an interchangeable unit, which was typically provided as a circuit board with a handful of DRAM chips and associated circuitry attached to it. Baker Decl. at ¶¶ 43-48 (*citing* Ex. I at 315 (describing "the ubiquitous memory module" as "a small computer board (a printed circuit board, or PCB) that has a handful of chips attached to it"; Ex. J at 480 (defining "module" as "[a] self-contained and usually standardized, unit that performs one or more tasks, and which can be incorporated into a complete system" and "can be disconnected and removed as a single unit, in addition to being replaced by an equivalent"); Ex. K at 1047 (defining "module" as "a self-contained unit or item, such as an assembly of electronic components and associated wiring . . . , which itself performs a defined task and can be linked with other such units to form a larger system"). Other courts have also recognized that the plain meaning of "memory module" imparts a structural limitation on the claims. *See, e.g.*, *Netlist, Inc. v. Samsung Elec. Co.*, No. 2:22-CV-00293, Dkt. 228 at 18 (E.D. Tex. Nov. 21, 2023) (holding "memory module" in preamble limiting since term has "essential structural requirements" including "the structure necessary to connect to a memory controller"); *see also Numatics, Inc. v. Balluff, Inc.*, No. 13-11049, 2014 WL 6886354, at *6 (E.D. Mich. Dec. 4, 2014) (recognizing "customary meaning" of "module" is a "standardized and self-contained component that is separable and connectable with other components").

A construction absent the preamble is incorrect because the remaining limitations in the '834 and '942 Patent claims merely recite the elements of memory cell groups, a logic unit, and two transmission buses coupled together, but not necessarily structured as a *memory module.* For

example, under WeCrevention's proposed construction, the claimed elements could map to disparate and remote components: a "memory cell array group" in a data center, a "logic unit" in a remote device, and the "buses" being network links (*e.g.*, optical links/wireless interconnects). Accordingly, by disregarding the preambles, WeCrevention attempts to impermissibly broaden the Module Patents to capture technology far beyond the purported invention. *See* '942 Patent, 1:15-19 ("The present invention relates to a high speed memory chip module…."); '834 Patent, 1:24-27 (same). And while a preamble term may be merely descriptive when other claim elements sufficiently describe the covered concepts, *see Am. Med. Sys.*, 618 F.3d at 1359-60, that is not the case here: nothing in the claim bodies of the '834 and '942 Patents otherwise conveys this modular structure. *See* Baker Decl. at ¶ 47. The preamble here therefore breathes "life, meaning, and vitality" into the claim because no other limitations in the claims capture the modular structure imparted by "[reconfigurable] high speed memory chip module." *See Deere*, 703 F.3d at 1358 (holding preamble limiting where it was "necessary to understand the subject matter encompassed by the claim").

B. "input/output [unit/circuit]"

Terms/Claims	**Plaintiff WeCrevention's Proposal**	**Defendant Apple's Proposal**
"input/output [unit/circuit]" '017 Patent, cl. 2; '098 Patent, cls. 3 and 6; '652 Patent, cls. 1, 2 and 3.	Plain and ordinary meaning; not governed by § 112 ¶ 6 In the alternative, to the extent governed by § 112 ¶ 6: **Function:** operate at a voltage **Structure:** input/output unit 106, and structural equivalents thereof	An "input/output [unit/circuit]" should be construed as a § 112, ¶ 6 means-plus-function limitation. **Function**: performing input and/or output functions with respect to memory. **Structure**: Lacks sufficient structure (indefinite).

The patentee claims to have invented a new, low voltage memory that operates below 1.1V. *See* '017 Patent, 3:56-4:11 (describing how the claimed dynamic random access memory is superior to the prior art because it operates at less than 1.1V); *see also* Baker Decl. ¶ 39. Indeed, several claims recite a functional element—an input/output "unit" or "circuit"—that operates at the claimed lower voltages. *See* '017 Patent, cl. 2; '098 Patent, cl. 3; '652 Patent, cl. 1; Baker Decl. ¶ 53. But these purely functional recitations claim only a result, not any specific structure—*e.g.*, a unit or circuit that operates at the allegedly novel voltages. As a result, the specification's failure to provide sufficient corresponding structure explaining how a POSA would achieve such a structure apart from a single graphical box labeled "input/output unit 106" renders the input/output terms indefinite.

1. The Terms "Input/Output Unit" and "Input/Output Circuit" Invoke § 112 ¶ 6

The patentee plainly engaged in functional claiming here. The terms "input/output unit" and "input/output circuit" are generic and connote no particular structure, let alone sufficiently definite structure to perform the further recited functions (performing input/output with respect to memory at voltages lower than 1.1V). The word "unit," like the word "means," is a well-known nonce word that fails to communicate any particular structure to a POSA. The patentee's substitution of the word "circuit" for "unit" fails to avoid means-plus-function treatment for the input/output terms, especially given the specification's failure to ever mention (let alone describe) an "input/output circuit." Finally, even assuming, *arguendo*, that the claims contain *some* structure, the claims do not describe sufficient structures for performing input/output operations with respect to memory, let alone how those structures manage to do so at the claimed voltages. Accordingly, the patentee has claimed only a generic means for performing the recited functions and 35 U.S.C. § 112 ¶ 6 applies.

a) "unit" is a nonce term and "input/output unit" fails to connote sufficient structure

The term "input/output unit" is subject to means-plus-function treatment because 1) the term "unit" is a common nonce word; 2) the preceding modifier "input/output" does not connote structure; and 3) surrounding claim language adds only functional/connection details rather than describing sufficient structure as to how the element operates.

First, "unit" is a common nonce term that serves the same purpose as the word "means" in a traditional means-plus-function claim. The Federal Circuit has recognized that "the word 'unit' does not sufficiently connote structure and is similar to other terms that we have held to be nonce terms similar to 'means' and invoke § 112 ¶ 6." *Optis Cellular Tech., LLC v. Apple Inc.*, 139 F.4th 1363, 1382-83 (Fed. Cir. 2025) (finding that the term "selecting unit" invoked § 112 ¶ 6); *see also* Baker Decl. ¶ 54.

Second, the preceding phrase "input/output" does not confer structure; that phrase provides at most a functional description. While certain "adjectival qualifications" can provide sufficiently definite structure, "not just any adjectival qualification or functional language will suffice" and "[t]he proper inquiry is whether the claim limitation itself, when read in light of the specification, connotes to the ordinarily skilled artisan sufficiently definite structure for performing the identified functions." *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1364-65 (Fed. Cir. 2013), *abrogated on other grounds by Brumfield v. IBG LLC*, 97 F.4th 854 (Fed. Cir. 2024). Here, it does not; "input/output circuit" is not a term of art and would not connote sufficiently definite structure to one skilled in the art. *See* Baker Decl. ¶¶ 56-58. Instead the phrase simply specifies that the "unit" handles inputs and outputs—it does not further describe the operations it performs on those inputs/outputs (if any) or what types of inputs/outputs they are (*e.g.*, inputs and outputs for: data, control signals, addresses, clock and timing signals, power, etc.). *See* Baker Decl. ¶¶ 57-58. As a functional modifier, the phrase "input/output" unit is no different

from the modifier "selecting unit" in *Optis*, where the Federal Circuit found that the modifier characterized the functions to be accomplished and did not specify any structure showing how the unit operates. *Optis*, 139 F.4th at 1383; *see also Diebold Nixdorf, Inc. v. ITC*, 899 F.3d 1291, 1297 (Fed. Cir. 2018) (concluding that "cheque standby unit" invokes § 112 ¶ 6); *WSOU Invs. LLC v. TP-Link Tech. Co.*, No. 6:20-cv-01016-ADA, Dkt. 49 at 1 (W.D. Tex. Feb. 15, 2022) (finding § 112, ¶ 6 applies to term "automatic descriptor unit"); *WSOU Invs., LLC v. Google LLC*, No. 6:20-CV-00571-ADA, 2021 WL 11745550, at *1 (W.D. Tex. June 2, 2021) (finding § 112, ¶ 6 applies to terms "alerting unit configured to issue an alert" and "signaling unit configured to locally signal to a user"), *aff'd in part*, *rev'd in part*, No. 2022-1063, 2023 WL 6889033 (Fed. Cir. 2023) (addressing other terms).

Third, the claim terms surrounding "input/output unit" do not impart sufficient structure to avoid § 112 ¶ 6. *See* Baker Decl. ¶ 59. For example, claim 2 of the '017 Patent and claim 3 of the '652 Patent recite "wherein the input/output [unit/circuit] is electrically connected to the DRAM core cell" and "the input/output [unit/circuit] is supplied with a third voltage to make the input/output circuit operate at the third voltage, wherein the third voltage is lower than 1.1V." Neither of these additional limitations describes the structure of the claimed "input/output unit" or how that "input/output unit" would operate. *See Optis*, 139 F.4th at 1383 (requiring description of "structure showing *how* [the disputed term] operates").

Instead, the operational voltage limitation describes the voltage at which input/output operations occur, but not the structure that would allow the "input/output [unit/circuit]" to perform those operations at the claimed voltages. *See* Baker Decl. ¶ 59. WeCrevention concedes as much, by identifying "operate at a voltage" as the claimed function. The electrical connection limitation describes only what other elements connect to the input/output unit. Other claims further recite the unit's connections to other components and its location within a system but again fail to provide

any structure of the input/output [unit/circuit] itself. *See, e.g.*, '098 Patent, cl. 3 (specifying that the input/output circuit is "electrically connected to the DRAM core cell," formed on the same chip as the DRAM core cell, and "external to the DRAM core cell"); '652 Patent, cls. 1 (similar), 2 (similar). This is insufficient. *See e.g.*, *Optis*, 139 F.4th at 1383 (finding that connection between "selecting unit" and "transmitting unit" did not impart any particular structure); *see also* Baker Decl. ¶ 59. Accordingly, "input/output unit" is subject to means-plus-function treatment under 35 U.S.C. § 112 ¶ 6.

b) Substituting the word "circuit" for "unit" does not rescue the term from means-plus-function treatment

The term "input/output circuit" is subject to § 112 ¶ 6 for the same reasons that apply to "input/output unit." As an initial matter, the intrinsic record confirms that these phrases are interchangeable labels for the same component. Federal Circuit precedent also makes clear that "circuit" is not a talisman against means-plus-function treatment. And again, neither the generic modifier "input/output" nor the subsequently claimed low-voltage operation supplies sufficient structure.

The intrinsic record confirms that patentee intended "input/output circuit" to mean the same thing as "input/output unit." The specifications of the asserted patents never use the phrase "input/output circuit"; they instead refer exclusively to an "input/output unit." During prosecution, the patentee used the phrases "input/output circuit" and "input/output unit" interchangeably. Ex. L at 6. Finally, as explained above, the claims directed at "input/output unit" mirror those directed at "input/output circuit," specifying that the input/output [unit/circuit] is connected to the DRAM core cell and that it operates at a third voltage that is lower than 1.1V. *Compare* '017 Patent, cl. 2 (reciting "input/output unit") with '098 Patent, cl. 3 (reciting "input/output circuit"), '652 Patent, cl. 1 (same). Accordingly, "input/output circuit" carries no meaning beyond the patents'

descriptions of "input/output unit." *See* Baker Decl. ¶ 55. The patentee's post-hoc relabeling is semantic, not substantive.

As the Federal Circuit has recognized, such semantic changes are insufficient. The Federal Circuit has held that the word "circuit" is not a talisman that always wards off § 112 ¶ 6. *See, e.g.*, *Apex Inc. v. Raritan Comput., Inc.*, 325 F.3d 1364, 1373 (Fed. Cir. 2003) ("[W]e do not find it necessary to hold that the term 'circuit' by itself always connotes sufficient structure"). While in *Apex*, the court held that "the term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies ***some*** structural meaning" (*Id.*), "[t]he question is not whether a claim term recites ***any*** structure but whether it recites ***sufficient*** structure—a claim term is subject to § 112(f) if it recites 'function without reciting sufficient structure ***for performing that function***.'" *Egenera*, 972 F.3d at 1374 (emphasis in original) (quoting *Williamson*, 792 F.3d at 1348); *see also Power Integrations*, 711 F.3d at 1364-65 ("*Abacus* establishes that in determining whether the word 'circuit' invokes means-plus-function claiming, the pivotal issue is 'whether the [circuit limitation] as properly construed recites *sufficiently definite* structure.'") (citations omitted). Other courts have accordingly found that the term "circuit" can be subject to means-plus-function treatment. *See, e.g., Limestone Mem. Sys. LLC v. Micron Tech., Inc.*, 2019 WL 6655273, at *17-20 (C.D. Cal. Sep. 11, 2019) ("activation control circuit" subject to means-plus-function treatment); *MLR, LLC v. Kyocera Wireless Corp.*, No. CIV. 05-CV-0935-BAJB, 2006 WL 6143076, at *1 (S.D. Cal. Oct. 27, 2006) ("adaptive control circuit" subject to means-plus-function treatment).

Indeed, the Federal Circuit has previously held that the additional recitation of "circuit" does not transform an otherwise functional limitation into a structural one. In *Intelligent Automation Design, LLC v. Zimmer Biomet CMF*, the Federal Circuit was confronted with two nearly identical claim limitations: the limitation of claim 1, which was held to be means-plus-

function, and the limitation of claim 6, which additionally recited "a control circuit for" but was otherwise identical to claim 1. 799 Fed. App'x. 847, 849 (Fed. Cir. 2020). Analyzing the situation, the Federal Circuit held that although "[t]he recitation of a 'control circuit for' performing the determining function in claim 6 provides detail about how the system achieves the function," this additional recitation did not "provide enough description of the structure to render the limitation structural, rather than functional." *Id.* at 851 (citing *Power Integrations* for the proposition that not just any adjectival qualification renders a circuit limitation structural, 711 F.3d at 1364-65).

Lastly, for the same reasons provided above, neither the description of the circuit's operation in the claims, nor the adjective qualifier "input/output," confers sufficient structure on the "input/output circuit." *See supra*, § IV.A.B.1.a. All circuits, from the most complex processor to the humblest scrap of copper wire, have an input and an output. *See* Baker Decl. ¶ 57. Adding "input/output" to "circuit" fails to connote any further structure, let alone sufficient structure to explain to a POSA how to perform the claimed input/output operations with respect to memory. *See* Baker Decl. ¶¶ 56-59.

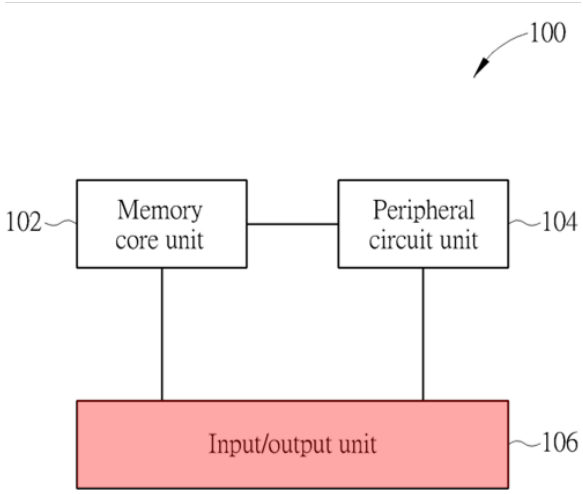
Further, the claimed "input/output circuit" must perform these input/output operations at the claimed sub-1.1V voltages. This is a technical design constraint that requires deliberate architectural choices and circuit structures. Baker Decl. ¶ 59. The word "circuit" communicates none of those choices—it does not tell a POSA what topology, logic, or signal-handling architecture enables the claimed input/output operations, much less how such operations are achieved at the low voltage levels recited in the claims. According to the patentees, operating at such low voltages is the technological advancement that the Low Voltage Patents contribute to the field. The patentee cannot simultaneously claim that sub-1.1V input/output operation is a novel advance and that the bare word "circuit" adequately conveys the structure needed to achieve it. Therefore, the phrase "input/output circuit" is also subject to § 112 ¶ 6.

2. The Specification Does Not Disclose Adequate Corresponding Structure for Performing the Claimed Functions

Because "input/output [unit/circuit]" are means-plus-function terms, "[t]he court must first identify the claimed function. Then, the court must determine what structure, if any, disclosed in the specification, corresponds to the claimed function." *Williamson*, 792 F.3d at 1351. Here, the specifications' sparse disclosures (a bare box titled "input/output unit") fail to recite sufficient structure corresponding to any identified function. *See* Baker Decl. ¶¶ 60-64.

As explained above, the function performed by the input/output unit/circuit is performing input and/or output operations with respect to memory at less than 1.1V. *See, e.g.*, '017 Patent, cl. 2; '098 Patent, cls. 3, 6; '652 Patent, cls. 1–3; Baker Decl. at ¶ 53. WeCrevention's proposal, "operate at a voltage," ignores the claim language. For example, the claims do not recite *any* unit/circuit, but rather an "input/output [unit/circuit]" that necessarily performs input and output functions. Nor do the claims recite that the unit/circuit operates at any voltage, as WeCrevention's proposal suggests—they recite an "input/output [unit/circuit]" that operates at a "third voltage [] lower than 1.1V." '017 Patent, cl. 2; '098 Patent, cls. 3, 6; '652 Patent, cls. 1-3; *see also* Baker Decl. ¶ 53.

The specification fails to disclose sufficient corresponding structure for performing input and output operations with respect to memory, much less for performing those operations within any particular voltage range. *See* Baker Decl. ¶¶ 61-62. The patents' sole figure is no more than a simple block diagram:



’017 Patent, Fig. 1 (annotated). The figure does not show any structure of the input/output unit (red) other than the connections between the input/output unit and the memory core unit and a peripheral circuit unit, respectively. The figure thus fails to describe how the unit performs input and output operations (or how those operations could be performed at less than 1.1V). *See* Baker Decl. ¶ 61. Accordingly, this “is essentially a black box that performs the recited function.” *Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1383 (Fed. Cir. 2009).

Similarly, the “Detailed Description,” shared by all patents and spanning little more than three columns, repeatedly refers to the “input/output unit” but does not describe its internal components, circuit topology, or architecture. *See* Baker Decl. ¶ 62. Instead, the written description mirrors the claims, sparsely identifying the unit’s connections to the peripheral circuit and the memory core, operating voltage, and functional result (lower power consumption). The patents contain two tables describing the invention’s operating voltage ranges. *See* ’017 Patent, 3:34-40, 4:17-24 (Tables II and III). These tables merely specify that, functionally, the input/output unit operates at voltages below 1.1V. But the written description provides no further detail on the ***structure*** that achieves the claimed functions. For example, these tables are not accompanied by any disclosure explaining what the unit or circuit is or how it achieves the claimed voltage range. *See* Baker Decl. ¶ 62.

Beyond the voltage tables, the specification provides that "[i]n addition, the input/output unit 106 is compatible with an interface provided by the prior art, so power consumption of the dynamic random access memory 100 is much lower than power consumption of the dynamic random access memory operating in the operation voltages specified by the Joint Electron Device Engineering Council." '017 Patent, 4:3-11. First, as a matter of law, it is improper for WeCrevention to rely on this assertion of backwards compatibility with prior art interfaces because "[s]imply mentioning prior art references in a patent does not suffice as a specification description." *Pressure Prods. Med. Supplies Inc. v. Greatbatch Ltd.*, 599 F.3d 1308, 1317 (Fed. Cir. 2010) ("Trial courts cannot look to the prior art, identified by nothing more than its title and citation in a patent, to provide corresponding structure for a means-plus-function limitation."). Second, even if WeCrevention could rely on this statement, this assertion of backward compatibility with unidentified prior art interfaces fails to describe the unit or circuit structure. Baker Decl. ¶ 62. The second portion of that statement, regarding lowering input/output power consumption, merely lists the desired result without specifying any structure showing *how* the unit operates. *See Optis*, 139 F.4th at 1383 (finding no structure disclosed where the patent "merely lists the functions of 'selecting unit,' and does not specify any structure showing how 'selecting unit' operates").[5]

In summary, the specification's scant disclosures regarding structure are deficient. The specification never identifies any circuit components such as transistors, buffers, drivers, receivers, level shifters, ports, or pads. It never provides a circuit schematic, topology, or architecture, nor does it disclose any algorithm or process by which the unit performs input/output operations.

[5] The disclosures in the '406 and '287 Provisionals mirror the disclosures already discussed above. *See generally* '406 Provisional, '287 Provisional; *see also* Baker Decl. ¶ 63. Accordingly, the provisionals also fail to disclose adequate structure for performing the claimed functions.

Consequently, the patents fail to explain *how* the input/output unit/circuit achieves input/output operation at sub-1.1V voltages—the purported innovation of the patents. Claiming input/output operations at lower voltages without explaining how is no different from claiming the aspiration of an electric car with a battery that uses less power. The value of a patent disclosure is explaining how an invention works, and the patents here fail to do so. *See Aristocrat Techs. Australia Pty Ltd. v. Int'l Game Tech.*, 521 F.3d 1328, 1334 (Fed. Cir. 2008) (merely "describ[ing] an outcome, not a means for achieving that outcome" is insufficient structure).

V. CONCLUSION

For the foregoing reasons, Apple respectfully requests that the Court adopt its proposed constructions.

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Respectfully Submitted,

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that, on May 6, 2026, all counsel of record who have appeared in this case are being served with a copy of the foregoing via the Court's CM/ECF system.

/s/ *Steven J. Wingard*
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