

Planarized Multilevel Interconnection Using Chemical Mechanical Polishing of Selective CVD-Al Via Plugs

Takao Amazawa, Eiichi Yamamoto, and Yoshinobu Arita

Abstract—A planarization process for selective CVD-Al via plugs using chemical mechanical polishing (CMP) is proposed and a four-level interconnection system with all stacked via plugs is demonstrated. A Cl_2/Ar post-cleaning treatment after Al plug CMP is shown to be the key process in obtaining excellent via chain characteristics with high yield and small resistance scattering. A sandwich of Ti/TiN/Ti barrier layers with a CVD-Al plug is proved to be one of the best via plug structures because of its low via resistance and high reliability. Quarter-micron 120-kG gate array LSI's have been successfully fabricated using a 1.4- μm , equal pitch and four-level interconnection.

Index Terms—Aluminum integrated circuit conductors, aluminum materials/devices, CVD, electromigration, integrated circuit metallization, interconnections, CMP

I. INTRODUCTION

VIA connection between upper- and lower-level interconnections will be a key technology in realizing future 0.1- μm ULSI's. Stacked via structures and borderless via layouts are becoming essential in reducing the interconnection pitch and increasing the packing density of LSI's [1]–[3]. Via size has to be reduced because it determines the minimum size of the interconnection pattern rule. However, the via size reduction process has some serious problems that need to be overcome. For instance, the poor reliability of conventional W via plugs due to current blocking has already become a significant problem in multilevel interconnections [4], [5]. The increase in via resistance with the reduction in via hole size can also lower the operating speeds of LSI's. Many kinds of via plugging methods using high-temperature Al-flow techniques have been proposed, but almost all of these have resulted in void formation in small Al via plugs [6]–[8]. Besides, the use of high-temperature processes above 400 °C is undesirable for low dielectric constant (low- k) organic materials, which are expected to replace conventional SiO_2 insulators in multilevel interconnections [9], [10].

In 1986, the authors reported for the first time that Al could be selectively deposited on a silicon substrate by CVD using tri-isobutyl aluminum, or TIBA, as the source gas [11], [12]. It has already been shown that this method can completely plug very small via holes only a quarter micron in diameter [13]. Se-

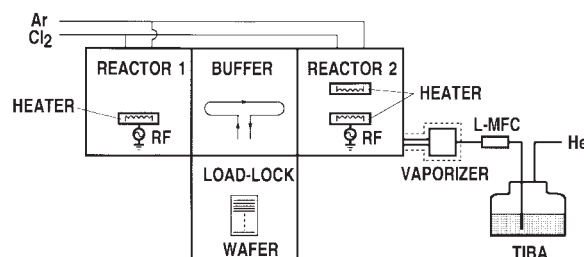


Fig. 1. Schematic diagram of multi-chamber Al-CVD system. The system consists of load-lock and buffer chambers and two reactors.

lective Al film can essentially grow only on the bottom of a via hole and very small holes are definitely plugged without voids. Recently, many researchers have reported using this approach to make contacts and vias [14]–[17]. It has a high compatibility with low- k materials because the deposition temperature can be as low as 300 °C [18]. However, the process has been found to have some drawbacks related to surface morphology. Selectively deposited plugs have sharp crystal facets and a little unevenness originating in the difference between the via depth and plug height. This unevenness degrades via connection characteristics in stacked via structures.

In this paper, a fully planarized and highly reliable new via plug process based on the chemical mechanical polishing (CMP) of selective Al CVD is presented and applied to quarter-micron LSI's with four-level interconnection.

II. PLUG PLANARIZATION PROCESS

A. Selective Al-CVD System

Selective Al plugs were formed in a production-model CVD system (Fig. 1). The system consists of load-lock and buffer chambers, and two reactors. All of the chambers were evacuated using a turbo-molecular pumping system and their ultimate pressures were in the order of 10^{-7} Torr (10^{-5} Pa). The central buffer chamber was equipped with a wafer handling arm. Reactor 1 has an infrared lamp heater and an RF stage, which are used for precleaning before Al-CVD. Al films were deposited in Reactor 2 using a double-wall CVD [12]. Double-wall CVD provided Al plugs of uniform height because high-density nuclei generated at the bottom of the via holes. The TIBA is stored in liquid form and vaporized near Reactor 2 after being supplied by a liquid mass flow controller.

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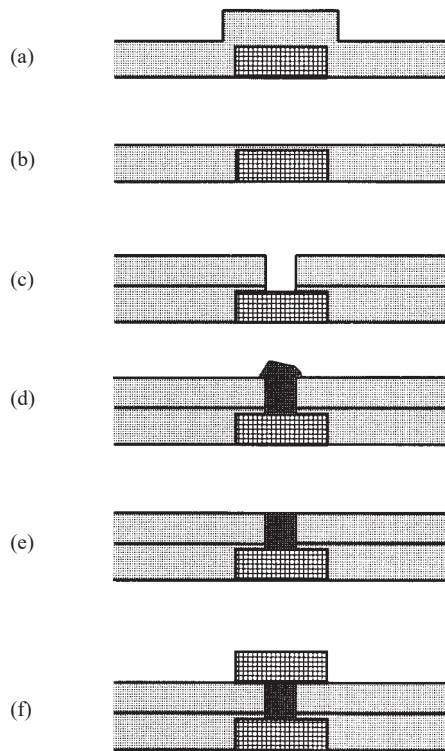


Fig. 2. Process flow for fully planarized multilevel interconnections with selective Al-CVD via plugs. Both the intermetal insulator and selective Al plugs were polished using the same CMP equipment. (a) Lower-metal patterning and insulator deposition. (b) Insulator CMP. (c) Insulator deposition and via opening. (d) Via cleaning and Al-CVD (over-deposition). (e) Al-plug CMP and post-cleaning. (f) Upper-metal deposition and patterning.

In the via plugging processes, wafer substrates after via hole opening are at first moved to Reactor 1, where they are preheated to 350 °C by an infrared lamp and the native oxide on the metal surface is precleaned by RIE with a 3% mixture of Cl_2 and Ar gas. They are then transferred to Reactor 2 and Al plugs are selectively deposited in the via holes. Typical CVD conditions are as follows: a 5-mm space between the substrate and the two heaters; front and back heater temperatures of 280 and 240 °C, respectively; and a TIBA pressure of 50 mTorr (6.7 Pa) with a liquid flow rate of 0.5 g/min. Wafers can also be cleaned just before deposition. The precleaning and Al-CVD process times for plugging holes 0.5- μm deep are about 3 min each.

B. Process Flow

Fig. 2 shows the process flow for fully planarized multilevel interconnection using the CMP of selective CVD-Al via plugs. In this process, both intermetal insulator and selective Al plugs are polished using the same CMP equipment. First, the intermetal insulator film is deposited on the lower metal pattern and planarized by CMP. The CMP slurry is an ammonia-based silica, which is commonly used for insulator CMP. After CMP, the interlayer insulator is deposited and via holes are opened. Then, Al is selectively deposited in the holes so that the holes are slightly overfilled. The overfilled Al heads are then polished under nearly the same conditions as intermetal insulator CMP. The polishing rate of SiO_2 during Al CMP

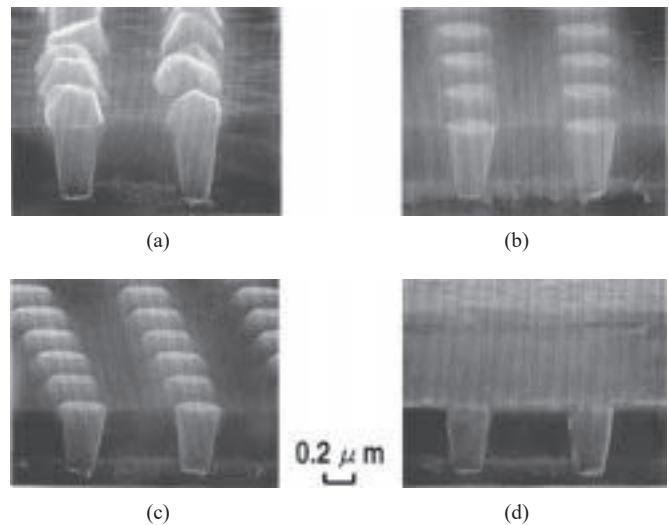


Fig. 3. SEM micrographs of Al plugs after (a) selective Al-CVD, (b) Al-plug CMP, (c) post-cleaning, and (d) upper-metal deposition.

is reduced to 35 nm/min and the Al plugs are completely planarized in one minute. The polishing rate of SiO_2 does not change due to the existence of Al plugs because the surface area of Al plugs in usual interconnection pattern is very small (under 0.1 cm^2 in a 6-inch wafer). The polishing residue on Al plugs is then cleaned by Cl_2/Ar RIE and the upper metal pattern is formed. Sputter-deposited Al alloys with Ti/TiN layers are used for the lower and upper level interconnections. Multilevel interconnection is achieved by simply repeating the above process steps.

Fig. 3 shows SEM micrographs of the Al plugs for each process step. Enough Al is deposited so that even the deepest holes can be fully plugged [Fig. 3(a)]. The Al plug is planarized by CMP [Fig. 3(b)] and the polished surface is efficiently cleaned by post-CMP cleaning [Fig. 3(c)]. There is no indentation in the upper-level metal surface [Fig. 3(d)].

The CMP process for selective CVD-Al plugs eliminates the drawbacks of both selective CVD itself and blanket CVD. Via holes with different depths can be plugged flush to the insulator surface by combining selective CVD with plug CMP. Furthermore, there is no need to be concerned about selectivity loss (i.e., deposition on SiO_2). There is no void formation which sometimes occurs with blanket CVD. The CMP of selectively formed Al plugs is very simple and it is much easier to control the polishing thickness than it is to control the thickness of blanket film.

C. Effect of CMP Post-Cleaning

Polishing is very effective in planarizing the surface, but as shown in Fig. 3(b), a small amount of residue remains on the Al plug surface. As a result, we examined post-cleaning treatment using Cl_2/Ar RIE in an R1 reactor. Fig. 4 shows the etching thickness of PECVD- SiO_2 as a function of etching time. Under these conditions, the etching rate of Al plugs was estimated to be smaller than that of SiO_2 by approximately 10–20% by measuring the steps between Al plugs and SiO_2 . The surfaces of Al plugs were always covered with a very thin aluminum oxide, the etching rate of which was much lower

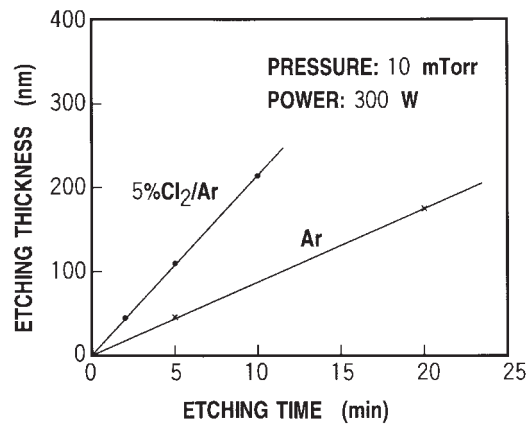


Fig. 4. Etching thickness of PE-CVD SiO₂ as a function of etching time for RIE with only Ar or 5%Cl₂/Ar.

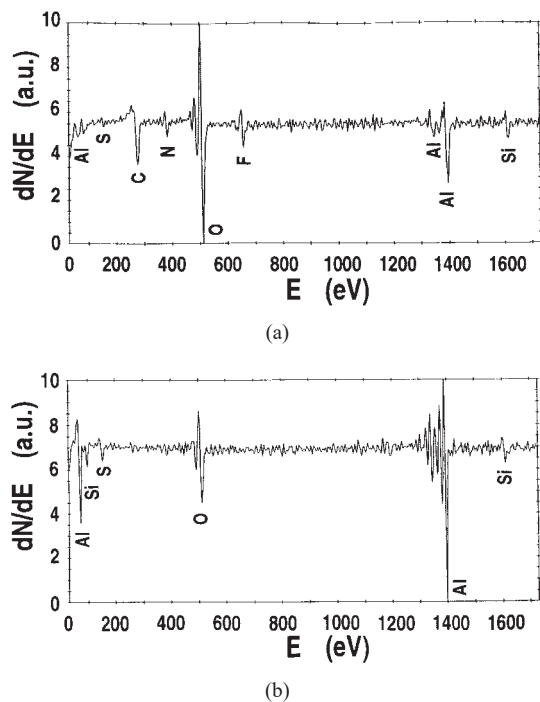


Fig. 5. Results of micro-Auger analysis of polished Al plugs before and after post-cleaning.

than Al itself in Cl₂/Ar RIE. For this reason, prior to Cl₂/Ar RIE, 10 nm of an Al-plug surface was sputter-etched using Ar gas. During CMP post-cleaning, about 50 nm of contaminated layer should be etched off. This is done in a 2-min Cl₂/Ar RIE following the Ar sputter-etch.

The results of the micro-Auger analysis of polished Al plugs 0.5- μ m in diameter before and after CMP post-cleaning are shown in Fig. 5. Many kinds of contaminants were detected on the polished Al plug surface. Oxygen, silicon and nitrogen were considered to have originated from the silica and ammonia in the slurry, and sulfur and fluorine were thought to have originated from the chemically amplified photoresist we used. These residues were removed thoroughly by the Cl₂/Ar post-cleaning treatment. The remaining peaks for silicon and oxygen were confirmed to originate from SiO₂ on the surroundings of the via plug. Fig. 6 shows cross-sectional

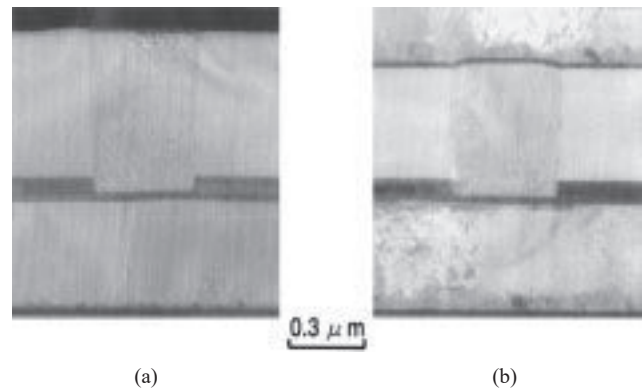


Fig. 6. Cross-sectional TEM images of Al-plugs before and after postcleaning.

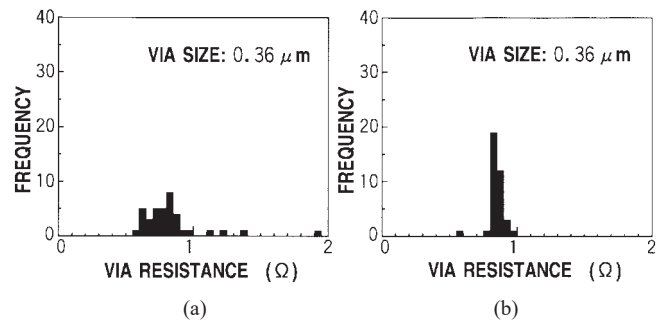


Fig. 7. Via resistance measured by the Kelvin method for CMP Al plugs (a) without and (b) with post-cleaning.

TEM images of Al plugs before and after post-cleaning. About a 50-nm thick contaminated layer, which covered the polished Al via plug surface, was completely removed by post-cleaning. The thickness of the contaminated layer can be reduced by optimizing CMP conditions.

The via resistance of two-level interconnections with and without cleaning was evaluated to clarify the effects of CMP post-cleaning. As shown in Fig. 7, the scatter of via Kelvin resistance in a wafer can clearly be reduced by post-cleaning. The yield of the 10⁵-via chain was also raised from 78% to 100% by removing the plug-CMP residue. These results confirm that post-cleaning treatment effectively improves the electrical characteristics of via connection.

III. VIA PLUG RELIABILITY

The electromigration reliability of Al plugs was evaluated using the layered and nonlayered metal structures shown in Fig. 8. The nonlayered Al plug structure in Fig. 8(a) has a Ti/TiN/Ti capping layer and a Ti wetting layer for the Al-1%Si-0.5%Cu alloy interconnection, which is sputtered at 100 °C. The via holes were opened such that the capping layer of the lower-level interconnections could not be etched during via-opening RIE. The capping layer was then etched off just before the Al-CVD under the same conditions as precleaning except for time, so there was no TiN barrier at the top or bottom of the plug. The layered Al plug structure in Fig. 8(b) employs Ti/TiN/Ti for both the capping and wetting layers. Here, only part of the Ti was removed during precleaning,

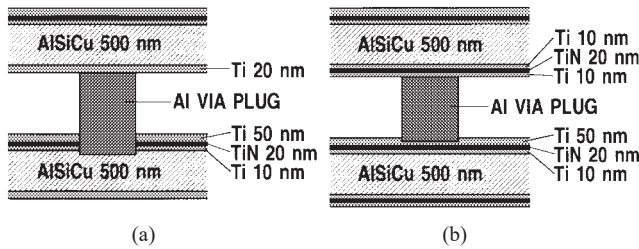


Fig. 8. Cross sections of (a) a nonlayered Al plug and (b) a layered Al plug with a TiN barrier.

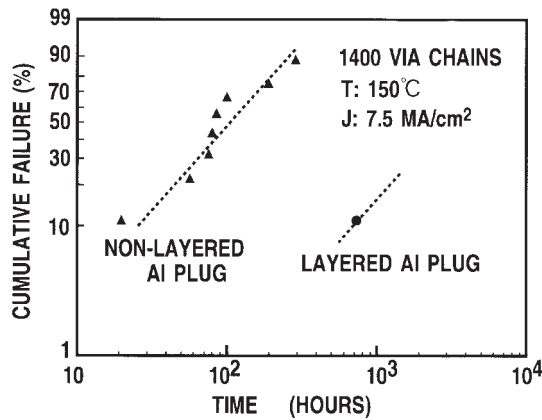


Fig. 9. Electromigration resistance of 1400 via chains for layered and non-layered Al plugs.

and the plug was sandwiched between two TiN barriers. The thickness of the TiN layers is 20 nm.

Electromigration stress testing was carried out using a serial via chain pattern with 1400 vias. The diameter of the vias was 0.36 μm , the distance between them was 2 μm , and the width of the metal line was 1.2 μm . The stress conditions were 7.5 MA/cm² for each via at a temperature of 150 °C. Fig. 9 shows the cumulative failure rate as a percentage of the total number over time for the two test structures. Many failures occurred in the via chain with nonlayered Al plugs in less than 100 h. By contrast, only one failure in eight samples occurred in the via chain with layered plugs in 750 h. The test was terminated after 1000 h.

Fig. 10 shows cross-sectional TEM images of Al plugs with layered and nonlayered structures. A grain boundary can be seen to have generated in the nonlayered Al plugs [Fig. 10(a)]. Such grain boundaries were observed when part of the grain boundary of the lower-level Al alloy was located at the bottom of the via hole. However, no grain boundaries were observed in a layered Al plug even when the plug was situated on a grain boundary in a lower-level Al alloy.

Fig. 11 shows a model to improve electromigration resistance. In nonlayered Al plugs without barrier layers, the grain boundary extends from the bottom of the via all the way through to the upper-level Al alloy on top. This occurs when a plug is situated on a grain boundary in a lower-level Al alloy. The grain boundary in an Al plug is considered to be formed during Al plug deposition. Al grows epitaxially on an Al alloy substrate, and if a grain boundary exists at the bottom of a via hole, it extends into the Al plug. It is well

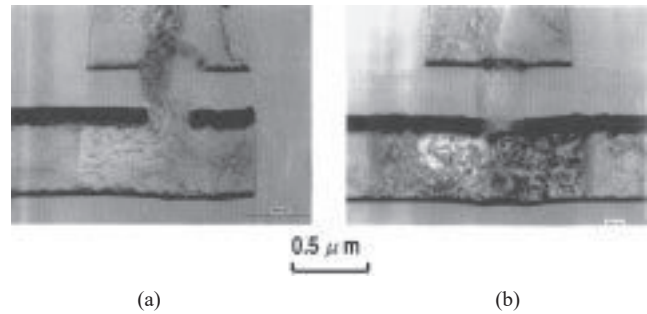


Fig. 10. Cross-sectional TEM micrographs of (a) a non-layered Al plug and (b) a layered Al-plug with a TiN barrier.

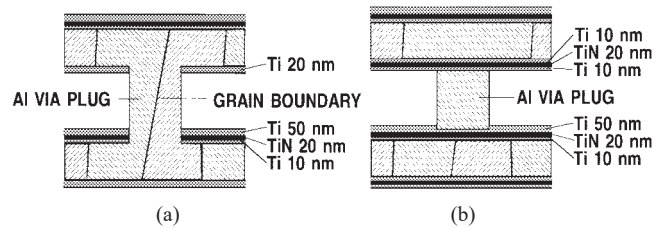


Fig. 11. The model for improved electromigration resistance. (a) A non-layered Al plug occasionally has a grain boundary. (b) A grain boundary in a lower-level Al alloy is terminated by barrier metals in a layered Al-plug structure.

known that Al atoms mainly migrate through grain boundaries during electromigration testing. If many Al plugs in a via chain have grain boundaries, Al atoms easily migrate in the via chain and electromigration resistance deteriorates. However, as shown in Fig. 11(b), the TiN barriers reduce the frequency of grain boundary generation in Al plugs. Here, the migration resistance of the via chain is greatly improved because there is hardly any migration of Al atoms in a single crystal Al plug.

Another mechanism whereby electromigration resistance is improved is when the TiN itself operates as a barrier to Al atom migration between an Al plug and Al alloy interconnection. It is generally known that the electromigration reliability of via chains with W plugs is largely affected by the blocking effect of W plugs [4]. When the distance between two vias is more than a few dozen microns, vacancies in the Al alloy interconnection collect at the lower course of the W plug and grow into a large void, which degrades electromigration reliability. However, if the Al alloy interconnection between vias is short enough, the electromigration resistance of the via chain is greatly strengthened because the W plug completely dams up the flow of Al atoms.

In our test structure, the interconnection patterns between vias were short and wide and the current density of interconnection had quite a low value (1.25 MA/cm²) compared to vias (7.5 MA/cm²). Failure analysis of electromigration samples revealed that the main cause of the failures was void formation in the Al plugs. If the blocking effect is the dominant factor affecting failure, voids should be formed in part of the interconnection near the via. Therefore, the difference in the failure time between the two structures in Fig. 9 is considered to originate from the crystal structure of the Al plug itself and we can at least conclude that the short lifetime of the nonlayered Al plug is greatly improved by a layered plug

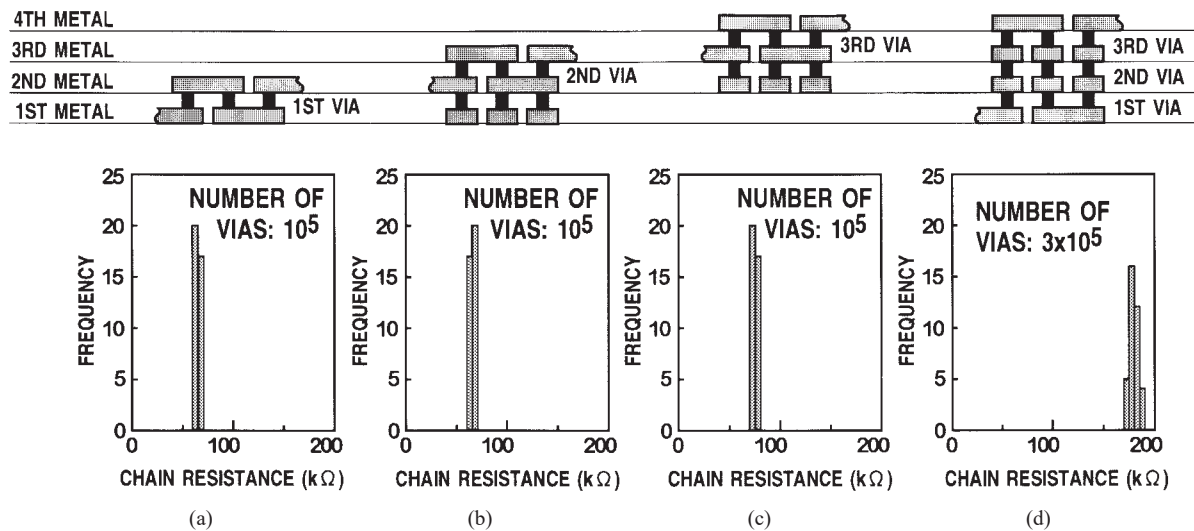


Fig. 12. Via chain resistance distributions for the (a) first, (b) second, (c) third, and (d) all stacked vias. There are 10^5 vias on each level and their diameters are $0.36 \mu\text{m}$.

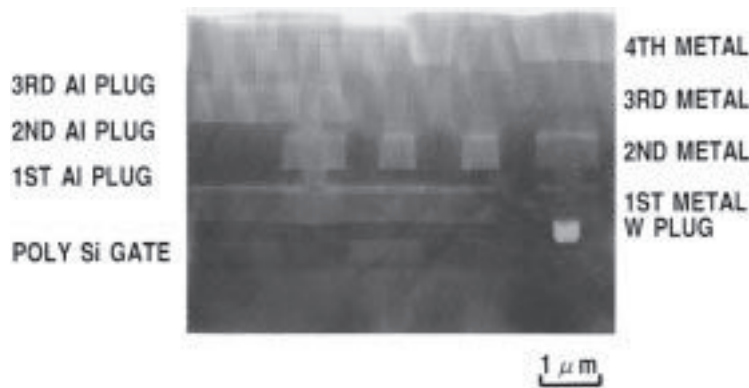


Fig. 13. SEM cross-section of four level interconnection with Al-CVD stacked via plugs applied to 120-kG gate array LSI's.

structure with a single crystal. In actual devices with narrow and long interconnections, lifetime will definitely be shortened by the blocking effect of the layered via plug structure. The degree of degradation is expected to change as a result of the structure of barrier layers especially the barrier layer thickness. This is the next subject to be discussed on layered Al plug reliability.

IV. APPLICATION TO LSIS

Fully planarized four-level interconnections were fabricated by the plug CMP process shown in Fig. 2 and their electrical characteristics were evaluated. The via chain pattern in each level interconnection was the same as that used in the electromigration test and the cross sectional views are shown in Fig. 12. The diameter and the depth of all vias were fixed at 0.36 and $0.5 \mu\text{m}$, respectively. The vias on the first level metal had a nonstacked structure, but all of those on the second and third metals had a stacked via structure with dummy vias just under all the vias. The chain resistance of the first-, second-, and third-level vias and the three-level stacks were measured individually. There were 10^5 vias in each level via chain, so the total number in the three-level stacks was three times that. The histograms show that the via chain resistance for each

level and for all-stacked vias is sufficiently small and that the distribution is very narrow. No failure could be observed in 37 chips on a 6-in wafer, and the chain resistance of a stack was about the same as that for a single level. From the chain resistance, the via resistance of one plug could be estimated to be from 0.5Ω to 0.7Ω .

Gate-array LSI's were fabricated using fully planarized four-level interconnection. All four levels had an equal pitch of $1.4 \mu\text{m}$, a via hole size of $0.36 \mu\text{m}$, a line width of $0.6 \mu\text{m}$, and a line spacing of $0.36 \mu\text{m}$. Stacked via structures were used for all four-level interconnections. Fig. 13 is a cross-sectional SEM image of a four-level interconnection in a 120-kG gate-array LSI fabricated by KrF-excimer-laser lithography and the quarter-micron-gate CMOS/SIMOX process. The polysilicon gate and all four metal layers are completely planarized and Al via plugs are all stacked. Fully functional operations were obtained in 120-kG gate-array LSI's.

V. CONCLUSION

We developed process to completely planarize Al plugs using selective Al-CVD and plug CMP. Cl_2/Ar post-cleaning treatment after CMP eliminated many kinds of contaminants on the CMP-Al plug surface, largely improved the yield, and

reduced the resistance scattering of via chains. A Ti/TiN/Ti-layered plug structure, in which Al plugs were sandwiched between TiN barriers, showed extremely high electromigration resistance. This is because the TiN barrier suppressed both grain-boundary generation and Al-atom migration in the via plug. Planarized interconnections with stacked vias exhibited excellent characteristics such as low via resistance, narrow distribution of resistances, and a high via-chain yield. Gate array VLSI's were fabricated using four-level interconnection and were confirmed to be fully functional. The CMP Al via plug with barrier layers is a promising candidate for future ULSI multilevel interconnections.

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REFERENCES

- [1] H. Shibata, N. Ikeda, M. Nagamatsu, Y. Asahi, and K. Maeguchi, "A novel zero-overlap/enclosure metal interconnection technology for high-density logic VLSI's," in *Proc. VLSI Multilevel Interconnection Conf.*, 1990, pp. 15–21.
- [2] K. Ueno, K. Ohto, K. Tsunenari, K. Kajiyana, K. Kikuta, and T. Kikkawa, "A quarter-micron planarized interconnection technology with self-aligned plug," in *IEDM Tech. Dig.*, 1992, pp. 305–308.
- [3] M. Norishima, T. Matsuno, M. B. Anand, M. Murota, M. Inohara, K. Inoue, H. Ohtani, K. Miyamoto, R. Ogawa, M. Seto, C. Fukuhara, H. Shibata, and M. Kakumu, "Fully integrated multilevel interconnect process for low cost sub-half-micron ASIC applications," in *Symp. VLSI Tech.*, 1995, pp. 47–48.
- [4] H. S. Rathore, R. G. Fillipi, R. A. Wachnik, J. J. Estabil, and T. Kwok, "Electromigration and current-carrying implications for aluminum-based metallurgy with tungsten stud-via interconnections," in *Proc. SPIE Conf.*, 1992, vol. 1805, pp. 251–252.
- [5] C. D. Graess, H. A. Le, J. W. McPherson, and R. H. Havemann, "Electromigration reliability improvement of W-plug vias by titanium layering," in *Proc. 32nd Annu. IRPS*, 1994, pp. 173–177.
- [6] H. Nishimura, T. Kouzaki, T. Yamada, R. Sinclair, and S. Ogawa, "A highly reliable high-temperature aluminum sputter metallization," in *Proc. SPIE Conf.*, 1992, vol. 1805, pp. 65–76.
- [7] G. A. Dixit, M. F. Chisholm, M. K. Jain, T. Weaver, L. M. Ting, S. Poarch, K. Mizobuchi, R. H. Havemann, C. D. Dobson, A. I. Jeffries, P. J. Holverson, P. Rich, D. C. Butler, and J. Hems, "A novel high-pressure low-temperature aluminum plug technology for sub-0.5- μm contact/via geometries," in *IEDM Tech. Dig.*, 1994, pp. 105–108.
- [8] G. Bai, C. Chiang, J. Neal Cox, S. Fang, D. S. Gardner, A. Mack, T. Marieb, X.-C. Mu, V. Ochoa, R. Villasol, and J. Yu, "Copper interconnection deposition techniques and integration," in *Symp. VLSI Tech.*, 1996, pp. 48–49.
- [9] J. Paraszczak, D. Edelstein, S. Cohen, E. Babich, and J. Hummel, "High-performance dielectrics and processes for ULSI interconnection technologies," in *IEDM Tech. Dig.*, 1993, pp. 261–264.
- [10] B. Zhao, M. A. Biberger, V. Hoffman, S.-Q. Wang, P. K. Vasudev, and T. E. Seidel, "Single step PVD planarized aluminum interconnect with low- ϵ organic ILD for high-performance and low-cost ULSI," in *Symp. VLSI Tech.*, 1996, pp. 72–73.
- [11] T. Amazawa, and H. Nakamura, "Selective chemical vapor deposition of aluminum," in *Ext. Abst. 1986 Int. Conf. Solid State Devices and Mater.*, pp. 755–756.
- [12] T. Amazawa, H. Nakamura, and Y. Arita, "Selective growth of aluminum using novel CVD system," in *IEDM Tech. Dig.*, 1988, pp. 442–445.
- [13] T. Amazawa, and Y. Arita, "A 0.25 μm via plug process using selective CVD aluminum for multilevel interconnection," in *IEDM Tech. Dig.*, 1991, pp. 265–268.
- [14] W. Y.-C. Lai, K. P. Cheung, D. P. Favreau, C. Case, R. Liu, R. G. Murray, L. F. Tz. Kwakman, and D. Huibregtse, "CVD aluminum for submicron VLSI metallization," in *Proc. VLSI Multilevel Interconnection Conf.*, 1991, pp. 89–95.
- [15] E. Kondoh, Y. Kawano, N. Takeyasu, T. Katagiri, H. Yamamoto, and T. Ohta, "Interconnection formation by simultaneous copper doping in chemical-vapor-deposited aluminum (Al-Cu CVD)," in *IEDM Tech. Dig.*, 1993, pp. 277–280.
- [16] T. Shinzawa, K. Sugai, A. Kobayashi, Y. Hayashi, T. Nakajima, S. Kishida, H. Okabayashi, T. Yako, K. Tsunenari, and Y. Murao, "Adhesion layerless submicron Al damascene interconnections using novel Al-CVD," in *Symp. VLSI Tech.*, 1994, pp. 77–78.
- [17] K. Masu, H. Matsuhashi, A. Gotoh, J.-H. Chung, M. Yokoyama, R. Tajima, Y. Fujita, and K. Tsubouchi, "Multilevel metallization based on Al CVD," in *Symp. VLSI Tech.*, 1996, pp. 44–45.
- [18] G. A. Dixit, A. Paranjpe, Q.-Zhong, L. M. Ting, J. D. Luttmer, and R. H. Havemann, "A novel 0.25- μm via plug process using low temperature CVD Al/TiN," in *IEDM Tech. Dig.*, 1995, pp. 1001–1003.



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