

Improved low frequency noise characteristics of sub-micron MOSFETs with TaSiN/TiN gate on ALD HfO₂ dielectric

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Received 9 April 2006; received in revised form 5 July 2006

Available online 2 July 2007

Abstract

Low frequency noise measurements were performed on n- and p-channel MOSFETs with TaSiN and TiN metal gates, respectively, deposited on ALD HfO₂ gate dielectric. Lower normalized current noise power spectral density is reported for these devices in comparison to poly-Si/HfO₂ devices and that yielded one order lower magnitude for extracted average effective dielectric trap density. In addition, the noise levels in PMOS devices were found to be higher than NMOSFETs and the dielectric trap distribution less dense in the upper mid-gap than the lower mid-gap region. The screened carrier scattering coefficient extracted from the noise measurements was approximately the same for metal and poly-Si high-*k* stacks but higher than that for the poly-Si SiO₂ system, implying higher Coulomb scattering effects. It is believed that the elimination of dopant penetration seen in poly-Si system and low thermal budgets for metal gate deposition helped lower the noise magnitude and yielded better mobility and effective trap density values.

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1. Introduction

Although high-*k* dielectrics decrease the gate leakage current thus allowing further down-scaling of the CMOS dimensions, there are inherent problems with using the conventional polysilicon gate on HfO₂ such as dopant diffusion, reactions at the junction with the dielectric and depletion effects. In order to circumvent these problems, researchers have gone back to exploring metal gates in conjunction with high-*k* dielectric gate stacks. Recently, energy band diagrams and current transport mechanisms for Al, Pt/HfO₂/Si structures have been reported [1]. However, Al reacts with metal oxide dielectric forming an interfacial layer while Pt is difficult to process as well as being expensive. Therefore, due to the non-feasibility of these metal

gates, alternative materials like Ta, TaN, RuO₂ have been suggested [2]. Promising results were reported as regards to device integration and characteristics with TaSiN and TiN on HfO₂ gate stacks [3–5]. Although superior noise characteristics are expected with improved carrier mobility, there are no published results on the low frequency noise of devices with these gate stacks. Low frequency noise measurements can be utilized to assess the quality of the dielectric and interfaces between the different gate stack materials [6–9], which are known to affect the carrier mobility as well as the noise characteristics.

In this paper, we present low frequency noise characteristics of MOSFETs with ALD HfO₂ gate dielectric and dual-metal gates of TiN for PMOS, and TaSiN for NMOS. Noise characteristics, dielectric trap density as well as carrier mobility and Coulomb-scattering-limited mobility parameter are evaluated and compared to those for poly-Si gate MOSFETs with SiO₂ and HfO₂ (MOCVD) dielectrics.

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2. Devices and measurements

The devices used in this work had a gate width of $\sim 10 \mu\text{m}$ with physical gate lengths varying from $0.065 \mu\text{m}$ to $0.11 \mu\text{m}$. The dielectric material used was ALD HfO_2 ($38 \text{ \AA}$ for NMOSFET and $23 \text{ \AA}$ for PMOSFET with $k \sim 19$) on SiO_2 interfacial oxide layer. The capacitance equivalent thickness (CET) in the case of n-type MOSFETs was $23.1 \text{ \AA}$ ($C_{\text{CET}} = 1.5 \times 10^{-6} \text{ F cm}^{-2}$) with a TaSiN gate (work function $\sim 4.4 \text{ eV}$), while PMOS devices had a CET of $29.5 \text{ \AA}$ ($C_{\text{CET}} = 1.05 \times 10^{-6} \text{ F cm}^{-2}$) with a TiN gate (work function $\sim 4.65 \text{ eV}$). The channel doping concentrations were $7 \times 10^{16} \text{ cm}^{-3}$ and $3 \times 10^{16} \text{ cm}^{-3}$ for NMOS and PMOS, respectively. The reference devices with poly-Si/ HfO_2 ($55 \text{ \AA}$ by MOCVD) gate stack had lengths of $0.065 \mu\text{m}$ (PMOS) and $0.11 \mu\text{m}$ (NMOS), CET of $23 \text{ \AA}$ and width of $\sim 10 \mu\text{m}$. The interfacial SiO_2 layer thickness for all the devices is believed to be $\sim 10 \text{ \AA}$.

Wafer level measurements were performed using a low noise probe station at room temperature with a custom made set-up which includes a low-noise DC biasing circuitry, an EG&G PAR113 pre-amplifier and a HP 3562A dynamic signal analyzer. Noise data were taken for a constant drain bias of $V_d = \pm 50 \text{ mV}$ in the strong inversion region. A detailed DC analysis was done using HP-4155B semiconductor parameter analyzer to obtain gate leakage current, AC conductance ($g_d = \partial I_d / \partial V_d$), transconductance ($g_m = \partial I_d / \partial V_g$), sub-threshold slope ($S = \partial \log(I_d) / \partial V_g$) and threshold voltage (V_t). The parameters, thus extracted, were used in conjunction with the measured noise magnitude to evaluate dielectric quality for metal gate transistors.

3. Results and discussion

Assuming the formation of fixed charges at the interface to be the cause of threshold shift, the fixed charge density was calculated from the measured threshold voltage using,

$$V_t = V_{\text{FB}}^0 - \frac{qN_f}{C_{\text{CET}}} \pm 2|\psi_b| \pm \frac{\sqrt{4q\epsilon_{\text{Si}}N_I|\psi_b|}}{C_{\text{CET}}} \quad (1)$$

where V_t is the measured threshold voltage (V), V_{FB}^0 is the difference in work functions between the gate material and

the Si substrate (V), N_f is the fixed charge density (cm^{-2}), C_{CET} is the equivalent oxide capacitance (F cm^{-2}), ψ_b is the bulk potential (V), N_I is the substrate doping concentration (cm^{-3}), and ϵ_{Si} is Si permittivity (F cm^{-1}). The substrate type, n or p, determines the sign in front of the last two terms in Eq. (1). With a reported magnitude of $\sim 1 \times 10^{11} \text{ cm}^{-2}$ in Table 1, the negative fixed charge density values extracted for metal-gate NMOS devices are about an order of magnitude lower than poly-Si NMOS high- k devices. As for PMOS, positive fixed charge density per unit area was also low, at $2 \times 10^{12} \text{ cm}^{-2}$, compared to $1 \times 10^{13} \text{ cm}^{-2}$ extracted for the poly-Si/ HfO_2 system [10]. The oxide/substrate interface trap density values (D_{it}) as given in Table 1 are obtained from sub-threshold slope characteristic. Since the interface trapped charge values were found to be similar for metal and poly-Si gate counterparts in both NMOS and PMOS, they would have a minimal effect on the relative fixed charge density of metal and poly-gated devices. In view of the above facts, the observed trend in the extracted fixed trap density can be better attributed to TiN or TaSiN/ HfO_2 interfaces. The model proposed in [11] for acceptor and donor interface states at poly-Si/ HfO_2 seems to hold for these metal gates as well. As Fermi level pinning due to Hf–Si bonds at the poly-Si/ HfO_2 interface was reported to be the cause for voltage shifts [12,13], a similar mechanism might be responsible for metal/ HfO_2 interface states. It should be noted here that the gate-semiconductor work function difference used in (1) might be slightly different from the actual values so that the accuracy of the absolute values for charge density is not guaranteed. Eq. (1) is used only as an indicator pointing to the presence of defect states at the metal/high- k interface.

The drain voltage noise power spectral density S_{V_d} is shown in Fig. 1 for TiN/ HfO_2 (PMOS) device biased at $V_d = -50 \text{ mV}$ and varying gate overdrive. For comparison, S_{V_d} was converted to current noise power spectral density S_{I_d} and normalized with respect to drain current, capacitance and channel length. Fig. 2 shows normalized noise power spectral density at 1 Hz for TaSiN/ HfO_2 NMOS (a) and TiN/ HfO_2 PMOS (b) devices. A comparison is made with corresponding n- and p-type poly-Si/ HfO_2 MOSFETs [10]. In Fig. 3, the data is re-plotted to compare

Table 1
Summary of extracted noise and device physical parameters

Gate material	L (μm)	C_{EOT} (F cm^{-2})	V_t (V)	μ ($\text{cm}^2/\text{V s}$)	μ_{Co} ($\text{cm}/\text{V s}$)	N_t ($\text{cm}^{-3} \text{ eV}^{-1}$)	D_{it} ($\text{cm}^{-2} \text{ eV}^{-1}$)	N_f (cm^{-2})
TiN (PMOS)	0.11	1.05×10^{-6}	-0.77	72	5.0×10^7	1.6×10^{18}	1.9×10^{12}	2.2×10^{12}
	0.095	1.05×10^{-6}	-0.80	82	4.5×10^7	9.0×10^{17}	2.0×10^{12}	2.4×10^{12}
	0.065	1.05×10^{-6}	-0.81	58	4.5×10^7	9.5×10^{17}	2.3×10^{12}	2.5×10^{12}
TaSiN (NMOS)	0.065	1.50×10^{-6}	0.30	101	7.5×10^7	1.0×10^{17}	4.7×10^{12}	-1.2×10^{11}
	0.08	1.50×10^{-6}	0.29	125	7.5×10^7	1.5×10^{17}	4.8×10^{12}	-2.7×10^{10}
	0.095	1.50×10^{-6}	0.30	137	1.0×10^8	1.7×10^{17}	3.8×10^{12}	-1.7×10^{11}
p-poly (PMOS)	0.065	1.50×10^{-6}	-1.02	33	5.0×10^7	1×10^{19}	4.4×10^{12}	1.0×10^{13}
n-poly (NMOS)	0.11	1.50×10^{-6}	0.28	131	1.5×10^8	1.4×10^{18}	3.4×10^{12}	-2.7×10^{12}

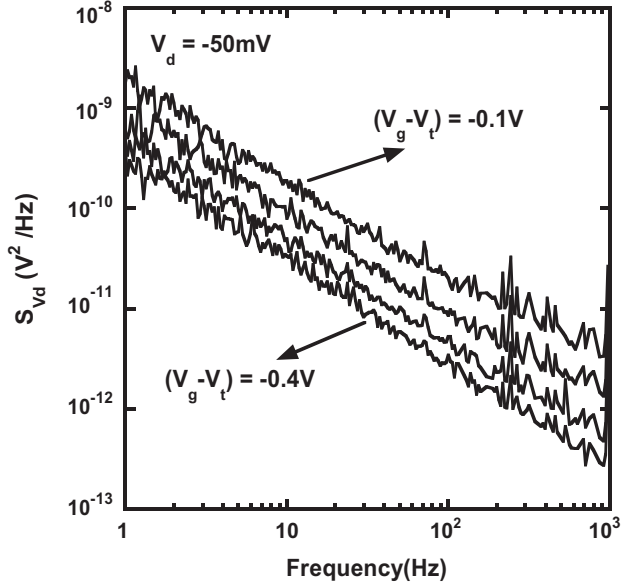


Fig. 1. Typical noise spectra for TiN/HfO₂ (PMOS) device in the inversion region at $V_d = -50$ mV and $(V_g - V_t)$ varying from -0.1 to -0.4 V in steps of -0.1 V.

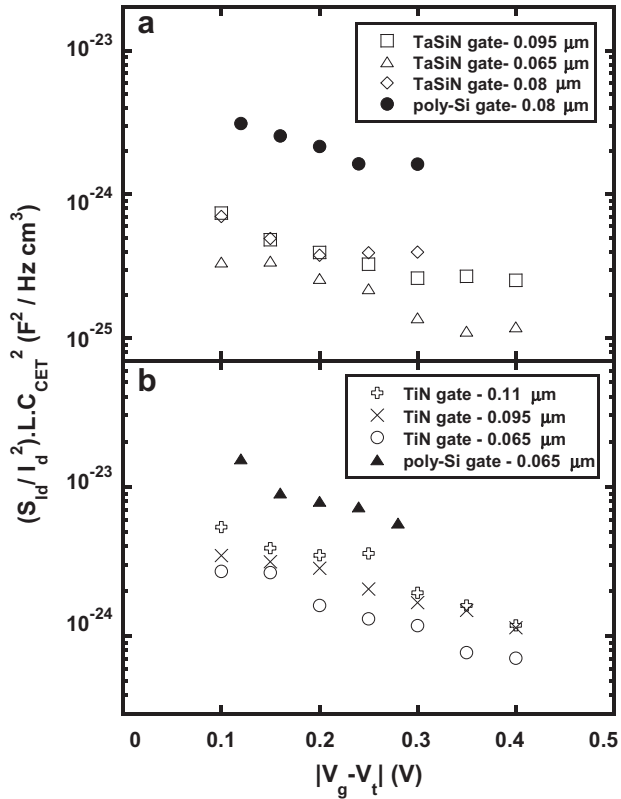


Fig. 2. Normalized drain current noise power spectral density (S_{Id}) at 1 Hz as a function of gate overdrive at $V_d = \pm 50$ mV. (a) TaSiN/HfO₂ and poly-Si/HfO₂ NMOS devices. (b) TiN/HfO₂ and poly-Si/HfO₂ PMOS devices.

the inherent device noise of N and PMOS devices for each gate type. PMOS devices were observed to exhibit higher

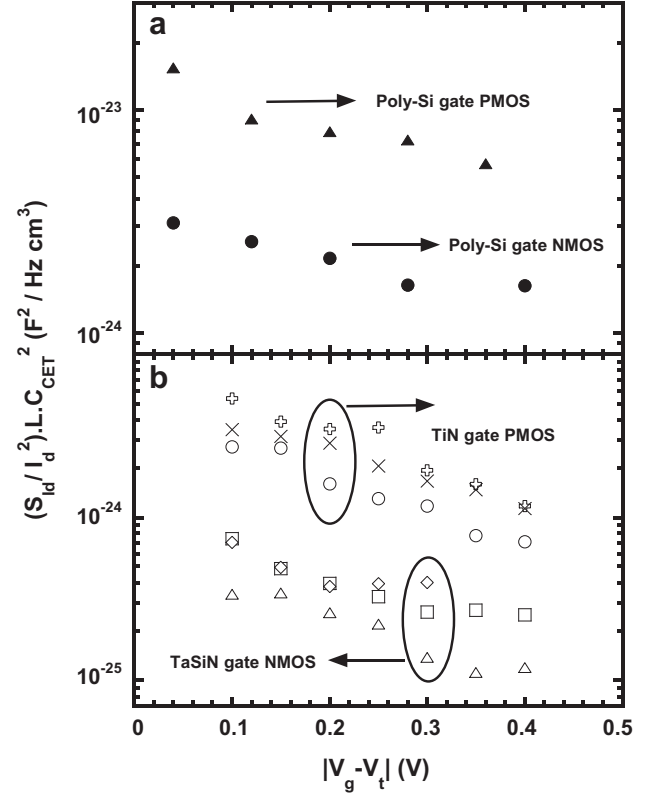


Fig. 3. Normalized drain current noise power spectral density (S_{Id}) at 1 Hz comparing the inherent noise characteristics among N and PMOS devices for (a) poly-Si and (b) metal gates. In either case, PMOS devices exhibit higher inherent noise. The absolute value $|V_g - V_t|$ is used in order to accommodate NMOS and PMOS data together for the same band bending conditions.

noise compared to NMOS devices in both metal and poly-Si gated lots.

The dielectric trap density values were obtained using the Unified Model [14,15] that attributes $1/f$ noise to correlated carrier density and mobility fluctuations due to fluctuations in the occupancy of the gate dielectric traps:

$$S_{Id} = \frac{kT\gamma^2}{\gamma fWL} \left(\frac{1}{N} + \frac{\mu}{\mu_{C0}\sqrt{N}} \right)^2 N_t \quad (2)$$

where S_{Id} is the drain current noise power spectral density ($A^2 \text{ Hz}^{-1}$), k is the Boltzmann constant (eV K^{-1}), T is the absolute temperature (K), γ is the carrier tunneling coefficient in the dielectric (cm^{-1}), f is the frequency (Hz), L is the effective channel length and W is the width of the MOSFET, N is the inversion layer carrier density (cm^{-2}), μ is the effective mobility ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). Here, oxide trap density N_t ($\text{cm}^{-3} \text{ eV}^{-1}$) and μ_{C0} ($\text{cm}^2/\text{V s}$) are fitting parameters. It should be noted that the model assumes strong inversion and the trap density to be uniform spatially into the dielectric. The strong inversion is valid for our case. However, the dielectric in our case is stacked, thus presenting multiple interfaces in the direction of carrier tunneling: substrate-SiO₂ and SiO₂-HfO₂. In addition, the density of traps in the interfacial layer and the bulk of HfO₂ are not

the same. Thus, the N_t values here merely represent the average effective trap density responsible for noise.

The validity of Unified Model over Hooge's mobility fluctuations model [16] was established for poly-Si gated devices [10] and metal gated devices [17] based on the fact that S_d/I_d^2 generally varied as $(g_m/I_d)^2$ rather than having a $1/I_d$ dependence.

Effective mobility (μ) used in Eq. (2) was calculated from the basic transconductance (g_m)-mobility relation. Table 1 gives only the peak mobility in the region of interest. The extracted peak mobility value for PMOS was considerably higher with metal gates than poly-Si gate for HfO₂ gate dielectric [10], while in NMOS there was a minor improvement. This can be attributed to the severity of dopant penetration in PMOS compared to NMOS as suggested in [18].

Table 1 gives the summary of the noise parameters extracted for the devices under study. The tunneling coefficient value of $0.476 \times 10^8 \text{ cm}^{-1}$ was used in Eq. (1) accounting for the presence of HfO₂ dielectric [10]. Typically, for Si–SiO₂ interface, a value of $1 \times 10^8 \text{ cm}^{-1}$ is adopted. Metal-gated n- and p-MOSFETs had an effective trap density of $\sim 1 \times 10^{17}$ and $1 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$, respectively. This is about an order of magnitude lower compared to corresponding n- and p-poly-Si gate devices.

There are several factors that could be responsible for the difference in the effective dielectric trap densities between poly and metal gate MOSFETs. First, ALD technique is known to introduce less contamination during deposition and might have resulted in a better HfO₂ quality when compared to MOCVD tool. Second, lower thermal budgets were realized in gate metal deposition than that required for dopant activation in poly-Si and thus the quality of the underlying dielectric was preserved. Finally, dopant diffusion from poly gate into the dielectric and associated defect generation were eliminated. It has been recently reported that MOCVD HfO₂ has an order of magnitude higher traps compared to ALD HfO₂ for the same EOT and that increasing the thickness of ALD HfO₂ from 30 Å to 50 Å results in an increase of the noise magnitude due to five times higher defect density [19]. In this context, although these results support the first reason stated above, the trap density obtained in our case for 55 Å MOCVD HfO₂ is an order of magnitude lower than that reported for 30 Å ALD HfO₂. Thus, employing the above scaling factors to account for different high- k deposition processes and thicknesses would yield a trap density that is as good as a conventional SiO₂ MOSFET. The trap density data in literature does not support this fact [20], so the extent of difference in the quality of HfO₂ with ALD and MOCVD is not expected to be as high as reported. In addition, noise scaling seen for different ALD HfO₂ thickness need not be the same for MOCVD HfO₂. Hence, it is very likely that the gate electrode material has a role in determining the underlying high- k quality.

The defect density values extracted for NMOSFETs are about an order of magnitude lower compared to PMOSFETs in both metal and poly-Si gate types. Thus, the trap

density is lower in the upper mid-gap region compared to that in the lower mid-gap region of the silicon band gap. The interface trap density (D_{it}) obtained from subthreshold characteristic does not indicate a clear trend. Nevertheless, an opposite trend for trap distribution has been reported recently [21,22] and this discrepancy might be attributed to different process-related parameters. It should be noted that the dielectric trap density (N_t) here is the average effective values for the multi-interfaced dielectric stack considered. In general, the trap density found in conventional SiO₂ devices is less than $1 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ so that the values obtained for high- k in this work are comparatively higher.

In addition, extracted μ_{C0} was lower in high- k devices compared to SiO₂ and the maximum values for the screened scattering coefficient (α) calculated as $(\mu_{C0}\sqrt{N})^{-1}$ with an average carrier density of about $2 \times 10^{12} \text{ cm}^{-2}$ were $1.76 \times 10^{-14} \text{ V s}$ for TiN/HfO₂ (ALD), $9.43 \times 10^{-15} \text{ V s}$ for TaSiN/HfO₂ (ALD), and $7.07 \times 10^{-15}/1.41 \times 10^{-14} \text{ V s}$ for n/p poly-Si/HfO₂ (MOCVD) systems. Values of α , as high as $1.4 \times 10^5 \text{ V s/C}$ or $2.2 \times 10^{-14} \text{ V s}$ were reported for SiO₂ PMOS [23]. In metal and poly-gated HfO₂ devices, NMOS and PMOS alike, the correlated mobility fluctuations (the 2nd term in Eq. (2)) were found to be comparable to or higher than the number fluctuation contribution (1st term) for $|V_g - V_t| \geq 0.2 \text{ V}$ [10]. This suggests that mobility is limited by Coulomb scattering by a greater degree in high- k devices. As such, from extracted N_t and μ_{C0} values, one can conclude that the mobility limited by Coulomb scattering $\mu_{Ct} = (\alpha N_t)^{-1}$ to be more severe in all these high- k devices when compared to SiO₂ systems [5,24,25]. However, the values of μ_{Ct} for metal-gated devices are higher than those for poly-Si gated devices indicating a relatively lower extent in the severity of Coulomb scattering in metal-gated devices. Nevertheless, the percentage improvement in electron mobility of TaSiN gate MOSFETs over poly-Si devices is not as high as that seen for hole mobility increase in TiN gate devices compared to poly-Si MOSFETs. The reason is unknown at this time. The fact that the electron and hole mobility values are lower than universal curve despite lowered Coulomb scattering implies the existence of other scattering sources. It was shown that phonon scattering is severe in poly-Si/HfO₂ compared to poly-Si/SiO₂ [24] and from the mobility data in our case, it is not clearly evident that phonon scattering contribution is reduced with metal gates as suggested in [26]. Inclusion of data on metal gated/SiO₂ stacks would have been relevant, providing better insight about the aforementioned phenomena responsible for the above observations. However, such devices were not available for measurements.

4. Conclusion

Low frequency noise was found to be lower in devices with TaSiN/TiN metal gate HfO₂ gate stacks compared to poly-Si HfO₂ systems. The average effective gate-oxide trap densities at $\sim 1 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ in TaSiN-gated NMOSFETs and $1 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$ in TiN-gated

PMOSFETs are an order of magnitude lower than that for poly-Si gated MOSFETs. In both poly-Si and metal gated MOSFETs, noise level in HfO_2 PMOS was higher than HfO_2 NMOS suggesting a lower trap density distribution in the upper half of the silicon band gap region compared to the lower mid-gap region. The trap density and Coulomb-scattering-limited mobility indicated by these noise measurements imply a better HfO_2 quality with ALD and TaSiN (NMOS), TiN (PMOS) gate stacks compared to MOCVD HfO_2 and poly-Si gate stacks.

Acknowledgements

This work is partially supported by Texas Higher Education Coordinating Board Advanced Technology Program under Grant #003656-0001-2001 and Semiconductor Research Corporation under Contract 2004-VJ-1193.

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