

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title: METAL GATE TRANSISTOR AND METHOD FOR
FABRICATING THE SAME

DECLARATION OF JACK LEE, Ph.D.

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I, Jack Lee, do hereby declare:

1. My name is Jack Lee. I am making this declaration at the request of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in the matter of the *Inter Partes* Review of U.S. Patent No. 7,888,195 (“the ’195 Patent”).

2. I am being compensated for my work in this matter at my standard rate of \$690 per hour for such consulting services. My compensation in no way depends on the outcome of this proceeding.

3. I have been asked to provide my opinion on the technology covered by the ’195 Patent and the validity or invalidity of claims 1-11 of the ’195 Patent (“Challenged Claims”).

I. Qualifications

4. My qualifications generally are set forth in my *curriculum vitae*, which is attached to this declaration as Appendix A.

5. I am an expert in the field of semiconductor design and process technology and have more than forty years of first-hand experience as a researcher, educator, and consultant in the field. My experience specifically includes high-k/metal-gate integration, replacement-gate (gate-last) processes, and work-function engineering for CMOS technologies at and before the 45-nm node.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and M.S. degree in Electrical Engineering in 1981, both from the University

of California, Los Angeles (“UCLA”). I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests encompass semiconductor devices including 3D structures such as FinFETs or tri-gate MOSFETs, high-k gate

dielectrics and gate electrodes, fabrication processes, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, semiconductor memory applications, and alternative channel materials.

11. I have been invited to give talks, teach short courses and participate in panel discussions at numerous conferences specifically on the topic of fabrication processes for nanoscale devices such as FinFETs and gate-all-around MOSFETs, high-k gate dielectrics, gate electrodes, and semiconductor memory devices. This includes prestigious conferences such as the Symposium on VLSI Technology, the IEEE International Electron Devices Meeting, and other global forums. My research group at The University of Texas at Austin is recognized as a pioneer in developing high-k gate dielectric metal-gate processes for nanoscale MOSFETs including FinFETs. I have extensive experience in this field, with numerous publications in journals and conference proceedings on the topics of nanoscale MOSFETs and FinFETs, fabrication processes, characterization, and device reliability.

12. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

13. I have authored over 600 journal publications and conference

proceedings papers and have coauthored eight book and book chapters on semiconductor technologies. I am a named inventor of nine U.S. patents. I have also received numerous teaching and research awards, e.g. inventor recognition and best paper awards.

14. In 2002, I became an IEEE Fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

15. I have served in various technology consulting and business advisor roles. For example, I have been teaching short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

16. Taken as a whole, my academic and practical experience has given me a substantial basis upon which to evaluate the technology that is in question in the claims of the '195 Patent. Based on my experience and education, and the acceptance of my publications and professional recognition by peers in my field, I believe that

I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '195 Patent (which I further describe below) and what such a person would have understood at that time, and the state of the art during that time.

II. Materials Reviewed

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the invention of the '195 Patent.

18. I understand that the prior art references and other documents that I discuss in this declaration will be filed with the Petition for *Inter Partes* Review in this matter ("Petition") and assigned exhibit numbers. I also understand that other exhibits, not referenced in this declaration, may also be filed with the Petition.

19. In forming my opinions, I have reviewed and considered the following documents, identified by exhibit number:

Exhibit No.	Description
TSMC-1001	U.S. Patent No. 7,888,195 ("the '195 patent")
TSMC-1002	Excerpts from the Prosecution History of the '195 Patent ("the Prosecution History")
TSMC-1004	U.S. Pub. 2007/0138559 ("Bohr")
TSMC-1005	U.S. Pub. 2005/0233527 ("Brask")
TSMC-1006	Wang et al., Chemical Mechanical Polishing for Selective CVD-W, Materials Chemistry And Physics, 51, 75-79 (1997)

	("Wang")
TSMC-1007	Amazawa et al., Planarized Multilevel Interconnection Using Chemical Mechanical Polishing of Selective CVD–Al Via Plugs, IEEE Transactions on Electron Devices, Vol.: 45, Is.: 4, 815 (April 1998) ("Amazawa")
TSMC-1008	U.S. Pub. 2009/0242997 ("Yu")
TSMC-1009	U.S. Pub. 2009/0315124 ("Chen")
TSMC-1010	U.S. Pub. 2006/0180851 ("Lee")
TSMC-1011	Hofstein et al., The Silicon Insulated-Gate Field-Effect Transistor, Proceedings of the IEEE, Volume: 51, Issue: 9, (September 1963) ("Hofstein")
TSMC-1012	U.S. Pat. No. 6,573,134 ("Ma")
TSMC-1013	U.S. Pat. No. 7,390,709 ("Doczy '709")
TSMC-1014	U.S. Pub. 2006/0278934 ("Nagahama")
TSMC-1015	U.S. Pat. No. 7,084,038 ("Doczy '038")
TSMC-1016	Mistry et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," 2007 IEEE International Electron Devices Meeting, 247-250, December 10-12, 2007
TSMC-1017	U.S. Pat. No. 7,211,869 ("Chan")
TSMC-1020	European Patent No. 2112687B1
TSMC-1021	U.S. Pub. 2008/0096383 ("Tigelaar")
TSMC-1022	U.S. Patent No. 6,225,168 ("Gardner")
TSMC-1023	Devireddy et al., "Improved low frequency noise characteristics of sub-micron MOSFETs with TaSiN/TiN gate on ALD HfO ₂ dielectric," Microelectronics Reliability Volume 47, 1228-1232 (2007).
TSMC-1024	U.S. Pub. 2006/0065939 ("Doczy '939")
TSMC-1025	U.S. Patent No. 6,559,051 ("Buynoski")
TSMC-1026	U.S. Pub. No. 2005/0051854 ("Cabral")
TSMC-1027	A. Chatterjee et al., "CMOS metal replacement gate transistors using tantalum pentoxide gate insulator," International Electron Devices Meeting 1998, Technical Digest (Cat. No.98CH36217), San Francisco, CA, USA, 1998, pp. 777-780, doi: 10.1109/IEDM.1998.746471. ("Chatterjee")
TSMC-1028	U.S. Patent No. 7,176,090 ("Brask '090")

TSMC-1029	U.S. Pub. No. 2007/0037343 (“Colombo”)
TSMC-1030	U.S. Pub. No. 2008/0265322 (“Lin”)
TSMC-1031	U.S. Pub. No. 7,208,361 (“Shah”)

III. Relevant Legal Standards

20. I am an engineer by training and profession. The opinions I am expressing in this report involve the application of my knowledge and experience to the evaluation of certain prior art with respect to the '195 Patent. My formal knowledge of patent law is no different than that of any lay person. Therefore, I have requested that the attorneys from Fish & Richardson, P.C., who represent TSMC, provide me with guidance as to the applicable patent law in this matter. The paragraphs below express my understanding of how I must apply current principles related to patent validity to my analysis.

A. Claim Construction

21. I have been informed that in determining whether a patent claim is obvious in view of the prior art, the Patent Office must apply the *Phillips* standard to construe the claim by giving the claim its plain and ordinary meaning as understood by a POSITA at the time of the invention, in light of the specification and prosecution history.

22. For the '195 Patent, I have been asked to consider the relevant time as just prior to August 26, 2008, which I understand is the filing date of the '195 Patent.

For the purposes of this review, I have construed each claim term in accordance with its plain and ordinary meaning under the *Phillips* standard, unless otherwise indicated.

B. Anticipation

23. I have been informed that a patent claim is unpatentable as anticipated under 35 U.S.C. § 102 if each and every element of a claim is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or necessarily includes the claimed elements, it anticipates.

C. Obviousness

24. I have been informed that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention. As mentioned above with respect to claim construction, I have been asked to consider the relevant time as just prior to August 26, 2008, the filing date of the '195 Patent. I understand that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

25. In determining the scope and content of the prior art, it is my understanding that a reference is considered analogous prior art if it falls within the

field of the inventor's endeavor. In addition, a reference is analogous prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

26. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment requires showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

27. It is my further understanding that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- a predictable use of prior art elements according to their established

functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results;

- choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

28. I have been told that a prior art reference may be combined with one or more references and/or with the knowledge of a person of ordinary skill in the art to show obviousness. I have also been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have also been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

29. I understand that when combining prior art elements, the obviousness analysis requires determining whether a person of ordinary skill in the art would have had a “reasonable expectation of success” in arriving at the claimed invention by combining those elements. I have been told that a “reasonable expectation of success” does not require “absolute predictability.”

30. I have been told that the strongest rationale for combining references is

a recognition, expressly or impliedly, in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. I have also been told that combining two embodiments disclosed adjacent to each other does not require a leap of inventiveness.

31. I have been told that, with respect to the obviousness of similar and overlapping ranges, where a claimed range overlaps or lies inside a range disclosed by the prior art, a *prima facie* case of obviousness exists. I have also been told that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. I have been told that obviousness in these cases may be rebutted if the claimed range is critical or demonstrates new and unexpected results.

32. I have been told that a mere change in the timing or sequence of steps without any new or unexpected results is generally obvious.

IV. PERSON OF ORDINARY SKILL IN THE ART

33. It is my understanding that when interpreting the claims of the '195 Patent, I must do so based on the perspective of a POSITA as of the relevant priority date. My understanding is that the earliest claimed priority date of the '195 Patent is August 26, 2008.

34. In my opinion, a person of ordinary skill in the art for the '195 Patent

would have been a person having a Master of Science degree from an accredited institution in electrical engineering, materials science, physics, or the equivalent, and at least three years of experience in the manufacturing of semiconductors including planar and non-planar transistors. Additional graduate education could substitute for professional experience, and significant work experience or training could substitute for formal education.

35. As described in detail above in the “Qualifications” section, my own training and experience exceed that of one of ordinary skill in the art.

V. Background

A. Technology Background

1. Overview of MOSFET Devices

36. Semiconductor devices are generally manufactured on substrates that are employed as a building foundation and comprise billions of transistors. Transistors are the fundamental building blocks for semiconductor devices. Each transistor operates as a switch that either allows or blocks the flow of electrical current. By combining thousands, or even billions of transistors together, circuit designers can implement electronic hardware like processors used in computers, mobile phones and other semiconductor devices.

37. Field-effect transistors (FETs) have been around for over 60 years, and as early as 1963, Hofstein disclosed a Metal-Oxide Semiconductor (MOS) transistor

that utilizes p-type and n-type materials. *See* TSMC-1011, 1191-92. Moreover, the CMOS (Complementary Metal-Oxide-Semiconductor) technology discussed in the '195 patent—where N-channel Metal-Oxide-Semiconductor (NMOS) and P-channel Metal-Oxide-Semiconductor (PMOS) transistors are paired together—has been in wide use for several decades. *See* TSMC-1022, 2:62-67; TSMC-1025, 1:55-2:17; *see also generally* TSMC-1027.

38. A MOSFET (metal-oxide-semiconductor field-effect transistor) is a semiconductor device commonly used as switches in modern integrated circuits. A MOSFET includes a gate structure above a substrate of semiconductor material such as silicon. A thin dielectric layer separates the gate structure from the substrate. The substrate further includes source and drain regions located at respective sides of the gate structure. When the transistor is “off,” no current flows between the source and drain. When a proper voltage is applied to the gate, the transistor is turned on, allowing current to flow through the “channel region” of the substrate between the source and drain. TSMC-1022, 5:14-60 (“When an input voltage is applied to the gate electrode 103, a transverse electric field is set up in the channel region 107. By varying the transverse electric field, it is possible to modulate the conductance of the channel region 107 between the source region and the drain region. In this manner, an electric field controls the current flow through the channel region 107. This type of device is commonly referred to as a MOS field-effect-transistor (MOSFET).”).

The source and drain regions being located at respective sides of the gate structure create a conductive channel beneath the gate and between the source and drain regions. *Id.*; *see also* TSMC-1030, [0005]-[0007] (“The source/drain 14 are in the two sides of the gate structure 12 in the substrate 10.”), [0019], [0026], [0029], [0036], FIG. 6; TSMC-1025, 3:12-33 FIGS. 7, 16. In MOSFET processes, source and drain regions were typically formed by ion implantation of dopants into the silicon substrate. TSMC-1030, [0019], [0029]; TSMC-1026, [0002], [0031]-[0033].

39. Through this configuration, a voltage applied to the gate structure can be used to modulate the conductivity of a channel region in the substrate beneath the gate structure and between the source and drain regions to attain a controlled flow of electrical current. TSMC-1022, 1:24-1:60; *see also* TSMC-1030, [0019], FIG. 6. These basic elements of a FET have been known for decades, as illustrated by the following figure from Hofstein (IEEE article from 1963):

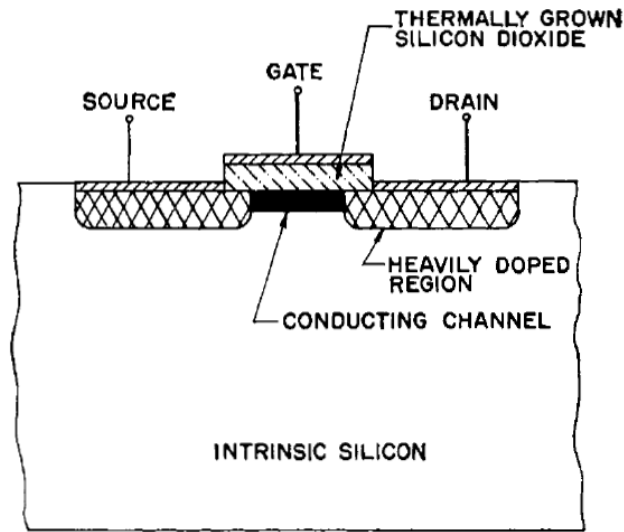


Fig. 2—Insulated-gate field-effect transistor.

TSMC-1011, FIG. 2

See also TSMC-1011, 1190-1202, FIGs. 1-3; TSMC-1022, 1:14-2:4, FIG. 1 (patent filed ten years before the '195 patent and describing how “[o]ver the last few decades, the electronics industry has undergone a revolution by the use of semiconductor technology” including MOSFETs).

40. I note that MOSFETs (metal-oxide-semiconductor field-effect transistor) are the most common insulated gate field-effect transistors and in modern electronics the terms are used interchangeably. As demonstrated by Hofstein and Gardner, these components of MOSFETs have been well known for decades. TSMC-1011, 1190-1202, FIGs. 1-3. TSMC-1022, 1:14-2:4, FIG. 1 (patent filed ten years before the '195 patent describing how “[o]ver the last few decades, the electronics industry has undergone a revolution by the use of semiconductor

technology” including MOSFETs).

41. Transistors are classified as either “n-type” or “p-type”. In n-type MOSFET (or NMOS), current is carried by negatively charged electrons, and the source and drain regions are doped with n-type impurities (e.g., arsenic or phosphorus), which contribute free electrons due to their higher valence electron count. In contrast, p-type MOSFET (or PMOS) conducts current via holes (positively charged carriers), and the source and drain regions are doped with p-type impurities (e.g., boron) which have fewer valence electrons and create a surplus of holes. In both cases, current flows through the channel when the transistor is in the on-state. Complementary Metal-Oxide-Semiconductor (CMOS) technology combines both NMOS and PMOS transistors in a single circuit, enabling efficient logic design with low power consumption by ensuring that only one type of transistor conducts at a time during switching. CMOS technology has been widely used for several decades. *See e.g.*, TSMC-1022, 2:62-67; TSMC-1025, 1:55-2:17; TSMC-1012 1:11-16 (“Dual metal gate CMOS devices are suggested in the 1999 edition of International Technology Roadmap for Semiconductors”) *see also generally* TSMC-1027.

2. Replacement Metal Gates

42. The gate-first process was the standard approach in early CMOS technology, particularly through the 90 nm (~2003) and 65 nm (~2005) technology

nodes. In this method, the gate electrode and dielectric are formed early, enabling self-aligned source and drain formation, which ensures precise alignment and helps minimize parasitic capacitance – key to enhancing device performance. However, the gate-first approach became problematic with the introduction of high-k (high dielectric constant) materials and metal gates, which replaced traditional poly/SiO₂ stacks to address excessive gate leakage and degraded electrostatic control at smaller nodes. *See* TSMC-1016. Specifically, high dielectric constant (high-k) material (including at the gate dielectric layer that separates the metal gate structure from the substrate) became desired in order to reduce the effective SiO₂ thickness of layers while mitigating against increased leakage current, thereby allowing for a reduction to the overall size of MOSFET devices.

43. By the 45 nm node (~2007) and beyond, it became clear that high-k/metal gate (HKMG) stacks are thermally sensitive, particularly to the junction activation anneals and SiGe source/drain regrowth processes used to form low-resistance, strain-enhanced regions. As a result, the gate-last (replacement metal gate) approach became the dominant and widely accepted industry solution, rather than a novel or unconventional process. These high-temperature steps can degrade the high-k dielectric and alter the metal gate's work function, leading to threshold voltage instability and reduced device reliability. To overcome this, the industry adopted the gate-last, or replacement metal gate (RMG), process. In this approach,

a sacrificial polysilicon “dummy” gate (sometimes referred to as a “sacrificial structure”) is patterned early to preserve self-alignment, while the final high-k dielectric and metal gate stack are introduced after all high-temperature processing is complete.

44. In more detail, this process generally involves forming “dummy patterns” in the shape of the gate structures over the substrate, forming a dielectric over the substrate and around the dummy patterns, removing the dummy patterns from the surrounding dielectric by a selective etching process, and then filling the openings left by removal of the dummy patterns with one or more metals for the gate structure. *See* TSMC-1013, Abstract, 1:15-48; 2:21-3:13; *see also* TSMC-1030, [0024]-[0026]. In several common implementations, the gate-last process involves depositing the dummy gate, forming sidewall spacers, creating source/drain regions through implantation and activation annealing — or by recessing and regrowing embedded S/D stressors — and then removing the dummy gate to expose the channel. The opening that results from removal of a dummy pattern in the gate-last process is sometimes referred to as a “trench” or a “recess.” In some implementations, a conformal high-k dielectric (e.g., HfO₂) and a metal gate stack are then deposited into the resulting trench. *See e.g.*, TSMC-1030, [0024]-[0026]. In other implementations, the high-k dielectric layer is formed before the dummy gate and retained after the dummy gate is removed, after which the metal stack are

deposited on top of the retained high-k dielectric layer. TSMC-1028, 7:1-9.

45. This method allows for: (1) enhanced work function tunability, since metals optimized for NMOS and PMOS can be selected post-anneal; and (2) preservation of gate stack integrity, as sensitive materials are never exposed to damaging thermal steps. Even at the most advanced nodes today, the gate-last process remains the industry standard for high-performance 3D nanoscale integrated-circuit devices.

46. In short, field effect transistors have been known for many years, but certain challenges to their fabrication emerged in the years leading up to the Critical Date (August 26, 2008) as metals began to replace polysilicon in the gate electrode to achieve smaller, more efficient designs. *See, e.g.*, TSMC-1027. The use of metal in the gate electrodes, for example, interfered with certain high-temperature steps in fabrication processes that had previously been used with polysilicon gates, *e.g.*, to activate dopants after an ion implantation step or to grow a high-quality oxide as the gate dielectric. *See, e.g.*, TSMC-1026, TSMC-1028, TSMC-1029. Thus, different techniques were needed to realize a gate dielectric with a high dielectric constant (“high-k”) material when using metal in the gate electrode. To this end, “gate-last” processes were developed that involved use of a sacrificial layer (*e.g.*, formed from polysilicon) during the high-temperature steps, followed by removal of the sacrificial layer through etching and replacement of the sacrificial layer with a

dielectric and a metal.

3. Work Function Engineering

47. The work functions of metal gate electrodes are modulated in order to improve performance of the transistor. The work function represents the minimum energy required to remove an electron from the gate electrode. The work function is tuned to establish the threshold voltage (V_t), which dictates the specific voltage required to switch the transistor. TSMC-1020, ¶5. The work function of metal electrodes “is affected by several factors, including composition, underlying dielectric and heat cycles during processing.” *See* TSMC-1021, ¶7, *see also id.*, ¶¶8-11; TSMC-1026, ¶¶22-23; TSMC-1014, ¶9; TSMC-1015, 4:8-43. In semiconductor fabrication, selection among known materials to achieve a desired work function or threshold voltage, particularly where references expressly invite ‘any suitable material’, is a paradigmatic example of routine optimization within ordinary skill.

48. In CMOS devices the metal gates for the NMOS and PMOS transistors are fabricated to have different work functions. *See* TSMC-1021, ¶11; TSMC-1024, ¶¶2-3. One common technique for tuning these work functions includes using different types of metals or gate stacks in the PMOS and NMOS transistors. TSMC-1024, ¶¶2-3; TSMC-1031, 7:48-8:46; TSMC-1020, ¶¶20, 50. Another common technique included using a thin capping layer to shift the effective work function by creating dipoles at the interface. *See e.g.*, TSMC-1021, ¶¶85-86; TSMC-1023;

TSMC-1020, ¶54. These techniques for fabricating CMOS devices were well known before the priority date of the '195 patent—e.g., forming dummy-gates, forming source and drain regions at each side of the dummy gates, replacing of dummy-gates with metal gates including high-k and metal layer deposition with work function tuning. *See also supra* §V.A.2. Accordingly, selecting among known metals, metal nitrides, metal oxides, and dielectric capping layers to achieve a target work function was a routine design choice for a POSITA, not an inventive step.

49. In short, a POSITA would have been familiar with integrating and modifying high-k/metal-gate stacks using known materials and known process steps, including routine substitution among work-function-tuning layers to achieve predictable electrical results.

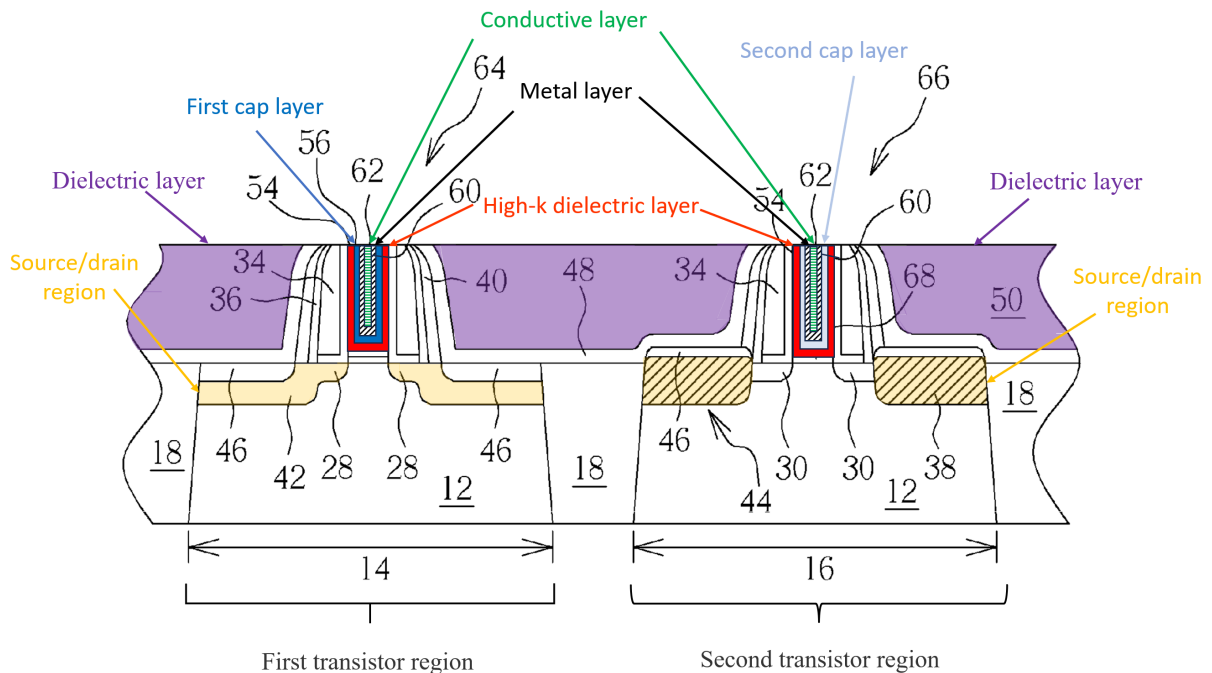
B. The '195 Patent

50. The '195 patent describes the well-known structure of a transistor having metal gates. *See supra* §V.A. The shape of the metal gates are created by forming dummy gates that are subsequently removed to form openings. TSMC-1001, Abstract. Gates are created by filling these openings with layers of different materials, such as dielectric layers, a capping layer, and a metal layer or another conductive layer. *Id.*

51. Polysilicon materials are commonly used when fabricating gate electrodes for metal-oxide semiconductor “(MOS”) transistors but present certain

tradeoffs. *Id.*, 1:11-17. For instance, because such polysilicon gates utilize semiconductor materials of high resistance, transistors with polysilicon gates operate at a lower speed than those with metal gates. *Id.*, 1:18-26. The '195 patent also explains that it was known that fabricating polysilicon gate electrodes could cause a depletion effect, further degrading performance. *Id.*, 1:27-39.

52. To address such issues, the '195 patent proposes to replace conventional polysilicon with metal as a gate material. TSMC-1001, 1:40-49. More specifically, the '195 patent utilizes dummy gates made from polysilicon 22 to fabricate metal gates 64, 66. *See id.*, 2:39-64, 4:61-6:8, FIGS. 1, 2, and 8. The '195 patent also uses a cap layer 56 to define the work function of a metal layer 60 that is deposited on the cap layer 56 of the NMOS transistor region 14 and the high-k dielectric layer 54 of the PMOS transistor region 16. *Id.*, 4:37-60. The '195 explains that a second cap layer can “be deposited between the high-k dielectric layer 54 and the metal layer 60 of the PMOS transistor.” *Id.* The '195 patent asserts that this increases the performance of a CMOS transistor. *Id.* Such a transistor is illustrated in the '195 patent as follows:



TSMC-1001, FIG. 8 (annotated)

53. As used in this declaration, the term ‘cap layer’ refers to a layer disposed between a high-k dielectric and a metal gate that modifies effective work function, regardless of whether that layer is metallic, dielectric, or metal-oxide in composition, and regardless of whether the layer is ultimately consumed, oxidized, or partially removed during subsequent processing. This usage is consistent with industry practice and the references discussed herein.¹

¹ I note that none of the challenged claims require the cap layer to be exclusively dielectric, exclusively metallic, or deposited by any particular method, nor do they exclude metals, metal nitrides, or metal oxides. A POSITA would not read such

54. In summary, the '195 patent claims a conventional replacement-metal-gate (RMG) process in which dummy gates are removed and replaced with a high-k dielectric, a work-function-tuning cap layer, and a metal gate, with region-selective removal and replacement of those layers for NMOS and PMOS devices. As I explain below, every claimed step including the use of lanthanide-based and aluminum-based cap layers, selective removal, and CMP planarization, was well known and taught in the prior art before August 2008. The prior-art references discussed below, including Bohr and Brask are representative examples of these well-established replacement-metal-gate flows. The '195 patent does not purport to invent replacement-gate processing or work-function tuning itself, but instead applies these well-known techniques in a conventional CMOS integration flow.

VI. Overview of the Prior Art

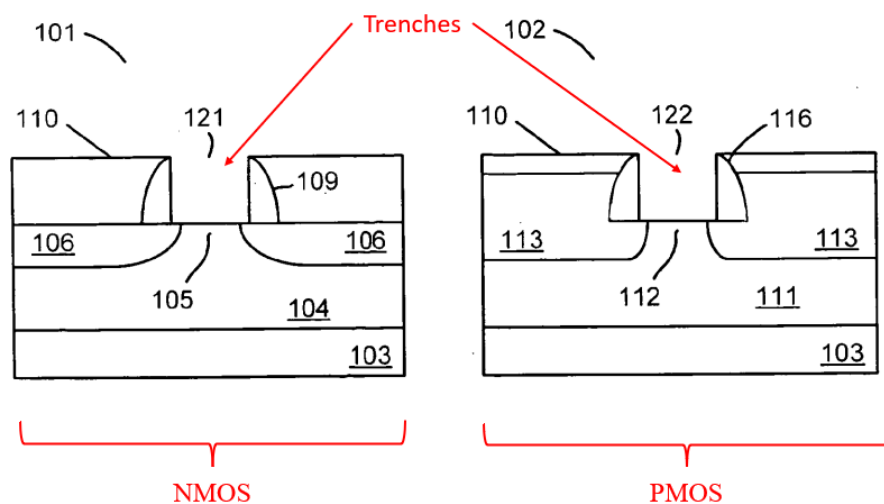
A. Overview of Bohr

55. Bohr discloses apparatuses and methods related to NMOS and PMOS

limitations into the claims. Nor do the claims require that the cap layer be electrically insulating, deposited prior to or after any particular anneal, or removed in any specific manner. A POSITA would understand the plain meaning of the term “cap layer” functionally, consistent with industry usage, rather than as a narrowly defined material category.

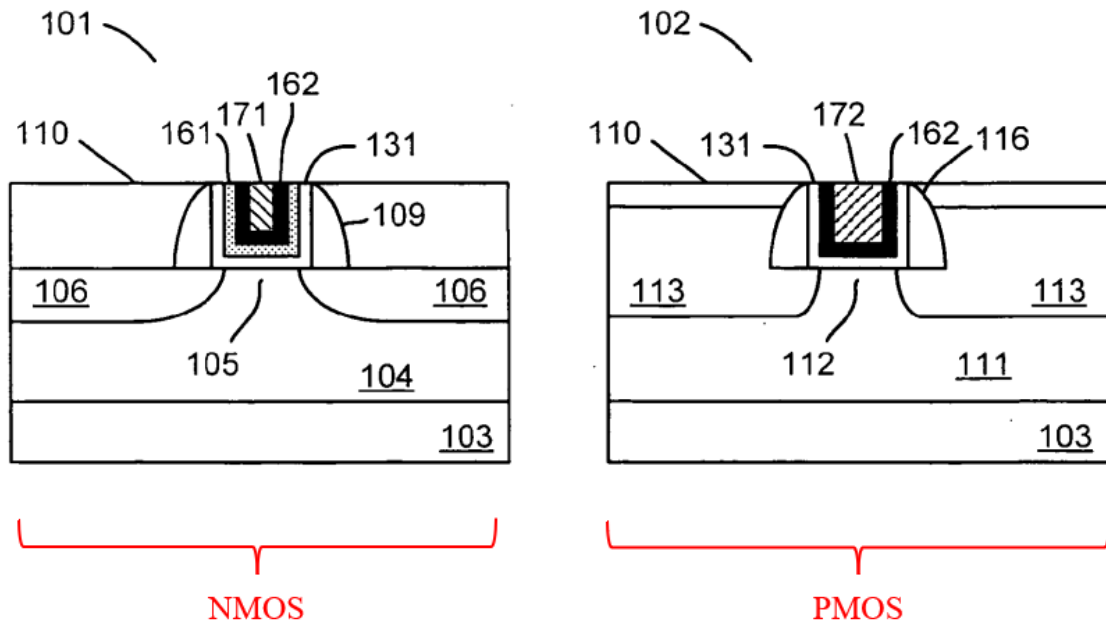
transistors. TSMC-1004, Abstract, ¶¶41-43. In particular, the device and method that Bohr describes “may provide for increased channel strain to enhance the performance of NMOS and PMOS transistors.” *Id.*, ¶16. An NMOS transistor 101 and PMOS transistor 102 are formed on a substrate 103 by replacing gate electrodes 108, 115 and depositing dielectrics and metals into trenches 121, 122 created by removal of the gate electrodes 108, 115 until the NMOS transistor 101 and PMOS transistor are formed, as shown in FIG. 8.

56. As I have illustrated below in FIG. 3, Bohr discloses forming trenches 121 and 122 in its NMOS and PMOS transistor regions, respectively, by removing sacrificial gate electrodes. *Id.*, ¶¶35, 50. A POSITA would understand Bohr’s “sacrificial” gate structures to be the same as “dummy gates” in the ’195 patent, as both are temporary gate structures removed and replaced later in the fabrication flow.



TSMC-1004, FIG. 3 (annotated)

57. Ultimately, as shown below in FIG. 8, NMOS transistor 101 and PMOS transistor 102 are formed on a substrate 103 by depositing/etching various dielectric and metal layers into these trenches. *Id.*, ¶¶49-50.



TSMC-1004, FIG. 8 (annotated)

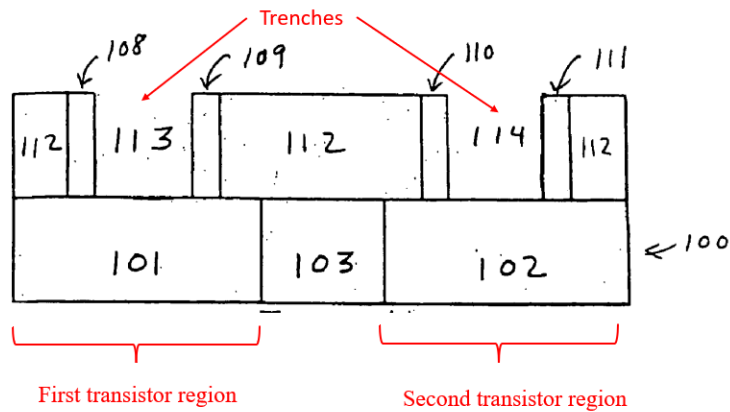
58. In more detail, in the NMOS transistor 101, the gate electrode 141 is formed in the trench 121 over a gate dielectric 131, the gate electrode 141 including an n-doped polysilicon or metal with an n-type work function. *Id.*, ¶40. By contracting more slowly than surrounding materials, gate electrode 141 can transfer a tensile strain to channel 105 via the gate dielectric 131 or spacers 109. *Id.*, ¶41. Bohr discloses that the material that the n-type work function metal provides the additional tensile strain to channel 105. *Id.*, ¶41. In the PMOS transistor 102, gate

electrode 142 is formed in the trench 122 over the gate dielectric 131. *Id.*, ¶42. The gate electrode 142 can include a p-doped polysilicon or a metal with a p-type work function. *Id.*, ¶42. Gate electrode 142 provides a compressive strain on the channel 112 via gate dielectric 131 or via spacers 116. *Id.*, ¶43. As disclosed, the p-type work function metal imparts the compressive strain on the channel 112. *Id.*, ¶43.

59. An n-type material 161 is formed over both trenches 121, 122, and then the n-type material 161 is selectively removed from the PMOS transistor 102 while remaining within the NMOS transistor 101. *Id.*, ¶¶45-46, FIG. 6. Turning to FIG. 7, a p-type material 162 is formed in the trenches 121, 122 over the NMOS transistor 101 and PMOS transistor 102. *Id.*, ¶46. Fill material 171 is selectively deposited into trench 121, and fill material 172 is selectively deposited into trench 122, and thereby form the NMOS transistor 101 and PMOS transistor 102, as illustrated in FIG. 8. *Id.*, ¶¶47-48.

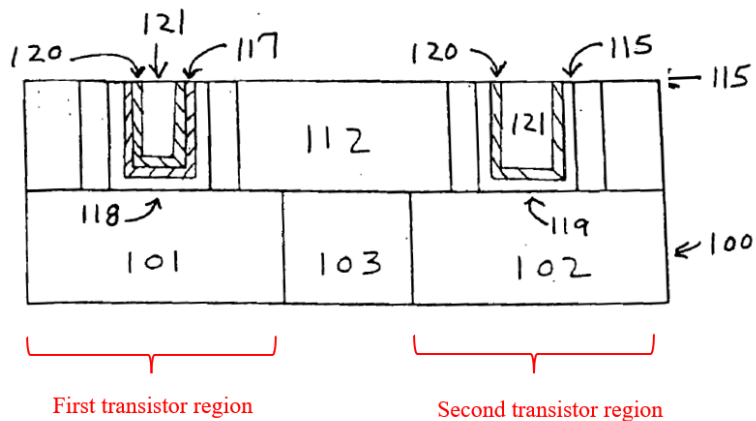
B. Overview of Brask

60. Brask discloses a method of making a semiconductor device, and more specifically one having metal gate electrodes and a structure with first part 101 (*e.g.*, NMOS) and second part 102 (*e.g.*, PMOS), as illustrated in FIG. 1a-1f. TSMC-1005, Abstract, ¶¶11, 13, 34. More specifically, as shown in annotated FIG. 1b below, Brask's fabrication method includes forming trenches 113, 114 in the dielectric 112. TSMC-1005, ¶24-27.



TSMC-1005, FIG. 1b (annotated)

61. Turning to annotated FIG. 1f shown below, Brask shows depositing/etching various layers over the trenches to form a semiconductor device having a high-k gate dielectric layer 115 and various metal layers 117, 120, among others. *Id.*, ¶35.



TSMC-1005, FIG. 1f (annotated)

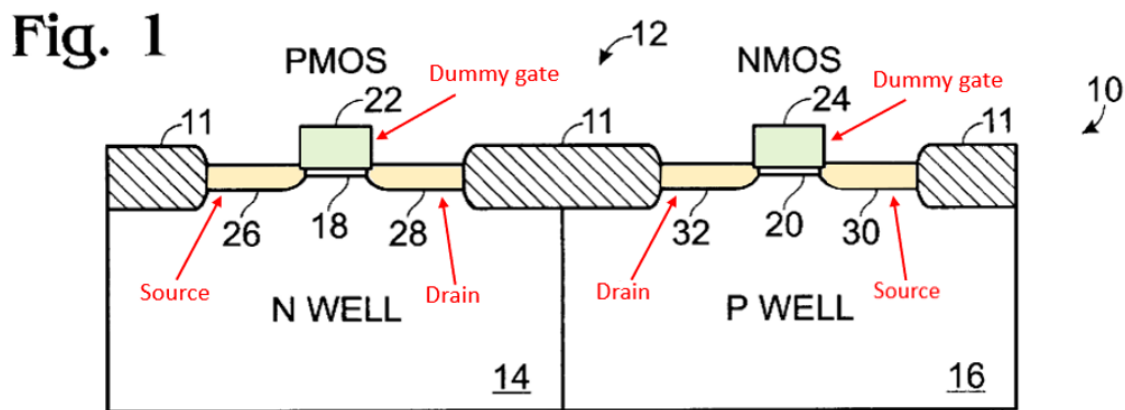
62. In more detail, in FIG. 1f Brask shows a “[s]econd metal layer 120 may

be formed on high-k gate dielectric layer 115 and first metal layer 117 using a conventional PVD or CVD process.” *Id.*, ¶35. The second metal layer 120 includes an n-type material, layer 120 preferably has a work function that is between about 3.9 eV and about 4.2 eV. *Id.*, ¶35. Metal layer 116 is used to form first metal layer 117 and can include an n-type material and a p-type material. TSMC-1005, ¶¶32-33.

63. Brask’s fabrication method includes forming a dielectric 112 on a substrate 100 as well as trenches 113, 114 in the dielectric utilizing sidewall spacers 108, 109 in the first part 101 and sidewall spacers 110, 111 in the second part 102. TSMC-1005, ¶24-27. Brask’s metal layer 116 is disposed on a high-k gate dielectric layer 115, both filling trenches 113, 114. *Id.*, ¶25-31. Brask’s first metal layer 117 is formed on first part 118 of high-k gate dielectric layer 115, such that first metal layer 117 covers first part 118 of high-k gate dielectric layer 115, but does not cover second part 119 of high-k gate dielectric layer 115. *Id.*, ¶33. As shown in FIG. 1e, second metal layer 120 is then deposited on first metal layer 117 and exposed second part 119 of high-k gate dielectric layer 115 generating the structure illustrated by FIG. 1e. If first metal layer 117 comprises an n-type metal, *e.g.*, one of the n-type metals identified above, then second metal layer 120 preferably comprises a p-type metal, *e.g.*, one of the p-type metals identified above. Conversely, if first metal layer 117 comprises a p-type metal, then second metal layer 120 preferably comprises an n-type metal. *Id.*, ¶34.

C. Overview of Ma

64. Ma generally describes a method of fabricating a dual metal gate CMOS including forming a gate oxide in a gate region and depositing a place-holder (dummy) gate in each of the n-well and p-well. TSMC-1012, Abstract. More specifically, Ma discloses forming “a ‘dummy’ gate, or a place-holder gate,” where such “[p]lace-holder gates 22, 24 are formed in the PMOS and NMOS.” *Id.*, 2:28-32. Additionally, as shown in annotated FIG. 1 below, Ma discloses “provid[ing] a source 26 and a drain 28 for the PMOS” and “provid[ing] a source 30 and a drain 32 for the NMOS.” *Id.*, 2:39-49.



TSMC-1012, FIG. 1 (annotated)

D. Overview of Wang

65. Wang discloses a method of chemical mechanical polishing, specifically, chemical mechanical polishing of tungsten filled contact holes. TSMC-1006, Abstract, 75-76. For example, Wang utilizes a lower down-pressure CMP to

polish overfilled nail heads of CVD deposited tungsten and tungsten particles deposited on the surface of dielectric. TSMC-1006, 78-79.

E. Overview of Amazawa

66. Amazawa discloses a planarization process for metal plugs using chemical mechanical polishing (CMP). *See* TSMC-1007, Abstract, 815. For example, Amazawa describes a CMP for aluminum plugs. *Id.*, 816. Notably, Amazawa teaches that selectively deposited plugs can result in sharp crystal facets and surface unevenness due to the difference between the via depth and plug height. *Id.*, 815. By planarizing metal plugs, Amazawa's CMP and post-treatment technique can improve the electrical characteristics of via connections. *See* TSMC-1007, 817.

F. Overview of Yu

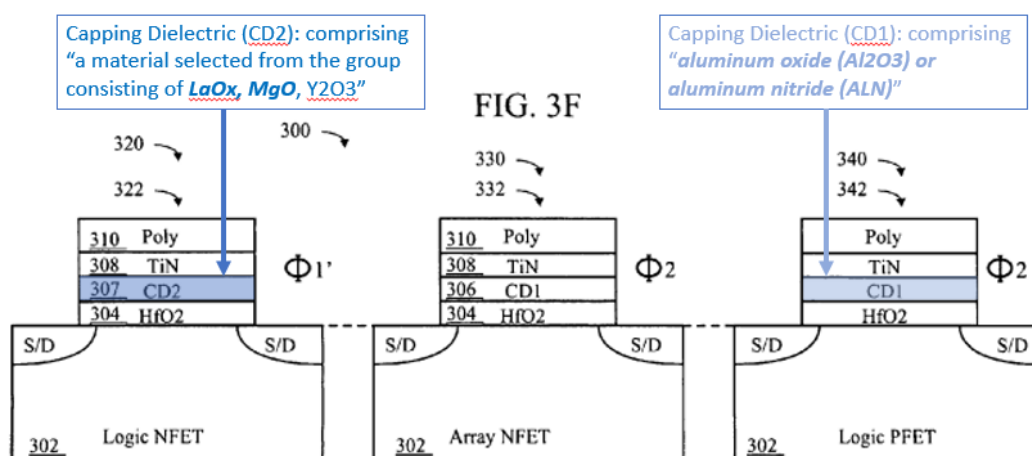
67. Yu is directed to a method of fabricating a semiconductor structure that involves replacing polysilicon with a metal gate to thereby avoid polysilicon depletion and reducing gate parasitic resistance. TSMC-1008, Abstract, ¶5. For example, Yu discloses a device made of a first type transistor 110', a second transistor 120', a high-voltage element 130', and a static random access memory 170'. *Id.*, ¶50, FIGS. 1E-1, 1E-2. Yu further discloses a dielectric layer 155, a high-k dielectric layer 157, a second type conductive layer 161 and a low resistance conductive layer 163 are formed on the substrate 100 within openings 181, 183, 185, 187. *Id.*, ¶45, FIG. 1B-1.

68. As shown in FIGS. 1A-1 – 1C-1 of Yu, the first type transistor 110' includes a dielectric layer 155, high-k dielectric layer 157, first type conductive layer 167, low resistance conductive layer 169, spacer 117 and a first type source/drain 119 within the substrate 100 deposited at two sides of the low resistance conductive layer 169. TSMC-1008, ¶50. The first type conductive layer 167 and a low resistance conductive layer 169 are formed in sequence on the first type transistor 110', and the first type conductive layer 167 can be a p-type metal with a working function between 4.9~5.1 eV. *Id.*, ¶48. Similarly, the second type transistor 120' has a dielectric layer 155, high-k dielectric layer 157, second type conductive layer 161, low resistance conductive layer 163, spacer 127 and second type source/drain 129 in the substrate 100 disposed at two sides of the low resistance conductive layer 163. *Id.*, ¶50. The first type source/drain 119 is a P-type doped region, making the first transistor 110 a P-type transistor. The second type source/drain 129 is an N-type source/drain, thus rendering the second transistor 120 an N-type transistor. *Id.*, ¶38.

G. Overview of Chen

69. Chen is directed to work function engineering for embedded DRAM (eDRAM) MOSFETs. TSMC-1009, Title; *see also id.*, ¶¶50-68. Chen discloses using capping dielectric “CD1” and “CD2” for tuning the work function in order to set the threshold voltage for the PFET and NFET respectively. *Id.* For example, Chen describes adding “metal oxide cap (CD1)” over the gate dielectric “to move the

workfunction” in order to increase the V_t of the EDRAM array device.” TSMC-1009, ¶51. Chen explains the NFET is formed without CD1 (e.g., by stripping CD1 from the NFET) because CD1 is “not good for NFET” devices. *Id.* ¶¶56, 109; *see also id.*, Abstract, ¶39. To further tune performance, Chen explains that a “second metal oxide layer (CD2)” can be “added between the HK gate dielectric (HfO2) and the metal gate (TiN) for the logic NFET” to modulate the work function thereby reducing the threshold voltage. TSMC-1009, ¶¶64, 68, 90-91. Notably, as shown below, Chen teaches that CD1 “may comprise aluminum oxide or aluminum nitride” and examples of CD2 include “LaOx, MgO, BaOx, Y2O3.” TSMC-1009, ¶¶51, 63-64, 91, 97; *see also id.*, FIG. 3F.



TSMC-1009, FIG. 3F (annotated)

H. Overview of Lee

70. Lee discloses a semiconductor device having, among other things, a gate electrode 58. The gate electrode 58 can be formed adjacent to a blocking

insulation layer 56. The blocking insulation layer 56 is made of a conductor having a higher work function than 4.0 eV in order to reduce the probability of charges tunneling through the blocking insulation layer 56. TSMC-1010, ¶82. Lee also discloses that the blocking insulation layer 56 can be made of a conductor, such as metal or P-type doped silicon, which has a higher work function than 4.0 eV of the N-type silicon. *Id.* In other words, the blocking insulation layer 56 can be “made of N-type silicon as well as “a conductor such as metal or P-type doped silicon having a higher work function.” TSMC-1010, ¶82. This metal/silicon layer in Lee corresponds structurally and functionally to the metal layer in Bohr, namely Bohr’s p-type material 162. Lee further discloses that by increasing a work function of the gate electrode, the tunneling probability of charge migrating to a blocking insulation layer from a gate electrode can be reduced. *Id.*, ¶106. As I described below, Lee discloses the claimed *metal layer* in claim 7.

VII. Ground 1A: Claims 1, 2, 4, and 7-11 are anticipated by and/or obvious over Bohr

71. Based on my review, Bohr anticipates and/or renders obvious claims 1, 2, 4, and 7-11 of the ’195 Patent.

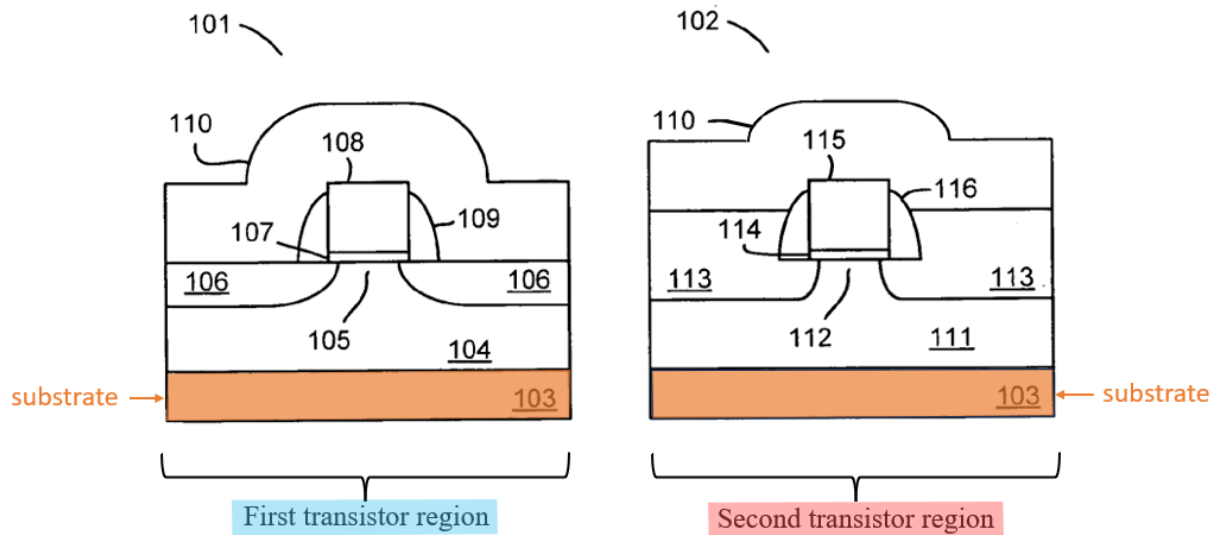
A. Claim 1

[1.pre] A method for fabricating metal gate transistor, comprising:

72. Bohr discloses and/or renders obvious limitation [1.pre]. For example, Bohr discloses methods for making “an NMOS transistor 101 and a PMOS transistor 102 on a substrate 103.” TSMC-1004, ¶17; *see also id.*, claims 1-24 (reciting the method of fabricating NMOS and PMOS transistors having metal gates).

[1.1] providing a substrate having a first transistor region and a second transistor region;

73. Bohr discloses and/or renders obvious limitation [1.1]. For example, Bohr discloses a substrate having a first transistor region and a second transistor region. As shown in annotated figure below, Bohr discloses providing “...an ***NMOS transistor 101*** and a ***PMOS transistor 102*** . . . on a ***continuous substrate 103***.” TSMC-1004, ¶17, FIGS. 1-2. Thus, Bohr discloses providing a substrate (substrate 103) that includes a first transistor region (NMOS transistor 101) and second transistor region (PMOS transistor 102).

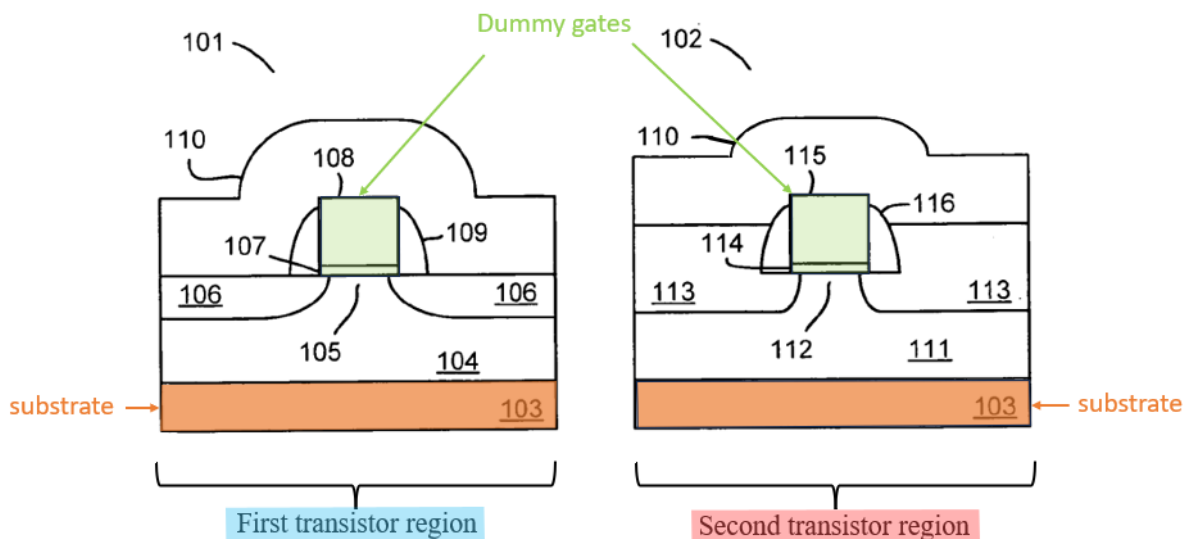


TSMC-1004, FIG. 1 (annotated)

[1.2] forming a plurality of dummy gates on the substrate and within the first transistor region and the second transistor region;

74. Bohr anticipates and/or renders obvious limitation [1.2]. Bohr discloses forming a plurality of dummy gates on the substrate within the first and second transistor regions. In the context of the '195 patent, dummy gates are gate structures that are formed on a substrate, then removed at a late stage and replaced with another gate structures. TSMC-1001 at Abstract, Figs. 2-6.

75. For example, as shown below, Bohr discloses forming dummy gates as ***gate dielectric 107 with gate electrode 108*** and ***gate dielectric with 114 with gate electrode 115***:



TSMC-1004, FIG. 1 (annotated)

76. The *gate dielectric 107 with gate electrode 108* and *gate dielectric 114 with gate electrode 115* are dummy gates because they are later removed and replaced with other gate structures as discussed below for [1.5]. TSMC-1004 ¶¶24, 29, 51; *infra* [1.5].

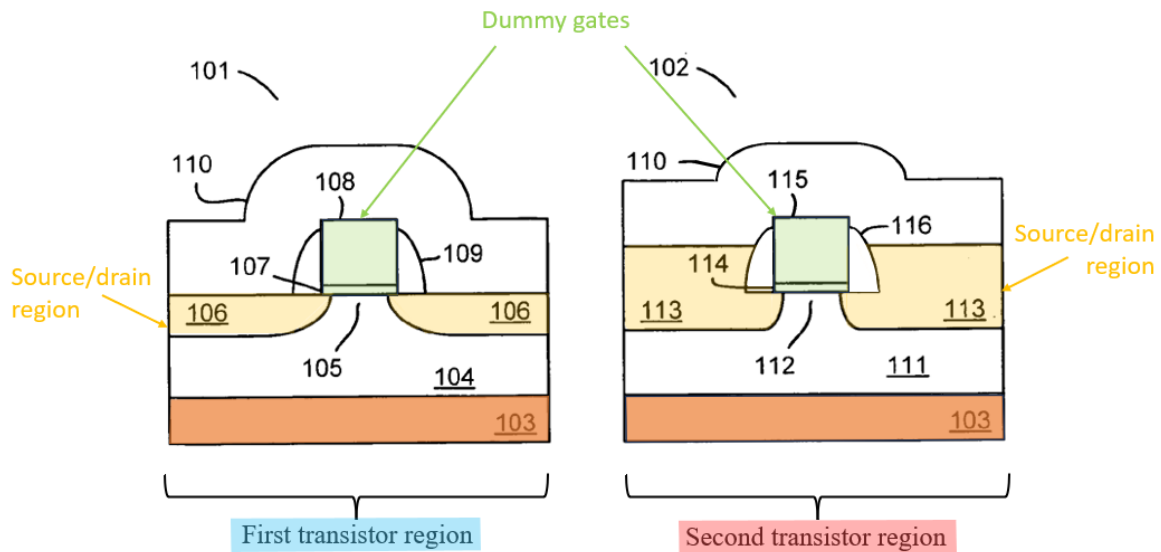
77. I note that Bohr does not expressly use the term “dummy gates” but instead refers to them as “sacrificial” because they are removed in subsequent steps. TSMC-1004 ¶¶24, 29, 51. The term “dummy gate” means a gate that is “sacrificed” (*i.e.*, removed) during formation of the transistor. As explained in Bohr “a portion or an entirety of the gate structure may be removed to enhance the strain in channel 105.” *Id.* ¶29. Therefore, a portion or an entirety of the gate structure may be considered sacrificial.” While the example illustrated here shows both the gate dielectrics 107, 114 and the gate electrodes 108, 115 being removed, the limitation

would also be met by Bohr's disclosure where "a portion" of the gate structure is removed (e.g., when only the gate electrodes 108, 115 are removed). TSMC-1004, ¶¶24, 29; *see also* TSMC-1001, 4:18-27 ("If the gate insulating layer 20 is composed of common dielectric material, the gate insulating layer 20 is preferably removed to expose the substrate 12 underneath"). Even in embodiments where only a portion of the gate structure is removed, the claim does not require complete removal of all gate materials, and Bohr's disclosure therefore satisfies the limitation under its plain and ordinary meaning.

[1.3] forming a source/drain region at two sides of each dummy gate;

78. Bohr discloses and/or renders obvious limitation [1.3]. Bohr discloses forming a source/drain region at two sides of each dummy gate. For example, Bohr discloses forming *source and drain regions 106* and *source and drain films 113* in the first and second transistor regions, respectively. TSMC-1004, ¶¶18-21, 26, 32, 37.

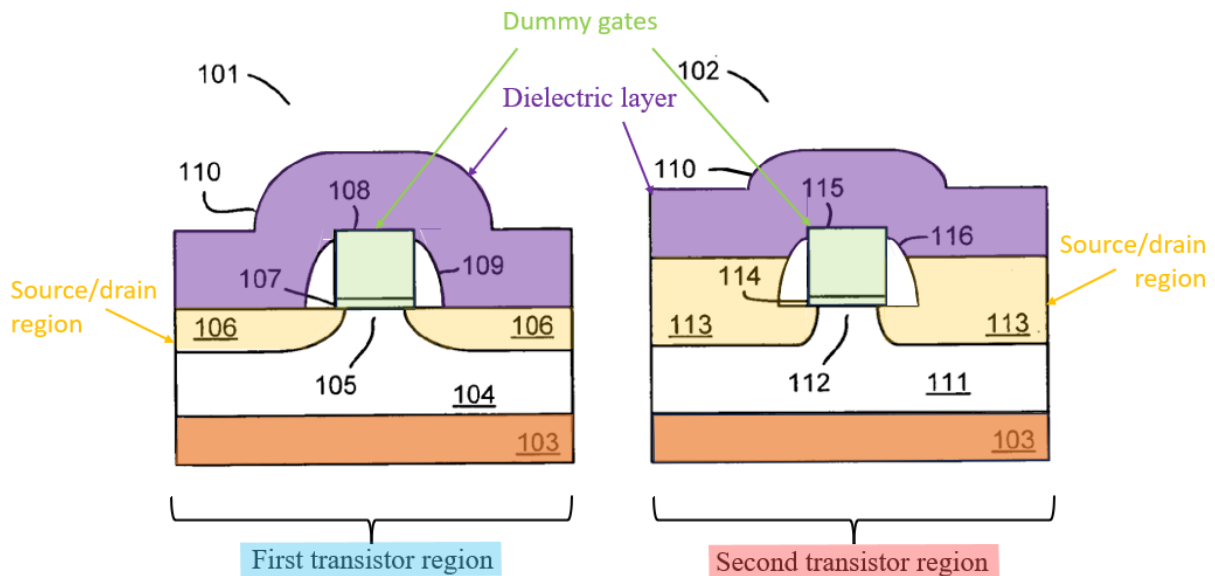
79. As I have shown in annotated FIG. 1 below, the source and drain regions 106 are formed at two sides of the gate dielectric 107 and gate electrode 108, *i.e.*, the claimed dummy gate. Similarly, the source and drain films 113 are formed at two sides of the gate dielectric 114 and gate electrode 115, *i.e.*, another one of the claimed dummy gates.



TSMC-1004, FIG. 1 (annotated)

[1.4] forming a dielectric layer to cover the dummy gates;

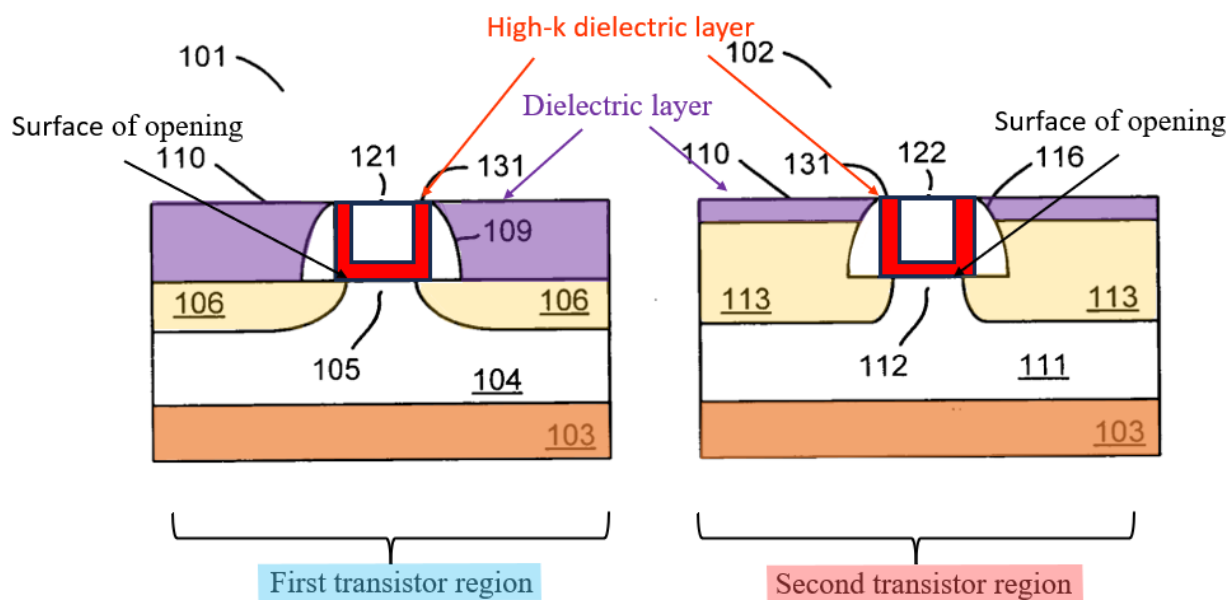
80. Bohr discloses and/or renders obvious limitation [1.4]. Bohr discloses forming a dielectric layer that covers the dummy gates. For example, Bohr discloses that “...a layer 110 may cover NMOS transistor 101 and PMOS transistor 102 and layer 110” and further that this “layer 110 may include a silicon nitride, such as Si_3N_4 .” TSMC-1004, ¶31. Silicon nitride (Si_3N_4), utilized in Bohr’s layer 110, is a well-known dielectric material used in semiconductor fabrication. As shown in annotated FIG. 1 below, Bohr’s layer 110 (*i.e.*, dielectric layer) is disposed over and covers the gate dielectrics/gate electrodes 107/108 and 114/115 (*i.e.*, the dummy gates). *Id.*



TSMC-1004, FIG. 1 (annotated)

[1.5] removing the dummy gates to form a plurality of openings in the dielectric layer of the first transistor region and the second transistor region;

81. Bohr discloses and/or renders obvious limitation [1.5]. Bohr discloses removing the dummy gates to form a plurality of openings in the dielectric layer of the first and second transistor regions. For example, Bohr states that “...***gate electrodes 108, 115 and gate dielectrics 107, 114 may be removed to form trenches 121, 122***” and further that “[***g***]***ate electrodes 108, 115 and gate dielectrics 107, 114*** may be removed by any suitable technique, such as a selective etch technique” (*i.e.*, the dummy gates 107/108 and 114/115). TSMC-1004, ¶35; *see also id.*, ¶36 (“Due to the removal of gate electrodes 108, 115 and gate dielectrics 107, 114 [*i.e.*, the dummy gates], the strain on channels 105, 112 may be increased or enhanced. The increased strain may be due to the removal of material from trenches 121, 122, which

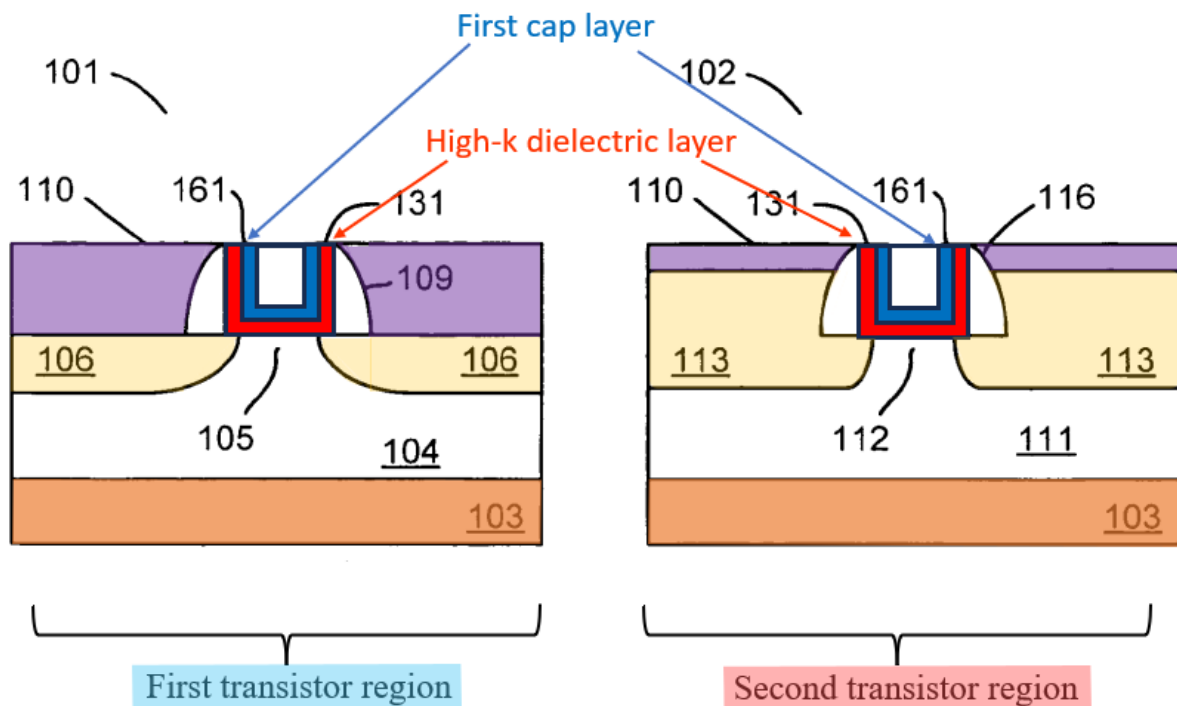


TSMC-1004, FIG. 4 (annotated)

83. Bohr discloses that “[g]ate dielectric 131 may be *any suitable material* and may be formed by any suitable technique” including “*a high-k gate dielectric*, such as hafnium oxide.” *Id.*, ¶38. While FIG. 4 does not show the high-k dielectric layer to cover the dielectric layer, Bohr discloses this when it explains that the “*gate dielectric 131 may also be formed over layer 110 (not shown).*” *Id.*, ¶39. Notably, in annotated FIG. 4 above, Bohr’s high-k dielectric layer is first formed to completely cover the underlying dielectric layer and then removed/patterned through a subsequent processing step. *See id.* (“[G]ate dielectric 131 may be subsequently removed from layer 110 by a CMP process such that gate dielectric 131 only remains in trenches 121, 122.”).

[1.7] depositing a first cap layer on the high-k dielectric layer;

84. Bohr discloses and/or renders obvious limitation [1.7]. Bohr discloses depositing a first cap layer on the high-k dielectric layer. For example, as shown in annotated Fig. 6 below, Bohr discloses that “...an n-type material 161 may be formed in trenches 121, 122.” TSMC-1004, ¶45. Here, Bohr’s n-type material 161 corresponds to the claimed first cap layer, providing a cap on the underlying high-k dielectric layer and serving to modify transistor behavior (e.g., work function) before completion of the gate.



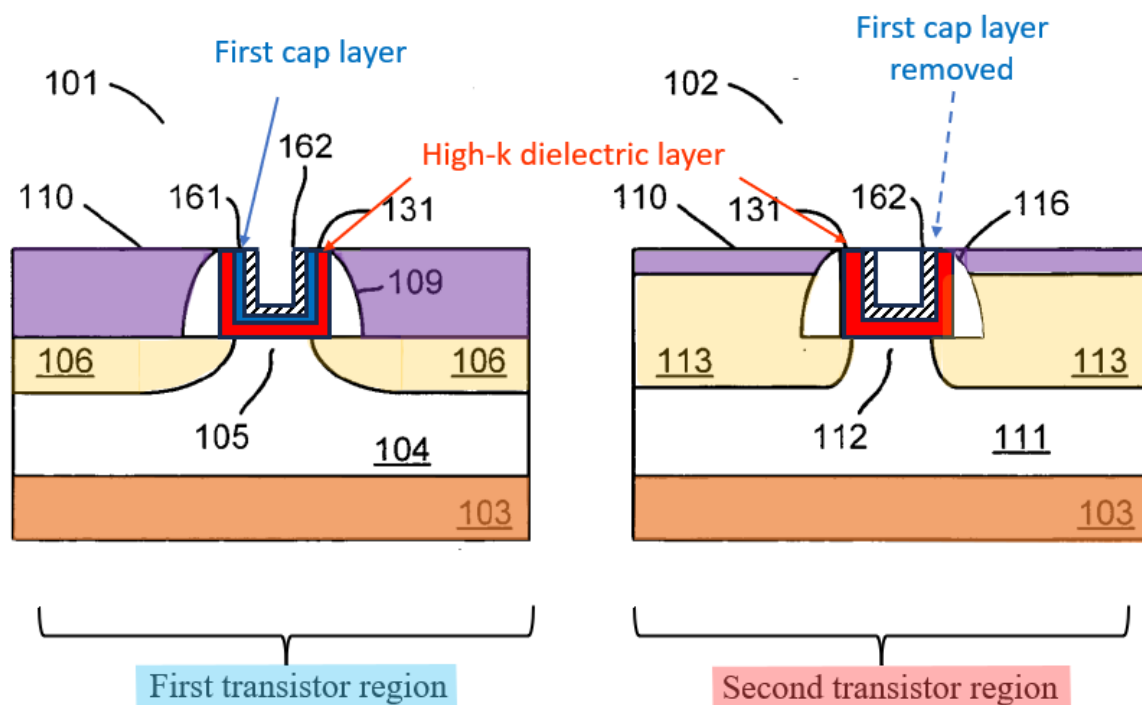
TSMC-1004, FIG. 6 (annotated)

85. Indeed, Bohr discloses that its n-type material 161 can be made from

“any suitable *n-type work function* material”—that is, a material that can be used for work function tuning of the n-type metal. Structurally, Bohr’s n-type material 161 is disposed directly on the high-k dielectric and beneath a subsequently formed metal gate, and functionally it serves the same work-function-modifying role as the claimed first cap layer. TSMC-1004, ¶45. Similarly, the claimed cap layer as mentioned in the ’195 patent is used to “define the *work function of the n-type metal*.” TSMC-1001, 4:42-49. I also understand that Patent Owner acknowledge during prosecution of the ’195 patent that a cap metal layer “may be construed as the first cap layer of the present invention.” TSMC-1002, 88-89 (citing TSMC-1024). Thus, Bohr’s n-type material 161 corresponds to the claimed first cap layer both structurally and functionally, by both providing a cap on the underlying high-k dielectric layer and being used to define the n-type work function. Functionally, Bohr’s n-type material 161 performs the same role as the claimed first cap layer, i.e., modifying the effective work function of the subsequently formed metal gate, and therefore corresponds to that limitation. Accordingly, Bohr’s n-type material 161 corresponds to the claimed first cap layer, and further, a POSITA would have recognized or otherwise found it obvious that Bohr’s n-type material 161 provides the claimed first cap layer.

[1.8] removing the first cap layer disposed in the second transistor region; and

86. Bohr discloses and/or renders obvious limitation [1.8]. Bohr discloses the removal of the first cap layer disposed in the second transistor region. For example, Bohr's n-type material (e.g., n-type material 161), corresponding to the first cap layer, is selectively removed as illustrated in annotated FIG. 7 below. Indeed, referring to FIG. 7, Bohr discloses that "...n-type material 161 may be *selectively removed from PMOS transistor 102* and a p-type material 162 may be formed." TSMC-1004, ¶46.



TSMC-1004, FIG. 7 (annotated)

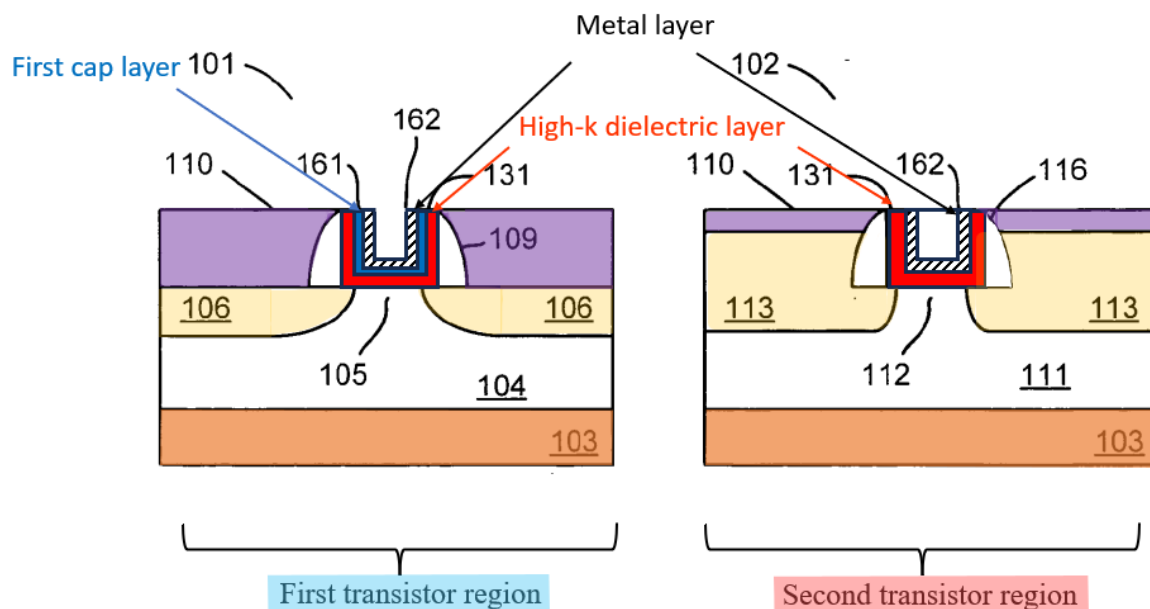
[1.9] forming a metal layer on the first cap layer of the first transistor region and the high-k dielectric layer of the second transistor region.

87. Bohr discloses and/or renders obvious limitation [1.9]. Bohr discloses the formation of a metal layer on the first cap layer of the first transistor region and the high-k dielectric layer of the second transistor region. For example, Bohr's p-type material 162 corresponds the claimed metal layer. Specifically, Bohr discloses that its "the p-type work function material may include ruthenium, palladium, platinum, cobalt, nickel, and their oxides." TSMC-1004, ¶¶42, 46. The enumerated chemicals are known metals that can form the p-type work function material of the p-type material 162. *See* TSMC-1013, 5:28-31.

88. As I have shown in annotated FIG. 7 below, Bohr's p-type material 162 is formed on the n-type material 161 (*i.e.*, the first cap layer) in the NMOS transistor 101, which corresponds to the claimed first transistor region. Turning to the PMOS transistor 102, Bohr shows the p-type material 162 disposed on the high-k dielectric layer 131 in the trench 122. Indeed, Bohr discloses that the "...p-type material 162 may be formed such that an opening remains in either or both of the trenches" and that the "p-type material 162 may complete the gate structure of PMOS transistor 102 or NMOS transistor 101." TSMC-1004, ¶46.

89. Bohr thus discloses the full replacement-gate workflow: dummy gate formation, ILD deposition, dummy removal, trench formation, and gate stack refill

— precisely the architecture claimed in the '195 patent. The claims do not require the metal layer to be deposited in a single step or to exclude additional conductive or work-function-modifying layers, and Bohr's disclosure therefore fully satisfies this limitation.



TSMC-1004, FIG. 7 (annotated)

B. Claim 2

[2] The method of claim 1, wherein the first transistor region is a NMOS transistor region.

90. Bohr discloses and/or renders obvious claim 2. Bohr discloses that the first transistor region is an NMOS transistor region. For example, referring to the analysis of [1.1] above, which is incorporated herein, Bohr discloses that “FIG. 1 illustrates an *NMOS transistor 101* and a *PMOS transistor 102* on a substrate 103”

and that the “**NMOS transistor 101** and PMOS transistor 102 may be on a continuous substrate 103.” TSMC-1004, ¶17; *see also*, TSMC-1004, ¶¶26, 31, 33.

C. Claim 4

[4] The method of claim 1, wherein the second transistor region is a PMOS transistor region.

91. Bohr discloses and/or renders obvious claim 4. Bohr discloses that the second transistor region is a PMOS transistor region. For example, referring to the analysis of [1.1] above, which is incorporated herein, Bohr discloses that “FIG. 1 illustrates an NMOS transistor 101 and a **PMOS transistor 102** on a substrate 103. NMOS transistor 101 and **PMOS transistor 102** may be on a continuous substrate 103.” TSMC-1004, ¶17; *see also*, TSMC-1004, ¶¶18, 20, 31-32.

D. Claim 7

[7] The method of claim 1, wherein the metal layer comprises TiN, TaC, Ta, TaSiN, Al, or TiAlN.

92. Bohr discloses and/or renders obvious claim 7. Specifically, as discussed above for [1.9], Bohr’s p-type material 162 corresponds to the claimed metal layer. Bohr discloses that its metal layer (p-type material 162) can be made from “any suitable p-type work function material” and specifically references the discussion of p-type materials articulated with reference FIG. 5. TSMC-1004, ¶46; *see also id.*, ¶¶40-43. In particular, with reference to FIG. 5, Bohr lists several materials that can be used as part of its p-type gate structure, including “...titanium,

nickel, copper, tin, *aluminum*, lead, zinc, alloys of these metals, or their silicides.”
Id., ¶43.

93. A POSITA further would have found it obvious to utilize one of the gate electrode materials in Bohr’s metal layer (162) for various reasons. For example, because Bohr indicates that any suitable materials may be used for its metal layer, it would have been obvious for a POSITA to look within Bohr’s disclosure for details of known and predictable material options, including other suitable materials, such as Al and TiN, that are known to be used in p-type gate structures. *See e.g.*, TSMC-1023 (explaining that conventional fabrication processes on p-type silicon substrates can use several different materials for metal gates including “TiN.”).

E. Claim 8

[8] The method of claim 1, further comprising performing a first chemical mechanical polishing process after forming the dielectric layer and before removing the dummy gate.

94. Bohr discloses and/or renders obvious claim 8. Bohr discloses a first chemical mechanical polishing process that occurs after forming the dielectric layer and before removing the dummy gate. For example, referring to FIGS. 1 and 2, Bohr discloses that “a portion of layer 110,” which corresponds to the claimed dielectric layer, “may be removed to expose gate electrode 108 and gate electrode 115” and that this “portion of layer 110 may be removed by *a planarization or chemical mechanical polishing (CMP) process.*” TSMC-1004, ¶34. Indeed, referring to FIG.

1-3 of Bohr, an optional CMP process is performed on the non-planar structure shown in FIG. 1, thereby resulting in the planarized structure shown in FIG. 2, before removing the dummy gate as shown in FIG. 3. *See* TSMC-1004, FIGS. 1-3, ¶¶5-7. and *supra* §VI.A. As a POSITA would further have known, Bohr's CMP step occurs after the deposition of the layer 110 (*i.e.*, dielectric layer) because Bohr discloses that a portion of the deposited layer 110 is to be removed by CMP. The CMP step also occurs before removal of the dummy gate, as Bohr goes on to explain that, in a subsequent step, "...gate electrodes 108, 115 and gate dielectrics 107, 114" are to be "removed to form trenches 121, 122." TSMC-1004, ¶35. Indeed, a POSITA would understand or otherwise find it obvious to use such a CMP process to fully expose the underlying polysilicon for the subsequent selective etching/trench forming step to occur. CMP was the industry-standard planarization technique for dielectric and metal layers at the relevant time, and its use here would have been automatic to a POSITA.

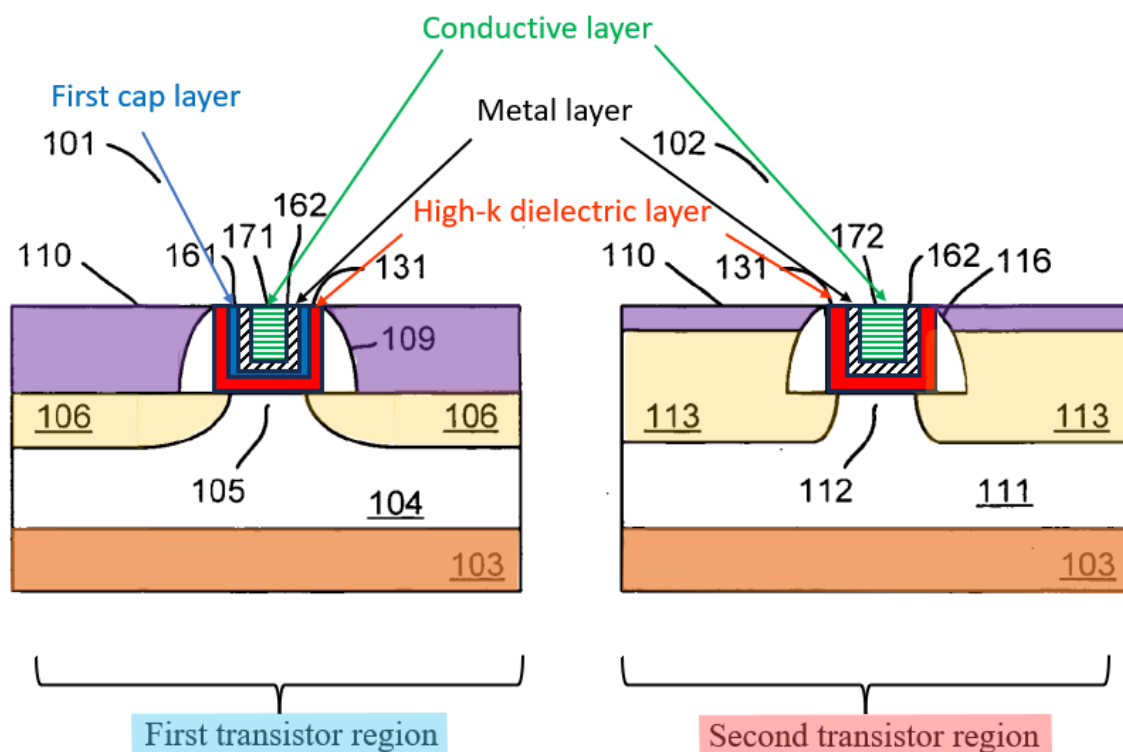
F. Claim 9

[9.pre] The method of claim 1, further comprising:

[9.1] forming a conductive layer to fill the openings of the first transistor region and the second transistor region after forming the metal layer on the first cap layer of the first transistor region and the high-k dielectric layer of the second transistor region; and

95. Bohr discloses and/or renders obvious limitations [9.pre] and [9.1].

Bohr discloses the formation of a conductive layer to fill the openings of the first and second transistor regions. For example, Bohr discloses “...*fill material 171 and fill material 172* may be selectively formed” and that they “may be chosen based on their *conductive properties*.” TSMC-1004, ¶47. Bohr identifies tungsten as a material that could be used for both fill material 171 and fill material 172, which are respectively formed on the metal layer on the first cap layer of the first transistor region and the high-k dielectric layer of the second transistor region as illustrated below. Fill material 171 and 172 thus disclose the claimed conductive layer.



TSMC-1004, FIG. 8 (annotated)

[9.2] performing a second chemical polishing after forming the conductive layer.

96. Bohr discloses and/or renders obvious limitation [9.2]. Bohr discloses performing a second chemical polish after the formation of the conductive layer. For example, as discussed above for [9.1], Bohr discloses that its conductive layer (*e.g.*, fill materials 171, 172) is “selectively formed,” TSMC-1004, ¶47. A POSITA would recognize that this phrase (“selectively formed”) discloses or renders obvious this claim limitation because CMP was the industry-standard planarization technique to selectively form a layer by removing only the undesired portion of a deposited material. Notably, Bohr discloses removing materials through CMP. TSMC-1004, ¶34; *see also id.*, ¶39. Indeed, using CMP to selectively remove conductive layers was exceedingly well-known and was a common component of semiconductor processing. TSMC-1006, Abstract, 75-79 (describing a method of chemical mechanical polishing, specifically, chemical mechanical polishing of tungsten filled contact holes including using a lower down-pressure CMP to polish overfilled nail heads of CVD deposited tungsten and tungsten particles deposited on the surface of dielectric); TSMC-1007, Abstract, 815 (describing a planarization process for metal plugs using CMP), 816 (describing a CMP for aluminum plugs), 817; *see also supra* §§VI.D-E.

97. To the extent that Bohr doesn’t expressly mention performing CMP on

its conductive layer (following its formation), a POSITA further would have found the same to be obvious. As noted, Bohr's fill material 171, 172 corresponds to the claimed conductive layer. A POSITA would have understood that depositing metal into plugs or holes can result in uneven surfaces and thus needs to be planarized to create the desired even surface. *See* TSMC-1007, 815; TSMC-1006, Abstract, 75, 78-79. Thus, the POSITA would have looked to the only planarization technique mentioned in Bohr, namely CMP, to achieve the same.

G. Claim 10

[10] The method of claim 1, wherein the high-k dielectric layer comprises HfSiO, HfSiON, HfO, LaO, LaAlO, ZrO, ZrSiO, or HfZrO.

98. Bohr discloses and/or renders obvious claim 10. For example, Bohr discloses that “[g]ate dielectric 131 may be any suitable material” and further “may include a high-k gate dielectric, such as *hafnium oxide*” as well as “*hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide*, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide aluminum oxide, lead scandium tantalum oxide, or lead zinc niobate.” TSMC-1004, ¶38.

H. Claim 11

[11] The method of claim 9, wherein the conductive layer comprises Al, W, TiAl or CoWP.

99. Bohr discloses and/or renders obvious claim 11. For example, Bohr discloses that “[f]ill material 172,” which corresponds to the claimed conductive layer, may be made from “any suitable material” including “boron carbide, *tungsten*, molybdenum, rhodium, vanadium, platinum, ruthenium, beryllium, palladium, cobalt, titanium, nickel, copper, tin, *aluminum*, lead, zinc, alloys of these metals, or their silicides.” TSMC-1004, ¶48.

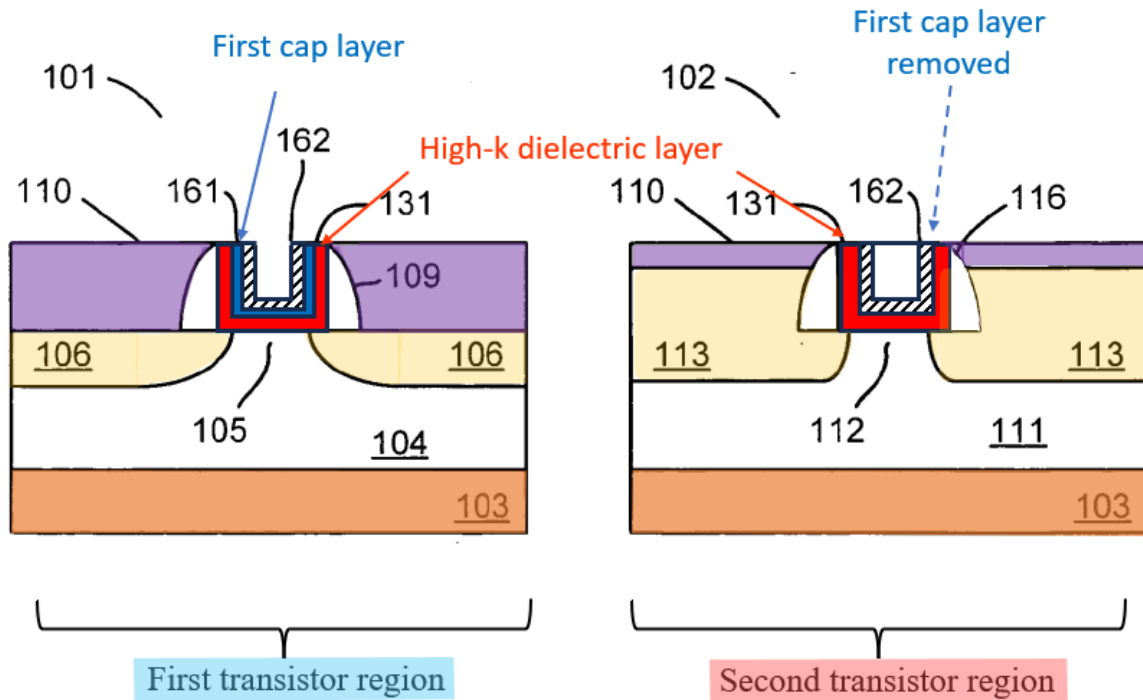
VIII. GROUND 1B: Claim 3 is obvious over Bohr in view Chen

100. Based on my review, Bohr in view of Chen renders obvious claim 3 of the ’195 Patent.

A. Claim 3

[3] The method of claim 2, wherein the first cap layer comprises LaO, MgO, Dy₂O₃, or other lanthanide oxides.

101. Bohr in view of Chen renders obvious claim 3. For example, Bohr in view of Chen renders obvious the first cap layer made of at least one of the materials recited in limitation [3]. As discussed above for claim 1, Bohr discloses a first cap layer (n-type material 161). *Supra* Ground 1A, [1.7].



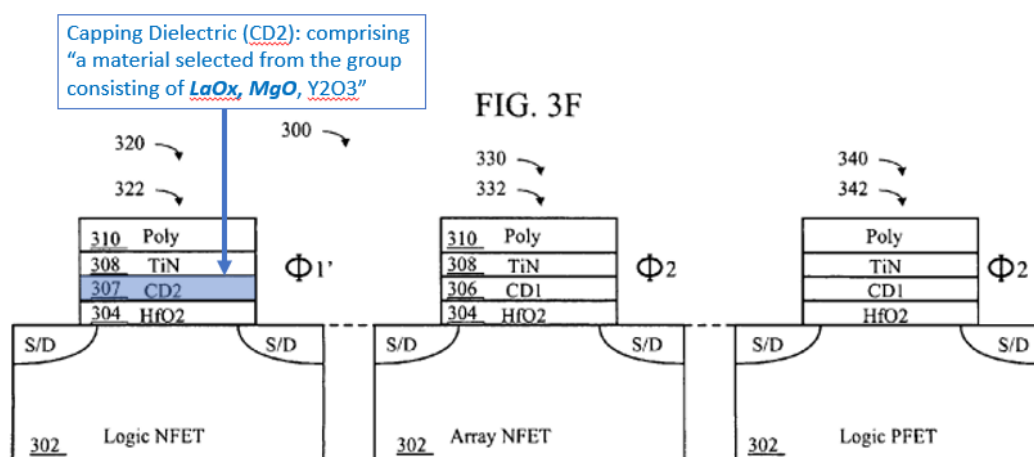
TSMC-1004, FIG. 7 (annotated)

102. Bohr explains that this cap layer “161 may be any suitable n-type work function material” and lists various examples including “hafnium, zirconium, titanium, tantalum, aluminum, their alloys, or carbides of those metals.” TSMC-1004, ¶¶40, 45.

103. Chen discloses depositing “second metal oxide layer (CD2) [*i.e.*, “second capping dielectric]” on “the high-K dielectric layer” for a logic NFET transistor.² TSMC-1009, ¶¶64, 68, 90-91 (“CD’ is short for capping dielectric.”),

² I note that Chen’s NFET and Bohr’s NMOS refer to the same type of transistor

FIG. 3F. Chen explains that the second capping dielectric (“CD2”) can “comprise a material selected from the group consisting of *LaOx*, *MgO*, BaOx, and Y2O3.” TSMC-1009, ¶64, *see also id.*, ¶¶68, 90-91 (“NFET CD2 (metal oxide 2) is a capping dielectric for logic NFET: *LaOx*, *MgO*, BaOx, Y2O3”), 114, FIG. 3F. Chen explains that the second capping dielectric is used to tune the work function for the gate. *See* TSMC-1009, ¶¶90-91, 114, *see also id.*, ¶¶55-56, 77; *supra* §VI.G.



TSMC-1009, FIG. 3F (annotated)

(*i.e.*, a n-channel metal-oxide-semiconductor field-effect transistor). *See* TSMC-1017, 2:31-34 (explaining that “in integrated circuit designs using both PFET and NFET transistors and CMOS technology (in which the logic is implemented principally by complementary PMOS and NMOS transistor pairs)”). Likewise, Chen’s PFET and Bohr’s PMOS refer to the same type of transistor (*i.e.*, a p-channel metal-oxide-semiconductor field-effect transistor). *Id.*

104. It would have been obvious to a POSITA to use Chen's second capping dielectric in place of Bohr's layer 161. Although Bohr discloses that its n-type material 161 can be made from "any suitable n-type work function material," it does not explicitly mention that "LaO, MgO, Dy₂O₃, or other lanthanide oxides" may be used. TSMC-1004, ¶45. Yet a POSITA would have found it obvious to utilize one of the above-mentioned materials of Chen for NFET in Bohr's cap layer (n-type material 161) for various reasons.

105. For example, because Bohr indicates that any suitable materials may be used for its first cap layer, it would have been obvious for a POSITA to look to other sources, such as Chen, for details of known and predictable material options.

106. Further, a POSITA would find it obvious to utilize one of Chen's second capping dielectric materials for NFET in connection with Bohr's first cap layer (*i.e.*, n-type material 161) for the purpose of modulating the work function, adjusting threshold voltage, and/or differentiating PFET/PMOS and NFET/NMOS behavior on the same substrate. TSMC-1009, ¶¶58, 60, 90-91, 109, 114; *supra* Footnote 2.

107. In light of Chen's disclosure, a POSITA would understand that lanthanum oxides (*i.e.*, "LaOx") or other similar materials (*i.e.*, "MgO") for NFET can be utilized in Bohr's first cap layer (*i.e.*, n-type material 161) for the NMOS because both were known to improve the ability to adjust or tune the work function

for NFET/NMOS gates. Additionally, a POSITA would understand that the standard deposition/etching processes used for forming the cap layer in Bohr would be fully compatible with the specific second capping dielectric materials disclosed in Chen.

108. In other words, the combination would have amounted to a merely obvious application of Chen's material options to Bohr's device, which was ripe for improvement and in a manner that would yield no more than predictable results. A POSITA would have had a reasonable expectation of success implementing the combination.

109. Both metal and dielectric materials were well known materials for cap layers used for work function tuning. I understand that Patent Owner even acknowledged during prosecution that a cap metal layer "may be construed as the first cap layer of the present invention," while the specification of the '195 patent describes the first cap layer as comprising dielectric materials. TSMC-1002, 88-89 (citing TSMC-1024). Moreover, several references demonstrate that it was common to use *LaO* as cap layer for tuning the work function of an NMOS gate. For example, Tigelaar (TSMC-1021) demonstrates that various materials for a dielectric capping layer were known. TSMC-1009, ¶¶85 (describing a "dielectric capping layer" which is used to "tune the workfunction of a gate electrode"), 86 (explain that that a variety of materials can serve as the "dielectric capping layer," including "***LaO(N)***, *AlO(N)*, *AlN*, *DyO(N)*, *ScO(N)*, *GdO(N)*, *CeO(N)*, *TbO(N)*, *ErO(N)*, *YbO(N)* or any

combination thereof.”); *see also id.* ¶¶11-12, 14-15, 30, 91. Substitution of a known material (metal) for another known material (dielectric) is a straightforward application of ordinary skill and creativity. *See also* TSMC-1023 (explaining that “La₂O₃ interfacial layer can be used to achieve *n*-type metal gate performance on Hf-based gate dielectrics”); Similarly, Chang (TSMC-1020) explains that a gate dielectric capping for a NMOS transistor “preferably [comprises] a lanthanide-based dielectric” because it is a dielectric element with more electropositive atoms. TSMC-1020, ¶54 (“In one embodiment, wherein the first transistor comprises a PMOS transistor and *wherein the second transistor comprises a NMOS transistor*, the first gate dielectric capping layer comprises preferably a dielectric element with higher electronegativity compared to another dielectric element from the second gate dielectric capping layer. The first gate dielectric capping layer comprises preferably the dielectric element with more electronegative atoms, whereas *the second gate dielectric capping layer comprises preferably the another dielectric element with more electropositive atoms*. The first gate dielectric capping layer may comprise preferably an aluminum-based dielectric, i.e. AlO, AlN, AlON and mixtures thereof, whereas *the second dielectric capping layer may comprise preferably a lanthanide-based dielectric*, i.e. any of DyO(N), *LaO(N)*, ScO(N), GdO(N), TbO(N), YbO(N), ErO(N) and mixtures thereof.”).

110. Moreover, a POSITA would have also been motivated to incorporate

Chen's capping dielectric materials into Bohr's process because these materials were widely explored in the industry for work-function engineering in advanced high-k metal gate nodes, offering improved band-offset control, better thermal stability, and enhanced PMOS tuning, among others. *See e.g.*, TSMC-1021, ¶¶85-86; TSMC-1020, ¶54. Substituting one known work-function-adjusting dielectric for another would have been considered a routine material selection consistent with standard scaling roadmaps and integration targets.

IX. GROUND 1C: Claim 5 is obvious over Bohr in view of Yu

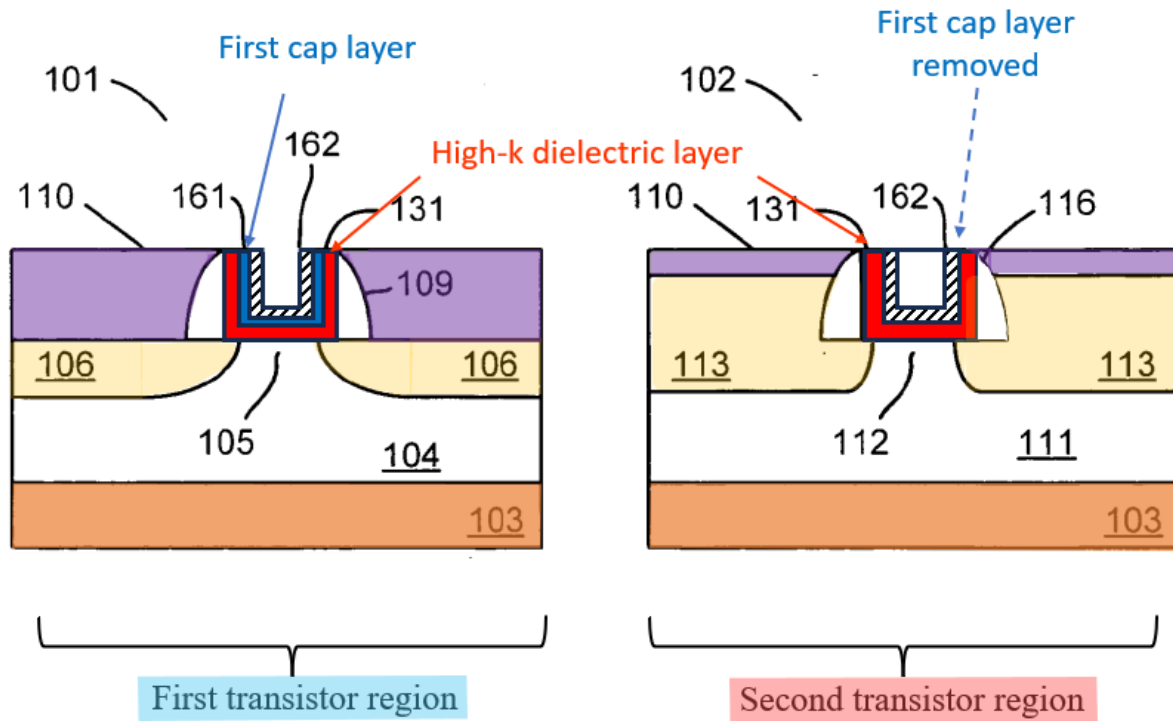
111. Based on my review, Bohr in view of Yu renders obvious claim 5 of the '195 Patent.

A. Claim 5

[5] The method of claim 4, further comprising forming a second cap layer in the second transistor region after removing the first cap layer from the second transistor region.

112. Bohr in view of Yu renders obvious claim 5. For example, Bohr in view of Yu renders obvious the formation of a second cap layer in the second transistor region [5], as claimed. Specifically, Bohr describes the removal of the first cap layer from the second transistor region, as shown in annotated FIG. 7 below. TSMC-1004, FIG. 7; *see also id.*, ¶46 (“...n-type material 161 may be selectively removed from PMOS transistor 102 and a p-type material 162 may be formed.”). Here, as

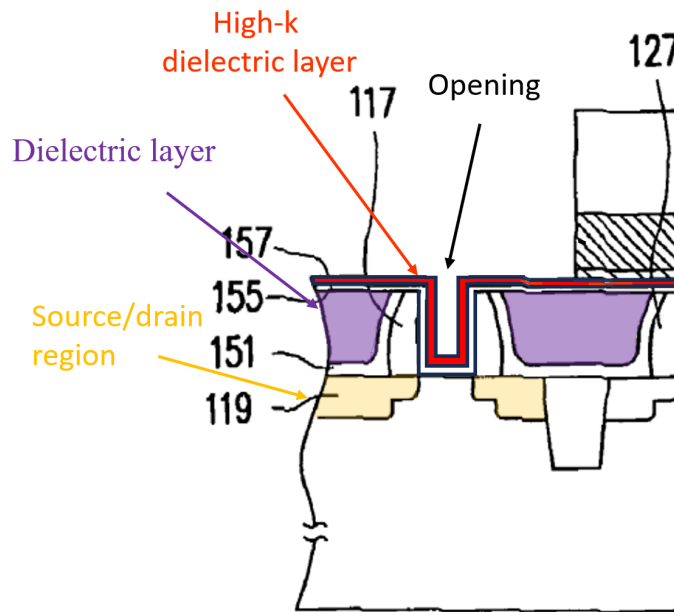
explained for [1.7], Bohr's material 161 corresponds to the claimed first cap layer that is removed in the second transistor region.



TSMC-1004, FIG. 7 (annotated)

113. Now referring to FIGS. 1C-1D, Yu discloses that after a patterned photoresist layer 154 is removed, a dielectric layer 155, a high-k dielectric layer 157, a second type conductive layer 161, and a low resistance conductive layer 163 are sequentially formed on the substrate 100. TSMC-1008, ¶45. A patterned photoresist layer 165 is also formed on the low resistance conductive layer 163, which fills an opening 181. The patterned photoresist layer 165 and the low resistance conductive layer 163 are disposed above the first type source/drain 119. TSMC-1008, ¶47. Subsequently, the patterned photoresist layer 165 is removed and

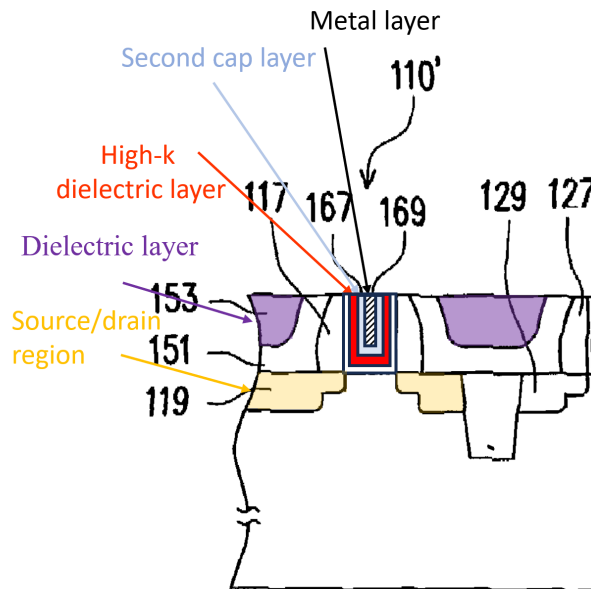
a *first type conductive layer 167* and *low resistance conductive layer 169* are *sequentially formed*. TSMC-1008, ¶48.



TSMC-1008, FIG. 1D-1 (annotated)

114. While Bohr does not explicitly disclose a second cap layer, a POSITA would have recognized or otherwise found it obvious that (i) Yu's first type conductive layer 167 corresponds to the claimed second cap layer and (ii) Yu's low resistance conductive layer 169 corresponds to the claimed metal layer. For example, Yu discloses that its "*first type conductive layer 167 is disposed above the first type doped region 107 and on the high-k dielectric layer 157*, and is disposed along an exposed side surface of the low resistance dielectric layer 157 and an exposed upper surface of the high-k dielectric layer 157 in the opening 187" and that its "*low*

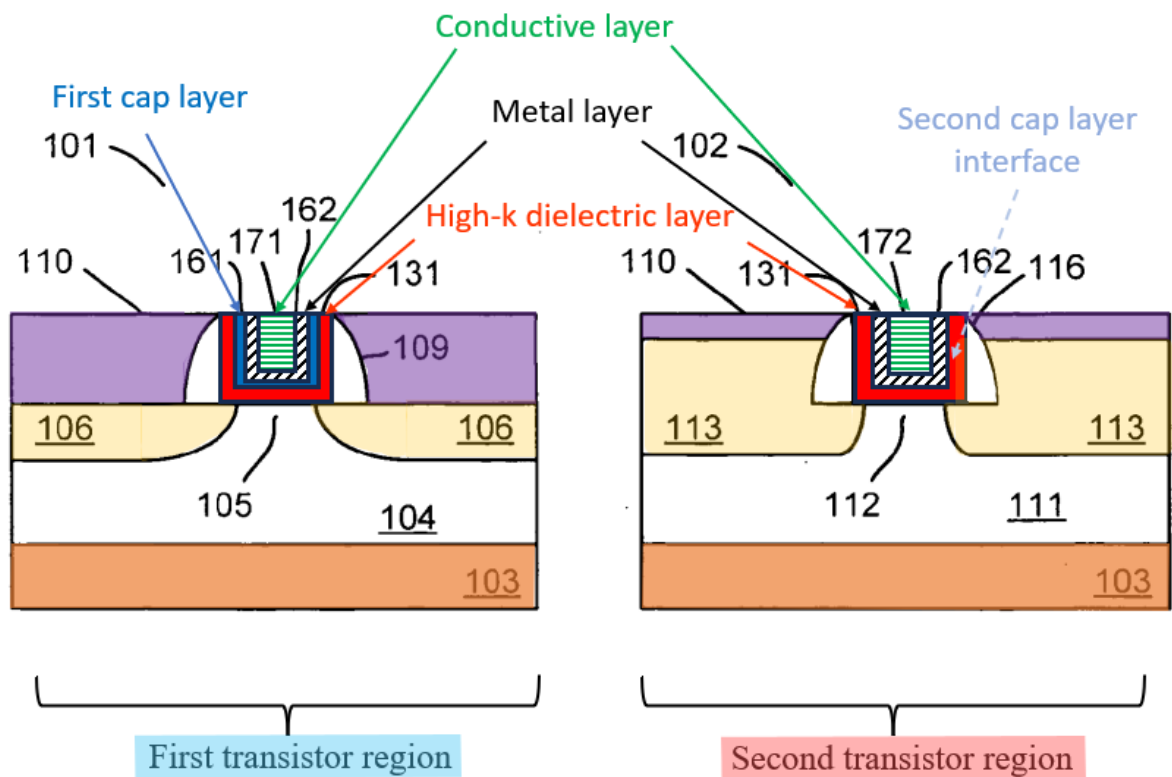
resistance conductive layer 169 is disposed on the first type conductive layer 167 and fills in the opening 187.” TSMC-1008, ¶51; *see also id.*, ¶30. That is, as shown in annotated FIG. 1E-1 below, Yu discloses a second cap layer (167) disposed over a high-k dielectric layer (157) and then a metal layer (169) disposed over the second cap (167).



TSMC-1008, FIG. 1E-1 (annotated)

115. A POSITA would have found it obvious and been motivated by multiple reasons to use a second cap layer as in Yu in Bohr’s device. For example, referring to annotated FIG. 8 of Bohr below, a POSITA would have found it obvious in view of Yu to dispose a metal layer over Bohr’s high-k dielectric layer (131), after removal of the first cap layer (161), for the purpose of “improving the stability of the transistor.” TSMC-1008, ¶56. A POSITA would have also recognized that

including a second cap layer (e.g., at the location indicated by “second cap layer interface” in the annotated drawing below), which is different from the first cap layer, in the second transistor region would allow the work function of its NMOS and PMOS transistors to be independently tuned. See TSMC-1021, ¶11 (explaining that “[t]o tune the workfunction of NMOS and PMOS transistors independently it may be necessary to put different dielectric materials or a different dielectric capping layer on the NMOS and PMOS transistor.”).



TSMC-1004, FIG. 8 (annotated)

116. Such modification of Bohr in view of Yu would have amounted merely to an obvious application of Yu’s well-known techniques to Bohr’s device, which

was ripe for improvement and in a manner that would yield no more than predictable results. A POSITA would have had a reasonable expectation of success implementing the combination.

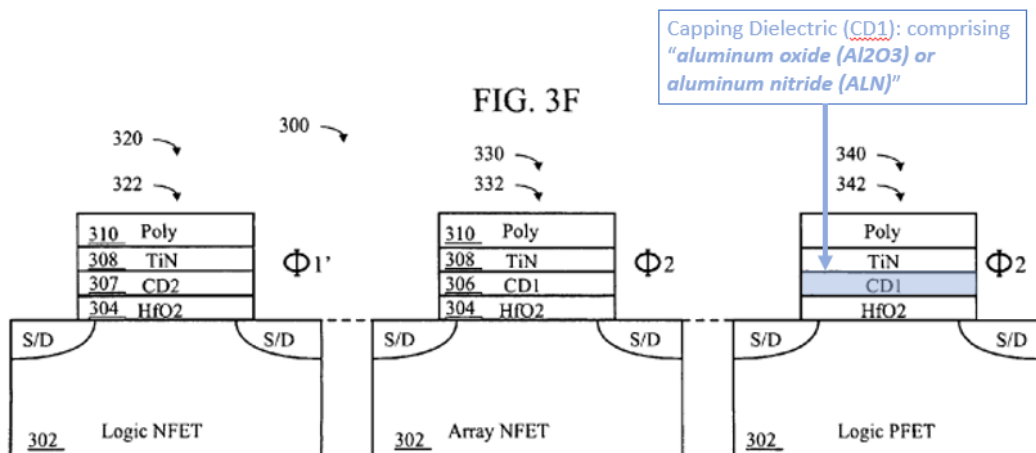
X. GROUND 1D: Claim 6 is obvious over Bohr in view of Yu and Chen

117. Based on my review, Bohr in view of Yu and Chen renders obvious claim 6 of the '195 Patent.

A. Claim 6

[6] The method of claim 5, wherein the second cap layer comprises Al₂O₃, AlN, or AlON.

118. Bohr in view of Yu and Chen renders obvious claim 6. Bohr in view of Yu (as described above for Ground 1C) further in view of Chen renders obvious this feature. For example, Chen discloses a first capping dielectric ("CD1") comprising "Aluminum Oxide (*Al₂O₃*)" or "Aluminum Nitride (*AlN*)."^{¶91}, *see also* 51, 63, 97; *supra* §VI.G. Chen explains that CD1 is used to tune the PFET. TSMC-1009, ^{¶¶}58, 91; *supra* §VI.G.



TSMC-1009, FIG. 3F (annotated)

119. For reasons similar to those discussed above with respect to [3], a POSITA would be motivated to use “aluminum oxide or aluminum nitride” as a material for Bohr’s second cap layer, in order to modulate the work function, adjust threshold voltage, and/or differentiate PMOS and NFET behavior on the same substrate. TSMC-1009, ¶¶51, 90-91, 109-110; *supra* §VIII.A. That is, in the combination, Yu’s first type conductive layer 167 corresponds to the second cap layer. A POSITA, in possession of Chen, would find it obvious to utilize “Al₂O₃” or “AlN” in Yu’s second cap layer (167), because of Chen’s disclosure for using such materials to modulate the work function of the PFET.

120. In fact, before the critical date, using an “AlN” capping layer on a high-k dielectric layer was well known. *See* TSMC-1023 (“We have previously reported that AlN interfacial layer can be used to achieve p-type metal gate on Hf-based gate dielectrics.”); *see also* TSMC-1021, ¶11, 84-85 (“the second dielectric material 203

may comprise a dielectric material which can tune the workfunction of a gate electrode...[s]uch a dielectric material is often referred to as dielectric capping layer”), 86 (“The dielectric material may comprise, e.g., LaO(N), AlO(N), *AlN*, DyO(N), ScO(N), GdO(N), CeO(N), TbO(N), ErO(N), YbO(N) or any combination thereof or any other dielectric material which can tune the workfunction of a dielectric/metal interface, e.g. a dielectric/metal control electrode interface, e.g. a dielectric/metal gate electrode interface.”); TSMC-1020, ¶54 (“In one embodiment, *wherein the first transistor comprises a PMOS transistor* and wherein the second transistor comprises a NMOS transistor, *the first gate dielectric capping layer comprises preferably a dielectric element with higher electronegativity compared to another dielectric element from the second gate dielectric capping layer. The first gate dielectric capping layer comprises preferably the dielectric element with more electronegative atoms*, whereas the second gate dielectric capping layer comprises preferably the another dielectric element with more electropositive atoms. *The first gate dielectric capping layer may comprise preferably an aluminum-based dielectric, i.e. AlO, AlN, AlON* and mixtures thereof, whereas the second dielectric capping layer may comprise preferably a lanthanide-based dielectric, i.e. any of DyO(N), LaO(N), ScO(N), GdO(N), TbO(N), YbO(N), ErO(N) and mixtures thereof.”).

121. Such modification of Bohr would have amounted to a merely obvious

application of Chen's material options to Bohr's device, which was ripe for improvement and in a manner that would yield no more than predictable results. A POSITA would have had a reasonable expectation of success implementing the combination.

122. Moreover, a POSITA would have been motivated to combine Yu's conductive/cap layer configuration with Chen's first capping dielectric ("CD1") materials because both references address the same industry need: reliable tuning of NMOS/PMOS work functions in dual-metal-gate flows. Integrating such teachings into Bohr's replacement-gate structure would have been a predictable and widely adopted approach to achieving tighter threshold voltage control, reducing leakage, and meeting manufacturing yield requirements for CMOS technologies.

XI. GROUND 1E: Claim 7 is obvious over Bohr in view of Lee

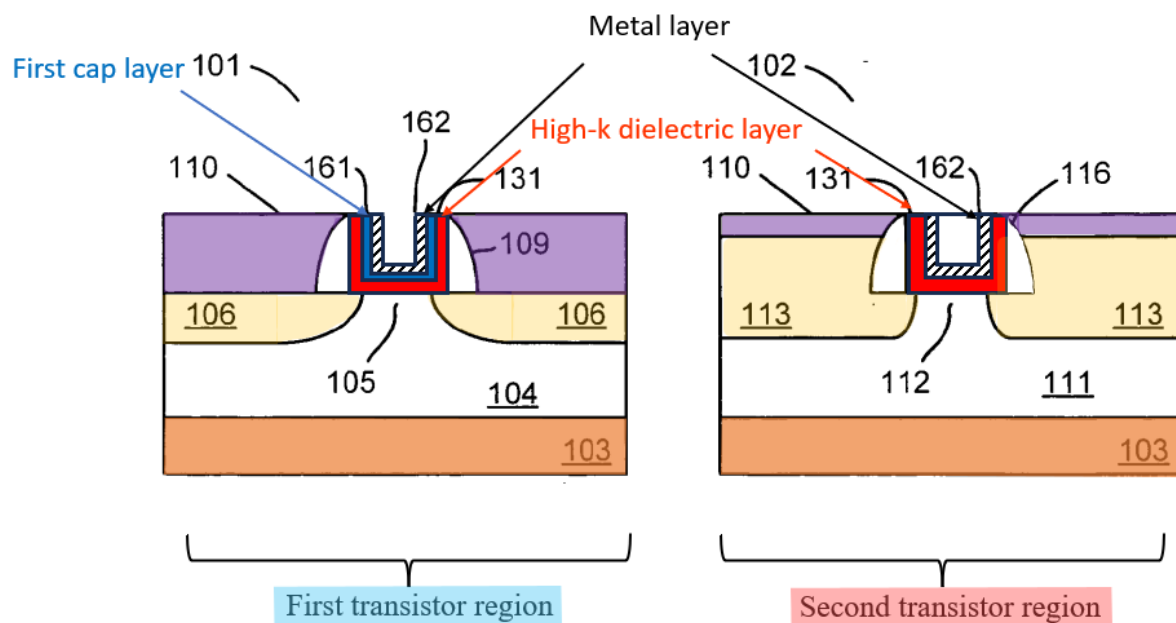
123. Based on my review, Bohr in view of Lee and Chen renders obvious claim 7 of the '195 Patent.

A. Claim 7

[7] The method of claim 1, wherein the metal layer comprises TiN, TaC, Ta, TaSiN, Al, or TiAlN.

124. Bohr in view of Lee renders obvious Claim 7. Specifically, as discussed above for [1.9] and further illustrated below, Bohr's p-type material 162 corresponds to the claimed metal layer. The corresponding layer in Lee, namely its layer 58, can

be made from various materials such as “P-type silicon, Ti, *TiN*, TaN, TaTi, *TaSiN*, *Ta*, W, Hf, HfN, Nb, Mo, RuO₂, RuO, Mo₂N, WN, WSi, NiSi, Ti₃Al, *Ti₂AlN*, Pd, Ir, Pt, Co, Cr, CoSi, NiSi, and AlSi.” TSMC-1010, ¶82.



TSMC-1004, FIG. 7 (annotated)

125. Although Bohr discloses that its metal layer (p-type material 162) can be made from any suitable material, it does not explicitly mention that “*TiN*, *TaC*, *Ta*, *TaSiN*, *Al*, or *TiAlN*” may be used. TSMC-1004, ¶46; *see also id.*, ¶¶42-43. Yet a POSITA would have found it obvious to utilize one of the above-mentioned materials of Lee in Bohr’s metal layer for various reasons. For example, because Bohr indicates that any suitable materials may be used for its metal layer but otherwise provides little detail about the specific types of materials that can be used, it would have been obvious for a POSITA to look to other sources, such as Lee, for

details of known and predictable material options. Such a modification of Bohr in view of Lee combination would have amounted to a merely obvious application of Lee's material options to Bohr's device, which was ripe for improvement and in a manner that would yield no more than predictable results. A POSITA would have had a reasonable expectation of success implementing the combination.

XII. GROUND 1F: Claims 9 and 10 are obvious over Bohr in view of Wang or Amazawa

126. While Ground 1A demonstrates that limitation [9.2] is disclosed or otherwise rendered obvious by Bohr alone, Ground 1B relies on the even more explicit disclosures of Wang and Amazawa to reach this feature, as well as dependent Claim 11. Integration of Wang or Amazawa does not disturb the mapping of Bohr to other claim elements. To avoid repetition, and because the analysis of all other claim elements is identical, I only address the pertinent portions of Claims 9 and 11—namely limitation [9.2]—in this section. The unaddressed elements of Claims 9 and 11 are disclosed by Bohr as I demonstrated above for Ground 1A. *See supra* §VII.

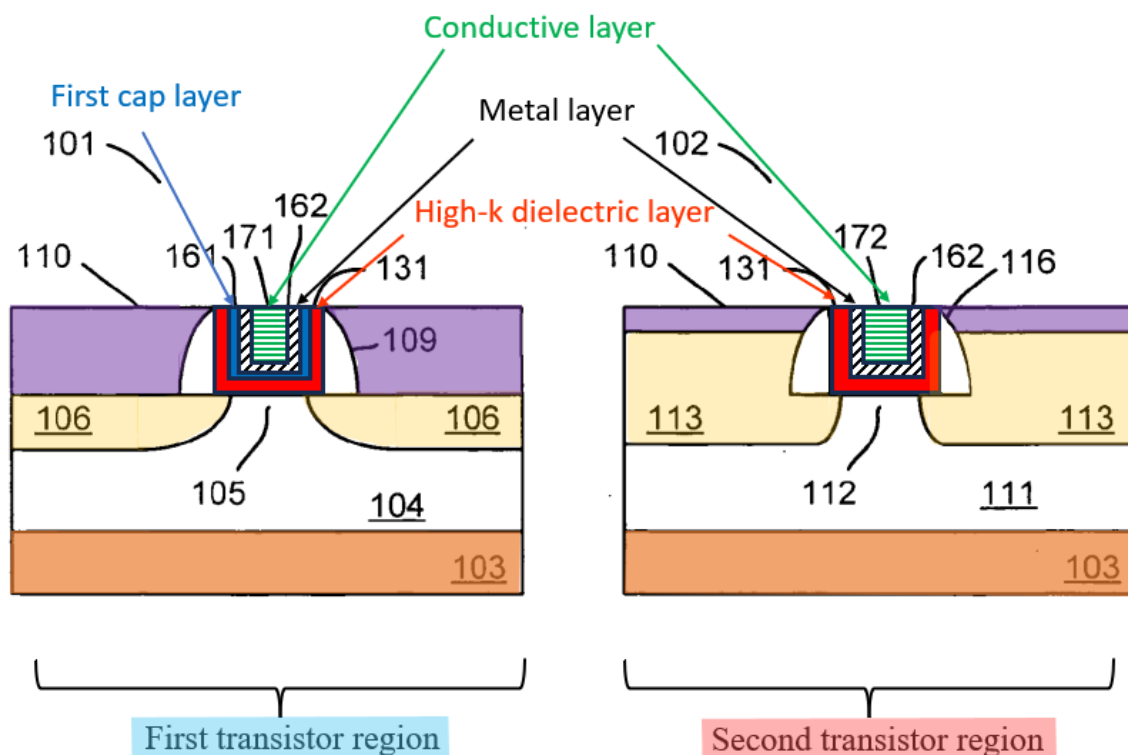
A. Claims 9 and 11

[9.2] performing a second chemical polishing after forming the conductive layer.

127. To the extent that Bohr does not teach the second chemical polishing

step after formation of the conductive layer as recited in limitation [9.2], Bohr in view of Wang or Amazawa renders such a step obvious.

128. Referring to my analysis of [9.1] above, the fill materials 171, 172 of Bohr (*i.e.*, conductive layer) were selectively formed as shown below:



TSMC-1004, FIG. 8 (annotated)

129. Although Bohr does not explicitly mention what processing was performed after deposition of the fill materials 171, 172 to yield the resulting configuration, it would have been obvious for a POSITA to turn to well-known planarization techniques, such as CMP, for example as taught by Wang and Amazawa, for details on how to achieve the structural configuration of fill materials

171, 172 in Bohr.

130. Wang, for instance, discloses a method of chemical mechanical polishing for tungsten filled contact holes. TSMC-1006, Abstract, 75-76. Wang explains that a metal, like tungsten, can overfill contact holes during deposition to ensure that the holes are completely filled. *Id.*, 76. Similarly, Bohr discloses that its conductive layer (fill material 171 and fill material 172) can be made of tungsten. *See* TSMC-1004, ¶¶47-48. A POSITA would have found it obvious to perform a second CMP step after depositing Bohr's conductive layer with a metal (*e.g.*, tungsten) to form the selectively polished and smooth fill structure that is shown in FIG. 8 of Bohr.

131. Similarly, Amazawa discloses a planarization process for selectively deposited metal plugs using a chemical mechanical polishing (CMP). *See* TSMC-1007, Abstract, 815. More specifically, Amazawa describes the selective deposition of via holes or openings with aluminum. TSMC-1007, 815-816. Then, utilizing a CMP process, "Al plugs are completely planarized," after being selectively filled. TSMC-1007, 816. Amazawa explains that such selective formation of Al plugs via CMP "is very simple and . . . much easier to control" compared to other methods. *Id.* Thus, a POSITA would have found it obvious to perform CMP on Bohr's device after depositing the conductive layers 171, 172 to simply and reliably create a "flush" surface. TSMC-1007, 816.

132. The combinations of Bohr with Wang/Amazawa, as described above, amount to an obvious application of known processing techniques as shown in Wang/Amazawa, applied to a known device structure as described in Bohr, which was ready for improvements that would yield predictable results. Bohr does not impose any restrictions on the types of planarization methods that can be used on its conductive layer, and in fact explicitly details the use of CMP in other layers. A POSITA would have been motivated to incorporate the CMP teachings of Wang or Amazawa into Bohr's process because CMP of metal-filled trenches had become a universal, standardized fabrication step in sub-100-nm technology nodes, highly effective for reducing topography, preventing voids, improving yield, and/or ensuring reliable metal-gate formation. Leveraging CMP to planarize Bohr's conductive fill would have been viewed as a routine, predictable enhancement aligned with industry-wide backend and replacement-gate process flows.

133. Accordingly, a POSITA would have had a reasonable expectation of success implementing the proposed modification. Thus, claim 9 and its dependent claim 11, are obvious in view of the above. *See supra* §VII.H (Ground 1A, Limitation [11]) (explaining that Bohr's "[f]ill material 172" corresponds to the claimed conductive layer and may be made from "any suitable material" including "*tungsten*" or "*aluminum*", thereby satisfying claim 11. TSMC-1004, ¶48.).

**XIII. GROUND 2A: Claims 1, 2, 4, and 7-11 anticipated by and/or obvious
over Brask**

134. Based on my review, Brask anticipates and/or renders obvious claims 1, 2, 4, and 7-11 of the '195 Patent.

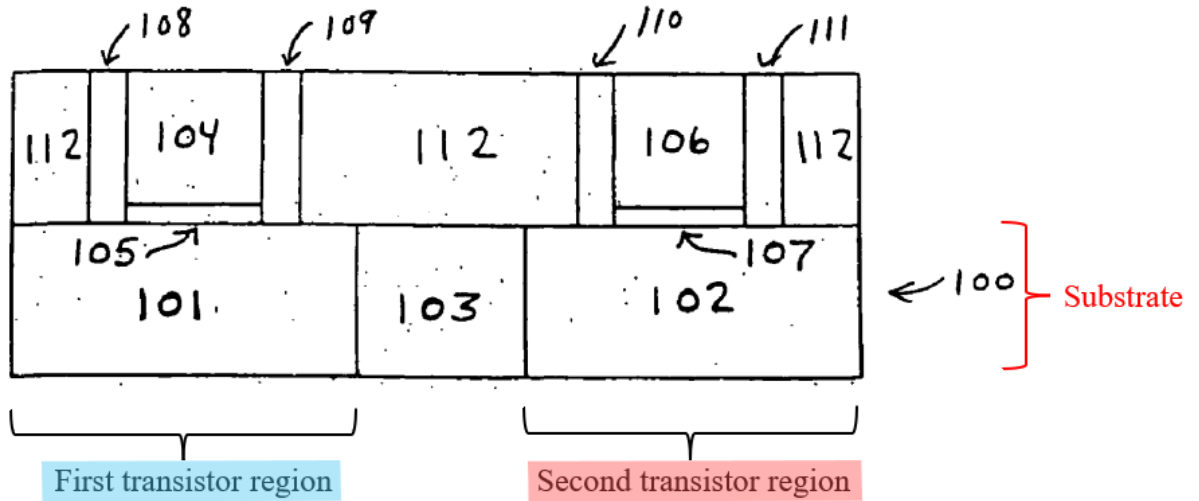
A. Claim 1

***[1.pre] A method for fabricating metal gate transistor,
comprising:***

135. Brask discloses and/or renders obvious limitation [1.pre]. For example, Brask discloses “methods for making semiconductor devices, in particular, semiconductor devices that include metal gate electrodes.” TSMC-1005, ¶1; *see also id.*, ¶¶2, 25-29.

***[1.1] providing a substrate having a first transistor region
and a second transistor region;***

136. Brask discloses and/or renders obvious limitation [1.1]. For example, Brask discloses a substrate having a first transistor region and a second transistor region. Specifically, as shown below, Brask discloses a substrate having an intermediate “structure [that] includes first part 101 [*i.e.*, first transistor region] and second part 102 [*i.e.*, second transistor region] of substrate 100.” TSMC-1005, ¶13, FIG. 1a.

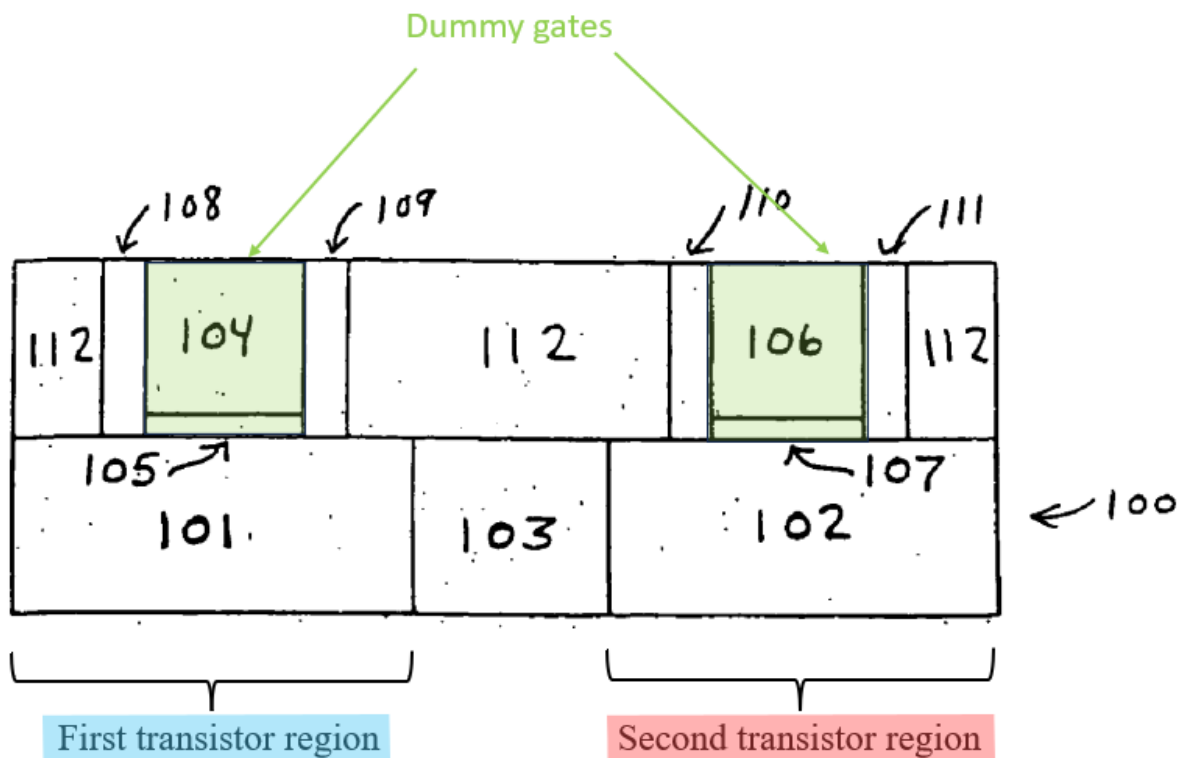


TSMC-1005, FIG. 1A (annotated)

[1.2] forming a plurality of dummy gates on the substrate and within the first transistor region and the second transistor region;

137. Brask discloses and/or renders obvious limitation [1.2]. Brask discloses forming a plurality of dummy gates on the substrate. For example, Brask discloses that a “[f]irst polysilicon layer 104 is formed on dielectric layer 105, and second polysilicon layer 106 is formed on dielectric layer 107.” TSMC-1005, ¶13. Brask discloses that “[a]fter forming the FIG. 1 a structure, first and second polysilicon layers 104, 106 are removed” and then dielectric “layers 105, 107 are removed.” TSMC-1005, ¶¶19, 24; *see also id.*, ¶¶22, 40 (“After forming the FIG. 2 a structure, polysilicon layers 104, 122 and dielectric layer 105 are removed”). The layers 104/105 and layers 106/107 are dummy gates because these structures are formed in the dielectric 112 and then subsequently etched away to form gates structures. TSMC-1005, ¶¶19, 22-24; *see* TSMC-1012, 2:27-33 (“Silicon nitride (SiN), or

polysilicon, in a thickness of between about 150 nm to 500 nm is deposited by plasma enhanced chemical vapor deposition (PECVD), to form what is referred to as a “dummy” gate, or a place-holder gate. Place-holder gates 22, 24 are formed in the PMOS and NMOS, respectively these are formed by photolithography and anisotropic plasma etching of the nitride, or polysilicon, with the etching stopping at the level of the gate oxide. The gate oxide may be partially etched or may be completely removed during this etch process”). Thus, Brask’s first polysilicon layer 104 with dielectric layer 105 and its second polysilicon layer 106 with dielectric layer 107 correspond to the claimed plurality of dummy gates.



TSMC-1005, FIG. 1a (annotated)

138. This annotated FIG. 1a, shows dummy gates 104, 105 and 106, 107 formed “on substrate 100” of Brask. TSMC-1005, ¶25, 39 (“*polysilicon layers 104, 122* that are formed on *dielectric layer 105, which is formed on substrate 100.*”), FIG. 2a.

[1.3] forming a source/drain region at two sides of each dummy gate;

139. Brask discloses and/or renders obvious limitation [1.3]. Brask discloses forming a source/drain (S/D) region at two sides of each dummy gate. For example, Brask discloses “...source and drain regions...that may be formed using conventional processes.” TSMC-1005, ¶16. The source and drain regions are formed at two sides of each dummy gate. This is evident because Brask’s device is a complementary metal oxide semiconductor (CMOS) device having a complementary pair of NMOS and PMOS field-effect transistors (FETs). TSMC-1005, ¶3, 13, 51. In such FETs, the source and drain regions are necessarily formed at the sides of the dummy gate structure because this allows the metal gate to be formed in a position that allows for the creation of a conductive channel through which an electrical current can flow between the source and the drain when a voltage is applied to the metal gate. TSMC-1022, 5:14-60 (“When an input voltage is applied to the gate electrode 103, a transverse electric field is set up in the channel region 107. By varying the transverse electric field, it is possible to modulate the conductance of the channel region 107

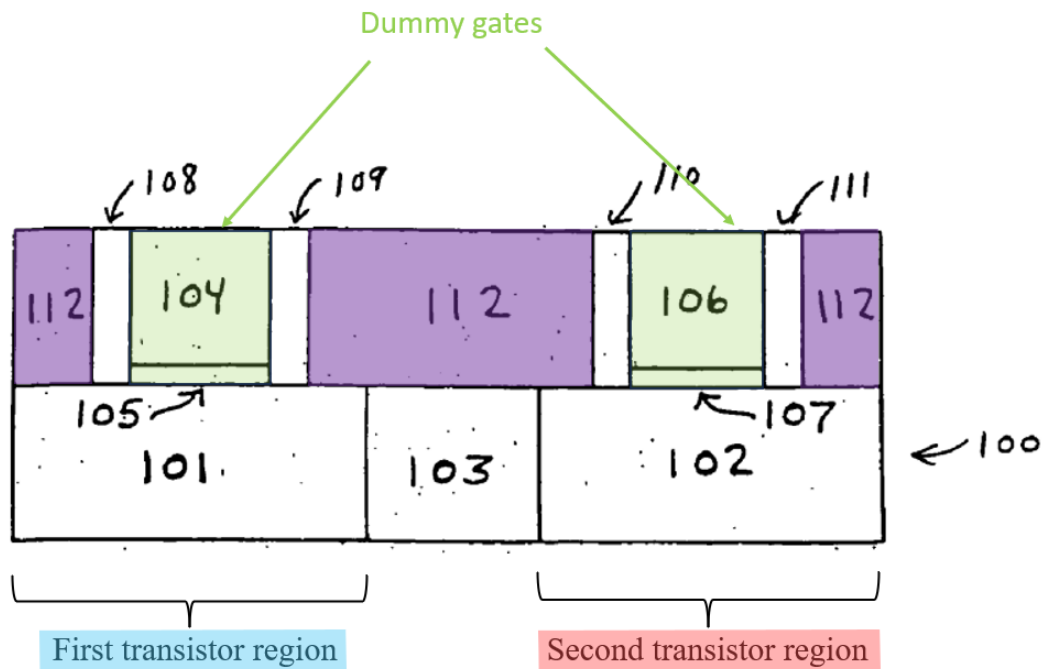
between the source region and the drain region. In this manner, an electric field controls the current flow through the channel region 107. This type of device is commonly referred to as a MOS field-effect-transistor (MOSFET).”); TSMC-1030, [0005]-[0007] (“The source/drain 14 are in the two sides of the gate structure 12 in the substrate 10.”), [0019], [0026], [0029], [0036], FIG. 6; TSMC-1025, 3:12-33 FIGS. 7, 16; TSMC-1026, [0002], [0031]-[0033]. The forming of the source and drain regions at each of the dummy gates is therefore implicitly and inherently disclosed in Brask.

140. To the extent that Brask does not disclose forming the S/D region at two sides of each dummy gate, a POSITA would understand that the S/D region would be formed at two sides of Brask’s first polysilicon layer 104 and second polysilicon layer 106. For example, Brask discloses that “[w]hen source and drain regions are formed using conventional ion implantation and anneal processes, it may be desirable to form a hard mask on polysilicon layers 104, 106—and an etch stop layer on the hard mask—to protect layers 104, 106 when the source and drain regions are covered with a silicide.” TSMC-1005, ¶17. Brask also discloses that “[w]hen ion implantation processes are used to form the source and drain regions, layers 104, 106 may be doped at the same time the source and drain regions are implanted. In such a process, first polysilicon layer 104 may be doped n-type, while second polysilicon layer 106 is doped p-type—or vice versa.” TSMC-1005, ¶18. In view of

Brask's disclosures regarding its source and drain regions and their relationship to the dummy gates, and further in view of the abundantly well-known concept of positioning a source/drain region at two sides of each dummy gate in order to create a functioning semiconductor device, a POSITA would have recognized or otherwise found it obvious that Brask's source/drain regions are formed at two sides of its dummy gate. See TSMC-1004, FIG. 1; TSMC-1012, FIG. 1.

[1.4] forming a dielectric layer to cover the dummy gates;

141. Brask discloses and/or renders obvious limitation [1.4]. Brask discloses forming a dielectric layer to cover the dummy gates. For example, Brask Figure 1a discloses “[d]ielectric 112 [that] lies next to the sidewall spacers [108, 109].” TSMC-1005, ¶13.

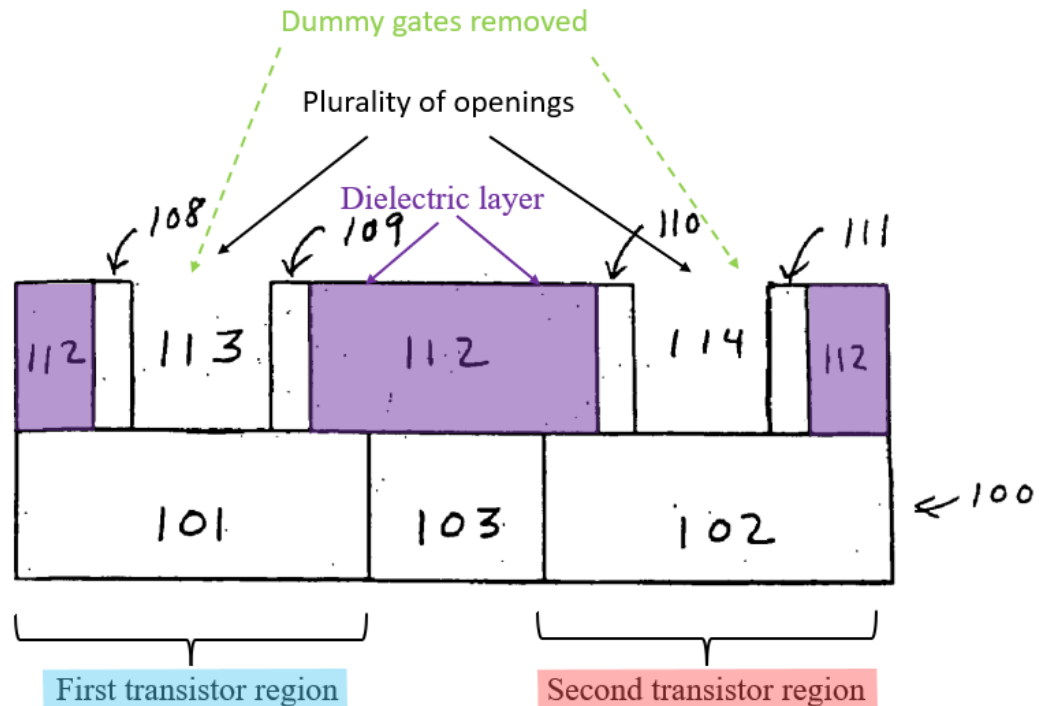


TSMC-1005, FIG. 1a (annotated to show the dielectric layer before and after being polished back to cover the dummy gates)

142. Although Figure 1a shows dielectric layer 112 on the sides of the gate, Brask further discloses that its “*dielectric 112 may be polished back...to expose first and second polysilicon layers 104, 106.*” TSMC-1005, ¶16. In order to expose the first and second polysilicon layers 104/105, 106/107 (*i.e.*, dummy gates) by polishing back the dielectric 112, the dielectric 112 would have been first deposited over the dummy gates 104/105, 106/107 to cover them before being polished back.

[1.5] removing the dummy gates to form a plurality of openings in the dielectric layer of the first transistor region and the second transistor region;

143. Brask discloses and/or renders obvious limitation [1.5]. Brask discloses removing the dummy gates to form a plurality of openings in the dielectric layer as claimed. For example, Brask describes and illustrates the formation of trenches 113, 114 in the dielectric layer 112 after removal of the polysilicon layers 104, 106 and dielectric layer 105, 107. Specifically, Brask discloses that “[a]fter forming the FIG. 1 a structure, first and second polysilicon layers 104, 106 are removed” and then dielectric “layers 105, 107 are removed.” TSMC-1005, ¶¶19, 24; *see also id.*, ¶¶22, 40 (“After forming the FIG. 2 a structure, polysilicon layers 104, 122 and dielectric layer 105 are removed”).



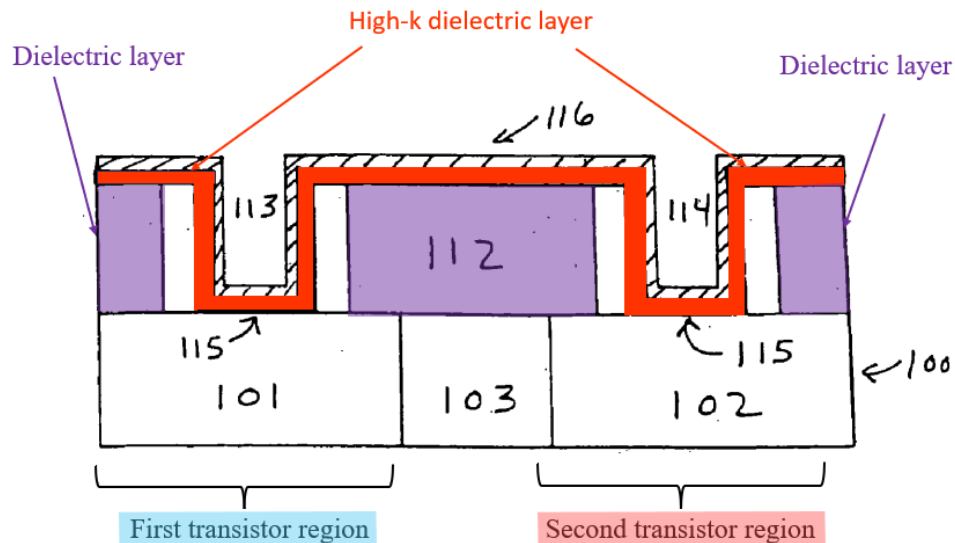
TSMC-1005, FIG. 1b (annotated)

Brask discloses that the “...removal of dielectric layers 105, 107 *leaves trenches 113, 114* within dielectric layer 112 positioned between sidewall spacers 108, 109, and sidewall spacers 110, 111 respectively.” *Id.* Thus, a plurality of openings are formed in the dielectric layer of the first transistor region and the second transistor region following removal of the dummy gates.

[1.6] forming a high-k dielectric layer to cover the dielectric layer and surface of each opening;

144. Brask discloses and/or renders obvious limitation [1.6]. Brask discloses forming a high-k dielectric layer over the surface of each opening. For example, as illustrated below, Brask discloses that “[a]fter removing dielectric layers 105, 107,

dielectric layer 115 is formed on substrate 100” where the “dielectric layer 115 comprises a *high-k gate dielectric layer*.” TSMC-1005, ¶25. In an implementation, Brask discloses that “an atomic layer CVD process is used to form high-k gate dielectric layer 115, that layer will form on the sides of trenches 113, 114.” *Id.*, ¶27.

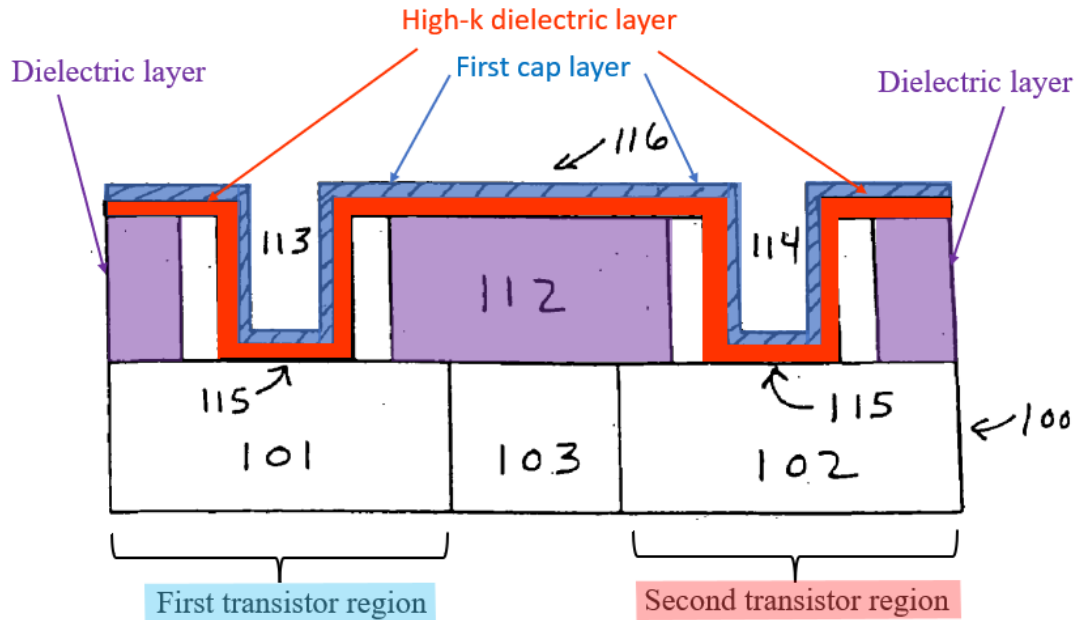


TSMC-1005, FIG. 1c (annotated)

[1.7] depositing a first cap layer on the high-k dielectric layer;

145. Brask discloses and/or renders obvious limitation [1.7]. Brask discloses depositing a first cap layer disposed on the high-k dielectric layer. In one mapping, Brask’s metal layer 116, which as shown in annotated FIG. 1c below is deposited on the high-k dielectric layer (*i.e.*, dielectric layer), corresponds to the claimed first cap layer. More specifically, Brask discloses its “metal layer 116 is formed directly on [high-k dielectric] layer 115” and that the “[m]etal layer 116 may comprise any

conductive material from which a metal gate electrode may be derived, and may be formed on high-k gate dielectric layer 115 using well known PVD or CVD processes.” TSMC-1005, ¶31. Although Brask refers to layer 116 as a metal layer, it occupies the same intermediate position between the high-k dielectric layer and a subsequently formed gate-filling metal, and therefore functions as a cap layer under the ’195 Patent’s plain-meaning usage.



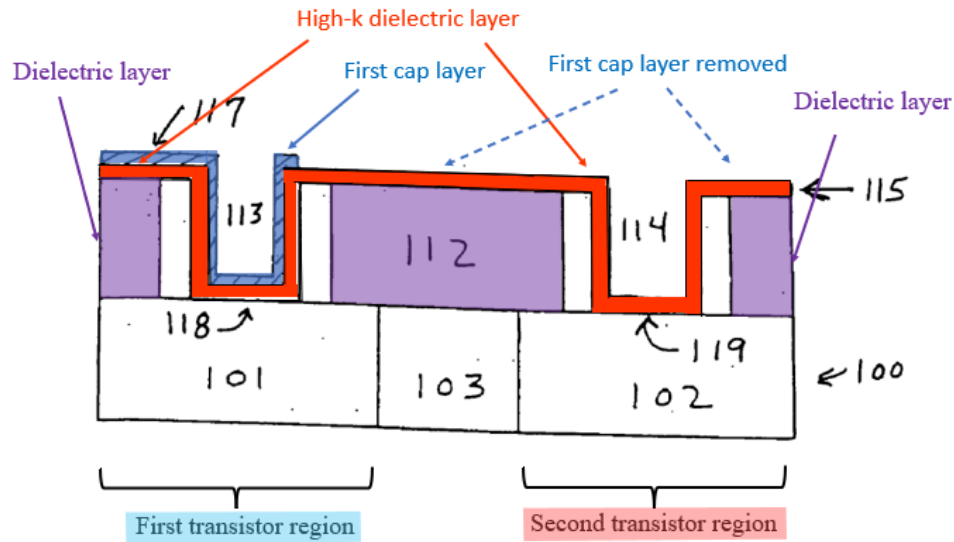
TSMC-1005, FIG. 1c (annotated)

146. Notably, Brask uses its metal layer 116 for the same purpose that the '195 patent uses its capping layer. Specifically, the '195 patent states that its capping layer is used to “define the work function.” TSMC-1001, 4:42-49. Similarly, Brask uses its metal layer 116 for the same purpose. TSMC-1005, ¶32 (“[w]hen metal layer

116 comprises an n-type material, layer 116 preferably has a workfunction that is between about 3.9 eV and about 4.2 eV”; “[w]hen metal layer 116 comprises a p-type material, layer 116 preferably has a workfunction that is between about 4.9 eV and about 5.2 eV.”). I note that Patent Owner stated during prosecution acknowledged that a cap metal layer “may be construed as the first cap layer of the present invention.” TSMC-1002, 88-89 (citing TSMC-1024). Accordingly, Brask’s metal layer 116 corresponds to the claimed first cap layer both structurally and functionally, and further, a POSITA would have recognized or otherwise found it obvious that Brask’s metal layer 116 provides the claimed first cap layer.

[1.8] removing the first cap layer disposed in the second transistor region; and

147. Brask discloses and/or renders obvious limitation [1.8]. Brask discloses removing the first cap layer that is disposed in the second transistor region, as illustrated in annotated FIG. 1d below.



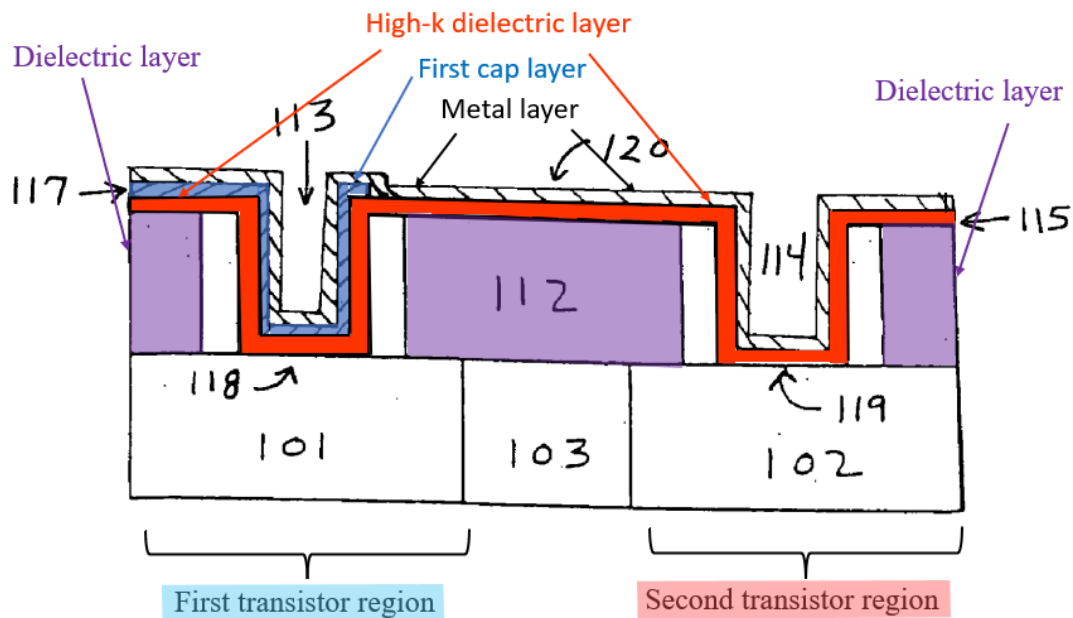
TSMC-1005, FIG. 1d (annotated)

148. Brask explains the removal of metal layer 116 from the second transistor region as follows: “After forming metal layer 116 on high-k gate dielectric layer 115, part of metal layer 116 is masked,” and “[t]he exposed part of metal layer 116 is then removed, followed by removing any masking material, to generate the structure of FIG. 1d.” *Id.* The result is that the metal layer is removed from the second transistor region as claimed.

[1.9] forming a metal layer on the first cap layer of the first transistor region and the high-k dielectric layer of the second transistor region.

149. Brask discloses and/or renders obvious limitation [1.9]. Brask discloses forming a metal layer on the first cap layer of the first transistor region and the high-k dielectric layer of the second region. For example, as shown in annotated Figure 1e below, Brask’s second metal layer 120 is formed on the first cap layer (*e.g.*, metal layer 116 and first metal layer 117) of the first transistor region (*e.g.*, a region over

the first part 101 of the substrate 100). TSMC-1005, FIG. 1e. Brask's second metal layer 120 is formed on the high-k dielectric layer (e.g., high-k gate dielectric layer 115) of the second transistor region (e.g., first metal layer 117 is formed after etching metal layer 116), as shown below. *Id.*



TSMC-1005, FIG. 1e (annotated)

B. Claim 2

[2] The method of claim 1, wherein the first transistor region is a NMOS transistor region.

150. Brask discloses and/or renders obvious claim 2. Brask discloses that the first transistor region is an NMOS transistor region. For example, Brask discloses that “[w]hen ion implantation processes are used to form the source and drain regions, layers 104, 106 may be doped at the same time the source and drain regions

are implanted” and that “[i]n such a process, ***first polysilicon layer 104 may be doped n-type***, while second polysilicon layer 106 is doped p-type—or vice versa.” TSMC-1005, ¶18; *see also id.*, ¶23. A POSITA would understand that the n-type doped source and drain region in the first part indicates that Brask’s first part 101 is an NMOS transistor region.

151. In addition, Brask discloses an embodiment where the second metal layer 120 is deposited on a first metal layer 117 and an exposed second part 119 of the high-k dielectric layer 115. TSMC-1005, ¶34. Brask discloses that “[i]f ***first metal layer 117 comprises an n-type metal***,” thus disclosing the scenario in which the first transistor region (which includes metal layer 117) is an NMOS transistor. TSMC-1005, ¶34. A POSITA would also understand that the first metal layer 117 having an n-type metal, would indicate that the first part 101 is an NMOS region.

C. Claim 4

[4] The method of claim 1, wherein the second transistor region is a PMOS transistor region.

152. Brask discloses and/or renders obvious claim 4. Brask discloses that the second transistor region is a PMOS transistor region. Brask discloses that “[w]hen ion implantation processes are used to form the source and drain regions, layers 104, 106 may be doped at the same time the source and drain regions are implanted” and that “[i]n such a process, first polysilicon layer 104 may be doped n-type, while

second polysilicon layer 106 is doped p-type—or vice versa.” TSMC-1005, ¶18; *see also id.*, ¶23. A POSITA would understand that the p-type doped source and drain region in the second part indicates that Brask’s second part 102 is a PMOS transistor region.

153. Brask discloses a scenario in which “*second metal layer 120 preferably comprises a p-type metal*, *e.g.*, one of the p-type metals identified above.” TSMC-1005, ¶34. A POSITA would also understand that the second metal layer 120 having a p-type metal, would indicate that the second part 102 is a PMOS region.

D. Claim 7

[7] The method of claim 1, wherein the metal layer comprises TiN, TaC, Ta, TaSiN, Al, or TiAlN.

154. Brask discloses and/or renders obvious claim 7. Brask discloses that its metal layer comprises TiN, TaC, Ta, TaSiN, Al, or TiAlN. For example, in explaining its deposition process, Brask discloses that its metal layer (*e.g.*, layer 120) “preferably comprises an n-type metal” (TSMC-1005, ¶34) and that such n-type metal materials can include “hafnium, zirconium, titanium, *tantalum*, *aluminum*, and metal carbides that include these elements, *i.e.*, titanium carbide, zirconium carbide, *tantalum carbide*, hafnium carbide and aluminum carbide.” *Id.*, ¶¶31, 34.

E. Claim 8

[8] The method of claim 1, further comprising performing a first chemical mechanical polishing process after forming the dielectric layer and before removing the dummy gate.

155. Brask discloses and/or renders obvious claim 8. Brask discloses performing a first chemical mechanical polishing process. For example, Brask describes that a “...dielectric 112 may be polished back, *e.g.*, via a conventional chemical mechanical polishing (‘CMP’) operation, to expose first and second polysilicon layers 104, 106.” TSMC-1005, ¶16. As noted above, a POSITA would have recognized or otherwise found it obvious that in order to expose the first and second polysilicon layers 104, 106 by polishing, the dielectric 112 would first cover the dummy gates 104, 106.

F. Claim 9

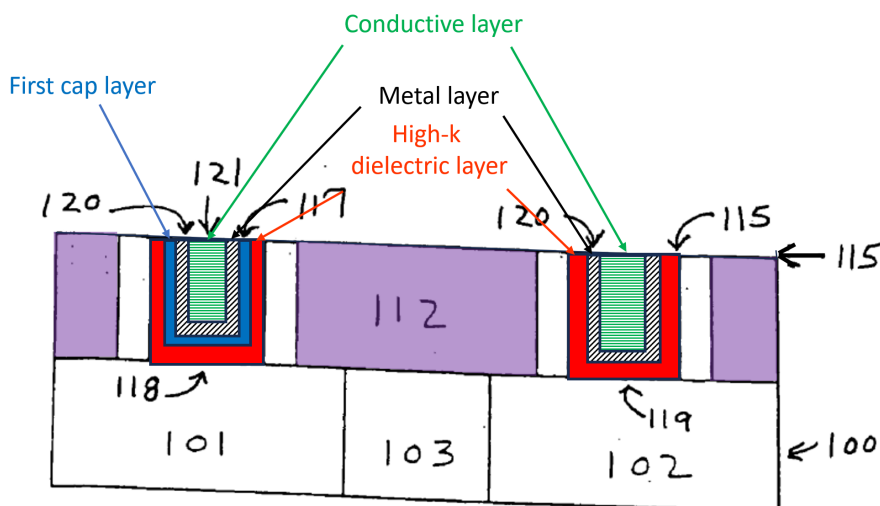
[9.pre] The method of claim 1, further comprising:

[9.1] forming a conductive layer to fill the openings of the first transistor region and the second transistor region after forming the metal layer on the first cap layer of the first transistor region and the high-k dielectric layer of the second transistor region; and

156. Brask discloses forming a conductive layer that fills the opening of the first transistor region and the second transistor region. Specifically, Brask’s trench fill metal (*e.g.*, metal 121) corresponds to the claimed conductive layer. For example, Brask discloses that “...***after depositing second metal layer 120*** on layers 117 and

115, the remainder of trenches 113, 114 is filled with a material that may be easily polished, *e.g.*, tungsten, aluminum, titanium, or titanium nitride. Such a **trench fill metal, *e.g.*, metal 121, may be deposited over the entire device using a conventional metal deposition process.** That trench fill metal may then be polished back so that it fills only trenches 113, 114, as shown in 1f.” TSMC-1005, ¶36; *see* annotated FIG. 1f, *infra*.

157. As shown in FIG. 1f, Brask illustrates and discloses that the metal layer 121 is deposited after the metal layer 120, thus disclosing that Brask’s conductive layer (121) is formed after “forming the metal layer [120] on the first cap layer [116] of the first transistor region and the high-k dielectric layer [115] of the second transistor region,” as claimed.



TSMC-1005, FIG. 1f (annotated)

[9.2] performing a second chemical polishing after forming the conductive layer.

158. Brask discloses performing a second chemical polish after forming the conductive layer. As indicated above, Brask discloses that “...after depositing second metal layer 120 on layers 117 and 115, the remainder of trenches 113, 114 is filled with a material that may be easily polished, *e.g.*, tungsten, aluminum, titanium, or titanium nitride. Such *a trench fill metal, e.g., metal 121, may be deposited over the entire device using a conventional metal deposition process. That trench fill metal may then be polished back so that it fills only trenches 113, 114, as shown in 1f.*” TSMC-1005, ¶36.

159. A POSITA would have recognized Brask’s statement that the metal 121 may be “polished back” to expressly refer to CMP. Although there exist other types of polishing in the semiconductor context, CMP is the best known and a POSITA would read “polished back” to be a shorthand for CMP. Indeed, when referring to the polishing back of other structures, Brask expressly listed “conventional chemical mechanical polishing” as a known example for polishing back excess materials. TSMC-1005, ¶16. Thus, even if it is argued that “polished back” is not an express reference to CMP, a POSITA would have nevertheless recognized or otherwise found it obvious that a similar polishing back technique—namely via chemical mechanical polishing—can be used to polish back the trench fill metals.

160. Moreover, a plethora of references, including Wang and Amazawa just to name a few, disclose the use of chemical mechanical polishing to polish back excess trench fill metals so that they only fill the trenches. *See e.g.*, TSMC-1006, Abstract, 75-76, 78-79; TSMC-1007, 815-817; *supra* §§VI.D-E. Thus, a POSITA would have found it obvious to perform a second CMP step after depositing Brask's conductive layer in the trenches to form the selectively polished and smooth fill structure that is shown in FIG. 1f of Brask.

G. Claim 10

[10] The method of claim 1, wherein the high-k dielectric layer comprises HfSiO, HfSiON, HfO, LaO, LaAlO, ZrO, ZrSiO, or HfZrO.

161. Brask discloses that the high-k dielectric layer is made of at least one of the claimed materials. Specifically, Brask's dielectric layer 115 corresponds to the claimed high-k dielectric layer. For example, Brask discloses that the "...dielectric layer 115 comprises a high-k gate dielectric layer. Some of the materials that may be used to make such a high-k gate dielectric layer include: **hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide**, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate." TSMC-1005, ¶25.

H. Claim 11

[11] The method of claim 9, wherein the conductive layer comprises Al, W, TiAl or CoWP.

162. Brask discloses that the conductive layer is made of at least one of the claimed materials. For example, Brask discloses that “...after depositing second metal layer 120 on layers 117 and 115, *the remainder of trenches 113, 114 is filled with a material that may be easily polished, e.g., tungsten, aluminum*, titanium, or titanium nitride. *Such a trench fill metal, e.g., metal 121*, may be deposited over the entire device using a conventional metal deposition process. That trench fill metal may then be polished back so that it fills only trenches 113, 114, as shown in 1f.” TSMC-1005, ¶36.

XIV. GROUND 2B: Claims 1, 2, 4, 7-11 are obvious over Brask in view of Ma

163. Ground 2B is substantively identical to, and incorporates the analysis of, Ground 2A in all but the following respects. Namely, while Ground 2A demonstrates that limitation [1.3] of Claim 1 is disclosed or otherwise rendered obvious by Brask alone, Ground 2B relies on the even more explicit disclosure of Ma to reach this feature. Integration of Ma does not disturb the mapping of Brask to other claim elements. To avoid repetition, and because the analysis of all other claim elements is identical, only the pertinent portions of Claim 1—namely limitation [1.3]—are addressed in this section. The unaddressed elements of Claims 1, 2, 4,

and 7-11 are disclosed by Brask as demonstrated for Ground 2A.

A. Claims 1, 2, 4, and 7-11

[1.3] forming a source/drain region at two sides of each dummy gate;

164. As I discussed above in Ground 2A, Brask discloses forming a plurality of dummy gates and corresponding source/drain (S/D) regions. For example, Brask discloses that “*source and drain regions* . . . may be formed using conventional processes.” TSMC-1005, ¶16. To the extent that Brask does not explicitly disclose forming the S/D region at two sides of each dummy gate, Ma provides explicit disclosures of same as noted above. For example, Ma discloses that a “[s]ource and drain junctions are formed in both the PMOS and NMOS” and that such source/drain regions, as illustrated in annotated FIG. 1 of Ma above, are formed at two sides of each of its place-holder (dummy) gates 22, 24. TSMC-1012, 2:39-40, FIG. 1.

165. A POSITA would have found it obvious and would have been motivated to look to the teachings of Ma to implement Brask’s source/drain regions. Indeed, Brask already indicates that conventional processes should be used to form various structures—such as the claimed source/drain regions—whose detailed implementations may not be expressly shown in Brask. TSMC-1005, ¶16. Thus, it would have been obvious for a POSITA to look to other sources, such as Ma, for details of known and predictable transistor designs, including how to configure and

form the source/drain regions relative to the dummy gates. A POSITA would further understand that configuring Brask's source and drain at two sides of the dummy gates as per Ma would enable the NMOS and PMOS transistors to properly function as a MOS transistor.

166. A POSITA would have also been motivated to incorporate Ma's explicit disclosure of forming source/drain regions adjacent dummy gates into Brask's process because both references describe standard self-aligned MOSFET fabrication sequences, and combining them would merely align Brask's description with conventional, industry-mandated transistor architectures. *See supra* §V.A.1. The modification would have improved process completeness without introducing new complexities, consistent with scalable CMOS design rules.

167. Moreover, such a combination would have amounted to a merely obvious application of Ma's processing techniques to Brask's device, in a manner that would have yielded no more than predictable results. Therefore, a POSITA would have had a reasonable expectation of success implementing the combination.

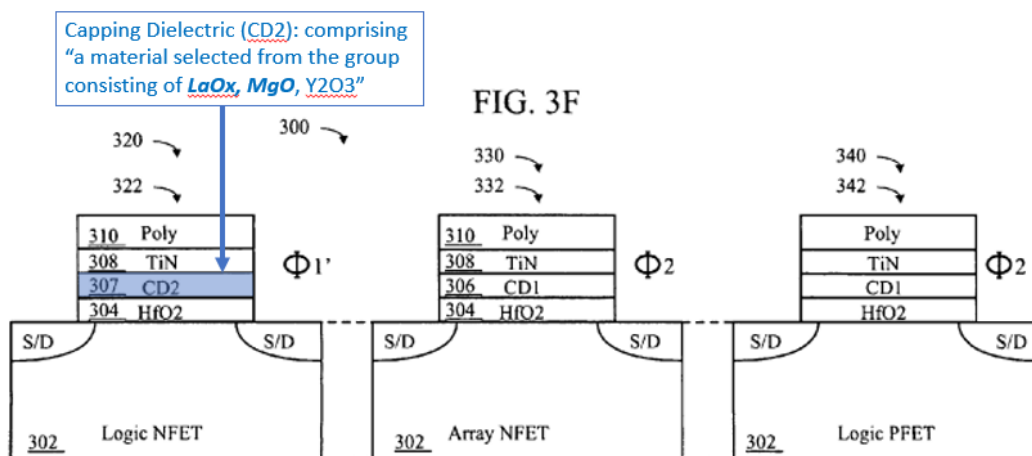
XV. GROUND 2C: Claim 3 is obvious over Brask in view of Chen

168. Based on my review, Brask in view of Chen renders obvious claim 3 of the '195 Patent.

A. Claim 3

[3] The method of claim 2, wherein the first cap layer comprises *LaO*, *MgO*, *Dy₂O₃*, or other lanthanide oxides.

169. Brask in view of Chen renders obvious the first cap layer made of at least one of the materials recited in [3]. For example, Chen discloses depositing “second metal oxide layer (CD2) [*i.e.*, ‘second capping dielectric’]” on “the high-K dielectric layer” for a logic NFET transistor. TSMC-1009, ¶¶64, 68, 90-91 (“‘CD’ is short for capping dielectric.”). Chen explains that the second capping dielectric (“CD2”) can “comprise a material selected from the group consisting of *LaOx*, *MgO*, *BaOx*, and *Y₂O₃*.” TSMC-1009, ¶64, *see also id.* ¶¶68, 90-91, 114, FIG. 3F. Chen explains that the second capping dielectric is used to tune the work function for the gate. *See* TSMC-1009, ¶¶90-91, 114, *see also id.* ¶¶55-56, 77; *supra* §VI.G.



TSMC-1009, FIG. 3F (annotated)

170. Turning to Brask, the metal layer 116 and first metal layer 117

correspond to the first cap layer. *See supra* §VIII (Ground 2A) limitation [1.7], *supra*. Similar to Chen, Brask's metal layer 117 is disposed between a high-k dielectric layer 115, disposed over substrate 100, and a metal layer 120. TSMC-1005, ¶¶26, 41-43. Moreover, Brask suggests using a "capping layer" which "may then be oxidized...to form a capping dielectric oxide" and that "in some embodiments it may be desirable to form a capping layer on high-k gate dielectric layer 115." TSMC-1005, ¶¶30-31. In view of this disclosure, a POSITA would have been motivated to look to Chen for examples of materials for the capping layer.

171. A POSITA would have found it obvious to utilize the capping dielectric material taught by Chen, such as LaOx or MgO, as a material for Brask's metal layer 116/117 for the purpose of tuning or improving the work function of the dielectric and metal interface. *See* TSMC-1009, ¶¶64, 91; TSMC-1020, ¶54.

172. Indeed, a POSITA would have been motivated to draw from Chen's use of LaOx for the capping dielectric layer because such materials were well-known in the art to improve work-function stability, chemical resistance, and integration margins in metal-gate stacks. TSMC-1021, ¶¶37, 99 (explaining that the "third dielectric material may comprise, e.g., LaO(N)...which can tune the workfunction of a metal gate electrode material"), 101 (explaining that the "third dielectric material 307 remains on and in contact with the first dielectric material 302 in the first region 310 a."), 103 (explaining that "the first region 310 *a* comprises an NMOS

transistor of the semiconductor device”); TSMC-1020, ¶54 (“*preferably a lanthanide-based dielectric*, i.e. any of DyO(N), LaO(N), ScO(N), GdO(N), TbO(N), YbO(N), ErO(N) and mixtures thereof...”); *see also* supra §VIII.A (Ground 1b, Claim 3). Their substitution into Brask would have been considered a standard material-engineering refinement aimed at, for instance, improving threshold-voltage uniformity and reliability.

XVI. GROUND 2D: Claim 5 is obvious over Brask in view of Yu

173. Based on my review, Brask in view of Yu renders obvious claim 5 of the '195 Patent.

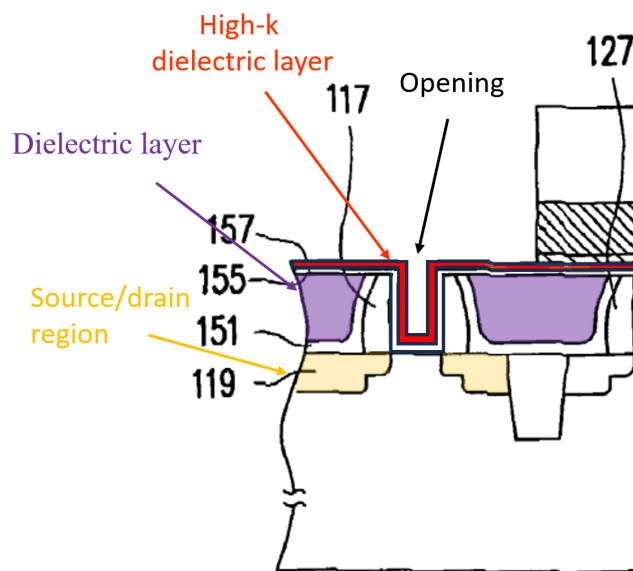
A. Claim 5

[5] The method of claim 4, further comprising forming a second cap layer in the second transistor region after removing the first cap layer from the second transistor region.

174. Brask in view of Yu renders obvious the formation of a second cap layer in the second transistor region.

175. For example, Yu renders obvious “forming a second cap layer in the second transistor region after removing the first cap layer from the second transistor region,” as claimed. Referring to FIGS. 1C-1D, Yu discloses that after a patterned photoresist layer 154 is removed, a dielectric layer 155, a high-k dielectric layer 157, a second type conductive layer 161, and a low resistance conductive layer 163 are

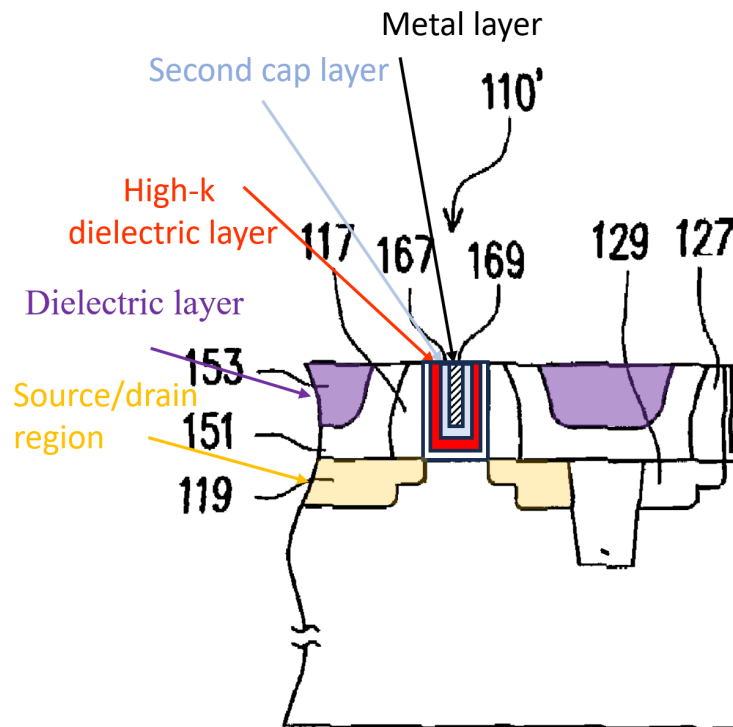
sequentially formed on the substrate 100. TSMC-1008, ¶45. A patterned photoresist layer 165 is also formed on the low resistance conductive layer 163, which fills an opening 181. The patterned photoresist layer 165 and the low resistance conductive layer 163 are disposed above the first type source/drain 119. TSMC-1008, ¶47. Subsequently, the patterned photoresist layer 165 is removed and a first type conductive layer 167 and low resistance conductive layer 169 are sequentially formed. TSMC-1008, ¶48.



TSMC-1008, FIG. 1D-1 (annotated)

176. Yu's first type conductive layer 167 corresponds to the claimed second cap layer, and Yu's low resistance conductive layer 169 corresponds to the claimed metal layer. For example, Yu discloses that "*The first type conductive layer 167 is*

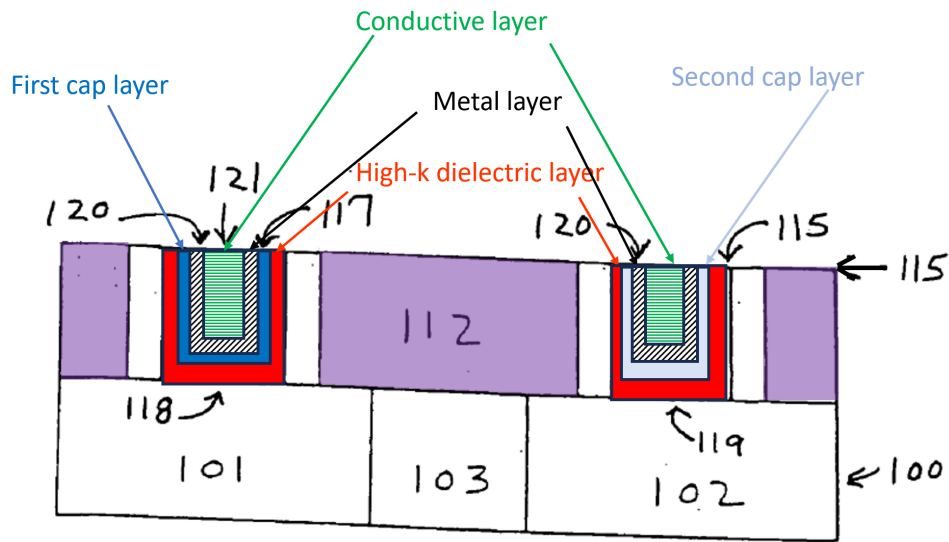
disposed above the first type doped region 107 and on the high-k dielectric layer 157, and is disposed along an exposed side surface of the low resistance dielectric layer 157 and an exposed upper surface of the high-k dielectric layer 157 in the opening 187. The low resistance conductive layer 169 is disposed on the first type conductive layer 167 and fills in the opening 187.” TSMC-1008, ¶51; *see also id.*, ¶30. Accordingly, Yu discloses and illustrates a second cap (167) disposed over a high-k dielectric layer (157) and a metal layer (169) disposed over the second cap (167), as I have shown in annotated FIG. 1E-1 below.



TSMC-1008, FIG. 1E-1 (annotated)

177. A POSITA would have found it obvious and been motivated by

multiple reasons to use a second cap layer as in Yu in Brask's device. For example, referring to annotated FIG. 1e of Brask below, a POSITA would have found it obvious in view of Yu to dispose a metal layer over Brask's high-k dielectric layer (115), after removal of the first cap layer (116), for the purpose of "improving the stability of the transistor." TSMC-1008, ¶56. A POSITA would have also recognized that including a second cap layer, which is different from the first cap layer, in the second transistor region, would allow the work function of its NMOS and PMOS transistors to be independently tuned. *See* TSMC-1021, ¶¶9-11 ("To tune the workfunction of NMOS and PMOS transistors independently it may be necessary to put different dielectric materials or a different dielectric capping layer on the NMOS and PMOS transistor."). Such modification of Brask in view of Yu would have amounted to a merely obvious application of Yu's well-known techniques to Brask's device, which was ripe for improvement and in a manner that would yield no more than predictable results. A POSITA would have had a reasonable expectation of success implementing the combination.



TSMC-1005, FIG. 1e (annotated)

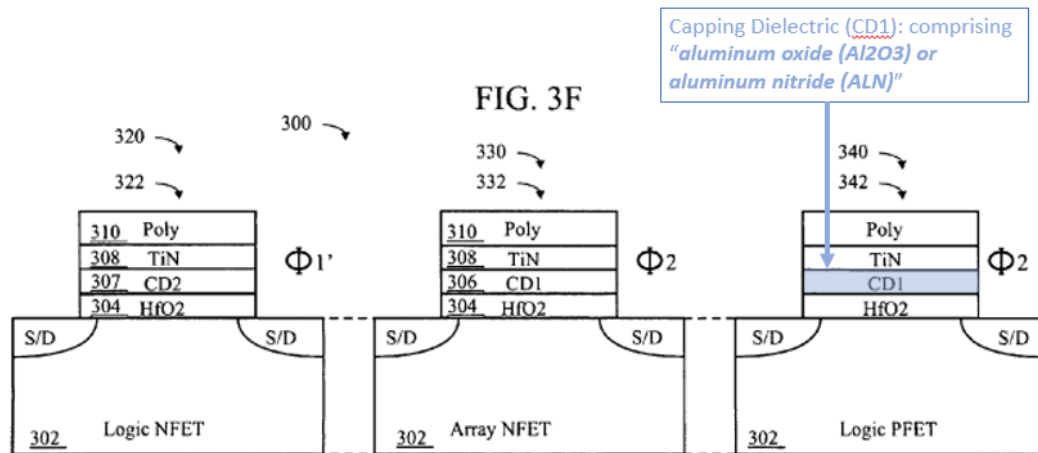
XVII. GROUND 2E: Claim 6 is obvious over Brask in view of Yu and Chen

178. Based on my review, Brask in view of Yu and Chen renders obvious claim 6 of the '195 Patent.

A. Claim 6

[6] The method of claim 5, wherein the second cap layer comprises Al_2O_3 , AlN, or AlON.

179. Brask in view of Yu (as described above for Ground 2D) further in view of Chen discloses the second cap layer comprising Al_2O_3 or AlN. For example, in the combination, Yu's first type conductive layer 167 corresponds to the second cap layer. Chen discloses deposition of a first capping dielectric layer of Al_2O_3 or AlN on the high-k dielectric layer. TSMC-1009 ¶91, *see also id.* ¶¶51, 63, 97, FIG. 3F; *supra* VI.G.



TSMC-1009, FIG. 3F (annotated)

180. A POSITA would have found it obvious to use Al_2O_3 or AlN as a material for Yu's second cap layer, in order to modulate the work function, adjust threshold voltage, and/or differentiate PMOS and NFET behavior on the same substrate. TSMC-1009, ¶¶51, 90-91, 109-110; TSMC-1020, ¶54 ("The first gate dielectric capping layer may comprise *preferably an aluminum-based dielectric, i.e. AlO, AlN, AlON* and mixtures thereof."); *see also* supra §X.A (Ground 1D, Claim 6).

181. As noted, Yu's first type conductive layer 167 corresponds to the second cap layer. A POSITA, in possession of Chen, would find it obvious to utilize Al_2O_3 or AlN in Yu's second cap layer (167), because of Chen's disclosure for using such materials to modulate the work function of the PFET. *See supra* §XV (Ground 2C, limitation [3]); *see also supra* §§VIII, X.

182. A POSITA would have been motivated to combine Yu's

conductive/cap-layer approach with Chen's capping dielectric materials in Brask's device because all three references address the same fabrication challenges—work-function alignment, high-k interface engineering, and dual-gate integration. Using Chen's materials within Yu's cap architecture in Brask's replacement-gate flow would have been technologically compatible, industry-aligned, and expected to yield predictable improvements in threshold voltage control and reliability.

183. Such modification of Brask would have amounted to a merely obvious application of Chen's material options to Brask's device, which was ripe for improvement and in a manner that would yield no more than predictable results. A POSITA would have had a reasonable expectation of success implementing the combination.

XVIII. OVERVIEW OF CONCLUSIONS FORMED

184. This declaration explains the conclusions that I have formed based on my independent analysis. To summarize those conclusions:

- Based upon my knowledge and experience, and my review of the materials listed above, Claims 1, 2, 4, and 7-11 of the '195 Patent are anticipated and/or rendered obvious by Bohr (TSMC-1004). *See above*, Ground 1A—Section VII.
- Based upon my knowledge and experience, and my review of the materials listed above, Claim 3 is rendered obvious by Bohr (TSMC-

1004) in view of Chen (TSMC-1009). *See above*, Ground 1B—Section VIII.

- Based upon my knowledge and experience, and my review of the materials listed above, Claim 5 is rendered obvious by Bohr (TSMC-1004) in view of Yu (TSMC-1008). *See above*, Ground 1C—Section IX.
- Based upon my knowledge and experience, and my review of the materials listed above, Claim 6 is rendered obvious by Bohr (TSMC-1004) in view of Yu (TSMC-1008) and Chen (TSMC-1009). *See above*, Ground 1D—Section X.
- Based upon my knowledge and experience, and my review of the materials listed above, Claim 7 is rendered obvious by Bohr (TSMC-1004) in view of Lee (TSMC-1010). *See above*, Ground 1E—Section XI.
- Based upon my knowledge and experience, and my review of the materials listed above, Claims 9 and 10 are rendered obvious by Bohr (TSMC-1004) in view of Wang (TSMC-1006) or Amazawa (TSMC-1007). *See above*, Ground 1F—Section XII.
- Based upon my knowledge and experience, and my review of the materials listed above, Claims 1, 2, 4, and 7-11 of the '195 Patent are

anticipated and/or rendered obvious by Brask (TSMC-1005). *See above*, Ground 2A—Section XIII.

- Based upon my knowledge and experience, and my review of the materials listed above, Claims 1, 2, 4, 7-11 are rendered obvious by Brask (TSMC-1005) in view of Ma (TSMC-1012). *See above*, Ground 2B—Section XIV.
- Based upon my knowledge and experience, and my review of the materials listed above, Claim 3 is rendered obvious by Brask (TSMC-1005) in view of Chen (TSMC-1009). *See above*, Ground 2C—Section XV.
- Based upon my knowledge and experience, and my review of the materials listed above, Claim 5 is rendered obvious by Brask (TSMC-1005) in view of Yu (TSMC-1008). *See above*, Ground 2D—Section XVI.
- Based upon my knowledge and experience, and my review of the materials listed above, Claim 6 is rendered obvious by Brask (TSMC-1005) in view of Yu (TSMC-1008) and Chen (TSMC-1009). *See above*, Ground 2E—Section XVII.

XIX. CONCLUSION

185. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both (under Section 1001 of Title 18 of the United States Code).

Executed this 13th day of February, 2026.

A handwritten signature in cursive script, appearing to read "Jack Lee", is written over a horizontal line.

Dr. Jack Lee

Appendix A

Jack Lee, Ph.D. CV

Jack C. Lee
Professor Emeritus
Electrical and Computer Engineering Department
The University of Texas at Austin

Current Status

Professor Emeritus
Department of Electrical and Computer Engineering
The University of Texas at Austin

Research / teaching experience and expertise:

- Integrated circuits manufacturing
- Photovoltaic/solar cell technologies
- Alternative channel devices
- Dielectric and passivation processes
- Display technologies
- Semiconductor memory devices

Education

9/84 – 8/88 Ph.D., Electrical Engineering, University of California at Berkeley
9/80 – 12/81 M.S., Electrical Engineering, University of California at Los Angeles
9/76 – 6/80 B.S., Electrical Engineering (with highest honors),
University of California at Los Angeles

Professional Career

9/23 – present Professor Emeritus
Department of Electrical and Computer Engineering
The University of Texas at Austin
9/00 – 8/23 Cullen Trust for Higher Education Endowed Professorship in Engineering #4
Department of Electrical and Computer Engineering
The University of Texas at Austin
9/96 – 8/23 Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
9/92 – 8/96 Associate Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
9/88 – 8/92 Assistant Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
1/88 – 6/88 Lecturer, Electrical Engineering and Computer Science Department
University of California at Berkeley
6/79 – 8/84 Member of Technical Staff, High-Speed Bipolar Device Program
TRW Microelectronics Center, Redondo Beach, CA

Honors and Awards

IEEE Electron Devices Society Distinguished Lecturer, 2004 - 2016.
Fellow, The Institute of Electrical and Electronic Engineers (IEEE), 2002 “For
contributions to the understanding and development of ultra-thin dielectrics and their
application to silicon devices”
Gordon Lepley IV Endowed Memorial Teaching Award, ECE Department, The
University of Texas at Austin, 2004

Cullen Trust For Higher Education Endowed Professorship in Engineering, 2000-present
 Dean's Fellow, College of Engineering, The University of Texas at Austin, 1999, 2003
 Lockheed Fort-Worth Division Award for Excellence in Engineering Teaching,
 College of Engineering, The University of Texas at Austin, 1996
 Award of Excellence, Halliburton Foundation, 1993
 Departmental Teaching Award, College of Engineering, The University of Texas at
 Austin, 1993
 SRC Inventor Recognition Award, Semiconductor Research Corporation, 1991
 Hughes Aircraft Company Endowed Faculty Fellowship in Engineering,
 The University of Texas at Austin, 1991- 2000
 Outstanding Engineering Teaching by an Assistant Professor, College of Engineering,
 The University of Texas at Austin, 1991
 Best Paper Award, SEMATECH Centers of Excellence Coordination Meeting, 1990.
 Dow Outstanding Young Faculty Award, American Society for Engineering Education,
 1990
 Engineering Research Initiation Award, Engineering Foundation of the United
 Engineering Trustees, 1989
 Best Paper Award, IEEE International Reliability Physics Symposium, 1988

Litigation Experience as Testifying Experts

The following is a list of cases in which I have provided expert testimony, including through a declaration, report or testimony at deposition or trial since 2016

- Longitude Flash Memory Solutions and IPValue Management v. SanDisk
 April 2025 –
 (Representing defendant, SanDisk)
- Marlin Semiconductor Limited v. TSMC
 April 2025 –
 (Representing defendant, TSMC)
- Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Mfg. Co. Ltd
 October 2024 –
 (Representing defendant, TSMC)
- Yangtze Memory Technologies v. Micron
 January 2024 –
 (Representing defendant, Micron)
- BeSang v. Micron
 March 2023 –
 (Representing defendant, Micron)
- The Trustees of Purdue University v. Wolfspeed, Inc.
 February 2022 – March 2025
 (Representing defendant, Wolfspeed)

- GlobalFoundries - IPR
March 2021 –
(Representing petitioner and filed an IPR declaration)
- HD Silicon Solutions LLC v. Microchip Technology Inc.
January 2021 – February 2025
(Representing defendant, Microchip Technology Inc.)
- Longitude Licensing Limited vs Western Digital
March 2023 – January 2024
(Representing defendant, Western Digital)
- Impinj, Inc. v. NXP USA, Inc.
September 2019 – July 2023
(Representing defendant, NXP USA, Inc.)
- Monterey Research, LLC v. Qualcomm Inc.
February 2020 – May 2022
(Representing defendant, Qualcomm)
- Bell Semiconductor, LLC v. Texas Instruments Incorporated
July 2020 – March 2021
(Representing defendant, Texas Instruments)
- Greenthread LLC v. Samsung
February 2020 – July 2020
(Representing plaintiff, Greenthread LLC)
- MLC Intellectual Property LLC vs. Micron Technology, Inc.,
June 2016 – January 2021
(Representing plaintiff, MLC Intellectual Property LLC)
- Hanwha v. LONGi Solar Technology
April 2019 – June 2020
(Representing defendant LONGi Solar Technology)
- Vista Peak Ventures, LLC v. Innolux Corp.
January 2019 – March 2019
(Representing IPR Petitioner, Innolux Corp.)
- Home Semiconductor Corp. v. Samsung
August 2018 – June 2020
(Representing plaintiff, Home Semiconductor Corp.)
- Mariner IC Inc. v. Asustek Computer Inc.

May 2018 – August 2019
(Representing plaintiff, Mariner IC Inc.)

- Godo Kaisha IP Bridge 1 v. OmniVision Technologies, Inc.
January 2018 – December 2018
(Representing defendant, OmniVision Technologies, Inc.)
- Macronix v. Toshiba
May 2017 – February 2018
(Representing defendant, Toshiba)
- University of Illinois v. Micron Technology
September 2009 – November 2017
(Representing plaintiff, Univ. of Illinois)
- Silicon Genesis v. Soitec
October 2016 – March 2017
(Representing plaintiff, Silicon Genesis)

Non-Litigation Consulting

- Applied Materials, Inc.
Teaching short courses on semiconductor physics, devices, design/layout, and fabrication technologies (2-3 courses per year).

Jack C. Lee is a Professor Emeritus of the Electrical and Computer Engineering Department. He held the Cullen Trust for Higher Education Endowed Professorship in Engineering # 4 at The University of Texas at Austin from 2000-2023. He received the B.S. and M.S. degrees in electrical engineering from University of California, Los Angeles, in 1980 and 1981, respectively; and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1988. From 1979 to 1984, he was a Member of Technical Staff at the TRW Microelectronics Center, CA, in the High-Speed Bipolar Device Program. He worked on bipolar device and circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research interests include semiconductor devices including 3D structures such as FinFETs, fabrication processes, characterization and modeling, dielectric process, characterization and reliability, high-K gate dielectrics and electrode, semiconductor memory applications, alternative channel materials, display technologies and photovoltaic/solar cell technologies. Dr. Lee has over 40 years of experience in semiconductor technology and dielectric processing. He has published over 600 journal publications and conference

proceedings and 9 patents; and co-authored 8 book and book chapters. He has also been recognized with many teaching and research awards. Dr. Lee is a Fellow of IEEE and had been a Distinguished Lecturer for the IEEE Electron Devices Society.

Publications

Jack C. Lee

Refereed Journal Publications

1. J. Lee, K. Mayaram and C. Hu, "A Theoretical Study of Gate/Drain Offset in LDD MOSFET's," IEEE Electron Device Letters, vol. EDL-7, no. 3, p. 152 - 154, March 1986.
2. J. Lee, I-C Chen and C. Hu, "Comparison Between CVD and Thermal Oxide Dielectric Integrity," IEEE Electron Device Letters, vol. EDL-7, no. 9, p. 506 - 509, September 1986.
3. K. Mayaram, J. Lee and C. Hu, "A Model for the Electric Field in Lightly Doped Drain Structures," IEEE Transactions on Electron Devices, vol. ED-34, no.7, p. 1509 - 1518, July 1987.
4. J. Lee and C. Hu, "Polarity Asymmetry of Oxides Grown on Polycrystalline Silicon," IEEE Transactions on Electron Devices, vol. ED-35, no. 7, p. 1063 - 1070, July 1988.
5. J. Lee, C. Hegarty and C. Hu, "Electrical Characteristics of MOSFET's Using Low-Pressure Chemical Vapor Deposited Oxide," IEEE Electron Device Letters, vol. EDL-9, no. 7, p. 324 - 327, July 1988.
6. J. Lee, I-C Chen and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," Special Issue of IEEE Transactions on Electron Devices on Reliability, Vol. ED-35, no. 12, p. 2268 - 2278, December 1988.
7. H. Hwang, W. Ting, D. L. Kwong, J. Lee, L. Buhrow and R. Bowling, "Electrical Characteristics of Reoxidized-nitrided CVD Oxide," Applied Physics Letters, 55(8), p. 755 - 756, 21 August, 1989.
8. R. Moazzami, J. Lee and C. Hu, "Temperature Acceleration of Time-Dependent Dielectric Breakdown," Special issue of IEEE Transactions on Electron Devices on Vacuum Microelectronic Devices, vol. ED-36, no. 11, p. 2462 - 2465, November 1989.
9. H. Hwang, W. Ting, D.L. Kwong, J. Lee, L. Buhrow and R.A. Bowling, "Effects of Dynamic Stressing on Nitrided and Reoxidized-Nitrided Chemical Vapor Deposited Gate Oxides," IEEE Electron Device Letters, vol. EDL-10, no. 12, p. 568 - 570, December 1989.
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11. K. Park, S. Batra, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeagain, and G. Lux, "Anomalous Capacitance-Voltage Behavior Due to Dopant Segregation and

Carrier Trapping in Arsenic-Implanted Polysilicon and Polycide Gates," *Applied Physics Letters*, vol. 56, no. 23, p.2325 - 2327, June 4, 1990.

12. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Anomalous Current-Voltage Behavior in Titanium-Silicided Source/Drain Junctions," *Journal of Applied Physics*, vol. 68, no. 3, p. 1082 - 1087, August 1, 1990.
13. H. Hwang, W. Ting, B. Maiti, D.L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Gate Dielectrics Prepared by Rapid Thermal Oxidation of Si in N₂O," *Applied Physics Letters*, vol. 57, no. 10, p. 1010 - 1011, Sept. 3, 1990.
14. S. Batra, K. Park, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain and G. Lux "Effects of Dopant Redistribution, Segregation and Carrier Trapping in As-Implanted MOS Gates," *IEEE Transactions on Electron Devices*, vol. 37, no. 11, p. 2322 - 2330, October, 1990.
15. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "The Impact of Trench Isolation on Latch-up Immunity in Bulk, Non-epitaxial CMOS," *IEEE Electron Device Letters*, vol. EDL-12, no. 2, p. 77 - 79, February, 1991.
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