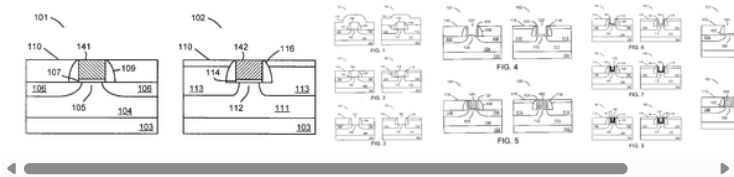


Replacement gates to enhance transistor strain

Abstract

Some embodiments of the present invention include apparatuses and methods relating to NMOS and PMOS transistor strain.

Images (5)



Classifications

 **H10D84/017** Manufacturing their source or drain regions, e.g. silicided source or drain regions

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Landscapes

Insulated Gate Type Field-Effect Transistor

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US20070138559A1

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Inventor: [Mark Bohr](#)

Current Assignee : [Intel Corp](#)

Worldwide applications

2005 [US](#) 2008 [US](#) 2011 [US](#) 2013 [US](#) 2014 [US](#) 2015 [US](#) 2016 [US](#) 2023 [US](#)

Application US11/305,465 events ⓘ

- 2005-12-16 Priority to US11/305,465
- 2005-12-16 Application filed by Intel Corp
- 2007-06-21 Publication of US20070138559A1
- 2012-01-24 Application granted
- 2012-01-24 Publication of US8101485B2
- Status Active
- 2028-10-28 Adjusted expiration
- Show all events ▾

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Claims (30)

Hide Dependent ^

1. A method comprising:

forming an NMOS transistor including a channel, a stressor, and a gate structure over the channel and between sidewall spacers, wherein the stressor causes a tensile strain on the channel; and

removing at least a portion of the gate structure to allow the stressor to enhance the tensile strain on the channel, wherein removing the portion of the gate structure forms a trench.
2. The method of claim 1, wherein the stressor comprises a tensile layer over the gate structure.
3. The method of claim 1, wherein removing the portion of the gate structure includes removing a gate electrode and a gate dielectric.
4. The method of claim 3, further comprising:

forming a high-k gate dielectric in the trench; and

forming a metal gate electrode over the high-k gate dielectric, wherein the metal gate electrode provides an additional tensile strain in the channel.
5. The method of claim 4, wherein providing the additional tensile strain comprises stressing the channel via the high-k gate dielectric.
6. The method of claim 4, wherein providing the additional tensile strain comprises stressing the channel via the sidewall spacers.
7. The method of claim 4, wherein the metal gate electrode comprises an n-type work function material including at least one of hafnium, zirconium, titanium, tantalum, or aluminum.
8. The method of claim 4, wherein the metal gate electrode includes at least one of tungsten or titanium carbide.
9. The method of claim 4, further comprising:

forming a PMOS transistor including a second channel, a second stressor, and a second gate structure over the second channel and between second sidewall spacers, wherein the second stressor causes a compressive strain on the second channel; and

removing the second gate structure to allow the second stressor to enhance the compressive strain on the second channel, wherein removing the second gate structure forms a second trench;

forming a second high-k gate dielectric in the second trench; and

forming a second metal gate electrode over the second high-k gate dielectric, wherein the second metal gate electrode provides an additional compressive strain in the second channel.

10. The method of claim 9, wherein the second metal gate electrode comprises a p-type work function material including at least one of ruthenium, palladium, platinum, cobalt, or nickel.

11. The method of claim 9, wherein the second metal gate electrode comprises a material having a coefficient of thermal expansion that is greater than the coefficient of thermal expansion of the channel.

12. The method of claim 9, wherein the second metal gate electrode comprises at least one of boron carbide, tungsten, molybdenum, rhodium, vanadium, platinum, ruthenium, beryllium, palladium, cobalt, titanium, nickel, copper, tin, aluminum, lead, or zinc.

13. The method of claim 3, further comprising:

forming a silicon dioxide gate dielectric in the trench; and

forming a polysilicon gate electrode over the silicon dioxide gate dielectric.

14. The method of claim 1, wherein removing the portion of the gate structure includes removing a gate electrode, and wherein a gate dielectric remains.

15. The method of claim 14, wherein the gate dielectric comprises a high-k gate dielectric.

16. The method of claim 15, further comprising:

forming a metal gate electrode over the high-k gate dielectric.

17. A method comprising:

forming a PMOS transistor including a channel, a stressor, and a gate structure over the channel and between sidewall spacers, wherein the stressor causes a compressive strain on the channel; and

removing at least a portion of the gate structure to allow the stressor to enhance the compressive strain on the channel, wherein removing the portion of the gate structure forms a trench.

18. The method of claim 17, wherein the stressor comprises an epitaxial source and drain film.

19. The method of claim 17, wherein removing the portion of the gate structure includes removing a gate electrode and a gate dielectric.

20. The method of claim 19, further comprising:

forming a high-k gate dielectric in the trench; and

forming a metal gate electrode over the high-k gate dielectric, wherein the metal gate electrode provides an additional compressive strain in the channel.

21. The method of claim 20, wherein the metal gate electrode comprises a p-type work function material including at least one of ruthenium, palladium, platinum, cobalt, or nickel.

22. The method of claim 20, wherein the metal gate electrode comprises at least one of boron carbide, tungsten, molybdenum, rhodium, vanadium, platinum, ruthenium, beryllium, palladium, cobalt, titanium, nickel, copper, tin, aluminum, lead, or zinc.

23. The method of claim 17, further comprising:

forming an NMOS transistor including a second channel, a second stressor, and a second gate structure over the second channel and between second sidewall spacers, wherein the second stressor causes a tensile strain on the second channel; and

removing the second gate structure to allow the second stressor to enhance the tensile strain on the second channel, wherein removing the second gate structure forms a second trench;

forming a high-k gate dielectric in the trench and the second trench;

forming an n-type work function material in the trench and the second trench;

removing the n-type work function material from the trench; and

forming a p-type work function material in the trench.

24. The method of claim 23, further comprising:

providing a fill material in the trench.

25. An apparatus comprising:

an NMOS transistor having a strained channel on a substrate, wherein the NMOS transistor includes a p-well on the substrate, the channel between n-doped regions in the p-well, and a gate structure including a high-k gate dielectric, an n-type work function metal, and a material that provides a tensile strain in the channel; and

a PMOS transistor having a strained second channel on the substrate, wherein the PMOS transistor includes an n-well on the substrate, the second channel between p-doped epitaxial films having larger lattice spacing than the substrate, and a second gate structure over the second channel.

26. The apparatus of claim 25, wherein the n-type work function metal comprises at least one of hafnium, zirconium, titanium, tantalum, or aluminum.

27. The apparatus of claim 25, wherein the material that provides the tensile strain comprises at least one of hafnium, zirconium, titanium, tantalum, aluminum, tungsten, or titanium carbide.

28. The apparatus of claim 25, wherein the second gate structure comprises a high-k gate dielectric, a p-type work function metal, and a material that provides a compressive strain in the channel.

29. The apparatus of claim 28, wherein the p-type work function metal comprises at least one of ruthenium, palladium, platinum, cobalt, or nickel.

30. The apparatus of claim 28, wherein the material that provides the compressive strain comprises at least one of boron carbide, tungsten, molybdenum, rhodium, vanadium, platinum, ruthenium, beryllium, palladium, cobalt, titanium, nickel, copper, tin, aluminum, lead, or zinc.

Description

TECHNICAL FIELD

[0001] Embodiments of the invention relate to semiconductor technology. In particular, embodiments of the invention relate to strained transistors.

BACKGROUND

[0002] In semiconductor processing, transistors may be formed on semiconductor wafers. The transistors may include a gate structure having a gate dielectric and a gate electrode, a source, a drain, and a channel region between the source and the drain. In CMOS (complimentary metal oxide semiconductor) technology, transistors may typically be of two types: NMOS (negative channel metal oxide semiconductor) or PMOS (positive channel metal oxide semiconductor) transistors. The transistors and other devices may be interconnected to form integrated circuits (ICs) which perform numerous useful functions.

[0003] The performance of the ICs may directly depend on the performance of the transistors. Transistor performance may be improved by providing a strain in the channel region. Specifically, NMOS transistor performance may be improved by providing a tensile strain in the channel region and PMOS transistor performance may be improved by providing a compressive strain in the channel region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The invention is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings, in which the like references indicate similar elements and in which:

[0005] FIG. 1 is a cross-sectional view of a partially formed NMOS transistor and a partially formed PMOS transistor, and a layer over the transistor gate structures.

[0006] FIG. 2 is a view similar to FIG. 1 with a portion of the layer removed to expose the gate structures.

[0007] FIG. 3 is a view similar to FIG. 2 with the transistor gate structures removed to form trenches.

[0008] FIG. 4 is a view similar to FIG. 3 with a gate dielectric formed in the trenches.

[0009] FIG. 5 is a view similar to FIG. 4 with gate electrodes formed in the trenches.

[0010] FIG. 6 is a view similar to FIG. 4 with an n-type material formed in the trenches.

[0011] FIG. 7 is a view similar to FIG. 6 with a portion of the n-type material removed and a p-type material formed in the trenches.

[0012] FIG. 8 is a view similar to FIG. 7 with fill materials formed in the trenches.

[0013] FIG. 9 is a view similar to FIG. 2 with a portion of the gate structures removed to form trenches.

[0014] FIG. 10 is a view similar to FIG. 9 with gate electrodes formed in the trenches.

DETAILED DESCRIPTION

[0015] In various embodiments, apparatuses and methods relating to strained transistors are described. However, various embodiments may be practiced without one or more of the specific details, or with other methods, materials, or components. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of various embodiments of the invention. Similarly, for purposes of explanation, specific numbers, materials, and configurations are set forth in order to provide a thorough understanding of the invention. Nevertheless, the invention may be practiced without specific details. Furthermore, it is understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0016] Transistor performance characteristics, such as transistor drive current, may be enhanced by providing strain to the transistor channels. For example, NMOS transistor performance may improve when the NMOS transistor channel is under lateral tensile stress. Also, PMOS transistor performance may improve when the PMOS transistor channel is under lateral compressive stress. Briefly, the present invention may provide for increased channel strain to enhance the performance of NMOS and PMOS transistors.

[0017] FIG. 1 illustrates an NMOS transistor **101** and a PMOS transistor **102** on a substrate **103**. NMOS transistor **101** and PMOS transistor **102** may be on a continuous substrate **103**. However, they are illustrated separately in FIGS. 1-10 for the sake of clarity. Substrate **103** may include any suitable semiconductor material. In an embodiment, substrate **103** may include monocrystalline silicon. Substrate **103** may also include isolation structures (not shown) to isolate the NMOS and PMOS transistors.

[0018] As shown, PMOS transistor **102** includes an n-well **111**, a channel **112**, source and drain films **113**, a gate dielectric **114**, a gate electrode **115** and spacers **116**. PMOS transistor **102** may be formed by any suitable processing techniques.

[0019] N-well **111** may include any suitable n-type dopants, such as phosphorus and arsenic, and may be formed by any suitable technique. In an embodiment, n-well **111** may be formed by doping substrate **103** by ion implantation.

[0020] Channel **112** may be under a compressive strain from any stressor source or material. As discussed, a compressive strain may increase the performance of PMOS transistor **102**. In an embodiment, source and drain films **113** may provide a compressive strain on channel **112**. In such embodiments, source and drain films **113** may therefore be considered stressors. In an embodiment, source and drain films **113** may be epitaxial and may have a greater lattice spacing constant than n-well **111** and channel **112**. Source and drain films **113** may transfer a compressive strain on channel **112** as they tend to, but are constrained from, expanding to their natural lattice spacing. In an embodiment, source and drain films **113** may include an alloy of materials. In an embodiment, source and drain films **113** may include an alloy of silicon and germanium. In an embodiment, source and drain films **113** may include a p-type dopant, such as boron. In an embodiment, source and drain films **113** may be formed in recesses of n-well **111**.

[0021] As illustrated, channel **112** may be under a compressive strain from source and drain films **113**. However, channel **112** may be under a compressive strain from any suitable stressor source or material. In an embodiment, a material may be formed over gate electrode **115** and spacers **116** to provide a compressive strain on channel **112**.

[0022] Gate dielectric **114** may be any suitable material. In an embodiment, gate dielectric **114** may include silicon dioxide. In other embodiments, gate dielectric **114** may include a high-k gate dielectric. In general, a high-k gate dielectric may include any material having a dielectric constant, k, that is greater than about 3.9 (the dielectric constant of silicon dioxide). In an embodiment, gate dielectric **114** may include hafnium oxide. In other embodiments, gate dielectric **114** may include hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide aluminum oxide, lead scandium tantalum oxide, or lead zinc niobate.

[0023] Gate electrode **115** may include any suitable material. In an embodiment, gate electrode **115** may include polysilicon. In another embodiment, gate electrode **115** may include polysilicon doped with a p-type dopant, such as boron.

[0024] Gate dielectric **114** and gate electrode **115** together may be considered a gate stack or a gate structure. In an embodiment, both gate dielectric **114** and gate electrode **115** may be a part of the gate structure. In other embodiments, the gate structure may be a single material. In other embodiments, the gate structure may include a hard mask or any number of additional materials. As is described further below, a portion or an entirety of the gate structure may be removed to enhance the strain in channel **112**. Therefore, a portion or an entirety of the gate structure may be considered sacrificial.

[0025] Spacers **116** may include any suitable dielectric materials, such as a nitride or an oxide. Spacers **116** may be along the sidewalls of gate electrode **108** and may therefore be considered sidewall spacers.

[0026] As shown, NMOS transistor **101** includes a p-well **104**, a channel **105**, source and drain regions **106**, a gate dielectric **107**, a gate electrode **108**, and spacers **109**. NMOS transistor **101** may be formed by any suitable processing techniques. P-well **104** may include any suitable p-type dopants, such as boron and indium, and may be formed by any suitable technique. Source and drain regions **106** may include any suitable n-type dopants, such as phosphorus and arsenic, and may be formed by any suitable technique, such as ion implantation or epitaxial deposition. Channel **105** may be between source and drain regions **106**.

[0027] Gate dielectric **107** may be any suitable material. In an embodiment, gate dielectric **107** may include silicon dioxide. In other embodiments, gate dielectric **107** may include a high-k gate dielectric. In an embodiment, gate dielectric **107** may include hafnium oxide. In other embodiments, gate dielectric **107** may include hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide aluminum oxide, lead scandium tantalum oxide, or lead zinc niobate. In an embodiment, gate dielectric **107** and gate dielectric **114** may include the same material.

- [0028] Gate electrode **108** may include any suitable material. In an embodiment, gate electrode **108** may include polysilicon. In another embodiment, gate electrode **108** may include polysilicon doped with an n-type dopant, such as phosphorus and arsenic.
- [0029] Gate dielectric **107** and gate electrode **108** together may be considered a gate stack or a gate structure. In an embodiment, both gate dielectric **107** and gate electrode **108** may be a part of the gate structure. In other embodiments, the gate structure may be a single material. In other embodiments, the gate structure may include a hard mask or any number of additional materials. As is described further below, a portion or an entirety of the gate structure may be removed to enhance the strain in channel **105**. Therefore, a portion or an entirety of the gate structure may be considered sacrificial.
- [0030] Spacers **109** may include any suitable dielectric materials, such as a nitride or an oxide. Spacers **109** may be along the sidewalls of gate electrode **108** and may therefore be considered sidewall spacers.
- [0031] Channel **105** may be under a tensile strain from any stressor source. As discussed, a tensile strain in channel **105** may improve the performance of NMOS transistor **101**. In an embodiment, a layer **110** may cover NMOS transistor **101** and PMOS transistor **102** and layer **110** may provide a tensile stress on channel **105** and channel **112** and may therefore be considered a tensile layer or a stressor. In an embodiment, layer **110** may include a silicon nitride, such as Si_3N_4 . Layer **110** may be formed by any suitable technique. In an embodiment, a tensile strain in channel **112** may diminish the performance of PMOS transistor **102**; however, due to source and drain films **113**, channel **112** may be under a net compressive strain.
- [0032] As discussed, channel **105** may be under a tensile strain due to layer **110**. However, channel **105** may be under a tensile strain from any suitable stressor material or source. In an embodiment, source and drain regions **106** may provide a tensile strain on channel **105**. In an embodiment, source and drain regions **106** may be epitaxial and may have a smaller lattice spacing constant than p-well **104** and channel **105**. Source and drain regions **106** may then be constrained from achieving their natural lattice spacing and may transfer a tensile strain on channel **105** as they tend to, but are constrained from, contracting to their natural lattice spacing. In an embodiment, source and drain regions **106** films may include carbon.
- [0033] NMOS transistor **101** and PMOS transistor **102** may also include other features that are not shown for the sake of clarity, such as halo implants, tip implants, silicide regions, and the like.
- [0034] As illustrated in FIG. 2, a portion of layer **110** may be removed to expose gate electrode **108** and gate electrode **115**. In an embodiment, a portion of layer **110** may be removed by a planarization or chemical mechanical polishing (CMP) process. In an embodiment, a portion of gate electrodes **108**, **115** may also be removed.
- [0035] As illustrated in FIG. 3, gate electrodes **108**, **115** and gate dielectrics **107**, **114** may be removed to form trenches **121**, **122**. Gate electrodes **108**, **115** and gate dielectrics **107**, **114** may be removed by any suitable technique, such as a selective etch technique.
- [0036] As discussed, channel **105** may be under a tensile strain and channel **112** may be under a compressive strain. Due to the removal of gate electrodes **108**, **115** and gate dielectrics **107**, **114**, the strain on channels **105**, **112** may be increased or enhanced. The increased strain may be due to the removal of material from trenches **121**, **122**, which may have been offsetting the desired stresses. In general, removing a portion or the entirety of a gate structure may remove an offsetting stress and allow the stressor to relax, which may increase the strain on the transistor channel. In other words, removing the gate structure may allow the stressor to enhance the desired strain on the channel.
- [0037] In an embodiment, NMOS transistor **101** may include a stressor that is relaxed to increase a tensile strain on channel **105**. In an embodiment, the stressor may include layer **110**. In another embodiment, the stressor may include source and drain regions **106**. In an embodiment, PMOS transistor **102** may include a stressor that is allowed to increase a compressive strain on channel **112**. In an embodiment, the stressor may include source and drain films **113**.
- [0038] As illustrated in FIG. 4, a gate dielectric **131** may be formed in trenches **121**, **122**. Gate dielectric **131** may be any suitable material and may be formed by any suitable technique. In an embodiment, gate dielectric **131** may include a high-k gate dielectric, such as hafnium oxide. In various other embodiments, gate dielectric **131** may include hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide aluminum oxide, lead scandium tantalum oxide, or lead zinc niobate. In another embodiment, gate dielectric **131** may include silicon dioxide.
- [0039] In an embodiment, gate dielectric **131** may be formed by a deposition process, such as chemical vapor deposition (CVD). As illustrated in FIG. 4, gate dielectric **131** may be formed along the bottom of trenches **121**, **122** and along the sidewalls of trenches **121**, **122**. In an embodiment, gate dielectric **131** may also be formed over layer **110** (not shown). In such embodiments, gate dielectric **131** may be subsequently removed from layer **110** by a CMP process such that gate dielectric **131** only remains in trenches **121**, **122**.
- [0040] As illustrated in FIG. 5, a gate electrode **141** and a gate electrode **142** may be formed. Gate electrode **141** may include any suitable material or materials. In an embodiment, gate electrode **141** may include an n-doped polysilicon. In another embodiment, gate electrode **141** may include a metal with an n-type work function. In other embodiments, gate electrode **141** may include a stack or structure of materials with the material in contact with gate dielectric **131** including a material with an n-type work function. In various embodiments, the n-type work function material may include hafnium, zirconium, titanium, tantalum, aluminum, their alloys, or carbides of those metals.
- [0041] In an embodiment, gate electrode **141** may include a material that provides an additional tensile strain on channel **105**. Gate electrode **141** may provide an additional tensile strain on channel **105** by including a material with a coefficient of thermal expansion (CTE) less than the CTE of substrate **103** that is deposited at a temperature greater than room temperature and the operating temperature of NMOS transistor **101**. Upon cooling, gate electrode **141** may contract more slowly than the surrounding materials and gate electrode **141** may then transfer a tensile strain to channel **105** via gate dielectric **131** or via spacers **109**. In an embodiment, the material that provides the additional tensile strain may be the n-type work function metal, as listed above. In other embodiments, the material that provides the additional tensile strain may be another material in the gate structure. In an embodiment, the material that provides the additional tensile strain may include tungsten. In another embodiment, the material that provides the additional tensile strain may include titanium carbide.
- [0042] Gate electrode **142** may include any suitable material or materials. In an embodiment, gate electrode **142** may include a p-doped polysilicon. In another embodiment, gate electrode **142** may include a metal with a p-type work function. In other embodiments, gate electrode **142** may include a stack or structure of various materials with the material in contact with gate dielectric **131** including a material with a p-type work function. In various embodiments, the p-type work function material may include ruthenium, palladium, platinum, cobalt, nickel, and their oxides.
- [0043] In an embodiment, gate electrode **142** may include a metal that provides an additional compressive strain on channel **112**. Gate electrode **142** may provide an additional compressive strain on channel **112** by including a material with a CTE greater than the CTE of substrate **103** that is deposited at a temperature greater than room temperature and the operating temperature of PMOS transistor **102**. Upon cooling, gate electrode **142** may contract more quickly than the surrounding materials and gate electrode **142** may then transfer a compressive strain to channel **112** via gate dielectric **131** or via spacers **116**. In an embodiment, the material that provides the additional compressive strain may be the p-type work function metal, as listed above. In other embodiments, the material that provides the additional compressive strain may be another material in the gate structure. In various embodiments, the material that provides the additional compressive strain may include boron carbide, tungsten, molybdenum, rhodium, vanadium, platinum, ruthenium, beryllium, palladium, cobalt, titanium, nickel, copper, tin, aluminum, lead, zinc, alloys of these metals, or their silicides.
- [0044] Gate electrode **141** and gate electrode **142** may be formed by any suitable technique. In an embodiment, gate electrode **141** may be selectively formed and then gate electrode **142** may be selectively formed. In an embodiment, gate electrode **142** may be selectively formed and then gate electrode **141** may be selectively formed.
- [0045] FIGS. 6-8 illustrate a method for forming gate electrodes with reference to the illustration of FIG. 4. As illustrated in FIG. 6, an n-type material **161** may be formed in trenches **121**, **122**. N-type material **161** may be any suitable n-type work function material as discussed above with reference to FIG. 5. In an embodiment, n-type material **161** may partially fill trenches **121**, **122**. In another embodiment, n-type material **161** may completely fill trenches **121**, **122**.
- [0046] As illustrated in FIG. 7, n-type material **161** may be selectively removed from PMOS transistor **102** and a p-type material **162** may be formed. P-type material **162** may be any suitable p-type work function material as discussed above with reference to FIG. 5. In an embodiment, p-type material **162** may be formed such that an opening remains in either or both of the trenches. In another embodiment, p-type material **162** may complete the gate structure of PMOS transistor **102** or NMOS transistor **101**.
- [0047] As illustrated in FIG. 8, fill material **171** and fill material **172** may be selectively formed. Fill materials **171**, **172** may be the same material or they may be different. In an embodiment, fill material **171** and fill material **172** may be chosen based on their conductive properties. In another embodiment, fill material **171** may be

chosen to provide a tensile strain on NMOS transistor **101** as discussed with respect to FIG. 5. In various embodiments, fill material **171** may include tungsten or titanium carbide.

[0048] Fill material **172** may also include any suitable material. In an embodiment, fill material **172** may be chosen to provide a compressive strain on PMOS transistor **102** as discussed with respect to FIG. 5. In some embodiments, fill material **172** may include boron carbide, tungsten, molybdenum, rhodium, vanadium, platinum, ruthenium, beryllium, palladium, cobalt, titanium, nickel, copper, tin, aluminum, lead, zinc, alloys of these metals, or their silicides.

[0049] As illustrated in FIGS. 6-8, n-type material **161** may be formed and selectively removed, p-type material **162** may be formed, and optional fill materials may be formed. In another embodiment, the n-type and p-type materials may be formed in the opposite order. For example, the p-type material may be formed first. Then, the p-type material may be selectively removed from NMOS transistor **101** and a subsequent n-type material may then be formed. Lastly, optional fill materials may then be formed.

[0050] The illustrated methods of FIGS. 3-8 show trenches **121**, **122** being formed and the stressors on channels **105**, **112** being allowed to simultaneously increase the strain on channels **105**, **112**. However, in other embodiments, trenches **121**, **122** may be formed and the strains increased independently. In an embodiment, trench **121** may be formed while gate dielectric **114** and gate electrode **115** remain. The strain on channel **105** of NMOS transistor **101** may then be independently increased. In another embodiment, trench **122** may be formed while gate dielectric **107** and gate electrode **108** remain. The strain on channel **112** of PMOS transistor **102** may then be independently increased.

[0051] The methods illustrated in FIGS. 3-8 show the entire gate structure being sacrificial. As illustrated in FIGS. 9-10, only a portion of the gate structure may be sacrificial.

[0052] In FIG. 9, gate electrodes **108**, **115** may be removed from the structure of FIG. 2 to form trenches **151**, **152**. Gate electrodes **108**, **115** may be removed by any suitable technique such as a selective etch technique.

[0053] Due to the removal of gate electrodes **108**, **115** the strain on channels **105**, **112** may be increased. The increased strain may be due to the removal of material from trenches **151**, **152**, which may have been an offsetting stress to the desired stresses as discussed above.

[0054] As illustrated in FIG. 10, gate electrodes **141**, **142** may be formed. Gate electrodes **141**, **142** may include any of the materials or attributes and may be formed by any of the methods as discussed above with respect to FIGS. 5-8.

[0055] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments.

[0056] It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of ordinary skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

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US7473947B2 *	2002-07-12	2009-01-06	Intel Corporation	Process for ultra-thin body SOI devices that incorporate EPI silicon tips and article made thereby
US6861712B2 *	2003-01-15	2005-03-01	Sharp Laboratories Of America, Inc.	MOSFET threshold voltage tuning with metal gate stack control
US7303949B2 *	2003-10-20	2007-12-04	International Business Machines Corporation	High performance stress-enhanced MOSFETs using Si:C and SiGe epitaxial source/drain and method of manufacture
US6967131B2 *	2003-10-29	2005-11-22	International Business Machines Corp.	Field effect transistor with electroplated metal gate
US7902058B2 *	2004-09-29	2011-03-08	Intel Corporation	Inducing strain in the channels of metal gate transistors
US7396724B2 *	2005-03-31	2008-07-08	International Business Machines Corporation	Dual-hybrid liner formation without exposing silicide layer to photoresist stripping chemicals
US7569443B2 *	2005-06-21	2009-08-04	Intel Corporation	Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gate
US8101485B2 *	2005-12-16	2012-01-24	Intel Corporation	Replacement gates to enhance transistor strain

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US20090087974A1 *	2007-09-29	2009-04-02	Andrew Waite	Method of forming high-k gate electrode structures after transistor fabrication
EP2061076A1 *	2007-11-13	2009-05-20	Interuniversitair Micro-Elektronica Centrum Vzw	Dual work function device with stressor layer and method for manufacturing the same
US20090194554A1 *	2008-02-06	2009-08-06	Gary Scott Bliss	Wipes Canister
US20090230479A1 *	2008-03-12	2009-09-17	Peng-Fu Hsu	Hybrid Process for Forming Metal Gates of MOS Devices
US20090298244A1 *	2007-03-11	2009-12-03	International Business Machines Corporation	Mobility Enhanced FET Devices
US20100052077A1 *	2008-08-27	2010-03-04	Taiwan Semiconductor Manufacturing Company, Ltd.	High-k metal gate structure including buffer layer
US20110001194A1 *	2007-01-23	2011-01-06	Taiwan Semiconductor Manufacturing Company, Ltd.	Hybrid Process for Forming Metal Gates
US20110210380A1 *	2010-02-26	2011-09-01	Thilo Scheiper	Contact bars with reduced fringing capacitance in a semiconductor device
US8211775B1	2011-03-09	2012-07-03	United Microelectronics Corp.	Method of making transistor having metal gate
US8278166B2	2010-07-16	2012-10-02	United Microelectronics Corp.	Method of manufacturing complementary metal oxide semiconductor device
US20120256276A1 *	2011-04-07	2012-10-11	Guang-Yaw Hwang	Metal Gate and Fabricating Method Thereof
CN102737971A *	2011-04-15	2012-10-17	联华电子股份有限公司	semiconductor element with metal gate and manufacturing method thereof
CN103077969A *	2011-10-26	2013-05-01	中国科学院微电子研究所	A kind of MOS device and its manufacturing method
US8486790B2	2011-07-18	2013-07-16	United Microelectronics Corp.	Manufacturing method for metal gate
CN103258823A *	2012-02-16	2013-08-21	国际商业机器公司	Semiconductor structure and formation method thereof
US8519487B2	2011-03-21	2013-08-27	United Microelectronics Corp.	Semiconductor device
US8536038B2	2011-06-21	2013-09-17	United Microelectronics Corp.	Manufacturing method for metal gate using ion implantation
US20130241004A1 *	2012-03-14	2013-09-19	Huaxiang Yin	Semiconductor device and method of manufacturing the same
US8551876B2	2011-08-18	2013-10-08	United Microelectronics Corp.	Manufacturing method for semiconductor device having metal gate
US20140001566A1 *	2008-08-18	2014-01-02	Taiwan Semiconductor Manufacturing Company, Ltd.	Method Of Forming A Single Metal That Performs N Work Function And P Work Function In A High-K/Metal Gate Process
US8673758B2	2011-06-16	2014-03-18	United Microelectronics Corp.	Structure of metal gate and fabrication method thereof
US8691681B2	2012-01-04	2014-04-08	United Microelectronics Corp.	Semiconductor device having a metal gate and fabricating method thereof
US8735269B1	2013-01-15	2014-05-27	United Microelectronics Corp.	Method for forming semiconductor structure having TiN layer
US20140264640A1 *	2013-03-18	2014-09-18	Nanya Technology Corp.	Semiconductor device and method for fabricating the same
US20140299938A1 *	2013-04-03	2014-10-09	Stmicroelectronics, Inc.	Methods and devices for enhancing mobility of charge carriers
US8860181B2	2012-03-07	2014-10-14	United Microelectronics Corp.	Thin film resistor structure
US8872286B2	2011-08-22	2014-10-28	United Microelectronics Corp.	Metal gate structure and fabrication method thereof
US8921947B1	2013-06-10	2014-12-30	United Microelectronics Corp.	Multi-metal gate semiconductor device having triple diameter metal opening
US8975666B2	2012-08-22	2015-03-10	United Microelectronics Corp.	MOS transistor and process thereof
US9054172B2	2012-12-05	2015-06-09	United Microelectrnics Corp.	Semiconductor structure having contact plug and method of making the same
US9105720B2	2013-09-11	2015-08-11	United Microelectronics Corp.	Semiconductor device having metal gate and manufacturing method thereof
US9105623B2	2012-05-25	2015-08-11	United Microelectronics Corp.	Semiconductor device having metal gate and manufacturing method thereof
US20150287740A1 *	2014-04-02	2015-10-08	International Business Machines Corporation	Strain engineering in back end of the line
US9159798B2	2013-05-03	2015-10-13	United Microelectronics Corp.	Replacement gate process and device manufactured using the same
US9196546B2	2013-09-13	2015-11-24	United Microelectronics Corp.	Metal gate transistor
US9196542B2	2013-05-22	2015-11-24	United Microelectronics Corp.	Method for manufacturing semiconductor devices

US9231071B2	2014-02-24	2016-01-05	United Microelectronics Corp.	Semiconductor structure and manufacturing method of the same
US20160013107A1 *	2014-07-11	2016-01-14	Samsung Electronics Co., Ltd.	Methods of forming semiconductor devices, including performing a heat treatment after forming a metal layer and a high-k layer
CN105742353A *	2014-12-11	2016-07-06	中芯国际集成电路制造(上海)有限公司	MOS transistor and formation method thereof
US9406516B2	2013-09-11	2016-08-02	United Microelectronics Corp.	High-K metal gate process for lowering junction leakage and interface traps in NMOS transistor
US9437714B1 *	2015-12-09	2016-09-06	International Business Machines Corporation	Selective gate contact fill metallization
US20160315100A1 *	2015-04-21	2016-10-27	United Microelectronics Corp.	Semiconductor device and method of forming the same
US9653300B2	2013-04-16	2017-05-16	United Microelectronics Corp.	Structure of metal gate structure and manufacturing method of the same
US9947772B2	2014-03-31	2018-04-17	Stmicroelectronics, Inc.	SOI FinFET transistor with strained channel
CN109980004A *	2017-12-27	2019-07-05	中芯国际集成电路制造(上海)有限公司	Semiconductor structure and forming method thereof
US11342231B2 *	2019-09-17	2022-05-24	Taiwan Semiconductor Manufacturing Co., Ltd.	Integrated circuit device with low threshold voltage
US20220181218A1 *	2018-09-28	2022-06-09	Taiwan Semiconductor Manufacturing Co., Ltd.	Gate structure and patterning method
WO2024258604A1 *	2023-06-12	2024-12-19	Qualcomm Incorporated	Field-effect transistors (fets) employing thermal expansion of work function metal layers for strain effect and related fabrication methods
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US8101485B2 *	2005-12-16	2012-01-24	Intel Corporation	Replacement gates to enhance transistor strain
JP5380827B2 *	2006-12-11	2014-01-08	ソニー株式会社	Manufacturing method of semiconductor device
JP5288789B2 *	2007-12-28	2013-09-11	株式会社東芝	Semiconductor device and manufacturing method thereof
US8122394B2 *	2008-09-17	2012-02-21	Taiwan Semiconductor Manufacturing Company, Ltd.	Performance-aware logic operations for generating masks
KR101556238B1 *	2009-02-17	2015-10-01	삼성전자주식회사	Method of manufacturing semiconductor device having buried wiring line
US20110147831A1 *	2009-12-23	2011-06-23	Steigerwald Joseph M	Method for replacement metal gate fill
US8232148B2 *	2010-03-04	2012-07-31	International Business Machines Corporation	Structure and method to make replacement metal gate and contact metal
CN102194693B *	2010-03-16	2013-05-22	中国科学院微电子研究所	Semiconductor device and manufacturing method thereof
JP5548224B2 *	2012-03-16	2014-07-16	富士フイルム株式会社	Semiconductor substrate product manufacturing method and etching solution
KR20130127257A	2012-05-14	2013-11-22	삼성전자주식회사	Semiconductor device and method for manufacturing the device
US8741717B2 *	2012-07-02	2014-06-03	GlobalFoundries, Inc.	Methods for fabricating integrated circuits having improved metal gate structures
FR2995135B1 *	2012-09-05	2015-12-04	Commissariat Energie Atomique	METHOD FOR PRODUCING FET TRANSISTORS
DE102014007470A1	2013-11-15	2015-05-21	Linde Aktiengesellschaft	Process and apparatus for steam reforming and steam cracking of hydrocarbons
KR102311552B1	2014-12-04	2021-10-12	삼성전자주식회사	Semiconductor device and method for manufacturing of the same
KR102235612B1	2015-01-29	2021-04-02	삼성전자주식회사	Semiconductor device having work-function metal and method of forming the same
FR3078108B1 *	2018-02-20	2020-01-31	Safran Nacelles	PROPELLANT ASSEMBLY COMPRISING LIFTING POINTS ARRANGED ON SUPPORTS OF PUSH-INVERTER CYLINDERS
KR102550652B1	2018-04-02	2023-07-05	삼성전자주식회사	Method for manufacturing semiconductor device
US11158721B2 *	2019-08-30	2021-10-26	Taiwan Semiconductor Manufacturing Co., Ltd.	Metal oxide interlayer structure for nFET and pFET
FI3889222T3	2020-03-30	2025-08-21	Henkel Ag & Co Kgaa	Curable potting composition free of substances of very high concern
KR102934380B1	2020-04-24	2026-03-05	에이에스엠 아이피 홀딩 비.브이.	Methods of forming structures including vanadium boride and vanadium phosphide layers

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US20230307455A1	2023-09-28	Replacement metal gates to enhance transistor strain
US12342610B2	2025-06-24	Method of manufacturing semiconductor device
US7112495B2	2006-09-26	Structure and method of a strained channel transistor and a second semiconductor component in an integrated circuit
US10811516B2	2020-10-20	Structure and formation method of semiconductor device structure with gate stack
US7545001B2	2009-06-09	Semiconductor device having high drive current and method of manufacture therefor
US9240351B2	2016-01-19	Field effect transistor device with improved carrier mobility and method of manufacturing the same
US7151023B1	2006-12-19	Metal gate MOSFET by full semiconductor metal alloy conversion
JP4630728B2	2011-02-09	Semiconductor device and manufacturing method thereof
CN104051276A	2014-09-17	Stressed field effect transistor and methods for its fabrication
US7166876B2	2007-01-23	MOSFET with electrostatic discharge protection structure and method of fabrication
US20080054347A1	2008-03-06	Composite stressors in MOS devices
US8932921B2	2015-01-13	N/P metal crystal orientation for high-k metal gate Vt modulation
US9054188B2	2015-06-09	Curved wafer processing on method and apparatus
US20140210011A1	2014-07-31	Dual Silicide Process
KR20110126711A	2011-11-23	Metal Oxide Semiconductor Devices With Doped Silicon-comprising Capping Layers and Methods of Making the Same
US9780209B1	2017-10-03	Semiconductor device and manufacturing method thereof
US20080272432A1	2008-11-06	Accumulation mode mos devices and methods for fabricating the same

Priority And Related Applications

Child Applications (2)

Application	Priority date	Filing date	Relation	Title
US12/288,937	2005-12-16	2008-10-24	Division	Replacement gates to enhance transistor strain
US13/233,297	2005-12-16	2011-09-15	Division	Replacement gates to enhance transistor strain

Priority Applications (8)

Application	Priority date	Filing date	Title
US11/305,465	2005-12-16	2005-12-16	Replacement gates to enhance transistor strain
US12/288,937	2005-12-16	2008-10-24	Replacement gates to enhance transistor strain
US13/233,297	2005-12-16	2011-09-15	Replacement gates to enhance transistor strain
US13/909,792	2005-12-16	2013-06-04	Replacement gates to enhance transistor strain
US14/573,242	2005-12-16	2014-12-17	Replacement metal gates to enhance transistor strain
US14/882,434	2005-12-16	2015-10-13	Replacement metal gates to enhance tranistor strain
US15/141,777	2005-12-16	2016-04-28	Replacement metal gates to enhance transistor strain
US18/204,231	2005-12-16	2023-05-31	Replacement metal gates to enhance transistor strain

Applications Claiming Priority (1)

Application	Filing date	Title
US11/305,465	2005-12-16	Replacement gates to enhance transistor strain

Legal Events

Date	Code	Title	Description
2005-12-16	AS	Assignment	Owner name: INTEL CORPORATION, CALIFORNIA Free format text: ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:BOHR, MARK T.;REEL/FRAME:017354/0805

Effective date: 20051211			
2012-01-04	STCF	Information on status: patent grant	Free format text: PATENTED CASE
2015-07-08	FPAY	Fee payment	Year of fee payment: 4
2016-12-03	FEPP	Fee payment procedure	Free format text: PAYER NUMBER DE-ASSIGNED (ORIGINAL EVENT CODE: RMPN); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY Free format text: PAYOR NUMBER ASSIGNED (ORIGINAL EVENT CODE: ASPN); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY
2019-07-11	MAFP	Maintenance fee payment	Free format text: PAYMENT OF MAINTENANCE FEE, 8TH YEAR, LARGE ENTITY (ORIGINAL EVENT CODE: M1552); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY Year of fee payment: 8
2023-06-21	MAFP	Maintenance fee payment	Free format text: PAYMENT OF MAINTENANCE FEE, 12TH YEAR, LARGE ENTITY (ORIGINAL EVENT CODE: M1553); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY Year of fee payment: 12

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