

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED,

Patent Owner.

Case No. IPR2026-00261

U.S. Patent No. 7,888,195 B2

DECLARATION OF JOSEPH MCALEXANDER

I. QUALIFICATIONS

1. I am a Registered Professional Engineer (#79454) and the President of McAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and

measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

II. OVERVIEW

4. In my opinion, none of the Petition grounds discloses each element of any challenged claim of U.S. Patent Number 7,888,195 (“the ’195 Patent”). For example, neither of the asserted primary references (Bohr and Brask) teach the claimed “first cap layer” recited in independent claim 1.

5. **Grounds 1A-1F (Bohr):** Bohr fails to disclose or render obvious the claimed “first cap layer.” The Petition alleges that “Bohr’s n-type material 161 corresponds to the claimed first cap layer.” Not so. Bohr’s n-type material 161 is a conductive n-type metal layer with a specific work function suitable for an n-type (or NMOS) gate. In other words, Bohr’s n-type material 161 is a part of the gate electrode itself, rather than being an insulating oxide layer. In contrast, the ’195 Patent’s “cap layer” is an insulating oxide layer, rather than a conductive metal layer. Moreover, in the ’195 Patent, “the present invention specifically uses the cap layer 56 to define the work function of the metal layer 60.” EX1001, 4:43-46. For example, “[i]n the aforementioned embodiment, a cap layer 56 composed of La_2O_3 is deposited before the formation of the metal layer 60 to define the work function of n-type metal.” *Id.*, 4:47-50. That is, the ’195 Patent’s cap layer is an insulating oxide layer that defines the work function of the n-type gate metal, rather than being an n-type metal itself. The ’195 Patent’s “metal layer 60” is the n-type metal layer. Conversely, Bohr’s n-type material is made from an “n-type work function material”—that is, Bohr’s n-type material is the n-type metal layer itself, rather than defining the work function of the n-type metal. Thus, Bohr’s “n-type material” is not the claimed “first cap layer” but rather is more akin to the ’195 Patent’s claimed “metal layer.”

6. **Grounds 2A-2E:** Brask fails to disclose or render obvious the claimed “first cap layer.” The Petition alleges that Brask’s “metal layer 116” is the claimed “first cap layer” of the challenged claims, but that is incorrect. Brask specifically states that its “metal layer 116” is not a “capping layer.” EX1005-Brask, ¶[0031] (“Although in some embodiments it may be desirable to form a capping layer on high-k gate dielectric layer 115, in the illustrated embodiment, metal layer 116 is formed directly on layer 115 to generate the FIG. 1c structure.”). Moreover, like Bohr’s “n-type material 161”, Brask’s “metal layer 116” is a conductive metal layer that is a part of the gate electrode itself, rather than being an insulating oxide layer.

III. MATERIALS CONSIDERED

7. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner’s expert, as well as the materials that they cite, including U.S. Patent No. 7,888,195 B2 (the “’195 Patent”), the ’195 Patent prosecution history, and the asserted prior art. The prior art asserted by the Petition to which I direct my analysis includes Bohr (EX1004) and Brask (EX1005).

IV. UNDERSTANDING OF THE LAW

8. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

9. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

- a. a method claim, which covers a process/activity, or
- b. an apparatus claim, which covers a physical machine, etc.

10. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an *inter partes* review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

11. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

12. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an *inter partes* review proceeding is by a preponderance of the evidence.

13. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

14. I have been informed that, in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

15. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that, for such objective evidence to be relevant to the non-obviousness of a claim, there must be a causal relationship (called a “nexus”)

between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

16. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

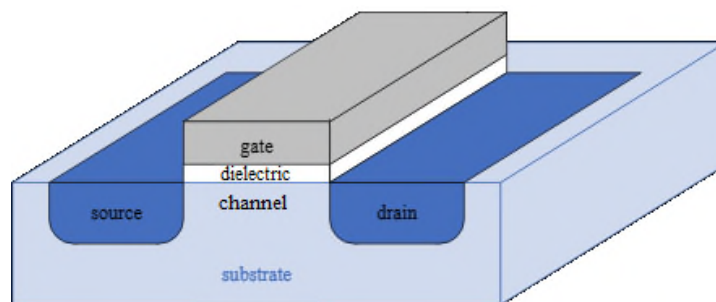
17. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; and (2) common process steps for creating transistors.

A. Basic Transistor Components

18. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). EX2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. EX2002 at 3.

19. One type of transistor typically used in an integrated circuit (or “chip”) is a “field effect transistor,” or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. EX2002 at 29-34. In a conductor (*e.g.*, a metal), electric current can flow freely. EX2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. EX2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. EX2002 at 31-34.

20. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See, e.g.*, EX2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.

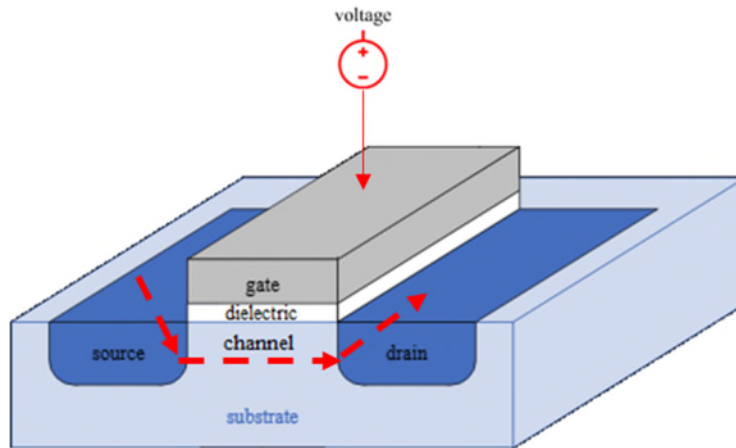


See, e.g., EX2002 at 510-511.

21. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). EX2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). EX2002 at 510-511.

22. The gate is a conductor (or semiconductor) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. EX2002 at 510-511. When a voltage is applied to the gate, the dielectric prevents the “flow of charge” (current) between the gate and the channel, but the applied voltage results in the creation of a “field effect” in the channel. EX2002 at 510-511. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). EX2002 at 510-511.

23. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current.



See, e.g., EX2002 at 510-511 (annotated).

B. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

24. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

25. In the first stage, the semiconductor material itself is created. EX2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. EX2002 at 13.

26. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” EX2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

27. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. EX2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. EX2002 at 14.

28. In the packaging stage, the wafer is separated into individual chips. EX2002 at 14-15.

2. The Wafer Fabrication Stage

29. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. EX2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). See EX2002 at 29-31, 71. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

30. **Layering** is the operation used to add thin layers to the semiconductor substrate. EX2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. EX2002 at 72.

31. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. EX2002 at 72.

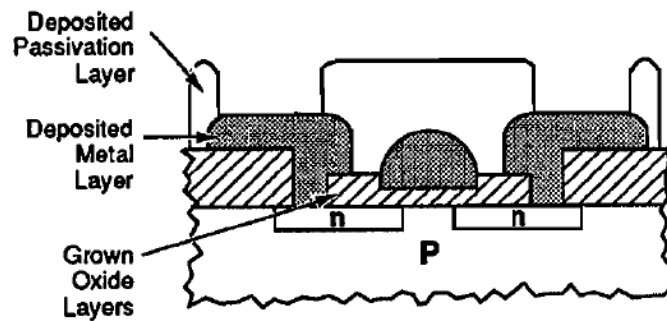


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

32. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. EX2002 at 72-73. This creates a pattern on the wafer surface. EX2002 at 72-73.

33. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. EX2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

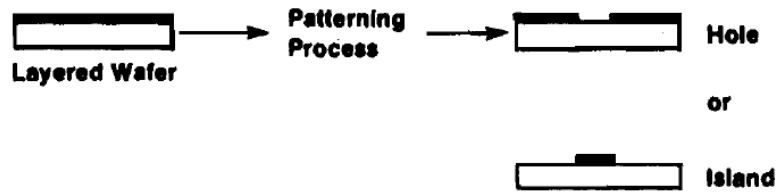


Figure 4.7 Patterning.

34. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

EX2002 at 73.

VI. THE CHALLENGED '195 PATENT

A. The Prior Art Problem and Exemplary Solution

35. The '195 Patent's "invention relates to a method for fabricating a transistor, and more particularly, to a method for fabricating a metal gate transistor." EX1001, 1:7-9. At the time of the '195 Patent, "polysilicon materials [were] commonly used to fabricate gate electrodes" due to these materials' "strong resistance for heat." *Id.*, 1:11-14. "However, devices fabricated by polysilicon still have many drawbacks." *Id.*, 1:18-19. For example, as the '195 Patent explains,

polysilicon gates generally perform at a lower rate compared to metal gates, necessitating further processing to increase the performance to an acceptable level:

In contrast to most metal, polysilicon gates are fabricated by semiconductor materials having high resistance, which causes the polysilicon gate to work under a much lower rate than other metal gates. In order to compensate for slightly lowered rate of performance, a significant amount of silicides is applied during the fabrication of polysilicon processes, such that the performance of the device could be increased to an acceptable level.

Id., 1:19-26.

36. Another drawback of polysilicon gates is that “[g]ate electrodes fabricated by polysilicon also causes a depletion effect.” *Id.*, 1:27-28. Polysilicon gates have a limited doping concentration, which “often results in a depletion region at the interface between the gate and the gate dielectric layer.” *Id.*, 1:28-33. “This depletion region not only thickens the gate dielectric layer, but also lowers the capacitance of the gate, and ultimately reduces the driving ability of the device.” *Id.*, 1:34-36. The ’195 Patent provides a solution to this problem: “In order to solve this problem, double work function metal gates are used to replace conventional polysilicon to fabricate gate electrodes for MOS transistors.” *Id.*, 1:36-39.

37. “However, it is well known in the art that the degree of difficulty for fabricating a well-controlled double work function metal is immense as the process

often involves complicated integration between NMOS device and PMOS device.”

Id., 1:40-42. “The difficulty increases even more as the thickness and materials used in double work function metal gates requires a much more strict demand.” *Id.*, 1:44-46. “Hence, how to successfully fabricate double work function metal gate transistor with lower cost and improved performance has become an important task in this field.” *Id.*, 1:46-49. Thus, the ’195 Patent provides a lower cost method of fabricating a double work function metal gate transistor that offers improved performance.

38. The ’195 Patent’s “FIGS. 1-8 illustrate a method for fabricating a metal gate transistor according to a preferred embodiment of the present invention.” EX1001, 2:31-33. “As shown in FIG. 1, a substrate 12, such as a silicon substrate or a silicon-on-insulator substrate is provided.”

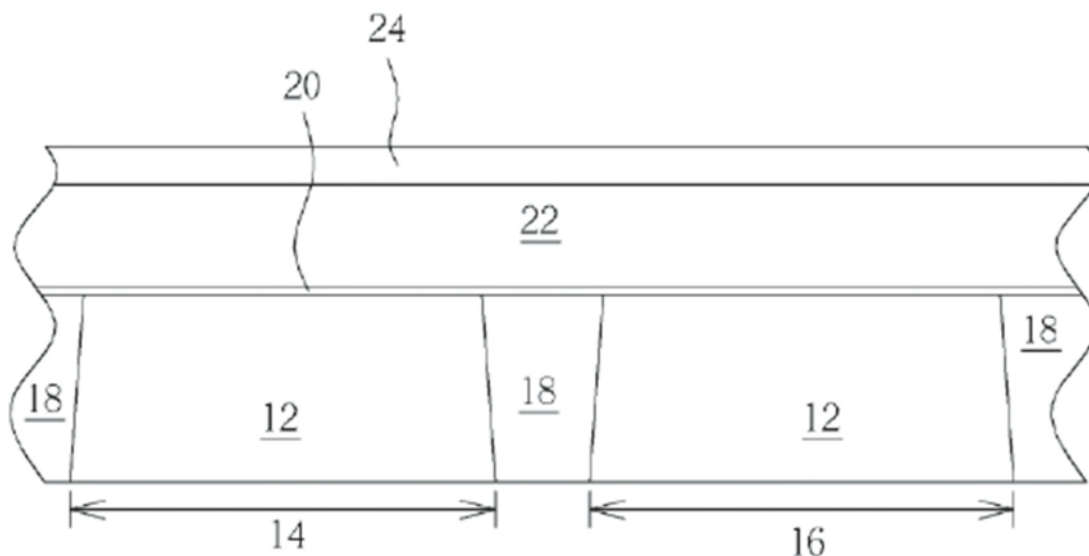


FIG. 1

Id., 2:33-35, Fig. 1.

39. “At least a NMOS transistor region 14 and a PMOS transistor region 16 are defined in the substrate 12.” *Id.*, 2:35-37. As shown, “gate insulating layer 20... is then formed on the surface of the substrate 12” and “polysilicon layer 22 serving as a dummy gate layer is deposited on the gate insulating layer.” *Id.*, 2:39-47. These layers are subsequently etched and “a plurality of dummy gates, such as the polysilicon gates 26 shown in this embodiment is formed in the NMOS transistor region 14 and the PMOS transistor region 16,” as shown in Fig. 2:

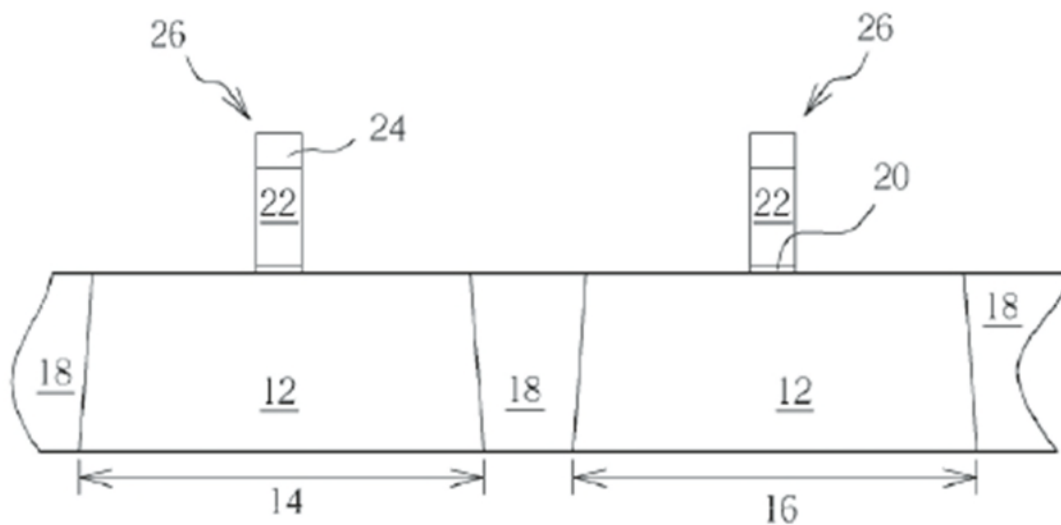


FIG. 2

Id., 2:55-64, Fig. 2.

40. These polysilicon dummy gates are later removed to form metal gates, as explained in more detail below.

41. In Fig. 4, source/drain regions (42 and 44) are formed in both the NMOS and PMOS transistor regions at two sides of the dummy gates:

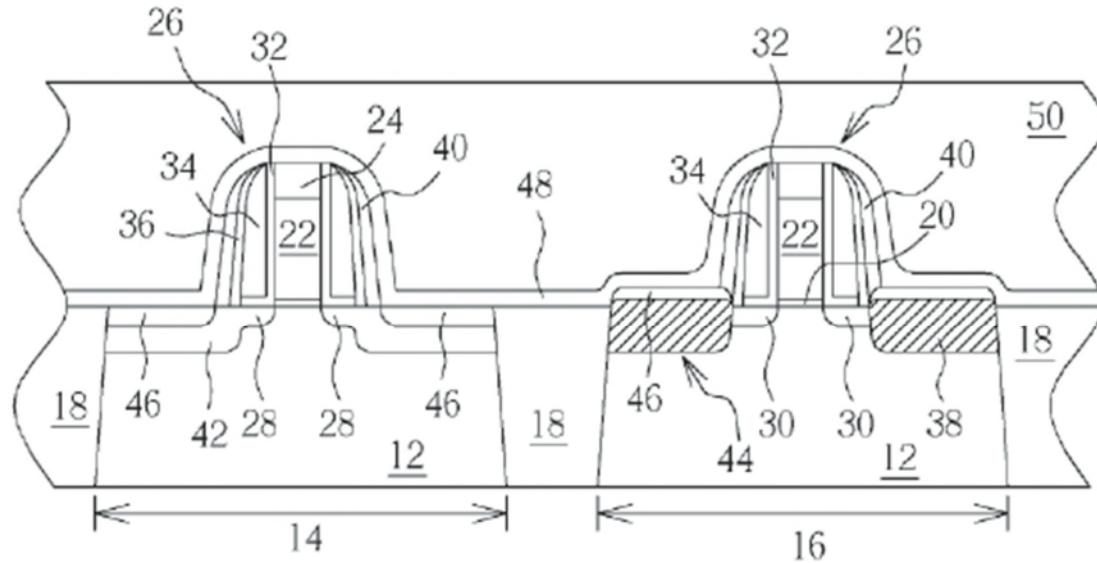


FIG. 4

EX1001, 3:36-52, Fig. 4.

42. Subsequently, as shown in Fig. 4 above, “[a]n interlayer dielectric layer 50 composed of oxides is then deposited,” covering both transistor regions. *Id.*, 3:64-67. This interlayer dielectric layer is then polished or etched down to the surface of the polysilicon dummy gates 26, as shown in Fig. 5:

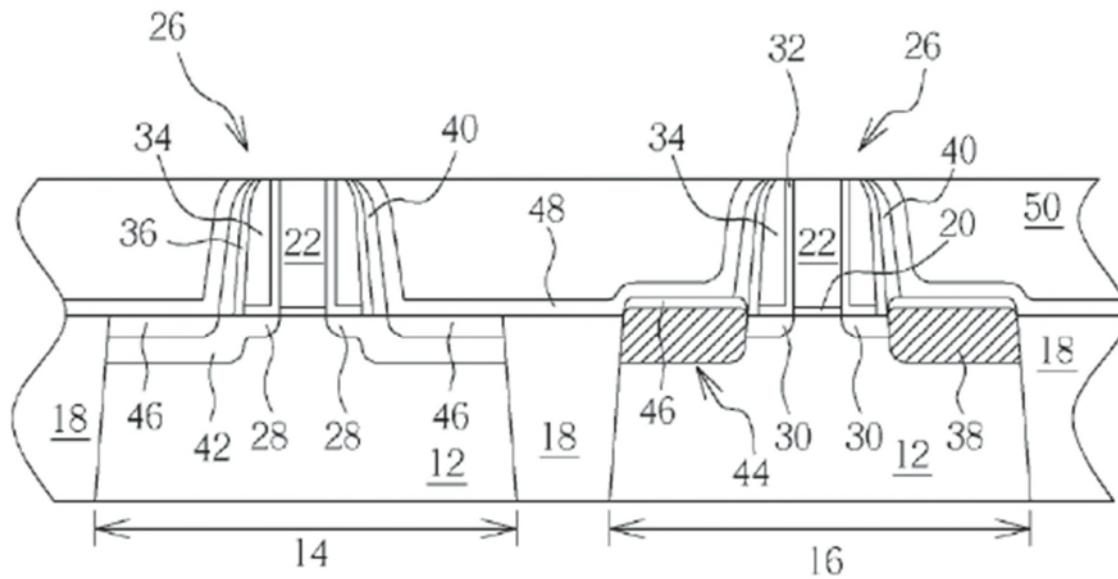


FIG. 5

EX1001, 4:1-7, Fig. 5.

43. At this point, the dummy gates are removed to be replaced by metal gates. "As shown in FIG. 6, a selective etching process is conducted... to remove the polysilicon gate 26 disposed in the NMOS transistor region 14 and the PMOS transistor region 16 without damaging the interlayer dielectric layer 50."

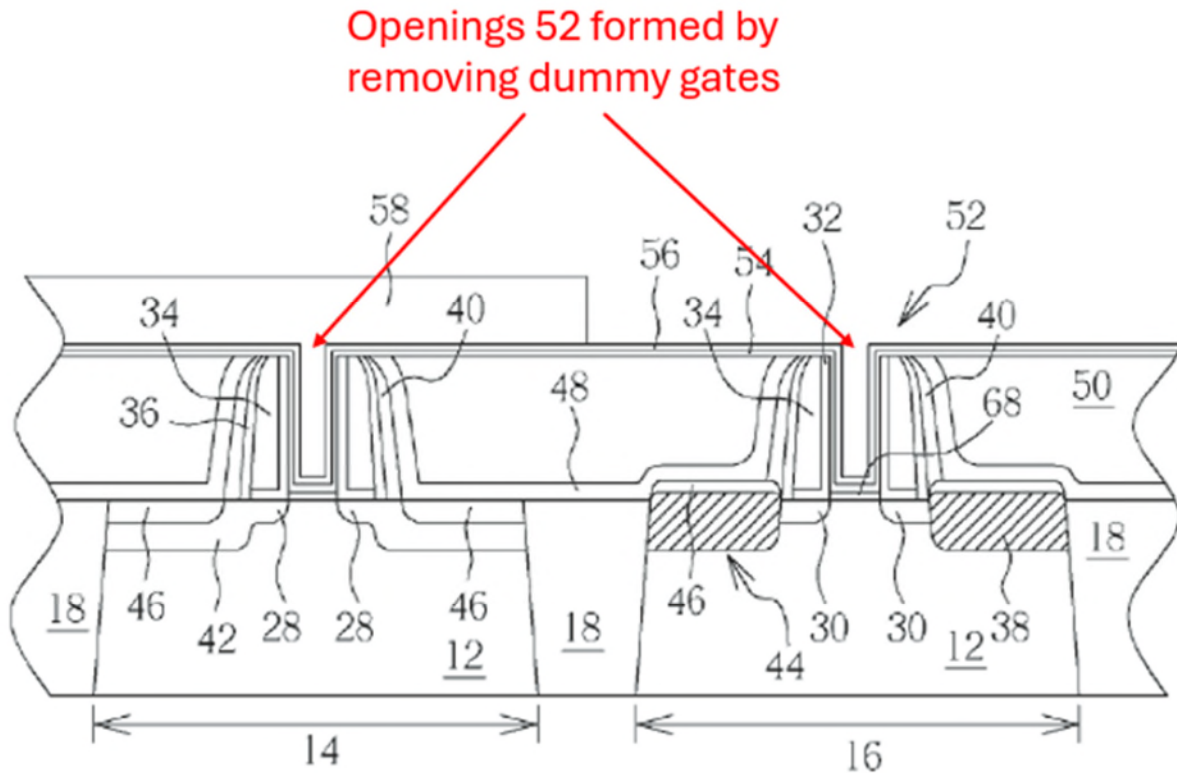
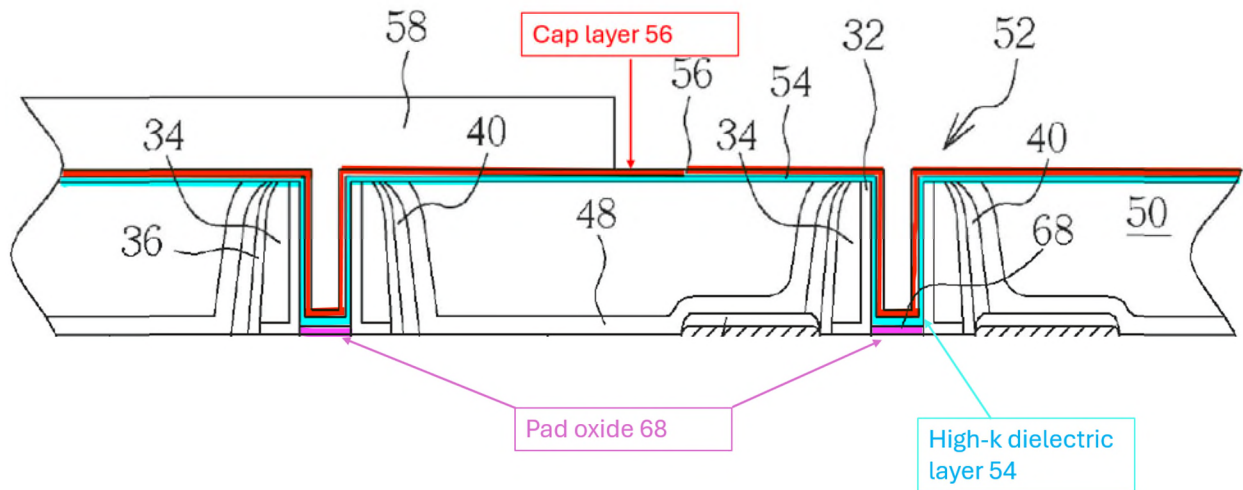


FIG. 6

Id., 4:8-13, Fig. 6 (annotated).

44. “[T]he etching process preferably removes the polysilicon gate 26 and forms an opening 52 in each transistor region 14, 16 for exposing the gate insulating layer 20 underneath.” *Id.*, 4:15-17.

45. In addition to showing the formation of openings 52 by removing the dummy gates, Figure 6 also shows the formation of several layers on the device, namely a pad oxide 68, a high-k dielectric layer 54, and a cap layer 56:



Id., 4:18-27, Fig. 6 (partial and annotated).

46. “[A] pad oxide 68, a high-k dielectric layer 54 and a cap layer 56 are sequentially deposited over the surface of the interlayer dielectric layer 50 of the two transistor regions 14, 16 and the sidewall and bottom of the openings 52.” *Id.*, 4:20-24.

47. Also shown in Fig. 6, “[a] patterned photoresist 58 is then disposed on the NMOS transistor region 14.” *Id.*, 4:33-34. “[A]n etching process is carried out by using the patterned photoresist 58 as a mask to remove the cap layer 56 in the PMOS transistor region 16.” *Id.*, 4:34-36. The result of this etching process is shown in Figure 7, in which the cap layer 56 in the PMOS transistor region 16 has been removed:

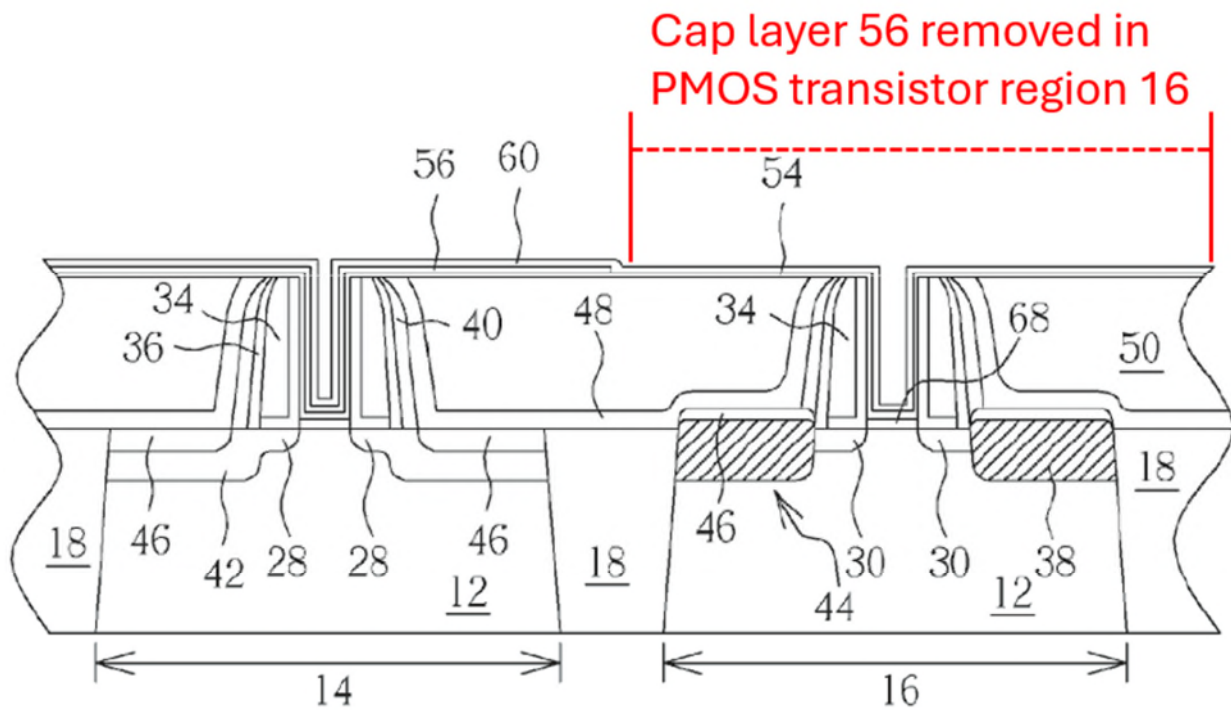
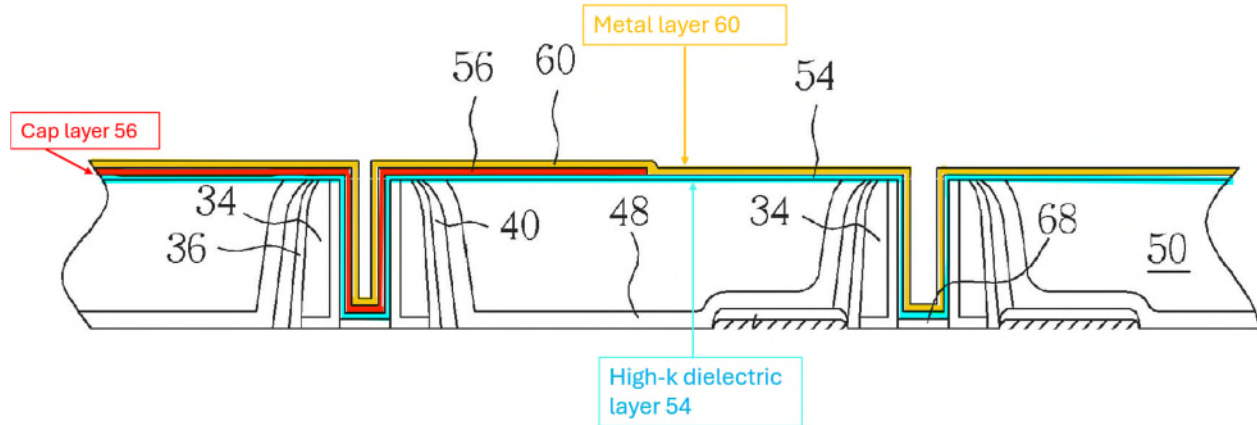


FIG. 7

Id., Fig. 7 (annotated).

48. Moreover, “[a]s shown in FIG. 7, after stripping the patterned photoresist 58, a metal layer 60 is deposited on the cap layer 56 of the NMOS transistor region 14 and the high-k dielectric layer 54 of the PMOS transistor region 16.”



Id., 4:37-40, Fig. 7 (partial and annotated).

49. Finally, as shown in Fig. 8, “a conductive layer 62 composed of low resistance material is selectively deposited on the metal layer 60 of the NMOS transistor region 14 and the PMOS transistor region 16 to fill the openings 52.”

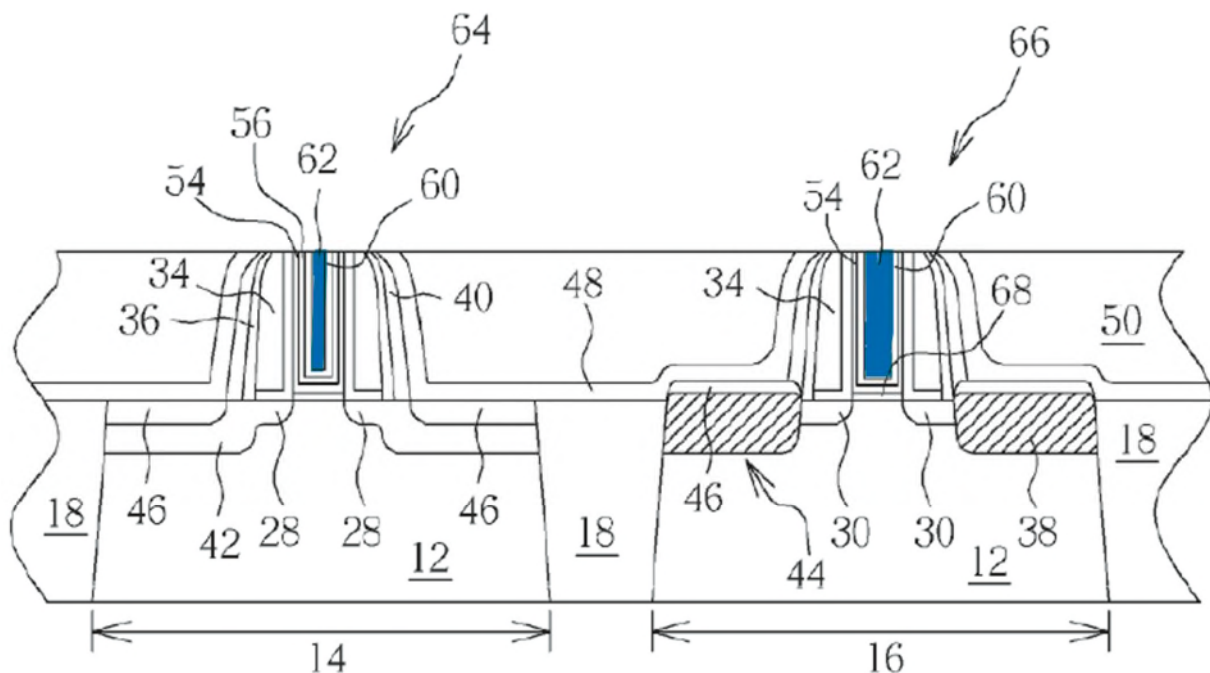


FIG. 8

Id., 4:61-65, Fig. 8 (annotated).

50. Figure 8 “illustrates a schematic view of a CMOS transistor with metal gates 64, 66 fabricated by the aforementioned process.” *Id.*, 5:4-6. “The metal gate 64 of the NMOS transistor region 14 includes a pad oxide disposed on the bottom of the metal gate 64, a U-shaped high-k dielectric layer 54 disposed on the pad oxide 68 and covering the sidewall of the metal gate 64, a U-shaped cap layer 56 disposed on the U-shaped high-k dielectric layer 54, a U-shaped metal layer 60 disposed on the U-shaped cap layer 56, and a substantially I-shaped conductive layer 62 filling the remaining opening of the metal gate 64.” *Id.*, 5:11-19. As shown, the metal gate 66 disposed in the PMOS transistor region 16 includes the same layers, except for the cap layer 56, which was removed. *Id.*, 5:20-30.

B. The Claimed “First Cap Layer” And “Metal Layer”

51. A critical aspect of the ’195 Patent’s fabrication method is the formation of the cap layer. The cap layer serves two important functions in the ’195 Patent’s fabrication process: (1) protecting the underlying NMOS transistor region during processing of the PMOS transistor region (by serving as a “cap”); and (2) defining the work function of the metal layer in the NMOS transistor region.

52. As explained above, after the removal of the dummy gates, the cap layer is disposed on top of the high-k dielectric layer. The ’195 Patent explains that “the cap layer 56 comprises La_2O_3 , MgO , Dy_2O_3 , or other lanthanide oxides.” EX1001,

4:26-27. This teaches that the cap layer is an insulating oxide layer, rather than a conductive metal layer.

53. The cap layer is then removed in the PMOS transistor region before a metal layer is formed. That is, in the NMOS transistor region, the cap layer is retained and the metal layer is formed on top of the cap layer. A unique aspect of the '195 Patent's cap layer is the usage of the cap layer to define the work function of the metal gate: "It should be noted that the present invention specifically uses the cap layer 56 to define the work function of the metal layer 60." EX1001, 4:43-46. I agree with Petitioner's expert that the work function of a metal gate electrode represents the minimum energy required to remove an electron from the gate electrode and is tuned to establish a threshold voltage, which dictates the specific voltage required to switch the transistor. EX1003-Lee-Decl, ¶47. Within the invention of the '195 Patent, the cap layer defines the work function of the overlying metal layer, which is a part of the gate electrode. Thereby, the cap layer and metal layer work together to tune the work function of the metal gate electrode.

54. For example, "[i]n the aforementioned embodiment, a cap layer 56 composed of La_2O_3 is deposited before the formation of the metal layer 60 to define the work function of n-type metal." *Id.*, 4:47-50. That is, the cap layer is an insulating oxide layer that defines the work function of the n-type gate metal, rather than being an n-type metal itself. The language of the specification is clear that this

function of the cap layer is a “specific” requirement of “the present invention” of the ’195 Patent. EX1001, 4:43-46.

C. Prosecution History

55. The Petition alleges that “Patent Owner acknowledge[d] during prosecution of the ’195 patent that a cap metal layer ‘may be construed as the first cap layer of the present invention.’” Pet., 21 (citing EX1002, 88-89). I disagree. The portion of the file history that the Petition cites to (pages 88-89) is an Office Action Response. The relevant passage is in response to a rejection based on the Doczy reference (EX1024), which discloses a “cap metal layer 115.” EX1024-Doczy939, ¶[0020]. In the Office Action Response, Applicant wrote: “Despite this cap layer 115a/115 may be construed as the first cap layer of the present invention, the cap layer 115a/115 is not removed from the second transistor region 202 and there is no metal layer formed on the cap layer 115a/115 of the first transistor region thereafter, as recited in claim 1 of the present invention.” EX1002, 88-89. I understand this passage as Applicant arguing that *even if* Doczy’s cap metal layer 115 could be construed as a “cap layer,” it still did not meet other requirements of the claimed cap layer. The Petition apparently interprets this sentence as conceding that any metal layer can be a cap layer. I disagree that Applicant made such a concession.

Doczy's "cap metal layer 115"

160 190 115 112 180

201 202 100 138 103 138a

This diagram shows a cross-sectional view of a semiconductor device. A blue cross-hatched layer, labeled 115, is identified as Doczy's "cap metal layer". It covers the top of the device. Below it, a layer 112 is visible. The device features a central opening 190 and side openings 160. A layer 180 is located between the cap metal layer 115 and the central opening 190. The device is supported by a substrate 100, which has a layer 138 and a layer 103. A layer 138a is also shown. Arrows 201 and 202 point to the substrate 100 and the layer 138, respectively.

Id., Fig. 10 (annotated).

Page 27 of 46

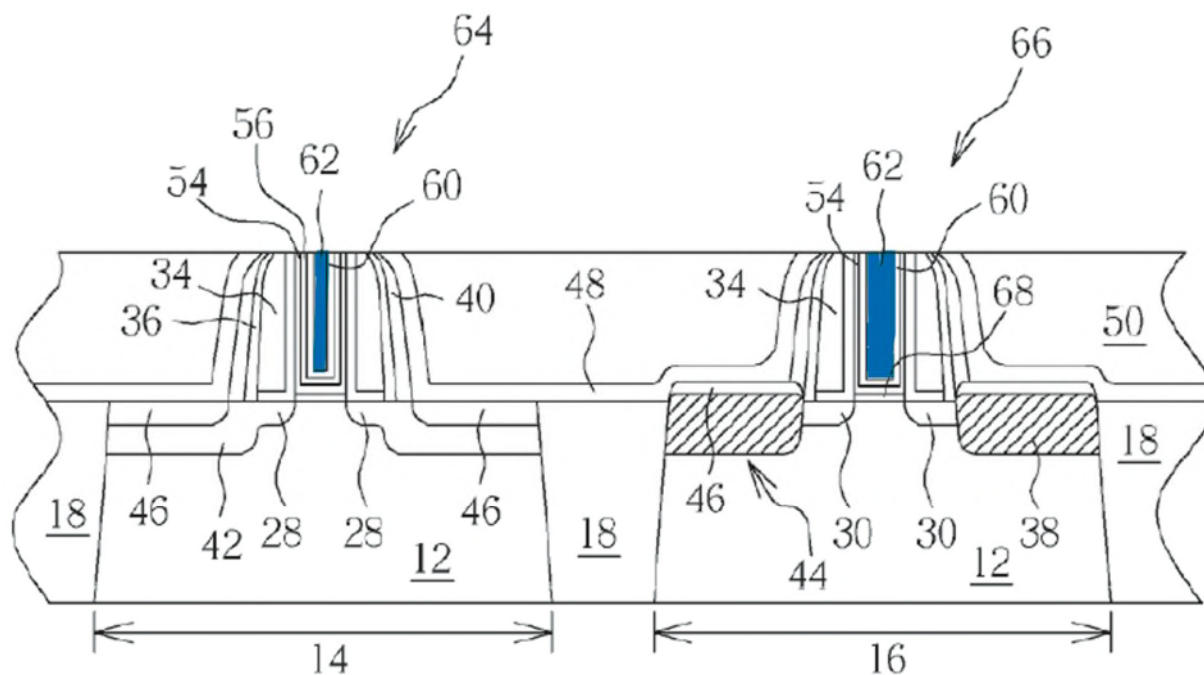


FIG. 8

EX1001, Fig. 8 (annotated).

58. Doczy's cap metal layer 115 is formed on top of "n-type metal layer 190." EX1024-Doczy939, ¶¶[0011]-[0012], [0048].

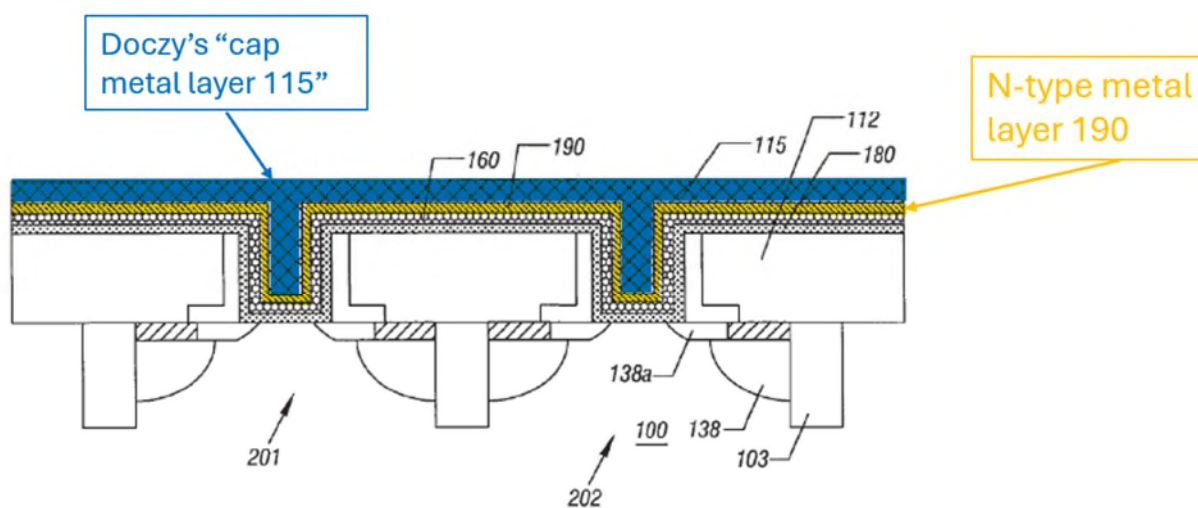


FIG. 10

Id., Fig. 10 (annotated).

59. Thus, Doczy specifically distinguishes a cap layer from an n-type metal layer. Even if Doczy's "cap metal layer 115" could be construed as a "cap", it still would not satisfy the requirements of the claimed "first cap layer" because no additional layers are formed on top of the cap metal layer 115. That is exactly what Applicant argued in the Office Action Response. EX1002, 88-89.

D. The Challenged Claims

60. The Petition challenges independent claim 1 and dependent claims 2-11, each of which includes the foregoing inventive concepts and combinations. For example, independent claim 1 recites:

[1.pre] A method for fabricating metal gate transistor, comprising:

[1.1] providing a substrate having a first transistor region and a second transistor region;

[1.2] forming a plurality of dummy gates on the substrate and within the first transistor region and the second transistor region;

[1.3] forming a source/drain region at two sides of each dummy gate;

[1.4] forming a dielectric layer to cover the dummy gates;

[1.5] removing the dummy gates to form a plurality of openings in the dielectric layer of the first transistor region and the second transistor region;

[1.6] ***forming a high-k dielectric layer to cover the dielectric layer and surface of each opening;***

[1.7] ***depositing a first cap layer on the high-k dielectric layer;***

[1.8] *removing the first cap layer disposed in the second transistor region; and*

[1.9] *forming a metal layer on the first cap layer of the first transistor region and the high-k dielectric layer of the second transistor region.*

EX1001, claim 1 (annotated to identify claim elements).

VII. THE PETITION GROUNDS AND ASSERTED ART

61. The Petition asserts the following grounds challenging claims 1-11 of the '195 Patent:

Ground	Challenged Claims	Statutory Basis	Prior Art
1A	1, 2, 4, 7-11	§102/§103	Bohr (TSMC-1004)
1B	3	§103	Bohr in view of Chen (TSMC-1009)
1C	5	§103	Bohr in view of Yu (TSMC-1008)
1D	6	§103	Bohr in view of Yu and Chen
1E	7	§103	Bohr in view of Lee (TSMC-1010)
1F	9, 11	§103	Bohr in view of Wang (TSMC-1006) or Amazawa (TSMC-1007)
2A	1, 2, 4, 7-11	§102/§103	Brask (TSMC-1005)

Ground	Challenged Claims	Statutory Basis	Prior Art
2B	1, 2, 4, 7-11	§103	Brask in view of Ma (TSMC-1012)
2C	3	§103	Brask in view of Chen
2D	5	§103	Brask in view of Yu
2E	6	§103	Brask in view of Yu and Chen

Pet., 1-2.

A. Bohr (Grounds 1A-F)

62. Grounds 1A-F rely solely or primarily on the Bohr reference. Bohr describes a semiconductor fabrication method involving replacing dummy gates with metal gates. For example, Bohr's Figs. 1-3 illustrate the formation and subsequent removal of dummy gates to form trenches, which will eventually be filled by a metal gate structure:

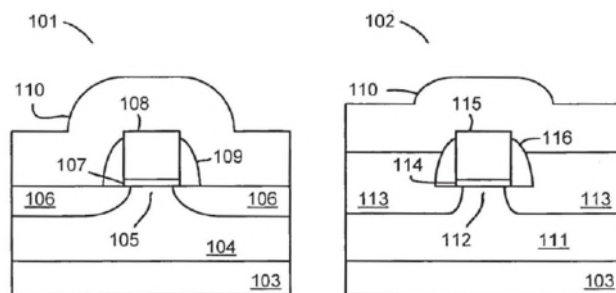


FIG. 1

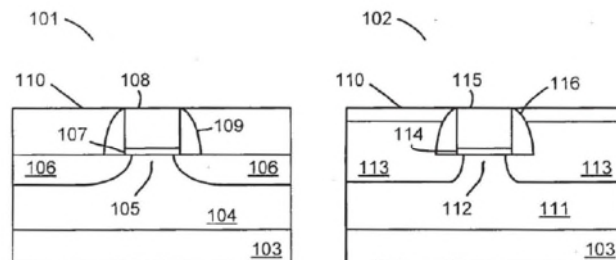


FIG. 2

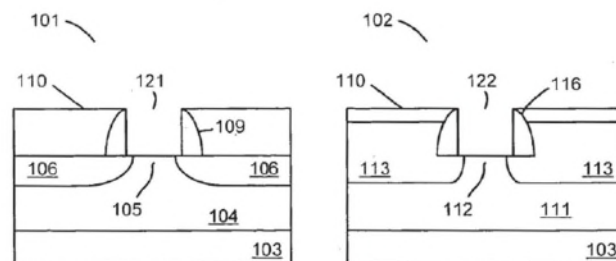


FIG. 3

EX1004-Bohr, Figs. 1-3.

63. “As illustrated in FIG. 4, a gate dielectric 131 may be formed in trenches 121, 122”:

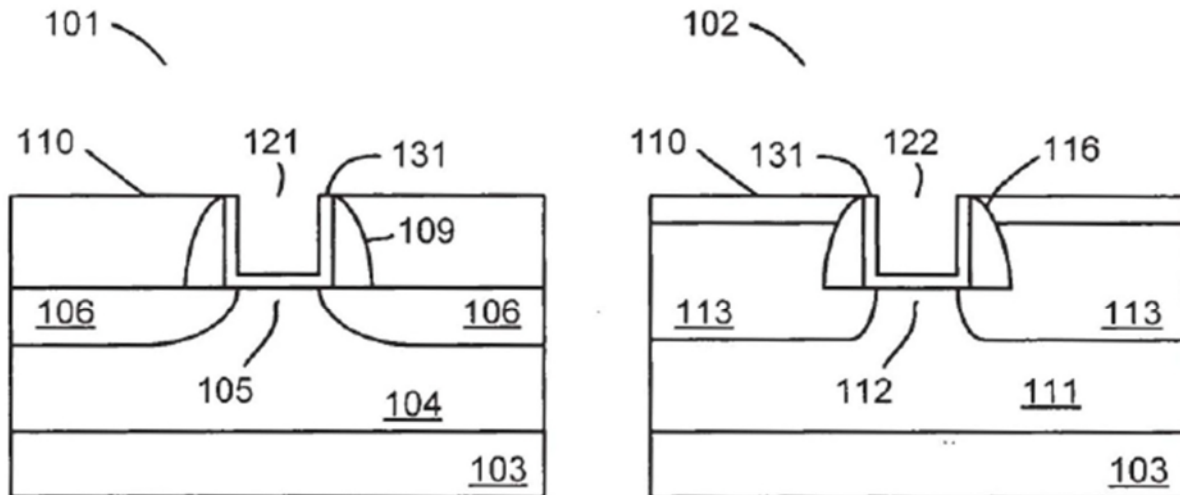


FIG. 4

EX1004-Bohr, ¶[0038], Fig. 4.

64. Unlike the '195 Patent's high-k dielectric layer, Bohr's gate dielectric 131 is formed only in the trenches, rather than also covering the inter-layer dielectric layer.

65. The Petition relies on Bohr's Figures 6-8 embodiment as allegedly disclosing the claimed "cap layer" and "metal layer" steps. Pet., 20-23. Bohr explains that "FIGS. 6-8 illustrate a method for forming gate electrodes with reference to the illustration of FIG. 4." EX1004-Bohr, ¶[0045]. "As illustrated in FIG. 6, an n-type material 161 may be formed in trenches 121, 122."

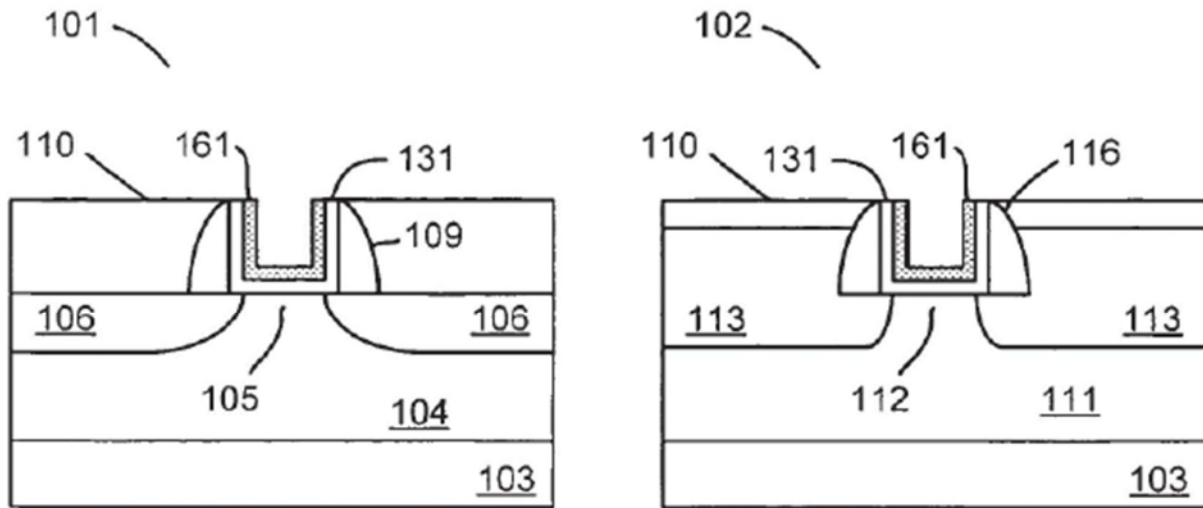


FIG. 6

Id., ¶[0045], Fig. 6.

66. “N-type material 161 may be any suitable n-type work function material,” including “hafnium, zirconium, titanium, tantalum, aluminum, their alloys, or carbides of those metals.” *Id.*, ¶¶[0040], [0044]. That is, n-type material 161 is a conductive n-type metal layer with a specific work function suitable for an n-type (or NMOS) gate.

67. Then, “[a]s illustrated in FIG. 7, n-type material 161 may be selectively removed from PMOS transistor 102 and a p-type material 162 may be formed.”

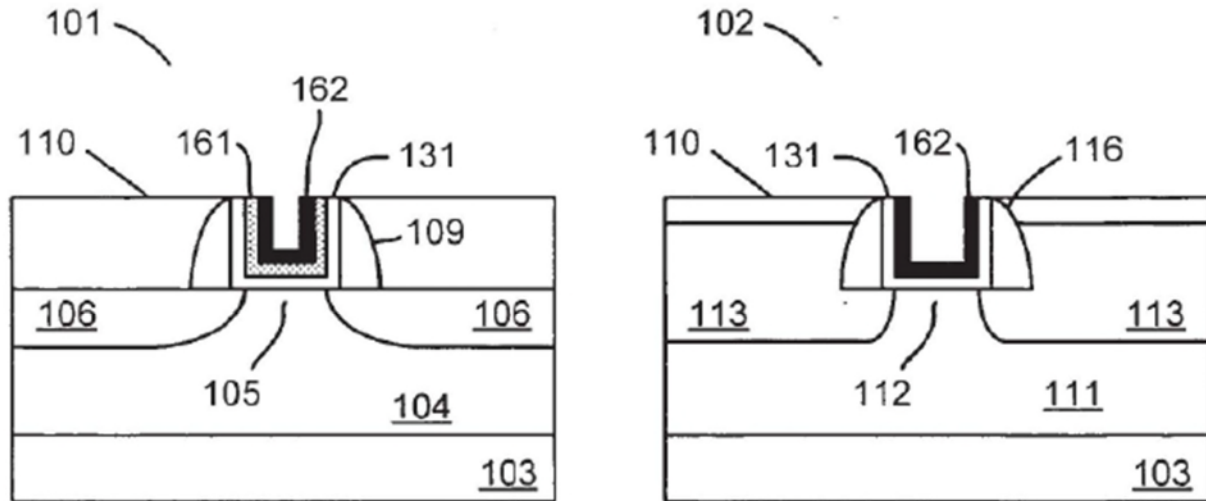


FIG. 7

EX1004-Bohr, ¶[0046], Fig. 7.

68. “P-type material 162 may be any suitable p-type work function material,” including “ruthenium, palladium, platinum, cobalt, nickel, and their oxides.” *Id.*, ¶¶[0042], [0046]. Thus, p-type material 162 is a conductive p-type metal layer with a specific work function suitable for a p-type (or PMOS) gate.

69. Therefore, unlike in the '195 Patent, Bohr's fabrication method employs two metal layers with specific work functions, rather than a cap layer and a metal layer. In contrast, the '195 Patent's cap layer is an insulating oxide layer that “define[s] the work function of n-type metal,” rather than the cap layer itself being the n-type metal. EX1001, 4:47-50.

B. Brask (Grounds 2A-E)

70. Grounds 2A-E rely solely or primarily on the Brask reference. Brask discloses a semiconductor fabrication method similar to Bohr's. For example, Brask's Figs. 1a and 1b illustrate the formation and subsequent removal of dummy gates to form trenches, which will eventually be filled by a metal gate structure:

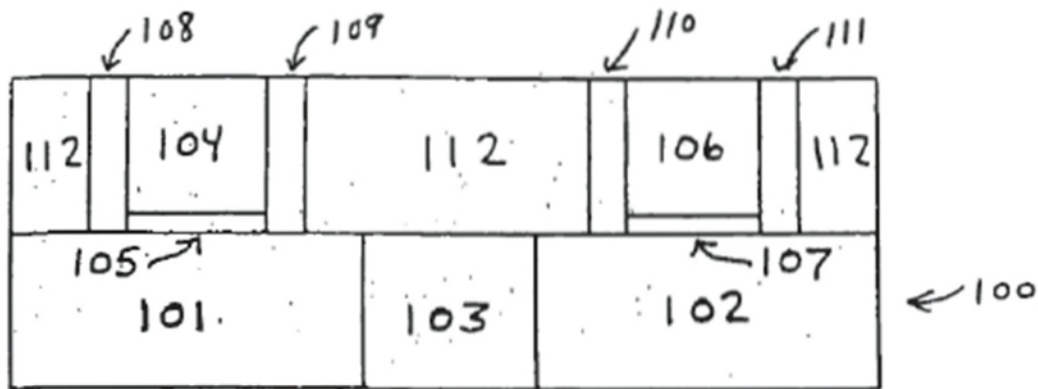


Figure 1a

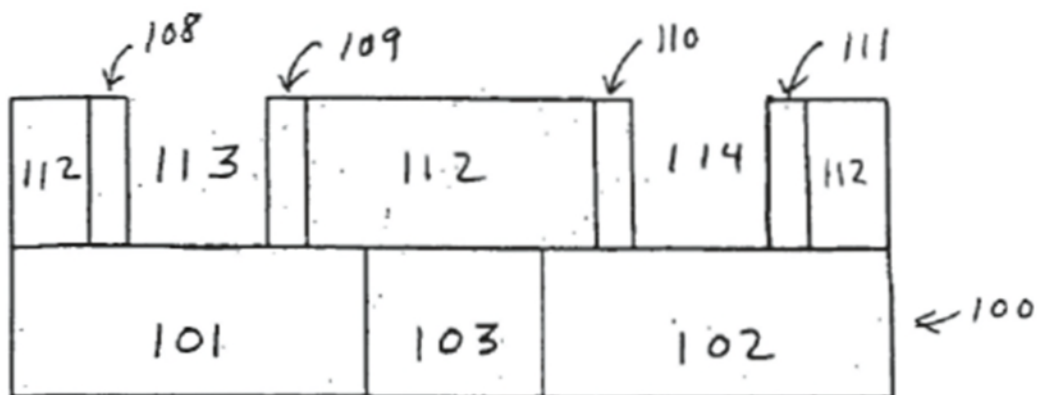
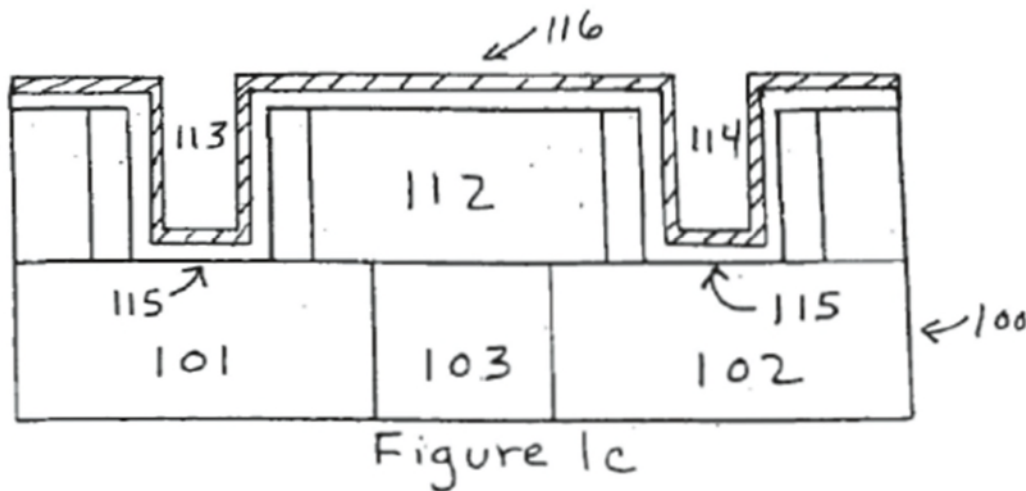


Figure 1b

EX1005-Brask, Figs. 1a and 1b.

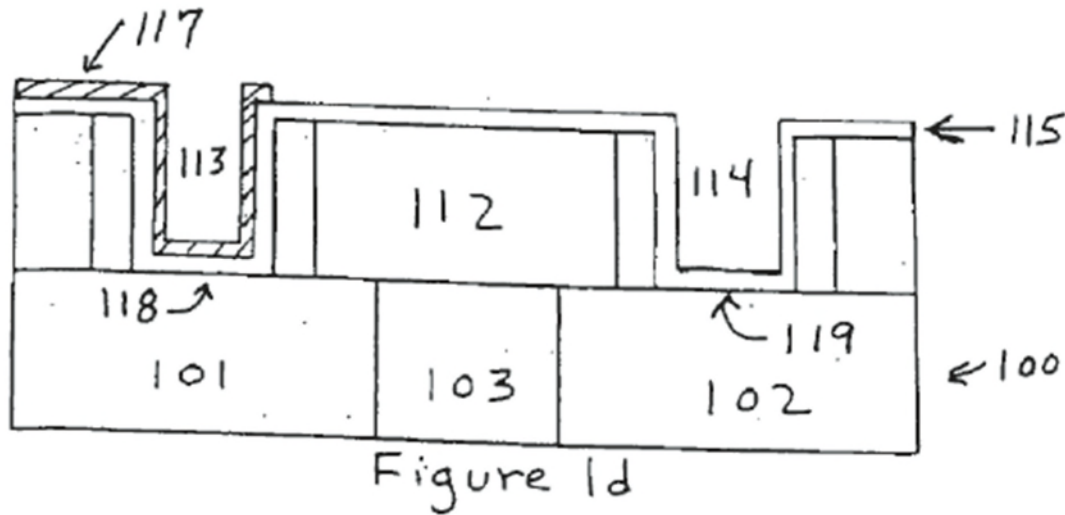
71. Then, as shown in Fig. 1c, a high-k gate dielectric layer 115 and metal layer 116 are formed:



EX1005-Brask, ¶¶[0026]-[0032], Fig. 1c.

72. “Metal layer 116 may comprise any conductive material from which a metal gate electrode may be derived.” *Id.*, ¶[0031]. “Examples of n-type materials that may be used to form metal layer 116 include: hafnium, zirconium, titanium, tantalum, aluminum, and metal carbides that include these elements.” *Id.* “When metal layer 116 comprises an n-type material, layer 116 preferably has a workfunction that is between about 3.9 eV and about 4.2 eV.” *Id.*, ¶[0032]. That is, metal layer 116 is a conductive metal layer with a specific work function.

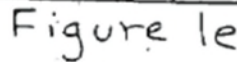
73. “After forming metal layer 116 on high-k gate dielectric layer 115, part of metal layer 116 is masked. The exposed part of metal layer 116 is then removed, followed by removing any masking material to generate the structure of Fig. 1d.”



EX1005-Brask, ¶[0033], Fig. 1d.

74. “In that structure, first metal layer 117 is formed on first part 118 of high-k gate dielectric layer 115, such that first metal layer 117 covers first part 118 of high-k gate dielectric layer 115, but does not cover second part 119 of high-k gate dielectric layer 115.” *Id.*, ¶[0033].

75. Then, “second metal layer 120 is then deposited on first metal layer 117 and exposed second part 119 of high-k gate dielectric layer 115 generating the structure illustrated by FIG. 1e.”



EX1005-Brask, ¶[0034], Fig. 1e.

76. “If first metal layer 117 comprises an n-type metal, e.g., one of the n-type metals identified above, then second metal layer 120 preferably comprises a p-type metal.” *Id.*, ¶[0034]. Thus, second metal layer 120 is a conductive p-type metal layer with a specific work function suitable for a p-type (or PMOS) gate.

77. Like Bohr, Brask's fabrication method employs two metal layers with specific work functions, rather than a cap layer and a metal layer. In fact, Brask specifically states that its "metal layer 116" is not a "capping layer." EX1005-Brask, ¶[0031] ("Although in some embodiments it may be desirable to form a capping layer on high-k gate dielectric layer 115, in the illustrated embodiment, metal layer 116 is formed directly on layer 115 to generate the FIG. 1c structure.").

VIII. ANALYSIS OF THE PETITION GROUNDS

A. Bohr Does Not Disclose Or Render Obvious The Claimed “First Cap Layer” (Elements [1.7] And [1.8])

78. The Petition alleges that “Bohr’s n-type material 161 corresponds to the claimed first cap layer.” Pet., 20. I disagree. Bohr explains that “[n]-type material 161 may be any suitable n-type work function material,” including “hafnium, zirconium, titanium, tantalum, aluminum, their alloys, or carbides of those metals.” EX1004-Bohr, ¶¶[0040], [0044]. That is, n-type material 161 is a conductive n-type metal layer with a specific work function suitable for an n-type (or NMOS) gate. In other words, Bohr’s n-type material 161 is a part of the gate electrode itself, rather than being an insulating oxide layer. See EX1004-Bohr, ¶[0045] (“FIGS. 6-8 illustrate a method for forming gate electrodes.”). In contrast, the ’195 Patent’s “cap layer” is an insulating oxide layer, rather than a conductive metal layer. For example, the ’195 Patent explains that “the cap layer 56 comprises La_2O_3 , MgO , Dy_2O_3 , or other lanthanide oxides.” EX1001, 4:26-27.

79. Moreover, in the ’195 Patent, “the present invention specifically uses the cap layer 56 to define the work function of the metal layer 60.” EX1001, 4:43-46. For example, “[i]n the aforementioned embodiment, a cap layer 56 composed of La_2O_3 is deposited before the formation of the metal layer 60 to define the work function of n-type metal.” *Id.*, 4:47-50. That is, the cap layer is an insulating oxide layer that defines the work function of the n-type gate metal, rather than being an n-

type metal itself. Conversely, Bohr's n-type material is made from an "n-type work function material"—that is, Bohr's n-type material is the n-type metal layer itself, rather than defining the work function of the n-type metal. EX1004-Bohr, ¶[0045].

80. The Petition alleges that "Patent Owner acknowledge[d] during prosecution of the '195 patent that a cap metal layer 'may be construed as the first cap layer of the present invention.'" Pet., 21 (citing EX1002, 88-89). I disagree. The portion of the file history that the Petition cites to (pages 88-89) is an Office Action Response. The relevant passage is in response to a rejection based on the Doczy reference (EX1024), which discloses a "cap metal layer 115." EX1024-Doczy939, ¶[0020]. In the Office Action Response, Applicant wrote: "Despite this cap layer 115a/115 may be construed as the first cap layer of the present invention, the cap layer 115a/115 is not removed from the second transistor region 202 and there is no metal layer formed on the cap layer 115a/115 of the first transistor region thereafter, as recited in claim 1 of the present invention." EX1002, 88-89. I understand this passage as Applicant arguing that *even if* Doczy's cap metal layer 115 could be construed as a "cap layer," it still did not meet other requirements of the claimed cap layer. The Petition apparently interprets this sentence as conceding that any metal layer can be a cap layer. I disagree that Applicant made such a concession.

81. In fact, the Doczy reference actually confirms that an n-type metal layer (such as Bohr's n-type material 161) is **not** a cap layer. In Doczy, the "cap metal layer 115" is a "capping layer" because it is the top/final layer of the gate. EX1024-Doczy939, ¶[0019].

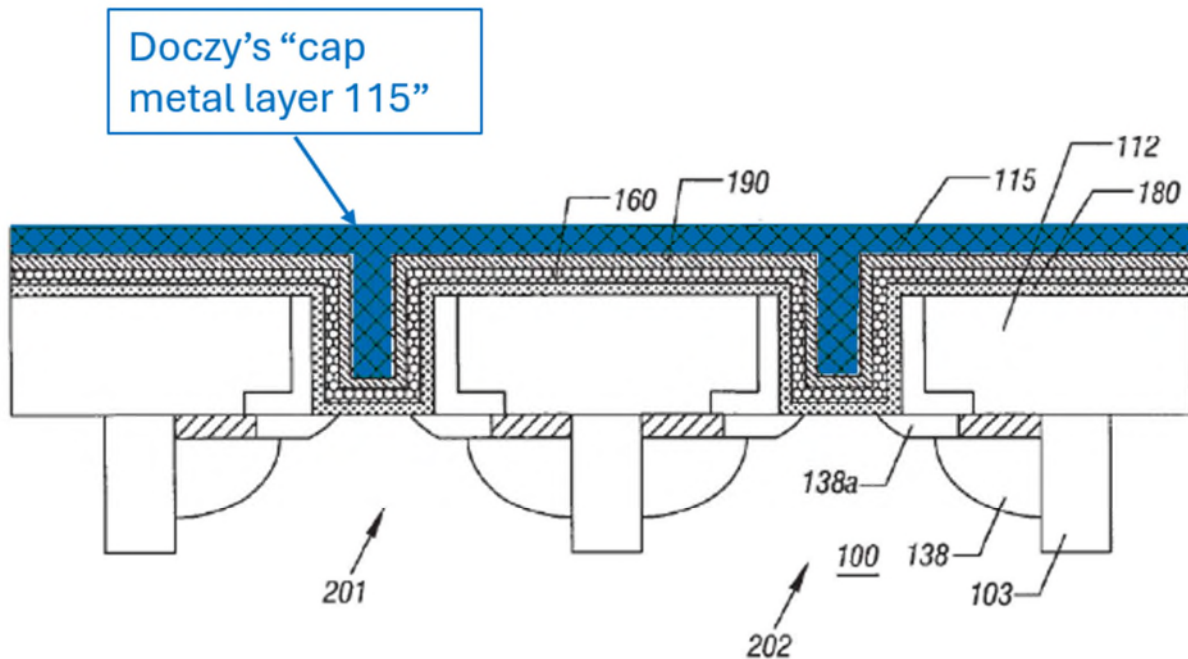


FIG. 10

Id., Fig. 10 (annotated).

82. Doczy explains that "after formation of the [n-type metal] layer 190, a contact/gap fill can be implemented by applying a bottom up superconformed filling (superfill), indicated as 115a." *Id.*, ¶[0048]. This corresponds to the '195 Patent's "conductive layer 62," which fills in the gate:

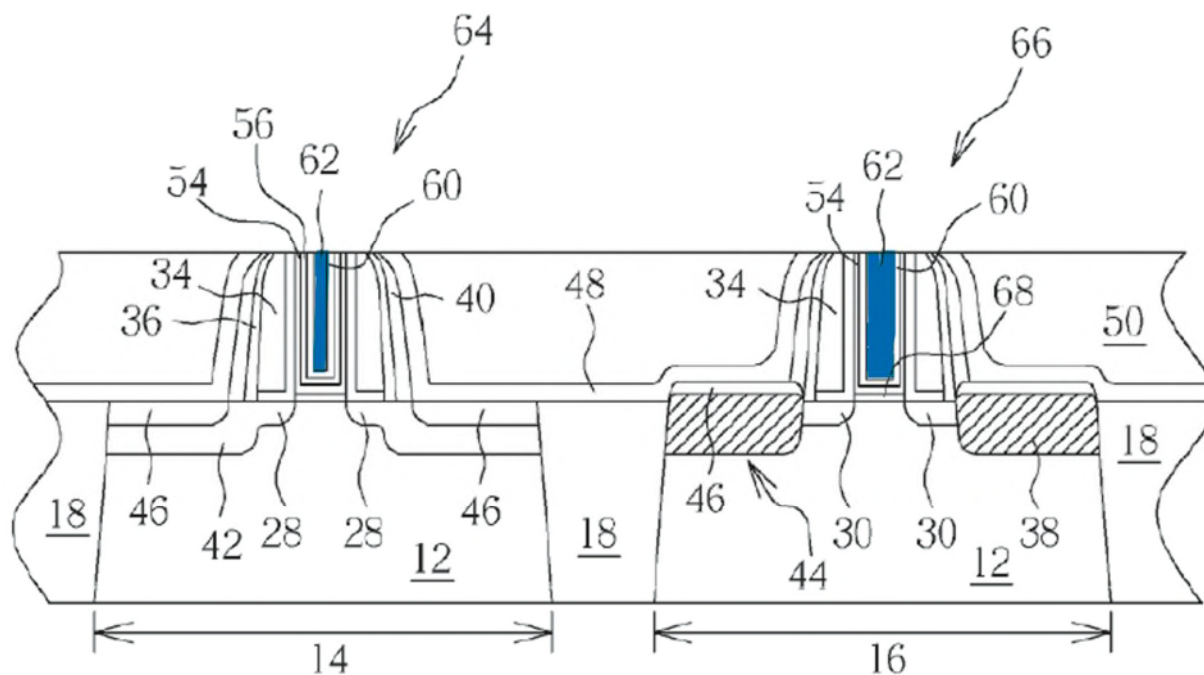


FIG. 8

EX1001, Fig. 8 (annotated).

83. Doczy's cap metal layer 115 is formed on top of "n-type metal layer 190." EX1024-Doczy939, ¶¶[0011]-[0012], [0048].

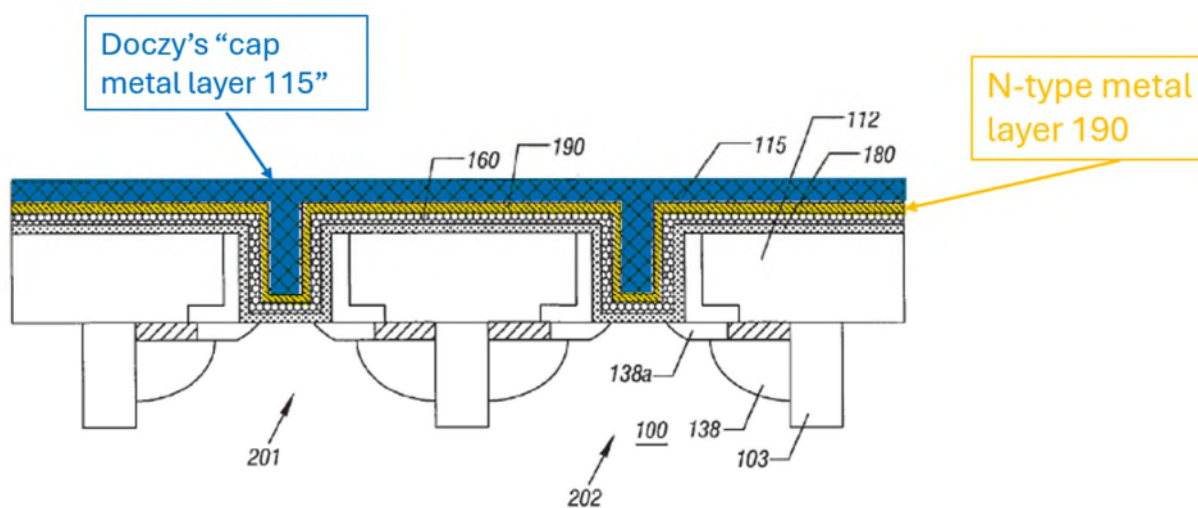


FIG. 10

Id., Fig. 10 (annotated).

84. “N-type metal layer 190 may serve as a metal NMOS gate electrode that, in one embodiment, has a workfunction that is between about 3.9 eV and about 4.2 eV.” *Id.*, ¶[0012].

85. Thus, Bohr’s “n-type material 161”—which the Petition alleges is the claimed “first cap layer”—does not correspond to Doczy’s “cap metal layer.” Rather, Bohr’s “n-type material 161” corresponds to Doczy’s “n-type metal layer 190,” which is not a cap layer and is distinguished from the cap metal layer. Thus, even if Doczy’s “cap metal layer” could be said to be construed as the claimed “first cap layer,” Bohr’s “n-type material 161” cannot.

86. Bohr’s “n-type material 161” is not the claimed “first cap layer” because it is a conductive metal layer that forms part of the gate electrode itself, rather than being an insulating cap oxide that defines the work function of the metal layer.

B. Brask Does Not Disclose Or Render Obvious The Claimed “First Cap Layer” (Elements [1.7] And [1.8])

87. The Petition alleges that Brask’s “metal layer 116” is the claimed “first cap layer” of the challenged claims. Pet., 59. Not so. Brask explains that “[m]etal layer 116 may comprise any conductive material from which a metal gate electrode may be derived.” EX1005-Brask, ¶[0031]. “Examples of n-type materials that may be used to form metal layer 116 include: hafnium, zirconium, titanium, tantalum,

aluminum, and metal carbides that include these elements.” *Id.* “When metal layer 116 comprises an n-type material, layer 116 preferably has a workfunction that is between about 3.9 eV and about 4.2 eV.” *Id.*, ¶[0032]. That is, metal layer 116 is a conductive metal layer with a specific work function that forms a part of the gate electrode. Thus, like Bohr’s n-type material 161, Brask’s metal layer 116 is a part of the gate electrode itself, rather than being an insulating oxide layer. In contrast, the ’195 Patent’s “cap layer” is an insulating oxide layer, rather than a conductive metal layer. For example, the ’195 Patent explains that “the cap layer 56 comprises La_2O_3 , MgO , Dy_2O_3 , or other lanthanide oxides.” EX1001, 4:26-27.

88. Moreover, in the ’195 Patent, “the present invention specifically uses the cap layer 56 to define the work function of the metal layer 60.” EX1001, 4:43-46. For example, “[i]n the aforementioned embodiment, a cap layer 56 composed of La_2O_3 is deposited before the formation of the metal layer 60 to define the work function of n-type metal.” *Id.*, 4:47-50. That is, the cap layer is an insulating oxide layer that defines the work function of the n-type gate metal, rather than being an n-type metal itself. Conversely, Brask’s metal layer 116 is made from an “n-type material”—that is, Brask’s metal layer 116 is the n-type metal layer itself, rather than defining the work function of the n-type metal. EX1005-Brask, ¶[0031]. In fact, Brask specifically states that its “metal layer 116” is not a “capping layer.” EX1005-Brask, ¶[0031] (“Although in some embodiments it may be desirable to

form a capping layer on high-k gate dielectric layer 115, in the illustrated embodiment, metal layer 116 is formed directly on layer 115 to generate the FIG. 1c structure.”).¹

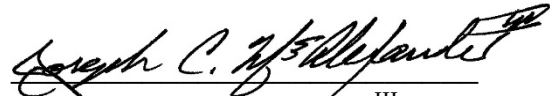
89. The Petition again alleges that “Patent Owner stated during prosecution [] that a cap metal layer ‘may be construed as the first cap layer of the present invention.’” Pet., 60 (citing EX1002, 88-89). As explained above, I disagree. Moreover, as explained above, the Doczy reference actually confirms that an n-type metal layer (such as Brask’s metal layer 116) is **not** a cap layer. In fact, Doczy’s description of its “n-type metal layer 190”—which is not a cap layer and is distinguished from its “cap metal layer”—is nearly identical to Brask’s description of its metal layer 116. *Compare* EX1024-Doczy939, ¶[0012] (“N-type metal layer 190 may serve as a metal NMOS gate electrode that, in one embodiment, has a workfunction that is between about 3.9 eV and about 4.2 eV.”) *with* EX1005-Brask,

¹ Although this passage of Brask discloses forming a capping layer on a high-k gate dielectric layer, Brask does not disclose that the capping layer is removed in either of the transistor regions, as required by element [1.8]. That is likely why Petitioner instead elected to try to shoehorn Brask’s “metal layer 116” as the alleged “first cap layer.”

¶[0032] (“When metal layer 116 comprises an n-type material, layer 116 preferably has a workfunction that is between about 3.9 eV and about 4.2 eV.”).

90. Brask’s “metal layer 116” is not the claimed “first cap layer” because it is a conductive metal layer that forms part of the gate electrode itself, rather than being an insulating cap oxide that defines the work function of the metal layer.

Dated: May 26, 2026


Joseph C. McAlexander III