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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		90019255
	Filing Date		2023-09-20
	First Named Inventor	Madhukar Reddy	
	Art Unit	3992	
	Examiner Name	LIE, ANGELA M	
	Attorney Docket Number	189005.TR003	

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	1	9210326	B2	2015-12-08	AKIRA MIYATA	
	2	5535240	A	1996-07-09	RONALD R. CARNEY et al.	
	3	6906498	B2	2005-06-14	GEORG BREUCH et al.	
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	7	7496158	B2	2009-02-24	GERALD L. FUDGE et al.	
	8	7421259	B2	2008-09-02	RAMON A. GOMEZ et al.	

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	9	7373125	B2	2008-05-13	NIHAL GODAMBE et al.	
	10	5280636	A	1994-01-18	EDWIN A. KELLEY et al.	
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	19	8374569	B2	2013-02-12	KISHORE SEENDRIPU et al.	

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	20	8374568	B2	2013-02-12	KISHORE SEENDRIPU et al.	
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	23	7027520	B2	2006-04-11	MICHAEL ANTHONY PUGEL	
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32	7783958	B1	2010-08-24	DONALD BRIAN EIDSON et al.	

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	3	20070081617	A1	2007-04-12	GERALD FUDGE	
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10	20080261638	A1	2008-10-23	SAMI R. WAHAB et al.	
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	19	20060029170	A1	2006-02-09	HENRIK T. JENSEN et al.	
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	1	2006119489	WO	A2	2006-11-09	DAVID LOWELL MCNEELY		☒
	2	2006119490	WO	A2	2006-11-09	DAVID LOWELL MCNEELY		☒
	3	2087623	EP	A2	2009-08-12	RF MAGIC INC		☒
	4	0696854	EP	A1	1996-02-14	WERNER BOIE		☐
	5	2007145637	WO	A1	2007-12-21	MICHAEL ANTHONY PUGEL		☐
	6	2006118722	WO	A1	2006-11-09	DAVID EMERY VIRAG et al.		☐

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1	JEFFREY A. WELDON, et al. "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers," IEEE Journal of Solid-State Circuits, December 2001, pages: 2003-2015, Vol. 36, No. 12, Seattle, WA, USA.	☐
2	FRANCESCO GATTA, et al. "An embedded 65nm CMOS low-IF 48 MHz to 1 GHz dual tuner for DOCSIS 3.0," 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, Feb. 12, 2009, pages: 122-123, San Francisco, CA, USA.	☐
3	System Art - Broadcom BCM 3380 Broadcom Jun. 10, 2008	☐
4	Silicon-based RF front-ends for ultra wideband radios UWB textbook Jan. 2008	☐
5	System Art - Motorola SURFboard cable modem SB6120 Motorola / Arris 2007	☐
6	MIRABBASI and K. MARTIN, "Classical and Modern Receiver Architectures," IEEE Communications Magazine, vol. 38, no. 11, pp. 132-139, November 2000	☐
7	JAN M RABAEY, "Digital Integrated Circuits: A Design Perspective" Pearson, 2nd ed. 2002	☐
8	J. CROLS and M. S. J. STEYAERT, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, March 1998	☐
9	A. P. CHANDRAKASAN, "Ultra low power digital signal processing," Proceedings of 9th International Conference on VLSI Design, Bangalore, India, 1996, pp. 352-357	☐

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Examiner Signature	/ANGELA M LIE/	Date Considered	07/31/2024
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Hao Tan/	Date (YYYY-MM-DD)	2024-06-18
Name/Print	Hao Tan	Registration Number	73,711

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