

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,

Petitioner,

v.

HEADWATER RESEARCH LLC,

Patent Owner

IPR2026-00271

Patent No. 9,491,564

**DECLARATION OF DR. MICHAEL C. BROGIOLI IN SUPPORT OF
PATENT OWNER'S RESPONSE**

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I, Michael C. Brogioli, PhD, hereby declare as follows:

I. INTRODUCTION

1. I am over the age of eighteen (18) years and otherwise competent to make this declaration.

2. I have been retained as an expert witness on behalf of Headwater Research LLC (“Headwater”) for the above-captioned *inter partes* review (“IPR”). I understand that the petition for *inter partes* review involves U.S. Patent No. 9,491,564 (“the ’564 patent”).

3. I make this declaration based on my personal knowledge, educational background and training, consideration of the materials I discuss herein, and my expert opinions.

4. I am being compensated at a rate of \$750 per hour for my time in this matter. My compensation does not depend on the outcome of this proceeding, and I have no financial interest in its outcome.

5. In preparing this Declaration, I have reviewed and considered the ’564 patent, the ’564 patent’s prosecution history, the Petition, Dr. Traynor’s declaration submitted in this proceeding, and each document cited in my declaration.

II. BACKGROUND AND QUALIFICATIONS

6. My qualifications for forming the opinions given in this declaration are summarized here and in Ex. 2007. That exhibit also includes a list of my publications.

7. I am currently an Adjunct Professor of Electrical and Computer Engineering at Rice University in Houston, TX, teaching Ph.D. candidate level courses in wireless telecommunications, embedded computing software, embedded computing hardware, and software/hardware design. I have held this position since July 2009. I am also currently the Managing Director of Polymathic Consulting in Austin, TX, a company that advises a variety of clients on engineering, research and development, intellectual property, and other technical leadership matters, and I have held this position since October 2011.

8. I am a named inventor on multiple issued and pending patent applications. The subject matter of these applications includes, but is not limited to, embedded processing, edge computing, and various aspects of distributed systems including computation, interconnectivity and hardware/software design and implementation.

9. From November 2009 to October 2011, I was Chief Architect, Senior Member Technical Staff at Freescale Semiconductor in Austin, TX (formerly Motorola), responsible for management of technology, engineering roadmaps,

design lead on compiler infrastructure and optimizations for mobile and embedded computing solutions, including the types of security and encryption technologies involved in this matter. From 2007 to 2009, I was a Senior Engineer working with high performance compiler design and next generation baseband compiler design and next generation baseband microprocessor and microcontroller architecture at Freescale Semiconductor in Austin, Texas, including regarding communications networks and how mobile device architecture and design interacts with network elements.

10. From June 2006 to August 2007, I worked as the Technical Co-Founder of Method Seven LLC, in Boston, MA, working with high performance software and hardware systems architecture. I am currently the co-founder, co-inventor, and Chief Technology Officer of Network Native, an Internet of Things hardware and software company. I have also served on multiple advisory boards for technology companies over the past 10+ years.

11. While at Rice University, I developed various computer architecture designs. For example, from 2002 to 2004, I developed Spinach, a simulator design toolset for modeling programmable network interface architectures, which models system components common to all programmable computing environments as well as components relating to embedded computing, wireless and mobile devices. From 2004 to 2009, I developed Spinach DSP-FPGA, a modular and composable

simulator design infrastructure for programmable and reconfigurable embedded SOC architectures specifically targeting mobile, embedded and portable computing devices. From 2005 to 2009, I developed and published a retargetable compiler infrastructure for software and systems related to mobile and embedded computing technologies. Many of these tools have been used at U.S. universities in the area of electrical and computer engineering research.

12. I am recognized as an expert in the field of communications systems, including computer architecture, hardware, and software as they relate to the subject matter at hand. I am a member of the Institute of Electrical and Electronics Engineers (IEEE). I have previously held the role of Program Chair of Design Automation Conference in the areas of Embedded and Wireless Solutions. I have been a Program Committee member for the IEEE and ACM Design Automation Conference from 2011 to the present, as well as other IEEE and ACM conferences. I have published, co-published and contributed to numerous works on wireless and mobile computing, digital networking, Internet of Things technology, software and hardware optimizations, and digital signal processing and related architectures among other topics.

13. I have previously served as an engineering consultant and testifying witness on matters related to, and including Internet and communications technologies such as those at hand in this matter. This experience is encompassed

in my work in academia and as a faculty member, my time in industry as a system designer and architect, as well as my work as an engineering consultant and expert witness over the past 20+ years.

14. Over the past 20+ years, I have authored numerous peer reviewed publications in the area of embedded and high performance computing, interconnect technologies, computer networking at the server and mobile handset level, and optimization at the hardware and software design level. I have also been a committee member, and chair of Design Automation Conference in areas of technology related to the '564 Patent, often reviewing and vetting submissions from major industry players often related to technologies at issue in this matter.

15. During my tenure at Freescale Semiconductor, I was in charge of system developer tools for baseband processor design, both in the hardware and software spaces. This work included hardware and software design issues of next generation wireless networking equipment, including system level programming models, interconnect technology, heterogeneous computing, various hardware acceleration technologies and related components.

16. My current curriculum vitae, provided in Exhibit 2007, contains more information on my background and experience, as well as the cases in which I have served as an expert witness over the past four years.

17. No part of my compensation is contingent upon the outcome of this litigation. I have no other interests in this litigation or with any of the parties.

III. LEGAL PRINCIPLES

A. Claim construction

18. I understand that the first step in performing a validity analysis of the patent claims is to interpret the meaning and scope of the claims by construing the terms and phrases found in those claims. I understand that the appropriate construction of a claim term is its ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent.

19. I understand that standard for claim construction in an *inter partes* review is the same standard as is applied in district court proceedings.

20. I understand that a determination of the meaning and scope of the claims is a matter of law. I have been informed that to determine the meaning of the claims, one should consider the intrinsic evidence, which includes the patent's claims, written description, and prosecution history.

B. Burden of Proof

21. I understand that in an *inter partes* review, the petitioner has the burden of proving unpatentability by a preponderance of the evidence. I further understand that for an *inter partes* review to be instituted, the petitioner must show

a reasonable likelihood that the petitioner would prevail with respect to at least one of the claims challenged in the petition.

C. Anticipation

22. I have been instructed by counsel and understand that a reference is anticipated if a single prior art reference discloses each and every claim element, either explicitly or inherently, as arranged in the same way as in the claim. I understand that where even one claim element is not disclosed in a reference, a contention of anticipation fails.

23. I further understand that when a reference fails to explicitly disclose a claim element, that reference inherently discloses that element only if the reference must *necessarily* include the undisclosed claim element.

D. Obviousness

24. I have been instructed by counsel and understand that a combination of prior art references may render a claim obvious if, at the time of the invention, a person of ordinary skill in the art would have selected and combined those prior-art elements in the normal course of research and development to yield the claimed invention.

25. I understand that in an obviousness analysis, one should consider the *Graham* factors: the scope and content of the prior art; the differences between the claimed inventions and the prior art; the level of ordinary skill in the art; and

certain secondary considerations, identified below. I further understand the obviousness analysis is to be performed on a claim-by-claim basis. I understand that a person of ordinary skill in the art is a person of ordinary creativity, not an automaton.

26. I have been instructed by counsel and understand that obviousness requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination. I understand obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have been *motivated* to combine those references in a manner that would include all limitations of the challenged claim, and, in making that combination, a person of ordinary skill in the art would have had a *reasonable expectation of success*.

27. I also understand that an obviousness analysis must be conducted with awareness of the distortion caused by hindsight bias and with caution of arguments reliant upon *ex post* reasoning. For instance, I understand that when considering obviousness, I should put myself in the position of a person of ordinary skill in the field at the time of the invention, rather than considering new information that is known today but was not known before the priority date of the challenged patent.

28. In particular, I understand that it is improper to use the challenged patent's disclosure or invention as a roadmap to find its prior-art components,

because such an approach discounts the value of combining various existing features or principles in a new way to achieve a new result.

IV. PERSON OF ORDINARY SKILL IN THE ART

29. Dr. Traynor states that a person of ordinary skill in the art (“POSITA”) relevant to the ’564 patent “would have had (1) at least a bachelor’s degree in computer science, electrical engineering, or a related field, and (2) 3–5 years of experience in services and application implementation in communication networks,” and that “More education could substitute for experience, and vice versa.” Ex. 1003, ¶¶30–33.

30. For purposes of this declaration, I do not dispute Dr. Traynor’s proposed level of ordinary skill in the art. My opinions set forth below would be the same under that definition.

31. I am a person of at least ordinary skill in the art, and was such a person as of the priority date of the ’564 patent. Unless I state otherwise, the opinions I express below reflect the understanding of a POSITA as of that priority date.

V. CLAIM CONSTRUCTION

32. Dr. Traynor does not propose that any claim terms be construed. For each claim limitation at issue, I apply the plain and ordinary meaning that the term

would have had to a POSITA as of the priority date of the '564 patent, read in light of the specification.

VI. OVERVIEW OF THE '564 PATENT

33. The '564 patent is directed to techniques for securing inter-process communications on a mobile end-user device. In the architecture described and claimed, the mobile device includes “an inter-process software communication (IPC) bus that provides secure communication between a device link agent and software component processes.” Ex. 1001, Abstract. A “device link object maintains a secure message link to a message link server that receives messages from plural network functions, identified for delivery to respective software components on the mobile device, and conveys them to the device link agent.” *Id.* The device link agent, in turn, delivers those received messages to the processes of the authorized software components. *Id.*

34. An important feature of the invention is a server-controlled restriction on which software components may access the bus to receive a given message. The “software processes are allowed to access the bus based on access authorization information from a secure server that identifies those components.” Ex. 1001, Abstract. Consistent with that design, the specification describes “agent level access authorization, which only allows access to the agents that are on the secure authorization list,” where “the list is provided by the secure server and signatures

are provided by the secure server.” *Id.*, 43:5–9. In this way, the bus is “secured, signed, encrypted, hidden, partitioned and/or otherwise protected from unauthorized monitoring or usage.” *Id.*, 42:28–30.

35. In my opinion, the protection the ’564 patent provides is not merely that messages are routed to the correct software component; the patent additionally teaches that software components not identified by the access authorization information are prevented from reading messages intended for the components that are identified by that information. The specification makes the point expressly, describing “a set of secure messages that can only be decoded or observed by the agents they are intended for.” Ex. 1001, 42:44–45. By confining who may “decode[]” or “observe[]”—that is, read—a message to the agents for which it is intended, the patent prevents components that are not the intended recipients from reading the message.

36. The independent claims capture this requirement in a limitation that is separate from, and additional to, the requirement of routing messages to identified components. Claims 1 and 14 require that the bus “provid[e] secure communication” by “allowing access to the bus only for software components identified by the access authorization information.” Ex. 1001, 167:11–19 (limitation [1B]); *id.*, 168:37–43 (limitation [14B]). Separately, the claims require that, “for software components identified by the access authorization information,”

the device link agent “route messages identified for delivery to a given one of those software components.” Id., 167:32–37 (limitation [1F]); id., 168:56–61 (limitation [14E]). In my opinion, the access-control limitation therefore is not satisfied by merely ensuring a message reaches its intended destination: it instead requires that access to the bus—and thus the ability to read the messages carried on it—be confined to the identified software components, so that components not identified by the access authorization information cannot access the bus to read messages intended for the identified components.

VII. DR. TRAYNOR FAILS TO SHOW THAT THE PRIOR ART RENDERS OBVIOUS “ALLOWING ACCESS TO THE BUS ONLY FOR SOFTWARE COMPONENTS IDENTIFIED BY THE ACCESS AUTHORIZATION INFORMATION”

37. I understand that Dr. Traynor opines that independent claims 1 and 14 are unpatentable on four grounds: Ground 1 based on TS-23.140 (which Dr. Traynor refers to as “MMS”) in view of Rakic, and Grounds 2A, 2B, and 2C based on that same combination further in view of Cole, Sathish, or both. I understand that no single reference is alleged, standing alone, to disclose “allowing access to the bus only for software components identified by the access authorization information,” and that Dr. Traynor relies only on the combination of TS-23.140 with Rakic to allegedly meet that limitation. In my opinion, for the reasons below, the combination Dr. Traynor describes would not meet that limitation, and Dr.

Traynor identifies no technical reason that a POSITA would have modified the references to meet it.

A. **The combination Dr. Traynor describes does not satisfy “allowing access to the bus only for software components identified by the access authorization information.”**

38. As I understand it, the only analysis Dr. Traynor offers for this limitation is that, in the combined MMS-Rakic system, the User Agent generates a key, signs the data block of a received message, compares the resulting signature to the message’s signature, and—“[i]f the signatures match”—routes the message to the identified destination application. Ex. 1003, ¶¶120–121. On that basis, Dr. Traynor opines that the combination “allow[s]” “access to the bus ... only for software components identified by the access authorization information.” Ex. 1003, ¶121.

39. I disagree. Dr. Traynor’s analysis describes conditionally transmitting a message over the bus—that is, conditioning whether the message is placed on the bus on the presence of a valid signature for the identified destination application. It does not describe allowing access to the bus only for the identified component. Conditioning transmission on a valid signature, at most, prevents transmission of a message when the identified software component is not present on the device; it does nothing to prevent other, unidentified software components connected to the bus from accessing the message once it is transmitted.

40. A simple example illustrates the point. Consider a bus (like Rakic’s “communication path 310” depicted in Rakic’s FIG. 3) to which several system components are connected—for instance, three applications A, B, and C, each with its own application identifier. Under Dr. Traynor’s theory, when a signature identifying application A is validated, the User Agent transmits the message intended for application A onto the bus. But the bus is also connected to applications B and C, and neither TS-23.140 nor Rakic discloses any mechanism that would prevent B and C from also reading the message intended for A. Dr. Traynor identifies no such mechanism.

41. This reflects how a bus typically operates. In my opinion, a POSITA would understand that a “bus” is a shared communication medium to which multiple components connect, and that, absent some additional, non-standard access-restriction mechanism, every component connected to a bus can read the data transmitted on it. That understanding is consistent with technical dictionaries. A “software bus” is described as a “programming interface that allows software modules to transfer data to each other,” with no suggestion that access is restricted among connected components. Ex. 1049 at 3. And the definition of “bus” from which that term derives states that “[a]ll signals on the bus go to all stations or devices connected to it.” Ex. 2008 at 4.

42. A POSITA would further understand that this is true even where a transmission is addressed to a particular recipient. For example, even when a “data packet ... contains the address of the destination station,” it “is broadcast to all nodes at the same time, and the recipient computer responds by accepting it.” Ex. 2008 at 4. In other words, addressing a message to a particular component does not restrict which components may access it; it merely identifies the intended recipient of a message that all connected components can read. None of TS-23.140, Rakic, or Dr. Traynor identify any mechanism that would restrict which connected components can read data transmitted over the bus.

43. The references confirm this. TS-23.140 does not describe any inter-process software communication bus; to the contrary, it states that “[d]etails of these applications or how an MMS User Agent or an MMS VAS Application would interface with them are outside the scope of this specification.” Ex. 1004, 54 (§ 7.1.18). TS-23.140 therefore discloses nothing about restricting which software components may access a bus, because any such details are explicitly stated as being outside the scope of that reference.

44. Rakic likewise discloses no such mechanism. Rakic is directed to validating a “secure push message” that a client device receives, and its signature techniques serve only to “verify that an intended recipient of the secure push message is the client device, and that the client device includes a correct

component.” Ex. 1007, [0041]. The only structure in Rakic that Dr. Traynor contends relates to a “bus” is a “communication path” 310, which “provide[s] an interface through which components of device 300 can communicate with one another.” Ex. 1007, [0058] (cited at Ex. 1003, ¶72); *id.*, FIG. 3. Consistent with the understanding above, Rakic’s communication path 310 connects numerous components, with no disclosure that any component would be prevented from reading a message transmitted over it. A POSITA would not understand that confirming that a message is destined for the correct device, and that the device includes the correct component, constitutes disallowing *other* components resident on that device from accessing the bus to read the message.

45. For these reasons, in my opinion, even if the prior art were combined exactly as Dr. Traynor describes, the combination would not “allow[] access to the bus only for software components identified by the access authorization information,” as limitations [1B] and [14B] require. Dr. Traynor’s contrary opinion (Ex. 1003, ¶¶120–121) describes a proposed signature-validation and routing mechanism but never explains why the resulting conditional transmission of a message would mean that access to the bus is allowed only for the identified components. In my opinion, it would not.

B. Dr. Traynor identifies no technical reason a POSITA would have arrived at the claimed access restriction.

46. Even setting aside that the combination Dr. Traynor describes would not meet limitations [1B] and [14B], I have seen no technical reason in Dr. Traynor's declaration that a POSITA would have found it obvious to modify the references to restrict access to the bus to only the identified software component. The motivations Dr. Traynor offers for combining TS-23.140 with Rakic are (1) to "implement the interface between TS-23.140's MMS User Agent application and the user device's other applications using a software bus for interprocess communications" (Ex. 1003, ¶74), and (2) to implement Rakic's "message signing and validation techniques" (Ex. 1003, ¶83). In my opinion, neither using a software bus nor applying Rakic's signing-and-validation techniques requires, or would lead a POSITA to implement, a mechanism that allows only the identified component to access the bus.

47. To the contrary, Rakic's techniques are directed to confirming that the client device "is the client device" and "includes a correct component." Ex. 1007, [0041]. Rakic says nothing about preventing components that are not the "correct component" from accessing a message on a bus, and I am aware of no evidence that a POSITA as of the priority date would have been motivated to restrict bus

access in the manner the claims require, or that any particular implementation achieving that result would have been obvious.

VIII. GROUNDS 2A, 2B, AND 2C DO NOT CURE THESE DEFICIENCIES

48. I understand that Grounds 2A, 2B, and 2C rely on the same TS-23.140–Rakic combination, further in view of Cole (Ground 2A), Sathish (Ground 2B), or both (Ground 2C). In my opinion, nothing in Dr. Traynor’s use of Cole or Sathish supplies the missing requirement of “allowing access to the bus only for software components identified by the access authorization information.”

49. Dr. Traynor relies on Cole only for its teaching of “a modem to enable communications over ... 2G/3G networks.” Ex. 1003, ¶¶196–197. That teaching has nothing to do with restricting access to a bus. And although Dr. Traynor relies on Sathish for its disclosure of a “D-Bus” used “to send information between applications” (Ex. 1003, ¶199), Dr. Traynor does not opine that Sathish’s D-Bus is configured—or would have been obviously configured—to “allow[] access to the bus only for software components identified by the access authorization information.” In my opinion, nothing in Sathish discloses or renders obvious that its D-Bus would restrict which connected components may read the information it carries.

50. Accordingly, in my opinion, none of Grounds 2A, 2B, or 2C cures the deficiency in Ground 1 as to limitations [1B] and [14B]. Because each ground that

challenges the independent claims relies on the same deficient theory regarding those limitations, the grounds that challenge only the dependent claims fail for at least the same reasons.

I declare under penalty of perjury that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

July 1, 2026



Michael C. Brogioli, Ph.D.