

Declaration of Dr. Stanley Shanfield
U.S. Patent No. 9,859,202

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.
Petitioner

v.

TOPWIRE LLC
Patent Owner

Case No. IPR2026-00303
U.S. Patent No. 9,859,202

**DECLARATION OF STANLEY SHANFIELD, PH.D.
ON BEHALF OF PETITIONER**

CLAIMS 1–9

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I, Stanley Shanfield, declare as follows.

Introduction

1. My name is Stanley Shanfield.
2. I received a B.S. Degree in Physics cum laude from University of California, Irvine in 1977. I received a Ph.D. in Physics from Massachusetts Institute of Technology in 1981.
3. After obtaining my Ph.D. in 1981, I was a Staff Scientist at Spire Corporation in Bedford, Massachusetts. From 1985–1999, I worked at Raytheon Corporation. As staff and later as section manager, among many other projects, I developed reactive ion etching (RIE) processes for patterning dielectrics (silicon dioxide, silicon nitride, silicon oxynitride, etc.), conductive layers (aluminum-copper, copper-silicon, W-silicide, TaN, doped polysilicon, etc.) and organic layers (photoresist, polyimide, etc.). In 1996, I became the Manager of Semiconductor Operations at Raytheon. As Manager, I built and led a 300-employee, \$60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. As part of my work at Raytheon Electronics in the 1990s, I provided the engineering support for an “old school” die packaging facility outside of Seoul, S. Korea. This facility packaged die produced in the U.S. using single chip plastic and sealed metal packages. The facility, under my direction, delivered some of the first encapsulated stacked-chip plastic

packages, and I was sometimes involved in hands-on work to resolve packaging issues that arose. In 1999, I was a co-founder and became Vice President of Operations at AXSUN Technologies in Bedford/Billerica, Massachusetts and later became Director of Manufacturing and Wafer Fab Technology. In 2003, I joined the Draper Laboratory in Cambridge, Massachusetts. Currently, I am the Division Leader of Advanced Hardware Development, with around 80 staff members; a Distinguished Member of Technical Staff; and Technical Director. I led the Advanced Hardware Development division in relaunching a multi-chip integrated circuit module facility.

4. At Draper Labs, a fabrication line for “multi-chip modules” had been established in the late 90s, and many of my chip and module projects incorporated some of the original “MCM-D” technology provided by this line. I became active in leading the implementation of a new set of processes for MCM-D in order to have it meet the standards required for military and space qualification. In addition to using the licensed MCM-D process, I helped implement several improved fabrication and test methods for building large, more advanced multi-chip modules. During the ‘00s, I published and received a patent for some of that development work. I led a team which carried out thermo-mechanical modeling of the various package configurations to determine which processes were appropriate to demanding Draper applications. I became familiar with the world-wide

development efforts in commercial packaging during that time and adopted some of the lessons learned from their published results, and from the results of Draper-sponsored reverse-engineering reports. In addition to other chip and sensor engineering work during 2015–2020, I assumed management responsibility for next-generation state-of-the-art multichip module process development and supervised further technical improvements.

5. I have received many awards at Draper, including the 2010 Distinguished Performance Award and the 2010 Best Patent Award.

6. I have nearly four decades of extensive experience working on and with semiconductors.

7. I have authored over 25 publications in peer-reviewed academic journals, transactions and books.

8. I am a named inventor in six issued U.S. patents.

9. I am a member of multiple societies, including the IEEE and the American Physical Society (APS).

10. A copy of my curriculum vitae (“CV”) is attached as Appendix A.

11. I understand that U.S. Patent No. 9,859,202 (“the ’202 Patent”) was filed on June 23, 2016 as U.S. Patent Application No. 15/190,695. I understand that this application claims priority to a U.S. Provisional Patent Application No. 62/184,034, filed June 24, 2015.

12. I am familiar with the technology of the '202 Patent.

13. I am familiar with the knowledge and capabilities of a person of ordinary skill in the art at the time of the earliest possible priority date of the '202 Patent – June 24, 2015 – which I have defined further below.

14. I have reviewed the following references in preparing this declaration, all of which I understand to be prior art to the '202 Patent:

- U.S. Patent Application Publication 2013/0182402 (“Chen”) (EX1003), which was filed on January 18, 2012 and published on July 18, 2013;
- U.S. Patent Application Publication 2011/0147908 (“Sun”) (EX1004), which was filed on December 17, 2009 and published on June 23, 2011;
- U.S. Patent Application Publication 2016/0056087 (“Wu”) (EX1005), which was filed on August 22, 2014 and published on February 25, 2016;
- U.S. Patent Application Publication 2009/0140415 (“Furuta”) (EX1006), which was filed on June 27, 2008 and published on June 4, 2009;

15. I provide below the list of exhibits that I have considered in preparing this Declaration. I have reviewed and considered the following exhibits and all

other documents mentioned in my declaration. Additionally, my opinions are based on my technical education, training and experience in the field.

Exhibit	Description
1001	U.S. Patent No. 9,859,202 (“’202 Patent”)
1003	U.S. Patent Application Publication No. 2013/0182402 (“Chen”)
1004	U.S. Patent Application Publication No. 2011/0147908 (“Sun”)
1005	U.S. Patent Application Publication No. 2016/0056087 (“Wu”)
1006	U.S. Patent Application Publication No. 2009/0140415 (“Furuta”)
1007	Prosecution History of U.S. Patent No. 9,859,202 (“’202 Patent FH”)
1008	U.S. Patent Application Publication No. 2014/0248742
1009	U.S. Patent Application Publication No. 2011/0159284
1010	U.S. Patent Application Publication No. 2008/0155820 (“Arai”)
1011	U.S. Patent Application Publication No. 2015/0001708

16. I have been retained to serve as an expert for Apple Inc. (“Apple”) in the field of semiconductor integrated circuit processing and fabrication.

17. I am being compensated at my usual hourly rate of \$450, and the conclusions or opinions that I reach and express in my declaration have no bearing on my compensation.

18. I do not have any financial interest in the outcome of this case nor do I have any financial interest in Apple.

19. I do not personally know Dyi-Chung Hu and have never had any personal contact with him.

I. Relevant Law

20. Counsel has informed me about the following aspects of patent law, which I have applied in my analysis and conclusions.

A. Person of Ordinary Skill in the Art

21. I have been informed and understand that a patent should be analyzed within the framework of a person of ordinary skill in the art (“POSITA”), which is a hypothetical individual. I have been told to assume that a POSITA would have been knowledgeable about the prior art that was publicly accessible at the time of the priority date of the patent. Here, the claimed priority date of the ’202 Patent is June 24, 2015.

22. I have also been informed that factors considered in determining a level of POSITA include (1) sophistication of the technology, (2) challenges and types of problems faced within the field, (3) solutions to these problems known at the priority date of the patent, (4) levels of education of professionals actively working in the field, including that of the named inventor, (5) types of testing described in the patent and the requisite skills needed to perform those tests, and (6) the general state of the technology overall.

23. I have been informed that a POSITA is a person of ordinary creativity. A POSITA is not an automaton and would be able to consider and put together teachings from multiple prior art references.

B. Claim Construction

24. I have been informed that to determine the meaning of the terms in the claims of the ’202 Patent for the purposes of the *inter partes review*, one should

generally use the ordinary and customary meaning as understood by a POSITA at the time of the claimed priority date, taking into consideration the claim language and patent specification.

25. I have been informed that a patentee can include a definition of a claim term in the specification. In such instances, I understand that the claim should generally be interpreted according to that definition provided in the patent.

26. I have been informed that the patent's claims, specification, and the file history (EX1007) should be analyzed to arrive at the proper interpretation of a claim term.

C. Obviousness

27. I have been informed that a claim can be found unpatentable based on obviousness if a prior art reference, either alone or in combination with other prior art reference(s), teaches or suggests the claims.

28. I further understand that although patent drawings may not necessarily be drawn to scale, patent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their spatial relations to one another.

29. I have been informed and understand that a patent claim is considered obvious to a POSITA in view of a single or multiple references if the differences between the subject matter in the prior art and the subject matter in the claim

would have been obvious to a POSITA before the priority date of the patent.

Therefore, I understand that the challenged claims of the patent should be read from the point of view of a POSITA. For example, I have been informed that a claim would have been found unpatentable for being obvious if a POSITA would have been motivated to combine the teachings of two or more prior art references to achieve the claimed subject matter, and the POSITA would have had a reasonable expectation of success to do so.

30. I have been informed that in an *inter partes* review, the Patent Trial and Appeal Board (the “Board”) evaluates obviousness of a claim under a preponderance of the evidence standard, which means that the Board determines that a claim is unpatentable for being obvious when the claim is more likely obvious than nonobvious.

31. I have been informed that the Supreme Court has held that the combination of known elements combined according to known methods that produces nothing more than predictable results is likely obvious. Additionally, I have been informed that the Supreme Court indicated that obviousness may be found if:

- there is some teaching, suggestion, or motivation in the prior art that would have led a POSITA to combine prior art reference teachings or modify the prior art to arrive at the claims;

- the modification is a combination of prior art elements according to known methods that yields predictable results;
- the combination of prior art is a simple substitution of one known element for another to obtain predictable results;
- the combination of prior art elements is an application of a known technique to a known device (or method) ready for improvement to yield predictable results;
- the changed element(s) represent one of a finite number of identified, predictable solutions, and a POSITA would have a reasonable expectation of success that such modification would work.

32. I have been informed that an obviousness determination cannot be based on the benefit of hindsight gained from the patent under consideration. Therefore, the patent's claim or its description of the claimed subject matter cannot be used as a roadmap in considering combinations of prior art references.

II. Summary of Opinions

33. For the reasons explained below, I conclude that claims 1–9 of the '202 Patent are anticipated and rendered obvious by the prior art.

Grounds	Under 35 U.S.C. §	Claims	Prior Art Reference(s)
I	103	1–4, 7–9	Chen in view of Sun
II	103	5–6	Chen in view of Sun and Furuta
III	103	1–4, 7–9	Chen in view of Wu
IV	103	5–6	Chen in view of Wu and Furuta

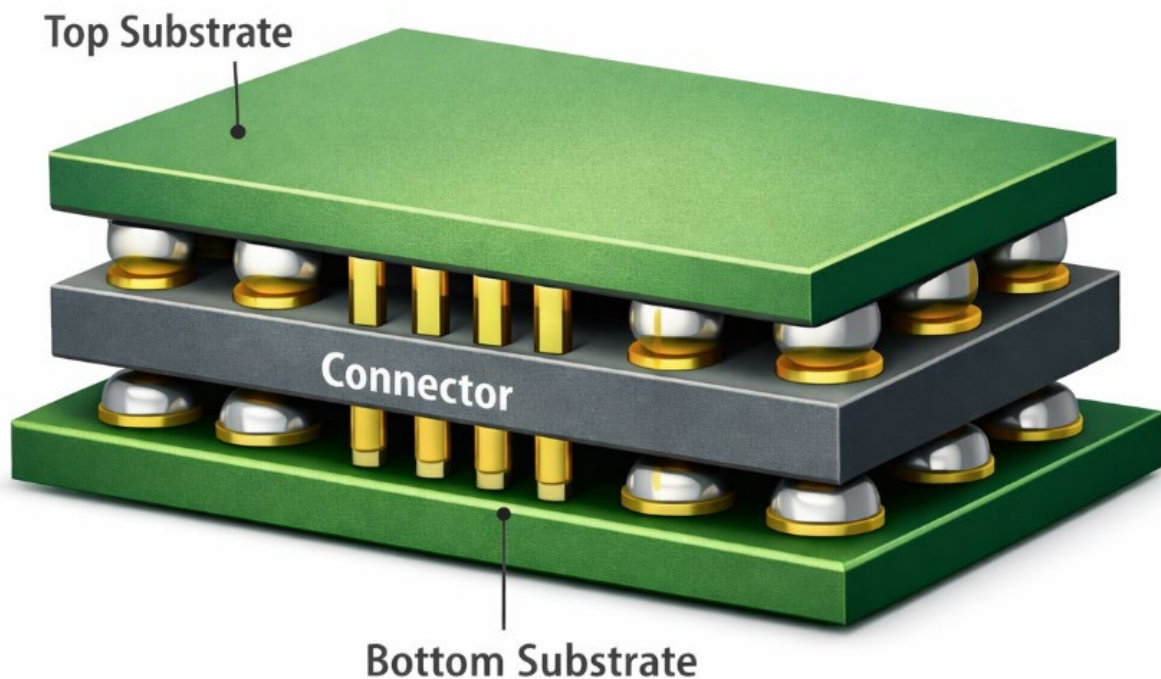
III. Technology Background

A. Semiconductor Packaging & Interconnects

34. Modern semiconductor devices (e.g., processors, memory) are mounted in packages that protect the die and provide electrical connections to the outside world. As chips have become smaller and more powerful, packaging technologies have evolved from simple wire-bonded plastic packages to multi-chip stacked systems. These multi-chip stacked systems often employ metal pillars, solder balls, or micro-bumps to form the requisite vertical connections. The '202 Patent focuses on a specific type of connector—which the '202 Patent calls a “spacer connector”—that fits between such substrates and provides these interconnects.

B. Connectors

35. A connector is a simple structure that serves two functions: (1) a mechanical spacer to define a controlled distance (or stand-off height) between two substrates and (2) an electrical interconnect electrically coupling the two substrates. Often, spacers utilize metal pillars that pass through the spacers and align with corresponding pillars or solder on the substrates above and below it. Solder is also often utilized to make the electrical connections between the substrates and the connectors.



IV. Overview of the '202 Patent

A. Summary of the '202 Patent

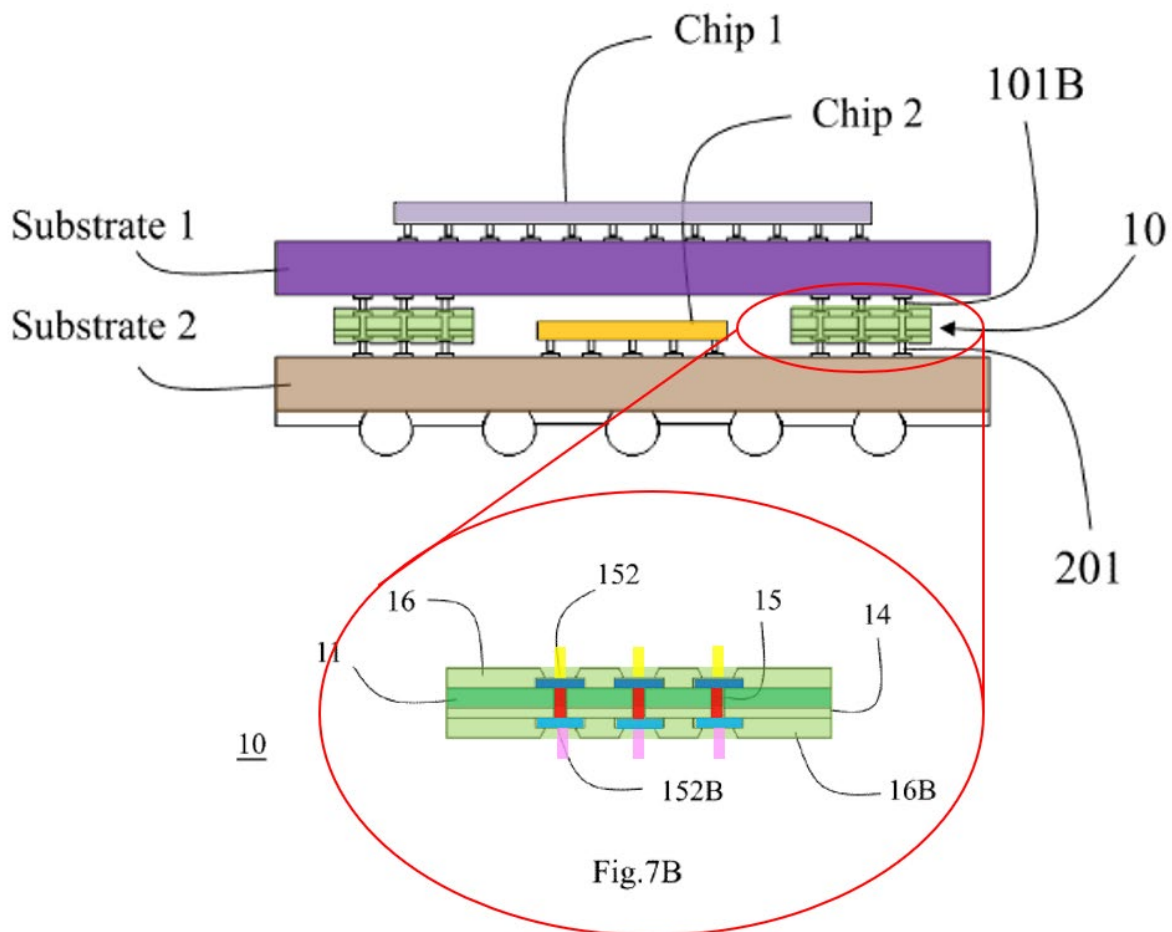
36. I have reviewed the '202 Patent. *See* EX1001.

37. The '202 Patent describes a spacer connector structure and associated fabrication method. EX1001 at 1:13–15 (“The present invention relates to a fabricating process for making a spacer connector, especially using a conductive carrier in an initial step of the fabrication process.”).

38. The '202 Patent describes three different embodiments for making a spacer connector.

39. “FIGS. 1A–7A show a fabricating process for a first embodiment.” EX1001 at 1:53–54. “FIG. 8 shows an application for the first spacer connector” in which “two **spacer connectors 10** are configured in between **package substrate 1** and **package substrate 2**. FIG 8 shows **chip 1** is configured on a top center of **package substrate 1**. **Chip 2** is configured on a top center of **package substrate 2**. **Package substrate 1** is stacked on a top of **package substrate 2**. The **package substrate 1** has a plurality of **bottom metal pillars 101B**, each **metal pillar 101B** is electrically coupled to a corresponding **top metal pad 152** of the **spacer connector 10**. The **package substrate 2** has a plurality of **top metal pillars 201**, each **metal pillar 201** is electrically coupled to a corresponding **bottom metal pad 152B** of the **spacer connector 10**.” EX1001 at 2:28–42. The **spacer connector 10** is made up of a **core substrate 14**, passivation 16, and dielectric adhesive 14 and includes **metal pillars 15** running through the **spacer connector 10**. *See* EX1001 at 2:1–27.

Fig.8

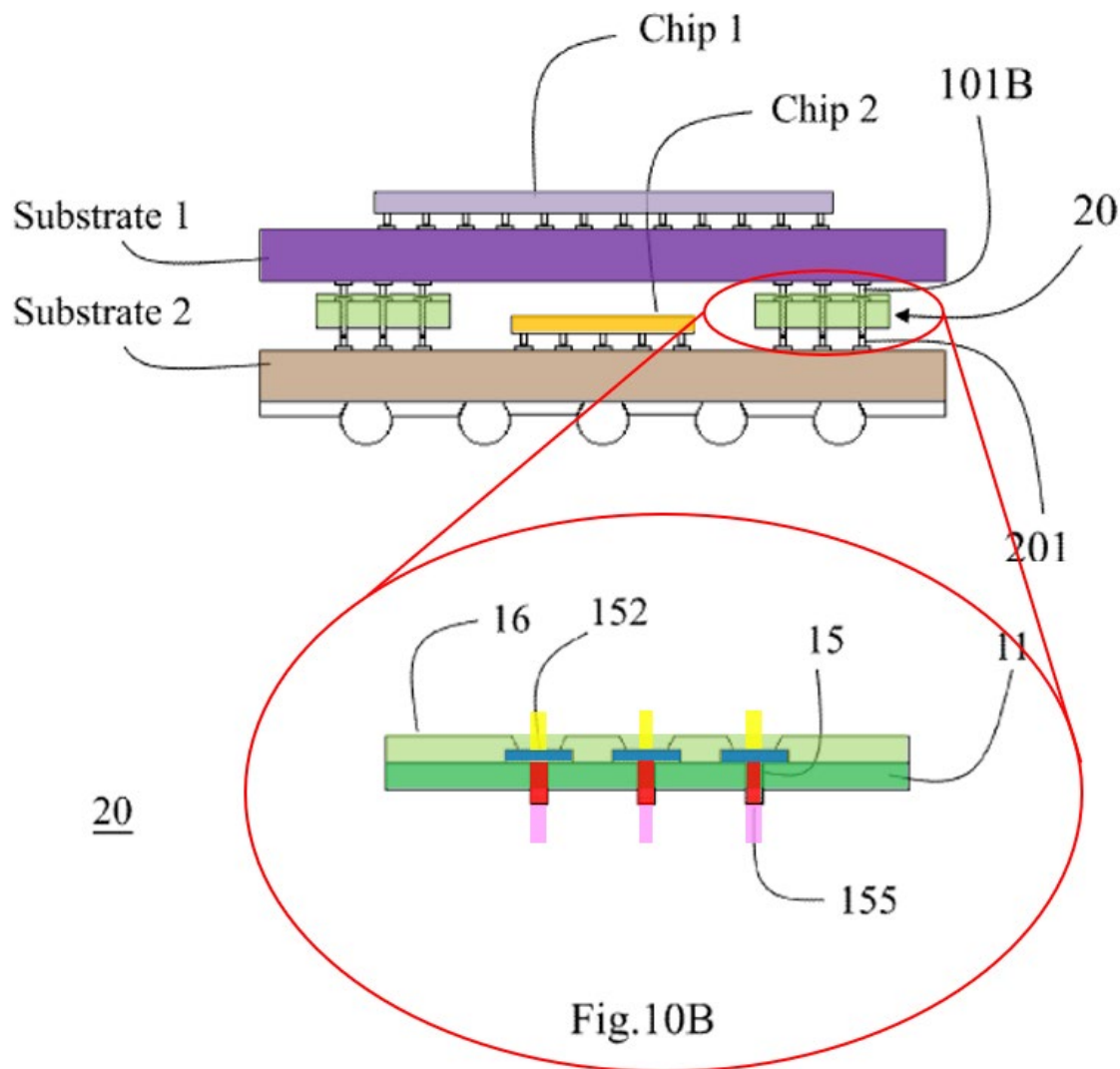


EX1001 at Figures 7B and 8.

40. FIGS. 1A–5B, 9A–10 show a fabricating process for a second embodiment.” EX1001 at 1:43–44. “FIG. 11 shows an application for the second spacer connector” in which “two **spacer connectors 20** are configured in between **substrate 1** and **substrate 2**. FIG. 11 shows **chip 1** is configured on a top center of

substrate 1. **Chip 2** is configured on a top center of **substrate 2**. **Substrate 1** is stacked on a top of **substrate 2**.” EX1001 at 2:59–65.

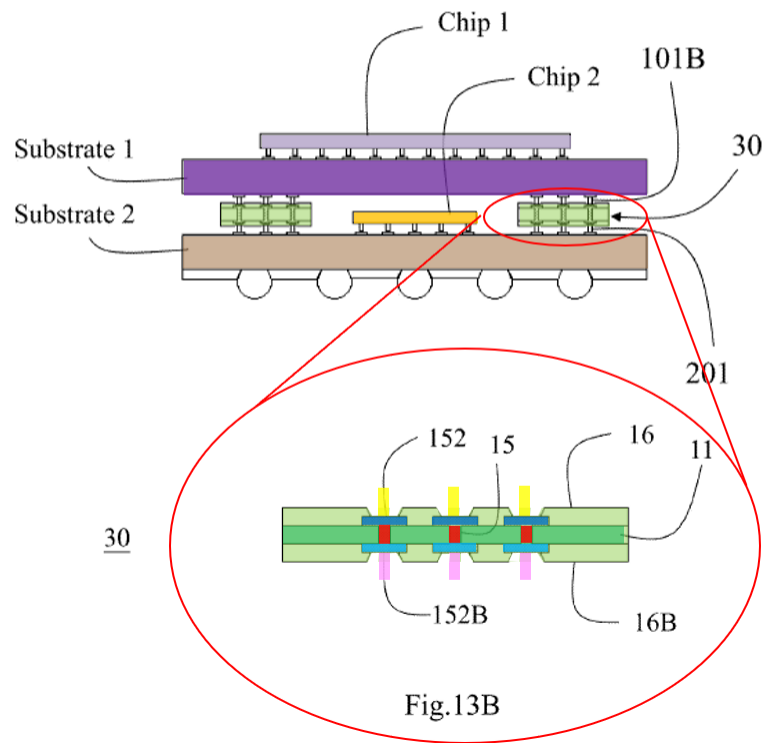
Fig.11



EX1001 at Figures 10B and 11.

41. “FIGS. 1A–5B, 12A–13A show a fabricating process for a third embodiment.” EX1001 at 2:66–67. “FIG. 14 shows an application for the third spacer connector” in which “two **spacer connectors 30** are configured in between **substrate 1** and **substrate 2**. FIG. 11 shows **chip 1** is configured on a top center of **substrate 1**. **Chip 2** is configured on a top center of **substrate 2**. **Substrate 1** is stacked on a top of **substrate 2**.” EX1001 at 3:17–23. This third embodiment does *not* appear to be claimed in claims 1–9 of the ’202 Patent because the “bottom end of each **metal pillar** among the **plurality of metal pillars** [do not] protrude[] downwardly from a bottom surface of the **core substrate**,” as claimed in claim 1. EX1001 at claim 1.

Fig.14



EX1003 at Figures 13B and 14.

B. Summary of the Prosecution History of the '202 Patent

42. I have reviewed the file history of the '202 Patent which I summarize below. *See* EX1007.

43. The Examiner issued a non-final office action on July 21, 2017, rejecting all of the claims that were pending as being anticipated or obvious over U.S. Patent Application Publication No. 2008/0155820 ("Arai"). *See* EX1007 at 100–104.

44. And because it is relevant to my discussion of claim 8, I specifically point out that for then-pending claim 19 (which corresponds to issued claim 8 of the '202 Patent), the Examiner rejected the claim as being anticipated by Arai, noting the following:

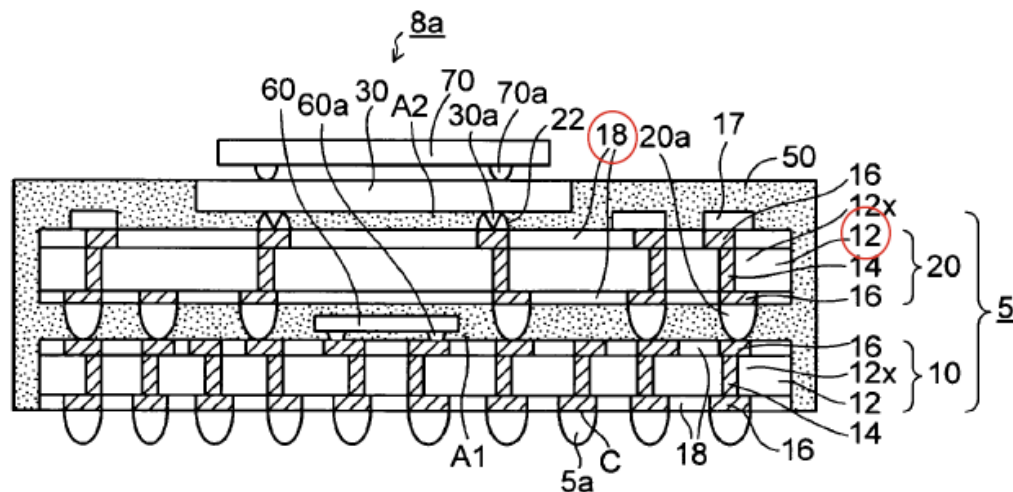
Re Claim 19, Arai show and disclose

The structure of claim 18, wherein the dielectric layer is a dielectric adhesive (dielectric layer 18 adhered to core 12, fig. 11) into which the core substrate is pasted.

EX1007 at 102.

45. Arai's Figure 11 is reproduced below, in which I have indicated the dielectric layer 18 and core 12 in red. As shown, the Examiner merely pointed to the dielectric layer 18 being "adhered to" core 12 as meeting this limitation.

FIG. 11



EX1010 at Figure 11.

46. However, the Examiner indicated three dependent claims 12–14 to be allowable, noting the following:

Claim 12 and all claims dependent thereof are allowable because the prior art of record neither anticipates nor renders obvious the limitations of the claim in combination as claimed, including:

further comprising: a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein the bottom chip is mounted to the top surface of the bottom package substrate, and the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

EX1007 at 104.

47. Without arguing against the rejection against Arai, on October 19, 2017, independent claim 10 was amended to incorporate the limitations that were recited in claim 12. *See* EX1007 at 113–125.

48. Specifically, Applicant acquiesced to the Examiner’s rejection that in then-pending claim 19 (now issued claim 8) the limitation is met by Arai’s “dielectric layer 18 adhered to core 12.” EX1007 at 102 and 113–125.

49. That led to the Examiner issuing a Notice of Allowance on November 7, 2017. *See* EX1007 at 129–137. Accordingly, on January 2, 2018, the '202 Patent issued.

V. Level of Ordinary Skill in the Art

50. As I noted above in paragraphs 21–23, I have been informed by the counsel that a patent and the prior art should be analyzed within the framework of a POSITA.

51. In my opinion, a POSITA as of the earliest claimed priority date of the '202 Patent (*i.e.*, June 24, 2015) would have a bachelor's degree in material science, mechanical engineering, electrical engineering, or physics, or an equivalent engineering discipline and a minimum of two years of experience in the field of integrated circuit processing, fabrication, and packaging. I note that a higher level of education or specific skills in the industry may make up for less experience and vice versa.

52. I met and/or exceeded these requirements for POSITA as of June 24, 2015, for at least the reasons provided above in paragraphs 2–10.

VI. Claim Construction

53. I have been asked to determine if any particular claim terms should be construed so the Board can understand how the prior art references read on the

challenged claims. As such, I have reviewed the claims, specification, and file history of the '202 Patent.

54. I have not found any specific definitions for any of the claim terms of the '202 Patent.

55. In my opinion, all of the claim terms are utilized in the plain and ordinary meaning of the words, although in some instances, it is unclear whether the claim language requires certain structures to be formed in certain order of steps.

56. For example, in limitation [1H], Patent Owner may argue that the “**plurality of bottom metal pillars**” must first be formed on the “**top package substrate**” because the limitation recites “the **top package substrate** has, on a bottom surface thereof, a **plurality of bottom metal pillars**.”

57. Similarly, in limitation [1I], Patent Owner may argue that the “**plurality of top metal pillars**” must first be formed on the “**bottom package substrate**” because the limitation recites “the **bottom package substrate** has, on a top surface thereof, a **plurality of top metal pillars**.”

58. I understand imparting processing step requirements in a claim that is directed to a structure is generally inappropriate. But nevertheless, because these particular processing steps were well-known in the art, I have provided Grounds III and IV demonstrating that the claims would have been obvious, even if the claims

were interpreted to require these additional processing steps to be performed in a particular order.

VII. Specific Invalidity Grounds

59. As I explained in paragraph 33, I conclude that claims 1–9 of the '202 Patent are rendered obvious by the prior art. In the sections below, I explain in detail how claims 1–9 of the '202 Patent are not patentable over prior art.

A. Ground I: Claims 1–4 and 7–9 Are Rendered Obvious By Chen In View Of Sun

60. In my opinion, claims 1–4 and 7–9 are rendered obvious by Chen in view of Sun for the following reasons.

1. Independent Claim 1

i. a) [1Pre] A structure, comprising:

61. In my opinion Chen teaches [1Pre].

62. I understand that the preamble may not limit the claims. Regardless, I have colored Figure 9 of Chen to demonstrate the various structures that I will describe in connection with independent claim 1. Similar to the '202 Patent, Chen concerns semiconductor packaging with a package-on-package configuration in which multiple integrated circuit packages are vertically stacked and electrically interconnected to achieve higher functional density within a reduced footprint. *See, e.g.,* EX1003, [0004] (“FIGS. 1 through 9 are cross-sectional views and a top view of intermediate stages in the manufacturing of a Package-on-Package (PoP)

structure”); EX1001, claim 1. Chen qualifies as analogous art at least because Chen resides within the same field of endeavor of semiconductor package-on-package structures as addressed by the '202 Patent. Chen is also analogous art because it is reasonably pertinent to the problem faced by the '202 patent as it addresses methods of electrically interconnecting a top package substrate to a bottom package substrate using two intervening substrate structures to establish conductive pathways between stacked packages. See EX1001, claim 1 (“the top package substrate is electrically coupled to the bottom package substrate through... the spacer connector...”).

63. But at a high level, Chen describes a structure in which a **top package component 62** is electrically coupled to a **bottom package component 56** through two **Through-Assembly Via (TAV) Modules 28** on either side of the **package component 24**. EX1003 at [0012] (“FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, **TAV modules 28** are disposed on opposite sides of **package component 24**. Although two **TAV modules 28** are illustrated, there may be one or more than two **TAV modules 28**.”), [0018], [0019] (“FIG. 9 illustrates the bonding of **top package component 62** to **bottom** package 60. In some embodiments, top package component 62 is a device die. Alternatively, **package component 62** is a package that includes a **device die (not shown) bonded to a package substrate (not shown)**, or the like. In the resulting

package, TAV modules 28 are used to electrically couple the circuit devices in
package component 62 to **package component 56.**”), Abstract.

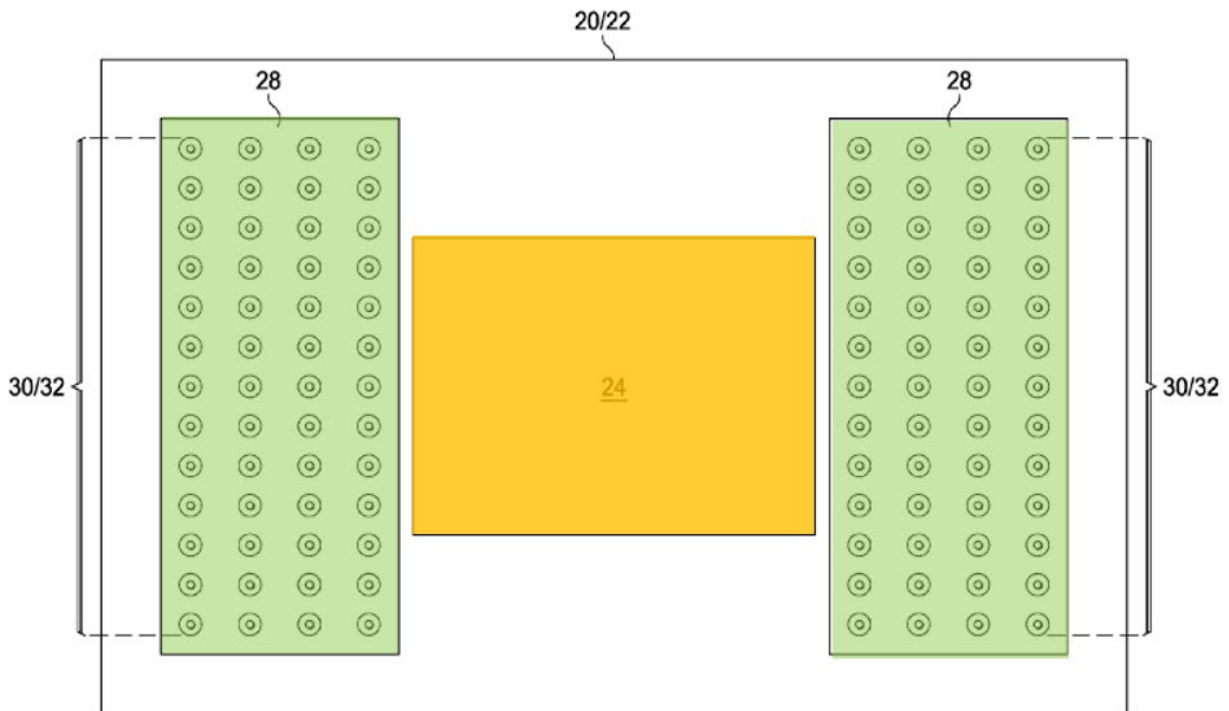


FIG. 2

EX1003 at Figure 2.

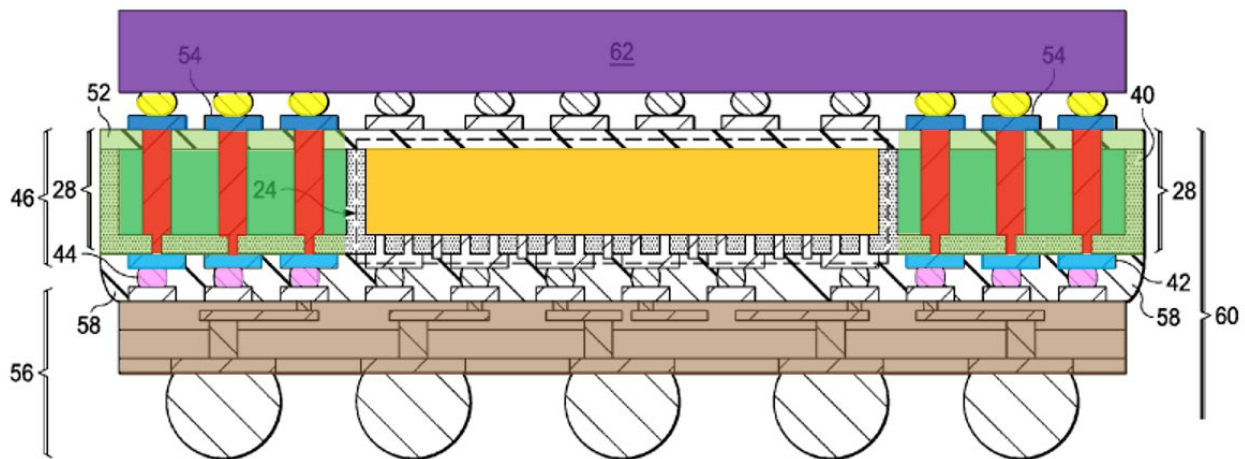


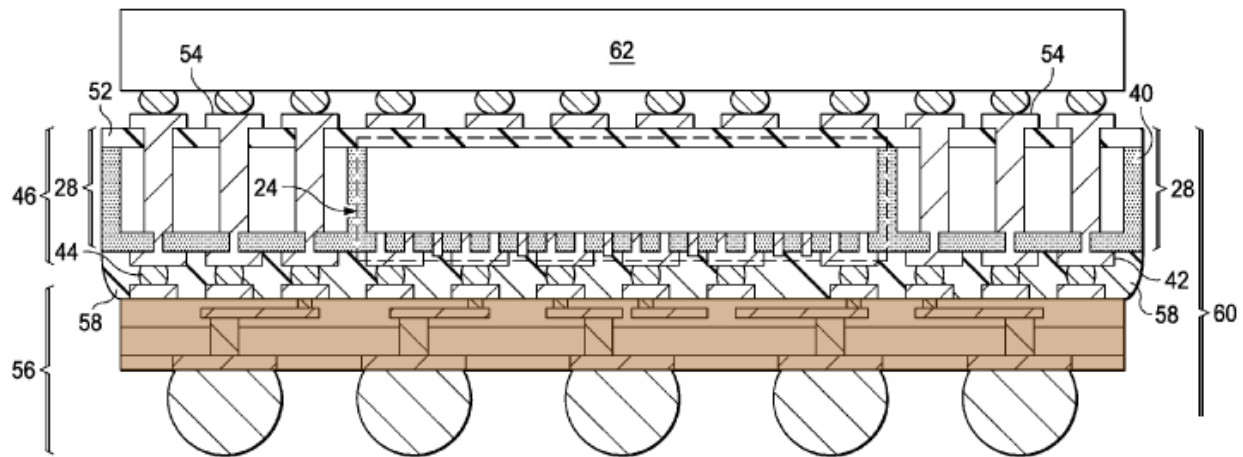
FIG. 9

EX1003 at Figure 9.

ii. [1A] a **bottom package substrate**;

64. In my opinion, Chen teaches [1A].

65. As I have highlighted in the bottom of Figure 9, Chen discloses **package component 56**, which Chen states “may be a **package substrate**.” EX1003 at [0018] (“Referring to FIG. 8, package 46 is bonded to **package component 56** to form bottom package 60. **Package component 56** may be a **package substrate**, an interposer, a device die, a Printed Circuit Board (PCB), or the like.”).



EX1003 at Figure 9.

iii. [1B] a **top package substrate** stacked on top of the **bottom package substrate**;

66. In my opinion, Chen teaches [1B].

67. As shown in Figure 9, the **top package component 62** (which includes a **package substrate**) is stacked on top of the **package component 56**. EX1003 at [0019] (“FIG. 9 illustrates the bonding of **top package component 62** to **bottom** package 60. In some embodiments, top package component 62 is a device die. Alternatively, **package component 62** is a package that includes a **device die (not shown) bonded to a package substrate (not shown)**, or the like. In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in **package component 62** to **package component 56**.”).

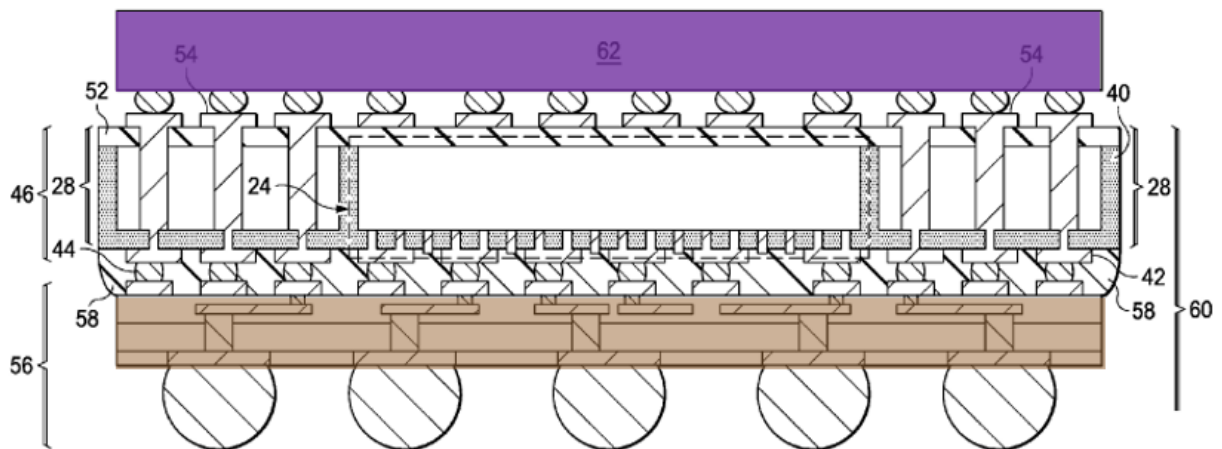


FIG. 9

EX1003 at Figure 9.

- iv. [1C] at least one **spacer connector** interposed between the **bottom package substrate** and the **top package substrate** to define a space between the **bottom package substrate** and the **top package substrate**,

68. In my opinion, Chen teaches [1C].

69. Figure 2 below clearly shows two **Through-Assembly Via (TAV) modules 28**. See EX1003 at [0012] (“FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, **TAV modules 28** are disposed on opposite sides of package component 24. Although two **TAV modules 28** are illustrated, there may be one or more than two TAV modules 28.”).

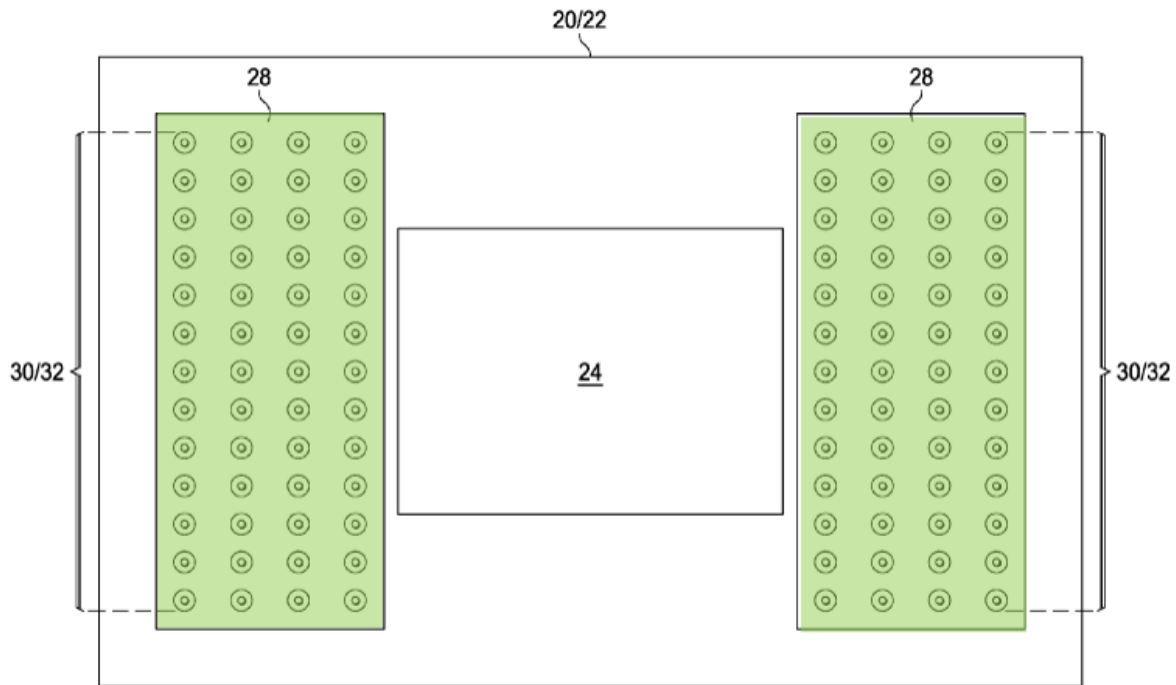


FIG. 2

EX1003 at Figure 2.

70. And as shown in Figure 9, the two **TAV modules 28** are placed between the **top package component 62** and the **bottom package component 56**.

EX1003 at [0019] (“In the resulting package, **TAV modules 28** are used to electrically couple the circuit devices in **package component 62** to **package component 56**.”).

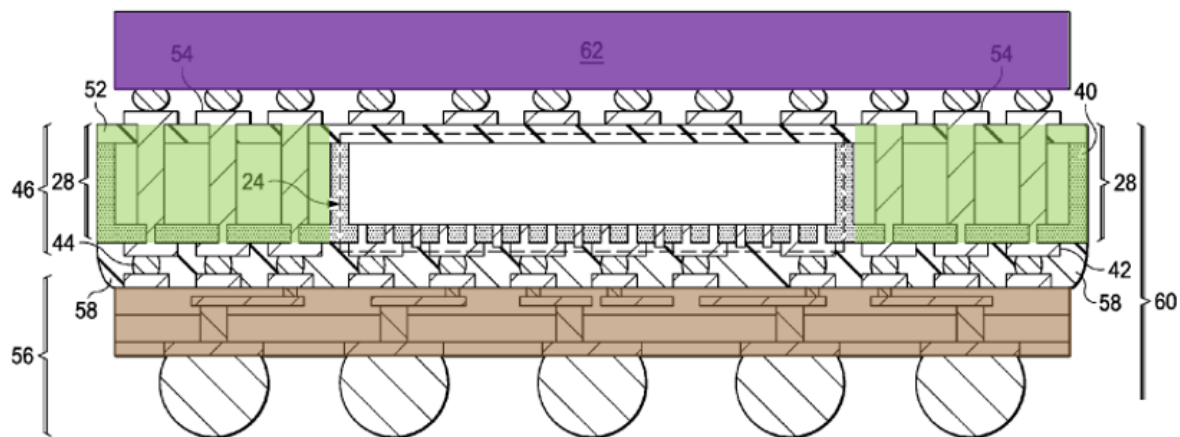


FIG. 9

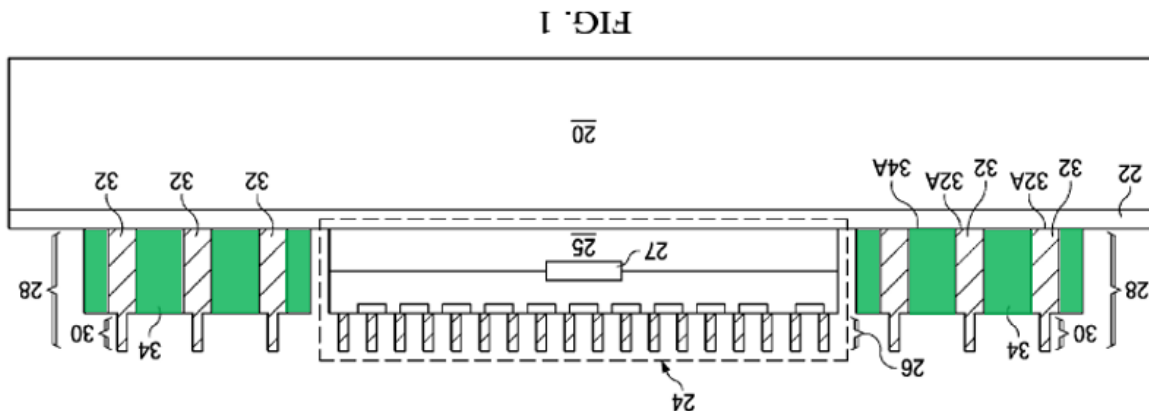
EX1003 at Figure 9.

71. And based on the plan and cross-sectional views shown in Figures 2 and 9, the two **TAV modules 28** define a space that allows the placement of package component 24 in that space. See EX1003 at [0009] (“Package component 24 and **Through-Assembly Via (TAV) modules 28** are then placed on release layer 22. The bottom surfaces of package component 24 and **TAV modules 28** are in contact with the top surface of release layer 22, and are level with each other. The position of package component 24 and TAV modules 28 are accurately aligned to desirable locations, so that the subsequent formed redistribution lines may electrically couple to metal posts 26 and 30. In some embodiments, a package component 24 include sone or a plurality of device dies. For example, package component 24 may include a Central Computing Unit (CPU) die or another type of logic die having logic circuits.”), [0023].

v. [1D] wherein the **spacer connector** comprises a **core substrate**;

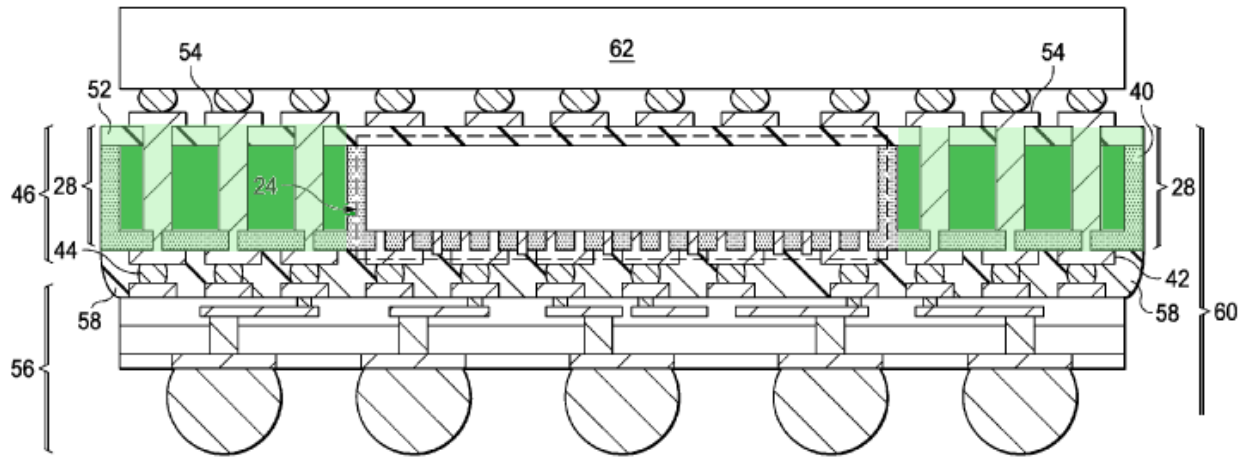
72. In my opinion, Chen teaches [1D].

73. As shown in the fabrication process described in conjunction with Figure 1 below, the **TAV modules 28** includes a **substrate 34**. See EX1003 at [0010] (“**TAV modules 28** include **substrate 34**, which may be a semiconductor substrate such as a silicon substrate.”).



EX1003 at Figure 1.

74. Figure 1 is rotated 180 degrees relative to Figure 9, but shows that **substrate 34** is part of the **TAV modules 28** in the structure shown in Figure 9.



EX1003 at Figure 9.

- vi. [1E] a plurality of metal pillars, each passing through the core substrate;

75. In my opinion, Chen teaches [1E].

76. As shown in the fabrication process described in conjunction with Figure 1 below, a number of different through substrate vias 32 and metal posts 30 made of metals (*e.g.*, copper) are fabricated to pass through substrate 34 of the TAV modules 28. See EX1003 at [0010] (“Through-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34. Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like. In some embodiments, bottom ends 32A of through-substrate vias 32 are level with the bottom surface 34A of substrate 34. Accordingly, bottom ends 32A of through-substrate vias 32 may be in contact with release layer 22. TAV modules 28 may

also include **metal posts 30** (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal post 26 and 30 are substantially level with each other.”).

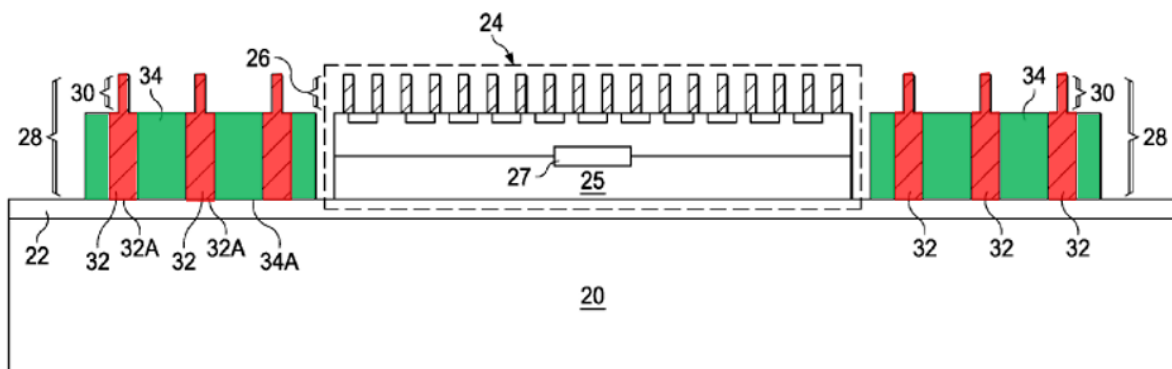


FIG. 1

EX1003 at Figure 1.

77. Figure 1 is rotated 180 degrees relative to Figure 9, but shows that **through substrate vias 32** and **metal posts 30** made of metals (*e.g.*, copper) pass through **substrate 34** of the **TAV modules 28** in the structure shown in Figure 9.

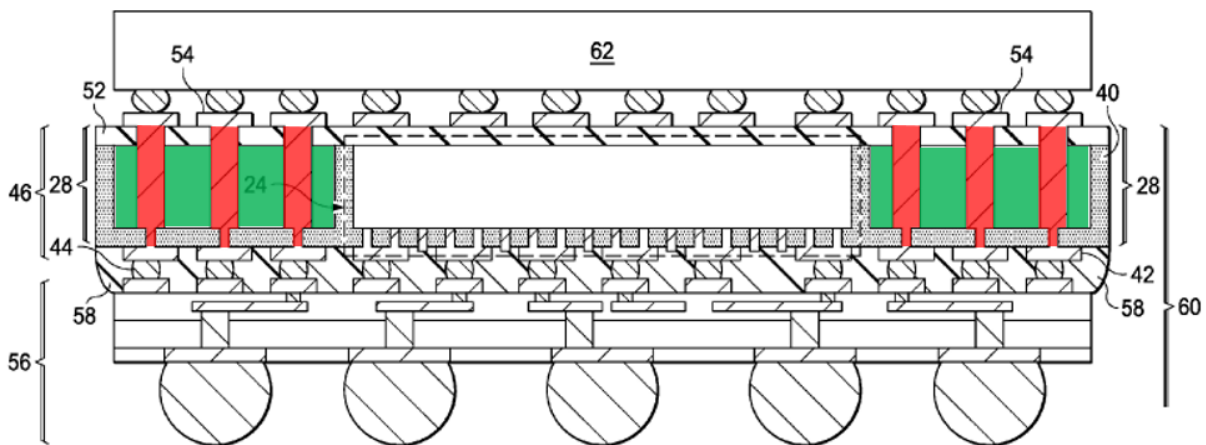


FIG. 9

EX1003 at Figure 9.

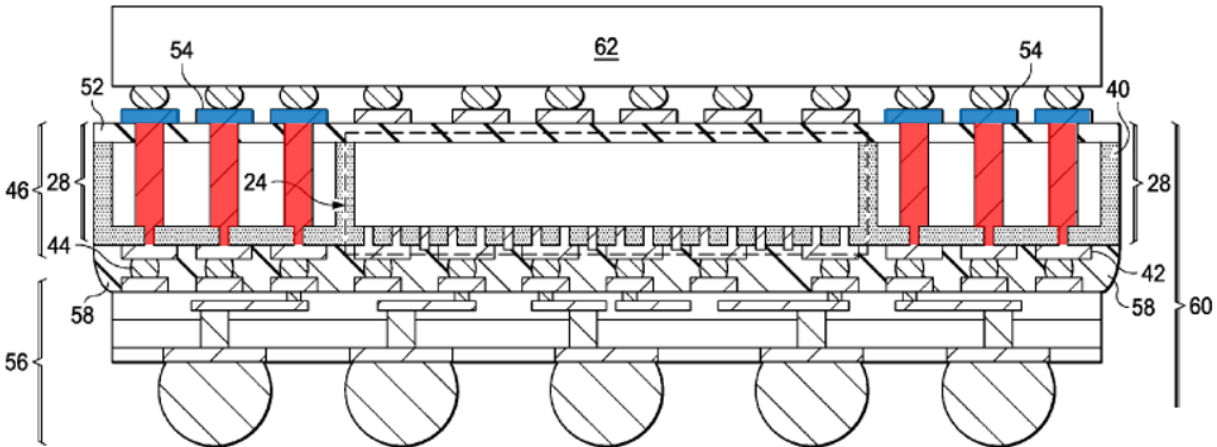
- vii. [1F] a **plurality of top metal pads**, each on a top end of a corresponding **metal pillar** among the **plurality of metal pillars**;

78. In my opinion, Chen teaches [1F]. At a minimum, Chen alone renders obvious [1F].

79. First, in my opinion, Chen teaches [1F] because Chen teaches **redistribution layers (RDLs) 54** that are located at the top end of the **through-substrate vias 32**. EX1003 at [0017] (“**RDLs 54** are then formed on dielectric layer 52 and connected to RDLs [42].”), claim 15 (“forming a first plurality of Redistribution Lines (RDLs) over the polymer and connected to the metal posts of the device die and the metal posts of the TAV module, wherein the device die, the TAV module, and the first plurality of RDLs form a package; ... forming a **second plurality of RDLs** coupled to the **plurality of through-vias**, wherein the first and the second plurality of RDLs are on opposite sides of the package.”), claim 17 (“wherein the **second plurality of RDLs** is electrically coupled to the **plurality of through-vias** through openings in the dielectric layer.”).

80. In my opinion, a POSITA would readily understand that these are made of metal because Chen describes that the same corresponding **RDLs 42** on the opposite side of the **TAV modules 28** are deposited as a metal layer and patterned. See EX1003 at [0014] (“**RDLs 42** may be formed by depositing a **metal**

layer, and then patterning the *metal layer*.”). A POSITA would understand **RDLs 54** to be formed in exactly the same manner.



EX1003 at Figure 9.

81. At a minimum, in my opinion, Chen renders obvious [1F] because applying the teachings of forming **RDLs 42** to that of forming **RDLs 54** would have an obvious modification, which amounts to using the known technique of depositing a metal layer and patterning it to form metal pads to obtain the same RDLs that function as metal pads. A POSITA would have had a reasonable expectation of success in applying the teachings associated with RDLs 42 to forming **RDLs 42** to that of forming **RDLs 54**.

viii. [1G] wherein a bottom end of each **metal pillar** among the **plurality of metal pillars** protrudes downwardly from a bottom surface of the **core substrate**;

82. In my opinion, Chen teaches [1G].

83. As shown in Figure 9 below, the **through-substrate vias 32** have **metal posts 30** that protrude down from a bottom surface of **substrate 34**.

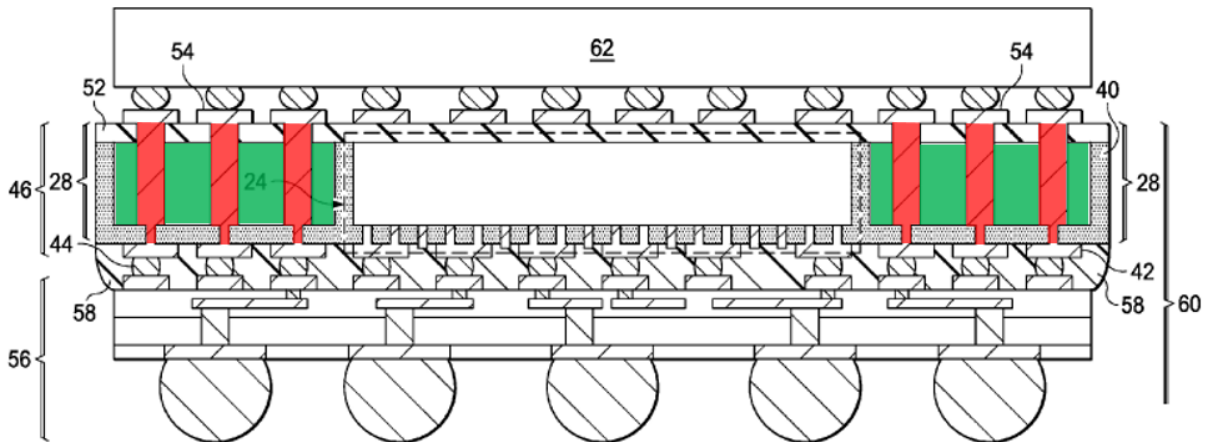


FIG. 9

EX1003 at Figure 9.

84. The fabrication process described in association with Figure further demonstrates this, although I have rotated Figure 1 by 180 degrees to match the orientation shown in Figure 9. See EX1003 at [0010] (“**Through-substrate vias 32** are formed in **substrate 34** for inter-coupling the conductive features on opposite sides of **substrate 34**. **Through-substrate vias 32** are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like. In some embodiments, bottom ends 32A of through-substrate vias 32 are level with the bottom surface 34A of substrate 34. Accordingly, bottom ends 32A of through-substrate vias 32 may be in contact with release layer 22. **TAV modules 28** may also include **metal posts 30** (such as copper posts) formed as top

ix. [1H] the **top package substrate** has, on a bottom surface thereof, a **plurality of bottom metal pillars** each coupled to a corresponding **metal pillar** among the **plurality of metal pillars** of the **spacer connector**,

86. At the outset, Figure 9 shows Chen’s package-on-package structure.

See EX1003 at [0004] (“FIGS. 1 through 9 are cross-sectional views and a top view of intermediate stages in the manufacturing of a Package-on-Package (PoP) structure in accordance with some exemplary embodiments.”).

87. Regardless of how the different components of the PoP structure were assembled, the **package component 62** shown in Figure 9 has a number of **unlabeled connectors** that are on the bottom surface of the **package component 62**. And each of those **unlabeled connectors** are coupled to a corresponding **through-substrate vias 32** and **metal posts 30** of the **TAV modules 28**. *See* EX1003 at [0019] (“FIG. 9 illustrates the bonding of **top package component 62** to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, **TAV modules 28** are used to **electrically couple** the circuit devices in **package component 62** to **package component 56**.”), claim 1 (“wherein the **first plurality of RDLs** is electrically coupled to the **second plurality of RDLs** through the plurality of **through-vias** in the **TAV module**”), claim 15 (“forming a **second plurality of RDLs** coupled to the **plurality of through-vias**, wherein the **first [plurality of RDLs]** and the **second plurality of RDLs** are on opposite sides of the package.”).

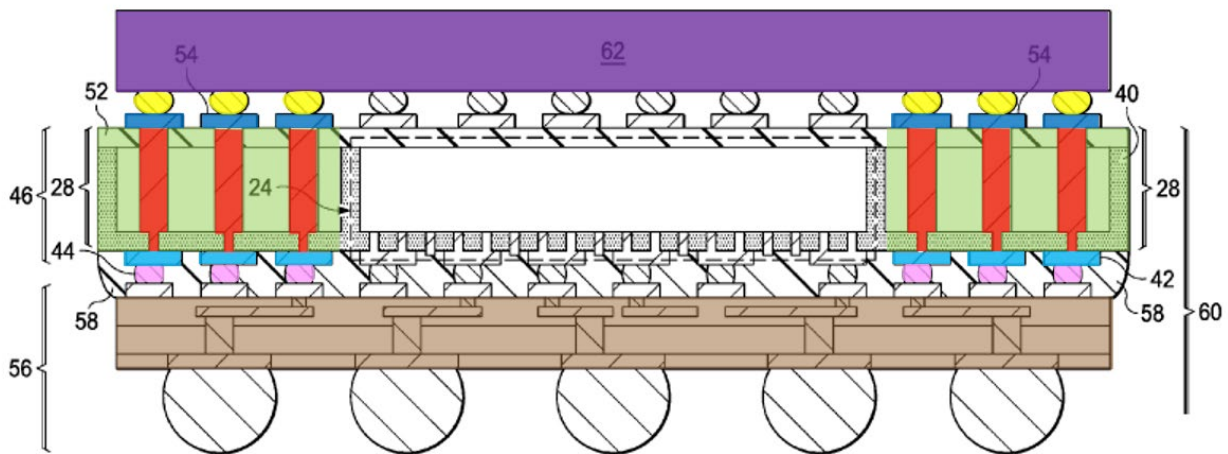


FIG. 9

EX1003 at Figure 9.

88. And these **unlabeled connectors** appear nearly identical to **connectors 44** on the opposite side of the **TAV modules 28** that are connected to **RDLs 42**, which in turn are connected to the same **through-substrate vias 32** and **metal posts 30** of the **TAV modules 28**. EX1003 at [0014] (“Next, referring to FIG. 4, **Redistribution Lines (RDLs) 42** and **connectors 44** are formed to connect to **metal posts 26** and **30**.”), [0017] (“**RDLs 54** are then formed on dielectric layer 52 and connected to **RDLs [42]**.”). Given the mirror symmetry, in my opinion, the **unlabeled connectors** are just like **connectors 44**. And as Chen teaches, “[c]onnectors 44 may also include **metal pillars**, or **metal pillars** and solder caps.” EX1003 at [0014]. As such, it would have been obvious to a POSITA to utilize similar **metal pillars** as the **unlabeled connectors** just like **connectors 44**.

89. And using **metal pillars** as a means to electrically couple two different substrates together was well-known in the art. Similar to the '202 Patent, Sun concerns semiconductor packaging with a package-on-package configuration in which multiple integrated circuit packages are vertically stacked and electrically interconnected to achieve higher functional density within a reduced footprint. *See, e.g.,* EX1004, [0002] (“A package on package (PoP) comprises two electronic packages assembled in a vertical stack.”), [0041] (“FIG. 12 is a schematic view of a PoP assembly comprising first and second modules.”); EX1001, claim 1. Sun qualifies as analogous art at least because Sun resides within the same field of endeavor of semiconductor package-on-package structures as addressed by the '202 Patent. Sun is also analogous art because it is reasonably pertinent to the problem faced by the '202 Patent as it addresses methods of electrically interconnecting a top package substrate to a bottom package substrate using two intervening substrate structures to establish conductive pathways between stacked packages.

90. Similar to Chen, Sun describes a structure having a **first substrate 110** electrically coupled to a **third substrate 20** via an intermediate **second substrate 300**. *See* EX1004 at [0012] (“In one aspect of the present invention a (first) module is proposed comprising a **first substrate** and at least one chip mounted on the first substrate; a **second substrate** mounted to the **first substrate**

...; the **first substrate** being electrically connected to the **second substrate** by at least one **first electrical connector**; and at least **one second electrical connector** extending from the **second substrate** through the overmold and having an exposed end for electrical connection to an external module.”), [0022] (“Preferably the at least **one second electrical connector** is in electrical contact with a conducting contact of the **third substrate**.”). And in between the **third substrate 20** and the **second substrate 300**, electrical **connection 310** is depicted in Figure 12 of Sun, the details of which are further shown in Figure 14.

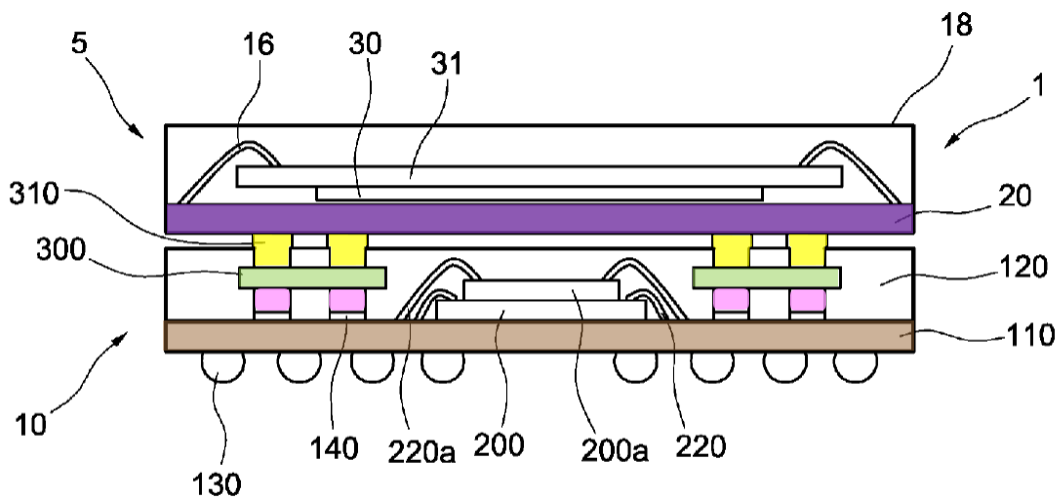
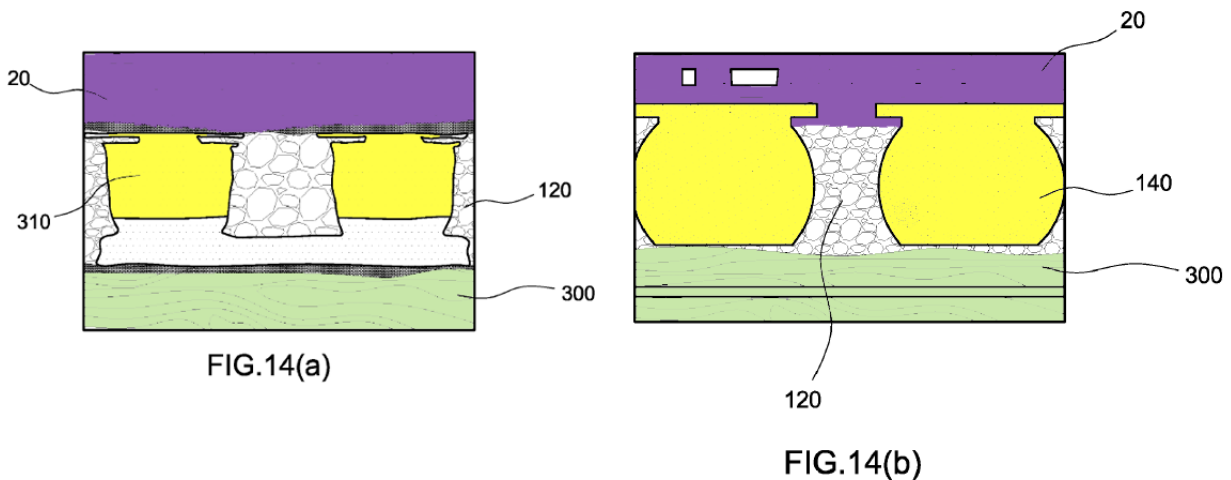


FIG.12

EX1004 at Figure 12.



EX1004 at Figure 14.

91. And Sun teaches that two possible well-known solutions are metal pillars, as illustrated in Figure 14(a) or solder, as illustrated in Figure 14b. *See* EX1004 at [0066] (“FIG. 14 (a) illustrates a pair of **second connectors 310**. They have the same structure as the first connectors 320. They are formed of **metal pillars**, preferably **copper pillars**. By way of contrast FIG. 14 (b) shows an arrangement with a pair of **solder balls 140** between a **substrate 20** and a **substrate 300**.”).

92. In fact, among these solutions, a POSITA would have been motivated to implement the **metal pillars** as a suitable solution instead of solder because Sun expressly teaches the advantages of employing **metal pillars** in lieu of alternative connector structures, such as solder. *See* EX1004 at [0066] (“FIG. 14 (a) illustrates a pair of **second connectors 310**. They have the same structure as the first

connectors 320. They are formed of **metal pillars**, preferably copper pillars. It can be seen that the pillars have fine pitch and a well defined shape. By way of contrast FIG. 14(b) shows an arrangement with a pair of solder balls 140 between a substrate 20 and a substrate 300. It can be seen that the solder balls have a less fine pitch and less well defined shape than the metal pillars. Furthermore, at typical processing temperatures (e.g. around 260 degrees Celsius) the solder balls will melt and collapse down, while the metal (e.g. copper) pillars will remain solid and well defined. *As a result, for a given stand off height, **metal pillars** provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates.* The **metal pillars** allow finer pitch and thus denser electrical connections. A small amount of solder or bonding pads may be used to connect the **metal pillars** to the respective other substrates.”).

- x. [1I] the **bottom package substrate** has, on a top surface thereof, a **plurality of top metal pillars** each coupled to a corresponding **metal pillar** among the **plurality of metal pillars** of the **spacer connector**,

93. In my opinion, Chen teaches [1I].

94. At the outset, Figure 9 shows Chen’s package-on-package structure. See EX1003 at [0004] (“FIGS. 1 through 9 are cross-sectional views and a top view of intermediate stages in the manufacturing of a Package-on-Package (PoP) structure in accordance with some exemplary embodiments.”).

95. Regardless of how the different components of the PoP structure were assembled, the **bottom package component 56** shown in Figure 9 has on its top surface **connectors 44** that are electrically coupled to the corresponding **through-substrate vias 32** and **metal posts 30** of the **TAV modules 28**. EX1003 at [0014] (“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and **connectors 44** are formed to connect to **metal posts 26** and **30**. ... **Connectors 44** may also include **metal pillars**, or **metal pillars** and solder caps, which may also be formed through plating.”).

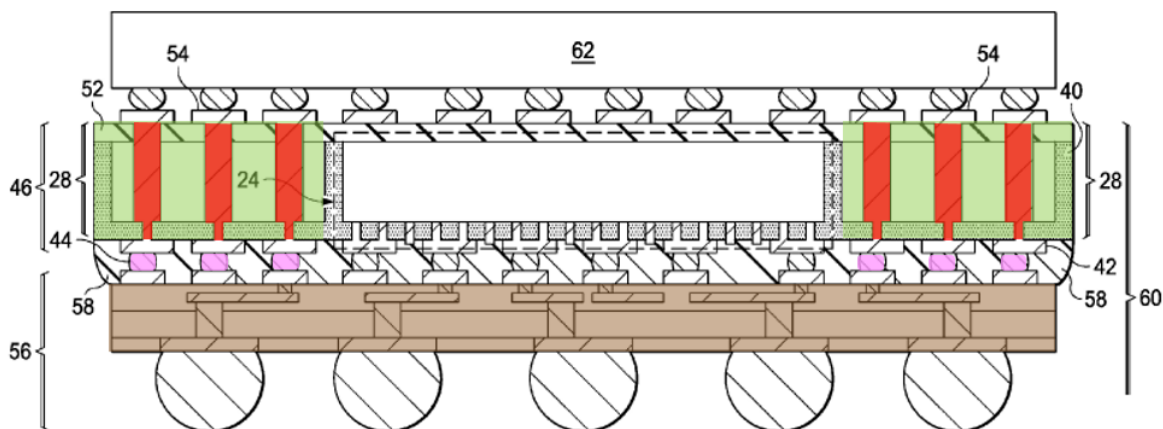


FIG. 9

EX1003 at Figure 9.

96. Chen also teaches that “[c]onnectors 44 may also include **metal pillars**, or **metal pillars** and solder caps, which may also be formed through plating.” EX1003 at [0014].

- xi. [1J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and

97. In my opinion, Chen in combination with Sun render obvious [1J].

98. Starting from the top of Figure 9, package component 62 is electrically coupled to the package component 56 by the following electrically conductive components: (1) unlabeled connectors that look like the connectors 44 on the opposite side of the TAV modules 28, (2) RDLs 54, (3) through-substrate vias 32 and metal posts 30 that pass through TAV modules 28, (4) RDLs 42, (5) connectors 44, and (6) the uppermost pads (uncolored) of package component 56. See EX1003 at [0019] (“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. ... In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.”), [0014] (“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30.”), [0017] (“RDLs 54 are then formed on dielectric layer 52 and connected to RDLs [42].”), claim 1 (“wherein the first plurality of RDLs is electrically coupled to the second plurality of RDLs through the plurality of through-vias in the TAV module”), claim 15 (“forming a first plurality of Redistribution Lines

(RDLs) over the polymer and connected to the metal posts of the device die and the metal posts of the TAV module, wherein the device die, the TAV module, and the first plurality of RDLs form a package”), claim 15 (“forming a second plurality of RDLs coupled to the plurality of through-vias, wherein the first [plurality of RDLs] and the second plurality of RDLs are on opposite sides of the package.”).

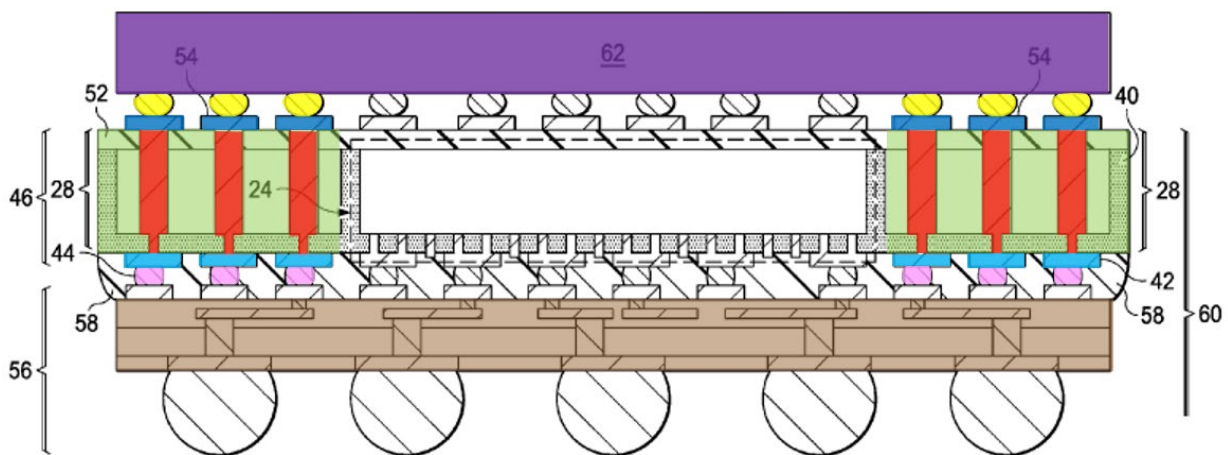


FIG. 9

EX1003 at Figure 9.

- xii. [1K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate,

99. In my opinion, Chen teaches [1K].

100. As shown in Figure 9, package component 24 is arranged in the space between the bottom package component 56 and the top package component 62. See EX1003 at [0019] (“In the resulting package, TAV modules

28 are used to electrically couple the circuit devices in **package component 62** to **package component 56.**")

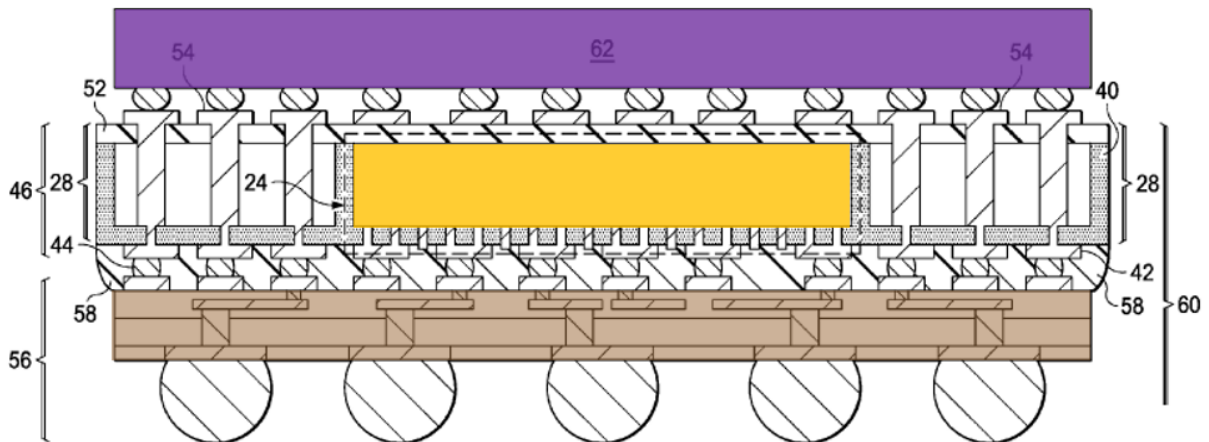


FIG. 9

EX1003 at Figure 9.

101. Chen also teaches that **package component 24** includes various **device dies**, such as a CPU die, memory die and the like. *See* EX1003 at [0009] (“In some embodiments, **package component 24** includes one or a plurality of **device dies**. For example, **package component 24** may include a **Central Computing Unit (CPU) die** or another type of logic die having logic circuits. In alternative embodiments, **package component 24** includes a plurality of **memory dies** stacked together (please refer to FIG. 11). In the embodiments wherein **package component 24** is a **device die**, package component 24 may include semiconductor substrate 25 and active devices (such as transistors) 27 at a top surface of semiconductor substrate 25.”).

102. These **device dies** meet the claimed “chip” because these two terms are often used interchangeably in the art, which a POSITA would have readily recognized. *See, e.g.*, EX1008 at [0007] (using the terms “integrated circuit (IC) **chip or die**” interchangeably).

xiii. [1L] wherein the **bottom chip is mounted to the top surface of the **bottom package substrate**,**

103. In my opinion, Chen teaches [1L].

104. As I illustrate below in Figure 9, **package component 24** is mounted on the top surface of the **bottom package component 56**. *See* EX1003 at [0014] (“Throughout the description, the structure including **package component 24**, TAV modules 28, and polymer 40 is referred to as **package 46**.”), [0018] (“Referring to FIG. 8, **package 46** is bonded to **package component 56** to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like.”).

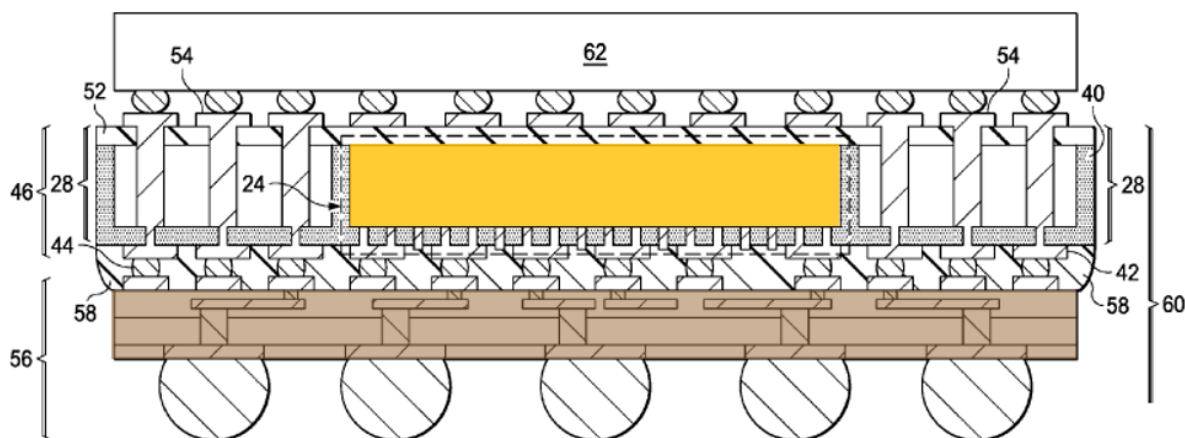


FIG. 9

EX1003 at Figure 9.

- i. [1M] the at least one **spacer connector** comprises two **spacer connectors** arranged on opposite sides of the **bottom chip**.

105. In my opinion, Chen teaches [1M].

106. Figure 2 below shows two **TAV modules 28** arranged on opposite sides of **package component 24**, which, as I explained above, includes **device dies** that meet the claimed “chip.” See EX1003 at [0012] (“FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, **TAV modules 28** are disposed on opposite sides of **package component 24**. Although two **TAV modules 28** are illustrated, there may be one or more than two **TAV modules 28**.”).

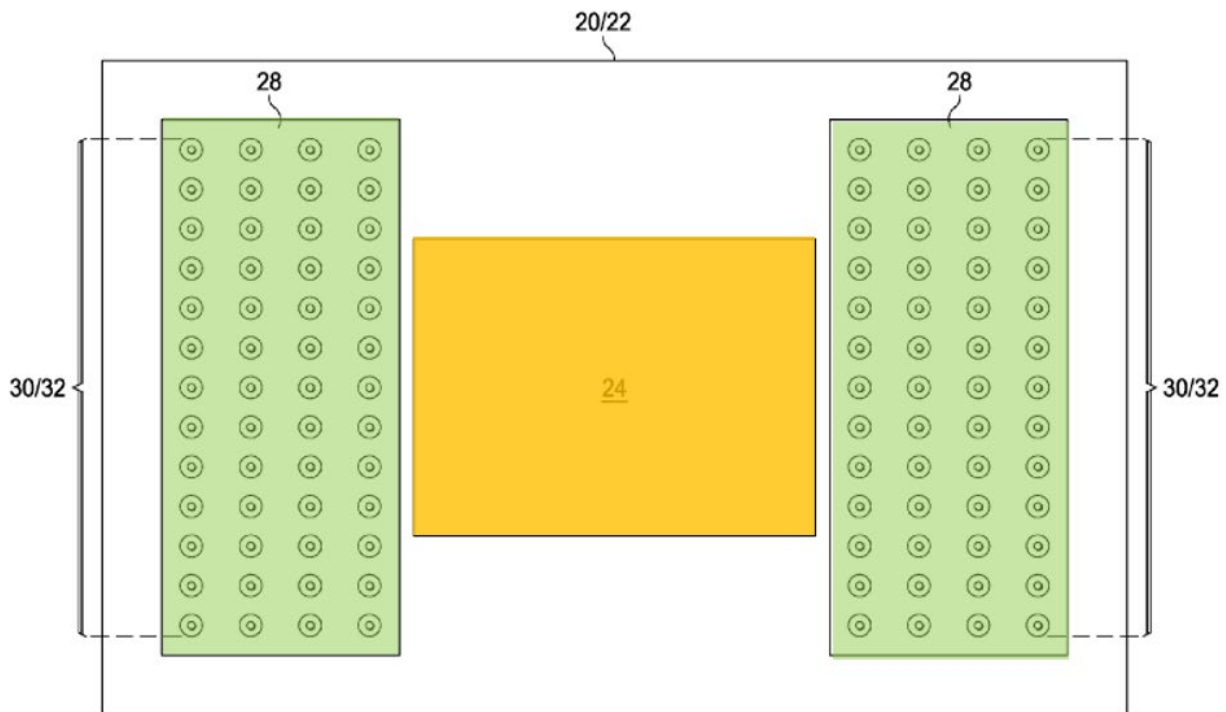


FIG. 2

EX1003 at Figure 2.

2. Dependent Claim 2

i. [2Pre] The structure of claim 1, wherein

107. As I explained above in paragraphs 61–106 in Ground I, in my opinion, Chen in combination with Sun render obvious the structure of claim 1.

ii. [2A] a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

108. In my opinion, Chen teaches [2A].

109. Figure 9 clearly shows that the top surface of the package component 24 is over and spaced downwardly from the bottom surface of top package

component 62. Chen additionally teaches that the **package component 62** is “over and aligned to” **package component 24**. *See also* EX1003 at [0020] (“FIG. 10 illustrates an exemplary embodiment wherein **package component 62** includes a plurality of stacked dies 64. In some embodiments, stacked dies 64 are memory dies. Stacked dies 64 may be bonded to RLDs 54 that are over and aligned to **package component 24**, which are further connected to the RDLs 54 over and aligned to TAV modules 28.”), [0014], [0018], [0019].

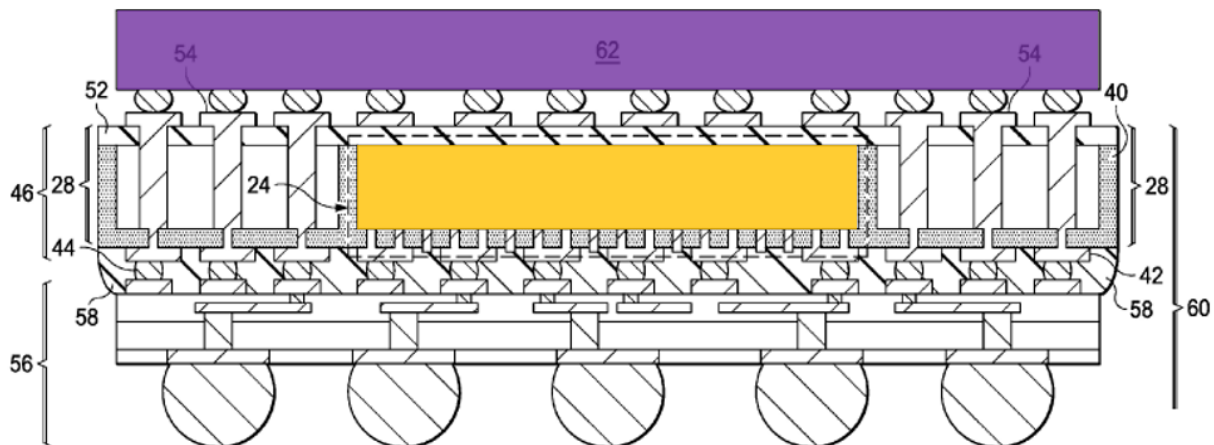


FIG. 9

EX1003 at Figure 9.

3. Dependent Claim 3

i. [3Pre] The structure of claim 2, further comprising:

110. As I explained above in paragraphs 107–109 in Ground I, in my opinion, Chen in combination with Sun render obvious the structure of claim 2.

ii. [3A] a top chip mounted to the top surface of the top package substrate,

111. In my opinion, Chen in combination with Sun render obvious [3A].

112. Chen teaches that “package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown).” EX1003 at [0019]. While a POSITA would have readily recognized that device die (not shown) would be bonded to the top surface of the package substrate (not shown), Chen does not explicitly teach it. But this is a well-known configuration that is routinely employed in the art.

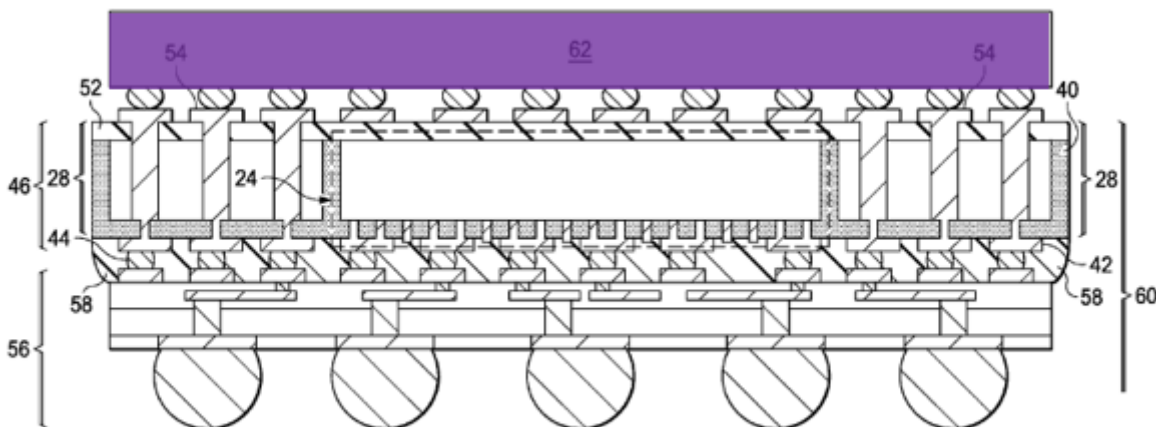


FIG. 9

EX1003 at Figure 9.

113. For example, as I explained in paragraphs 90–92 in Ground I with respect to [1H], Sun shows, in Figure 12, chips 30 and 31 that are mounted to the top surface of the third substrate 20. See EX1004 at [0059] (“The upper module 5 comprises a pair of chips 30, 31 mounted to a first (upper) side of a third

substrate 20. The **third substrate** may be a PCB, preferably a BT core substrate.

The **chips 30, 31** are electrically connected to the **third substrate 20** by wires or any other suitable means.”).

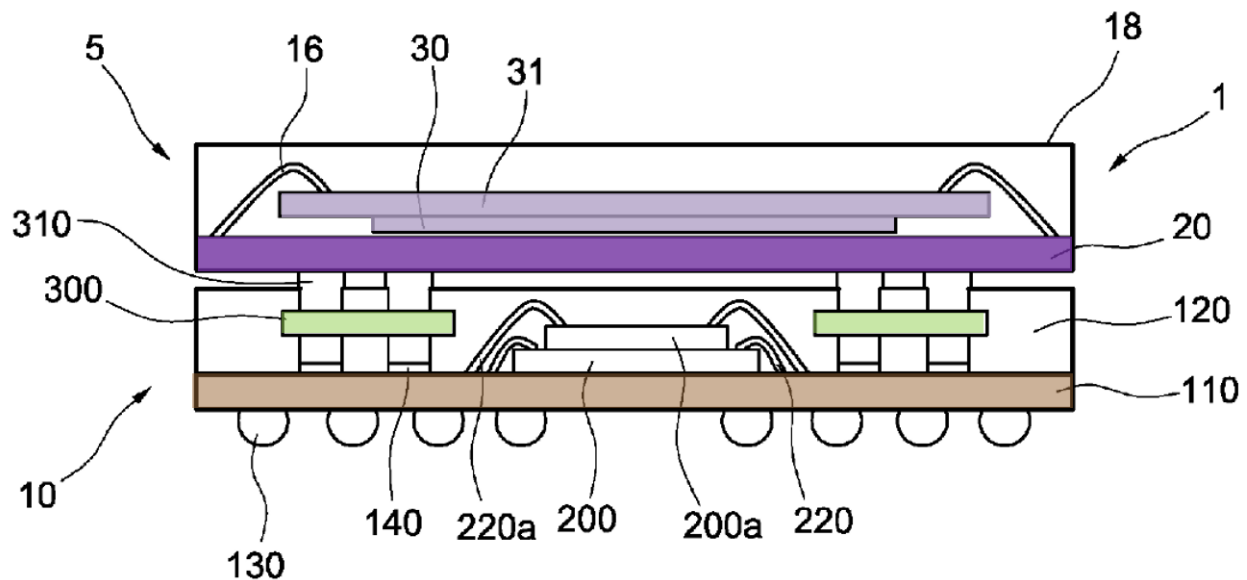


FIG.12

EX1004 at Figure 12.

114. There is nothing inventive about mounting Chen’s **device die (not shown)** on the top surface of the **package substrate** of Chen’s **package component 62**. A POSITA would have been able to mount Chen’s **device die (not shown)** on Chen’s **package substrate (not shown)** in the manner shown in Figure 12 of Sun with a reasonable expectation of success because it merely provides one particular configuration of placing a **device die** on a **package substrate**.

115. Alternatively, it would have been obvious to mount Sun's **chips 30 and 31** on Chen's **package substrate (not shown)** in the manner shown in Figure 12 of Sun with a reasonable expectation of success because it merely provides one other well-understood method of placing one or more **device dies** on a **package substrate**. Placing Chen's **device die (not shown)** or Sun's **chips 30 and 31** on the top of Chen's **package substrate (not shown)** represents the straightforward integration of known prior art components—namely, Chen's **device die (not shown)** or Sun's **chips 30 and 31** with Chen's **package substrate (not shown)**—implemented using established semiconductor assembly techniques, specifically by positioning Chen's **device die (not shown)** or Sun's **chips 30 and 31** onto the available top surface of Chen's **package substrate (not shown)**, to achieve the predictable and routine result of a semiconductor **die or chip** being placed on the top surface of a **package substrate** to enable electrical interconnection with other components within a stacked package configuration. Selecting the top surface of the **package substrate** as the mounting location would have at least constituted an obvious-to-try design choice from among a limited and well-defined set of feasible mounting surfaces—namely, the top or bottom surfaces of the **package substrate**—because a POSITA, familiar with conventional package assembly constraints and electrical routing considerations, would have immediately recognized that mounting **dies** to the lateral side surfaces of the **package substrate**

would be impractical and inefficient, and would have reasonably expected successful electrical and mechanical integration when selecting either of the planar major surfaces.

- iii. [3B] wherein in a direction in which the **top package substrate** is stacked on top of the **bottom package substrate**, the **top chip** overlaps the **bottom chip** and each of the two **spacer connectors**.

116. In my opinion, Chen in combination with Sun render obvious [3B].

117. Chen teaches that “**package component 62** is a package that includes a **device die (not shown)** bonded to a **package substrate (not shown)**.” EX1003 at [0019]. Chen also teaches that “[i]n some embodiments, **top package component 62** is a **device die**.” EX1003 at [0019]. In other words, Chen itself teaches that the **device die (not shown)** overlaps the **package component 24** and each of the two **TAV modules 28**.

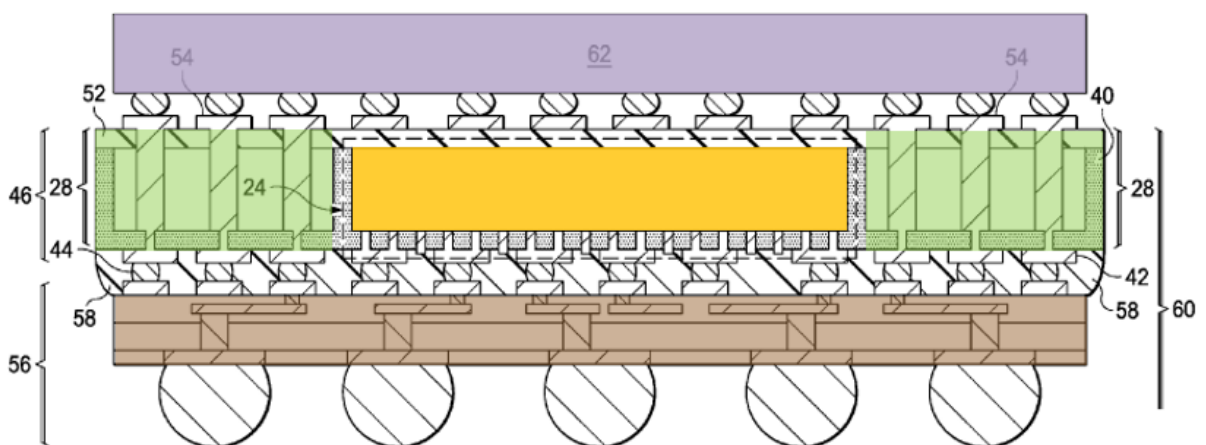


FIG. 9

EX1003 at Figure 9. *See also* EX1003 at [0020] (“FIG. 10 illustrates an exemplary embodiment wherein **package component 62** includes a plurality of **stacked dies 64**. In some embodiments, **stacked dies 64** are **memory dies**. **Stacked dies 64** may be bonded to RLDs 54 that are over and aligned to **package component 24**, which are further connected to the RDLs 54 over and aligned to **TAV modules 28.**”), [0014], [0018].

118. Sun also teaches that **chips 30 and 31** overlap the **chip 200** and each of the **second substrates 30**

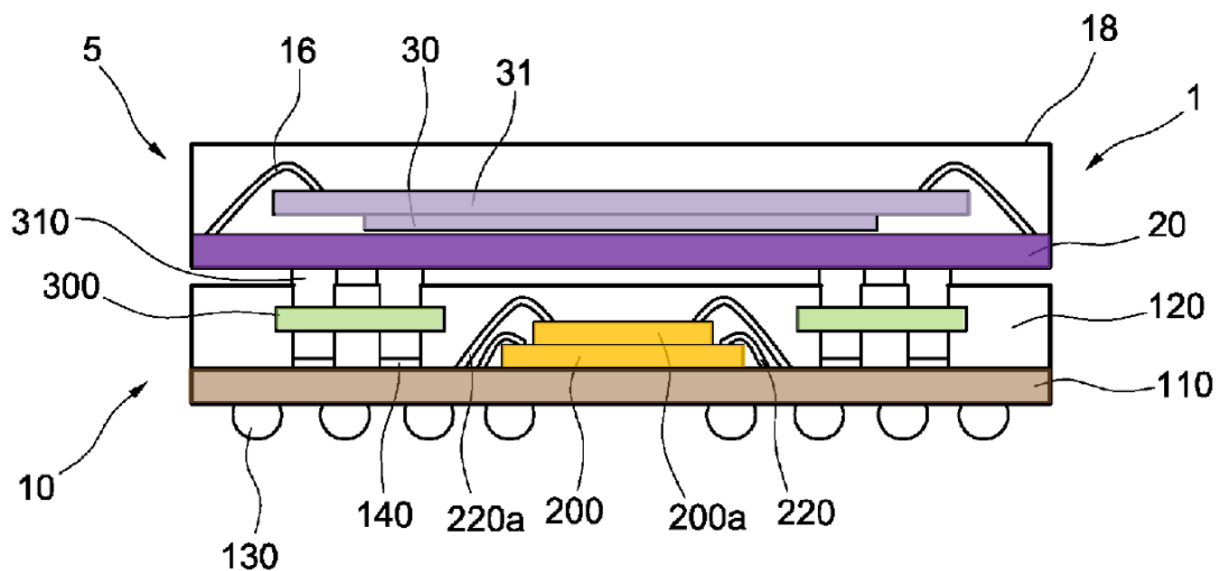


FIG.12

EX1004 at Figure 12.

119. Hence, based on the teachings of either Chen or Sun, in my opinion, a POSITA would have found it obvious to bond Chen's **device die (not shown)** or Sun's **chips 30 and 31** to Chen's **package substrate (not shown)** in any one of the configurations shown above, such as in Figure 9 of Chen or Figure 12 of Sun with a reasonable expectation of success, as I explained above in paragraphs 111–115 in Ground I with respect to [3A].

4. Dependent Claim 4

i. [4Pre] The structure of claim 1, wherein

120. As I explained above in paragraphs 61–106 in Ground I, in my opinion, Chen in combination with Sun render obvious the structure of claim 1.

ii. [4A] each **bottom metal pillar** among the **plurality of bottom metal pillars** of the **top package substrate** is aligned with a corresponding **metal pillar** among the **plurality of metal pillars** of the **spacer connector**, and with a corresponding **top metal pillar** among the **plurality of top metal pillars** of the **bottom package substrate**.

121. As I explained above in paragraphs 85–92 in Ground I with respect to [1H] and in paragraphs 93–96 in Ground I with respect to [1I], in my opinion, Chen in combination with Sun render obvious [4A].

122. The resulting structure is shown below demonstrating how [4A] is rendered obvious by the structure shown in Figure 9 of Chen, applying the teachings of Sun that it would have been obvious to utilize **metal pillars** as the

unlabeled connectors between the package component 62 and the TAV modules 28.

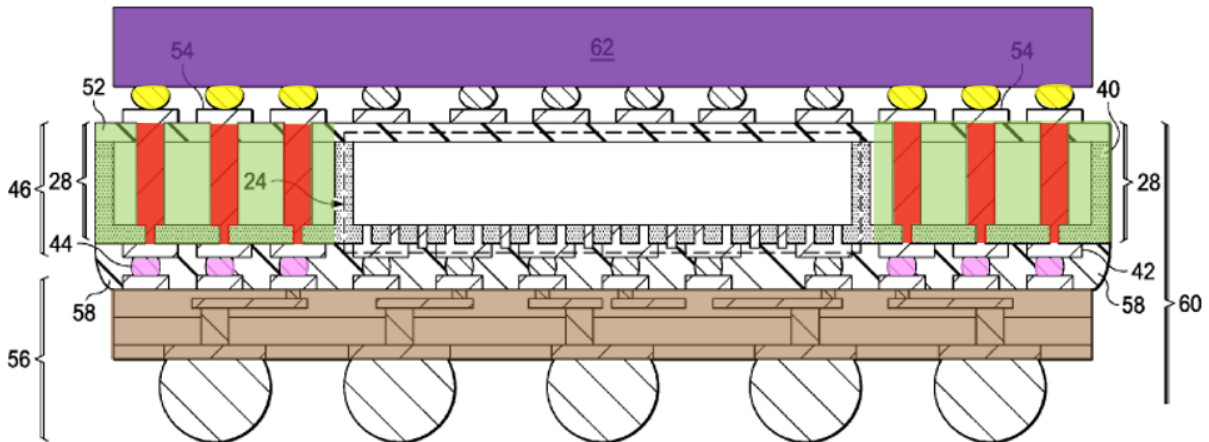


FIG. 9

EX1003 at Figure 9.

5. Dependent Claim 7

i. [7Pre] The structure of claim 4, wherein

123. As I explained above in paragraphs 120–122 in Ground I, in my opinion, Chen in combination with Sun render obvious the structure of claim 4.

ii. [7A] the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate, and

124. In my opinion, Chen teaches [7A].

125. Chen utilizes polymer 40 to fill in the gaps between various different components. See EX1003 at [0013] (“Referring to FIG. 3, polymer 40 is molded on package component 24 and TAV modules 28. Polymer 40 fills the gaps between package component 24 and TAV modules 28, and may be in contact with

release layer 22. Furthermore, **polymer 40** is filled into the gaps between metal posts 26, and into the gaps between metal posts 30. **Polymer 40** may include a molding compound, a molding underfill, or a kind of epoxy. The top surface of **polymer 40** may be level with or higher than the top surfaces of metal posts 26 and 30.”). A POSITA would have readily understood that a polymer layer would be a dielectric layer. *See, e.g.*, EX1011, [0056] (discussing an “insulating layer 144 contain[ing] ... polymer dielectric”). And as shown in Figure 9, a layer of **polymer 40** is formed on the bottom surface of the **substrate 44**.

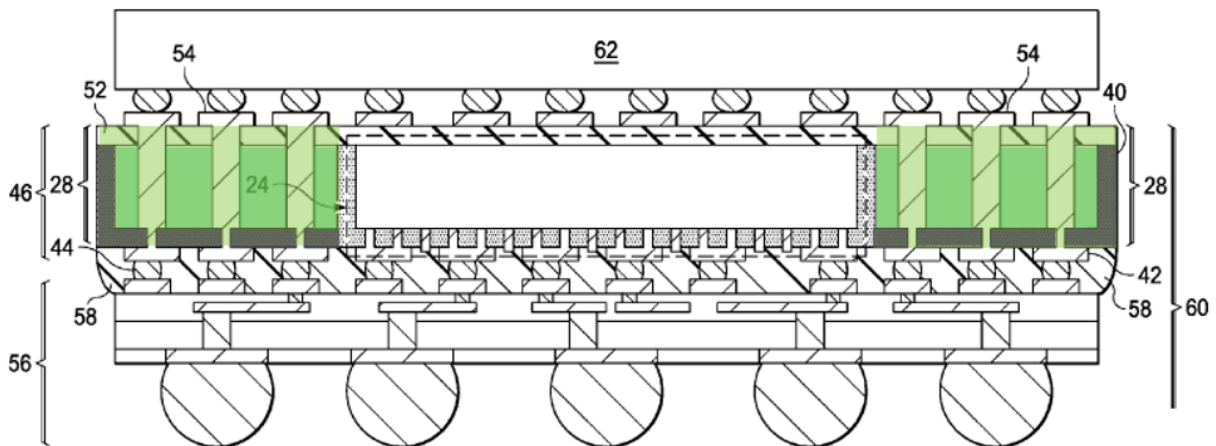


FIG. 9

EX1003 at Figure 9.

- iii. [7B] the **plurality of metal pillars** pass through the **core substrate** and the **dielectric layer**.

126. In my opinion, Chen teaches [7B].

127. As shown in Figure 9, Chen's **through-substrate vias 32** and **metal posts 30** pass through the **substrate 34** and **polymer 40**.

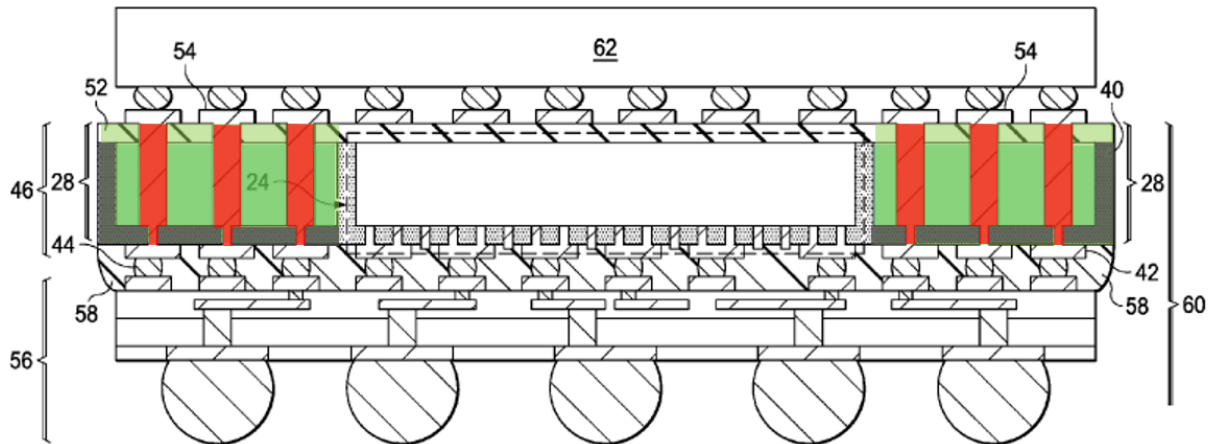


FIG. 9

EX1003 at Figure 9. See EX1003 at [0010] (“**Through-substrate vias 32** are formed in **substrate 34** for inter-coupling the conductive features on opposite sides of **substrate 34**. **Through-substrate vias 32** are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like. In some embodiments, bottom ends 32A of **through-substrate vias 32** are level with the bottom surface 34A of **substrate 34**. Accordingly, bottom ends 32A of **through-substrate vias 32** may be in contact with release layer 22. TAV modules 28 may also include **metal posts 30** (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of **metal post 26** and **30** are substantially level with each other.”), [0013] (“Referring to FIG. 3, **polymer 40** is molded on package component 24 and TAV modules 28. **Polymer 40** fills the gaps between package

component 24 and TAV modules 28, and may be in contact with release layer 22. Furthermore, **polymer 40** is filled into the gaps between metal posts 26, and into the gaps between **metal posts 30**. **Polymer 40** may include a molding compound, a molding underfill, or a kind of epoxy. The top surface of **polymer 40** may be level with or higher than the top surfaces of **metal posts 26** and **30**. A grinding step may be performed to grind **polymer 40**, until **metal posts 26** and **30** are exposed.”).

6. Dependent Claim 8

i. [8Pre] The structure of claim 7, wherein

128. As I explained above in paragraphs 123–127 in Ground I, in my opinion, Chen in combination with Sun render obvious the structure of claim 7.

ii. [8A] the dielectric layer is a dielectric adhesive in which the core substrate is pasted.

129. In my opinion, Chen teaches [8A].

130. Chen teaches that “[p]olymer 40 may include a molding compound, a molding underfill, or **a kind of epoxy**.” EX1003 at [0013]. A POSITA would have readily recognized that epoxy is both a dielectric, because it is not conductive, and an adhesive that is routinely utilized in integrated circuit fabrication. For example, U.S. Patent Application Publication No. 2011/0159284 provides numerous examples of epoxy resins that function as a dielectric adhesive. *See*

EX1009 at [0036] (“The epoxy resin may have a high cross-linking density, e.g., sufficient to exhibit strong curing and adhesive functions. Curing density of the epoxy resin may be controlled by mixing a difunctional epoxy resin with polyfunctional epoxy resins to ensure that an adhesive prepared from the adhesive composition has a low shear viscosity even after curing. The difunctional epoxy resin may be present in an amount of about 20 to about 60 parts by weight, based on 100 parts by weight of the epoxy resin.”), [0037] (“The difunctional epoxy resin may include, e.g., bisphenol F, bisphenol A, and/or bisphenol AD epoxy resins. For example, a bisphenol F epoxy resin, such as YSLV-80XY commercially available from Kukdo Chemical Co., Ltd., may be used as the difunctional epoxy resin. The difunctional epoxy resin may be included in the adhesive composition to maintain a low viscosity of the adhesive prepared from the adhesive composition even after semi-curing. Other examples of the difunctional epoxy resin may include: Epicoat 807, Epicoat 827 and Epicoat 828, which are commercially available from Yuka Shell Epoxy Co., Ltd.; D.E.R 330, D.E.R. 331 and D.E.R. 361, which are commercially available from Dow Chemical; and YD128 and YDF 170, which are commercially available from Tohto Kasei Co., Ltd.”).

131. Chen also teaches the latter portion of [8A]—“in which the **core substrate** is pasted.” As I explained in my explanation of the file history in paragraphs 42–49, the Examiner rejected this limitation based on a prior art

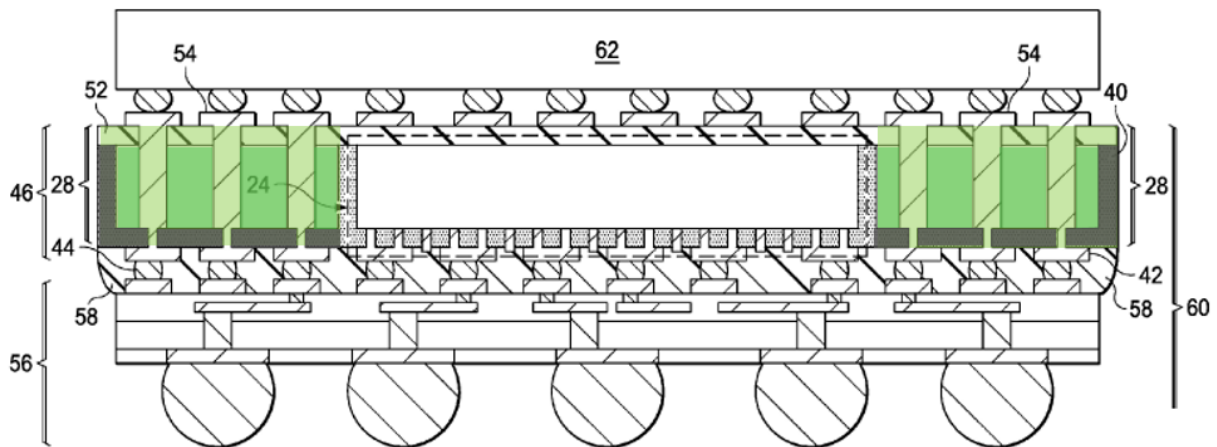


FIG. 9

EX1003 at Figure 9.

7. **Dependent Claim 9**

i. **[9Pre] The structure of claim 4, wherein**

133. As I explained above in paragraphs 120–122 in Ground I, in my opinion, Chen in combination with Sun render obvious the structure of claim 4.

ii. **[9A] the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars,**

134. In my opinion, Chen teaches [9A].

135. As shown in Figure 9, the bottom end of **metal posts 30** include **RDLs 54**.

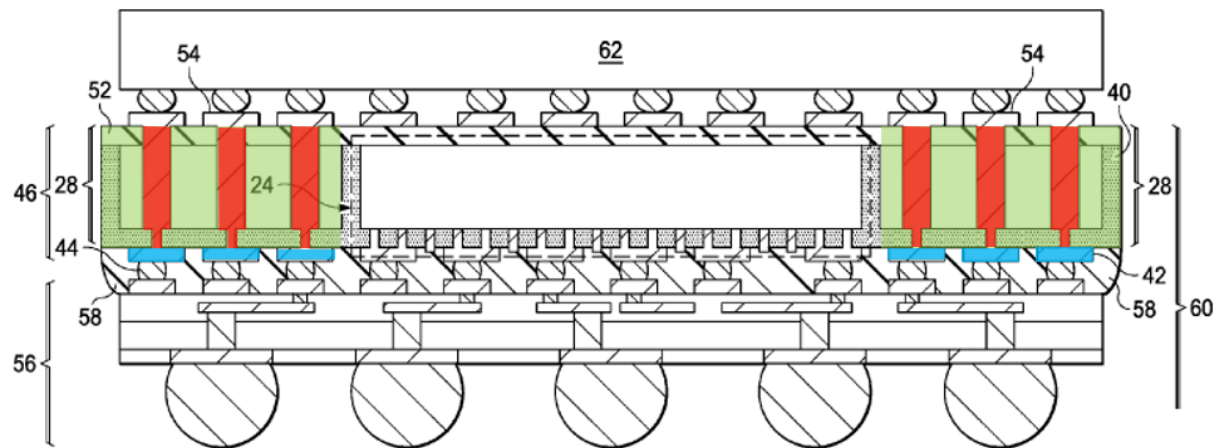


FIG. 9

EX1003 at Figure 9. See EX1003 at [0014] (“Next, referring to FIG. 4, **Redistribution Lines (RDLs) 42** and connectors 44 are formed to connect to **metal posts 26 and 30**. As indicated by dashed lines, **RDLs 42** may also interconnect **metal posts 26 and 30**. **RDLs 42** may be formed by depositing a metal layer, and then patterning the metal layer.”).

- iii. [9B] the bottom ends of the **plurality of metal pillars** are connected to corresponding top ends of the **plurality of top metal pillars** of the **bottom package substrate** via the corresponding **bottom metal pads** of the **spacer connector**, and

136. In my opinion, Chen teaches [9B].

137. First, as I explained above in paragraphs 93–96 in Ground I with respect to [1I], Chen teaches that “[c]onnectors 44 may also include **metal pillars**, or **metal pillars** and solder caps, which may also be formed through plating.” EX1003 at [0014].

138. And as shown in Figure 9, the top ends of the **connectors 44** are connected to the bottom ends of the **metal posts 30** via the corresponding **RDLs 42** located on the bottom of the **TAV modules 28**. EX1003 at [0014] (“Next, referring to FIG. 4, **Redistribution Lines (RDLs) 42** and **connectors 44** are formed to connect to **metal posts 26** and **30**. As indicated by dashed lines, **RDLs 42** may also interconnect **metal posts 26** and **30**. **RDLs 42** may be formed by depositing a metal layer, and then patterning the metal layer.”), [0019] (“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. ... In the resulting package, **TAV modules 28** are used to electrically couple the circuit devices in package component 62 to **package component 56**.”).

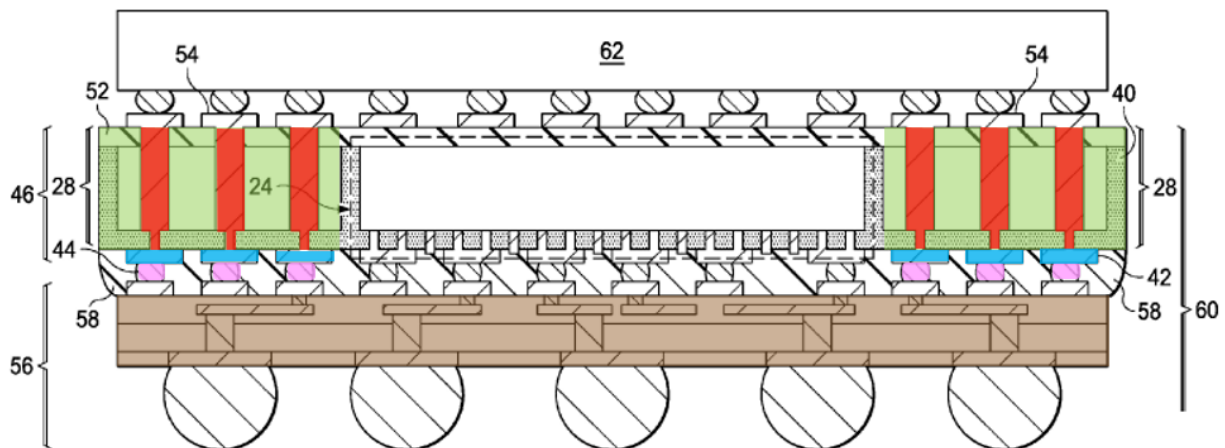


FIG. 9

EX1003 at Figure 9.

- iv. [9C] bottom ends of the **plurality of bottom metal pillars** of the **top package substrate** are connected to the corresponding top ends of the **plurality of metal pillars** of the **spacer connector** via the corresponding **top metal pads** of the **spacer connector**.

139. As I explained above in paragraphs 78–81 in Ground I with respect to [1F] and paragraphs 85–92 in Ground I with respect to [1H], in my opinion, Chen in combination with Sun render obvious [9C].

140. The resulting structure is shown below demonstrating how [9C] is rendered obvious by the structure shown in Figure 9 of Chen, applying the teachings of Sun that it would have been obvious to utilize **metal pillars** as the **unlabeled connectors** that connect to the top ends of the **through-substrate vias** **32** via the corresponding **RDLs 54**.

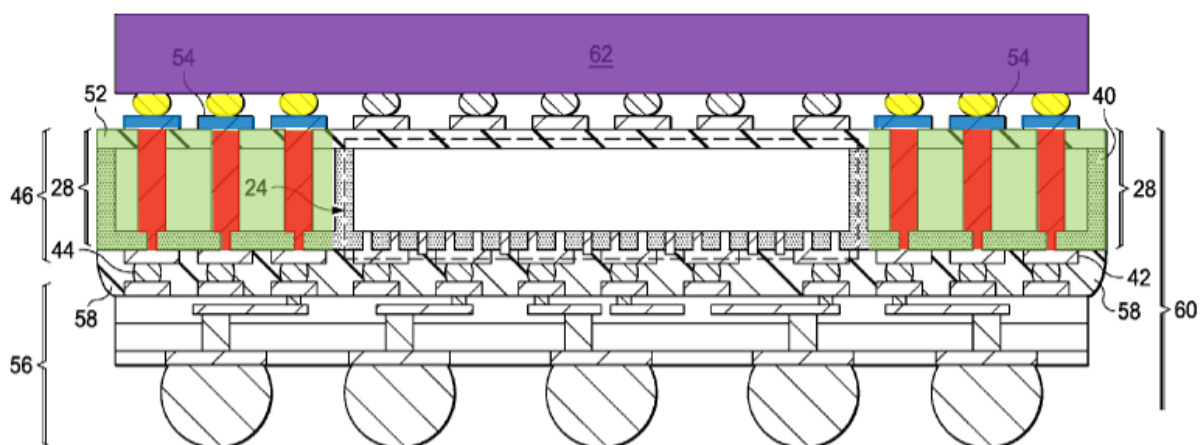


FIG. 9

EX1003 at Figure 9.

B. Ground II: Claims 5–6 Are Rendered Obvious By Chen In View Of Sun And Furuta

1. Dependent Claim 5

i. [5Pre] The structure of claim 4, wherein

141. As I explained above in paragraphs 120–122 in Ground I, in my opinion, Chen in combination with Sun render obvious the structure of claim 4.

ii. [5A] the **spacer connector is free of **metal pads** on the bottom ends of the **plurality of metal pillars** protruding downwardly from the bottom surface of the **core substrate**, and each **metal pillar** among the **plurality of metal pillars** and the corresponding **top metal pad** of the **spacer connector** form a T shape.**

142. In my opinion, Chen in combination with Sun and Furuta render obvious [5A].

143. Although Chen utilizes **RDLs 42** between the **connectors 44** and the **metal posts 30** that protrude downwardly from the bottom surface of **substrate 34**, it would have been obvious to make such a connection without the **RDLs 42**.

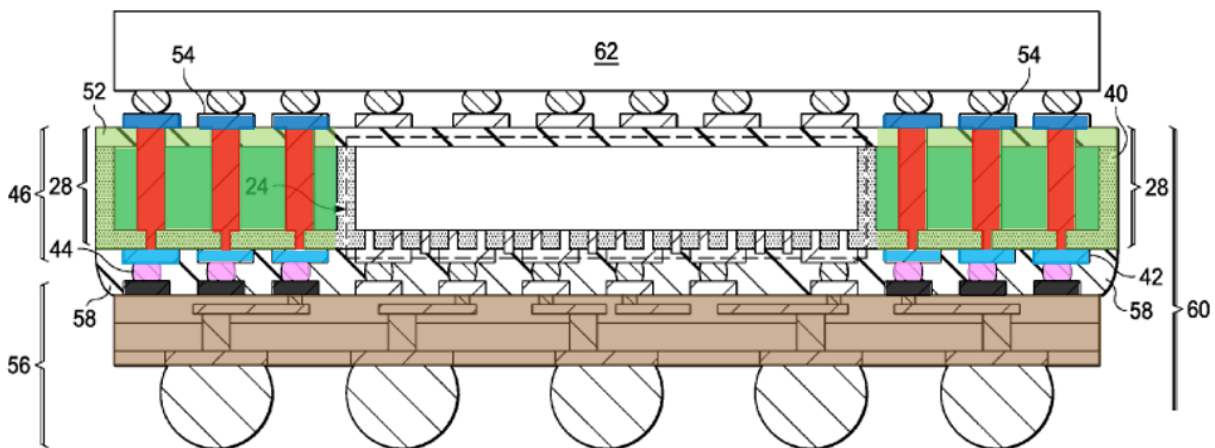


FIG. 9

EX1003 at Figure 9.

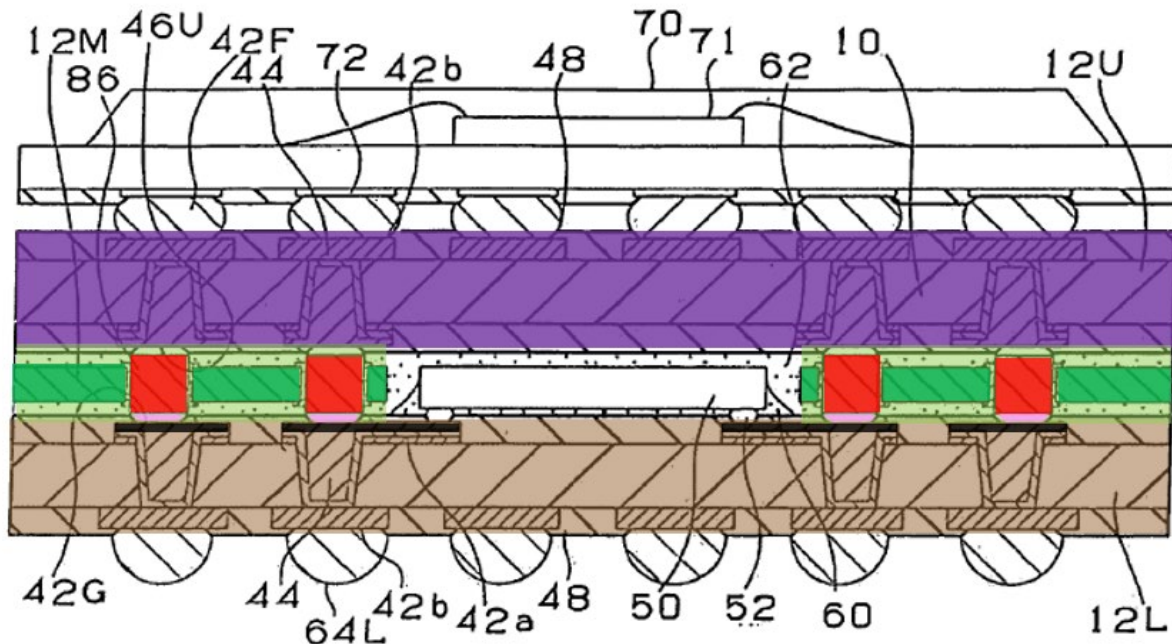
144. Similar to the '202 Patent, Furuta concerns semiconductor packaging with a package-on-package configuration in which multiple integrated circuit packages are vertically stacked and electrically interconnected to achieve higher functional density within a reduced footprint. *See, e.g.,* EX1006 at [0003] (“The present invention relates to a combination substrate on which to mount a package substrate with a mounted semiconductor element; especially to a combination substrate where the package substrate and a substrate are electrically connected in a POP (Package On Package) structured with at least two substrates.”). Furuta qualifies as analogous art at least because Furuta resides within the same field of endeavor of semiconductor package-on-package structures as addressed by the '202 Patent. Furuta is also analogous art because it is reasonably pertinent to the problem faced by the '202 Patent as it addresses methods of electrically

interconnecting a top package substrate to a bottom package substrate using two intervening substrate structures to establish conductive pathways between stacked packages. See EX1001, claim 1 (“the top package substrate is electrically coupled to the bottom package substrate through... the spacer connector...”).

145. Just like Chen’s package-on-package structure, Furuta a **upper substrate 12U-on-lower substrate 12L** structure that is electrically connected to each other using an **interposer 12M**. See EX1006 at [0020] (“FIG. 6(A) shows a cross-sectional view of combination substrate 10 according to Example 1. Combination substrate 10 is structured with **upper substrate (12U)**, **interposer (12M)** as an intermediate and **lower substrate (12L)**.”).

FIG. 6

(A)



EX1006 at Figure 6.

146. The **metal posts 86** running through the **interposer 12M** electrically couple the **upper substrate 12U** and **lower substrate 12L**. See EX1006 at [0021] (“**Metal posts 86** are formed, for example, of copper or copper alloy.”), [0023] (“In combination substrate 10 according to Example 1, through **posts 86** fitted into through-holes 82 in **interposer (12M)**, connection pads (42G) on **lower substrate (12L)** and connection pads (42F) on **upper substrate (12U)** are electrically connected.”).

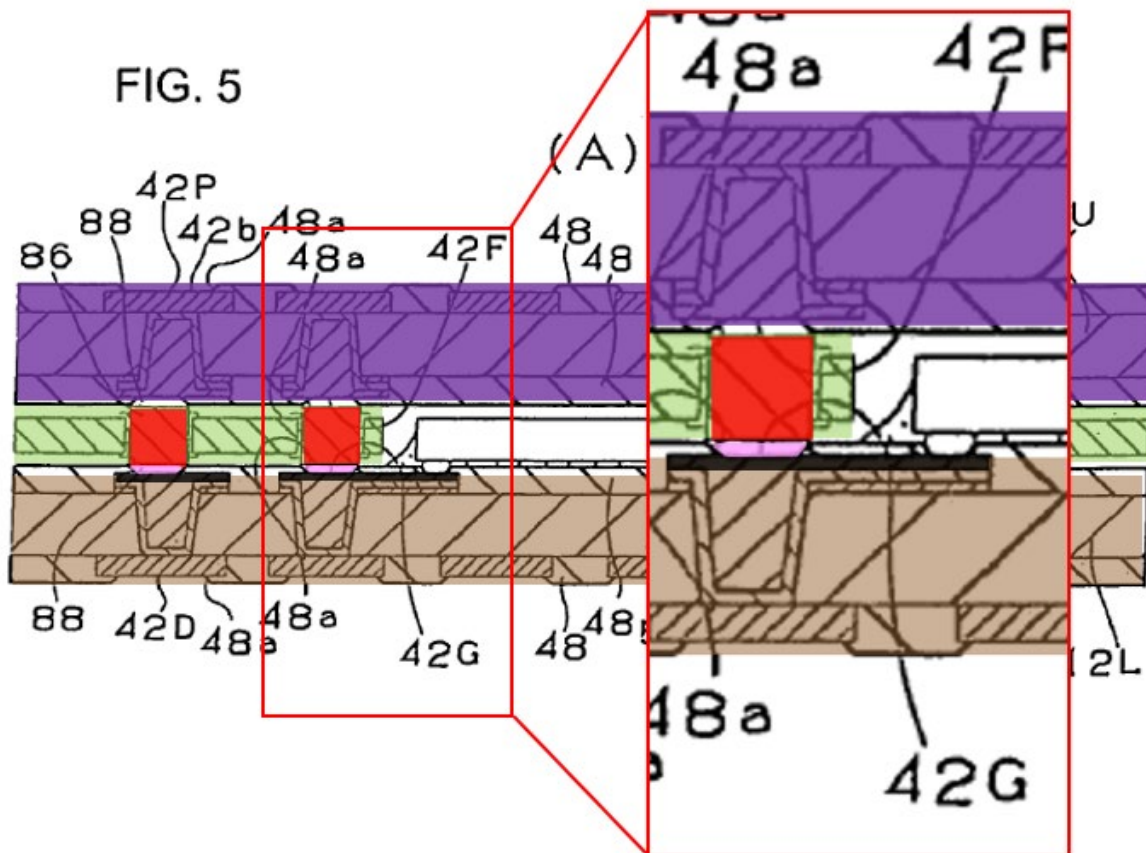
147. Much like Chen's **through-substrate vias 32** and **metal posts 30** that protrude downwardly from the bottom surface of **substrate 34**, Furuta's **metal posts 86** similarly protrude downwardly from the bottom surface of the **insulative substrate 80**. See EX1006 at [0037] ("The pierced implant material is inserted in openings 82 of **insulative substrate 80** prepared above, then pounded in. Accordingly, **conductive members (metal posts) 86** penetrating the **insulative substrate** are formed (FIG. 4(D)). Then, the implant material is separated and the height of **posts 86** protruding beyond **insulative substrate 80** is aligned. In doing so, **insulative substrate 80**, which is **interposer (12M)**, obtains **conductive members (posts) 86**, *which enable electrical connection between the top and bottom*, and whose heights protruding beyond **insulative substrate 80** are substantially the same.").



EX1006 at Figure 4D.

148. But unlike Chen, which forms **RDLs 42** on the bottom of **metal posts 30**, Furuta does not form any **metal pads** on the bottom of **metal posts 86**. Rather, **adhesive agent 88** that may be a "**solder or the like**" is formed between the bottom of **metal posts 86** and **pads (42G)** that are on the top surface of the **lower**

substrate (12L), which is similar to the **unlabeled pads** formed below **connectors 44** in Figure 9 of Chen. See EX1006 at [0038] (“**Circuit (pads) (42G)** of **lower substrate (12L)**, **posts 86** of **interposer (12M)** and circuit (pads) (42F) of upper substrate (12U) are aligned (FIG. 5(A)). Here, **circuit portions (42G)** of **lower substrate (12L)** come in contact with **posts 86** of **interposer (12M)**; ... **Posts 86** of **interposer (12M)** and **conductive layers (42G, 42F)** of each substrate may be connected using **solder or the like as conductive adhesive agent 88.**”).



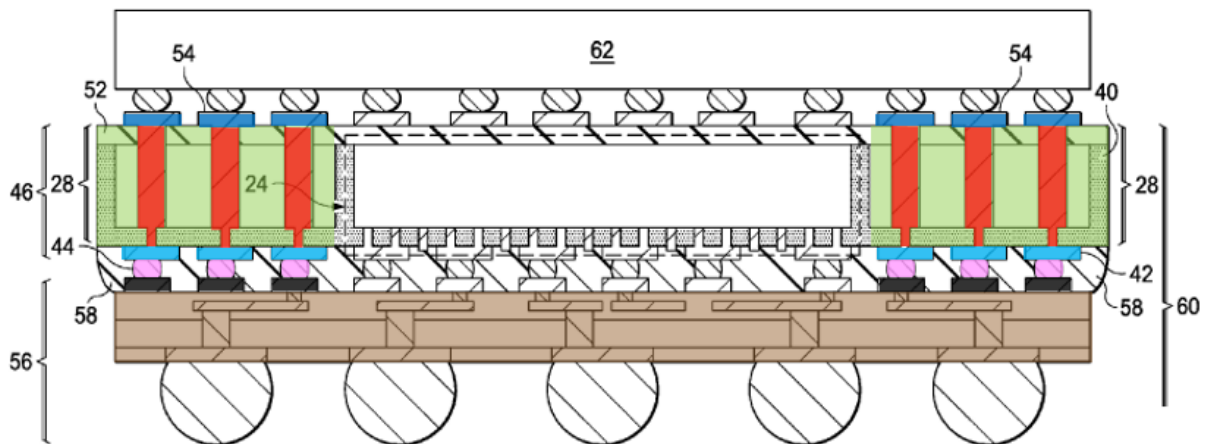


FIG. 9

EX1003 at Figure 9.

149. Indeed, Furuta teaches the desirability of removing such **RDLs 42** in Chen making a direct electrical connections between **metal posts** and **connectors 44** can lead to a number of benefits. See EX1006 at [0023] (“Accordingly, it is possible to obtain connection through **posts 86** with a smaller diameter than solder bumps, and thus wiring may be arranged with a **fine pitch**. Also, since **uniformly manufactured posts 86** are used, unlike solder bumps of varying sizes, **heat is generated uniformly, thus high temperatures in spots may seldom be generated**. Moreover, since **interposer (12M)** lies in between, the height between **upper substrate (12U)** and **lower substrate (12L)** may be adjusted, **making it easier to secure electrical connectivity and reliability.**”).

150. I have graphically represented such a structure that removes **RDLs 42**. As shown, the combination of **RDLs 54**, **through substrate vias 32**, and **metal posts 30** form a T shape which electrically connects to **connectors 44**.

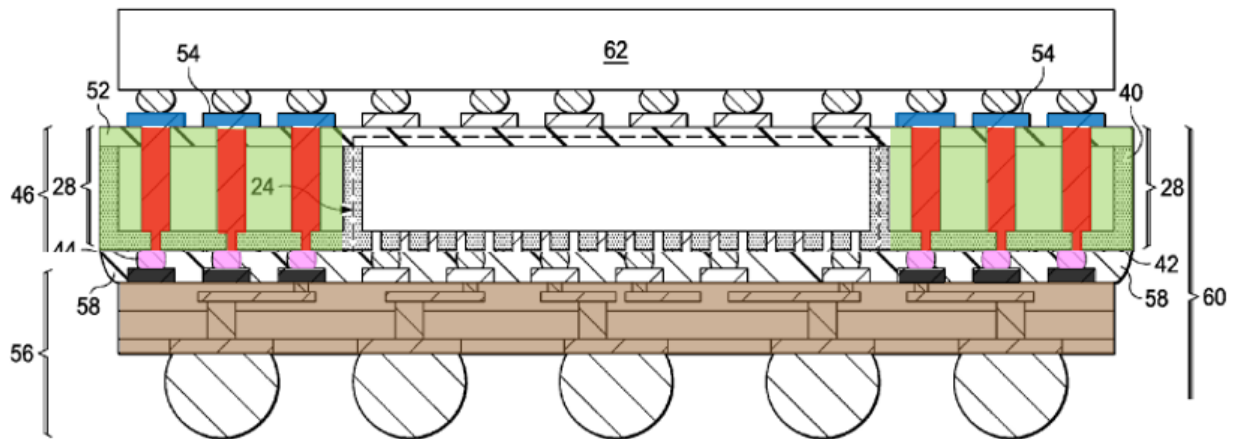


FIG. 9

EX1003 at Figure 9 (as modified with Sun and Furuta).

151. And removing just one of the RDLs (i.e., **RDLs 42**), and not both (i.e., not **RDLs 54**), would have been a routine design choice that would have been obvious to try depending on the particular design constraints. For example, the **metal posts 30** of Chen are significantly thinner than the **through-substrate vias 32**, which in certain instances may lead to additional requirements of improved manufacturability and reliability, which Furuta teaches may have been achievable by making a direct connection between **metal posts 30** and **connectors 44**. Accordingly, a POSITA would have been able to readily make the modification with a reasonable expectation of success.

2. Dependent Claim 6

i. [6Pre] The structure of claim 4, wherein

152. As I explained above in paragraphs 120–122 in Ground I, in my opinion, Chen in combination with Sun render obvious the structure of claim 4.

ii. [6A] the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

153. In my opinion, Chen in combination with Sun and Furuta render obvious [6A] for at least the reasons I stated in paragraphs 141–151 in Ground II with respect to [5A] and paragraphs 85–92 in Ground I with respect to [1H] to obtain a structure that I explained with respect to [5A].

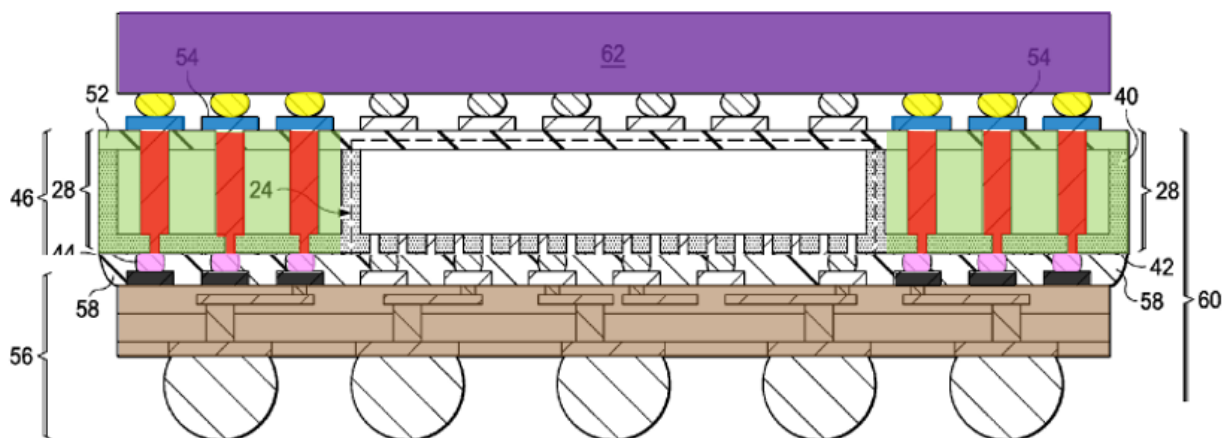


FIG. 9

EX1003 at Figure 9 (as modified with Sun and Furuta).

C. Ground III: Claims 1–4 and 7–9 Are Rendered Obvious By Chen In View Of Wu

1. Independent Claim 1

i. [1Pre] A structure, comprising:

154. As I explained above in paragraphs 61–63 in Ground I with respect to [1Pre], in my opinion, Chen teaches [1Pre].

ii. [1A] a bottom package substrate;

155. As I explained above in paragraphs 64–65 in Ground I with respect to [1A], in my opinion, Chen teaches [1A].

iii. [1B] a top package substrate stacked on top of the bottom package substrate;

156. As I explained above in paragraphs 66–67 in Ground I with respect to [1B], in my opinion, Chen teaches [1B].

iv. [1C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate,

157. As I explained above in paragraphs 68–71 in Ground I with respect to [1C], in my opinion, Chen teaches [1C].

- v. [1D] wherein the **spacer connector** comprises a **core substrate**;

158. As I explained above in paragraphs 72–74 in Ground I with respect to [1D], in my opinion, Chen teaches [1D].

- vi. [1E] a **plurality of metal pillars**, each passing through the **core substrate**;

159. As I explained above in paragraphs 75–77 in Ground I with respect to [1E], in my opinion, Chen teaches [1E].

- vii. [1F] a **plurality of top metal pads**, each on a top end of a corresponding **metal pillar** among the **plurality of metal pillars**;

160. As I explained above in paragraphs 78–80 in Ground I with respect to [1F], in my opinion, Chen teaches [1F].

161. At a minimum, as I explained above in paragraph 81 in Ground I with respect to [1F], in my opinion, Chen renders obvious [1F].

- viii. [1G] wherein a bottom end of each **metal pillar** among the **plurality of metal pillars** protrudes downwardly from a bottom surface of the **core substrate**;

162. As I explained above in paragraphs 82–84 in Ground I with respect to [1G], in my opinion, Chen teaches [1G].

- ix. [1H] the **top package substrate** has, on a bottom surface thereof, a **plurality of bottom metal pillars** each coupled to a corresponding **metal pillar** among the **plurality of metal pillars** of the **spacer connector**,

163. In my opinion, Chen in combination with Wu render obvious [1H].

164. As I explained above in paragraphs 86–89 in Ground I with respect to [1H], Figure 9 of Chen shows **package component 62** and **package component 56** that are **electrically coupled** to each other by a series of electrically conductive components. Starting from the top, Figure 9 of Chen shows **unlabeled connectors**, **RDLs 54**, **through-substrate vias 32**, **metal posts 30**, **RDLs 42**, and **connectors 44**, which “may also include **metal pillars**, or **metal pillars** and solder caps,” all being electrically connected to each other. *See* EX1003 at [0014], [0019], [0017], claim 1, claim 15.

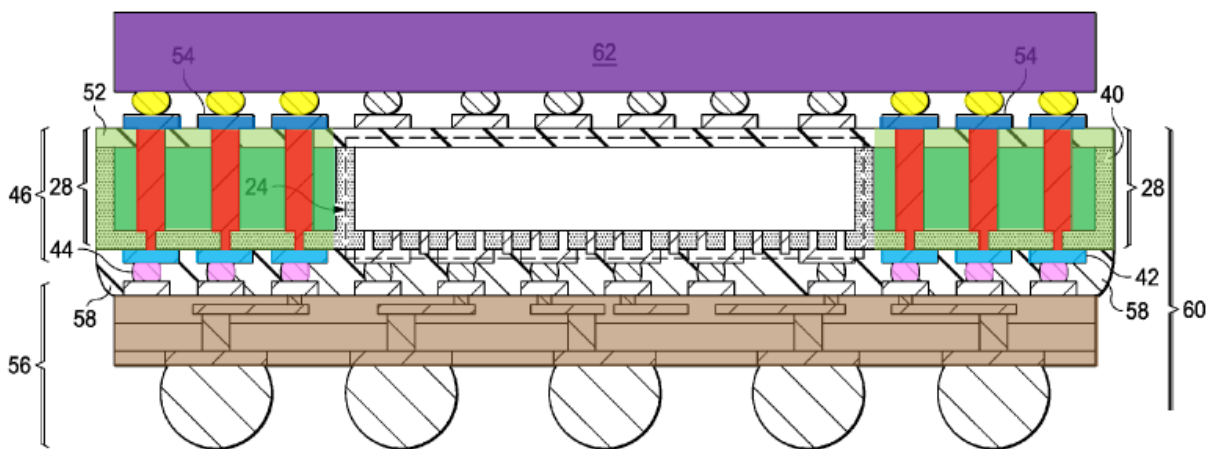


FIG. 9

EX1003 at Figure 9.

165. But Chen does not explicitly state the **unlabeled connectors**—despite appearing nearly identical to **connectors 44** on the opposite side of the **TAV modules 28**—are metal pillars. But a POSITA would have understood that it would have been obvious to use **metal pillars** as the **unlabeled connectors**.

166. Similar to the '202 Patent, Wu concerns semiconductor packaging with a package-on-package configuration in which multiple integrated circuit packages are vertically stacked and electrically interconnected to achieve higher functional density within a reduced footprint. *See, e.g.*, EX1005, Title (“Package-on-package structure with organic interposer.”), [0005] (“FIGS. 1 through 7 are cross-sectional views illustrating intermediate steps of a process for forming package-on-package structures”); EX1001, claim 1. Wu qualifies as analogous art at least because Wu resides within the same field of endeavor of semiconductor package-on-package structures as addressed by the '202 Patent. Wu is also analogous art because it is reasonably pertinent to the problem faced by the '202 Patent as it addresses methods of electrically interconnecting a top package substrate to a bottom package substrate using an intervening substrate structure to establish conductive pathways between stacked packages. *See* EX1001, claim 1 (“the top package substrate is electrically coupled to the bottom package substrate through... the spacer connector...”).

167. Figure 7 of Wu shows a top **package 702** that includes a **package substrate 706** that is electrically connected to an **interposer 402** using **package connectors 704**. *See* EX1005 at [0030] (“FIG. 7 is a cross-sectional view illustrating mounting a **package 702** on the **interposer 402** according to some embodiments. ... The **connectors 704** electrically connect the lands 412 on the top

surface of the **interposer 402** to the lands 716 on the bottom surface of the **package 702**.”).

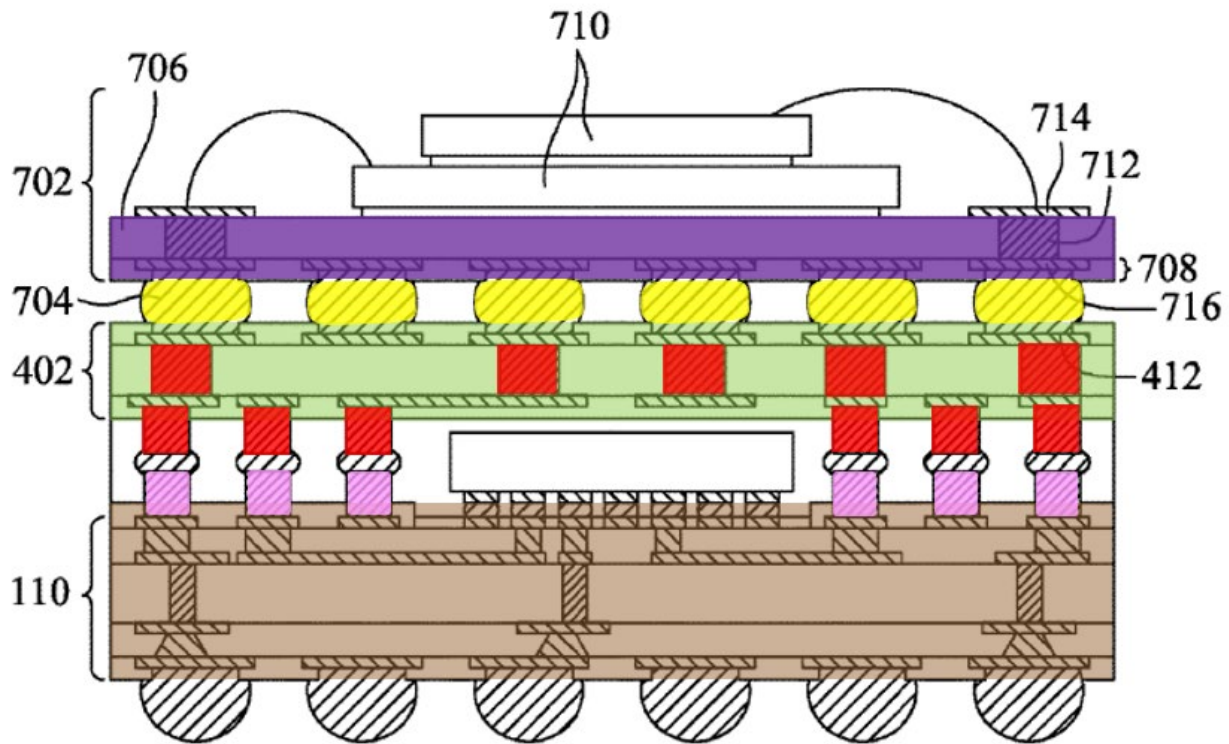


Fig. 7

EX1005 at Figure 7.

168. Wu explains that **connectors 704** can be **metal pillars** because it teaches that different pillars, such as pillar 202, can be made out of metal. *See* EX1005 at [0030] (“**Package connectors 704** such as, for example, solder balls, **pillars**, studs, conductive bumps, or the like bond the package 702 to the interposer 402.”), [0017] (“In some embodiments, the **pillars** 202 are formed by initially

depositing a seed layer over the lands 106. **The seed layer is formed** from copper (Cu), titanium (Ti), aluminum (Al), an alloy of the same, or another conductive material. The seed layer is formed by, for example, electroless copper deposition, atomic layer deposition, physical vapor deposition (PVD) by sputtering Ti, Cu, or another deposition process. **A mask layer is formed over the seed layer** from a material such as a photoresist or the like. The mask layer is patterned to form openings exposing the lands 106 by, for example, exposing and developing a photoresist mask layer. **A metal layer is formed over the patterned mask layer** by, for example physical vapor deposition, electroless plating, seed layer deposition by ALD and electroplating, or by another metal formation process. In some embodiments, **the deposited metal layer is planarized** by, for example, a chemical-mechanical polish (CMP), grinding, etching, or the like. The planarization step removes excess deposited metal from over the patterned mask layer, leaving **pillars** 202.”).

169. Wu further explains that the **package 702**, which includes the **package substrate 706**, has the **connector 704** mounted thereon. *See* EX1005 at [0031] (“While the **package 702** is illustrated herein as having a substrate 706 with dies 710 disposed thereon, the structure is not limited to having such a **package 702** with such an arrangement. In other embodiments, the **package 702** is a die or

chip mounted directly on the **connectors 704**, *multiple dies or packages on the* **connectors 704** or another arrangement.”).

170. The fact that **connector 704** mounted on **package substrate 706** is evident from Figures 5 through 7 of Wu, which shows the sequential fabrication steps culminating in Figure 7. In Figure 5, **interposer 402** has been mounted on the **substrate 110** and filled with moldable underfill (MUF) 502. *See* EX1005 at [0021] (“FIG. 4 is a cross-sectional view illustrating mounting an **interposer 402** on the **substrate 110** according to some embodiments.”), [0028] (“FIG. 5 is a cross-sectional view illustrating application of a moldable underfill (MUF) 502 according to some embodiments.”).

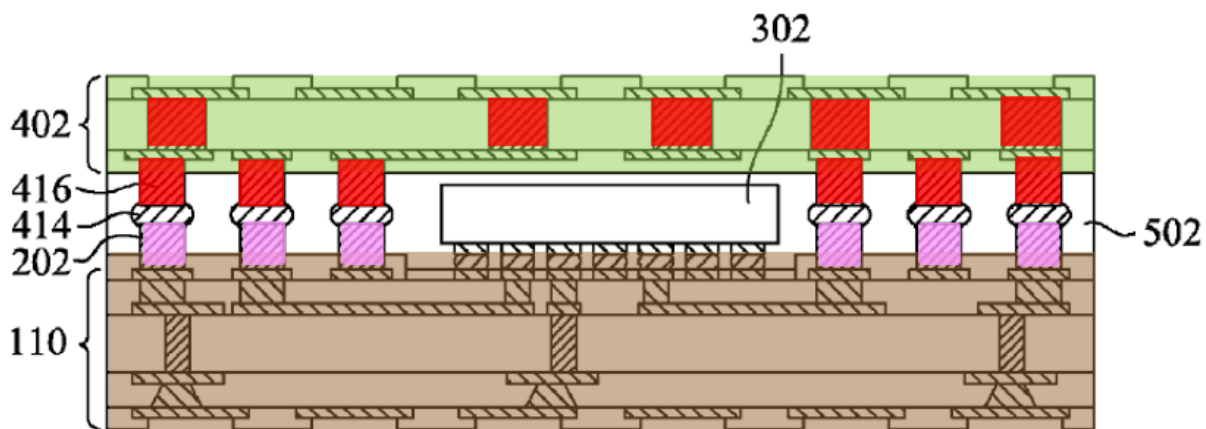


Fig. 5

EX1005 at Figure 5.

171. Then, **connector 602** (see **blue arrow**) are added to the bottom of the **substrate 110**, but *not* to the top surface of **interposer 402**. See EX1005 at [0029] (“FIG. 6 is a cross-sectional view illustrating mounting **connectors 602** on the **substrate 110** according to some embodiments. **Connectors 602**, such as, for example, solder balls, are mounted on the lands 114. In other embodiments, the **connectors 602** are conductive bumps, pillars, studs, or another conductive structure.”).

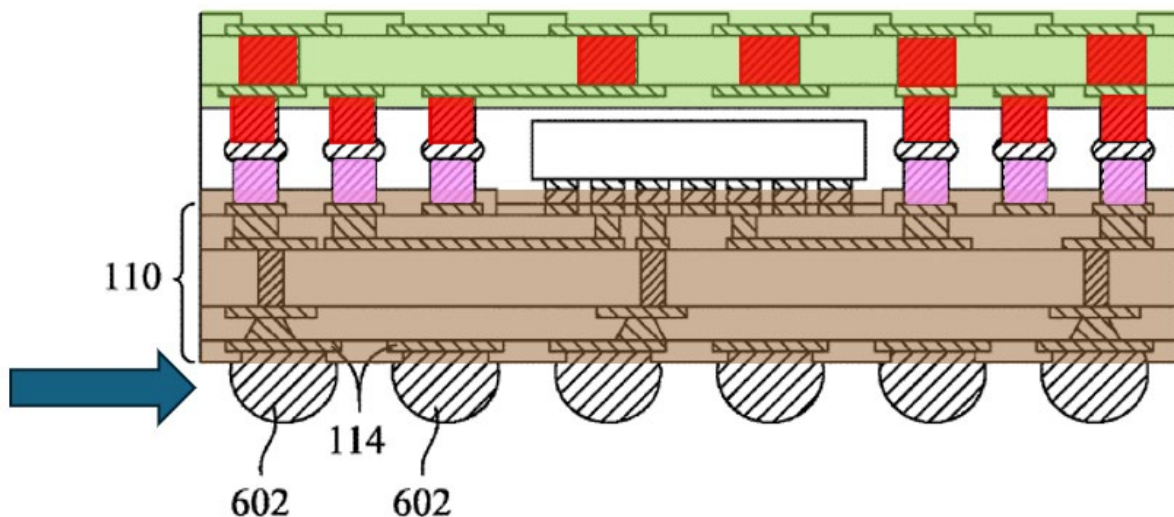


Fig. 6

EX1005 at Figure 6.

172. Then, as shown in Figure 7, the final structure is obtained which has the **connector 704** mounted on **package substrate 706**.

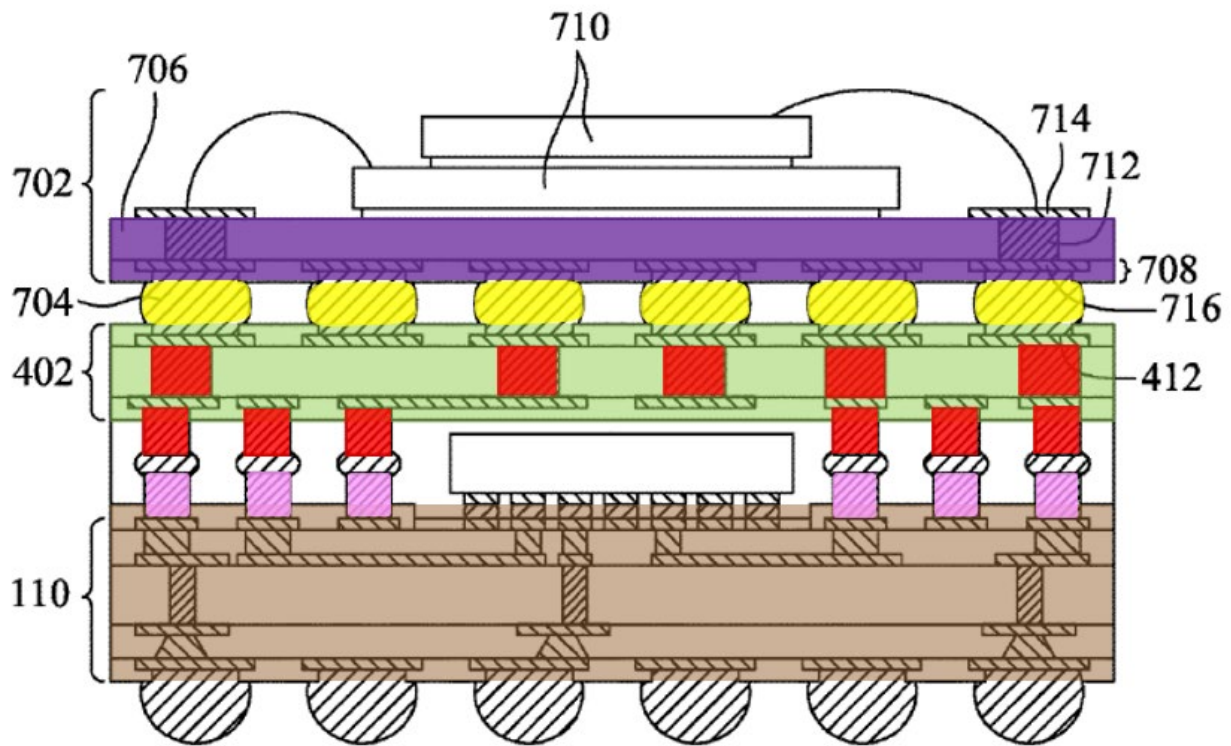


Fig. 7

EX1005 at Figure 7.

173. And Figure 7 of Wu is similar to the structure of Chen because it includes **package substrate 706** electrically connected to **substrate 110** using an **interposer 402** that has **vias 410**. See EX1003 at [0021] (“In an interposer first process, an **interposer 402** is initially provided and mounted over the substrate 110 by attaching **pillars 416** on the **interposer 402** to the **pillars 202** on the **substrate 110**. The **interposer 402** has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer

substrate 408. **Vias 410** in the **interposer** substrate 408 connect the bottom RDL 406 to the top RDL 404.”).

174. Hence, a POSITA would have found it obvious to place **metal pillars** on the bottom surface of the **top package component 62** for electrical coupling to Chen’s **TAV modules 28** in light of the teachings of Wu. Not only would a POSITA have found it obvious to utilize **metal pillars** as a suitable connectors between **TAV modules 28** to the **top package component 62**, placing such **metal pillars** on the **top package component 62** for electrical coupling to the **TAV modules 28** is a routine design choice that would have been obvious to a POSA. Indeed, using **metal pillars** of Wu is merely one well-known method to electrically couple one substrate to another. The modification amounts to nothing more than substitution of one well-known connector (i.e., **metal pillars** of Wu) instead of the **unlabeled connector** shown in Chen that would have led to the predictable result of electrically coupled substrates.

175. In fact, as I explain in greater detail in the next limitation [1I] in paragraphs 176–181, Wu describes placing **pillars 202** on a **bottom substrate 110** for electrical coupling to **interposer 402**. Placing **metal pillars** on **top package component 62** to electrically couple those **metal pillars** to the **TAV modules 28** would have been readily achievable as it simply combines known prior art elements (**metal pillars**) according to known methods (placing **metal pillars** onto

top package component 62) to yield predictable results (structure having **TAV modules 28** electrically coupled to **top package component 62**). And a POSITA would have been able to make such a modification with a reasonable expectation of success because it would be a simple substitution of two known elements.

- x. [1I] the **bottom package substrate** has, on a top surface thereof, a **plurality of top metal pillars** each coupled to a corresponding **metal pillar** among the **plurality of metal pillars of the spacer connector**,

176. As I explained above in paragraphs 93–96 in Ground I with respect to [1I], in my opinion, Chen teaches [1I] .

177. Alternatively, Chen in combination with Wu render obvious [1I]. Figure 7 of Wu shows **package 702** electrically coupled to **substrate 110** with an **interposer 402** that has **pillars 416** on the bottom of the **interposer 402** and **pillars 202** that are on the **substrate 110**.

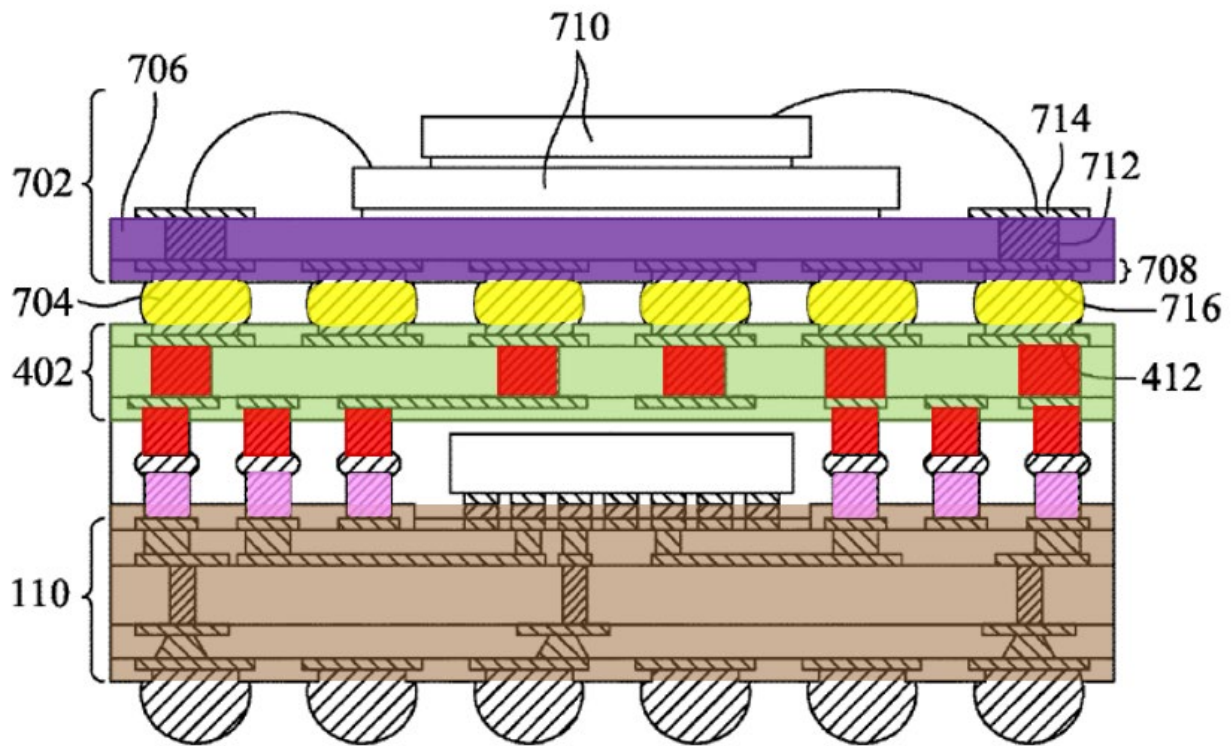


Fig. 7

EX1005 at Figure 7.

178. Figures 2 through 4 shows how the **pillars 202** are first formed on **substrate 110**. EX1005 at [0017] (“FIG. 2 is a cross-sectional view illustrating formation of **pillars 202** on the **substrate 110** according to some embodiments.”).

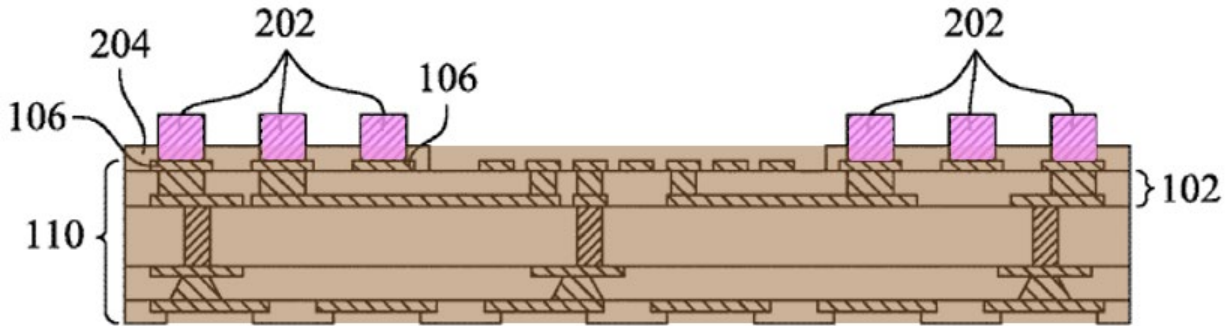


Fig. 2

EX1005 at Figure 2.

179. Then, as shown in FIG. 4, “[t]he **interposer 402** is mounted to the **substrate 110** by aligning the **pillars 416** over the **pillars 202** and bonding the aligned pairs of **pillars 202** and **416** to each other.” EX1005 at [0027]. *See also* EX1005 at [0021] (“FIG. 4 is a cross-sectional view illustrating mounting an **interposer 402** on the **substrate 110** according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the **pillars 202** on the **substrate 110**.”).

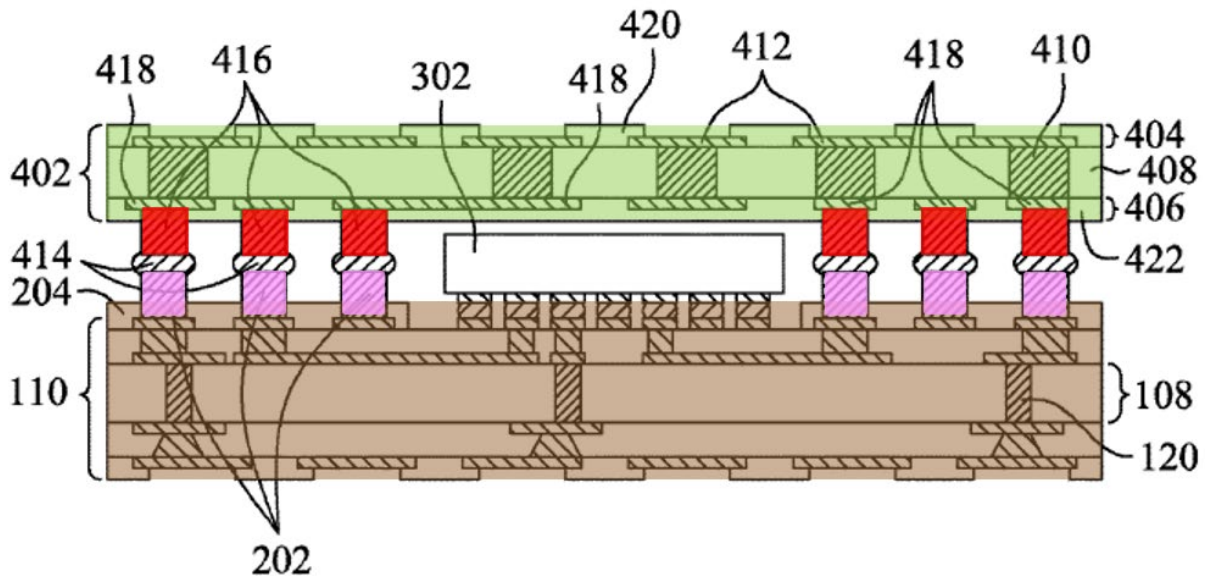


Fig. 4

EX1005 at Figure 4.

180. The **pillars 202** are made of **metal**. See EX1005 at [0017] (“In some embodiments, the **pillars 202** are formed by initially depositing a seed layer over the lands 106. **The seed layer is formed** from copper (Cu), titanium (Ti), aluminum (Al), an alloy of the same, or another conductive material. The seed layer is formed by, for example, electroless copper deposition, atomic layer deposition, physical vapor deposition (PVD) by sputtering Ti, Cu, or another deposition process. **A mask layer is formed over the seed layer** from a material such as a photoresist or the like. The mask layer is patterned to form openings exposing the lands 106 by, for example, exposing and developing a photoresist mask layer. **A metal layer is formed over the patterned mask layer** by, for

example physical vapor deposition, electroless plating, seed layer deposition by ALD and electroplating, or by another metal formation process. In some embodiments, **the deposited metal layer is planarized** by, for example, a chemical-mechanical polish (CMP), grinding, etching, or the like. The planarization step removes excess deposited metal from over the patterned mask layer, leaving **pillars 202**.”).

181. Place **metal pillars** onto the **bottom package component 56** for electrical coupling to **TAV modules 28** would have been a trivial modification and amounts to nothing more than combining prior art elements (**metal pillars**) according to known methods (placing **metal pillars** onto **bottom package component 56**) to yield predictable results (device that has **TAV modules 28** electrically coupled to **bottom package component 56**). And a POSITA would have been able to make such a modification with a reasonable expectation of success because it would be a simple substitution of two known elements.

- xi. [1J] the **top package substrate** is electrically coupled to the **bottom package substrate** through the **plurality of bottom metal pillars** of the **top package substrate**, the **plurality of metal pillars** of the **spacer connector**, and the **plurality of top metal pillars** of the **bottom package substrate**; and

182. As I explained above in paragraphs 163–175 in Ground III with respect to [1H], in my opinion, Chen teaches [1J].

- xii. [1K] a **bottom chip** arranged in the space between the **bottom package substrate** and the **top package substrate**,

183. As I explained above in paragraphs 99–102 in Ground I with respect to [1K], in my opinion, Chen teaches [1K].

- xiii. [1L] wherein the **bottom chip** is mounted to the top surface of the **bottom package substrate**,

184. As I explained above in paragraphs 103–104 in Ground I with respect to [1L], in my opinion, Chen teaches [1L].

- xiv. [1M] the at least one **spacer connector** comprises two **spacer connectors** arranged on opposite sides of the **bottom chip**.

185. As I explained above in paragraphs 105–106 in Ground I with respect to [1M], in my opinion, Chen teaches [1Pre].

2. Dependent Claim 2

- i. [2Pre] The structure of claim 1, wherein

186. As I explained above in paragraphs 154–185 in Ground III, in my opinion, Chen in combination with Wu render obvious the structure of claim 1.

- ii. [2A] a top surface of the **bottom chip** is spaced downwardly from the bottom surface of the **top package substrate**.

187. As I explained above in paragraphs 108–109 in Ground I with respect to [2A], in my opinion, Chen teaches [2A].

3. Dependent Claim 3

i. [3Pre] The structure of claim 2, further comprising:

188. As I explained above in paragraphs 186–187 in Ground III, in my opinion, Chen in combination with Wu render obvious the structure of claim 2.

ii. [3A] a top chip mounted to the top surface of the top package substrate,

189. In my opinion, Chen in combination with Wu render obvious [3A].

190. Chen teaches that “package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown).” EX1003 at [0019]. While a POSITA would have readily recognized that device die (not shown) would be bonded to the top surface of the package substrate (not shown), Chen does not explicitly teach it. But this is a well-known configuration that is routinely employed in the art.

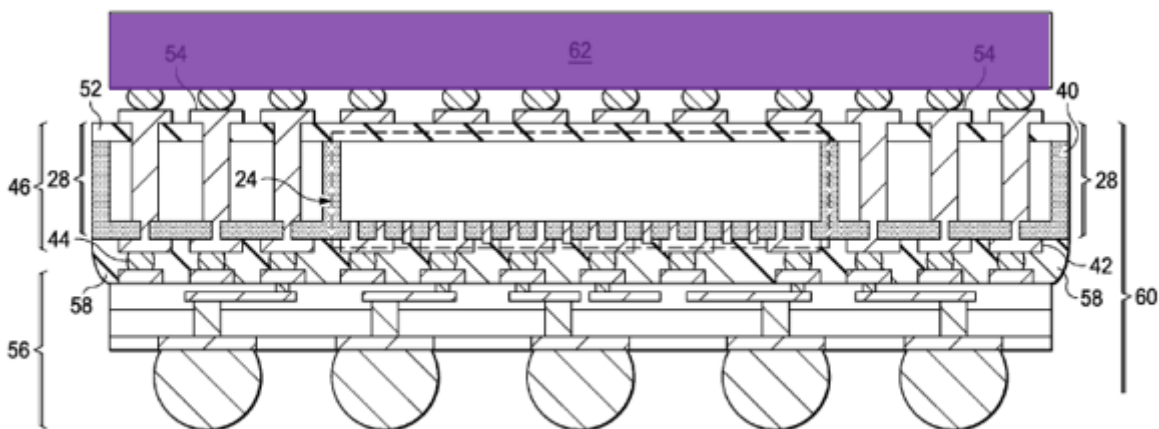


FIG. 9

EX1003 at Figure 9.

191. For example, as I explained in paragraphs 163–175 in Ground III with respect to [1H], Wu shows, in Figure 7, **dies 710** that are mounted to the top surface of the **package substrate 706**. See EX1005 at [0030] (“In some embodiments, the **package 702** has **one or more dies 710** electrically connected to conductive features 714 that are in turn electrically connected to the lands 716 by way of vias 712 disposed in a **package substrate 706**.”).

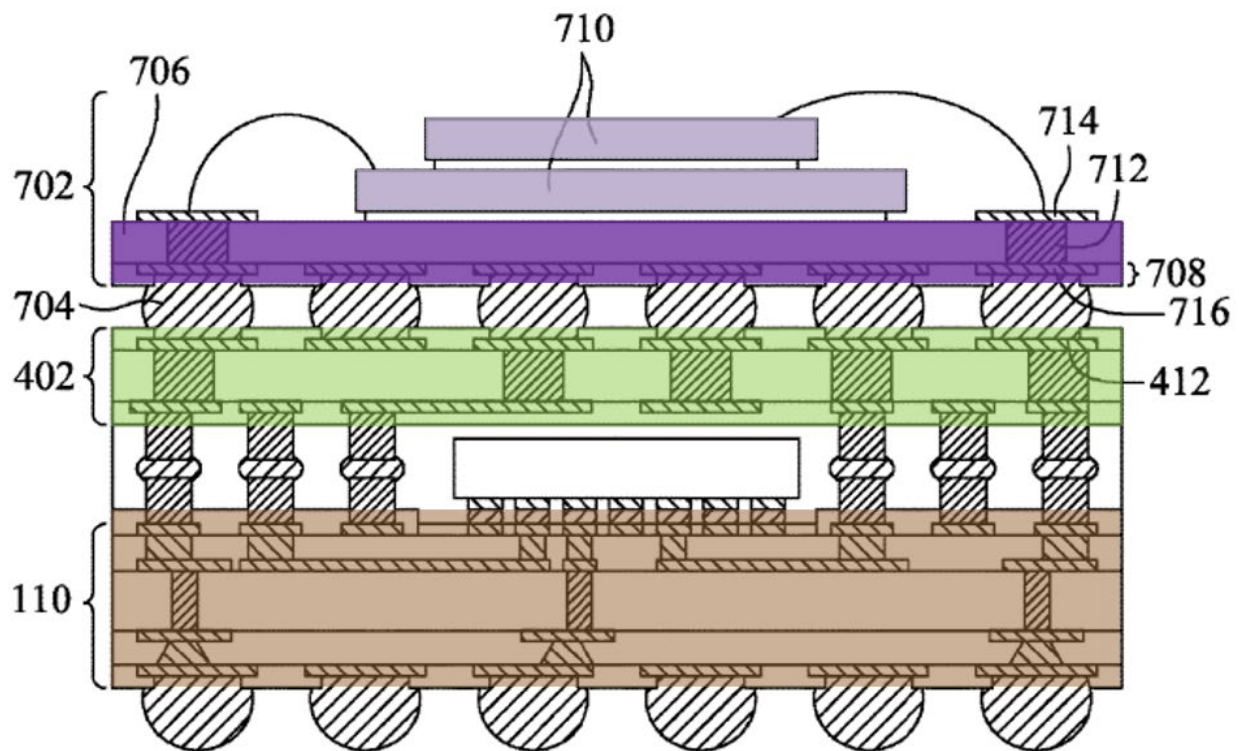


Fig. 7

EX1003 at Figure 7.

192. There is nothing inventive about mounting Chen's **device die (not shown)** on the top surface of the **package substrate** of Chen's **package component 62**. A POSITA would have been able to mount Chen's **device die (not shown)** on Chen's **package substrate (not shown)** in the manner shown in Figure 7 of Wu with a reasonable expectation of success because it merely provides one particular configuration of placing a **device die** on a **package substrate**.

193. Alternatively, it would have been obvious to mount Wu's **dies 710** on Chen's **package substrate (not shown)** in the manner shown in Figure 7 of Wu with a reasonable expectation of success because it merely provides one other particular configuration of placing one or more **device dies** on a **package substrate**. Placing Chen's **device die (not shown)** or Wu's **dies 710** on the top of Chen's **package substrate (not shown)** represents the straightforward integration of known prior art components—namely, Chen's **device die (not shown)** or Wu's **dies 710** with Chen's **package substrate (not shown)**—implemented using established semiconductor assembly techniques, specifically by positioning Chen's **device die (not shown)** or Wu's **dies 710** onto the available top surface of Chen's **package substrate (not shown)**, to achieve the predictable and routine result of a semiconductor **die or chip** being placed on the top surface of a **package substrate** to enable electrical interconnection with other components within a stacked

package configuration. Selecting the top surface of the **package substrate** as the mounting location would have at least constituted an obvious-to-try design choice from among a limited and well-defined set of feasible mounting surfaces—namely, the top or bottom surfaces of the **package substrate**—because a POSITA, familiar with conventional package assembly constraints and electrical routing considerations, would have immediately recognized that mounting **dies** to the lateral side surfaces of the **package substrate** would be impractical and inefficient, and would have reasonably expected successful electrical and mechanical integration when selecting either of the planar major surfaces.

- iii. **[3B] wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.**

194. In my opinion, Chen in combination with Wu render obvious [3B].

195. Chen teaches that “**package component 62** is a package that includes a **device die (not shown)** bonded to a **package substrate (not shown)**.” EX1003 at [0019]. Chen also teaches that “[i]n some embodiments, **top package component 62** is a **device die**.” EX1003 at [0019]. In other words, Chen itself teaches that the overlaps the **package component 24** and each of the two **TAV modules 28**.

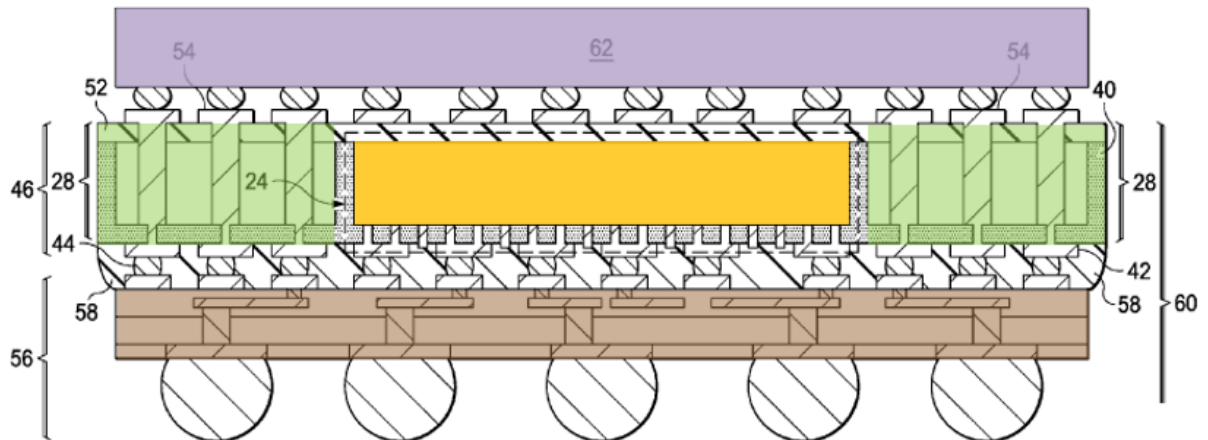


FIG. 9

EX1003 at Figure 9. *See also* EX1003 at [0020] (“FIG. 10 illustrates an exemplary embodiment wherein **package component 62** includes a plurality of **stacked dies 64**. In some embodiments, **stacked dies 64** are **memory dies**. **Stacked dies 64** may be bonded to RDLs 54 that are over and aligned to **package component 24**, which are further connected to the RDLs 54 over and aligned to **TAV modules 28**.”), [0014], [0018]. As shown below in Figure 7 of Wu, two **dies 710** mounted on **package substrate 706**. The **lower die 710**, relative to the **upper die 710** and **die 110** on the **bottom substrate 110**, is much larger such that it extends over the

pillars 416 that is adjacent to the **die 302**.

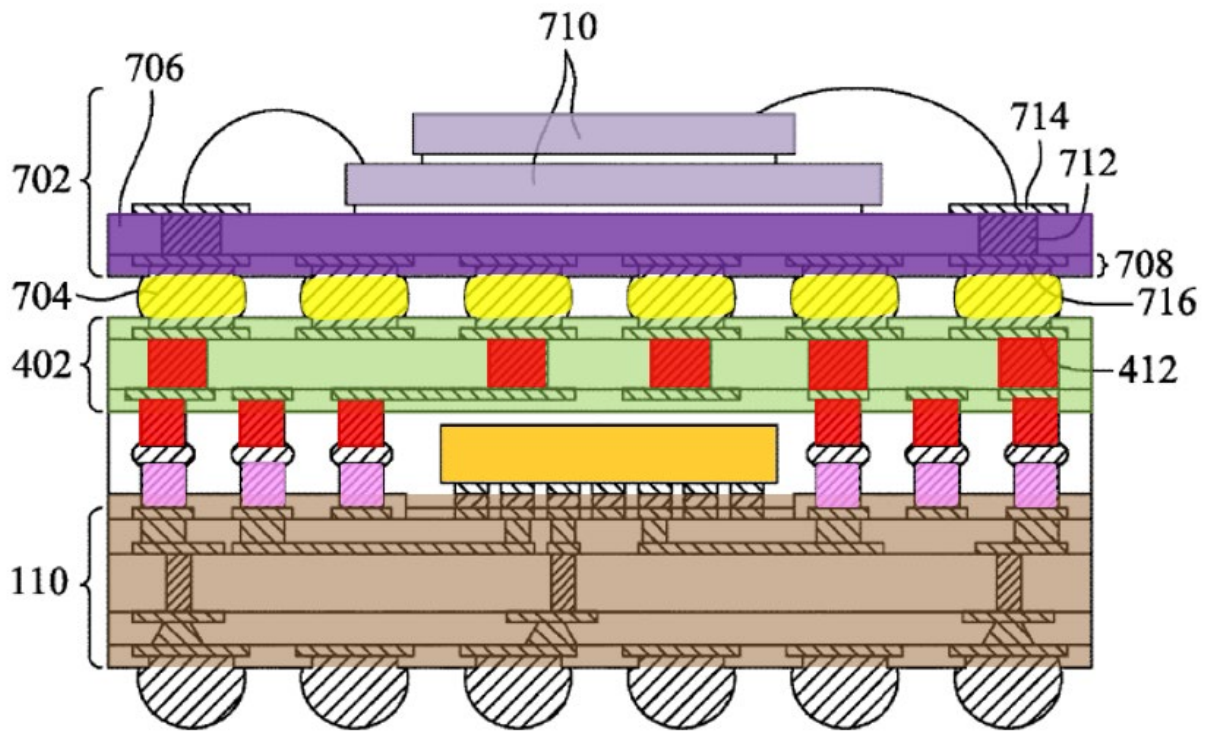
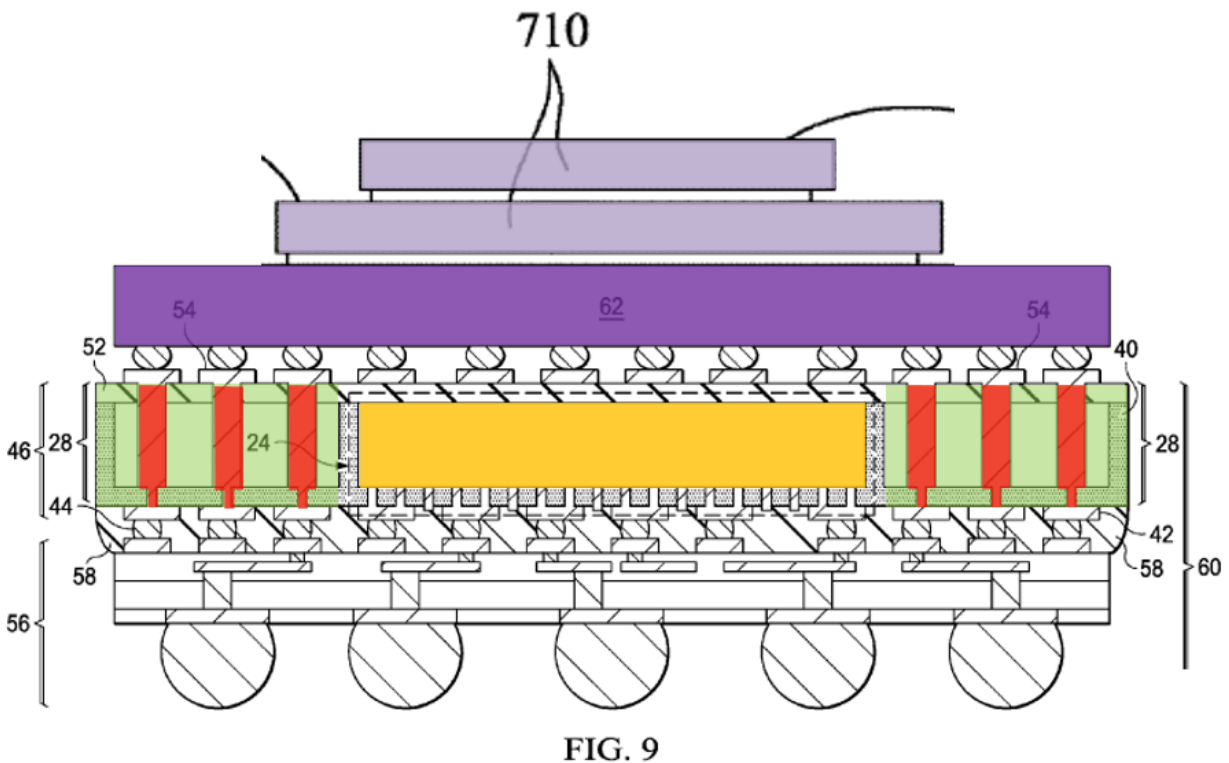


Fig. 7

EX1005 at Figure 7.

196. It would have been obvious to a POSITA to replace Chen's **device die (not shown)** in Chen's **package component 62** with Wu's **dies 710** to obtain a package as shown below, where the **die 710** overlaps the **package component 24** and each of the two **TAV modules 28** in a direction in which the **package component 702** is stacked on top of the **bottom package component 56**, and a POSITA would have had a reasonable expectation of success in making that

substitution because it was well known that **dies** of various sizes could be placed on packages.



EX1003 at Figure 9 (as modified with Wu).

4. Dependent Claim 4

i. [4Pre] The structure of claim 1, wherein

197. As I explained above in paragraphs 154–185 in Ground III, in my opinion, Chen in combination with Wu render obvious the structure of claim 1.

- ii. [4A] each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

198. As I explained above in paragraphs 163–175 in Ground III with respect to [1H] and in paragraphs 176–181 in Ground III with respect to [1I], in my opinion, Chen in combination with Wu render obvious [4A].

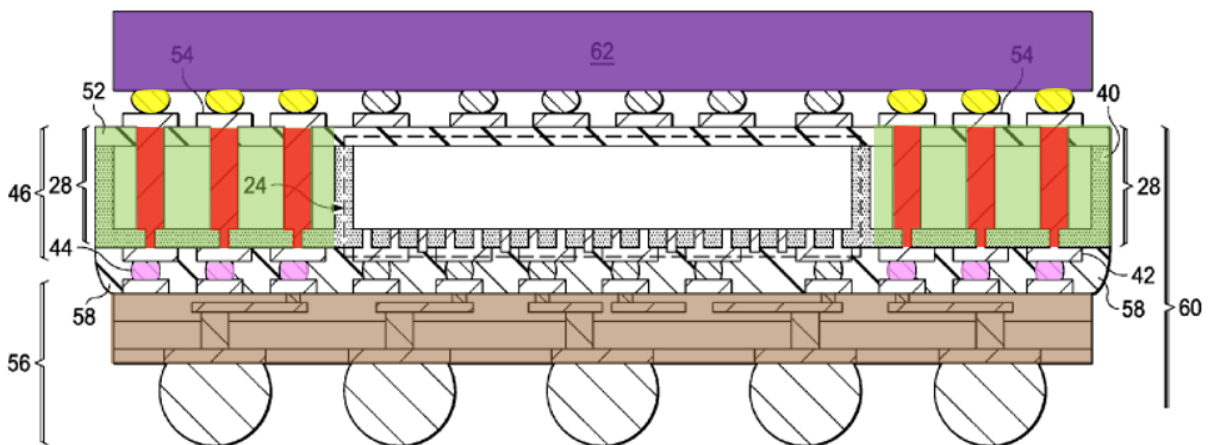


FIG. 9

EX1003 at Figure 9.

5. Dependent Claim 7

- i. [7Pre] The structure of claim 4, wherein

199. As I explained above in paragraphs 197–198 in Ground III, in my opinion, Chen in combination with Wu render obvious the structure of claim 4.

- ii. [7A] the **spacer connector** further comprises a **dielectric layer** on the bottom surface of the **core substrate**, and

200. As I explained above in paragraphs 124–125 in Ground I with respect to [7A], in my opinion, Chen teaches [7A].

- iii. [7B] the **plurality of metal pillars** pass through the **core substrate** and the **dielectric layer**.

201. As I explained above in paragraphs 126–127 in Ground I with respect to [7B], in my opinion, Chen teaches [7B].

6. Dependent Claim 8

- i. [8Pre] The structure of claim 7, wherein

202. As I explained above in paragraphs 199–201 in Ground III, in my opinion, Chen in combination with Wu render obvious the structure of claim 7.

- ii. [8A] the **dielectric layer** is a dielectric adhesive in which the **core substrate** is pasted.

203. As I explained above in paragraphs 129–132 in Ground I with respect to [8A], in my opinion, Chen teaches [8A].

7. Dependent Claim 9

- i. [9Pre] The structure of claim 4, wherein

204. As I explained above in paragraphs 197–199 in Ground III, in my opinion, Chen in combination with Wu render obvious the structure of claim 4.

- ii. [9A] the **spacer connector** further comprises a plurality of **bottom metal pads**, each on the bottom end of a corresponding **metal pillar** among the **plurality of metal pillars**,

205. As I explained above in paragraphs 134–135 in Ground I with respect to [9A], in my opinion, Chen teaches [9A].

- iii. [9B] the bottom ends of the **plurality of metal pillars** are connected to corresponding top ends of the **plurality of top metal pillars** of the **bottom package substrate** via the corresponding **bottom metal pads** of the **spacer connector**, and

206. As I explained above in paragraphs 136–138 in Ground I with respect to [9B], in my opinion, Chen teaches [9B].

- iv. [9C] bottom ends of the **plurality of bottom metal pillars** of the **top package substrate** are connected to the corresponding top ends of the **plurality of metal pillars** of the **spacer connector** via the corresponding **top metal pads** of the **spacer connector**.

207. As I explained above in paragraphs 160–161 in Ground III with respect to [1F] and in paragraphs 163–175 in Ground III with respect to [1H], in my opinion, Chen in combination with Wu render obvious [9C].

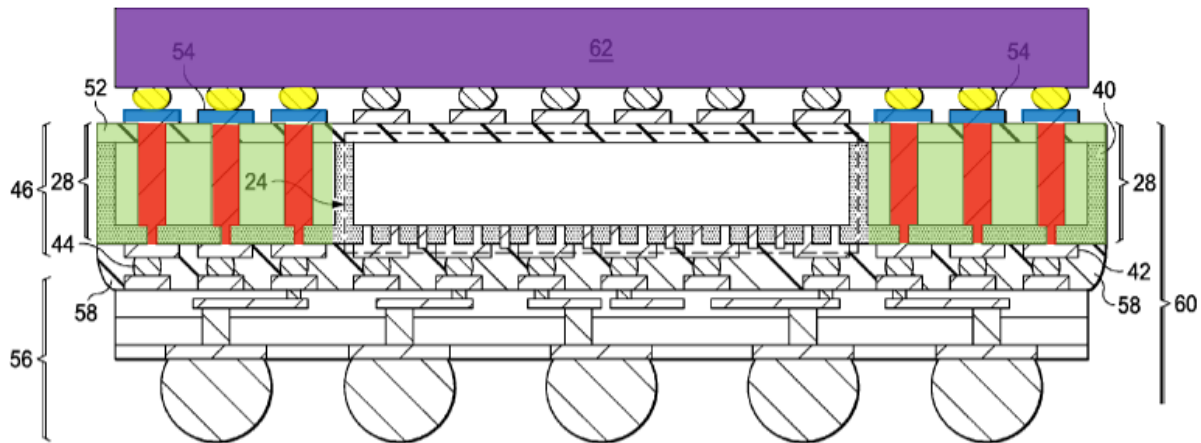


FIG. 9

EX1003 at Figure 9.

D. Ground IV: Claims 5–6 Are Rendered Obvious By Chen In View Of Wu And Furuta

1. Dependent Claim 5

i. [5Pre] The structure of claim 4, wherein

208. As I explained above in paragraphs 197–198 in Ground III, in my opinion, Chen in combination with Wu render obvious the structure of claim 4.

ii. [5A] the **spacer connector is free of **metal pads** on the bottom ends of the **plurality of metal pillars** protruding downwardly from the bottom surface of the **core substrate**, and each **metal pillar** among the **plurality of metal pillars** and the corresponding **top metal pad** of the **spacer connector** form a T shape.**

209. As I explained above in paragraphs 142–151 in Ground II with respect to [5A], in my opinion, Chen in combination with Wu and Furuta render obvious [5A].

210. Specifically, as I explained above in paragraphs 148–151 in Ground II with respect to [5A], a POSITA would have found it obvious to remove **RDLs 42** from the system that combined the teachings of Chen and Wu for the same reasons stated above, which would have led to the structure schematically illustrated below.

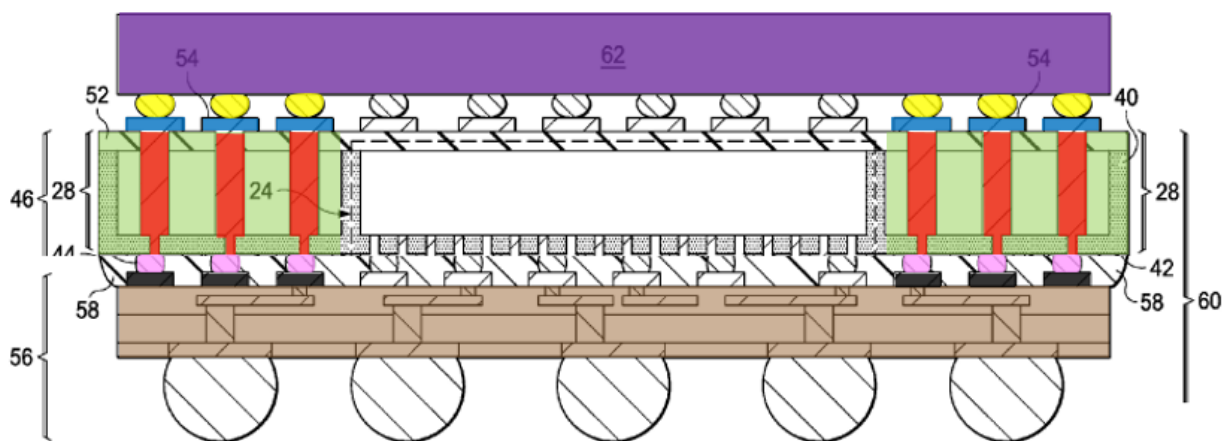


FIG. 9

EX1003 at Figure 9 (modified with Wu and Furuta).

2. Dependent Claim 6

i. [6Pre] The structure of claim 4, wherein

211. As I explained above in paragraphs 197–198 in Ground III, in my opinion, Chen in combination with Wu render obvious the structure of claim 4.

- ii. [6A] the bottom ends of the **plurality of metal pillars** protruding downwardly from the bottom surface of the **core substrate** of the **spacer connector** are connected, in an end-to-end manner, to corresponding top ends of the **plurality of top metal pillars** of the **bottom package substrate**, and bottom ends of the **plurality of bottom metal pillars** of the **top package substrate** are connected to the corresponding top ends of the **plurality of metal pillars** of the **spacer connector** via the corresponding **top metal pads** of the **spacer connector**.

212. As I explained above in paragraphs 209–210 in Ground IV with respect to [5A] and in paragraphs 163–175 in Ground III with respect to [1H], in my opinion, Chen in combination with Wu and Furuta render obvious [6A], which would have led to the structure schematically illustrated below.

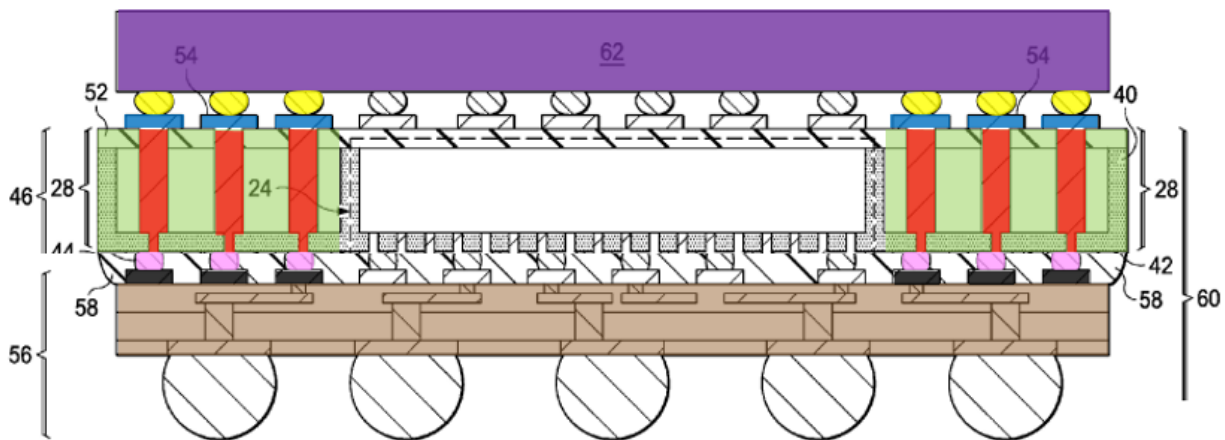


FIG. 9

EX1003 at Figure 9 (modified with Wu and Furuta).

VIII. Availability for Cross-Examination

213. In signing this declaration, I recognize that the declaration will be filed as evidence in a case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination.

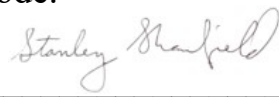
IX. Right to Supplement

214. I reserve the right to supplement my opinions in the future to respond to any arguments that the Patent Owner may raise and to take into account new information as it becomes available to me.

X. Jurat

215. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

March 12, 2026
Date



Dr. Stanley Shanfield

APPENDIX A

Stanley Shanfield



Curriculum Vitae for Stanley Shanfield

Education:

Massachusetts Institute of Technology, Ph.D., Physics, 1981

University of California, Irvine, B.S. Cum Laude, Physics, 1977

Educational Awards:

Outstanding Research Project, U.C. Regents Award, 1977

Phi Beta Kappa, 1977

Four Year Scholarship, Tuition & Research, ERDA/DOE, 1977-1981

Hands-On Professional Expertise:

Semiconductor Physics & Chemistry

Semiconductor Fabrication: Silicon and III-V Materials

Semiconductor Device & Integrated Circuit Engineering

Semiconductor Equipment: Front & Back End

Semiconductor Packaging Design and Manufacturing

Passive Component Design and Manufacturing

RF Design and Fabrication

Digital Design & Fabrication

Semiconductor Manufacturing in Silicon and III-V Materials

MEMS Design and Fabrication: Electrical, Optical, & Sensing Devices

Fiber Optic Device Design and Fabrication

Integrated Optics & Electro-Optical Devices

Plasma Physics

Specialized Training:

Global Positioning Electronics, Systems and Components

Six Sigma Semiconductor Manufacturing

Microwave Engineering

US Patent Law in Technology

Patent Application and Prosecution

Semiconductor Plasma Processing

Thin Film Physics and Technology

MEMS-based Gyroscopes and Accelerometers

Thermoelectric Materials & Technology

Phased Array Radar Engineering

Antennas and Electromagnetic Propagation

Solid State Optical Devices

Fiber Optic Communication System Operation

HALT and HAST Reliability Testing Methods

Professional Experience:

Draper Laboratory Cambridge, MA

2003 – present

Division Leader, Advanced Hardware Development Distinguished Member of Technical Staff Technical Director

Led division (about 80 staff) in re-invigorating multi-chip integrated circuit module facility, more than doubling associated revenues in two years. By most accounts, made division a viable business & technological entity again. Invented & led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Led team in realization & fabrication of a newly designed precision MEMS-based gyroscope and associated ASIC. Found funding and led team in developing a miniature power source with energy density at least two orders of magnitude higher than any source previously built. Developed fabrication technology for semiconductor-based low phase noise oscillator design, allowing for receiver operation with extremely low signal strength. Many awards received, most recently, the Draper 2010 Distinguished Performance Award, and 2010 Best Patent Award. Recent work in ASIC process design and circuit design for ultra-high performance government and space systems.

Clarendon Photonics Newton, MA

2002 – 2003

Director, Packaging & Integration

30 person photonic chip startup with \$18 million 2nd round funding. Invented and productized new, low cost and reliable semiconductor processing, packaging and pig-tailing technology for optical add-drop multiplexer. Established assembly and packaging process and developed control electronics. Partner with Micron Technologies, using their R&D semiconductor facility.

AXSUN Technologies Bedford/Billerica, MA

1999 – 2002

Vice President, Operations, Co-Founder 1999 – 2000

Initially three staff members with \$6 million funding. Designed, fabricated and productized AXSUN's micro-electromechanical (MEM) Fabry-Perot optical filter. Patents granted on semiconductor processing and control electronics. Completed facility and semiconductor processing design, then completely equipped. Raised 2nd round funding for \$36 million. Established process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material.

Director, Manufacturing & Wafer Fab Technology

2000 – 2001

After 3rd round funding, led device manufacturing, creating wafer fab and assembly infrastructure; hired 70+ people, led production. Delivered first generation product for revenue to multiple customers. Converted pure technology to dominant company revenue with high yield.

Company purchased by Volcano Technologies, San Diego.

Raytheon Corporation Lexington/Andover, MA

1985 - 1999

Manager, Semiconductor Operations

1996 – 1999

Built and led a 300 employee, \$60 million revenue 24/7 semiconductor development and manufacturing operation resulting from the consolidation of a number of smaller organizations. Key player in technological development and recipient of Raytheon's 6 Sigma Leadership training. Decision maker in Texas Instrument group acquisition, providing significant expert opinion on semiconductor and design facilities. Obtained state-of-art yields using best available steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-manufacturing circuit design and layout methodology.

Research Laboratory Manager

1992 – 1996

Leader of a 90 employee development and contract research organization in high performance semiconductor devices and circuits, measurement, assembly and wafer fab. Led a team which invented and implemented a major revenue generating technology (\$.100 million) based on semiconductor device development (pseudomorphic high electron mobility transistor). Increased outside research funding by 50% in 3 years through superior technical performance relative to competitors.

Section Manager, Semiconductors & ICs

1985 – 1992

Led a MM-Wave Circuit and Module Development program over 2 years, leading to production win of a satellite terminal electronics generating \$320 million in sales. Developed processes for fabricating high power, high frequency multi-function integrated circuits, and combining high performance digital and analog devices in a single integrated circuit.

Spire Corporation Bedford, MA

1981 – 1984

**Staff Scientist
Senior Staff Scientist**

Developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. Wrote joint papers with MIT professor, and had process adopted by equipment manufacturers. Built, operated and characterized ion-assisted deposition system for making coating for semiconductor and machine tool industries. Process eventually purchased by Kennametal, Inc.

Publications

Restricted Publications & Reports

Process Sequence for Formation of Ultra-High Density Multi-Chip Modules:

A high yield, low cost method for creating a system-in-a-package consisting of numerous semiconductor die, passive components, and sensors. Process formed basis for new (2008) facility.

Design and Method of Fabrication of Ultra-High Density Radioisotope Power Source:

In test, a miniature power source that achieves energy density more than 1000X the best chemical battery. Method uses planar semiconductor processing of bulk thermoelectric materials.

Design and Method of Achieving Extremely Low Crystal Oscillator Phase Noise:

Method developed for very low power refrigeration of quartz or sapphire crystal resonators, resulting in extremely low phase noise oscillators. The low phase noise allows extremely high sensitivity in digital receivers, including GPS receivers, leading to use in extremely low signal conditions.

Design, Evaluation & Production of MEMS-based Fabry-Perot Interferometer:

Design and method for ultra-compact spectral analyzer made using semiconductor and optical thin film processing.

Design & Evaluation of Ultra-Fast Control Electronics for Integrated Optical Multiplexer:

Design and performance evaluation of silicon-based integrated optical multiplexer using chip-based local heating

Design and Fabrication of Q-band MILSTAR Communications Terminal Transmitter:

Record power and efficiency 44 GHz transmitter design using new transistor design, and combined waveguide

Key Publications (selected)

Process Characterization of PSG and BPSG Plasma Deposition, J. Electrochem. Soc., Volume 131, Issue 9, pp. 2202-2203

A double-recessed Al_{0.24}GaAs/In_{0.16}GaAs pseudomorphic HEMT for Ka- and Q-band power Applications, Electron Device Letters, IEEE, Volume 14, Issue 9, pp. 456 - 458

Formation of Thick Metal Structures on GaAs MMICs Using Image Reversal Lithography and Evaporated Metal Deposition, J. Electrochem. Soc., Volume 136, Issue 9, pp. 2687-2690

Contact Hole Etching in Load-Locked Hexagonal Reactive Ion Etch System, J. Electrochem. Soc., Vol. 131, No. 8, 1984

An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with Improved Breakdown Voltage for X and Ku-band power applications, Microwave Theory and Techniques, IEEE Transactions on, Volume 41, Issue 5, May 1993, pp. 752 - 759

Hot-electron-induced Degradation of Metal-Semiconductor Field-Effect Transistors, Integrated Circuit Symposium, 1994. Technical Digest 1994., 16th Annual Volume , Issue , 16-19 Oct. 1994, pp. 259

Ion Beam Deposition of Cubic Boron Nitride, J. Vac. Sci. Technol. A Volume 1, Issue 2, pp. 323-325

Patents**US Patent 6504235 - Passivation layer and process for semiconductor devices**

Method of coating semiconductor devices that prevented parametric shift in electrical performance. Solved key processing problem.

US Patent 4440108 - Ion Beam Deposition Apparatus

Design of equipment for deposition of thin films in the presence of ion bombardment. System produced thin films of interest for mechanical, electrical and optical properties and was sold as an equipment product.

US Patent 6525880 - Integrated Tunable Fabry-Perot filter and Method of Making Same

Design and method for fabricating very small, very high performance variable optical filter using semiconductor fabrication technology. In current use in fiber optical networks, chemical sensors, and 3-D medical imaging applications.

US Patent 5175020 - Boron Nitride Films and Process of Making Same

Ion assisted deposition of ultra-hard cubic boron nitride films for semiconductor and machine tool applications. Significant use in both areas.

US Patent 4526673 - Coating Method

Method for deposition of thin films used in semiconductor device fabrication. Method based on direct control of the kinetics of thin film deposition.

US Patent 7727806 - Systems and Methods for High Density Multi-Component Modules

Method for fabrication of electronic modules using multiple thinned integrated circuits, patterned multi-level interconnects, passive electronic components, and sensors

US Patent Application 2009/TBD - Devices, systems, and methods for controlling the temperature of resonant elements

Devices and systems for achieving low phase noise crystal oscillators using unique low power thermoelectric structures

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Email: shanfield@alum.mit.edu