

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION**

TOPWIRE LLC,

Plaintiff,

V.

APPLE, INC.,

Defendant.

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Case No. 7:25-cv-00551-ADA

Jury Trial Demanded

PLAINTIFF'S FIRST AMENDED COMPLAINT

Plaintiff TopWire LLC (“TopWire”) files this First Amended Complaint against Defendant Apple, Inc. (“Apple” or “Defendant”) for patent infringement under 35 U.S.C. § 271. Plaintiff alleges, based on its own personal knowledge with respect to its own actions and based on information and belief with respect to all others’ actions, as follows:

THE PARTIES

1. Plaintiff TopWire LLC (“TopWire”) is a Texas limited liability company that holds all rights, title, and interests in United States Patent No. 9,859,202 (the “Asserted Patent”). TopWire has a mailing address and a registered office address at 5900 Balcones Drive Suite 100 Austin, Texas 78731.

2. Defendant Apple is a corporation organized and existing under the laws of the State of California, with its principal place of business at One Apple Park Way, Cupertino, CA 95014. Apple may be served with process through its registered agent, CT Corporation System, at 330 North Brand Boulevard, Suite 700, Glendale, California.

JURISDICTION & VENUE

3. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because the action brought by TopWire against Apple arises under the patent laws of the United States, 35 U.S.C. §1 *et seq.*

4. This Court has personal jurisdiction over Apple at least because Apple conducts business in this District and throughout the state of Texas.

5. This Court also has personal jurisdiction over Apple because Apple has committed acts of patent infringement in this District and throughout Texas, including selling, and offering for sale, products and services that infringe TopWire's Asserted Patent.

6. This Court also has personal jurisdiction over Apple because Apple has placed infringing products and services into the stream of commerce, with the expectation they will be purchased and used by customers in Texas and in this District, such that customers in Texas and in this District have purchased and used, and continue to purchase and use, Apple's infringing products and services, which has allowed Apple to derive substantial benefits from infringing acts in Texas and in this District.

7. Venue is proper in this District against Apple pursuant to 28 U.S.C. §§ 1391 and 1400(b).

8. Venue is proper in this District against Defendant Apple under 28 U.S.C. § 1391(c)(3) because Apple maintains many regular and established places of business within the Western District of Texas including: (1) its two Austin campuses located at 12545 Riata Vista Circle, Austin, Texas 78727 and 6900 W Parmer Lane, Austin, Texas 78729; (2) a technical and engineering center at 320 S. Capital of Texas Hwy, West Lake Hills, Texas 78746; and (3) several retail stores, including ones at located at (a) 3121 Palm Way, Austin, Texas 78758; (b) 2901 S. Capital of Texas Highway, Austin, Texas 78746; (c) 15900 La Cantera Parkway, San Antonio,

Texas 78256; (d) 7400 San Pedro Avenue, San Antonio, Texas 78216; and (e) 8401 Gateway Boulevard West, El Paso, Texas 79925.

9. Apple has operated in Austin, Texas since 1992. Since then, Apple has steadily grown its presence in Austin. On information and belief, Apple employees in Austin have worked on the iPhone X series and all other subsequent iPhone series (collectively, “the Accused Products”). As of the filing of this lawsuit, Apple’s campus in Austin, Texas is located at and around 12545 Riata Vista Cir, Austin, TX 78727. Apple is currently renovating its Austin campus and moving some of its employees to its new multi-billion-dollar campus down the road at 6900 W Parmer Lane, Austin, Texas 78729.¹

10. On information and belief, Apple employs thousands of workers at its Austin campuses within this District. According to Apple’s website, it employs over 8,400 workers within the State of Texas, with about 6,000 of those employees being in Austin.² Apple claims that Austin represents Apple’s second largest corporate presence in the world.³

11. On information and belief, Apple has employees that have personal knowledge of the structures (hereinafter, “the Infringing Structures” or “the Infringing Semiconductor Structures”) inside the Accused Products made, used, sold, and/or offered for sale by Apple in the United States and/or imported by Apple in the United States that infringe the Asserted Patent.

12. Apple’s website lists several jobs related to the technology covered in the Asserted Patent. For example, as of February 23, 2025, Apple lists 583 Austin-based jobs on its website and

¹ See KVUE, *Apple plans multimillion-dollar renovation to old Austin campus as employees move in to new space*, available at <https://www.kvue.com/article/money/economy/boomtown-2040/austin-texas-apple-campus-renovations-2024/269-72b92e91-5561-4214-9fba-b59819da0ad0> (last visited November 20, 2025).

² See Apple, *Two million U.S. jobs*, available at <https://www.apple.com/job-creation> (last visited February 23, 2026).

³ *Id.*

283 of those jobs relate to the iPhone.⁴ These jobs include positions such as PCB designer, hardware systems engineer for board design, CPU pre-silicon engineering program manager, SoC DFT DC engineer, and emulation integration engineer, many of which have personal knowledge of the internal hardware layout of iPhones.⁵ On information and belief, Apple engineers at its Austin office have personal knowledge of the Infringing Semiconductor Structures.

13. Relevant third-party witnesses, such as semiconductor device manufacturers, are also located in this District. Apple manufactures integrated circuits and other semiconductor components for Apple's iPhones at its manufacturing plant in Austin, Texas located at 12100 Apple Blvd, Austin, TX 78754.⁶ GlobalWafers manufactures advanced wafers for integrated circuits in Apple's iPhones at its manufacturing plant in Sherman, Texas located at 200W FM1417, Sherman, TX 75090.⁷ On information and belief, employees at these offices work with components that are part of Infringing Semiconductor Structures in Apple's iPhones.

14. Other relevant third-party witnesses, such as semiconductor integration providers, are also located in this District. On information and belief, Taiwan Semiconductor Manufacturing Company ("TSMC") provides Apple most of the integrated circuits it includes in its iPhones. TSMC also operates a design services center in Austin, Texas located at 11921 N Mopac Expy #340, Austin, TX 78759 that provides support for implementing TSMC integrated circuits in

⁴ See Apple, *Find your perfect role*, available at <https://jobs.apple.com/en-us/search?location=austin-AST&product=iphone-IPHN> (last visited February 23, 2025).

⁵ *Id.*

⁶ See Apple, *Apple increases U.S. commitment to \$600 billion, announces American Manufacturing Program*, available at <https://www.apple.com/newsroom/2025/08/apple-increases-us-commitment-to-600-billion-usd-announces-ambitious-program/> (last visited November 20, 2025).

⁷ *Id.*

customer devices. On information and belief, employees at this office help Apple integrate TSMC's integrated circuits into the Infringing Semiconductor Structures in Apple's iPhones.

15. Apple works with hundreds of suppliers, many of which have operations in Texas. For example, Apple suppliers such as Analog Devices, Coherent Corporation, Flex, Infineon Technologies, Murata Manufacturing Company, Power Integrations, ON Semiconductor, Qorvo, Qualcomm, Skyworks Solutions, have design and/or manufacturing operations in Texas.⁸ On information and belief, employees at these offices work with components that are part of Infringing Semiconductor Structures in Apple's iPhones.

THE ASSERTED PATENT

16. On January 2, 2018, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 9,859,202 ("the '202 Patent"), entitled "Spacer Connector," with Dyi-Chung Hu, a resident of Taiwan at the time of filing for patent protection, listed as the sole inventor. The '202 Patent claims priority to U.S. Provisional Application No. 62/184,034, filed June 24, 2015. A copy of the '202 Patent is attached as Exhibit A. On April 27, 2025, Dyi-Chung Hu subsequently assigned all rights, titles, and interests in the '202 Patent to TopWire.

17. Dr. Dyi-Chung Hu is a leading expert in semiconductor packaging. Dr. Hu has a PhD in material science from the Massachusetts Institute of Technology ("MIT") and has experience in industry and academia. During his career, Dr. Hu has worked for IBM East Fishkill, served as a professor at the National Chao Tung University, served as a member of the Industry Research Organization in Taiwan, and helped pioneer the thin film transistor ("TFT") LCD industry in Taiwan. Additionally, Dr. Hu has served as a founding committee member of SEMCON

⁸ See Apple, *Supplier List*, available at https://s203.q4cdn.com/367071867/files/doc_downloads/2024/04/Apple-Supplier-List.pdf (last visited November 20, 2025).

Taiwan electronic packaging and served as the Senior Vice President of Research and Development at Unimicron. Dr. Hu is the founder of two Taiwanese LCD companies, E-Ink and HannStar, and he currently serves as the founder and CEO of SiPlus Co., a systems integration company. Dr. Hu has been invited to speak on semiconductor packaging at numerous conferences and is a named inventor on more than 100 patents.

18. The '202 Patent is valid, enforceable, and was duly issued in full compliance with Title 35 of the United States Code.

19. The '202 Patent is directed to patentable subject matter. Particularly, the '202 Patent is directed to a novel semiconductor structure for separating and electrically connecting two layered packaging substrates. In the claimed semiconductor structure, an integrated circuit can interface with the lower packaging substrate of the two layered packaging substrates. Accordingly, the claimed semiconductor structure can facilitate integrated circuit layering in electronic devices like smartphones.

20. To the extent any marking or notice was required by 35 U.S.C. § 287, TopWire has complied with the applicable marking and/or notice requirements of 35 U.S.C. § 287.

FACTUAL BACKGROUND

Semiconductor Packaging

21. In smartphones, semiconductor packaging plays a crucial role in balancing performance, size, and power efficiency. Modern phones are designed to be compact yet highly capable, which places extreme constraints on how chips are packaged and integrated. Because smartphone chips handle functions like computing, graphics, communications, and sensing, their packaging must support both high-speed data transmission and effective thermal management in a small, tightly confined space.

Apple's Use of the Patented Technology

22. Apple is one of the leading smartphone companies in the United States, with the company selling millions of iPhones each year. Some estimates peg Apple as having at a majority share of the U.S. smartphone market.⁹

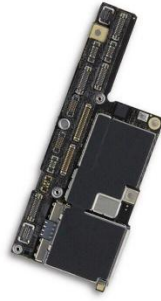
23. Every iPhone Apple has ever created includes a small logic board—sometimes also referred to as a main board or motherboard. The logic board serves as the brains for the iPhone, controlling and facilitating most of the iPhone's core functions. For example, the logic board controls the display interface, the camera, the speaker, and many other features of the iPhone.

24. Early iPhone models used a single-layered logic board—that is, the logic boards each included a single substrate and chips interfacing with this substrate. As the iPhone introduced more features and functions, the number of components inside the iPhone steadily increased, creating more space constraints for the engineers designing new iPhones.

25. Apple's release of the iPhone X on November 3, 2017 introduced a new logic board design.¹⁰ The iPhone X employed a double-layered logic board with two substrates. The top surface of each substrate included integrated circuits, allowing the logic board to support more chips without increasing its surface area.

⁹ See Counter Point Research, *U.S. Smartphone Market Share: Quarterly*, available at <https://counterpointresearch.com/en/insights/us-smartphone-market-share> (last visited November 20, 2025).

¹⁰ See Apple, *The future is here: iPhone X*, available at <https://www.apple.com/newsroom/2017/09/the-future-is-here-iphone-x/> (last visited November 20, 2025).



iPhone X logic board

26. The double-layered logic board with two substrates is an Infringing Semiconductor Structure. Many iPhone models include an Infringing Semiconductor Structure.

27. The Accused Products with the Infringing Semiconductor Structures at least include the following iPhone models: the iPhone X, the iPhone XS, the iPhone XS Max, the iPhone XR, the iPhone 11, the iPhone 11 Pro, the iPhone 11 Pro Max, the iPhone SE, the iPhone 12 mini, the iPhone 12, the iPhone 12 Pro, the iPhone 12 Pro Max, the iPhone 13 mini, the iPhone 13, the iPhone 13 Pro, the iPhone 13 Pro Max, the iPhone 14, the iPhone 14 Plus, the iPhone 14 Pro, the iPhone 14 Pro, the iPhone 14 Pro Max, the iPhone 15, the iPhone 15 Plus, the iPhone 15 Pro, the iPhone 15 Pro Max, the iPhone 16, the iPhone 16 Plus, the iPhone 16 Pro, the iPhone 16 Pro Max, the iPhone 16e, the iPhone 17, the iPhone 17 Pro, the iPhone 17 Pro Max, and the iPhone Air. All of these iPhone models include a “sandwiched” logic board design.¹¹

28. On information and belief, Apple continues to make, use, sell, and/or offer for sale iPhones with the Infringing Semiconductor Structures in the United States and/or import iPhones with the Infringing Semiconductor Structures into the United States.

¹¹ See *How to Safely Separate iPhone Logic Boards (X to Latest Models)*, available at <https://www.youtube.com/watch?v=cPXUyO4h4TU> (last visited November 20, 2025).

29. On information and belief, future iPhone models made, used, sold, and/or offered for sale by Apple in the United States and/or imported by Apple into the United States will include Infringing Semiconductor Structures.

30. Apple does not have any ownership rights to the technology covered by '202 Patent. Additionally, Apple does not have a license to make, use, sell, or offer for sale the technology covered by the '202 Patent.

31. Apple has actual notice of the '202 Patent before the commencement of this lawsuit. On July 10, 2025, TopWire sent a letter ("the Notice Letter") addressed to Apple's Legal Department. The letter is attached hereto as Exhibit B.

32. The Notice Letter stated, in relevant part, "It has come to the attention of Topwire that Apple Inc. ("Apple") is selling (directly or indirectly), advertising, offering for sale, or importing into the United States devices (e.g., [] hand-held mobile devices) that infringe Topwire's patents either directly or through intermediaries."

33. The Notice Letter stated, in relevant part, "the '202 patent relates to a spacer connector used to electrically connect two substrates such as those used in hand-held or other smaller form factor electronic devices. For example, it has been brought to Topwire's attention that Apple sells a line of mobile devices containing processors that utilize a spacer connector to provide for a reduced overall device thickness, such as the Apple iPhone (e.g., iPhone 11, iPhone 13, and other device versions)."

34. The Notice Letter stated, in relevant part, "I draw your attention to, for example, claim 1 of the '202 patent."

35. The Notice Letter specifically identified the '202 Patent.

36. The Notice Letter accused Apple of infringing the '202 Patent.

37. The Notice Letter identified a specific exemplary claim of the '202 Patent.

38. The Notice Letter stated, in relevant part, “Apple sells a line of mobile devices containing processors that utilize a spacer connector to provide for a reduced overall device thickness.”

39. The Notice Letter accused specific exemplary Apple devices of infringing the '202 Patent.

40. Apple received the Notice Letter prior to the date that the original complaint in this case was filed.

41. Apple responded to the Notice Letter on July 22, 2025 and requested that TopWire provide claim charts and other information to support its contention.

42. The Infringing Semiconductor Structures separate and electrically connect two layered packaging substrates. Additionally, the Infringing Semiconductor Structures can facilitate integrated circuit layering in electronic devices, including the Accused Products.

43. Apple has capitalized on the Infringing Semiconductor Structures to simultaneously reduce the size of its logic boards and increase their computational and technical capabilities, both of which provide Apple meaningful advantages over its smartphone competitors.

44. In the interest of providing detailed averments of infringement, TopWire has identified below at least one claim of the '202 Patent to demonstrate infringement. However, the selection of claims should not be considered limiting, and additional claims of the '202 Patent that are infringed by Apple will be disclosed in compliance with the Court's schedule.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 9,859,202 (“’202 Patent”)

45. TopWire incorporates by reference the preceding paragraphs as if fully set forth herein.

46. Apple has directly infringed and continues to directly infringe the '202 Patent under 35 U.S.C. § 271(a). The infringing acts include, but are not limited to, the manufacture, use, sale, importation, and/or offer for sale of the Accused Products with Infringing Semiconductor Structures to practice the claimed invention in the '202 Patent. For example, claim 1 of the '202 Patent¹² recites:

A structure, comprising:

a bottom package substrate;

a top package substrate stacked on top of the bottom package substrate;

at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein the spacer connector comprises

a core substrate;

a plurality of metal pillars, each passing through the core substrate; and

a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;

wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,

the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,

the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and

the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and

¹² Claim 1 is referenced herein for representative purposes. Plaintiff intends to identify additional asserted claims and reserves its right to provide greater detail and scope via its Infringement Contentions at the time required under this Court's scheduling order.

a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein

the bottom chip is mounted to the top surface of the bottom package substrate, and the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

The Infringing Semiconductor Structures meet the recited elements of the structure in Claim 1.

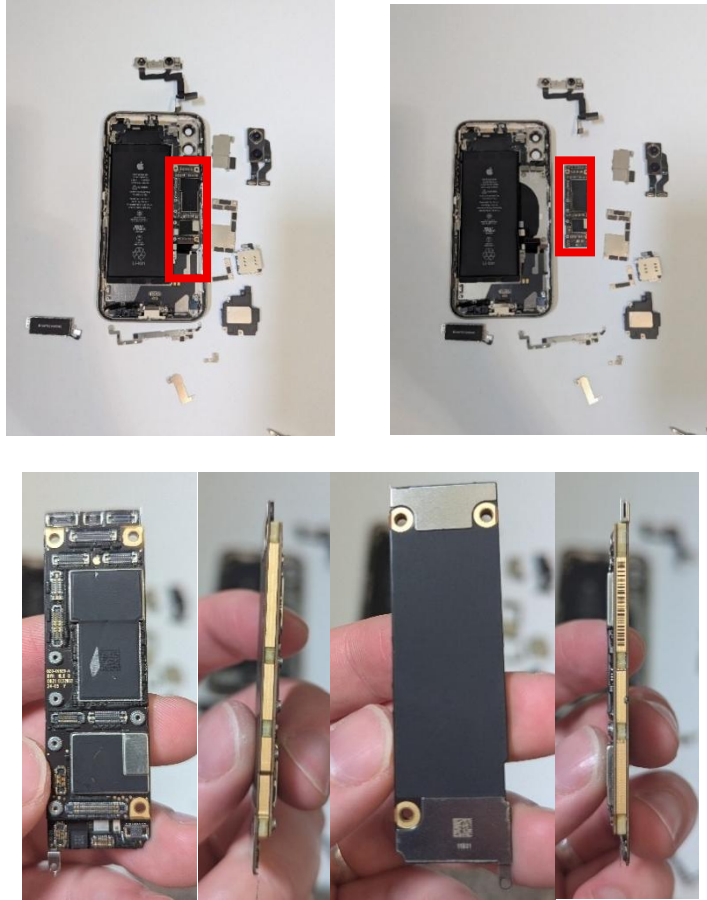
47. For the purposes of showing infringement, the iPhone 11 is selected as a representative Accused Product with an Infringing Semiconductor Structure. However, all iPhone models released since the iPhone X series share a similar structure that infringes in the same way.



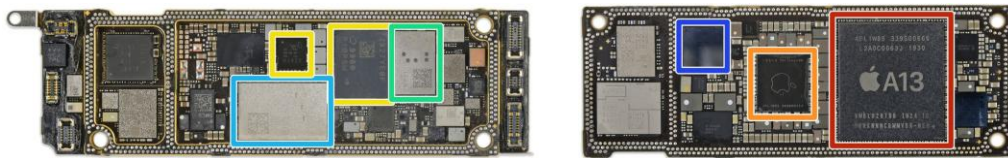
48. Opening the iPhone 11 reveals the internal components of the phone.



49. Removing the shielding and other components exposes the logic board.



50. The logic board includes several chips, including an APL1W85 (Apple's A13 Bionic system-on-chip ("SoC") layered over SK Hynix's LPDDR4X RAM) (red), an Apple APL1092 343S00354 PMIC (orange), an Intel 9960 P10PSM modem / a P10 406 transceiver (yellow), an Apple I7J9, Apple/Murata 339S00647 WiFi/Bluetooth SoC (light blue), and a Cirrus Logic 338S00509 audio codec (dark blue).¹³



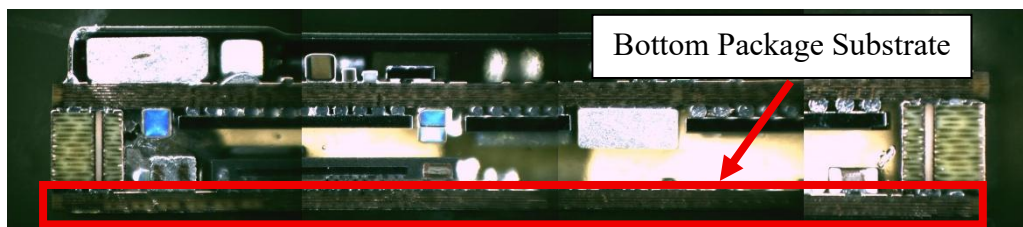
¹³ See iFixit, *iPhone 11 Teardown*, available at <https://www.ifixit.com/Teardown/iPhone+11+Teardown/126192> (last visited November 20, 2025).

51. The logic board in the iPhone 11 is an Infringing Semiconductor Structure. On information and belief, all other logic boards in iPhones sold since the release of the iPhone X series are Infringing Semiconductor Structures.

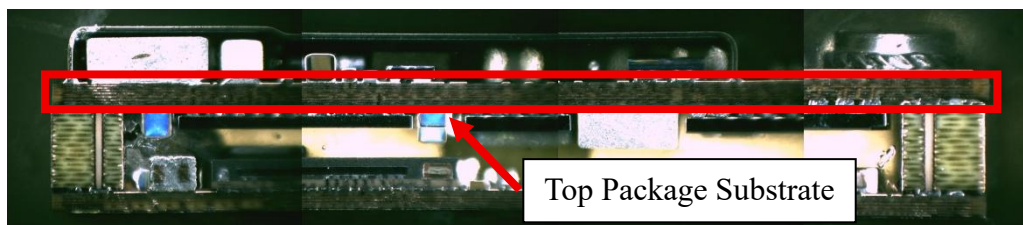
52. A cross-sectioned, microscope view of the logic board in the iPhone 11 shows that the logic board is a structure.



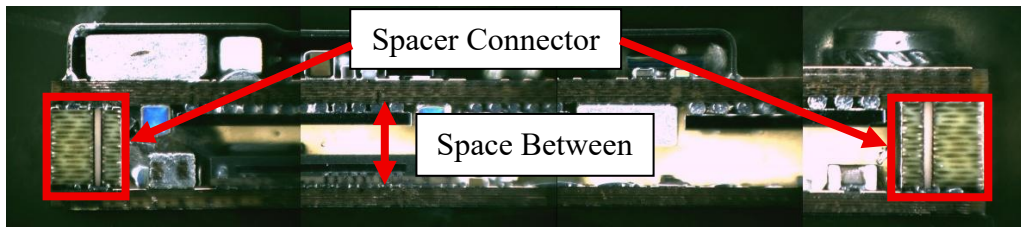
53. The logic board includes a bottom package substrate.



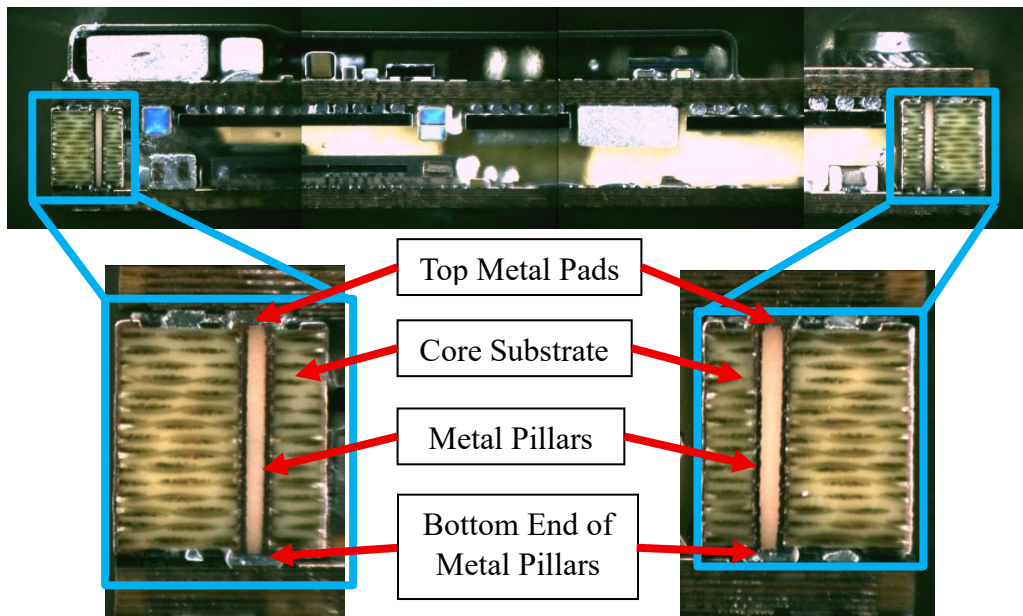
54. The logic board includes a top package substrate stacked on top of the bottom package substrate.

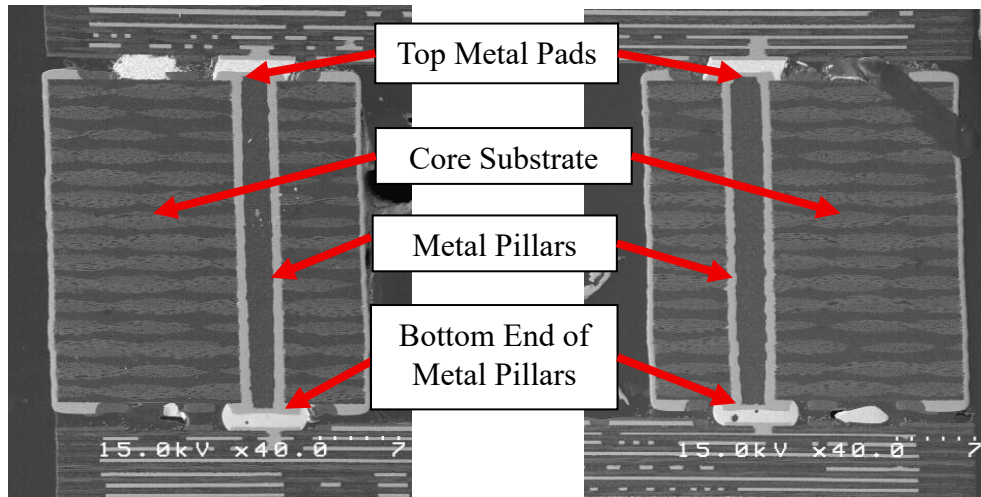


55. The logic board includes at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.

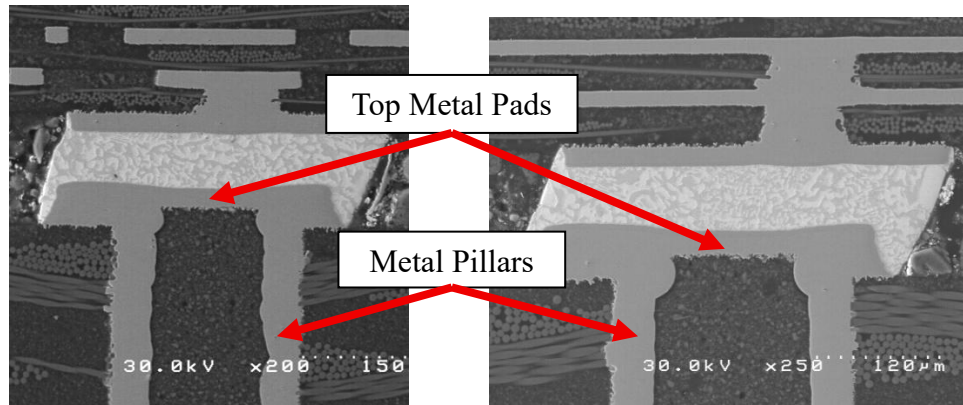


56. The spacer connector in the logic board includes a core substrate, a plurality of metal (e.g., copper) pillars, each passing through the core substrate, and a plurality of top metal (e.g., copper) pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars. A bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.

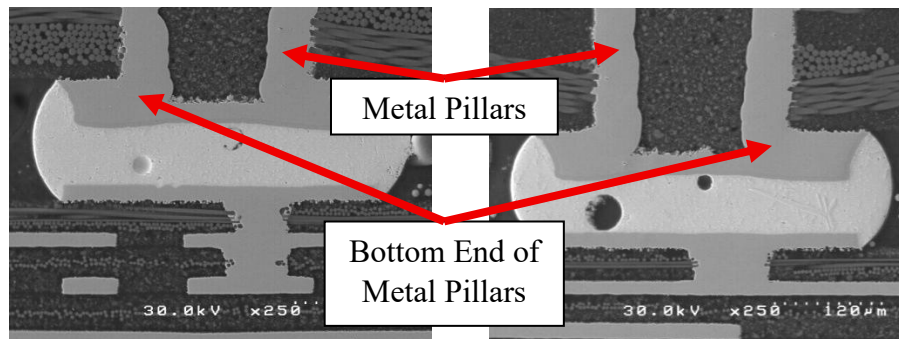




Scanning electron microscope images (“SEM”) of the spacer connectors

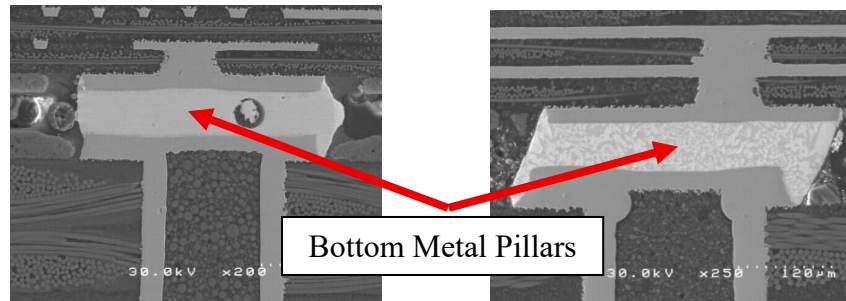


SEM images of the top metal pads and the metal pillars



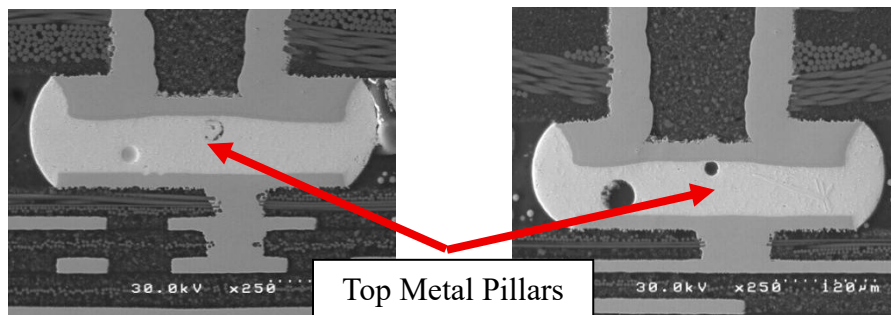
SEM images of the metal pillars and the bottom ends of the metal pillars

57. The top package substrate has, on a bottom surface thereof, a plurality of bottom metal (e.g., tin) pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.



SEM images of the bottom metal pillars

58. The bottom package substrate has, on a top surface thereof, a plurality of top metal (e.g., tin) pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.



SEM images of the top metal pillars

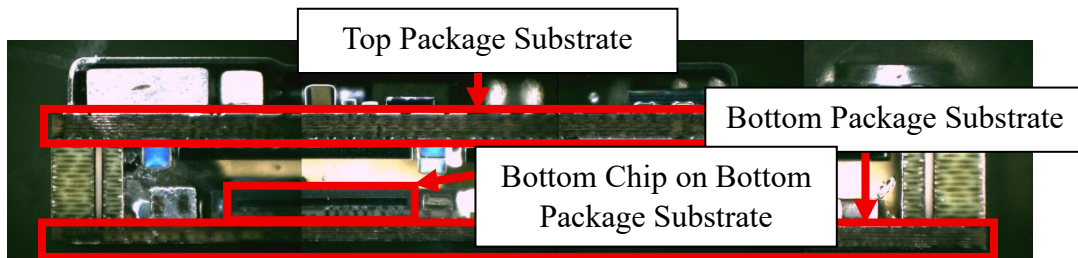
59. The top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate. For example, electrical signals flow between the top package substrate and the bottom package substrate via the plurality of bottom metal pillars, the plurality of metal pillars, and the

plurality of top metal pillars. The electrical signals are in turn routed to different integrated circuits interfacing with the top package substrate and the bottom package substrate.

60. A bottom chip is arranged in the space between the bottom package substrate and the top package substrate.



61. The bottom chip is mounted to the top surface of the bottom package substrate. In other words, the bottom chip is sandwiched between the top package substrate and the bottom package substrate.



62. The spacer connector in the logic board includes two spacer connectors arranged on opposite sides of the bottom chip. The two spacer connectors define a cavity in between the top package substrate and the bottom package substrate.



63. Apple has indirectly infringed and continues to indirectly infringe the '202 Patent because it has induced third parties, including customers, suppliers, end users, distributors, and/or

retailers, to have made, use, offer for sale, sell, and/or import the Accused Products without TopWire's permission in violation of 35 U.S.C. § 271(b).

64. Based on information and belief, third parties, including customers, subsidiaries and wholly- or partially-owned companies, end users, distributors, and/or retailers including Best Buy, T-Mobile, AT&T, Verizon, Walmart, among others, have directly infringed the '202 Patent by having made, using, offering for sale, selling, and/or importing the Accused Products, including, for example, by manufacturing, configuring, using, selling, and operating the Accused Products.

65. Apple induced these third parties' direct infringement by advertising, encouraging, instructing, providing support for, and/or operating the Accused Products for or on behalf of such third parties. For example, on information and belief, Apple induces retailers to import, market, offer to sell, and sell the Accused Products within the United States. Also, Apple publishes specifications, datasheets, instruction manuals, support materials, developer materials, marketing materials, and user guide materials that explain, advertise, instruct on, or provide support for the Accused Products.¹⁴

66. Upon information and belief, Apple knew of the '202 Patent and knew of its infringement of the '202 Patent, including by way of its receipt of the Notice Letter and service of the original complaint in this lawsuit as described above.

67. Apple took the above actions intending to cause infringing acts by these third parties.

¹⁴ For example, see the "iPhone User Guide" (<https://support.apple.com/guide/iphone/welcome/26/ios/26>).

68. If Apple did not know that the actions it encouraged constituted infringement of the '202 Patent, Apple was willfully blind as to its inducing infringement of others. Apple subjectively believed that there was a high probability that others would infringe the '202 Patent.

69. Apple's infringement has also been and continues to be willful and deliberate. On information and belief, Apple deliberately infringed the Asserted Patent and acted recklessly and in disregard of the Asserted Patent by making, having made, using, importing, and offering for sale products that infringe the Asserted Patent. On information and belief, the risks of infringement were known to Apple and/or were so obvious under the circumstances that the infringement risks should have been known. On information and belief, Apple has no reasonable non-infringement theories. On information and belief, Apple has not attempted any design/sourcing change to avoid infringement. Apple has acted despite an objectively high likelihood that its actions constituted infringement of the Asserted Patent. In addition, this objectively-defined risk was known or should have been known to Apple. On information and belief, Apple has willfully infringed and/or continues to willfully infringe the Asserted Patent. Apple exhibited egregious behavior beyond typical infringement in that, despite being aware of its infringement, Apple did not develop any non-infringement theories, did not attempt any design or sourcing change, and did not otherwise cease its infringement.

JURY DEMAND

70. TopWire hereby demands a trial by jury on all issues.

PRAYER

Wherefore, TopWire prays for entry of judgment as follows:

71. A judgment in favor of TopWire that Apple has infringed, directly and/or indirectly, and is infringing, either literally and/or under the doctrine of equivalents, the Asserted Patent;

72. A judgment in favor of TopWire that Apple's infringement has been and continues to be willful; in the alternative, a judgment in favor of TopWire that Apple's infringement is willful and continues to be willful as of the date of this Complaint;

73. An award of damages in favor of TopWire adequate to compensate TopWire for Apple's infringement of the Asserted Patent which shall in no event be less than a reasonable royalty, together with interest and costs as fixed by the court pursuant to 35 U.S.C. § 284;

74. A permanent injunction in favor of TopWire against Apple enjoining Apple, its officers, agents, employees, and others acting in privity, from further infringement of the Asserted Patent;

75. An award of an ongoing royalty for Apple's post-judgment infringement in the event a permanent injunction is not granted;

76. An award of attorneys' fees pursuant to 35 U.S.C. § 285 or as otherwise permitted by law in an amount deemed just and appropriate by the Court;

77. An award of costs and expenses as deemed appropriate by the Court; and
Any other legal or equitable relief to which TopWire is justly entitled.

Dated: February 23, 2026

Respectfully submitted,

/s/ Warren J. McCarty, III

Warren J. McCarty, III

State Bar No.: 24107857

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COUNSEL FOR PLAINTIFFS

CERTIFICATE OF SERVICE

I hereby certify that on the February 23, 2026, a copy of the foregoing was served on the following party electronically through the U.S. District Court, Western District of Texas ECF system to all counsel of record all of whom are Filing Users of the Court's Electronic Filing System.

/s/ Warren J. McCarty, III
Warren J. McCarty, III

EXHIBIT A



US009859202B2

(12) **United States Patent**
Hu

(10) **Patent No.:** **US 9,859,202 B2**
(45) **Date of Patent:** **Jan. 2, 2018**

(54) **SPACER CONNECTOR**

(71) Applicant: **Dyi-Chung Hu**, Hsinchu (TW)

(72) Inventor: **Dyi-Chung Hu**, Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

21/56; H01L 21/60; H01L 23/00; H01L 23/02; H01L 23/12; H01L 23/14; H01L 23/28; H01L 23/31; H01L 23/48; H01L 23/52

USPC 174/262, 251, 252, 255, 258, 260, 261, 174/265; 257/675, 676, 686, 741, 758, 257/774, 777, 778, 787; 361/306.3, 752, 361/760, 773, 783; 29/830, 841
See application file for complete search history.

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H01L 23/498 (2006.01)

H01L 21/48 (2006.01)

H01L 25/10 (2006.01)

(52) U.S. Cl.

CPC **H01L 23/49838** (2013.01); **H01L 21/486** (2013.01); **H01L 21/4846** (2013.01); **H01L 23/49827** (2013.01); **H01L 25/105** (2013.01); **H01L 2224/16227** (2013.01); **H01L 2225/107** (2013.01); **H01L 2225/1023** (2013.01); **H01L 2924/15313** (2013.01); **H01L 2924/15331** (2013.01)

(58) Field of Classification Search

CPC .. H05K 1/02; H05K 1/03; H05K 1/09; H05K 1/11; H05K 1/14; H05K 1/16; H05K 1/18; H05K 3/00; H05K 3/30; H05K 3/32; H05K 3/36; H05K 3/40; H01L 21/02; H01L 21/48; H01L 21/50; H01L

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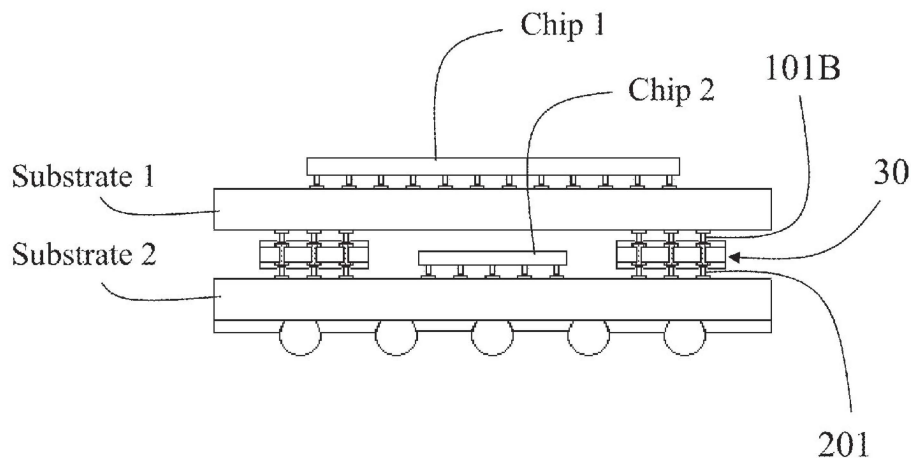
Primary Examiner — Xiaoliang Chen

(74) Attorney, Agent, or Firm — JCIPRNET

(57) ABSTRACT

A fabricating process for a spacer connector is disclosed. A core substrate with a plurality of through holes is prepared. A conductive carrier with a dielectric adhesive configured on a top surface is prepared. The core substrate is then pasted on a top surface of the dielectric adhesive layer. The dielectric adhesive exposed in the through hole is then etched. An electric plating process to form metal pillar in the core substrate is performed using the conductive carrier as one of the electrode.

9 Claims, 14 Drawing Sheets



US 9,859,202 B2

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Fig.1A

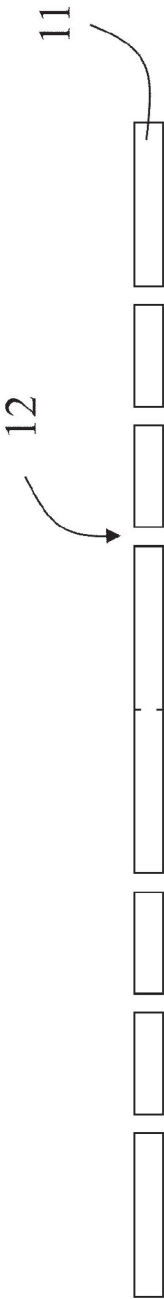
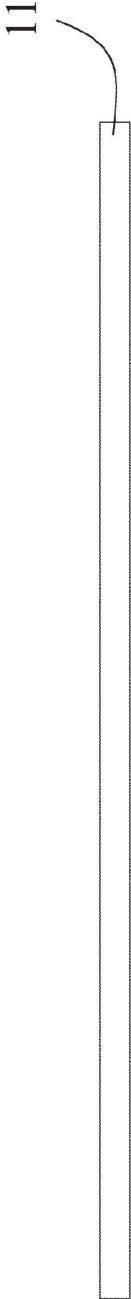


Fig.1B

Fig.2

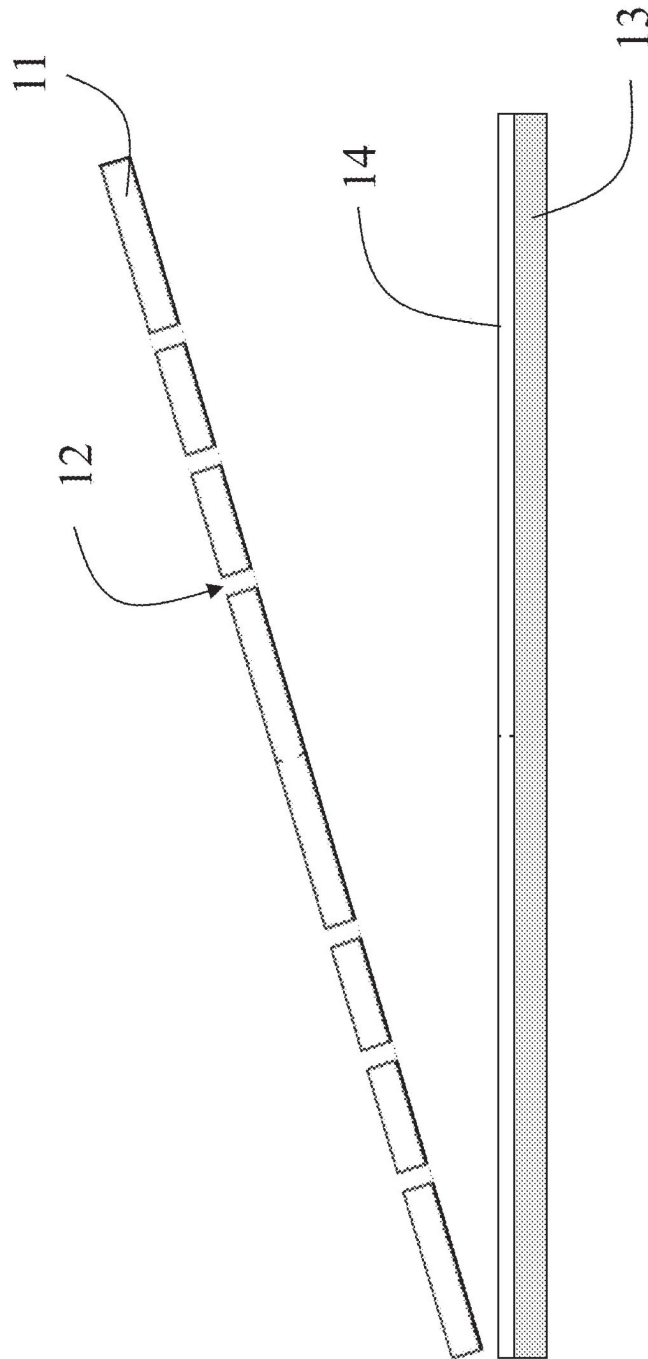


Fig.3A

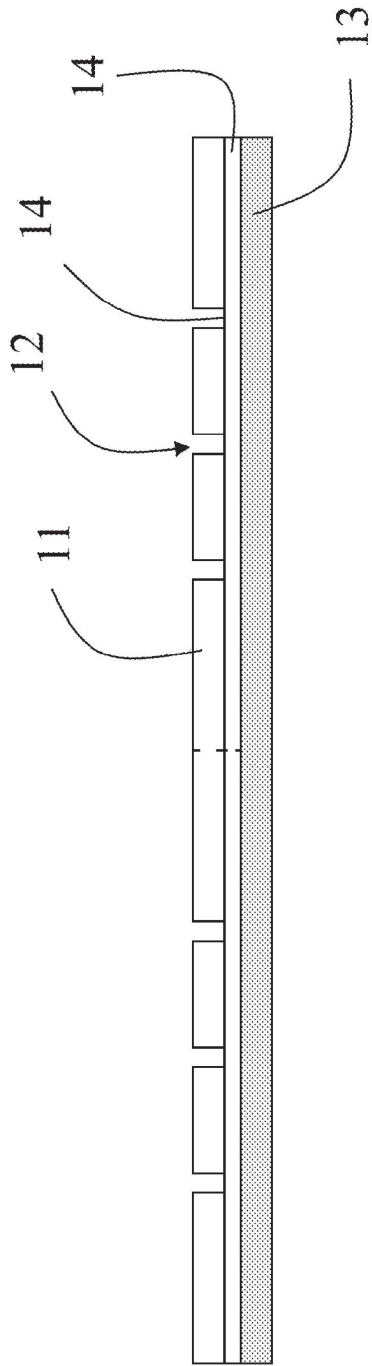


Fig.3B

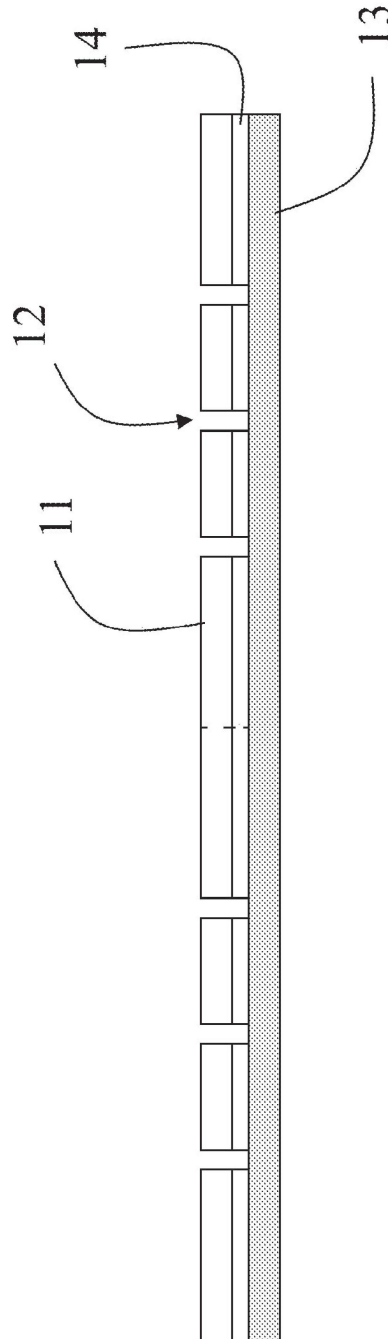


Fig.4A

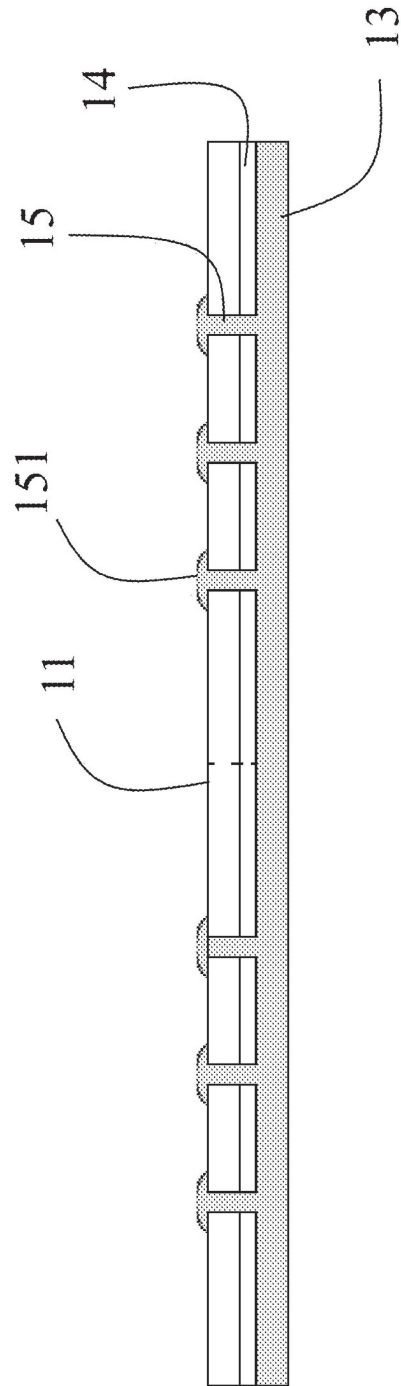


Fig.4B

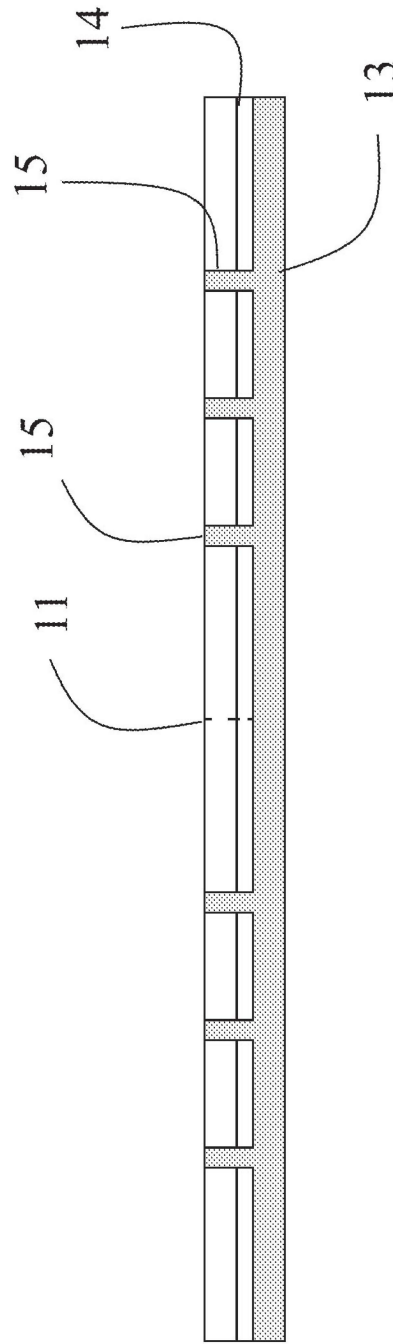


Fig.5A

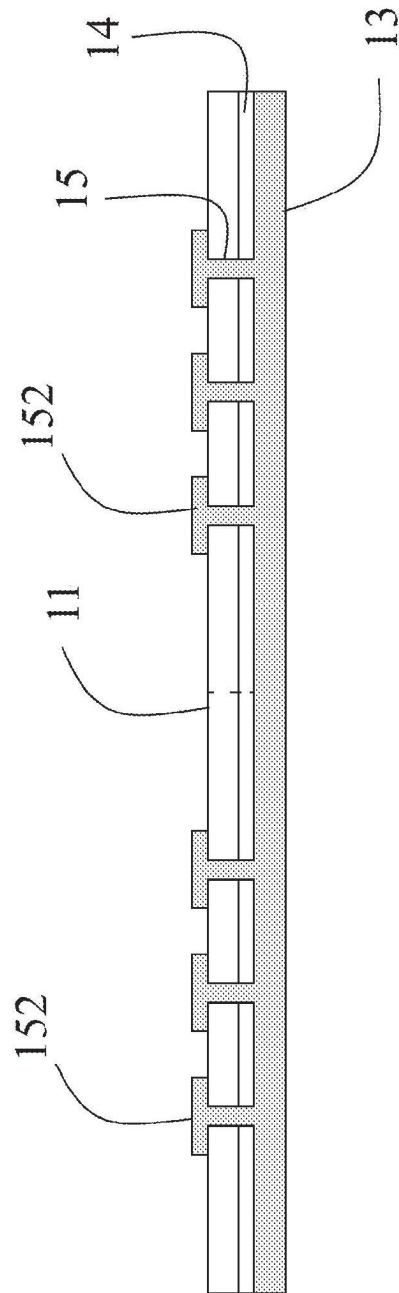


Fig.5B

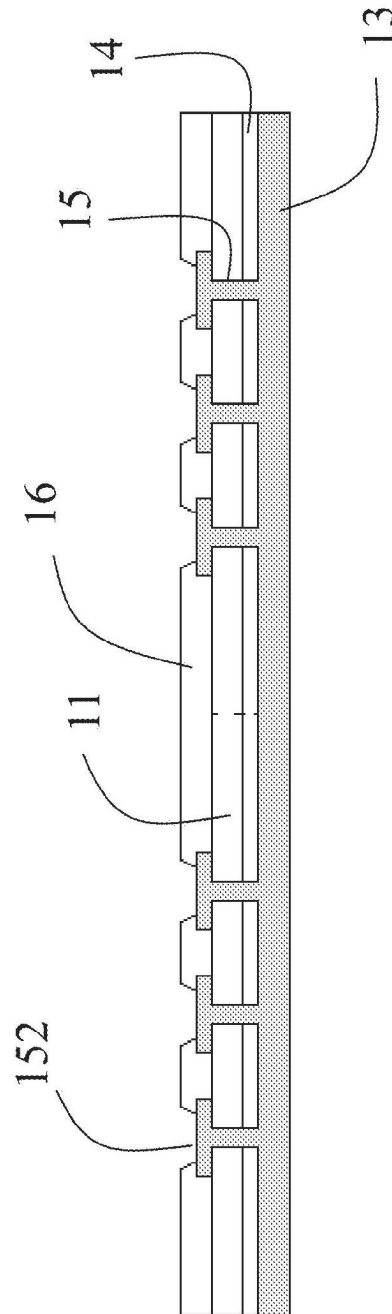


Fig.6A

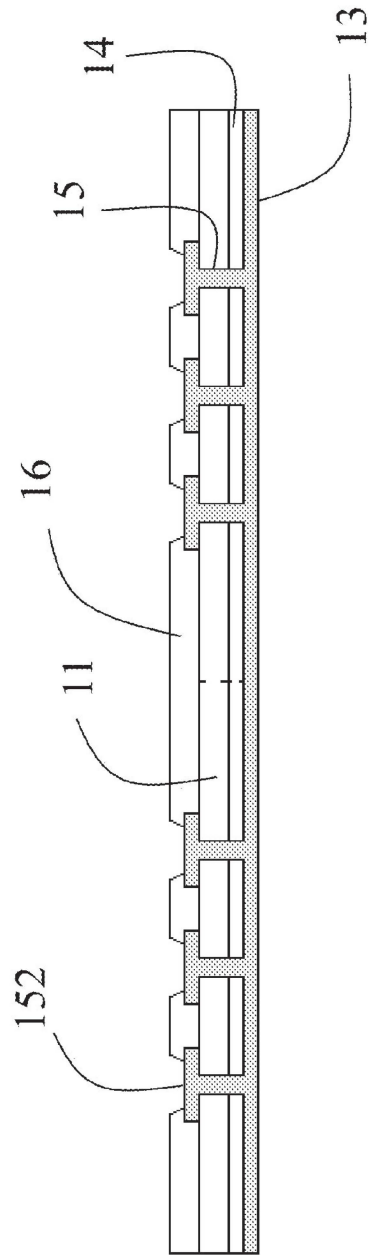


Fig.6B

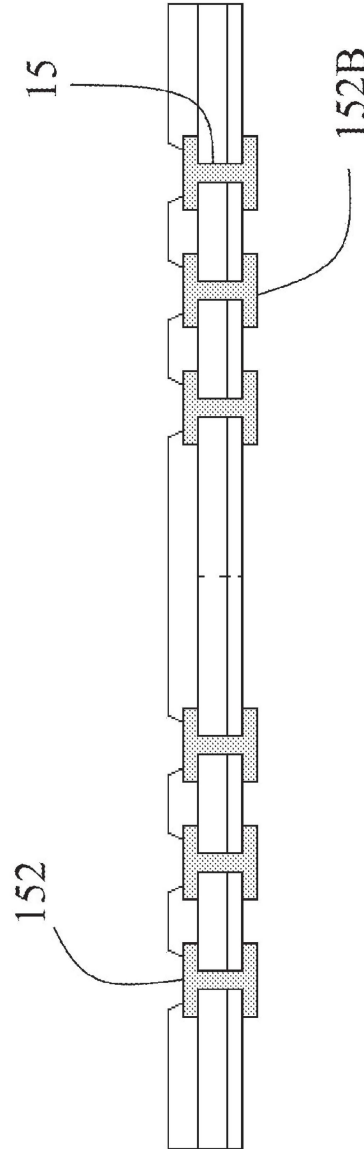


Fig.7A

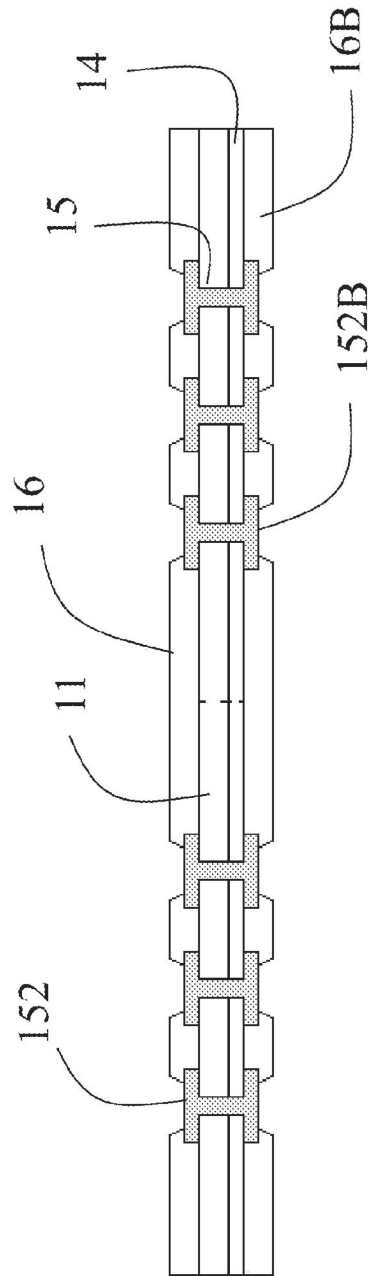


Fig.7B

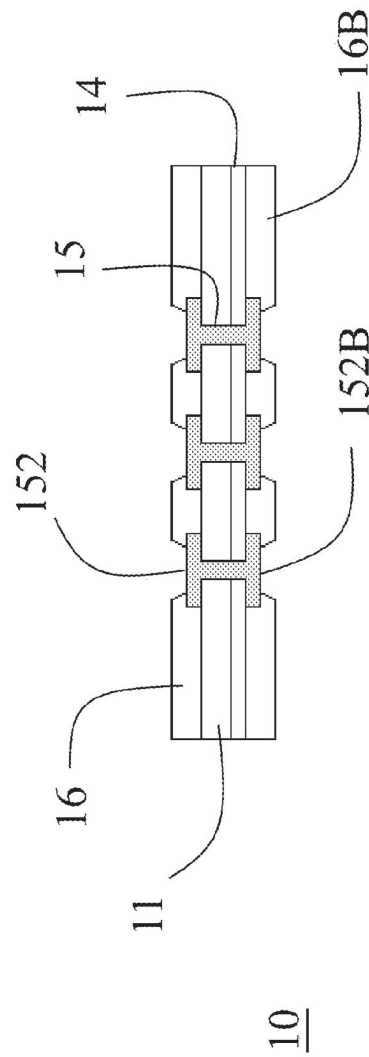


Fig.8

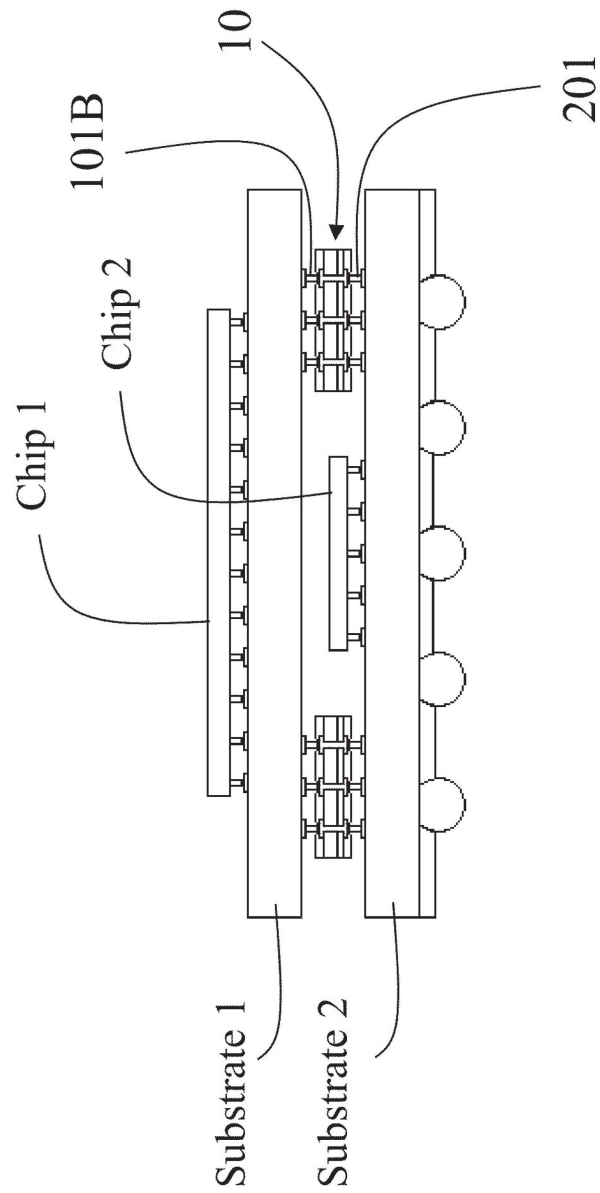


Fig.9A

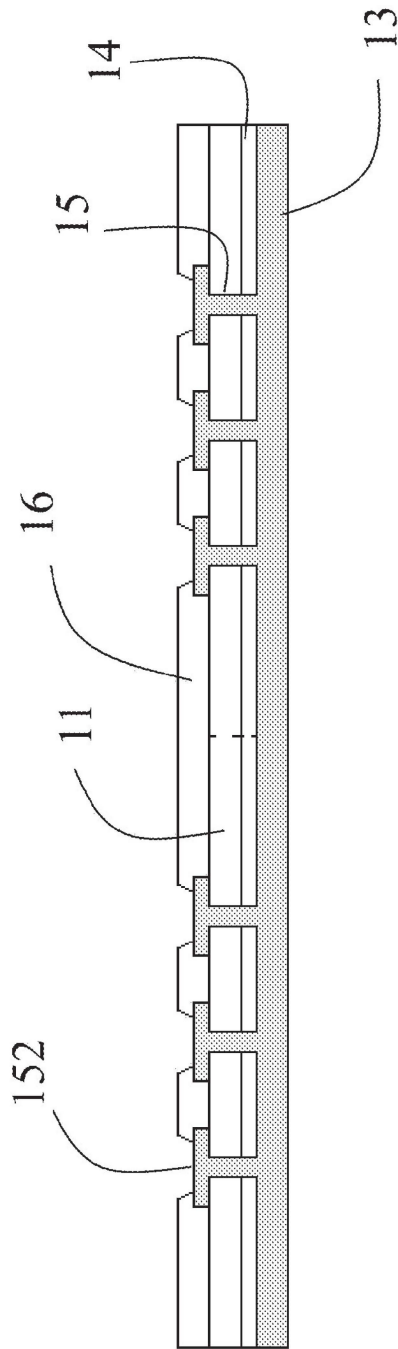


Fig.9B

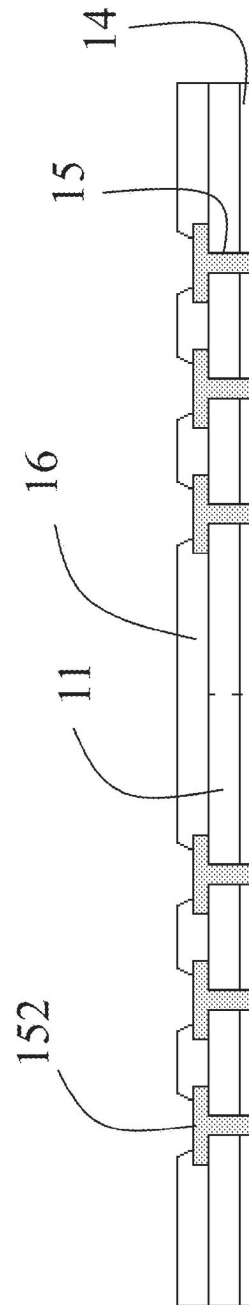
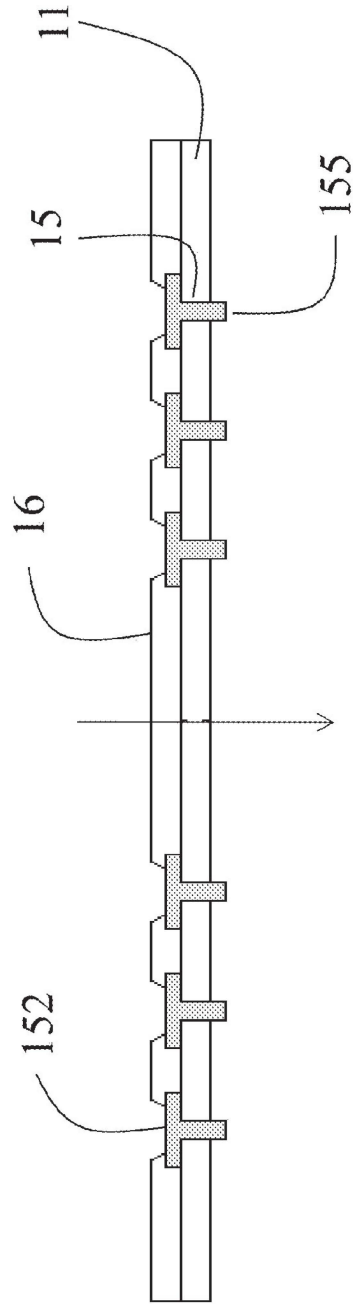


Fig.10A



20

Fig.10B

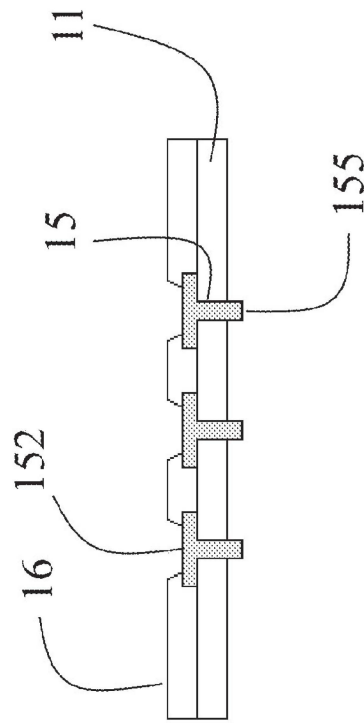


Fig.11

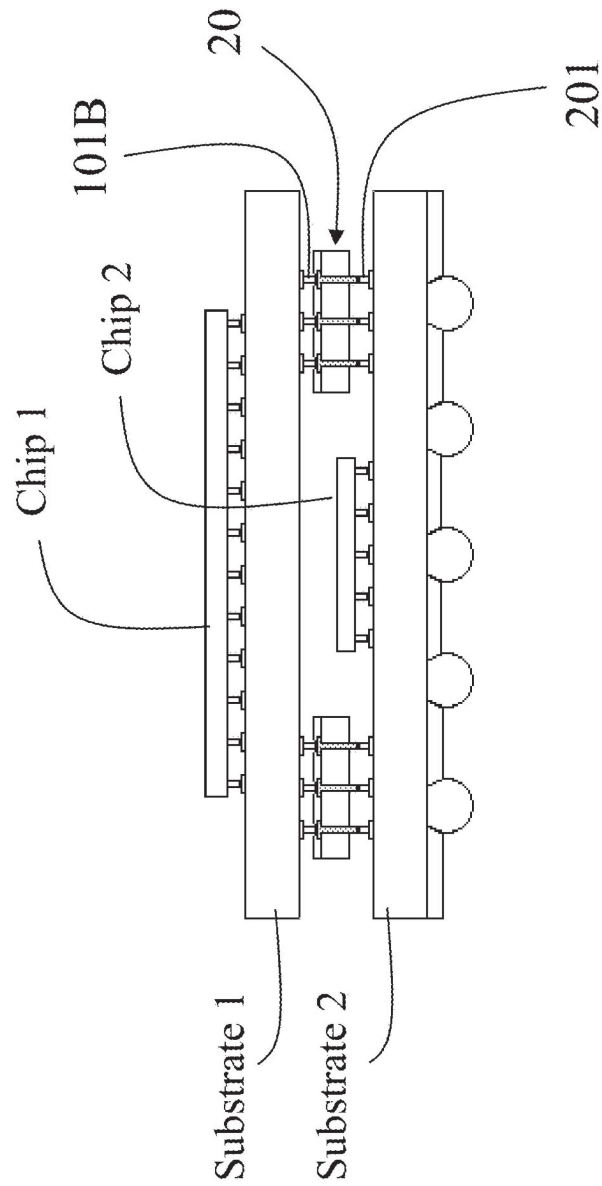


Fig.12A

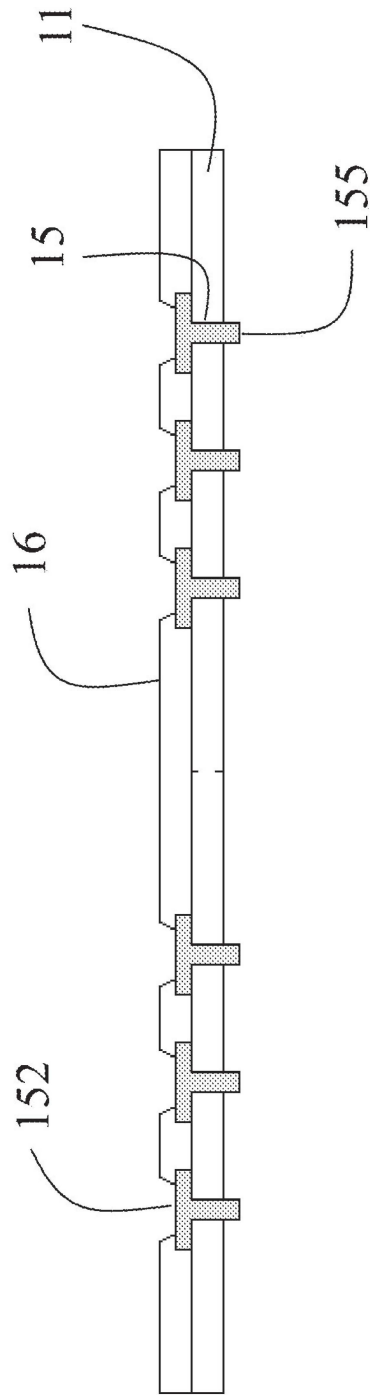


Fig.12B

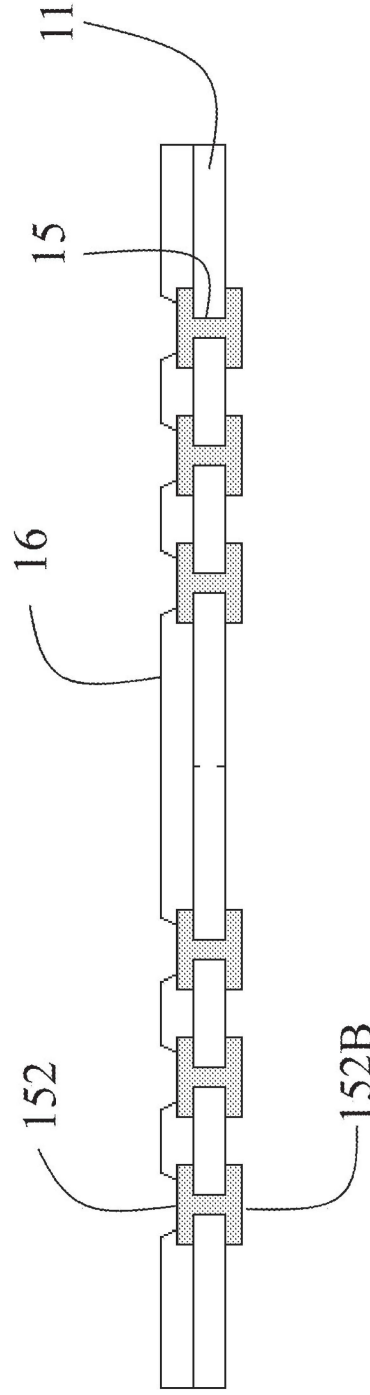


Fig. 13A

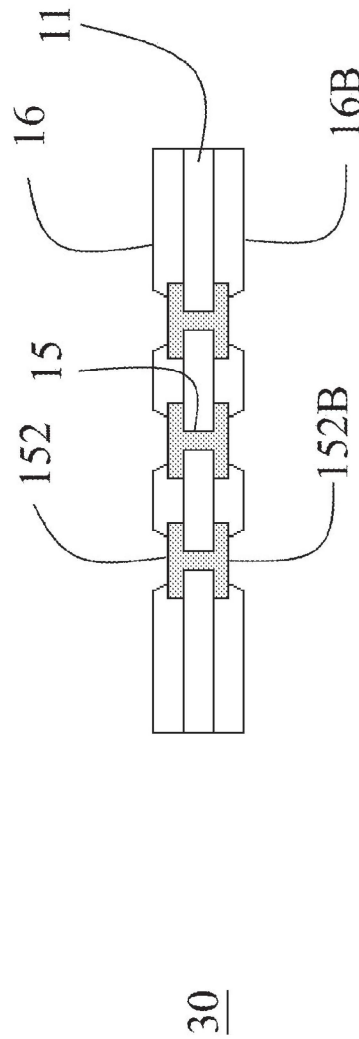
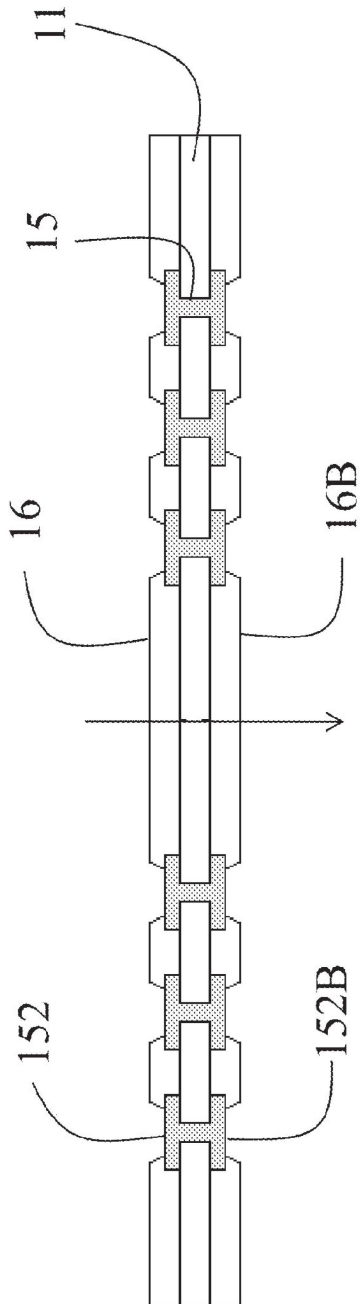
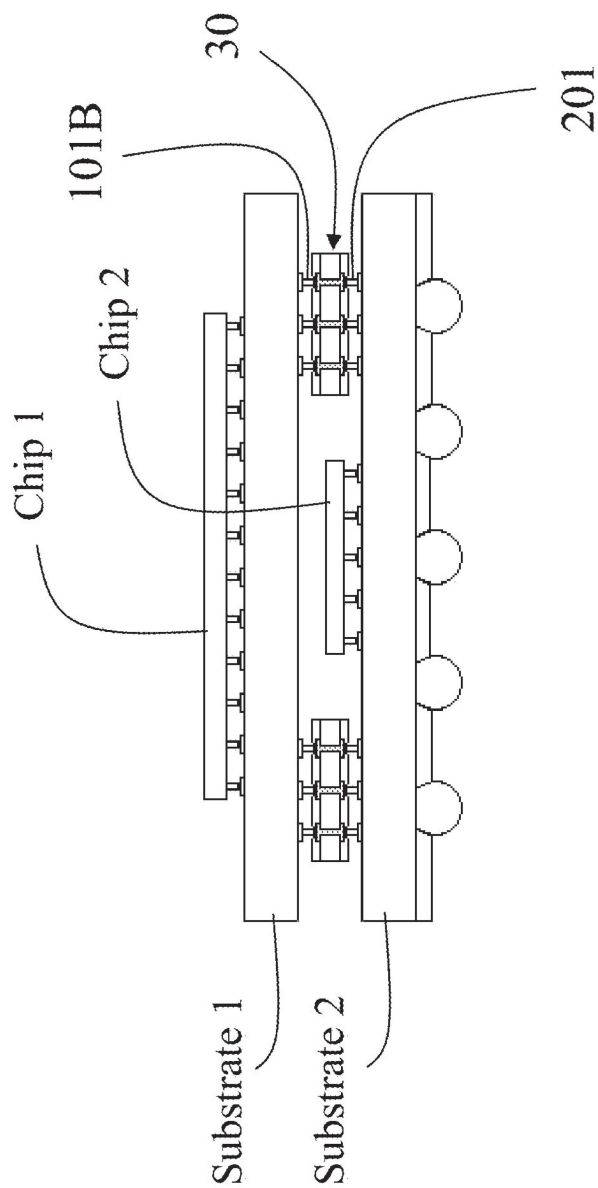


Fig. 13B

Fig. 14



US 9,859,202 B2

1

SPACER CONNECTOR**RELATED APPLICATIONS**

The present application claims the benefit of U.S. Provisional Application No. 62/184,034, filed Jun. 24, 2015, the disclosure of which is hereby incorporated by reference herein in its entirety.

BACKGROUND**Technical Field**

The present invention relates to a fabricating process for making a spacer connector, especially using a conductive carrier in an initial step of the fabrication process.

Description of Related Art

One of the traditional processes for fabricating metal circuitry, a seed layer is often applied before electric plating. In a later process, the seed layer needs to be stripped. However, the stripping of the seed layer reduces the size of the circuits. Although such a circuit reduction is tiny, it is critical when it comes to nanotechnology. A fabricating process without reducing the dimension of a circuitry is one of the popular topics to study for a long time in the semiconductor industry.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A~7A show a fabricating process for a first embodiment according to the present invention.

FIG. 7B shows a first embodiment according to the present invention.

FIG. 8 shows an application for the first spacer connector according to the present invention.

FIGS. 9A~10A show some steps in a fabricating process for a second embodiment according to the present invention.

FIG. 10B shows a second embodiment according to the present invention.

FIG. 11 shows an application for the second spacer connector according to the present invention.

FIGS. 12A~13A show some steps in a fabricating process for a third embodiment according to the present invention.

FIG. 13B shows a third embodiment according to the present invention.

FIG. 14 shows an application for the third spacer connector according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A fabricating process for making a spacer connector without using seed layer is disclosed.

FIGS. 1A~7A show a fabricating process for a first embodiment according to the present invention.

FIG. 1A shows that a core substrate 11 is prepared. The core substrate 11 is made of a material of glass or silicon.

FIG. 1B shows a plurality of openings 12 is made through the core substrate 11.

FIG. 2 shows a temporary conductive carrier 13 is prepared. A dielectric adhesive 14 is applied on a top surface of the conductive carrier 13. The core substrate 11 with through holes 12 is pasted onto the dielectric adhesive 14.

FIG. 3A shows that the core substrate 11 is configured on a top surface of the dielectric adhesive 14.

FIG. 3B shows that the dielectric adhesive 14 on a bottom of each through holes 12 is etched, and a top surface of the conductive carrier 13 is exposed.

2

FIG. 4A shows copper plating is performed using the conductive carrier 13 as one of the electrode. Copper pillar 15 is formed starting from the exposed conductive carrier in each through holes 12. A metal head 151 is configured on a top of the copper pillar 15.

FIG. 4B shows the metal heads 151 are removed.

FIG. 5A shows that top metal pad 152 is formed.

FIG. 5B shows that a passivation 16 is formed on a top of the core substrate 11. The passivation 16 also covers peripheral area of each top metal pad 152 and a central portion of the top metal pad 152 is exposed for electrical connection.

FIG. 6A shows thinning process is performed from a bottom the temporary conductive carrier 13.

FIG. 6B show etching process is performed to the conductive carrier 13 to form a plurality of bottom metal pads 152B. Each of the bottom metal pads 152B is configured on a bottom of a corresponding metal pillar 15.

FIG. 7A shows a bottom passivation 16B is formed on a bottom surface of the dielectric adhesive 14. The bottom passivation 16B also covers peripheral area of each bottom metal pad 152B and a central portion of the bottom metal pad 152B is exposed for electrical connection.

FIG. 7B shows a first embodiment according to the present invention.

FIG. 7B shows a first embodiment of the spacer connector 10 is produced after a singulation process performed on a product of FIG. 7A.

FIG. 8 shows an application for the first spacer connector according to the present invention.

FIG. 8 shows two spacer connectors 10 are configured in between package substrate 1 and package substrate 2. FIG. 8 shows chip 1 is configured on a top center of package substrate 1. Chip 2 is configured on a top center of package substrate 2. Package substrate 1 is stacked on a top of package substrate 2.

The package substrate 1 has a plurality of bottom metal pillars 101B, each metal pillar 101B is electrically coupled to a corresponding top metal pad 152 of the spacer connector 10. The package substrate 2 has a plurality of top metal pillars 201, each metal pillar 201 is electrically coupled to a corresponding bottom metal pad 152B of the spacer connector 10.

FIGS. 1A~5B, 9A~10A show a fabricating process for a second embodiment according to the present invention.

FIGS. 1A~5B have been described in previous paragraphs and are omitted for simplification.

FIG. 9A is the same of the product of FIG. 5B which is a product prepared according to process FIGS. 1A~5A.

FIG. 9B shows the conductive carrier 13 is stripped. The dielectric adhesive 14 is revealed.

FIG. 10A shows the dielectric adhesive 14 is stripped. A bottom end 155 of the copper pillar 15 protruded below a bottom surface of the core substrate 11.

FIG. 10B shows a second embodiment according to the present invention.

FIG. 10B shows a second embodiment of the spacer connector 20 is produced after a singulation process is performed on the product of FIG. 10A.

FIG. 11 shows an application for the second spacer connector according to the present invention.

FIG. 11 shows two spacer connectors 20 are configured in between substrate 1 and substrate 2. FIG. 11 shows chip 1 is configured on a top center of substrate 1. Chip 2 is configured on a top center of substrate 2. Substrate 1 is stacked on a top of substrate 2.

FIGS. 1A~5B, 12A~13A show a fabricating process for a third embodiment according to the present invention.

US 9,859,202 B2

3

FIGS. 1A~5B have been described in previous paragraphs and are omitted for simplification.

FIG. 12A is the same of the product of FIG. 10A.

FIG. 12B shows a plurality of bottom metal pads 152B is formed. Each bottom metal pads 152B is configured on a bottom of a corresponding copper pillar 15.

FIG. 13A shows a bottom passivation 16B is formed on a bottom surface of the core substrate 11. The bottom passivation 16B also covers peripheral area of each bottom metal pad 152B and a central portion of the bottom metal pad 152B is exposed for electrical connection.

FIG. 13B shows a third embodiment according to the present invention.

FIG. 13B shows a second embodiment of the spacer connector 30 is produced after a singulation process is performed on the product of FIG. 13A.

FIG. 14 shows an application for the third spacer connector according to the present invention.

FIG. 14 shows two spacer connectors 30 are configured in between substrate 1 and substrate 2. FIG. 11 shows chip 1 is configured on a top center of substrate 1. Chip 2 is configured on a top center of substrate 2. Substrate 1 is stacked on a top of substrate 2.

While several embodiments have been described by way of example, it will be apparent to those skilled in the art that various modifications may be configured without departs from the spirit of the present invention. Such modifications are all within the scope of the present invention, as defined by the appended claims.

What is claimed is:

1. A structure, comprising:

a bottom package substrate;

a top package substrate stacked on top of the bottom package substrate;

at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein

the spacer connector comprises

a core substrate;

a plurality of metal pillars, each passing through the core substrate; and

a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;

wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,

the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,

the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and

the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and

a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein

4

the bottom chip is mounted to the top surface of the bottom package substrate, and

the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

2. The structure of claim 1, wherein

a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

3. The structure of claim 2, further comprising:

a top chip mounted to the top surface of the top package substrate,

wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

4. The structure of claim 1, wherein

each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

5. The structure of claim 4, wherein

the spacer connector is free of metal pads on the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate, and

each metal pillar among the plurality of metal pillars and the corresponding top metal pad of the spacer connector form a T shape.

6. The structure of claim 4, wherein

the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and

bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

7. The structure of claim 4, wherein

the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate, and the plurality of metal pillars pass through the core substrate and the dielectric layer.

8. The structure of claim 7, wherein

the dielectric layer is a dielectric adhesive in which the core substrate is pasted.

9. The structure of claim 4, wherein

the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars,

the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and

bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

* * * * *

EXHIBIT B



Robert D. Katz
Direct Dial: (469) 278-5999
rkatz@katzfirm.com

July 10, 2025

VIA USPS

Apple Inc.
Attn: Legal Department
One Apple Park Way,
Cupertino, California 95014

Re: Topwire LLC

Dear Sir/Madam,

I hope this letter finds you well. We represent Topwire LLC (“Topwire”) in the enforcement of its intellectual property rights. Topwire is the assignee of United States Patent Nos. 9,737,215 (“the ’215 patent”) and 9,859,202 (“the ’202 patent”) (collectively “the patents”)¹. It has come to the attention of Topwire that Apple Inc. (“Apple”) is selling (directly or indirectly), advertising, offering for sale, or importing into the United States devices (e.g., wearable health tracking devices and hand-held mobile devices) that infringe Topwire’s patents either directly or through intermediaries. The ’215 patent relates to a light-based sensor module for tracking health information such as those used in wearable health tracking devices. For example, it has been brought to Topwire’s attention that Apple sells a line of wearable devices that include a light-based sensor model, such as the Apple Watch (e.g., Apple Watch Series 6 and other series versions). I draw your attention to, for example, claim 1 of the ’215 patent. Additionally, the ’202 patent relates to a spacer connector used to electrically connect two substrates such as those used in hand-held or other smaller form factor electronic devices. For example, it has been brought to Topwire’s attention that Apple sells a line of mobile devices containing processors that utilize a spacer connector to provide for a reduced overall device thickness, such as the Apple iPhone (e.g., iPhone 11, iPhone 13, and other device versions). I draw your attention to, for example, claim 1 of the ’202 patent. Apple may wish to have its patent counsel examine the patents to determine whether a non-exclusive license to the patents is needed.

Please let me know whether Apple is interested in taking a license to the patents. We hope that we will have an opportunity to discuss this matter, and to explain the benefits of an amicable licensing arrangement. I look forward to a productive dialog.

Very truly yours,

A handwritten signature in blue ink, appearing to read 'R. Katz', written over a light blue horizontal line.

Robert D. Katz

cc: Topwire LLC

¹ Copies of the patents are publicly available at <https://patents.google.com>.