

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE, INC.,
Petitioner,

v.

TOPWIRE, LLC,
Patent Owner.

Case No. IPR2026-00303
U.S. Patent No. 9,859,202

PATENT OWNER'S PRELIMINARY RESPONSE

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Exhibit No.	Description
1001	U.S. Patent No. 9,859,202 (“the ’202 Patent”)
1002	Declaration of Dr. Shanfield
1003	U.S. Patent Application Publication No. 2013/0182402 (“Chen”)
1004	U.S. Patent Application Publication No. 2011/0147908 (“Sun”)
1005	U.S. Patent Application Publication No. 2016/0056087 (“Wu”)
1006	U.S. Patent Application Publication No. 2009/0140415 (“Furuta”)
1008	U.S. Patent Application Publication No. 2014/0248742 (“Gonzalez”)
2004	Apple’s Invalidation Contentions, <i>TopWire, LLC v. Apple Inc.</i> , No. 7:25-cv-00551 (W.D. Tex.)
2012	Frank Malloy, “ <i>What is a Silicon Die?</i> ”, Synopsys.com, August 22, 2025, https://www.synopsys.com/glossary/what-is-silicon-die.html

I. INTRODUCTION

Patent Owner TopWire LLC respectfully submits this Preliminary Response and requests that the Board deny institution of inter partes review of U.S. Patent No. 9,859,202 (“the ’202 Patent”) (EX1001). The Petition (Paper 1, “Pet.”) fails to demonstrate a reasonable likelihood of prevailing on any ground, and the Board should decline to institute trial under 35 U.S.C. § 314(a).

The ’202 Patent, titled “Spacer Connector,” claims a package-on-package structure with spacer connectors having metal pillars passing through a core substrate, top metal pads on top ends of the metal pillars, bottom metal pillars on the top package substrate, top metal pillars on the bottom package substrate, and a bottom chip arranged in the space between the two substrates with at least two spacer connectors arranged on opposite sides of the bottom chip. The ’202 Patent addresses the technical challenge of electrically coupling stacked package substrates in a compact, reliable configuration—a chip-level board-on-board structure that was not obvious in view of the prior art.

Petitioner Apple Inc. (“Apple” or “Petitioner”) challenges claims 1–9 of the ’202 Patent across four grounds, each predicated on Chen (EX1003) as the primary reference, combined with either Sun (EX1004) or Wu (EX1005), and further combined with Furuta (EX1006) for dependent claims 5–6. But the Petition is fatally flawed for multiple, independent reasons.

First, Chen discloses a fundamentally different structure from the '202 Patent. Chen is directed to a die-level package-on-package structure using Through-Assembly Via (“TAV”) modules, where a device die is embedded inside a substrate—not a chip mounted between package substrates as claimed. The structural and functional differences between Chen’s TAV modules and the claimed spacer connectors are not mere semantics; they reflect entirely different architectural approaches to package-on-package design.

The Petition improperly conflates “die” and “chip” without any basis in the art. Petitioner cites Gonzalez (EX1008) for the proposition that these terms are interchangeable, but Gonzalez draws no such equivalence. To the contrary, a “die” is an unpackaged piece of silicon containing an integrated circuit, while a “chip” is a die that has been packaged with leads or bumps and placed into a protective casing. *See* EX2012. This distinction matters because the '202 Patent claims a “bottom chip”—a packaged component—arranged between the substrates, not an unpackaged die embedded within a substrate as in Chen.

Second, the Petition relies on unlabeled, ambiguous features in Chen’s Figure 9 that do not clearly disclose metal pillars. Six bulb-shaped components appear in Figure 9 without any label, description, or indication of material composition. Petitioner simply assumes these are “bottom metal pillars” without any support in Chen’s specification. Under *PlaSmart, Inc. v. Kappos*, 482 F. App’x 568, 571 (Fed.

Cir. 2012), patent drawings can only serve as prior art for what they clearly disclose. Chen's Figure 9 clearly discloses nothing about the composition or function of these unlabeled features.

Third, Chen's thin redistribution lines do not disclose, teach, or suggest metal pads. The "RDLs" Petitioner repeatedly point to throughout the Petition are redistribution lines—not, as Petitioner incorrectly claims, redistribution layers. In fact, the redistribution lines are merely one part of the redistribution layers. Chen explains that the "layer" in the redistribution layer is a non-metal, dielectric material. The redistribution lines are derived from metal layers and then inserted into this dielectric material. Accordingly, the redistribution lines are part of a non-metal layer.

For these reasons, and as further detailed below, Patent Owner respectfully requests that the Board deny institution of inter partes review.

II. BACKGROUND

A. Background of the Invention

The '202 Patent, titled "Spacer Connector," was filed on June 23, 2016, and claims priority to U.S. Provisional Application No. 62/184,034, filed June 24, 2015. The patent issued on January 2, 2018. EX1001.

The '202 Patent addresses a challenge in semiconductor packaging: how to electrically couple stacked package substrates in a package-on-package configuration while maintaining a compact and reliable structure.

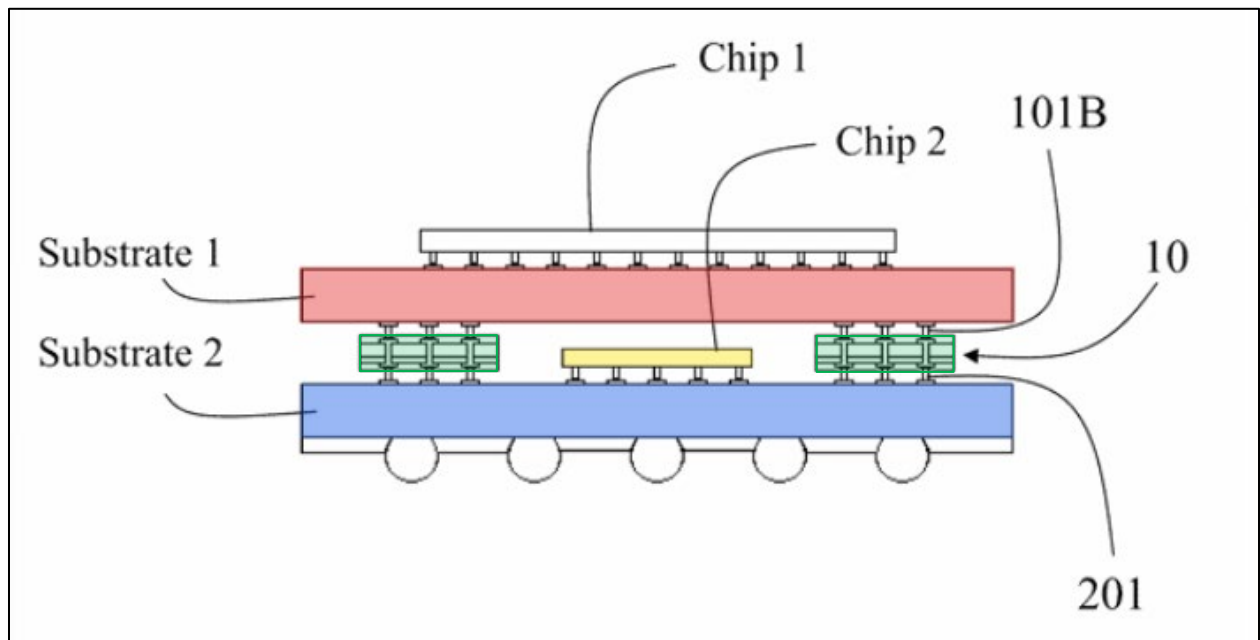
The claimed structure has three principal components: a bottom package substrate (1[A]), a top package substrate stacked above it (1[B]), and at least one spacer connector interposed between them (1[C]). EX1001 at Cl. 1. The spacer connector comprises a core substrate (1[D]), a plurality of metal pillars each passing through the core substrate ([1E]), and a plurality of top metal pads each on the top end of a corresponding metal pillar ([1F]). *Id.* The bottom end of each metal pillar protrudes downwardly from the bottom surface of the core substrate, extending below it. *Id.* (1[H]).

The spacer connector connects to the package substrates above and below through metal pillar interfaces. The top package substrate carries a plurality of bottom metal pillars on its bottom surface, each coupled to a corresponding metal pillar of the spacer connector. *Id.* ([1H]). The bottom package substrate carries a plurality of top metal pillars on its top surface, each coupled to a corresponding metal pillar of the spacer connector. *Id.* ([1I]). This pillar-to-pillar coupling—top package substrate to spacer connector to bottom package substrate—is the electrical backbone of the claimed structure. *Id.* (1[J]).

Critically for this proceeding, claim 1 also requires a bottom chip arranged in the space between the two package substrates and mounted to the top surface of the bottom package substrate (1[K]), with at least two spacer connectors arranged on opposite sides of that chip ([1M]). *Id.* The '202 Patent uses the term “chip”—not

“die”—throughout the specification and claims to describe this component. *See, e.g.*, EX1001 at 2:30–35 (“FIG. 8 shows chip 1 is configured on a top center of package substrate 1”), 2:59–65 (“chip 1 is configured on a top center of substrate 1”). The chip sits in the open space the spacer connectors define, mounted directly to the top surface of the bottom package substrate below it. That open-space, direct-mount architecture is illustrated in Figure 8 of the ’202 Patent.

The claimed structure is illustrated in Figure 8 of the ’202 Patent, which shows two spacer connectors 10 interposed between package substrate 1 (top) and package substrate 2 (bottom), with chip 2 sitting in the open space between the substrates, mounted to the top center of package substrate 2. EX1001, 2:28–42.



EX1001, Figure 8 (annotated).

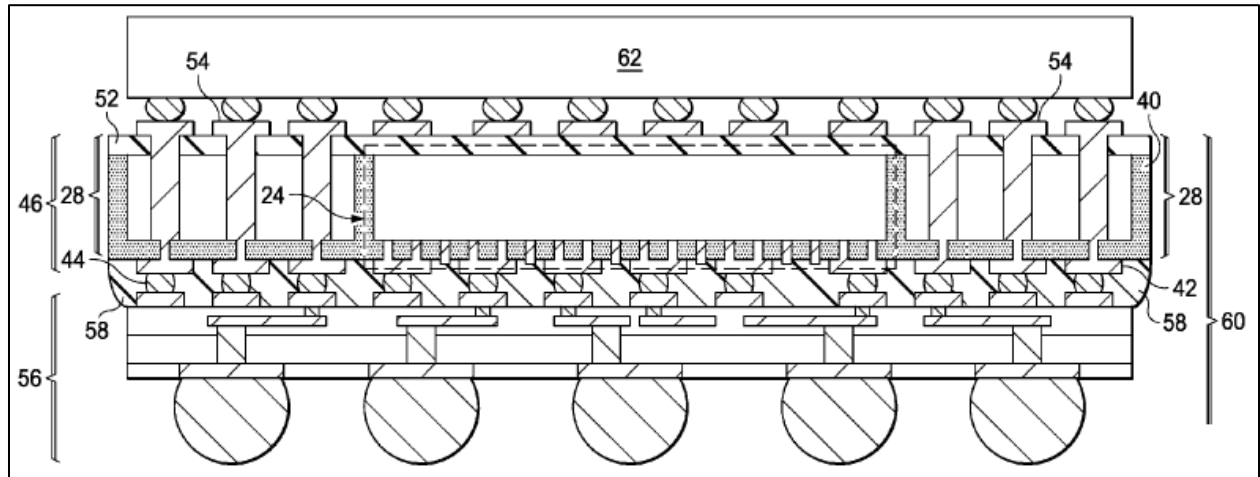
This configuration—a chip-level board-on-board structure—is distinct from prior art approaches that embedded dies within substrates rather than mounting chips between substrates.

B. U.S. Patent Application Publication No. 2013/0182402 (“Chen”)

Chen is directed to a die-level package-on-package structure using Through-Assembly Via (“TAV”) modules. Importantly, Chen’s structure includes a device die embedded *inside* a substrate—not a chip mounted between package substrates as claimed in the ’202 Patent. *See* EX1003 at [0009], FIG. 9. Chen’s TAV modules serve structurally and functionally different roles from the claimed spacer connectors: they provide vertical electrical connections through an assembly that encapsulates a die, rather than connectors interposed between two package substrates with a chip arranged in the space between them.

Moreover, key features that Petitioner relies upon in Chen are not actually taught, disclosed, or suggested. For example, Petitioner points to six unlabeled, bulb-shaped components in Chen’s Figure 9 and asserts—without any support from Chen’s specification—that these represent “bottom metal pillars.” *See* Pet. at 21–23. Chen’s specification says nothing about the material composition or function of these features. *See id.* at 30–32.

Chen’s Figure 9—the figure the Petition relies upon for both the “bottom chip” and “bottom metal pillar” limitations—is reproduced below. EX1003, FIG. 9.



EX1003, FIG. 9.

Petitioner also mislabels components Chen discloses. For example, Petitioner incorrectly refers to “RDLs 54” as “redistribution layers.” *See* Pet. at 18. Chen specifically defines “RDLs 54” as “redistribution *lines*” throughout the specification. *See* EX1003 at [0014], Cl. 1, Cl. 8, Cl. 15.

C. U.S. Patent Application Publication No. 2011/0147908 (“Sun”)

Sun was published on June 23, 2011. Sun discloses a package-on-package structure in which a first substrate is electrically connected to a third substrate through an intermediate second substrate using metal pillars. *See* EX1004 at [0012], [0066].

The Petition combines Sun with Chen in Grounds I and II solely to supply a motivation to replace Chen’s six unlabeled Figure 9 connectors with metal pillars—relying on Sun’s teaching that metal pillars offer finer pitch and superior stand-off stability compared to solder. Pet. at 25–26; EX1004, [0066]. As discussed in Section

V.B.3, that generic observation does not supply the particularized motivation the law requires, particularly where Chen itself identifies its TAV modules—not any unlabeled connector—as the fine-pitch solution in that structure. *See* EX1003 at [0021].

D. U.S. Patent Application Publication No. 2016/0056087 (“Wu”)

Wu was published on February 25, 2016. Wu discloses a package-on-package structure with an organic interposer, in which a top package is mounted to the interposer using connectors Wu describes as “solder balls, pillars, studs, conductive bumps, or the like.” EX1005 at [0030].

The Petition combines Wu with Chen in Grounds III and IV as an alternative to Sun, relying on Wu’s Figure 7 to argue that metal pillars at Chen’s unlabeled connector location would have been obvious. Pet. at 57–64. As discussed in Section V.B.3, a reference that lists pillars as one undifferentiated item in a menu of connector alternatives—with solder balls named first—does not supply a reason to select pillars for a specific, unlabeled location in a different reference’s structure.

E. U.S. Patent Application Publication No. 2009/0140415 (“Furuta”)

Furuta was published on June 4, 2009. Furuta discloses a combination substrate for electrically connecting stacked package substrates using metal posts that penetrate through an interposer. *See* EX1006 at [0003], [0020]–[0021]. The Petition relies on Furuta only for the T-shape limitation [5A] and end-to-end

connection limitation [6A] of dependent claims 5 and 6, combined with Chen and Sun (Ground II) or Chen and Wu (Ground IV). Pet. at 3–4. Because Furuta adds nothing to claim 1, the failure to establish [1H] through Chen is independently fatal to both grounds that invoke it.

III. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of denying institution and finding that Apple has not met its burden to show a reasonable likelihood of prevailing, TopWire submits that the Board need not determine the level of ordinary skill in the art. *Johnson & Johnson Surgical Vision, Inc. v. Alcon Inc.*, IPR2021-01003, 2021 WL 6338373, at *4 (P.T.A.B. Nov. 23, 2021) (denying institution in part because the Board found that it did “not [need to] determine the level of ordinary skill in the art . . .”).

TopWire reserves the right to address the level of ordinary skill in the event the Board institutes trial.

IV. CLAIM CONSTRUCTION IS NOT NECESSARY TO DENY INSTITUTION HERE

Apple asserts in the Petition that it “does not believe that any term requires explicit construction” in this proceeding. Pet. at 12. For purposes of denying institution because Apple has not met its burden to show a reasonable likelihood of prevailing, TopWire submits the Board need not construe any terms of the challenged claims. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir.

2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

TopWire reserves the right to assert claim construction positions if trial is ordered.

V. THE PETITION’S CHALLENGES ARE NOT REASONABLY LIKELY TO PREVAIL

The Board should decline to institute trial because the Petition fails to show a reasonable likelihood of prevailing on any ground. Claim 1 is the sole independent claim challenged by Apple. All four grounds rely on Chen as the primary reference, and none of the Petition’s challenges are reasonably likely to prevail because Apple does not meet its burden to show obviousness based on Chen—whether combined with Sun, Wu, or Furuta.

A. All Grounds fail because Chen does not teach, disclose, or suggest a “bottom chip” as required by limitations [1K] and [1L] (Claims 1–9)

Each of the Petition’s four grounds is fatally deficient because Chen does not teach, disclose, or suggest a “bottom chip arranged in the space between the bottom package substrate and the top package substrate” as required by limitation [1K], or a bottom chip “mounted to the top surface of the bottom package substrate” as required by limitation [1L]. EX1001 at Cl. 1. The Petition’s entire showing on these limitations reduces to a single unsupported equivalence—that a “die” is a “chip”—

propped up by a single phrase from a reference outside the grounds, and two quotations from Chen that defeat, rather than support, the Petition's position. Because all grounds only rely on Chen for these limitations, the deficiency is dispositive of the entire Petition.

1. Chen's "Package Component 24" Is A Bare Device Die—Not The Claimed "Bottom Chip"

The Petition maps limitations [1K] and [1L] to Chen's "package component 24"—a component the Petition itself describes, parenthetically, as "(e.g., CPU die, memory die, device die, etc.)." Pet. at 28. Chen likewise describes package component 24 as including "one or a plurality of device dies" or "a packaging component that includes device die(s)." EX1003, [0009]; Pet. at 28. To bridge the gap between Chen's die and the claimed chip, the Petition offers one sentence: "[i]t is well-known that the terms 'die' and 'chip' are synonymous with one another." Pet. at 29 (citing EX1008, [0007]). But that assertion is wrong, and the reference on which Petitioner relies does not support it.

Dies and chips are different structures according to the plain and ordinary meanings of these terms. For example, one source explains "die" is an unpackaged piece of silicon containing an integrated circuit whereas "chip" is a die that has been packaged with leads or bumps and placed into a protective casing. *See* EX2012. This distinction is well-understood in the art, and Chen's own disclosure—quoted by the

Petition itself—confirms that package component 24 is a die in precisely this sense: “package component 24 may include semiconductor substrate 25 and active devices (such as transistors) 27 at a top surface of semiconductor substrate 25.” EX1003, [0009]; Pet. at 28. A bare semiconductor substrate with transistors formed at its top surface is the very definition of an unpackaged die. The package component 24 is not packaged with leads or bumps or placed into a protective casing before being embedded in Chen’s molded assembly.

2. Neither Gonzalez nor Dr. Shanfield can transform Chen’s die into a “chip”

Gonzalez does not say what the Petition claims. Gonzalez states that “[s]emiconductor packages are used for protecting an integrated circuit (IC) chip or die.” EX1008 at [0007]. That language does not equate the two terms; to the contrary, it distinguishes them by using the disjunctive “or.” And even if Gonzalez could be read as suggesting some overlap between the terms, Gonzalez is not incorporated by reference in Chen, is not relied upon as a prior art reference in any ground, *see* Pet. at 3–4, and cannot be used to rewrite the disclosure of Chen’s specification. A single passing phrase in an unrelated publication is not evidence that interchangeability was “well-known” in the art; conclusory assertions that a claim limitation is supplied by the common knowledge of a skilled artisan must be

supported by record evidence. *See K/S HIMPP v. Hear-Wear Techs., LLC*, 751 F.3d 1362, 1365–66 (Fed. Cir. 2014).

Gonzales also expressly distinguishes between “chip” and “die”—each of which is presumed to have different meanings. *See Apple Inc. v. Omni MedSci, Inc.*, No. 2023-1034, 2024 WL 3084509, at *3 (Fed. Cir. 2024) (“Different claim terms are presumed to have different meanings.”). For example, claim explains that dies are part of a multi-chip package:

1. A method of forming **a multi-chip** package comprising:

attaching **a first die** to a carrier;

forming a first insulating layer over said **first die** and said carrier such that said **first die** is embedded within said first insulating layer;

placing **a second die** above said first insulating layer; and

forming a second insulating layer over said **second die** so that said **second die** is embedded within said second insulating layer.

EX1008 at Cl. 1 (emphasis added). Claim 1 discloses a first die embedded within a first insulating layer and a second die embedded with a second insulating layer. In other words, the first die is packaged within the first insulating layer and the second die is packaged within the second insulating layer. Together, these packaged dies form a “multi-chip package.” This arrangement tracks with the plain and ordinary meaning of “chip” and “die.”

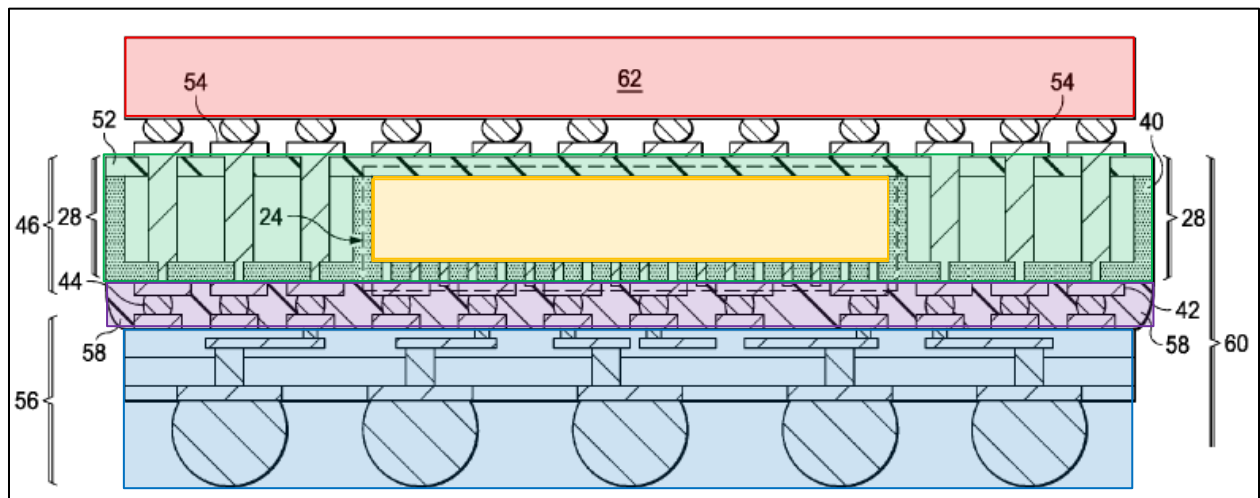
Petitioner's expert, Dr. Shanfield, does nothing to cure this deficiency. His treatment of the issue is a single sentence: “[t]hese device dies meet the claimed ‘chip’ because these two terms are often used interchangeably in the art, which a POSITA would have readily recognized”—supported by nothing but the same Gonzalez phrase. EX1002 at ¶102. Dr. Shanfield identifies no other reference, no industry usage, and no technical reasoning for the proposition that the art “often” treats the terms interchangeably; his remaining paragraphs simply repeat, quotation for quotation, the Petition's citations to Chen. *Compare* Pet. at 28–30 with EX1002, ¶¶99–104. An expert declaration that “merely parrots the words in the Petition” is insufficient to meet Petitioner's burden. *See, e.g., One World Techs., Inc. v. Chevron (HK) Ltd.*, PGR2020-00059, Paper 16, at 41 (P.T.A.B. Dec. 7, 2020).

3. Chen's die is not “mounted to” the bottom package substrate

Even setting aside the die/chip distinction, Chen's structure independently fails limitation [1L], and the Petition's evidence on that point is self-defeating.¹

¹ The Petition's affirmative showing for [1K] fares no better—the only passages Apple cites for that limitation describe what package component 24 is and what the TAV modules do; neither says anything about a chip arranged in any space. *See* 37 C.F.R. § 42.104(b)(4).

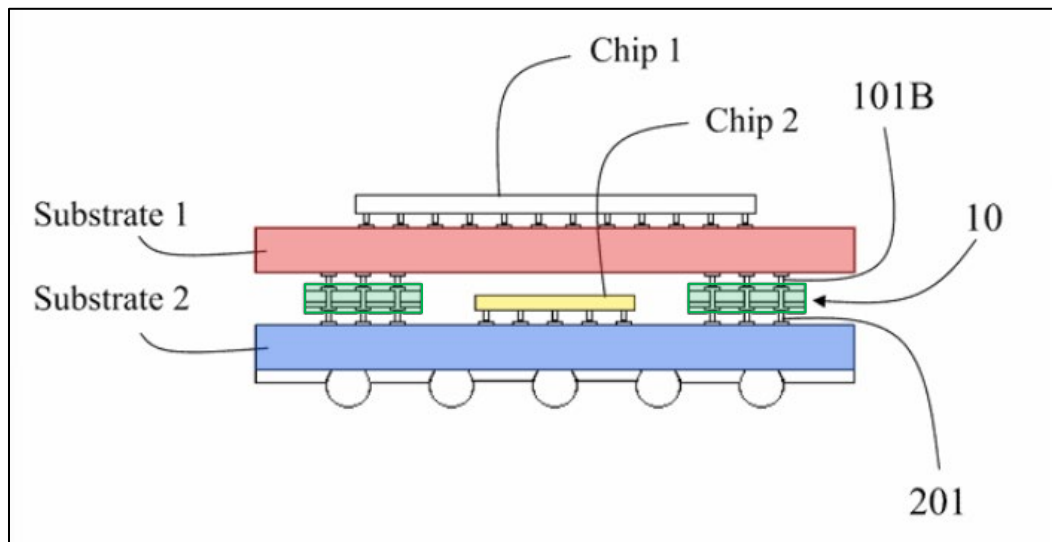
Limitation [1L] requires that the bottom chip be “mounted to the top surface of the bottom package substrate.” The Petition asserts that “package component 24 is mounted on the top surface of the bottom package component 56,” Pet. at 29, but the only two passages it cites affirmatively refute that assertion. Apple quotes Chen’s statements that “the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46” and that “package 46 is bonded to package component 56 to form bottom package 60.” Pet. at 29–30 (quoting EX1003 at [0014], [0018]) (emphasis added). It is the molded package—not the die—that is bonded to package component 56. Chen then interposes still more structure between them: “Polymer 58 is dispensed between package 46 and package component 56.” EX1003 at [0018].



EX1003 at FIG. 9 (annotated).

The die is thus separated from the top surface of the bottom package component by its own redistribution lines, connectors 44, the package's molded polymer body, and **underfill polymer 58**. It is mounted, if anywhere, to the interior of its own molded assembly. Dr. Shanfield offers only the same two quotations without analysis. *See* EX1002 at ¶¶103–04.

The contrast with the claimed invention is dispositive. The '202 Patent claims a structure in which a **chip** sits in the open space defined by the **spacer connectors** and is mounted directly to the top surface of the **bottom package substrate**: “FIG. 8 shows **chip 1** is configured on a top center of **package substrate 1**.” EX1001 at 2:30–35.



EX1001. Figure 8 (annotated).

Chen's architecture—an unpackaged die encapsulated in a molded assembly that is then bonded to a substrate through underfill polymer—is not that structure, and the Petition never confronts the difference.

Because all four grounds rely on Chen's package component 24 to satisfy limitations [1K] and [1L]—Grounds II, III, and IV incorporate, directly or indirectly, the Ground I analysis for claim 1, *see* Pet. at 47, 54, 69, 81–82—Petitioner's failure to establish that package component 24 discloses, teaches, or suggests these limitations is independently fatal to the entire Petition.

B. All Grounds fail because the petition does not establish the “plurality of bottom metal pillars” required by limitation [1H] (Claims 1–9)

Claim 1 separately requires that “the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.” EX1001 at Cl. 1 ([1H]). For this limitation, every ground rests on the same evidence: six unlabeled features in Chen's Figure 9. The Petition is explicit that it “specifically relies on the [six unlabeled connectors](#) colored in Figure 9 of Chen . . . as rendering obvious the claimed ‘plurality of bottom metal pillars.’” Pet. at 21 n.2; *see id.* at 57 n.7 (relying on the same six features for Grounds III and IV). That reliance fails three times over: Chen does not teach, disclose, or suggest anything about the six features; the Petition's fallback assertion that it “would have been obvious to utilize” metal

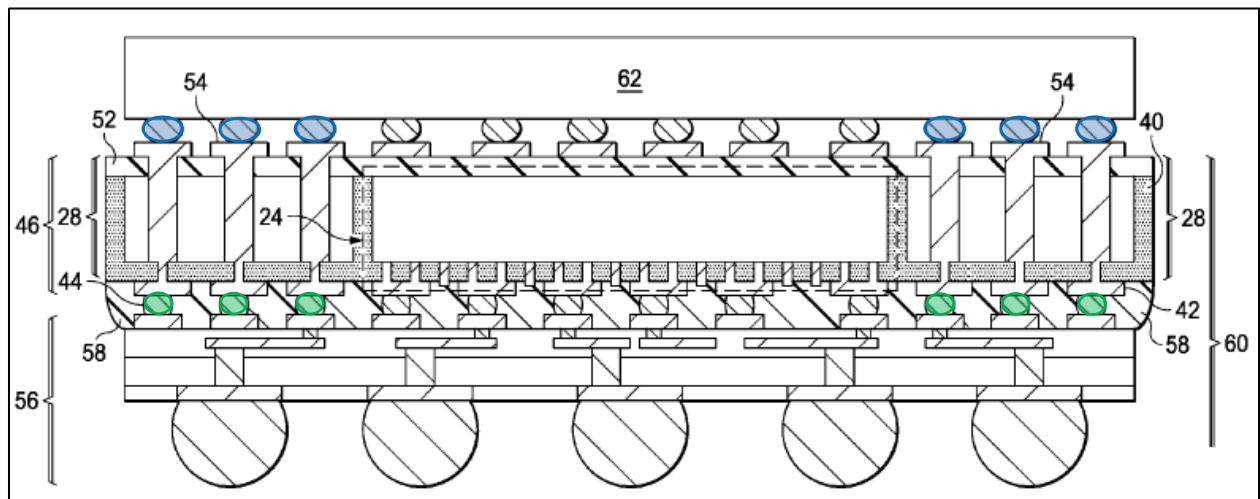
pillars is unsupported attorney argument echoed by a conclusory expert declaration; and neither Sun nor Wu supplies any reason—apart from the '202 Patent's own claims—to modify Chen. Because limitation [1H] is required by claim 1, and every challenged claim depends from claim 1, this failure of proof is independently fatal to all four grounds.

1. Chen does not teach, disclose, or suggest anything about the six unlabeled features in Figure 9

The Petition's primary theory is that Chen itself teaches, discloses, or suggests the claimed bottom metal pillars. It does not, and the Petition concedes as much. Chen's specification never identifies the [six features](#) at all. Paragraph [0019]—the only passage describing Figure 9—states that “FIG. 9 illustrates the bonding of top package component 62 to bottom package 60” and that “TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” EX1003 at [0019]. It assigns the [six features](#) no reference numeral, no name, no structure, and no material composition. The Petition admits the gap: “Chen does not explicitly state that the [unlabeled connectors](#) . . . are metal.” Pet. at 23.

The [six unlabeled features](#) the Petition relies upon are shown in Figure 9 of Chen, annotated below. They appear at the top of the TAV modules 28, between the TAV modules and top package component 62, without any reference numeral, name,

or material designation in Chen's specification. EX1003 at [0019]. Their rounded, dome shape is also visible—characteristic of a reflowed solder bump, not the straight-sided profile of a metal pillar. *Compare* EX1004 at [0066] (metal pillars have “fine pitch and a well defined shape”) *with id.* (solder balls have “a less well defined shape”).



That admission should end the inquiry. Patent drawings “can be used as prior art, without referring to the surrounding description, *only if the prior art features are clearly disclosed by the drawing.*” *PlaSmart, Inc. v. Kappos*, 482 F. App’x 568, 571 (Fed. Cir. 2012) (emphasis added). An unlabeled, undescribed shape in a cross-sectional figure does not “clearly disclose” that the depicted feature is metal—much less that it is a metal *pillar*.

The Petition’s attempt to fill the gap by visual inference—that the [six features](#) “appear nearly identical to [connectors 44](#) on the opposite side of the TAV modules

28,” Pet. at 21—defeats itself. The Petition quotes a single sentence of Chen’s paragraph [0014] stating that “[c]onnectors 44 may also include metal pillars, or metal pillars and solder caps.” Pet. at 23 (quoting EX1003 at [0014]). But the Petition omits what precedes that sentence: in Chen’s lead embodiments, connectors 44 are solder. Chen teaches that “the formation of connectors 44 includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls,” or alternatively “performing a plating step to form solder regions on RDLs 42, and then reflowing the solder regions”—with metal pillars appearing only in a final “may also include” option. EX1003 at [0014]. And the Petition asserts in the same breath that “solder and metal pillars are two distinct structures and are not equivalent to one another.” Pet. at 23 n.3. Taking the Petition’s visual-similarity premise at face value, then, it establishes at most that the six unlabeled features resemble structures Chen forms from reflowed solder—structures that, by the Petition’s own admission, are not metal pillars. The drawing itself confirms the point: the six features are rounded, bulb-shaped domes—the signature of a reflowed solder bump, and the very shape that Petitioner’s own reference attributes to solder rather than to pillars. *See* EX1004 at [0066] (solder balls have a “less well defined shape than the metal pillars,” which have “fine pitch and a well defined shape”).

2. The Petition's "obvious to utilize" fallback is conclusory

Apparently recognizing that Chen discloses no bottom metal pillars, the Petition pivots to a conclusory, one-sentence obviousness theory: "a POSITA would have readily recognized that it would have been obvious to utilize metal pillars as the unlabeled connectors." Pet. at 23. That sentence is the entire analysis. The Petition offers no reason why a person of ordinary skill building Chen's structure would have selected the one optional species mentioned for connectors 44—pillars—over the solder structures Chen actually teaches forming, let alone for different, unlabeled features elsewhere in the structure. "To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). There must be "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). And an appeal to what a skilled artisan "would have readily recognized" cannot serve "as a wholesale substitute for reasoned analysis and evidentiary support" where, as here, it is invoked to supply "a limitation missing from the prior art references." Pet. at 23, 35, 58, and 73; *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361–62 (Fed. Cir. 2016).

Dr. Shanfield adds nothing. His paragraph 88 repeats the Petition's visual comparison, asserts that "[g]iven the mirror symmetry . . . the unlabeled connectors

are just like connectors 44,” quotes the same lone sentence of paragraph [0014], and concludes—again, in a single sentence—that “it would have been obvious to a POSITA to utilize similar metal pillars as the unlabeled connectors just like connectors 44.” EX1002 at ¶88. Like the Petition, Dr. Shanfield never acknowledges that Chen forms connectors 44 from reflowed solder in the embodiments Chen actually describes, and he identifies no facts or data supporting the leap from “unlabeled” to “metal pillar.” Expert testimony that merely repeats the Petition’s conclusory assertions without disclosing the underlying facts or data on which it is based “is entitled to little or no weight.” 37 C.F.R. § 42.65(a); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (P.T.A.B. Aug. 24, 2022) (precedential).

3. Neither Sun nor Wu supplies a reason—apart from the ’202 patent’s claims—to modify Chen

For Grounds I and II, the Petition invokes Sun’s generic observation that metal pillars offer “finer pitch” and better reflow stability than solder balls. Pet. at 25–26 (quoting EX1004 at [0066]); EX1002 at ¶92. But a generic benefit, untethered to the structure being modified, is not a motivation to modify it. *ActiveVideo Networks, Inc. v. Verizon Commc’ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012) (rejecting generic motivation testimony that bore no relation to any specific combination of references and failed to explain why a skilled artisan would have combined them as

the claimed invention does). The Petition never explains why pitch density or stand-off stability mattered at the particular interface where the six unlabeled features sit. Chen answers that question itself: Chen touts its TAV modules—not the unlabeled features—as its fine-pitch solution, explaining that “the connection between top package component 62 and bottom package 60 is through TAV modules 28, rather than large solder balls,” such that “the pitches and the sizes of through-substrate vias 32 may be very small.” EX1003 at [0021]. The proposed combination is also internally inconsistent. The Petition insists the unlabeled features already “appear nearly identical” to connectors 44 that “may also include metal pillars”—yet simultaneously asks the Board to modify those features to be metal pillars. If Figure 9 showed metal pillars, no modification would be needed. The Petition’s need to import pillars from Sun is an admission that Chen does not show them, and the only thing directing a POSITA to place metal pillars at that particular location is claim 1 of the ’202 Patent itself.

Grounds III and IV fare no better with Wu. Wu identifies its “connectors 704” only as an undifferentiated menu of alternatives—“solder balls, pillars, studs, conductive bumps, or the like”—with solder balls listed first. EX1005 at [0030]. The Petition characterizes the proposed swap as “nothing more than simple substitution of one well-known connector,” Pet. at 64, but a simple-substitution rationale presupposes knowing what the original element *is*. The Petition cannot say what

Chen's six unlabeled features are; it therefore cannot show that replacing them with metal pillars substitutes one known element for another, nor explain why a POSITA would pluck "pillars" from Wu's interchangeable list rather than the solder balls Wu names first and Chen actually teaches. Dr. Shanfield again tracks the Petition without independent analysis. *Compare* Pet. at 57–64 with EX1002 at ¶¶163–72.

Because the Petition fails to establish Chen alone anticipates limitation [1H] or renders it obvious in combination with Sun or Wu—and every challenged claim requires that limitation through its dependence from claim 1—institution should be denied on all grounds for this independent reason as well.

**C. All Grounds fail because the petition does not establish the
“plurality of top metal pads” as required by limitation [1F]
(Claims 1–9)**

All of Petition's grounds are fatally deficient because Chen does not disclose, teach, or suggest a “plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars” as required by limitation [1F] EX1001 at Cl. 1. The Petition's evidence for this limitation improperly conflates Chen's redistribution lines (RDL) 54 with “redistribution layers.” This distinction matters because the redistribution lines 54 and the redistribution layers are different structures. The redistribution lines do not disclose, teach, or suggest “top metal pads.” Because all grounds only rely on Chen for these limitations, the deficiency is dispositive of the entire Petition.

1. Chen's "RDLs 54" are redistribution lines—not redistribution layers

Petitioner's flawed analysis begins with the first sentence of the section analyzing limitation [1F]. There, Petitioner explains that "Chen discloses, or at least renders obvious, [1F]. Chen discloses a number of **redistribution layers (RDLs) 54**, each of which are formed on top end of the **through-substrate vias 32**." Pet. at 18. This is incorrect.

Petitioner purports that RDLs 54 are the same as RDLs 42. *See* Pet. at 19 ("[I]t would have been obvious to form **RDLs 54** as **metal pads** because Chen describes that the same corresponding **RDLs 42** on the opposite side of the **TAV modules 28** are deposited as a metal layer and patterned."). But Chen defines RDLs 42 as redistribution *lines*—not redistribution *layers*. *See* EX1003 at [0014] ("Redistribution Lines (RDLs) **42** and connectors **44** are formed to connect to metal posts **26** and **30**"). Chen further reinforces this point by consistently referring to RDLs as redistribution lines throughout the specification. *Id.* at Abstract ("A first **plurality of Redistribution Lines (RDLs)** is underlying a bottom surface of the second and the third portions of the polymer . . ."), Cl. 1 ("a **first plurality of Redistribution Lines (RDLs)** underlying a bottom surface of the second and the third portions of the polymer"), Cl. 8 ("a **first plurality of Redistribution Lines (RDLs)** under the molding compound and electrically coupled to the device die and

the plurality of through-vias in the TAV module . . .”), Cl. 15 (“forming **a first plurality of Redistribution Lines (RDLs)** over the polymer and connected to the metal posts of the device die and the metal posts of the TAV module . . .”).

2. Chen’s “RDLs 54” do not disclose teach or suggest “a plurality of top metal pads”

The distinction between redistribution lines and redistribution layers matters because these are different structures. Indeed, Chen explains that “TAV modules **28** may include redistribution layer(s) that include redistribution lines . . .” *Id.* at [0011]. In other words, redistribution lines are merely a component of the redistribution layers. The RDLs 54 are merely thin trace lines, none of which Chen describes as metal lines; they do not disclose, teach, or suggest “a plurality of top metal pads.” The “layer” in the redistribution layer is a dielectric layer, a non-metal material. Referring to Figure 7, Chen explains that “dielectric layer **52** is formed on the illustrated top surface of package **46**” and then “RDLs **54** are then formed on dielectric layer **52** and connected to RDLs **54**.” *Id.* at [0017].

Petitioner attempts to remedy this shortcoming by explaining how “**RDLs 42** may be formed by depositing a metal layer, and then patterning the metal layer.” Pet. at 19 (quoting EX1003, [0014]). Putting aside Chen’s explanation that RDLs 54 are lines within the non-metal dielectric layer 52, this undermines, rather than

supports, Petitioner's argument. The RDLs 42 are not metal layers; they are thin trace lines derived from patterning metal layers.

Dr. Shanfield's opinions on this limitation simply regurgitate the points the petition makes. *See generally* EX1002, 36–37. He cites the same passages from Chen—many of which undermine his opinion for the reasons explained above—to conclude that redistribution lines 54 disclose, teach, or suggest “a plurality of top metal pads.” *Id.* at 36. And he makes the same incorrect claim that the redistribution lines 54 are metal layers, even though Chen explains that the redistribution lines 54 are lines derived from metal layers. *Id.* at 37.

Because all four grounds rely on Chen's redistribution lines 54 to satisfy limitation [1F]—Grounds II, III, and IV incorporate, directly or indirectly, the Ground I analysis for claim 1, *see* Pet. at 47, 54, 56, 81–82—Petitioner's failure to establish that the redistribution lines 54 disclose, teach, or suggest this limitation is independently fatal to the entire Petition.

VI. CONCLUSION

For any of these reasons, the Board should deny institution of the Petition.

Respectfully submitted,

Dated: June 22, 2026

/s/ Zachary Grinovich

Zachary Grinovich
Reg. No. 80,584
Attorney for Patent Owner
TopWire, LLC

AHMAD ZAVITSANOS & MENSING PLLC
2001 Ross Avenue, Suite 520
Dallas, TX 75201
Telephone: (214) 800-4501
Facsimile: (713) 655-0062

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITS

Pursuant to §42.24(d) and the Director's Memorandum on Interim Processes for PTAB Workload Management, the undersigned certifies that this paper no more than 14,000 words, not including the portions of the paper exempted by §42.24(b). According to the word-processing system used to prepare this paper, the paper contains 5,765 words.

Dated: June 22, 2026

/s/ Zachary Grinovich

Zachary Grinovich
Reg. No. 80,584
Attorney for Patent Owner
TopWire, LLC

AHMAD ZAVITSANOS & MENSING PLLC
2001 Ross Avenue, Suite 520
Dallas, TX 75201
Telephone: (214) 800-4501
Facsimile: (713) 655-0062

CERTIFICATE OF SERVICE

I hereby certify that the foregoing document and Exhibits listed on Patent Owner's Exhibit List were served on June 22, 2026, by electronic mail to the following:

Lead Counsel	Back-up Counsel
Yung-Hoon Ha Reg. No. 56,368 Desmarais LLP 230 Park Ave New York, NY 10169 Telephone: (212) 351-3400 Email: yha@desmaraisllp.com	Cosmin Maier Reg. No. 75,387 Desmarais LLP 230 Park Ave New York, NY 10169 Telephone: (212) 351-3400 Email: cmaier@desmaraisllp.com

Respectfully submitted,

Dated: June 22, 2026

/s/ Zachary Grinovich

Zachary Grinovich
Reg. No. 80,584
Attorney for Patent Owner
TopWire, LLC

AHMAD ZAVITSANOS & MENSING PLLC
2001 Ross Avenue, Suite 520
Dallas, TX 75201
Telephone: (214) 800-4501
Facsimile: (713) 655-0062