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(54) **SPACER CONNECTOR**

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(51) **Int. Cl.**

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H01L 23/498	(2006.01)
H01L 21/48	(2006.01)
H01L 25/10	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/49838*** (2013.01); ***H01L 21/486*** (2013.01); ***H01L 21/4846*** (2013.01); ***H01L 23/49827*** (2013.01); *H01L 25/105* (2013.01); *H01L 2224/16227* (2013.01); *H01L 2225/107* (2013.01); *H01L 2225/1023* (2013.01); *H01L 2924/15313* (2013.01); *H01L 2924/15331* (2013.01)

(58) **Field of Classification Search**

CPC .. H05K 1/02; H05K 1/03; H05K 1/09; H05K 1/11; H05K 1/14; H05K 1/16; H05K 1/18; H05K 3/00; H05K 3/30; H05K 3/32; H05K 3/36; H05K 3/40; H01L 21/02; H01L 21/48; H01L 21/50; H01L 21/56; H01L 21/60; H01L 23/00; H01L 23/02; H01L 23/12; H01L 23/14; H01L 23/28; H01L 23/31; H01L 23/48; H01L 23/52

USPC 174/262, 251, 252, 255, 258, 260, 261, 174/265; 257/675, 676, 686, 741, 758, 257/774, 777, 778, 787; 361/306.3, 752, 361/760, 773, 783; 29/830, 841

See application file for complete search history.

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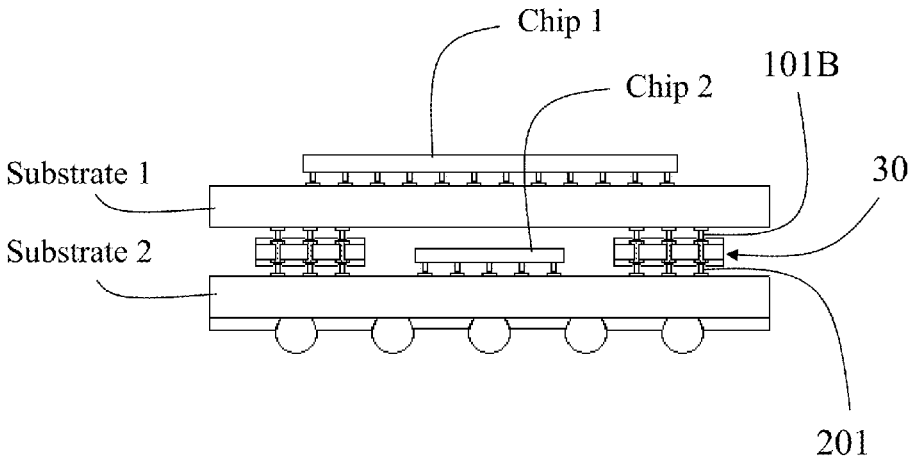
(57) **ABSTRACT**

A fabricating process for a spacer connector is disclosed. A core substrate with a plurality of through holes is prepared. A conductive carrier with a dielectric adhesive configured on a top surface is prepared. The core substrate is then pasted on a top surface of the dielectric adhesive layer. The dielectric adhesive exposed in the through hole is then etched. An electric plating process to form metal pillar in the core substrate is performed using the conductive carrier as one of the electrode.

9 Claims, 14 Drawing Sheets



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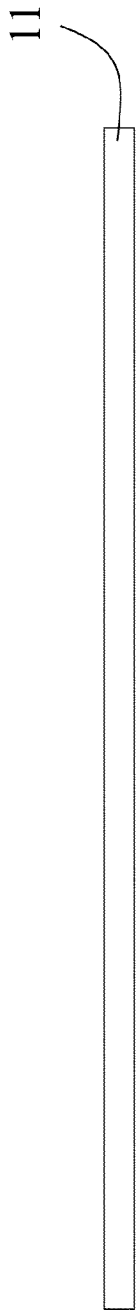


Fig.1A

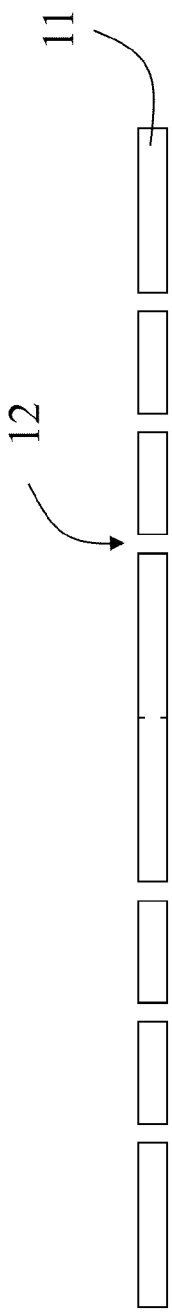


Fig.1B

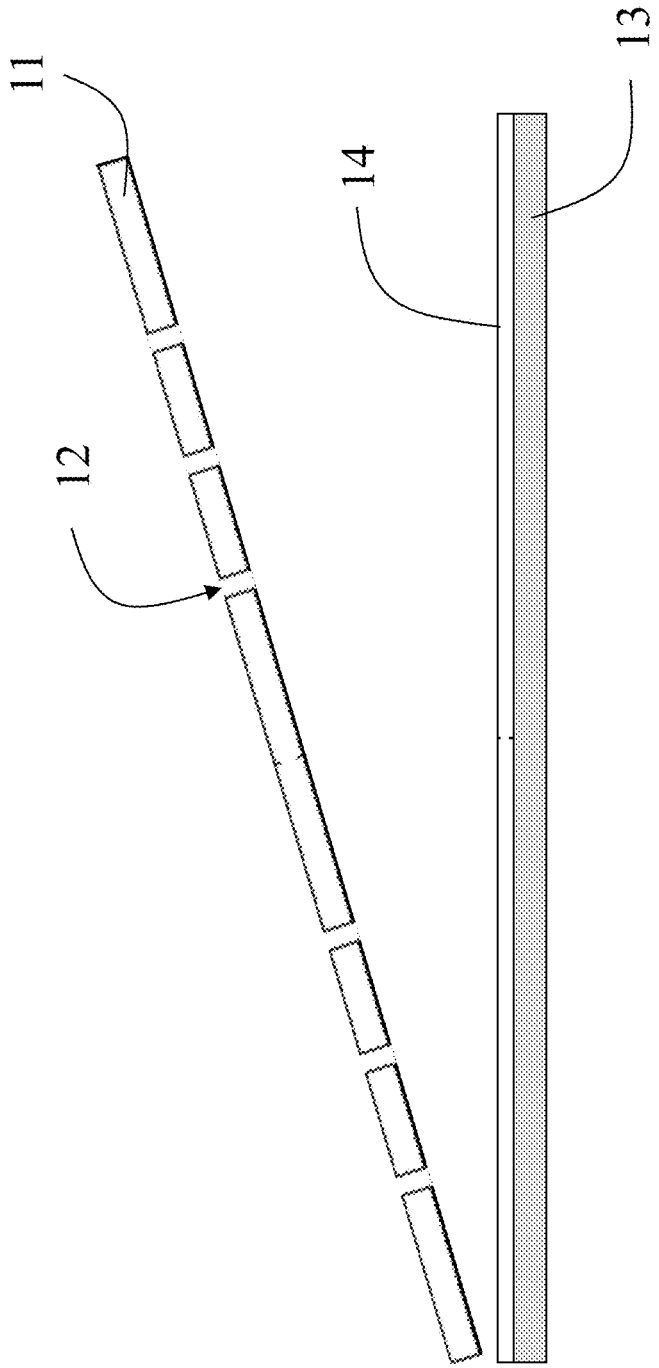


Fig.2

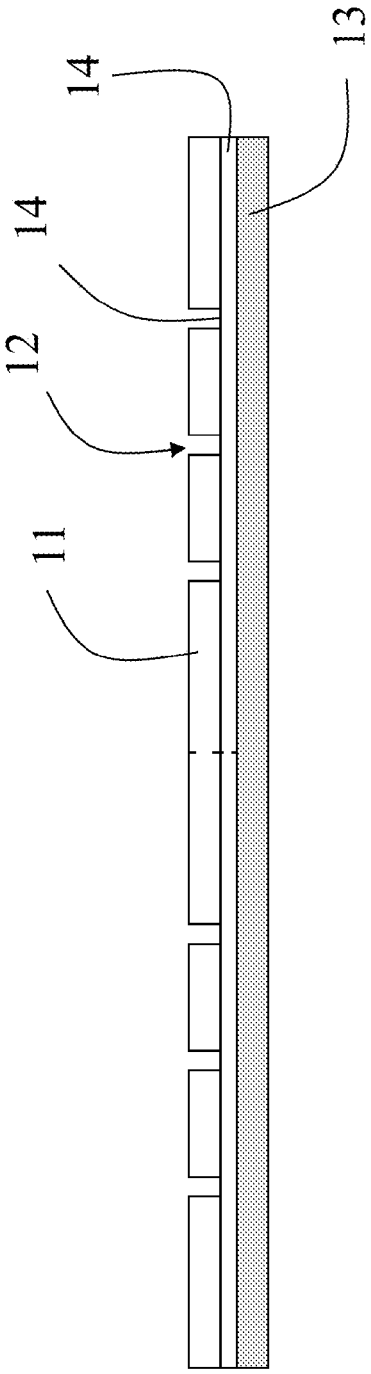


Fig.3A

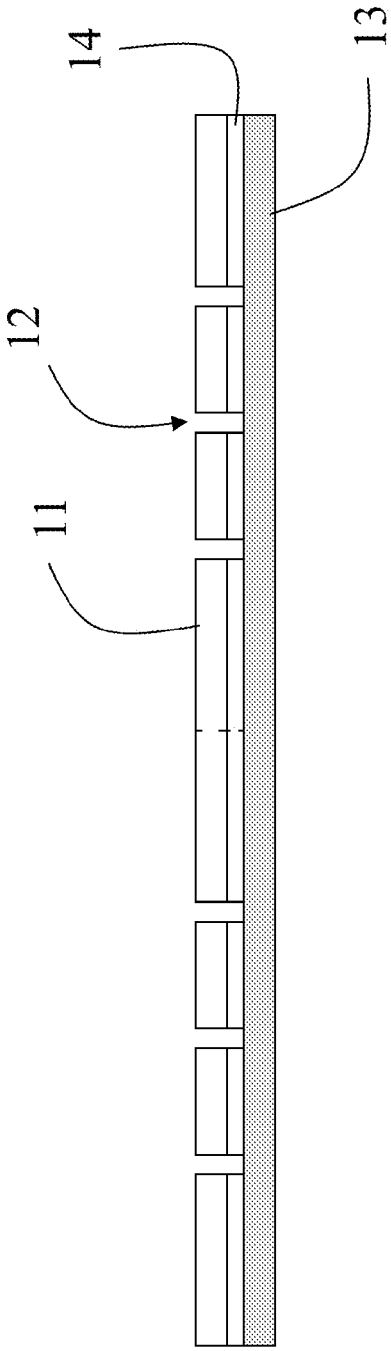


Fig.3B

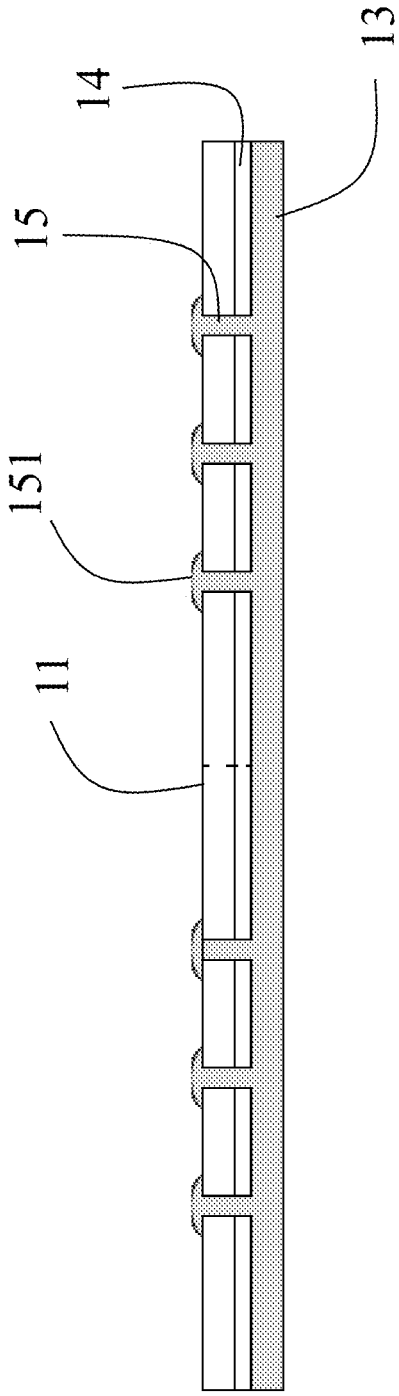


Fig.4A

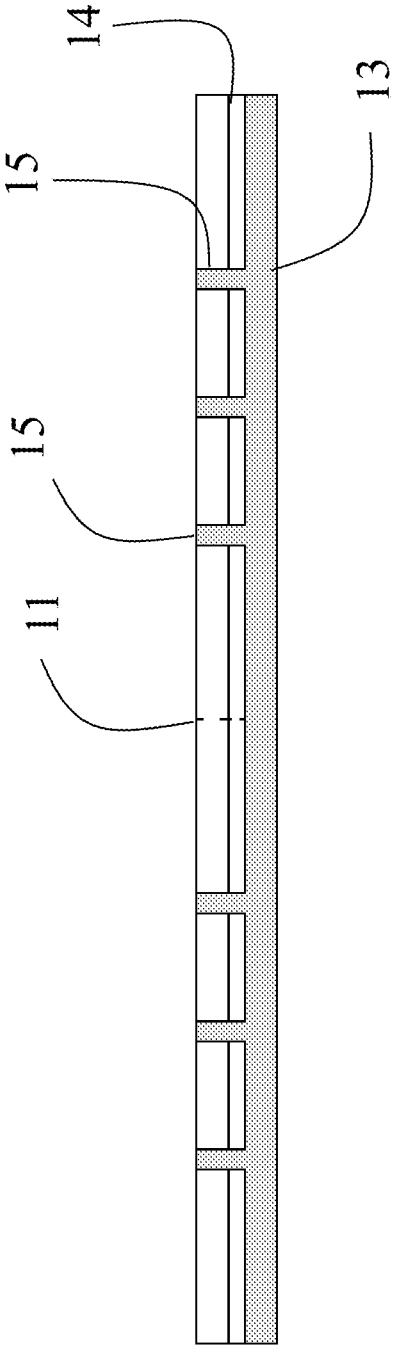


Fig.4B

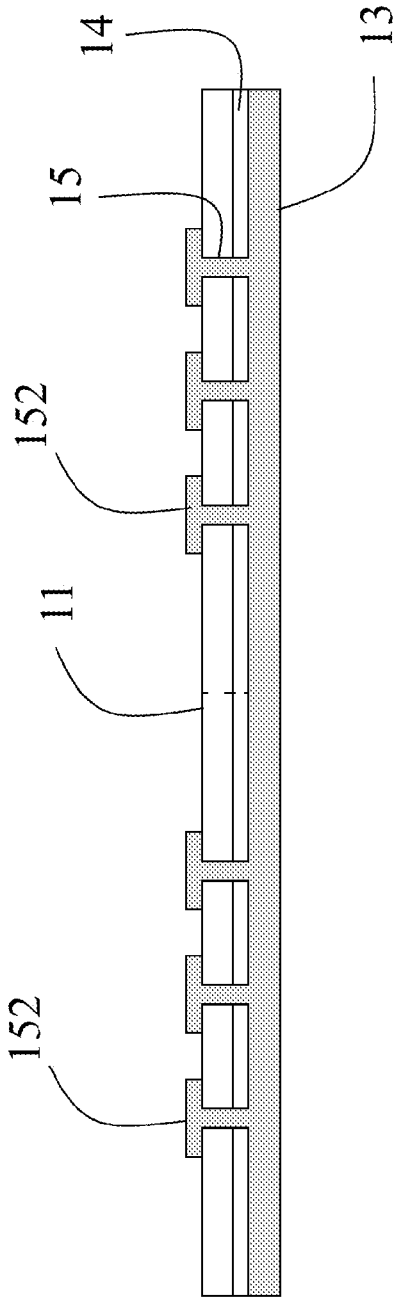


Fig.5A

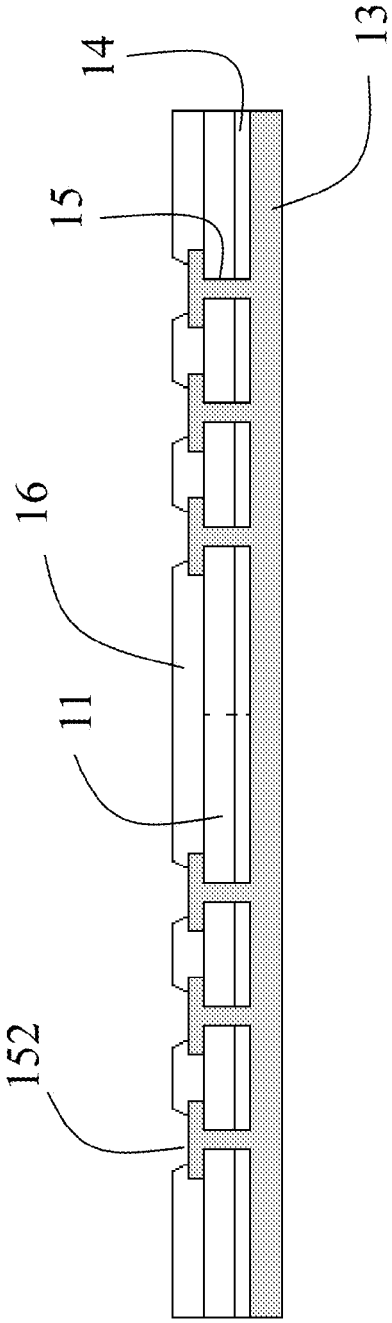


Fig.5B

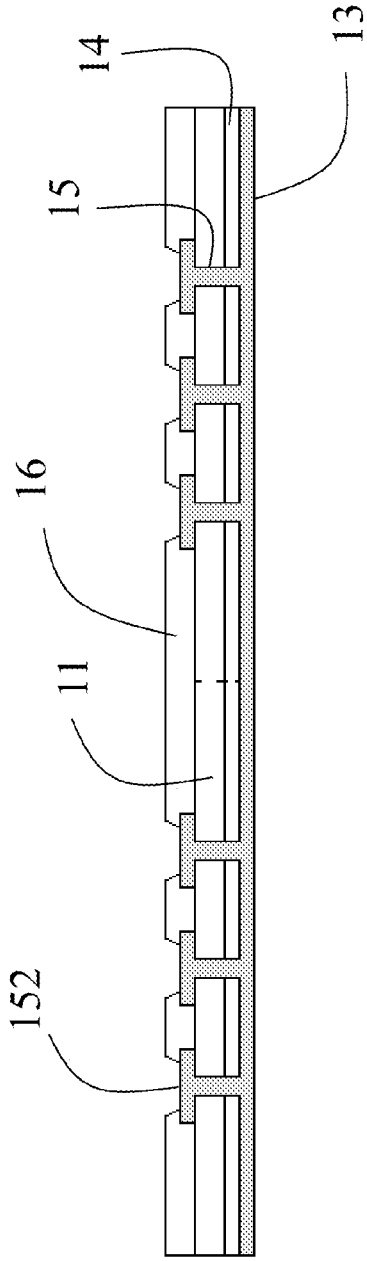


Fig.6A

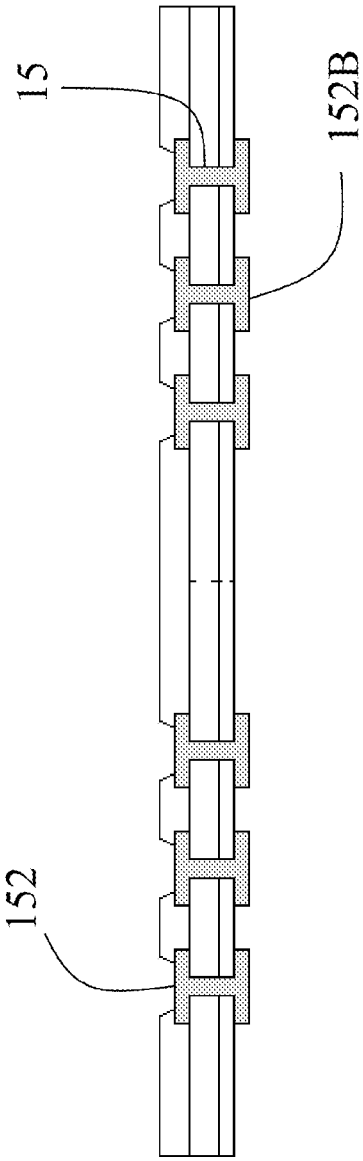


Fig.6B

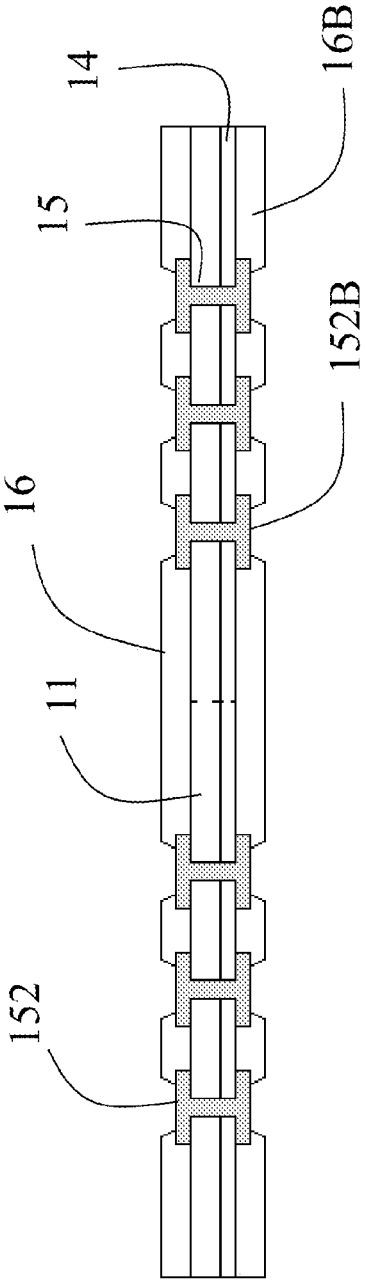


Fig.7A

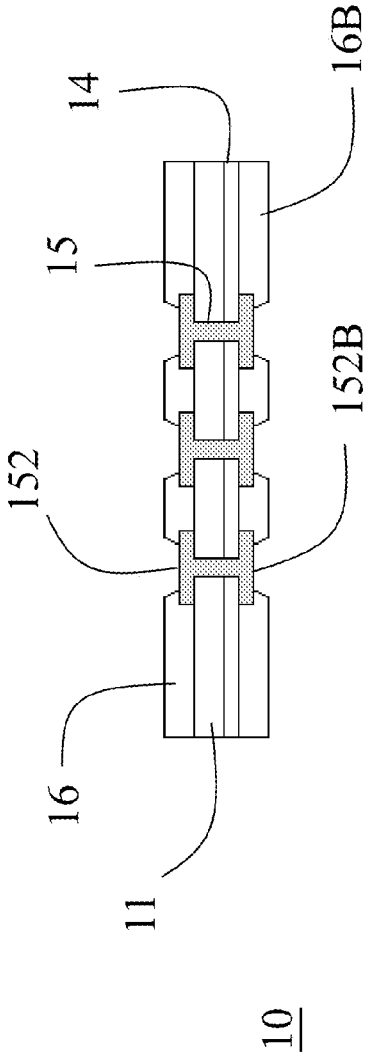
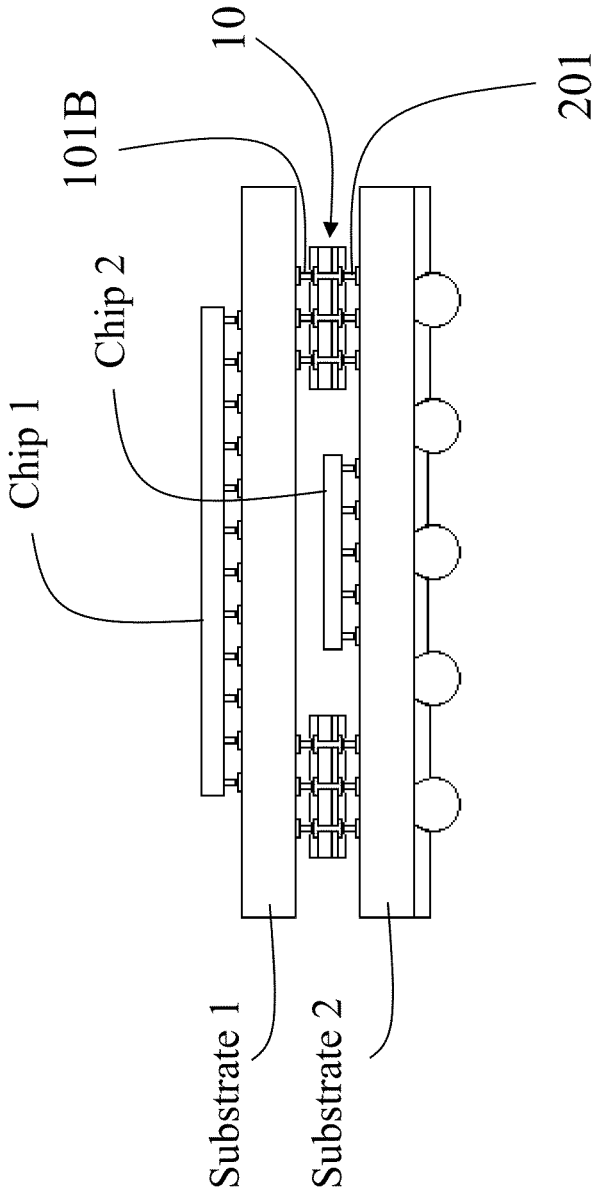


Fig.7B

Fig.8



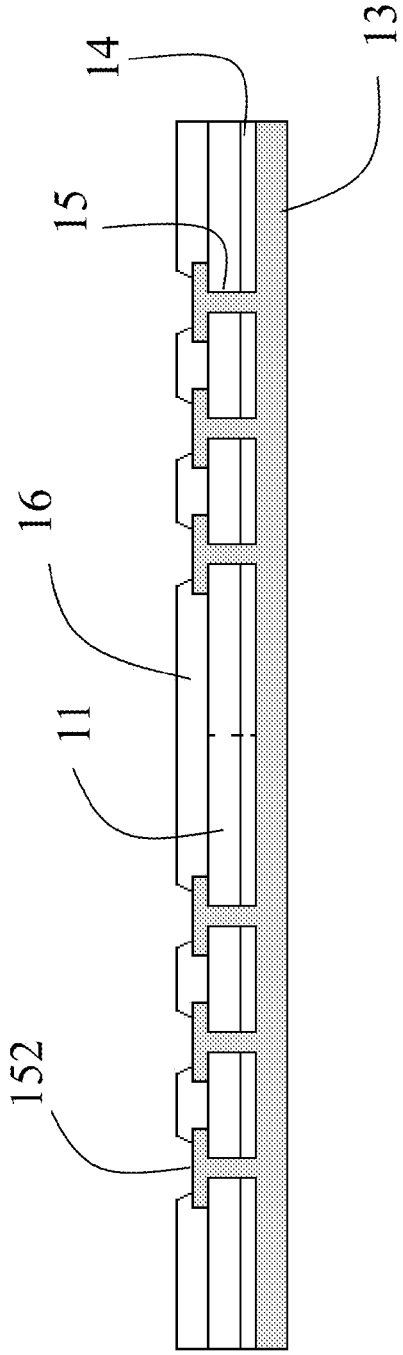


Fig.9A

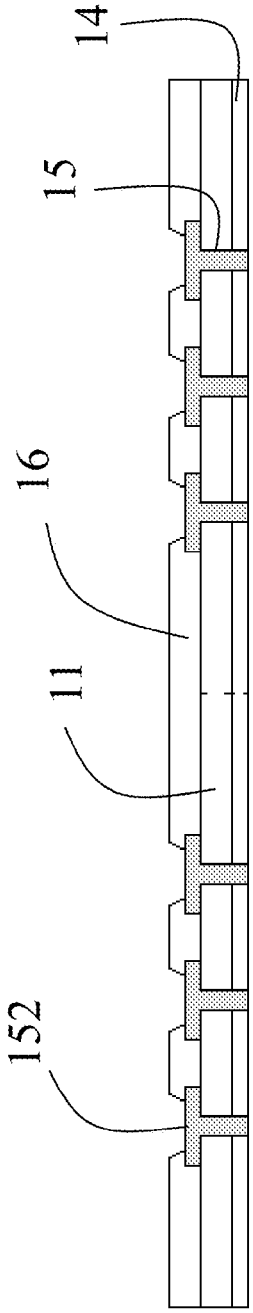


Fig.9B

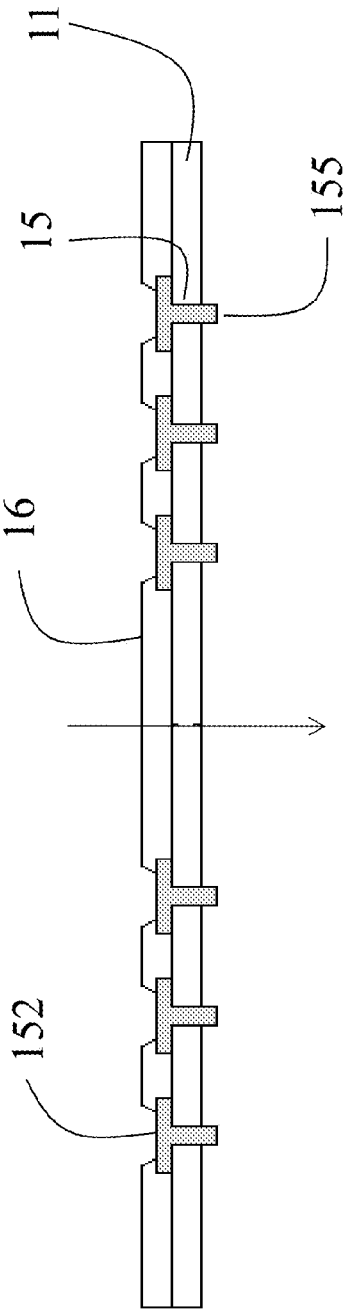


Fig.10A

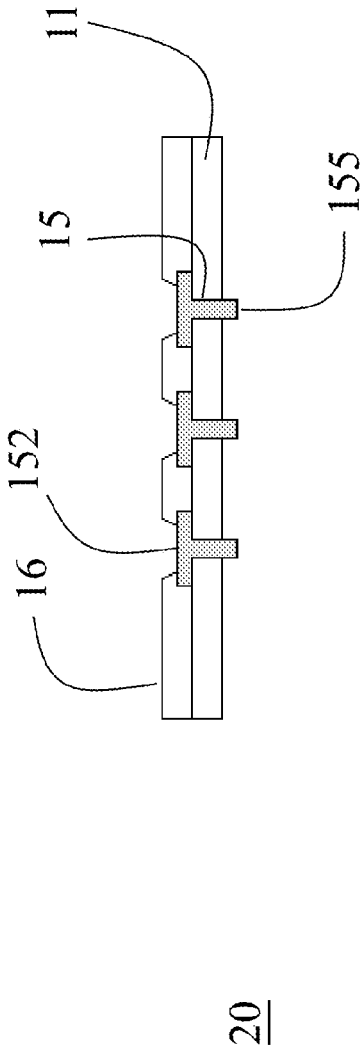
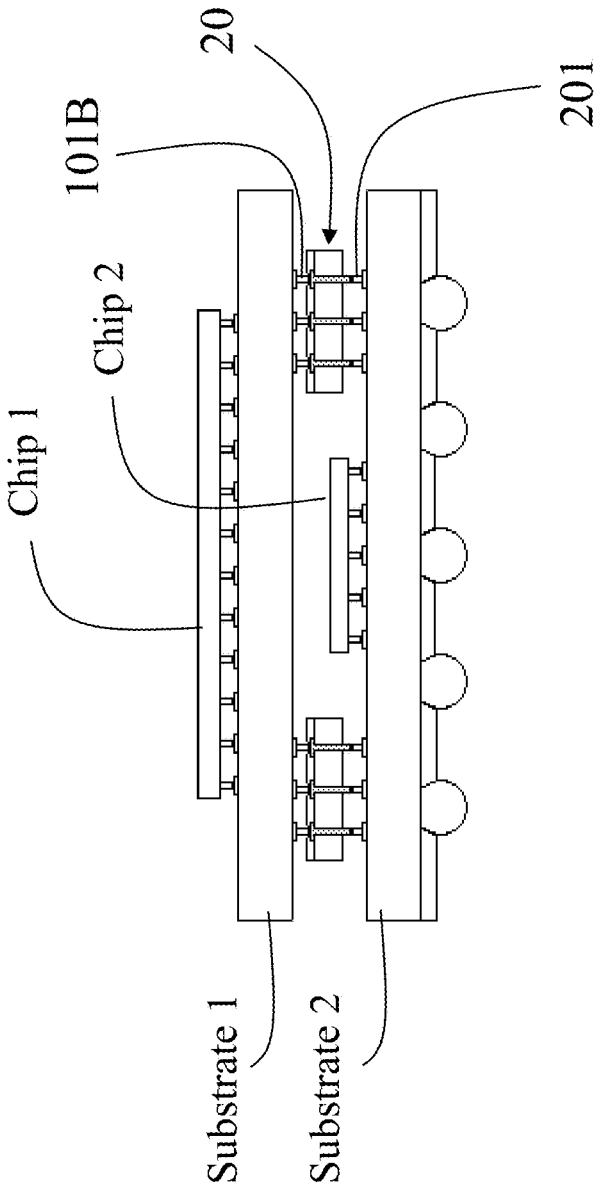


Fig.10B

Fig.11



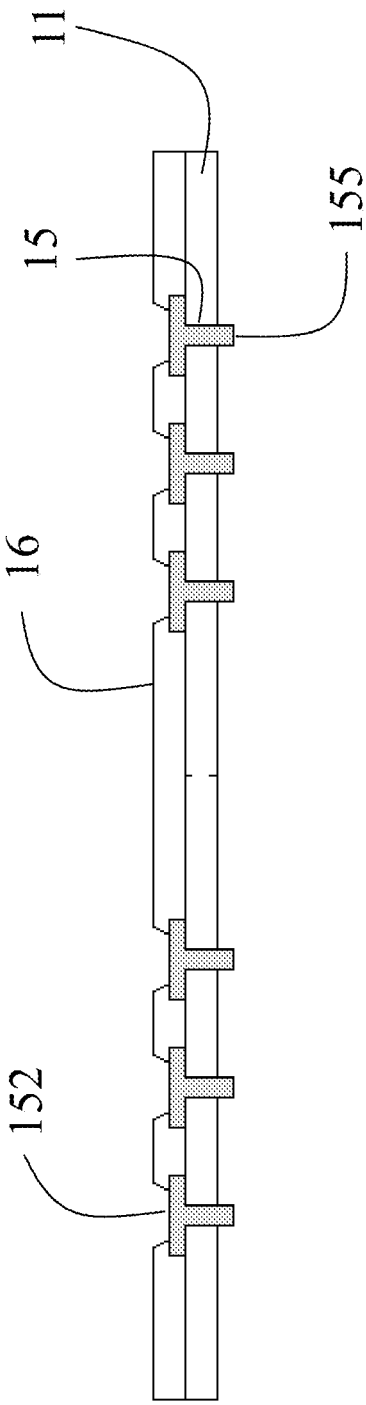


Fig.12A

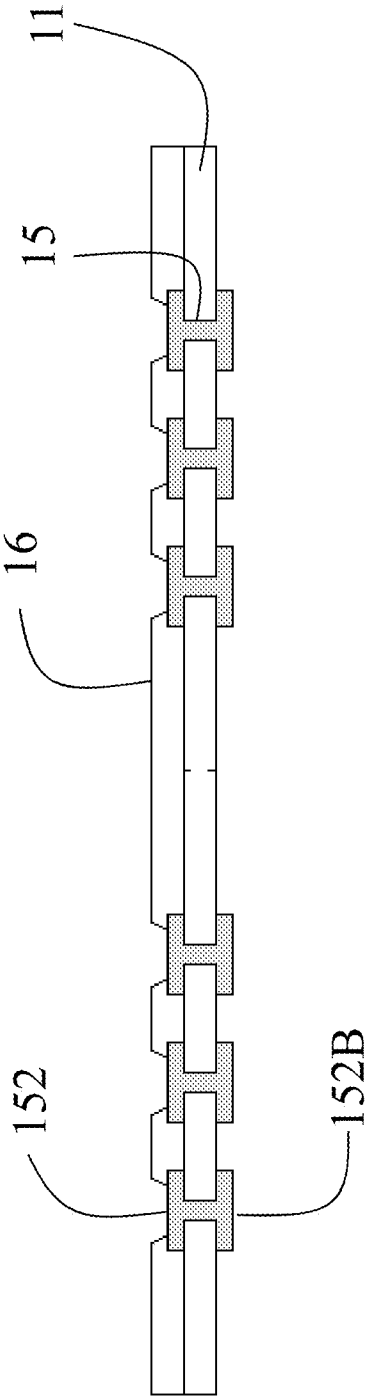


Fig.12B

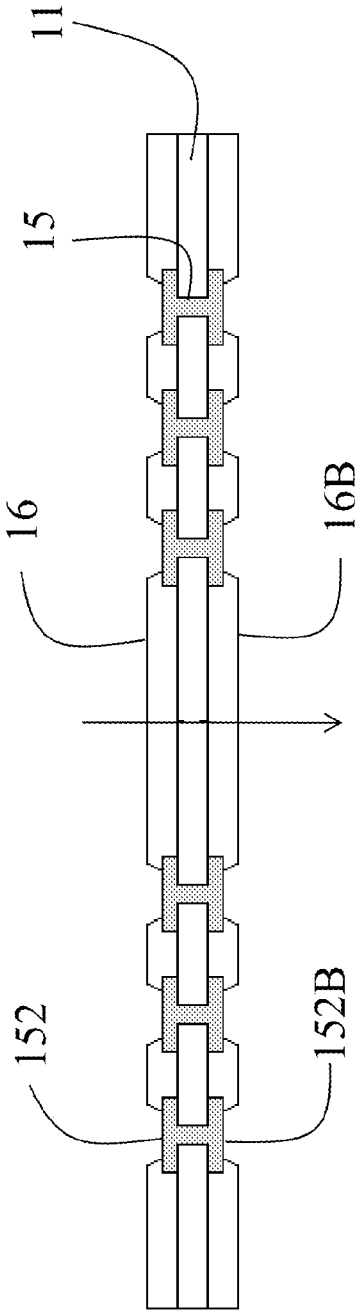


Fig.13A

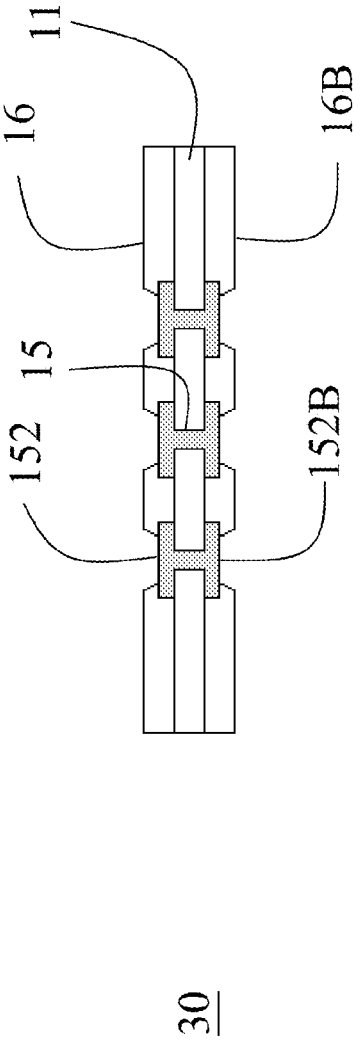
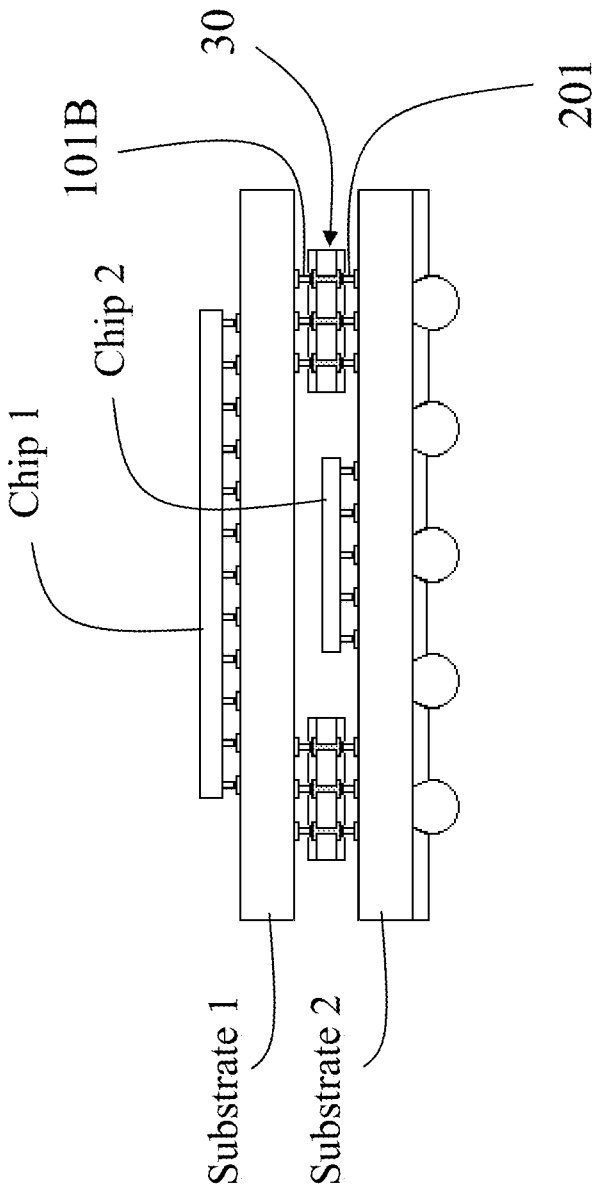


Fig.13B

Fig.14



SPACER CONNECTOR

RELATED APPLICATIONS

The present application claims the benefit of U.S. Provisional Application No. 62/184,034, filed Jun. 24, 2015, the disclosure of which is hereby incorporated by reference herein in its entirety.

BACKGROUND

Technical Field

The present invention relates to a fabricating process for making a spacer connector, especially using a conductive carrier in an initial step of the fabrication process.

Description of Related Art

One of the traditional processes for fabricating metal circuitry, a seed layer is often applied before electric plating. In a later process, the seed layer needs to be stripped. However, the stripping of the seed layer reduces the size of the circuits. Although such a circuit reduction is tiny, it is critical when it comes to nanotechnology. A fabricating process without reducing the dimension of a circuitry is one of the popular topics to study for a long time in the semiconductor industry.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A~**7**A show a fabricating process for a first embodiment according the present invention.

FIG. **7**B shows a first embodiment according to the present invention.

FIG. **8** shows an application for the first spacer connector according to the present invention.

FIGS. **9**A~**10**A show some steps in a fabricating process for a second embodiment according the present invention.

FIG. **10**B shows a second embodiment according to the present invention.

FIG. **11** shows an application for the second spacer connector according to the present invention.

FIGS. **12**A~**13**A show some steps in a fabricating process for a third embodiment according the present invention.

FIG. **13**B shows a third embodiment according to the present invention.

FIG. **14** shows an application for the third spacer connector according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A fabricating process for making a spacer connector without using seed layer is disclosed.

FIGS. **1**A~**7**A show a fabricating process for a first embodiment according the present invention.

FIG. **1**A shows that a core substrate **11** is prepared. The core substrate **11** is made of a material of glass or silicon.

FIG. **1**B shows a plurality of openings **12** is made through the core substrate **11**.

FIG. **2** shows a temporary conductive carrier **13** is prepared. A dielectric adhesive **14** is applied on a top surface of the conductive carrier **13**. The core substrate **11** with through holes **12** is pasted onto the dielectric adhesive **14**.

FIG. **3**A shows that the core substrate **11** is configured on a top surface of the dielectric adhesive **14**.

FIG. **3**B shows that the dielectric adhesive **14** on a bottom of each through holes **12** is etched, and a top surface of the conductive carrier **13** is exposed.

FIG. **4**A shows copper plating is performed using the conductive carrier **13** as one of the electrode. Copper pillar **15** is formed staring from the exposed conductive carrier in each through holes **12**. A metal head **151** is configured on a top of the copper pillar **15**.

FIG. **4**B shows the metal heads **151** are removed.

FIG. **5**A shows that top metal pad **152** is formed.

FIG. **5**B shows that a passivation **16** is formed on a top of the core substrate **11**. The passivation **16** also covers peripheral area of each top metal pad **152** and a central portion of the top metal pad **152** is exposed for electrical connection.

FIG. **6**A shows thinning process is performed from a bottom the temporary conductive carrier **13**.

FIG. **6**B show etching process is performed to the conductive carrier **13** to form a plurality of bottom metal pads **152**B. Each of the bottom metal pads **152**B is configured on a bottom of a corresponding metal pillar **15**.

FIG. **7**A shows a bottom passivation **16**B is formed on a bottom surface of the dielectric adhesive **14**. The bottom passivation **16**B also covers peripheral area of each bottom metal pad **152**B and a central portion of the bottom metal pad **152**B is exposed for electrical connection.

FIG. **7**B shows a first embodiment according to the present invention.

FIG. **7**B shows a first embodiment of the spacer connector **10** is produced after a singulation process performed on a product of FIG. **7**A.

FIG. **8** shows an application for the first spacer connector according to the present invention.

FIG. **8** shows two spacer connectors **10** are configured in between package substrate **1** and package substrate **2**. FIG. **8** shows chip **1** is configured on a top center of package substrate **1**. Chip **2** is configured on a top center of package substrate **2**. Package substrate **1** is stacked on a top of package substrate **2**.

The package substrate **1** has a plurality of bottom metal pillars **101**B, each metal pillar **101**B is electrically coupled to a corresponding top metal pad **152** of the spacer connector **10**. The package substrate **2** has a plurality of top metal pillars **201**, each metal pillar **201** is electrically coupled to a corresponding bottom metal pad **152**B of the spacer connector **10**.

FIGS. **1**A~**5**B, **9**A~**10**A show a fabricating process for a second embodiment according the present invention.

FIGS. **1**A~**5**B have been described in previous paragraphs and are omitted for simplification.

FIG. **9**A is the same of the product of FIG. **5**B which is a product prepared according to process FIGS. **1**A~**5**A.

FIG. **9**B shows the conductive carrier **13** is stripped. The dielectric adhesive **14** is revealed.

FIG. **10**A shows the dielectric adhesive **14** is stripped. A bottom end **155** of the copper pillar **15** protruded below a bottom surface of the core substrate **11**.

FIG. **10**B shows a second embodiment according to the present invention.

FIG. **10**B shows a second embodiment of the spacer connector **20** is produced after a singulation process is performed on the product of FIG. **10**A.

FIG. **11** shows an application for the second spacer connector according to the present invention.

FIG. **11** shows two spacer connectors **20** are configured in between substrate **1** and substrate **2**. FIG. **11** shows chip **1** is configured on a top center of substrate **1**. Chip **2** is configured on a top center of substrate **2**. Substrate **1** is stacked on a top of substrate **2**.

FIGS. **1**A~**5**B, **12**A~**13**A show a fabricating process for a third embodiment according the present invention.

FIGS. **1**A~**5**B have been described in previous paragraphs and are omitted for simplification.

FIG. **12**A is the same of the product of FIG. **10**A.

FIG. **12**B shows a plurality of bottom metal pads **152**B is formed. Each bottom metal pads **152**B is configured on a bottom of a corresponding copper pillar **15**.

FIG. **13**A shows a bottom passivation **16**B is formed on a bottom surface of the core substrate **11**. The bottom passivation **16**B also covers peripheral area of each bottom metal pad **152**B and a central portion of the bottom metal pad **152**B is exposed for electrical connection.

FIG. **13**B shows a third embodiment according to the present invention.

FIG. **13**B shows a second embodiment of the spacer connector **30** is produced after a singulation process is performed on the product of FIG. **13**A.

FIG. **14** shows an application for the third spacer connector according to the present invention.

FIG. **14** shows two spacer connectors **30** are configured in between substrate **1** and substrate **2**. FIG. **11** shows chip **1** is configured on a top center of substrate **1**. Chip **2** is configured on a top center of substrate **2**. Substrate **1** is stacked on a top of substrate **2**.

While several embodiments have been described by way of example, it will be apparent to those skilled in the art that various modifications may be configured without departs from the spirit of the present invention. Such modifications are all within the scope of the present invention, as defined by the appended claims.

What is claimed is:

1. A structure, comprising:

a bottom package substrate;

a top package substrate stacked on top of the bottom package substrate;

at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein

the spacer connector comprises

a core substrate;

a plurality of metal pillars, each passing through the core substrate; and

a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;

wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,

the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,

the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and

the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and

a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein

the bottom chip is mounted to the top surface of the bottom package substrate, and

the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

2. The structure of claim **1**, wherein

a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

3. The structure of claim **2**, further comprising:

a top chip mounted to the top surface of the top package substrate,

wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

4. The structure of claim **1**, wherein

each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

5. The structure of claim **4**, wherein

the spacer connector is free of metal pads on the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate, and

each metal pillar among the plurality of metal pillars and the corresponding top metal pad of the spacer connector form a T shape.

6. The structure of claim **4**, wherein

the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and

bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

7. The structure of claim **4**, wherein

the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate, and

the plurality of metal pillars pass through the core substrate and the dielectric layer.

8. The structure of claim **7**, wherein

the dielectric layer is a dielectric adhesive in which the core substrate is pasted.

9. The structure of claim **4**, wherein

the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars,

the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and

bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

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