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InfoTracks

Semitracks Monthly Newsletter

Copper Pillar Bumping Technology

By Christopher Henderson

This article provides an overview of copper pillar technology and discusses some of the challenges.

Copper pillar bumping has become more common in the past couple of years for several reasons. One financial reason is the increased cost of gold for wire bonding. However, that can be solved through standard copper wire bonding. A more important reason is that copper pillar technology promotes a fine pitch, flip chip process, which is vital for today and tomorrow's portable devices. Copper pillar bumping enables Thru Silicon Vias (TSVs), face-to-face bonding, and chip-on-chip bonding configurations that allow the manufacture of high-density electronic components.

Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.

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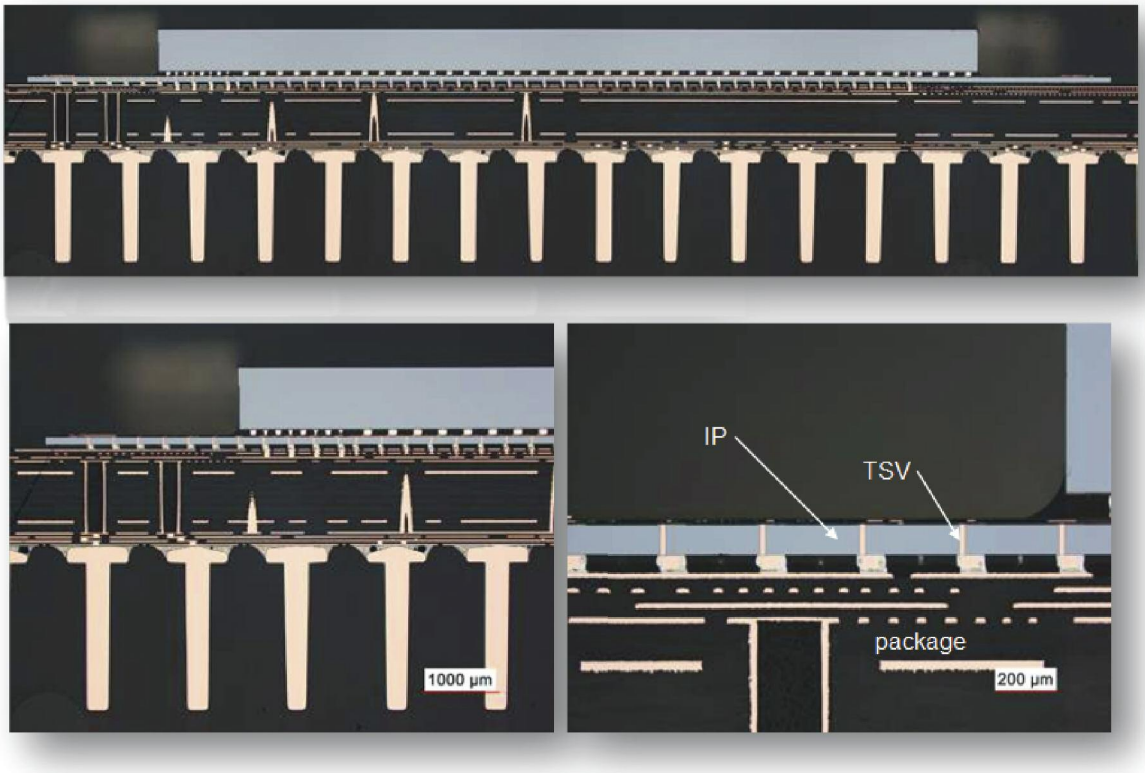

Figure 1. An example of a circuit that employs copper pillar bumping.

Copper pillar bumping is intended as a replacement to traditional solder bumping. While solder bumping is a lower cost process than copper pillar bumping, it doesn't allow for the density and current capacity afforded by copper pillar bumping. Because of their lower resistance, they don't heat as much as a solder bump, reducing electromigration issues. This permits higher densities; copper pillars can be utilized on pitches of less than 400 microns as well as in wafer level chip scale packages. Copper pillars also afford superior power management, both thermal and electrical. Lower resistances mean less heating in the pillars and less voltage drop within each pillar.

Copper pillars can be held to the substrate more securely through the use of an underfill. The underfill is applied as a non-conductive paste in the open areas between the pillars. The chip is then placed onto the substrate and the underfill is snap-cured. The coefficient of thermal expansion of the underfill pulls the chip to the substrate more than the copper pillar bumps, placing them in compression. Figure 2 shows the deformed tin-silver cap on the copper pillar that results from this process.

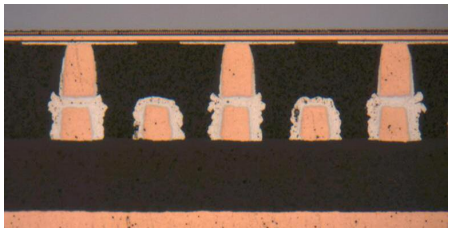

Figure 2. Copper pillar bumps with tin-silver cap. Image courtesy ChipWorks.

Copper pillar technology can be used on small dice in small packages like quad flat no-lead, or QFN, packages, on medium dice with the pillars providing connection to a laminate substrate, and on large dice

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mounted on fine-pitch laminate substrates.

For small dice, copper pillars can be used with no underfill in injection-molded components like QFN and Thin Small Outline Packages, or TSOPs. The connections can be made using solder materials with no-clean fluxes. For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate. The underfills can use capillary action and can be reworkable or non-reworkable.

Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflowable tin solder.

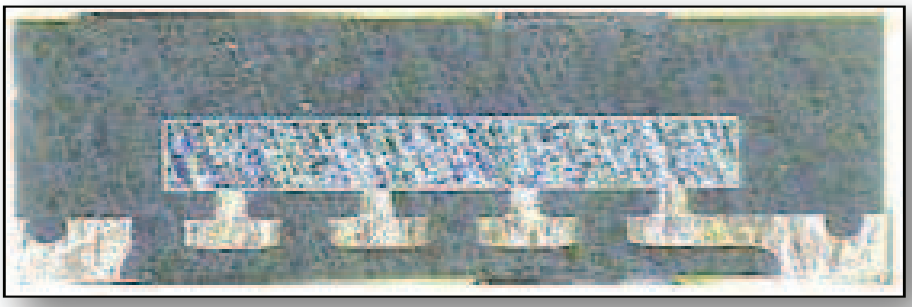

Figure 3. Optical image of a cross-section through an FCOL package with copper pillar bumps.

Copper pillar bumps are now commonly used on QFN packages. They provide benefits for high-speed circuits, including improved co-planarity and heat dissipation. QFN packages do not have gull wing leads that act as antennae, creating noise in high frequency applications. The electrical performance is also better than traditional leaded packages.

For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections. These manufacturers have primarily used no-clean fluxes.

Copper pillar bumping is now being used in microprocessor applications as well. The advantages are a similar to those of other components; one can achieve superior electrical performance, improved thermal management, and implement this with a lead-free solution.

Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow. The solder is consumed, as well as a portion of the copper pillars, forming an intermetallic compound that provides the mechanical and electrical connection.

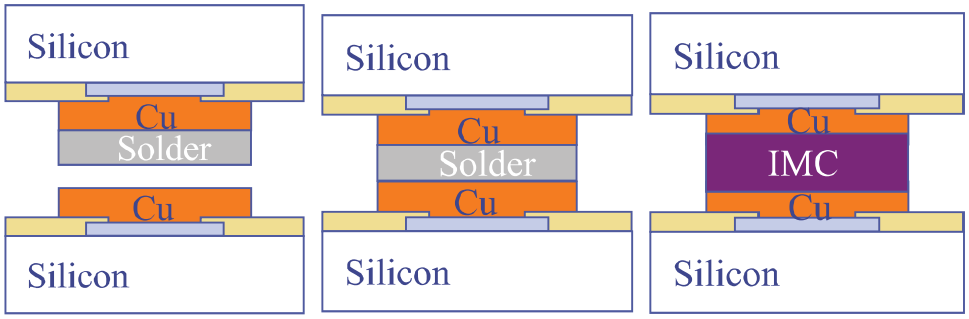

Figure 4. Die-to-die bonding using copper pillar bumps and tin solder.

The materials used for copper pillar bump assembly vary from company to company. Most manufacturers are experimenting with no-flow underfills, no-clean fluxes, and pre-plated leadframes (typically nickel-palladium-gold) to provide both manufacturability and reliability improvements.

Let's focus on the flux issue for a moment. Ultrasonic cleaning is a popular method for the cleaning of flux residue. In fact, ultrasonic frequencies around 40 kilohertz work great for cleaning flux residue from stencils and bare boards. However, applying the frequency for a longer time period, or using lower frequencies may cause damage to certain components when a board is populated. This has lead to the use of multisonic cleaning where a combination of frequencies is used to reduce damage. Therefore one must be careful of how frequencies are applied for cleaning. One phenomenon that occurs during ultrasonic cleaning is micro-bubble cavitation. However, decreased bump height and copper pillar heights cannot be cleaned as easily since the ultrasonic wavefronts cannot penetrate the smaller features. The smaller features are also more susceptible to damage, since lowering the energy reduces the cleaning capability. This involves tradeoffs in time, ultrasonic energies, and ultrasonic frequencies.

Scaling has introduced several problems with flip chip bump scaling. One issue is intermetallic compound formation. As the solder bumps scale down the intermetallic formation does not. This leads to situations where all that remains of the solder joint is the intermetallic compounds. Voiding can lead to weak mechanical and higher resistance pillars.

Another source of reliability problems with copper pillar bumping is with the thermomechanical stress inherent in the package. These forces introduce stress into the interconnect layers on the IC. Copper has a different coefficient of thermal expansion than the die, which leads to these stresses. Figure 6 shows how those stresses manifest themselves in the vicinity of the copper pillar. The red regions indicate high stress levels.

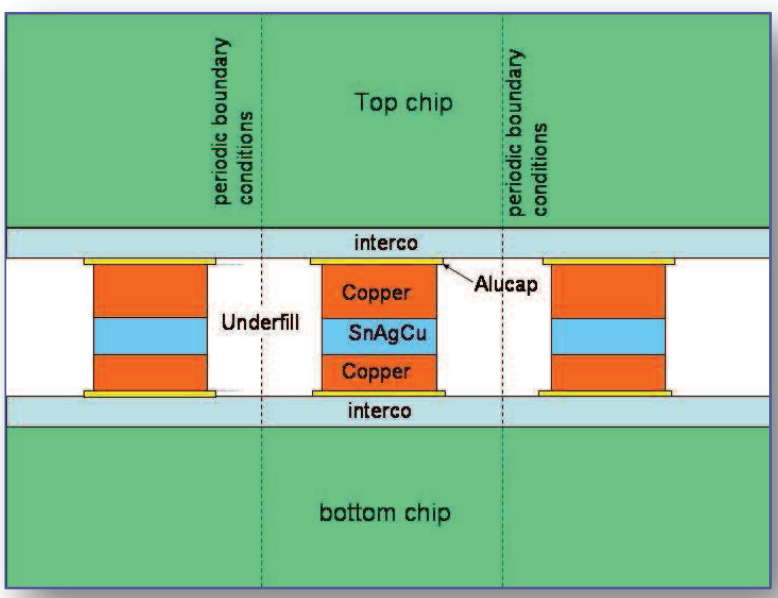

Figure 5. Simplified model for thermomechanical stresses in copper pillar bumps.

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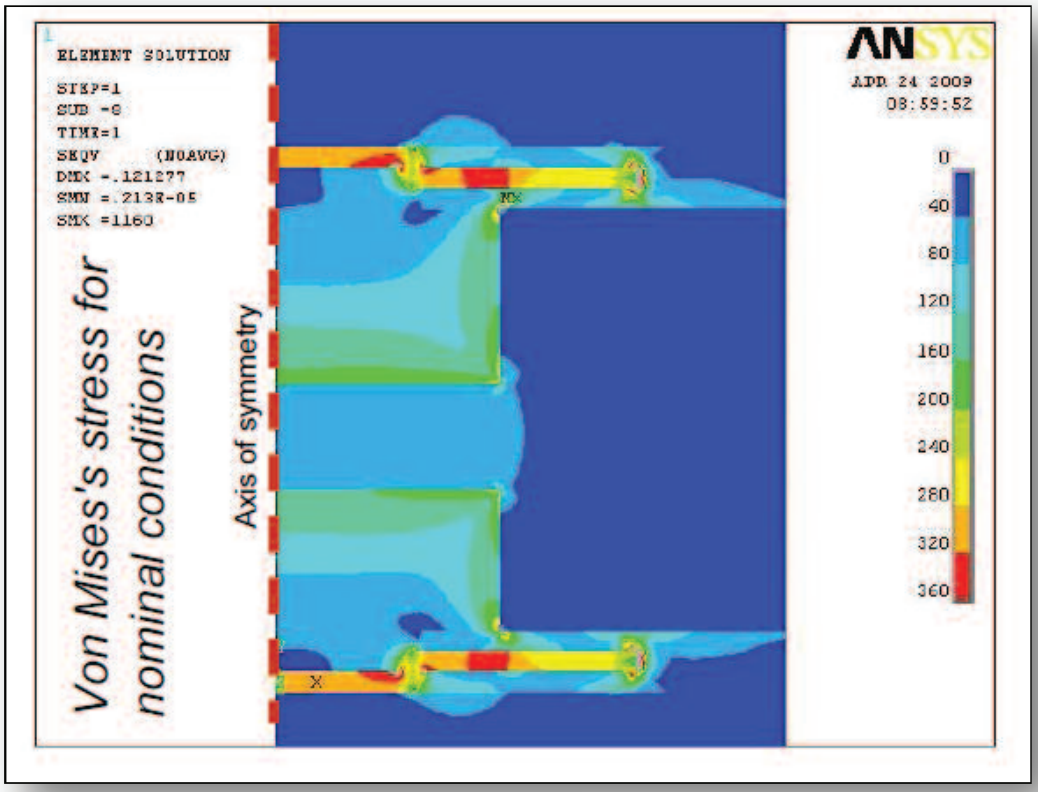

Figure 6. Simulation data showing high levels of stress in the interconnect layers just above and below the copper pillar bump.

In conclusion, copper pillar bumping is likely to increase in the future as a packaging technology. The superior resistance properties of copper allows for smaller bumping pitches, and improves electrical and thermal performance on these circuits. Although thermomechanical stresses are a concern, as well as the processing constraints that surround copper wires and pillars, the advantages outweigh the problems. Expect to see this technology more in the future.

Technical Tidbit

Muons and Single Event Upsets

Most people working in semiconductor reliability positions are aware that alpha particles and neutrons can lead to single event upsets. Alpha particles are generated by contaminants and radioactive materials in both plastic and ceramic packages, and solder bumps. They can also be generated by neutron collisions with silicon, and with boron-10 in borophosphosilicate glasses. Another particle that is less known for upsets is the muon (μ). Muons are subatomic particles that can be either positively or negatively charged (μ−, μ+). They have a mass of approximately 200 electrons, and a lifetime of approximately 2.2μsec. Low-energy muons with energies of 0.5 to 1.0 MeV can generate significant charge within an integrated circuit. Unlike neutrons that infrequently impact the nuclei of other atoms, muons generate charge carriers through the electromagnetic force. If the technology feature sizes allow for the collection of that charge, the integrated circuit can experience an upset. So even low muon fluxes can significantly add to the single event rate for sensitive devices. Figure 1 below shows simulated muon kinetic energy distributions, as seen on the front of the part, corresponding to experimental momenta including upstream energy losses and straggling on the bottom part of the figure. Experimental error counts for 65 nm, 45 nm, and 40 nm SRAMs versus estimated muon kinetic energy at 1.0 V bias on the top part of the figure. The dashed horizontal line represents an approximate muon-induced SEU cross-section for reference.

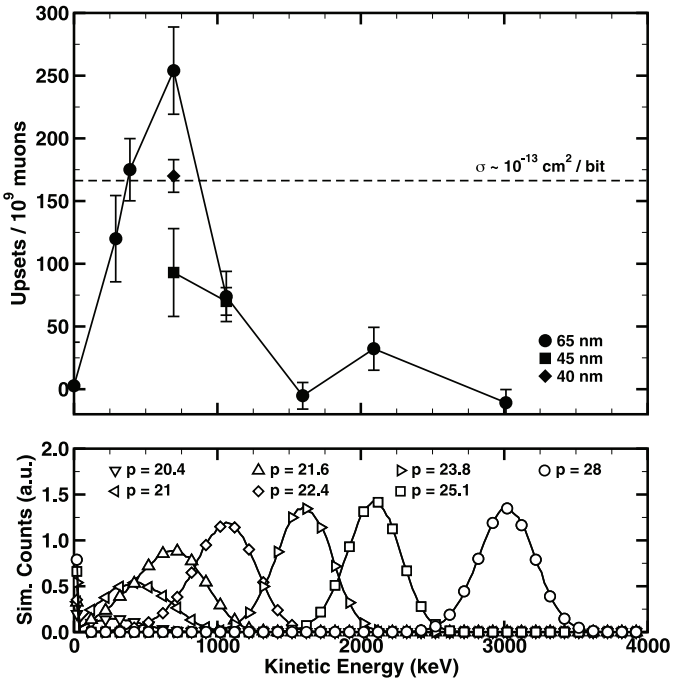

Figure 1. (Top) experimental error counts in three IC technologies, and (bottom) simulated muon kinetic energy distributions. Sierawski et al., IRPS, pp. 247-252, 2011.

This problem is likely to increase in the future as we scale to smaller devices since the charge volumes decrease. Many researchers believe muons will become a more significant contribution to single event upsets at the 32nm node and below.

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Ask the Experts

Q: Can etching of the polyimide layer to form windows for the bond pads on a circuit subsequently create poor contact for bond wires?

A: Yes, this has been observed in the past. The etch residues and hydrolysis products affect the surface of the bond pad, degrading its adhesive properties. An early paper that discussed this problem is C.G. Shirley and M.S. DeGuzman, "Moisture-Induced Gold Ball Bond Degradation of Polyimide-Passivated Devices in Plastic Packages," Proc. IRPS, pp. 217 – 226, 1993.

Spotlight on our Courses: Package Reliability & Device Qualification

We will begin offering a new course on Package Reliability and Device Qualification later this year. Here is more information about the course. If you are interested in attending this course, or if you're interested in having this course as an in-house course for your staff, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. In particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. Semiconductor Reliability and Qualification is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.

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3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.

Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is application. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

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COURSE OUTLINE

Day One (Lecture Time 8 Hours)

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information
2. Statistics and Distributions
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Which Distribution Should I Use?
   d. Acceleration
   e. Number of Failures

Day Two (Lecture Time 8 Hours)

3. Overview of Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Negative Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding
4. Package Level Mechanisms
   a. Ionic Contamination
   b. Moisture/Corrosion
      i. Failure Mechanisms
      ii. Models for Humidity
      iii. T_{ja} Considerations
      iv. Static and Periodic stresses
      v. Exercises
   c. Thermo-Mechanical Stress
      i. Models
      ii. Failure Mechanisms
   d. Interfacial Fatigue
      i. Low-K fracture
   e. Thermal Degradation/Oxidation

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Day Three (Lecture Time 8 Hours)

5. Package Attach (Solder) Reliability
    a. Creep/Sheer/Strain
    b. Lead-Free Issues
    c. Electromigration/Thermomigration
    d. MSL Testing
    e. Exercises
6. TSV Reliability Overview
7. Board Level Reliability Mechanisms
    a. Interposer
    b. Substrate
8. Electrical Overstress/ESD
9. Test Structures and Test Equipment
10. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
    d. JEDEC-based Tests
    e. Exercises

Day Four (Lecture Time 8 Hours)

11. Calculating Chip and System Level Reliability
12. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. JEDEC Documents (JESD47H, JESD94, JEP148)
    e. Exercises

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Semitracks will be offering two courses this year in conjunction with Semicon West: Copper Wire Bonding and Challenges, and Advanced Semiconductor Reliability and Characterization Challenges.
Click here for more information on the Copper Wire Bonding Course, and here for the Reliability Challenges Course.

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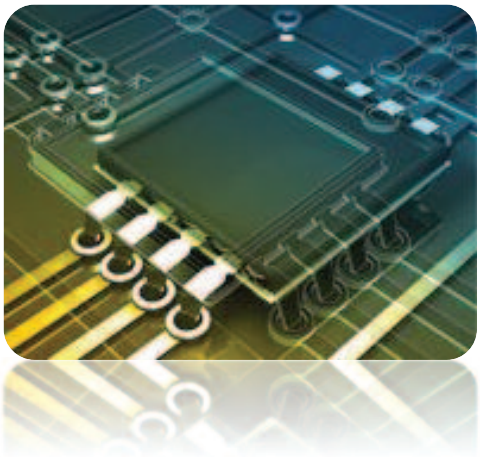

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!
http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

MEMS Technology
June 12 – 13, 2012 (Tues – Wed)
Enschede, Netherlands

Reliability Challenges
July 11, 2012 (Wed)
San Francisco, CA, USA

Copper Wire Bonding
July 11 – 12, 2012 (Wed – Thur)
San Francisco, CA USA

ESD Design and Technology
July 15 – 17, 2012 (Sun – Tues)
Tel Aviv, Israel

Failure and Yield Analysis
July 15 – 18, 2012 (Sun – Wed)
Tel Aviv, Israel

Copper Pillar Technology and Challenges
July 18 – 19, 2012 (Wed – Thur)
Penang, Malaysia

Semiconductor Reliability
July 31 – August 3, 2012 (Tues – Fri)
Singapore

Polymers and FTIR
August 16 – 17, 2012 (Thur – Fri)
San Jose, California

Failure and Yield Analysis
August 27 – 30, 2012 (Mon – Thur)
San Jose, California

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