# ELECTRONIC PACKAGING AND INTERCONNECTION HANDBOOK

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# CHAPTER 7

# PACKAGING AND INTERCONNECTION OF INTEGRATED CIRCUITS

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## 7.1 INTRODUCTION

One of the most critical levels of electronic packaging is that of packaging and interconnecting integrated circuits (ICs). The ICs are at the heart of electronic system controls, and since they are typically sensitive to electrical, mechanical, physical, and chemical influences, they require special considerations by the packaging engineer. IC packaging is the middle link of the process that produces these systems. Hence, it must respond to demands from both ends, that is, wafer fabrication and device trends upstream (circuit level) and circuit board assembly and system performance trends downstream (system level). This is particularly true in the design, piece part fabrication, and assembly aspects of IC packaging. Today's circuit and system level requirements of high performance, high reliability, and low cost have placed greater demands on the packaging engineer to have a better understanding of the existing and emerging packaging technologies. Many electronic system performance problems result from a lack of knowledge and understanding of the interaction of the many materials and processes that are a part of this first level of packaging. Packaging engineers must be aware of the latest industry demands and be able to trade off among the various packaging technologies on what works and what is economically feasible to satisfy these demands. This chapter addresses the current state of IC packaging technologies and provides an insight into new IC packaging concepts.

### 7.1.1 Terms and Definitions

The semiconductor industry has undergone many changes over the past two decades, among them the terminology used in the packaging of ICs. Acronyms have found wide


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acceptance and usage in the semiconductor industry; many are used in this chapter or will be found in the papers and books referenced. Some of the acronyms that are encountered by the packaging engineer in daily activities in the office, the laboratory, and on the manufacturing floor are listed in Appendix A.

An IC package is the housing, which assures environmental protection to the IC chip and provides for complete testing and high-yield assembly to the next level of interconnection. Levels of electronic packaging are defined in Fig. 7.1. This chapter deals with the first level of packaging, where the IC is assembled into a package such as a quad flatpack (QFP), pin grid array (PGA), or ball grid array (BGA) using wire-bonding (WB), tape automated bonding (TAB), or flip chip (FC) bumping assembly techniques. The packaged device, as defined, is then attached either directly to a printed wiring board (PWB) or to another type of substrate, which is defined as the second level of packaging. An alternative would be to assemble the packaged device to an intermediate vehicle, such as a hybrid circuit or a multichip module (MCM), which are described in Chap. 9. Hybrid circuits contain substrates that are typically ceramic with thick or thin film metallization, while MCMs utilize substrates made of either multilayer PWBs, multilayer ceramic, or silicon substrates with built-up multilayer dielectric insulators and metal conductors to achieve the required system performance. In the MCM option, chips are placed on the substrate bare (without package) and, after interconnection and test, the assembly is sealed to provide environmental protection to the MCM.

The specific function of the IC package is to protect the chip from mechanical stress, environmental stress (such as humidity and pollution), and electrostatic discharge during handling. In addition, the package provides mechanical interfacing for testing, burn-in,

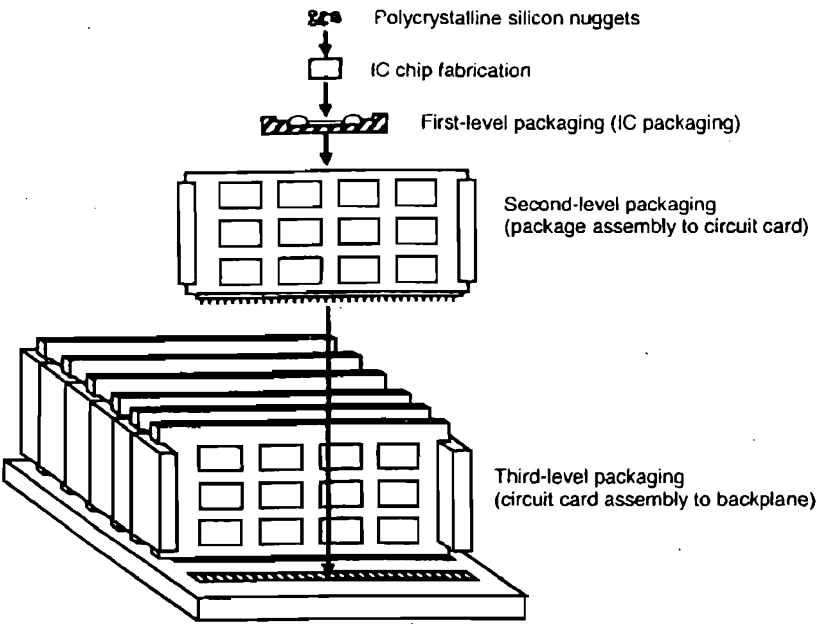


**FIGURE 7.1** Electronic packaging hierarchy.

and electrical interconnection to the next level of packaging. The package must meet all device performance requirements such as electrical (inductance, capacitance, crosstalk), thermal (power dissipation, junction temperature), quality, reliability, and cost objectives. Until recently, the packaging and interconnecting technologies have not been the limiting factors in the performance of most silicon devices in high-volume production. But, as circuit and system demands are increasing, more attention is needed in selecting package technologies, materials, and designs that will meet these challenges. Some package designs may need to provide special design enhancements to accommodate such demands as higher power dissipation, signal terminations, power and ground distribution, and matched impedance terminations.

IC packages come in a variety of lead arrangements and mounting types that are grouped into families defined by the method of mounting to level 2 [through-hole (TH) or surface-mount (SM)] and by the physical arrangement of the leads on the package (in-line, perimeter, or array). Figures 7.2 and 7.3 illustrate some of the more popular package types used today in the TH and SM families. Section 7.5 describes these and other emerging types in more detail.

### 7.1.2 Circuit and System Driving Forces

Over the last four decades, the electronics industry has grown very rapidly, with increases of over an order of magnitude in sales of ICs. In the 1960s, the IC market was dominated by bipolar transistors but, by 1975, digital metal-oxide semiconductors (MOS) emerged as

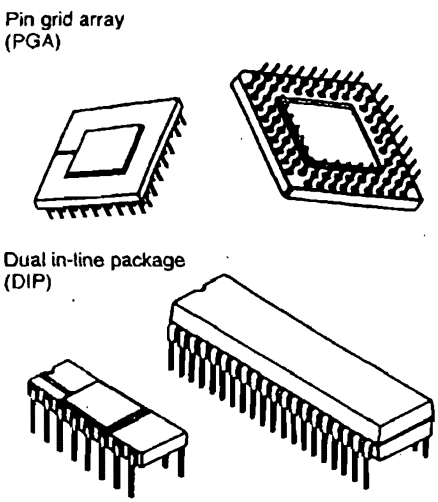


**FIGURE 7.2** IC packaging families, TH (through hole) type. Design variations exist within families, such as the way leads are attached to or exit the body, as illustrated in the DIP family, and in the direction the cavity faces with respect to the PWB (up or down), as shown in the PGA family.

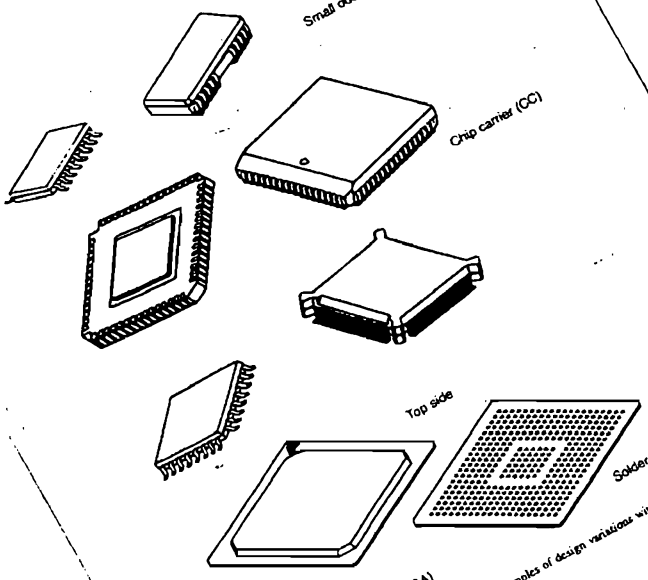


**FIGURE 7.3** IC package families. SM type. Examples of design variations within families are lead geometry (gull wing, J, leadless, or solder balls).

the predominant IC group. Because of MOS's advantage in device miniaturization, low power dissipation, and high yields, its dominance has continued to this day, having captured a major market share of IC sales.

*7.1.2.1 Circuit-Level Demands.* IC complexity over the last four decades has advanced from small-scale integration (SSI) in the 1960s to medium-scale integration (MSI), to large-scale integration (LSI), and finally to very-large-scale integration (VLSI), which characterizes devices containing $10^5$ or more components per chip. This rate of growth[3] is

exponential in nature (Fig. 7.4) and, at the current rate of growth, the complexity is expected to reach about $5 \times 10^9$ devices per chip by the year 2005.

Continued reduction of the minimum IC feature dimensions[3] (Fig. 7.5) is a major factor in achieving the complexity levels mentioned. The feature size has recently been shrinking at an approximate annual rate of 11 percent, thus reaching an expected minimum feature size of $10^2$ nm (0.10 μm) by the year 2006. For many years, the packaging and PWB interconnection technologies have not enjoyed an equal rate of advancement over the same period, as the ICs did. In recent years, the board area necessary to interconnect the chip to the PWB has been significantly reduced by the introduction of ball grid array (BGA) packages with solder balls on a pitch as small as 0.020 in (0.5 mm). In addition, the use of bare chips (no package), with wire bonds, TAB or flip-chip (FC) bonding, and chip-scale packaging have further reduced the interconnection area to where it now approaches IC dimensions.

The rapid increase in the number of components per chip and the performance requirements of these devices create major challenges for packaging designers. Memory devices have been the driving force in the advancement of leading-edge wafer fabrication technology. However, they do not challenge packaging to the same extent as logic chips, which dissipate more power and require more inputs and outputs (I/Os). Although memory chip complexity and chip size have increased significantly over the last four design generations, and this trend will continue in the future[3] (Fig. 7.6), the challenge to packaging in terms of I/O increased at a slower rate due to multiplexing techniques on the chip. In contrast, the number of I/O terminals required for logic (such as ASIC) and microprocessor devices continues to increase proportionally to the number of gates on the chip. Figures 7.7*a* and *b* show the extreme demands placed on packaging by logic and microprocessor devices as compared with memories (Fig. 7.7*c*), where the I/O count has remained essentially constant for $2.7 \times 10^8$ to $2.8 \times 10^{11}$ bit dynamic random-access memories (DRAMs).

Rent's rule is an empirical expression defined as

$$\text{Number of I/Os} = \alpha(\textit{gate count})^{\beta}$$

where α and β are constants determined by device design. Rent's rule is used to estimate the number of package I/Os that will be needed as a function of the number of gates in the device design. The examples shown in Figs. 7.7*a, b,* and *c* use these constants and give a good fit to logic (gate-array), microprocessor, and memory devices.

Device miniaturization has further improved the circuit-level performance, one example being the reduction of power consumption at the per-gate level. Figure 7.8 illustrates the exponentially decreasing trend and the power per gate for five major IC application groups: automotive, high-performance, cost-performance, hand-held, and memory. Figure 7.8 illustrates the exponentially decreasing trend in the power per gate for all groups. Figure 7.9, on the other hand, shows that the power dissipation per chip actually increased over the same period of time for the high-performance and cost-performance groups, whereas for the automotive, hand-held, and memory groups, the power dissipation remained relatively constant. This is explained by the fact that, while the power per gate scales linearly with feature size, the power dissipation per chip is largely influenced by the inverse square of the feature-size, as shown below:

$$\text{Power dissipation per chip, } P = f(\textit{Freq}, C, V^2, \textit{gate count})$$

where $\textit{Freq}$ = clock frequency
$C$ = capacitance
$V$ = voltage
$\textit{gate count}$ = chip area/(feature size)$^2$

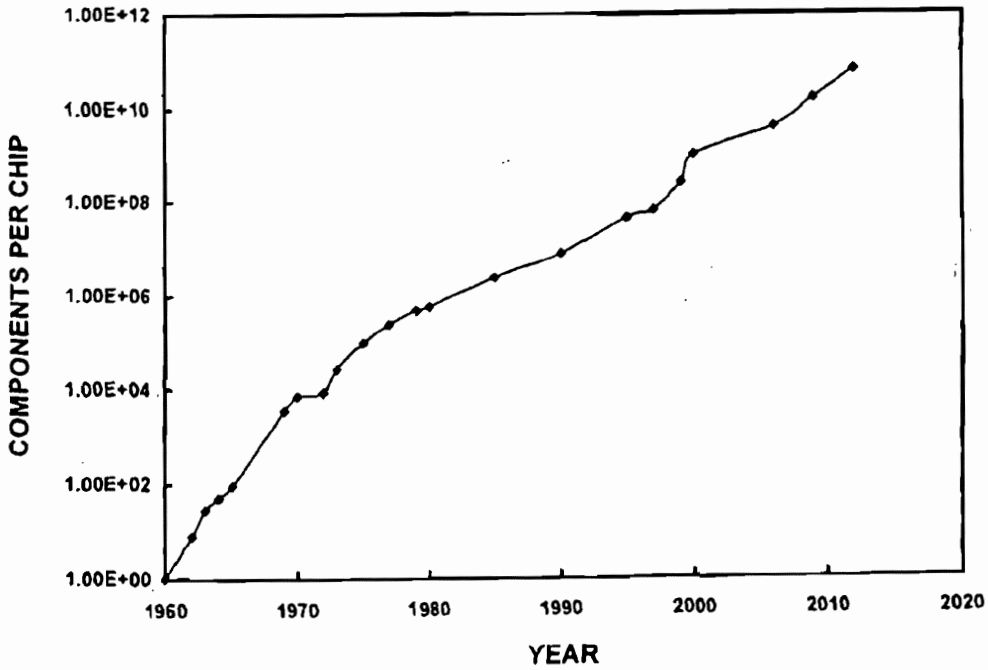


FIGURE 7.4 Exponential growth of the number of components per IC chip for MOS memory. *(After SIA[3])*

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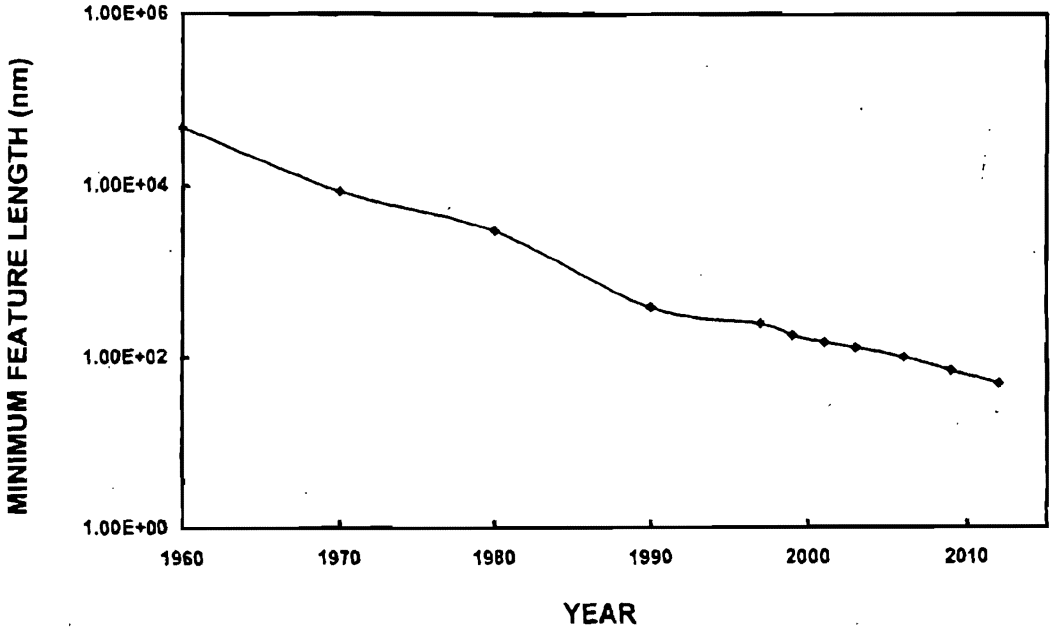


**FIGURE 7.5** Exponential decrease of minimum device dimensions. *(After SIA[3])*

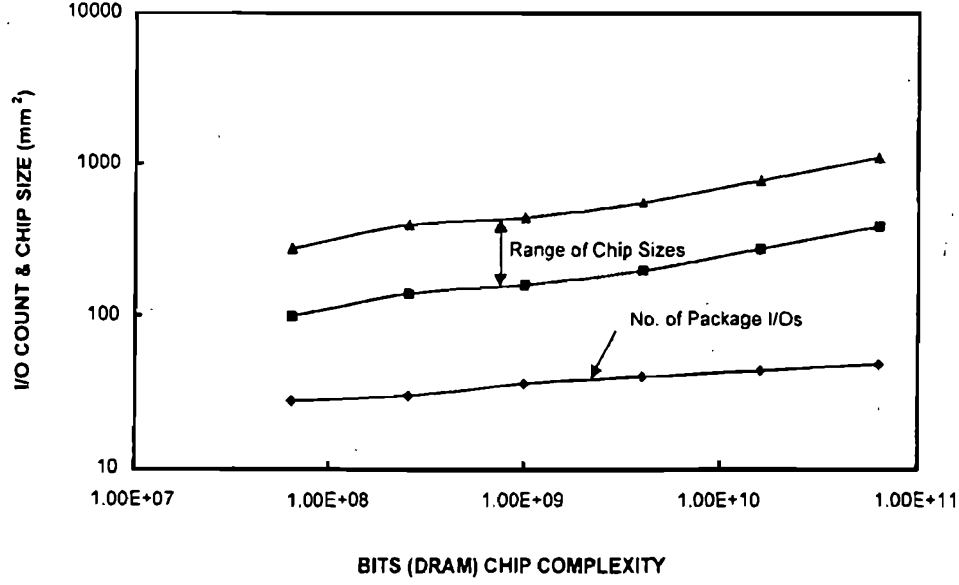


**FIGURE 7.6** Continuous growth in DRAM complexity and size place little demand on package size and number of I/Os. *(After SIA[3])*

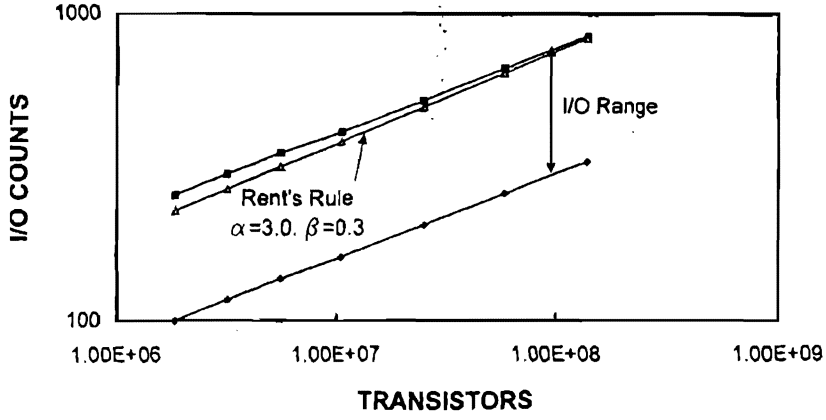


**FIGURE 7.7a** Comparison of I/O requirements for logic devices as a function of circuit complexity. *(After SIA[3])*



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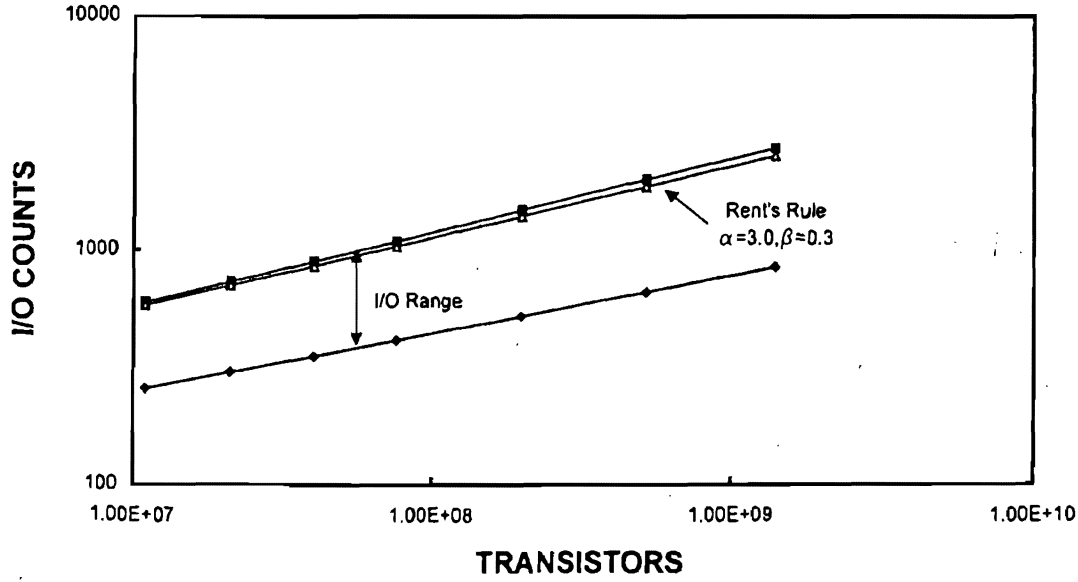


**FIGURE 7.7b** Comparison of I/O requirements for microprocessor as a function of circuit complexity. *(After SIA[3])*

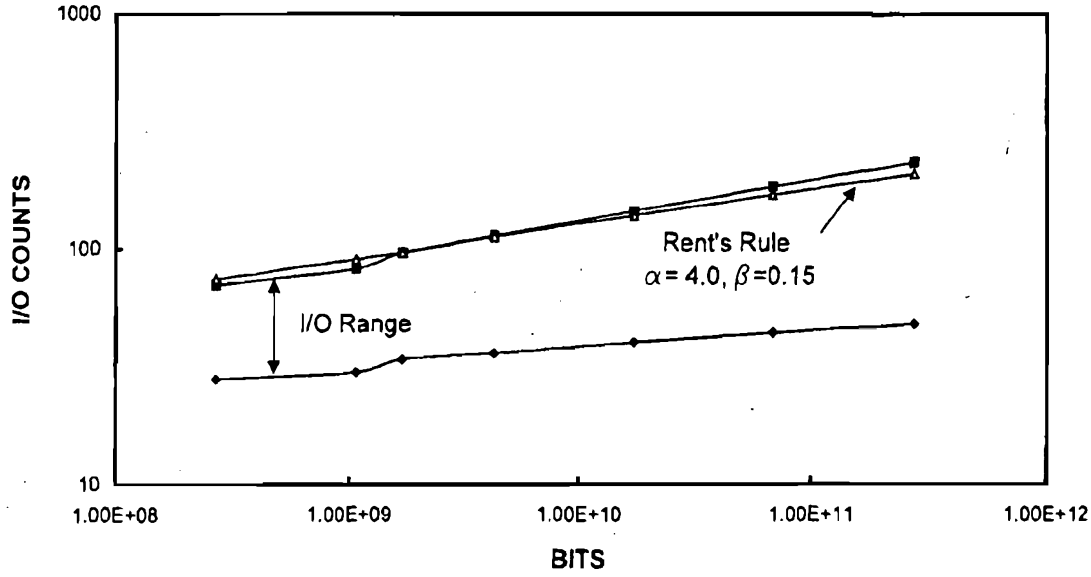


**FIGURE 7.7c** Comparison of I/O requirements for a memory device (DRAM) as a function of circuit complexity. *(After SIA[3])*

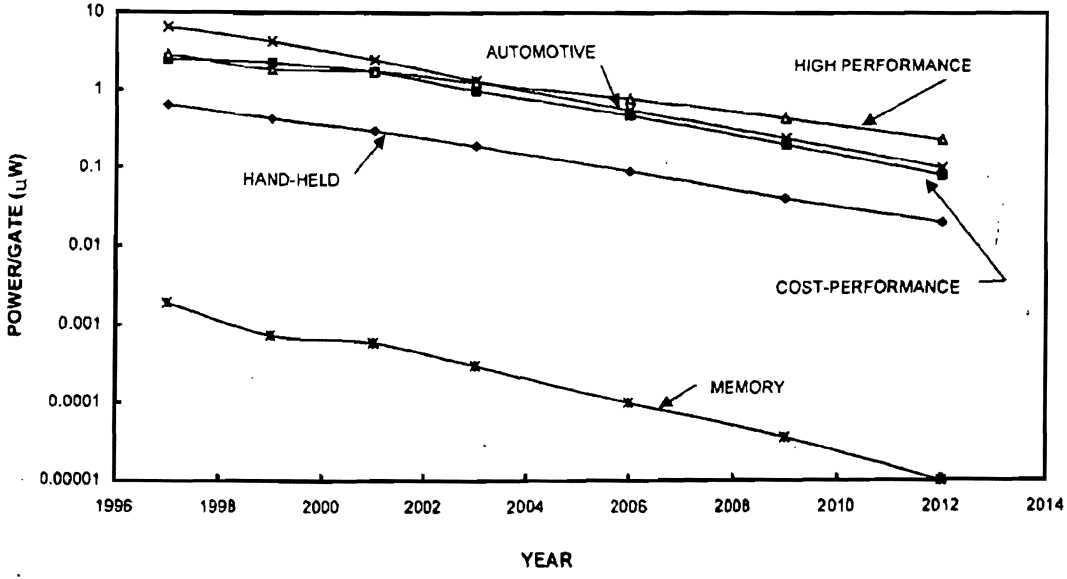


**FIGURE 7.8** Trends in circuit power dissipation per gate. *(After SIA[3])*

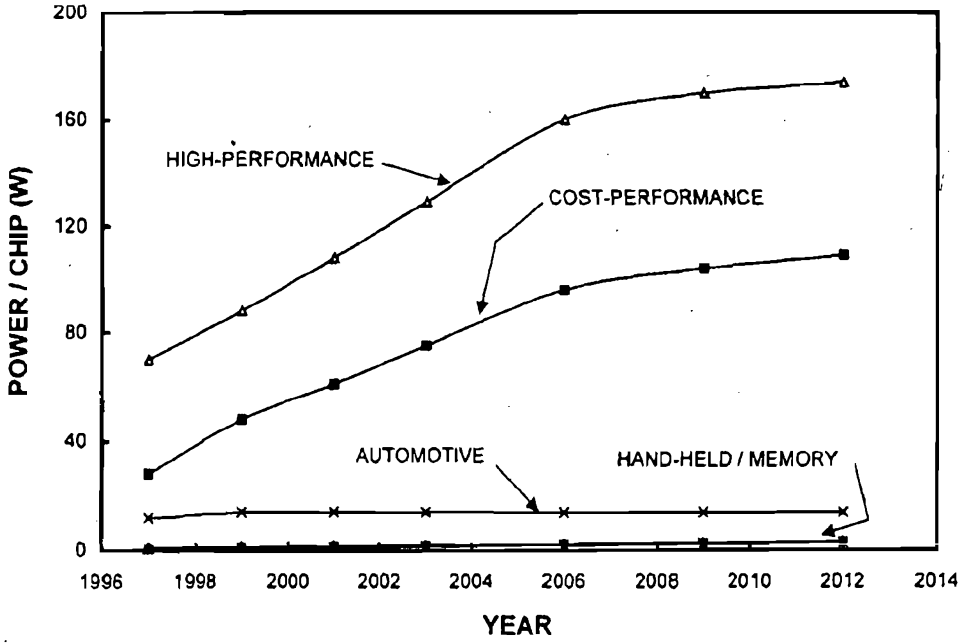


**FIGURE 7.9** Trends in circuit power dissipation per chip. *(After SIA[3])*

While the clock frequency and gate count have been increasing exponentially over the years (Figs. 7.4 and 7.10), the capacitance and voltage have been decreasing. Therefore, the increase in chip power dissipation is primarily due to the greater number of gates on a chip made possible by the decrease in the feature size.

Device miniaturization has resulted in significant improvement in on-chip switching speeds. These improvements impact the technologies used for interconnection from level 1 to level 2. Off-chip driver rise-time trends for ECL, CMOS, and GaAs are shown in Fig. 7.11. MOS circuits are known to be more sensitive to loading conditions due to their relatively high output impedance. Hence, interconnect density is more important in MOS systems than for bipolar designs. As the applications for these devices tend toward the nano- and subnanosecond signal rise times, more attention will be directed to the electrical design consideration of packages and interconnections.

Reduced unit cost per function is a direct result of miniaturization. The cost per bit of memory chips was cut in half every two years for successive generations of DRAMs. By the year 2005, the cost per bit is projected to be between 0.1 and 0.2 microcents for a 1-Gb memory chip. Similar cost reductions are projected for logic ICs. Packaging and interconnection greatly impact the overall cost of the device. The package technology used can be a significant portion of the total device cost, ranging from 10 percent for DRAMs in a low-cost plastic SOJ to 50 percent for complex devices in multilayer ceramic pin grid arrays (CPGAs).

Chip-to-package interconnection, in particular wire bonding, can dictate the physical size of the silicon and thus the cost of the chip. The mechanical limit in gold ball bonding is the minimum pitch between adjacent ball bonds on the chip. The current production limits are in the order of 0.0028-in (70-μm) pitch, but when the bond pads are staggered, as illustrated in Fig. 7.64, the effective pitch (wire-to-wire pitch) can be reduced to approximately 0.002 in (50 μm). The active area required is determined by the design rules for the particular wafer fabrication process used in manufacture. As device miniaturization progresses down the curve in Fig. 7.5, the device designer will be capable of placing more active circuitry, requiring more I/Os, onto each chip. A condition where, for a given number of I/Os, the chip size design is dictated by the effective bond-pad pitch on the perimeter of the chip is known as a *bond-pad-limited* chip. The bond-pad pitch has a profound effect on the chip cost. For example, at the 500-I/O level, the chip cost decreases approximately 64 percent as the in-line pitch decreases from 0.004 to 0.0028 in (100 to 70 μm). These considerations are driving the interconnect technology vendors to develop finer-pitch wire-bonding capability and forcing the packaging engineer to evaluate alternatives, such as TAB and FC bonding techniques. This is covered in Secs. 7.7.1.2, 7.7.1.3, and 7.7.1.4.

*7.1.2.2 System-Level Demands.* The rapid advances in wafer fabrication also drive system-level demands. Effective utilization of chips with improved performance, that is, faster on-chip switching speeds, requires higher device density at the second level of interconnection. This is achieved by considering several aspects of IC packaging simultaneously; the physical size of the package, lead spacing or pitch, and the method of attachment to the next level of interconnection.

The DIP family, introduced in the early 1970s, with dual in-line leads on 0.100-in (2.54-mm) centers, becomes prohibitively large (Fig. 7.12) as the number of I/Os increases to levels needed to accommodate the more complex chips. Pin grid arrays (PGAs), with leads arranged in a 0.100-in. (2.54-mm) area array pitch instead of in-line, provide improvement in area savings over the DIP. However, as the requirement for I/Os increases beyond 300 leads, the PGA package sizes again become very large and intolerable. In the late 1980s, a different type of package, the ball grid array (BGA), was devel-

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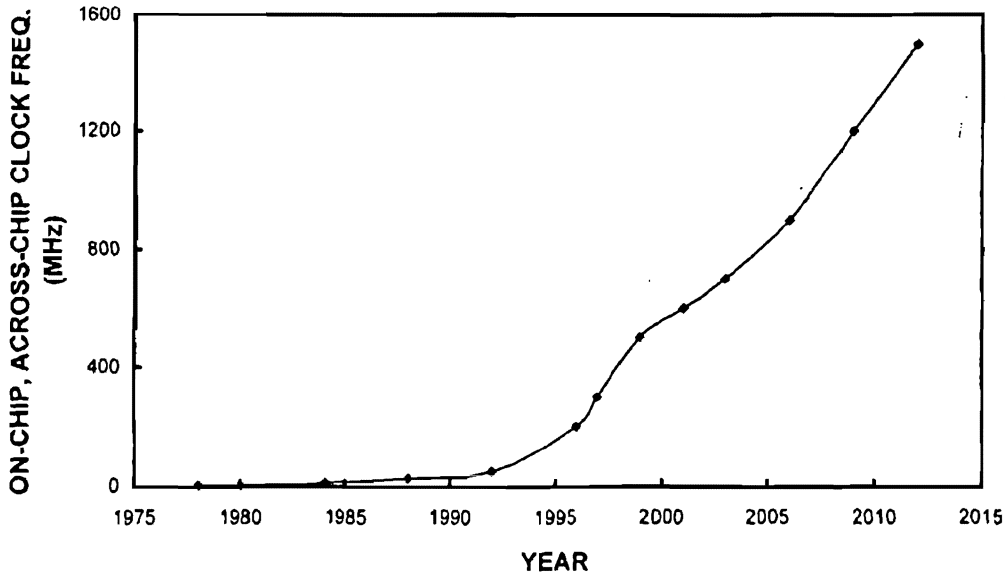


FIGURE 7.10 Frequency trends of high-performance ASIC chips. *(After SIA[3])*

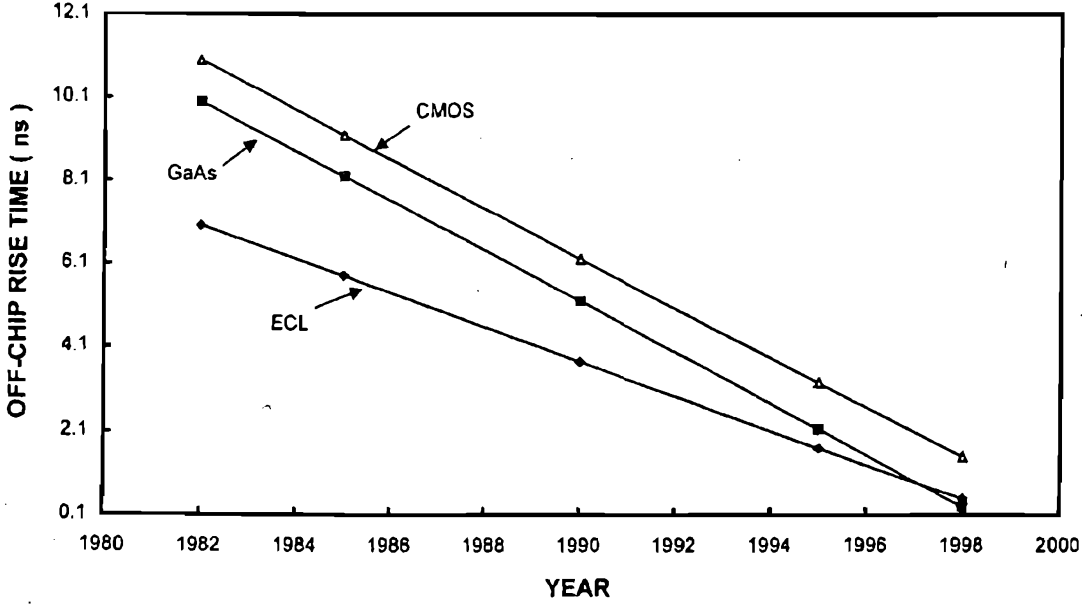


**FIGURE 7.11** Off-chip driver rise times (typical loading). *(After SIA[3])*

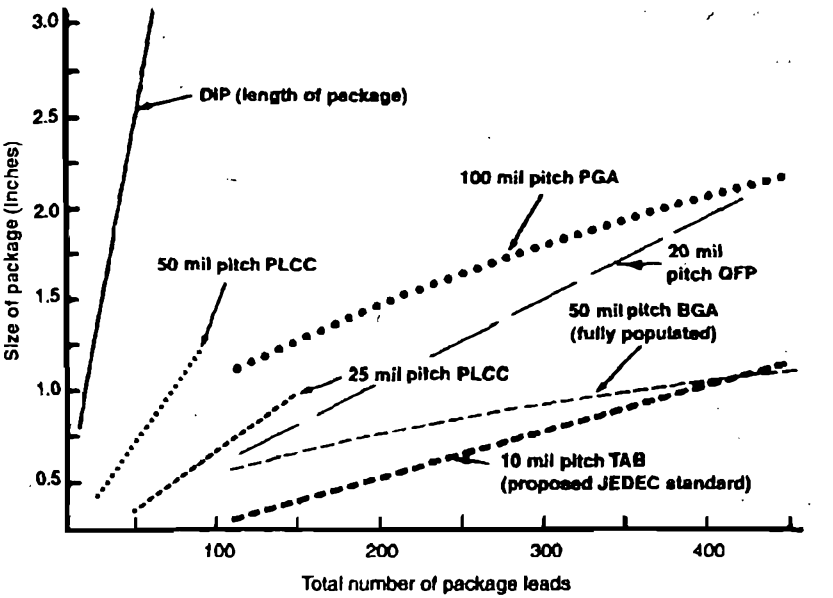


FIGURE 7.12 Sizes of some common TH and SM packages as a function of number of package leads and pitch.

oped that offers a high density solder bumped array, down to 0.020-in (0.5-mm) pitch, for surface mounting (SM). The ball grid array (BGA) is thus becoming the package of choice because of its smaller size per I/O count (Fig. 7.12) and better electrical characteristics.

Within a given package, there is a distribution of traces that connect the chip to the external leads. Large packages, and in particular those with rectangular shapes such as DIPs, require very long traces to the corner leads of the package. Array-type packages, typically square, also contain a distribution of traces, with the longest trace going to the outermost rows of leads in particular those in the corner of the package. This distribution of trace lengths within the package, in series with similar distributions of trace lengths on the PWB due to the location and placement of large packages, could result in undesirable signal delays, missed line driver requirements, or crosstalk between critical signal leads. Hence, the demands on packaging are for smaller physical-size packages (see Sec. 7.3.) with higher-density circuitry, thus minimizing the variation of trace lengths within the respective distributions and reducing their undesirable effects on performance. Figure 7.12 compares the package areas for some typical surface mount (SM) and through-hole (TH) mount packages.

High-density packaging cannot be achieved with TH-type packages, such as DIPs and PGAs, that are limited to 0.100-in (2.54-mm) lead pitch by current IC package and PWB design rules and process capabilities. Either perimeter or array-type SM packages with finer lead-pitch capability are needed to satisfy this demand. Some packages now require more than 1000 I/Os, an unachievable task for perimeter packages. But, given an array type package like the BGA, with a 0.040-in (1.0-mm) pitch, the feasibility of meeting the

1000+ I/Os capability becomes much more attractive. Through-hole (TH) packages require one hole for each pin, typically 0.035 in (0.90 mm) in diameter. Current PWB ground rules dictate that THs must be on 0.100 in (2.54 mm) grid to have a viable manufacturing process. Surface-mount technology (SMT) eliminates the need for through holes. Perimeter leads for SM packages with a pitch as fine as 0.016 in (0.40 mm) have been achieved, but handling and assembly at these levels has been difficult.

The demand for SM packages has placed a great deal of pressure on the IC package technology. Processes such as vapor-phase (VP) and infrared (IR) solder reflow have placed stringent requirements on the physical design of SM packages that were not required for the TH types. Some of the most important aspects are lead integrity, lead finish, lead geometry, lead true position and thermal effects. To ensure a reliable and high-yield (cost-effective) SM attachment, the perimeter leads on a SM package must be coplanar to within 0.002 to 0.004 in (0.05 to 0.10 mm), and the solder balls on a BGA must be coplanar to within 0.006 to 0.008 in (0.15 to 0.20 mm). In contrast, lead lengths are not critical with TH components, since the assembly process used usually calls for the leads to be cut off after insertion into the PWB and then crimped to provide mechanical backup. The solder joint is another critical item for SM packages. Since the solder joint provides both electrical connectivity and mechanical attachment of the packaged device, its integrity must be preserved through all the stress encountered in subsequent assembly and test, over the life of the system in its operating environment. Solder embrittlement must be avoided; hence, lead-finish materials and the gold plating thickness on BGA solder pads must be specified with care.

Variations in package mounting to PWBs are illustrated in Fig. 7.13. The lead geometries shown in Fig. 7.13*a* through *g* are in common use today for attachment to practically any substrate material. Each shape has its unique list of advantages and disadvantages, some of which are covered in Sec. 7.5.

Reliability of SM packaged devices could be affected directly by the stresses imposed during VP or IR solder reflow. This is particularly true if the packaged device is inadvertently exposed to high levels of moisture during the periods of time between device assembly and board assembly. Immersion of the package into the hot vapor of VP soldering or direct heating by IR occurs so rapidly that even small amounts of moisture, on the order of 0.20 percent by weight, could subject the package to severe internal stresses and initiate cracks from the device surface to the outside. Most of these fine cracks are not readily detected by visual inspection after board assembly because, initially, they are usually nonfatal to the device and are hidden from view at the package surface. But, if left undetected, the fine cracks may provide a relatively easy path for the ingress of contaminants from fluxes and solvents used in board assembly, and moisture from subsequent operations such as testing, shipping, storage, or from the ambient. These contaminants may result in conditions at the IC-to-package interface that could lead to premature reliability failures.

The thermal design objective of SM packages is to operate at a junction temperature, $T_j$, low enough to prevent temperature-activated reliability failures, such as chemical corrosion or interfacial diffusion, prior to the design end of life. In addition, the electrical performance of the devices, that is, their electrical speed and the fundamental device physics, are affected adversely by temperature. The thermal analysis of the package will need to consider the complete environment to which the package will be exposed over its lifetime. Specific variables such as PWB operating temperature, total PWB power dissipation, local neighbor power dissipation, cooling technique used, thermal properties of the materials used, and any special requirements defined by the system user must be considered. No longer can the packaging engineer specify a generic package for a system and expect it to meet all system requirements without considering all possible conditions that the component will encounter in the field.

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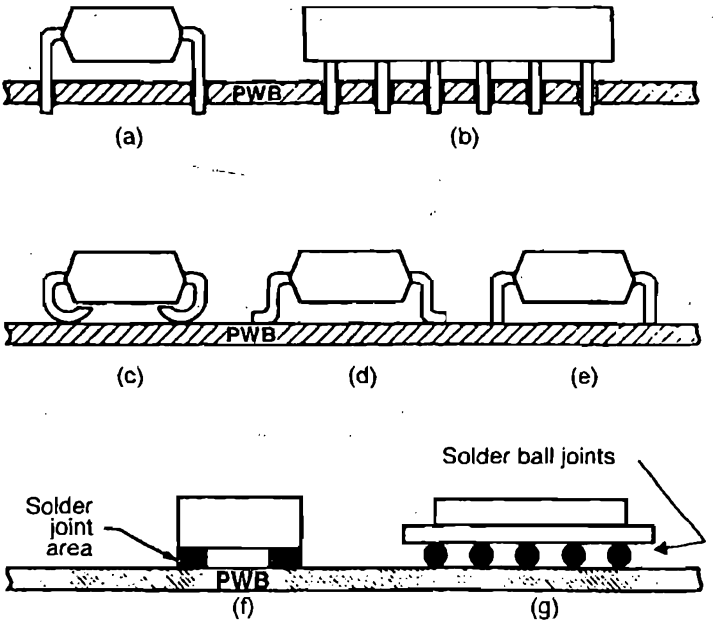


**FIGURE 7.13** Examples of packages, package lead geometries, and mounting methods in current use: (*a, b*) typical TH packages, (*c–g*) typical SM packages. Lead geometry options are (*a*) DIP, (*b*) PGA, (*c*) SOJ and PLCC, (*d*) SOIC, SOG, QFP, PQFP, and fine-pitch LDCC, (*e*) butt-leaded package, (*f*) LLCC, and (*g*) BGA.

Improved quality, reliability and cost are other system demands receiving much attention today. Systems manufacturers are driving down their costs and consequently are putting great pressure on the quality and reliability of the components that they purchase. Terms such as *zero defect* are used to define quality and reliability objectives and *just-in-time* (JIT) manufacturing to describe the strategy for reducing cost associated with having to carry large in-plant inventories. JIT manufacturing requires that the assembly lines be running defect-free, which demands very high-quality components and assembly processes. Today, the quality of the product received by the system user is expected to have incoming defect levels in the parts per million (ppm) or even parts per billion (ppb) range.

Reliability requirements are also becoming more stringent. System users require that packaged devices pass moisture pre-conditioning followed by several reflow simulations, temperature-humidity-bias (THB) test and an accelerated temperature-humidity test such as the pressure-cooker test (PCT). Figure 7.48 illustrates typical test requirements for device qualification.

The packaging of more complex high-I/O devices into smaller high-density SM packages will severely challenge the thermomechanical reliability of the package. These new high-density packages, constructed with a variety of materials, exhibit a wide range of thermal expansion coefficients and strength properties. The packages are being subjected to a variety of temperature stresses such as those encountered in first level of package assembly, test, burn-in if required, and SM board assembly, with the cumulative effect

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being an increased potential for failure due to thermally induced stress. The package engineer will be forced to evaluate the thermomechanical stresses during the initial stage of the design before committing capital and expense dollars to the project. The analysis is used to gain insight and confidence that the design will have a good chance, at an acceptable risk, of meeting all objectives. Computer-aided design (CAD) tools such as the finite-element analysis can be used to perform these complex two- and three-dimensional analyses.

## 7.2 CONVENTIONAL PACKAGE TECHNOLOGIES

IC package technologies fall into three basic categories: molded plastic, pressed ceramic, and laminated ceramic/plastic technologies.

In the molded plastic technology, the package is constructed around the IC chip assembled on a metal lead frame in strip form. The IC chip is first mechanically bonded to the die attach paddle and then electrically interconnected by fine wires from chip bond pads to the corresponding package wire bond fingers. If TAB bonding is used, then the IC chip pads are directly connected to the bumped lead frame fingers. The final package configuration is formed by plastic molding around the lead frame subassembly. The portion of the lead frame that is external to the package body is subsequently trimmed and formed into specific geometries suitable for either TH or SM attachment.

The pressed ceramic technology package contains a lead frame embedded and glass sealed into a pressed ceramic base. The IC chip is attached and wire bonded to the lead frame and hermetically sealed using a ceramic cap or lid. The leads external to the package body are trimmed and formed to the geometries needed for TH or SM attachment.

A laminated ceramic or plastic package circuitry consists of a substrate with an integral metallized fanout circuitry and external terminals that are either leadless, leaded, or with solder balls for SM, or leaded for TH attachment.

The substrate body may come with either a cavity to accept the chip or an in-plane configuration where the chip attach area and the bond pads are on the same level. The electrical interconnections are done using assembly techniques similar to those used with the plastic molded package types. The substrate material may be either ceramic or plastic, of single-layer or multilayer construction, depending on the functional requirements. Both the ceramic and plastic substrates can equally provide high performance, but the ceramic has hermetic sealing capability, whereas the plastic substrate is overheat and requires some form of epoxy encapsulation for environmental protection of the chip.

A comparison of cost, performance, and reliability among the various package technologies shows the multilayer ceramic package to be best suited when the requirements call for high performance, hermeticity, and high reliability, but the trade-off is high cost. A multilayer plastic package, with electrical and thermal enhancements (see Sec. 7.2.4), can provide equal or better performance at a lower cost, trading off hermeticity. For the lower end of consumer electronic products, the package requirements, in order of importance, are low cost, reliability, and performance. These attributes can be satisfied with plastic molded packages, the proper selection of materials, and rigid process controls. Sections 7.2.1 to 7.2.4 discuss packaging technologies that are generally applicable to a variety of package types and families. Section 7.4 presents package technology comparisons and trade-offs.

### 7.2.1 Molded Plastic Technology

The plastic package technology is widely accepted in the industry as reliable and low in cost. Package family outlines have been standardized in the Electronic Industries Alliance

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(EIA), the Joint Electron Device Engineering Council (JEDEC), and the Electronic Industries Alliance of Japan (EIAJ). These are covered in Sec. 7.5.

*7.2.1.1 Post-Molded Plastic Package.* Figure 7.14 illustrates the construction of a QFP in the post-molded plastic package technology. A metal lead frame, usually copper, copper alloy, or Alloy-42 (42 percent Ni, balance Fe) provides the mounting surface for the chip, that is, the chip support paddle. The lead frame also provides the electrical fanout path from the fingers to the outside leads, which vary in pitch from 0.040 in (1.0 mm) to 0.016 in (0.40 mm) as shown in Fig. 7.14. The lead frame is usually spot plated with silver or gold on the paddle and at the tip of the wire-bond fingers to provide reliable chip attachment and wire bonds. Silver spot plating is gaining popularity for lowest cost and better adhesion to the molding compound. Wire-bond interconnects are gold wires, typically 0.00125 in (0.032 mm) in diameter, with wire span lengths ranging from 0.050 to 0.200 in (1.27 to 5.08 mm) with the potential of extending the length to 0.225 in (5.72 mm) in the near future. Thermosetting (cross-linking) epoxy resin is molded around the lead-frame-chip subassembly after the chip has been wire-bonded to the lead frame, that is, the package is molded around the chip in situ. After molding, the external portion of the lead frame must be processed to the final form and lead finish for assembly to the next level. This assembly sequence is shown in Fig. 7.15 and applies to all plastic molded package types. Details such as lead-frame design and format, workholders for chip and wire bonders, molding dies, trim and form tools, and handling hardware will vary according to package types.

The post-molding process is relatively harsh. Major yield and reliability problems, observed in post-molded parts, are wire sweep caused by the flow of viscous molding materials, and local stresses on the device surface caused by sharp edges of filler particles. The use of round-edge filler particles have reduced the IC surface microstresses. In addition, plastic packages, being overheat, have a tendency of allowing moisture to ingress to the device very rapidly, on the order of days, as shown in Fig. 7.16. The aluminum metallization generally used in IC manufacture is susceptible to rapid corrosion in the presence of moisture, contaminants, and electric fields. Impurities from the plastic or other materials used in the construction of the package can cause voltage threshold shifts or act as catalysts in metal corrosion. Fillers can also affect reliability and thermal performance of the plastic package. Advances have been made on the IC devices themselves in the form of improved passivation, such as silicon nitride and others, to achieve a "nearly hermetic" chip. This is desirable to protect the chip from the potentially hostile environment encountered in the plastic molding technology.

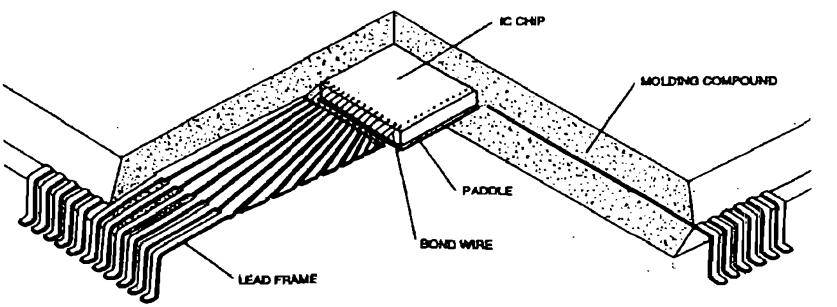


**FIGURE 7.14** Sectional view of a typical QFP illustrating molded plastic (post-molded) technology.

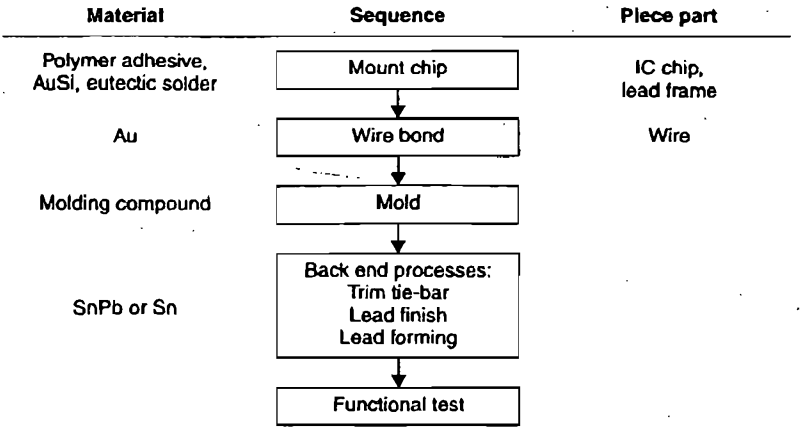


**FIGURE 7.15** Assembly sequence for post-molded plastic technology packages.

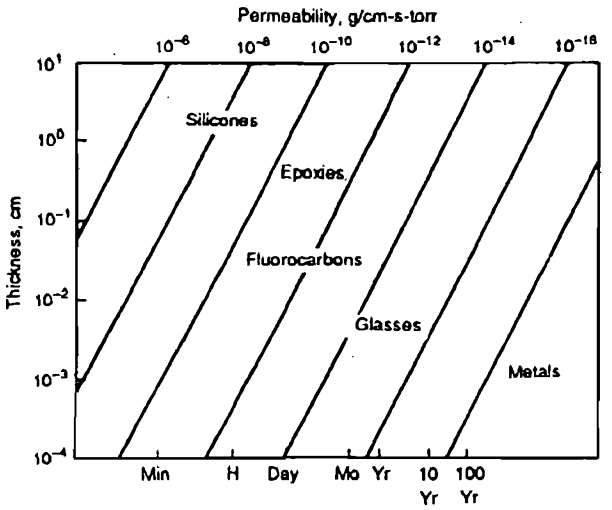


**FIGURE 7.16** Calculated time for moisture to permeate various sealant materials (to 50 percent of exterior humidity) in one defined geometry. Organics are orders of magnitude more permeable than materials used for hermetic seals.

The two critical steps in producing a molded product, which meet the device reliability objectives, are selection of the molding material and control of the molding process itself. Overall integrated automation of the assembly process, in particular the automation of chip attachment, wire bonding, molding and selection of die attach material, are also

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important. The polymer most commonly used for plastic IC packages is epoxy. The composition of a typical epoxy molding compound, shown in Table 7.1, consists of the epoxy resin portion (approximately 25 to 35 percent by weight of the total composition), a hardener, and a curing agent. Novolac epoxies are generally preferred, because their higher functionality gives them improved heat resistance. The synthesis of the resins produces sodium chloride as a by-product. Both sodium and chloride ions are deleterious to device reliability. Therefore, these by-products must be washed carefully from the resins before they are synthesized into useful molding compounds. Reduction of the chloride content in the epoxy resin is especially effective in decreasing corrosion of the aluminum metallization in plastic packages.

**TABLE 7.1 Composition of Epoxy Molding Compounds**

| Material Family | Example | Purpose | Technology Thrust |
|---|---|---|---|
| Epoxy resin | Bisphenol-A epoxy, Novolac epoxy | To cure by a cross-linking reaction | Lower ionic impurities (lower $Cl^-$) |
| Hardener | Amine, anhydride, phenol Novolac | To cure by a cross-linking reaction | — |
| Reaction accelerator | Tertiary amine | To cure by a cross-linking reaction | — |
| Filler | Silica powder, alumina powder, glass fiber | Adjust CTE, thermal conductivity, mechanical strength | Low alpha particle (lower uranium) |
| Flame-retardant agent | Brominated epoxy, $Sb_2O_3$, hydrited alumina | Flame retardancy | — |
| Coupling agent | Epoxy silane, amino silane | Better contact between resin and filler | — |
| Releasing agent | Stearic acid, natural wax, synthetic wax | Release from mold | Balanced releasing contact |
| Coloring agent | Carbon black, iron black, $FeO_3$, organic dye | Coloring | Laser marking |

Molding compound vendors are constantly upgrading the properties of their materials to achieve improved performance. Fillers, such as amorphous or crystalline silica ($SiO_2$) or glass fibers, and sometimes $Al_2O_3$, are added to the resin so that the resultant mixture is 65 to 73 percent filler by weight. Amorphous $SiO_2$ is used when a minimum expansion coefficient is desired, at some sacrifice of thermal conductivity, while crystalline $SiO_2$ improves thermal conductivity at the expense of the coefficient of thermal expansion. $Al_2O_3$ has a high thermal conductivity (as a filler material) but is very abrasive to molds. Fillers greatly improve the mechanical strength of the resin and reduce its coefficient of thermal expansion, hence reduce shrinkage after molding. Silica fillers normally contain uranium and thorium, which radiate alpha particles and may cause reliability failures (soft errors) in alpha-sensitive memory devices. The introduction of low alpha radiation molding compounds and the development of devices with structures that are immune to alpha particles has minimized soft errors.

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Small amounts of pigments, coupling agents, mold release agents, reaction accelerators, antioxidants, water getters, plasticizers, and flame retarders must also be added to complete and optimize the molding resin. Coupling agents improve the adherence of the resin with the organic fillers, metal lead frames, and silicon chips. This minimizes moisture penetration at the various interfaces and improves device reliability. Mold release agents are used to release the molded part from the mold. Since they can also decrease the adherence of the resin to the lead frame, their behavior and effect on device reliability must be carefully evaluated. Reaction accelerators may decrease the volume resistivity of the molding compound. A flame retardant, normally brominated epoxy and antimony trioxide, is added to meet the industry flammability standard (UL94 V-O). Selection of all additives must be made very carefully to optimize the reliability of the molded device.

It is important to understand the rheological, chemical, and thermophysical properties of molding compounds, both for the molding process and for their interrelation with the reliability of the finished device. Moldability and the thermal expansion coefficient are two of the most important characteristics of a molding compound. The molding process is not cost-effective unless it has high yield. The most common reliability problems can be related to the mechanical quality of the molded part and its ability to withstand thermal stresses.

Thermoset molding materials are usually transfer molded in large multicavity molds (Fig. 7.17). After entering the pot, the preheated molding compound, under pressure and heat, melts and flows to fill the mold cavities containing lead frame strips with attached and wire bonded ICs. The IC lead frame often has long, fragile lead fingers, particularly in the higher I/O package types. The chip is interconnected to these thin, fragile leads with 0.001 to 0.00125-in (0.025 to 0.032-mm) diameter gold wires at wire spans from 0.050 to 0.200 in (1.27 to 5.08 mm) in length. To avoid damaging this fragile structure, the viscosity and velocity of the molding compound entering the mold must fall within certain ranges. Commercial molding compounds are designed to meet these requirements when molded at approximately 175°C, with pressures of about 6 MPA and a mold cycle that ranges from 1 to 5 min. Figure 7.18 shows an 80-cavity mold used for a 68 I/O PLCC.

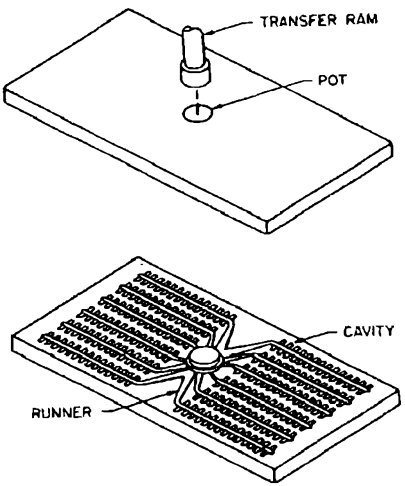


**FIGURE 7.17** Schematic of a manual, single-plunger, multicavity transfer mold showing ram, pot, and runner system. Small packages such as DIPs or SOs use molds containing upward of 168 cavities, while larger packages such as high-I/O PLCCs use molds with fewer cavities, such as the 80-cavity mold of Fig. 7.18.

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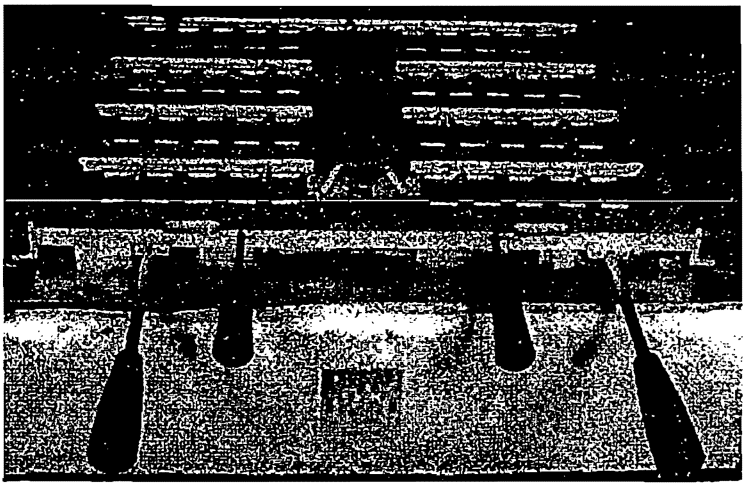

**FIGURE 7.18** 80-cavity transfer mold for 68-I/O PLCC. Each lead frame accommodates five chips; cavity gate is located in corner of package.

To control the velocity of the molten molding compound, each device cavity has a gate, or restriction, to slow the material flow. The fluid mechanics of molding is relatively complex, because the materials are non-Newtonian. In addition, partial cross-linking can occur during the molding process, affecting the material viscosity. Elaborate mold designs have been proposed to compensate for these variables. An automated multipot approach, as shown in Fig. 7.19, can also provide improved control of these molding variables.

The reliability performance criteria for post-molded plastic packages are defined by the level of stresses resulting from expansion mismatches within the package and by performance of the packaged device in a humid environment. Figure 7.20 illustrates how thermal expansion differentials between two leading lead frame materials and typical molding compounds cause changing conditions at the interfaces during thermal sequences. For example, the conditions change from interference fits on cooling to room temperature, to tensile stresses, at the higher temperatures encountered during solder reflow at board assembly.

The molding compounds exhibit two distinct expansion rates. Below the glass-transition temperature $T_g$, the rate $\alpha_1 \approx 20$ ppm/°C and above $T_g$, the rate $\alpha_2 \approx 60$ to 70 ppm/°C. The expansion rates for the lead-frame materials are linear over the temperature range shown, with Alloy-42 at $\approx 4.3$ ppm/°C and copper at $\approx 17$ ppm/°C. During cooling from the molding temperature (≈175°C), the molding compound contracts faster than the lead frame, thus causing an interference fit between the two materials. This tight fit will prevent the entry of unwanted contaminants and impede the ingress of moisture into the chip region of the package. Unfortunately, as the package is subjected to board assembly processes, such as solder reflow, the stress at the interface reverses from the compressive stress experienced below $T_g$ to a tensile stress at the solder reflow temperature of ≈245°C. Under this condition, a gap may form between the molding compound and the lead frame, depending on the magnitude of the tensile stress and the initial chemical adherence of the molding compound to the lead frame. A similar stress differential exists between the chip

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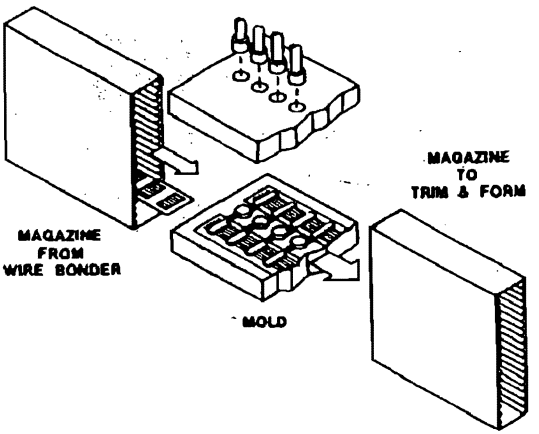


**FIGURE 7.19** Schematic of two-strip, automatic multiplunger molding system. Lead frames are loaded and unloaded directly from and into magazines that are compatible with assembly equipment located upstream (wire bonding) and downstream (trim and form) from molding operation. Schematic illustrates one pot for two cavities and requires fast-curing molding compounds to achieve similar economics as large multichip cavity molds.

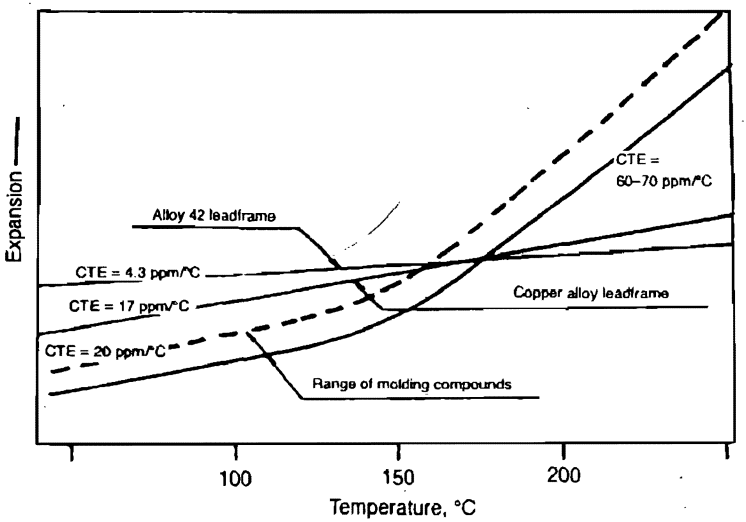


**FIGURE 7.20** Thermal expansion rates for molding compounds and lead frames. *(After Murtuza et al.,* [5] *© 1986, IEEE)*

surfaces and the molding compound due to the differences in the coefficients of thermal expansion between the silicon and the molding compound, as seen in Fig. 7.21. Gap formation is undesirable because fatal contaminants may find their way to the wire-bond pads on the chip and result in reliability failures in the field due to aluminum corrosion. To avoid these problems, much attention must be given in selecting the proper materials, for both lead frame and molding compound, and in specifying the lead-frame finish and design, such as the addition of special features for locking in the leads that will prevent slippage between the critical surfaces. Automation increases the need for more aggressive molding compound properties, which will lead to faster cure cycles and better batch-to-batch control of critical properties. Most of the molding compounds used for post-molded plastic packages require at least four hours cure at 150°C to complete the cross-linking process and stabilize the material. The post mold cure of four hours is a rather long process time. To assist the assembly house in streamlining the assembly process and reduce the lead-time, several molding compound manufacturers have come up with non-post mold cure compounds. Some assembly houses have qualified the non-post-molded cure compounds and process with excellent results. The non-post-molded cure process is gaining popularity and will become mainstream when more data and materials become available.

Molding equipment vendors are being encouraged to provide process flexibility, that is, the ability to mold a wide variety of packages in smaller production runs, with the intent to automate the molding process. Users today have many options, which range from production molds (Figs. 7.17 and 7.18), handling many packages per shot, to automatic multiplungers with small pots (Fig. 7.19), handling only a few packages per shot. These multiplunger types require lower transfer or injection pressures, which results in minimum wire sweep, fewer voids, better flash and bleed qualities, and more processing latitude.

*7.2.1.2 Premolded Plastic Package.* A premolded package concept, shown in Fig. 7.22, provides a more benign environment for the chip. Delicate wire spans and strain-sensitive features on the chip surface are decoupled from the molding process, thus avoiding the stresses associated with post-molded packages. The assembly sequence for a premolded plastic technology package is shown in Fig. 7.23.

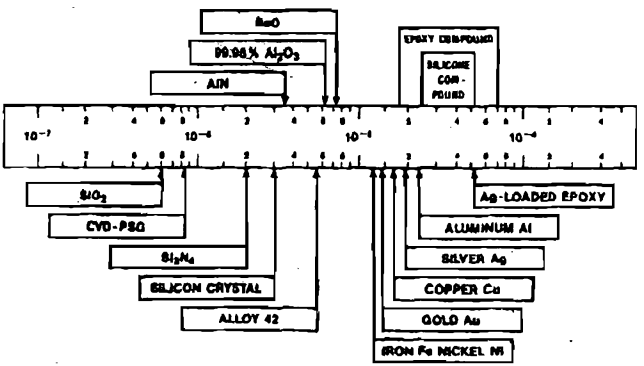


FIGURE 7.21 Coefficients of thermal expansion of materials for semiconductor devices, $°C^{-1}$. CTE of FR-4 and other PWB materials (not shown in figure) fall within 1.2 to 1.5 ($10^{-5}$) $°C^{-1}$ range.

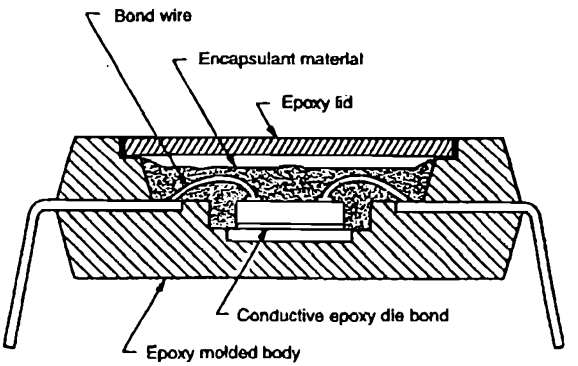


**FIGURE 7.22** Cross-sectional view of a completed premolded plastic DIP, including IC chip.

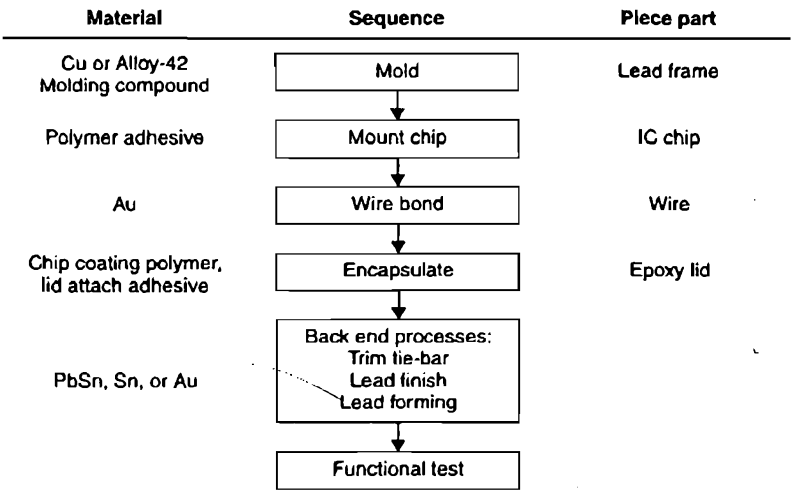


**FIGURE 7.23** Assembly sequence for premolded plastic technology packages. Package is fabricated using preplated lead frame then either transfer or injection molded using a thermoset epoxy B or a thermoplastic polymer molding compound.

The package is fabricated using a preplated lead frame, in strip form with multiple sites per strip, and then either transfer molded, using a thermoset epoxy B molding compound, or injection molded, with a thermoset or a thermoplastic polymer such as polyphenylene sulfide. The lead frame, usually made of a copper alloy for better thermal performance, is spot plated with either silver or gold in the die attach paddle area and wire bond fingers. The external leads may be selectively plated with thin gold to retain solderability for final

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lead finishing. After molding, the package may need to be deflashed to remove any molding compound flash deposited on the chip-bonding areas and then cleaned to remove any residual particulate matter. Chip attachment is done with a polymer adhesive, either conductive (silver-filled) or nonconductive epoxy or polyimide paste. Wire bonding is either thermosonic or thermocompression ball-wedge bonding using 0.001 to 0.00125-in (0.025 to 0.032 mm) diameter, 99.99 percent pure gold wire. This is followed by chip encapsulation with a die coating or, preferably, a flow coating to fill the entire cavity, thus environmentally protecting the chip and the wedge bond areas in the cavity. Candidate materials include room temperature vulcanized (RTV) silicone rubbers and combinations of silicon gels and cover coats.[4] In some cases, a plastic lid is used instead of encapsulation. Back-end processes include trim and form to the final package configuration, be it a DIP or a plastic leaded chip carrier (PLCC). Final lead finish is then applied by solder dipping. Another option is to use the original thin gold plate as the final finish, making sure that solderability is not degraded in the assembly process. A gross leak tight-lid seal will preclude the subsequent ingress of cleaning solvent (used in PWB assembly) into the chip cavity, where it could interact with the flow coat to cause swelling and stress the delicate wire bonds or degrade the interface integrity between chip and encapsulant.

The benign chip environment provided by the premolded package construction sequence is similar to that provided by a ceramic cavity package. Striny and Schelling[4] reported superior reliability performance during the temperature-humidity-bias (THB), 85 percent RH and 85°C test of 4-kbit MOS DRAM devices in premolded plastic packages compared with a post-molded package control group containing devices from the same wafer lots. The premolded plastic technology is potentially useful for packaging very sensitive IC devices requiring low-cost assembly. The post-molded package technology, on the other hand, is the more cost-effective of the two and is by far the predominant package technology in use today.

### 7.2.2 Pressed Ceramic (Glass-Sealed Refractory) Technology

Pressed ceramic technology packages are used mainly for economically encapsulating ICs requiring hermetic sealing. Hermeticity means that the package must pass both gross and fine leak tests and also exclude environmental contaminants and moisture for a long period of time. Further, any contaminants present before lid sealing must be removed to an acceptable level before or during the sealing process. Glass, as illustrated in Fig. 7.16, is an effective material for achieving a hermetic seal for high-reliability applications. Leak rate, as defined by MIL-STD-883, is "that quantity of dry air at 25°C in atmospheric cubic centimeters per second flowing through a leak or multiple leak paths from a high-pressure side of one atmosphere (760 mm Hg absolute) to the low-pressure side at or less than 1 mm Hg absolute." Standard leak rates are expressed in units of atmosphere cubic centimeters per second (atm • $cm^3/s$). Procedures for detecting gross and fine leaks in hermetic packages are detailed in MIL-STD-883. Gross-leak tests, such as die penetrants and bubble tests, are capable of detecting leaks in the range of $10^{-1}$ to $10^{-5}$ atm • $cm^3/s$. Fine-leak testing procedures, such as helium and radioactive tracer techniques,[6] will detect leaks in the range from $10^{-4}$ to $10^{-9}$ atm • $cm^3/s$. MIL-STD-883 requires that hermetic packages pass a leak test at $10^{-8}$ atm • $cm^3/s$ on equipment having a detection sensitivity of at least $10^{-9}$ atm • $cm^3/s$.

The process flowchart[7] for fabricating the basic piece parts used in the pressed ceramic packaging technology is shown in Fig. 7.24. Also shown alongside is the process flow sequence for the laminated ceramic package technology, which is described in Sec. 7.2.3. Pressed ceramic piece parts require fewer and simpler process steps, resulting in the low-

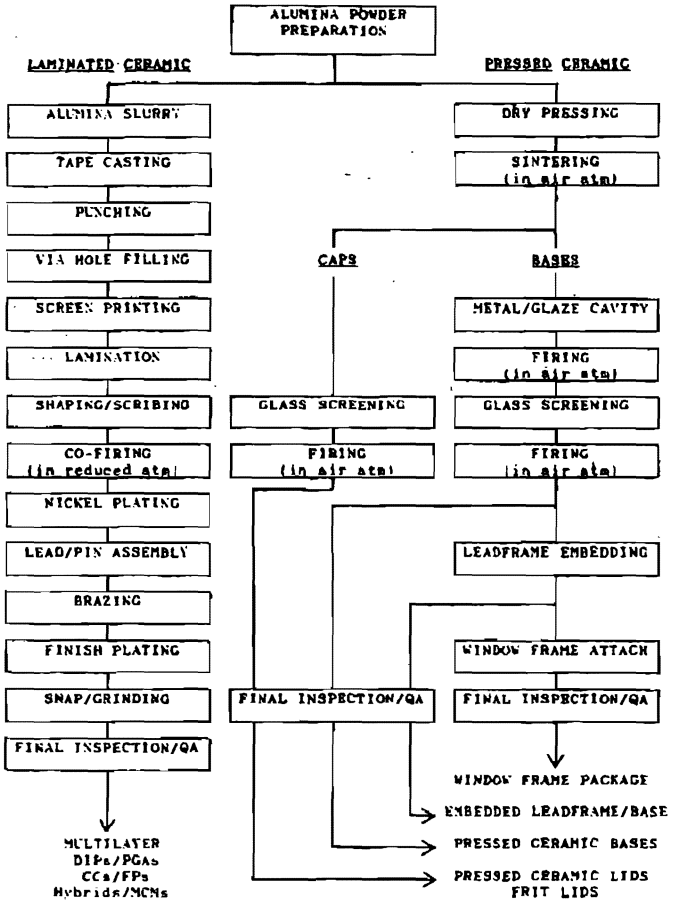


**FIGURE 7.24** Process flowchart for piece parts and prefabricated packages for pressed ceramic and laminated ceramic package technologies. *(After Kyocera[7])*

est-cost piece parts for a hermetic package technology. This technology, when implemented with a lead frame in strip format (that is, multiple sites per strip) can be automated and therefore is competitive with the plastic technology for low-cost packaging. The IC package designer has a choice of three pressed ceramic options as shown in Fig. 7.24: basic piece parts (bases and caps), partially assembled subassemblies (embedded lead frame and base), and a prefabricated package known also as a window-frame package. The IC assembly sequence is described in Fig. 7.25.

In the first option, the package is constructed around the IC chip using basic piece parts, for example, ceramic base, lead frame, and ceramic cap. When done in house, this is the lowest-cost option, because the IC manufacturer controls all of the assembly process

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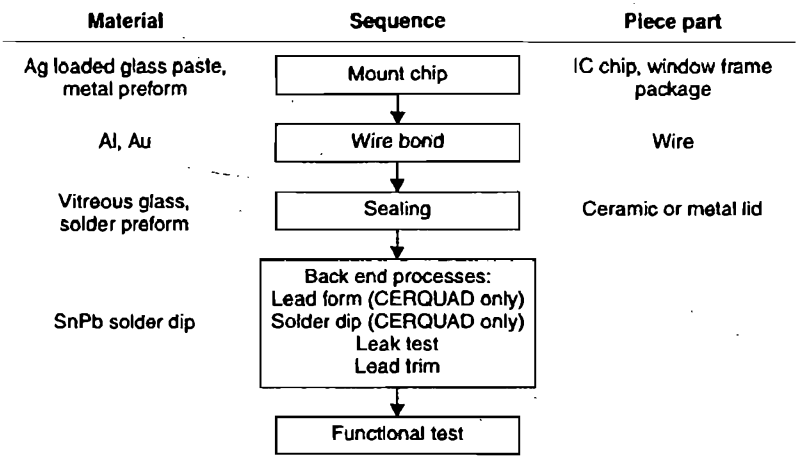


**FIGURE 7.25** IC assembly sequence for pressed ceramic package technology.

steps. Option 2 is a minor variation of option 1, where the IC manufacturer purchases the lead frame already embedded into the base ceramic and ready for IC chip mounting. This option is attractive to manufacturers who do not have, nor wish to invest in, the equipment needed for embedding the lead frame. These options are known in the industry as the CERDIP or CERQUAD packaging technology. The assembly structure is shown in Fig. 7.26*a*.

In both options, the IC chip is attached to the lead frame using either AuSi eutectic or silver-loaded glass adhesive technologies. Hermetic sealing is done with a glassed ceramic cap or lid. Due to the relatively high temperature used for glass sealing, typically greater than 400°C, an all-aluminum monometallic system is used. This consists of the aluminum bond pads on the chip, ultrasonic aluminum wedge-to-wedge wire bonding, and lead frame fingers that have aluminum deposited or cladded surface finishes in the bond areas.

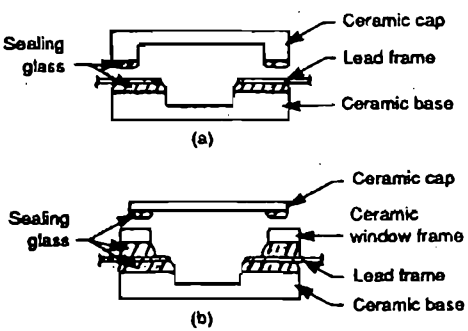


**FIGURE 7.26** Structures of (*a*) CERDIP and (*b*) window frame. *(Courtesy of Kyocera America, Inc.)*

The gold-aluminum intermetallic interface, which has caused many reliability problems in the past, is thus avoided. Lid sealing is done in a controlled nitrogen atmosphere conveyor-type furnace in which the heat is transferred by conduction and convection or by infrared radiation. A typical sealing temperature profile, usually recommended by the package vendor, is shown in Fig. 7.27. Back-end processes include leak testing, lead finishing, and lead trim and form. External leads are typically plated with matte tin, which provides a finish that is compatible with the subsequent lead trim and form operation and final assembly to the next-level packaging. CERDIP lead frames are procured already formed and require only to be finished and trimmed prior to testing. Lead frames for SM types such as the CERQUAD, usually come planar and are processed planar through lead finishing, then trimmed and formed into the desired shape for the final package configuration.[8,9]

The third pressed ceramic option, known in the industry as a window-frame package, is the structure shown in Fig. 7.26*b*. The assembly sequence is given in Fig. 7.25. This design concept provides the option of decoupling the IC chip from the high-temperature glass-sealing procedure by providing a low-temperature solder seal capability for the final hermetic seal. This option is used for temperature-sensitive chips that cannot go into a glass-sealed package without degrading their performance or reliability. In addition, this option also allows the use of thermosonic or thermocompression gold ball-wedge wire-bonding equipment, which extends this package technology to those manufacturers who have this wire-bonding capability but not the ultrasonic aluminum wedge-to-wedge bonders needed to achieve the desired all-aluminum monometallic structure for glass seals. Back-end processes are similar to those used with the other options.

Two types of solder glasses are used today for glass sealing: devitreous or vitreous. Table 7.2 lists the major properties of some of the solder glasses currently in use. Seal glass is an important constituent of the pressed ceramic technology, because it influences both electrical performance and reliability of the packaged device. The dielectric constant of the glass used to embed the lead frame can affect the capacitance between the leads, that is, the speed of the I/O signals through the lead frame. Seal glass is exposed to the cavity; hence, alpha-particle emission from the glass fillers may affect the soft error reliability of some sensitive devices.

Glass sealing is a complex process that must be understood fully and implemented under rigorous control. Tight temperature control and minimum mechanical and thermal handling are necessary to minimize hermeticity yield loss. The hermeticity of the finished package[11] is influenced by the adhesion of the seal glass to the ceramic, the seal glass to the lead frame, the mechanical strength of the glass, and the dissolution of fillers into the

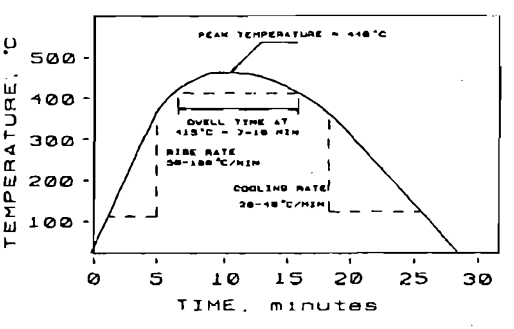


**FIGURE 7.27** Typical glass-sealing profile as recommended by package manufacturers.

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**TABLE 7.2 Major Seal Glass Properties**

| Filler System | Lead-Titanate-Zircon | Cordierite | Beta Eucryptite | Zircon |
|---|---|---|---|---|
| Glass type | Vitreous | Vitreous | Vitreous | Devitreous |
| Sealing temperature, °C | 450 | 430 | 430 | 485 |
| Dielectric constant | 33 | 12.2 | 12.1 | 17.8 |
| Alpha emission, count/(cm$^2$ · h) | 29 | 0.8 | 0.2 | 41 |
| Mechanical strength, kg/cm$^2$ | 550 | 460 | 460 | 650 |
| CTE mother glass, $10^{-7}$/°C | 110 | 110 | 110 | – |
| CTE Filler, $10^{-7}$/°C | –30/20 | 8 | –80 | 20 |
| Particle-size distribution | Very fine to coarse | Fine | Fine | Coarse |
| Filler volume ratio | High | Medium | Medium | Medium |
| Filler dissolution | Low | High | High | Low |

*Source:* From Loo[11]

mother glass. Residual stress in the mother glass (due to the mismatch in thermal expansion between ceramic, Alloy-42 lead frame, and glass) and particle-size distribution of the filler influence the mechanical strength, or the ability to provide reliable hermetic seals. Ideally, seal glass should have a low dielectric constant, high mechanical strength, low alpha emission, and low sealing temperature. None of the glasses listed in Table 7.2 comes close to the ideal glass definition, each having its advantages and disadvantages. The package designer must know which properties are needed for a particular device and base the selection of the glass on that input. For example, a device not requiring low-alpha-emission sealing glass, low dielectric constant, and low sealing temperature may be sealed using a lead-titanate-zircon system to take advantage of the high mechanical strength. On the other hand, if the device requires low-alpha-emission sealing glass, low dielectric constant, and low sealing temperature, either the cordierite or the beta eucryptite system may be the better choice.

The raw material for the pressed ceramic technology is alumina ceramic (90 percent minimum $Al_2O_3$) in black-brown characteristic color. Package vendors are also providing ceramic materials such as aluminum nitride (AlN), silicon carbide (SiC), and low-thermal-expansion sealing glasses (4.7 ppm/°C), for improving hermeticity yields of pressed ceramic. Pressed ceramic parts, made with SiC and low-thermal-expansion glass, were exposed to a sequence of mechanical shock (1500 g), vibration variable frequency (20 g) and constant acceleration (3000 g) test conditions. No hermeticity rejections were seen in a sample of 200 packages exposed to this sequence. A second group of 280 parts, exposed to a sequence of thermal shock (–65 to +150°C, 15 cycles), temperature cycles (–65 to +150°C, 100 cycles), and moisture resistance tests (10 cycles) also passed with no hermeticity rejections.

### 7.2.3 Cofired Laminated Ceramic Technology

The cofired laminated ceramic technology is the most reliable IC packaging technology currently available. The technology is constantly responding to the device- and system-level demands for higher performance and higher-density applications. This section

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addresses the technology for single-chip packages. The cofired laminated ceramic technology is also being used for such applications as hybrids and MCMs, which are covered in Chapter 9.

*7.2.3.1 High-Temperature Cofired Ceramic Technology.* The process flowchart for the cofired laminated ceramic package technology is shown in Figs. 7.24 and 7.28. A dispersion or slurry of ceramic powder and liquid vehicle (solvent and plasticized resin binder) is first prepared then cast into thin sheets by passing a leveling or doctor blade over the slurry. After drying, the sheets are in the green-tape stage, ready for cutting to size, punching of via holes (through the dielectric layers for future interconnection), and cavities. Custom conductor paths are then screened onto the surface (usually a slurry of tungsten powder), and the via holes are filled with metal. Several of these sheets are press-laminated together in a precisely aligned fixture, and the entire structure is fired at 1600°C, in a reducing atmosphere, to form a monolithic sintered body. The cofired laminated refractory ceramic technology is a complex process requiring careful control throughout.

After the laminate has been sintered, it is ready for the finishing operations of lead/pin attachment and metallization plating. Nickel is plated over the tungsten in preparation for lead/pin brazing. The lead/pin material is either Kovar (a Fe-Ni-Co alloy) or Alloy-42, and the brazing material is a Ag-Cu eutectic alloy. After lead/pin brazing, all exposed metal surfaces are electroplated or electroless plated (usually gold over nickel) for bondability and environmental protection. Multilayer ceramic packages can be made in lateral dimensions of up to 150 by 150 mm, to a tolerance of ± 0.5 percent, and with more than 30 tape layers in the most advanced processes. A typical single-chip package could contain up to seven tape layers and four screened dielectric layers. The thickness of the taped layer, for tape with tungsten-filled vias, ranges from 0.008 to 0.025 in (0.20 to 0.64 mm). Screened dielectric layers are typically 0.001 to 0.003 in (0.025 to 0.076 mm) thick.

The cofired laminated ceramic package technology is very effective for constructing complex packages with signal, ground, power, bonding, and sealing layers. Electrical characteristics such as line capacitance, propagation delay, impedance, and inductance can be customized for a particular application by design layout and specification of layer thicknesses. Design guidelines[12] are available from package vendors, and designers are encouraged to get the package vendor involved early in the design stage.

This technology, however, has three technical areas of weakness: hard-to-control tolerances caused by high shrinkage in processing, a high dielectric constant of 9.5, and a modest thermal conductivity of $Al_2O_3$. The tolerance problem makes it difficult to use edges as accurate references, and the high dielectric constant affects signal-line capacitive loading. The use of beryllia (BeO), AlN, or SiC, instead of the 90 to 92 percent $Al_2O_3$, will result in a greatly superior thermal performance and a significantly lower dielectric constant. Properties of advanced ceramics are compared in Table 7.3 with those of $Al_2O_3$ and silicon.

A typical DIP construction is illustrated in Fig. 7.29 and consists of three cofired laminated ceramic layers, with a chip cavity formed by the middle layer and a wire-bond ledge formed by the top layer. There are two buried layers and one top-layer metallization in the construction. The bottom buried layer provides the metallization for the chip cavity base, while the top buried layer provides the signal fanout path and bond pad from the wire-bond ledge to the external pins. The different levels can be interconnected by vias, as shown in Fig. 7.30. Top-layer metallization provides the seal ring for hermetic sealing. The seal ring may be tied to a ground plane through a via which may be located near the notch, as illustrated in Fig. 7.29. The same construction applies to a wide variety of package configurations (Fig. 7.31). Packages today come with brazed leads/pins for TH or SM, and leadless perimeter or array pads for SM. The package is delivered to the IC assembly

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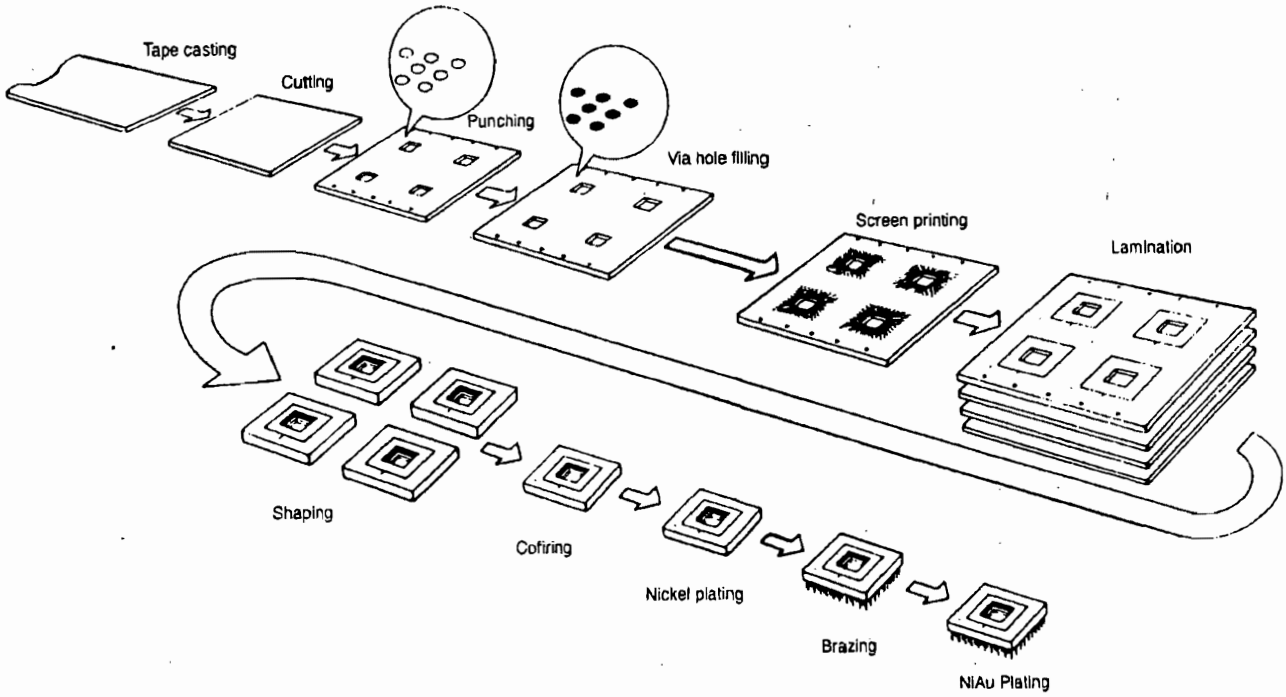


**FIGURE 7.28** Process flow chart of laminated ceramic package technology. *(After Kyocera[12])*

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**TABLE 7.3 Performance of Advanced Ceramics**

| | 98% $Al_2O_3$ | AlN | BN | BeO | SiC | Si |
|---|---|---|---|---|---|---|
| Thermal conductivity | | | | | | |
| Rank* | 1 | 3 | 2 | 3 | 2 | – |
| Value, W/m · °C | 21 | 170–200 | 60 | 250 | 70 | – |
| Coefficient of thermal expansion | | | | | | |
| Rank | 1 | 3 | 1 | 1 | 3 | – |
| Value, $10^{-6}$/°C | 7.1 | 4.1 | 0.0 (75–500°C) | 8.0 | 3.8 | 4.0 |
| Dielectric constant | | | | | | |
| Rank | 1 | 2 | 3 | 2 | 1 | – |
| Value at 10 MHz | 10 | 8.8 | 4.0 | 7.0 | 40 | – |
| Availability, rank | 3 | (2)† | 2 | 2 | (1) | – |
| Metallizing, rank | 3 | (2) | 1 | 2 | (2) | – |
| Cost | | | | | | |
| Rank | 3 | (2) | 2 | 1 | (2) | – |
| Value, $/in$^2$ (approx.) | 0.50 | 2 | 2–3 | 3.5–4 | 2 | – |
| Figure of merit, sum of rankings | 12 | 14 | 11 | 11 | 11 | – |

*Rank order: best = 3.
†Values in parentheses are predicted to improve over time.
*Source:* Data from the Carborundum Co.

manufacturing line with leads/pins, cavity, and bond sites finish-plated to customer specification, and ready for all subsequent level 1 and 2 assembly steps.

An assembly sequence flowchart for cofired laminated ceramic IC packages, with wire bond interconnection, is shown in Fig. 7.32. Chip bonding is done with either an AuSi eutectic, AuSn eutectic or polyimide system, to achieve a high yield and highly reliable mechanical and electrical connection. AuSi and AuSn preforms vary from 99.99 percent pure gold, with dopants to provide a reliable electrical back contact, to alloys of a variety of constituents, such as 80Au/20Sn for lower eutectic temperature bonding. Polymer die attachment in hermetic packages have also been used for many years. Filled and unfilled polyimides were found to withstand the hermetic assembly processing temperatures. Electrical interconnections are generally done using thermosonic ball-wedge gold wire bonding with wire diameters typically at 0.001 in (0.025 mm). Wire spans are usually limited to 0.160 in (4.0 mm) to meet shock, vibration, and acceleration requirements. Excessively long wire spans are avoided by going to a two-tiered, or in some cases three-tiered, wire bond construction, as shown in Fig. 7.33. Final hermetic sealing is done with an 80Au/20Sn braze, in a dry nitrogen ambient, either in a belt furnace with a temperature profile peaking at about 350°C or in a controlled-ambient glove box containing a parallel-gap seam sealer. The seam seal brazing operation confines the heat locally to the seal ring area,

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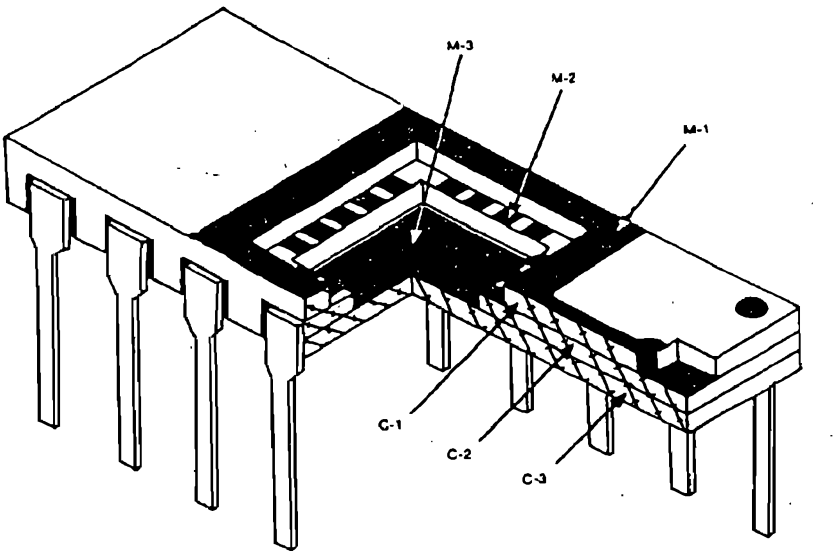


**FIGURE 7.29** Isometric sectional view of cofired laminated ceramic technology in DIP configuration.

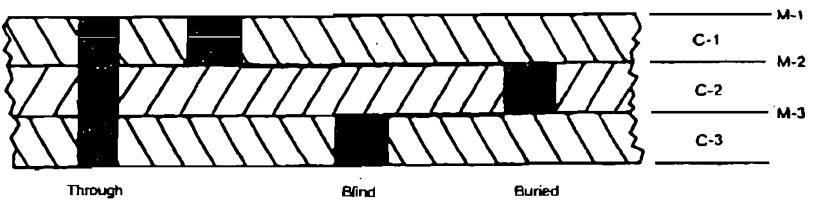


**FIGURE 7.30** Cross section illustrating blind, buried, and through-hole vias in structure of Fig. 7.29.

and thus the package and IC are not significantly heated by the operation. The environment in the sealed package is predominantly nitrogen and the moisture content is typically at or below 1000 ppm $H_2O$ by volume, which meets the military standard requirement for high-reliability applications.

Back-end processes are similar to those for pressed ceramic—that is, leak test, lead trim or lead trim and form,[9] and sometimes lead finish for SM packages. As mentioned, these packages usually come from the supplier with the external leads finished for level 2 assembly to the PWB. The most popular lead finishes available from package vendors range from electroplated gold for soldering and socketing to tin plating for soldering applications only. In between, there are several other combinations involving proprietary alloys of Au-Pd-Ni, Au-Ni, and electroless gold and nickel. Some of these finishes are not compatible with one or more of the assembly processes and may degrade solderability to

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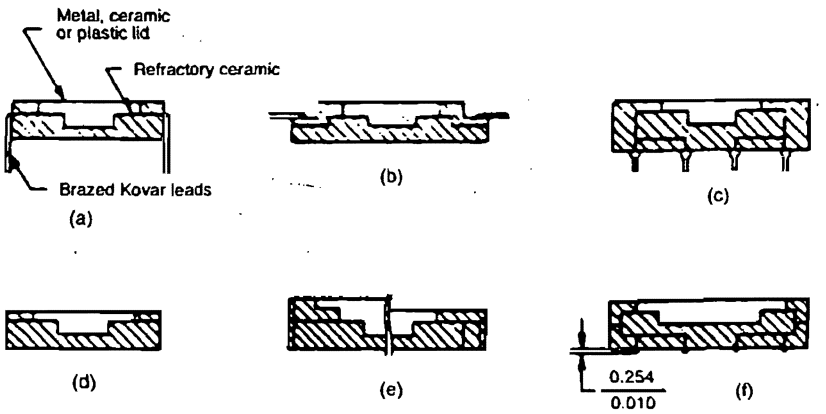


**FIGURE 7.31** Cross-sectional sketches of several package types. (*a*) Side brazed, (*b*) top brazed, (*c*) pin grid array, (*d*) leadless with edge metallization, (*e*) leadless with via holes, (*f*) leadless array package with stand-offs. *(After Kyocera[12])*

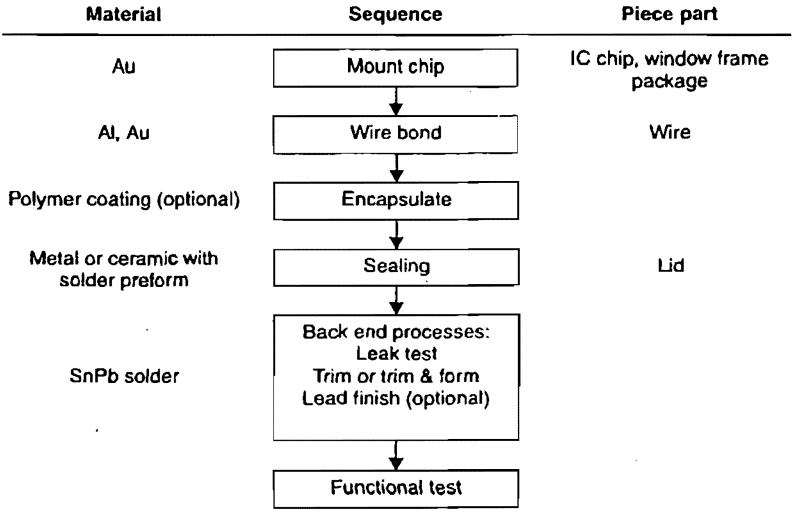


**FIGURE 7.32** IC assembly sequence for cofired laminated ceramic packages.

the point where the SM solder reflow quality may be jeopardized. Leads with thick gold or alloys with significant amounts of gold will cause brittle solder joints that cannot be tolerated in SM. Fine-pitch leaded ceramic chip carriers (LDCCs) may require a solder dip coating to achieve high yields and reliability.

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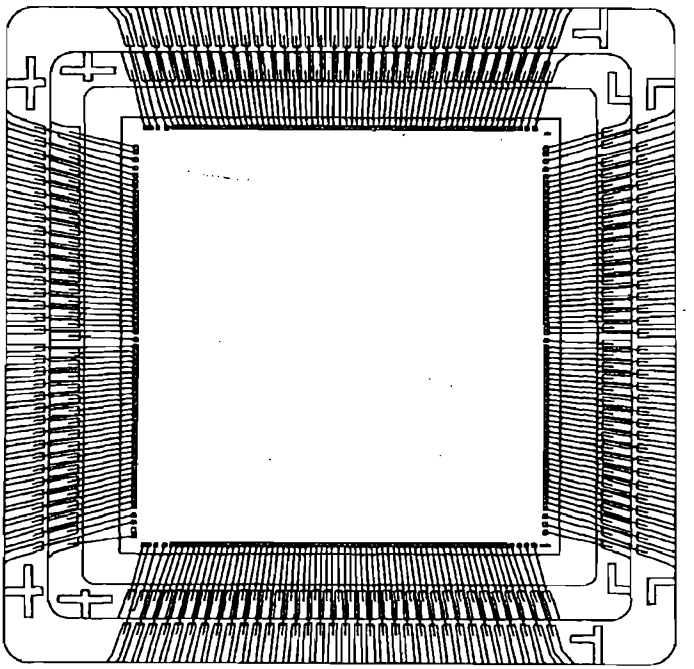

**FIGURE 7.33** Tiered wire bond configuration.

*7.2.3.2 Low-Temperature Cofired Ceramic Technology.* MCP and MCM packages, with functional substrates, are gaining popularity for RF applications. The most common use of the low-temperature cofired ceramic (LTCC) technology is to provide embedded inductors, capacitors, and resistors for functional substrates. The manufacturing processes of the LTCC substrate are exactly the same as those of high-temperature cofired ceramics, except the firing for the LTCC substrate can range from 850 to 1000°C. Most of the Japanese manufacturers use their own proprietary material and green tape for LTCC manufacturing. Several other manufacturers in the U.S.A. and Europe use green tapes provided by DuPont. The most common metallizations in use for vias and internal conductors are Cu and Ag. For the external conductors, Cu, Pt/Ag, or Pd/Ag can be used. There are several technical issues and challenges (such as cost, shrinkage factors, quality, and accuracy of the embedded component) that need to be improved before LTCC can become mainstream material for wireless applications.

## 7.2.4 Laminated Plastic Technology

The laminated plastic packaging technology is a spin-off of the traditional PWB technology where bare chips are mounted directly to the substrate in a technique known as *chip on board* (COB). Early vintage laminated plastic packages used FR-4 epoxy substrates,

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which exhibited high contamination levels due to the flame-retardant fillers. FR-4 epoxy substrates also suffered from a low glass-transition temperature (140°C), making them incompatible with many standard IC package assembly processes. Substrate materials, such as high-temperature epoxies, polyimides, and triazines, are being used today to overcome these deficiencies. These materials exhibit glass-transition temperatures in the range of 180 to 240°C, thus overcoming a major deficiency of the FR-4 material. In addition, these materials also have a much lower level of contamination than the FR-4 boards. A comparison of properties of various organic substrate materials is shown in Table 7.4.

**TABLE 7.4 Typical PBGA Substrate Material Properties**

| Laminate Material | $T_g$ (°C) | X/Y CTE ($10^{-6}$/°C) | Water Absorption (%) | $D_k$ | $D_f$ | Relative Cost |
|---|---|---|---|---|---|---|
| Standard FR-4 epoxy | 130 | 14–20 | 0.14 | 4.2 | 0.020 | 1.0 |
| High-temperature epoxy | 175 | 12–14 | 0.13 | 4.2 | 0.018 | 1.15 |
| Epoxy "Thermount" | 170 | 7–10 | | 3.8 | 0.020 | 2.3 |
| BT | 180 | 10–14 | 0.20 | 4.1 | 0.012 | 1.4 |
| Polyimide | 220 | 9–11 | 0.43 | 4.1 | 0.011 | 4.0 |
| Cyanate ester | 250 | 11–13 | 0.70 | 3.8 | 0.006 | 4.5 |

Notes:
1. Cost values are for materials only and do not include costs associated with processing.
2. Thermount, a nonwoven aramid laminate, is made by DuPont.
3. $D_k$ = dielectric constant.
4. $D_f$ = dissipation factor.

The substrate construction may contain either single-sided, double-sided, or multilayer circuitry, depending on the application needs, and can be provided with or without a cavity to house the chip. The exposed copper metallization is generally plated with nickel and gold to prevent oxidation and provide wire bondable pads. The most popular package types using this technology are the plastic pin grid array (PPGA) for TH mounting and the plastic ball grid array (PBGA) for SM.

The PPGA illustrated in Fig. 7.34 is a nonhermetic prefabricated package that houses the IC chip, providing electrical interconnection to the motherboard and protection from hostile environments. The package consists of a square plastic PWB body with round pins press-fitted and solder reflowed to the underside. The pins can be configured in any desired footprint as long as the pin field is in a straight or staggered array of 0.100 in (2.54 mm) pitch and is restricted to the outside of the die attach and wire-bond pad areas. The PPGA configuration results in the highest density of pins per package area and highest pin count of any TH-type package. PPGAs come in various forms (Fig. 7.35): chip down facing the motherboard or chip up mounted to the top of the package, double-sided or multilayer construction, and with or without a chip cavity. In addition, thermally enhanced PPGAs may also contain plated THs, "thermal vias," under the chip or a copper slug to spread the heat dissipated by the chip.

The PPGA package is constructed[13] by first fabricating the substrate from a rigid double-sided or multilayer PWB by either the additive, semi-additive, or subtractive process, using copper conductors. The substrate contains plated-through holes and, depending on design complexity, may also have buried and semi-buried vias for electrical interconnection.

Pins are made of phosphor bronze,[13] typically 0.018 in (0.46 mm) in diameter, instead of the more expensive Kovar or Alloy-42 used with ceramic packages. The solder-plated

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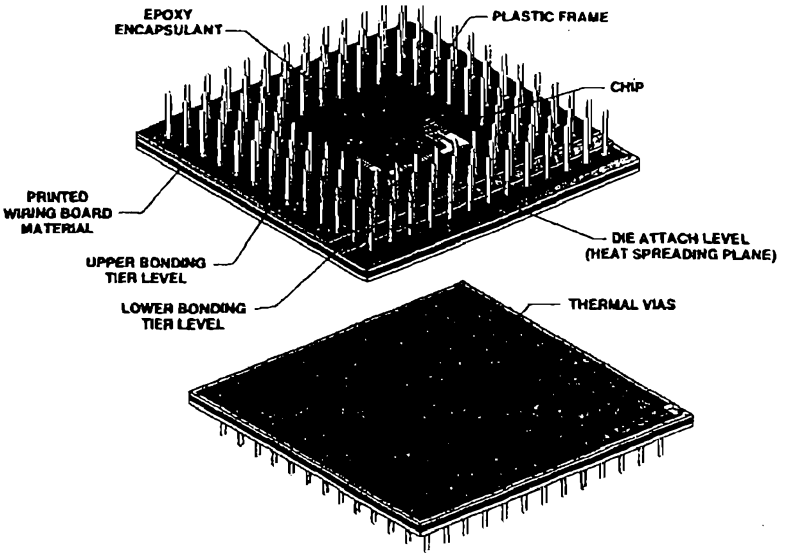


**FIGURE 7.34** Multilayer PPGA with chip cavity facing down. *(After Cohn et al.[13] © 1990, IEPS)*

(60Sn/40Pb or 90Pb/10Sn) pin is inserted through a gold- or solder-plated through hole in the substrate, and the connection is made by a press fit and solder reflow. A star or knurl is incorporated into the shank of the pin to facilitate a more reliable interconnection.

Solder reflow is accomplished by either dipping the entire length of the pin into a solder bath or laser spot heating the base of the pin. During solder dipping, the solder wicks up into the interface between the plated hole and the shank of the pin and, at the same time, forms a fillet at the base of the pin. This provides for a strong, reliable contact but results in a variable solder thickness along the length of the pin, which may affect solderability when tested per MIL-STD-883.

Another solder reflow process uses a laser beam to spot heat the base of individual pins at a rate of approximately 25 pins per second, causing the solder in the hole-to-pin interface to reflow. Sufficient solder must be available at the hole-to-pin interface so that, when reflowed, will produce a strong interconnection. Since laser reflow heating affects only the base of the pin, the original solder-plated thickness along the length of the pin remains unchanged.

The chip is assembled to the PPGA using most of the same assembly processes and techniques used for the plastic molded technology. The assembly flowchart is shown in Fig. 7.36. The chip is first attached using one of the polymer adhesive systems, such as silver-filled epoxies or polyimides, then wire bonded by either the thermosonic gold ball-wedge or the ultrasonic aluminum wedge-wedge process. The chip is then polymer coated for environmental protection using a glob-top liquid epoxy, flow-coated silicone gel, or RTV rubber. A resin dam is desirable, when encapsulating a chip that is not in a cavity, to confine the materials to the IC and wire-bond areas. A metal or nonmetal lid, attached with a polymer adhesive, is optional and is provided for a chip-up configuration, mainly for physical protection when gels or RTV rubber systems are used.

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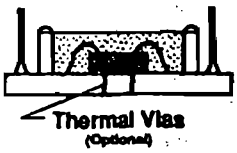
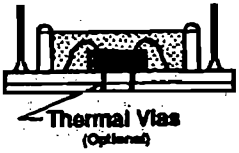
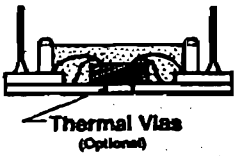


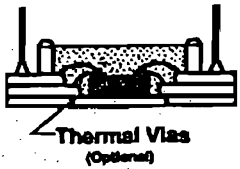

Double Sided,
Chip Down, W/O Cavity




4 Metallization Layers
Chip Down W/O Cavity

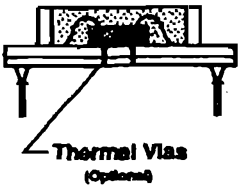



4 Metallization Layers
Chip Down, W/Cavity

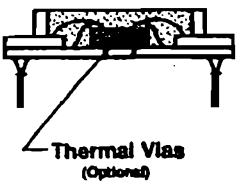



6 Metallization Layers
Chip Down, W/Cavity

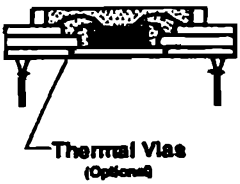
Double Sided
Chip Up, W/O Cavity




4 Metallization Layers
Chip Up, W/O Cavity




4 Metallization Layers
Chip Up, W/Cavity




6 Metallization Layers
Chip Up, W/Cavity

FIGURE 7.35 PPGA package configurations. *(After Cohn et al.[13] © 1990, IEPS)*

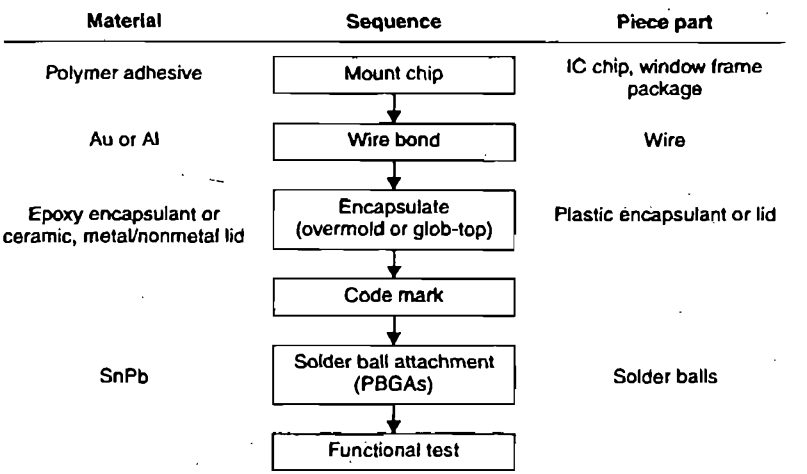



**FIGURE 7.36** IC assembly sequence for laminated plastic technology packages (PPGAs and PBGAs).

The PPGA comes in either a low-cost or an enhanced, high-performance configuration, depending on the application and customer's design objective. The low-cost version, shown in Figure 7.37, consists of a conventional 0.060-in (1.5-mm) thick copper-clad laminate processed as a single- or double-sided substrate with no cavity. Pins are press fitted and solder reflowed. The chip is encapsulated with either a glob-top liquid epoxy or covered with a silicone gel or RTV and lidded. This low-cost design, of single-layer bonding, is limited to approximately 240 I/Os. The limitations are due to a combination of an inability to fan out a greater number of bonding pads in the central "no-pin" area and the constraints of minimum pad pitch design rules. Enlarging the central "no-pin" area to accommodate an expanded bond-pad fanout would result in a larger PPGA size for the given pin count and thus a costlier package. The 240-I/O PPGA limit, for single-layer bonding, is based on a 1.77-in (45.0-mm) sq. substrate with a 0.007-in (0.18-mm) wire bond pad pitch and a pad limited chip size of 0.35 μm features.

A performance-driven device[13] will require a multilayer substrate with power and ground planes and multiple bonding tiers to yield the appropriate interconnection density within the allowable wire-bond design rules. Liquid epoxy or a lid is used to encapsulate the chip. Pins may be inserted to provide either a cavity-up or a cavity-down configuration. A typical cross section through the chip cavity of such a laminated PPGA, showing the multilayer, two-tier bond pads and thermal vias, is illustrated in Fig. 7.38. The thermal characteristics of a cavity-down 223 PPGA, having thermal vias under the chip and heat spreading power and ground planes, are shown in Fig. 7.39. For IC chips dissipating approximately ≥3 W, and depending on the environmental conditions and the maximum $T_j$ allowed, it may be necessary to mount the chip directly to a heat spreading copper slug of a cavity down package configuration as shown in Fig. 7.40.

The low dielectric constant of PPGA substrate materials (in the range of 4 to 5) and the ability to provide thermal vias under the chip, or a heat spreading copper slug, result in equivalent or better electrical and thermal performance as compared to cofired laminated ceramic CPGAs using $Al_2O_3$.

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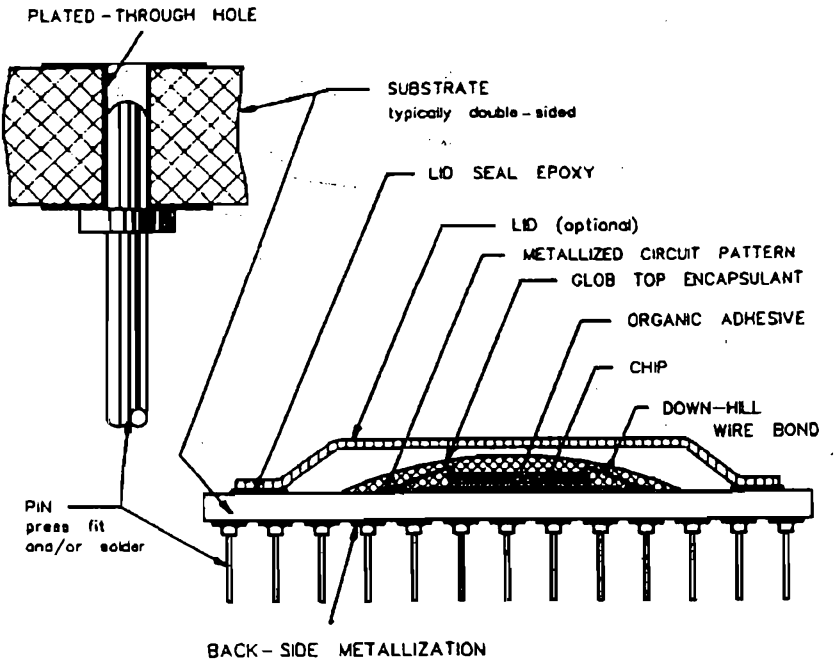


**FIGURE 7.37** Cross section of low-cost PPGA in laminated plastic technology. Substrate is either single- or double-sided PWB with no cavity for IC. Chip is environmentally protected by glob-top epoxy encapsulant. Metal or plastic lid is optional for physical protection.

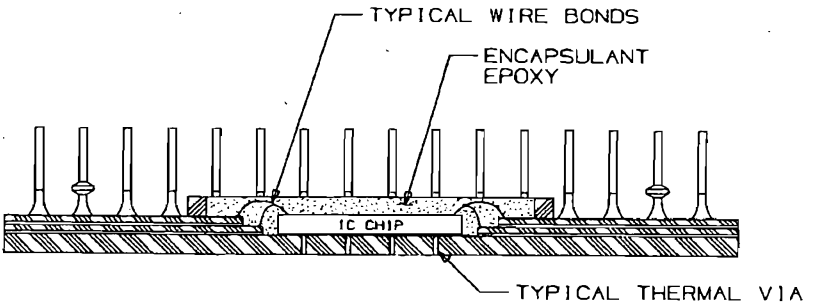


**FIGURE 7.38** Cross section of a multilayer PPGA with chip cavity facing down.

Another IC package that utilizes the laminated plastic technology is the plastic ball grid array (PBGA) package. The PBGA (Fig. 7.41) leverages on the PPGA technology, but replaces the pins with solder balls for surface mounting (SM). PBGAs are described in greater detail in Section 7.3.2.

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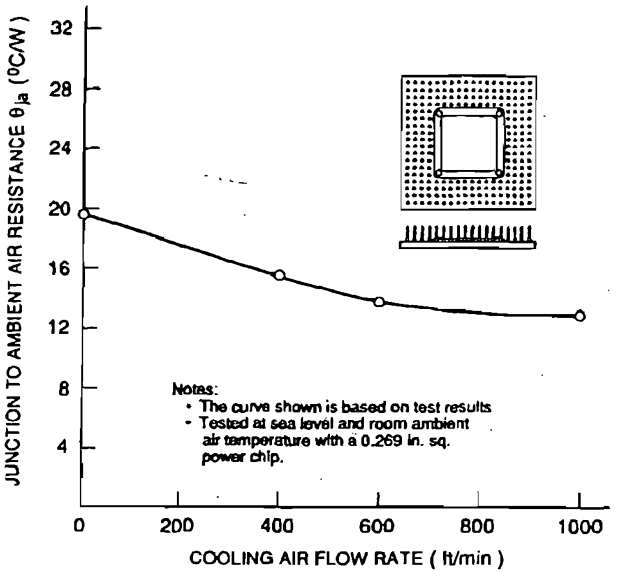


**FIGURE 7.39** Thermal characteristics of a 223-I/O PPGA with cavity facing down and thermal vias under the chip.

## 7.3 ADVANCED PACKAGE TECHNOLOGIES

### 7.3.1 Ceramic Ball Grid Array Packages

With the advent of high-density, high-pin-count, and high-performance SM package requirements, the ceramic ball grid array (CBGA) was developed to meet related demands. The CBGA is constructed in a similar fashion as other laminated ceramic packages (Fig. 7.31) but, instead of perimeter leads and area array pins, the CBGA contains area array pads for solder ball attachment. The substrate consists of a single or several cofired laminated ceramic layers, with molybdenum metallization, and with vias interconnecting the circuitry on the top side to the solder pads on the bottom. The IC chip is interconnected to the alumina substrate by wire bonding or flips chip techniques, as discussed in Secs. 7.7.1.2 and 7.7.1.4. The substrate is lidded or capped to protect the chip, and solder interconnects are attached to the underside to complete the assembly.

The CBGA-to-board interconnects[1] consist of high-temperature 90Pb/10Sn solder balls, which are attached to the substrate with eutectic 63Sn/37Pb solder. The solder balls are 0.035 in (0.89 mm) in diameter, for grid arrays on 0.050-in (1.27-mm) pitch, and 0.025 in (0.64 mm) in diameter for a 0.040-in (1.0-mm) pitch.

To overcome the thermally induced fatigue strain on the solder balls, caused by the CTE mismatch between the alumina substrate and the glass-epoxy PWB, the solder balls

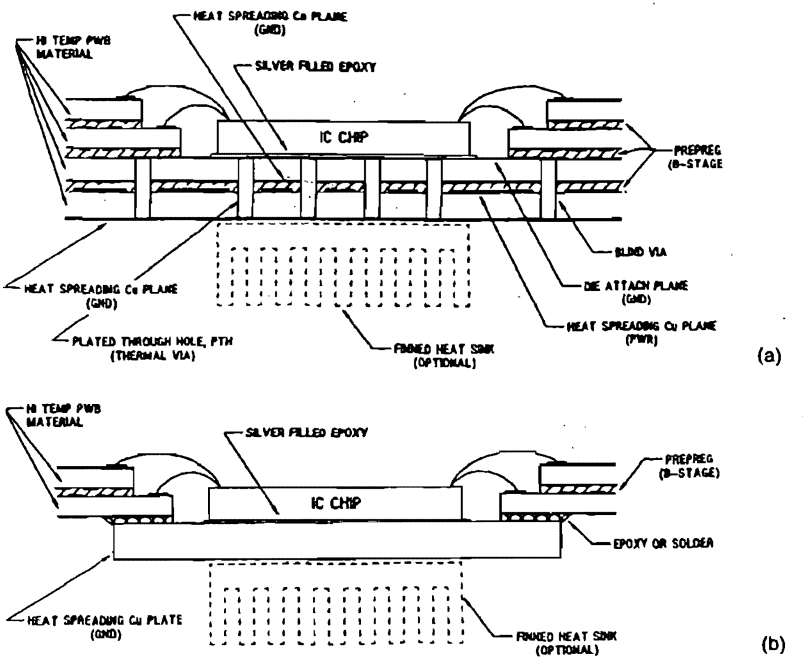


**FIGURE 7.40** (*a*) PPGA package thermal enhancements using heat spreading Cu planes and thermal vias and (*b*) PPGA package thermal enhancements using a heat spreading Cu plate. *(After Cohn et al.*[13] *© 1990, IEPS)*

are replaced with more compliant solder columns; thus, the CBGA becomes a CCGA. The solder columns,[1] which are 0.020 in (0.50 mm) in diameter and 0.050 or 0.087 in (1.27 or 2.2 mm) high, can be either directly attached to the underside of the alumina substrate, or a 63Sn/37Pb solder can be used as an interface for attachment. The different types of solder interconnects are shown in Fig. 7.42.

The CBGA and CCGA packages offer high reliability and high performance, with pin counts exceeding 1000 and area array interconnect densities as small as 0.032-in (0.8-mm) pitch.

### 7.3.2 Plastic Ball Grid Array (PBGA) Packages

Plastic ball grid arrays (PBGAs), Fig. 7.4.1, were first introduced by Motorola in 1989 for low-I/O devices and were then called *over molded pad array carriers* (OMPACs).[2] The PBGA has since emerged as the SM package of choice, because it offers many attractive features such as:

- High I/O to package area ratio
- Multilayer substrate capability

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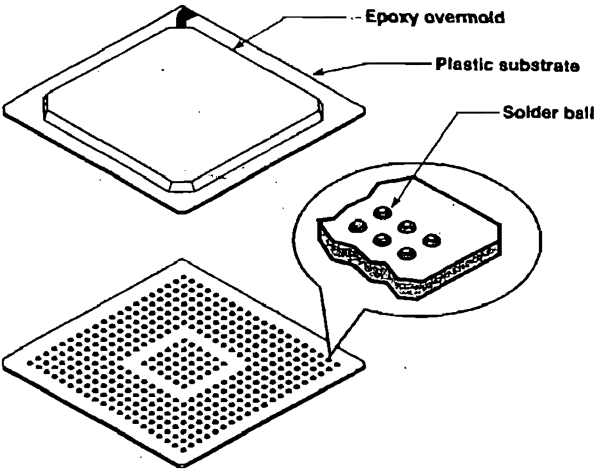


**FIGURE 7.41** Plastic ball grid array (PBGA) package (overmolded type).

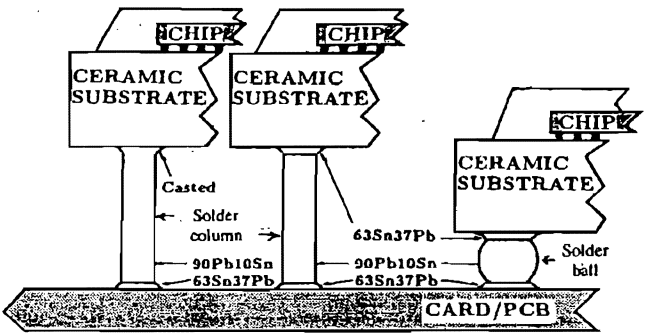


**FIGURE 7.42** IBM's ceramic ball grid array (CBGA) showing different types of solder interconnects and attachments. *(After Lau[1])*

- Improved electrical/thermal performance
- Increased interconnect density
- Ball coplanarity less critical during SM, ≈0.006 in (0.15 mm) to 0.008 in (0.20 mm)
- Self-centering during SM solder reflow
- Elimination of fine pitch solder paste printing
- Pad-to-pad shorting diminished
- Low profile
- Expected solder joint defect level < 5 ppmj

A PBGA package consists of a chip mounted and interconnected to a double-sided or multilayer PWB substrate. Vias interconnect the top surface signal traces to the respective solder pads under the substrate. After chip attachment and wire bonding, the assembly is overmolded using a transfer or injection molding process. Another encapsulation method is to "glob top" the chip and its bond wires with a liquid-dispensed epoxy, which is confined within a resin dam or a chip cavity. Attaching solder balls to the underside of the package then completes the assembly.

The PBGA substrate provides structural support for the chip overmold and solder balls. It also facilitates electrical interconnection between the chip and motherboard and helps dissipate the power generated by the chip. Some of the issues encountered with substrates are electrical interference to chip's functionality (electrical noise, current leakage, high trace resistance), affinity for excessive water absorption that may lead to popcorning, warpage affecting coplanarity, and CTE mismatch that may affect solder joint reliability. Proper design and material selection can minimize these issues.

The PBGA substrates are usually fabricated by a PWB vendor in singulated or strip (multisite) form, according to the customer's design specifications, and then shipped to the semiconductor manufacturer for assembly. The substrates may be selected from standard open-tooled artwork configurations, available from vendor stock, or they may be custom designed to fit special applications. General-purpose substrate designs help reduce assembly turnaround time and inventory logistics problems. In addition, open-tool designs eliminate tooling charges and take advantage of possible volume discounts.

The most commonly used substrate material in the industry today is bismaleimide triazine (BT), although other materials have been used to a lesser extent. Table 7.4 shows the characteristics of some of these materials. Selection of the optimum substrate material for PBGAs depends on the following:

- Low dielectric constant ($D_k \leq 4$)
- Low dissipation factor over a wide frequency band ($D_f \leq 0.01$)
- High glass transition temperature ($T_g \geq 180°C$)
- Low coefficient of thermal expansion (CTE)
- Low z-axis expansion
- Low moisture absorption
- Dimensional stability
- Standard fabrication processes
- Compatibility with BGA assembly processes
- Low cost

The substrate can be fabricated by the subtractive process, using either panel or pattern plating, or the additive process, which is used for high-density applications. A typical construction of double-sided and multilayer substrates is shown in Fig. 7.43.

The industry trend for overmolded-type PBGA substrates is to standardize the thicknesses according to the substrate size and number of metallization layers as follows:

| BGA Substrate Size (mm) | No. of Metallization Layers | Substrate Thickness |
|---|---|---|
| ≤27 × 27 | 2 | 0.36 mm |
| ≤27 × 27 to 35 × 35 | 2 | 0.56 mm |
| ≤35 × 35 | 4 | 0.56 mm |
| ≤17 × 17 | 2 | 0.25 mm (for low-profile EMBGA pkgs.) |

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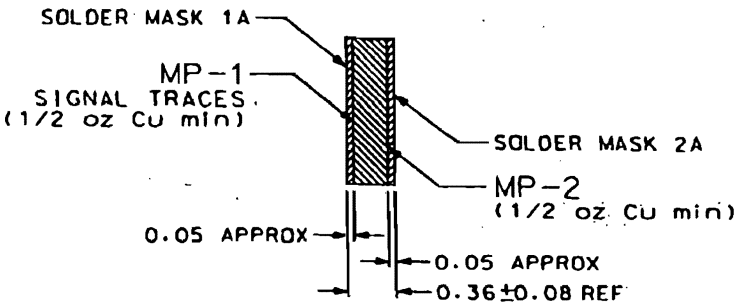
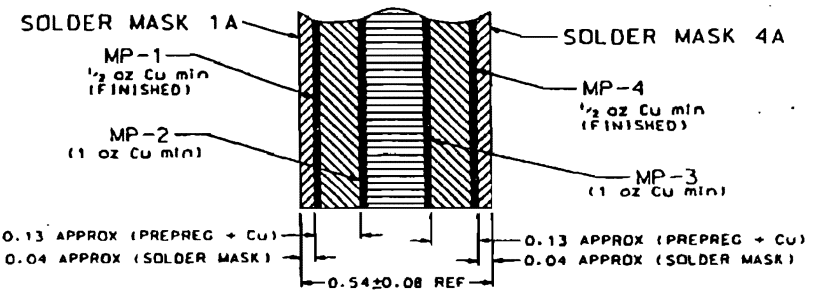



**Two Metallization Layers**




**Four Metallization Layers**

**FIGURE 7.43** Cross section through typical double-sided and multilayer PBGA substrates.

Substrates larger than 35 × 35 mm may require thicker substrates to minimize solder ball coplanarity issues.

The solder pad, at the underside of the substrate, is defined by either the opening in the solder mask (SMD) or by the Cu pad itself (NSMD), as illustrated in Fig. 7.44. The characteristics of SMD and NSMD pads are:

- Solder Mask Defined Pads (SMD)

  Good adhesion strength

  Better performance during rework

  Better heat spreading to the PWB due to larger Cu pads

  Slightly higher surface tension (better self-centering)

  Stress concentrations in solder ball to pad interface

  Solder mask registration ± 0.075 mm

  Solder mask opening variation ± 0.05 mm

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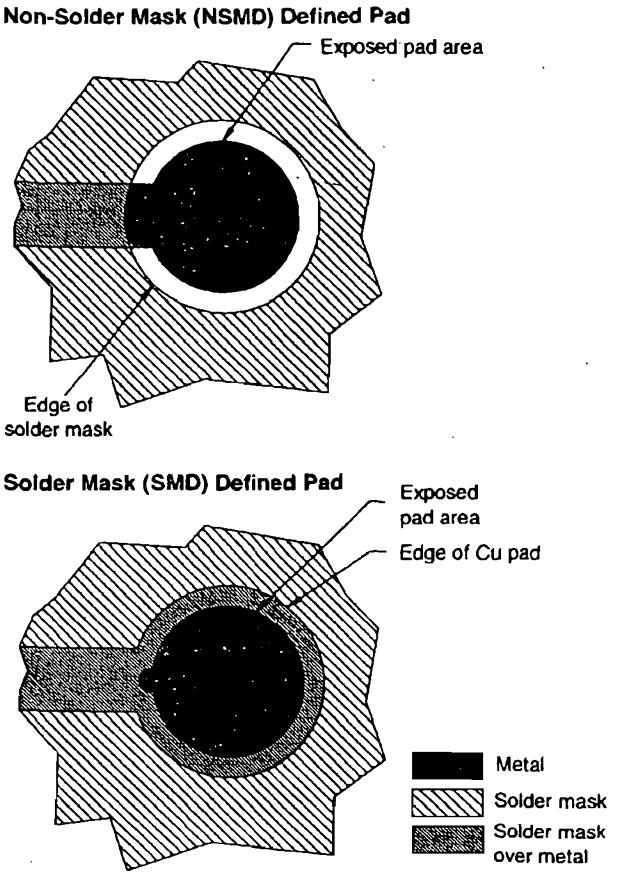


FIGURE 7.44 PBGA solder mask and non-solder mask defined pad designs.

- Non-solder Mask Defined Pads (NSMD)
  - No stress concentrations in solder joint
  - No solder mask CTE mismatch issues
  - Reduced Cu-to-PWB adhesion strength
  - Potentially longer temperature cycling life
  - Cu pad registration ± 0.03 mm

The pads are sized according to the solder ball diameter used and second-level solder joint reliability effects. The pads are arranged in a standard JEDEC area array on a pitch of 0.020, 0.030, 0.040, 0.050, or 0.060 in (0.5, 0.8, 1.0, 1.27 or 1.50 mm). The exposed Cu metallization is either electroplated or electroless plated with nickel and gold to prevent

oxidation and facilitate wire bonding to the bond pads and solder ball attachment to the solder pads.

The composition of the solder balls is either 63Sn/37Pb or 62Sn/36Pb/2Ag. The ball diameter varies from 0.012 to 0.030 in (0.30 to 0.75 mm) and is dependent on the ball pitch and the substrate size used for the given application. Table 7.5 shows the industry's commonly used sizes for solder ball/pad diameter vs. ball pitch.

**TABLE 7.5 Typical PBGA Solder Ball Pitch vs. Ball/Pad Diameters**

| | | SMD | | NSMD |
|---|---|---|---|---|
| Solder Ball Pitch (mm) | Solder Ball Dia.* mm (mils) | Cu Pad Dia. (mm) | Solder Mask Opening Dia. (mm) | Cu Pad Dia. (mm) |
| 0.5 | 0.30 + 0.10/–0.05 (12) | 0.40 | 0.30 ± 0.05 | 0.30 |
| 0.8 | 0.40 + 0.10/–0.05 (16) | 0.45 | 0.32 ± 0.05 | 0.32 |
| | or 0.50 ± 0.10 (20) | 0.60 | 0.45 ± 0.05 | 0.45 |
| 1.0 | 0.50 ± 0.10 (20) | 0.60 | 0.45 ± 0.05 | 0.45 |
| | or 0.63 ± 0.10 (25) | 0.75 | 0.60 ± 0.05 | 0.60 |
| 1.27 | 0.75 ± 0.15 (30) | 0.83 | 0.63 ± 0.05 | 0.63 |
| 1.50 | 0.75 ± 0.15 (30) | 0.83 | 0.63 ± 0.05 | 0.63 |

*Before reflow

PBGAs contain many materials with various coefficients of expansion, thermal conductivities, and elastic behavior. Typical PBGA materials are shown in Table 7.6. Maintaining adequate thermal-mechanical performance, mechanical tolerances (e.g., flatness, coplanarity), moisture sensitivity, and overall device reliability with these materials is a major challenge to the industry.

**TABLE 7.6 Typical PBGA Materials**

| Item | Specification |
|---|---|
| Substrate material | High glass transition temperature, $T_g > 160°C$<br>Epoxy/glass laminate, e.g., bismaleimide triazine (BT) |
| Metallization | 0.5 oz min. Cu on outside layers and 1 oz min. Cu on internal layers |
| Plating | 20 µinch min. gold over 50 µinch min. nickel |
| Die attachment | Silver-filled epoxy |
| Bonding wire | 1.0 mil dia. gold wire |
| Encapsulant | Epoxy overmold or dispensed epoxy |
| Balls | Eutectic solder, e.g., 62Sn/36Pb/2Ag or 63Sn/37Pb |

*Source:* after Cohn et al.,[2] © 1995, IEEE.

The cross section of a typical PBGA having a double-sided substrate with the chip mounted to the top surface, wire bonded, overmolded, and solder balls attached is shown in Fig. 7.45. For enhanced power dissipation, the substrate contains "thermal vias" under the chip and a center array of thermal solder balls that are normally grounded. In a high-performance PBGA configuration, the substrate is multilayered with internal power and ground planes for improved electrical inductance and heat spreading capability (Fig. 7.46). The internal Cu planes are normally 1-oz thick, but better heat spreading and lower junction-to-air thermal resistance (≈10 percent less, depending on substrate size) can be achieved if a 2-oz Cu thickness is used. The substrate for a high power dissipating device (≥4 W) typically contains a chip down cavity with single or double bonding tiers and a heat spreading copper slug to which the chip is directly attached (Fig. 7.47).

Wire bonding is the leading chip interconnection process used today for PBGAs. Flip chip bonding, although not widely used, is expected to become a leading contender in the near future (see Sec. 7.7.1.4).

Each substrate size (27 × 27 mm, 35 × 35 mm, etc.) has a given plastic overmold configuration that does not change with different circuitry or pin count. This enables the package designer to take advantage of existing mold cavities.

Figure 7.36 (p. 7.43) illustrates a typical PBGA assembly sequence, processed in strip form with wire bond interconnection.

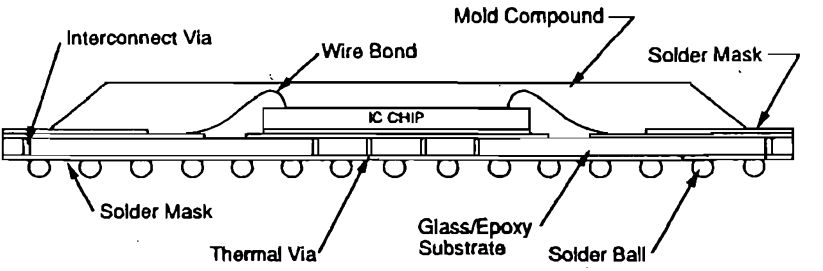


**FIGURE 7.45** Cross section through a PBGA with a double-sided metallization substrate. *(After Cohn et al.,[2] © 1995, IEEE)*

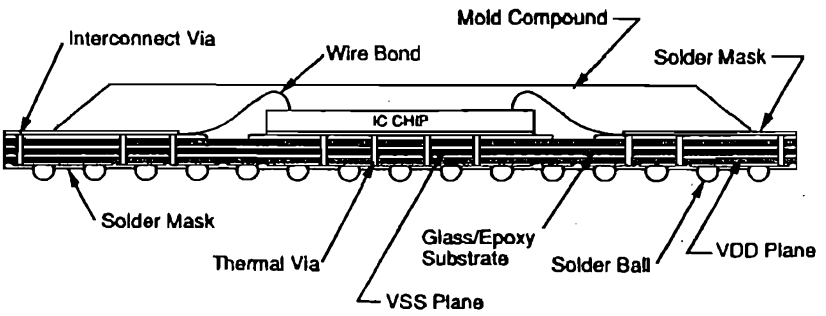


**FIGURE 7.46** Cross section through a PBGA with a multilayer metallization substrate.

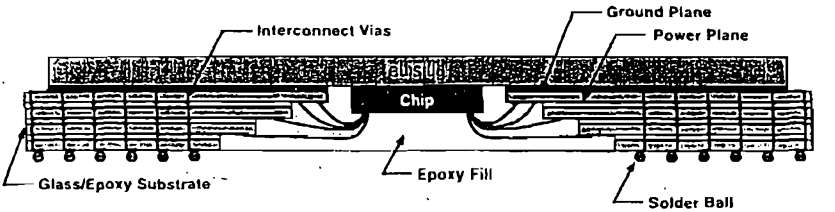


**FIGURE 7.47** Typical cross section through a thermally enhanced PBGA.

The assembly is described as follows:

Mount wafer, saw, and clean. Silver-filled epoxy is transfer printed onto the die attach area, the chip is placed over the epoxy, and the assembly is cured. The chip is thermosonically ball-wedge gold wire bonded and visually inspected. The strip sites are overmolded or encapsulated with a liquid dispensed epoxy resin system and cured. After overmolding, the sites are code marked, and solder balls are attached to the underside of the individual sites. The individual PBGA devices are separated from the strip by routing or punching and inspected, cleaned, electrically tested, burned-in when required, electrically retested, placed in bakeable shipping trays, baked/bagged, and shipped to the customer.

Prior to committing a PBGA device to production, the device is usually qualified by conducting a series of tests according to the customer's requirements or to the semiconductor manufacturer's own standard specifications. Requalification of an already qualified device may be required whenever materials change, different substrate or assembly vendors are used, the chip technology changes, or the design rules have drastically changed. Figure 7.48 illustrates typical test requirements for PBGA device qualification.

The PBGA, being a relatively new package technology, has a number of drawbacks that undoubtedly will be resolved with time and a better understanding of the issues. Some of the concerns expressed within the industry are as follows:

1. *Moisture Sensitivity.* Many of the materials that make up the present PBGA configurations are susceptible to moisture absorption. As a result, the PBGAs, while being stored in a factory environment awaiting assembly to the PWB, are prone to absorb moisture that may cause internal delamination (popcorning) and cracking during solder reflow. Thus, some semiconductor manufacturers ship the PBGAs prebaked and in vacuum-sealed bags to be opened prior to board assembly. Manufacturers continue to improve the material properties and designs of PBGAs, and it is now possible to achieve a JEDEC, Level 3 condition, defined as a floor life of 168 hours in a 30°C/60 percent RH environment before rebaking is required to solder reflow.
2. *Solder Joint Reliability.* The number of solder joints on a circuit board has increased dramatically over the last few years. Thus, it is critical that the effects on solder joint integrity are understood and solutions implemented to improve their reliability. This is particularly important when dealing with PBGAs, which have solder joints far less compliant than leads. Cycle-to-failure tests and finite element modeling have been used to predict the life cycle of PBGA solder joints in a given application. Most of the solder joint failures in PBGAs have been attributed to thermal fatigue induced by temperature cycling and caused by the CTE mismatch between the PBGA structure and its PWB attachment surface. Other failure mechanisms may be creep rupture

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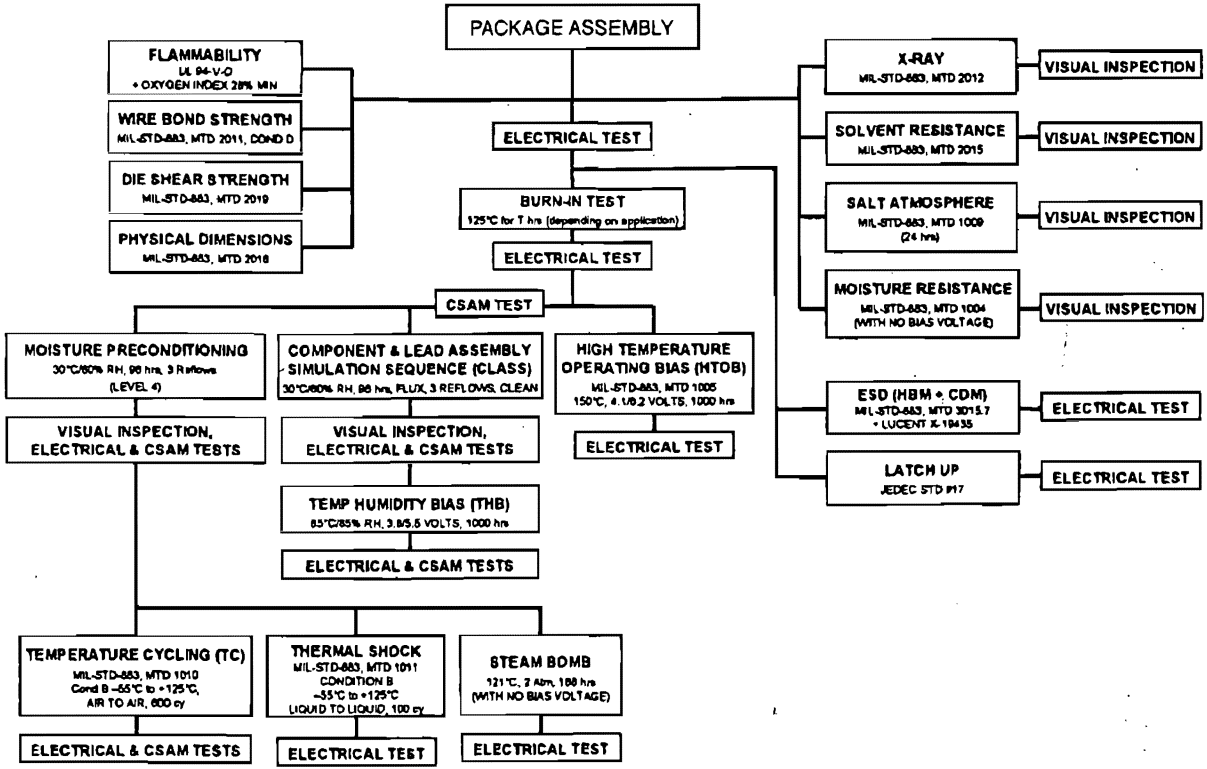


**FIGURE 7.48** Typical PBGA device qualification tests.



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and solder joint/pad interface cracking. Solder joint integrity is affected by factors such as joint location relative to the chip, solder joint configuration (as influenced by the solder ball/pad size), intermetallic structure, substrate thickness, number of temperature cycles and range, stress concentration from the sharp edges of the solder mask defined pads (SMD), etc. The PBGA and its board interconnection are to be designed for reliability at the outset to achieve the required service life for a given application.

3. *Solder Joint Inspection/Repairability.* Other PBGA technology issues of concern to end-users are that inspection of all solder joints requires expensive x-ray equipment, and repairability is complicated.

*7.3.2.1 Tape BGA (TBGA).* A tape BGA is defined as a package having a copper/polyimide flex tape for a substrate. The tape contains one or two metallization layers interconnected by plated-through holes. Tape substrates have been utilized in EMBGAs (see Sec. 7.3.2.3), thermally enhanced cavity type packages, low-I/O flip chip BGAs, etc.

In a cavity-type TBGA[28] (Fig. 7.49*a*), one side of the tape contains the wedge bond pads and the circuitry to fan out to the solder ball pads. The metallization layer on the other side of the tape can be utilized as a ground plane.

Another example of a TBGA package (Fig. 7.49*b*), developed by IBM,[27] utilizes flip chip bonding to a copper/polyimide tape containing two metallization layers. The top circuitry layer fans out the I/Os from the chip to solder ball pads on the bottom layer via plated-through holes. The remaining space between the BGA pads is utilized as a functional ground plane. The circuitry is formed by electroplating Cu onto the polyimide tape, as defined by the resist mask. A stiffener ring is attached to the tape, using an adhesive, to provide rigidity and solder ball coplanarity to the package.

The interconnection between the chip and the tape is accomplished by a modified solder-bumped flip chip process developed by IBM, which consists of a chip with 97Sn/3Pb solder bumps in an area array placed on matching footprints on the tape. Bonding to the tape is achieved by a partial reflow of the solder bumps without flux while applying a slight pressure to the bumps.

An epoxy underfill is applied between the chip and the substrate tape. The underfill provides moisture protection to the chip surface and reduces the thermal stresses induced in the solder joints due to coefficient of expansion mismatches of the bonded materials.

On the BGA side, 0.025-in (0.635-mm) diameter 10Sn/90Pb solder balls on a 0.050-in (1.27-mm) pitch are attached to the pads on the tape using a resistance heating process. At the center of each BGA pad is a 0.008-in (0.200-mm) plated-through hole that is used for electrical interconnection and to anchor the solder ball. To enhance the thermal character-

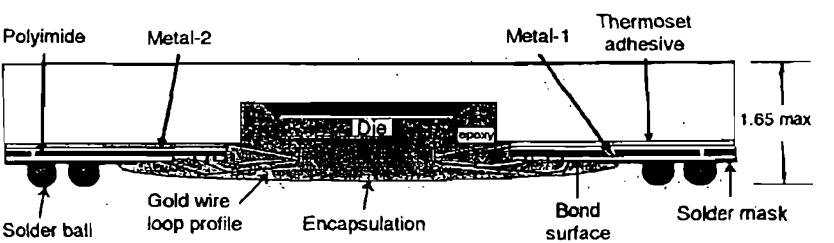


**FIGURE 7.49a** Cross section through a thermally enhanced tape BGA. *(After ASAT[28])*

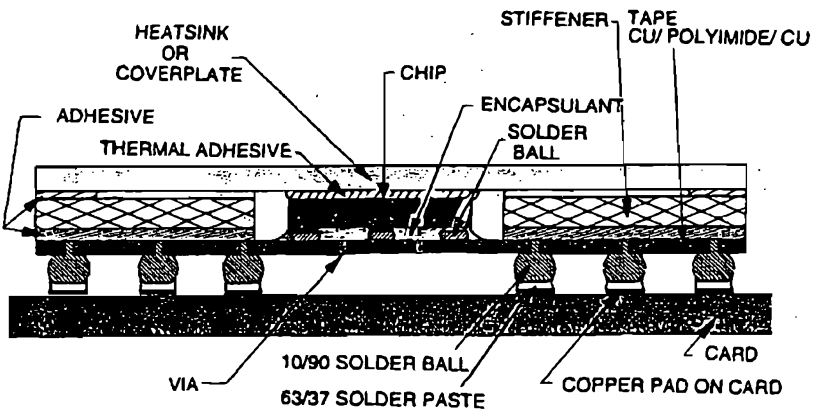


**FIGURE 7.49b** Cross section through a flip chip tape BGA. *(After IBM[27])*

istics of the TBGA, a Cu plate is attached to the stiffener and to the back of the chip to provide heat spreading.

As a result of the relatively short conductor lengths and close proximity of the ground plane, the FC-type TBGA has low signal line inductances as well as low power and ground inductances.

The capability to route higher-density circuitry on polyimide tape is an advantage that tape currently has over laminate substrates. This advantage is slowly eroding because of the advancements in laminate technology, which have resulted in laminate design rules to approach that of tape. In addition, the polyimide tape is more expensive than a laminate substrate of the same size, except at very high volumes. Therefore, at low and moderate volumes, a laminate substrate should be considered if the routing density required for the given design can be achieved in this technology.

*7.3.2.2 Chip Scale Package (CSP).* A new class of IC packages has emerged with dimensions only slightly larger than the chip itself (maximum of 1.2 times the size of the chip). The new technology, called *chip scale packaging* (CSP), comes closest to direct chip attachment but without the responsibilities usually imposed on the board assembler for handling, attachment, wire bonding, and encapsulation of known good die (KGD). Using CSP, the above tasks are shifted back to the semiconductor manufacturer in that the device comes fully tested, burned-in, and ready for SM assembly to the PWB by conventional means, like any other IC package. Several chip scale package configurations were developed to provide a lower-cost, high-I/O, high-density, compact package. One such package was developed by Tessera Inc., called the micro-BGA (μBGA®).[26] It combines a unique chip interconnection with BGA technology that results in a highly miniaturized package (Fig. 7.50). The μBGA® consists of a copper/polyimide flex-tape substrate with an array of pads interconnected to Cu ribbon leads extending from the substrate edge and joined at their tips to a common bus bar. Both the pads and ribbon leads are Ni/Au plated. The ribbon leads are thermosonically bonded to the perimeter pads on the chip and separated from the bus bar at the same time. A silicone elastomer layer between the flex tape and the chip surface cushions any impact to the chip during socketing or board assembly. The compliant layer also reduces any stresses caused by the CTE mismatch between the

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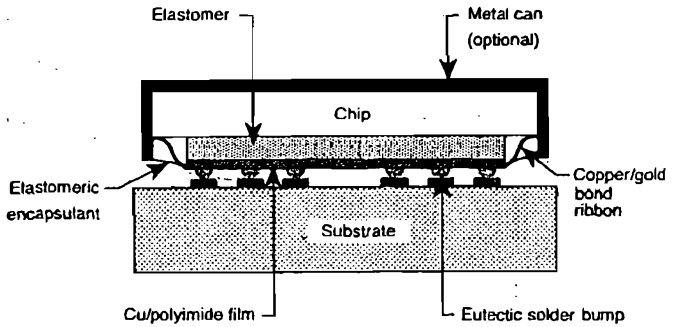


**FIGURE 7.50** Typical cross section through a μBGA®. *(After Tessera[26])*

silicon and the solder ball joints when surface mounted to a PWB. A molding compound encapsulates the ribbon leads and supports them during package handling.

*7.3.2.3 Edge Molded BGA (EMBGA).* The plastic edge molded BGA (EMBGA) (Fig. 7.51), also called fpBGA™ by ASAT and Chip Array® BGA by Amkor, is a conventional PBGA with the overmold extending to the edge of the substrate. The thickness of the overmold, being uniform across the substrate, provides protection to the bond wires—even at the edge. The substrate is designed with the wedge bond pads placed close to the edge and interconnected to the solder ball pads on the BGA side through fan-in circuitry and plated-through holes. A solder mask covers the entire surface of both sides of the substrate, with the exception of clearances to expose the wedge bond pads and solder ball pads. Although most of the plated through holes are located under the chip, qualification tests have shown that this is not a problem.

The EMBGA substrates range in size from 4.0 × 4.0 mm to 17.0 × 17.0 mm, with ball counts from 24 to 256 I/O, in an area array of 0.5, 0.8, or 1.0 mm pitch. The organic substrate is usually made of bismaleimide triazine (BT) or equivalent with two metallization layers, although additional power and ground planes can be incorporated for electrical enhancement. The substrate consists of multiple sites in an array configuration with tie bars connected to common buss bars to facilitate Ni/Au electroplating. Since the tie bars

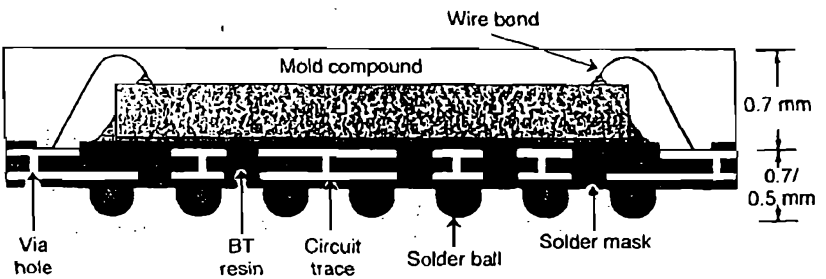


**FIGURE 7.51** Typical cross section through an edge molded BGA. *(After ASAT[28])*

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cannot be cut after substrate fabrication to isolate each site for electrical testing of opens and shorts, the sites are usually checked, prior to applying the solder mask, by automatic optical inspection (AOI) equipment. The defective sites are identified with markings that will prevent placement of a chip on the affected site during assembly.

Assembly follows the same process flow as for conventional PBGAs (Fig. 7.37), with the exception of overmolding and singulating. The overmold covers the entire array of sites instead of individual sites. After ball attachment and code marking, the sites are singulated using a wafer saw that cuts through the overmold and substrate.

The overall thickness of an EMBGA, including solder balls, is 1.37 mm (Fig. 7.51). The demand for thinner packages has forced the assembly vendors to find ways to reduce the overall thickness to 1.2 mm by reducing the thickness of the substrate from 0.36 to 0.25 mm. The EMBGA package has an interconnection density (ratio of substrate area to solder ball count) that comes close to that of the chip scale package (CSP).

*7.3.2.4 Flip Chip BGA (FCBGA).* Combining a BGA package configuration with flip chip bonding results in a most effective high-density interconnection (Fig. 7.52). The solder bumped chip is placed face down onto matching wettable bonding pads on a multilayer BGA substrate, and the assembly is reflowed. The bonding pads on the substrate may initially be bare of any solder or may be solder bumped and coined prior to chip assembly. After flip chip attachment, the chip is underfilled with an epoxy resin formulated to relieve the stresses induced by the thermal mismatch between the chip and the substrate and to prevent moisture from getting to the chip surface. The flip chip can be capped or topped with a liquid epoxy, which is retained within the confines of a resin dam. For low cost, the back of the flip chip is left exposed, but this leaves the edges of the chip susceptible to chipping during handling. Where chip power dissipation is of concern, a Cu stiffener ring, slightly thicker than the chip standoff, is attached to the substrate prior to chip assembly. After chip assembly, an adhesive is applied to the top surface of the stiffener ring, and the back of the chip is covered with a pliable conductive adhesive. A Cu plate is attached to the stiffener ring, while the center of the plate is in contact with the adhesive on the back of the chip. The heat dissipated by the chip is thus conducted through the adhesive to the heat spreading Cu plate. A finned heat sink can be attached to the plate to further lower the case to ambient air thermal resistance. After chip encapsulation, solder balls are attached to the underside of the substrate to complete the FCBGA.

The high-density interconnection emanating from the chip requires equal high-density circuitry on the substrate. To achieve these circuit densities, the substrates have to be fabricated by the more expensive additive or build-up process. Substrate vendors utilizing the build-up process have reported current production capabilities of 30/30 μm lines/spaces

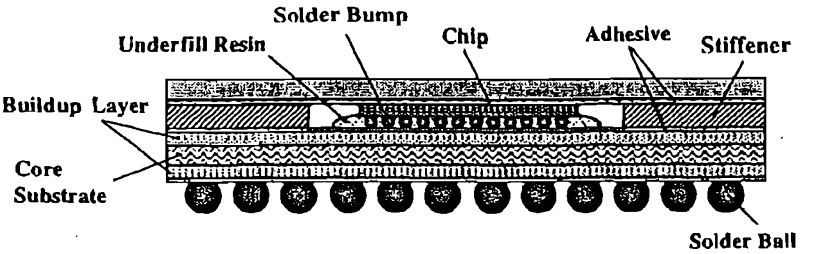


FIGURE 7.52 Typical cross section through a flip chip PBGA.

and 60/110 μm via dia./land dia. The exposed metal surface finishes on the substrate may be electroplated or electroless plated with Ni/Au or coated with an organic surface preservative (OSP).

Although the infrastructure for flip chip bonding is currently not industry wide, it is expected that FC will be a leading interconnection technology for the future, particularly for high I/Os and where high electrical performance is required.

## 7.4 COMPARISON OF TECHNOLOGIES

A comparison based on the attributes and trade-offs of the four contending IC packaging technologies, described in Secs. 7.2 and 7.3, is shown in Table 7.7.

**TABLE 7.7 Package Attributes and Trade-Offs vs. Package Technologies**

| Attributes and Trade-Offs | Molded Plastic | Pressed Ceramic | Laminated Ceramic | Laminated Plastic |
|---|---|---|---|---|
| Hermeticity | No | Yes | Yes | No |
| Power/ground distribution capability | Doable custom design | Not feasible | Standard | Standard |
| High-density routing capability | Custom TAB design | Not feasible | Standard | Standard |
| Power dissipation capabilities | Fair | Fair | Excellent | Excellent |
| Thermal design enhancements | Heat spreaders | New materials | New materials | Thermal vias and heat spreaders |
| Capability for handling bond-pad-limited chips | Yes | Yes | Yes | Yes |
| Automated assembly | Excellent | Feasible | Good | Excellent |
| Max. I/O capability | 375 | 196 | 1000+ | 1000+ |
| Cost rank order (lowest = 1) | 1 | 2 | 3 | 2+ |

Pressed and laminated ceramic technologies have hermetic sealing capability, which provides the best environmental protection for the IC. High-reliability performance is achieved if the sealing operation is done properly—that is, if it provides a leak-tight seal and a cavity free of contaminants, and if moisture is controlled to an acceptable level. Nonhermetic molded and laminated plastic technologies can provide equal reliability performance for most applications.

In determining relative electrical performance, the capacitance between adjacent leads is a property that is influenced by the dielectric constant of the material in direct contact with the leads. Table 7.8 lists the materials and dielectric constants for each package technology. Plastic technologies have the potential for best electrical performance due to their lower dielectric constants. The high dielectric constant inherent in the laminated alumina ceramic technology can be avoided by the use of thin-film metal-polymer multilayer structures as used in MCMs (see Chap. 9). MCM structures make laminated ceramic competi-

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tive with laminated plastic. Electrical performance is further optimized by the use of power and ground planes and high-density routing within the package. Both laminated plastic and ceramic technologies have this as a standard design capability.

**TABLE 7.8 Physical Properties vs. Package Technologies**

| Physical Properties | Molded Plastic | Pressed Ceramic | Laminated Ceramic | Laminated Plastic |
|---|---|---|---|---|
| *Dielectric constant at 1 MHz* | | | | |
| Plastic overmold | 5.0[36] | | | 5.0[36] |
| Ceramic body | | 9.0[34] | 9.0[34] | |
| BT resin lamina | | | | 3.9[31] |
| *Thermal conductivity, W/m K* | | | | |
| Plastic overmold | 0.80[30] | | | 0.80[30] |
| Ceramic body | | 20.9[34] | 20.9[34] | |
| BT resin lamina | | | | 0.26[31] |
| *CTE, ppm/°C* | | | | |
| Chip mount surfaces | | | | |
| Copper LF | 17.2[31] | | | |
| Alloy-42 LF | 8.0[34] | | | |
| Ceramic body | | 6.0–7.7[35] | 6.0–7.7[35] | |
| BT resin lamina | | | | 15.0[32] |
| Plastic overmold | 13.0[30] | | | 13.0[30] |
| IC chip (silicon) | 2.7–3.5[35] | 2.7–3.5[35] | 2.7–3.5[35] | 2.7–3.5[35] |

Thermal performance is influenced by the thermal conductivity of the basic package materials (Table 7.8) and the use of thermal design enhancements (Table 7.7). The thermal conductivity of alumina ceramic materials is an order of magnitude better than that of plastic materials. Materials such as AlN and SiC, with higher thermal conductivities and heat spreading copper-tungsten slugs, have further improved the thermal performance of ceramic packages. Design enhancements in laminated plastic packages such as thermal vias under the chip, center array of thermal solder balls, heat spreading internal planes or copper slugs, and heat spreaders in molded plastic packages have closed the gap and are competing in thermal performance with laminated ceramics.

Mechanical performance is related to internal stresses developed within the package as a result of the mismatches of the coefficients of thermal expansion (CTE) of the different materials used in the package construction. CTEs of the silicon IC and of the substrate material to which the chip is mounted, for each technology, are listed in Table 7.8. The mismatches are displayed in Fig. 7.20. The best match is between silicon ICs and ceramic-type packages. Further complications are encountered in technologies where the chip is not decoupled from other materials, such as molding compounds in molded plastic and glob-top or flow coats in laminated plastic technologies. Chips in the pressed ceramic and cofired laminated ceramic technologies are usually decoupled from other materials; however, their assembly processes, which include high-temperature exposure during chip mounting and hermetic sealing, can present problems, particularly for very large chips, greater than 0.500 in (12.7 mm). Other material properties, such as Young's modulus and Poisson's ratio, also affect the magnitude of stresses in packages where the chips are not decoupled. The finite-element analysis is a useful CAD tool for modeling stress conditions in new package designs before committing them to development and manufacturing stages.

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The cost of packaging is best addressed by using a rank-order system rather than an absolute cost. Many factors and assumptions enter into a cost analysis of packaging, and these are beyond the scope of this chapter. Molded plastic technology packages, such as plastic quad flat packs (QFPs) (which are assembled on lead frames) and plastic ball grid arrays (PBGAs) (which are assembled on single layer, multisite strip substrates) rank low, whereas the multilayer laminated technology packages such as CPGAs or PPGAs, which are singulated and need to be assembled in "boats," rank higher.

The ability of a package to accommodate bond-pad-limited chips is an important factor influencing the cost of the chip. For example, the ability to accommodate bond-pad-limited chips in molded plastic and pressed ceramic packages is sometimes limited by the fabrication process for the lead frame. The lead-frame feature size is dictated by its thickness. The use of thinner lead frames and TAB tape, such as in fine-pitch, high-I/O packages, has extended the capability for the plastic molded technology. The laminated ceramic and plastic technologies solve the bond-pad-limited chip problem for high I/O devices by using tiered wedge bond sites, thus bringing the wire bonds closer to the chip and minimizing the span length. The ability to multilayer and to provide high-density routing has made tiered bonding feasible. A trade-off exists in the cost of packaging bond-pad-limited chips. Cost savings realized by shrinking the chip size are sometimes reduced by the higher packaging cost. Each application must be evaluated thoroughly to determine the bottom-line cost for both chip and package.

Table 7.9 compares most of the attributes discussed in this section by rank order, providing a simple format to evaluate trade-offs between the competing package technologies.

**TABLE 7.9 Attribute Rank Order vs. Package Technologies**

| Physical Properties | Molded Plastic | Pressed Ceramic | Laminated Ceramic | Laminated Plastic |
|---|---|---|---|---|
| Moisture sensitivity | 2* | 1 | 1 | 2 |
| Lead capacitance | 1 | 3 | 2 | 1 |
| Power dissipation | 3 | 2 | 1 | † |
| CTE mismatch, chip-to-chip-mount surface | ‡ | 1 | 1 | 2 |
| Automated assembly capability | 1 | 1 | 2 | ** |
| Capability of accommodating bond-pad-limited chips | 1 | 1 | 1 | 1 |
| Cost | 1 | 2 | 3 | 2+ |

*Rank order: best = 1.
†Rank order depends on lead-frame material used: 1– = Alloy-42; 3 = copper alloy.
‡Rank order depends on thermal design of substrate; 1+ = design with thermal vias and heat-spreading planes., 2+ = design without thermal vias.
**Rank order depends on package type; 1– = PBGAs (overmolded), 2 = PPGAs.

## 7.5 PACKAGE FAMILIES

IC package designs have proliferated over the years into a wide variety of shapes, sizes, number of I/O pins, lead arrangements, and geometries in response to circuit and system-level demands. This proliferation of package types becomes very uneconomical to end

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users. For example, original equipment manufacturers (OEMs) using electrically equivalent components from different suppliers must use several PWB designs if the components are in different package types.

Assembled packages need to be handled economically and with special precautions (e.g., electrostatic protection) through a series of back-end processes that include lead trim and form, code marking, electrical testing, electrical burn-in when required, shipping, and subsequent assembly to the next level of packaging. These activities need major industry support in the development of specialized custom equipment and tooling; for example, magazines, sticks, trays, or tape and reel for handling through the back end, test sockets for production testing, sockets and boards for device burn-in, test handlers and electrical contacts for production testing, and automatic placement and insertion equipment for component board assembly. The industry has been very active in the standardization of IC package outlines, which has resulted in footprint and handling compatibility of components from different vendors and the focusing of the above-listed support activities on fewer package types, thereby optimizing the overall economics of electronic packaging.

Packages with similar traits are being grouped into families by lead arrangement. These standard outlines then control all dimensions, tolerances, and all other information necessary to define, manufacture, and assemble the package. In the U.S.A., the EIA-JEDEC, JC-11 committee is the dominant body developing new package outlines. Over the past several years, JEDEC has been working closely with EIAJ to reduce a further proliferation of outlines and to focus similar outlines from each organization into one worldwide standard outline.

Table 7.10 lists the package families available in each of the package technologies described in Secs. 7.2 and 7.3. They are also broken down by the mounting method to second-level board assembly (TH vs. SM). Package families are typically grouped and defined by lead arrangement such as in-line, perimeter, or area array. Package outlines considered shall be EIA-JEDEC or EIAJ registered or standard outlines. Registration is the first step to having a package outline accepted as an industry standard. To become a standard package, a registered package must be generally used in the industry and then approved by a majority of JEDEC, JC-11 member companies in an official balloting process. A complete listing of all registered and standard outlines is available in EIA Publication 95.[17] Sections 7.5.1 and 7.5.2 review these package families.

### 7.5.1 Through-Hole Mounted Packages

One of the oldest IC package families still in use today is the DIP family, illustrated in Fig. 7.2. A DIP is a through-hole mount package with its leads on a 0.100-in pitch and is generally available in three package technologies: molded plastic, pressed ceramic, and laminated ceramic. DIPs can accommodate devices with as few as 8 and up to 64 I/Os. The family is defined by width, or lead row spacing, ranging from 0.300 in for the narrowest to 0.600 in for the widest. The 0.300-in lead row spacing DIP family was the first to be standardized by JEDEC and is identified as MS-001. Other DIP families that have been standardized are the 0.400-in row spacing MS-010 and the 0.600-in row spacing MS-011. MS-001 covers pin counts ranging from 8 to 28, MS-010 covers pin counts from 22 to 32, and MS-011 covers pin counts from 24 to 48. In the MS-001 family, three pin counts at 22, 24, and 28 leads are referred to in the industry as *skinny* DIPs because the bodies were narrowed from the original lead row spacing width of 0.400 in for 22 leads and 0.600 in for 24 and 28 leads (MS-011) to 0.300 in. Another variation, known as *shrink* DIPs (SDIPs), has the same lead row spacing as the standard family but with the lead pitch reduced from 0.100 to 0.070 in to provide higher pin-count capability for the same size package, as outlined in MS-019, MS-020, and MS-021.

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**TABLE 7.10 Package Families by Packaging Technology**

| | Package Technology | | | |
|---|---|---|---|---|
| | Molded Plastic | Laminated Plastic | Laminated Ceramic | Pressed Ceramic |
| Sealing method | Molded | Molded/encapsulated | Metal lid seal | Glass lid seal |
| Surface mount | SOIC | PBGA | CQFP | CERQUAD |
| | SOJ | | LLCC | CQFP |
| | PLCC | | LDCC | |
| | BQFP | | SMPGA | |
| | MQFP | | CBGA | |
| | TQFP | | | |
| | TSOP | | | |
| | TAB | | | |
| | TapePak* | | | |
| Through hole mount | DIP | PPGA | DIP | DIP |
| | SIP | LLCC | SIP | CERDIP |
| | ZIP | | PGA | |
| | QUIP | | | |

*Registered trademark of National Semiconductor Corporation.

Similar DIP families are defined in the pressed ceramic technology (CERDIP) and in the laminated ceramic technology. Their outlines are registered and available to the user in Publication 95.[17] Pressed ceramic, both CERDIP and window-frame types, come in four body widths, with pin counts and footprints that are identical to those for the plastic DIP family. Laminated ceramic DIPs, however, come in a wide variety of configurations, identified by the method of lead attachment to the ceramic body. Laminated ceramic DIPs can be side-brazed, top-brazed, or bottom-brazed, as shown in Fig. 7.31. Side-brazed DIPs are footprint compatible with the plastic and pressed ceramic DIP families. Top- and bottom-brazed DIPs are generally supplied by a vendor as a flat pack, and the leads are then formed to the specification of the end user, which may or may not be footprint compatible with the side-brazed variety.

DIPs are limited in pin count to 64 leads by the physical size of the package, which approaches 3.0 inches in length at 64 I/Os. At this level, the package piece part becomes very expensive, is difficult to handle, generally begins to degrade the electrical performance of the device, and uses up a lot of expensive PWB real estate. Area array packages (e.g., PGAs) were developed to extend the pin-count capability for TH-mount-type packages with a significant saving in PWB area. Figure 7.12 compares the physical size of a PGA package with pins on an area array of 0.100-in pitch to the DIP at an in-line 0.100-in pitch. The 0.100-in pitch PGA family is available in both laminated plastic and ceramic technologies and can provide pin-count capability above 1000 pins. JEDEC registered outline MO-066 covers a range of CPGA pin arrays from 9 × 9 (81 maximum pin count) to 20 × 20 array (400 maximum pin count) in both cavity-up and cavity-down configurations.

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The largest registered CPGA outline, at 1300 pin count, has an overall body size of 2.66 in (67.6 mm) with a staggered pin arrangement.

Other in-line families that are popular today are the single-in-line package (SIP) family, MO-035, the zigzag-in-line package (ZIP) family, MO-054 and MO-072, and the quad-in-line package (QUIP) family, MO-029, MO-030, MO-031, and MO-033. All were introduced to meet special product needs, e.g., SIPs for memory chips and memory modules. These package families have pins typically on 0.100-in pitch and are available to 40 pin counts for ZIPs and to 64 for QUIPs. A QUIP has four in-line rows of leads, with the rows generally spaced 0.100 in apart, and the leads in each row staggered with respect to each other to maximize hole-to-hole spacing on the PWB. This package option effectively reduces the package length by one-half over the equivalent DIP of the same pin count. The wide range of IC packages in use worldwide is illustrated in Fig. 7.53.

### 7.5.2 Surface Mounted Packages

The first SM packages were introduced in the early 1980s to achieve higher board density and better electrical performance. Initially, industry acceptance of SM did not advance as rapidly as expected. However, the acceptance rate in the 1990s accelerated, and the demand for SM packages exceeded that for TH packages. Thus, the availability of new SM package types has expanded greatly into a very formidable list (Table 7.10).

Mature SM families today are those introduced in the early 1980s, such as the small-outlined (SO) and PLCC types in molded plastic, CERQUAD in pressed ceramic, and leadless (LLCCs) and leaded (LDCCs) chip carriers in laminated ceramic. These packages have leads on 0.050-in pitch instead of the 0.100-in pitch used in the TH families. SO is an in-line type, defined by body width, or lead row spacing, similarly to the way the DIP family is defined. MS-012 and MO-046, both narrow-body SOs, and MS-013, a wide-bodied SO, are gull wing (GW) families. The SO package with J leads (SOJs), a JEDEC-registered outline MS-023, has the same body width as MS-013; that is, it uses the same plastic molding die but has a J-formed lead for surface mounting. PLCCs, CERQUADs, LLCCs, and LDCCs are perimeter-type packages with the leads on all four sides of the package. The lead geometries vary with the technology used. PLCCs, MS-016 and MS-018, use J-shaped leads designed to provide the highest possible density on the PWB. CERQUAD packages generally come from the vendor as a leaded flat pack, and the device manufacturer or end user does the final lead forming (GW or J) prior to SM. The LLCC packages, MS-002 and MS-003, are generally restricted to surface mounting on substrates with similar thermal expansion coefficients. This limitation is overcome by using an LDCC, MO-081 and M-082. One way to achieve this is by converting an LLCC to an LDCC by means of one of the commercially available soldered clip-lead techniques. Today, LDCCs can be purchased either as leaded flat packs with the leads formed to the appropriate shape (GW or J) by the device manufacturer or end user, or as finished packages with the leads in final form ready for SM. Examples of SO, PLCC, and CC packages are shown in Fig. 7.3.

The drive for higher pin counts and higher interconnect density has been very evident in the development of fine-pitch SM packages. Since the pin count of a perimeter package is a function of package size and lead pitch, as illustrated in Fig. 7.12, achieving a high pin count with PLCCs, at a 0.050-in lead pitch, requires very large packages. Difficulties in molding large plastic packages and maintaining coplanarity of all leads, necessary to achieve high board assembly yields, limited the practical PLCC size to 124 I/Os and 1.699-in lead-to-lead overall.

A new package family evolved to fill the needs for high pin count, namely the quad flat pack (QFP) with gull wing leads on all four sides (Figs. 7.54 and 7.55). The QFP has a lead

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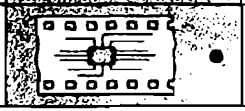
| Type | Package | Lead pitch |
|---|---|---|
| DIP | | • 2.54 mm (100 mil) |
| Shrink-DIP | | • 1.78 mm (70 mil) |
| Skinny-DIP | | • 2.54 mm (100 mil)<br>• Width ½ size |
| Zigzag in-line | | • 2.54 mm (100 mil)<br>• Two rows |
| Pin grid array | | • 2.54 mm (100 mil) |
| Ball grid array | | • 1.5 mm (60 mil)<br>• 1.27 mm (50 mil)<br>• 1.0 mm (40 mil) |
| Small-outline | | • 1.27 mm (50 mil)<br>• Leads on two sides |
| Flatpack | | • 1.0 mm<br>• 0.8 mm<br>• 0.5 mm<br>• 0.4 mm<br>• 0.8 mm<br>• Leads on four sides |
| Leadless chip carrier | | • 1.27 mm (50 mil)<br>• 1.00 mm (40 mil) |
| Leaded chip carrier | | • 1.27 mm (50 mil)<br>• J-leaded |
| Small-outline J-leaded | | • 1.27 mm (50 mil)<br>• Two rows |
| Tape automated bonding |  | • Thin package |

● Plastic ○ Ceramic

**FIGURE 7.53** A sampling of commercially available package types.

pitch that varies from 0.40 to 0.16-in (1.0 to 0.40 mm) and a maximum pin count of 376 leads. Two QFP families exist: the EIAJ MQFP version, shown in Fig. 7.54, and the bumpered JEDEC BQFP, shown in Fig. 7.55. The MQFP family is characterized as fixed body size, variable pitch. That is, a variety of pin counts can be manufactured from a single body size using lead frames of various external lead pitches from 0.040 in (1.0 mm) down to 0.016 in (0.40 mm), MS-022, MO-108, MO-112, and MS-029. The BQFP family is characterized as variable pitch, consisting of 0.020-in (0.50-mm), 0.025-in (0.60-mm) and 0.500-in (1.27-mm) pitches, and a variable body size, with a variety of pin counts. A different molding die is required for each package size, which range from 0.450 in at 52 I/Os to

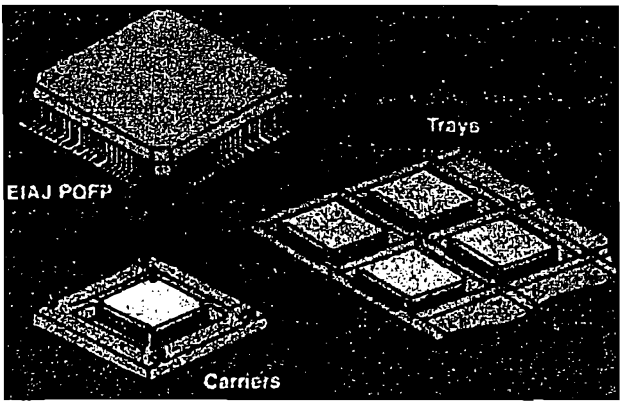



FIGURE 7.54 EIAJ MQFP packaging and handling options.

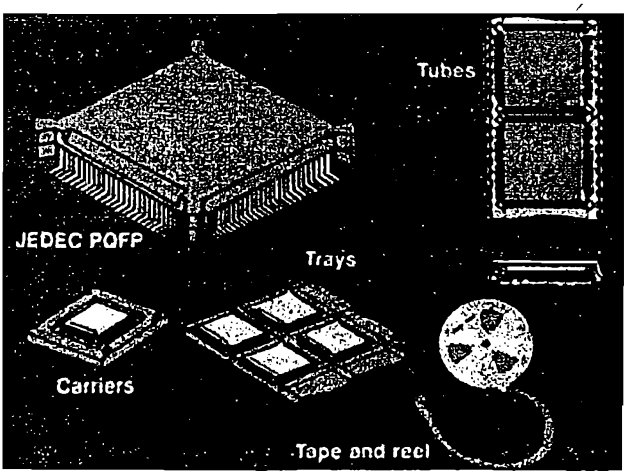



FIGURE 7.55 JEDEC BQFP packaging and handling options.

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1.650 in at 244 I/Os (MO-069, MO-071, MO-086, and MO-089). Major advantages of the JEDEC over the EIAJ version are that the bumpers provide for safe handling in tubes, trays, carriers, and tape and reel, and the generous stand-off provides for easy removal of flux from under the package after board assembly. The major advantage of the EIAJ over the JEDEC is the multiple lead counts available per package, compared with only one pin count per package size for the JEDEC. EIAJ packages are more difficult to handle without bending the leads and the low standoff on higher pin counts, causes high stress on solder joints due to board warp. EIAJ's head start by several years provided valuable experience in high-volume production, which enabled EIAJ to become the industry de facto standard before the JEDEC version left the ground. Both versions are in use today, but the EIAJ version has gained in popularity. The EIAJ MQFP family provides pin counts up to 376 I/Os, while the JEDEC BQFP has leveled off at 244 I/Os.

Another family of SM packages has been developed that are shorter, smaller, thinner, and lighter. The new package family consists of thin quad flat packs (TQFPs) that have been JEDEC registered as MS-026 outlines. Whereas the standard MQFP body thickness varies from 2.0 to 3.8 mm, depending on the package outer dimensions, the TQFP body thickness are 1.0 and 1.4 mm. The TQFP packages vary in lead count from the smallest, at 32 I/Os with a body size of 5.0 × 5.0 × 1.0 mm and an 0.80-mm lead pitch, to the largest, with a maximum lead count of 256 I/Os in a body size of 28.0 × 28.0 × 1.40 mm and a 0.40-mm pitch.

As the demand for packages with high I/O counts and high performance increases, the industry has turned to BGAs as a favorable alternative to the fine-pitch QFPs, which are difficult to handle. A great number of BGA outlines have been JEDEC registered in both laminated ceramic (MO-156 and MO-157) and plastic technologies (MS-028, MO-151, MO-192, and MO-205). The arrays range from 4 × 4 to 49 × 49, in sizes of 7.0 × 7.0 to 50.0 × 50.0 mm.

## 7.6 PACKAGE DESIGN CONSIDERATIONS

### 7.6.1 Electrical Design

Electrical performance at the IC package level is of general interest for silicon devices.[18] The ever-increasing speed of today's circuits and their potentially reduced noise margins require great care and consideration in IC package design. Several electrical performance criteria are of interest, namely, low ground resistance (minimum power-supply voltage drop), short signal leads (minimum self-inductance), minimum power-supply spiking due to signal lines switching simultaneously, short-paralleled signal runs (minimum mutual inductance and crosstalk), short-length signal runs near a ground plane (minimum capacitive loading), and the maximum use of matched impedances to avoid signal reflection. These criteria are, of course, not all mutually independent. They may be related through simple geometric variables such as conductor cross section and length, dielectric thickness, and dielectric constant of the package body. These problems are usually handled with transmission-line theory in PWBs, where the lengths of circuit paths are more obviously a cause for concern. A wealth of papers and books cover this topic, and all of the techniques described are generally applicable at the package level.[19–21]

Package inductances,[1] as a function of pin counts, for QFPs and BGAs are shown in Fig. 7.56. The higher inductance of the QFP is attributed to the larger perimeter lead package, and thus longer traces, when compared to the high interconnect density area array of

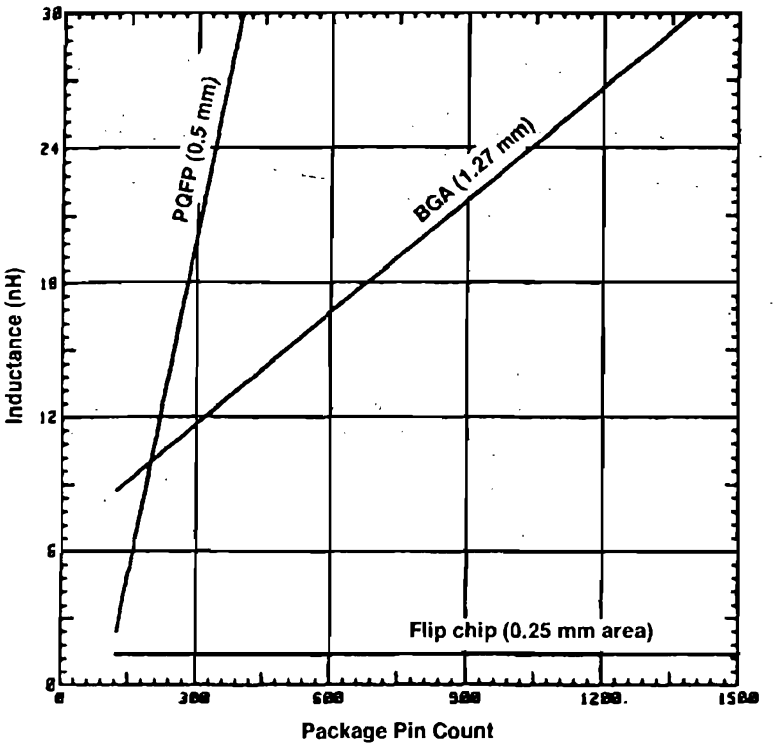


**FIGURE 7.56** BGA and PQFP comparison: performance (inductance). *(After Lau[1])*

BGAs. Similarly, package propagation delays are also affected by trace lengths, as shown in Fig. 7.57 for different package types.

The most important practical electrical design problem in IC packages is noise reduction. Basically, when a line switches, the voltage induced in the ground line is given by:

$$V_i = L_g \frac{di}{dt}$$

where $V_i$ is the induced voltage, $L_g$ is the inductance of the ground lead, and $di/dt$ is the derivative of current with respect to time. If $j$ lines are switching, then $V_i$ is given by:

$$V_i = L_g \sum_j \frac{di}{dt} j$$

To reduce $V_i$, multiple grounds must be used to lower $L_g$. If $m$ ground leads are used, the total inductance is approximately $L_g/m$. The practical result is that up to 25 percent of the leads may have to be grounded to control noise. This high percentage has a large impact

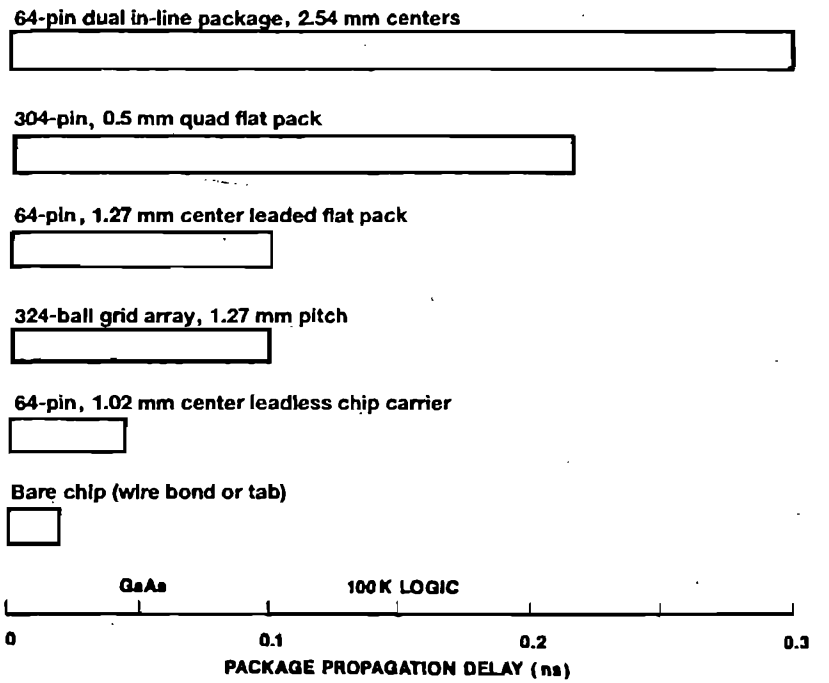


FIGURE 7.57 Comparison of maximum propagation delays for typical IC packages.

on packaging density and creates an incentive to reduce $L_g$. Inductance can be reduced significantly through the use of large-area power and ground planes within the package.[13]

### 7.6.2 Thermal Design

The thermal design objective is to keep the operating junction temperature of a silicon chip low enough to prevent triggering the temperature-activated failure mechanisms for the particular application in which the chip is used. Only in the simplest possible applications can this objective be met, considering the packaged silicon device alone. Usually, the packaged device environment must be established for most of the following variables: PWB temperature, total power dissipation on the board, local-neighbor power dissipation, degree of forced-air cooling, space usable by the package both laterally and vertically (between boards), conductivity of the PWB, and ideal performance of the isolated package. The following paragraphs discuss the thermal modeling of a single chip in a package.

In a simplistic heat transfer model of a packaged chip, the heat is transferred from the chip to the surface of the package by conduction and from the package surface to the ambient by convection and radiation. Typically, the temperature difference between the case and ambient is small and hence radiation can be neglected. This model also neglects conduction heat transfer out of the package terminals, which can become significant, par-

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ticularly with high-I/O packages. The overall thermal resistance in this model can be considered as the sum of two thermal resistance components $\theta_{jc}$ and $\theta_{ca}$ defined as:

$$\theta_{ja} = \theta_{jc} + \theta_{ca}(°C/W)$$

$$\theta_{jc} = \frac{T_j - T_c}{P}$$

$$\theta_{ca} = \frac{T_c - T_a}{P}$$

where $\theta_{ja}$ = junction-to-ambient thermal resistance
$\theta_{jc}$ = junction-to-case thermal resistance
$\theta_{ca}$ = case-to-ambient thermal resistance
$T_j$ = average die or junction temperature, °C
$T_c$ = average case temperature, °C
$T_a$ = ambient temperature, °C
$P$ = power dissipated, W

$\theta_{jc}$, the conductive thermal resistance for low-power applications, is relatively insensitive to the ambient and is mainly a function of package materials and geometry. For high power dissipation devices, one must also consider the temperature dependence of materials selected in design. For example, the thermal conductivity of typical materials used in ceramic packaging is temperature-dependent, as shown in Fig. 7.58.

$\theta_{ca}$ depends on package geometry, package orientation in the application, and the conditions of the ambient in the operating environment (free or forced convection heat transfer). In actual practice, most designers use experimental methods to determine the thermal resistance of a package configuration. Thermal characterizations are performed with a thermal chip assembled in the given package, which is then mounted into any number of

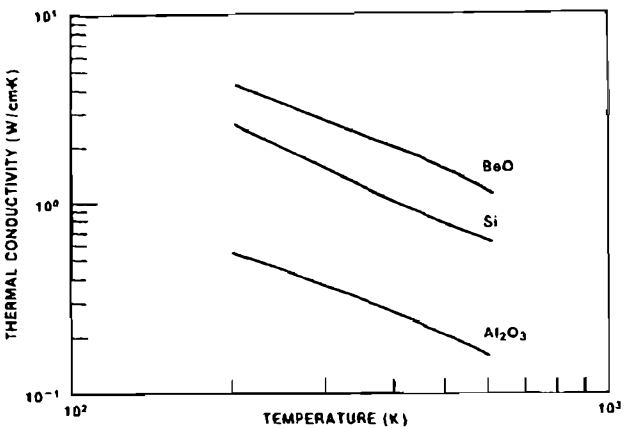


**FIGURE 7.58** Influence of temperature on thermal conductivity of IC-related materials.

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configurations such as in a fluid bath, on a heat sink, in a wind tunnel, or in still air. The package is monitored for input power as well as junction, case, and ambient temperatures. The results show that packaged devices with a preferred heat-flow path (most ceramic packages) may be thermally characterized independent of external heat sinking, while those with no preferred heat-flow path (most plastic packages) should be thermally characterized with a specific mounting arrangement and a convection heat-flow environment.[22,23] The use of simple modeling supported by experimentally derived values of thermal resistance is probably adequate for first-order determinations but should be followed by a more sophisticated program using specially designed test chips and computer modeling.

### 7.6.3 Thermomechanical Design

As the size of an IC chip increases, it presents new challenges to the package designer. Ideally, one prefers to use materials in package construction that are matched in physical properties, in particular the coefficient of thermal expansion. In the real world, however, we see that the materials currently in use have coefficients that vary by orders of magnitude, as shown in Fig. 7.20. The designer could achieve better matches by making engineering trade-offs that do not degrade the packaged-device yields, performance, or reliability. For example, if a chip in a molded plastic package is directly attached to an Alloy-42 lead frame, which has a good CTE match to silicon, the thermal stresses will be minimized. But, because of the poor thermal conductivity of Alloy-42, the lead frame may have an impact on the thermal performance of high power dissipating chips. In applications where high-power chips are used, an Alloy-42 lead frame could bring on higher thermal stresses, resulting in chip cracking or "pop-off " or degradation of performance and reliability due to higher junction temperatures during normal operating conditions. As a result, more than 80 percent of the current molded plastic packages utilize copper lead frames for applications where high thermal performance is required. The thermal stresses caused by the CTE mismatch between the copper lead frame, silicon, and molding compound are minimized by using a low-stress molding compound and die-attach epoxies.

In the preceding discussion, only base materials at the chip-attach interface were considered. In the actual design, the chip is attached using a material such as solder, braze, or polymer adhesive where heat is introduced to either melt the solder or braze material, or to thermally cure the polymer adhesive. Physical properties of these materials are shown in Table 7.11. The CTE and stiffness, which is a function of the tensile modulus $E$, significantly affect the thermal stress and the chip-attach interface as shown in Fig. 7.59. In addition, the thickness of the joint also impacts the thermal stress in the interface as shown in Fig. 7.60. Therefore, thermal stresses increase with increasing $E$ and decreasing thickness. Eutectic chip bonding has a very high $E$ and a thin bond line, thereby limiting its usefulness with very large chips.

Another major mismatch in expansion coefficients of materials used in package construction is between the epoxy molding compound and the chip. This mismatch does not exist in the pressed and laminated ceramic package technology, since no package materials come in direct contact with the IC surface. The chip itself is constructed of materials with over an order of magnitude difference in the CTE (Fig. 7.20), thus compounding the thermal-stress problem in plastic packages.

Analysts have developed sophisticated stress models and introduced computer aids, such as finite-element analyses, to increase their ability to characterize the thermal stresses and deformations throughout the entire plastic package, with the goal to optimize the reliability of the package. The molded plastic IC package is basically a composite structure

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**TABLE 7.1 Typical IC Package Material Properties**

| Material | Thermal Conductivity, K (W/m K) | Coefficient of Thermal Expansion CTE ($10^{-6}$/°C) | Density ρ (g/cm$^3$) | Specific Heat $C_P$ (cal/g °C) | Modulus of Elasticity, E (GPa) | Poisson's Ratio μ | Dielectric Constant @ 1 MHz | Application |
|---|---|---|---|---|---|---|---|---|
| Silicon | 150[35] | 2.7–3.5[35] | 2.3[29] | 0.18[29] | 13.0[29] | – | 11.7[35] | Integrated circuit |
| Silver-filled epoxy | 1.57[29] | 41.0[31] | 3.5[29] | 0.17[29] | 3.5[29] | – | 5.0[36] | Die bond adhesive |
| Bismaleimide triazine (BT) laminate | 0.26[31] | 15.0[32] | 1.8[31] | 0.30[31] | 20.9[31] | 0.19[32] | 3.9[31] | Substrate |
| 90–99% $Al_2O_3$ | 20.9[34] | 6.0–7.7[35] | 3.8[34] | 0.19[34] | 314[34] | 0.23[34] | 9.0[34] | Substrate |
| Beryllia (BeO) | 251[34] | 8.0[34] | 2.9[34] | 0.25[34] | 343[34] | 0.26[34] | 6.5[34] | Substrate |
| Copper | 398[37] | 17.2[31] | 8.9[31] | 0.093[29] | 117[31] | 0.31[37] | – | Cu circuitry on lamina, lead frame |
| Ni-Fe Alloys (Alloy-42) | 16.0[34] | 8.0[34] | 8.2[34] | 0.12[34] | 146[34] | | – | Lead frame |
| Gold | 318[37] | 14.1[33] | 19.3[29] | 0.03[29] | 78.0[29] | 0.2937 | – | Bond wire |
| Epoxy w/fused silica filler | 0.80[30] | 13.0[30] | 2.0[30] | 0.20[30] | 20.7[30] | ≈0.3 | 5.03[6] | Molding compound |
| Solder (63Sn/37Pb) | 50.0[38] | 24.0[38] | 8.4[31] | 0.036[38] | 16.0[38] | 0.4[38] | – | Solder balls (BGA) |



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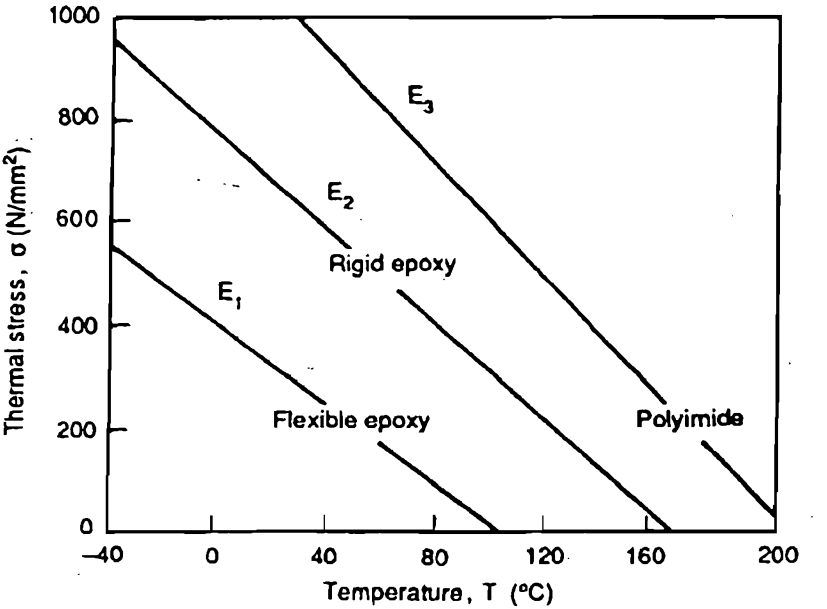


**FIGURE 7.59** Thermal stress predicted for flexible epoxy (tensile modulus $E_1$), rigid epoxy ($E_2$), and polyimide ($E_3$) as a function of temperature where $E_3 > E_2 > E_1$.

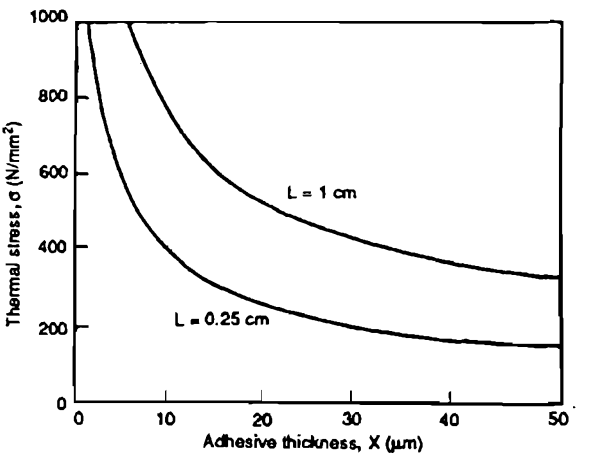


**FIGURE 7.60** Effect of chip length, $L$ and adhesive thickness on thermal stress.

consisting of a silicon chip, metal lead frame, and plastic molding compound, as shown in Fig. 7.61. A two-dimensional finite-element model of the cross section is shown in Fig. 7.62. The model is divided into small elements, interconnected at a discrete number of nodal points, creating a finite-element mesh. Material properties are assumed to be linearly related to the thermal load. Material interfaces are assumed to have perfect adhesion to each other. The model further assumes an initial isothermal condition of 17°C, corresponding to the molding temperature. The thermal stresses are then calculated at the desired isothermal temperature, which is typically set at –65°C, the lowest temperature expected during service or in transit. Figure 7.63 is a plot of the minimum principal stresses (compression) in both the molded plastic body and the silicon chip. The stress contours represent isobars of equal stress within the package and chip. Severe stress con-

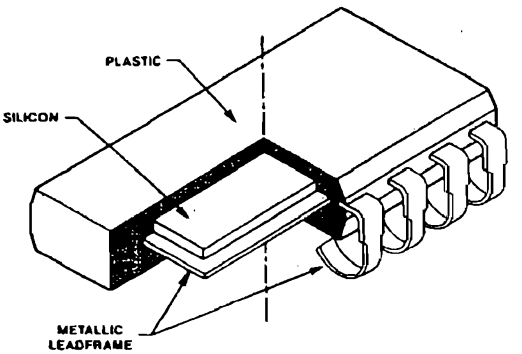


**FIGURE 7.61** The molded plastic package is basically a composite structure consisting of a silicon chip, metal lead frame, and plastic molding compound.

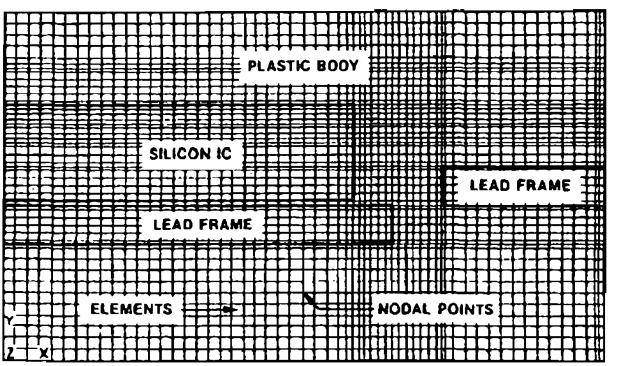


**FIGURE 7.62** Plane stress analysis is assumed for two-dimensional model. Model is divided into many small elements interconnected at a discrete number of nodal points. Because of symmetry, model covers only half the IC package.

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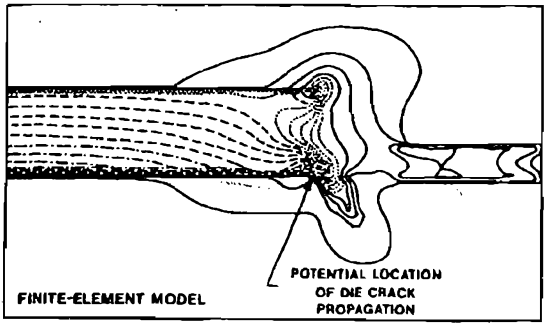


**FIGURE 7.63** Finite-element analysis plot showing contours of constant stress (minimum principal stress in compression) in both plastic body and silicon chip.

centration is evident at the lower edge of the chip, which could lead to chip cracking. The use of finite-element analysis has become a powerful tool for quickly predicting the impact of design and process changes with respect to stress-related failure mechanisms.

### 7.6.4 Physical Design—Chip Design Rules

The establishment of, and adherence to, good chip design rules is absolutely essential to achieving high yields in IC package assembly. Rules must be generated for the particular package type used and must be compatible with the assembly equipment. These decisions should be made early, preferably before the chip layout is started, and definitely before the layout is completed. As the I/O count grows and the active device feature size shrinks, the space required for interconnection could represent a major fraction of the chip area. To avoid this problem, the effective bonding pad sizes and pitch should be reduced. Not only must the pitch decrease, but the tolerances required to produce quality bonds must also decrease. Reliability and the ability to assemble IC chips automatically are affected directly by the chip layout. The chip-to-package interface design must ensure high assembly yields and avoid reliability problems associated with poor design rules.

Typical current production design rules for in-line wire bonding and the staggered-row bond pad configuration are illustrated in Fig. 7.64. Design rules recommend wire-bond pad sizes and pitch, clearance between pads, and the edge of the separated chip. Also shown are the maximum recommended wire-bond span lengths (chip to lead frame or substrate bond site) and the maximum recommended angle of the wire from the normal direction off the chip. These rules attempt to minimize wire sweep in plastic molding, which could lead to potential edge short circuits to silicon and short circuits to adjacent conductors on the lead frames or metallized conductors of the package.

Design rules can be integrated into chip design CAD systems. Figure 7.65 shows a typical package wire-bond CAD design template for a PBGA device. The locations of all lead frame wedge-bond targets and the optimized locations for the ball bonds on the chip are shown. The chip designer superimposes or merges this template with the proposed chip layout and can immediately see where bonding pads should be placed to achieve a manufacturable and reliable design. Figure 7.65 also illustrates two types of CAD wire-span templates used to verify design rules and to help decide cases where bond pad placement

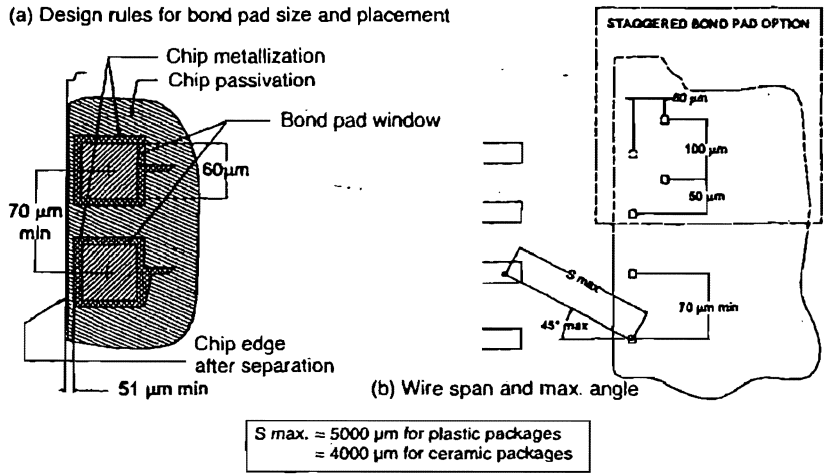


**FIGURE 7.64** (*a*) Typical chip design rules for bond pad size and placement. Bond pads should provide 60 × 60 μm open area and be on at least 70 μm center-to-center spacing. Maximum allowable wire span depends on package type used, with typical values noted. Wire angle, determined by chip-package interface, should not exceed 45° with respect to normal as shown in (*b*). Arrangement of staggered bonding pads results in lower pitch than that attainable with single in-line pads. Further restrictions on wire angle may be required.

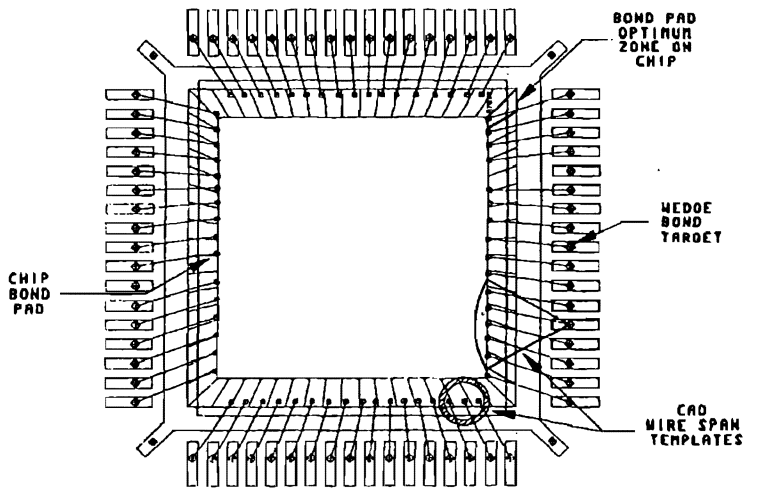


**FIGURE 7.65** Example of CAD template for positioning bonding pads on chip in optimum location to achieve high assembly yields and high-reliability performance. Support templates check adherence to wire-span guidelines and provide design flexibility for special cases where optimum zone is too restrictive for electrical layout.

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falls outside the optimum zone. The use of a CAD system by the device designer ensures the best possible design, particularly for high volume and low cost. In the case of high-performance custom designs, the same design rules apply. Since CAD tools may be too restrictive, chip and package designers must work as a team to ensure a manufacturable design.

## 7.7 PACKAGE IC ASSEMBLY PROCESSES

This section covers the first-level assembly processes used with each of the four package technologies. A detailed listing of all major package families, showing the preferred method of chip attachment and first level interconnection, is presented in Table 7.12. Also shown are lead form, lead arrangement, and type of mounting used at second-level assembly.

### 7.7.1 Chip to Package Interconnection

There are four chip-to-package interconnection options in use today, as illustrated in Fig. 7.66: wire bond (WB), flip chip (FC), beam lead (BL), and TAB. For wire-bonded packages, the chip interconnection process generally consists of two steps. In the first step, the back of the chip is mechanically attached to an appropriate mounting surface, for example the lead frame paddle or the die attach area of a laminated ceramic or plastic substrate. This attachment sometimes enables electrical connections to be made to the backside of the chip. There are three types of chip attachments in use today: metal alloy bonding (AuSi eutectic, AuSn eutectic, and soft solders), organic adhesives (epoxies and polyimides), and inorganic adhesives (silver-filled glasses). In the second step, the bond pads on the circuit side of the chip are electrically interconnected to the package by wire bonding. Wire bonding can be accomplished by either a thermosonic or thermocompression ball-wedge process using gold wire, or an ultrasonic wedge-to-wedge process using either gold or aluminum wire.

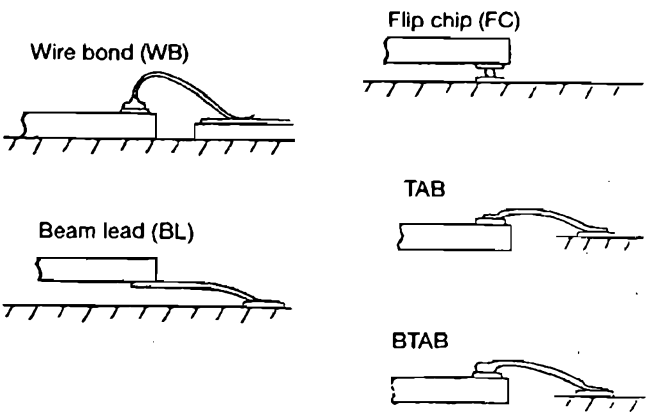


**FIGURE 7.66** IC package interconnection options.

**TABLE 7.12 Interconnection Levels and Major Process Options***

| Package | Chip attachment | Level 1 connection | Level 2 connection |
|---|---|---|---|
| Molded plastic | Ag-loaded organic | WB, Au | TH, IL |
| PDIP | None | TAB | |
| | Ag-loaded organic | WB, Au | SM, IL, GW/J |
| SOIC/J | Ag-loaded organic | WB, Au | SM, P, J |
| PQFP | Ag-loaded organic | WB, Au | SM, P, GW |
| | None | TAB | |
| TapePak | Nonconductive organic | TAB | SM, P, GW |
| Pressed ceramic | | | |
| CERDIP | Ag-loaded inorganic | WB, Al | TH, IL |
| CERQUAD/CQFP | Ag-loaded inorganic | WB, Al | SM, P, GW |
| Laminated ceramic | | | |
| DIP-STB/TB/BB | Metal, AuSi | WB, Au | TH, IL |
| PGA | Metal, AuSi | WB, Au | TH, AA |
| LLCC | Metal, AuSi | WB, Au | SM, P |
| LDCC | Metal, AuSi | WB, Au | SM, P, CL, BZL |
| FP-LDCC/QFP | Metal, AuSi | WB, Au | SM, P, GW/BZL |
| MCM-Si on C | Ag-loaded organic | WB, Au | |
| | None | TAB | |
| | None | FC | |
| BGA | Metal, AuSi | WB, Au | SM, AA |
| | None | FC, SB | |
| Laminated plastic | | | |
| LLCC | Ag-loaded organic | WB, Au | SM, P |
| PGA | Ag-loaded organic | WB, Au | TH, AA |
| SMBA/LGA | Ag-loaded organic | WB, Au | SM, AA |
| BGA | Ag-loaded organic | WB, Au | SM, AA |
| | None | FC, SB | |
| Other options | | | |
| COB | Ag-loaded organic | None | WB, Au/FC, SB |
| | None | None | OLB, TAB |
| TOB | None | ILB, TAB | OLB, TAB |
| MCM-Si on Si | FC, SB | FC, SB | |
| TQFP | Ag-loaded organic | WB, Au, WBT | SM, P, GW |

* BZL = brazed lead; J = J-formed lead; P = perimeter lead locus; SB = solder-bumped; SBZ = side-braced; AA = area array; for all other abbreviations, see App. A.

The other interconnection options illustrated in Fig. 7.66 (FC, BL, and TAB) generally are done as a one-step process, where the mechanical and electrical connections are provided by the same feature. The most popular interconnection process in general use today is thermosonic ball-wedge bonding. Table 7.13 shows the processing temperatures used in assembling IC packages in the four technologies.

*7.7.1.1 Chip Attachment.* As chip sizes increase, it places more stringent demands on the processing and reliability of chip bonding. Chip bonding of large chips (greater than 12 mm on a side) requires special attention to thermal and stress management, as dis-

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**TABLE 7.13 IC Assembly Process Temperatures**

| Process | | | Approximate Process Temp. °C |
|---|---|---|---|
| Die attachment | Eutectic bonding | Gold-silicon (98Au/2Si) | 425 |
| | | Gold-phosphorus (99.5Au/.5P) | 450 |
| | | Gold-tin (80Au/20Sn) | 280 |
| | Soft soldering (95Pb/5Sn) | | 315 |
| | Glass | | 450 |
| | Silver-glass | | 375 |
| | Epoxy (Ablestik #8360) | | 175 |
| Die interconnection | Wire bonding | Thermocompression | 300–400 |
| | | Ultrasonic | Room temp. |
| | | Thermosonic | 150 |
| | Tape automated bonding (TAB) | Thermocompression | 300–400 |
| | *(bumped chip or tape)* | Ultrasonic | Room temp. |
| | | Thermosonic | 150 |
| | Flip chip | Soldering (63Sn/37Pb) | 215 |
| Package sealing | Hermetic packages | Soldering (95Pb/5Sn) | 315 |
| | | Brazing (Au-Sn) | 320–350 |
| | | Welding | 1000–1500 (localized) |
| | | Glass sealing | 420 |
| | Nonhermetic packages | Epoxy molding | 175 |
| Package interconnection | Ceramic BGA | Solder cast column (90Pb/10Sn) | 315 |
| | Plastic BGA | Solder ball (63Sn/37Pb) | 215 |

cussed in Secs. 7.6.2 and 7.6.3. Chip size also impacts wafer fabrication guidelines and assembly automation. These issues influence equipment selection and determine how easily a controllable process can be achieved.

The major choices for a chip attach process include metal alloys (AuSi eutectic, AuSn eutectic, or soft solders), organic adhesives (epoxies), and inorganic adhesives (silver-filled glasses). Table 7.12 shows the preferred method of chip attachment for the various package types. Care must be exercised in the selection of a chip-bond process for the particular application, and in the implementation of stringent process controls to ensure high-quality bonds.

**TABLE 7.14 Inductance of Chip Attachment Technologies***

| | Cross Section, in | Length, in | Inductance,† nH |
|---|---|---|---|
| Wire bond | 0.001 (diameter) | 0.05 | 0.9 |
| TAB | 0.001 × 0.003 | 0.05 | 0.7 |
| Solder bump | 0.004 × 0.004 | 0.002 | <0.05 |

*Based on three-dimensional simulation of 200-I/O chip.
†25 percent of I/Os are power/ground.

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The eutectic chip attach process is essentially contamination-free, has excellent shear strength, provides high thermal conductivity across interface, and ensures low moisture in package cavities. The major disadvantages are that the preforms are difficult to handle for high-speed automation as compared to epoxy die attach. This process may also induce high thermal stresses on the chip due to the high process temperature. Using ceramic substrate materials (e.g., AlN and SiC) whose coefficient of thermal expansion closely matches that of silicon will reduce the thermal stresses, which can be detrimental to large chips.

The organic chip attach process uses an epoxy that may be electrically and thermally conductive or nonconductive. The epoxy has the advantages of being less expensive, more flexible, and easy to automate, and it requires low-temperature curing which minimizes thermal stresses in large chips. As a result, epoxy chip-bond adhesives are preferred for attaching large chips in both ceramic and plastic packages.

Silver-filled epoxy adhesives are of major interest today as chip-bond materials. The use of silver fillers (typically flakes) makes the epoxy both electrically conductive, to provide low resistance between the chip and the substrate, and thermally conductive, to allow a good thermal path between the chip and the rest of the package.

The epoxy chip-attach process can be highly automated and accurate, since the epoxy can be applied at very high rates to the die-attach area by transfer-printing, epoxy writing, or syringe dispensing, and the chip can be placed with high-speed pick-and-place tools. Accurate chip placement affects automatic wire bonding by yielding greater consistency of wire lengths and improved looping characteristics. In addition, chip placement accuracy also enhances the wire bonder's pattern-recognition performance and efficiency. The chip is removed from its film frame tape using a surface or collet pickup tool and placed over the die attach area, contacting the epoxy pattern. Because epoxies are thermosetting polymers (they cross link when heated), they must be cured at elevated temperatures to complete the chip bond. Typical cure temperatures range from 125 to 175°C. In general, epoxy chip bonds are as good as or better than their metal counterparts, except in the most demanding applications where high temperatures, high current through the chip bond, and critical thermal performance are required.

The inorganic chip attach process is used in the assembly of pressed ceramic CERDIP- and CERQUAD-type packages where the final cure is done at the same time as the high-temperature glass-sealing operation. The chip attach material is a silver-loaded glass system in an organic medium, which is applied as a paste. In the wet form, silver-loaded glass contains 66.4 percent silver, 16.6 percent glass, 1.0 percent resin, and 16.0 percent solvent by weight. After drying and organic burnout, the system is completely inorganic with 80.0 percent silver and 20.0 percent glass by weight. The diffusion of silicon from the chip backside is important in the development of the bond. Adhesion between the silver glass and the silicon chip is achieved via a glass network structure that starts at the silicon dioxide film on the silicon chip backside, while the bonding mechanism between the silver glass and the ceramic substrate appears to be mechanical in nature. These materials have excellent thermal stability, are lower in cost than the AuSi eutectic, and can provide a void-free bond for high-reliability hermetic parts.

*7.7.1.2 Wire Bonding.* Wire bonding to silicon ICs is the most common interconnection process in use today. After attaching the IC to either a lead-frame paddle, a Cu slug, or top surface of a laminated plastic or ceramic substrate, the IC is wire bonded with either gold wire by the thermosonic, thermocompression, or ultrasonic techniques, or with aluminum wire by the ultrasonic process. Today, gold wires are mostly used for thermosonic wire-bonding and aluminum wires for ultrasonic bonding.

Gold wire is commonly used for ball-wedge bonding, that is, ball bonded to the chip bond pad (typically aluminum finish) and wedge bonded to a plated lead frame or sub-

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strate pads (typically gold or silver-plated), as shown in Fig. 7.67. One advantage of ball-wedge bonding comes from the symmetrical geometry of the capillary tip. The ball is formed at the tip of the capillary and then pressed against the die (Fig. 7.67*b*). The pressure and the thermosonic action result in bonding the ball to the die. The wedge bond can then be placed anywhere on a 360° arc around the ball bond, using the capillary tip (Fig. 7.67*d* and *e*). This capability to dress the wire in any direction from the ball is the key fac-

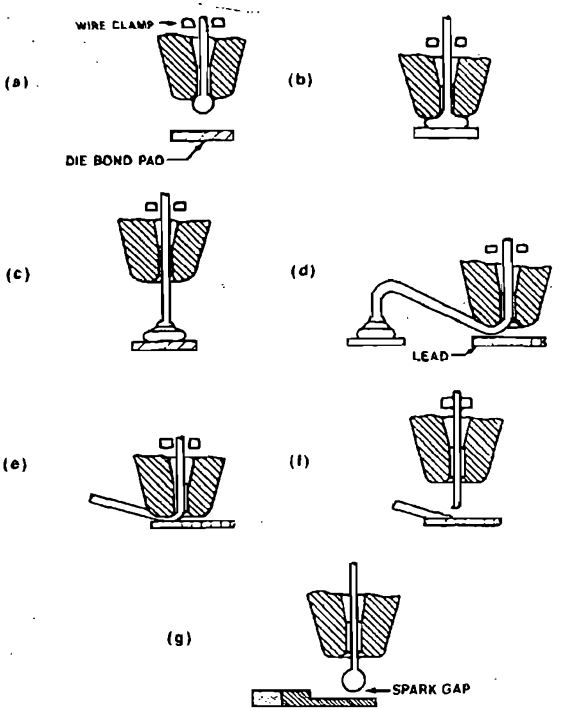


**FIGURE 7.67** Tailless ball-and-wedge bonding cycle. (*a*) Capillary is targeted on die's bond pad and positioned above die with ball formed on end of wire and pressed against face of capillary. (*b*) Capillary descents, bringing ball in contact with die. Inside cone, or radius, grips ball in forming bond. In a thermosonic system, ultrasonic vibration is then applied. (*c*) After ball is bonded to die, capillary rises to loop-height position. Clams are open and wire is free to feed out end of capillary. (*d*) Device lead is positioned under capillary, which is then lowered to lead. Wire is fed out end of capillary, forming a loop. (*e*) Capillary deforms wire against lead, producing wedge-shaped bond, which has a gradual transition into wire. In a thermosonic machine, ultrasonic vibration is then applied. (*f*) Capillary rises off lead, leaving stitch bond. At a preset height, clamps are closed while capillary is still rising with bonding head. This prevents wire from feeding out capillary and pulls at bond. Wire will break at thinnest cross section of bond. (*g*). New ball is formed on tail of wire, which extends from end of capillary. A hydrogen flame or an electronic spark may be used to form ball. Cycle is completed and ready for next ball bond.

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tor that makes this process attractive for high-speed automated bonding; that is, the bonding head or package table does not have to rotate to form the wedge bond. Figure 7.68 shows a typical device that is ball-and-wedge bonded on today's state of the art automatic wire bonders running at approximately 8 wires per second, depending on wire lengths.

Aluminum wire is typically wedge-to-wedge bonded. In a wedge-to-wedge configuration, the orientation of the wedge bond on the chip determines the direction of the wire that terminates on the substrate wedge bond. The complication of requiring motion in both the bonding head and the work holder results in a slower wire bonding process. On the other hand, wedge-to-wedge wire bonding has the capability of bonding to bond pads on tighter centers than ball-wedge bonding. Recent advances in wire bonders and tool geometries reduced the in-line wedge bond pad pitch capability on the chip to 0.002 in (50 μm), compared with an in-line pitch of 0.0028 in (70 μm) or a staggered configuration with an effective pitch of 0.002 in (50 μm) for ball bonding in production (see Fig. 7.64), both using 0.0010-in (0.025-mm) diameter wire. But the current advantage of the wedge-wedge fine pitch bonding will be diminished in the near future as the ball bonding pitch is further reduced. It is reported[28] that, by the year 2001, the in-line ball bonding pitch in production will be 0.0020 in (50 μm) or a staggered ball bond configuration with an effective pitch of 0.0014 in (35 μm).

The major issue in establishing a quality and reliable wire-bonding process is process control. Two types of process tests are in use today, the wire pull test and the ball shear test.

*7.7.1.3 Tape Automated Bonding.* In the 1960s and 1970s, tape automated bonding (TAB) was used for low-cost, high-volume production of products referred to as *jelly bean* devices. The driving force was strictly low cost, which was achieved by using automated

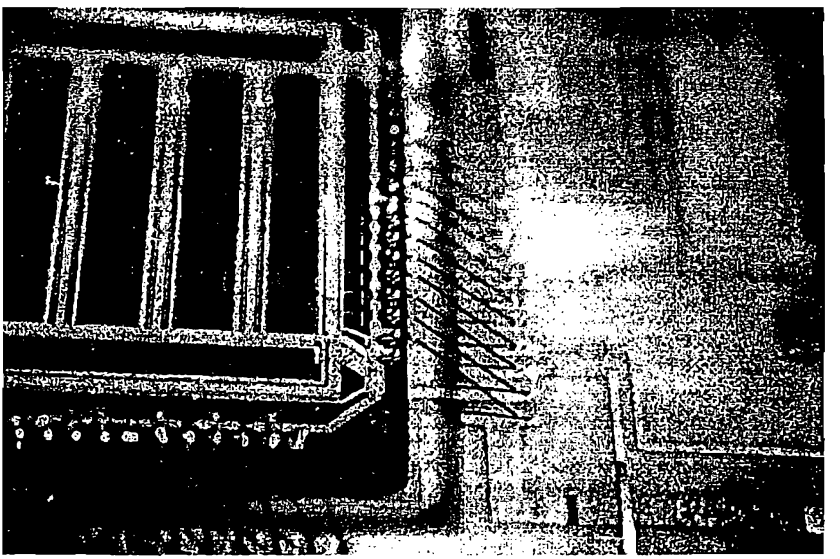

FIGURE 7.68 Typical thermosonic ball wire bonds on IC chip.

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gang bonding of the inner and outer leads in place of the then very slow manual wire bonding. The process was faster and cheaper than the other options illustrated in Fig. 7.66, and it resulted in higher bond strength (reliability) than the other options.

In the 1980s, TAB was pursued because of its many attributes, such as lower inductance, controlled lead geometry, higher bond strength (reliability), and controlled impedance capability, all resulting in better electrical performance than wire bonding. In addition, the characteristic smaller bond pad and pitch significantly reduced the chip size, resulting in better wafer yields and lower chip cost. The physical size of TAB devices also resulted in a significant reduction of real estate at the PWB level.

TAB technology uses a photo-imaging/etching process to produce conductors on a dielectric conductor tape in a "movie-film" format, as illustrated in Fig. 7.69. Carrier tape is stored on reels in widths from 1.4 to 2.8 in (35 to 70 mm). The final tape design has a window with "beam-type" leads that extend over the windows of the tape. Conductors are fanned out from the high-density beams on 0.002- to 0.004-in (0.05- to 0.10-mm) pitch to the external outer bond locations on 0.006- to 0.02-in (0.15- to 0.50-mm) pitch and then beyond to test pads placed on a 0.050-in (1.27-mm) pitch, compatible with conventional test probes. An example of a 300-I/O tape with inner beams on a 0.004-in (0.10-mm) pitch is shown in Fig. 7.70.

In inner-lead bonding (ILB), the beams are bonded to an IC chip that is precisely located under the windows, as shown in Fig. 7.69. Figure 7.71 is a scanning electron microscope (SEM) view of an ILB chip. Once the chips are bonded to the tape, the leads are isolated electrically by a punching operation, and then the chip-in-tape is electrically tested and, if required, burned-in. Finally, the outer lead bonding (OLB) operation transfers the chip, with its leads, to the next-level package. This could be the plastic molding of a QFP with over 164 leads, an MCM, or direct bonding to a PWB or other substrate.

TAB wafer preparation is similar to that for wire-bonded wafers. Either a pinhole-free silicon nitride, silicon dioxide, or a polyimide is deposited at low temperatures. Passivation is selectively removed, leaving a good portion of the aluminum pads exposed. The

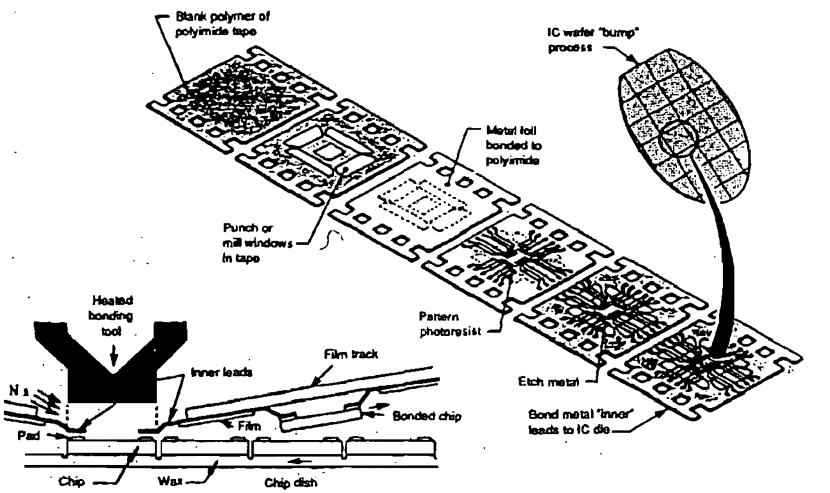


**FIGURE 7.69** Overall TAB process diagram with chip-on-tape component manufacture.

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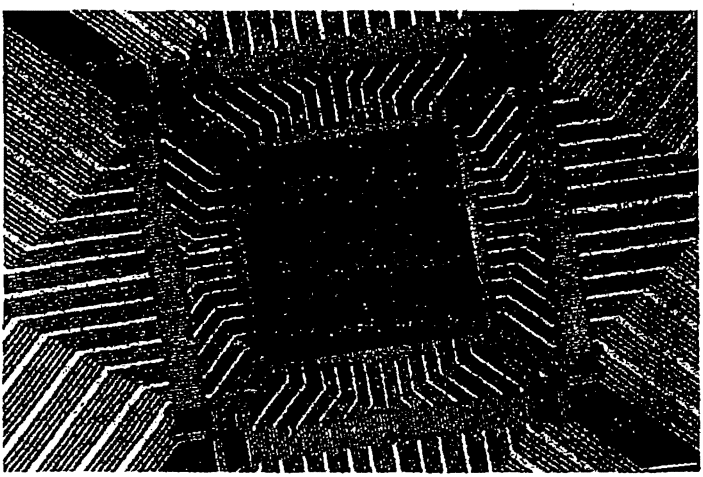

FIGURE 7.70 TAB tape with inner leads on 0.004-in pitch. *(Courtesy of Mesa Technology)*

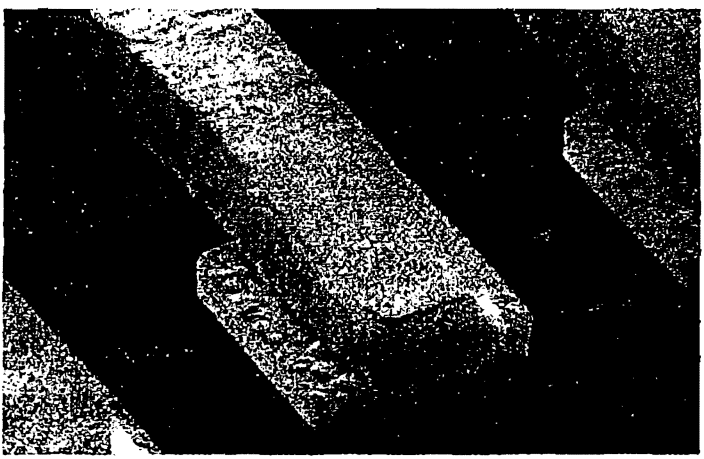

FIGURE 7.71 Inner-lead bonded chip. *(Courtesy of Aptos and Mesa Technology)*

chip is now in a state where it is ready for wire bonding or sent on for additional TAB fabrication, that is, preparation of the pads for TAB bonding. There are basically two methods of TAB in use: bumped chip, as shown in Figs. 7.72 and 7.73, and bumped tape, as illustrated in Figs. 7.74 and 7.75.

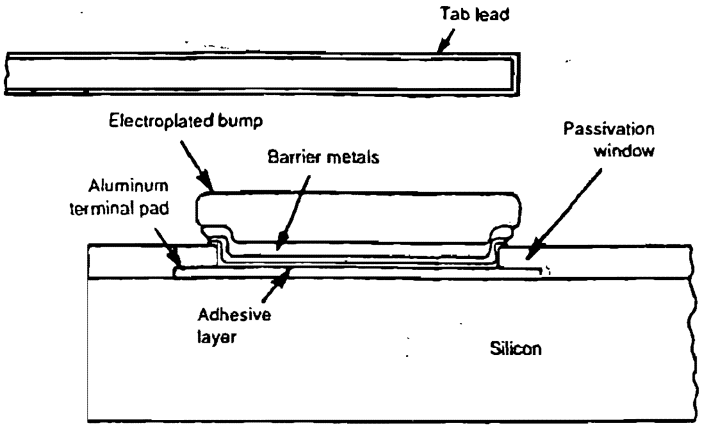


**FIGURE 7.72** Interconnection geometry of bumped-chip TAB. TAB lead is either copper foil, ranging in thickness from 2 oz (0.0028 in/0.07 mm) to 1/2 oz, depending on feature sizes required in tape design. Lead is gold plated to facilitate TC ILB. Electroplated bump thickness is typically 0.001 in (0.025 mm). Barrier metals are deposited in three layers, such as 600-Å Ti, 400-Å Pd, and 2000-Å Au.

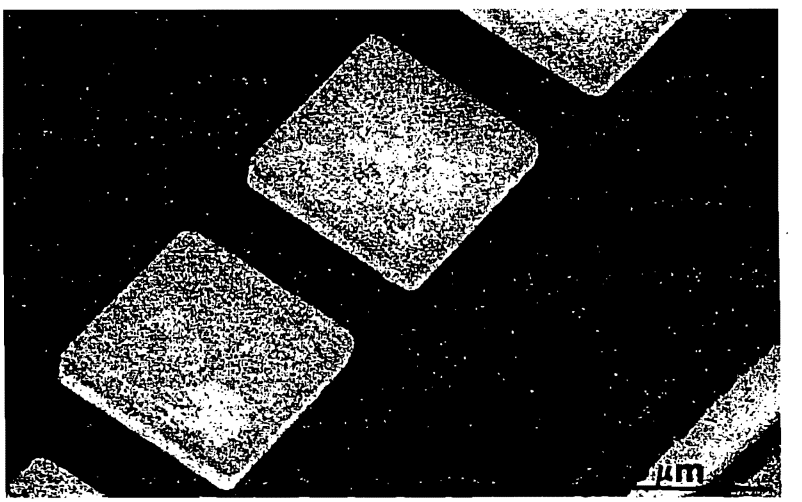


**FIGURE 7.73** SEM view of gold bumps on a chip. *(Courtesy of Aptos)*

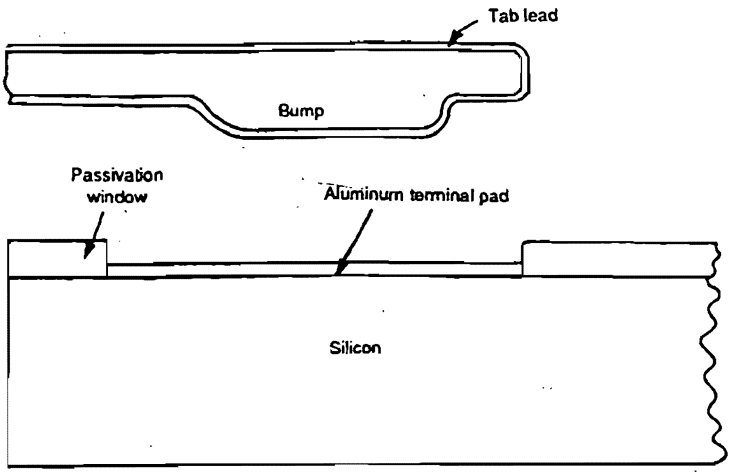


**FIGURE 7.74** Interconnection geometry of bumped-tape TAB (BTAB). TAB lead is copper foil with etched bumps and gold plated to facilitate TC ILB.

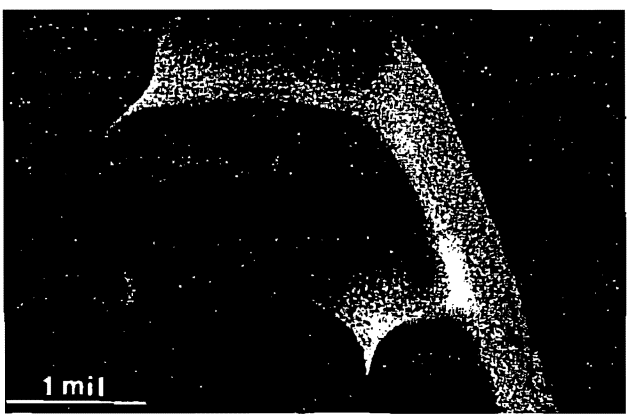


**FIGURE 7.75** SEM view of bumped tape lead. *(Courtesy of Mesa Technology)*

Three types of TAB tapes are in use today: single-layer, two-layer, and three-layer. Single-layer tape is a conductive foil without any insulating layer. It is the lowest-cost TAB construction and is used in jelly bean products where pre-electrical testing is not required. Two- and three-layer tapes are composed of conductive and insulating layers that are combined by direct deposit of copper on film (two-layer) or by the use of adhesives to hold them together (three-layer). In either tape, the insulator acts as a carrier and isolates the leads electrically. The various types of tape construction are shown in Fig. 7.76. Also

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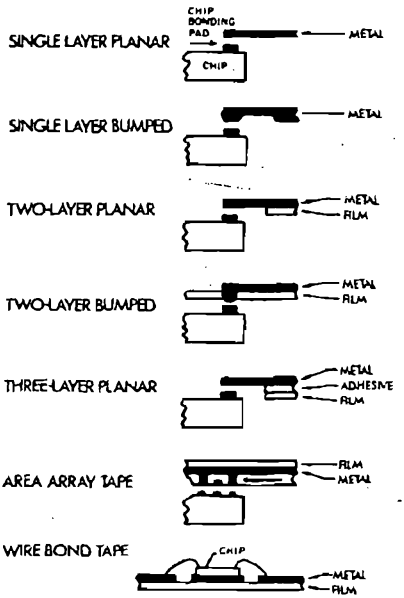


**FIGURE 7.76** Various types of tape construction. *(Courtesy of 3M Corporation)*

shown is an area array tape, which contacts pads anywhere on the chip surface, and a wire-bondable tape, which allows the extension of wire bonding to chips.

As a result of technological advancements in wire bonders, TAB no longer has the fine-pitch bonding advantages over wire bonding. Whereas TAB can accommodate an in-line bond pad pitch on the chip of 0.002 in (50 μm), the projected capability for wire bonding by the year 2001 is an in-line pitch of 0.0020 in (50 μm) or a staggered effective pitch of 0.0014 in (35 μm). An IC on TAB tape has the advantage that it can be fully tested and burned-in before committing to the next level of assembly. On the other hand, TAB requires a tape design for each chip size and pad location variation, as well as special tooling and expensive bonding equipment for ILB and OLB (second-level interconnection). The ICs are typically bumped, even with bumped tape, which adds to the cost. Finally, tight tolerances are required on planarity for gang bonding. If this is not achieved, the bonding yield and device reliability will be degraded. Single-point bonding (generally modified wire bonders) is sometimes used to overcome the lack of planarity.

*7.7.1.4 Flip Chip Bonding.* Flip chip (FC) bonding is a process that facilitates direct attachment and electrical interconnection of the chip to the substrate circuitry. Whereas wire bonding requires peripheral pads on the chip, the flip chip technology utilizes area array terminals that result in the highest I/O interconnection density of any of the bonding techniques. The terminals on the chip are placed face down (flip chip) onto matching footprints on the substrate, interconnecting through electrically conductive bumps. The bumps may be either solder or conductive epoxy, depending on the reliability requirements for a given application. Conductive epoxy bumping is a lower-cost, lower-reliability flip chip process that has recently been developed, but its acceptance by the industry has been slow, awaiting further evaluation.

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In the higher-reliability solder bump interconnection process, the ICs are solder bumped at the wafer level using various *bumping techniques*. One bumping scheme[16] consists of electrolytic tin/lead plating to wettable chip bonding pads, followed by a reflow to form the solder bumps, as illustrated in Fig. 7.77. The solder bumps vary in composition (97Pb/3Sn, 95Pb/5Sn, or 60Sn/40Pb), depending on the reflow temperatures that the applicable substrate can withstand. For ceramic substrates, a high melting temperature solder alloy (95Pb/5Sn, melting at ≈ 308°C) is preferred to avoid remelting of the bumps when the package is reflowed to the PWB. Since organic substrates are assembly processed at lower temperatures, the solder bumps require a lower melting temperature solder such as 63Sn/37Pb, which melts at ≈ 183°C.

Flux is applied to the IC solder bumps, which are then placed on matching footprints (FC pads) on the substrate and reflowed. The Cu FC pads are protected from corrosion by an electrolytic or electroless plated Ni/Au finish or with an organic surface preservative (OSP). To increase the volume of solder at the joint, the pads may also be solder bumped and coined. This operation can be done by the substrate manufacturer/vendor or prior to chip assembly.

After chip attachment, an epoxy underfill is dispensed along the edge of the chip and by capillary action it fills the gap between the chip and substrate. The purpose of the epoxy underfill is to protect the chip surface from moisture and to help reduce the stresses developed in the solder joints caused by the coefficient of thermal expansion mismatches of the materials being joined.

The short and stubby solder bump interconnections, between the chip and substrate, provide inductances that are significantly lower than for TAB or wire bonded chips, as shown in Table 7.14 (p. 79). The lower inductances, in combination with the higher interconnection density, result in improved electrical performance. The major disadvantage of flip chip bonding is the thermal mismatch between the chip and substrate that may cause the solder bump interconnections to fatigue during thermal cycling.

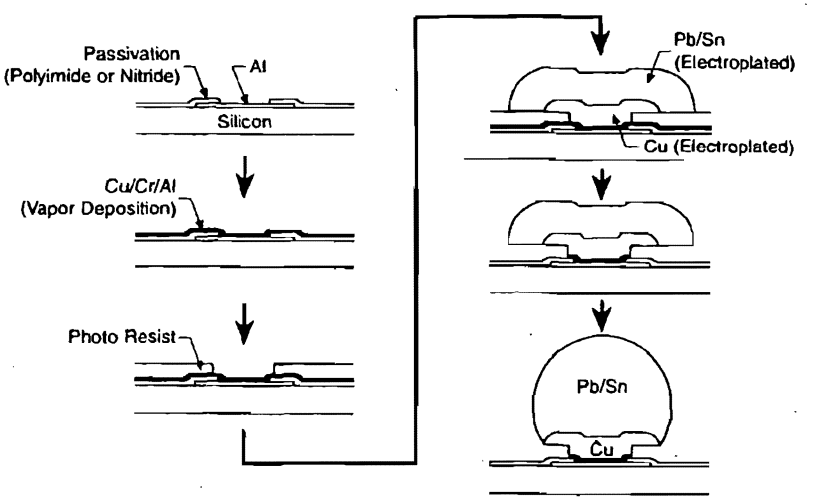


**FIGURE 7.77** Typical solder bump-forming process. *(Courtesy of Citizen Watch Co., Ltd.; after Citizen[16])*

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## 7.7.2 Other Assembly Processes

This section looks at other package assembly processes that must be considered to have a complete package assembly methodology. Among them are cleaning, package lid sealing, encapsulation, alpha particle protection, and assembly environment.

*7.7.2.1 Cleaning.* In IC packaging, the most critical cleaning steps are before wire bonding, FC underfill, before ink code marking, and after BGA solder ball attachment. The cleaning process must be chemically compatible with the chip metallurgy. Aluminum has a very narrow range of pH values in which its oxide protects it from corrosion in aqueous solution. Corrosion reactions, with metal dissolution, can occur in both basic and acidic solutions. Two objectives are usually sought in cleaning. One is the removal of organic species that can affect bondability; an organic solvent is usually required for this. The second is the removal of ionic species that can cause corrosion during the life of the device or, in an unusual instance, contribute to surface charge accumulation. Water is a very good solvent for ionic species.

Due to concerns of waste disposal and possible ozone depletion, the use of powerful solvents such as chlorofluorocarbon (CFC) and trichloroethylene (TCA) have been curtailed. Alternatives to cleaning with CFC and TCA solvents have emerged, such as aqueous, semiaqueous, and fluorocarbon inerted organics, oxygenated organics, and other cleaning agents. But the most significant trend has been to shift to a "no-clean" IC assembly operation. The elimination of cleaning during IC assembly was made possible by (a) requiring that all incoming assembly components be in a certified clean condition and (b) minimizing contamination during assembly by conducting the operation in a Class 10,000 or better clean room environment. In addition, user-friendly cleaning processes are being used in assembling BGAs, such as UV-plasma cleaning prior to ink code marking the overmold and the use of aqueous cleaning agents to remove the water soluble flux after BGA solder ball attachment.

*7.7.2.2 Hermetic Package Lid Sealing.* The major objective of package sealing is to protect the device from external contaminants during its expected lifetime. Furthermore, any contaminants present before sealing must be removed to an acceptable level before or during sealing. Packages may be hermetically sealed with glass or metals or nonhermetically lidded with polymers. The definition of *hermeticity* used here includes not only the ability to pass a fine vacuum leak test, but also to exclude environmental contaminants for long periods of time.

Figure 7.16 shows the relative capabilities of several materials to exclude moisture over long time periods. Clearly, organic sealants are not good candidates for hermetic packages. However, in some cases, organic sealants, properly integrated into the package design, do meet the operational definition of a hermetic seal as given above. For almost all high-reliability applications, the hermetic seal is made with glass or metal. Glass sealing was mentioned previously for pressed ceramic, and the process is essentially the same for lid sealing. Many of the metal alloys used for chip bonding are suitable for lid sealing. A leak-tight metal seal that excludes the external environment can be made without difficulty. The real difficulty has been freeing the package of contaminants, especially water, before sealing.

No package should be sealed with greater than 6000 ppm water by volume (dew point 0°C). The technology to measure such moisture levels has been studied thoroughly.[25] The military specification limit is set at 5000 ppm by volume, mainly because of the technical difficulties in measuring moisture in small packages. Although 5000 ppm is the specification limit, the package assembler wants to achieve as low a moisture level as possible. A

particularly effective method to achieve low moisture levels makes use of the ability of atomic silicon to react with water to form SiO.[24] The atomic silicon is formed during lid sealing through the melting of the chip bond material or an added gettering preform. The reaction is

$$Si + H_2O \rightarrow SiO_2 + 2H_2$$

*7.7.2.3 Organic Encapsulation.* For applications where hermetic sealing is not a requirement, organic encapsulation is used. Encapsulation technologies may include either molding, potting, glob-top, or cavity fill and surface chip coatings when lid sealing. The encapsulant must possess material properties that will enable it to protect the chip from adverse environments, contaminants, package handling, storage, and second-level assembly. Mechanical strength, adhesion to silicon and substrate, CTE compatibility with silicon and substrate, temperature and moisture resistance, electrical insulation, chemical resistance, and flow characteristics are some of the traits to consider when selecting an encapsulant for a given application.

In all cases, the encapsulants are used to cover the chip surface and the fragile wire bonds. It is critical that the dispensing techniques and flow characteristics of the epoxy compound be tailored to the specific configuration to prevent air from being trapped or bond wire sweeps that may cause shorts.

Plastic packages, such as QFPs and BGAs, are encapsulated with a Novolac-based epoxy molding compound, typically consisting of an epoxy resin, accelerator, curing agent, silica fillers, flame retardant, and a mold release agent.

Potting compounds, usually consisting of a liquid two-component system, are used for hybrid modules and discrete devices. Glob-top or cavity-filled encapsulants are thermoset epoxies or silicone resin filled with inorganic fillers. Glob-top encapsulants are used in low-cost, single-layer PPGAs and on chip-on-board assemblies, whereas cavity-filled epoxies are primarily used for encapsulating cavity-structured, multilayer substrates for PPGAs and PBGAs.

In cases where polymer lid sealing is utilized, surface chip coatings can be used to protect the aluminum metallurgy from atmospheric contaminants such as moisture, alpha particles, and mechanical damage. Silicones, epoxies, and polyimides are very effective for this purpose and are used as encapsulants in premolded and laminated PPGAs in combination with a protective lid or cap.

*7.7.2.4 Alpha Particle Protection.* Soft errors in memory circuits due to alpha particles emanating from packaging materials were first reported in 1978;[10] since then, many papers have been published on the subject. Alpha particles are emitted by the decay of uranium and thorium atoms contained as impurities in packaging materials such as molding compounds and some lid sealing materials. As the features of the chip decrease, the chip becomes more sensitive to alpha particle emission.[4,15] Packaging materials (particularly ceramics) will probably not be pushed below the 0.001 to 0.01 alpha-particle/($cm^2 \cdot h$) level. Because alpha particles have low penetrating power in solids, low-alpha materials have been suggested as alpha-absorbing coatings on silicon chips.[14,15] An 0.001 alpha-particle/($cm^2 \cdot h$) emission rate, the lowest level anticipated, has been reported using silicone coatings.[15]

Molding compounds are typically filled with silica fillers to reduce the CTE, but a side effect is alpha-particle emission that can cause soft errors in memory devices assembled in plastic packages. Applying a silicone coating to the surface of the memory chip, prior to molding, reduces the alpha-particle absorption. The molding compounds used for encap-

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sulating memory devices contain silica fillers, made by chemical vapor deposition (CVD), that do not emit alpha particles, thus surface coating of memory chips is no longer required for alpha-particle protection.

*7.7.2.5 Assembly Environment.* The ever-decreasing feature sizes on chips, down into the submicrometer range (Fig. 7.5), and the use of finer bond pad pitches impose stringent requirements on the control of cleanliness in the assembly environment. At a feature size of 1 μm, as shown in Fig. 7.78, the density for foreign particles of 1 μm or greater in a typical room environment is astronomical. Foreign particles not removed before molding of plastic packages, or lid sealing in ceramic packages, can degrade the reliability of the packaged device. Examples of such failures are electrical short-circuiting between adjacent interconnections by metallic foreign particles and hard failures due to metal corrosion from foreign particles with high levels of contaminants. Critical assembly processes, such as chip attachment, wire bonding, and molding or lid sealing, are currently being done by many assembly houses in clean rooms having a Class 10,000 or better environment.

## 7.8 OUTSOURCING—SUBCONTRACT ASSEMBLY

As the demand for IC packages increases, semiconductor companies are increasingly looking at assembly contractors to fill the order. Semiconductor companies must evaluate their packaging strategy and decide whether to assemble in house, rely on contract assembly, or depend on some combination of the two. As assembly volumes rise and the number of assembly contractors increases, the industry can expect to see price reductions and a broader range of packaging services.

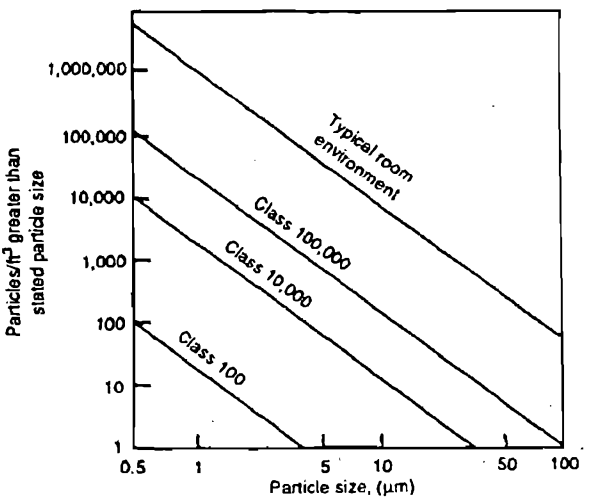


**FIGURE 7.78** Particle-size distribution in typical room atmosphere and in three classes of clean environments.

This section introduces the reader to contract assembly, lists some of the current assembly contractors and suggests guidelines for contractor selection. Opportunities exist for semiconductor manufacturers and contract assemblers to establish close, long-term business relationships as long as mutual requirements and expectations are clearly communicated.

### 7.8.1 What Is a Contract Assembly Vendor?

A contract assembly vendor is a manufacturer who has contractually agreed to supply materials and perform work for the semiconductor company in accordance with the specifications, drawings, and purchase order for the applicable product. The vendor becomes an extension of the semiconductor company's manufacturing business and, to some extent, is a partner with common interests and goals. The vendor's role in the partnership becomes more critical when a vendor is also asked to provide design, package characterization, and electrical test services in addition to assembly. Thus, the contract assembly vendors become an integral part of both product development and manufacture, from concept to market.

### 7.8.2 The In-House or Contract Assembly Decision

When semiconductor companies face a high-volume demand for a particular IC packaging technology, they must consider whether to manufacture in house or delegate this task to a contractor. The highly competitive state of the semiconductor business forces companies to continuously reevaluate their business strategy. In some cases, this means concentrating their resources in areas other than package design, development, and assembly, opting instead to outsource portions or all of these functions. Other companies have found that in-house design and assembly gives them better control over cost, the quality of the product, and production planning and thus creates or maintains a competitive edge. The decision whether to assemble in house or outsource should be based on the company's self-examination of business objectives, areas to concentrate its business, and company's strengths and weaknesses. Some of the advantages and disadvantages of in-house assembly vs. outsourcing are listed in Table 7.15. These are to be included in the strategic planning and should be evaluated for their effect on business objectives and the needs of each product line. Once the manufacturing strategy has been decided and acted upon, periodic reviews should be conducted to determine if the company's objectives continue to be met by the original approach or a new strategy needs to be implemented. Some companies that have initially opted for contract assembly have decided, after subsequent reviews, to convert to in-house assembly. The change may have been prompted by a reversal in the company's business strategy or product volumes that have matured enough to warrant investment in capital equipment and resources.

### 7.8.3 Guidelines for Selecting a Contract Assembly Vendor

Choosing a contract assembly vendor must be viewed as the beginning of a process that may eventually lead to a long-term business, technical, and manufacturing relationship. Unless the goal is simple assembly of a few prototype parts for a one-time-only, cost-insensitive application (rarely if ever the case), a great deal of effort needs to be spent in evaluating and selecting a contract assembly vendor. Once the commitment to go with a

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**TABLE 7.15 The Advantages and Disadvantages of In-house and Contract Assembly**

| Manufacturing Strategy | Advantages | Disadvantages |
|---|---|---|
| In-house assembly | Better production planning<br>Leverages internal technology and manufacturing know-how<br>Protects critical design and manufacturing processes<br>Enhanced quality control | Large investment in capital equipment that may not be recovered if life of product is short<br>Requires internal resources for design, development and manufacturing support |
| Contract assembly | Capital equipment investment not required<br>Improved initial time to market<br>Cost advantage of high volume manufacturing<br>Reduces manufacturing learning curve<br>Access to vendors manufacturing capability and expertise<br>Manufacturing base may be closer to customers | Must conform to contractor's manufacturing design rules<br>May unintentionally disclose business strategies and technology information<br>No control over manufacturing queue.<br>Indirect quality control<br>Subject to vendor's development plans and schedules |

particular vendor is made, the customer and assembly vendor must be ready and willing to dedicate the time and resources required to build an effective relationship. This is a process that is measured in months and years rather than days or weeks.

Many factors influence assembly vendor selection, as shown in Table 7.16. A few of the more important items to look for in a good vendor are discussed below.

**TABLE 7.16 Contract Assembly Vendor Selection Guidelines**

- Competitive pricing and intervals
- Broad experience and established history of contract assembly
- Well developed product line, including open tooled standard offerings
- Good design capability (staff, tools, CAD compatibility and automatic design checking)
- Good production management system (preferably accessible by customer)
- Rapid and accurate response to requests for information (price, delivery, technical)
- Technical expertise (package design process development, package characterization)
- Clear single point interface for technical issues
- Regular contact with account representative

Competitive pricing, manufacturing intervals, and experience in contract assembly are first on the list. A good assembly vendor will have demonstrated a commitment to the industry with significant and continuous investment in capacity to meet projected assembly requirements. The vendor should have proven experience in various package types. Pricing and intervals should reflect this experience.

The vendor should offer types of packages required for current and future applications without distracting the customer with niche or dead-end package types. A broad package

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offering with many footprints and types to choose from is attractive and desirable. The downside is that too many package offerings reduce the opportunity for both the customer and the vendor to leverage the advantages of standardization.

The vendor should clearly identify standard packages, emerging standards, and packages in development or with limited production history. This will help the customer develop a realistic assessment of the risks involved in selecting a particular configuration.

The vendor should promote IC package standardization across the industry by defining and supporting work on open tooled standard test sockets, shipping trays, etc. To meet the semiconductor manufacturer's needs, a better assembly vendor will develop new IC package configurations and introduce them to market backed by qualification and electrical/thermal performance data.

The vendor should provide clear and timely responses to the semiconductor manufacturer's information requests through the account representative. Initially, during the design phases of a project, the inquiries may be about product offering, cost, or assembly design rules. But, after production starts, the vendor is expected to provide timely and accurate production and delivery information over the product lifetime. Production programs extend over months and years and thus reinforce the need for an established long-term relationship between the semiconductor manufacturer and the assembly vendor.

A partial list of contract assembly vendors include Apack, Anam, ASAT, ASE, Carsem, Chipak, Citizen, Fujitsu, Hana, Kyocera, Rohm, and Shinko. Each vendor specializes in assembling certain types of IC package technologies. The reader should consult the vendor's latest offerings.

## 7.9 PACKAGE TO SECOND-LEVEL INTERCONNECTION

Second-level interconnections for the four package technologies, in TH and SM configurations, are compared in Table 7.12. Parameters affecting the second-level interconnections are lead configuration (in-line, perimeter, or area array) and shape or geometry of the leads (GW, J, TAB, side-brazed leads, solder balls, or FC). Details of the TH and SM processes are covered in Chap. 8.

The reliability of the second-level interconnection is affected by the expansion mismatches between the IC package materials and the circuit board during system temperature fluctuation. The differential expansions induce stresses in the leads or solder ball joints that may result in early fatigue failure, if not controlled.

Taking a BGA package as an example, the fatigue stresses that contribute to crack initiation and propagation in the solder joints are influenced by the following:

- Solder pad diameter on substrate circuit board
- Circuit board thickness
- Ball position from edge of chip
- Solder ball diameter
- Solder joint height after reflow
- Chip size
- Fluctuating temperature range
- CTE of the composite materials associated with the BGA and circuit board

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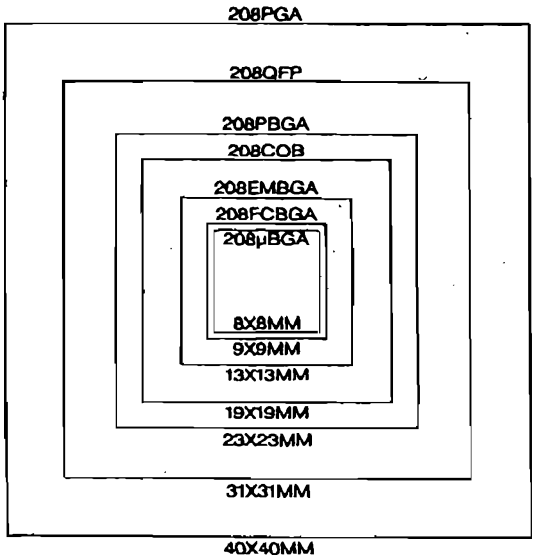
## 7.10 SUMMARY AND FUTURE TRENDS

Four package technologies have emerged over the years, and each has enjoyed its share of success. Demand for higher pin counts will undoubtedly continue with ever-increasing silicon capability. Laminated $Al_2O_3$ ceramic packages dominated the high-performance packaging technology until several years ago, but factors such as its high dielectric constant, modest thermal conductivity, and high cost have forced the industry to consider other packaging materials, including laminated plastic packages.

Requirements for higher packaging density on the PWB level are driving package designs towards smaller perimeter lead pitches and array type packages. To illustrate the differences in mounting areas of various package technologies, a 208-I/O package was used for comparison (Fig. 7.79). The demand for BGAs has increased over the past few years because of their robust construction, ease of assembly to the PWB, and area advantage over peripheral lead type packages such as QFPs (Fig. 7.80).




Comparisons based on the following:

| | |
|---|---|
| 208 I/O die size | = 7.6 x 7.6 mm max. |
| 208 PGA | = 40 x 40 mm, 100 mil pin pitch |
| 208 QFP | = 31 x 31 mm, 20 mil lead pitch |
| 208 PBGA | = 23 x 23 mm, 1.27 mm solder ball pitch |
| 208 COB | = 19 x 19 mm, wire bonded, 0.23 mm pad pitch |
| 208 EMBGA | = 13 x 13 mm, 0.8 mm solder ball pitch |
| 208 FCBGA | = 9 x 9 mm, 0.5 mm solder ball pitch |
| 208 μBGA | = 8 x 8 mm, 0.5 mm solder ball pitch |

**FIGURE 7.79** Mounting area comparison of IC packages.

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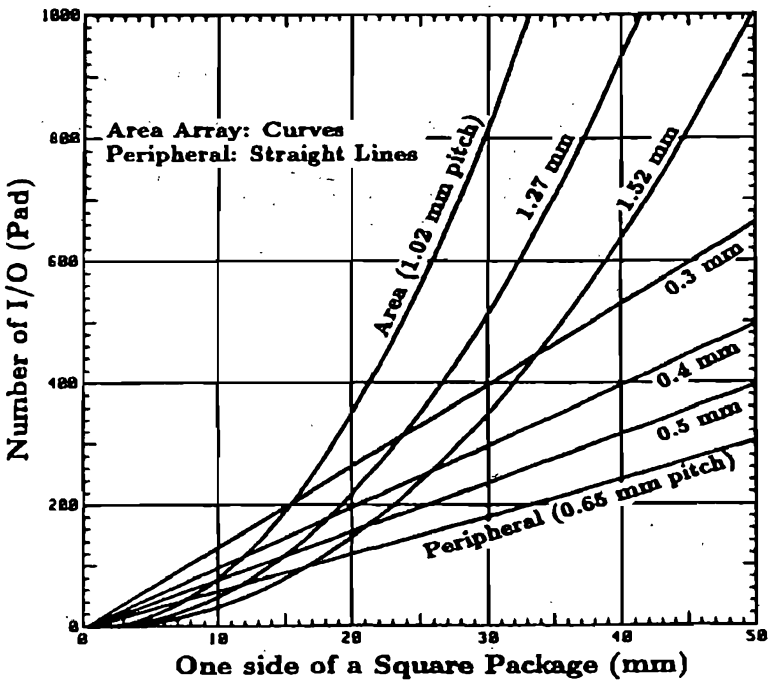


FIGURE 7.80 BGA and PQFP comparison: pin counts vs. package size, assumes full array for BGAs. *(After Lau[1])*

Figure 7.80 shows that, above 100 I/Os, the BGA, with solder balls on 0.050-in (1.27-mm) pitch and fully populated, uses less area on the PWB than the QFP with peripheral leads on 0.020-in (0.50-mm) pitch. At a peripheral lead pitch of 0.012 in (0.30 mm), the crossover is at approximately 300 I/Os. BGAs are now challenging the fine-pitch perimeter packages, which are difficult to handle and have a greater board assembly yield loss than the array-type packages.

Competing with traditional packaged devices will be the drive to direct chip attach (both perimeter and array types) and chip scale packaging where the ultimate in high density and performance can be achieved.

Newer packaging materials are being developed so as to improve material properties to achieve better performance, better reliability, and lower costs. Designers will make more use of package enhancement features, e.g., heat spreaders in molded plastic packages, internal ground/power planes, and heat spreading copper slugs in laminated plastic packages.

The ever-decreasing feature sizes of IC chips will place demands on interconnect technology capabilities for connecting to very closely spaced bond pads. Wire bonding in particular will be challenged. If wire bonding is to survive, it will need improvements in placement accuracy to meet demands of tighter bond pad pitches. It will also be necessary to provide the capability of longer wire spans with controlled wire dressing to bridge the gap between the chip bond pads and the second bond targets, while avoiding short circuits

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between adjacent wires in the dense wire fan-in pattern. Wire bonding of high-I/O chips will need to be done in Class 10,000, or better, clean rooms to optimize automatic wire-bonder performance and achieve acceptable bonding yields.

FC will be giving wire bonding serious competition as the future interconnection technology for IC packaging. FC has the advantage of very low power and ground inductance connections to the package and the best capability in terms of the density of interconnection (using an area array) to the device compared to wire bonding or TAB.

The system design will depend more and more on a systematic optimization of the entire interconnection scheme to achieve the potential benefits of improved silicon capability. This optimization may lead to completely new requirements for assembly and packaging but, more likely, it will lead to a sorting out of the various existing assembly technologies and packages.

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