

Packaging Technologies for Mobile Platforms

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Abstract

As electronic devices do more in less space, the technologies that enable them are challenged to do the same. Semiconductor packaging is no exception. As manufacturers attempt to integrate more functionality into slimmer, smaller form factors, advanced packaging, along with SOC integration, is used to reduce the size, cost and power consumption of the integrated circuits inside those mobile devices. New technologies such as multi-die SiP (System-in-Package), stacked packages or PoP (Package-on-Package), packages integrating other packages or PiP (Package-in-Package), packages that integrate passives with silicon die or LTCC (Low Temperature Co-fired Ceramic) and finally Redistributive Chip Packaging (RCP), all promise to improve performance and reduce package sizes. These innovations in IC packaging technology will enable manufacturers of converged products such as smart phones and multimedia players, to create the small, sleek multifunction devices to meet their market demands. However, each of these packaging technologies has trade-offs and benefits that should be carefully evaluated prior to final selection a device packaging solution.

Introduction

Packaging is the final step in the complex process of turning silicon into a useful semiconductor device. As such, it has a significant effect on the appearance and function of end-user devices, from computers to cell phones to embedded processors. As in most electronics, the trend is to make semiconductor devices smaller yet more powerful. This evolution can be traced through three types of packaging technologies: system in package (SiP), package on package (PoP) and a new packaging innovation, Redistributive Chip Packaging (RCP).

All of these packaging technologies provide benefits not only to end device manufacturers, but also to consumers. Manufacturers gain the benefit of high levels of integration so that they can use increasingly sophisticated electronics without adding bulk. This integration also saves board space, enabling additional functionality such as cameras, multimedia players, and PDA's, thus creating converged mobile devices and creating true form factor freedom. Consumers see the benefit of these feature rich, smaller mobile devices as an increase in their mobility and a decrease in the number of products they carry with them.

SiP and PoP

System in package, as the name implies, is a technology that allows the placement of several integrated circuits in one package, providing a complete set of device electronics in a small area. This technique saves board space by integrating die that were once spread farther apart on the circuit board.

Package on package takes this integration a step further, placing one package on top of another for greater integration complexity and interconnect density. PoP also offers procurement flexibility, lower cost of ownership, better total system and solution costs and faster time to market.

PoP packaging makes it a very flexible choice. The baseband and memory or other silicon are assembled, tested and yielded independently. Figure 1 illustrates how the top chip in this kind of package can be any ASIC, such as memory, an applications processor, a Bluetooth module or a camera module.

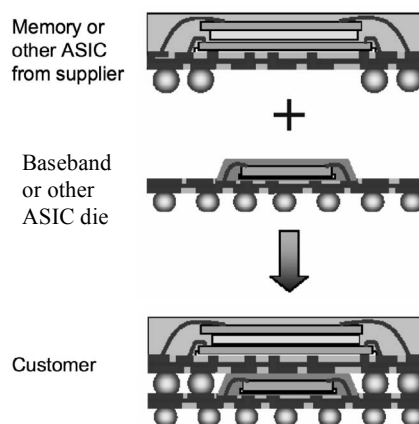


Figure 1. Package-on-Package Assembly Process

End users can change memory configurations as needed, providing great product flexibility and inventory control. Because PoP is a Joint Electron Device Engineering Council (JEDEC) standard, the lower package design can be optimized to accommodate any component integration as long as the upper package meets the defined standards.

PoP enables standardization of I/O pin out configurations for easier implementation. Application level integration, done during application assembly, is part of the set of services we offer our customers. Software modifications are driven by customers' applications, not by memory selection.

Scalability is another PoP advantage. Because PoP body sizes must conform to the JEDEC standard, customers can maintain control of memory procurement, enabling multiple suppliers, supplier qualifications and certifications and minimal inventory vulnerability. Customers can choose from various memory types and sizes such as Flash, SDRAM or DDR.

In terms of cost, the standards-based PoP approach limits exposure to memory market fluctuations, design choices and demand plans. PoP enables faster transitions to lower-cost memory and system solutions, including faster

implementations of die shrinks, faster qualification cycles and the ability to add and maintain multiple sources. Memory and baseband are tested separately, creating higher final test yields. Because known good die (KGD) and its rigorous testing costs are not required, memory suppliers can save money. Additional cost savings can be realized through standardization of test equipment and using it on a wider range of JEDEC-compliant packages.

Although PoP is preferable in many cases, there are cost and complexity choices that may lead an end user to choose SiP. Affordability of two packages, stacking the packages during application reflow, and package warpage issues represent only a few of the trade-off considerations.

Wire Bonding

SiP and PoP packages both use wire bonding to connect the die and the package. Innovation in wire bond technology is critical to the successful implementation of either of these packaging solutions. For example, bond and probe over passivation and bond over active for low-k (<90 nm) dielectrics, can reduce die sizes, increase functional integration, and optimize a packaged system solution. Both these techniques place active circuitry in previously unused areas beneath bond pads. Wire bonded devices that have high I/O counts also have high bond pad counts, which results in a significant portion of the die not being available for routing of active circuitry. Being able to use more space on the die allows smaller, denser die designs with higher levels of functionality.

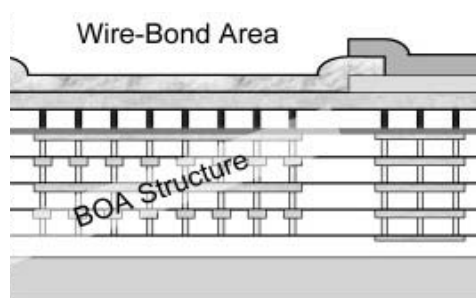


Figure 2. Example of Bond Over Active structure (BOA)

To meet the needs of increased functionality and improve die area utilization, I/O densities continue to increase. Wirebond pad layout designs for both fine pitch dual in-line and staggered configurations are widely used throughout the semiconductor industry today. As the wafer fabricating processes continue to enable die size reduction, the bond pad pitch and bond pad size must also reduce to prevent the smaller die from becoming pad limited. Bond pad pitch reduction from 47 to 40 microns combined with smaller bond pads enables high I/O counts for small die. The result is a higher level of functional integration for a given die size and a requirement for more complex and costly packaging solutions.

In the case of SiP packaging solutions, unless the die being stacked have been designed for die-to-die wirebonding, the wirebond requirements may be non-manufacturable. This type of non-optimized intergration will also significantly impact the complexity of the substrate design often forcing the use of

the most advance substrate design and manufacturing techniques available. It is not uncommon for these substrate designs to require 4 or more laminate layers. In cases where the wirebond count is high and the die size is small, the substrate design may become un-routable due to the requirements and limitations for the layer escape vias. In these extreme cases, the substrate may also be determined to be cost prohibitive to manufacture due to yield concerns or limits of available production technology.

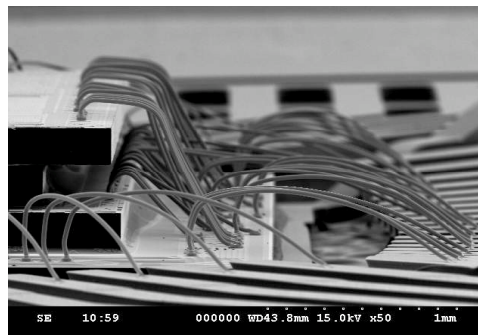
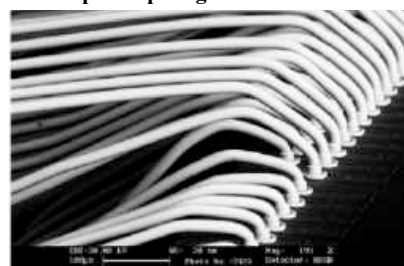


Figure 3: 3-Active die and silicon spacer wirebond

From a substrate wirebond layout perspective, PoP package designs usually are not as complicated as SiP designs. However, they present their own challenges from a wirebonding process perspective. When IC packages are being integrated by stacking, wirebond loop height and wire length must receive extra consideration. Because the clearance between the two packages is minimal, the wirebond loop heights must decrease. The combination of a reduction in wirebond loop height and the need to maintain acceptable assembly manufacturing throughput and yield, forces the wirebond lengths to be constrained. These constraints combine to reduce the flexibility of PoP for functional integration and to decrease the cost effectiveness of this packaging solution. For small die with a large number of I/O, these limitations can completely eliminate the PoP technology as a viable packaging solution.

Figure 4. 47μ-fine pitch wire bond example showing multiple loop heights



The End of Wirebond

While wirebond technology is the mainstay of the semiconductor packaging process, it still has limitations. The wires themselves are problematic when used in high density, fine pitch applications. As previously mentioned, the substrate designs are complex and often non-manufacturable.

In addition, due to wirebond manufacturing requirements and substrate design limitations, the size of the substrates are often larger than the target applications accommodate. Flip chip is a step in the direction of eliminating wire bonding. In the flip chip process, a die is connected facedown to a board or substrate using a ball array pattern or other conductive bumps attached to peripheral pads such as those used for wirebonding. This approach eliminates wire bonds, improves performance, and reduces size, but increases cost.

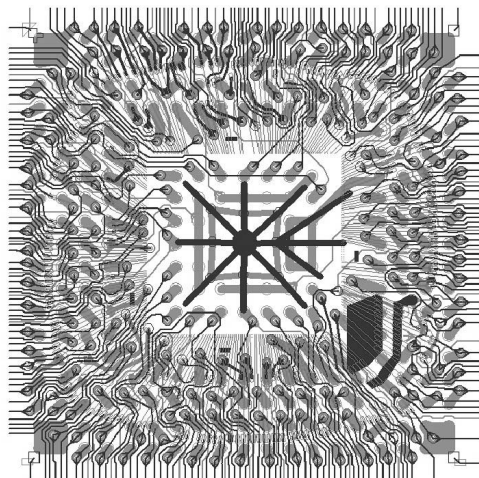


Figure 5. 13x13mm fine pitch wirebond substrate supporting 280 I/O at 47 μ wirebond pitch

Devices designed for flip chip benefit from interconnect densities at the die level but still are subject to the same substrate or interposer design limitations as wirebond products. Flip chip designs depend on traditional substrate solutions and technology to provide the interface between the die and the motherboard. Usually this results in a reduction in package size as the constraints in the substrate design for wirebonding are removed. However, since at the die level the redistribution designs for flip chip are fan-in only, they are restricted by many of same constraints seen in wirebond substrate designs. Signal route and trace rules and via escape limitations remain consistent between the two technologies. For die with a small number of interconnect requirements, the final package can be close to the die size. However, for small die with high interconnect requirements, the end result is a package that often is only slightly smaller than or even the same as the wirebond equivalent.

Many flip chip packaging solutions target performance improvements, such as lower signal inductance paths and improved thermal characteristics. However, since these designs are still substrate dependent, many of these enhancements can be compromised.

RCP technology goes beyond flip chip by eliminating the package substrates altogether. In doing so, the signal interconnect density is increased beyond what is achievable using conventional organic or film substrates. Organic and film substrates are limited to routing densities determined by the die size to package ratio, the material properties, pitch of

the wire bond fingers or bump interface, and the routing rules used to connect the wire bonds to the solder balls. Ultimately, this limits I/O density for a given package body size and pitch. RCP enables interconnect routing directly to the IC surface. This eliminates the need for the bond fingers, resulting in a smaller package with higher I/O density for a given package body size and pitch.

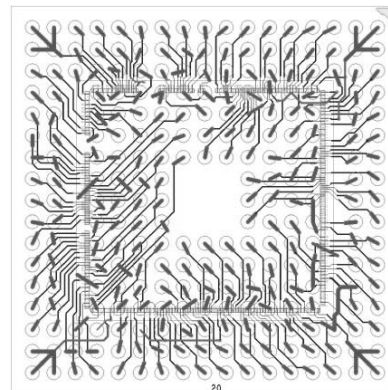
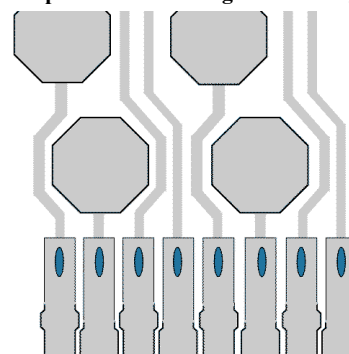


Figure 6. Equivalent interconnect to Figure 3 using RCP technology. New package body size is 9x9mm using 2-layers of Cu routing

In addition to reducing the interconnect complexity and size of the package, RCP technology also improves the overall package electrical characteristics. Using the above device as an example, a design using RDL (Redistribution Layer – Figure 6) resulted in an average of 0.5nH per lead increase when compared to an equivalent design that used Cu filled via's and Cu interconnect routed directly to the wirebond pads. This highlights the value and importance of optimizing an IC design for the targeted packaging

Figure 7. Example of RDL routing for die designed for



wirebond interconnect.

technology. In this case, IC designs optimized for RCP would result in reduced interconnect inductance and improved device performance. The ability to reduce the interconnect inductance and IR drop of signal pins is critical in all die designs and especially those targeted for low power, high speed applications such as those found in converged wireless products.

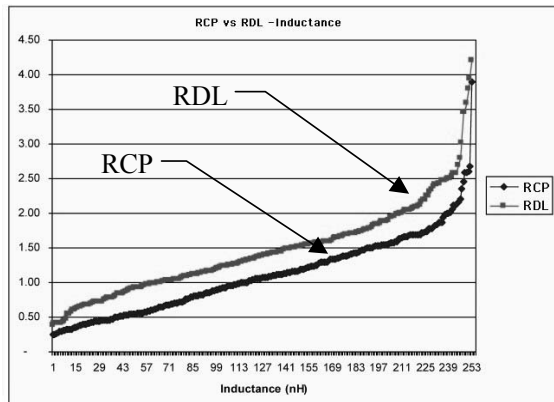


Figure 8. Inductance modeling results comparing RDL to RCP direct via interconnect.

When this same modeling technique is applied in a direct comparison between a wirebonded package and an RCP package of the same size, a significant reduction in lead interconnect inductance is noted. Specifically, in the RCP technology, a routing trace length of $200 \leq$ and $10 \leq$ thick, results in an inductance of approximately 2.25nH.

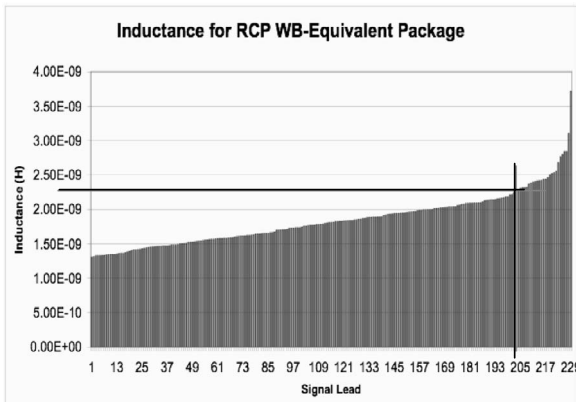


Figure 9. Trace inductance for 13x13mm RCP package; 200µ trace, 10µ Cu routing thickness

Modeling a wirebonded configuration of the same package body size using a 1.0-mil, 4N wire $200 \leq$'s in length resulted in a signal path inductance of approximately 7nH – over three times the effective loading!

These results are not trivial especially for products targeted for the wireless and portable products market. Designs for devices used in these applications typically have I/O counts in excess of 200 pads that now include high-speed interface ports targeted for large density memories such as DDR. To maintain the required signal integrity and minimize power loading effects, the package interconnect inductance must be kept at a minimum. Eliminating wirebonds is a major step forward in accomplishing both of these goals. In addition, wafer technologies of ≤ 90 nm often produce small die of high I/O designs requiring routing densities that go beyond the capabilities of traditional wirebond and substrate technologies.

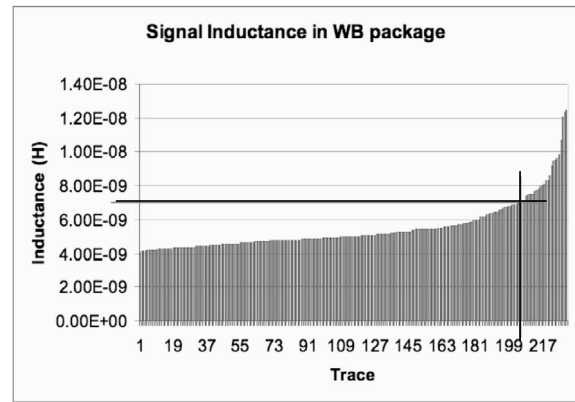


Figure 10. Lead inductance for 13x13mm wirebond package; 200µ wire length, 1.0mil diameter 4N wire, 10µ Cu thickness - substrate trace

Eliminating Substrates

As a “buildup” technology, the RCP technology actually builds the device package around pre-tested and singulated die. Other packaging methodologies and techniques insert a die directly onto or into a substrate and then uses flip chip RDL and bumps, or wire bond techniques to provide the die-package interconnect. In those cases, the substrate serves as the interface for routing between the die, other embedded components, and, ultimately, between the package and the application. As previously discussed, this approach to package design and interconnect construction usually defines the final package size and can result in the package being larger, more complex, and costly than desirable; especially true for wireless and portable applications.

On the other hand, RCP eliminates the substrate and the need for intermediate interconnects typically found with IC packaging solutions such as flip chip BGA and wirebond BGA (ball grid array). These technologies depend on the bumps or wires combined with a substrate to provide a complete interconnect solution. By using a dielectric material buildup process, the RCP technology creates the required electrical signal interface, provides the signal interconnect solution, while at the same time defining the final package body size.

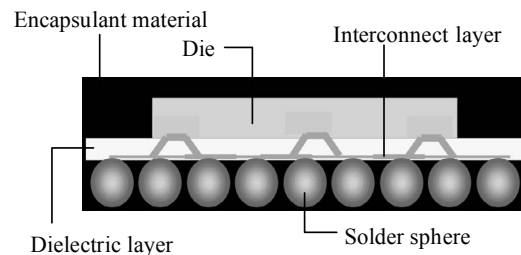


Figure 11. RCP single die package cross section

Due to the high density interconnect capabilities of RCP packaging technology the size of high-I/O count packages can be significantly reduced. For a given die size and pin-count, a package size can be reduced by up to 50 percent. The flexible routing characteristics achieved in a multi-layer buildup process can enable greater routing densities at finer geometries exceeding what can be achieved using the most aggressive techniques available for traditional substrate technologies. By comparison, RCP technology supports designs capable of $20 \leq$ route and trace while laminate substrate technology is only now capable of $50 \leq$ pitch with development plans of achieving $\leq 40 \leq$ at some time in the future.

I/O Count	BGA	FCBGA	RCP
257	13x13mm	10x10mm	9x9mm
383	14x14mm	12x12mm	10x10mm
573	14x14mm	13x13mm	12x12mm
652	15x15mm	14x14mm	13x13mm

Table 1: Package size comparison; BGA/FCBGA/RCP with solderball pitch of 0.5mm

Using fan-in and fan-out routing techniques, the routing densities of RCP far exceed the capabilities of laminate, film, or ceramic substrate technologies. Typical via capabilities of flip chip and wire bond substrates are currently limited to $60 \leq$ via on $130 \leq$ pad for two layer designs using advanced design and manufacturing techniques. For four layer substrate designs, these traditional substrate technologies are limited to $80 \leq$ via on $180 \leq$ pad. This limits the interconnect density and bond finger pitch for small die, high I/O designs, resulting in a significant impact to the final package body size. These larger package sizes are a delimiter for wire bond packaging solutions used in portable, converged mobile applications.

Flip chip designs have a secondary routing density limitation found at the die level. Typical interposer or substrate designs supporting C4 array die bump pad pitch are limited to $200 \leq$ bump pitch. Using advanced design and manufacturing techniques as described above can reduce this pitch to $150 \leq$. However, these fine pitch designs are limited to lower I/O count devices and are further constrained by the substrate design limitations described above. In addition, die bump designs are fan-in only and as such are size restricted to the interior of the die. Sensitive device structures such as analog, PLL, and oscillator circuits often further restrict the routing densities for the bump routing. In addition, certain memory designs and configurations are susceptible to soft errors and other functional issues when RDL, UBM, and/or bumps are placed over them. These “keep out zones” result in significant reduction of surface area for die bumping, often restricting the bumping area to the perimeter of the die. When these restrictions exist, the effectiveness of the flip chip technology to reduce package size is significantly impacted. When compared to a wirebond BGA, the combination of substrate routing limitations and die bump density restrictions can completely negate the package size reduction.

When compared to an equivalent RCP design, flip chip BGA package solutions are typically 15% larger for a given

die size and number of I/O. RCP technology currently supports $130 \leq$ via pitch and $25 \leq$ route/trace with development that will enable $40 \leq$ via pitch and $15 \leq$ route/trace. Using these ultra-fine pitch routing capabilities and the fan-in/fan-out interconnect routing capabilities, RCP typically enables the size reduction of traditional BGA or FC-BGA packaging solutions conservatively by 30%.

Further, by eliminating the substrate and enabling large array batch processing, RCP lowers packaging costs, allowing it to compete with commodity BGA packaging solutions. As discussed earlier, the RCP technology enables high-density pad array designs and provides significant design flexibility with improved noise, power distribution, and thermal characteristics.

Low K Compliance

Today's CMOS manufacturing processes enable superior conductivity with copper interconnects, and use low-k and ultra-low-k dielectric materials to further improve device performance. To provide die level interconnect, these new processes use multiple metal layers which significantly increases metal line capacitance, especially the capacitance between metal lines on the same level. The low-k dielectric materials are used as interlayer dielectrics (ILDS) to effectively reduce propagation delay, cross talk noise, and power dissipation due to resistance-capacitance (RC) coupling. Conventional over mold packaging technologies using either wirebonding or even flip chip bumping, place stress on the silicon dielectric material and can alter the device electrical characteristics.

Table 2: Benchmark comparison of SiP/PoP/RCP packaging technologies.

Legend: ● = Best ○ = Good △ = OK ☒ = Not good			
	SiP	PoP	RCP
Package/system cost	☒ ☒	△ △	● ●
Package reliability	○	△	Data not available
Package footprint	○	△	●
PCB footprint	○	△	●
Integration density	○	△	●
Customer surface mount technology (SMT) assembly	○	△	●
Electrical performance	○	△	●
Thermal performance	△	△	●
Flexibility	☒	○	●
Requires memory known good die (KGD)	Yes	Yes, for top package	No

As manufacturing processes shrink from 90 to 65 to 45 nanometers, these packaging concerns become more critical. Molding and wirebonding operations can induce mechanical stress on the low-k ILDS altering the functional behavior of a device and result in reliability failures. RCP technology eliminates the need for costly low-stress molding compounds and additive polyimide passivation processes. The dielectric material used in the RCP buildup process places minimal stress on the surface of the die and is inherently compatible with low-k silicon devices.

Benefits of Redistributed Chip Packaging

As an emerging technology, RCP may displace current packaging solutions in many applications. In some applications there will be cost and manufacturability tradeoffs that make SiP, PoP, flip chip or other packaging technologies a better choice. These technologies will continue to be required to support a wide variety of low I/O IC designs (≤ 200 I/O) that do not require high density interconnect or, not targeted for markets driven by low power, limited battery budgets, and miniaturization.

As I/O and interconnect density increases, the benefits of RCP rise exponentially. The primary limitation for a technology such as RCP is the I/O density relative to the die size. This implies that the number of I/O and the die size will determine the absolute size of an RCP package. As shown in Table 1, the relative size of an RCP package designed for a high I/O count device will be smaller when compared to either a BGA package or a FCBGA. For very small die and low I/O, package designs using any of the three technologies may result in package sizes of near the same size. An additional technology that must be considered for the small die/low I/O designs is WL-CSP (Wafer Level CSP). This packaging technology will result in very small packages and for devices with high raw or native yields in wafer fabrication, this technology may be cost effective as well. The primary constraints for this technology is that the die size determines the package size, it is a “fan-in” interconnect only, and the package cost is dependent on the wafer cost and yield.

I/O Count	BGA (mm)	FCBGA (mm)	WLCSP (mm)	QFN (mm)	RCP (mm)
48	8x8	8x8	4x4	7x7	5x5
76	8x8	8x8	5x5	7x7	5x5
144	10x10	8x8	6x6	8x8	5x5

Table 3. Package body size comparison for small die and low I/O. Data from production products.

However, the RCP technology does not require substrates, wires, or additional interconnect processing steps as seen with these other packaging technologies. The ability to add packaging cost only to the die yielded after probe is a significant cost advantage. Another key differentiator of this technology is the ability to route the electrical interconnect in both a fan-in and fan-out manner. This enables the ability to route and provide electrical contact points across the entire surface of a die without damaging sensitive circuitry, altering device performance, or, in the case of low-k materials, applying damaging stress to the die structure.

An additional benefit of the RCP technology is the ability to integrate additional functionality into the package itself during the buildup process. Power busses required for multi-CORE designs used in wireless baseband designs can be moved from the die design and into the package fabricating process. In a similar fashion, inductors can be built. Due to the nature of the dielectric material used in the RCP buildup, these inductors can be designed and made to be very accurate and with high Q values >50 .

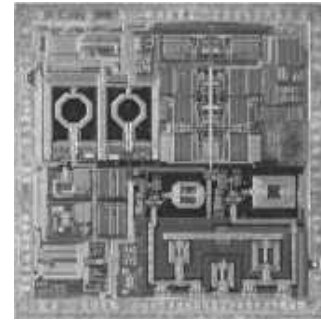
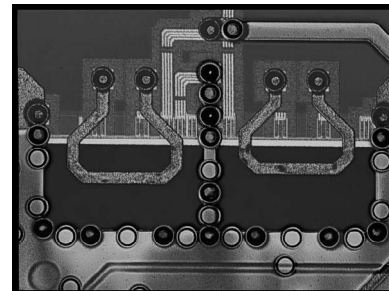


Figure 12. RCP test vehicle showing various structures including inductors of Q ~ 100.

This capability enables circuits such as harmonic filters, multi-layer inductors, and VCO's to be integrated into the package during the fabrication process. In addition to building component elements such as these, passive peripheral components such as chip capacitors and resistors can be embedded at multiple levels within the package. This reduces the number of external components required for a system level design. This capability is critical for enabling the integration of functionality into small, compact converged wireless and portable products.

Figure 13. VCO inductors built in RCP M1 Cu layer using



M3 Cu layer for ground (not shown).

Because of the dense routing and 3D capabilities, the RCP technology enables very small and highly integrated, innovations such as the example shown in Figure 14. This fully integrated Radio-in-Package (RiP) in effect replaces the electronics of an entire cell phone with one integrated package-like module. This high level of functional system integration enables new form factors for wireless applications such as a self-contained cell phone in a headset. Functional integration at the package level is a key enabler of this technology. RCP assembled packages can be easily combined in applications using non-RCP assembled packages. Existing packaging technologies can be integrated with RCP packages ensuring the best approach for any application. Further, this technology enables the convergence of multiple wireless or portable applications into a single module solution and in doing so, will create new markets for wireless products.

As illustrated in Figure 14, the RCP system integration process for RiP takes memory, RF and PA modules, baseband or applications processors and power management components and integrates them into a single chip. All “sub-

assemblies” are fully tested using traditional, non-integrated methodologies and using conventional lowest cost test (ATE) platforms. Shown here is an RCP system integration of a GSM-EDGE radio for cellular application. Known as a Radio-in-Package, this fully integrated system solution is physically the size of a US postage stamp – 18x20mm – and includes a 32MB NOR FLASH and 8MB PSRAM embedded in the “memory base”. Other integrated peripheral components include two crystals, a quad-band saw filter, and 26 chip capacitors.

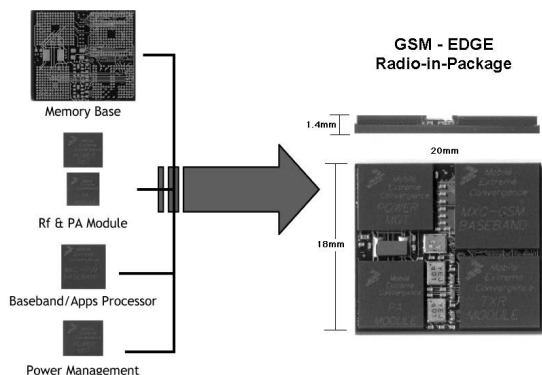


Figure 14. Fully integrated GSM-EDGE radio using RCP packaging technology

Evaluation of this system using a Rohde & Schwarz CMU200 revealed significant improvement in the RF performance of the radio. Specifically, when the transceiver output was monitored, it was found that the signal modulation was centered and evenly distributed for each of the GSM qual band frequency ranges. The radio design required no modification and no additional tuning was required to optimize the RF operation. The expected output of the transceiver was 27 to 30dBm. The measured results showed 32dBm or ~2-Watts. This represents a significant improvement and is attributed to the short interconnect routing and dielectric material used in the RCP process. (Figures 15 - 18)

Conclusion

Mobile devices are converging in both functionality and size. OEM manufacturers are seeking ways to increase the functionality of their products while reducing their size. Semiconductor suppliers are under intense pressure to increase the functional integration of the IC's, provide integrated system solutions, and reduce the size and cost of their solutions. Traditional packaging technologies will not always provide a solution that satisfies these converging needs. SoC, SiP, PiP, and PoP all provide varying degrees of functional and system integration but are limited by conventional substrate design and manufacturing capabilities as well as traditional interconnect technologies such as wire bond and flip chip.

RCP technology has the potential to make ICs smaller and more cost-effective, and enable a tremendous amount of system integration while maintaining minimal package size. Beyond providing smaller device packaging solutions, RCP

will enable the flexibility OEM manufacturers require for converging, innovating, and differentiating new mobile devices. Unlike conventional packaging technologies, RCP assembled products utilize the packaging as an integral part of the system solution. This convergence of IC packaging and IC functionality enabled by RCP technology will result in new innovations that are smaller, provide more flexibility, and achieve higher levels of integration than available with conventional IC packaging technologies.

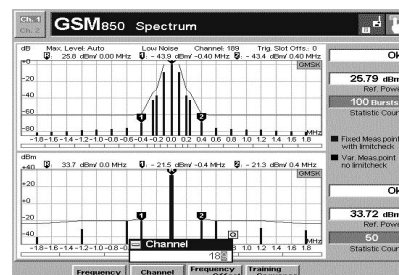


Figure 15. 850MHz modulation output of transceiver

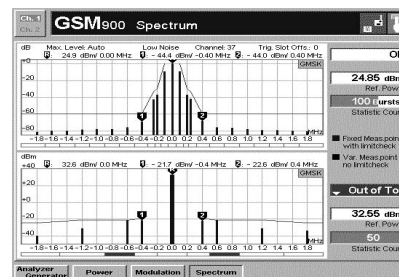


Figure 16. 900MHz modulation output of transceiver

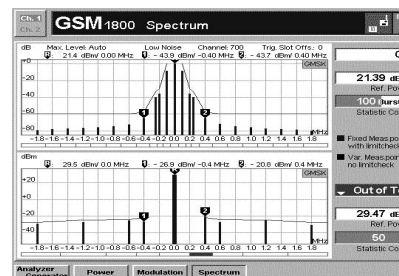


Figure 17. 1800MHz modulation output of transceiver

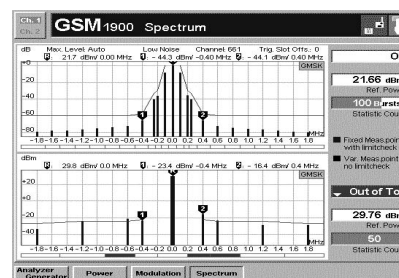


Figure 18. 1900MHz modulation output of transceiver