

From Thin Cores to Outer Layers: Filling through Holes and Blind Micro Vias with Copper by Reverse Pulse Plating

Stephen Kenny and Bernd Roelfs

Atotech Germany

Erasmusstr. 20, 10553 Berlin

stephen.kenny@atotech.com; bernd.roelfs@atotech.com

Abstract

This paper presents new advancements in copper electroplating technology for both Blind Micro Vias and Through Holes. Processes and manufacturing technology are described as well as current limitations and requirements. As a highlight the complete filling of through holes with electroplated copper by Reversed Pulse Plating, RPP, is described. Both Blind Micro Via and Through Hole filling using this technology are already targeted for production at HDI and also at the packaging level.

The basis of the latest advancements has been the development of the so called SuperFilling™ process. SuperFilling™ combines the electrolytic reverse pulse deposition of copper into specific structures together with the simultaneous etching of copper from the substrate bulk surface in a continuous panel plating step. This combination reduces the amount of overplated Cu by up to 50% compared to conventional copper deposition processes for HDI fine line applications. The SuperFilling™ mechanism as well as manufacturing requirements and production supervision tools such as online analysis are described in detail.

The latest development, through hole filling by RPP, offers a viable alternative to the standard paste plugging for core processing in substrate manufacturing. Current core manufacturing requires a paste plugging process for through holes so that subsequent build up layers can be produced by sequential lamination, the flat core surface is essential for stacked via and also via in pad technology.

This paste plugging process requires additional process steps, each of which has its own limitations and contributes to the overall cost. Filling the core through vias by electroplating can eliminate the plugging process and significantly reduces the number of overall process steps which will also reduce costs. Moreover, it offers certain advantages such as potentially higher reliability in accelerated aging tests and an improved thermal management as the thermal conductivity of a completely copper filled through via is significantly higher than a paste plugged through via.

First manufacturing experiences with the Through Hole filling technology are presented along with a discussion of its manufacturing prerequisites and limitations.

Introduction

The manufacturing process for substrate cores requires production of a planar surface which is subsequently used as the starting point for the high-density build-up layers. The core is normally mechanically drilled to produce the required through-via connections which are then metalized and plugged with a thermally cured resin material. There is a current tendency for reduced core thickness and this has implications for yield, quality and ultimately for cost for

product from the complete process. The plugging process itself is relatively labor-intensive and requires, as part of the sequence, a mechanical abrading or brushing process after resin cure, which can cause problems of dimensional stability, particularly for substrate cores less than 100µm thick. The plugging resin itself has disadvantages in that it is a high-solid content material, which has a different coefficient of thermal expansion (CTE) to that of the surrounding material, including the copper metal in the via and also to that of the dielectric of the core itself, typically a glass-reinforced resin material.

The disadvantages of the existing plugging process can be eliminated by using pure copper to produce the planar surface. For the next-generation process, copper is deposited into the through via as an integral part of the metallization process. The drilled dielectric is made conductive and a thin layer of copper metal is deposited to give a seed layer for the copper deposition process. The through-vias are then completely filled by a modified electrolytic copper deposition process, which can be accomplished in a single, fully automatic continuous processing line.

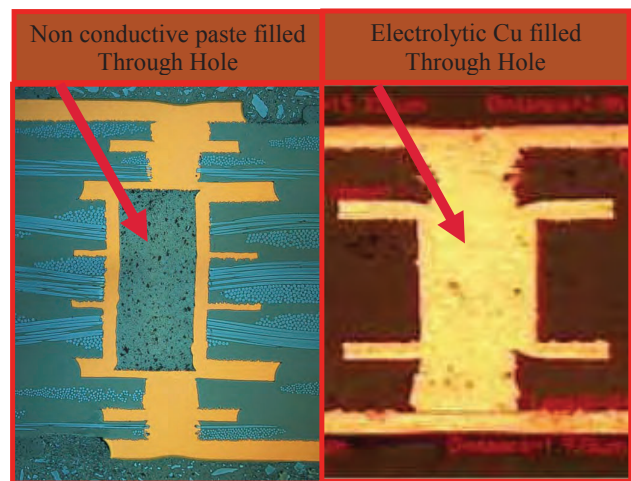


Fig. 1 X-sections showing a paste plugged through via in a core (left) and an electrolytically Cu filled through via (right), both with blind micro via layers on top (Via in pad).

The use of pure copper has obvious advantages in that its thermal characteristics are significantly better than any type of resin material available. This fact can give more design options to utilize the improved thermal transfer capability of vias in a substrate than are currently available. The CTE of the copper-filled core is dependant only on the copper metal and the glass-supported resin of the drilled dielectric. The copper

structures in the subsequent layers may be positioned directly above the copper-filled through-vias with no reliability implications. In fact, the conductive path within the substrate may be designed to utilize the more direct and parallel connection from one side of the substrate to the other.

Table 1 Process flow for paste plugging and Cu plugging for through holes

	Conventional Process (Paste)	Electrolytic Process
1	Through hole drilling	Through hole drilling
2	PTH (Hole metallization)	PTH (Hole metallization)
3	Panel plate 18-25 μm	Panel plate 3 μm
4	Resin plug	Electrolytic through hole fill (12-20 μm Cu)
5	Cure	Dry film
6	Grind / Brush	-
7	Resin metallization	-
8	Panel plate 18-25 μm	-
9	Dry film	-

Via hole plugging [1] as a process is used to produce a planar surface which enables subsequent sequential lamination for production of build up structures, the planar surface is particularly important to ensure uniform dielectric spacing between circuit layers critical for controlled impedance in high frequency applications.

The standard process is to use a plugging paste which is applied by methods such as stencil printing or roller coating. On top of the plugging paste there will either be the next resin layer which may be glass reinforced, or a plated copper layer. This copper surface may be used to allow production of staggered or stacked blind micro vias which are conformably copper plated or copper filled depending on the application requirements. An example for an HDI board with a paste plugged core is given in Fig. 1 (left) as well as an example for a copper filled core. Both examples show also filled BMVs directly on top of the through hole (Via in pad technology). This example illustrates well the technique of blind micro via filling to ensure void free sequential lamination. The direct positioning of the BMV on the core through hole will save space in the substrate design.

Blind Micro Via Filling and SUPERFILLING™

The need for finer lines and higher reliability has driven the development for filled BMVs. The main drivers of the BMV filling technology were IC substrate manufacturers who are very sensitive on reducing real estate on their product and apply the stacked via technology which is based on perfectly filled Blind Micro vias of small dimensions (60 μm ×40 μm). HDI manufacturers have followed this approach and tried to use the filling technology for their application. Unfortunately, HDI manufacturing requires filling of much larger BMVs (e.g. 125 μm ×75 μm) at a significantly higher production throughput. Where IC substrates are produced at about 1-1.5

ASD, HDI boards are often produced with 5-10 ASD. This requires a significantly different production scenario. The key for success at such high current densities is a perfect distribution of copper, since the BMV filling is much more sensitive to copper thickness variations than normal conformal plating applications. Not only the distribution within the panel but also the panel to panel and batch to batch distribution needs to be optimized. For this very specific application we designed a completely horizontal conveyORIZED plating line comprising of a desmear process, initial metallization of the surface and hole by electroless copper and an electrolytic copper plating step. A conveyORIZED approach is extremely beneficial as the panel to panel variation in such a system is minimized. For perfect distribution within a panel both the e'less and the electrolytic copper deposition was optimized.

The first step was to improve the distribution the e'less deposition of copper. It was necessary to improve the amount of copper in a BMV since drilling through a glass fiber reinforced material for HDI often results in a non regular BMV shape. Fig. 2 depicts such a non optimal BMV shape but the newly developed e'less process Printoganth U Plus covers every part of the hole. To make this visible the board was run 10 times through a uniplate line otherwise the e'less layer would be too thin for a microscopic evaluation. This development required a variety of changes in the electrolyte and system set up.

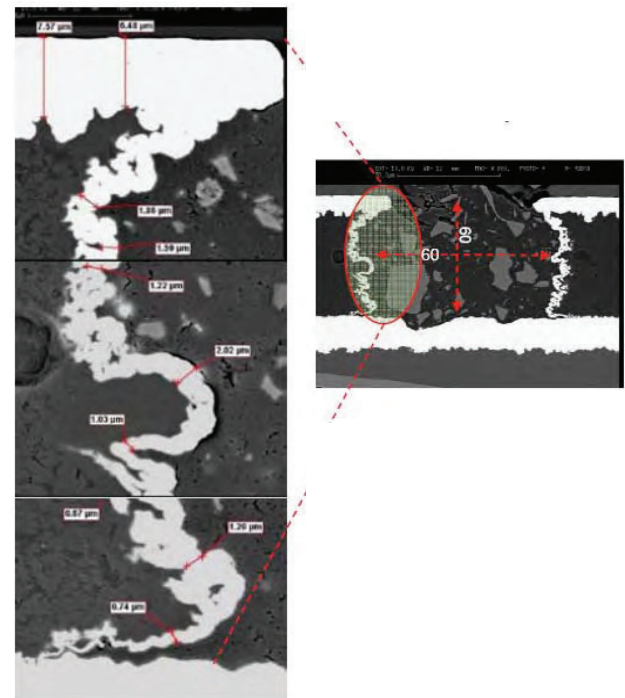


Fig. 2 BMV after exposure to the latest eless copper version Printoganth U Plus. Coverage is also achieved under wedges.

The biggest advancement in the subsequent electrolytic copper deposition was the development of the so called SUPERFILLING™ process for our Impulse system. The Impulse system is based on a combination of inert anodes and

reverse pulse plating. The process is in fact a combination of a simultaneous electrolytic copper plating and copper etching in one electrolyte. This is realised by using an electrolyte which contains copper and $\text{Fe}^{2+/3+}$ at the same time.

Originally, the Fe redox system was introduced as a replenishment aid [2] for copper ions and as reaction partner for the inert anodes instead of additives and water. It reduces the consumption of the additives significantly. Moreover, it increased the life time of the expensive Iridium oxide coverage for such anodes since anodes are operating at the lower oxidative potential of the Fe redox couple. But the Fe^{3+} can be further used to minimize the amount of surface copper which is the basic idea behind the SUPERFILLING™ approach.

The principle of this SUPERFILLING™ process is shown in Fig. 3.

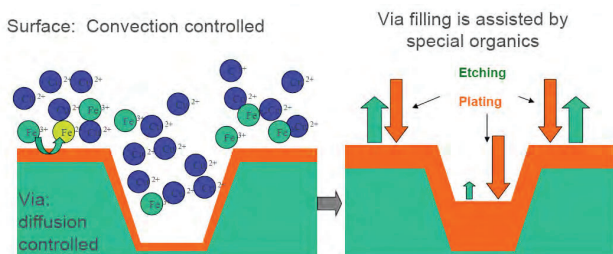
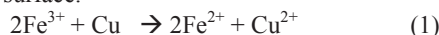


Fig. 3 Showing the principle of simultaneous plating and etching with preferred surface etching

This illustrates well the difference between a surface and the bottom of the BMV. Transport of ions and additives is for the surface mainly convection controlled due to the extremely high flow rate whereas a BMV behaves completely differently. The transport is diffusion controlled and as such is orders of magnitude slower. This leads to a concentration difference of Fe^{3+} ions between surface and BMV bottom. The Fe^{3+} ions are able to etch by Equation 1 preferentially from the surface.



By running this system with extremely high Fe^{3+} concentrations of 4-6g/l it is possible to reduce the amount of surface copper by up to 50% compared to a conventional non redox system.

Through Hole Filling with Electrolytic Copper-Mechanism

In the development work for the blind micro via filling SUPERFILLING™ process it was seen in early experiments that through vias were excessively plated at the centre of the hole. This result is normal when reverse pulse plating is used however the extent of the plating thickness in the hole centre was a surprise, as can be seen in Fig. 4.

How is such an exaggerated plating possible? The answer to the questions lies in the mechanism of the reverse pulse plating and its influence on the electrolyte additives. A copper electrolyte usually consists (not only) of a well balanced mixture of suppressing and accelerating additives. The suppressing additives (carriers and levellers) slow down the

copper deposition whereas the accelerating additives (brighteners) act as a catalyst for the copper deposit.

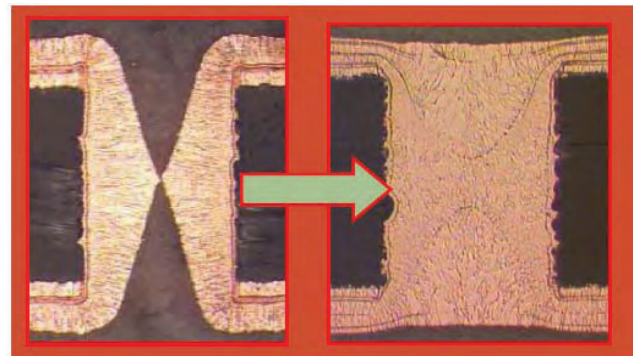


Fig. 4 Two step process for through hole filling. 1st X plating with extreme reverse pulse and 2nd BMV filling

The application of the reversed pulse now interferes with the distribution of these additives in a hole and on the surface. The reverse pulse is able to modify the concentration equilibrium in a hole and on the surface in such a way that the accelerating catalyst concentrates in the middle of a hole and is depleted from the surface. This is due to the fact that under reverse (=anodic) pulse conditions the catalyst is desorbing together with a small amount of copper. Since the concentration of the brightener is relatively small it takes a while to re-adsorb again and this catalyst is now partly missing for the subsequent cathodic pulse. The hole is compared to the surface electrically shielded so that the reverse pulse does not reach its maximum strength especially in the middle of the hole. Here, the desorption of the catalyst is incomplete and it can react immediately after switching the pulse to cathodic values. As a consequence the deposition speed in the middle of the hole is increasing compared to the surface. This mechanism is depicted in Fig. 5.

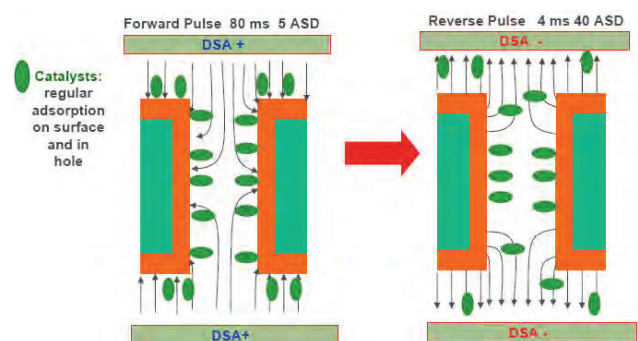


Fig. 5 Schematic model for the exaggerated X-plating. Left: Cathodic pulse with regular distribution of copper deposition catalyst. On right: Depletion of catalyst from surface during reverse anodic pulse (DSA= dimensionally stable anodes)

Through Hole Filling-History and Outlook

When we started with our development in 2005 we did not see an immediate benefit of this technology due to the fact that a considerable amount of surface copper was necessary to fill through vias. In fact, more than 50µm panel plated copper

was necessary to fill a 100 μm thin panel with 100 μm diameter holes (Fig. 6). Together with the copper laminate of 17 μm it was not possible to apply this technology for HDI boards or IC substrates. HDI boards were in general based on sub 75 μm and now on < 50 μm structures. These boards undergo an etching step for the final circuitization. The accessible fine line resolution is, by rule of thumb, about twice that of the overall copper thickness. To enter the 50 μm lines and space arena it was necessary to reduce the amount of plated copper significantly down to about 20 μm and work with thinner laminated copper (e.g. 3 μm copper).

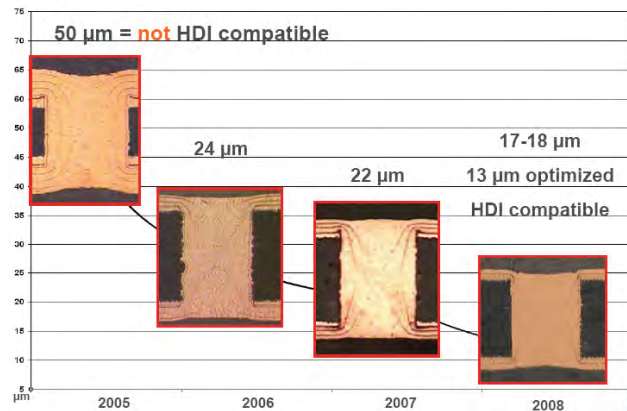


Fig. 6 Development of the amount of necessary surface copper to fill a 100 μm hole in a 100 μm thin panel for TH filling capability

There is also the possibility to reduce plated copper thickness by subsequent etching or even mechanically abrading to reach the thickness tolerances for HDI however this option was discarded during development as any copper removal process adds processing steps, wastes raw material and increases cost. Thus the only option was to optimize both equipment and the plating process.

We constantly improved the performance in the last years and as a result of our development work we decreased the amount of plated copper down to the imaginary 20 μm border line for which HDI with this technology becomes feasible.

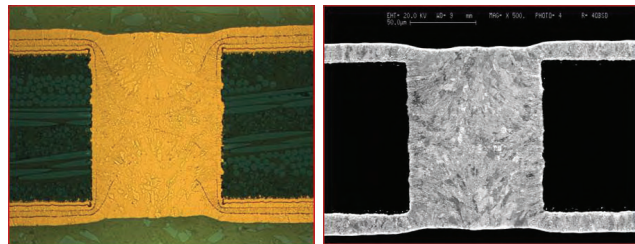


Fig 7 Showing an etched X-section and an SEM micrograph of a copper filled through hole plated with the latest technology

We not only decreased the amount copper but also had to improve the crystal structure and physical properties of the deposit to meet the IPC norms. In Fig. 4 especially on the left picture one can see rather orientated copper (columnar growth), which may arouse concerns about the reliability.

Thus, a specially developed electrolyte system has been developed and optimized for this special application.

Fig. 7 shows the copper deposit of the present electrolyte. Both the etched and the SEM micrograph show the normal polygonal copper structure as we know it from numerous investigations. A variety of measurements on ductility, tensile strength and differential scanning calorimetry (DSC) showed that this deposit is comparable to the normal HDI copper quality and withstands the usual requirements.

Two significant approaches made it possible to reduce the amount of copper so significantly: 1st the optimization of aforementioned SuperFillingTM process and 2nd the development of new rectification system. This new system allows improvement in especially the X- plating performance and reduces the amount of plated copper drastically to form a bridge between the hole wall sides.

We are constantly working to further reduce the amount of plated copper so that this panel plate process will keep pace with the requirements of future HDI technology.

Process Advantages for copper through hole filling

Numerous advantages of copper filled through holes can be described.

Not the least should be the expected increase in reliability. Reliability issues in accelerated aging test occur usually when the CTEs of adherent materials are very different. This is in fact the case for every PCB. The CTE of copper is approx. 17ppm/K and the CTE of typical FR4 base material is approx. 110ppm/K. The CTE of plugging pastes for the standard through hole filling process is at 30-40ppm/K in between that of the other materials. This means that a copper barrel in a through hole comes under stress from outside and inside the barrel. This often results in corner and barrel cracks

Such a stress for a completely copper filled through hole can only be induced from outside but a thicker copper barrel is a mechanically strengthened system due to the superior mechanical properties of copper layer

Another benefit of copper filled through holes could be the application for thermal vias. Copper has obvious advantages for thermal vias due to its high thermal conductivity; this is at 360 W/m K much higher than that of any plugging material. Normal plugging materials have thermal conductivity values of about 1W/m K, specially developed high thermal conductivity paste up to 8W/m K. Compared to these pastes the thermal conductivity of copper is about 40-50 times better. Simple calculations show that more than 90-99% of the heat transfer is still carried by the copper barrel depending on which paste is used for plugging. This effectively reduces the application of such paste plugged thermal vias. A comparison of the capability can be easily done by the introduction of a thermal resistance concept [3]. The through hole can be seen as thermally conductive wire for which the thermal resistance " R_{th} " can be described by,

$$R_{th} = d[\mu\text{m}] / (\lambda [\text{W/mK}] \cdot A[\text{m}^2])$$

In the formula "d" is the length of the heat conductor, in this case the thickness of the substrate and λ is the thermal conductivity of in this case either copper or the plugging material. A is the cross sectional area of the heat conductor, the plated copper in the barrel of the hole or the plugging material. The theoretical calculation for a via diameter of

120 μ m and panel thickness 150 μ m shows that the thermal characteristics of a plated through hole are determined mostly by the plated copper thickness in the barrel of the hole. To improve the thermal performance it is more effective to increase the plated copper thickness in a barrel than to use a plugging material. The best result from the theoretical calculation was found, as could be expected by simulating a fully copper filled barrel.

Table 2 Comparison of heat transfer capabilities

Through via 20 μ m copper	Through via 30 μ m copper	Through via 20 μ m copper plugged	Through via copper filled
84 K/W	62 K/W	80 K/W	47 K/W

Also due to the increased thermal and electrical characteristics of a solid copper core the number of thermal vias required may be reduced whilst maintaining an equivalent thermal capability. This again can free up surface which could be required for circuitry so allowing further miniaturization. Build up layers may be positioned directly above the filled core with no loss in reliability and this design gives the shortest and most direct circuit path from one side of a substrate to the other.

Limitations of the Through Hole filling technology:

So far this technology can be applied to thin cores only ranging from 50 μ m to max. 400 μ m. For thicker cores the aspect ratio becomes too difficult so that small voids in the holes may be left. It is still unclear to which extent these voids are critical for the accelerated aging test such as TCT and IST but this will be the topic for the future.

As the next step in our development we are trying to apply this technology to a pattern plating sequence. Pattern plating is currently process of record for IC substrates with lines and spaces dimensions of below 20 μ m. The IC substrate manufacturer are widely using the via in pad technology and would benefit significantly from the copper plugging process. First tests with the existing system showed promising results. The adoption of the copper through hole filling technology for a pattern plating process requires both changes in the plating equipment and electrolyte system. The fine line structure of the pattern layout is very sensitive to mechanical damages and requires a touchless transport system. Moreover, modifications in the electrolyte system are necessary to generate a rectangular line shape.

Production experience

SUPERFILLINGTM technology for filling BMVs has been recently adapted and can be seen as state of the art for HDI manufacturing. It is now part of the reliable production sequence for several mobile phone suppliers.

Qualification of the Inpulse 2THF through hole filling process has been successfully passed at a Taiwanese IC substrate manufacturer for 0.1mm thin cores with up 500 k holes per board. These boards with areas of clustered and isolated through holes have been successfully plated with 20 μ m copper on 3 μ m copper laminate.

Summary

This paper describes the progress in filling both BMV and through holes by electrolytic copper. Whereas BMV filling technology has been widely adapted by the HDI manufacturer, TH filling by copper is a new technology and is still waiting for its introduction into mass manufacturing. We have shown that through hole filling can be an interesting alternative for thin cores to the standard paste plugging process as it simplifies the production sequence and reduces significantly the number of production steps. This in turn can minimize costs for the manufacturing process. Several other benefits such as increased thermal conductivity and higher stress resistance are described. Qualification for IC substrates has been successfully passed and the application for the HDI segment with its thicker cores will be the next task. So far this technology is limited to thin cores up to 400mm only and the process is a pure panel plating process. The amount of surface copper can be limited to below 20 μ m which makes this process feasible for fine line application below 50 μ m.

The development of TH filling in a pattern plating process is under way to apply this technology for ultra fine line application.

References

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