

High-performance Flip-Chip BGA Technology Based on Thin-core and Coreless Package Substrate

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Abstract

A new organic build-up substrate packaging technology was developed in Fujitsu for high-end servers, where lower V-G impedance on substrate and thermal resistance are realized by applying metallic thermal injection materials. In the present paper, two important accomplishments in assembling process, eliminating voids with metallic thermal injection and controlling substrate flatness on mounting large LSIs, are investigated, and evaluated.

1. Introduction

With a continuous increment of power consumption for high performance LSIs of high-end servers, the LSI package requires for higher cooling capacity, better electric capacity and lower thermal resistance, while comprised of lead-free materials as well. In dealing with these issues, a low thermal resistance package with low electric inductance was developed in Fujitsu, advanced in three major tapped technologies of a large-scale LSI mounting process, a low thermal resistance joint structure and assembly process, and a low electric inductance organic SMD packaging technology.

High efficient and low inductance capacitors are used to suppress a high frequency noise in power voltage of the processor. By arranging the capacitors on an opposite side of the LSI, it shows an effective way to lower tremendously the inductance between the LSI and capacitors.

Moreover, lowering the power ground inductance of the substrate is necessitated for an effective operation of the low inductance capacitor, which can be achieved by effectively reducing the via pitch, while thinning the substrate thickness. Based on an organic build-up substrate technology, two advanced package substrates, the thin-core and coreless substrates, respectively, with low V-G loop inductances are successfully developed in Fujitsu, cooperated with Fujitsu Interconnect Technologies.

Meanwhile, for achieving high cooling performance, the packaging technology was also evaluated with applying a new metallic thermal interface material in between the LSI and attached heat spreader. Though the thin-core and coreless substrates have the advantages of less expensive in cost and high density interconnections, they generally have relative high thermal expansion properties. Therefore, lowering thermal stresses among the LSI solder bumps, as well as that at the thermal interface between the LSI and heat spreader are extremely important in the technology development.

Details are explained, and evaluated in the following sections.

2. Package and substrate structure

The package structure is shown in Fig.1, with a size of 42.5mm in square, and total 908 EIO (BGA)s. BGA-material

is Sn-Ag-Cu. Chip size is 20x20mm, number of jointed bump is 6900 by Sn-AG solder bump with 200 μ m pitch. Its is filled by underfill. The material of thermal joint is In-Ag.

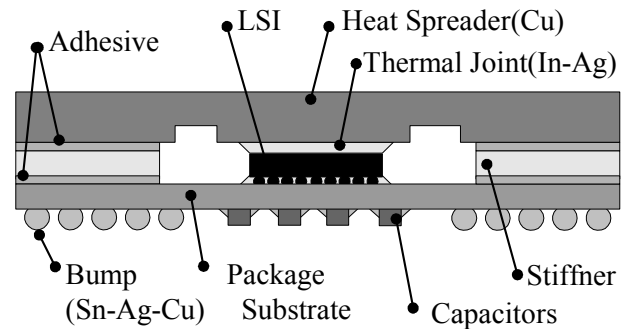


Fig.1 Package structure

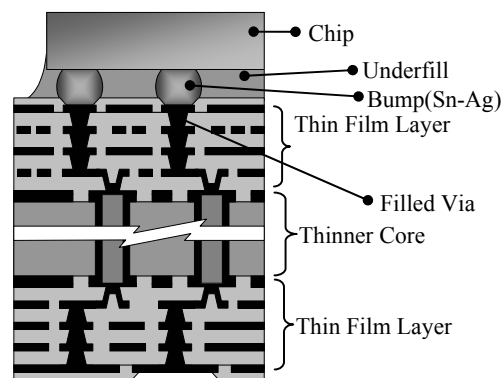


Fig.2-1 Thin-core substrate structure

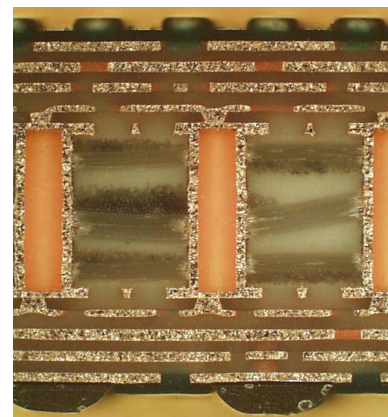


Fig.2-2 Thin-core substrate cross-section

Fig.2 shows thin-core structure of thin film build up layers.

The substrate is comprised of five thin-film layers on each side of a 2-layer core (5-2-5). The minimum line/space is 15/15 microns. The via land and hole sizes are 100 and 50 microns, respectively. Also, it is connected straightly with a filled via from the surface to fourth layer.

Sliming core material (0.6 to 0.4mm) and narrowing pitch of core via (0.635 to 0.400mm) lowers the loop inductance from 3.5pH to 0.89pH.

Fig.3 shows a structure of the coreless substrate. Thin film substrate specification is the same as that of the thin-core substrate. But this substrate do not have core layer by special producing process.

The structure made it possible for the thin substrate (from 1.1 to 0.35mm) and narrow via pitch to 0.2mm, accordingly the loop inductance was improved to 0.45pH dramatically.

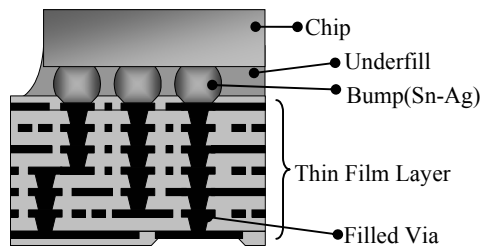


Fig.3-1 Coreless substrate structure

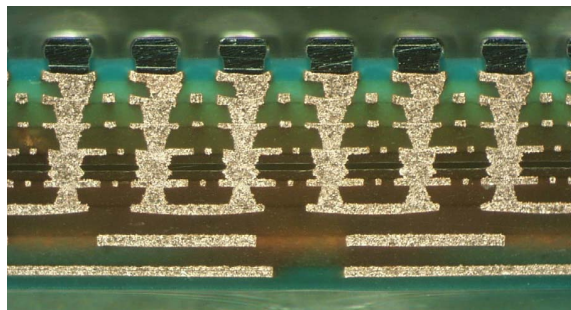


Fig 3-2 Coreless substrate cross-section

3. Major targets on packaing

Targets on package sliming were indicated as follow;

- 1) Warpage in LSI area is 32micron or less.
- 2) Warpage of package after assembly components is 150micron or less.
- 3) Heat-resistance in large LSI package is 0.08degreeC/W or less.
- 4) Eliminating lead from packaging components completely.

4. Warpage of package substrate and package

4.1 Warpage comparison of the package substrates

Fig.4 shows the comparison of bending degree between thin core and coreless substrate. As keeping LSI assembly yield rate requires board bending degree equivalent to established one, highly stiff core material achieved it. On the other hand, significant decline of bending is essential for coreless substrate.

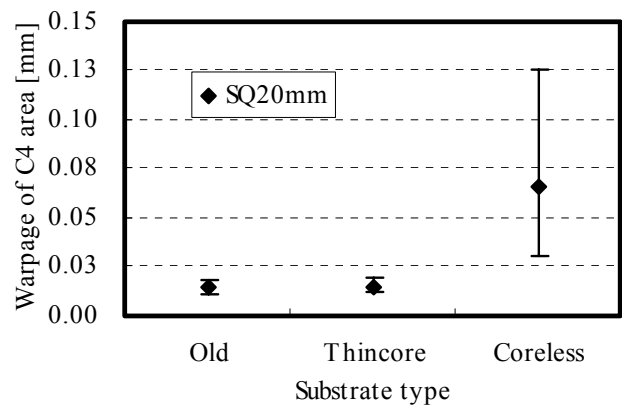


Fig.4 Substrate type and warpage

4.2 Stiffner assembly process optimization

Comparing to copper or SUS, usual stiffner material, whose expansion coefficient are equivalent, coreless substrate has higher level, 25ppm/K or more. Under assembling temperature, stiffner prevented coreless substrate shrinking and bending degree was suppressed. On the contrary, over the assembling temperature substrate bends caused by expansion coefficient difference, which showed that assembling stiffner at higher temperature is very efficient for inhibiting to bend.

To develop assembling material of which curing temperature is high and to mount materials within the welding force which do not influence on thermal expansion of substrate led the optimized stiffner assembling. The result is referred to Fig.5.

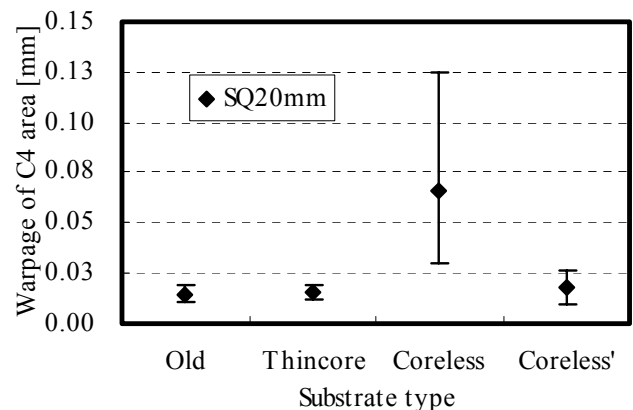


Fig.5 Substrate type and warpage

To develop assembling material of which curing temperature is high and to mount materials within the welding force which do not influence on thermal expansion of substrate led the optimized stiffner assembling. The result is referred to Fig.5.

4.3 Package warpage controlling by LSI thickness optimization

Since bending degree of coreless substrate increased after assembling LSI, we studied correlation between substrate type/bending degree and LSI thickness. The search result (Fig.6) made it possible to achieve the coreless substrate

bending equivalent to general package by choosing appropriate LSI thickness.

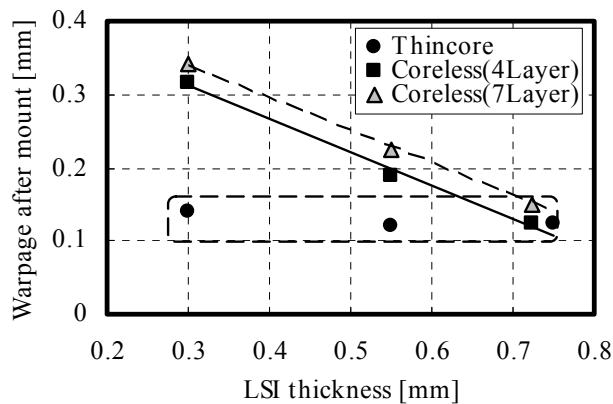


Fig.6 Relationship between warpage after LSI mounting and LSI thickness

5. Package cooling design

5.1 Consideration for thermal injection part

0.08degreeC/W of package heat resistance requires to keep heat resistance between LSI and heat spreader under 0.04degreeC/W, which means thermal conduction of metal contact between them should be high. That connection should be without void because even small void causes heat spots. Void comes from air trap where solder partially flow surface tension flows some solder since the temperature exceeds solder melting point before metal diffusion. Also we consider high thermal stress caused by difference of heat expansion rates on connection with LSI though copper is appropriated for heat spreader material in terms of thermal conduct and cost.

5.2 Lead free material choosing

There were two reasons why In-Ag solder material was selected among typical lead-free solder material, Sn-Ag/ Sn-Bi/ In-Sn/ In-Ag. One is that In-Ag solder's range from liquidus to solidus temperature is wider in which solder is not completely melted with metal diffusion and rare airtrapping. The other is that it is very soft with low melting point and flexible against thermal stress.

Table.1 shows thermal resistance readings of representative metal materials and Fig.7 correlation between metal contact thickness and thermal resistance.

[Table.1.Thermal Interface Material and thermal resistance]

material	liquidus temperature degree-C	solidus temperature degree-C	Heat resistance 0.2mmt degree-C/W
In-10Ag	231	141	0.0383
In-48Sn	118		0.0696
Sn-20Pb	199	183	0.0543

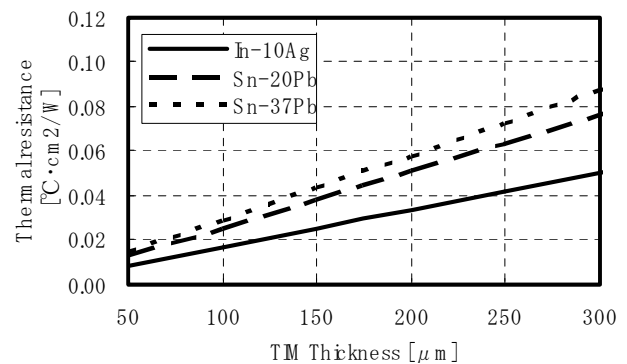


Fig.7 Relation between TIM thickness and thermal resistance

5.3 Optimized In-Ag solder composition for no void contact

In-Ag eutectic solder composition is In-3Ag of which the liquidus temperature rises as the concentration of Ag increases. The wider range from solidus to liquidus temperature metals diffuse at partially melting status in, the less void the contact has. Addition to that, stable wetting from over liquidus line temperature through package reflow (Max: 260C) favors the maximum liquidus temperature is 260C or less. Therefore the ideal concentration of Ag is 10wt%. Fig.8 shows the result of experiment; wetting area with varying from 3Ag to 15Ag. As X-ray picture of Fig.9, it was possible to reduce air bubble to almost nil.

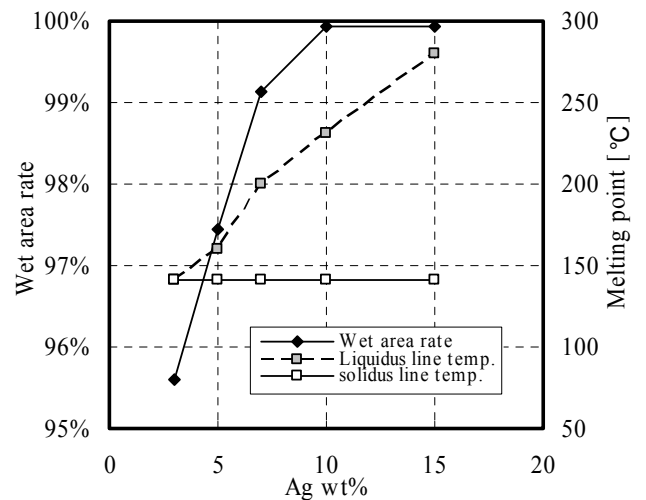


Fig.8 Relation between Ag density and wet area

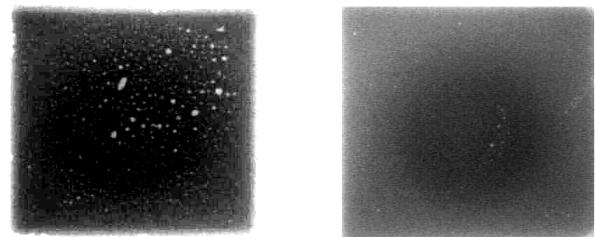


Fig.9 Void in metallic joint part (Xray)

5.4 Optimization of metal contact through thermal stress analysis

For another issue of thermal stress, we demonstrated stress simulation based on package assembling process flow, using ABAQUSV6.4.4 general nonlinear finite element analysis tool. Fig.10 shows stress distribution at TIM and Fig.11 a photo of cracks at external area caused by thermal shock test.

The fact that the position of crack through thermal shock test was correspondent to the simulation result of Fig.10 (rupture stress:3.8MPa) verified the validity of simulation.

For less stress with this structure, it is reasonable to thicken this metal contact. Then we tried to optimize the contact thickness figuring the tensile stress at each thickness by means of simulations.

The result graph is displayed as Fig.12; vertical axis: tensile stress, horizontal, axis: center-to-corner length of the model.

The metal contact needs 460 μ m in thickness to hold the LSI-heat spreader thermal resistance up to 0.08C/W (the reference of metal contact thickness is 200 μ m)

Then we confirmed the stress under the estimated rupture stress (3.8MPa) with metal contact 400 μ m or more

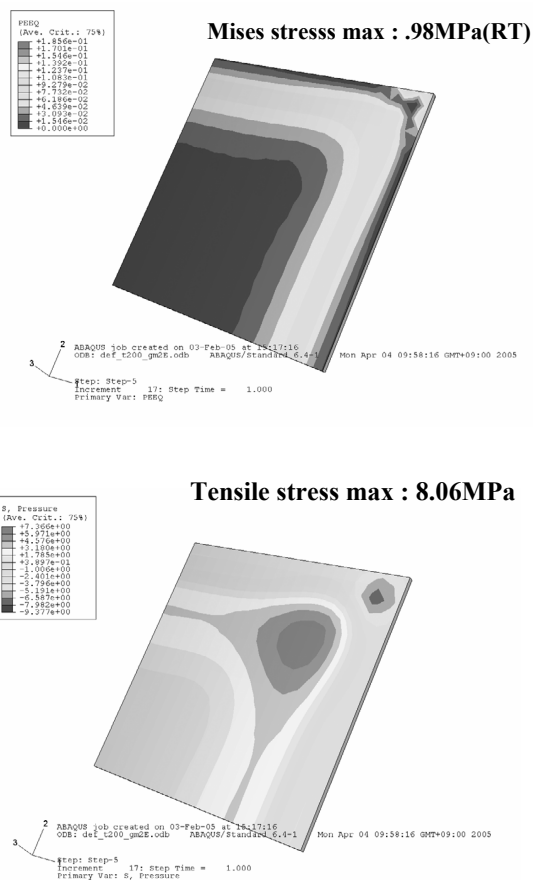


Fig.10 Mises stress /Compression stress of TIM

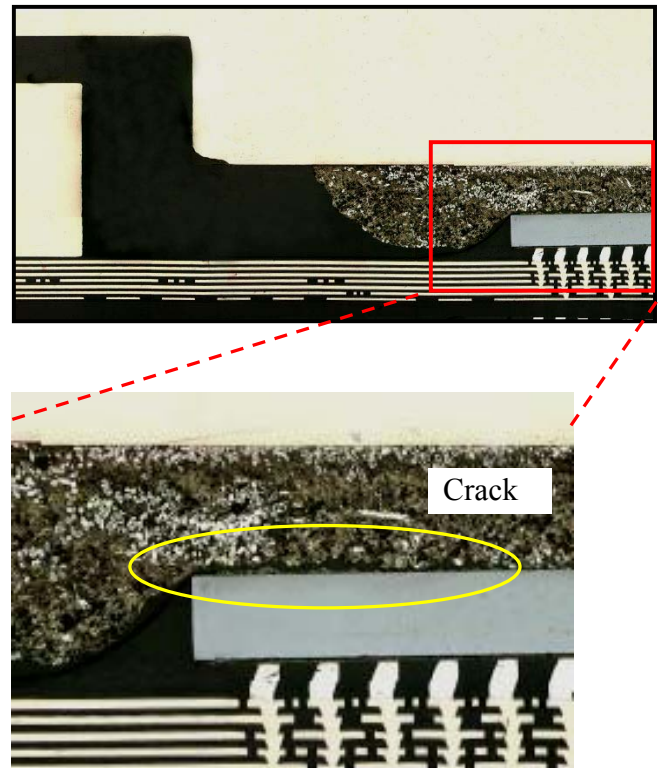


Fig.11 Crack after Thermal shock test

The result graph is displayed as Fig.12; vertical axis: tensile stress, horizontal, axis: center-to-corner length of the model.

The metal contact needs 460 μ m in thickness to hold the LSI-heat spreader thermal resistance up to 0.08C/W (the reference of metal contact thickness is 200 μ m)

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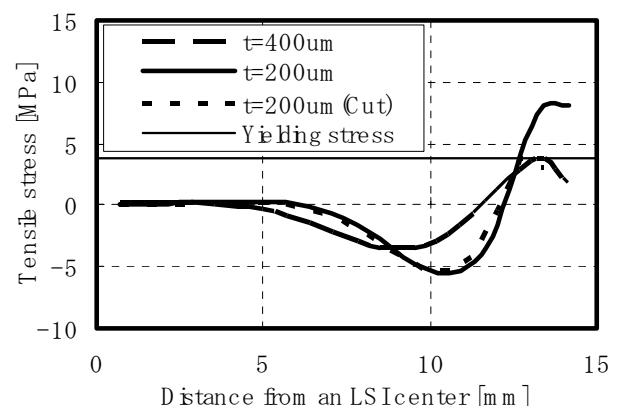


Fig.12 Relation between joint-thickness and tensile stress

6. Reliability assesment

At the reliability assessment, we confirmed the reliability of stand-alone package over 10 year's worth through thermal shock test and the heat-resistance as JEDEC Level 14.

Besides either LGA or BGA as packaging assembly form was verified to guarantee over 10 years through vibration shock test and thermal shock test.

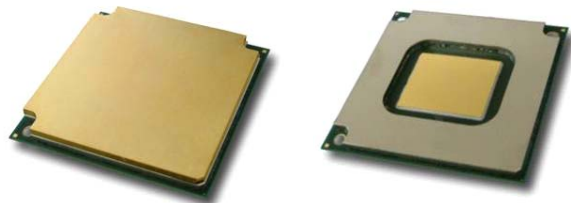
Table 2-1 Thin-core Package reliability test result

Test condition	Test Results
Heat resistance JEDEC J-STD-020C Level4	Reflow stress 255(C) Max. 5cycles pass
Thermal shock (Stand-alone Package)	-10/+100(C) 2,000cycles pass
Thermal shock (Test card mounted)	-10/+100(C) 2,000cycles pass

Table 2-2 Coreless Package reliability test result

Test condition	Test Results
Heat resistance JEDEC J-STD-020C Level4	Reflow stress 255(C) Max. 5cycles pass
Thermal shock (Stand-alone Package)	-10/+100(C) 2,000cycles pass
Thermal shock (Test card mounted)	-25/+125(C) 300cycles pass

7. Photograph of Packages



Conclusion

This study gave us the following conclusions and challenges, working on assembly issues like bending degree and lowering heat-resistance with lead-free materials, advancing on the course of low heat-resistance of thin core/coreless substrate lead free packaging.

1) For slim or super-slim substrate including core less structure, stiffer assembly material and appropriate process enabled the same assembling level as general organic substrate.

2) Metal joins between LSI and heat spreader for large LSI successfully decreased heat-resistance impressively to realize the inner heat resistance of package under 0.08degreeC/w.

3) All packages above were confirmed that the practical use of BGA assembly with lead-free condition.

Acknowledgments

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References

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