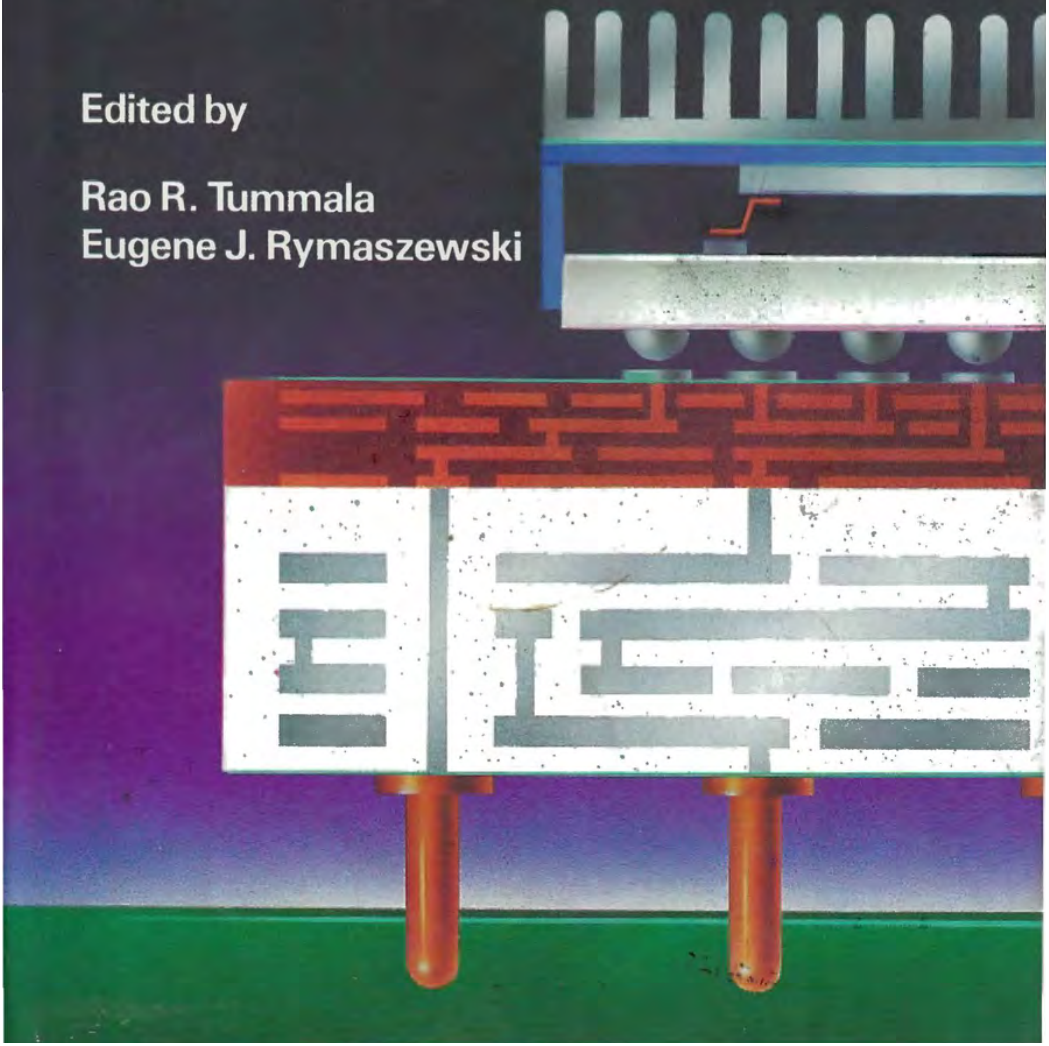
Microelectronics Packaging Handbook

Edited by

Rao R. Tummala
Eugene J. Rymaszewski



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Alan G. Klopfenstein

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FOREWORD

RALPH E. GOMORY

IBM SENIOR VICE-PRESIDENT, SCIENCE AND TECHNOLOGY

Far from being passive containers for microelectronic devices, the so-called "packages" in today's advanced computers pose at least as many engineering challenges as the chips that they interconnect, power, and cool. New packaging concepts often lead their developers into uncharted areas of science.

Ultimately, progress in packaging is likely to set the limits on how far computers can evolve. And yet, this technology has never captured the public imagination in the way that chips have. Worse, it has been largely overlooked by universities as a prime subject for teaching and research.

In part, this academic oversight stems from packaging's multidisciplinary nature. Packaging involves the solution of electrical, mechanical, and thermal problems; it requires understanding at the molecular level not only of silicon but of metals, ceramics, polymers, glass, and composites. In short,

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it is poorly matched to the traditional separation of university disciplines. Another roadblock has been the lack of a comprehensive book dealing adequately with state of the art packaging design and modern industry requirements.

To meet the latter need, IBM Fellow Rao Tummala and Eugene Rymaszewski, Manager of Strategic Analysis, have assembled an outstanding team of packaging practitioners from across the IBM Corporation. Together, they have produced in the **Microelectronics Packaging Handbook** an unmatched book both the industry and university need. It is equally appropriate as an introduction to the field for those just entering it, and as an up-to-date reference for those already engaged in packaging design and development.

No longer can electronic packaging be regarded as an engineering commodity. Industry is putting tremendous resources into both packaging for large-scale computers, where speed is the driving factor, and packaging for consumer electronics, which strives primarily for low cost per interconnection. In each case, further evolution is required if we are to capitalize on the continuing advances in very large-scale integrated circuits.

Microelectronics Packaging Handbook is offered in much the same spirit as the recent competition held by IBM for $25 million in material and processing sciences research grants and equipment (which drew more than 200 proposals for the 12 available grants). I join the authors in hoping that this book will help focus the attention of outstanding faculty and students, as well as working engineers and scientists, on the complex packaging challenges which must be solved.

PREFACE

This book reflects a need based on an ever-increasing realization by the microelectronics community that while the semiconductors continue to be improved upon relentlessly for performance, cost, and reliability, it is the packaging of these microelectronic devices that may limit the systems performance. In response to this need, the academic community began to ask its industrial counterparts what packaging is all about, and what scientific and technological areas should be pursued in collaboration with industry. As a result of these discussions, a number of universities in the United States and throughout the world already have research and/or teaching programs in various aspects of packaging, ranging from materials, electrical and thermal modeling, thin films, and many others. The multidisciplinary nature of packaging technology clearly poses challenges not only to this community, but also to industrial colleagues who will have to use scientific fundamentals from a cross section of disciplines to bring about advanced products.

While the book is not intended to be a classic textbook for any course in packaging, it introduces the academic community to what microelectronics packaging is all about, to the current state of the technology in each of the disciplines, and to what fundamental areas could impact the industrial needs. To the industrial community it provides a comprehensive source of informa-

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tion ranging from consumer electronics to the most complex computers on all aspects of microelectronic packaging.

Packaging of LSI electronic circuits is the science and art of establishing interconnections and a suitable operating environment for primarily electronic circuits to process or store information. Accordingly, microelectronic packaging in this book is assumed to mean those designs and interconnection technologies necessary to support electrically, thermally, mechanically, and chemically those semiconductor devices with micron dimensions that are often referred to as integrated circuits.

Electronic packages contain many — in the case of large computers many millions — of electronic circuit components, notably resistors, capacitors, diodes, and transistors. To form circuits, these components need interconnections. Individual circuits must also be connected with each other to form functional units. Mechanical support and protection are required. To function, electrical circuits need to be supplied with electrical energy, which is consumed and transformed into thermal energy (heat). Since all circuits operate best within a limited temperature range, packaging must offer an adequate removal of heat. This leads to the four major functions of the package, i.e., power distribution, signal distribution, heat dissipation, and circuit protection. This book addresses all these technologies.

The book is organized into four basic categories. Chapter 1 addresses what packaging technology is and gives an overview of the entire book. The second category, Chapters 2 through 5, sets the electrical, thermal, and reliability objectives for packaging technologies. The third category, Chapters 6 through 14, reviews the various hierarchical technologies and the technology options for each hierarchy. The fourth category, chapters 15 and 16, gives product examples spanning from consumer products to supercomputers.

The main problem of creating a handbook in any field is obvious: by the time the book is completed, much of the information in it may require updating. This is particularly true with microelectronic packaging, which is one of the fastest if not the fastest growing of all technologies. But there must be a beginning. Further development and refinement, based on the comments and suggestions of the users, can appear in future editions. The book in its present state reflects what we believe the community wants currently.

Even though the book is written entirely by IBMers (at the time of starting the book), we have tried to include as many non-IBM technologies as possible, even to the extent of including recent Japanese patent information. We have also tried to minimize the IBM terminology that most of us are used to within IBM. Nevertheless, we feel the book does show the IBM flavor in some instances, particularly in dealing with mainframe packaging technologies. Some of this is inevitable and adds to the comprehensive and diverse nature of the subject matter. The book is not sponsored by IBM even though IBM gave permission to the authors for this undertaking.

Any handbook requires the dedication of a number of individuals involved in writing, typing, graphics preparation, manuscript reviewing, copyediting and publishing, and managing all these operations in such a way that a camera-ready manuscript is available in a timely manner. Above all, a free and stimulating environment is necessary, particularly in an industrial laboratory, where this work is carried out. In addition to the chapter authors, we would like to acknowledge two individuals without whom the book would not have gotten to "first base." Gigi Mongero, Rao's secretary, who coded the vast majority of the book and revised each chapter at least four times; Al Klopfenstein, Technical Assistant to Rao, who assumed the role of managing editor, interfacing with chapter authors, graphics vendor, publisher, Gigi, and Staff Programmer, Joan Dunkin. Our special thanks to Joan Dunkin who customized and recustomized the word processing style files to permit the production of a camera-ready manuscript with excellent engineering change control. We would also like to extend our thanks to Joan Connelly, who worked with us with full dedication, typing the manuscript and providing chapter copies to wherever necessary in a timely manner.

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Rao R. Tummala

Eugene J. Rymaszewski

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1

MICROELECTRONICS PACKAGING — AN OVERVIEW

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RAO R. TUMMALA

1.1 INTRODUCTION

Packaging of electronic circuits is the science and the art of establishing interconnections and a suitable operating environment for predominantly electrical circuits to process or store information. It is one of the least understood and yet one of the most important and challenging technologies in the information-processing industry. For years only those who were directly involved in either developing, manufacturing, marketing, or using packages knew what the technology was about. A good handbook that served the needs of the electronic community has been available since 1969 [1], and the reader is referred to this book for classical details on this subject. Another recent handbook covering primarily low-end packaging is complementary to this book [2].

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8

PLASTIC PACKAGING

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8.1 INTRODUCTION

Integrated circuit (IC) chips are enclosed in hermetic or plastic packages that provide protection from hostile environments and enable chip electrical interconnection to printed-circuit boards.

A hermetic package is constructed of metal and ceramic materials and has a sealed cavity where the chip resides. Polymer and metal are the flesh and bones of a plastic package. The chip, in this design, is attached to a metal lead frame, and subsequently encapsulated with a dense and rigid plastic by a transfer molding process. The plastic forms a protective envelope and defines the outer surface of the module.

Cost competitiveness in the semiconductor industry was the driving force behind development of the molded plastic package. A plastic version

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of its hermetic counterpart is the most cost-effective design on the market today. One such device typically costs three or four times less than a similar hermetic device. Furthermore, the various processing steps involved with the plastic encapsulation readily lend themselves to automated assembly. Along with the elimination of error-prone manual operations come lower manufacturing cost, higher productivity, and improved part reliability. The drive by electronic equipment manufacturers to reduce cost at the system level has catapulted the plastic package into first position in sales worldwide. Currently, approximately 85% of all IC packages produced are protected by plastic. Plastic encapsulation will continue to be used in the realm of high Input/Output (I/O), Very Large Scale Integrated (VLSI) circuits, and Ultra Large Scale Integrated (ULSI) circuits, since chips must be protected from the hazards of printed-circuit board assembly and field environment at reasonable costs.

Ever-increasing pin counts to accommodate more circuits per chip is the trend in IC packaging. Tape Automated Bonding (TAB) is starting to look promising as a packaging technique for I/O counts greater than 200. Improvements in chip passivation coupled with TAB will introduce the hermetic chip, thus eliminating the package envelope altogether. This trend is apparent in advanced memory packaging today.

The use of plastics as protective barriers raises a whole family of issues dealing with processing conditions, material compatibility, and reliability that need to be resolved. In the encapsulation of a device, no single factor predominates. Unfortunately, it is frequently and incorrectly assumed that the whole problem resides in the selection of the polymeric coating and that all the issues will disappear once some magically versatile material is found. This is far from the truth. A systematic approach needs to be considered because the design of a plastic package involves many factors, any of which can initiate several studies by itself. Attempts at improving the package by simply altering the material formulation regardless of other ramifications may ultimately create more problems than helpful solutions [1]. Typical factors, along with some of the well-known design options, may include the following: junction seal (SiO_2, Si_3N_4), configuration, and chip size; metallization (Au, Al, Al/Si); passivation (chemical vapor – deposited phosphosilicate glass, plasma-coated nitride, silicone); chip mounting (polyimide adhesive, conductive epoxy, eutectic); encapsulation (epoxy, silicone, thermoplastics, polymer blends); and, processing parameters (temperature, pressure, time, cure conditions). For instance, when the die is too large for the designed package, the encapsulation curing stresses may become sufficiently large to affect the delicate underlying circuitry.

This chapter presents an overview of the technology for fabricating encapsulated IC packages. The "ideal" polymeric coating is discussed in terms of functional requirements, which are then used to evaluate conventional

materials, such as epoxies and silicones. Similarly, more exotic alternatives, such as thermoplastics and the new class of polymer blends known as interpenetrating polymer networks, are also assessed. Aside from the material considerations, processing requirements for three molding techniques, namely, transfer molding, radial-spread coating, and reaction-injection molding, are also appraised. The material and technique selected essentially determine the future performance of the encapsulated parts. Materials with high shrinkage and post-curing conditions can impart to the dies various levels of stresses. At low magnitudes, metal lines can be shifted, or miniature cracks can be initiated in the passivation layer. Ionic entrapment occurs subsequently, and, ultimately, accelerates the corrosion process. At the other extreme, stresses can be drastically high enough to completely fracture the die into pieces. Furthermore, the compounding of high concentrations of fillers into the resins reduces the severity of thermal-expansion mismatch. However, some of these fillers carry low, albeit unacceptable, levels of radioactivity. The alpha particles emitted can possess sufficient kinetic energies to penetrate the protective inorganic layer and alter the electronic state of the device. Stresses, corrosion, and alpha particle-induced errors are the three common failure mechanisms influencing the reliability of plastic-coated components, that are discussed.

8.1.1 Chapter Organization

A brief history of chips in plastic forms the starting point for this treatment of the technology of plastic packaging. The chapter is divided into the following six main sections:

1. Plastic Molded IC Package Design (8.2, "Plastic Molded IC Package Design")
2. Lead Frame Design, Materials, and Processes (8.3, "Lead Frame Design, Materials, And Processes")
3. Encapsulation Materials (8.4, "Encapsulation Materials")
4. Encapsulation Processes (8.5, "Encapsulation Processes")
5. Plastic Package Reliability (8.6, "Plastic Package Reliability")
6. New Developments (8.7, "New Developments")

Section 8.2, "Plastic Molded IC Package Design," on page 527, provides a physical description of dual-in-line and surface-mount packages, and outlines some of the manufacturing and operating issues commonly encountered with these modules. This leads to a more detailed discourse on lead frame design in section 8.3, "Lead Frame Design, Materials, And Processes," on page 544. In section 8.4, "Encapsulation Materials," on page 555, the functional requirements for a polymeric encapsulant are considered. Some conventional materials are then evaluated in terms of those conditions. Subsequently, three encapsulation techniques are discussed and processing-re-

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lated issues are analyzed in section 8.5, "Encapsulation Processes," on page 570. Once the package has been assembled, section 8.6, "Plastic Package Reliability," on page 629, briefly describes traditional stress tests used to assess plastic-package reliability and their implications. Finally, the latest developments in packaging of chips with polymers are discussed in section 8.7, "New Developments," on page 650.

8.1.2 History of Chips in Plastic

Plastic is a generic term for a host of man-made organic polymers. These compounds have always been used in the design of electrical and electronic equipment. One of the first applications of phenol-formaldehyde resin in the early 1900s, for instance, was molded distributor caps. Prior to the development of integrated circuits, the densest electronic packages were welded cordwood modules, which used epoxy as an encapsulant.

The first transistors were packaged in hermetically sealed metal cans, a design so effective that it is still in use today. Transistors encapsulated in plastic appeared in the late 1950s. Two plastic transistor package designs prevailed at that time. One, popularly known as the "glob top," used a ceramic header to which the chip was attached and wirebonded. A drop or glob of epoxy resin was placed over the chip and, when cured, formed a shiny, black hemisphere on the ceramic header. The second package used a sheet-metal frame as its central supporting structure. The chip was attached and wirebonded to this frame. Plastic was then molded around the chip, wires, and frame to form the outer envelope. The latter design, lead frame, chip, and plastic, was the fundamental starting point from which all subsequent plastic IC packages evolved.

The early sixties saw the development of integrated circuits. These, like transistors, were initially packaged in metal cans, but cans were pin limited and difficult to place on printed-circuit boards. As a result, a new package specifically designed for ICs was subsequently introduced and called a "flat pac."

Flat pacs were small, rectangular boxes made of metal, ceramic, or glass that had 12/20 leads emanating from the long side of the rectangle. The chip was bonded, wired, and sealed into a central cavity. Lead pitch or centerline-to-centerline spacing was 1.27 mm. Since this dimension was relatively narrow (for the existing technology), flat-pac leads had to be soldered to copper pads located on the surface of a circuit board. Thus, the first IC packages used surface solder for board assembly, giving rise to the now familiar terminology of surface-mount technology.

Circuit-board designers and assemblers were accustomed to mounting components to boards by inserting terminal leads through holes and wave-soldering the complete assembly. On the other hand, flat pacs required hand placement and hot-knife soldering, a costly operation. Economic incentives

were, therefore, clamoring for a new IC package design with a configuration that could be mounted and soldered to a printed circuit board in the conventional manner. Packaging engineers in Silicon Valley solved this problem by modifying the flat pac design. They stretched the flat pac lengthwise to accommodate a 2.54 mm pin pitch. Each row of pins was bent downward so that they could be plugged into a socket or soldered to holes in a circuit board. Because there were two rows or lines of pins, the design was dubbed the dual-in-line package, and the DIP was born.

As with flat pacs, the first DIPs were constructed of metal, glass, or ceramic, and had an internal cavity for chip mounting. This was an effective and reliable design, but was relatively costly. The semiconductor industry, being one of the most cost-competitive in the world, placed great emphasis on reducing IC packaging cost. This striving for cost-effectiveness led to the design of a molded plastic DIP that utilized the same elements as the molded transistor — lead frame, chip, and plastic. The plastic DIP (P-DIP) design was simple, used inexpensive materials, and was amenable to mass production. These attributes enabled the P-DIP to become the most popular IC package ever and led to production volumes measured in the billions per year.

P-DIP dominance is being challenged in the eighties by the very package it superseded — the flat pac. Made of plastic this time around and called a Small Outline Package (SOP), it is already supplanting P-DIPs in consumer products. As in the design for the DIPs, leads on SOPs emanate from two sides only. For pin counts from 20 to 84, the square, Plastic Leaded Chip Carrier (PLCC), with leads on all sides, was developed. This was followed by the quad flat-pac configuration where the lead pitch was halved to 0.64 mm, enabling pin counts as high as 200.

SOPs, PLCCs, and quad flat pacs use similar molded construction concepts as their precedents, namely, the P-DIP and the Plastic Transistor. Combining lead frame, chip, and plastic into a viable IC package is the topic of this chapter. Although a large portion of the chapter is devoted to molded packages, another package configuration obtained with the "glob top" process will also be discussed.

8.2 PLASTIC MOLDED IC PACKAGE DESIGN

8.2.1 Functional Requirements

IC packages are designed to accomplish the following three basic functions:

1. Enclose the chip within a protective envelope.
2. Provide electrical connection from chip to circuit board.
3. Establish a thermal path from the semiconductor junction to the environment.

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To execute these functions in metal and plastic, package designers start with a fundamental concept and, using principles of engineering, materials science, and processing technology, create a design that encompasses:

1. Low lead capacitance and inductance.
2. Safe stress levels.
3. Material compatibility.
4. Low thermal resistance.
5. Seal integrity.
6. High reliability.
7. Ease of manufacture.
8. Low cost.

Success in performing the functions outlined naturally depends on the package-design configuration, the choice of encapsulating materials, and the operating conditions. Unfortunately, all the desirable properties for a package are highly interdependent, and maximizing one feature may well be detrimental to several others. For instance, steps taken to reduce the stress-induced failures in a package may also increase the moisture permeability of the encapsulation. In turn, the package will become more prone to corrosion. Thus, it is important to consider the special packaging needs of each individual case in a systematic manner before deciding on a particular design combination. Some chip parameters to consider may include, for example, limiting die size, intended power dissipation, maximum allowable junction temperature, and back-end-of-the-line (BEOL) structures. Similarly, package parameters, which have to be evaluated concurrently, can encompass the interconnection method (wire bond, C4, TAB, etc.), the package-form factor, and the heat removal scheme. Wirebond, C4, TAB are addressed in Chapter 12, "Printed-Circuit Board Packaging."

Consider, for example, the influence of the BEOL on the package design. The push for ever more functions on single chips has produced increasingly larger dies. Once encapsulated in plastic, however, large thermal expansion mismatches will occur. Consequently, the dies become more susceptible to failure from stress-induced imperfections, such as passivation cracking, metallization lines opens, ensuing corrosion, and bond failure. Thus, BEOL passivation techniques and metallization materials may, in this respect, play a key role in device reliability.

Typically, passivation cracking is related to the ductility and strength of the passivating materials. Silicon dioxide, for instance, is extremely brittle and cracks readily. Further improvements may encompass more ductile insulators, such as compressive silicon nitride, phosphosilicate glass (PSG), and polyimide. These materials, however, may introduce a new set of problems. When the doping level in PSG is too high, phosphorus ultimately leaches out during harsh environmental testing, combines with residual absorbed water to form phosphoric acid, and starts corrosion [2, 3]. Polyimide passivation,

on the other hand, has high purity and acts as an excellent barrier to alpha particles, but allows ionic migration and water permeation. Metallization failures frequently seem to occur near sharp bends in the lines. Since the metallization has to traverse severe topography, such areas are stress concentrators, which can accelerate crack initiation and propagation. Another important variable to consider is the heat dissipation, which is directly related to the chip technology, e.g., bipolar versus CMOS. Indeed, low-power chips are typically difficult to package reliably in plastic because insufficient heat is generated to drive off any moisture absorbed into the packages.

As with chip features, package parameters also play similar important roles. Most conventional packages are made by transfer molding, as is discussed later. With this form factor, the die is completely surrounded by encapsulant, and as the plastic material cures, the enclosed die is under compression from all sides. When chip protection is achieved with a conformal coat or by glob topping, as may be the case with TAB parts, the top side is under compression while the bottom is in tension. In this case, chip cracking may be commonly encountered, especially with resins displaying large cure shrinkage. Furthermore, adhesion of the resin to the lead frame is governed both by the design of the frame and by the metallization.

Finally, the reliability of a device is strongly dictated by the interconnection method used. In most conventional packages, a gold wire is bonded directly to an aluminum pad, leaving still a fairly large area of the pad exposed. Aluminum, which is the predominant metal in chip-level metallization, has a very high chemical reactivity. Without its protective oxide layer, aluminum reacts readily with even pure water. With other interconnection methods such as C4 or TAB, a thin layer of interfacial metallurgy (e.g., titanium, copper, and gold) is first deposited over the aluminum. Subsequently, a solder ball is deposited (with C4), or a gold bump is plated over the pad (with TAB). In effect, the highly corrosion-sensitive aluminum becomes "passivated," and the incidence of device failures from corrosion can thus be reduced.

Unwanted elements from the environment can permeate the package by several mechanisms. Unlike metals or inorganic insulators, polymer materials all have relatively porous structures, which may allow absorption or transport of water molecules and/or ions. The ability of a polymer to absorb water from either the liquid or the gaseous state is related to the chemical nature of the polymer; polymers that contain very polar groups (such as epoxies, polyamides, or polyvinyl alcohols) absorb relatively large amounts of water compared to nonpolar materials (such as fluorocarbon or hydrocarbon polymers). Water absorption is only meaningful when measured at the equilibrium value. A more significant parameter in defining the moisture resistance of a material is the moisture vapor transmission rate, which measures how rapidly moisture is transported through a polymer film of known

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dimensions under standard conditions of temperature and humidity. This parameter is dependent on the physical structure of the polymer; highly crosslinked materials, for instance, tend to minimize the extent of moisture infiltration into the packages. Some of the techniques used to measure the moisture content are well known, and encompass the mass spectrometer, the laser spectrometer, the electrical hygrometer, the aluminum oxide transducer, and the surface conductivity sensor. These techniques have to be chosen in some combination that will optimize both the selection of materials and design of the package. The mass spectrometer and hygrometer, for instance, can be used to evaluate materials that are thermally stable and display low outgassing. Laser spectroscopy, on the other hand, is a relatively new technique based on the derivative infrared tunable-diode laser spectrometer developed recently [4]. In this case, precise (± 50 ppm) determination of trace amounts of moisture ($\geq$ 50ppm) in small samples of gas ($10 - 100\mu\ell$) can be obtained as the gas expands into an evacuated chamber cell. The aluminum oxide sensor can be relied upon for measuring the conductivity of potential candidate materials with or without contamination. Finally, the surface sensor can indicate the internal moisture level at controlled operating conditions. The sensitivity limit of the surface sensor depends on the size of the micropores of the oxide layer and the maximum shift of the triple-point temperature of the water molecules physisorbed to these micropores [5]. More information on the measurement techniques can be found in section 8.6.2.2, "Corrosion- and Moisture-Induced Fails," on page 639.

It can be seen, therefore, that the functional requirements for an IC package are highly interdependent. To optimize a given design, specific and measurable material and device parameters need to be characterized and related to the available reliability data base. In the following section, some of the design requirements and factors influencing the performance of an encapsulated device are discussed.

8.2.2 Design Concept

As shown in Figure 8-1, molded IC packages consist of:

1. Metal lead frame.
2. Chip bonding material.
3. Chip.
4. Fine-diameter gold wire.
5. Plastic molding compound.

The lead frame is the central supporting structure of the package to which every other element is attached. Etched or stamped from a thin sheet-metal strip into a filigree of narrow beams that radiate from a center platform, the frame carries the chip throughout the assembly process and is imbedded in plastic after molding. Bonded to the lead frame's central platform is the semiconductor chip, which, in turn, is electrically connected to the radiating beams of the frame with fine-diameter gold wires. This assembly of chip, wires, and frame is covered with a thermoset plastic in an operation called **transfer molding**. With the body now defined in rigid plastic, the leads are trimmed, formed, and plated to finish the package. The progression of the configuration of the plastic module is shown in Table 8-1.

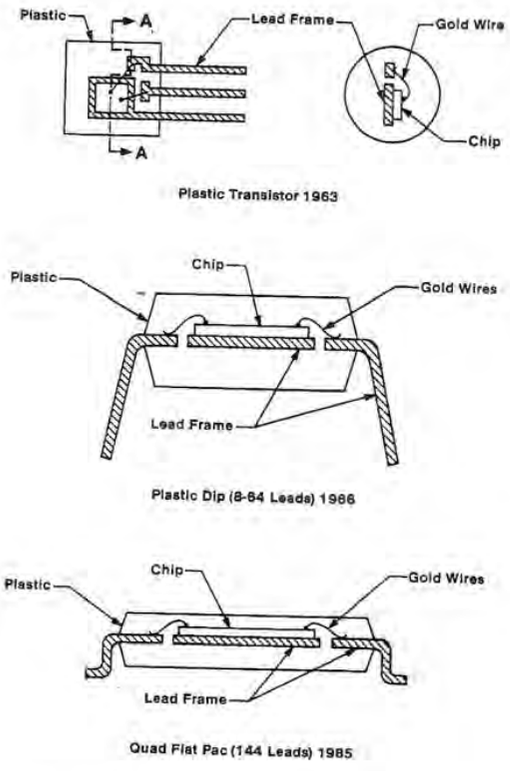


Figure 8-1. Molded Plastic Package.

Similarly, the electrical and thermal parameters of a few representative plastic packages are illustrated in Table 8-2. The ability of a package to conduct heat from the chip to the environment is usually expressed in terms of thermal resistance, normally called θ_{JA}. θ_{JA} is the total resistance from the junction to the ambient environment, and is often separated into two components, namely, θ_{JC} (junction-to-case) and θ_{CA} (case-to-ambient), so that $\theta_{JA} = \theta_{JC} + \theta_{CA}$. Test conditions for Table 8-2 are as follows: 1) Test

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Table 8-1. Molded Plastic Packages (Part 1 of 3).

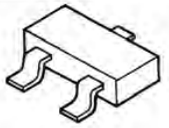
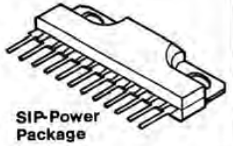
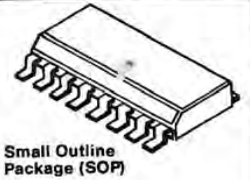
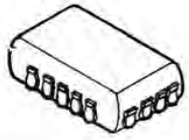
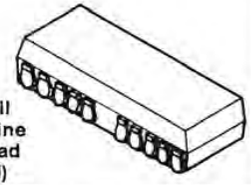
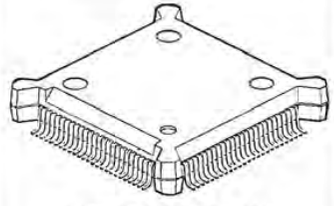
Package Type	Pin Count	Lead Pitch mm	Devices Used for
 SOT-23, SC-59	3	3.0	Diodes & Transistors
 SIP-Power Package	3-12	2.54	Power Transistors, Darlingtons Plus Control Logic
 Plastic Dip	8-64	2.54	Linear, Logic, DRAMS, SRAMS, Microprocessors, ROMS, PROMS Gate Arrays
 Zig-Zag In Line Package (ZIP)	16-24	1.3	DRAMS & SRAMS
 Small Outline Package (SOP)	8-28	1.3	Linear, Logic, SRAMS

Table 8-1. Molded Plastic Packages (Part 2 of 3).

Package Type	Pin Count	Lead Pitch mm	Devices Used for
 PLCC	18	1.3	64 & 256K DRAM
 Small Outline J-Lead (SOJ)	20-26	1.3	One & Four Megabit DRAM
 Plastic Leaded Chip Carrier (PLCC)	20-84	1.3	Logic, PROMS, Microprocessors, Gate Arrays, Standard Cell
 Plastic Quad Flat Pac (PQFP)	88-200	0.64	Gate Array & Standard Cell Logic

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Table 8-1. Molded Plastic Packages (Part 3 of 3).

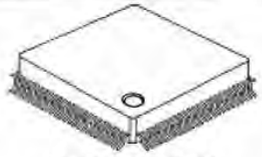
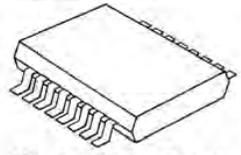
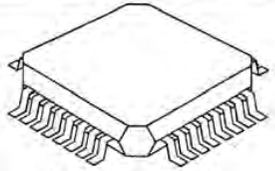
Package Type	Pin Count	Lead Pitch mm	Devices used for
 Square Quad Flat Pac (SQFP)	88-200	0.64	Gate Array & Standard Cell
 Rectagular Quad Flat Pac (RQFP)			
 Very Small Outline Package (VSOP)	16-30	0.65	DRAMS
 Very Small Quad Flat Pac (VSQF)	32-100	0.5	Gate Array

Table 8-2. Electrical and Thermal Characteristics of Some Plastic Packages.

Module Type	No. of Pins	THERMAL CHARACTERISTICS Thermal Resistance Junction-to-Case (θ_{JC}) (°C/W) A42 L.F.	Cu L.F.	Thermal Resistance Junction-to-Ambient (θ_{JA}) (°C/W) A42 L.F.	Cu L.F.	Electrical Characteristics C (pF)	L (nh)
DIP	8	79	35	184	110	–	–
	14	44	30	117	85	0.38–1.13	3.2–10.2
	16	47	29	122	80	–	–
	20	26	19	88	68	0.53–1.49	3.4–13.7
	24	34	20	76	66	–	–
	28	34	20	65	56	–	–
	40	36	18	60	48	–	–
	48	45	–	–	–	–	–
	64	46	–	–	–	–	–
SOP	8	–	45	236	159	–	–
	14	–	29	172	118	0.22–0.54	2.6–3.6
	16	–	27	156	110	–	–
	16w	–	21	119	97	–	–
	20	–	17	109	87	0.45–0.85	4.9–8.5
	24	–	15	94	75	–	–
	28	–	71	92	71	–	–
PLCC	20	–	56	–	20	0.3–0.4	3.5–6.3
	28	–	52	–	15	0.4–0.5	3.7–7.8
	44	–	45	–	16	0.02–0.8	4.3–6.1
	52	–	44	–	16	0.02–0.8	4.3–6.1
	68	–	43	–	13	0.02–1.0	5.3–8.9
	84	–	42	–	12	–	–
PQFP	84	–	14	–	47	–	–
	100	–	13	–	44	–	–
	132	–	12	–	40	–	–
	164	–	12	–	35	–	–
	196	–	11	–	30	–	–

ambient: still air; 2) Test fixture: glass-epoxy test board; 3) Test board size: 28.4 mm x 19.1 mm x 1.5 mm for DIPs, SOPs, PQFPs, and 56.9 mm x 56.9 mm x 1.5 mm for PLCCs.

In Table 8-2, the capacitance (C) is determined by the length of the leads, the distance separating the leads, the dielectric constant of the composite material between the leads, the thickness of the leads, and the number of leads involved. Capacitance measurement is done using two separate tests. The first technique is to describe the capacitance of a single lead in the pres-

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ence of a system of conductors. This is called the "loading capacitance." The second technique is to represent the capacitance of two leads, isolating them from all the other leads. This is the "lead-to-lead capacitance." The "loading" values are always larger than the "lead-to-lead" values due to the increase in the number of leads since the lead-to-lead system contains only two leads. Values from both methods are given in Table 8-2. The inductance (L), on the other hand, is governed primarily by the location of, and the area included in the circuit loop. Generally, small values are obtained in the smaller packages with shorter leads and I/O circuits with adjacent leads.

Chip, wire, lead frame, and molding compound are joined in the assembly operation to form a plastic IC module. The objective of this operation is to fabricate, at high yields and low cost, a package which meets specifications and the customer's reliability requirements. Users of IC modules are driving down defects as low as 10 ppm. Traditional sampling plans used by receiving inspection will not guarantee such low defect rates. To achieve these quality levels, every process used to fabricate chips, packages, and their constituent parts must be controlled with the goal of producing defect-free parts. The complexity of the various steps involved can be seen in Table 8-3.

8.2.3 Package Seal

The first function of a semiconductor package is to protect the chip by sealing it from environmental hazards that will be encountered during its lifetime. Such hazards can be divided into two broad categories, namely:

1. Those caused by environmental factors to the package, e.g., humidity, soldering stress, and handling during assembly.
2. Hazards induced by the package itself, e.g., material shrinkage stresses.

The design of the package seal is paramount in minimizing environmental effects. Indeed, the seal must protect the chip from lead-finishing operations (trimming, forming, plating, and dipping), mechanical and thermal shock (shipping stresses), board assembly (insertion, soldering, and cleaning), and end use or machine environment (heat, humidity, and vibration).

The seal as well as the body of a hermetic package is made from materials that are impervious to liquids and gases. Protective features of this design are obvious. The chip is sealed within a metal enclosure in an inert atmosphere, and provided that the integrity of the seal remains intact, nothing gets through. Chip protection in a plastic package, on the other hand, is more subtle. All organic polymers will transmit water vapor, some more rapidly than others. Because polymers are the main constituents of molding compounds, the chip is never sealed from water molecules. Water is transported to the chip surface along two avenues: one is the interface between the lead frame and the plastic; the other by diffusion through the molding material itself. Ways to retard or prevent water diffusion into the package from taking place are discussed in section 8.4, "Encapsulation Materials," on page 555.

Table 8-3. General Assembly Flow Process (Part 1 of 2). Process flow with typical control tests.

OPER. NO.	OPERATION	CONTROL
1	WAFER MOUNT	Orientation to Ring Carrier.
2	WAFER SAW	Feed, Speed, Blade Dress and Replacement Interval. Visual Check for Excessive Chipping or Passivation Damage.
3	FIRST OPTICAL	Gross Chip Defects Such as Chips and Cracks Intruding Into Active Areas, 50% Narrowing of Metal Lines, Passivation on Bond Pads.
4	CHIP BOND	Heater Block Temp (Eutectic Only). Chip Push Test on Specified Sample Size Twice Per Shift/Machine. Cure Oven Atmosphere Time and Temperature.
5 (One Pass Bond Rework Allowed)	WIRE BOND	Capillary Pressure, Preheater and Bonding Stage Temp., Scrub Frequency. Wire Pull Tests on Specified Number of Wires Twice Per Shift/Machine. Fail on Break of Less Than 3.5 Grams or any Ball Lift from Pad.
6	SECOND OPTICAL	Wire Dress, 75% Haloing on Eutectic Bond, Snowplowing over Chip with Polymer Bond; any Silver Epoxy on Chip Surface.
7	MOLDING	Ram Pressure and Speed, Mold Clamping Force, Temperature Across Chases, Cycle Time. Pellet Internal Temperature at Preheat.
8	POSTMOLD CURE	Oven Temp. Profile, Time.
9	DEFLASH	Chemical - Bath Temp. Immersion Time. Bath Renewal Cycle. Cleaning Water Temp/Time. Mechanical - Grit Removal. Lead Damage.
10	BACKSIDE MARK	Correct Wafer Lot Number
11 (One Pass Rework Allowed)	LEAD FINISH IF ELECTROPLATE	Chemical Bath Assays - Time and Temp. Cleaning Bath Time and Temp. Plating Uniformity and Thickness.
12	DAM BAR SHEAR	Shear Punch and Die Maintenance Freq. Punch Offset. Ragged Shear Edges, Splinters.

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Table 8-3. General Assembly Flow Process (Part 2 of 2). Process flow with typical control tests.

OPER. NO.	OPERATION	CONTROL
13	LEAD TRIM & FORM	Lead Holding Anvil Pressure. Lead Spread (Dips). Package Cracking. Coplanarity (Surface Mount Packages). Dimensions.
11A (One Pass Rework Allowed)	LEAD FINISH IF SOLDER DIP	Belt Speed, Flux Type, Solder Bath Temp. Resistivity of Last Cleaning Zone. Coating Uniformity, Thickness.
14	SHORTS AND OPENS ELECT. TEST.	Yield.
15	BURN-IN (if req'd)	Oven Temp., Time, Applied Voltage.
16	POST BURN-IN ELECTRICAL	Yield.
17	MARK	Ink - Cure Time and Temp. Rework Allowed. Marking Durability. Laser - Readability.
18	FINAL ELECTRICAL	DC and AC Tests at Room Ambient and Elevated Temp.
19	FINAL Q.C. GATE	Dimensions. Correct Park No. Marking. Electrical. Lead Finish. Solderability. Correct Shipping Container. Cosmetic.

Thus, the plastic seal around the chip serves the dual purpose of slowing down water transport along the lead frame and diffusion routes, and preventing water from accumulating in liquid form on the chip's metal wiring patterns.

8.2.4 Plastic-Lead Frame Interface

Molding compounds used for encapsulating chips in plastic packages are modified epoxy resins. Epoxies are good adhesives, readily forming chemical bonds with surfaces they are in contact with. This adhesive property can be inhibited by adding waxes or mold-release agents to the resin so that parts can be easily removed from mold cavities. When epoxies cure to solids, they shrink in volume by about 0.3 to 0.5%. The extent of shrinkage depends on the nature of the resin used, the type of fillers added, and the volume loading

of fillers compounded. Shrinkage is the mechanism that seals a plastic IC package. The resin exerts compressive forces around chip, wires, and lead frame as it contracts during cure to form a compressive seal.

The plastic-lead frame interface is a mechanical joint whose sealing integrity can be improved by mechanical and chemical means. Mechanical enhancement is described in section 8.3, "Lead Frame Design, Materials, And Processes," on page 544. Currently, chemical seal improvement is accomplished by two methods. The first is synergistic and employs the wax used as a mold release in the molding compound. The wax migrates during molding to the metal surface of the lead frame and all the interconnect wiring, and as the epoxy shrinks around these same surfaces, the wax is forced into potential voids and delamination existing between plastic and metal. Because waxes are hydrophobic, water ingress along the lead frame tends to be inhibited. Alternatively, chemical bonding between epoxy and the metallic oxides on the lead frame surface can also be improved by treating the frame with organosilane coupling agents. Silane treatment was used in the early 1970s with some success, but the operation was expensive. Lead frame treatments were abandoned when small amounts of coupling agents compounded directly to the molding resins for adhesion enhancement were successfully developed.

8.2.5 Chip Surface

Chip design, particularly phosphorus control and passivation selection, is important to the plastic package system.

There are some chip designs, such as dynamic random access memories (DRAMs), that require a phosphorus-rich oxide under the aluminum metallization. The phosphorus reduces strain and prevents cracking of the oxide during glass reflow. Excess phosphorus in heavily doped oxide forms P_2O_5, which is one of the most hydrophilic compounds known. Water molecules getting through the package to the chip will combine with P_2O_5 to generate phosphoric acid, which subsequently attacks the aluminum lines from below. Chips that are destined for plastic packages must be fabricated with the minimum phosphorus required to achieve a crack-free oxide layer. Current manufacturing processes call for reducing excess P_2O_5 by steam leaching the wafers after oxide reflow.

The seal of a plastic package is not a perfect barrier. Water eventually arrives at the chip surface and must be prevented from accumulating as liquid around the aluminum lines and wirebond pads. The first line of defense against moisture-induced corrosion is chip passivation.

The original material used in the wafer process for chip passivation was chemically vapor-deposited phosphosilicate glass (CVDPSG). It was originally intended to protect the aluminum lines from scratches during handling, and was never an effective moisture barrier. Glass deposited by this method always has residual tensile stresses, and is prone to pinhole formation,

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cusping at the metal edges, leaching of the phosphorus, and cracking from mechanical and thermal stresses. A breakthrough in chip passivation came about in the late 1970s with the development of CVD compressive nitride films.

Silicon nitride is chemically deposited by reacting dichlorosilane and ammonia at reduced pressures between 700°C and 800°C, or by reacting silane and ammonia at atmospheric pressure and at temperatures between 700°C and 900°C. The resulting passivation glasses are characterized by residual compressive stresses, exhibit good adhesion to the silicon substrate, show excellent conformability over the aluminum metal lines, can be deposited pin-hole free, and are relatively crack resistant. These attributes enable nitride films to withstand repeated thermal shocks encountered during package assembly without developing cracks; resist delamination, thereby eliminating the buildup of an ultimately corrosive water reservoir; form a good barrier to the diffusion of water and ionic impurities (e.g., *Cl* and *Na*); and are resistant to thermally-induced deformation stresses [6, 7, 8]. Pure compressive nitride films of 1 μm minimum thickness or nitride/plasma oxide sandwich structures can currently be found as passivation on most commercial chips that are to be encapsulated or molded in plastic.

8.2.6 Chip Coatings

In a typical plastic package, the cured molding compound is pressing down directly onto the chip surface. This interface is altered in some designs by the addition of a chip-coating material, usually a silicone elastomer or a polyimide resin. Both families of compounds are chlorine-free and form adhesive bonds with the semiconductor surface. Chip coatings are used to provide a halogen-free polymer around the chip, isolate the chip surface from the plastic molding compound curing stresses, and serve as an alpha particle radiation barrier.

8.2.7 Halogen-Free Coating

The initial epoxy compounds used for molding ICs in the late sixties and early seventies had high (relative to today's standards) percentages of hydrolyzable chloride (typically in the 100 ppm range). Because the prevalent failure mode of the plastic package is chlorine-induced corrosion of the aluminum metallization, the addition of a chlorine-free barrier between plastic and chip seemed prudent.

Silicone elastomers were the first coating materials used for this purpose. However, the addition of an elastomer barrier slowed the onset of corrosion but did not stop it. Furthermore, the use of silicone elastomers in molded packages presents several disadvantages such as:

- A large difference (over 30 times) in expansion rates between the elastomer and the plastic usually leads to premature failure of gold wires on temperature-cycling stress tests.
- When the elastomer is applied over large chips, a thick dome forms. During temperature cycling, the dome expands and tends to force the plastic away from the lead frame.
- The coating application adds an extra assembly operation that would ultimately raise the unit cost of the modules.

The development of low-chloride molding compounds has curtailed the use of silicone elastomers as a corrosion inhibitor.

8.2.8 Distribution of Stresses

There are families of semiconductor chips, such as Hall-effect devices and linear circuits, that contain resistors, which must be balanced to achieve circuit performance. These resistor elements on a chip's active surface change values as a function of pressure (due to piezoresistive effects). The resistor sets become unbalanced when the pressure exerted on them is nonuniform, as is the case when plastic is in contact with the chip surface.

Silicone elastomers are tailor-made for solving the piezoresistive problem. Hall-effect chips are completely encapsulated with a thin layer of elastomer prior to molding. The nonuniform compressive forces of the rigid plastic are transmitted to the elastomer, which exerts uniform hydrostatic pressure on the entire Hall-effect chip. Each resistor now has equal pressure applied, and the set remains in balance in the final molded configuration. Hall-effect chips are an extreme case of linear devices which require an elastomeric coating for stress redistribution.

Nowadays, silicone elastomers are increasingly being used as stress buffers for large CMOS logic-array chips. Molding compound induced-stress increases as silicon dies get larger. Eventually, stresses reach a critical point where aluminum lines deform and the passivation layers crack. A conformal coating of a silicone elastomer on the chip separates the rigid plastic from the surface structures of the semiconductor, thus eliminating any potential deformation induced by molding stresses. More recently, polyimide resins have supplanted silicone elastomers for linear device applications since these polymers do not have the drawbacks of elastomers mentioned previously [9, 10, 11, 12, 13, 14].

8.2.9 Radiation Barriers

Alpha particle-induced errors in semiconductor devices were recorded for the first time in 1978 [15]. Such errors are likely to be magnified with the current trend toward higher levels of integration.

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A soft error is defined as a random, nonrecurring single-bit change in the information stored within a memory cell. The passage of an alpha particle through an active device region may upset an electron-hole pair sufficiently to alter its logic state. However, no physical or permanent damage is recorded. In fact, the single bit will recover by the next read/write cycle and show as much likelihood of further failure as any other bit in the device. As a result, such errors have been identified in the past as "voltage marginality," "system noise," or "pattern sensitivity" [16].

Alpha particles (α) originate from the residual radioactivity of uranium and thorium present as trace impurities (a few parts per million range) in the raw materials used to make a plastic package. For example, 1.0 ppm of U^{238} or 0.4 ppm of Th^{232} can produce alpha fluxes of the order 0.1 α/cm^2/hour. This is one-to-two orders of magnitude higher than the level found to be tolerable in memory devices [17, 18]. Some emitted particles can have energies up in the range of 8.8 MeV, enough to go through the interior surface of the package.

This type of memory-chip failure is a physical phenomenon rather than a statistical mechanism. It can occur only when all of the following three conditions are met [19]:

1. Because alpha particles are readily absorbed internally by the device, they have to be located near the active surface in order to have any major effect. This distance was found to be in the order of 50 μm.
2. Sources of alpha particles must have a direct line of sight of the active surfaces.
3. Devices need to be particularly sensitive to alpha radiation. The carriers generated by the passage of a particle need to be collected in sufficient quantities to upset the logic state of a memory cell [20, 21].

Since the main source of radiation in plastic packages comes from fillers, the ensuing alpha flux varies depending on the activity of the fillers. Usually, this falls in the range of 0.1 α/cm^2/hour or less. The reinforced resin in direct contact with the chip-top surface will be constantly bombarded by the ionizing rays. Aside from occasional cosmic ray interactions [22], no other sources of soft errors exist. This underlines the main difference existing between plastic and hermetic (cerdip and side-braze ceramic) packages. With the latter, alpha fluxes can emanate not only from the lid (gold-plated Kovar®, Alloy 42 materials, or ceramic) and the sealing glass, but also from potential airborne radon in contact with the surface [23, 24]. Therefore, with plastic packages, a straightforward solution to eliminating soft errors would be to switch to colder fillers and to clean up the resin of radioactive traces. Although this is acceptable in principle, the cost would be prohibitive for both low- and high-end applications. However, residual activity can still be a major problem. The sensitivity of current measurement techniques is already strained to their lowest counting limit [25].

Designing new technologies or developing new devices immune to alpha fluxes would certainly be the most desirable alternative. Error-correction systems, for instance, have been introduced in large memory devices to counter soft errors. Extending that technology down to the smaller scale of random logic circuits would be difficult. The stringent cost constraint inherently associated with low-end packaging will also have to be relaxed drastically. Currently, three approaches are being taken to solve the alpha radiation problem:

1. Place an alpha particle barrier between the alpha particle generating source and the memory cells.
2. Eliminate the alpha radiation source from packaging materials.
3. Design memory chips for reduced alpha radiation susceptibility.

The cheapest and easiest alternative would be to interpose a shielding layer between the active surface and the encapsulating resin. For the shield to be an effective barrier to alpha fluxes, the material itself has to meet three criteria. First, it has to be free of any residual radioactivity. Since the shield is deposited on the silicon die surface, emitted alpha particles would have a direct and potentially damaging line of sight to memory cells. Thus, even the slightest level of ionizing radiation in the shielding material would be intolerable. Second, the barrier has to be of sufficient thickness to absorb the released particles. Stopping most particles while letting a few get through still defeats the purpose of such a barrier, and third, the shield has to exhibit good adhesion characteristics to the uppermost layer of the active device. Delamination of the layer, for instance, can introduce paths for moisture collection or hot spots with poor thermal-dissipation characteristics.

One such application has recently been recorded with moderate success [14]. It has been suggested that alpha particles in the 8.0 MeV range would be stopped by a layer of a material such as silicone at least 0.03 mm thick [26, 27]. A room-temperature vulcanized (RTV) silicone was subsequently selected for shielding static random access memory (RAM) circuits mounted within hermetic multilayer ceramic DIPs. The material itself was found to radiate, on the average, 0.001 α /cm^2/hour, which would generate a tolerable soft-error rate of slightly less than 0.1% per thousand hours. Currently, aside from silicone elastomers, polyimide resins are also commonly used. As a result, previous problems associated with chip coating (e.g. molding stresses, interfacial adhesion, thermal stability) were revisited. A better solution was required.

Molding-compound formulators started developing low alpha radiation compounds in 1979. By 1983, compounds were on the market with alpha emission levels of less than 0.001 α/cm^2/hour. These developments, in conjunction with chip designs that were less susceptible to alpha particle hits, rendered chip coating for radiation protection obsolete.

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Therefore, it seems that trading the potential of a small number of soft errors for a guaranteed number of future hard errors would compromise the long-term reliability of the device. Balancing the sensitivity of the device with the residual alpha radioactivity will be a delicate and necessary task. Failures may occur even in "good" devices, and replacing a failed package with a "good" one does not alter the rate of failure as would be the case with hard errors. Alpha particle-induced errors, thus, appear to be a fundamental package parameter that device, systems, and manufacturing designers have to contend with — much like circuit response or thermal dissipation.

8.3 LEAD FRAME DESIGN, MATERIALS, AND PROCESSES

The lead frame is the backbone of a molded plastic package. Fabricated from a strip of sheet metal by stamping or chemical milling, it serves first as a holding fixture during the assembly process, then, after molding, becomes an integral part of the package. The functional requirements of a lead frame are:

1. A holding fixture that indexes with tool-transfer mechanisms as the package proceeds through various assembly operations.

Table 8-4. Lead Frame Materials (Part 1 of 2).

PART NO.	CAR'P A-42	CDA-151	OLIN CDA-194	OLIN CDA-195	HUSSEY CDA-155	HUSSEY KPC	KOBE KLF-1	KOBE KLF-2	KLF-5
TYPICAL ELEMENTS (%)	*Fe-58 A-42*	*Zr-0.1 Cu-bal*	*Fe-2.3 P-0.03 Zn-0.1 Cu-bal*	*Fe-1.5 Co-0.8 Sn-0.6 P-0.1 Cu-bal*	*Ag-0.034 P-0.058 Mg-0.11 Cu-bal*	*Fe-0.1 P-0.058 Cu-bal*	*Ni-3.2 Si-0.7 Zn-0.3 Cu-bal*	*Sn-0.1 Fe-0.1 P-0.03 Cu-bal*	*Sn-2.0 Fe-0.1 P-0.03 Cu-bal*
Melt P (°C)	1425	1000	1009	1090	1002	1083	1090	1083	1068
Spec. Grav.	8.15	8.94	8.8	8.92	8.91	8.9	8.9	8.9	8.9
E (GPa)	144.83	120.37	120.37	118.89	117.43	120.37	124.28	127.22	120.37
Thermal Conductivity (W/m/°C)	15.89	359.8	261.5	196.65	347.27	435.14	219.66	376.56	133.89
Linear Expansion (10^{-7}/°C)	43	177	163	169	177	170	170	170	165
Electrical Conductivity (% IACS)	3.0	90	65	50	86	92	55	82	35
Temper	H	3/4H	H	H		H	H	H	H H
Tensile Strength (GPa)	0.64	0.35	0.41	0.47	0.3 0.3 0.5	0.39	0.54	0.39	0.54
Elongation	10	7 min	3 min	3 min	2 2 2	4 min	7 min	4 min	7 min
Vickers HD	210	104	135	147	95 113 137	125	180	140	180

2. A dam that prevents plastic from rushing out between leads during the molding operation.
3. Chip attach substrate.
4. Support matrix for the plastic.
5. Electrical and thermal conductor from chip to board.

8.3.1 Materials

Lead frame material selection depends on factors such as cost, ease of fabrication, and the functional requirements of the frame. There are three categories of materials to choose from when designing lead frames: nickel–iron, clad strip, and copper-based alloys. Many alloys, specifically formulated for plastic IC packages, exist within these categories, as indicated in Table 8-4.

Table 8-4. Lead Frame Materials (Part 2 of 2).

PART NO.	MIT'B MF-202	TAMAGAWA TAMAC-2	TAMAGAWA TAMAC-5	T.I. 410SS	OLIN 19750	OLIN 19700	PAN PMC-IC
TYPICAL ELEMENTS (%)	*Sn-2.0 Ni-0.2 P-0.15 Cu-bal*	*Sn-0.15 P-0.006 Cu-bal*	*Fe-0.75 Sn-1.25 P-0.03 Cu-bal*	*Cr-12.0 Fe-bal*	*Fe-0.6 Mg-0.05 P-0.02 Sn-0.23 Cu-bal*	*Fe-0.6 Mg0.05 P-0.02 Cu-bal*	*Ni-1.0 Si-0.2 P-0.03 Cu-bal*
Melt P (°C)	1065	1083	1075	–	1085	1086	1090
Spec.Grav.	8.8	8.9	8.8	7.8	8.82	8.84	8.9
E (GPa)	112.54	117.43	117.43	19.96	120.37	118.41	127.22
Thermal Conductivity (W/m/°C)	154.81	376.56	138.07	24.27	261.5	320.49	259.41
Linear Expansion (10^{-7}/°C)	169	177	167	110	169	168	169
Electrical Conductivity (% IACS)	30	92	40	30	65	80	60
Temper	H	H	H		S	H	H
Tensile Strength (GPa)	0.59	0.34	0.48	0.62	0.56	0.45	0.55
Elongation	7 min	4 min	4 min	5 min	1.9	1.5	4-8
Vickers HD	185	105	150	220	160	144	160

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Nickel-Iron Alloys: The most widely used metal for lead frame fabrication is Alloy 42 (42% Nickel–58% Iron). This material was originally formulated as a glass-seal alloy for use as terminal pins on light bulbs and vacuum tubes. The first chip-attach method on hermetic as well as plastic modules was a gold/silicon eutectic alloy bond. Silicon/gold eutectic melts at 370°C, and when solid, has a high elastic modulus. A close match of thermal-expansion coefficient between silicon and substrate is mandatory with this bonding system to avoid chip fracture. Alloy 42, the vacuum tube terminal pin material, was chosen since its expansion coefficient is close to that of silicon (45 vs. 26×10^{-7}/°C). Alloy 42, furthermore, can be heat-treated to obtain optimum tensile strength and ductility for subsequent stamping and lead forming operations. The alloy can also be easily electroplated or solder-dipped directly without a nickel barrier plating.

Low-thermal conductivity is the most important drawback of nickel-iron alloys. Since the lead frame is the main conduit by which heat flows from the chip to the printed circuit board, this can have a profound effect on the package thermal resistance after prolonged device operation. Clad materials and copper-based alloys have been developed to reduce thermal resistance [28].

Clad Materials: A layered composite strip, such as copper-clad stainless steel, was developed to emulate the mechanical properties of Alloy 42 while increasing thermal conductivity. Cladding is accomplished by high-pressure rolling of copper foil onto stainless steel strip and annealing the composite to form a solid-solution weld. Properties are given in Table 8-4 [29]. More detailed discussions on this subject can be found in Chapter 13, "Coated-Metal Packaging."

Copper Alloys: Copper would be an ideal lead frame material from an electrical and thermal conductivity standpoint, but it has properties that must be modified before it can be successfully used in plastic packages [30].

8.3.2 Strength

The tensile strength of copper alloys is lower than that of nickel-iron or copper-clad stainless steel. The addition of iron, zirconium, zinc, tin, and phosphorus serves to improve the heat-treating and work-hardening properties of these alloys. The resulting tensile strength and ductility are adequate for lead frame fabrication and function.

Copper-alloy frames can be specified with tempers from one-half hard to spring temper. Half-hard material is less likely to crack when bending, but full-hard or spring temper is preferred for modules that are automatically inserted. Hard copper alloys approach iron-nickel in bending characteristics so that automatic inserters can be set up to run both alloy types without constant adjustments to cut and clinch mechanisms.

8.3.3 Thermal Conductivity

The ability of the lead frame to channel heat from chip to board is related to the thermal conductivity of the frame material. The main advantage of copper alloys is their high coefficients of thermal conductivity (see Table 8-4). The largest reduction in package thermal resistance is achieved by the use of copper alloys as shown in Figure 8-2 [31].

8.3.4 Thermal Expansion

Copper alloys have high thermal-expansion rates with respect to silicon but nearly match the expansion rate of low-stress molding compounds. This property affects the selection of chip-bonding materials. Silicon/gold eutectic bonding cannot be used with copper frames because its high elastic modulus couples thermally induced bending stress to the silicon, which can cause potential chip fracture. Silver-filled epoxies and polyimide chip-attach adhe-

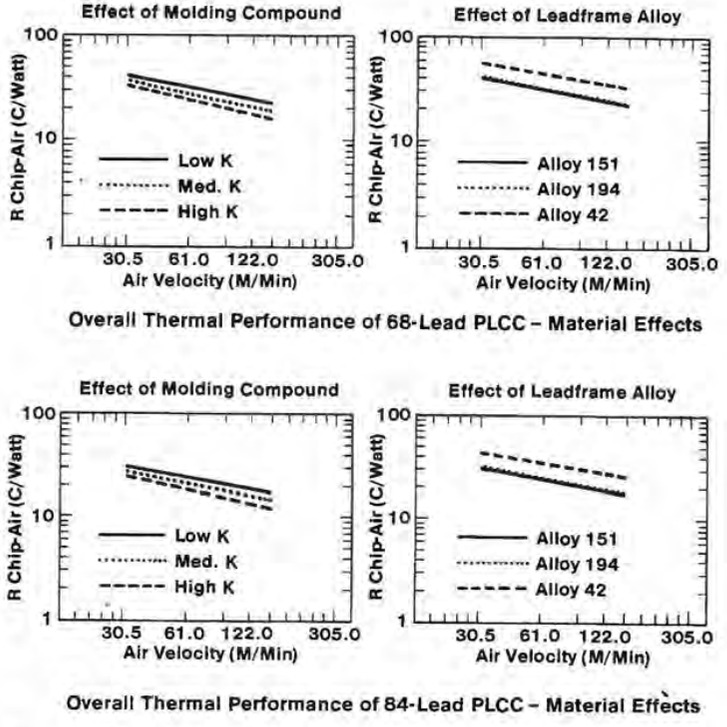


Figure 8-2. Overall Thermal Performance of 84-Lead PLCC - Material Effects.

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sives have been developed and are flexible enough to absorb the strain developed between chip and copper.

8.3.5 Mechanical Design

Considerations in lead frame mechanical design are:

1. Ease of fabrication.
2. Indexing features for package assembly.
3. Chip-attachment substrate and gold wire span.
4. Coplanarity for wire bonding.
5. Lead-locking and moisture-inhibiting configuration.
6. Stress relief.
7. Plastic support matrix.
8. Terminal lead and standoff configuration.

Ease of Fabrication: Figure 8-3 illustrates design rules for considerations 1, 3, and 4. Specifying a single temper for strip feedstock avoids proliferation of expensive progressive-stamping dies.

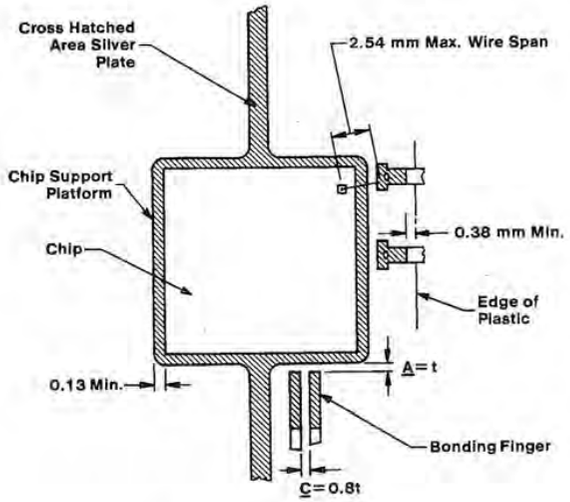


Figure 8-3. Lead Frame Clearances, Wire Span, Plating, Limits, and Coplanarity.

Indexing Features: Design of lead frame strips must consider the package-assembly system. Tooling holes are located along frame-strip-edges. These mate with the transfer-mechanism pins, which are part of the assembly equipment, and include chip bonders, wire bonders, molds, auto-inspection stations, trim and form equipment, and marking machines. In-process storage and transport-magazine design depend on the frame-strip length.

Lead Locking and Moisture-Inhibiting Configurations: The bond between lead frame and plastic is mechanical. Therefore, any protrusion or hole on the frame that serves to lock the terminal leads within the cured molding compound is desirable. Several mechanical features have been developed to inhibit moisture penetration along the plastic lead frame boundary. These, along with lead-locking configurations, are shown in Figure 8-4.

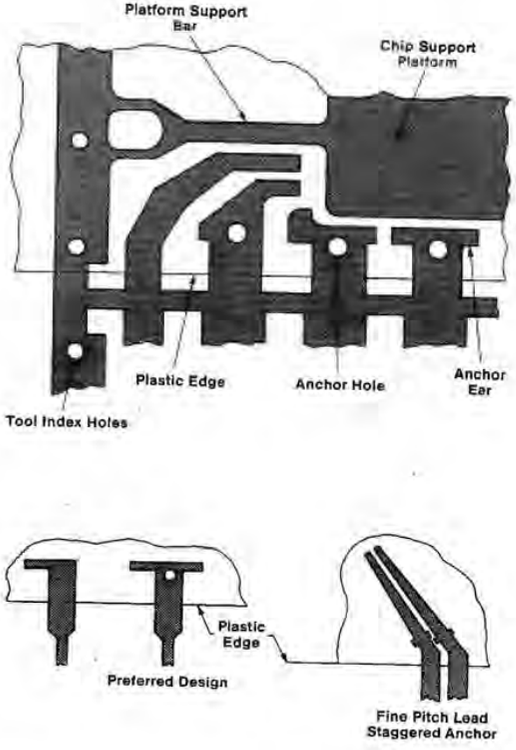


Figure 8-4. Typical Dip Lead Locking Design.

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Stress Relief: Lead frames cause two types of stress that can be reduced by design. The most severe one is due to the inherently large thermal coefficient of expansion (TCE) mismatch between the plastic and the metal. In the severe cases that may occur during thermal-shock testing, bending of the package can reach sufficient proportions to impair the operation of the device. Such bending stress on the chip surface can be minimized by locating this surface on the neutral bending axis of the package. The chip-attach platform is offset downward to accomplish this effect, as shown in Figure 8-5.

The other stress condition encountered is caused by stress concentration points located on the bottom edges of each stamped lead frame, as depicted in Figure 8-5. When a stamping punch drives through the sheet metal to form a radius, it tends to pull material with it by friction. Conversely, on the exit side some metal is extruded, forming a burr. Burrs are sharp and act as

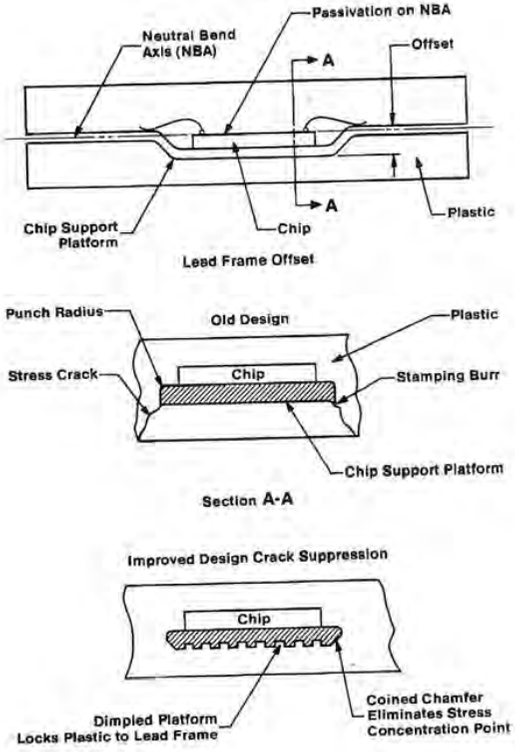


Figure 8-5. Lead Frame Offset — Crack Suppression.

stress concentrators. Once cracking occurs, the cracks tend to propagate from the edge burrs on the chip-attach platform toward the bonding figures, forming in the process a water-ingress channel. These internal cracks are insidious since they cannot be detected by conventional x-ray techniques. Burrs are generally removed by adding a coining station to the progressive die set. The burr is in effect forged into an edge chamfer.

Plastic Support Matrix: The lead frame functions as a reinforcement matrix for the molding compound, literally something for the plastic to hang onto while forming the module body. Top and bottom sections of a plastic module hold together because the plastic is contiguous between sections. As the metal area is increased, the force needed to shear top from bottom decreases to a point where fracture occurs along the metal/plastic boundary during lead-bending or soldering operations.

The ability to retard water penetration along the metal/plastic interface is a function of plastic shrinkage around the metal lead frame members. Generally the more plastic coverage, the greater will be the compressive forces. An ideal plastic-to-metal ratio for lead frame design is given by

$$A_m/A_p \leq 1 . \qquad [8.1]$$

where A_m = metal area and A_p = plastic area.

Terminal Leads: There are four lead configurations used on molded plastic packages: integral standoff, gull wing, J-Bend, and butt joint, as illustrated in Figure 8-6. Dual-in-line modules use integral-standoff leads. They are designed to give clearance between the module bottom and the printed circuit board surface for cleaning. Integral standoffs should be designed to provide a clearance between the module and the board of 0.38 mm minimum when placed in a 1.09 mm maximum diameter plated-through-hole. Lead configurations for surface mounting require multiple bends. Therefore, tempers ranging from one quarter to one half hard are chosen to avoid cracking at the bend radii.

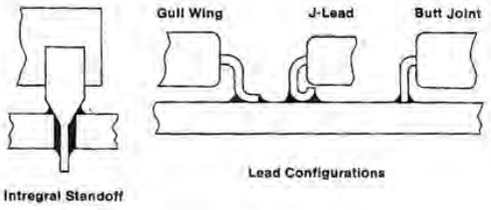


Figure 8-6. Lead Configurations.

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8.3.6 Lead Frame Fabrication

Lead frames are either chemically milled or mechanically stamped from rolled strip stock. Typical strip thickness is 0.25 mm, with thinner material (0.20 mm) used on high lead count packages such as the 84-pin PLCC and quad flat pacs. Chemical milling is a process that uses photolithography and metal-dissolving chemicals to etch a pattern from metal strip. The process begins by punching registration holes in the strip, then coating both sides with a photoresist material. The resist is exposed to ultraviolet (UV) light through a photo mask, developed, and cured. The lead frame is now delineated with cured photoresist and is ready for etching. Chemicals such as ferric chloride or ammonium persulfate are sprayed onto both sides of the strip to etch away exposed metal — leaving the lead frame intact. Chemically milled lead frames cost more than stamped frames, although the corresponding tooling costs are much lower. Furthermore, chemical milling provides a faster turn-around time (typically, one month compared to 6 to 12 months for stamping). This process is ideal for packages under development, short production runs, and frames too complicated for stamping.

Stamped lead frames are fabricated by mechanically removing metal from strip stock with tools called **progressive dies**. The energy required to shear metal is directly proportional to the length of shear. Lead frames have large shear lengths per unit area. Therefore, a large amount of energy is required to stamp a full frame with one press stroke. Progressive dies are usually made of tungsten carbide and are arranged in stations. Each station punches a small area of metal from the strip as it moves through the die set. Dies for complex lead frames can have up to 16 stations. This is shown in Figure 8-7.

Progressive stamping dies are expensive, currently about $135,000 for a 40-pin DIP lead frame, and take 6 to 12 months to design and build. Trouble shooting the die before introducing it to the production line is usually required. Fortunately, stamping rates can be rather impressive, with modern presses able to turn out 900 to 1,000 frames per minute. Stamped frame costs are a factor of 10 lower than etched parts, so tooling costs can be amortized rapidly.

8.3.7 Plating

Some lead frames in the late sixties were fully plated with gold or silver. Cost pressures over the years have caused the plating to recede, until only the chip-attach platform and bonding finger ends remain plated with silver. Silver spot plating is done with conventional plating baths. Spot dimensions are controlled by masking and should be specified so the silver limit is 0.38 mm (minimum) from the outer surface of the module. Silver may be plated di-

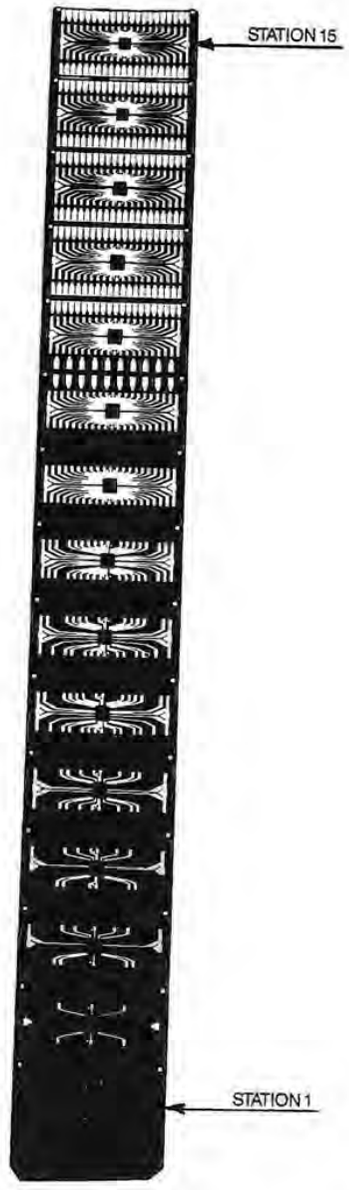


Figure 8-7. 40-Pin Dip Lead Frame, 15-Station Stamping Die Proof.

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rectly onto iron-nickel alloy surfaces, but a nickel underplate is recommended for copper alloys.

8.3.8 Chip Attach

Both silicon/gold eutectic and polymer bonding are used to bond the chip to the lead frame. The operation begins with the loading of the film ring holder, with sawed wafer attached, onto the index stage of the bonding machine. Lead frames are then fed from magazines along a track to a heater block. A small square of silicon/gold alloy (6% *Si*, 94% *Au*) is cut from a feed ribbon and transferred to the chip support platform. An optical scanner detects a good chip on the sawed wafer causing a probe to push the chip above the wafer plane where a collet picks it up, and transfers it to the heated chip support platform. Chip and eutectic are now scrubbed together by the collet, forming a hard alloy bond. Heater temperature is approximately 420°C. Total cycle time for eutectic bonding is about 6 to 8 seconds.

Polymer bonding is faster than eutectic with a cycle time of 2 seconds. Feed mechanisms for polymer bonding machines are the same as eutectic bonders. However, lead frames are not heated. Silver-filled epoxy or polyimide adhesive paste is transferred to the chip support platform by a print head, and the chip is pressed into the paste immediately after printing. The chip attach adhesive properties are listed in Table 8-5. Chip bonded lead frame strips are loaded into transport magazines. Eutectic bonded frames go directly to wire bonding while magazines containing polymer-bonded frames are routed to ovens for adhesive curing. The curing atmosphere is dry nitrogen, and typical schedules are one hour at 150°C for epoxies, and 30 minutes at 150°C, followed by 30 minutes at 275°C for polyimides.

More recently, improved silicone gels were introduced as an alternative means of fastening the silicon die to the support platform [32]. Pin-grid arrays (PGA) soldered on standard FR-4 boards were used as test vehicles. In this case, the chip was initially bonded with the gel to the epoxy base of the PGA. After wirebonding, the entire PGA cavity was encapsulated with the same gel. Thus, the chip resided in a substantially compliant medium, and could readily withstand thermal and environmental stresses. The higher reliability achieved resulted from using the same gel throughout. Previous attempts at bonding the die with an epoxy-based adhesive, followed by die coating with a gel were unsuccessful for two reasons. First, improper cure conditions can leave low molecular weight amine residues in the epoxy. The unbound amine leached out under environmental testing and reacted adversely with the silicone gel. and, second, although the stiffer epoxy can hold the chip rigidly to the base, thermal mismatch would generate significantly higher stresses ultimately harmful to the integrity of the device.

8.4 ENCAPSULATION MATERIALS

Molding compounds are mixtures of various chemical compounds that are formulated for making molded plastic products. Thermosets and thermoplastics are two general categories of plastics used in molding compounds. Thermoplastics can be remelted and reused after molding while thermosets cannot. Molded IC packages use thermosetting compounds exclusively, although there is some development underway with thermoplastic materials. This section is concerned mainly with conventional thermosetting resins. The polymer chemistry of epoxies as it pertains to properties affecting semiconductor packaging is also described briefly. A more rigorous and thorough treatment of epoxy chemistry can be obtained from *The Handbook of Epoxy Resins* by Lee and Neville, from which certain chemical descriptions have been excerpted [33].

Phenolics, bis-phenol epoxies, and silicones were the three types of molding compounds in use when production of plastic ICs began. The molding characteristics of these compounds was excellent. Presses produced packages with minimal cosmetic defects, high yields, and thus far, unmatched production rates. Black, smooth, and shiny packages, albeit aesthetically pleasing, however, were not a guarantee of reliability. Each of these compound types had deficiencies that caused the modules to fail on reliability stress tests and in the field.

ICs molded in phenolic had unacceptable numbers of corrosion failures on temperature-humidity stress tests. Propensity for early corrosion failure was caused by phenolic properties such as generation of ammonia within the compound during postmold cure, relatively high levels of ionic contaminants (e.g., *Cl* and *Na*), and high moisture absorption.

Molding materials based on diglycidyl ether of bisphenol-A (DGEBA) were popular for molding IC packages in the sixties. DGEBA is produced by reacting epichlorohydrin with bisphenol-A. Epichlorohydrin is made from propylene and chlorine. During the DGEBA reaction, excess chlorine is produced. Most of this is removed during manufacturing by treating the resin with sodium hydroxide. The chlorine content is further diluted in the compound formulation process by the addition of other materials to the base resin. Processes used during the 1960s were successful in reducing hydrolyzable chlorine levels to about 400 ppm.

The thermal coefficient of expansion of the plastic changes markedly when an inflection point called the **glass transition temperature**, T_g, is reached on the expansion rate curve as depicted in Figure 8-8. Bis-A resin-based molding compounds have T_gs in the range of 100°C to 120°C (Fig. 8-9).

After assembly, the potential thermal stresses that an IC package might incur result from electrical testing both at ambient temperature and 125°C, temperature-cycling tests (0°C to 125°C) during reliability qualification and at life-test incoming inspection, and on/off cycling in the application.

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Table 8-5. Chip Bonding Adhesives (Part 1 of 2).

Supplier	Type No.	Resin Type	Filler Type	Components	Electrically Conductive
Epotek	H20E	Epoxy	Silver	2	Yes
	H20E-175	Epoxy	Silver	2	Yes
	H35-175M	Epoxy	Silver	1	Yes
	H41	Epoxy	Silver	1	Yes
	H44	Epoxy	Gold	1	Yes
	H81E	Epoxy	Gold	2	Yes
	P-1011	Polyimide	Silver	1	Yes
Amicon	C-840-4	Epoxy	Silver	1	Yes
	C-868-1	Epoxy	Silver	1	Yes
	C-940-4	Polyimide	Silver	1	Yes
	C-966	Polyimide	Silver	1	Yes
	C-990	Epoxy	Silver	1	Yes
	CT-4042	Epoxy	Silver	2	Yes
	ME-868	Epoxy	Oxide	1	No
Ablestik	71-1	Polyimide	Silver	1	Yes
	71-1LM1	Polyimide		1	Yes
	84-1LM1	Epoxy	Silver	1	Yes
	84-1LM1	Epoxy	Silver	1	Yes
	84-1A	Epoxy	Silver	1	Yes
	84-1LM1S1	Epoxy	Silver	1	Yes
	941-3	Epoxy	Silver	1	Yes

Table 8-5. Chip Bonding Adhesives (Part 2 of 2).

Maximum Cure Temperature °C	Lap Shear Strength kg/mm²	Remarks
175	1.06	Two-component epoxy adhesive with high electrical & thermal conductivity
180	1.06	Low ionic impurity, dual T_g version of H20E
180	1.27	Similar to H20E except single component, no mixing required
150	2.11	Single-component epoxy adhesive with low cure temp & high lap shear strength
150	2.11	Single-component, gold-filled epoxy adhesive
150	0.91	Two-component gold-filled epoxy adhesive
150	0.50	Low cure temperature polyimide adhesive
200	1.6	Low ionic impurity epoxy adhesives can be pre-cured as B-stage on lead frames
180	1.6	Low ionic impurity epoxy adhesive with low cure temp. can be B-staged
270	1.45	Low ionic impurity polyimide adhesive. Excellent heat resistance to 400°C
180	2.5	Low temp. cure polyimide adhesive with low ionic impurities
275	1.55	Very rapid cure epoxy adhesive, cures on wire bond heater block
150	1.6	Low ionics two-component epoxy adhesives
180	1.6	High thermal conductivity, electrical insulation epoxy adhesive
275	0.70	General purpose polyimide direct-attach adhesive
275	2.04	Very low ionic impurity version of 71-1
150	4.58	Low temp. cure conductive epoxy adhesive with low levels of ionic impurities
150	4.30	High, thermal conductivity version of 84-1LM1
200	4.23	Rapid cure version of 84-1LM1
200	2.11	Low viscosity, low ionic version of 84-1LM1
175	2.11	13-stageable epoxy chip adhesive for pre-printing of lead frames

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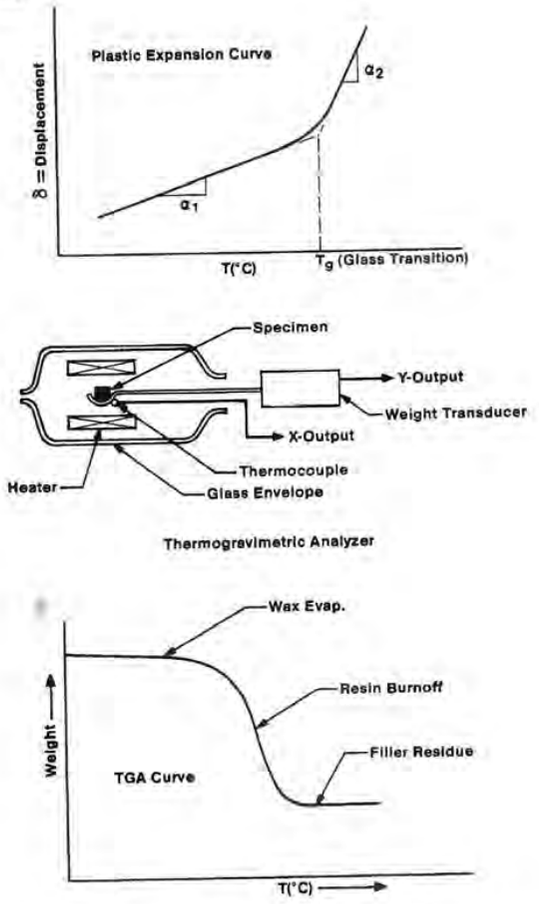


Figure 8-8. Dilatometer/Thermogravimetric Analyzer.

Packages molded with bisphenol-A compounds exhibited a failure mode called **windowing**. As the module ramped up in temperature, the plastic would pass through its T_g, thereby increasing the expansion rate approximately three times. The ensuing motion resulted in a higher stress level on the wirebonds, which can be ultimately pulled away from the bond pads. As the module cooled down, the same ball bonds recontacted the chip, and the part would test electrically good. This time, however, when the module temperature increased again, the wirebonds would open (or close if the temperature

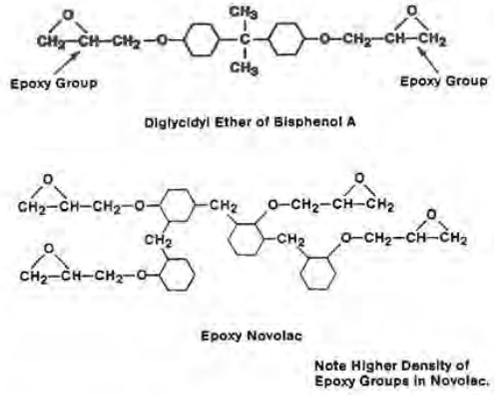


Figure 8-9. Diglycidyl Ether of Bisphenol A/Epoxy Novolac.

dropped) within a temperature range or "window." This was not a popular phenomenon among machine program managers. The low T_g giving rise to the windowing failure mode led to the demise of bisphenol-based molding compounds in the early 1970s.

Silicone resins have many of the attributes of an ideal semiconductor molding compound. They are synthesized from silicones, a pure compound with respect to ionics like chlorine, sodium, and phosphorus. More discussion on silicones can be found in a subsequent section. Silicones possess relatively low T_g (typically between $-20°C$ to $-70°C$), which are relatively hard to discern during typical differential scanning calorimetry runs. Furthermore, these resins are so slippery that an internal mold release is usually not required. This last drawback, poor adhesion with the device and the metallization, was the compound's undoing. Indeed, modules molded with silicone can be easily ejected from the mold, but this self-lubricating characteristic produced a poor seal between the lead frame and the resin. Silicone molded modules never passed salt spray tests, were susceptible to flux penetration during wave soldering, and had the same windowing failure mode as the bisphenols. The latter cannot be explained as a function of low T_g, but was caused by shearing stresses induced by the plastic sliding over the lead frame and chip surface during temperature cycling.

A molding compound was needed that had a high T_g and low moisture permeability. Epoxy novolac resins have these attributes.

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8.4.1 Conventional Materials

8.4.1.1 Epoxy Novolac–Based Molding Compounds

Novolac-based molding compounds were in use long before plastic IC packages were introduced. Designs that required high heat distortion temperatures used these compounds. Semiconductor grade novolacs were not developed until the early 1970s. Novolac resins are produced by the reaction of phenol and formaldehyde in the presence of acid. Alkyl-substituted phenol may be used as a starting material. Epoxy novolacs are made from epichlorohydrin via the same route as the bisphenols. The resins are solid at room temperature, have high crosslinking density and functionality. The chemical structure of a novolac epoxy is shown in Figure 8-9.

High crosslinking density gives the resin a low moisture-absorption rate while high functionality imparts heat stability and a correspondingly higher T_g. Novolac-based molding compounds generally have T_g of 150°C or greater. Epoxy novolac molding compounds, specifically formulated for semiconductor packaging, have replaced phenolics, bisphenol epoxies, and silicones, and are the major compound used for IC molding today.

Formulation: Molding compounds are mixtures of various materials formulated for a specific molding application. A novolac-based, semiconductor-grade compound typically consists of:

1. Cresol novolac epoxy resin (25.5 – 29.5%).
2. Accelerator.
3. Curing agent.
4. Inert filler (68 –72%).
5. Flame retarder (2%).
6. Mold-release agent.
7. Colorant (0.5%).

Resin: The epoxy novolac resin is the base upon which the molding compound is built. It is the organic binder that, when cured, holds all the constituents together and imparts the inherent characteristics of high T_g: shrinkage on cure, low moisture absorption, and chemical inertness to the plastic package.

Bulk resins are purchased by formulators from large chemical concerns which guarantee minimum levels of hydrolyzable chlorine. Purification technology from the late 1960s through the 1970s produced resins that had high chlorine contents (up to 3%). Further processing by the formulators reduced this level in the final molding compound to approximately 400-800 ppm. The drive to bring failure rates of plastic packages down to the levels of their hermetic counterparts accelerated the development of resin-purification technology by the compound formulators. Resin-refinement methods are

proprietary, but small-batch processing with tight controls plays a significant role in reducing ionics. Suppliers of IC molding compounds now specify chlorine levels of less than 30 ppm.

Accelerators: Molding compounds are blended in two parts, A and B, before final mixing and grinding. The A part usually contains the resin with the desired amount of fillers, while the B part is a mixture of resin hardener and accelerators (also commonly known as kickers). These compounds act as catalysts to initiate and accelerate cross-linking of the epoxy when heat and pressure are applied in the molding process. Accelerators affect the set or gel time of a molding compound.

Curing Agent: Besides affecting the viscosity and the reactivity of the final compound, curing agents (or hardeners) also govern the nature of the dominant chemical bonds established and the final extent of crosslinking obtained. Depending on the nature of the resin and hardener in the system, a wide latitude of concentrations exists — from as low as 1 part of hardener per 100 parts of resin (1 phr) to 100 phr. By-products are not generated under normal conditions. The formation of an epoxy network can proceed via three general and well-characterized routes [33]:

- Crosslinking of the matrix via various functional groups of the hardener.
- Linkage of epoxy groups with aliphatic or aromatic hydroxyls.
- Direct linkage between the epoxy groups through self-polymerization.

The most widely used hardeners are of the amine or acid anhydride type. For the conventional bisphenol-A and novolac types, aliphatic amines are generally used to produce room-temperature curing systems with relatively low heat-deflection temperatures. Aromatic amines, on the other hand, can be blended to yield products with higher thermal performance and chemical resistance. Many of the aromatic amines, however, are solid at room temperature and will require elevated temperatures for processing and curing. Such criteria have to be considered, because the necessary postcuring step will introduce extra stresses when carried out at high temperatures. The functionality of the amine is determined by the number of active hydrogens. Each hydrogen atom attached to nitrogen opens up an epoxy ring. In the process, primary amines are converted to secondary amines with the corresponding hydroxyl. These secondary amines react in turn with other epoxy groups to form tertiary amines.

For electronic applications, liquid anhydrides have considerable utility, especially the cyclic types. There is typically no reaction between the anhydride and the epoxy group until the ring is opened. An ester or another linkage can be established from the combination of an epoxide group with a carboxylic group or a hydroxyl group, respectively. Or alternatively, the anhy-

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dride ring may be opened by a hydroxyl group. Such reactions are rather sluggish at room temperature but proceed at faster rates at high temperatures. An accelerator or catalyst, usually a tertiary amine, is also blended in minute concentrations to speed gel and curing times. The optimum amount is critical and certainly depends on the cure schedules and the resin/anhydride combination. The principal role of the catalyst is to initiate the polymerization and the subsequent crosslinking of hardeners at appropriate molding conditions. Catalysts generally fall within one of the following three categories [34]: 1) Lewis acids (e.g., zinc or stannous octoate); 2) Lewis bases (e.g., phosphorus compounds, urea derivatives, imidazoles, and tertiary amines); 3) organometallics (e.g., metal acetyl acetonates). For the anhydride curing process, imidazoles and their derivatives seem to predominate over metal complexes, phosphines, and Lewis acids.

Deviations from the prescribed stoichiometry usually affect the high-temperature performance. Anhydride-cured products provide characteristically high heat resistance (and correspondingly high T_gs) but are fairly brittle. Nevertheless, the latter drawback can be corrected with a judicious selection of flexibilizers and fillers. Modifiers, for instance, can enhance some physical properties of the final crosslinked network at the expense of others. Thermal-shock resistance and flexibility, for instance, must be balanced against high glass transition temperature and chemical resistance. Both reactive and nonreactive types can be used at ratios up to one. Carboxyl-terminated butadiene acrylonitrile rubbers (CTBNs) are often blended with nitrogen-containing curing agents as additives to certain epoxy resin systems. The rubber precipitates into a two-phase structure, which imparts flexibility and toughness to the matrix. Nonreactive modifiers, on the other hand, lower cost considerably. When blended to an epoxy system, however, gross reduction in the cured resin properties is recorded. As a result, such additives are rarely used in formulations for plastic packaging.

Fillers: Epoxy resins and curing agents cannot be used alone for molding ICs. They must be modified by the addition of inert materials called **fillers**. Specific desired properties are obtained from the inclusion of fillers into an epoxy resin formulation. With the current concern about shrinkage stresses inside the package, cost, and alpha particle-induced errors, emphasis has been placed on obtaining a more fundamental understanding of the nature of the fillers needed, the aspect ratio of a typical particle, the volume fraction blended, and the resulting mechanical properties. Inert silicas are fairly common in electronic packaging. For other less rigorous applications, calcium carbonates, calcium silicates, talcs, micas, and even clay can be incorporated into the bulk system. Some of the more important effects of filler inclusion are:

- Low exotherm peak — Silica and other common bulk fillers have relatively higher specific heats ($\simeq$ 0.19 cal/g°C) than the resin ($\simeq$ 0.072 cal/g°C). Much of the exotherm is thus used up in heating the particles during the polymerization phase.
- Improved thermal conductivity — Once a critical volume fraction of fillers has been reached, the composite system will also display enhanced thermal conductivity. Interparticle contact must exist for efficient heat transfer to occur through the sample. Particle shape, size, concentration, and distribution are important considerations, and maximum loading is generally sought after. Elongated particles induce a higher occurrence of paths for thermal transfer. However, even at loadings extremely high that processing would be difficult, the increase in thermal conductivity is considerable over the base resin (two to three orders of magnitude), and yet still much lower than the metallic counterpart.
- Enhanced thermal-shock resistance — Because the fillers occupy a large volume of the system and do not either expand or contract substantially, the total shrinkage of the resin is reduced. A corresponding decrease in the coefficient of thermal expansion of the filled system greatly promotes thermal stability and thermal-shock resistance during any wide temperature fluctuation.

Powdered fused quartz (SiO_2) is currently the primary filler used in IC molding compounds. Fused quartz powder is obtained by melting pure silica sand and casting into boules. The boules are then pounded and crushed until the desired particle size is reached.

Neat phenol-cured cresol novolacs have expansion rates of approximately 400-500x10^{-7}/°C. Addition of 68-70% silica filler (by weight) reduces the TCE to 200-240x10^{-7}/°C. The need for low-stress compounds increases as chips get larger. Adding more filler to decrease the TCE of the resulting composite is an obvious solution but rather risky. More filler decreases the tensile strength of the compound while increasing water permeability. Packages molded with compounds modified in this manner still exhibit cracks during temperature cycling. Lower stress compounds are best achieved by modifying the base resin with flexibilizer to reduce the elastic modulus while increasing filler content slightly (1-2%).

Reduction of package thermal resistance is an important design goal, since cooler chips imply lower failure rates. Molding compounds are excellent electrical and thermal insulators. An increase in thermal conductivity, k, in the molding compound leads to a decreased package thermal resistance. Fillers increase k, some more than others. Alpha quartz, a crystalline form of SiO_2, is more thermally conductive than fused quartz, and is added to enhance the thermal conductivity of molding compounds. Unfortunately, alpha quartz expands thermally at a greater rate than its fused counterpart. Indeed, it was

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found that larger packages (e.g., 24-pin DIP and up) molded with compounds modified with alpha quartz sometimes crack in half when thermal stress is encountered. A more efficient, less risky method for achieving low thermal resistance is to use copper alloy lead frames, as shown in Figure 8-2.

Fillers such as powdered SiO_2 tend to increase water absorption rates through the cured compound. This is caused by the wicking action of the filler particles, and the process is analogous to mixing sand with impervious clays in order to increase water permeation in soils. Fillers are treated with silane coupling agents to retard wicking. Processing fillers with coupling agents is not easy. Theoretically, the optimum coupling results are obtained with coatings that are a monolayer thick. This can rarely be achieved in practice. Most filler treatment processes are proprietary. Coating is probably accomplished by suspending the filler particles with compressed air in a fluidized bed. Vaporized coupling agent is introduced to the fluidized powder, where it coats each particle uniformly.

The section on Plastic Molded IC Package Design mentioned alpha radiation protection for memory chips. The source of alpha particles in plastic packages is thorium or uranium present as impurities in the silica filler. Alpha quartz has a relatively high concentration of *Th* and *U*, and is ruled out as a filler material for low-alpha molding compounds.

Development of low-alpha molding compounds was started in 1980. A source of silica, free of radioactive elements, was found in Brazil. What was once probably a high-quality sand pit became a gold mine overnight as formulators rushed to buy the unique filler. SiO_2, produced as a by-product of silicon refining and chemically vapor-deposited from silanes, is also free of alpha-emitting elements. Low-alpha molding compounds are now available with alpha particle fluxes below the measuring capability of the best radiation-detection equipment. Of course, someone has to pay for single sources of supply and other refinements. A low-alpha compound is eight times more expensive than standard compounds. However costly these new compounds are, their use can be justified when chip coating operations are eliminated.

Flame Retarders: Product safety requirements for plastic modules used in electronic equipment specify an Underwriter's Lab flame retardant ratio of 94V-O. This can be met only by the addition of flame retarders such as tetrabromobisphenol-A and antimony trioxide to the molding compound. Recent developments have replaced halogenated bisphenols with brominated novolacs to achieve better heat stability [35].

Mold Releases: Molded parts are designed with draft angles to facilitate ejection from the mold cavity. A compound that adheres to the mold surface causes defective parts and frequent mold repairs. Mold releases are added to prevent cured compounds from sticking to the cavity walls. Carnauba, a natural wax extracted from a palm tree, was a commonly used release agent but is now being replaced by synthetic ester waxes.

Colorant: To borrow a phrase from Henry Ford, "They can have any color make they want so long as it's black." Similarly, black also seems to be the preferred color for plastic IC modules. The black colorant is either lampblack or an organic dye.

Mixing Process: Molding compounds are created in automated processing plants that take raw materials and blend them into a molding powder with the properties required for molding ICs. Usually, the formulation process is proprietary. A representative process flow is given in Figure 8-10.

Blending is a batch process and is lot-controlled. Shipping lots range from 2,000 to 18,000 kg. A small sample is generally taken from each lot and sent ahead to the customer for lot-control testing. Resin, hardener, and accelerator are in close proximity after final grinding, and slow curing begins at room temperature. To retard this reaction, the molding compound must be refrigerated until needed at the molding press. A list of IC grade molding compound suppliers is given in Table 8-6.

8.4.1.2 Silicones

Although silicone materials have been applied to IC encapsulation since 1969 [36], they have not quite gained the same popularity enjoyed by their epoxy counterparts. Nevertheless, for applications requiring specific properties such as high heat resistance, low-dielectric properties, low-temperature properties, and low moisture absorption, silicones tend to outperform the best epoxies [37, 38]. Silicones, for instance, can generally maintain their useful characteristics up to 400°C — a range that would be hard to achieve even with highly filled epoxies. This is brought about by the silicon-to-oxygen building block, which is much stronger than the normal carbon-to-carbon linkage found in most organic resins such as polyesters and epoxies. At the other temperature extreme, whereas other materials become brittle and crack-prone, silicone rubber remains stable down to −60°C. Similarly, a certain extent of hydrophobicity and ensuing moisture protection can also be achieved by coating surfaces with layers of silicone derivatives [39]. The current trend toward higher circuitry density and reliability underscores the need to gain more insight into the cure mechanism, surface chemistry, and level of ionic contaminants associated with silicone resins.

The Rochow process is still the major commercial source of silicone polymers [40]. In this process, a heated bed of copper metal and pure silicon is

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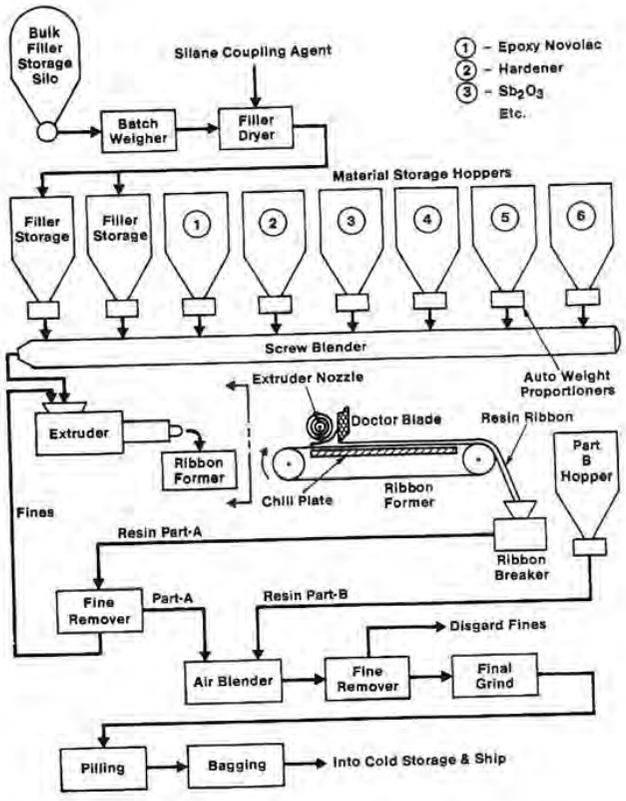


Figure 8-10. Molding Compound Formulation Process.

exposed to a stream of alkyl or aryl monohalide. The resulting mixture of organohalosiloxane complexes is collected, purified, and catalytically hydrolyzed into a blend of cyclic siloxane oligomers and linear hydroxy end-blocked siloxane polymers. The cyclic oligomers are subsequently ring-opened into more linear polymers. The reaction conditions can be tailored so that siloxane polymers of different molecular weights can be generated. Resins with viscosities from a few to the 10,000 Pa·s range have been produced. The latter form, however, is not suitable for coating or encapsulation, often requiring dilution with an appropriate solvent such as xylene or toluene. Use of solvent-diluted materials raises two major drawbacks. First, a high degree of

shrinkage necessarily ensues from the evaporation of the solvent, and, second, an improper rate of evaporation might produce varying degrees of porosity. These cavities form weak insulating domains within the encapsulation since dielectric breakdown occurs more readily in air-filled gaps. Thus, to ensure good coverage and protection, some form of crosslinking reactions, preferably without the use of solvents, is needed.

For electronic packaging, polymerization of the siloxanes through the alkoxide route is often preferred. One of the methoxy end groups reacts with a substrate hydroxyl end group. This step generally requires the catalytic effect of some organotitanates or organotin compounds. A methanol molecule is then released to produce subsequently a silicon-oxygen-substrate linkage. Similarly, at the other end of the silicone chain, moisture present in the air will react with another methoxy end group. An additional methanol molecule is liberated while the resultant silicone-hydroxy end group can react freely with neighboring methoxy end groups to propagate the network formation. Under mild basic or acidic conditions, these silanol end-capped polymers are also susceptible to condensation. Some typical alkoxy silanes include, for instance, tetraethoxysilane, tetrapropoxysilane, methyltriethoxysilane, and methyldiethoxysilane. On the other hand, tin (II) octoate and dibutyltin-dilaurate are effective catalysts. Silanol end-capped polydimethysiloxanes are supplied either in one or two parts. Single component systems are usually formulated with acetoxysilanes, such as methylacetoxysilanes. With binary systems, one of the components is, or contains, the catalyst. In this case, the two components are mixed shortly before use. To extend the working life of the systems, a solvent dispersion of each of the two components using xylene or some other aromatic solvents can be made prior to use.

In some instances, the catalyst can be selected so that curing only takes several minutes. Generally, however, depending on the encapsulation thickness, polymerization times of several hours are more typical. Tack-free parts are usually obtained after 24 hours. Raising the temperature will only accelerate the reaction to a certain extent. Very high temperatures should definitely not be used before the coating is at least partially cured. Attempts to do so may guarantee one of the following two adverse effects: an external temperature close to the boiling point of the curing agent will cause the latter to evaporate progressively and, consequently, polymerization will not proceed to completion; less than optimal properties will be obtained. Alternatively, the solvent used for dilution may also escape at such high rate that blisters and cavities might result in unacceptable parts.

Substrate hydroxyls are readily available from water adsorbed onto most surfaces at room temperature. The energy of adsorption is sufficiently high that even heat treatments of up to 400°C will not remove all existent groups [41].

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Table 8-6. Properties of Semiconductor Molding Components (Part 1 of 2).

Supplier	Compound No.	Thermal conductivity W/m/°C	Thermal expansion 10^{-7}/°C	Flexural strength GPa	Flexural modulus GPa
Sumitomo	EME-1100-T	0.67	200	0.14	15.66
	EME-1100-H	0.67	200	0.14	15.66
	EME-1100-K	0.67	200	0.14	14.19
	EME-6200	0.67	200	0.13	12.72
	EME-6300	0.42	170	0.13	12.23
	EME-9100—XK	0.67	200	0.14	14.19
	EME-9200	0.67	200	0.13	12.72
	EME-9300	0.42	170	0.13	12.23
	EME-5000LS	0.67	200	0.15	14.68
Plaskon	3100	1.0	270–750	0.14	14.68
	3100LS	0.71	210–600	0.14	14.68
	3200	1.0	270–750	0.15	14.68
	3200LS	0.71	220–600	0.15	14.68
	3300	1.0	270–750	0.15	14.68
	3300LS	0.71	210–600	0.15	15.81
	3300SH	0.71	210–600	0.15.7	15.81
Hysol	MG15f	0.71	250–700	0.12	13.76
	MG35F	1.46	260–750	0.13	14.44
	MG36f	0.75	170–700	0.13	13.76
Nitto	HC10-2	0.63	200–700	0.15	13.70
	HC20-2	0.92	240–700	0.15	13.70
	HC30-2	1.46	260–700	0.15	14.68
	HC50-2	1.97	250–700	0.15	14.68
	MP119	0.63	180–650	0.13	12.23
	MPX-75	0.71	200–650	0.16	14.19
	MP150	0.71	160–740	0.13	11.74
	MP150-164	0.71	160–740	0.13	11.74

Sorption and diffusion of water in silicone rubber involve very little interaction between the polymer and the water. However, at high relative humidities, clustering of the water molecules has been recorded [42].

8.4.2 Control Testing

Tests are performed on molding compounds to ascertain design parameters, assure lot uniformity, guarantee reproducible moldability, and analyze package construction.

Test types, their purposes, and comments are given in Table 8-7. Examples of curves and test equipment for two thermal tests are shown in

Table 8-6. Properties of Semiconductor Molding Components (Part 2 of 2).

Extractable Chlorine ppm	Flame Rate UL	T_g °C	Remarks
50	94-VO	155	General purpose molding compound for DIPs with small chips
20	94-VO	155	Same as above, but better humidity resistance
20	94-VO	155	Better temperature-cycle performance
25	94-VO	165	Low stress M. C. for large DIPs & PLCCs
25	94-VO	165	Very low stress compound for SO & large thin packages
20	94-VO	155	High purity, low stress, low alpha particle count for molding DRAMs
25	94-VO	165	Lower stress than 9100-XK low alpha particle count for DRAMs in PLCC & SOJ
25	94-VO	165	Lowest stress & low alpha particle count for DRAMs in thin packages
20	94-VO	135	Low-stress molding compound for SOPs that are solder dipped
30	94-VO	150	Standard molding compound for ICs & discretes
30	94-VO	150	Low-stress version of 3100 for resistor networks & MOS devices
20	94-VO	150	General purpose IC molding compound
20	94-VO	155	For large chips in DIPs or PLCCs
20	94-VO	150	For SMT packages & larger DIPs
20	94-VO	155	For gate arrays & microprocessors
20	94-VO	155	For large SMT packages (68-, 84-PIN PLCC) & QFPs
20	94-VO	190	Anhydride cured. Used for high-voltage chips (50-90V)
10	94-V0	160	For high-power discrete
10	94-VO	160	Low-stress compound for large chips in small packages
20	94-VO	162	For small DIP, thin flat packages
20	94-VO	161	28–42-lead chips
20	94-VO	162	Discrete devices high voltage; ICs >30 volts
20	94-VO	170	Power transistors, power packages
10	94-VO	170	Low stress and low ionics for SOIC packages
25	94-VO	151	Good adhesion to lead frame for SMT packages
15	94-VO	150	Very low stress for SOIC & PLCCs
15	94-VO	158	Same as MP150 except low alpha particle count

Figure 8-8. In general, the most important criteria for the package designer are the glass transition temperature, the thermal coefficient of expansion, the hydrolyzeable chloride content, and the moldability of the resin. The last parameter, moldability, deserves some comment. A molding compound may test perfect for an IC package application, i.e., high T_g, low *Cl*, and acceptable stress level, but mold atrociously. Compounds of this nature are bound to fail for reason of yield and reliability. Poor moldability leads to pushing specifications to their limits in the mold room with negative effects on product field performance, as shown in Table 8-7.

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Table 8-7. Molding Compound Tests.

Test Type	To Find	Comments
Thermo-Mechanical Analysis (TMA)	Glass Transition Temp (T_g) Coefficients of Expansion (x1 & x2)	Key design parameter & degree of cure check
Thermo-Gravimetric Analysis (TGA)	Heat stability & Filler	Useful for high temperature applications. Important to know filler % for effects on expansion rate and water permeability
Differential Scanning Calorimetry (DSC)	Degree of cure check on T_g	Useful when degree of cure or T_g is in question
Gas Chromatography	Elements in Resin	Important to formulator. Not much use to Packaging Engr.
U.V. Spectrophotomtry	Elements in filler	Important to know filler type. Rules out changes without notice.
I.R. Spectrophotometry	Resin type	
West Chemical	Hydrolyzeable halides	Very important for finding % *Cl* available for corrosion. Gives feel for purity of resins in compound
Spiral Flow	Mold-filling capability Degree of flash	Very important to Molding Dept. Supervisor, Affects yields
Gel Time	Mold-filling capability	Same as above

8.5 ENCAPSULATION PROCESSES

8.5.1 Functional Requirements

The current technology of IC encapsulation can be listed under the more global heading of Reactive Polymer Processing. As its name implies, reactive polymer processing is the combined polymerization and processing of reactive polymers or prepolymers in a single operation. The field encompasses numerous processing methods, including transfer molding, radial-spread coating, and reaction-injection molding. The first two have already been used in electronic packaging for some time. The third one, on the other hand, is a relatively new and growing fabrication method. It has, thus far, proven itself mainly in the automobile industry, in the production of relatively large parts. In the following section, these three techniques will each be evaluated in terms of processing practicality and the reliability of the ensuing package.

Although inherent differences exist between the three methods, some threads of commonality can nevertheless be established. Processing criteria, for instance, can be formulated and applied to determine the parameters, if

any, which would facilitate the encapsulation of a given resin. To grasp the full extent of the inherent difficulties associated with molding thermosetting resins, it would be helpful to list the following functional requirements expected from the ideal plastic-packaging method:

1. Low resin viscosity — Thermoplastic melts (used mainly in injection molding) and B-stage thermosets (used in compression and transfer molding) exhibit inherently high viscosities in the upper 100 Pa·s. In an ideal molding process, the reacting mixture should initially display a low viscosity. This would provide not only good wetting of the device topology, but also require less energy for metering through the small runners and gates into the final tool cavity.

2. Good wetting of chip components — Both resin and surface tension inherently control the wetting of any chip component. In a process such as transfer molding, for instance, the extent of coverage of a chip is also governed by the molding pressure. Higher packing would force more material into the mold cavity to take up any slack caused by poor wetting. The rule of thumb, however, generally indicates that wetting would be obtained with intrinsically low-viscosity resin compounds. Estimation of the wetting behavior of a given resin with a surface can be determined by the familiar Young's equation (or modified versions of it) relating the surface tensions of the solid and the liquid, and the interfacial tension between the two would apply for different cases [43].

3. Good adhesion to chip components — Adhesion is controlled by both resin chemistry and chip-surface pretreatment. Different plastics behave differently. Silicones, for instance, are well known for their relatively poor adhesion properties compared to those of epoxies. The formation of good bonds between the reacting resin and the uppermost layer of the chip is a direct corollary of good wetting. Pretreatment, on the other hand, may include, for instance, texturing the surface for added exposed area and extra mechanical interlocking at the chip-resin interface. Naturally, the bond quality is also governed by the wetting behavior of the resin/chip system. Poor wetting leads to the formation of interfacial defects which act as potential sites for future crack propagation. This problem is analogous to that of determining the optimum wettability condition for adhesion. The corresponding criteria have already been established and have become standard "guidelines" in the adhesive industry for gaging bond strength [44, 45, 46].

4. Short cure time — Mixing-activated systems possess different reaction kinetics from heat-activated systems. The type of catalyst, the nature of the crosslinking agent, the level of the initiator, the level of prepolymerization of

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the resin, and the molding temperature all affect the rate of network formation. Ideally, parts should be completed within a reasonable cycle time without ever generating damaging exotherms. Formulating a resin system to provide the proper kinetics necessitates the proper processing conditions. In transfer molding, for instance, the advanced B-stage resins start to cure as soon as they make contact with the hot mold. Frictional heating against the mold walls speeds the polymerization further, and thus requires close control on the transfer pressure, rate, and mold configuration. In a process such as reaction injection molding, on the other hand, the reactive components must be formulated in the stoichiometric ratio appropriate for rapid molding. The characteristic times involved with such a process have been determined [47]. In this case, the kinetics need to be tailored in such a way that mold filling has to be complete before gelation can occur to avoid incomplete filling.

5. Resin with inherently low TCE — The TCE of a polymeric encapsulant protecting a substrate dictates the magnitude of the residual stresses arising from the inherent thermal mismatch between the two materials. The differential expansion effects from a range of materials used in the device can cause small-scale motions of several μm [48]. Such relaxation motions necessary to accommodate interfacial strains would be sufficient to shift metal lines — especially in VLSI submicron structures. The effect of stress imparted to the structure by either the shrinkage of the encapsulation or by the thermal mismatch will be treated separately in a later section.

This property can be controlled to a certain extent by the type and volume/weight loading of fillers and by the chemical nature of the polymeric matrix. A high volume/weight fraction of fillers would also enhance the heat-transfer characteristics of the package, and improve its barrier properties to moisture and solvent absorption. Unfortunately, one of the undesirable side effects of high-filler addition is the drastic rise in viscosity with the accompanying processing complications. The rheological dependence of the resin on the filler concentration and dispersion has been the subject of many studies on various aspects of colloids, dispersions, and suspensions. Over 100 equations have been proposed for estimating the viscosity of a liquid with spherical particles introduced at moderate concentrations [49, 50, 51, 52]. One of the best and most general equations was proposed by Mooney [53]. It describes the maximum possible packing fraction of fillers in a resin of certain intrisic viscosity. Extensive treatment can also be found in both references [54, 55], or specifically for dispersed flow of particulate-filled polymeric systems [56].

6. Good dimensional stability — Each encapsulant displays unique characteristics upon curing. Predicting the final properties is not a simple task as the material may vary from batch to batch, and can be easily changed by the

molding conditions. In-mold shrinkage and thermal stability at extreme operating conditions of temperatures are two issues that have to be dealt with. A direct effect is the building of mechanical stresses into silicon device structures.

Table 8-8 lists representative linear shrinkage values for some commercially available epoxies, polyesters, phenolics, and silicones. One should note the relatively wide range indicated, which depends on the particular resin chemical structure, shape, and filler loading. The sign and magnitude of such residual stresses naturally depend on the design of the particular package. In some cases, the stresses locked within the device by the encapsulation can lead to a deviation of resistor values of up to 15% from the on-slice values. Under the worst possible conditions, when resistors are positioned near the edges of a large chip, errors up to 30% have been recorded [48]. As a result, active circuits are generally embedded in the proximity of the chip center rather than the edges because the corresponding strain field will have a smaller relative effect. Similarly, mobility parameters such as transconductance in CMOS and signal current gain in bipolar devices are altered by the presence of strains. The effect of high internal stresses will thus be reflected on the device in its mechanical integrity or its electrical properties, and most frequently, in both.

7. Low moisture permeability — Water can penetrate to the resin/device interface through even the most-water-resistant polymer, either by filtering through microcracks or by capillary migration along the leads. "Permeability" is used more often than "diffusivity" to describe such a phe-

Table 8-8. Polymerization Shrinkage.

Material	Linear Shrinkage (%)
Epoxy	
Resin - Rigid	0.1–0.4
Resin - Flexible	0.3–1.5
Resin - Mineral filled	0.05–0.2
Laminated glass cloth	0.05-0.2
Glass fiber molding compound	0.1–0.2
Polyester	5
Phenolic	0.5–0.9
Silicone	
RTV - Unfilled	0.1–0.6
RTV - Mineral filled	0.05–0.5

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nomenon because it describes the amount of a material passing through a layer of another material for a given amount of time. The effects of diffusivity and solubility are implicitly included.

Once moisture gets inside the package, corrosion guarantees future reliability problems and ultimately failure of the device. Moisture measurements indicate that the first-order threshold for corrosion failures happens when a film of liquid water is formed on the device surface or in the case of hybrids, on the interconnection pattern [57]. More details can be found later in section 8.6, "Plastic Package Reliability," on page 629.

Knowledge of the permeability (together with properties such as TCEs, thermal, and electrical) is important from a reliability viewpoint. However, much more attention has been devoted in the research literature on the effect of fillers on mechanical behavior [58]. A general solution can, nevertheless, be obtained for all the previous properties since the laws of transport can be represented by the same fundamental equations dubbed with the appropriate nomenclature and modified to account for intrinsic physical differences.

It should be evident that the permeation process depends on a number of factors such as the shape and nature of the fillers, the relaxation of the polymeric matrix to the water influx, the filler/matrix interface, and the solubility of the components present in the package [59, 60, 61, 62]. The transport coefficient within the structure is a discontinuous function of space, that is it varies from one domain to the other. The length scale of the penetrant is assumed here to be much smaller than that of the interested phase or domain. Such phases may not be connected and can actually be separated by sharp boundaries. Therefore, diffusion can proceed across the phases or along the disconnected, simply connected, or multiply connected surfaces. An effective diffusion coefficient can be estimated but its magnitude will vary with the intended use. Sorption and differential permeation can give different results that are highly dependent on the morphology [63]. For instance, sorption of water in glassy unfilled epoxy resins can produce various kinds of anomalies [64, 65, 66, 67, 68, 69, 70]. Aside from the molecular relaxation and extent of curing effects mentioned previously, oxidation was also found to yield non-Fickian behavior [71]. With prolonged exposure to water (liquid), the resin turned darker. This suggested a degradation of the resin during the sorption process and a subsequent alteration in the resin chemical structure. The oxidized resin had a higher sorption affinity towards water. Generally, the basic difference between sorption and permeation is that permeation makes use only of pathways while sorption requires all the dead ends in the pathways as well as those that do not lead to dead ends.

With filled systems, the presence of an impermeable filler leads to a reduced cross-sectional area available for diffusion and a longer path length. Permeation would be slowed down substantially. The first effect is directly proportional to the volume fraction of reinforcement. The second factor,

commonly known as the "tortuosity factor," τ, describes the ratio of the travel path through the maze of fillers to the macroscopic length (thickness) of the encapsulation as

$$\tau \simeq 1 + 0.5v_f \qquad [8.2]$$

where v_f is the filler volume fraction. The electrical analog of this factor was actually derived in 1904 by Maxwell and gave a reasonable limiting case [72]. More accurate and general equations have since been developed to account for the aspect ratio of fillers [73, 74]. The particle shape plays a decidedly important factor in controlling permeation. Cubes and spheres are an order of magnitude less effective than thin plates lying perpendicular to the direction of moisture ingress. This has a rather important processing implication. A structure can be envisioned, for instance, where thin flakes added to the resin are oriented parallel to the device surface by the flow field during molding. Upon curing of the thermoset or solidification of the thermoplastic resin, the flakes trapped in such a configuration would slow down permeation considerably.

The more sophisticated treatments consider cases where fillers or filler interfaces absorb the penetrant [75], or when the fillers are poorly wetted by the resin [59, 62]. A complete molecular description of the permeation through a filled system is lacking in these models. Nevertheless, they can qualitatively predict the effects of various factors deemed to control the process. The two most salient points of the models concern the polymer-filler interactions and the case of permeation through the filler phase.

- *Polymer-filler interaction* — It is widely believed that penetrant molecules travel through the media by jumping from hole to hole. Such holes are created by random chain motions to accommodate the presence of another species. This mobility is also known to affect the glass transition temperature and the relaxation behavior of the polymer [76, 77, 78, 79]. Large particles (e.g., greater than 1 μm) should have little immobilizing influence on material far removed from the fillers. Nevertheless, it was observed with epoxy resins and copolymers of vinyl acetate and vinyl chloride that TiO_2 (around 0.2 μm) increases the T_g but also reduces the sorption of the resins to organic vapors [80, 81, 82]. Furthermore, above T_g, as little as 0.1% TiO_2. drastically affects the activation energy for permeation – up to 40%. Ordering of chain segments accompanying the reduction in internal pressure accounts for the lowering of this activation energy. Of particular interest to electronic packaging is the observation that filling an epoxy resin with glass spheres raises the T_g of the material while reducing its permeation much more than can be predicted with previous theories based on the tortuosity concept for a given volume fraction of fillers [83]. Immobilization

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of the matrix resin segments has been postulated to be due to the differential cooling after curing. Matrices that shrink upon network formation (as with epoxy resins) generally produce a long-range state of compression about the fillers. Hole formation would be inhibited due to the reduction in free volume.

- *Porous fillers* — Permeation through the filler phase is encountered with porous inorganic fillers or in blends of different polymers. When exposed to a given penetrant, it was found that such systems give rise to an apparent paradox. The first few penetrant molecules entering the matrix are trapped and become immobilized, resulting in a large time lag before steady state can be reached [84]. Therefore, this suggests that in order to retard permeation for a certain time span, fillers that absorb the penetrant should be added to the base resin. The time lag before any permeation can occur will be greatly increased. Molecular sieves, for example, can extend the onset of permeation of gases by almost two orders of magnitude. Once it occurs, however, the steady-state rate may be only slightly altered. Nevertheless, the ability to delay permeation, even temporarily, has good implications for the reliability of a package. During operation, moisture is slowly driven off as the device heats up. If the time lag is tailored to fall within the operating cycle of the device, any amount of moisture that has permeated the package since the last on-state will be removed before water can collect sufficiently at the resin/chip interface to cause corrosion.

Morphology is taken into account in a rather limited manner in the previous models — even when an impedance factor is included. The latter is a semi-empirical parameter, which is the product of the tortuosity and a chain immobilization factor. Either ideal random arrays of spherical particles in a continuous matrix or completely ordered structures are explicitly assumed. Polymer blends and composites, however, rarely are completely random or completely ordered [85, 86]. This apparent deficiency is remedied by considering morphology in the analysis of permeation as in the percolation theory discussed next [87, 88, 89, 90, 91].

The structure of a composite can be characterized by geometrical and topological parameters. The former describes the shape of second phase particles while the latter quantifies the connectedness of the phases. The percolation concept in a medium of two phases A and B is illustrated in Figure 8-11 [92].

An arbitrary composite can be represented by a network (regular or random tesselation of space) in which clusters of phase A exist within a continuous matrix of B. The volume fraction of A, Φ_A is the contribution of an "accessible fraction," Φ_A^A, and an isolated fraction, Φ_A^I, or

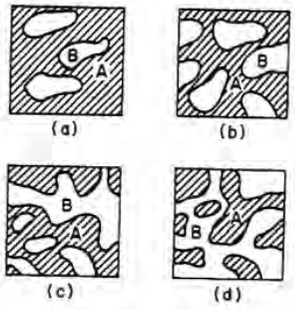


Figure 8-11. Percolation Model. Role of topology in governing transport properties in a medium made up of A and B. Φ_i^A and Φ_i^I are the "accessible fraction" and "isolated fraction" of i, respectively, where $i = A$ or B. (a) Below the percolation threshold for material B: $\Phi_B = \Phi_B^I$, $\Phi_B^A = 0$; (b) Below the percolation threshold for material A: $\Phi_A = \Phi_A^I$, $\Phi_A^A = 0$; (c) Above the percolation threshold for material B; (d) Above the percolation threshold for material A.

$$\Phi_A = \Phi_A^A + \Phi_A^I \quad [8.3]$$

The accessible volume fraction of A is also called the percolation probability of material A. Below a percolation threshold, Φ_A^C, defined as $\Phi_A^A > 0$ when $\Phi_A > \Phi_A^C$ and $\Phi_A^A = 0$ when $\Phi_A < \Phi_A^C$, A exists mainly as isolated clusters with no interconnected pathways. On the other hand, sample spanning clusters exist beyond Φ_A^C. The media is discretized into a networklike structure characterized by a coordination number which is the number of bonds emanating from a site. In the most general case, this number is a random variable characterizing the geometrical distribution of the basic building block. Triangles, squares, hexagons, and cubes would have coordination numbers of 3, 4, 6, and 6, respectively [93]. Φ_A^C decreases with increasing dimensionality and coordination number. Thus, the concept of percolation threshold can account for phase inversion and quantify the complex stereology so characteristic of composite media.

The thread of commonality that links all the models describing the transport behavior in composite media is the linear relationship developed initially from thermal or electrical concepts

$$J = -K\Delta\Phi \quad [8.4]$$

where J, K, and Φ are the flux, an effective material constant, and the potential, respectively. For mass transport, K and Φ are replaced by an effective diffusion constant, D, and the concentration, C.

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8.5.2 Transfer Molding

Transfer molding has been and still is the standard workhorse of the electronic packaging industry. It is an automated version of compression molding in which a preform of the plastic compound is forced from a pot into the hot mold cavity.

8.5.2.1 Process

The operation begins with the loading of chip–wire–lead frame assemblies into the mold, then transferring hot, liquid molding compound from a reservoir to the mold cavities and ends with the ejection of a completed part. The equipment used for this process includes a transfer-molding press, a radio frequency (R.F.) preheater, a platen leader, and a multicavity mold. Generally, transfer-molding presses have three main elements — a hydraulic power unit that feeds high-pressure fluid to clamping and injection pistons, a mold clamping section, and a control unit that ties everything together, as shown in Figure 8-12.

Two types of presses are in use today. One has a large-diameter, single-injection piston that supplies pressure that forces compound into as many as 300 mold cavities. The other is a multiplunger press and has multiple small-diameter plungers with each supplying resin to an array of one to six cavities. Both press types can be automated.

Preheating of the resin pellet is usually required in the normal transfer process. The plunger compresses the charge and maintains the forcing pressure for 10 to 50 seconds, depending on the mold temperature and the resin. Once the material has softened to a workable viscosity range, the actual transfer into the cavities via runners and gates occurs within only a few seconds. Heat input to the pellets prior to transfer comes mainly via conduction through the walls. Viscous heating does not become a factor until flow is forced through the mold runners. More frequently, however, the resin charge is heated by a high-frequency dielectric field prior to transfer. Full transfer pressure is not applied until the preform is partially transferred. A shorter mold residence time is thus obtained, as long as extended runners and restricted gates are avoided in the mold design to avoid premature gelation.

8.5.2.2 Molds

Gouged out of tool steel by electro-discharge machining, mold cavities define the size, shape, and surface finish of a plastic IC package. Mold design is critical to assembly yield and component reliability.

A mold set has two halves, top and bottom, that open to receive lead frames and are closed during the molding cycle. Their mating surface is called a parting line. A set consists of a pair of platens and chases. Platens are massive steel blocks that are bolted to the base (bottom) and crosshead (top) of the molding press. Both platens are aligned by four corner pins. The



Figure 8-12. Transfer-Molding Press. Courtesy of Kras Corp.

bottom platen contains ejector pins and cams used to push molded parts from the cavities. A series of parallel holes traverse each platen horizontally and contain cartridge heaters that maintain the chases at the specified molding temperature. Platens are designed to bear tons of clamping force exerted by the press crosshead.

Chases are parts of a mold set that actually contact and give form to the molding compound. Machined into their hardened steel surfaces are gates and runners that transfer the hot, viscous plastic to the mold cavities. Top and bottom chases are bolted to their respective platens and are aligned with steel locating pins, as shown in Figure 8-13. The surface finish of the cavities, gates, and runners is designed to provide a nonstick surface for easy part ejection and to resist wear from the abrasive molding compounds. Hard

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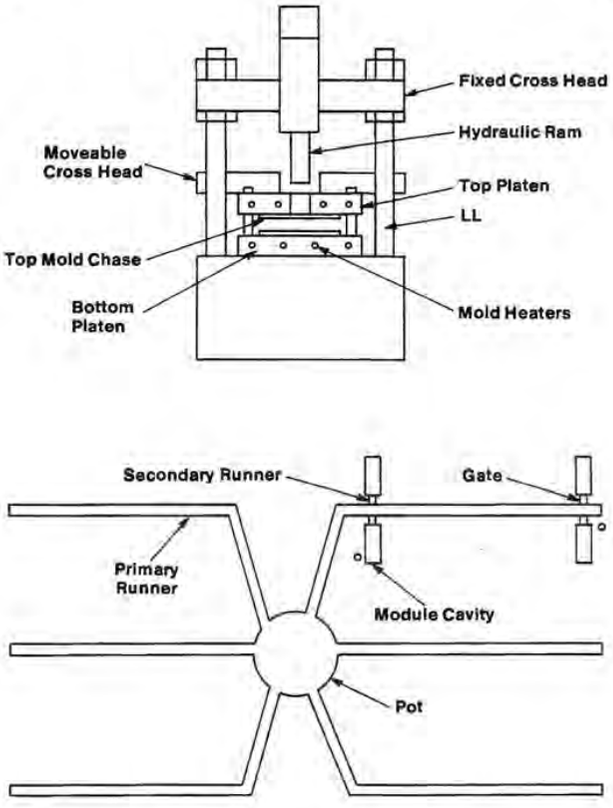


Figure 8-13. Transfer-Molding Press Schematic.

chrome electroplating is a typical finish used on mold chases. A new development, titanium nitride, which is driven into the steel by ion implantation, provides a slippery, wear-resistant surface for the latest mold designs. Mold surfaces are generally relieved so that if flashing does occur, the mold would still close after the transfer cycle. Molding pressures are determined on the basis of the total projected mold area, which should include the pot, runner, gate, and part. Furthermore, an extra 10% clamping pressure is added to reduce flashing and minimize the risk of mold opening.

The layout of the runner system is balanced to provide for an even distribution of molding compound to each cavity. The objective is to fill every cavity with compound of uniform density so that parts located next to the pressure ram will have identical properties to those at the end of the runner. A simplified schematic of a typical runner system is illustrated in Figure 8-14.

Gates are small openings into the cavities where the liquid compound is injected. Opposite the gate is a small air-vent slot. Gates are usually placed in the bottom chase under the plane of chip and wires, to minimize wire sweep. Air-vent slots should be large enough to prevent partial fill and voids in the finished part.

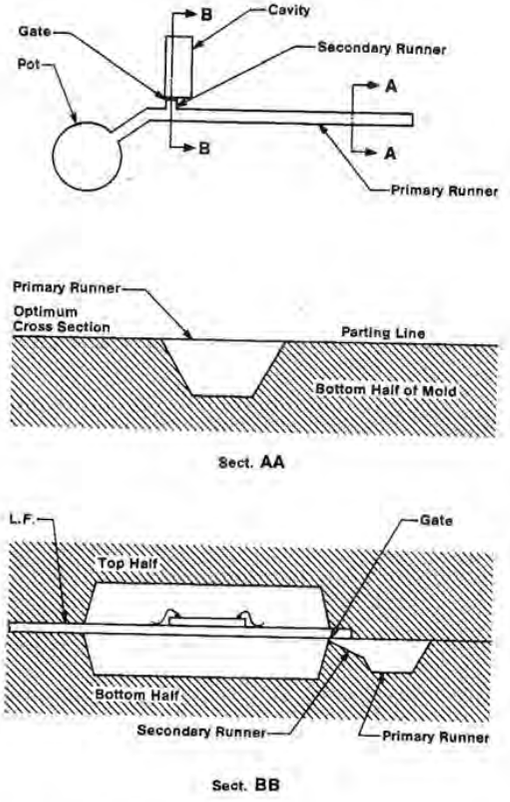


Figure 8-14. Runner Design.

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Molding-equipment improvements rarely qualify as dramatic breakthroughs, although the technology is evolving slowly. Multiplunger presses and automation are two major advances that should be pointed out.

It can be readily seen that in the conventional press, one single plunger serves one single pot. Relatively long runners need to be installed in order to distribute material to all the cavities. Any reacted material trapped in the runners, however, is not reusable. For the high-volume production with a large mold, waste can be fairly substantial. A patent pending design filed by Towa Precision Industry Ltd., Japan, suggested that a single mold, equipped with several pots served by the corresponding number of plungers, can increase material usage significantly by eliminating the long conventional runners. Due to the shorter paths from pots to cavities, complete filling is almost always guaranteed. Similarly, the smaller shot size results in much shorter gel and cure times. Because a plunger serves a much smaller area than in the conventional process, pressure within the cavities is distributed more uniformly with a lesser risk of short shots.

Another factor, which is gaining wider acceptance because of the low offshore labor cost, is automation. Robotics are ideal for repetitive tasks such as mold loading, cleaning, trimming, and forming. Several commercially available systems have already incorporated semi- or fully automatic features with varying degrees of human supervision [94]. A typical system would load lead frame magazines in or out of the mold. After molding, the parts are conveyed to an in-line trim-and-form unit. "Buffer" regions are necessary to take up any slack in the timing sequence. Generally, however, totally automatic systems are disfavored by most manufacturers and users. Once one link in the system malfunctions, the entire system will cease to operate until the problem is fixed.

8.5.2.3 Transfer-Molding Resins

Resins used in transfer-molding operations are generally advanced B-stage compounds. In general purpose applications, wood-flour-filled phenolics, for instance, are fairly popular due to their excellent moldability and low cost. As powders and granules, they are also easily shaped into pellets by automatic preformers. The main drawback with phenolics is the limited colorability. Whenever coloring is a major design factor, melamine, polyester, or urea are usually selected because there is a wider selection of shades and colors. High-temperature applications often call for silicone, phenylsilanes, and polyimides. Most of these materials are resistant up to 315°C and higher. For electronic packaging requirements, however, the preferred resin is epoxy, as discussed previously.

8.5.2.4 Advantages

1. Multiple cavities — As indicated earlier, transfer molds usually have multiple cavities. A standard mold for DIPs has 360 cavities, although large tools with up to 400 cavities have also been reported. When examined in conjunction with the fast curing time of 1 to 2 minutes for typical B-stage resins, it can be seen that a relatively large output rate is possible. Higher yield would be achieved when some of the tasks requiring manual input, such as mold unloading, cleaning, and reloading, can be relieved by automation.

2. Relative material savings — The excess feed material outside the mold cavity is discarded. For each run, waste consists mainly of the principal material in the feed orifice (known as sprue or stalk), and runners formed by cured material between the sprue and the gates to the tool cavities. For small production runs, the reacted resin discarded is tolerable. For large volumes, however, cumulative material costs can be substantial. This is where multiplunger systems can have their largest payback.

3. Short cycle time — When the effect of viscous heating is accounted for in the design of the mold, relatively short cycle times can be achieved (slightly over a minute). Loading preforms into the common pot takes much less time than loading each individual cavity.

4. Low tool maintenance costs — The actual cavities encounter no direct forcing pressure from the plunger. Nevertheless, because all the materials used are heavily loaded with extremely abrasive fillers, wear and erosion of the gates and runners are common.

An estimate of the tool life of a standard runner system can be easily computed. Let us assume that epoxy resin highly filled with silica particles is forced through a cylindrical runner, 12.7 mm in diameter and 127 mm long. Considering the problem as that of a 2-body abrasion, the silica particles (hardness of 800 kg/mm^2) would tend to penetrate the softer tool steel (hardness of 82 kg/mm^2) under normal flow conditions. For a typical injection speed of 0.15 m/sec, the shear stress developed against the walls of the runner would be around 120 Pa. This corresponds to an approximate normal load of 0.12 kg. Because tool steel has an abrasive wear constant of 0.08, the theoretical volume worn out by each pass predicted by the 2-body abrasive wear model is 0.005 mm^3 [95, 96]. For the runner system under consideration, this translates approximately to a decrease in wall thickness of 0.006 μm. Thus, a 1% deviation from the initial diameter would require slightly over 200,000 cycles of operation. With a 3-minute cycle time, this is the equivalent of a tool life of 1.1 year of continuous operation. Naturally, such prediction varies with the operating conditions, the mold cavity, and the molding compound.

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5. Flash-free parts — Inserts are clamped sturdily between the two halves of the mold. As a result, flash-free insert faces can be obtained readily. Tight tolerances at the parting line are usually maintained to allow for the consistent forming of flash-free parts.

6. Choice of chip coverage — Finally, another advantage of transfer molding (and of any molding operation with preshaped cavities) is the choice of resin coverage. The cavity can be designed to provide custom tailored encapsulation and protection, e.g., one side, one side and the four edges, or total chip coverage.

8.5.2.5 Drawbacks

1. High molding pressure — In order to fill up small recesses, pressures as high as 170 MPa are commonly required. Such enormous driving pressures would be potentially harmful to the fragile inner leads and wirebonds. In the worst-case scenario, the highly viscous melt front may cause enough shearing action to lift off the wirebonds completely. More often, however, wire sweeping is reported as one of the major causes of shorts in large I/O devices where long interconnect wires are looped between bond pads. For most of the regimes encountered during the typical molding operation, creeping flow usually applies. The Reynolds number (based on some characteristic length, e.g., runner diameter or cavity thickness) is on the order of unity. Nevertheless, the melt front possesses sufficient momentum to level flexible structures such as wirebonds strewn across its path.

Several interdependent factors govern the extent of wire sweep in a mold cavity of arbitrary geometry. The dimensions of the cavity, for instance, dictate the velocity of the melt-front profile with the corresponding flow stresses and shear rates. The location of the chip to be encapsulated similarly influences the plastic filling pattern. So does the configuration of the particular chip design (e.g., planar versus recessed lead frames). Naturally, the severity of the problem is also controlled by the nature of the wires used during bonding. For example, wire sweep may be controlled to a certain degree by tailoring the wire modulus to offer resiliency and springback after the melt front has swept across but prior to curing. Furthermore, a low drag coefficient would also be obtained if some measure of control on the shape of the wire (e.g., circular versus elliptical cross section) or the profile exposed (e.g., angle of orientation of the wires with respect to the flow) is exerted.

Wire wash and wire sweep may be predicted, and thereby avoided, by modeling the flow behavior of the plastic into the cavity. This can actually be done with various software packages available on the market, including Moldflow® by Moldflow Australia, Total Molding Concept® by Plastics and Computer, Simuflow® and Simucool® by Graftek, PC-Flow® and C-Flow® by Advanced Cae Technology, and Moldfill/Moldcool® by Application Engineering. These programs have been developed solely for the injection molding of thermoplastics rather than for the thermosetting materials commonly used in packaging. Nevertheless, by carefully selecting a thermoplastic analog to the thermoset under investigation, simulation at selected operating conditions can provide some insight into the dynamics of cavity filling. Flow deflectors or leaders, for example, can be positioned strategically along a flow path to control the stress level and the magnitude of the shear rate. However, awareness of the assumptions underlying the software logic is necessary for any meaningful extension of the simulated data to processes other than injection molding.

Another factor resulting from high molding pressure to consider is the shrinkage. Typically, it is 25-50% greater than in compression molding. A difference of 0.10 mm/mm, for instance, has been observed between 20 MPa and 70 MPa.

2. High viscosity — The current commercially available resins formulated for transfer-molding operations possess intrinsically high viscosities (> 10 Pa·s). The trend towards faster in-mold curing requires the use of prereacted compounds needing only heat to complete the polymerization. High packing pressures and trial-and-error flow balancing are currently needed to ensure complete filling of the tool. Imperfect wetting of the leads and chip surfaces, especially at corners and recesses away from the runners, may produce less than optimal adhesion properties.

3. Restriction to the packaging of metal lead frames — The process has thus far been considered mainly for the molding of standard DIP packages. These are mounted on discontinuous lead frames which are sturdy enough to withstand the high molding pressures. However, it is still unclear how the process can be extended to other package designs, such as TAB. The TAB format accounts for its attractiveness as the tape lends itself readily to automation and continuous operation. Unfortunately, in order to adapt transfer molding to TAB, the tape would need to be excised into smaller portions, which would then have to be positioned inside the mold within delicate metal inserts. Because the supporting TAB structure is flimsier than the DIP metal counterparts, extra care needs to be exercised in the handling of the tape. Although the positioning step can be automated, the discontinuites introduced into the tape and the time lag created during mold setup would counter any advantage of selecting TAB.

Two other options considered for TAB possess similar inherent drawbacks. The first one calls for the automatic positioning of the tape within a modified mold. The two mold halves would clamp down on only a predetermined portion of the tape to allow the molding of frames within the enclosed section. Such a task would require accurate tape indexing fixtures and fairly

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high mold tolerances. However, the standard 35 mm polyimide film format yields a tape which does not have the stiffness required for the accuracy of the operation. An operator would have to monitor the press at all times to detect any tape breakage or misalignment. This problem can be eliminated with the second option which suggests the use of a stronger tape able to withstand rough handling.

These problems seem to have been solved recently by National Semiconductor with the TapePac® design. In this case, the TAB tape is a two-ounce single-layer copper tape with etched bumps. After inner lead bonding, the chip is encapsulated by transfer molding. A guard ring is simultaneously molded around the outer lead perimeter of the structure to support the fragile beam leads during subsequent handling. These outer leads are extended to a 1.27 mm grid for burn-in and testing, and are protected by the support ring until the package is placed on the board. Standard soldering processes can be used on the outer leads. The main drawback of the configuration seems to be its relatively low number of I/Os. Current prototypes have a lead count limited to 40, with 0.15 mm inner leads and 0.51 mm outer lead centers. A higher lead count in the future will certainly present more design challenges. Indeed, as the pitch gets finer, each lead becomes increasingly more delicate. Damage can easily occur during handling and molding.

8.5.2.6 Resin Chemorheology

The resin viscosity increases dramatically during processing — typically six or seven orders of magnitude for nonnetwork polymers, and essentially "infinite" whenever gelation occurs. Knowledge of the reaction viscosity profile (commonly referred to as **rheokinetics**) is a prerequisite to the optimum design of processing strategies, especially with respect to mold design. As the resin is forced rapidly through small gates and runners, the pressure drop is rapidly converted to frictional heat. Viscous heating speeds the cure and consequently shortens the cycle time. Currently, such complicated effects can be reasonably predicted by semi-empirical relations. Some have been incorporated into the design of tool cavities of ideal rectangular or circular shapes to benefit the operator [97, 98, 99]. For instance, when high pressures are tolerable, small gates could dramatically reduce the cycle time. Ultimately, however, a thermokinetic model developed from first principles would be needed to describe more accurately the reacting melt.

Nevertheless, with the current knowledge of the rheokinetic behavior of a generic thermoset, a general description of the melt-front profile can be adequately formed. The high resin viscosity will produce flows of rather low Reynolds number through the sprue and runners. The familiar velocity profile characteristic of non-isothermal flows will be observed. Since the mold is heated, material directly in contact with the walls will start curing before that contained within the inner core. As a result, the viscosity of that thin outer

layer will increase, causing a sluggish flow near the walls. The material in the inner core, however, is still unaffected and will move faster than the outer skin. A phenomenon analogous to the "fountain effect" encountered in the injection molding of thermoplastics is observed. The outer skin in the latter case would consist of highly oriented plastic which is frozen when the hot plastic makes contact with the cold walls. With very hot mold walls, the polymerization in the outer skin may be so advanced that the layer acts effectively as an insulator. Heat flow to the inner core is subsequently restricted. The differential polymerization may ultimately produce parts with high internal residual stresses. From an esthetic point of view, overheating of the outer skin may produce knit-lines wherever divided-flow fronts with advanced stages of polymerization meet.

Depending on the resin kinetics and the melt velocity, plug flow may also be encountered. With slow-reacting polymers and fast transfer rates, less viscous material may exist at the walls. This drop in viscosity may become more dramatic at higher mold and melt temperatures.

8.5.2.7 Curing Characteristics

The degree of cure is the most important factor controlling the physical properties of the epoxy network (and of any thermosetting network). Its magnitude is governed by the functionality of the raw ingredients and the chemical conversion of the reaction. Some direct implications of a high extent of curing include, for instance, high glass-transition temperature, good chemical resistance, and excellent barrier against moisture channeling. Sensitivity of epoxies to moisture should not be too surprising considering their highly polar character. Water was shown to disrupt the interchain bonding mechanism, lowering the tensile strength of the material in a manner analogous to a plasticizing effect [100]. The physical hydrolysis can act in conjunction with the polymerization shrinkage stresses to produce a marked decrease in aging resistance.

Numerous techniques have already been used to evaluate the cure behavior and its related phenomena. Deformation under load at high temperatures, for instance, can be used in conjunction with hardness, plasticity, heat distortion temperature, or dilatometric measurements to give a qualitative estimate of the completeness of network formation.

The extent of swelling by solvents of an epoxy network also characterizes the degree of crosslinking. As the latter increases, molecular motion becomes more restricted, lowering subsequently the tendency of the epoxy to absorb solvents. Swelling tests have actually become standard tests for evaluating the quality of epoxy powder coatings [101]. For instance, methyl ethyl ketone (or other suitable solvents) absorption by epoxy coatings is governed by the epoxy equivalent weight, the carboxy terminated butadiene/ acrylonitrile copolymer, the homogeneity of mix, and the state of cure. Although the

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encapsulated components encounter milder environments than those in which the coatings have to perform, similar physical similarities can be found in both cases. Water or solvent (liquid or vapor) during use or any of the various manufacturing steps will ultimately reach the interface and, subsequently, affect the adhesion quality. Corrosion will likely occur over some period of time. The ensuing failure mechanisms are discussed later in more detail.

Refractometry is another simple technique that can be used for clear resins. As the polymer cures, its density and refractive index are altered. However, because epoxies formulated for packaging are heavily filled and deliberately dyed black to block out UV rays, this method would not be of much use. The speed and efficiency of infrared (IR) spectroscopy have also led to its widespread use to pinpoint the extent of reaction. The existence of residual epoxides can be detected via three characteristic absorption bands at 1250 cm^{-1}, 916 cm^{-1}, and 830 cm^{-1}. Nevertheless, IR necessitates the removal of fillers for proper operation. Testing based on the electrical volume resistivity [102, 103, 104], dielectric properties [105, 106, 107], or nuclear magnetic resonance [108] have been tried with varied degrees of success. By far, the most widely used techniques involve differential scanning calorimetry (DSC), thermogravimetric analysis (TGA), thermomechanical analysis (TMA), and dynamic mechanical analysis (DMA) [109, 110, 111, 112, 113, 114, 115, 116, 117]. For a given temperature, generally, the glass-transition temperature shifts upward as long as crosslinking is taking place. As a matter of fact, the T_g of the composite is often de facto regarded as the quantitative indicator of complete reaction. Similarly, the dynamic mechanical moduli describes the distribution of network chains-per-unit volume of the system. Furthermore, direct observation by electron microscopy can be correlated to the molecular weight of epoxy resins and the homogeneity of the network [118].

More recently, near-infrared reflectance analysis (NIRA) was evaluated as a potential technique for determining the state of cure of polymers [119]. The near infrared interval covers the spectral region from 750 nm to 2,500 nm. Usually, spectra obtained in these intervals are mostly due to first or second overtones and combination bands of the frequencies observed in the mid-IR range for hydrogenic bonds (e.g., $C-H, O-H, N-H$). Typical spectra are displayed as $\log(1/R)$, where R is the reflectance of the material, between 1,100 nm to 2,500 nm. Linear regression is subsequently used to provide a correlation between the chemical analysis of end groups and the reflectance data at each wavelength. By curing samples for varying amounts of time to yield different degrees of cure and comparing the corresponding spectra, a calibration curve between curing time and extent of cure can be established. Thus far, however, more success has been reported with polyester resins than with epoxies.

Regardless of the technique used, the resin components need to be mixed with extreme care. Inhomogeneities resulting from poor compounding, either by hand or even with mechanical stirrers, can affect the morphology and the thermal stability of the cured product. Electro-mechanical mixing was reported to improve the homogeneity of the parts [120].

8.5.2.8 Wire Sweep and Molding-Related Issues

Wire sweep is the largest and predominant cause of defects in the molding of packages. During the filling stage, the flow front of the resin entering the mold cavity possesses sufficient momentum to displace the wires bonded between the die and the lead frame. The ensuing plastic deformation causes adjacent wirebonds to contact and short the device. The following discussion is based on a recent treatment of molding of electronic packages [121].

Causes of Wire Sweep: The forces encountered by the wirebonds as the melt front enters a mold cavity are shown in Figure 8-15a for a typical transfer-molding operation. Each wire is subjected to both tensile and bending forces.

Tensile forces are exerted on the wirebonds due to the flexing of the lead frame from the flow imbalance between the two cavity halves. Current mold designs call for the resin to exit the gate, and flow under the tie bar loop before emerging into a cavity. The lead frame subsequently divides the melt profile into two fronts. A good design would balance the two flows, and ensure that both reach simultaneously the far end of each cavity. This would avoid any "racing" effect between the two fronts, and reduce the potential for air entrapment. This was an issue regularly plaguing past mold designs. More clearance used to be allowed for the upper half of the cavity containing the silicon die. As a result, the front in the upper half always preceded that in the lower half. Although the lead frame can be considered as a highly porous membrane separating the fronts, the highly viscous nature of the resin dictated a minimal amount of recirculation. The ensuing lead-lag acted as a rolling, bending moment on the entire lead frame, and put all the wire bonds present under tension at various points in time. Fortunately, lead-lag no longer is an issue with the introduction of the recessed lead frame. In the new configuration, as shown in Figure 8-15b, the chip sits on a paddle depressed below the level of the lead frame. Thus, the lead frame can be positioned to divide each cavity into two approximately equivalent halves to reduce racing effects and any ensuing flow-induced tensile forces on the wirebonds.

Drag forces on the wires, however, cannot be eliminated. Pressure drag is negligible in most cases because the melt stays within the creeping flow regime. The major contribution to the drag comes from shear stresses acting on the exposed cross-sectional profile of the wirebonds. Current aluminum and gold wires are cylindrical, although rectangular-shaped wires have been used in high-power devices. The magnitude of the frictional drag observed is

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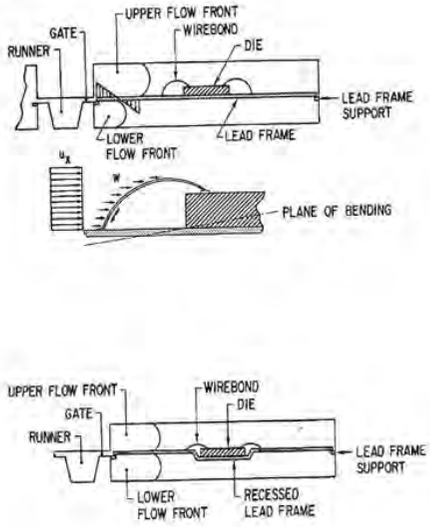


Figure 8-15. Forces Encountered by the Wirebonds. a) Traditional lead frame: the lead-lag in the two flow fronts induces a rolling, bending moment on the lead frame, and generates in the process tensile forces in the wires. Drag forces are produced by the advancing front; b) Recessed lead frame: the elimination of the lead-lag reduces the potential for bending stresses.

highly dependent on the wire profile exposed but also on the Reynolds number. As long as the drag does not exceed the elastic strength of the individual wire, wire sweep is prevented. Although there will be some deformation, springback may actually happen to a certain extent before the material gels completely. Most likely, however, high resin viscosity and flow rates act in unison to deflect the wire past the yield limit.

Stages of Occurrence of Wire Sweep: Wire sweep can occur during any of two stages in the molding process, namely, filling and packing. In the filling step, close control of the ram transfer speed is crucial. Too low a speed translates into pushing a resin in an advanced state of cure into the cavity, causing wire sweep. On the other hand, when filling speeds are programmed too fast, the high flow momentum also tends to level the wirebonds. In this case, void formation is also more likely to be incorporated into the molded package. This manufacturing defect can actually be easily detected. Wire sweep in end cavities can usually be traced back to slow transfer speeds. Excessive speeds, however, result in wire sweeping in initial cavities closest to

the pot. The proper filling speed resides somewhere between these two extremes. In some cases, the hydraulic back pressure of the ram can also be used to govern the rate of filling of the cavities [122]. Regardless of the method used, the end result is still the control of the resin velocity either through ram speed or ram pressure.

Packing starts when the cavities become partially filled (90-95%). As back pressure gradually builds up, compaction of the resin follows resulting in increased part density. Poor yield at this stage often results from either low packing pressure, or long hold time, resulting in freezing of the material at the gates before complete packing can be achieved. However, rapid compaction induces sudden rapid movement of the resin front which can also produce wire sweep. The continuous application of high-packing pressures produces excessive flash. Nevertheless, if the pressure is suddenly relieved, any residual air entrapped within the melt will depressurize, causing further fluid motion across the wire bonds. Resin bleed is reduced at the expense of more harmful wire [123].

Wire sweep can be seen to originate from various potential sources. Close control on the resin velocity through ram transfer pressure or velocity is certainly needed. This must be done concurrently with a packing hold and release profile which minimizes both flash and wire sweep.

Mold-wire sweep is common to all IC packaging, but becomes more prevalent in small outline packages because of the fine pitch lines and part dimensions. The problem has received wide attention [124, 125] but, thus far, has not been treated analytically (Fig. 8-16). The extent of wire sweep has been analyzed recently by considering the transfer-molding operation in the form of an electrical analog [125]. The resulting model treated all the hydraulic-flow passages as electrical resistances. The hydraulic system with the flow-control valve was assumed to be a constant current generator with a voltage clamp. With voltage and current behaving as the equivalent of pressure and flow, respectively, the voltage (pressure) drop across each resistance was computed for the whole transfer cycle. The model, however, did not take into account two important features, namely, the compressibility of air entrapped in the initial filling period and the ever-changing viscosity of the resin. He defined wire sweep as any plastic deformation of a wirebond to within 0.25 mm of an adjacent lead finger, as projected onto the plane of the lead frame. By counting the number of units exceeding this limit, the severity of wire sweep in a given test mold can be quantified. The criterion is somewhat arbitrary and will probably have to be redefined with every new package footprint. Nevertheless, it provided a practical "go/no go" attribute to assess a given mold design.

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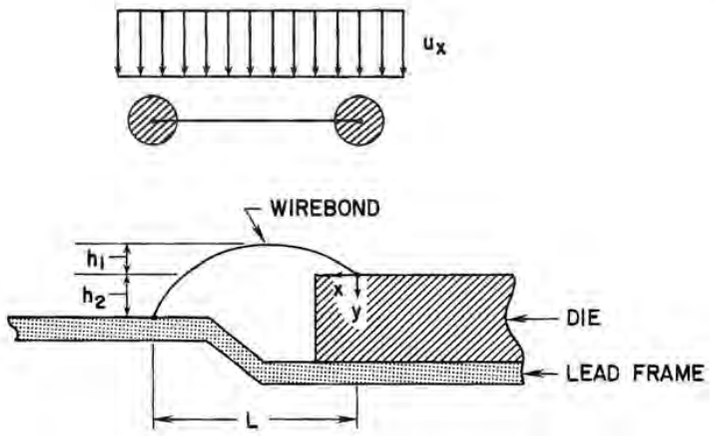


Figure 8-16. Idealized Wirebond Configuration. A transverse load is applied to the wirebond. The top figure illustrates the vertical projection of the wire and the melt front approaching at a mean velocity u_x.

Flow-Induced Stresses on a Parabolic-Shaped Wirebond: An idealized wirebond configuration is depicted in Figure 8-16. One end of the wire is anchored to the aluminum pad while the other is bonded to the lead frame. The wire is assumed to have a uniform cross section throughout its length. In this case, the profile traced by the wire can be expressed by the following relationship

$$y = ax^2 + bx = \frac{4}{L^2}\left(h_1 + \frac{h_2}{2}\right)x^2 - \frac{1}{L}(4h_1 + h_2)x \quad [8.5]$$

When a distributed load, w, is applied to the wire across $x = \ell_1$ and $x = \ell_2$, the resulting reactions H_0 and V_0 and moment M_0 are shown in Figure 8-17. The bending moment at C, neglecting the weight of the wire, is

$$M = M_0 - V_0 x - H_0 y + w(\ell_2 - \ell_1)(x - \ell_0) \quad [8.6]$$

Solving for the corresponding angular displacement and component displacements gives the following expressions, which apply for the general case when the load w covers the entire wire. This occurs during molding be-

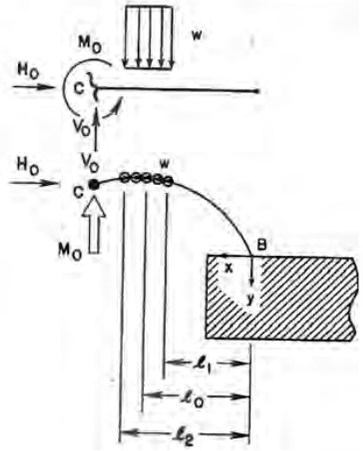


Figure 8-17. Cross Section of a Wirebond Under a Transverse Load. For a transverse load w acting between ℓ_1 and ℓ_2, the resulting reactions H_0 and V_0 and moment M_0 are shown.

cause the flow front fills the cavity, and subjects the whole wire to flow-induced stresses. With $\ell_1 = 0$, $\ell_2 = L$, $\ell_0 = \ell = L/2$, we have

$$V_0 = w\left(\frac{L}{3aL + 4b}\right)(aL + b) \quad [8.7]$$

$$H_0 = w\left(\frac{L}{aL + b}\right) \quad [8.8]$$

$$M_0 = w\left(\frac{L}{aL + b}\right)\left(\frac{2aL^2 + 3bL}{6}\right) \quad [8.9]$$

The drag load w generated by a melt front advancing at a given Reynolds number Re can be described by

$$w = \left| \frac{1}{4} C_D(\omega)\left(\frac{d_w}{d_c^2}\right)\left(\frac{\eta^2}{\rho}\right) Re^2 \sin\omega \right| \quad [8.10]$$

for $0° \leq \omega \leq 180°$

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where
η = resin viscosity
ρ = resin density
ω = orientation of the wire with respect to the melt front
C_D = drag coefficient of the wire
d_w = characteristic dimension of the wire (thickness for a ribbon interconnection or diameter for a circular-shaped wire)
d_c = thickness of the cavity.

The Reynolds number is $Re = \frac{\rho u_x \ell_{char}}{\eta}$, where ℓ_{char} is a characteristic dimension of the flow and can be taken to be half of the cavity size, or $\ell_{char} = d_c/2$. Because the drag coefficient depends on the Reynolds number, the drag force is seen to increase with small cavity sizes, a large exposed wire profile, and high-flow Reynolds numbers. C_D is described by the following semi-empirical equation, which holds mainly for creeping flows (e.g., $Re < 1.0$) [126].

$$C_D(\omega) = \frac{8\pi}{Re(2.002 - \ln Re)} \qquad [8.11]$$

Strongly influenced by the wire-orientation angle ω, Equation 8.11 describes the drag on a cylinder in the low Reynolds number regime when flow separation is highly unlikely. The wake is laminar, and any drag induced is predominantly friction drag. The wire surface is inherently assumed to be smooth. Rough irregularities, although extremely rare with wirebonds, will have to be accounted for by the inclusion of a friction factor. Similarly, C_D will also have to be adjusted accordingly for molding cases where the flow Reynolds numbers exceed unity. Experimental data of drag coefficients as a function of Reynolds numbers for $Re > 1.0$ are available [126].

Thus, once values of the melt-front velocity are known, either from experimental measurement or from flow simulation, the loading on the wirebond can be estimated at various times during the mold-filling process.

Once Equation 8.10 is substituted back into Equation 8.8, the horizontal displacement of the wirebond, H_0, can be readily calculated. Furthermore, the exact location of the maximum deflection can also be predicted.

For gold wires typically doped with traces of beryllium, it was found that once the elastic limit is reached, a rather constant moment is achieved and maintained [127]. This physical property can be compared to that of a plastic hinge. The latter allows large rotations to occur at constant moments. In contrast, a frictionless hinge is capable only of large rotations at no moment. In this case, the constant bending moment observed can be approximated by the ultimate or plastic moment for a given cross section.

By introducing plastic hinges at points of maximum moments in the wirebond, a kinematically admissible collapse mechanism is created. Subsequently, in permitting unbounded movement in the wire, the ultimate load-bearing capacity of the configuration can be determined. This can be found by differentiating Equation 8.5, which gives the critical distance x_p as

$$x_p = \left(\frac{1}{3aL + 4b}\right)\left(aL^2 + \frac{b^2}{2a}\right) \qquad [8.12]$$

and the corresponding plastic load w_p

$$w_p = \frac{1}{2\ell(\ell_0 - x_p)} M_p(M_0, V_0, H_0, a, b, x_p) \qquad [8.13]$$

Effect of Flow Parameters: Figure 8-18 depicts the behavior of a 0.03 mm circular gold wire exposed to an advancing melt front under different regimes of Reynolds numbers. The flow front encounters the wirebond at an angle $\omega = 90°$. The deflection H_0 discussed is the lateral displacement of the vertical projection of the wire on to the plane of the lead frame. The wire is pushed gently sideways by the flow, moving by less than 0.03 mm which is slightly over one wire diameter. However, H_0 increases up to 0.17

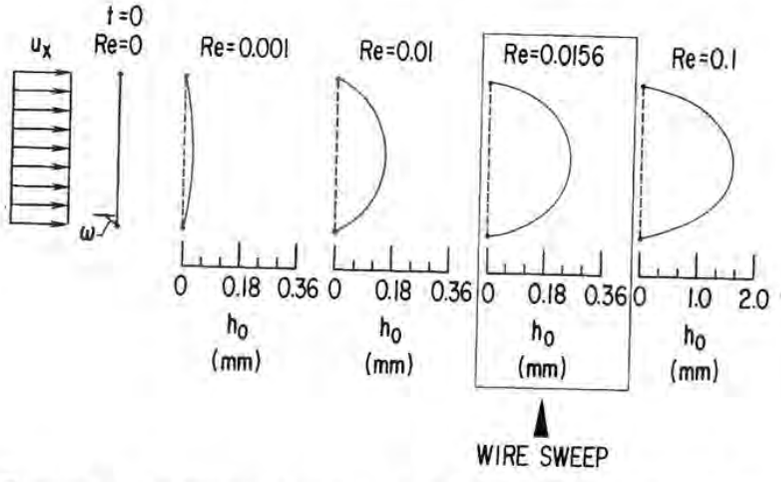


Figure 8-18. Horizontal Displacement of a Wirebond at Different Flow Regimes. Deflection (H_0) illustrated for increasing higher flow Reynolds numbers to show the ultimate collapse of the wire. For a package with a pad spacing of 0.254 mm, wire sweep occurs at $Re = 0.0156$. This critical value is governed by the wire properties, the flow characteristics, and the package configuration.

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mm as the velocity of the front is raised by an order of magnitude ($Re = 0.01$). Wire sweep occurs when Re reaches 0.0156 where a wire deflection of 0.254 mm is observed. This wire-sweep criterion would certainly depend on the package configuration, the wire pitch, and I/O density. As the Reynolds number is raised further, wire sweep becomes more pronounced. A deflection of up to 1.6 mm is recorded at $Re = 0.1$. The flow has leveled the wirebond almost down to the level of the lead frame.

Effect of Wire Length: As the vertical projected length of the wire gets longer, the structure becomes inherently unstable. This is illustrated in Figure 8-19.

Both the height of the wire ($h_1 + h_2$) and the wire diameter d_w are fixed in the configuration analyzed. At a Reynolds number of 0.0001, it takes up to 50 seconds to fill a cavity with a typical volume of 0.9 cm^3. Wire sweep, as defined by the 0.254-mm lead pitch, does not happen at such long and unlikely filling times. However, as the flow momentum is raised ($Re = 0.001$), the critical length before wire collapse approaches 3.6 mm. This value is lowered by another 30%, down to 2.5 mm, when the Reynolds number is raised by another order of magnitude ($Re = 0.01$). Sweeping at $Re = 0.0156$ lowers the critical length further to 2.3 mm. At $Re = 0.1$, however, the whole structure becomes inherently unstable, regardless of the wire lengths.

The coordinate of the wire collapse can be predicted from Equation 8.11 with the implicit assumption that the melt front encounters the wire at $\omega = 90°$. The analysis considered only the geometry of the configuration for general wire physical properties and, thus, would hold for wires of differing cross-sectional shapes and areas. Naturally, although these wires buckle at different flow regimes, the location of maximum collapse remains flow independent.

For instance, Figure 8-20 shows the behavior of x_p, when the wire length is kept at 2.2 mm, the chip thickness (t_c) at 0.635 mm, and five h_2/t_c ratios are considered, namely, 0.5, 0.9, 1.0, 1.1, and 1.5. The critical distance (x_p) resides at approximately the same location ($\simeq$ 0.8 mm) from the chip bond for small values of h_1. It should be noted here that $h_2/t_c < 1.0$ implies a recessed lead frame while $h_2/t_c > 1.0$ refers to a configuration where the chip resides at a higher level than that of the lead frame. When the wire height is increased slightly, x_p edges closer to the chip-bond connection. In other words, at small wire heights, wire collapse under the full leveling momentum of the flow is likely to occur near the chip-bond pad. Thus, the lifting and shearing action of bond pads discussed earlier can theoretically occur.

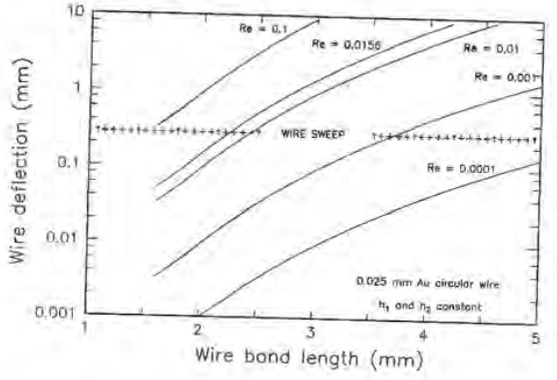


Figure 8-19. Flow-Induced Displacement for Wirebonds of Different Lengths. The wire-diameter (0.03 mm) and the wire height (h_1 and h_2) are held constant. Various flow regimes are considered. Wire sweep is shown for the range delineated by the vertical arrows.

Effect of Wire Height: Figure 8-21 indicates that molding at a low Reynolds number ($Re = 0.001$) can be accomplished without any worry about wire sweep. This applies to a 0.025 mm gold wire at constant L and h_2 with varying h_1 and chip thickness, t_c. The situation is completely reversed, however, at $Re = 0.01$. The five configurations mentioned earlier, namely, $h_2/t_c = 0.5$, 0.9, 1.0, 1.1, and 1.5 are considered again.

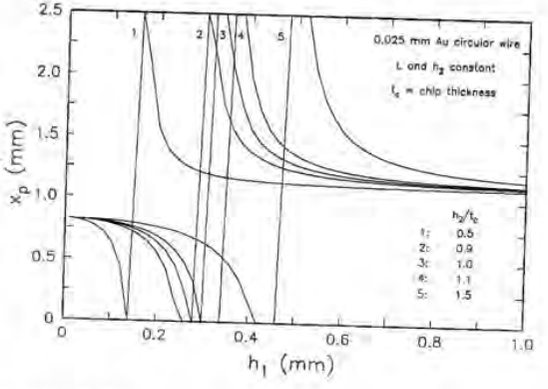


Figure 8-20. Location of Critical Point of Wire Collapse.

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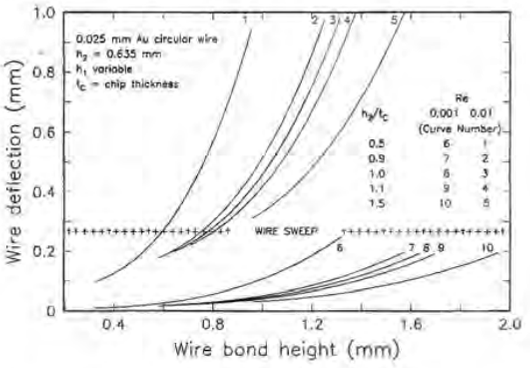


Figure 8-21. Flow-Induced Displacement for Wirebonds of Different Heights. Two flow Reynolds numbers are shown. For a chip 0.635 mm thick ($t_c = 0.635$ mm), h_2 is varied for 5 cases, namely, h_2/t_c =0.5, 0.9, 1.0, 1.1, and 1.5. The height of the wirebond configuration refers to the sum of h_1 and h_2.

For the same Reynolds number, the recessed lead frame structure gives a critical value lower than for the other types of configurations. Fixing L and varying h_2 exposes the wire more directly to the melt front, resulting in higher risk of wire sweep. This is the case with the recessed configuration. The raised configuration leaves the wire in a similar predicament but stretches the wire more tightly, allowing it to withstand more loading before collapsing. The analysis indicates, for example, that when the chip is 50% recessed with respect to the lead frame level, wire sweeping starts at heights larger than 0.6 mm. As h_2/t_c is raised, the allowable wire height is correspondingly increased. At h_2/t_c, this height can reach up to 0.9 mm before the whole structure would become unstable.

Effect of Wire Flexural Rigidity: Aside from the kinematic constraints discussed previously, the wirebond behavior is governed also by physical parameters such as modulus, wire diameter, and cross-sectional profile (e.g., circular versus parallelepiped). Figure 8-22 depicts the effects of these conditions for both gold and aluminum wires. The melt front is assumed to advance at a Reynolds number of 0.01. All the other conformational parameters such as h_1, h_2, and L are kept constant.

With a modulus approximately 10% lower than that of gold, aluminum wires deflect more by the same amount, regardless of the cross-sectional profiles. For a given material, however, altering the wire profile can have a dramatic effect on the onset of wire instability. In general, the circular wire

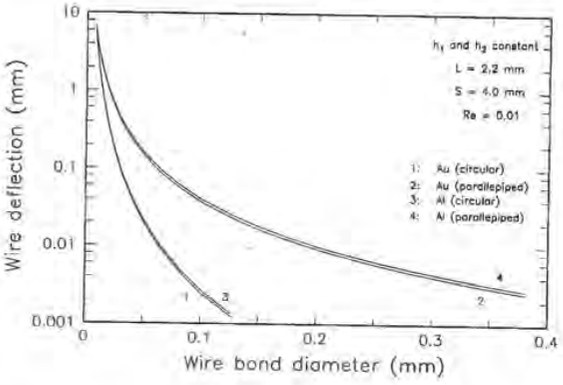


Figure 8-22. Flow-Induced Displacement for Wirebonds of Different Profiles. The flexural rigidity of the wire, EI, strongly influences its deflection. E is the wire modulus and I is the moment of inertia of the wire with respect to its centroid. Values for circular and parallelepiped wires made of gold and aluminum are used.

seems to withstand the flow-induced loads much better than its parallelepiped counterpart. At $Re = 0.01$, a circular wire with a characteristic diameter $d_w = 0.1$ mm deflects by $H_0 = 0.0024$ mm if it is made out of gold, and 0.0026 mm for aluminum. Under similar flow conditions, however, the parallelepiped-shaped wire buckles more: 0.036 mm for gold and up to 0.040 mm for aluminum, respectively. In order to get the same amount of deflection, a parallelepiped ribbon would have to be at least an order of magnitude thicker ($\simeq$ 0.3 mm) than the circular wire.

When the wire characteristic diameter is small, however, the differences in the exposed profiles become less severe. Circular and parallelepiped-shaped wires behave similarly under these conditions. This is mainly due to the fact that the drag coefficient becomes approximately the same for both profiles at low Reynolds numbers. The observed behavior ensues mainly from the rigidity of the wires as dictated by the moments of inertia of the wire structures.

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Effect of Wire Orientation: The orientation of the structure with respect to the advancing front also dictates the extent of deflection observed. This is shown in Figure 8-23 for a 0.025-mm gold-wire structure with $h_1 = 0.073$mm, $h_2 = 0.422$ mm, and $L = 2.2$ mm. Configurations with $\omega = 0°$and$180°$ exhibit the lowest profiles to the melt front. As a result, these configurations naturally exhibit the lowest horizontal deflection ($H_0 \simeq 0$) under an advancing melt front. There is, however, some wire motion within the vertical plane of projection of the wire onto the lead frame. Such motion is less critical than any lateral deflection as it does not result in electrical shorting.

More area of the wire becomes exposed as ω increases gradually to reach a maximum at 90°. As expected, at this orientation, the wirebond becomes fully exposed to the resin front. Once the impingement angle exceeds this critical value, however, the exposed profile decreases monotonically resulting in lesser damage to the wire configuration.

Thus, positioning the wirebonds within the mold cavity can have a significant influence on their structural and electrical integrity. A highly viscous melt rushing out of a gate onto a row of wirebonds all angled at 90° will cause much more damage than in configurations where $\omega < 90°$ or $90° < \omega < 180°$. Wire sweep will be minimized in this case by redirecting the flow or repositioning the silicon die within the cavity to avoid full frontal encounter with the melt.

8.5.2.9 Molding Stresses: Two-Sided Coverage

Curing and thermal stresses occur regularly in plastic-encapsulated packages. Typically, curing stresses result from a combination of resin shrinkage during polymerization, and differential thermal contraction after some elevated-temperature post curing. Shrinkage subsequently yields sink marks and other surface defects. In the later stages of the reaction, this shrinkage produces microstresses that cannot be relieved. On the other hand, thermal stresses arise from the TCE mismatch between the silicon substrate and the filled polymeric matrix. Such stresses are additional to any stresses generated from outside loading. In some cases, however, such stresses are high enough to induce microcracks, even in the absence of external loads.

The existence of these microstresses within the resin and across the filler-resin interface has been documented by photoelastic studies [128, 129], embedded strain gages [130, 131], holographic interferometry [132, 133], and more recently, x-ray diffraction [134, 135, 136, 137, 138, 139]. The advantages and drawbacks of these techniques have been outlined recently [134]. The two-sided residual-stress model presented here follows from recent results on a systematic investigation of the behavior of molding compounds for packaging low-end electronic devices [134]. Some of the issues affecting the stress profile are considered. These may include, for instance, the effect of

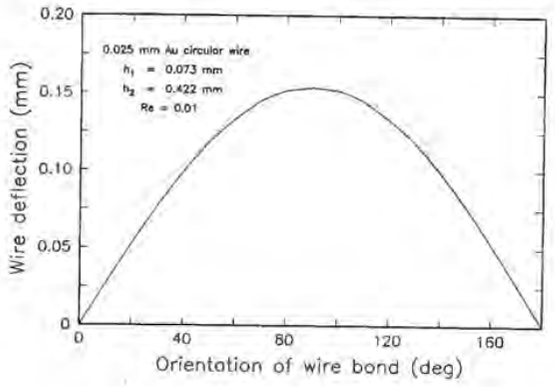


Figure 8-23. Flow-Induced Displacement for a Wire at Various Flow Orientations. All the wire configuration parameters (wire diameter, height, and length) are kept constant. The flow Reynolds number is 0.01. The orientation angle refers to the angle formed between the vertical projection of the wire on to the lead frame and the flow direction.

resin chemistry, curing schedules, nature of the filler, filler loading, and filler aspect ratio, the effect of thermal cycling and external loading, and the influence of moisture absorption on the filled matrix.

Several models describing the state of stress and strain within films on substrates already exist. All the problems considered thus far, however, deal with the preparation of thin films by sputtering, evaporation, or chemical deposition [140, 141]. The stresses are measured by either the bending-beam or bending-plate methods, which record the deflection of thin strips or plates coated with the film, and deformed by the film stresses [142]. The magnitude of these stresses can be computed from the deformation. X-ray diffraction and optical-interference techniques have also been reported [143]. However, these models possess several inherent limiting assumptions, such as equal Young's moduli and Poisson's ratios [144], and isotropic [145] and homogeneous stresses [146]. A variation of these problems was recently considered for determining the adhesion of thin, brittle films on low modulus substrates [147, 148]. In this case, Griffith's energy criterion was used to derive an expression for interfacial stresses in terms of material constants, film thickness, and external loading. This model was subsequently extended to layered composites of polymeric films [149]. However, the system analyzed related to the minimization of edge curl in a solvent-coated, layered composite. As the solvent evaporated in the different films, the T_gs of these films changed

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continuously, altering in the process the rate of solvent diffusion. Knowledge of the stress relaxation behavior is critical to the modeling.

In the encapsulation of silicon dies with thermosetting resins, however, the situation differs since the protective coatings are much thicker than the thin films discussed earlier. Therefore, a plane-strain condition is more likely to occur than the plane-stress state encountered with thin films. Furthermore, once the resin has fully cured, stress relaxation does not usually become an issue, since typical thermal-cycling stresses the parts below the T_g of the encapsulant (between 150°C to 180°C for most anhydride-cured epoxies).

Figure 8-24 depicts an idealized plane substrate of thickness t_0 and length L_0. Both sides of the substrate are covered with the encapsulation resin over an area of characteristic length L_1 to a thickness t_1. The films are assumed to be in plane strain, that is, the stress σ_{zz} parallel to the thickness direction in both films is small compared to the normal stress σ_{xx}. In the initial molding stage, the resin is still liquid and flowable, and stresses are not developed. Once polymerization starts, however, the modulus increase of the coatings is accompanied by a corresponding volumetric shrinkage. As a result, in the final cured state, both films and substrate exhibit the same length L_f, albeit different thickness t_{1f} and t_{0f}, respectively. Forces from the resin shrinkage and the thermal mismatch are represented in Figure 8-24. These forces can be resolved into a tensile, F_1, or compressive, F_0, pair, and an ensuing set of bending moments, M_1 and M_2. Equilibrium dictates that no net force or moment exists, so that

$$[\Sigma F_i = 0] \quad 2F_1 - F_0 = 0 \tag{8.14}$$

$$[\Sigma M_i = 0] \quad F_1(t_0 + \frac{t_1}{2}) - F_1(t_0 + \frac{t_1}{2}) = M_1 + M_2 \tag{8.15}$$

In Equation 8.15, the moment balance is taken at point A, which is located on the neutral plane $\phi\phi'$ of the composite structure. Both Equations 8.14 and 8.15 yields $M_1 + M_2 = 0$, which confirms the common knowledge that a substrate coated on both sides with the same thickness of a material does not undergo any bending. The maximum stress in the encapsulation layer is

$$(\sigma_1)_{xx} = \frac{F_1}{t_{1f} L_f} \tag{8.16}$$

in which $t_{1f} = t_1 + (\Delta L_1)_{\text{shrinkage}} t_1$, where $(\Delta L_1)_{\text{shrinkage}}$ is the linear shrinkage of the resin. For highly filled systems, however, $(\Delta L_1)_{\text{shrinkage}}$ is typically around 0.3-0.5%, so that $(\Delta L_1)_{\text{shrinkage}} t_1$ can be reasonably neglected when compared to shrinkage in the axial direction. For small dimensional changes, $\Delta L = L_f - L_1$, the axial strain in the film, $(\varepsilon_1)_{xx}$, can be expressed by

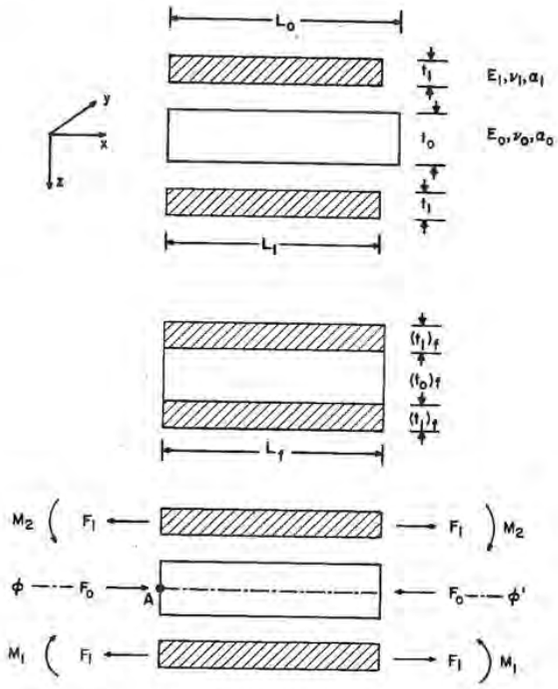


Figure 8-24. Idealized Silicon Substrate with Two-Sided Encapsulation. (a) Before curing, (b) Coated substrate after curing, (c) Free body diagram showing forces and bending moments acting on each layer of the coated substrate. Subscripts 0 and 1 refer to the silicon and the coating, respectively.

$$\begin{aligned}(\varepsilon_1)_{xx} &= \ln\left(\frac{L_f}{L_1}\right) - \nu_1 \ln\left(\frac{L_f}{L_1}\right) \\ &= (1 - \nu_1)\left(\frac{L_f - L_1}{L_1}\right)\end{aligned} \tag{8.17}$$

so that $(\sigma_1)_{xx}$ can be rewritten in terms of material constants as

$$(\sigma_1)_{xx} = \frac{E_1}{1 - \nu_1}(\varepsilon_1)_{xx} = E_1\left(\frac{\Delta L}{L_1}\right) \tag{8.18}$$

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Combining Equations 8.16 and 8.18 gives

$$F_1 = E_1 t_1 L_f \left(\frac{\Delta L}{L_1} \right) \qquad [8.19]$$

which shows that the tensile force exerted on the film depends on the film thickness while the film stress is independent of thickness. A similar analysis carried out for the substrate yields

$$(\sigma_0)_{xx} = \frac{F_0}{t_0 L_f} = E_0 \left(\frac{\Delta L}{L_0} \right) \qquad [8.20]$$

and

$$F_0 = E_0 t_0 L_f \left(\frac{\Delta L}{L_0} \right) \qquad [8.21]$$

Equations 8.14, 8.19, and 8.21 finally give

$$(\sigma_0)_{xx} = \left(\frac{2t_1}{t_0} \right) (\sigma_1)_{xx} = \left(\frac{2t_1}{t_0} \right) \left(\frac{\Delta L}{L_1} \right) E_1 \qquad [8.22]$$

Equations 8.18 and 8.22 reveal some interesting findings about two-sided substrate coverage. First, and foremost, the radius of curvature of the composite structure remains at zero for all coating thickness, as long as both sides are covered with the same thickness. Any bending induces extraneous stresses into the package. However, this is unlikely to occur in practice because the normal package benefits from the stiffening effect of the metallic lead frame. The analysis presented earlier did not take this factor into consideration, and thus, would give the highest stress profile encountered by the silicon die in the worst possible scenario. Second, the stress generated within each film is independent of the film thickness. Stress relief may occur to a certain extent, however, in the form of crazing or cracking. Such a condition is likely to occur in thin films of dimensions similar to those of filler particles. Third, as the film thickness is raised, the stress in the substrate increases linearly. Very thick films can generate stresses sufficiently high to induce microcracks in the substrate [134]. At intermediate thickness levels, no substrate cracking is observed, although the system may possess residual stresses which may subsequently cause cracking under harsh thermal cycling [150].

8.5.3 Radial-Spread Coating

Radial-spread coating has been in vogue only recently, with the advent of surface-mount packages [151]. Sometimes referred to by the name of "glob top," the coating produced is usually much thicker than that obtained with a conformal coating technique. The latter generally yields a very thin overcoat

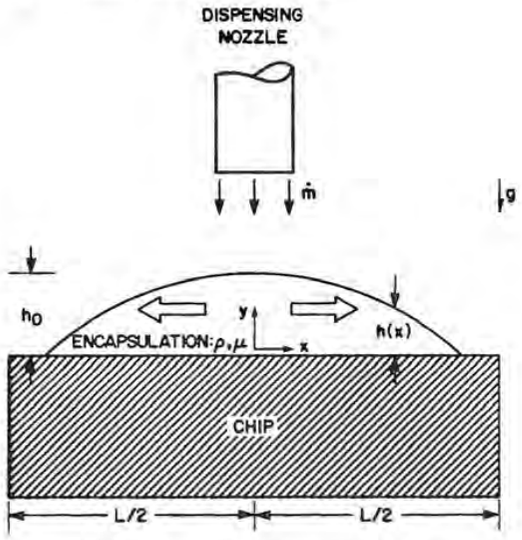


Figure 8-25. Model of the Radial-Spread Coating Process.

that can faithfully replicate the device topology. A conformal coat can be introduced in a variety of ways, such as spinning, spraying, and vapor deposition. In terms of coating thickness, therefore, the radial-spread method and the conformal technique can be considered as opposite extremes of the coating-processing spectrum.

Devices encapsulated specifically with the radial-spread technology have a more restricted latitude of design configurations. In this process, the surface to be coated is positioned under a dispensing nozzle connected to a fluid reservoir. The surface is generally heated to a given temperature known to impart the appropriate viscosity range to the spreading resin. A pressure pulse of known magnitude and duration is then applied to disgorge a calibrated volume of material. The flow is essentially surface-driven, and viscous effects tend to dominate during the injection. It should be stressed that the logistics of the process currently allows only the top and any exposed areas of a chip to be coated. Figure 8-25 depicts a model of the coating process.

Material flowing out of the nozzle impinges against the surface and fans radially outward. Once the calibrated volume has been dispensed, a short-time interval is usually maintained to allow for complete breakup of the resin stream. Premature retraction of the nozzle will entrain some of the resin and result in incomplete coverage. Some of the operating parameters include reservoir pressure, resin viscosity, separation distance between nozzle and

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surface, characteristics of the pressure pulse, nozzle shape (conical versus straight), nozzle rigidity, and nozzle tip (angled versus straight). Vacuum pullback is often needed for low-viscosity materials to reduce dripping between shots. In some applications requiring the delivery of small and precise quantities of resin, a positive-displacement design may be more applicable. In this case, controlled retraction of the piston would exert suction on the material to negate the effects of gravity.

At steady state, the thickness of the coating is fairly uniform and is independent of the volume dispensed. Any flow nonuniformities have been smoothened by surface tension. This applies mainly to large and essentially unbounded surfaces. With areas that are delimited by edges (e.g., silicon dies), on the other hand, a certain thickness can be built up before overflow would occur. However, during the injection step, a certain thickness profile is induced — thick at the impingement point and progressively thinner towards the outer edges. Such thickness distribution is governed mainly by the mass flow rate. For fast-reacting resins and highly viscous materials, this will be the final profile preserved. Obviously, the spreading rate of the advancing front into recessed corners depends on the rheokinetics of the particular resin used. Unfortunately, sole reliance on surface tension to cover the die corners is not sufficient. Current practice calls for the use of a programmable motion table equipped with a dispensing arm which can follow the contour of the chip. Various options for the travel pattern of the arm can be programmed. For instance, it can follow the contour of the chip to dispense a light stream of resin that would then essentially act as a dam holding back any material subsequently injected within the encircled area. Similarly, in another alternative, the four corners would be covered first with small drops, followed by a larger deposition at the center. A succession of small drops deposited according to some preprogrammed pattern can also be visualized. Spreading of the resin would cause the fronts to reach out and merge with one another into a thin coating. In some cases, however, the topology of the surface may not be very conducive to spreading. Bond pads and beam structures can readily act as dams to stop the advancing front. In such a case, directing a stream of air at the surface would force the material radially out and speed up the coating process.

After the deposition, the coated package is usually conveyed to a curing station where some form of energy input is imparted to initiate the polymerization. Heat is commonly delivered either via a convection oven, a series of infrared lamps, or more efficiently, by dielectric or microwaves beamed directly at the package. When the resin chemistry requires a particular curing schedule of increasingly higher temperatures, a series of heating stations would be needed. In order to obtain reproducible curing conditions, good control of the residence time needs to be maintained.

8.5.3.1 Advantages

1. Thin coating — Depending on the application requirements, the use of a resin with the appropriate viscosity can produce very thin protective coatings (typically less than 2 mm). The resulting package can thus be smaller than the conventional DIP or PLCC counterpart, and is an attractive feature of TAB.

The low-viscosity character of UV curable resins, for instance, can produce extremely thin coatings. The free radical polymerization often encountered in such resins produces systems with relatively short curing times. In this case, the flash of an intense beam of UV light would be sufficient to decompose the photoinitiator. Depending on the coating thickness, curing can be started and completed in from a few seconds to a few minutes.

2. No deleteriously high molding pressure — The process takes advantage of the wetting and spreading characteristics of the particular resin selected. Although the advancing front has some momentum inherently associated with it, the forces generated are negligible. No molding pressure is applied directly to the chip surface, eliminating the risk of damaging the fragile interconnecting beams. Current wirebonds have a typical pull strength of between 5 and 10 grams. This is sufficient to resist the shearing motion induced by the advancing melt front encountered in a transfer-molding operation. However, with higher I/O devices, longer wires are installed on the device. The resulting wire loops, anchored only at the two endpoints, have the freedom to sway back and forth to accommodate the surrounding flow field. In fact, this is exactly what happens once the melt front enters the cavity. The wireloops will be displaced in the flow direction, causing wires to cross over one another, and leading to disastrous shorts. However, wire wash is unlikely to be a problem with TAB packages. The bonds are quite strong, residing somewhere between 50 and 100 grams. Similarly, the beam leads are also designed to be sturdy and can readily stand up to the melt front.

3. No flow and/or cavity-filling problem — These are issues present only when complex multicavity molds are invoked in the process. The need to determine experimentally, for a given mold geometry, material, and set of processing conditions, values of such variables as pressure, pressure drop, temperature, shear stress, shear rate, and cooling time at specified points within the mold is no longer necessary. The radial-spread coating technique also eliminates the alternative and equally complicated issue of determining the optimum mold geometry that satisfies certain operating conditions. For instance, one of the most common problems facing the mold designer is to balance an unbalanced runner system by sizing the flow channels to accommodate a given flow rate and pressure drop. It is currently difficult to predict accurately the rheology of the reactive flow in such a case. Shear heating

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during injection of the resin into the narrow gates and runners speeds up the polymerization, and complicates the picture even further. Some design "rules of thumb" do exist but are based more on intuition and experience than on a fundamental understanding of the rheokinetics of the thermosetting material. The absence of any tooling simplifies the packaging and dramatically reduces the large capital expenditures for tooling necessary in any molding operation.

4. Adaptability to TAB — The resin is directed to wherever the dispensing nozzle is aimed. Unless provisions for clearance underneath the chip are allowed for flow pathways, coverage is limited only to the top exposed surface. The sequential operation involved lends itself readily to a TAB application. For instance, the tape can be positioned so that each chip is located strategically underneath the nozzle. After the desired amount of material is dispensed, the tape is reeled forward to the next frame. Good repeatability is achieved via the accurate positioning of the syringe arm, dispensing nozzle tip, and tape indexing. Nevertheless, with the appropriate resin viscosity, there is an allowance for a small margin of error which is lacking in transfer molding. Slight misalignment will still produce good coverage. The surface-driven nature of the flow is such that the material front will stop at a sharp discontinuity in topology, e.g., the edge of the chip. The material will then redistribute itself over the rest of the surface to produce a coverage that would be hard to achieve under similar conditions with B-stage thermosets.

8.5.3.2 Drawbacks

1. Susceptibility to moisture absorption — The benefit derived from the small dimensions associated with the radial-spread coating is obtained only at the risk of providing inadequate moisture protection. In the TAB package, the chip is protected only from the top, unlike standard DIPs and PLCCs. Bare silicon on the sides and the back is left exposed in order to reduce the size of the package. This may provide potential paths for moisture to leak in and initiate corrosion.

2. Narrow viscosity window — The degree and rate of coverage of the chip are controlled by the resin viscosity. An ideal resin for radial-spread coating should exhibit just the right viscosity at a given temperature for good flow and wetting characteristics. Low-viscosity resins would promote rapid surface coverage. With TAB, however, low viscosities will cause the resin to spread onto beam leads to form an undesirable cloverleaf pattern. Another problem with surface-driven flows is the tendency for the liquid to minimize its state of internal energy by adopting the familiar spherical shape. Such a flow pattern would be ideal for the coating of packages with a circular pattern. However, with the square or rectangular shapes common to standard chips, the four corners and corner lead connections are left potentially uncovered

with the ensuing exposed metal lines. Installing an X-Y-Z programmable-motion control table to dispense the resin in a predetermined pattern would eliminate this deficiency.

3. Stress from one-sided coverage — Another disadvantage to one-sided chip coverage is the state of stress imbalance created by the curing and postcuring required of the encapsulation. The encapsulant shrinks during the network formation stage as a result of the gradual loss in free volume of the individual molecules. The degree of shrinkage depends on the particular resin and the filler loading used. For thin TAB coatings, the stiff silicon substrate would dominate the flexural behavior of the package. However, as the coating thickness increases, more stress is applied to the substrate and causes increased bending, with a consequent decrease in the radius of curvature of the device. Care must be taken so that the sign and magnitude of the shrinkage-induced strains reside below the critical strain necessary to fracture the die. The critical strain would naturally depend on the presence and nature of potential defects introduced into the manufacturing steps (e.g., grinding, lapping, and dicing of the wafer). The Griffith fracture criterion can be used to give an estimate of the critical crack length in the silicon die [152]. Incipient failure is postulated to occur when the magnitude of the elastic energy supplied at the crack tip during an incremental increase in crack length is equal to or greater than the magnitude of the elastic energy at the crack tip during an incremental increase in crack length. Assuming a through-thickness crack of length $2a$ in a brittle material of surface energy, γ, and Young's modulus, E, the nominal stress required for crack propagation is given by

$$\sigma = \sqrt{\frac{2\gamma E}{\pi a}} \qquad [8.23]$$

Bending of the silicon is set into motion by the shrinkage of the polymerizing epoxy and the cooling of the package from its postcuring temperature. For a linear shrinkage value of 0.43% typical of a low-stress compound, a coating-to-chip thickness ratio of 1.0, and a cooling differential of 100°C, the maximum tensile stress at the center back side of the chip is around 25 MPa. With γ = 930 erg/cm^2 and E = 106.9 GPa, the corresponding critical crack length is slightly above 200 μm. This suggests that fracture of the die is likely to occur under previous loading conditions when a crack reaches that magnitude. Alternatively, this may also happen when the die already possesses inherent flaws of such size and subsequently subjected to a critical stress σ. Handling of the chip during manufacturing steps such as lapping or grinding should, therefore, be done with extreme care.

The reported value for the K_I factor for bulk silicon is 0.7 MPa $\sqrt{m}$ [153, 154]. This is the mode *I* loading for fracture instability with small crack

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tip plastic deformation. Such a value would describe the inherent ability of the silicon to withstand a given stress field intensity at the tip of a crack and to resist the progressive crack extension under plane strain conditions. Knowledge of such value would give an indication of the tolerable flaw size for a given loading condition on the die. Let us assume that a thumbnail crack is introduced into the silicon die as a result of one of the processing steps. In the one-sided coverage, when such a crack is located on the die back side, a more dramatic effect would be obtained than with an edge crack. The resultant K_I factor is given by the expression [155, 156]

$$K_I = 1.12\sigma\sqrt{\frac{\pi a}{Q}} \qquad [8.24]$$

where Q is the shape factor, which is an elliptical integral reflecting the configuration of the crack Q is described by

$$Q = \int_0^{\pi/2}\left[1 - \left(\frac{c^2 - a^2}{c^2}\right)\sin\theta\right]^{1/2} d\theta \qquad [8.25]$$

where a and c represent the minor (depth) and major (length) axes of the crack, respectively. For $a/2c$ ratios between 0 to 0.6, Q varies from 0.7 to 3. With the previous estimated crack length of 200 μm and a corresponding Q of 2.25, Equation 8.23 estimates a critical fracture stress of 37 MPa. Such stresses lie within the range of values observed to promote fracture through the silicon devices.

The stress profile and the resulting strain distribution within the package can be readily estimated either by modeling the device as a multi-ply laminate or by finite element analysis. Such an approach would be extremely useful to the setting of processing parameters such as the optimum ratio of coating to substrate thickness, the ideal modulus and thickness of the passivating layer, or the TCE of the encapsulation.

The stress field within such a region is analogous to that encountered around a fibrous reinforcement, its coating, and the surrounding matrix (metallic or polymeric). Without the coating, there is a rather sharp stress gradient across the fiber-matrix interface. The shear-lag analysis applied with the assumptions that both fiber and matrix remain elastic can readily describe that stress field. The tensile stress is zero at the fiber ends and reaches a maximum at the center of the fiber. However, the shear stress achieves a maximum value at the fiber ends and falls almost to zero in the center. There are regions in the fiber which do not carry the whole load so that the average stress in a fiber of a certain length is less than in a continuous fiber subjected

to the same external conditions [157, 158, 159, 160]. Under conditions of high loading, the resulting large stress field is likely to result in shear debonding at the interface, initiate cracks, and facilitate their damaging propagation. The addition of a passivating coating on the fiber reduces the stress concentration by redistributing the load more evenly. This holds only when the coating is compatible to both fiber and matrix. When such a condition is met, the coating can play a major factor in the dramatic increase in interlaminar shear stresses observed in fibrous composites [161, 162, 163, 164, 165, 166, 167].

Finally, to retain proper electrical integrity, bending stresses within the device should also be small enough to avoid the shifting of metal lines. As was pointed out earlier, in the extreme case, shifting motions can be within 6 to 7 μm — enough to affect the time constant and other electrical operating parameters of the device. Some of the options available for reducing the one-sided stress issue may encompass the coating of the back side of the chip, backbonding to the board, or a similar arrangement where a rigid backing structure is attached to counter the negative effects of the bending stress field, the formulation of encapsulation materials with lower stiffness moduli, or even the casting of a complete package to enclose the chip on all sides.

4. Long cycle time — The nature of the process requires the use of resins with rather low viscosities (between 0.1 to a few Pa·s). The advanced B-stage compounds popular with transfer molding are no longer applicable due to their high viscosities. Therefore, resins available for conformal coating are mainly in monomeric form and require much longer gel times. Epoxies formulated for glob-top applications, for instance, take between 6 to 15 minutes at 120°C. For optimum properties, further postcuring is recommended for at least another 6 hours.

8.5.3.3 Resin Chemorheology

The radial-spread coating process resembles the well-known problem of free jet impingement. Indeed, mass and heat-transfer to surfaces from jet impingement is encountered in a wide range of industrial applications. Jet impingement, for instance, is particularly attractive in intensifying the heat transfer rates and controlling the heat transfer distribution over a cooled or heated surface. Turbine-disk cooling systems is an obvious area taking advantage of jet impingement. Drying of textiles and paper, and heat treatment of glass and metal sheets are a few more examples of the versatility of the process. As a result, the problem has been investigated extensively [168, 169, 170, 171, 172].

These studies, however, dealt with relatively high-flow velocities, where the fluid exits the nozzle as a turbulent jet. More recently, round jets impinging on a flat plate with exchangeable heat-transfer enhancing boundaries

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were investigated [173]. Flows were at rather high Reynolds numbers — between 14,000 and 67,000. Under analogous flow conditions, a two-equation k-ε turbulence model which provided for a turbulent kinetic-energy equation and a turbulent energy dissipation can be used [174]. In this hybrid finite difference model, the cells near the wall (viscous sublayer) are assumed to adopt a parabolic kinetic-energy profile which subsequently becomes linear in the fully turbulent region. Impingement at oblique angles was also considered with a similar k-ε turbulence model [175]. Even higher velocity jets were investigated where the dependence of the periodicity of the pressure fluctuations on the separation distance between nozzle and surface was found [176].

Heat or mass transfer with a laminar jet has received less attention [177, 178, 179, 180, 181]. Slot jets (two-dimensional jets) were considered in half of the studies [178, 179, 180], while only a few treated the problem of axisymmetric jets [177, 181]. For instance, the fluid-flow and heat-transfer characteristics of a slot jet with a nonuniform velocity profile was considered [178]. It was discovered that the stagnation point heat, or mass, transfer coefficient corresponding to the initial velocity profile was almost twice as large as that of an initially flat velocity profile. The transfer coefficients, furthermore, were insensitive to the distance separating the impingement surface and the duct exit within a limited range of values. The velocity field within the impinging jet, however, was solved within the framework of an inviscid fluid model. The inviscid solution was then used to solve for the boundary layer heat, or mass, transfer. A similar potential-flow approach to get the main-stream velocity over the flat plate by conformal mapping was used [177]. The boundary layer and the energy equations were then solved via a finite-difference method to yield the Nusselt number, Nu, and the local friction factor, C_f. It is found that when the distance of the nozzle from the plate is approximately three times that of the half width of the nozzle, the profile of the main-stream velocity coincided substantially with that formed by a nozzle placed at infinity. Both Nu and C_f behaved similarly, increasing with a decrease in the nozzle separation distance. At a distance equal to the half width of the nozzle, both Nu and C_f attained values 3.5 times larger than those for a nozzle at infinity.

In a later study, the nonmonotonic decrease of the transfer coefficients with increasing separation distance resulting from the opposing effects of diminished jet velocities and mixing-induced turbulence was recorded [179]. As expected, the surface distribution of the coefficients were bell-shaped, and depended strongly on the initial velocity profile. Increases in the Reynolds number led to a corresponding increase in these coefficients. The analysis was extended further by considering the case of a semipermeable plate to which moderate suction may be applied [181]. Heat transfer to the plate was enhanced as indicated by almost a 10% rise in the Stanton number, St, over the case without suction. In order to make the problem tractable, however, the full Navier-Stokes equations and the energy equation in their vorticity stream function formulation were treated. Viscous dissipation was assumed to be negligible. This was also the assumption postulated in a study [182], which extended the previous development of an analytical solution for the velocity field in an impinging Gaussian jet [183]. It was shown that the jet-velocity profile is uniform when the nozzle is held near the impingement plane. When the nozzle is pulled away far from that plane, however, a Gaussian profile occurs. The analysis converted the inviscid momentum equations into the vorticity equation so as to eliminate the pressure [183]. A stream function was subsequently introduced to satisfy the continuity equation. The resultant third-order partial-differential equation was solved by expressing the stream function as a power series in the radius. These functions were then solved numerically in sequential fashion using the governing equation. However, the solution was of limited usefulness since the axial velocity of the jet must be known at all times. A similar approach to the problem resulted in a numerical solution and an approximate algebraic expression for the same Gaussian jet [182].

The effect of surface roughness on the heat-transfer characteristics of a two-dimensional jet striking a surface with embossed ribs was considered [184]. Large-scale vortex stretching in the stagnation region combined with flow separation and reattachment resulted in transfer coefficients appreciably higher in the downstream region than in the case of a smooth surface. A deviation of the previous class of problems involved the case of evaporation under an impinging jet. A numerical model was subsequently developed to predict the flow and coupled-heat and mass-transfer behavior under a round laminar jet of hot humid air hitting a plane wall maintained at a constant wet bulb temperature [185]. A modified Sherwood number, Sh, was defined and rendered the log-mean mole-fraction driving potential insensitive to the evaporation rate.

The basic coating process has some similarities with the flows discussed previously. The dispensed fluid impinges the surface and spreads radially outward under its own momentum. Heat can be introduced prior to dispensing, during the dispensing, or after coating of the surface is completed. Mass transfer should also be considered when dealing with solvent-laden fluids. Differences in the systems presented thus far reside mainly in the relatively lower Reynolds number flows of the radial-spread coating process. Furthermore, a more difficult picture is presented when dealing with resins which polymerize either during flow or after coating. In either case, heat transfer is critical since it governs the rate of curing and the ensuing viscosity profile in the coating.

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8.5.3.4 Surface Coverage – Related Issues

Coating Thickness: Consider the simplified radial-spread coating description pictured in Figure 8-25. An object such as a chip, a silicon wafer, or a circuit board is placed underneath the tip of a dispensing nozzle. At the onset of the process, the nozzle is lowered to a predetermined distance from the surface. Under normal operating conditions, this surface is stationary throughout the dispensing step. However, with larger areas encountered in the typical circuit boards, for instance, some motion must be imparted, either to the nozzle or to the surface, while material is being dispensed in order to speed up the deposition process. Such motion will also be needed whenever a particular resin-deposition pattern is required for the surface. This task can be accomplished with relative ease by either attaching the nozzle or clamping the surface to a microprocessor-controlled X-Y-Z table.

The surface and the material can also be preheated. In the coating with thin films, for instance, the temperature of the surface needs to be maintained within tight tolerances since the heat transfer will determine both the extent of coverage and the film quality. Surface temperature will certainly dictate the rate of solvent evaporation from the film or the degree of chemical reaction within the coating. In any case, the material viscosity will be effectively lowered, and coverage of the surface by the resin will be enhanced. The latter criterion is critical since the surface could be a chip attached to some type of lead frame carrier via fragile wirebond or a circuit board with active devices needing a protective barrier against external contaminants.

A pressure pulse of known duration and amplitude is then applied to deliver a calibrated volume of material. Alternatively, the resin can also be dispensed via a positive-displacement piston. Each system has its own set of inherent advantages and distinct drawbacks. The process is governed by a host of factors such as resin viscosity, amount dispensed, accuracy and repeatability required, inter-shot material dripping, and maintenance. Selection of the appropriate dispensing mechanism would depend ultimately on the particular set of applications planned.

When the workpiece is stationary, any material dispensed spreads radially outward from the impingement point of the stream. Once some slight motion is imparted to the workpiece relative to the nozzle, however, lines of resin can be formed. In that case, the travel speed of the surface and the rate of deposition shape the width of each line. For simplicity purposes, only the problem of a stationary workpiece is discussed here. The actual thickness of the coating deposited, h, is governed mainly by the interfacial tension between the resin dispensed and the surface of the workpiece. This applies to both nonreactive fluids and to systems with slow kinetics. The value of h can be derived in a relatively straightforward manner [186].

In the following discussion, it is assumed that the surface to be coated is that of a chip. Scale differences, however, should not have too much of an

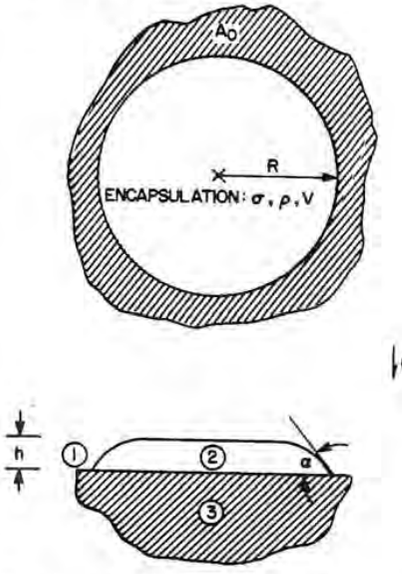


Figure 8-26. Encapsulation Thickness Obtained by Radial-Spread Coating.

effect once nondimensional arguments are used. In this case, the parameters of interest are:

- α, contact angle between the drop of encapsulant and the chip surface.
- μ, viscosity of the resin.
- ρ, density of the drop of encapsulant.
- σ, interfacial tension; subscripts 12, 23, and 13 refer to the air-encapsulant, encapsulant-surface, and air-surface interfaces, respectively.
- A_0, any residual surface left uncovered by the drop of encapsulant.
- g, gravitational acceleration.
- h, thickness of the encapsulation.
- L, characteristic length of the chip.
- R, radius of the spherically shaped drop of encapsulant.
- V, final volume of material coating the surface of interest.

With the assumption that the surface is completely impervious to the diffusion of the polymeric coating as shown in Figure 8-26, h is given by

$$h = \sqrt{\frac{2\sigma_{12}(1 - \cos\alpha)}{\rho g}} \qquad [8.26]$$

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For small contact angle, $\sqrt{2(1-\cos\alpha)} \simeq \tan\alpha$, so that Equation 8.26 reduces to the simpler expression

$$h = \sqrt{\frac{\sigma_{12}}{\rho g}} \tan\alpha \qquad [8.27]$$

At equilibrium, for a chip of large surface area, the thickness of the coating is independent of the volume of the drop and is mainly a function of the interfacial nature between the resin and the chip outermost layer. Equation 8.27 also points out the need for extreme cleanliness in handling the surface. Dirt, oil, grease, or any other contaminant would drastically alter the contact angle and subsequently affect the coating thickness. Furthermore, the equation also indicates that a heavily filled encapsulant would spread out into a thinner coating than an unfilled material. The drop would adopt a spherical shape with a radius, R, given by

$$R = \left(\frac{V}{\pi \tan\alpha \sqrt{\frac{\sigma_{12}}{\rho g}}} \right)^{1/2} \qquad [8.28]$$

Although the resin will spread out to cover the chip surface according to Equation 8.28, surface tension will prevent the four corners from being coated. Proper precautions need to be taken to insure full coverage. This can include, for instance, the use of lower resin viscosity or the dispensing of a multiple pattern of smaller volume shots.

Influence of Resin Viscosity on Thickness Fluctuations: As indicated earlier, at steady state, the thickness of the coating covering the chip is fairly uniform and is independent of the volume dispensed. This applies only after equilibrium has been reached. During the injection step, however, the flow induces nonuniformities in the coating — thick at the center where the bulk of the material is injected and progressively thinner toward the edges. This is the final thickness profile retained with fast-reacting resins. On the other hand, slower-reacting systems such as epoxies present a smoother profile due to the finite time lag inherent in the spreading process. Assuming that viscous effects dominate and that material is delivered to the surface at a rate per unit area $\dot{m}$, the expression for the film thickness over the chip is given by

$$h_0^4 - h^4 = \frac{6\mu\dot{m}x^2}{\rho^2 g} \qquad [8.29]$$

where h_0 is the film thickness at the chip center. For a thin coating, the thickness at the edges can be assumed to be negligible compared to that at the center. In other words, for $x = L$, $h \simeq 0$, and Equation 8.29 reduces to

$$\frac{h_0}{L} \simeq \left(\frac{6\mu\dot{m}}{\rho^2 L^2 g} \right)^{1/4} \qquad [8.30]$$

Equation 8.30 describes the thickness profile over the top of the chip providing that the following two criteria are satisfied:

1. $\frac{\partial h}{\partial x} << 1$, or in other words,

$$\frac{h_0}{L} \simeq \left(\frac{6\mu\dot{m}}{\rho^2 L^2 g} \right)^{1/4} << 1 \qquad [8.31]$$

This condition requires that the coating over the chip surface should be fairly thin. In this case, the thickness decreases progressively from a maximum value at the center, given by Equation 8.30, to a negligible value at the four edges. For the majority of coating applications discussed in this chapter, this requirement holds. Coating of a chip would provide a good case in point since it gives an upper bound to the values of the ratio h_0/L. For a typical chip, L is usually between 2.5 to 5.1 mm. The encapsulation coating thickness, on the other hand, ranges typically from 0.1 to 0.5 mm. The latter values refer to the thickest portion of the coating, measured at the center of the package. For such settings, h_0/L would assume values from 0.02 to 0.2.

2. $\left(\frac{\partial h}{\partial x}\right) Re << 1$, or, $\left(\frac{h_0}{L}\right)\left(\frac{\rho h_0}{\mu}\right)\left(\frac{Q}{h_0}\right) << 1$

where Q is the volumetric flow rate per unit depth ℓ. Since $Q \sim \frac{\dot{m}L}{\rho}$, the criterion reduces to

$$\left(\frac{6\mu\dot{m}}{\rho^2 L^2 g} \right)^{1/4} \left(\frac{\dot{m}L}{\mu} \right) << 1 \qquad [8.32]$$

The injection of the encapsulant must be carried out at a rather low Reynolds number. This can be accomplished either by using rather viscous resins or by maintaining the material exit velocities to moderately low values. Under such conditions, the temporal terms in the Navier Stokes equation can be reasonably neglected. Optimal dispensing conditions call for a delicate balance between these two requirements. A highly viscous material will not provide the good wetting characteristics required for conformal coating applications. Although resins with lower viscosity tend to flow and wet surfaces more readily, it is more difficult to confine the flow front to certain specific areas of coverage. Similarly, a moderate dispensing velocity is also needed in order to maintain reasonable production rates. An acceptable value for the

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Reynolds number describing the laminar flow in radial-spread coating is around 100.

Various criteria can be developed to describe the flow regimes that may be potentially encountered. Similarly, dimensionless variables can also be formed to delineate each flow regime. Therefore, from the onset of an encapsulation run, the best operating parameters can be readily identified [186]. Similar parameters can also be characterized for reactive systems. The reaction rate, in this case, governs the profile dispensed [187].

8.5.3.5 Molding Stresses: One-Sided Coverage

In the two-sided configuration, it was seen that both films exhibit a constant stress which is independent of the film thickness. The film thickness, however, dictates directly the stress profile within the substrate. Furthermore, as long as both films are deposited to the same thickness, the whole composite structure displays a net zero radius of curvature.

The situation is drastically different when only one side of the film is coated with the encapsulant as shown in Figure 8-27 [134]. In this case, once the film is cured, shrinkage of the resin deforms the substrate into the shape of a deployed parachute, with the encapsulation layer on the concave side. The stress in the substrate, $(\sigma_0)_{xx}$, and coating, $(\sigma_1)_{xx}$ can be obtained

$$(\sigma_0)_{xx} = \frac{2C_1}{t_0(t_0 + t_1)R} \qquad [8.33]$$

and

$$(\sigma_1)_{xx} = \frac{2C_1}{t_1(t_0 + t_1)R} \qquad [8.34]$$

where

$$C_1 = \frac{E_0}{1 - \nu_0}\left(\frac{t_0^3}{12} + \delta^2 t_0\right) + \frac{E_1}{1 - \nu_1}\left[\frac{t_1^3}{12} + t_1\left(\delta - \frac{t_1 + t_0}{2}\right)^2\right] \qquad [8.35]$$

and δ is the shift of the neutral axis during bending from the center of the encapsulated structure $[(t_0 + t_1)/2]$ due to the different film and substrate moduli. Small strains are implicitly assumed. Such a shift can be rewritten in the appropriate form as

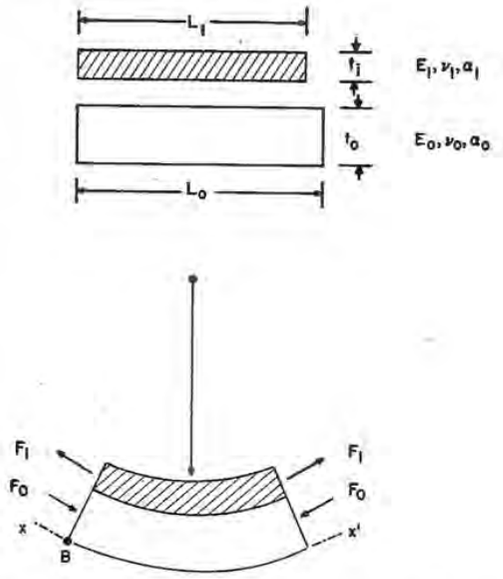


Figure 8-27. Idealized Silicon Substrate with One-Sided Encapsulation. (a) Before curing. (b) Coated substrate after curing.

$$\delta = \left(\frac{E_1}{E_0}\right)\left(\frac{t_1}{2}\right)\left(\frac{1 + \frac{t_1}{t_0}}{1 + \frac{E_1 t_1}{E_0 t_0}}\right) \qquad [8.36]$$

For given experimental values of the radius of curvature R, Equations 8.33 and 8.34 give the stress level within the substrate and film, respectively. R, in turn, can be derived from the compatibility conditions at the film/substrate interface to give

$$R = \frac{1}{L_1 - L_0}\left[\frac{L_1 t_1 + L_0 t_0}{2} - \frac{2C_1 C_2}{t_1(t_0 + t_1)}\right] \qquad [8.37]$$

where

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$$C_2 = \left[\frac{1 - \nu_1}{E_1} + \frac{t_1}{t_0} \left(\frac{1 - \nu_0}{E_0} \right) \right] \qquad [8.38]$$

Thus, for known material elastic constants such as E_0, E_1, ν_0, ν_1, and the physical characteristics of the systems such as t_0, L_0, t_1, and L_1, the curvature of the composite structure can be determined. The effect of resin shrinkage due to polymerization, $(\Delta L_1)_{\text{shrinkage}}$, and the mismatch due to different TCEs can be included into Equation 8.37 by expressing the initial film length L_1 as

$$L_1 = L_0 - (\Delta L_1)_{\text{shrinkage}} - L_1(\alpha_1 - \alpha_0)\Delta T \qquad [8.39]$$

where α_0 is the TCE of the silicon substrate, α_1, the TCE of the coating, and ΔT, the temperature differential between room temperature and the post-cure setting.

Equations 8.33 and 8.34 describe average stress levels in the die and coating, respectively. A profile of these residual stresses, however, has to include the stress component in the z direction perpendicular to the coating/die interface as illustrated in Figure 8-27. Within the substrate, the residual stresses are described by

$$\sigma_0(z) = (\sigma_0)_{xx} + E_0 \left(\frac{z - \frac{t_0}{2}}{R} \right) \qquad [8.40]$$

for $0 \geq z \geq -t_0$. The profile within the coating can be expressed in a similar fashion

$$\sigma_1(z) = (\sigma_1)_{xx} + E_1 \left(\frac{z - \frac{t_1}{2}}{R} \right) \qquad [8.41]$$

for $0 \leq z \leq t_1$ where z is defined from the interface [188].

The analysis reveals a clear drawback of one-sided encapsulation structures. Thermal and curing stresses always create a state of stress imbalance in the configuration, and care must be taken to maintain all the shrinkage-induced strains below the critical value which fractures the die. Figure 8-28 illustrates the stress profile which would be encountered in one-sided coated systems and determined by using Equations 8.40 and 8.41.

Three film thickness are considered, namely, 0.13 mm ($t_1/t_0 = 0.47$), 1.01 mm ($t_1/t_0 = 3.61$), and 2.31 mm ($t_1/t_0 = 8.25$). In the first case, the stresses are highest at the outermost fiber ($\simeq$ 10.7 MPa), decrease linearly as one progresses toward the neutral plane located at $z = -0.20$ mm, where they change sign to become compressive up to the interface. Only tensile

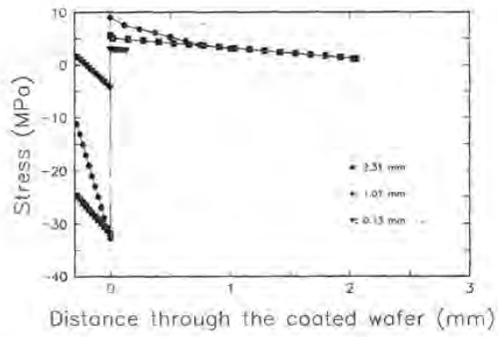


Figure 8-28. Stress Profile Through an Encapsulated Silicon Substrate. Three encapsulated systems with different thickness are considered: t_1 = 0.13 mm, 1.01 mm, and 2.31 mm.

stresses are encountered in the epoxy films, varying from a maximum of 20.7 MPa at $z = 0$ for $t_1 = 1.01$ mm to 19.3 MPa at $z = 0.13$ mm for $t_1 = 0.13$ mm. Tensile stresses in films, however, are undesirable because crack propagation is likely to occur in those instances when the stresses reach a critical value defined by Equation 8.23. As the film thickness increases, interestingly enough, the stiffness of the film becomes the governing factor. The whole substrate is then put under compression. For example, at $t_1 = 1.01$ mm, $\sigma_0 = -226$ MPa at the substrate/film interface, while the back of the die sees only −76.8 MPa.

Figure 8-29 shows the stresses observed in a silicon wafer coated on one side with a filled epoxy resin. The curvature of the wafers reported was measured by x-ray diffraction with an automated Elliot Bristol Lang Topography Camera [134]. Each measured radius of curvature was substituted back into Equations 8.33 and 8.34 to give a direct measurement of the stress levels within both substrate and film. As the epoxy film increases, the stress within the substrate increases dramatically. For example, with a coating 0.13 mm thick ($t_1/t_0 = 0.47$), residual stresses within the silicon and epoxy are −9.8 MPa and 20 MPa, respectively. When the film reaches the thickness of the substrate, about the same stress magnitude is recorded, namely 22.8 MPa for the silicon die and 23.4 MPa for the epoxy. With thicker coatings ($t_1/t_0 = 2.5$), the stress within the substrate increases up to 62 MPa, although the film still exhibits an approximately constant stress of 25 MPa.

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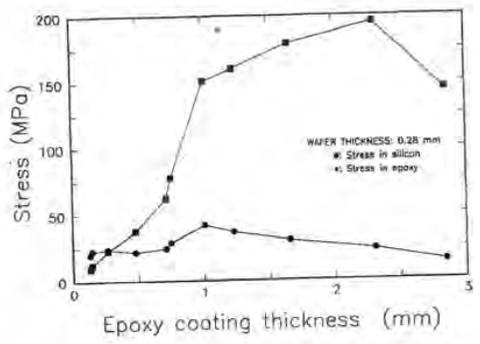


Figure 8-29. Stress Within a One-Sided Encapsulated Structure. Silicon substrate = 0.28 mm. Stresses are determined at $t_0/2$ for the silicon and $t_1/2$ for the film.

8.5.4 Reaction-Injection Molding

Reaction-Injection Molding (RIM) allows rapid in-mold polymerization. The basic process involves metering two (or more) streams of reactants into a small chamber where turbulent mixing rapidly breaks up the reactants into finely interspersed striations. The mixture is next conveyed into a mold cavity while undergoing polymerization. The part is subsequently ejected from the mold once gelation has proceeded to the point where handling can occur without running the risk of warpage or tearing. The total cycle time is typically close to 2 minutes for large parts (e.g., 6 to 10 kg automobile fascia) and much less for the smaller volumes needed for a typical chip-encapsulation operation. A schematic of a typical RIM unit is shown in Figure 8-30.

As was pointed out earlier, polyurethane is the current RIM material of commercial importance. Typical polyurethanes are made of low-molecular

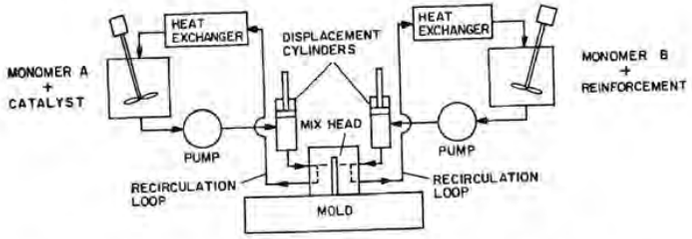


Figure 8-30. Schematic of a Reaction-Injection Molding Unit.

weight prepolymers that mix easily, cure within 10 to 20 seconds, and display a moderate exotherm posing little danger of thermal degradation. Other two-part reactive polymers, such as epoxy, polyester, nylon, and polydicyclopentadiene, are also under active consideration.

RIM is an ideal candidate process for encapsulating IC packages. It can offset the drawbacks inherently associated with transfer molding and radial-spread coating while displaying the following advantages.

8.5.4.1 Advantages

1. Energy efficiency — Metering low-viscosity components consumes much less energy than pumping highly viscous prepolymers. For ideal mixing conditions, RIM requires that the viscosities of the reactive components be less than 10 Pa·s — preferably 1.0 to at most 5.0 Pa·s. Current resins formulated for RIM applications have such viscosities, which increase further with the addition of fillers for improved part dimensional stability. A polyurethane part, for instance, is made from the reaction between two low-viscosity monomers such as a polyol and an isocyanate. Such a part contains an energy content of about 90×10^6 J/m^3, a value which includes a processing energy of only 0.25 J/m^3. A transfer-molded compound, by comparison, requires a processing energy of close to 130×10^6 J/m^3. During large-volume production, this could potentially add up to substantial energy savings.

2. Low mold pressure — The injection pressure is confined mainly to the small mixing chamber. Current commercial machines operate at impingement pressures below 20 MPa. The high stream momenta rapidly reduce the scale of segregation down to a few microns to facilitate molecular diffusion across the component lamellae. With resins such as polyurethanes that can be catalyzed to react in less than 10 seconds, reaction planes can be formed rapidly and the process becomes diffusion-controlled within the tool cavity [189, 190]. However, delivery of the mixture into the mold cavity is usually carried out in a laminar mode to minimize air entrapment. Mold cavities encounter typical pressures between 0.3 MPa to 0.5 MPa. Such a low pressure allows the rapid molding of either small- or large-area parts with relatively inexpensive molds. Heavy clamping forces are not required and, thus, eliminate the need for any expensive mold carrier. The potential damage, wire wash, and shearing of wirebonds or beam leads that plague transfer molding would be eliminated.

3. Good wetting of chip topology — Resins formulated for RIM applications possess relatively lower viscosities than resins processed by transfer molding. Mold filling is conducted while the mixture is still partially under monomeric form. Tailoring the kinetics to the proper rate would allow for complete cavity

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filling before gelation and produce knit-line-free parts. Better wetting of chip and lead components would also yield better resin/chip adhesion interfaces.

4. Adaptability to TAB — RIM can be readily adapted for high-volume production and automation. Since the pressure generated within the cavity is much lower than in transfer molding, light mold halves made of aluminum or composites rather than the usual heavy tool steel can be used readily. In one scenario envisioned for TAB production, for instance, a mold with a multicavity linear track can enclose several tape frames at once. Cavities can be designed to provide different coverage configurations, e.g., top, top and sides, or complete enclosure. One single RIM mixhead can then dispense materials to the whole tool. After curing, the encapsulated portion can be ejected and the whole tape indexed to the next sequence of frames.

5. New materials — A wide range of materials can be processed by RIM. As already mentioned, aside from epoxies and silicones, other materials that can be used would include, for instance, thermosets such as polyurethanes, polyesters, and phenolics, or thermoplastics such as nylon and polycarbonate, or finally, IPNs. With a judicious selection of material combinations, resins with low shrinkage, low stress, low TCE, high purity, and good barrier properties can be processed.

8.5.4.2 Drawbacks

1. Need for good mixing — RIM systems are mainly mixing-activated. Once the streams of reactants are injected into the chamber, both mixing and reaction kinetics act in unison to decrease the composition inhomogeneities. The interrelationship between chemical reactions and turbulence can be described in terms of a ratio of time scales. The characteristic time of the reaction, t_k, is expressed by the inverse rate constant, while the characteristic mixing time, t_m, is assumed to be of the order of the decay time of the fluctuations in the scalar field. Three cases can be visualized [47, 191].

1. $t_m/t_k >> 1$: Very rapid reaction occurs. In the initial period, the distribution of the species is nonuniform and the reaction will be diffusion-controlled. Thus, the more intense the mixing, the smaller the scale will be, and the faster the reaction will be completed. This is the range of current RIM formulations.
2. $t_m/t_k = (O)\ 1$: Moderate reaction ensues and complex coupling between the kinetics and turbulence prevails even under statistically homogeneous conditions.
3. $t_m/t_k << 1$: With slow kinetics, the mean composition concentration dictates the rate of reaction since fluctuations in the reactant species will be smoothed out by the turbulent flow field.

Optimum properties are obtained only through intimate mixing of the reactants. Fortunately, the scale of mixing is relatively well characterized, and several aftermixer designs have been proposed to reduce the scale of segregation even further [192, 193, 194, 195, 196].

The scale of mixing was determined by impinging two reactive streams, allowing the mixture to react and set, extracting one of the components with an etching solution, and studying the resulting morphology with an image analyzer to determine the cell size of the dissolved component. The morphology of a RIM part is found to approximate the flow field generated where each cell represents either a single eddy or a cluster of smaller eddies. The largest eddies can be as large as the width of the flow and carry most of the flow momentum. The corresponding length scale, also referred to as the **integral scale**, is often used to depict the dynamics of turbulence. However, due to the nonlinearity of the mechanics, smaller eddies are formed continuously and get progressively smaller until their kinetic energy is dissipated entirely by viscous effects. The main difference between two turbulent streams with similar integral scales but varying Reynolds numbers resides in the size of the small eddies. As a result, the impingement scale obtained in RIM can be estimated using the Kolmogorov microscale for an isotropic turbulent flow. Dimensional analysis suggests that [192]

$$\frac{\ell_m}{D} \sim Re^{-3/4} \qquad [8.42]$$

where ℓ_m, D, Re represent the mixing scale, the characteristic dimension in the machine (usually the width of the mixing chamber), and the lowest stream Reynolds number, respectively. Figure 8-31 provides experimental verification of the exponent $-3/4$. The influence of the stream Reynolds numbers on the geometric mean of the cell and, correspondingly, on the eddy sizes, is illustrated for different gel times. The trend observed suggests smaller cell (eddy) dimensions at higher Reynolds numbers and faster kinetics. Slow reaction rates would allow coalescence to occur, resulting in a broadening of the cell-size distribution. The constant of proportionality in Equation 8.42 depends on the impingement configuration, the runner and mold geometry, the reactivity of the resin systems, and the corresponding stoichiometric ratios.

Mixing research in RIM has focused primarily on single-stage impingement of either two or three reactants. Aftermixers have been assumed a priority to enhance mixing, although experimental evidence was obtained mainly with model fluids at relatively low Reynolds numbers [192]. It was only recently that multiple impingement has been studied [196]. Multiple impingement refers to the act of impinging the reactants once in the mixing chamber (primary impingement), breaking up the mixture into two separate streams for reimpingement (secondary impingement), and repeating the process through several more stages until the desired scale is achieved. The

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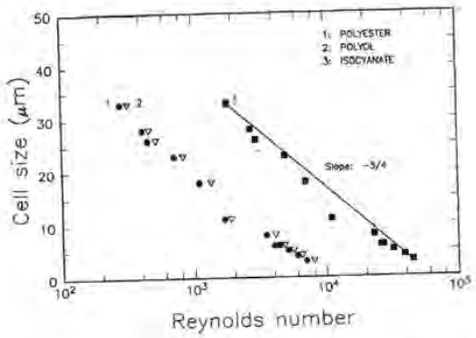


Figure 8-31. Scale of Mixing Obtained in a RIM Mixing Head. Cell size with the greatest frequency in a 50/50 polyurethane/styrene blend obtained at varying gel times (30, 70, 120, 180, and 200 sec) and for different polyol stream Reynolds numbers.

analogy with a cascading flow can be readily visualized, which gives the terminology of "cascade-impingement." If $\ell_m^{(i)}$ is the length scale obtained after the i^{th} step, after n stages, the degree of mixedness would be

$$\frac{\ell_m^{(n)}}{D} \sim \left(Re^{-3/4}\right)^n \qquad [8.43]$$

Equation 8.43 assumes that the Reynolds number can be maintained constant from one secondary stage to another and that mixing improves continuously down the cascade. The assumption of a constant flow rate should apply reasonably well within the first few stages. However, path restrictions and frictional losses would affect the pressure drop as the mixture flows along the cascade. Using the same extraction technique reported earlier [195], it was found that the mixing scale can be decreased further by incorporating a cascade-impingement feature into current RIM units. However, an upper bound on the mixing improvement obtained appears to exist. Indeed, transition zones in the cascade are demarcated by the skewness of the cell distributions achieved. Relatively narrow distributions are obtained up to the transition zone which, depending on the impingement conditions, can vary from 10 to 30 stages. Beyond this zone, increasing the number of stages provided only marginal returns on the mixing goodness.

Another aspect of impingement mixing that also needs to be addressed is the incorporation of fillers in the resin. In order to lower the TCE of the resin, it will be necessary to introduce fillers into one or both streams. High-

filler loading, however, will raise the resin viscosity, require constant bath agitation to prevent settling, and increase the power needed to inject the streams at the high Reynolds numbers needed for good mixing. The reaction must also be tailored to allow sufficient time to fill all the mold cavities before gelling would start. Too short a reaction time generates wasteful short shots, while slowing down the process would lengthen the cycle time.

2. Unavailability of proven resin systems for electronic packaging — Although several potentially attractive systems for electronic packaging can be examined, there still is no proven resin tailored for RIM encapsulation. The organometallic catalysts added to current polyurethanes, for instance, would be highly undesirable from a corrosion point of view.

Epoxy RIM systems have been marketed for some time but have not sparked as much enthusiasm among users as with earlier polyurethanes. Cost and slower cycle times compared to polyurethanes have contributed to their lackluster performance. Another factor to consider is the glass transition temperatures of the resulting RIM materials. In order to facilitate the metering and pumping functions, low molecular-weight reactants with correspondingly low viscosities have to be used. The resulting T_gs are thus lower than would be obtained with B-stage thermosets. For instance, the experimental epoxy RIM systems currently marketed by Shell Chemical have heat-distortion temperatures between 100°C to 110°C. B-stage thermosets synthesized for encapsulation purposes, on the other hand, display T_gs in the upper 150°Cs. High T_gs are imperative to future high I/O packages requiring more power dissipation. Formulating a resin system that satisfies this viscoelastic requirement will be a challenge.

More recently, a fast-reacting cycloaliphatic epoxy formulation suitable for RIM encapsulation was successfully prepared [150, 197]. Cycloaliphatic epoxides have several features which are attractive for encapsulating electronic devices, such as low ionic impurities, low viscosities, and high-temperature electrical characteristics. In the unmodified state, however, these epoxies have rather poor toughness and cannot withstand the harsh thermal-cycling treatments imposed on any potential encapsulant. For instance, thermal-shock test conditions from -40°C to +150°C applied to unfilled cycloaliphatic epoxies may result in microcrack formation, loss in mechanical integrity, and decrease in adhesion to chip components and interface. The addition of flexibilizing agents can improve toughness of the material albeit at the cost of lowering its heat-distortion temperature and strength. Indeed, formulations with low molecular-weight (< 2,000) flexibilizers produce compatible single-phase systems with T_g residing somewhere between those of the flexibilizer and the unmodified resin. A more successful approach incorporates a second phase within the cured matrix using a carboxyl terminated nitrile rubber as the reactive flexibilizer [198]. Two to tenfold improvements

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were observed both at room temperature and at −70°C with rubber modifications of only 4 to 33 (weight) %. In the molecular weight range from 4,000 to 9,000, this two-phase morphology was also observed [199].

In the new fast-reacting formulation, the thermal-shock resistance (TSR) of the cycloaliphatic epoxy was enhanced by the addition of an aliphatic epoxide flexibilizer [150]. Crosslinking was achieved with methyl hexahydrophthalic anhydride. An amine catalyst was used as the initiator for fast reaction. TSR was found to be strongly dependent on both the concentration of flexibilizer present and the level of crosslinking of the matrix.

Figure 8-32 shows, for instance, the effect of the flexibilizer on the T_g of different compositions. In this case, the T_gs were collected with a Polymer Laboratory dynamic mechanical thermal analyzer (DMTA) at 1.0% strain, 1.0°C/min, and for three frequencies (0.1, 1.0, and 10.0 Hz). Along with the individual T_g of each composition, expected values derived from the linear rule of mixtures for a binary system are also shown. Such a rule is described by

$$T_{gb} = w_1 T_{g1} + w_2 T_{g2} \qquad [8.44]$$

where T_{gb}, T_{gi}, and w_i refer to the glass-transition temperature of the blend, that of component i, and the weight fraction of component i, respectively. Equation 8.44 yields an average value based on the weight fraction of each component in the blend, and does not take into account any positive or negative deviations from copolymerization, molecular interpenetration, or reinforcement. The existence of a single T_g in all the blends formulated suggests that the flexibilizer becomes uniformly incorporated into the epoxy network. Actually, a high degree of chemical crosslinking between the two components is present as indicated by the range of changes of the storage moduli. The T_g observed for the blends occurred over a temperature range varying in width from 30°C up to 60°C. For example, the 60/40 epoxy/flexibilizer composition exhibits a T_g of 152°C, with changes in moduli starting around 130°C and ending approximately at 180°C. Incompatible systems usually show much larger spans [200]. The extent of crosslinking in the matrix, on the other hand, was controlled by altering the anhydride/epoxy ratio. When this ratio was changed from 0.75 to 0.97, DMTA scans on 60/40 compositions indicated that the T_gs increased correspondingly, suggesting a rise in the degree of crosslinking with increasing functionality. To achieve optimum TSR, the proper anhydride/epoxy ratio needs to be adjusted. For the current system, the desired nominal ratio is 0.89. High levels of anhydride would result in a rather brittle matrix unable to withstand the thermal shock. While lower levels of anhydride would minimize this cause of failure, the ensuing T_gs would not be optimal.

More recently, another system was considered for RIM encapsulation of electronic components [201]. The resin is a styrene-based material, ionically catalyzed with n-butyl lithium with a small amount of 15-crown-5 added

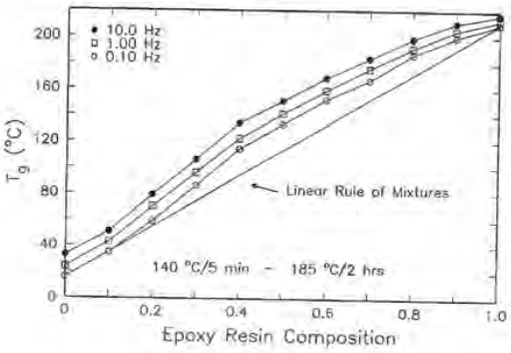


Figure 8-32. Effect of Flexibilizer on Glass Transition Temperature. Measurements were carried out with a Polymer Laboratory DMTA at three frequencies (0.1, 1.0, and 10.0 Hz). The curing schedule was set at 140°C for 5 minutes followed by a 2 hour postcure at 185°C.

to serve as the promoter for faster induction time during polymerization. The violent reaction and large exotherm generated, however, require very close control of the molding pressure and the use of high-silica filler loading (up to 70 weight %). Silica filler particles are needed in this case to reduce the composite TCE and act as heat sinks to reduce the fiery polymerization exotherm. Indeed, more than 16,000 cal/g mole are produced by this polymerization step. Under such conditions, the styrene which has a boiling point of only 146°C, will foam, resulting in undesirably porous parts of poor quality. Unfortunately, the system selected for this study suffers from three main drawbacks, such as low T_g (around 100°C), high ionic impurities (> 100 ppm of Na^+ and Cl^-), and rather high viscosity (> 100 Pa·s) for a typical formulation containing 70 weight % of silica fillers. It is unlikely that the present formulation, in its unmodified state, will ever see any practical use.

8.6 PLASTIC PACKAGE RELIABILITY

8.6.1 Testing For Reliability

Correlating processing parameters and material properties with long-term device reliability is not an easy task [202, 203, 204]. Meaningful answers can be obtained only when the proper failure mechanism is accelerated, and the corresponding acceleration factors are properly understood. Improved formulations of resin compounds have dramatically increased the reliability of

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plastic encapsulated devices. For example, a few years ago it would take less than 1,000 hours to induce failure in a package. Nowadays, on the other hand, more than 5,000 hours of accelerated testing are needed to cause any major device damage. It has even been suggested that, for military applications, the median life of plastic packages for such tests be extended up to 20,000 hours [205]. Three typical stress tests used to predict plastic IC-package reliability are 1) high temperature/voltage bias; 2) temperature cycling; and 3) temperature/humidity/voltage bias.

1. High Temperature/Voltage Bias: High-temperature bias testing is used to accelerate failure caused by device/plastic interaction. Package thermal resistance is crucial in this test since it determines semiconductor junction temperature as a function of power dissipation and ambient temperature. Devices are operated electrically at maximum rated voltages and currents in an oven held at 125°C to 150°C. Overvoltage conditions are used in some cases to accelerate semiconductor oxide failure. Modules are removed periodically for electrical readouts, and failures are analyzed to determine failure mode [206, 207, 208, 209].

Most of the failures occurring on this test can be attributed to the semiconductor, e.g., oxide defects and aluminum electromigration, and are not package-related. However, in a few rare cases, failure modes such as ionic contamination can be traced to the plastic package. Ball-bond failure can occur when overvoltage bias is applied in conjunction with high-temperature testing at 150°C. The typical junction temperature can approach 200°C in these conditions. Eventually the molding compound will break down at these temperatures, releasing methylene chloride which migrates to the gold/aluminum interface of the ball bond. Chlorine accelerates gold/aluminum intermetallic formation, and the bond fails. Failures of this type are characterized by a black void located where the ball contacted the aluminum pad. Microprobe analysis of this area usually reveals chlorine. This failure mode is an artifact of the high-stress condition and cannot occur in the application since junction temperatures are well below the energy required to cause this reaction [210, 211].

More recently, ultraviolet fluorescent dyes were used to demarcate corroded areas in microelectronic devices for microscopic observation. For instance, pH-sensitive dyes can render electrolytic corrosion sites under applied bias visible under fluorescent light [212, 213]. The technique can be extended readily to other uses such as the study of structural defects in insulator coatings and dielectric films.

2. Temperature Cycling: Temperature-cycling tests are used to thermally stress hermetic and plastic IC packages. Typical temperature ranges are:

−65°C to 150°C — 1 hour at extremes; air to air.
−55°C to 200°C — 10 minutes at extremes; liquid to liquid.

0°C to 125°C — 3 cycles/hr; air to air.

Cycling is done with a dual-chamber arrangement with the hot chamber located over the cold. A platform, with module-holding baskets attached, moves between chambers. Transfer and dwell times are programmed according to the particular test specification. Failures accelerated by temperature cycling are:

1. 100% shift in line resistances.
2. Ball-bond lifts.
3. Wire breaks.
4. Chip and package cracks.
5. Single-bit errors caused by passivation cracks on RAMs.

Plastic modules designed with the latest low-stress molding compounds and lead frame configurations routinely pass 1,000 cycles of −65°C to +150°C without failures. Nowadays, typical qualification tests require readouts up to at least 5,000 hours. Similar in nature to this thermal cycling is the power cycling test. In this case, heat is generated by the device through its own power dissipation. While this relates more closely to real-life operating conditions, power-cycling is more difficult to perform and, thus, is not as widely used as thermal cycling.

3. Temperature/Humidity/Voltage Bias (THB): The stress that tests the design, materials, and processes of a plastic IC module most stringently, as well as the sanity of packaging-engineers, is temperature/humidity with voltage bias (THB). This test is done in a T&H chamber which is typically set at 85°C with 85% relative humidity. Modules are plugged into sockets located on load boards that are inserted into a wiring cage within the chamber, and are biased with the rated application voltage, which is usually around 5 V. An alternate-pin biasing scheme is currently popular because it serves to stress the chip and accelerates metal migration between module pins external to the package. Devices are removed periodically for electrical readouts, with a typical schedule being 24, 168, 500, 1,000, 1,500, and 2,000 hours. The primary failure mode accelerated by this test is chlorine-induced corrosion of bond pads and aluminum lines.

85°C/85% **rh** is an accelerated stress test, and therefore has a theoretical Acceleration Factor (AF) associated with it. Acceleration factors are constants derived from models or measured from a multicell stress matrix, and are used to predict field performance. Assume the acceleration factor is 1,000 for module operation in a 55°C/25% **rh** environment, and the first corrosion fail occurs at 500 hours on the 85/85 test; then the expected field-failure time for modules from the test population would be 500 hours. The key word here is **occur**. Modules under stress are not monitored in situ, therefore, the exact time of failure is not known. A conservative engineer would use a failure time of one hour after the last readout that had zero fails.

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There are almost as many models for predicting 85°C/85%**rh** acceleration factors as there are companies doing reliability testing of plastic IC modules [205, 214]. Useful models must take into account the testing temperature, humidity, and life for electrolytic corrosion of the aluminum metallization. Any extrapolation of the autoclave results must take into account the aging effects of the plastic.

Multicell matrix testing is also used to measure acceleration factors. Three or more stress cells are set up with different temperatures and relative humidities. Failure distribution is assumed to be log-normal and cumulative failure rate is plotted on log-normal paper. Theoretically, failures from each cell will plot as parallel lines. Extrapolation of these lines will give T_{50} or time for 50% of the population to fail. A line representing field environment can be drawn in parallel to the stress-cell lines. The acceleration factor is calculated by Equation 8.45:

$$AF = \frac{T_{50}(\text{Field})}{T_{50}(\text{Stress})} \qquad [8.45]$$

In practice, plotted lines seldom are parallel, readouts are not done in situ, therefore, time to fail is unknown, and one will wait forever for fails to occur in the low stress cells. To justify the expense of such testing, computer programs are written to bend lines parallel, and failures are assumed in the low cells, but, at least, an acceleration factor can be extracted.

While the 85°C/85%**rh** acceleration factor may be observed with a baleful eye, the stress test itself is useful. It provides a high hurdle that the package designers must overcome by pushing the art in chip passivation, lead frame and molding compound development, and assembly discipline. This test also predicts field performance. Modules that fail at 168-hour readout are manufacturing-defect, related and will almost certainly fail in the field. T&H testing is also used as an incoming acceptance test by quality control. The ability of a plastic IC module to endure 85°C/85%**rh** for 1,000 hours without failure has improved since the late sixties. Figure 8-33 graphically illustrates 85°C/85%**rh** performance over the years for bipolar TTL devices.

Bias-humidity performance improvement of N-channel dynamic random access memory (N-DRAMs) molded in plastic is even more dramatic. These devices are the most difficult to package in plastic because chip size is large with respect to plastic area and DRAM oxides are rich in phosphorus which is present as P_2O_5, extremely hydrophilic material. N-DRAM chips passivated with CVDPSG and molded with the older novolacs had 85°C/85%**rh** performance ranging from 100% fails at 168 hours to 20% fails at 100 hours. The introduction, over a two and a half year period, of nitride passivation, improved molding compounds, phosphorus reduction, and wafer-fab and module-assembly controls, has pushed the 85°C/85%**rh** failure rate below 0.5% at 1,000 hours.

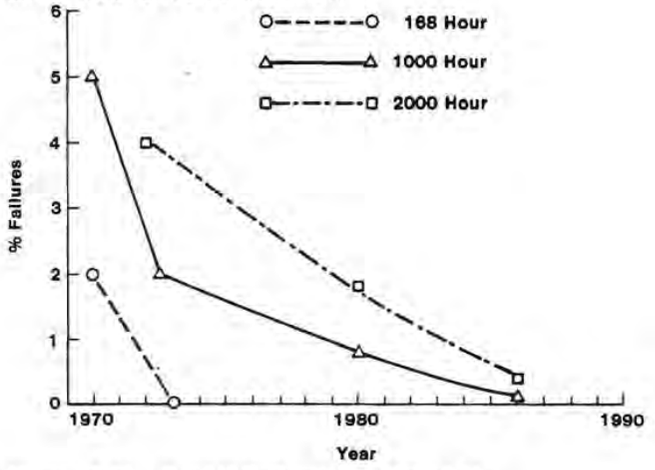


Figure 8-33. T and H Performance BiPolar TTL.

A variant of THB is the so-called HAST, which stands for Highly Accelerated Stress Test. Used for very rapid acceleration of possible packaging failures, HAST applies, aside from the normal biasing voltage, high temperature (100°C to 175°C) and high humidities (50% to 85%). Acceleration factors up to 250 times over standard 85°C/85%**rh** have been reported [215]. It is still unclear whether HAST results can be correlated with real-life failure mechanisms, although published reports have so far suggested that HAST failures are similar in nature to those induced from THB. Chlorine-induced corrosion of the metallization tends again to be the likely culprit. Furthermore, extra care has to be taken in selecting the nature of the carrier gas used in HAST environments. For instance, the reliability outcome strongly depends on whether the carrier gas used is an air/water stream or a nitrogen/water line.

A final variant on the THB is the "G1" test. This is a stress test where connectors, components, or complete packages are tested for over 300 hours in well-controlled gaseous environments selected to simulate real-life operating conditions. Typical gases introduced may include, for instance, chlorine, hydrogen sulfide, nitrogen dioxide, ozone, and sulfur. Gas concentrations generally reside in the parts per billion range and depend on the test purpose. To create suitable office-like environments, rather low concentrations (1 to 100 ppb) are needed. Accelerated tests, on the other hand, require much higher dosage (~ 500 to 700 ppb). Test conditions can vary from 25°C to 70°C with a relative ambient humidity of 70% to 80%. This is shown in Table 8-9.

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Table 8-9. G1 Stress Test. G1 and G2 are for product environments. G1-T and G2-T are accelerated test environments. Gas concentrations are in parts per billion (ppb). Source of data: I.B.M. CB 1-9700-002 (December 1974).

GAS/TEST	G1	G2	G1-T	G2-T
Cl_2	1	5	3	52
H_2S	2.5	15	40	350
NO_2	75	75*	500	700
O_3	50	50*	—	—
SO_2	100	198	351	496
S_8	—	—	0.5	2
TEMPERATURE (°C)	Systems			Components
20 ± 4	70 ± 2			
rh (%)	70 ± 5			80

(*) Minimum, upper limit is not established.

A more comprehensive treatment of reliability theory and modeling is given in Chapter 5, "Package Reliability."

8.6.2 Failure Mechanisms

8.6.2.1 Mechanical Stresses

Shrinkage during polymerization of a thermoset such as polyester generates internal hydrostatic pressures of 14 MPa to 20 MPa as measured with strain-gage transducers embedded in the resin at 120°C [216]. Large additional stresses are set up between the die and the surface when the device cools. Silicon has a TCE of $26 \times 10^{-7}/°C$, while that of a typical filled-epoxy encapsulant is around $240 \times 10^{-7}/°C$. Therefore, when the package cools down from the postcuring step (done around 150°C for at least 6 hours) to room temperature, a temperature differential over 100°C and a corresponding strain mismatch of 2.6×10^{-3} needs to be accommodated. The large stress magnitude involved has often been linked to the damage imparted to the delicate wirebonds. In some cases, interfacial motion can be sufficiently large that shearing and complete lift-off can occur [217]. To relieve the interfacial stresses, current research has been focused at either introducing a passivating layer which will alleviate any potential stress concentration location or at formulating "low-stress" molding compounds.

The "low-stress" terminology, coined by material suppliers such as Hysol, is actually rather misleading. There is not much difference in the TCE values of such materials compared to those of previous standard molding

compounds — approximately between 50 to $80 \times 10^{-7}/°C$. In this case, the main factor that contributes to stress reduction capability of the material is its flexural strength — 120 MPa for the "low stress" resin and only around 50 MPa for the standard compound. The addition of flexibilizers to the resin mix tends to minimize cracking so that the material can withstand more mechanical stresses before the onset of breakage. The stress pattern depends on the size and geometry of the package and can be determined either directly or indirectly. Known test methods have been outlined in a recent publication of the A.S.T.M. Committee on Electronics (Committee F-1 on Electronics, A.S.T.M., Philadelphia [1985]) and encompass the following: finite element analysis, metal-collar method, strain gage on device, piezoresistor, dynamic modulus measurements, thermal shock tests, and stress relief (hole drilling). Each technique has its own inherent set of advantages and drawbacks intrinsically linked to the system size and geometry. Meaningful information can only be obtained by comparing data collected from more than one technique.

Passivation Layer: The passivation layer consists mainly of some dielectric materials such as polyimides. The coating planarizes the topology and is applied either via spinning or spraying. Such a coating is necessary in the back end of the line of complex logic chips with multi-level metallization and lithography. The stress field at the chip/resin interface will be analogous to that at the interfacial region separating a fiber and the surrounding matrix. Without the polyimide layer, stresses developed by the shrinking polymeric coating are sufficient to shift metal lines. In the extreme case, the physical contact between the edge of a sharp filler particle and the underlying circuitry can exert enough pressure to alter the logic state of a memory cell. Thus, the coating acts as a buffer zone to dampen the harsh material mismatch.

The introduction of a low modulus compound to absorb the differential thermal mismatch between the die and the encapsulation has been known for some time. The problem is magnified further due to the resin shrinkage after cure. A variant to the passivation layer concept is the analogous "jelly bean" approach. In this case, the components are draped with a relatively thick low modulus coating, such as silicone or polysulfide rubber. The remaining space is subsequently covered with a high-modulus material for protection during handling. This can be any one of the epoxy systems discussed previously. During thermal cycling or in operation, thermally induced motions will be accommodated by the compliant layer without exerting damaging strain to the device.

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"Low-Stress" Molding Compounds: On the other hand, reducing the TCE of the encapsulation down to a value matching that of silicon is a difficult and challenging task. Positive and negative TCE values for a number of polymers, metals, and ceramics are listed in Table 8-10. Some general observations can be readily made:

1. TCEs for polymers generally lie in the range from $500 \times 10^{-7}/°C$ for polyphenylene sulfide to $2{,}000 \times 10^{-7}/°C$ for polyethylenes.
2. Metals, on the other hand, except for Invar and SuperInvar (TCE $\simeq 10 \times 10^{-7}/°C$), display TCEs ranging from $50 \times 10^{-7}/°C$ for molybdenum and tungsten to close to $240 \times 10^{-7}/°C$ for tin and aluminum (see Chapter 1, "Microelectronics Packaging — An Overview," Table 1-7 on page 37).
3. Finally, the TCEs of ceramics are much wider, spanning over three orders of magnitude. For instance, Corning 7971 has a TCE of $0.3 \times 10^{-7}/°C$, while magnesium oxide has a TCE of $100 \times 10^{-7}/°C$.

One important conclusion to draw from Table 8-10 is that some materials (e.g., Invar and Corning 7971) can exhibit zero TCE at some temperatures and negative TCE over another, smaller range of temperatures. Studies of fused silica, for instance, indicate that the TCE is negative at low temperatures, becomes positive at higher temperatures, and turns negative again at still higher temperatures. The same behavior is observed with TiO_2 - SiO_2 mixtures. At high TiO_2 concentrations, an extended region of low TCE is obtained - around $0.3 \times 10^{-7}/°C$ for Corning 7971 [218, 219]. Obtaining even lower TCEs in single-phase materials seems to be a very difficult problem since current theories of thermal expansion do not provide any guidance for developing such materials. The TCE of such materials seems to be structure insensitive. Small quantities of second phases and oriented grains do have some effect — typically less than 30%. Porosity, dislocation density, grain-boundary area, and stoichiometry, however, have been found to exert no major influence on the TCE.

It appears that the best approach to achieving low or near-zero TCE materials is through the development of polyphase materials. For instance, composites made of a highly anisotropic second phase inserted into an isotropic matrix can have zero or ultralow TCE for a range of temperatures. Low-expansion glasses, graphite epoxy, or metal composites are good examples. However, the anisotropic thermal expansion rules out their usage in quite a few applications. In PC board applications, for instance, the z axis expansion of Teflon® glass is worse than that of FR-4 epoxy glass laminate, being almost three times that of FR-4 at the latter's glass-transition temperature (120°C). Only particle-reinforced systems can yield a material with isotropic ultralow thermal expansion.

Research into the development of mirror substrates for high-altitude large optics (HALO) and high-energy laser optics (HELO) has pointed out

Table 8-10. Thermal Expansion of Some Representative Materials at 25°C.

Material	Coefficient of Thermal Expansion
POLYMERS	
Polyethylene	1,500–3,000
Polyester	954
Nylon	820
Epoxies (cast rigid)	500
Polyphenylene sulfide	540
Polyphenylene oxide	684
METALS	
Aluminum	235
Boron	48
Copper	170
Gold	141
Invar	2
Molybdenum	48
Nickel	129
Silver	187
Tin	235
CERAMICS	
Al_2O_3	54
MgO	104
Fused silica	9
Quartz	18
TiO_2	75
Si_3N_4	8
Supertemp (Pycobond) graphite pitch material	−45
Corning 9617	—
Nb_2O_5 (sintered)	−20
β-eucryptite $(Li_2O \cdot Al_2O_3 \cdot 2SiO_2)$	−60
$SiO_2 \cdot 12Li_2O \cdot 8Al_2O_3 \cdot 1\,GeO_2$	−28
β-quartz $(64.68SiO_2 \cdot 19.9ZnO \cdot 14.9Al_2O_3)$	−3
$Li_2O \cdot Ta_2O_5$	−110
$Ta_{16}W_{18}O_{94}$	−50

an approach that might be extended to the encapsulation of chips. Requirements of high thermal conductivity, high microyield strength, low density, and distortion of less than 0.1 μm/m in the temperature range of 150°K to 300°K were imposed. Only a metal matrix composite can potentially satisfy such constraints. The two experimental systems selected, $Ni - Nb_2O_5$ and

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SuperInvar-Nb_2O_5, exhibited TCEs higher than desired for HALO/HELO applications. It was found that a two-phase metal composite will possess ultralow or zero TCE when the matrix has a low positive TCE while the filler should display a large negative TCE [220]. Furthermore, the volume ratio of matrix to dispersed phase requires very close and accurate monitoring. Good interphase bonding has been assumed implicitly.

A lot of research on estimating the TCEs of particulate composites has already been conducted [221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232]. There are two basic motivations for understanding the TCE behavior of composites. First, as discussed previously, the matching of TCEs is highly desirable since the differential contraction and expansion might lead to unacceptable internal stresses and, second, lowering the TCE of the composite would improve the dimensional stability of the package during manufacturing and thermal cycling.

The first model formulated assumed that each phase is constrained to contract or expand at the same rate as the aggregate [221]. Shear deformation was not postulated. Furthermore, the model does not take into account the aspect ratio of the fillers. Large-scale homogeneity was assumed in a subsequent study [222]. In this case, the second phase is randomly distributed as spherical grains protected by an average shell of surrounding medium. In the limit when the volume fraction of this fluid goes to zero, its properties assume those of the composite. However, a state of isostatic stress was postulated, which seems highly unlikely. Similar equations were derived by others [224, 225, 226, 227, 233]. Qualitative agreement exists for most models with varying degrees of fit. Furthermore, the lack of accurate and reliable TCE values at low-temperature ranges also contributes to the experimental scatter. Yielding of the matrix, debonding at the numerous matrix/filler interfaces, fracture of fillers, and even microcracking during measurement are major causes for the erratic results reported. Another study treated the composite as a core of one phase surrounded by shells of the other [234]. By alternating layers of one phase with the other, a certain extent of interphase mixing can be accounted for. A new approach to the problem was presented where the upper and lower bounds for isotropic and anisotropic composites were determined [235]. This method allowed a reasonable analysis for systems with an arbitrary geometry and number of phase constituents. In some cases, the two bounds converged to result in exact solutions. More often, however, only approximations could be found.

Unfortunately, all the previous models lack the explicit equations describing stress and strain fields developed within both the dispersed filler and the surrounding matrix. Such a fundamental understanding would be needed in the development of a low-TCE encapsulant. Unlike models developed for metal matrix composites, relaxation of the polymer network must be included in any attempt at predicting the behavior of the filled composite. Viscoelastic

properties would accommodate some of the stresses. Nevertheless, the wide-temperature fluctuations encountered during a procedure such as the shipping test can push the design tolerance of a device to its limit. In this accelerated screening, the package is cycled from −40°C to 65°C three times per hour while the resistance integrity is monitored. Testing at such extreme temperatures usually weeds out packages with weak or defective bond pads.

8.6.2.2 Corrosion- and Moisture-Induced Fails

Corrosion in encapsulated components is initiated via a complex mechanism which can essentially be broken down into four steps [236, 237, 238].

1. *Permeation of water through the protective plastic coating*: This is a relatively fast step with respect to the time required to initiate some failure [239]. Even at ambient conditions, considering an effective diffusion coefficient on the order of 10^{-6} cm^2/sec, it takes less than 8 hours for moisture to permeate through a polymer distance of 3 mm, which is about the thickness of a typical encapsulation coating. Sometimes, moisture can also penetrate the package via another unexpected route. During lead forming, for instance, a certain extent of separation is introduced between the lead frame and the plastic coating. In a humid environment, moisture and external board contaminants can migrate along the beams, climb across the network of wirebonds, and, finally, directly onto the die surface [240].
2. *Diffusion of moisture through the bulk or defects in the passivation layer to reach the metallization*: Slightly slower rates have been found than during the previous step [238, 241].
3. *Ionic transport to corrosion sites*: Moisture acts as an electrolyte for all the residual chemicals left by the various processing steps or by the polymer itself [2, 242].
4. *Electrochemical reaction between the aqueous solution and metallization*: It is widely known that corrosion occurs via a combination of the following three reactions

$$6HCL + 2Al \rightarrow 2AlCl_3 + 3H_2\uparrow \qquad [8.46]$$

$$AlCl_3 + 3HOH \rightarrow Al(OH)_3 + 3HCl \qquad [8.47]$$

$$2Al(OH)_3 + Aging \rightarrow Al_2O_3 + 3H_2O \qquad [8.48]$$

If the encapsulated device were dry and hermetic, the aluminum will stop being attacked once Equation 8.46 proceeds to completion. When water is present, however, reaction will continue until all the bare metal has been dissolved away. Only 1.7% water is needed to maintain such a reaction cascade. This translates to an atmosphere of approximately 65% relative humidity at room temperature [243, 244].

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Due to the hydrophilic character of the epoxy bond, water uptake can reach fairly high equilibrium values, resulting in matrix plasticization followed by the ensuing T_g depression [245]. Under the rigorous testing conditions of high temperature, high humidity, and bias voltage to accelerate potential failure mechanisms, swelling of the encapsulation can occur to a certain extent. Even though there is no direct contact between parts and (liquid) water, water vapor will permeate the bulk of the encapsulation, and, ultimately, reach the matrix/bond pads/beam interface. Sufficient water collection can lead to deteriorating adhesion quality and set up numerous corrosion paths. Prior water-sorption studies in epoxy resins indicated that both the kinetics and apparent equilibrium sorption phenomena are strongly influenced by the temperature and humidity history of the samples. Furthermore, diffusion coefficients obtained from analysis based on the dual-mode sorption theory indicated that the heterogeneous nature of the moisture-induced damage to the matrix is associated with the inhomogeneities of regions with low and high crosslink densities [64, 246]. The incorporation of a high concentration of fillers in the matrix strongly affects the water transport properties. This has led to the suggestion, in the case of coatings, that epoxy binder with hydrophobic coal tar would decrease the equilibrium value of moisture sorption [167].

Triple-Track Test: With the higher emphasis recently placed on package reliability, the triple-track test is seeing much more use [247, 248, 249, 250, 251, 252]. Basically, aluminum triple-track patterns deposited on oxidized silicon are used as a test vehicle for checking the efficiency of the doping level in the oxide, the characteristics of some metallization, or the moisture barrier properties of organic conformal coatings and molded-plastic packages. Usually, parts are introduced into a pressure cooker, and standard THB conditions are applied. Surface-conduction currents and track resistance are monitored continuously. Failures are indicated by a sudden rise in conduction currents above some preset threshold, a rise in track resistance, or track opening. The predominant failure mechanism recorded is aluminum corrosion, which is initially manifested as a leakage current increase, and eventually as visually observable dissolution of the metal track. The useful information garnered would be the crucial role of surface contaminant in the corrosion process, especially when thin films of condensed water can be formed at the metal surfaces. In some cases, the triple-track patterns can even be incorporated with other structures onto a single-test device for monitoring the electrical, thermal, and corrosion resistance characteristics of plastic packages [253].

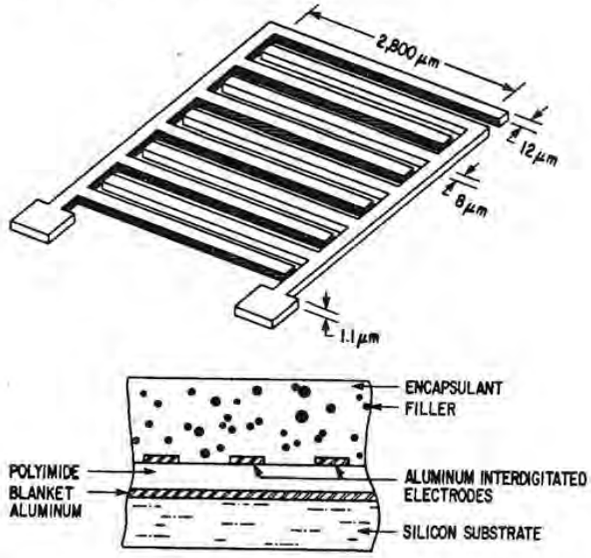


Figure 8-34. Schematic Top View of the Interdigitated Electrode Structure. Each stripe is 1.1 μm thick, 12 μm wide, 2,800 μm long, and spaced 8 μm apart from each other. The cross section of the structure shows a 2.6 μm thick layer of polyimide and a 1 μm blanket layer of aluminum.

Capacitive Measurement: More recently, a direct and quantitative measure of moisture ingress into electronic packages was reported [254]. In this case, interdigitated aluminum electrodes deposited on polyimide-insulated silicon chips were used as capacitors. This is shown in Figure 8-34. The following parameters were investigated: physical characteristics of the encapsulation (e.g., filler size, shape, and loading, and degree of cure of the resin), thickness of the coating, smoothness of the coating (machined versus as-molded samples), configuration of the package (molded versus face coating), relative humidity, and temperature of the surrounding medium. Results indicated that the bare device showed a fairly rapid response time to any changes in the ambient atmosphere. However, when a polymeric coating was layered on the device, the resulting response time was significantly retarded. Initial diffusion kinetics showed Fickian behavior [255]. Water vapor permeation was found to be thermally activated because both equilibrium moisture values and induction times to reach those values were drastically altered by the temperature of the device. The resins studied included two resins,

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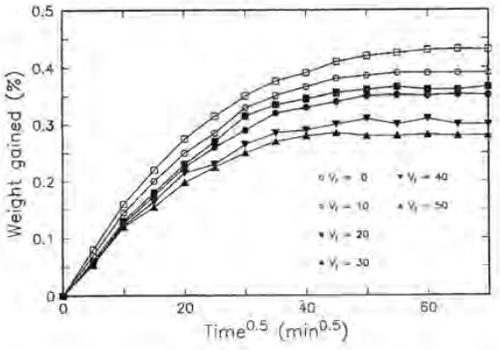


Figure 8-35. Moisture Absorption as a Function of Filler Loading. CNB 435-7 is a blend of bisphenol-A and cycloaliphatic epoxy cured with methyl hexahydrophthalic anhydride. Fused silica particles of 1.5 μm in diameter were used.

namely, a silicone-modified epoxy and a blend of bisphenol-A and cycloaliphatic epoxies.

Figure 8-35 depicts the effect of filler loading on the permeation characteristics of the system. As the volume fraction of silica fillers was raised, dual-mode absorption was recorded. Water molecules are likely to be divided into two populations, one which is dissolved in the epoxy matrix and free to diffuse, while the other is sorbed into microvoids and becomes partially immobilized. Similarly, the diffusion coefficient was found to be strongly in-

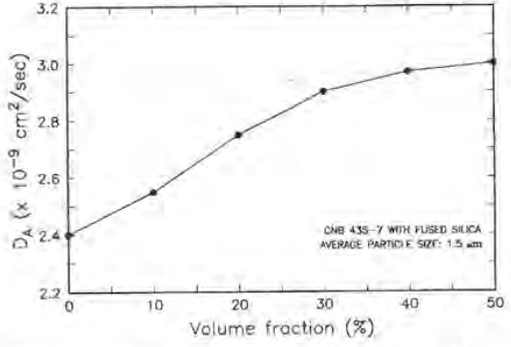


Figure 8-36. Effective Diffusion Coefficient of Moisture in an Epoxy Coating.

fluenced by the filler concentration, as illustrated in Figure 8-36. A host of factors can account for this dependency such as interaction between matrix and moisture, microvoids within the composite, or clustering of water within the polymer matrix.

When the filler-aspect ratio was altered, different permeation characteristics were observed, as shown in Figure 8-37 [256]. For instance, silica flakes were more efficient in retarding moisture ingress into the encapsulant than spherical particles. This is not too surprising, because for the same volume packing fraction, diffusing molecules have to travel a more circuitous route with platy fillers than in the presence of spheres. For each specific absorption level of the epoxy matrix, an equal volume loading of nonsorptive fillers, with an aspect ratio larger than unity, would be more effective in slowing down the rate of permeation.

Another important factor to consider in diffusion through filled media is the nature of the filler/matrix interface. Water can interact with a filler particle either through accumulation in interfacial voids or some surface reactivity. The latter would depend on the polarity of the filler surface. For instance, TiO_2 is highly polar, while copper phthalocyanine blue is nonpolar [82]. The influence exerted by a filler particle is not necessarily limited to the immediate vicinity of the filler surface. Indeed, an "effective" layer, approximately 2,000 Å thick, was found to surround the particle, as determined by x-ray diffraction, electron diffraction, ellipsometry, and vapor sorption studies [82]. However, such investigation assumed that perfect adhesion existed at the filler interface. Poor wetting by the resin would produce localized debonding. The ensuing microcracks act as miniature capillaries that can imbibe high concentrations of water. Annealing the matrix was reported to help since some extent of crack healing can occur from the partial softening [201]. As revealed in Figure 8-37, silica flakes treated with glycidyl ether for enhanced adhesion improve the barrier properties of the encapsulant.

An interesting finding also emerged from the study. The permeation characteristics of the encapsulant were strongly dictated by the hygrothermal history of the sample, as illustrated in Figure 8-38. Once the sample has been exposed to a given environmental condition, the material will sustain some structural damage that can be manifested in the form of microvoids. As long as the material was not subjected to a more severe hygrothermal state, the distribution of these microvoids remained constant. This result stresses caution in the use of accelerated tests for parts qualification since these same tests induce crazing in the matrix which subsequently speeds moisture diffusion into the package.

The configuration of the package tested also dictates the moisture permeation characteristics observed. The previous discussion centered mainly on the face coating profile encountered in TAB. When the same capacitive sensor was molded in 84-lead PLCC configurations, some interesting findings

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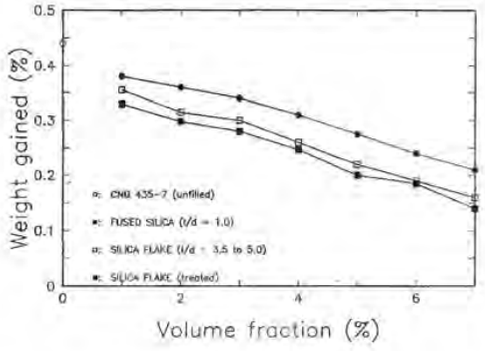


Figure 8-37. Effect of Filler-Aspect Ratio on Permeation Characteristics. Face coatings were 0.25 ± 0.025 mm thick.

were discovered. The following experiment was conducted to study the role of the two major routes of moisture ingress, namely, the bulk of the plastic and the interfacial paths between the resin, the lead frame, and the wirebonds [256]. Four samples were tested at 85°C/85% **rh**: (1) Bare device with no encapsulation; (2) Transfer-molded device cured under recommended conditions; (3) Transfer-molded device rendered impermeable to the environment by blanket aluminum metal deposition; and (4) Transfer-molded device with aluminum metal deposition except near the plastic/lead frame interface. As revealed in Figure 8-39, the bare sensor responded quickly to environmental changes, and was used as a reference to compensate for the capacitive coupling effects of the leads. The sensor with blanket-metal evaporation showed essentially no changes, suggesting perfect metal film hermeticity. The regular transfer-molded package showed a response delayed by the epoxy layer (≃ 1.5 mm thick) on top of the sensor. Water diffusion through the epoxy/lead frame interface was, interestingly, only a minor percentage of the total amount absorbed. Although no coupling agents were used on the Alloy 42 lead frame, the current adhesion seemed sufficiently strong to deter water from migrating into the package via the epoxy/metal interface. Thus, water ingress into a molded package seemed to occur through the bulk of the plastic coating rather than the resin/metal interface. This fact agrees with a previous study conducted with 16-pin DIPs [257]. Failure to detect any significant contribution from the epoxy/leads interface, however, may be due to whether the parts have undergone any thermal cycling. Extended cycling through severe temperature extremes can induce localized interfacial delamination due

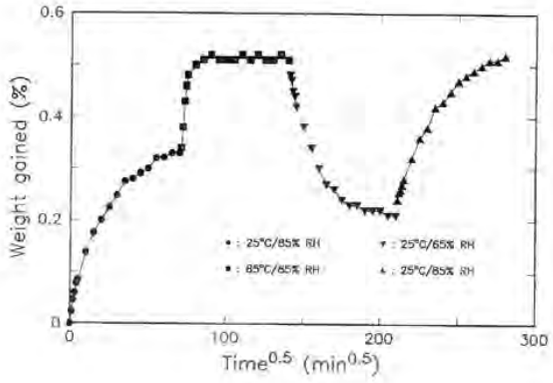


Figure 8-38. Effect of Hygrothermal History on Moisture Permeation. The most important factor in the hygrothermal history of the sample appears to be the highest temperature for a given level of humidity. The irreversible change suggests that once an encapsulant is exposed to a given T/H condition, its structure acquires a certain amount of physical damage which remains constant as long as the sample does not encounter a more severe condition.

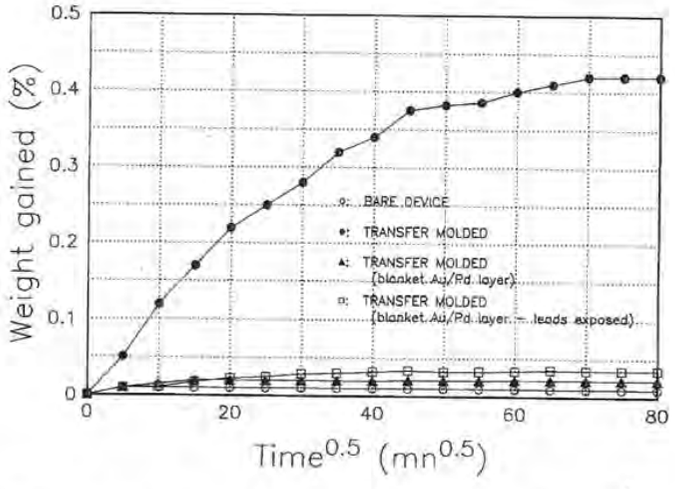


Figure 8-39. Permeation Characteristics of Transfer-Molded Packages. 84-lead PLCC configurations were tested. A low stress silicone-modified epoxy, Nitto HC-10-2-LS (Nitto Electric Industrial Co., Osaka, Japan), was used.

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to the TCE mismatch. Moisture can subsequently leak into the package via these interstitial cracks.

Regardless of the paths of ingress, controlling the resulting level of moisture absorbed in a plastic component is critical to subsequent manufacturing steps. Indeed, during board assembly, for instance, the components are bonded by standard vapor phase or IR reflow techniques. The sudden heat flux applied (up to 260°C for a period varying from 10 to 20 seconds [258]), turns the water trapped within each part into steam, which expands the whole structure unevenly. Package doming is mostly associated with such moisture vaporization. The ensuing passivation cracking and localized delamination eventually lead to a sharp decrease in moisture resistance. This was evaluated by scanning acoustic tomography [259]. Cracks can be easily initiated and propagated across the entire package [260]. This observation occurs only when the moisture concentration is above a certain package-dependent threshold.

Finite-element analysis of standard plastic packages reveals high-stress concentration between the header and the lead frame [9]. During the solder-reflow phase, steam pressure will accentuate this stress profile. For a thin package, the stress located at the corner of the header can exceed the fracture strength of the resin, and ultimately results in bottom cracking. Increasing the thickness of the plastic bottom layer reduces the stress gradient, as would be the case with SOP and PLCC packages. However, this alteration will just shift the high stress profile upward. As a result, when the fracture strength is reached, side cracking is likely to occur. Currently, such "popcorn effect" can be averted by changes in resin composition, chip coating, and lead frame design.

Moisture-Induced Fails: To reduce ionic transport and resist the subsequent electrolytic degradation of the device, corrosion inhibitors can also be compounded directly into the resin. These are compounds that interfere directly with either the anodic or cathodic reaction and, thus, affect the effective corrosion rate [261]. Such inhibitors protect the aluminum metallurgy by one of three mechanisms. Adsorption inhibitors, for instance, have strong polar groups that displace water attached to any exposed aluminum and, in turn, bind strongly to the metal to minimize early stages of aqueous attack. Oxidation inhibitors, on the other hand, induce oxidation of the metal, which can subsequently heal minute cracks and defects in the passivation layer. Finally, buffer inhibitors can alter the local pH differential between the anode and the cathode to effectively minimize the electrolytic attack on the aluminum. Although several inhibitors were evaluated, ammonium tungstate and calcium citrate (both at concentrations less than 1,000 ppm) were found to increase significantly the THB life of the devices tested.

The amount of moisture saturating a plastic package is so minute that special techniques need to be developed for characterization. This was the

subject of a workshop sponsored jointly by the Defense Advanced Research Projects Agency and the National Bureau of Standards (Semiconductor Measurement Technology, DARPA/NBS Workshop on Moisture Measurement Technology for Hermetic Semiconductor Devices, May 1981).

Once moisture reaches the interface, failure of the device can occur in several ways. In one case, the oxide surface becomes partially conductive, resulting in a "charge-spreading" phenomenon that forces the region under the field oxide to invert [262, 263]. Or direct conduction between two metal lines can also happen. In this instance, the moisture-induced leakage of charge stored in a capacitive node of a flip-flop circuit exceeds that generated by the junction-leakage current, which normally governs the node. This second failure mode is general and can be present in any dynamic circuit exposed to high humidity conditions. However, the previous two failures are reversible. Usually, after a bake cycle at 150°C to 200°C for one or two hours, moisture is driven off completely from the package, higher surface resistivities are restored, and the failed device recovers. Exposure to incident light (after removal of the polymeric coating) can also accomplish the same goal. Light produces additional junction-leakage current needed to counterbalance the surface leakage. The activation energy for the latter type of failure was found to reside between 0.40 to 0.70 eV, with decreasing value for decreasing sheet resistance [264]. The charge-spreading mechanism, on the other hand, exhibits an activation energy of approximately 1.0 eV. The surface-conduction mechanism observed in SiO_2 is thought to be due to the dissociation of surface hydroxyl groups or adsorbed water molecules into mobile protons [265]. Once adsorption occurs, the dielectric constant is raised, inducing subsequently a decrease in the proton dissociation energy.

Based on the previous information, the characteristics of the water extract from epoxies used for encapsulation should correlate well with the extent of damage. High pH and ionic content, for instance, should increase the risk potential for corrosion. However, this did not always hold [266, 267]. For small devices (less than 10 mm^2), the failure rate was found to be approximately the same for all the epoxies tested even though one resin exhibited pH, ionic conductivity, and chlorine content of 6.9, 150 $\mu V/cm$, and 7.0 ppm, respectively, compared to a corresponding average of 4.5, 70, and 3.5 for the others. As larger and larger chips were evaluated — from 15 to 36 mm^2 — higher aluminum corrosion fails were recorded for the epoxy with high pH, conductivity, and chlorine content. Forensic examination indicated that every corroded part showed a passivation defect in the immediate surrounding area. After all the manufacturing steps had been traced one by one, the highest defect rate was found to occur right after (transfer) molding, with the highest distribution around the outer edges of the devices. Since the stresses in those areas are approximately an order of magnitude higher than in the vicinity of the device center, and increase with increasing die areas, strong evidence

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suggested that the fails were of thermal- and/or shrinkage-stress origin. As a matter of fact, once the passivation defect-density was computed, direct correlation with failure rates was found. Depending on the type of epoxies used, defect densities introduced vary from 670 up to 1,400/cm², compared to an equivalent of 330/cm² for silicone. This study strongly underlines the fact that for improved moisture resistance, either one or both of the following techniques should be considered. First, stronger passivation layers are required to withstand the stresses from resin shrinkage or from differential cooling after the molding operation. Second, as mentioned previously in the discussion on thermal stresses, flexible resins would provide a certain degree of resiliency to the structure and would exert a milder stress distribution on the die and accompanying circuits.

Moisture is insufficient to initiate the corrosion by itself. Ions present in the package as process residuals (traces of the wafer-cleaning solutions such as sulfuric, hydrochloric, nitric, and hydrofluoric acids, hydrogen peroxide, and ammonium hydroxide), all of which can be heated up to 110°C or leached out from the polymeric encapsulation (e.g., chlorine from unreacted catalysts), form the necessary aggressive complement for promoting corrosion [268]. Intense galvanic effects can be set up since in some small structures, a small area aluminum anode comes into direct contact with a large-area gold-wire cathode. The metallurgical dissimilarity sets up approximately a 3-volt potential. With gold-metallized devices, the problem can be compounded further since conditions can be severe enough to cause redeposition of the gold. This is especially significant at high temperatures, relative humidity, and bias voltages. When a voltage is applied to the device — as during accelerated testing or in actual operation — the resulting ionic breakdown and migration are analogous to a similar phenomenon observed in an electrolyte under electrical bias. At the chip level, once the electrochemical corrosion has been initiated, the kinetics of ionic migration as determined by ion chromatography were found to be relatively fast [3]. Ultimately, the rate-determining step is governed by the kinetics of moisture diffusion through the passivation system, as indicated by the activation energies computed for the various mechanisms discussed previously.

Another form of corrosion failure seemingly unrelated to moisture attack can also occur. Products outgassed from the plastic coating during high-temperature applications have also been found to be highly detrimental to the wirebonds [269]. Outgassing refers here to the evolution of both trapped volatiles and volatile by-products formed during handling at high temperatures. During this particular type of accelerated testing, packages with $Au - Al$ wire bonds are exposed at 200°C without bias to epoxies reacted with either a phenolic or an anhydride curing agent. Overmolding of the packages to be tested essentially allowed the decoupling of stress-induced phenomena from outgassing-induced failures. Analysis of the volatile products by gas chromatography revealed the following compounds in varying proportions. Major components included phenol, acetone, methyl bromide, and propylene, while minor components encompassed water, methane, ethane, propyl bromide, toluene, and methyl isobutyl ketone. Among the trace components discovered were carbon dioxide, methanol, ethyl chloride, benzene, and dichlorobenzene. The trace halogen compounds identified were of interest due to their well-known reactivities with aluminum [270]. Methyl bromide originated from flame retardants compounded into the resin, while ethyl chloride was a probable catalyst residual from the manufacturing of the resin. When pure methyl bromide and ethyl chloride were passed over $Au - Al$ bonded devices for 72 hours at 200°C, numerous bond failures were recorded in terms of lift-offs and drastic strength reduction (down to less than 10% of the original values). Aluminum metallization corrosion was observed around the perimeter of the bond pads. Microscopic analysis of the fail sites revealed a distinct lamellar structure which was highly uncharacteristic of the normal $Al - Au$ intermetallic growth. Such a structural configuration is normally achieved when a single-phase material becomes unstable (e.g., under chemical attack), and decomposes through a growth process into a two-phase morphology. Voiding accompanying the grain boundary diffusion accounts for the degradation of the intermetallic compounds [241]. Similar effects have also been reported to occur with silicone-encapsulated triple-track conductors and resistors exposed to hydrogen chloride [38].

It should be apparent that besides moisture, contaminants, and voltage, numerous other factors can also have a significant impact on the migration and corrosion phenomena observed in plastic encapsulated packages. Operating temperature, for instance, governs the threshold for moisture and contamination, which can subsequently affect the life of the devices. Other factors may encompass thermal cycling, package volume, substrate materials, and line spacing.

More information on general reliability issues can be found in Chapter 5, "Package Reliability."

8.7 NEW DEVELOPMENTS

Plastic packages have evolved from three leaded transistors to 200-pin Quad Flat Pacs in about 20 years. The trend in chip design is less cost per function through higher integration. Package design will follow, with more pins in smaller areas and with higher reliability at reduced cost. Plastic packages will play an increasing role in cost-driven IC packaging in the near future.

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8.7.1 Chip Connection

Wirebonding, a process used since the inception of IC packages, is less effective with pin counts greater than 150 because of geometric constraints. Large chips require less space between bond pads to conserve silicon. Gold ball bonds will not fit on these extremely small pad pitches. Lead frame bonding fingers recede from chip-support platforms as the number of leads increase causing wire spans to lengthen. Lower molding yields result due to wire-sweep shorts.

Tape Automated Bonding (TAB) solves these problems and is beginning to replace wirebonding on high pin-count chips. Bond-pad pitch on a typical wirebonded chip is 8 mils, while metal bumps on TAB chips can be spaced as close as 4 mils, thus allowing more I/O per unit area. Single-chip TAB packages are in production with 176 I/O. Pin counts as high as 350 are in development, with an ultimate target of 500. Even higher I/Os can be visualized without increasing the size of the chip to unruly proportions. Future devices will have active circuits directly underneath the bond pads to conserve precious silicon real estate.

Power dissipation with TAB can be enhanced by mounting a heat sink directly to the chip back side. Heat-sink designs are in development that can handle 10-watt chips. The plastic encapsulant surrounding a TAB chip is much thinner than conventional transfer-molded DIPs or small outline SMT packages. More details can be found on TAB in Chapter 6, "Chip-to-Package Interconnections."

8.7.2 Alternative Materials

As was discussed earlier, encapsulation with B-stage materials by transfer molding results in inherently long cycle times. Deflashing and mold cleaning are two other main deficiencies associated with processing thermosets.

Wasteful scrap is also produced after each cycle. The reacted material collected in the pot, sprue, runners, and gates of large molds can be fairly substantial at the end of a full production shift. Currently, however, such material is discarded and treated as an unavoidable by-product of the process. Recycling has not been considered yet in IC encapsulation because the extra steps involved may introduce undesirable impurities. Nevertheless, when proper care is taken, waste products can be used as fillers/extenders in the same plastic or different plastic matrices [271, 272, 273]. In nonelectronic molding applications, the thermoset waste is fed into granulators. A series of hammermills pulverized the reacted material into 200-mesh-size particles (or finer), suitable for subsequent blending with virgin material. The addition of small amounts of reground epoxies into virgin material will not affect the final mechanical properties of the resin. When good adhesion exists between the recycled and virgin resin, no stress concentration is formed since both

phases have the same stiffness, provided that similar cure conditions are met. The recycled material acts essentially as an extender. Material costs can thus be reduced significantly during large-volume production. Since 20% to 30% of a shot is locked in the sprue and runners of a mold, the amount of savings will be significant. However, care should be taken when reground thermosets contain fibrous fillers. The process reduces the average fiber length and/or filler aggregates. At a high-volume loading of reground material, complications would arise from flow disruption, altering the filler alignment distribution. Furthermore, as the packing of the particles gets higher, little resin is present at the interfaces, weakening the physical integrity of the structure. Any cost saving will be negated by the drastic reduction in strength of the recycled resin.

Replacing the standard epoxy molding compound with other commercially available materials would not alleviate the drawbacks mentioned earlier. One possible alternative often mentioned is encapsulating ICs by injection molding with high-performance engineering thermoplastics. In this case, the thermoplastic is heated until it softens. It is then delivered to the mold cavity under considerable pressure. The cycle time can be much faster than with transfer molding and is governed entirely by the rate of heat transfer in and out of the tool. Cycle times can be around 20 seconds or as fast as frames can be loaded. There is no ongoing reaction and, thus, simpler rheology is involved than with thermosets. Another alternative to epoxy, interpenetrating polymer networks, has received attention only lately, and yet promises to confer encapsulants with a new set of physical properties. These two potentially attractive alternatives to VLSI encapsulation will be discussed next.

A more recent addition to the list includes two newly introduced encapsulating grades of diallyl phthalate (DAP) compounds. The base resin is a diallyl ortho phthalate, which is postulated to be a viable alternative to epoxies. Both grades offer good resistance to humidity and can withstand a wide range of temperature extremes. High dimensional stability and low volatility are two other characteristics of these new encapsulation grades. However, more tests need to be carried out before a proper verdict can be announced.

8.7.2.1 Thermoplastics

The current emphasis on faster cycling, automation, lower pressure, and recycling has the effect of bringing thermoplastic molding into competition with thermoset molding. So far, however, thermoplastics have not seen any direct applications in electronic encapsulation. Discussion on thermoplastics in the electronic industry has been linked mainly to the fabrication of printed-circuit boards [274, 275]. Indeed, certain thermoplastics introduced recently match up very well to the ubiquitous FR-4 epoxy-glass laminate. As shown in

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Table 8-11. Properties of Thermoplastics For Electronic Applications.

Property	Polysulfone	Polyetherimide	Polyimide Glass	FR-4
ELECTRICAL				
Dielectric Constant				
1 MHz	3.0	3.1	4.5	4.5–5.0
10 GHz	3.0	3.4	—	—
Dissipation Factor				
1 MHz	0.004	0.007	0.010	0.20
10 GHz	0.006	0.003	—	—
THERMAL				
Glass Transition Temp. (°C)	190	217	275	120
Combustion (UL-94)	V-2	V-0	HB	V-0
Max. Op. Temp. (°C)	150	170	240	125
COST				
Approximate Price Ratio	6.0	6.0	5.5	1.0

Table 8-11, these materials can exceed the thermal and electrical performance of epoxy-glass.

In making planar boards, for instance, it can be found that polysulfone, polyethersulfone, and polyetherimide can have dissipation factors and dielectric constants closer to those of Teflon® glass than those of FR-4. Plating adhesion to Teflon® glass, however, requires fairly elaborate preparation. With engineering thermoplastics, however, simpler processing methods can be used. One technique, for instance, known as "swell and etch," requires a first-pass treatment with a strong organic solvent such as dimethylformamide to roughen the surface. This is followed by exposing the surface to chromic acid to improve its wetting characteristics, paving the way to subsequent plating operations. Since a Teflon® glass part would cost approximately three times more than its polyetherimide counterpart, there is added incentive to look at thermoplastics. Furthermore, better thermal stability can also be reached with the new materials. The glass-transition temperatures of polysulfone and polyetherimide, for instance, are 190°C and 217°C, respectively. By comparison, FR-4 has a T_g of only 120°C.

Thermoplastics also offer a previously unachievable ability to incorporate three-dimensional features into the boards. Recessed features such as tapered holes, chamfered edges, ribs, supporting structures, bosses, holes, and slots can be easily sculpted into the boards. Aside from the three thermoplastics listed in Table 8-11, others that promise to be equally promising include reinforced nylon 6/6, polyesters (polybutylene terephthalate and polyethylene terephthalate), aromatic copolyester, polyamide-imide, polyimide, polyarylate, polyphenylene sulfide, polyetherketone, and fluorocarbons.

Current work reported in the literature has so far focused mainly on potential uses for high-performance engineering thermoplastics in second and third-level packaging. However, the versatility of the materials has not extended itself to encapsulation yet. So far, there is little work reported on such an application. Processing thermoplastics for electronic packaging presents some complications, which have still hindered their uses. High viscosity and low inherent adhesion are the most serious ones.

1. High viscosity — Depending on the shear rate encountered during injection molding, thermoplastic melts can have apparent viscosities between 1,000 Pa.s to the upper 10,000 Pa·s. Shear thinning can reduce the viscosity considerably. At shear rates of 500 sec^{-1} and 5,000 sec^{-1}, for instance, polyphenylene sulfide has melt viscosities of 3,000 Pa·s and 1,000 Pa·s, with corresponding shear stresses of 0.35 MPa and 0.14 MPa, respectively. Wire crossover and wire wash are likely to occur when the delicate wirebonds are exposed to melt fronts of such viscosities. Even under the much lower epoxy-resin viscosities encountered with transfer molding, shearing of bond pads has already been reported. Thus, unless wirebonds of much greater strengths can be achieved, resistance to using thermoplastics will always be strong. However, with a surface-mounting technology such as TAB, where typical pull strengths lie between 50 to 100 grams, such concern is unjustified. The shear strength would be approximately half of the pull strength. With a typical beam/bump contact area of 0.10 x 0.13 mm, the corresponding shear stresses would be between 20 MPa to 80 MPa — high enough to withstand the melt front.

The moldability window of a given thermoplastic for a given part design can be readily obtained provided a good mathematical model of the melt rheology is established. Unfortunately, although several theories of varying levels of complexity do exist, there is no clear consensus on which one would be the best one to use under some arbitrarily given conditions [276, 277, 278, 279]. The models formulated separately by Bueche [276] and Graessley [277, 278] assumed some degree of chain entanglement which is formed and relieved continuously with the dynamic state of shear. On the other hand, at the other extreme, the familiar sigmoidal viscosity curves can be fitted with a semi-empirical expression such as the Cross equation [279]. At the high shear rates encountered in injection molding, the previous theories can all be approximated by the power law expression. The constant n assumes values of 0, 0.2, and 0.5 for curves predicted by Williams, Graessley, and Bueche, respectively. Data published to date, however, show sufficient scatter that will accomodate all three theories [280].

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2. Low inherent adhesion — Most thermoset resins and some thermoplastics are known to produce chemical coupling with inorganic fillers such as glass fibers or mineral flakes. There is a large body of literature documenting the quality of adhesion of thermoplastics to various surfaces [281, 282, 283]. Generally, the lack of reactive sites in thermoplastics accounts for their relatively weak quality of adhesion to surfaces. Nevertheless, physical coupling via acid/base interactions or solubilization can still occur. Physical couplings, however, are more likely to degrade under stresses than their chemical counterparts. This was found in a recent attempt to encapsulate monolithic ceramic capacitors with polyphenylene sulfide [284]. Poor adhesion between the plastic and the lead wire surface reduced the resistance to moisture penetration, as indicated by the Zyglo test. The problem was further compounded by the numerous leaking interfacial paths between the thermoplastic and the pigments and reinforcing fillers. Indeed, when the fillers were chemically treated for enhanced compatibility, moisture diffusion was dramatically retarded.

Chemical modifications of the basic molecular structure can unleash untapped potential for using thermoplastics in encapsulation. For instance, grafting or end-capping the structure with reactive sites can improve the adhesion between the plastic matrix and the device surface. Similarly, adhesion would also improve by copolymerizing the main chain with low-molecular weight monomers carrying groups compatible with the added fillers. Alloying the matrix with other polymers would be another possible way to achieve the desirable adhesion or moisture-resistant properties. It should be stressed that adding a second component to the primary matrix would introduce another level of flow complexity and unpredictability. When a mixture of two polymers is deformed by the flow field, for instance, shear rate dependent morphologies can develop. One component may be drawn into filaments which may retain that shape after solidification, or break up subsequently into smaller drops. Under the proper conditions, an interconnected network can be generated [285]. Furthermore, in the case of graft polymers, the viscosity is much higher than can be predicted purely from either the composition or the molecular weight of the mixture. Deformation of the two-phase domain structure under elongation and shear accounts for this apparent viscosity increase [286].

8.7.2.2 Interpenetrating Polymer Networks

Interpenetrating polymer networks (IPNs) are a type of polymer alloy made up of two or more crosslinked polymers. The networks interact with each other only through permanent entanglements with only occasional covalent bonding. As a result, IPNs are also sometimes called polymeric catenanes [287, 288]. The entanglements are of a permanent nature and can be formed either sequentially or simultaneously.

The *sequential method* calls for swelling polymer I with a mixture of a second monomer II, the appropriate initiator, and the corresponding crosslinking agent, and curing the swollen polymer in situ [289, 290, 291]. The IPN terminology was initially coined to describe the microscopic interpenetration of two networks in the extreme case of high compatibility. The first IPN was prepared with two networks of identical styrene-divinyl benzene formulations [289]. The equivalent single network was predicted to swell more than the IPN at constant nominal crosslink density. The intrusion of monomer II deforms permanently the matrix of I. Nevertheless, a Maxwell demon released within such an IPN morphology will always be able to recognize the network it is following. Such a concept of network swelling is often used to distinguish one network from the other although both may be chemically identical.

Swelling of either a linear or crosslinked polymer with a smaller-molecular-weight material, however, takes orders of magnitude longer than the typical cycle for molding DIPs (less than 2 minutes). Rapid polymerization is a required and necessary condition for the economic viability of a material geared toward large volume production. Furthermore, a host of other factors, such as test temperature, test pressure, and solubility with the matrix of the diffusing mix of monomer, initiator, and crosslinker also governs the diffusion process. Another direct and faster synthesis route involves the *simultaneous polymerization* of the two networks via two independent mechanisms, e.g., a condensation-reaction and an addition-reaction scheme [195, 292, 293]. For instance, acrylic solutions (addition) can be added to epoxy resins (condensation) and reacted [294]. Phase separation seemed to be the smallest under conditions of simultaneous polymerization.

IPN synthesis does not necessarily have to be limited to binary compounds. Ternary IPNs have also been reported [295, 296]. In this case, polymethyl methacrylate, a polyurethane, and an epoxy were reacted under different polymerization conditions to yield blends of varying morphologies. Special charge groups were attached to the backbones of the individual components to compatibilize the networks. A summary of IPNs synthesized to date can be found in two recent comprehensive studies [296, 297]. Compared to normal polymer blends, IPNs exhibit the following two main features:

- The two components are held together by permanent chain entanglement. Some degree of interpenetration between the networks is usually present. Actually, the IPN synthesis route represents the only way to blend two crosslinked polymers with limited phase separation. With normal blending, the thermodynamic incompatibility generally produces a multiphase morphology. Highly incompatible polymers, for instance, induce such powerful thermodynamic forces that segregation occurs regardless of any kinetic ramifications. With more compatible polymers, however, more intimate molecular mixing can be achieved

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with a lesser degree of domain formation. Nevertheless, perfect compatibility is not required since physical entanglement occurring during the growth of the two networks inhibits segregation to some extent. As a result, depending on the crosslink density, reaction kinetics, thermodynamic compatibility, and surface tension of the individual components, IPNs with phases ranging from a few hundred angstroms to up to a few microns can be created.

- The synergistic properties of IPNs have been attributed to the special two-phase structure and special topology created. When one glassy polymer, for instance, is blended with an elastomer at room temperature, the concentration of each component essentially determines whether the resulting alloy is a high-impact plastic or a reinforced rubber. With complete phase mixing, experimental evidence suggests that mechanical properties such as impact strength and tensile properties are enhanced further by chain interlocking [298, 299]. Dual phase continuity in the IPNs has been established by a series of experiments involving dynamic mechanical spectroscopy, thermal analysis, transmission electron microscopy, and small-angle neutron scattering [300]. Similarly, decrosslinking followed by extraction and scanning electron microscopic (SEM) observation has also been carried out [301]. In this case, a sequential IPN was made by using an initial structure of poly n-butyl acrylate crosslinked with acrylic acid anhydride followed the subsequent *in situ* formation of a polystyrene matrix. When the IPN is exposed to warm ammonia water, the acrylic acid hydrolizes and promotes depolymerization of the initial structure. Extraction would reveal a porous continuous structure of polystyrene.

Although the IPN concept promises a lot of versatility for IC encapsulation, no direct application has been reported yet. Currently, there are two thermoplastic resin systems advertised directly as IPNs. The first one is the Shell Kraton G® -based thermoplastic elastomer, where Kraton G® is blended with either nylon or polyesters. In the resulting morphology, one network is crosslinked by segments of glassy block copolymers and the other network by crystalline regions. Petrarch Systems is marketing the second system under the trade name Rimplast® , which is a combination of a silicone rubber and a semicrystalline nylon. A vinyl functional silicone reacted with a silicone carrying a reactive hydrogen forms the densely crosslinked silicone network within the nylon resin matrix. Nylon, however, is a strongly hygroscopic material which would rule it out for electronic packaging. Nylon 6/6 molding compound, for instance, can absorb moisture up to 8.5% of its weight. For resins reinforced with 30% to 33% of fillers, this amounts to approximately 6.5%. Dimensional stability and high risk of corrosion would be two of the major drawbacks associated with these systems. Suitable systems of epoxies and silicones, epoxies and polyurethanes, or polyurethanes and polyesters can, nevertheless, be envisioned to give desirable properties for packaging. Some advantages with using IPNs for encapsulation may include the following:

- *Minimum shrinkage* — The introduction of a second system into the network reduces the combined free volume of the system. Shrinkage of the plastic package would thus be minimized with a lower-volume loading of fillers.
- *Lower exotherm* — With a judicious selection of base ingredients, the polymerization exotherm can be tamed to a reasonable level. The heat generated from curing epoxies, for instance, can be channeled into the initiation and propagation of a second component, such as a vinyl system. Thus, the level of residual stresses imparted to the passivating layers and underlying circuitry would be reduced.
- *Improved barrier characteristics* — Chain entanglement holds the two networks closely together with some slight extent of interpenetration. For a given volume of material, a true IPN exhibits higher density than a normal blend. The reduced free volume translates into high barrier-resistance properties. Permeability and diffusion coefficients of a polyurethane/epoxy IPN has been reported to decrease by a factor of 3 and 7, respectively [302].
- *Thermal stability* — Combining a network of high glass-transition temperature with another of similar characteristics would lead to large thermal stability. Higher continuous-use temperatures would be possible. For instance, an IPN system of polyurethane/polyester exhibited a glass-transition temperature between 80°C to 94°C. This was significantly higher than the transition temperatures of the individual components, namely, 64°C for polyurethane and 75°C for polyester [303].
- *Good wetting* — Mixtures with low critical surface tensions are theoretically possible with the proper combination of materials. From a processing viewpoint, minima in-surface tension would guarantee good wetting of the chip, interconnecting wires, and wirebonds. This was found to be the case with several polyurethane/epoxy IPNs [294]. With the advancing contact-angle method, the critical surface tension of these materials can be determined. Compositions that yielded maxima in ultimate properties of the IPNs also produced minima in surface tension.

8.7.3 Direct Chip Attach

The best packaging of the future may be as few levels of packaging as possible for a given application. Why not eliminate all the expense associated with package assembly by directly mounting the chip on the board surface? Also known as chip-on-board, this method of bare chip attachment to a substrate

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can provide the smallest and cheapest package among various packaging technologies.

The TAB design gives the designer one approach to direct chip attach. Before bonding to the board surface, chips on tape can be electrically tested to assure reasonable yields after board assembly. Wirebonding provides another alternative whereby chips can be directly bonded to the board, thus, eliminating the complexities of another intermediate level. Since wirebonding is the cheapest chip-connection technique at low I/O (less than 200), this approach may be the cost-effective solution to packaging low-cost systems such as consumer electronics, typewriters, and printers. This approach, however, requires that chips can be backbonded to a thermally compatible board, eliminating the need for heat sinks. Similar arguments can also be made with solder connection of chip to board.

The main concern at this point will be the inherent TCE mismatch between the chip and the substrate. Better substrate materials will be needed to replace the conventional FR-4 glass fiber-reinforced epoxy boards. Cost, obviously, is a major factor that needs to be factored in. Currently, thermal mismatch can be alleviated to a certain extent by the use of ceramic substrates. Hybrid systems used in automobile electronics, for instance, use alumina-based ceramics as supporting carriers. Interconnections between the device and the board will also be another concern. Currently, bonding the chip to the board with organic adhesives filled with metal powder (*Ag* or *Al*) is the preferred method. High filler loading, however, is usually needed to provide good electrical contact and unimpeded thermal paths for heat dissipation. Future alternative materials for bonding can include, for instance, organometallic compounds and conductive polymers.

Boards, however inexpensive, will not be shipped with bare chips. Devices still need protection from process chemicals, dust and humidity. Liquid epoxy-chip encapsulants will be developed to protect chips directly mounted to printed circuit boards. Thus, the circle has completed a full turn, and we are back again to the "glob top" transistor design of the early 1960s.

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11

PACKAGE-TO-BOARD INTERCONNECTIONS

TIMOTHY C. REILEY
DA-YUAN SHIH

11.1 INTRODUCTION

One element of electronic packaging that influences the overall packaging strategy is the structure and the joining process used to interconnect packaged electronic devices to higher-level assemblies, e.g., boards, cards, or flexible substrates. The choice of interconnection is coupled to system reliability and performance requirements, and is an important factor in establishing the board configuration and certain materials choices. Indeed, the temperature cycle associated with the solder-joining or pin-brazing processes commonly fixes the minimum thermal stability standards for all the materials in the elements to be interconnected.

A major constraint on the interconnection technique is imposed by the need to replace upgraded, failed, or imperfect devices on the board. This re-

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quires for most assemblies a solder joint (see typical examples, Fig. 11-1) which is sufficiently impermanent to allow device replacement. This need for joint reworkability places reliability limits on the joint itself that may not exist for permanent or irreversible interconnections. The primary alternative to a soldered interconnection is a mechanical, pluggable pin interconnection, such as the one used in the IBM Corporation's machines to connect the liquid-cooled multichip module (LCM) to the board (see Fig. 11-2). This alternative is particularly attractive for field upgrading or pre-ship testing of these complex modules. For some card assemblies, particularly those for which assembly replacement rather than device replacement is most cost-effective, other alternatives to solder joints are available. These may include conductive adhesives or direct-chip-attach using wire bonding, both of which have some inherent limitations in reworkability. Another determining factor in the choice of package-to-board interconnection is the desired area density of packaged devices. As the board wiring density has increased to accommodate increased levels of device integration, the capacity for greater packaging density has also increased. This has provided the degree of freedom necessary for the introduction of Surface-Mount Technology (SMT) to replace such less area-efficient devices as Dual-In-Line-Packages (DIP) and other pin-though-hole packages; examples of PTH packages are compared in Table 8-1 on page 532 with those meant for surface mounting. For example, it is projected that for the integrated circuits used in the combined consumer and industrial electronics industry [1], the use of pinned packages will decrease from 86% to 66% and the use of SMT packages will increase from 14% to 34% of the total during the period 1985-1990. The consumer electronics industry is in the process of completing the transition to SMT (see Fig. 11-3 for detailed projections), given the need for miniaturization and cost reduction. Some

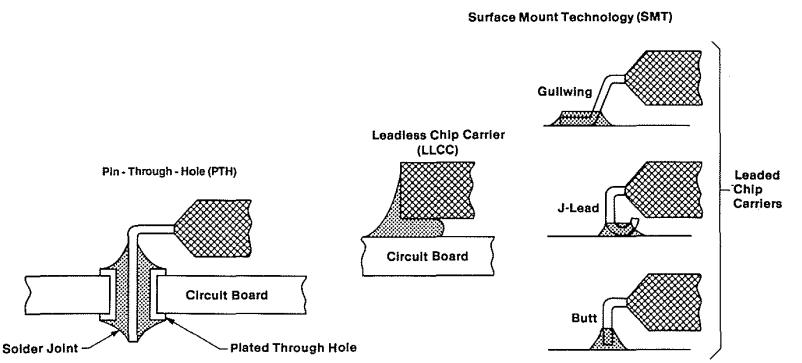


Figure 11-1. Pin-Through-Hole and Surface-Mount Technology (SMT).

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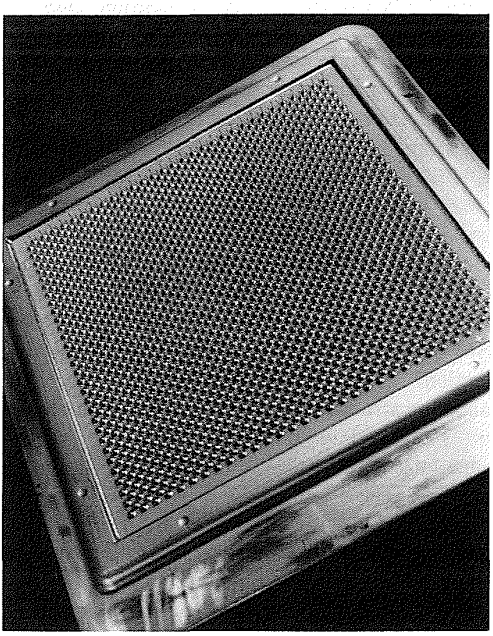


Figure 11-2. 1800 Brazed Pins. 1800 pins on 1.78 mm minimum spacing, brazed to a flanged ceramic module.

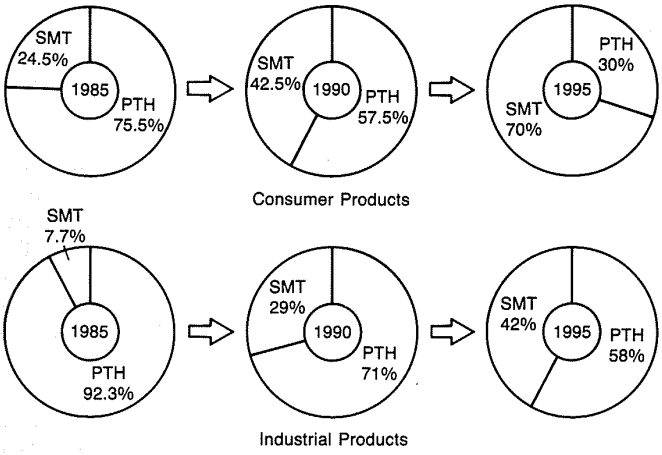


Figure 11-3. SMT Growth Projections. Courtesy of IBM, Inc., Tokyo, 1986.

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segments of the computer industry are currently in this transition. For the computer industry, high-density packaging options that reduce signal-propagation delay are desirable and are most often pursued at the expense of board complexity. This is so for the higher-performance machines; however, for lower-performance systems a moderate packaging density for VLSI components coupled with fewer board wiring planes may reduce overall system cost. Also for high-end computers, electrical and thermal performance dominate the package selection, which may be incompatible with packaging optimization based only on area density. In many cases SMT devices and pin-through-hole mount (PTH) devices must coexist on the same board. This impacts the joining process, since the chosen joining technique may be a compromise approach or a two-stage approach. This choice must be compatible with both PTH and SMT devices, rather than one that is optimized for a single form of interconnection.

In this chapter, interconnection structures representative of current and projected practices are given. The major emphasis is on pinned and surface-mounted device interconnections. Methods and material constraints for pin attachment are reviewed for pluggable and soldered packages. Solder-joint reliability issues are discussed, along with the fundamental mechanical behavior and underlying metallurgical or microstructural origins. The techniques for solder joining, such as vapor phase, wave solder, IR reflow, and others, along with the factors affecting applicability of a given technique to a given interconnection structure, are described. A brief overview of solders, solder pastes, and solderability, including flux selection criteria and wettability measurements, is provided. Examples of evolving interconnection concepts, such as conducting adhesive or pressure connections, are also given.

11.2 PINNED PACKAGES

The use of pins to provide interconnection between an electronic device and the next level package has, historically, been the most common form of interconnection. The configurations range from simple pinned resistors or other passive devices to the very high pin count, multichip modules used in large, mainframe computers. In this section some of the approaches for pin connections to the board or card are reviewed. Emphasis is given to packages for high-end computer applications, although other pinned packages are discussed. For the LCM, a closely spaced grid pattern of 1,800 input/output (I/O) pins are brazed onto a 90 x 90 mm module. These modules are directly plugged into the harcon springs on the board, thus forming a two-level planar package system with either the module or the board as the FRU.

Also considered in this section are pin attach processes, pin design, and choice of base metals and plating metallurgy of the pin to meet stringent electrical and mechanical requirements throughout product life. Electrical requirements include low ohmic contact resistance, current-carrying capabil-

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ity, nearly constant resistance in aggressive environments, and the capability for multiple insertion and withdrawal cycles. Mechanical requirements include braze joint strength, the ability of the pin-joint to withstand multiple chip reflow and pin-repair thermal cycles without degradation in strength, and the ability of the pins to accommodate the stresses generated by differential deformations between module and the card or board assemblies. Dimensional tolerance of the pin arrays, along with the alignment considerations between the first-level and second-level packages, is also included in the discussion. The factors that limit the use of pin-grid array packages, as both the pin count and module size continue to increase, and the developments in Zero-Insertion-Force (ZIF) connectors are discussed.

11.2.1 Packaging Design

As pointed out in earlier chapters, an increase in the level of circuit integration is accompanied by an increase in the number of I/O counts. This strongly influences the form of package-to-board interconnections. For pinned packages for VLSI devices two basic styles are used: peripheral and area arrays. The best-known example of the former style is the dual-in-line package, which has been the mainstay package for interconnecting small- and medium-scale integrated devices to the printed wiring board since the early 1960s. It serves primarily as a space transformer to fan out the denser chip I/O terminals to the less dense wiring pattern on the printed-circuit board. This configuration has leads on 2.54 mm (0.1 inch) centers and along two edges of the package, and is inserted into a socket or soldered into a matching grid of plated-through-holes on a printed-circuit board. DIPs are available having either plastic or ceramic bodies, which provide environmental protection for the chip. The plastic DIP is a low-cost package; however, it suffers from limitations in hermeticity and heat removal, as discussed in Chapter 8, "Plastic Packaging."

Alternatives to the DIP have been developed in recent years to accommodate the shortcomings of this package with respect to I/O count and electrical performance. Other peripherally pinned packages have been used, but, given the intrinsic inefficiency in board utilization associated with the 2.54 mm pin pitch, more space-efficient options are necessary, as illustrated in Figure 11-4. For pinned packages the primary alternative to the DIP is the Pin-Grid Array (PGA), which uses an area array pinning geometry. This higher-cost package offers improvement in virtually all areas of performance compared to the DIP. The PGA has been available for many years in ceramic form; several plastic PGA versions have now become available, as well. Packages are also available that have several peripheral rows of pins, thereby offering an intermediate structure between the DIP and PGA. Another important alternative to the either of these pinned packages, which is discussed at length in a later section, is the surface-mounted package. Although for

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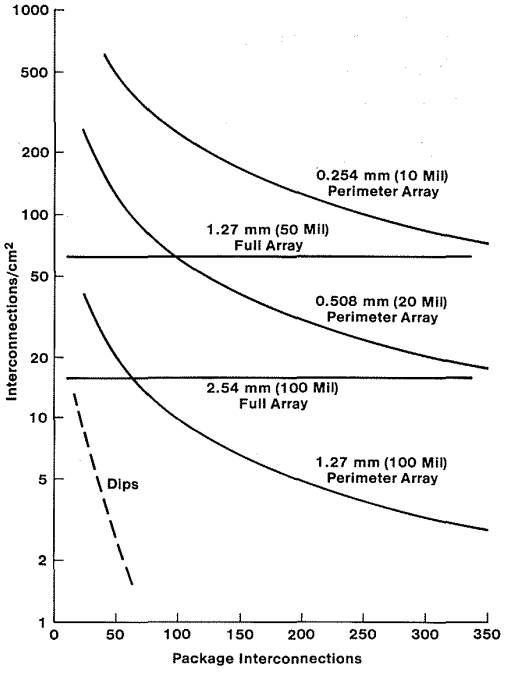


Figure 11-4. Area Density of Interconnections vs. Package Format.

SMT the package-to-board interconnection is made at the package perimeter, the finer lead pitch available and the increased wireability allowed by the surface contact only (not all the signal planes in the board must be contacted, as is normally the case with pinned packages) can allow a significant advantage in overall wireability and packaging density for single-chip packages [2]. The relative suitability of one package type or another is a highly application- or system-specific judgment, based on a wide range of performance, reliability, and cost issues, many of which are described in this and other chapters. One of the latest designs that uses pins at 1.27 mm spacing, and yet allows SMT-like connection densities on the board is illustrated in Figure 11-5, as practiced by Fujitsu in its 730 series. Butt soldering, as referred to in the industry, started with the need to surface attach DIPs by chopping the leads off the DIP. The process involves dipping the pin-grid array or DIP in solder paste and placing it on to pads on the printed-circuit board, thereby converting the pin-grid array into a surface-mounted device.

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A primary advantage is the increased density of connections onto a given circuit board, associated with surface mounting, plus compatibility with other surface mounting fabrication processing. Increased height, higher-lead inductance, and inability to inspect the joint are the major disadvantages. In spite of these, the technology is being applied by Northern Telecom and General Dynamics, in addition to Fujitsu and others [3].

The ceramic PGA was developed in the 1960s [4] to allow the efficient packaging of the area-array, flip-chip devices. It was originally designed as a single-chip carrier to function as a space transformer by fanning out the spatially dense set of area-array solder-bump terminals to a less dense matrix of pins. The pins are inserted through preformed holes in the substrate and are mechanically swaged in place [5]; see Chapter 7, "Ceramic Packaging." After package assembly the pins are then inserted into the matching grid of plated-through-holes on the printed-circuit card and wave soldered in place. The early chips using this package, the so-called Solid Logic Technology [6], were the first to use flip-chip connection with solder-coated copper balls; see Chapter 6, "Chip-to-Package Interconnections." The terminal I/O pads were 125 to 150 μm (5 to 6 mils) in diameter on 300 to 380 μm (12–15 mil) centers. Later, this technology was extended as the higher-density chips required more I/Os and greater wiring capabilities. To accommodate this growth, the copper ball was replaced with evaporated tin-lead C4s on a finer pitch. The reduced pitch required a change from the thick-film conductor processing on the ceramic to photolithographic processing. A 9 x 9 mm array of pins was initially attached to a 24-mm-square substrate. To meet the demand for more interconnections, the metallized ceramic (MC) technology was extended to 116 I/O pins for the 28-mm-square substrate and later to 196 pins for the 36-mm-square substrate [7]. The need for continued increase in both circuits and I/O terminals on the chip surpassed the capability for in-

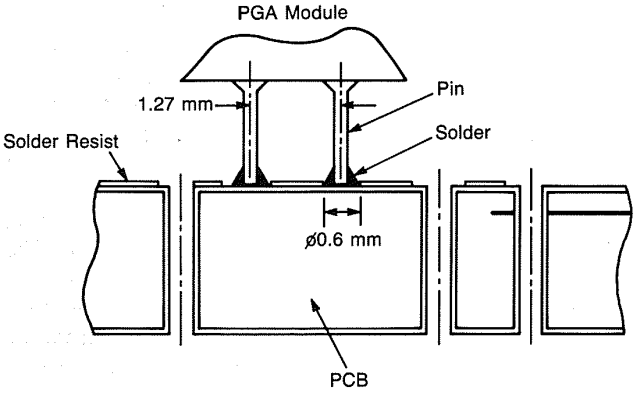


Figure 11-5. Butt Soldering of Pinned Module. (Fujitsu 730)

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terconnection on a single-conduction layer on the chip carrier. Also, for reasons of performance, cost, and reliability, the multilayer, multichip technology was developed. A major pinning change accompanied this technology. For the multichip module (MCM), the pins are attached by brazing rather than swaging. For the first generation of modules, these brazed pins are soldered to the board; for later, larger versions the pins are inserted into connectors. The pin-grid-array package has been the package of choice for all three technologies.

The multichip module [8], as shown in Figure 11-2, containing 33 conductor layers, can accommodate between 100 and 133 high-speed chips on a 90-mm-square area. On the bottom surface, 1,800 pins are brazed to a 2.5 mm staggered grid pattern. Because a considerable amount of chip-to-chip communication occurs within the multichip module, the number of pins is well below that number of I/O that would be extrapolated for the number of circuits contained in all the chips. This effective reduction in I/O scales as the size of the substrate and hence the level of circuit and chip count increases. For example, the ratio of module I/O pins to total number of chip-to-substrate interconnections has been reduced from about 1:3 (361 pins:1,080 chip terminals) for the 50 mm multichip module MCM module to approximately 1:8 (1,800 pins:15,000 chip terminals) for the 90 mm multichip module.

Pin grids on the 50 mm module (shown in Fig. 11-6) and on the smaller substrates are typically on 2.54 x 2.54-mm-square grids, matching the industry standard for mounting of pinned packages, including DIPs, on printed-circuit boards. The diameter of the screened Bottom Surface Metallurgy (BSM) pads to which the pins are brazed is 2.08 mm (82 mils); this allows enough wetting area to accommodate an adequate filleting around a 0.97 mm (38 mils) diameter pin head [9], given manufacturing tolerances. The I/O pin density has been doubled on the MCM module design by accommodating an additional pin at each interstitial site of the 2.5-mm-square grid pattern, thus forming a so-called staggered grid, which becomes, effectively, a 1.8 mm (71 mil) grid. To accommodate the density increase, the pad diameter is reduced to 1.52 mm (60 mils) and is coupled with a smaller pin head 0.80 mm (32 mils) design. The shortest distance between any two pads is now reduced to 0.254 mm (10 mils) from 0.48 mm (18 mils), still sufficient to meet the insulation requirement as well as manufacturing tolerances.

Mechanically swaged pins (see Fig. 11-7), on the same grid, 1.78 mm, have been successfully pinned, and 1.27 mm (50-mil) grids are projected. The limiting factors that become important as the distance between the holes is decreased are the strength of the substrate and the minimum hole diameter. Although substrates up to 36 mm square have been successfully pinned, the accuracy of hole location, substrate flatness, and thickness uniformity are is-

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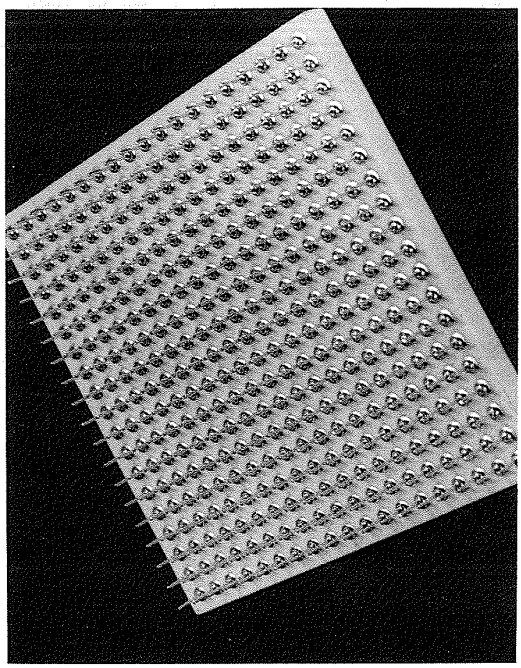


Figure 11-6. Pins Brazed to 50 mm Pin-Grid Array MLC Modules. Back side of a multichip, multilayer ceramic module, having 361 pins on 2.54 mm centers.

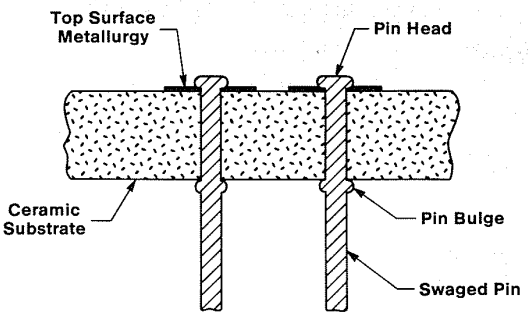


Figure 11-7. I/O Pins Attached to a Ceramic Substrate. Pins formed into pre-holed, prefired ceramic substrates, for the IBM MC and MCP pin-grid arrays. After Larnerd and Darrow, Ref. [5], ©1985, IEEE.

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sues to be resolved before a larger substrate with swaged pins can be manufactured.

In the approach taken for MCM, the chip and the area array of pins are mounted on the opposite sides of the substrate forming the "cavity-up" configuration as shown in Figure 7-18 on page 477 of Chapter 7, "Ceramic Packaging." Other commercialized packaging approaches, in which the chip is wirebonded to the PGA, use both cavity-up and cavity-down designs (see Fig. 11-8). The latter has two or more concentric rows of pins with the center location being free of pins to make room for the chip attachment, as shown. The cavity-up configuration permits the use of a full matrix of pin arrays. The cavity-up design, when combined with the back-bonding approach widely used in the industry, possesses a major drawback by not allowing heat sinking of the substrate when high heat dissipation is needed [10]. It is for this reason that even though the cavity-down configuration does not permit a full grid and presents some bonding difficulties, it is favored by the industry for chips that need high heat dissipation. Most common is the placement of the die cavity and I/O pins on the same side, with an optional heat sink attached on the opposite side.

In the module card assembly, when the module pins are inserted into plated-through-holes and attached by wave soldering (see Fig. 11-9 for joint cross section), both the pins and pin joints can experience high stresses arising

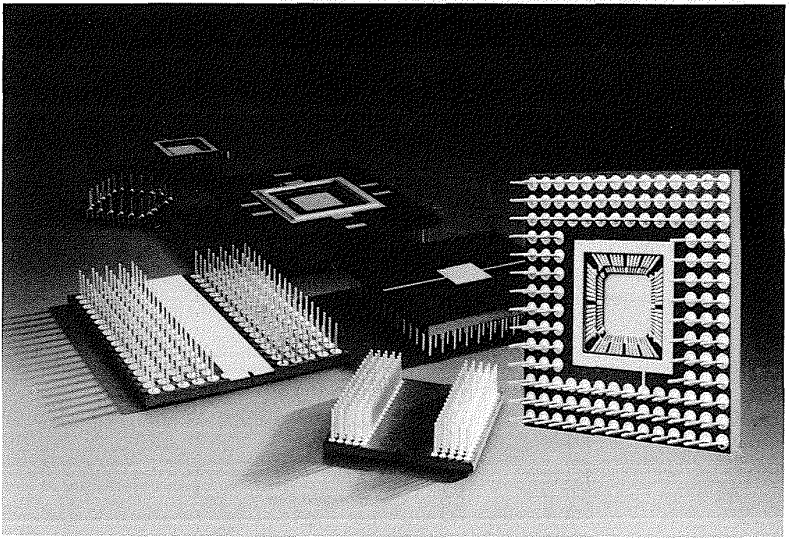


Figure 11-8. Cavity-Up and Cavity-Down PGA Configurations. Typical, commercially available ceramic pin-grid arrays, showing both cavity-up and cavity-down version. Photo courtesy of General Electric Co., Ceramics Division.

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from differential thermal expansion between the two levels of packaging. The differences in expansion can be caused by either thermal-expansion mismatch between the ceramic module (TCE ~ $60x10^{-7}/°C$) and the epoxy-glass board (TCE ~ $150x10^{-7}/°C$) during cooling from the soldering temperature or by the thermal stresses generated during power-on and power-off cycles. The former was observed and modeled after wave soldering the modules on to the board; all pins were found to experience bending moments and axial forces [11]. The bending moment decreases slowly from the outermost row to the center of the module; and the axial loads are compressive for all pins other than those in the outermost row, which are tensile. The largest tensile force is present at the corner pins where the distance from the neutral point is greatest. The tensile stresses due to TCE mismatch scale with module size. The corner pins on the large module are found, in this study, to be severely deformed after the wave-soldering and cooling cycle. A ceramic module greater than 50 mm in size presents a serious reliability concern, if the pins are to be soldered into plated-through holes. (Alternatives to the relatively rigid pins for interconnections described here are shown in the next section of the chapter; these include solder posts or elongated pillars). A pluggable module was therefore required for the replacement of modules on the card or planar board without reflowing solder [12]. Instead of soldering the pins into the plated-through-holes, the area array of pins is plugged into a matching

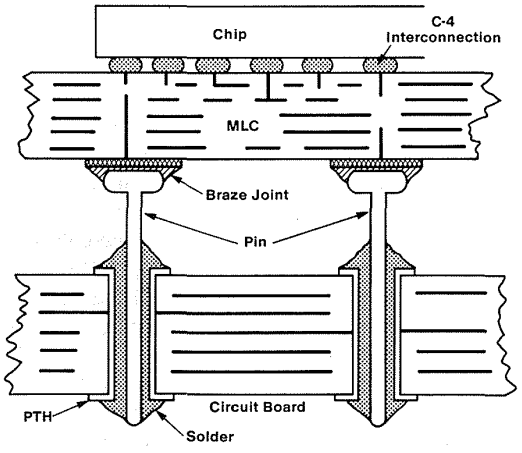


Figure 11-9. Module Brazed Pins Soldered into Printed-Circuit Board. Schematic cross section, showing a chip C4-mounted to an MLC module, having brazed pins which are soldered into a multilayer printed-circuit board. The actual cross section shows a *Ni/Au* plated, Kovar pin brazed to the ceramic with *Au–Sn* braze, and soldered to the board.

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array of spring connectors, whose tails are soldered into plated-through-holes. Since the module and board are processed separately, the thermal-expansion mismatch problem during wave soldering is eliminated. This structure and its fabrication are described in the next section.

The structure of the plastic PGA assembly, which is currently receiving considerable attention, is similar to its ceramic equivalent. Instead of alumina or other types of ceramic material, low cost FR-4 or G-10 epoxy-glass materials (see Chapter 12, "Printed-Circuit Board Packaging") are used for the low-temperature plastic PGA applications, while polyimide-glass materials are used for high-temperature performance. The fabrication of the plastic PGA packages shares most of the same assembly processes and techniques with the circuit board manufacturing process [13, 14]. After lamination, the holes for the pins and shorting bars are drilled, and the pins can be either pressfit or reflow-soldered into the plated-through-holes, similar to the swaged-pin approach discussed earlier in the chapter. The advantages of the plastic PGA are low cost, as well as better electrical performance. The use of the less expensive epoxy-glass laminates offers the cost advantage, while the low dielectric constant epoxy coupled with the high electrical-conductivity copper offers higher electrical performance over the ceramic PGA. Despite the low cost and better electrical performance issues, reliability and nonhermeticity are major concerns in the plastic PGA applications. Thermal management, as well, in the plastic PGAs is more difficult than in the ceramic equivalent, given the lower thermal conductivity of the organic dielectrics.

11.2.2 Connector System Design

For a pinned package the pins provide mechanical support and electrical connections for power and signals between board and module. In the case where pins are inserted and wave soldered into the plated-through-holes, electrical conduction is achieved through an intermediate solder layer joining the pins to the board. Although the soldered pin joint, which is widely used in the industry, has achieved a high level of reliability, its implementation, when coupled with ceramic modules, is restricted by differential module/board thermal expansion. A pluggable interconnection has been used to overcome this limitation. Furthermore, since the connector can provide increased compliance to accommodate slightly bent pins and other dimensional tolerances during insertion, the pluggable connector design relaxes other design constraints [15]. When the pins are engaged into the spring contact area, stresses generated from the power-on and power-off cycles during machine operation or due to any differential deformations between the two packaging levels are also absorbed by the flexible tails of the spring. The result is that the MCM module size can be greatly extended. Another considerable advantage of a pluggable module is the ability to replace, customize, or upgrade a module within a computer with minimal impact on the overall

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machine hardware or operation. The pluggable design also facilitates computer-failure diagnosis and repair at the final assembly stage of module manufacturing or during field service. The field maintenance strategy has, therefore, evolved from the replacement of the card or board to the use of the pluggable MCM module as the FRU.

As with other types of separable connectors, the pluggable connector, described here, requires a pressure contact together with a suitable wiping action at the mating interface between the pin and the spring connector to provide acceptable electrical contact. The contact resistance must be held at a low and very constant value. Even though the module ages and may be repeatedly removed and replaced, the maximum tolerable change in contact resistance may be specified, for some applications, as low as a few milliohms. Also, since a large number of pins are simultaneously engaged into the mating connectors, the actuation force per pin must be kept at the minimum level. This requires minimal frictional forces. The optimization of the pluggable connector design requires a low and stable contact resistance, good wear resistance, and low friction coefficient. All these necessary properties are achieved with the contact structures and materials described in subsequent paragraphs.

Figure 11-10 illustrates the bifurcated connector design now in extensive use. Each of the dual contacts, when mated with a module pin, is capable of providing the necessary electrical connection. This configuration provides a redundant path for each electrical connection such that system failure will not result from the failure of any single contact. Because the primary requirement is to have each spring in the connector array capture its mating pin on every insertion operation, the split design also provides adequate guiding action, which permits a lateral tolerance mismatch of about 0.4 mm; that is, the pin can be captured by the spring as long as the pin center is no more than 0.2 mm from the spring centerline [15]. Misalignment within this limit is compensated by the flexible tail on the spring as well as by the open flare design of the spring entrance ramp area. In the actuation direction, the tolerance constraints are that the pin must drive all the way through the lead-in area of the spring and wipe some distance along the ridges but must not travel all the way through to strike the back of the housing. Failure to satisfy the former criterion will cause unstable contact resistance, while failure to achieve the latter will result in excessive force applied, leading to permanent deformation in both pin and housing. The tolerance limit in the actuation direction is about 0.4 mm wide. A plastic housing is used to provide mechanical protection for the array of springs, to restrict the motion of the springs, and to insulate them, electrically, from one another. The housing must also be strong enough to support the high loading force, 1,000 to 2,000 N for the 1,800 pins, during pin actuation.

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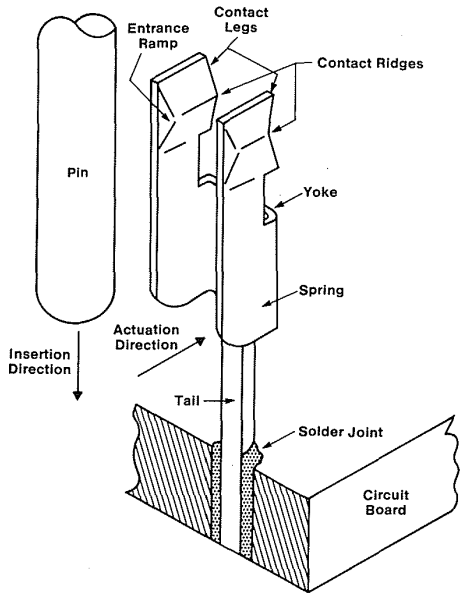


Figure 11-10. Bifurcated, Mechanical Pin Connector. After Babuka et al., Ref. [15], 1982.

The major engagement steps of module to board are illustrated in Figure 11-11. The module is inserted into the board site along the Z-axis, then is actuated along the X-axis. Both rough and precision-guide pin holes assure accurate Z-plane alignment of the mating arrays without contact between pins and springs. After insertion and before actuation, each pin is positioned beside its mating spring, facing the entrance opening. An actuation tool then drives the pins into the springs.

One of the connector members must be compliant. For the approach described here, the contact spring is designed to provide the flexibility, given the relative rigidity of the module pins. The base metal of the spring is formed with a precipitation-hardened, beryllium copper alloy, which is sufficiently strong to prevent any permanent set due to pin insertion, and sufficiently compliant to accommodate the deflections. The pins are made of Kovar, an alloy of iron, nickel, and cobalt. The primary reason for the choice of Kovar alloy is that it provides a close match in thermal coefficient expansion with the alumina substrate to which it is brazed. This serves to reduce the stresses in

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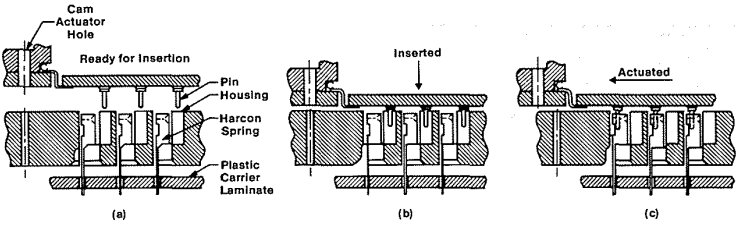


Figure 11-11. Pin Insertion and Actuation. After Seraphim, Ref. [16], 1982.

the braze joint during changes in temperature. The Kovar alloy also has high enough modulus and yield strength to ensure that elastic deflection and permanent set will be small during actuation.

The plating metallurgy on the connector surface is also of primary importance. It should serve the purpose of providing a wettable surface for subsequent soldering or pin brazing on one end of the connector. And when the other end is in pressure contact, it must provide the ability to withstand corrosion and contact wear. This is necessary at the initial insertion as well as after repeated insertion and withdrawal operations, while still maintaining a low, stable contact resistance. To meet both of these goals, the pin is first electroplated with a palladium layer. This provides resistance to corrosion [17, 18] and also the hard surface required to prevent mechanical wear-through of the finish during the repeated plug-in. Palladium also has high electrical conductivity, which allows the contact resistance to remain low and stable. A protective, surface layer of electroplated gold is applied. The gold surface resists organic contamination and surface oxidation, and enhances braze wettability. The thin gold layer over the palladium actually acts as a lubricant between the contact members in maintaining a low-friction condition. However, an upper limit must be set on the gold thickness, because the actuation force rises sharply with increasing gold thickness on the pin [15, 17].

For the bifurcated spring connectors, a layer of sulphamate nickel is first electroplated over the rough, mechanically formed surface. Then the connectors are electroplated with palladium to provide corrosion and wear resistance, followed by gold plating to provide a low-resistivity surface and also for good wettability for soldering into the plated-through-holes.

A metallic surface, when exposed to the atmosphere, is covered with several atomic layers of adsorbed gases, and possibly with a thin tarnish layer formed by chemical reactions of the surface with the atmosphere. As a consequence the electrical resistance of the contact consists of the sum of a con-

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striction resistance associated with the actual contact area, the resistance of the contaminating film, and the bulk resistance of the contact member itself [19]. The successful use of the contacts depends on the rupture of these tarnish films so that clean, metal-to-metal contact occurs. The contact force, mechanical slide, or wipe and lubricant are all factors ensuring an intimate contact between members.

Achieving the desired contact resistance in a low-force electrical connector depends, therefore, on supplying sufficient load or load concentrations to break down, mechanically, the tarnish films. The sliding movement of one contact member against its mate is also necessary to ensure efficient removal of debris and foreign particles from the contact interface. Therefore, the requirement for high contact force and wipe action results in the need for very high engagement forces when many connectors must be actuated simultaneously in a single operation. Two factors tend to reduce the actual engagement forces required. First, in practice, lubricants or protectants are often used. They can minimize contact wear by reducing the frictional force between mating members. (This also limits wear and reduces the concern that the less-noble base metal will be exposed and corroded [18]). Second, since the housing may deflect during actuation, only a fraction of the pins are actually seated simultaneously. Therefore, the total actuation force is considerably less than the multiplication of total number of pins by the peak force generated by a single pin entering the spring.

As the module size continues to grow improved connectors are required to optimize the contact geometry and surface metallurgy, and to reduce the contact forces. An example of an advanced connector approach is the Zero-Insertion-Force (ZIF) connector, which appears to be a viable solution to this concern. With an ideal ZIF connector design, insertion becomes a two-step process. First, pins are brought into mating position and seated without requiring force. Second, a cam is actuated to apply the required contact force. Removal is performed in the reverse order. A major advantage of ZIF is that there is no force-imposed limit to the number of contacts in the connector. The camming action is shown in Figure 11-12. Other approaches to development of ZIF connector with high I/O pin count include the use of shape memory alloys [21]; and the use of low-temperature-melting *In*–48%*Sn* solder as the connector media [22]. The latter approach eliminates the need for contact force or wiping action between the contact members.

11.2.3 Pin Joint Mechanical Design

The mechanical integrity of the pin system is of primary importance to the overall package reliability for multichip modules. The enormous number of pins involved aggravate the risk of failure. For the optimum mechanical design the factors that influence the strength of the pin and braze joint, and the relationship between loading force and the stress distribution have been stu-

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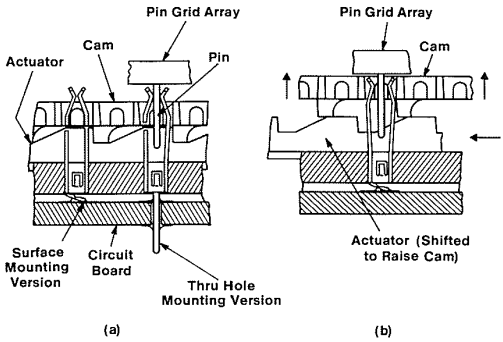


Figure 11-12. Actuation of a Zero-Insertion-Force (ZIF) Connector. The horizontal motion of the actuator drives the cam vertically, which opens the connector. (a) Pins engaged by the connector housing. (b) Pins free to be inserted or withdrawn. After Waltersdorf, Ref. [20], ©1983 by IEEE.

died and reviewed in detail [9, 11]. It has been shown that the strength of the braze joint is determined by the mechanical properties of the filler metal, fillet morphology, pin head diameter, shape, and thickness. For the case where the substrate has rather good mechanical strength, such as for an alumina substrate, the use of a pin head with a relatively high degree of fillet accumulation around the pinhead periphery demonstrated the highest strength. However, the same joint configuration, when applied to a weaker ceramic substrate, results in irreparable ceramic fracture at relatively low externally applied force. Further studies, involving finite element analysis, indicate that the high residual stresses generated in the ceramic after solidification of the molten braze alloy are critically dependent upon the thickness of the fillet, TCE mismatch between the filler metal and the substrate, and the mechanical properties of the filler metal. The use of a hard filler metal, thick fillet, or a filler metal which has a large thermal expansion mismatch with the substrate all cause the residual stresses generated in the ceramic during brazing to increase. To minimize the stresses in the ceramic new joint designs have been examined, which include the use of a large-head pin with head diameter matching that of the metallized pad, along with a thin fillet sandwiched between them [23] (see Fig. 11-13), or a modified pin head geometry that significantly reduces the braze accumulation around the pin head periphery. Both designs have been shown to reduce the braze stresses significantly.

To provide an additional safety factor, the pin is designed to yield before excessive force can be transmitted to the braze joint and/or ceramic substrate.

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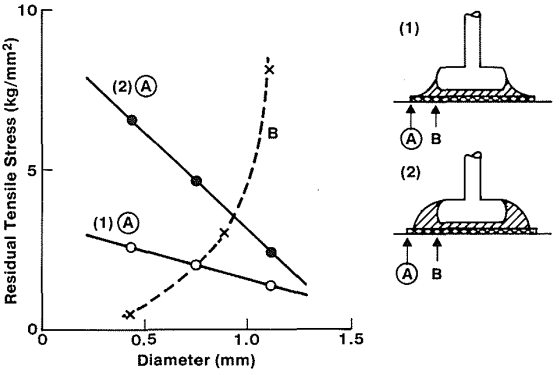


Figure 11-13. Stresses in Brazed Pin Joints. Measured residual stresses in an eutectic *A–Cu* brazed pin joint, as a function of pin head diameter. In the idealized case minimum stresses are found when the pin head diameter matches that of the metallized footprint, and when the braze volume is minimized. After Sahara et al., Ref. [23], © 1982 by IEEE.

However, a threshold pin stiffness is also required to withstand normal handling or actuation forces, without the pin being permanently deformed. In testing and evaluating these various designs, angled pin pull testing, which simulates both the bending and tensile forces from pin loading, is most commonly used, along with the shock and vibration, bending, flexing, and multiple insertion/extraction tests, and others. A rule of thumb is that the strength of the braze joint should be stronger than the pin shank to avert fracturing during handling, bending, or straightening, and that the combined stresses from braze and pin loading should not exceed the fracture strength of the ceramic substrate (to avert irreparable damage). Moreover, the pin base metal should be selected with a thermal coefficient of expansion matching that of the substrate to further reduce the braze stresses. These design criteria have been successfully implemented on the pin-connector system widely used on various multichip modules with dimensions ranging from 35 to 127 mm. For example, the braze joint formed with eutectic *Au–Sn* alloy is stronger than the pin shank, which is made from Kovar, having a yield strength of 480 MPa (70 ksi) and an ultimate tensile strength of 620 MPa (90 ksi).

11.2.4 Metallurgy of Brazed Pin Joint

In Figure 11-14, the cross-sectional view of an array of pins brazed to the bottom surface of a MLC substrate is shown. The pin joint is formed using eutectic gold–tin alloy as the filler metal. When melted at a temperature

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above 280°C, the alloy wets well to both pins and terminal pads. A braze fillet with a controlled morphology (shown at higher magnification in Fig. 11-15) is formed around the pin head. The selection of eutectic gold-tin alloy as the brazing filler material is based on its metallurgical compatibility with the plated layers on both the pins and the pads, the narrow melting range (which greatly reduces the susceptibility to cold joint problems), and the ability of the braze joint to withstand the thermal, mechanical, and reliability requirements for the module and for the module-board interconnection.

In the *Au–Sn* phase diagram, there are four intermediate phases: $AuSn_4$, $AuSn_2$, *AuSn*, and the gold-rich, ζ phase, shown in Figure 11-16. At the eutectic composition of *Au*-20 wt.% *Sn*, congruent melting occurs at 280°C, where a single liquid phase is converted, upon cooling, into two solid phases. Figure 11-17 shows a brazed joint cross section, viewed in the scanning electron microscope (back-scattered mode) and in the X-ray Microprobe, tuned to the presence of *Sn*. In the SEM photograph the gray phase is the *AuSn* intermetallic compound, while the bright continuous matrix is the ζ phase. To enhance braze wettability, the cofired molybdenum pad to which the pin is brazed is first plated with a few microns of electroless nickel, heat-

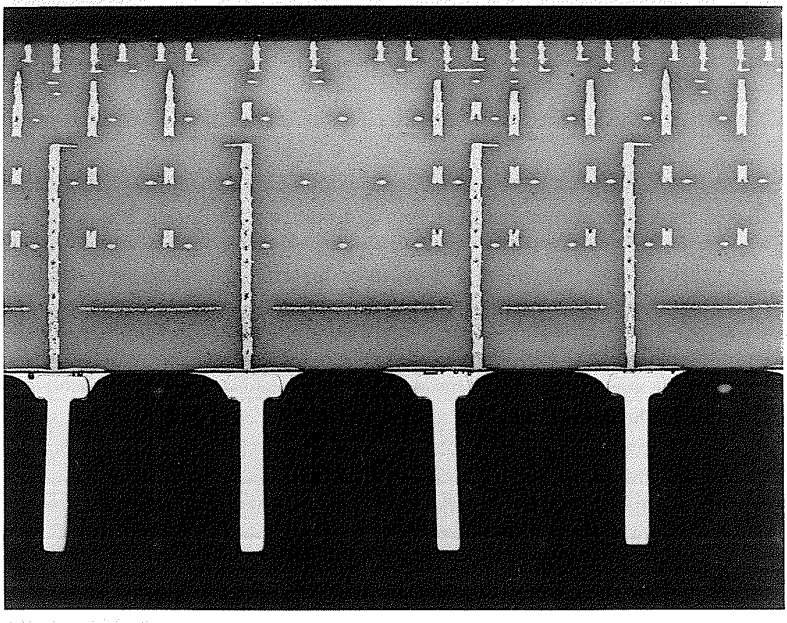


Figure 11-14. Cross Section of Pins Brazed to MLC Module.

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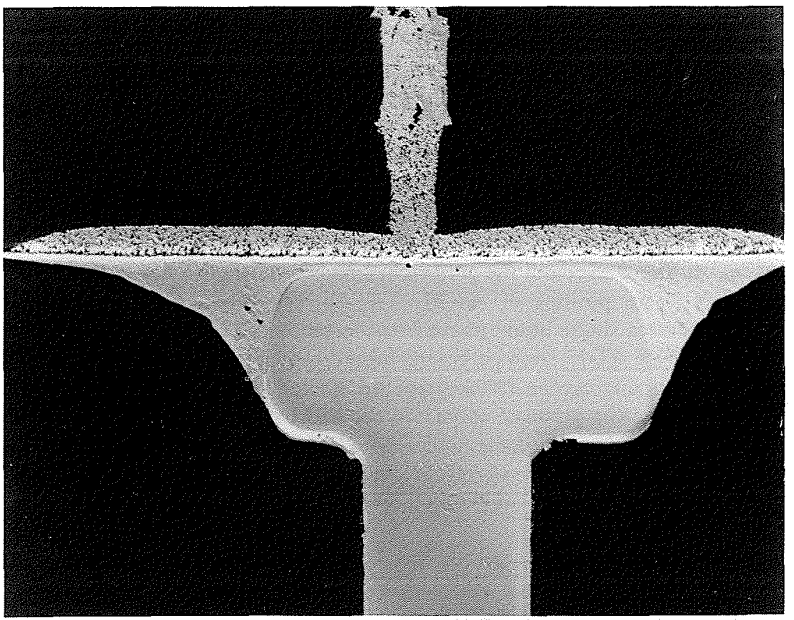


Figure 11-15. Cross Section of Brazed Pin Joint.

treated in a diffusion furnace to promote molybdenum-nickel bonding, then followed by a thin immersion gold plating to prevent oxidation of the nickel. Two versions of the pin-plating metallurgies are chosen for the soldered and the pluggable pins, respectively. Pins to be inserted and wave soldered into plated-through-holes are plated with nickel and gold in a relatively standard procedure. The preparation of the pluggable pin is somewhat more involved. The pin is plated first with a layer of palladium. This provides corrosion resistance, high surface hardness (to ensure a favorably low mating force when inserted into the harcon springs), plus a low contact resistance. At this point the pins are annealed in nitrogen to promote adhesion of the plating. During diffusion treatment, the iron, which is the major constituent of the base-metal Kovar alloy, diffuses into the palladium more rapidly than the nickel or cobalt, producing an iron–palladium interdiffusion zone of about 1 μm. Although this zone enhances braze wettability and therefore increases the joint strength, its thickness must be limited to prevent iron out diffusion to the plating surface. The existence of even small amounts of iron at the contact

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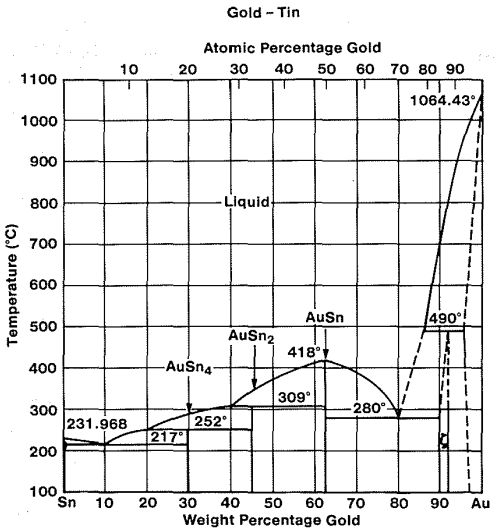


Figure 11-16. Phase Diagram — Gold–Tin. From the Metals Handbook, Vol. 8 [24], 1973 — with permission.

surface represents a potential contact resistance failure. The final plating consists of electrodeposited gold. The gold surface protects the underlayer from environmental attack, provides a wettable surface, and controls the height of the braze fillet.

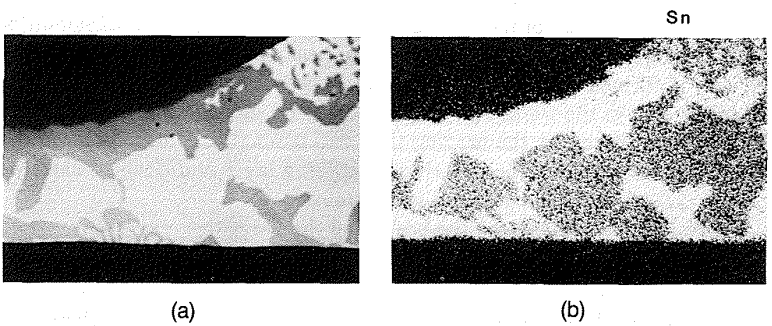


Figure 11-17. Metallurgical Cross Section of Brazed Joint. (a) Image taken in the SEM using backscattered electrons. (b) Microprobe X-ray image, keyed for *Sn*.

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To enhance the braze wettability further, the eutectic *Au–Sn* powders are uniformly mixed with about 1% of abietic acid, which serves as both binder and flux. The paste is then screened through a metal mask onto the plated I/O pads. The amount of braze material used at each joint is fixed by mask thickness and hole diameter. In this process pins are loaded in to the support plate of a graphite fixture, which has a matched coefficient of expansion to that of the alumina substrate. The same type material is used for the substrate holder. Alignment of pins to the substrate pads is achieved through locating holes in the fixture. After the module, pins, and fixture are assembled, the assembly is sent through a resistance-heated conveyor-type-belt furnace in a controlled forming gas ($N_2 - H_2$) environment. The reducing atmosphere protects the component from oxidation during brazing and reduces any oxide to restore a clean surface condition. The use of flux in the paste, which wets and breaks up any remaining oxide films, ensures good wetting and spreading characteristics. Filling of the pin joint begins when the paste starts to melt, as the fixture is slowly transported through the furnace. The molten braze then displaces the flux, completely dissolves the gold platings from the pins and the pads, and starts to react with the underplate. The dissolution of nickel or palladium into the molten braze is observed to be the driving force for the wetting and spreading action of the braze. Although dissolution of the gold plating is almost instantaneous, the dissolution of nickel plating is much slower. In the case of nickel plating on the pads or on the MCM pins, nickel first dissolves and is preferentially incorporated into the tin-rich, *AuSn* intermetallic phase. The molten braze continues to dissolve the nickel plating while the furnace is cooling. This dissolution rate decreases as the braze approaches the saturation level of the dissolving metal. When equilibrium is reached, a thin layer of nickel–tin intermetallic layer (Ni_3Sn_4) starts to precipitate at the liquid–metal interface and the pin-joining process is complete. However, for the condition where the braze alloy is held over the liquidus temperature for too long a time, complete dissolution of nickel plating will occur. Since braze wets poorly on molybdenum, the depletion of nickel plating results in poor braze-to-pad adhesion, and consequently, a weak pin joint is formed. This joint would not only fail to meet the strength requirement but, in the worst case, could escape the screening test, resulting in field failure. Therefore, the brazing time and temperature must be carefully controlled to ensure that the pad always retains a layer of unreacted nickel in order to maintain consistent braze-joint strength.

The interaction between the braze and the pluggable, palladium-plated pins is somewhat different. Palladium dissolves into the molten braze more rapidly than nickel, although both elements are preferentially incorporated into the *AuSn* intermetallic phase. Complete dissolution of the palladium plating occurs at the pin head periphery, where a high volume of braze accumulation prevents the saturation of braze with the dissolving metal. The

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braze then reacts and bonds directly to the palladium–iron diffusion zone. At this point, the dissolution rate is significantly reduced, and a strong metallurgical bond is formed. In the area where thin braze is formed (beneath the pin head), as soon as the gold plating has dissolved, the thin braze fillet begins to react with palladium. Because of the low fillet volume, equilibrium is easily established when the molten braze is saturated with the dissolved palladium metal. During continued contact, a *Pd–Sn* intermetallic phase starts to precipitate at the liquid–metal interface, and the joint is formed. Control of the palladium plating thickness has proven to be critical. Because complete separation can occur between the *Pd–Sn* intermetallic compound layer and the unreacted remaining palladium plating, the palladium plating thickness must be limited. Also, during the advancement of the braze melt toward pin shank, the leading edge of the melt becomes increasingly gold-rich after dissolving all the gold plating. Increasing the gold content of the alloy to the hypo-eutectic composition greatly increases the liquidus temperature of the melt. Thus the advance of the braze melt is self-limiting, thereby helping to control the morphology of the joint fillet.

In selecting the eutectic *Au–Sn* alloy as the filler metal, the major concern is its low melting temperature, which is significantly below the chip reflow temperature of 350°C. Therefore, each time the module is reflowed, the braze joint experiences partial melting, resulting in pin movement and the tendency of the fillet to creep away from the initial joint, with an attendant loss of strength and side support of the pins. The liquid also reacts vigorously with the surrounding metallurgies to form many intermetallic compounds, which grow and become more highly stressful and brittle with each reflow. To prevent pin movement, the substrate and pins are held in a fixture during each of the module reflow operations. This is clearly not a fundamental solution to the problem. An improved solution would allow the pin joint to remain undisturbed, and, more importantly, not allow metallurgical degradation during the repeated reflows. To achieve the desired stability and strength, while still being able to use the same basic *Au–Sn* alloy, the existence of the liquid phase at reflow temperature must be minimized or eliminated such that only sluggish, solid-state reactions occur. This can be achieved either by adding Group 1B metals such as gold and copper into the binary alloy, which increases the amount of the high melting point ζ phase of the alloy [25, 26], or by using nickel or palladium platings on the pins or the substrate pads to draw tin out of the melt. This latter approach minimizes the amount of the low-melting-point, tin-rich phase of the alloy [27]. In both cases, the melting point of the modified braze alloy is raised above the chip reflow temperature, and the joint becomes capable of withstanding repeated reheating cycles without degradation.

As an alternate approach, pins can be brazed with the high-melting-point, silver-containing brazing alloy such as the eutectic, copper–silver alloy

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[28], which melts at 779°C, or an indium–copper–silver ternary alloy [29], both of which are widely used in the brazing industry. However, a major concern with using a silver alloy as the joint material is the potential seriousness of electrical insulation breakdown due to silver migration between adjacent joints. It has been shown that, upon exposure to elevated humidity, joints maintained under a DC bias may develop silver filament growth, resulting in shortcircuiting. Many of the previous issues associated with the choice of braze and pin materials are summarized in Table 11-1.

As a projection of the shift from current pin interconnection practices, particularly for the low end, the following connector developments are expected:

1. SMT connectors replacing pinned connector sockets expected by 1990.
2. ZIF connectors to handle up to 2000 pins, compared to about 200 currently.
3. Optical connectors for system-to-sytem communications.
4. Card-edge connectors surface mounted in excess of 96 contacts.

11.3 SURFACE-MOUNTED PACKAGES

Table 11-1. Pin and Pin Joint Considerations.

PIN MATERIAL	PIN BRAZE
Coefficient of expansion; matched to substrate modulus, yield strength, ductility	Melting temperature; higher than subsequent processing temperatures
Plateability	Stable melting T; little change after joining or postprocessing
PIN PLATING	Narrow melting range (e.g. at eutectic comp.)
Corrosion resistance	Wettability; complex optimization of surface energies, viscosity, oxid. resistance, flux, fillers, atmosphere, etc.
Wettability by braze alloy/solder	Stable, controllable reaction layer at joint interfaces
Coefficient of friction, wear resistance	Coefficient of expansion; matched to substrate
Hardness, ductility	
Low, stable contact resistance	
PIN AND PIN-JOINT DESIGN	OTHER ISSUES
Pin strength; pin breaks before joint	Rework (both pin braze and solder joint)
Joint strength; joint breaks before ceramic	Degree of process control, reproducibility
Pin and pin joint designed for minimal residual stress in ceramic	Long term corrosion, migration
High pin density	

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11.3.1 SMT Structures

Surface-Mount Technology (SMT) provides a wide range of alternatives to pinned packages. The significant driving force for the use of SMT is the reduced package size and cost, and improved board utilization as the package-to-board interconnection spacing changes from 2.54 mm to 1.27 mm or below. For example, for certain consumer electronics applications a component density on the circuit board of nearly ten components per cm^2 per side has been achieved. The most common forms of SMT packages are shown in Figure 8-1, along with generally accepted acronyms and applications. See [30] for the evolution of SMT packages, which were first introduced in the mid-1960s. They may be divided into two primary categories for purposes of evaluating joint behavior and reliability: (1) leadless devices, which include leadless chip carriers (LLCC), surface-mounted arrays, and passive devices such as chip capacitors, inductors, and resistors, and (2) leaded chip carriers, which includes a long list of packages for active devices, distinguished mostly by material (plastic or ceramic) or lead configuration ("J-Lead" "gullwing," or butt joint); see Figure 11-1. Another, similar form of leaded packaging, Tape Automated Bonding (TAB), is covered in detail in Chapter 6, "Chip-to-Package Interconnections." In the first category, LLCC, the package-to-board interconnection consists of a solder bridge between metallized areas on package and board. The solder geometry is defined by the package placement, the solder volume, and the solder wetting and flow processes during joining. For the second category, leaded chip carriers, the term SOIC (Small Outline Integrated Circuit) is used as a general referent. These contain metal leads extending from the package body to small solder pads on the circuit board. In both cases the surface solder joint provides the electrical and mechanical connection between package and board. While surface-mount technology is expected to grow significantly, as shown in Figure 11-3 for 1986 and 1990 (based on the data for low-end commercial and industrial packages), through-hole components will continue to play a key role well into 1990s, both for active and passive components.

The major distinction between the two categories is the elastic compliance of the elements interconnecting the relatively rigid package body and circuit board. This becomes important as the devices are thermally cycled during operation, given the differences in thermal expansion for the materials of package and board, and given the differences in temperature (both transient and steady state) between package and board. Numerous analyses and reviews have been published regarding thermal-cycle-induced fatigue failure of SMT joints, examples of which are shown in Figure 11-18. In this section, these studies are used to describe the problem and methodologies for evaluating both LLCC and SOIC interconnections. Several other solder interconnection concepts for SMT have been recently developed [31, 32, 33, 34, 35] which have aspects of both LLCC and SOIC structures; two of these are

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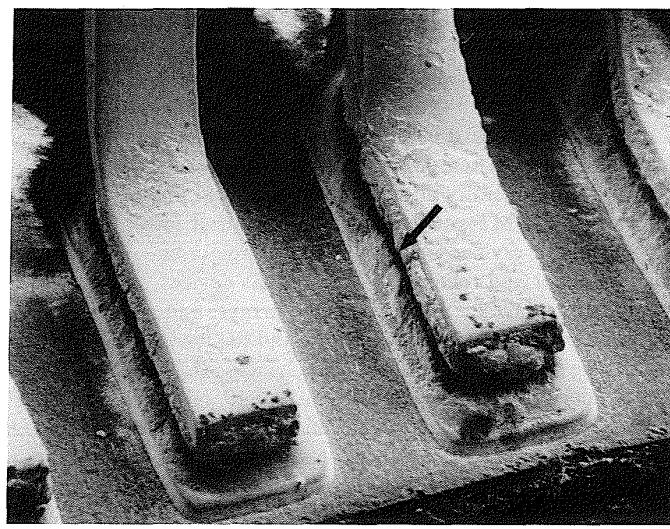


Figure 11-18. Solder Joint Failures. a) Cracking of the solder joint under thermal fatigue cycling in a Gullwing SOIC. b) Cracking of the solder joint under thermal fatigue in leadless chip carrier. Photograph courtesy of R.N. Wild, IBM-Owego

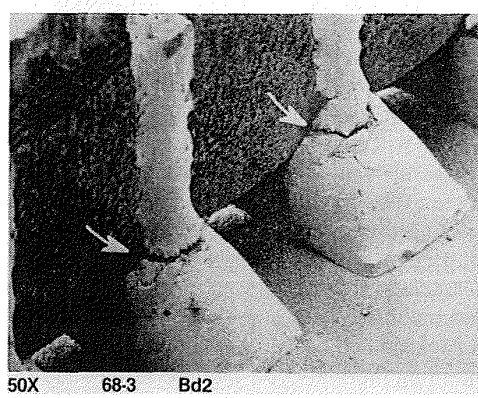


Figure 11-19. Cast Solder Column Interconnections. The solder columns are prepared using spherical solder preforms, which are cast into mold cavities adjacent to the I/O contact pad. The mold is removed and the package is surface soldered to the circuit board. Photograph courtesy of J. R. Fisher, AT&T Technologies [31], © 1984 by IEEE.

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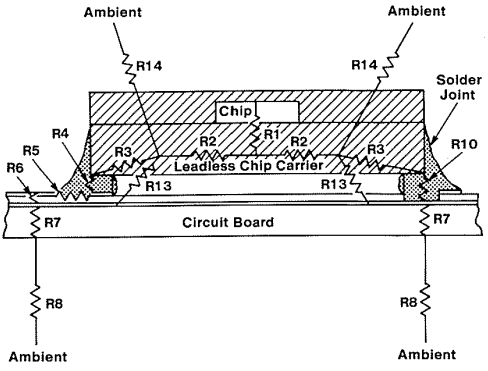


Figure 11-20. Thermal Resistance Model of Leadless Chip Carrier. The resistors represent thermal resistances between the elements of the package and board. After Welling, Ref. [36], 1982 — courtesy International Electronic Packaging Society.

shown in Figure 11-19, and Figure 6-21 in an earlier chapter. Some standards have been established for SOIC and LCCC devices [4, 38, 39], although this process is far from complete.

11.3.2 Thermal Displacements and Fatigue Behavior

As an active device dissipates heat to its surroundings during operation, or as the ambient system temperature changes, differential thermal expansions cause stresses to be generated in the interconnection structure. These stresses produce instantaneous elastic and, most often, plastic strains, as well as time-dependent (plastic and anelastic) strains in the joint, especially within its weakest segment. To evaluate the magnitude of the thermally induced strains, the temperature profile of the interconnected components must be known throughout an operational cycle or system temperature excursion. An example is shown in Figure 11-20, in this case for a LLCC [36], of the level of detailed thermal-resistance modeling, generated by experimental and/or analytical techniques, of the device, package, joint, and board assembly that is necessary to predict transient and steady-state temperature distribution. Once a thermal model for a particular package is generated, it can be applied to the specific component/board environment to be evaluated. The result is a set of temperature profiles for the package and environments, as indicated in Figure 11-21, for a J-leaded package [37]. This modeling effort may be very difficult for either air-cooled or conduction-cooled systems, given uncertainties in local airflow conditions or conduction paths (see Chapter 7,

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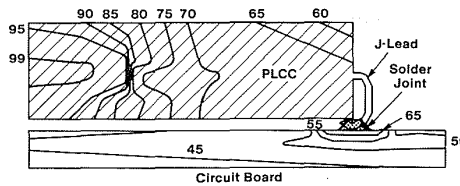


Figure 11-21. Isotherms of SOIC Package. The steady-state isotherms for a 68-lead Plastic Leaded Chip Carrier, having a chip operating at 1 W under forced convection (2 m/s). The numbers shown are the percentage of the maximum temperature less the ambient temperature, reached at each point. After Fox et al., Ref. [37] © 1985 by IEEE.

"Ceramic Packaging"); however, this thermal analysis is necessary to predict the thermal displacements which may lead to joint failure.

Once the time-dependent temperature profile is known, the thermal displacements may be predicted for the rigid elements of the structure. (For the present we will assume that the temperature is uniform in both the LLCC and the board, and that displacements are in-plane, only; the more complex, actual displacements are addressed later). For the LLCC structure shown in Figure 11-22, a simplified expression may be written to describe the relative displacement, δ, between the top and the bottom of the solder joint. Assuming a uniform LLCC temperature, T_L, and a uniform board temperature, T_B, the temperature-dependent length of these elements can be given as: $L_L = l_0(1 + \alpha_L(T_L - T_0))$; $L_B = l_0\,(1 + \alpha_B(T_B - T_0))$, where α_L and α_B are the coefficients of expansion of the LLCC and board, respectively, l_0 is the length of of the LLCC diagonal, and T_0 is the original temperature. The joint displacement is given by the difference in length between these elements, assumed to be rigid with respect to the solder joint: $\delta = 0.5l_0(\alpha_L(T_L - T_0) - \alpha_B(T_B - T_0))$. For a power-on cycle, in which T_L exceeds T_B, a displacement, here defined as negative, occurs. If, as is often the case, the value of α_B exceeds α_L, (e.g., for a ceramic LLCC on an epoxy-glass board) and the temperatures of LLCC and board achieve similar values during steady-state, then the displacement takes on a positive value. This is shown schematically in Figure 11-23. Thus, the displacement imposed on the solder joint consists of a transient plus a steady-state component, both of which may produce strain in the joint and, therefore, must be added to evaluate the total power-on displacement. The power-off cycle may show similar transient plus steady-state displacements.

The shear strain during a displacement cycle for the the LLCC joint is approximated by the relative displacement of the board and package, divided

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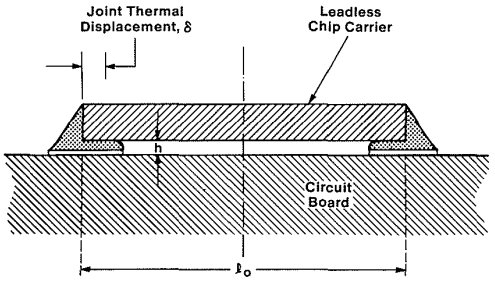


Figure 11-22. Schematic of LLCC.

by the height of the solder separating board and package. The rate of temperature change gives the strain rate. For most metals at room temperature the number of fatigue cycles necessary to produce failure is independent of imposed strain rate; however, for solders, given their low melting points, time-dependent deformation occurs that affects the failure process. Figure 11-24 shows a recent study of the effect of cycle frequency on number of cycles to failure [37]. The mechanism giving rise to the behavior shown in this figure is associated with the stress relaxation that occurs during the displacement-controlled, thermal or mechanical cycle. As the displacement is imposed, the shear strain consists of several components, elastic, plastic, anelastic, and, if the displacement is imposed slowly enough or at sufficiently high temperature, creep. The total shear strain, defined for the LLCC by the relative displacement, is equal to the sum of these strain components. At the steady-state condition (either power-on or power-off), the stress, generated

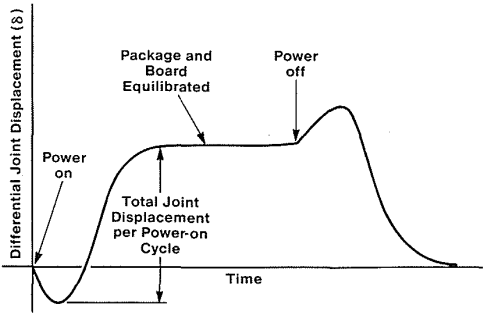


Figure 11-23. LLCC Joint Shear Displacements during Power Cycle.

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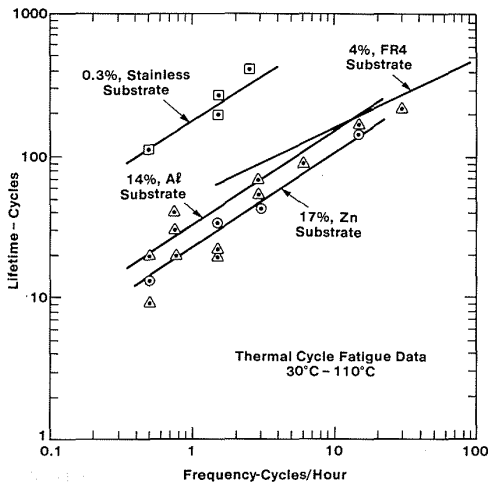


Figure 11-24. Frequency Effects on Fatigue Life. Thermal cycle fatigue life of a 29 x 29 mm ceramic LLCC, joined to solder pads supported by different substrate materials. After Fox et al., Ref. [37], © 1985 by IEEE.

as the displacement was imposed, relaxes through the conversion of the elastic and anelastic strains to creep strain. The amount of creep deformation is dependent on time and temperature. Thus, for a fatigue cycle having longer times between loading and unloading, the amount of stress relaxation and associated creep deformation increases. This phenomenon is generally referred to as creep–fatigue interaction and has been analyzed using a variety of procedures, the most notable of which is strain-range partitioning; [40, 41, 42]. This mode of analysis is considered in the Chapter 5, "Package Reliability," as it applies to the reliability testing of solder joints. Recently, several studies have been performed on *Pb–Sn* alloys to understand creep-fatigue in solders and solder joints [37, 43, 44, 42, 45, 46, 47, 48, 49]. Creep deformation adversely affects joint lifetime through grain-boundary cavitation and/or wedge cracking at grain boundaries (see, e.g., Ref. [50]); these defects promote fatigue-crack nucleation and propagation, (see, e.g. [51]). Figure 11-25 shows fracture micrographs of bulk specimens tested under load control at varying frequencies. The character of the fracture surface and, particularly, the number and size of voids change with frequency; as the frequency is decreased, the fracture morphology more closely resembles that of a creep-ruptured specimen. Further discussion of solder deformation and

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failure is deferred to section 11.4.1, "Solder Microstructure, Deformation, and Failure," on page 819.

SMT packages are most conveniently tested using thermal cycling of board plus package between temperature limits designed to induce a given differential thermal displacement. The displacement is somewhat idealized, given that significant transient-induced deformation during thermal cycling is eliminated, since the package and board are maintained at roughly the same temperature. Furthermore, temperature cycling beyond the normal operational temperature bounds (upper or lower) will result in a different de-

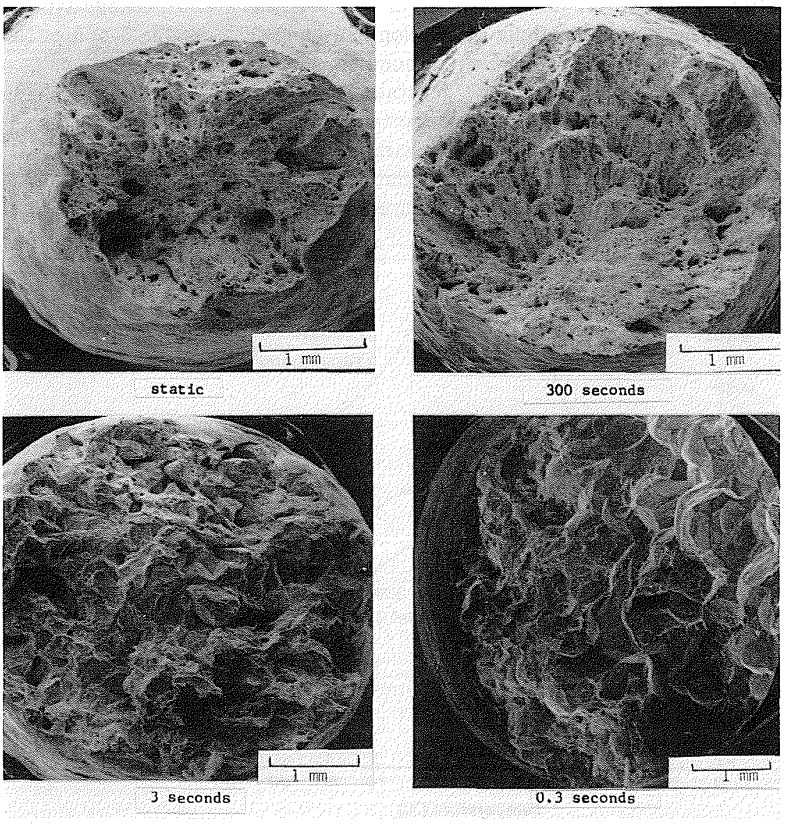


Figure 11-25. SEM Micrographs of Eutectic Lead–Tin Fracture Surfaces. Stress-controlled fatigue specimens, tested at a maximum stress of 27.6 MPa (4 ksi) for hold periods as labeled. After Weinbel et al., Ref. [43], 1987 — courtesy of J. Materials Research.

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gree of creep deformation and stress relaxation than an active device would experience. All four strain components are temperature-sensitive, and the rate of stress relaxation (conversion of elastic plus anelastic strain to creep strain) will be accelerated at higher temperatures [52]. Other metallurgical or microstructural effects, which will be discussed later, are also affected by the temperature cycle. In general, as the temperature is increased, the creep per cycle increases, resulting in reduced fatigue lifetime with respect to lower-temperature mechanical cycling at the same strain levels [37, 54]; see Figures 11-26 and 11-27.

Differences in LLCC test geometry, frequency, and temperature, and testing mode make comparisons of data between packages or between labs difficult. However, for a fixed set of test conditions and package type, a Coffin–Manson-like fatigue correlation can be developed which relates the estimated total shear strain to the number of fatigue cycles to failure (see Fig. 11-28). These data were generated, however, under high strain rate conditions and do not reflect the important time-dependent aspects of the deformation, which have just been illustrated. A phenomenological modification to the simple Coffin–Manson relation has been developed for high-*Pb*, C4 joints to accommodate temperature and frequency effects [55, 56], and

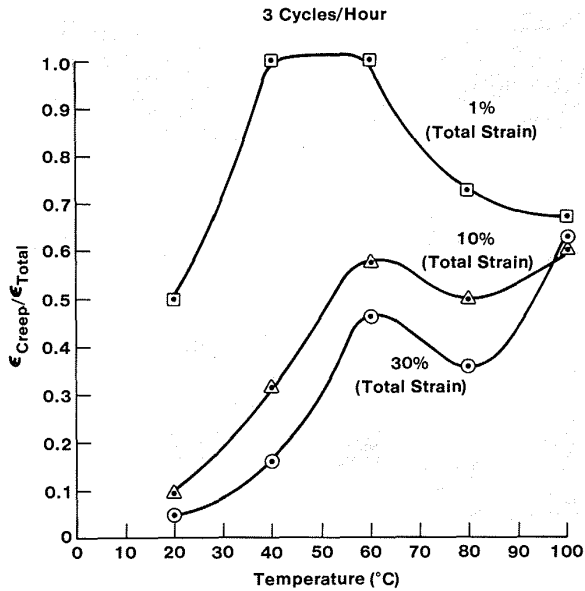


Figure 11-26. Creep Strain during Fatigue Testing. Estimated fraction of total strain which arises from creep during a fatigue cycle, based on bulk stress/strain rate relations for solder. After Shine et al., Ref. [44], courtesy of International Electronic Packaging Society.

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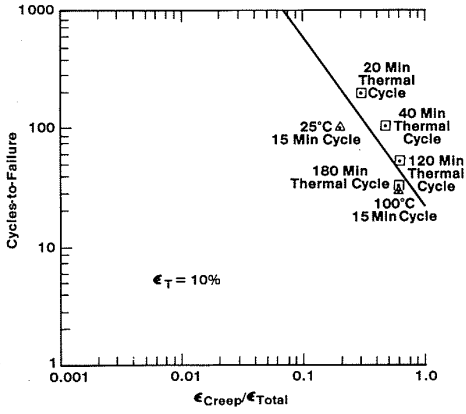


Figure 11-27. Fatigue Life as a Function of Creep Strain. Fatigue lifetime for both thermal and mechanical fatigue, plotted against the estimated fraction of total strain arising from creep. Fatigue data taken from tests on 84 lead ceramic LLCC packages on a variety of substrates. After Shine et al., Ref. [44], 1984 — courtesy of International Electronic Packaging Society.

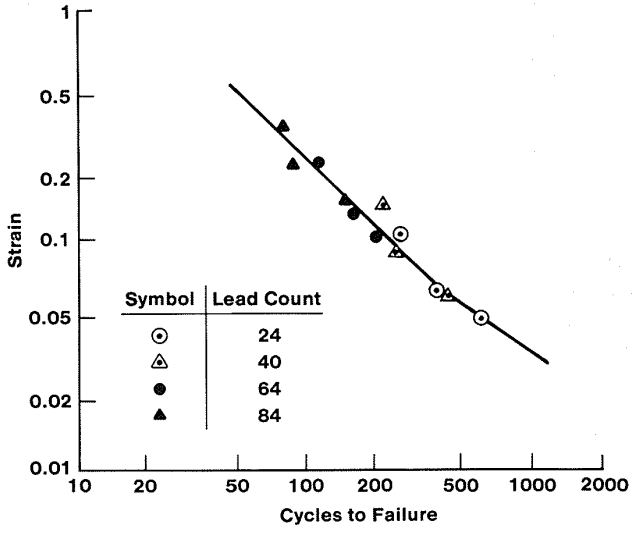


Figure 11-28. Strain vs. Fatigue Life under Thermal Shock. Fatigue life under thermal shock testing conditions, for LLCC packages having variable solder height (85, 135, and 185 μm) and leadcount. Data replotted by Hagge, Ref. [49], after Itoh et al. [53], courtesy of the International Electronic Packaging Society.

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efforts have been made to evolve similar relations for other solders and solder joints [45, 48, 49, 57] (see Chapter 5, "Package Reliability").

Most of the fatigue behavior listed previously has been associated with LLCC packages, given the limited elastic compliance of the joint. Similar fatigue concerns, although to a much lower degree [52, 59, 60] exist for SOIC leaded packages. In the J-lead or gullwing configuration (see Fig. 11-1), the thermal displacements between board and package are initially accommodated primarily by elastic deformation of the leads. These leads, therefore, greatly reduce the plastic strains in the solder joint on loading or unloading; however, the solder is stressed by the leads and undergoes creep deformation. The essential difference between the LLCC and SOIC joints is that for LLCCs the elastic plus anelastic stresses, generated in the solder on loading, are being relaxed by solder creep deformation; for SOICs the elastic stresses within the leads are being relaxed by solder creep deformation. This is so, providing that the lead stiffness, dependent on lead thickness and shoulder design, is relatively low [61]. Normally, lead thickness ranges from 150 to 250 μm for SOIC packages and may be reduced to about 25 μm for TAB packages. The packaging consideration that opposes thin leads is the increased sensitivity to handling damage. A recent study [37] has shown that for a typical J-leaded device a creep strain on the order of 0.1% arises during the power-on cycle; this is about a factor of 10 lower than the typical total strain imposed during a power-on cycle of LLCC packages. An IEEE Compliant Lead Task Force, having as contributors most of the computer, device, and package manufacturers in the United States, has completed an initial study to determine those factors that affect fatigue life of J-leaded packages [62].

A key element in evaluating the joint deformation and lifetime is the nature of the circuit board to which the package is joined. A listing of available board materials and their properties is given in Table 11-2 (see also [63, 64]). The primary board characteristics that influence joint lifetimes are thermal expansivity, which impacts relative package-board thermal displacements for a given temperature rise, and thermal conductivity, which impacts temperature excursions and distribution. The effect of substrate material on solder-joint fatigue life has been demonstrated in numerous studies [57, 58, 60, 65, 66, 67, 68] (see Table 11-3). Strain gauge and holographic techniques were used [69, 70] under thermal-cycling conditions to determine the local board and package bending and associated out-of-plane deformation, that arise from the nonuniform temperature distribution within the board and the package, and from package-to-board mechanical forces. Recent estimates have been made [71] on the effect of temperature gradients within a powered LLCC package. They show that these gradients, which are larger along the package centerlines and smaller along the diagonals, serve to make the thermal displacements much more uniform at each interconnection (within about

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Table 11-2. General Substrate Materials. After Lau and Rice [48], reprinted with permission of Solid State Technology. T_g = Glass transition temperature, °C; CTE = Coefficient of thermal expansion, 10^{-7}/°C ; κ = Thermal conductivity, W/m·K; E = In-plane tensile modulus, GPa; ε = Dielectric constant measured at 1 MHz; ρ_v = Volume resistivity, Ω·cm; ρ_s = Surface resistivity, Ω·cm H_2O Abs. = Moisture absorption, %.

Substrate/Property Material	T_g	CTE	κ	E	ε	ρ_v	ρ_s	H_2O Abs.
Epoxy Fiberglass	125	140–180	0.16	35	4.8	10^{12}	10^{13}	0.10
Polyimide Fiberglass	250	120–160	0.35	40	4.8	10^{14}	10^{13}	0.35
Epoxy Aramid Fiber	125	60–80	0.12	60	3.9	10^{16}	10^{16}	0.85
Polyimide Aramid Fiber	250	50–80	—	4.0	56	10^{12}	10^{12}	1.50
Epoxy Quartz (Fused Silica)	125	60–120	—	—	—	—	—	—
Polyimide Quartz (Fused Silica)	250	60–120	—	—	—	10^{8}	10^{8}	0.50
Fiberglass/Aramid Fiber Composite	125/250	50–80	—	—	—	—	—	—
Fiberglass/Teflon Laminates	75	200	0.26	3	2.3	10^{10}	10^{11}	1.10
Alumina-Beryllia Ceramic	NA	50–70	21.0	560	8.0	10^{14}	—	—

Table 11-3. Thermal Cycles to Failure for Several Substrate Materials. Failure of Leadless Chip Carriers vapor phase reflowed to several substrate materials, during thermal cycling between −55 and 125°C. After C. J. Brierley, D. J. Pedder, J. P. McCarthy [58], 1985 — Plessey Research (Caswell) Ltd., courtesy International Electronic Packaging Society.

Chip Carrier Size (I/Os)	FR4 Glass Epoxy	FR4 + Acrylic Elastomer	FR4 + Butadiene Elastomer	Kevlar-Polyimide	Quartz-Polyimide	FR4 Copper Clad Invar
16	940	>1000	>1000	272		
20	821				>1500	>1500
28	517	>1000	>1000	217	>1500	>1500
44	279	945	810	237	>1500	>1500
52	170	642	614	182		
68	105	535	394	153	1006	>1500
84	60				795	>1500

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1%) than would be observed for thermal-cycling experiments (about 40% difference). Holographic measurements and full finite element analysis have been used [11] to observe nonplanar deformation for a pinned package soldered to a circuit board. As with the effect of nonplanar deformation of C4 solder joints arising from chip bending [72] (see Chapter 6, "Chip-to-Package Interconnections"), the tensile and compressive SMT joint loadings are expected to have an important effect on joint lifetimes, when superimposed on the nominal shear loading. As yet, however, models have not been published that quantify the effect of multi-axial displacements on solder-joint fatigue lifetimes. Studies on materials other than solders have demonstrated the importance of modest loadings that are applied on axes other than the primary fatigue-loading axis (see, e.g., [73, 74]).

11.3.3 SMT Solder Joints

The general properties of solder are discussed in section 11.4, "Solder and Solder Joining," on page 819 however, the actual behavior of SMT solder joints may depend primarily on complicating, joint-specific factors, such as adjacent metallurgy, joint geometry, defects, or fabrication procedures, rather than on bulk properties.

A first issue considered, here, is the formation of intermetallic phases at the solder-to-board or solder-to-package interfaces. Although most current-carrying members used in the first-level package and in the circuit boards are copper or copper-base alloys, it is most common for these conductors to be coated with other metal(s) to provide solder wettability, inertness with respect to storage environments, or resistance to joint degradation during prolonged operation at elevated temperatures. Conventional metal coatings include nickel and/or gold plating, tin or solder plating, or dipping. More complex, multilayered interconnection structures such as *Ti/Cu/Ni/Au*, or *Ti/Pd/Cu/Ni/Au* may be used for ceramic chip carriers or substrates [75, 76]. The interconnection structure may be subjected to high temperatures during some package fabrication or testing steps, such as die-attach or burn-in, which cause interdiffusion of the coating layers. This can facilitate the formation of intermetallics, or may affect their subsequent formation during soldering, thereby adversely impacting solderability; this is discussed in section 11.4.3, "Solderability," on page 836. The primary interest in intermetallic formation in the joint is associated with the solder joining and/or dipping process, as well as the subsequent processes of burn-in and device operation. During joining the solder is melted, at which time much of the reaction between *Sn* and the underlying metallurgies occurs. Several recent studies have analyzed the interaction of liquid tin and solder with gold, nickel, and copper [77, 78, 79, 80, 81]. The rate of dissolution of gold and subsequent dispersion of the *Au–Sn* intermetallics into the molten solder is quite rapid compared to copper or nickel [78]. All of these metals are "fast diffusers" in

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solder, with diffusivities 3 to 5 orders of magnitude faster than self-diffusion of lead [82]. It is shown that significant reaction between gold and solder can occur well below the melting point [78, 83]. This may have important consequences for the situation where gold is plated over a material, such as nickel, which requires a relatively high temperature to react with the solder. The dissolution of the gold, leaving a less wettable underlying layer, may result in limited adhesion between the coating and solder or tin [79]. Gold dissolution is slowed considerably by alloying with palladium [85]. For copper or nickel, layers of intermetallic are formed adjacent to the unreacted metal, with the kinetics of copper intermetallic formation being much more rapid than for nickel. At a $Cu - Sn$ interface layers of both Cu_3Sn and Cu_6Sn_5 are normally observed, with the growth being controlled by diffusion through the intermetallics [84, 86, 87]. Earlier work shows a linear time dependence to the growth of Cu_6Sn_5 at room temperature, attributed to interface-controlled growth kinetics [88]. Studies on the growth of nickel intermetallics show that after an initially rapid growth for short times, diffusion-controlled growth occurs [77, 80]. Three Ni–Sn phases have been observed: Ni_3Sn, Ni_3Sn_2, and Ni_3Sn_4 [89]. Figure 11-29 shows the rate at which copper and nickel react with molten $60Sn$–$40Pb$ solder. A layer of Ni is commonly used as a diffusion barrier to inhibit the formation of thick Cu–Sn intermetallics [90]. Although much of the intermetallic reaction and growth occurs during joining, this layer can continue to grow at lower temperatures [84, 91], as shown in Figure 11-30.

The reaction of solder with the metal contacts to form an intermetallic compound is a positive contributor to the establishment of a good joint.

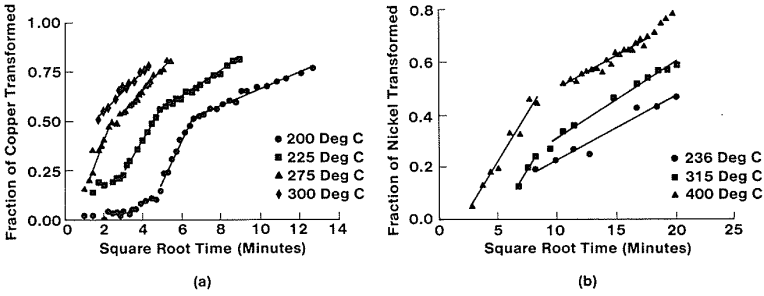


Figure 11-29. Reaction Rate of Copper and Nickel with 60/40 Solder. The reaction of copper or nickel with solder was measured by the reduction of the X-ray reflection associated with the bulk metal phase, as the metal was dissolved into the solder or as intermetallic compounds were formed at the reaction interface. After DeHaven, Ref. [77], 1985 — courtesy of Materials Research Society, reprinted with permission.

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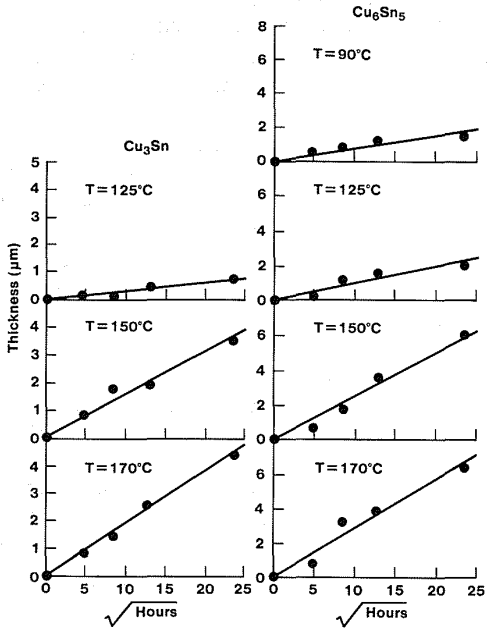


Figure 11-30. Growth of Copper–Tin Intermetallics. The thickness of the two copper–tin intermetallics was metallographically measured after aging of reflowed solder paste on copper (100) single crystals. After Dunn et al., Ref. [84], 1985 — courtesy of Materials Research Society, reprinted with permission.

However, the degree of reaction is also important to the mechanical behavior of the joint. Studies of solder joints have shown that the strength of a given joint can be adversely affected by a prolonged reflow cycle in which the joint is molten [92, 93, 94], and by prolonged aging at elevated temperature [83, 87, 92, 95, 96]. Figure 11-31 gives an example of such effects. Fatigue life can also be affected by the joint structures developed under differing reflow conditions [93, 97]. The solder/metallization reaction affects intermetallic thickness and, for a *Pb–Sn* solder, the thickness and composition of the lead-rich region, adjacent to the tin-rich intermetallic layer. This compositional inhomogeneity will deform in an inhomogeneous manner, as well. Such a condition may be particularly harmful where it coincides with a point of stress concentration. This is one of the likely causes of early fatigue failure in an LLCC joint, in which a weak, low tin layer is developed between the relatively

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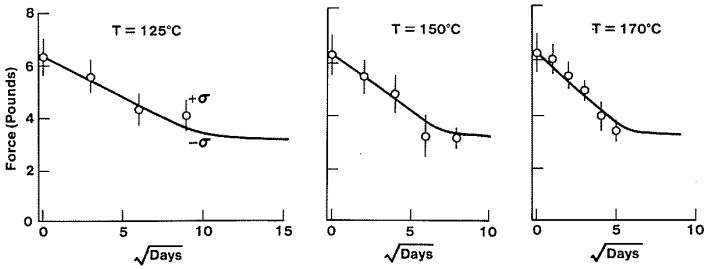


Figure 11-31. Effect of Thermal Aging on Solder Joint Strength. Joints, prepared using solder-clad (*60Sn–40Pb*) phosphor bronze pin clips, were soldered to ceramic substrates having *Pt–Pd–Ag* thick-film metallization. These were then aged and pulled After Marinis and Reinert, Ref. [87], © 1985 by IEEE.

strong eutectic solder and intermetallic regions [84, 87, 98]. These low tin regions have been observed [95] at crack surfaces in solder joints. Another effect of the solder/metal reaction may be to change the bulk properties of the solder. For example, metals such as gold, and to a lesser degree, copper, which are reacted with and dispersed into the solder, strengthen the solder, thereby reducing fatigue life [49, 60, 99, 100]. Solubility data for contact metals in molten solder is given in Chapter 6, "Chip-to-Package Interconnections," and other sources [101, 102].

In summary, regarding the interaction of the interconnection points with the solder, it is desirable to have a reactive couple but one which has a limited extent of reaction. This would eliminate the problems of (1) a thick, brittle intermetallic, (2) a soft, tin-depleted layer in the solder adjacent to the intermetallic layer, and (3) a joint having properties that degrade with time. Frequently the leads of SOIC devices, subject to the considerations mentioned previously, must also be immune to lead-forming operations. This imposes an additional constraint that the plated metallization and reaction layers be sufficiently ductile to avoid cracking during forming; this may impact the choice of lead finish [103].

Another issue that affects SMT interconnection performance is the joint geometry. For LLCC joints, particularly, the height of the solder pillar connecting package to board has a very important impact on fatigue life. The first-order relation of strain per cycle to the inverse of solder height, h, is linear, resulting in a nearly quadratic increase in cycles-to-failure, N_f, with joint height; i.e., N_f is roughly proportional to h^2. This has been experimentally substantiated for LLCC joints [31, 57, 60, 93]. Note, since the grain size of the joint may increase with joint thickness [46, 104] (presumably arising from

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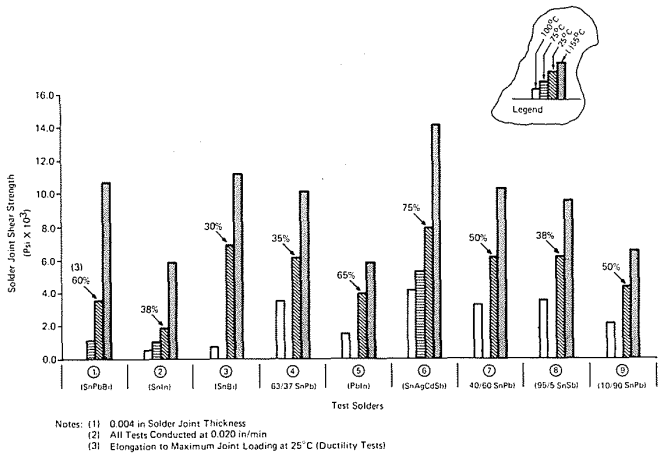


Figure 11-32. Solder Joint Shear Strength vs. Solder Composition. Lap shear strength of solder joints (0.1 mm thick, 1.1 mm wide, 2.9 mm long), tested at a shear displacement rate of 0.085 mm/s. Compositions: (1) *16Sn 32Pb 52Bi*, (2) *50Sn 50In*, (3) *42Sn 58Bi*, (4) *63Sn 37Pb*, (5) *50Pb 50In*, (6) *95Sn 3.5Ag 1.0Cd, 0.5 Sb*, (7) *40Sn 60Pb*, (8) *95Sn 5Sb*, (9) *10Sn 90Pb*. After Wild, Ref. [46], 1973 — courtesy of the author.

local cooling-rate effects during reflow), and since reduced fatigue life may accompany grain coarsening (see section 11.4.1, "Solder Microstructure, Deformation, and Failure," on page 819), a joint lifetime prediction based only on shear strain considerations may be incomplete. The solder height for SOIC joints is less critical, given the compliance of the leads; however, wicking of the solder up the leads can affect compliance [61] and cracking behavior. It has been demonstrated [105] that extension of the LLCC pads on the board well beyond the package edge extends fatigue life. This is caused by the increased distance which the crack, which nucleates beneath the LLCC package [60], must propagate through a solder volume wherein the strain, arising from the thermal displacements, is much less localized. Several standard [71] and nonstandard [106] LLCC geometries have been studied, illustrating the significance of joint geometry on joint stresses and fatigue life.

Defects within the solder joint, such as voids, are frequently observed. One limited study [107] shows a link between the presence of voids (the origin of which was ascribed to flux decomposition), and reduced mechanical and thermal fatigue life. However, other work on joints where voids were present showed considerably less effect on mechanical behavior, except where the

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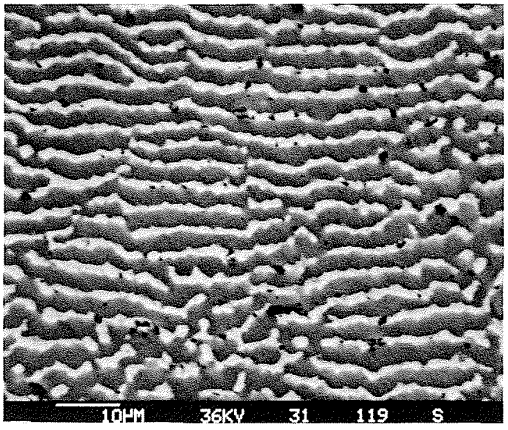


Figure 11-33. Cast Lead–Tin Eutectic, Cooled Slowly. SEM micrograph of cast eutectic solder, slowly cooled, etched with 2% *HCl*, 98% ethanol.

voids significantly reduced joint cross section [108]. A correlation between void cross section, generated under several reflow conditions, and a slight (~10%) decrease in joint shear strength was also observed [109].

11.4 SOLDER AND SOLDER JOINING

11.4.1 Solder Microstructure, Deformation, and Failure

In this section the general properties of solders are described. Given the predominant use of eutectic or near-eutectic *Pb–Sn* solder for most package/board interconnections, this solder will receive the major focus. Comparative strength and elongation values for lap shear joints for other solder compositions at several temperatures [46] are given in Figure 11-32. The relative thermal fatigue life for several *Pb–Sn* solders has recently been evaluated for die-bonding applications [110] and other joint configurations [111]. The compositions and melting temperatures of other common solders are listed in Table 6-1. Phase diagrams are shown in Figure 6-11.

The first aspect of eutectic solder to be considered is the variety of microstructures which may be observed; these diverse structures strongly affect the mechanical response. Figures 11-33 and 11-34 show two extremes of the as-cast structure, developed at relatively slow (<1 K/s) and very fast (~100 K/s) cooling rates through the solidification temperature. In these figures the *Pb*-rich and *Sn*-rich phases are differentiated and show, in the first case, a

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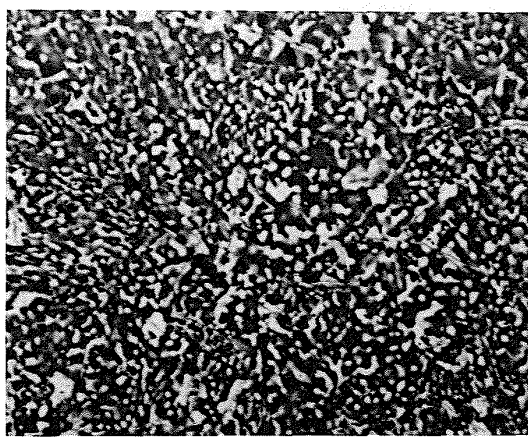
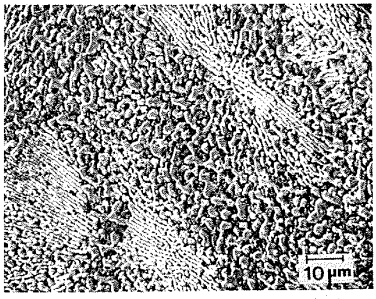


Figure 11-34. Cast Lead–Tin Eutectic, Cooled Rapidly. SEM micrograph of cast eutectic solder, very rapidly cooled, etched with 2% *HCl*, 98% ethanol.

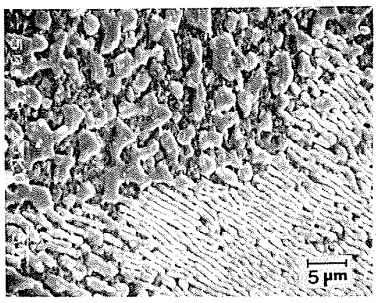
well-defined lamellar structure of alternating platelets of the two phases and, in the second case, an irregular, spherodized distribution of the *Pb*-rich phase in the *Sn*-rich matrix. Figure 11-35 shows the microstructure arising from an intermediate cooling rate, in which regions of lamellar and near-spherodized structures are both present. This type of mixed structure is similar to that of a vapor-phase reflowed J-lead joint shown in Figure 11-36. In general, as the cooling rate during solidification decreases, the interlamellar spacing decreases, the lamellar colony (grain) size decreases, and the incidence of the spherodized, rather than the platelet morphology of the *Pb* -rich phase increases. To the considerable degree that microstructure influences the mechanical behavior of eutectic solder, the joining technique will also have an influence, given the large span in solidification and cooling rates which may be observed during reflow (~1-1000 K/s).

The as-cast structure is not stable with respect to aging or deformation. It has been observed in several studies that both thermal aging and thermal cycling induce coarsening in as-cast solder-joint structures and bulk materials [46, 95, 104, 112, 113, 114]. The instability of the cast structure given earlier in Figure 11-35 is illustrated in Figure 11-37, which shows the effect of annealing at 150°C for various lengths of time. A transition occurs from the as-cast structures to a much more equiaxed distribution of the two phases, after annealing. If the as-cast material is significantly deformed (~10-15% uniaxial strain, or at much lower levels under repeated fatigue cycling), then annealed at room temperature or above, it undergoes recrystallization, as

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(a)



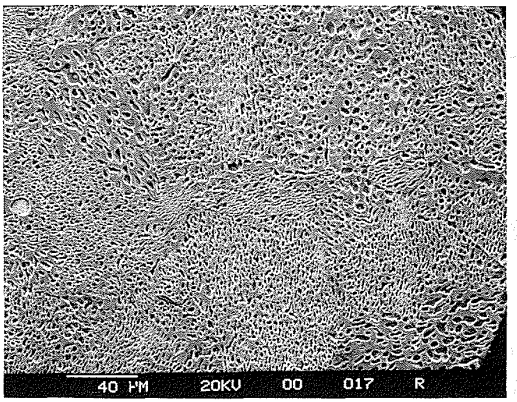
(b)

Figure 11-35. Sperodized and Lamellar As-Cast Eutectic Solder. SEM micrograph of as-cast eutectic *Pb–Sn* solder, electropolished, and etched using a solution of sodium acetate, acetic acid, and water at room temperature, at 40 V using a *Pt* electrode. This etches the *Sn* phase preferentially.

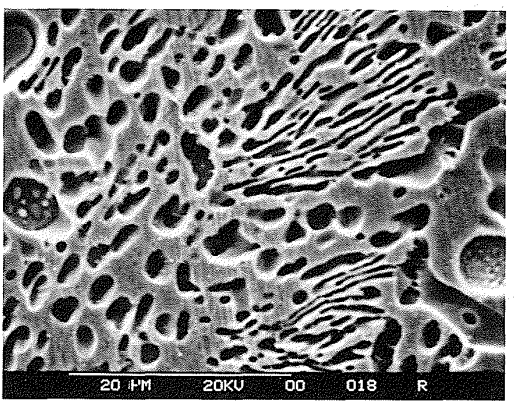
shown in Figure 11-38. This process leads to a structural refinement, rather than to the structural coarsening associated with annealing alone. Figure 11-38 shows this equiaxed structure, which is observed to be quite stable with respect to annealing or deformation [112]. Given the variation in mechanical properties among each of these structures, as described subsequently, it is essential to know the solder-joint microstructure before predicting mechanical response.

In summary, eutectic solder can assume any of several microstructures, depending on solidification conditions and subsequent annealing and/or deformation: (1) a lamellar, as-cast structure, in which alternate platelets of *Pb*-rich and *Sn*-rich phases are formed in coarse colonies; (2) a near-equiaxed distribution of the two phases, after annealing; (3) a refined, equiaxed structure formed after deformation and recrystallization. Furthermore, regarding

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(a)



(b)

Figure 11-36. Microstructure of Reflowed Solder Joint. SEM Micrograph of a vapor-phase reflowed J-Lead eutectic solder joint. This was polished, then etched with four parts glycerol, one part acetic acid, one part nitric acid. This solution etches the *Pb* phase preferentially.

the as-cast structure, the fineness and degree of perfection are quite dependent on solidification rate.

For materials used at high temperatures with respect to their melting points, processes which are affected by diffusion, such as deformation, recovery, and recrystallization, are enhanced. Solders, for which room temperature may well exceed one half of the melting temperature, exhibit creep deforma-

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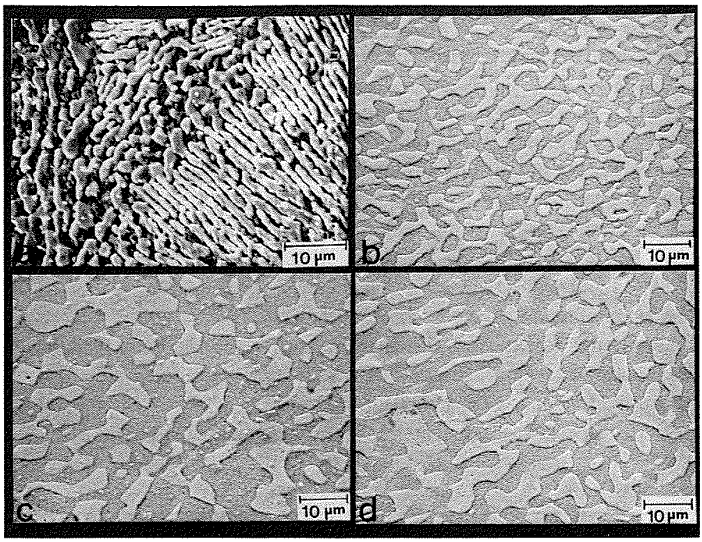


Figure 11-37. Cast Eutectic Solder, Annealed at 150°C.. The polished and etched eutectic *Pb–Sn* solder shown: (a) As-cast; (b) 15 hours at 150°C; (c) 150 hours at 150°C; (d) 300 hours at 150°C, etched as described in Figure 11-35. After Raman and Reiley, Ref. [112], 1988.

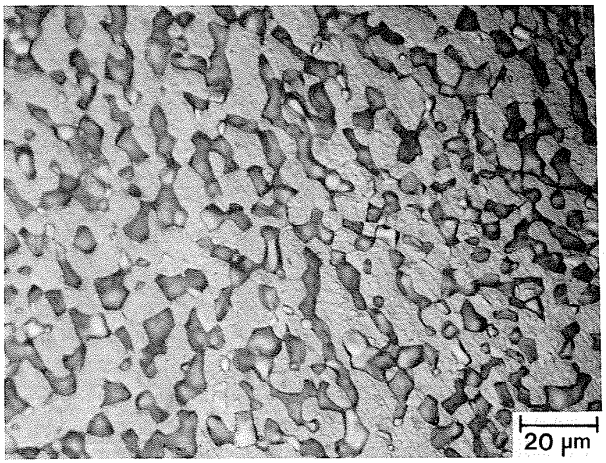


Figure 11-38. Rolled Eutectic Solder, Recrystallized at Room Temperature. Eutectic *Pb–Sn* solder rolled and recrystallized at room temperature, etched as described in Figure 11-36. Courtesy of V. Raman, IBM-Research.

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tion mechanisms not observed to any appreciable extent near room temperature in higher melting-point materials. The deformation mechanisms are frequently separated into the regions of temperature and applied stress in which a particular mechanism is dominant; this is usually given graphically in the form of a deformation map [115]. Note that these maps are normally defined for steady-state conditions and for stabilized microstructures, neither of which may be appropriate to the solder-joint structure or deformation conditions of interest, as pointed out earlier.

Deformation maps for pure lead and other pure metals or alloys are available [115, 116, 117]; however, maps for eutectic solder have not been generated because of uncertainty in the deformation mechanisms and their interplay. This is not to say that the phenomenology of the deformation in terms of strain-rate sensitivity, temperature and grain-size dependence have not been studied [112, 113, 118, 119, 120, 121, 122]. The origin of the uncertainty is that eutectic solder, in its fine-grained, recrystallized form, exhibits a phenomenon known as superplasticity, in which extremely large elongations-to-failure are observed, associated with extensive grain-boundary sliding (GBS). It is the interaction of the several individual creep mechanisms with grain-boundary sliding which has not been satisfactorily incorporated.

Normally, the independent deformation mechanisms are described by a relation between tensile strain rate, $\dot{\varepsilon}$, and applied stress, σ:

$$\dot{\varepsilon} = \frac{A\mu bD}{kT}\left(\frac{\sigma}{\mu}\right)^n\left(\frac{b}{d}\right)^p \qquad [11.1]$$

where

μ = shear modulus
A = a constant
b = relevant Burger's vector
d = grain size
D = diffusion coefficient for the rate-limiting diffusion process (which is both temperature dependent and path dependent)
n and p = exponents characteristic of the mechanism
k = Boltzmann's constant
T = absolute temperature.

The total strain rate is the sum of the contributions of all the operative mechanisms. Frequently, in studies on superplasticity the analyses are given in terms of the strain rate sensitivity, $m \equiv d \ln \sigma / d \ln \dot{\varepsilon}$, which is the same as $1/n$ in Equation 11.1 for a constant temperature and grain size. These studies (see, e.g., [123]) have divided the room temperature deformation behavior for eutectic solder into three regimes: Region I, for low-strain rates ($\dot{\varepsilon}<10^{-5}s^{-1}$), where n is high (≥ 5); Region II, for intermediate strain rates ($10^{-5}s^{-1}<\dot{\varepsilon}<10^{-2}s^{-1}$), where n is low (~ 2); and Region III, for high strain

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rates ($\dot{\varepsilon}>10^{-2}s^{-1}$) , where n is high (≥ 5). Most deformation studies on solder, from which the general phenomenology given previously is extracted, have been performed on relatively fine-grained, worked-recrystallized material. However, as-cast material at room temperature does not show the high strain-rate sensitivity associated with (and necessary for) superplastic deformation [112, 119, 124] and essentially exhibits only Region III behavior, which extends to low-strain rates. Furthermore, the elongation-to-failure, which is much reduced for as-cast material, increases sharply as the interlamellar or interparticle spacing is decreased [125]. To the degree that ductility under fatigue deformation follows that of uniaxial deformation, it may be projected that a more rapidly solidified solder joint, having a more refined structure, will exhibit improved fatigue ductility. This has been substantiated in recent reverse-bending fatigue experiments on eutectic solder solidified at widely differing rates [126]. In these experiments bulk solder was cast under widely differing solidification rates; and, as the solidification rate increased, the decreased grain size was accompanied by an increase in fatigue life by a factor of 10. One explanation is the reduction in the localized deformation which occurs at the intercolony boundary, as the colony size is reduced.

Several efforts have been made to use deformation-modeling techniques to predict load/time behavior and fatigue lifetime for solder structures. Stone and colleaques [127] have applied Hart's model [128] to a well-characterized solder-post joint [70]. This model incorporates the parallel rate-controlling processes of grain-matrix deformation (plastic and creep) and grain-boundary sliding accommodated by matrix deformation. The interaction of the two processes is treated using semi-empirical structure parameters, rather than detailed deformation mechanisms. Shine and Fox [104] have also modeled the deformation observed in solder joints, in this case, under isothermal fatigue conditions. Their model is based on the independent operation of matrix deformation and grain-boundary sliding plus matrix accommodation. Using instantaneous stress-strain rate data and constitutive relations, they separate the two creep components for the various temperatures and geometries of the experiments. The correlation of the relative contribution of plastic and creep strain for the fatigue of lap-shear joints, using several strain-range partitioning methodologies was attempted [42]. The conclusion of this work was that a failure criterion could be developed based only on a creep-time damage function, rather than on a creep-strain function. This was felt to imply an environmental degradation, such as would be associated with oxidation, a phenomenon which has been observed in solders [130, 131] and in lead [132, 133]. Other recent work on fatigue of low-tin solder reinforces this conclusion[134].

The failure mechanisms under uniaxial creep deformation have been studied extensively, using, for example, stress/temperature maps of predominant fracture mechanisms [50]. However, high-temperature fatigue-crack

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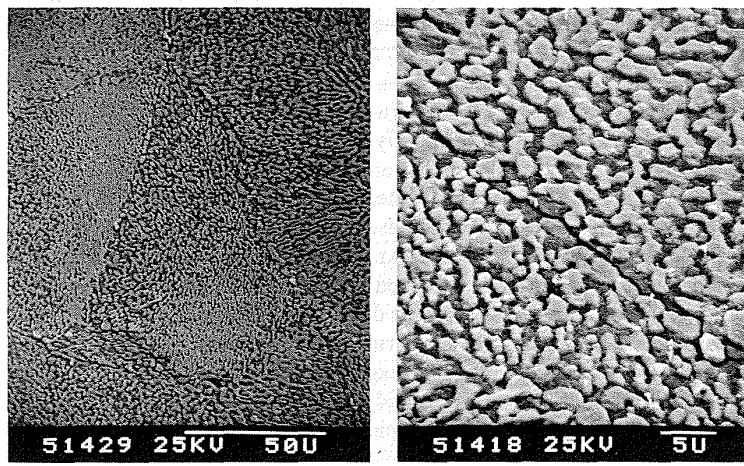


Figure 11-39. Cracking at Grain Boundaries in Cast Eutectic Solder. Polished and etched surface of cast *Pb–Sn* solder, cycled under reverse-bending fatigue at +/- 0.75% strain for 2200 cycles at room temperature at 0.0055 Hz, etched under conditions given in Figure 11-35. Cracking is observed at the boundaries between the lamellar colonies (the grain boundaries). After Raman and Reiley, Ref. [129], 1987.

nucleation and propagation mechanisms have not been studied so closely, although similarity to creep-failure mechanisms is expected for the local deformation processes causing cracking under high temperature fatigue. Several recent studies have been made to characterize and model fatigue failure processes in solder [43, 47, 51, 112, 123, 129, 135]. Figure 11-39 shows the microstructural features of eutectic solder deformed under reverse-bending fatigue. Here, cracking is observed at the interlamellar colony (grain) boundaries under fatigue [129] and, as well, under low strain rate tensile deformation [112]. This is clearly the point at which strain is localized during high-temperature deformation and may be the key microstructural element which sets the intrinsic fatigue limit in cast eutectic solder joints. In the single phase, low-tin alloy grain-boundary migration and sliding are observed, along with grain-boundary cavitation and cracking [123, 129, 137], under similar deformation conditions.

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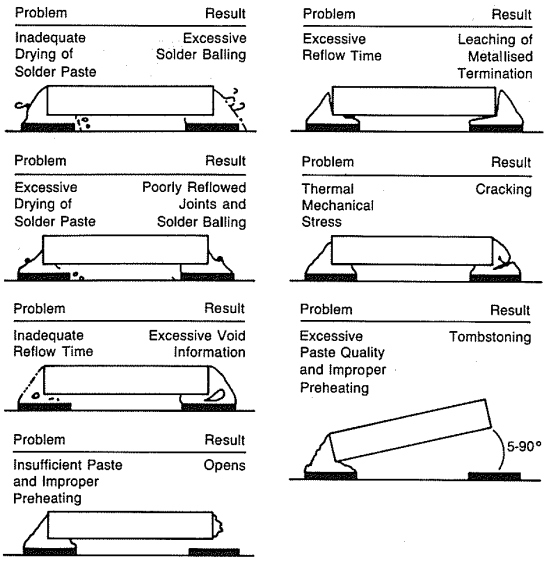


Figure 11-40. Typical SMT Problems. After C.J. Brierley, L. Considine, and D.J. Pedder, Ref. [136], 1985.

11.4.2 Solder Joining Techniques

Many techniques have been demonstrated for solder application and package-to-board joining. For solder deposition the dominant approaches involve dipping (or wave soldering), paste screening or stenciling, plating or the application of pre-forms. Although evaporation of solder C4s on chips for chip/substrate interconnection is used, evaporation is not normally used as a solder application technique for package-to-board interconnections. The joining of package and board is performed with a variety of reflow processes which depend on the form of the applied solder, the structures to be joined, and other factors, described in this section. Figure 15-9 on page 1043 of Chapter 15, "Consumer Product through Mid-Range Computer Packaging" illustrates the four steps involved in attaching a surface-mount component (SMC) to a second-level package. The major joining techniques include wave soldering, vapor-phase reflow, infrared (IR) reflow or hot-gas reflow, laser soldering or hot-knife soldering. Each technique has its own advantages or specific areas of applicability. A number of SMT problems that are typically experienced, illustrated in Figure 11-40, will be discussed in this section.

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Wave Soldering: Wave soldering [138, 139, 140, 141, 142, 143, 144] is a technique which has been practiced for over 30 years and is applicable to both PTH and SMT interconnections. However, in contrast to PTH components, SMT components must be secured to the board during wave soldering, usually with an adhesive. This requires adhesive dispensing and curing operations, which precede wave soldering; (see, e.g., [145]). With wave soldering the two processes of solder deposition and solder joint formation occur in a single operation. It has evolved to the current configuration in which a circuit board plus attached components are conveyed through the machine along a slightly ascending incline, where the board is preheated and fluxed, then directly exposed to molten solder on the underside of the board at a solder temperature of about 240 to 260°C (for eutectic or 60/40 solder). The soldering operation is commonly carried out using either a single- or a double-wave system. The latter approach includes, for the first wave, a highly turbulent solder jet with local velocities sufficient to allow solder penetration into fine-dimensioned crevices. The second wave, separated from the first wave to allow for flux outgassing [64] and to prevent oxide entrapment [143], has a laminar flow pattern to distribute the solder uniformly. The time of contact between molten solder and the assembly is on the order of a few seconds. This time may be controlled by several factors: for example, a lower bound may be set to allow solder penetration into the plated-through-holes in the board, or an upper bound may be set to prevent prolonged high-temperature exposure of certain devices [142]. The final contact between solder wave and board should be well controlled to minimize solder bridging between metallization points. Another recent modification to minimize bridging is the use of a hot-air knife, in which an air jet is directed on the board shortly after leaving the solder wave [146] (see Fig. 11-41). There are substantial reservations regarding the applicability of wave soldering for VLSI SMT packages having lead pitches at or below 1.27 mm, because of the solder bridging problem [141]. Given the following three factors — (1) a large, successful experience base for wave soldering for PTH packages; (2) the need for PTH packages on a large fraction of boards for the foreseeable future; (3) the problems of wave soldering for fine-leaded SMT devices — it is likely that many board-soldering procedures will involve wave soldering plus a second soldering technique.

Solder Paste: Another method for applying solder to the board for subsequent reflow, which is compatible with a number of reflow techniques, is the use of solder paste [94, 147, 148, 149, 150]. Solder paste consists of metal-alloy powders ranging in size from about 150 μm to less than 30 μm (100 to 400 mesh), mixed in an organic vehicle, which contains flux, solvents, plus a thixotropic agent to regulate viscosity. The metal powders may be prepared from a wide range of solder compositions, usually by inert gas atomization. The powders are chosen for size and morphology to accommo-

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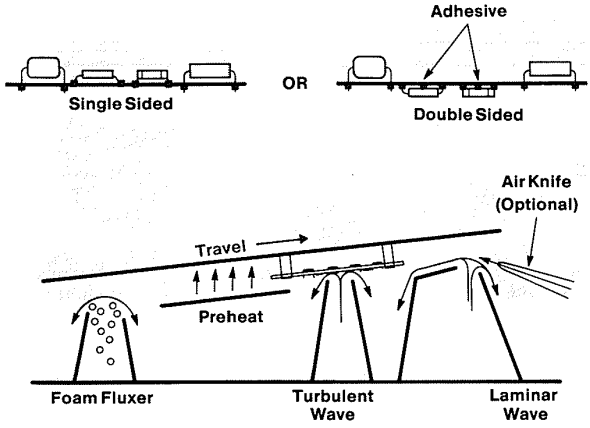


Figure 11-41. Schematic Diagram of Wave-Solder Proccess.

date screen or stencil printing dimensions and to regulate viscosity for the desired metal loading, typically 75 to >90 wt%. Paste is commonly applied to the board by forcing the material through openings in wire screens or sheet-metal masks, although other techniques are also used [147]. Solder paste that has been screened onto a printed-circuit board interconnection pad is shown in Figure 11-42. For screening, the particle size must be kept well below the screen mesh or mask opening dimensions to avoid clogging. On the other hand, a particle distribution having appreciable fractions below about 5 μm will likely contain a large oxide content, a factor that may affect the choice of flux and/or optimum reflow cycle (to allow time for oxide reduction). The final solder pattern prior to joint formation is quite dependent on the screening precision and on the postscreening paste flow, both of which require a well-controlled viscosity, over quite a range of shear rates. It should be noted that the choice of solder paste and processing parameters may change with the pad dimensions and applications of interest. See the list of references given previously for details regarding solder paste; in addition, some of the important characteristics will be briefly described in the following paragraphs.

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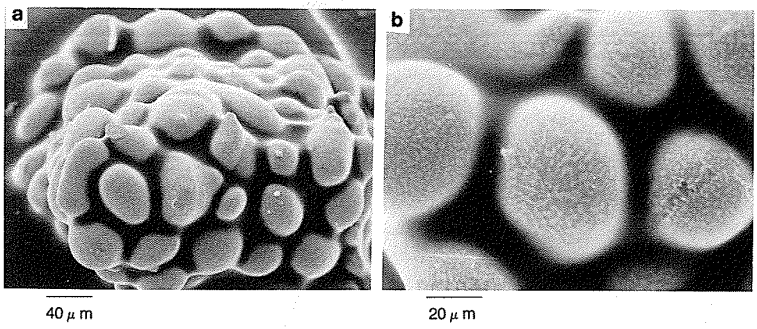


Figure 11-42. SEM Micrograph of Screened Solder Paste. (a) A screened solder pad. (b) Closeup of paste powders; the contrast difference marks the *Pb*-rich and *Sn*-rich phases. Courtesy of S. K. Kang, IBM-Research.

Viscosity: The ability to force the paste into a given pattern and, as well, the ability for the pattern to be stable through the intervening steps between screening and reflow, are dependent on paste viscosity. This property is a coarse measure of the complex interplay between particle size distribution, particle shape, metal loading, and properties of the multicomponent vehicle. The value of viscosity must be measured over a range of shear rates appropriate to the paste deformation during and after printing; e.g., the shear rates during screening may exceed 100/s, while during handling they will drop to values many orders of magnitude lower [147]. This low shear-rate paste spreading is referred to as "slump" and may be the important factor that must be adjusted to avoid bridging of fine solder patterns. This is especially so when fine and coarse patterns are printed simultaneously using a single paste thickness. The empirically determined values of viscosity/shear rate which give acceptable paste behavior are likely to be applicable only to a given paste [94]; these values may be used to determine lot-to-lot variations, shelf life, effectiveness of mixing operations, or, in some cases, necessary additions to the paste.

Component-to-Paste Adhesion: For many SMT applications the printed paste serves as an adhesive to hold the components in place until reflow. This requires a minimum shear strength to avoid component misalignment, especially where relatively massive components are subjected to rapid board movements during component placement or other board-handling operations. Because the adhesive strength is quite dependent on the solvent retention in the printed paste [151], this may become an important factor in

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choosing the paste solvent and, as well, the allowable drying time between printing and component placement.

Solder Balling: It is essential that, during reflow, the solder aggregate into a single mass, rather than into multiple, unconnected masses. The propensity for this latter behavior, which can lead to short circuits caused by extraneous bits of solder, is known as solder **balling** and is shown in Figure 11-43. Solder balling [150]) is avoided through the use of paste formulations and reflow processes which (1) have low oxide levels and larger particle size, (2) promote oxide reduction, e.g., through increased flux activity, and (3) remove low-boiling-point solvents prior to reflow and/or reduce the rate of temperature increase to avoid violent solvent boiling. Solder balling is also reduced as the pad metallization becomes more wettable.

Wetting Activity: This paste characteristic refers mainly to the flux within the paste and its activity on pad and component lead metallizations. A common test for wetting activity is a measurement of the spreading of a reflowed pattern on a blank conductor. It is noted [94] that this test may be dominated by properties of the paste, such as viscosity, which are unrelated to the actual wetting; this makes the spreading test more appropriate for monitoring lot-to-lot variations than for absolute comparisons. General wetting and solderability are discussed in section 11.4.3, "Solderabiiity," on page 836.

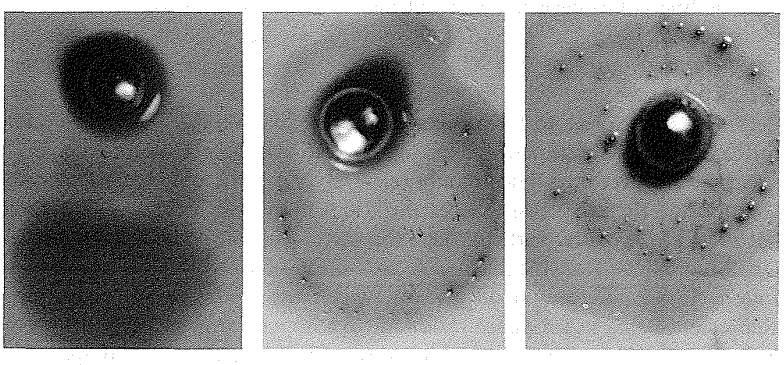


Figure 11-43. Solder-Ball Testing for Solder Paste. (a) Acceptable test result. (b) Questionable test result. (c) Unacceptable solder balling. Courtesy of R. A. Reich, IBM-Austin.

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Void Formation: The number and distribution of voids formed during reflow is shown to be sensitive to reflow process and process parameters [107, 109, 150], boiling point of the solvents [150], paste composition [94], degree of flux activation [150], and conductor-pad metallization [148]. Although the presence of void within a solder joint can affect its mechanical properties, this condition is not normally cited as a critical problem in SMT solder-joint fabrication.

Once the paste is applied, components are placed using a variety of tools, ranging from high-speed/fixed-format machines to low-speed ones having near-robotic flexibility [152]. Currently, the fixed-format tooling, mainly used for passive or low-I/O devices, appears to be relatively mature. It is for high-I/O, finely spaced, leaded devices where vision-enhanced, robotic functions are still evolving, along with the machine configuration.

Vapor Phase Reflow: After populating the board with SMT components and heating the assembly to remove paste solvents and to cure any adhesive used, the solder joints are formed using any of several reflow techniques. The primary approaches include vapor phase reflow, IR reflow, or hot-gas reflow, each of which utilizes a distinct heat transfer mechanism to the panel/component. Vapor phase reflow (VPR), for example, uses the heat of condensation of a perfluorocarbon, having a rather narrow boiling range. To use this technique, the assembly to be reflowed is conveyed into a chamber containing vapor and boiling liquid. The temperature of the assembly rises rapidly to the boiling point of the liquid and is equilibrated at this point. Several different perfluorocarbon materials are commercially available that have boiling points covering much of the range of solder reflow temperatures of interest (~175°-250°C) [153]. A material used commonly in the industry has a boiling point of 215°C. These liquids themselves are quite inert, chemically; however, when exposed to temperatures above the boiling point, they may decompose to form highly corrosive materials. This places some restrictions on the nature of the heaters used to boil the perfluorocarbons. (It also requires that the liquid remain relatively pure to avoid char-coating the heaters, and thereby causing local variations in heat transfer coefficient and hot spots at the heater surface; thus, the perfluorinated liquid is normally filtered to remove flux residues). A schematic of a VPR unit is shown in Figure 11-44. Figure 11-45 gives a typical time-temperature curve for a component being vapor-phase reflowed. An important aspect regarding this type of reflow is the relatively high rate of temperature rise, compared to other techniques. This is an advantage in decreasing cycle time or minimizing total exposure to elevated temperature; however, the problems of thermal shock and inhomogeneous heating may now become important. The problem of thermal shock may affect device reliability but more likely will impact the degree of solder-paste eruption and spattering (as well as the formation of solder balls) due to too rapid organic volatilization. The concern with inho-

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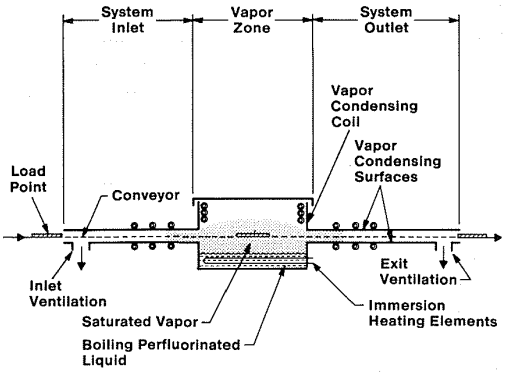


Figure 11-44. Schematic Diagram of Vapor Phase Reflow Unit. After Hall, Ref. [154], courtesy of International Electronics Packaging Society, 1982.

mogeneous heating arises since the heat input into a body to be heated is proportional to the surface area, while the temperature response of the body to a given heat input is governed by its thermal mass. Therefore, two bodies having dissimilar surface-area/thermal-mass ratios will respond differently during reflow. This is manifested in two problem areas for SMT joining: (1) wicking of the solder along the more rapidly heated leads, away from the desired location of the solder fillet, and (2) "tombstoning," whereby solder

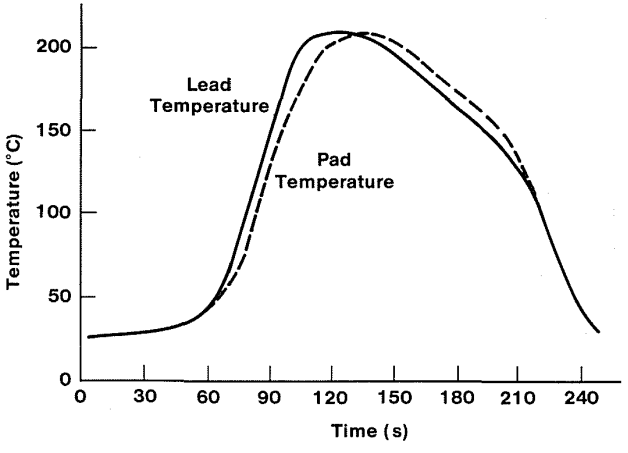


Figure 11-45. Temperature Profile during Vapor Phase Reflow. After Hutchins and King, Ref. [155], 1986, courtesy of International Electronic Packaging Society.

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melting occurs at different times at two points of a sufficiently low mass component that surface tension forces may significantly reposition the component. (The name, in this case, is derived from the look of a passive component, such as a capacitor or resistor, when raised from a horizontal to vertical orientation through the action of surface tension of molten solder at one end). These problems have been overcome through a variety of solutions, including solder-pad design optimization [156], alternative solder and paste preparation [155, 157], and others[158].

Infrared Reflow: The next reflow technique to be considered is infrared (IR) reflow. With this technique thermal energy is supplied via lamps radiating primarily at a given wavelength, usually in the range of 1 to 5 μm. The wavelength for peak IR is controlled by the power input to the lamps. Secondary IR heat sources, or panels, may also be used; these operate at lower temperatures and longer IR wavelengths. At the shortest wavelengths a slight amount of energy is transmitted through the surface of some of the materials, such as epoxy-glass [159]; however, this heating approach is, in its pure form, essentially a line-of-sight surface-heating technique. Plated solder and most of the nonmetallic materials contained in the assemblies to be reflowed are not very reflective at these wavelengths [159, 160]. This allows the board and components to be heated prior to solder-pad reflow, which decreases the degree of solder wicking. A typical time/temperature profile for an IR reflow system is shown in Figure 11-46. Two significant disadvantages are associated with an IR reflow system: (1) the components being irradiated are able to reach quite high temperatures, given the lack of a thermal constraint mechanism of the sort present in VPR system, and (2) the temperature will vary within the assembly in association with local variations in the thermal mass. These factors may lead to difficulties with temperature overshoots or prolonged machine adjustments to accommodate irregular assemblies. One modification that has served to address some of these difficulties is the incorporation of convective heat transfer, along with IR radiation at longer wavelengths [161]; systems are currently commercially available with an advertised convection/IR heat-input ratio of 3:2.

As the ratio of convective to radiative heat transfer increases, this hybrid reflow method begins to approach a hot-gas reflow technique. This technique has been used for small-scale reflow and joining processes, such as rework, and in particular for hot-gas "leveling," a means of solder deposition whereby a layer of molten solder is applied to pads on a circuit board [146, 162]. It has been used with air or nitrogen, although process costs may be significantly increased with the latter. This must be weighed against the reduced degree of oxidation within the assembly when reflow occurs in an inert gas.

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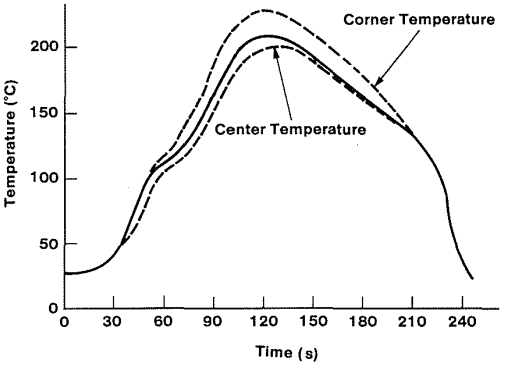


Figure 11-46. Temperature Profile during IR Reflow. After Hutchins and King, Ref. [155], 1986, courtesy of International Electronic Packaging Society.

Laser Reflow: To this point, primarily mass joining techniques have been considered. However, a recent approach using lasers for solder joining [160, 163, 164, 165] has been developed, having somewhat less general areas of application. Laser heat sources demonstrated include a CO_2 (10.6 μm) and a Nd-YAG laser (1.1 μm), which have been used with pretinned or prereflowed parts [160, 165], or with solder paste [163]. The limitation with the technique is the throughput, which ranges from 0.1 to 0.5 s per joint, making this a costly option for many joining applications. However, on the positive side, the rapid solidification rate associated with this approach may produce an intrinsically more fatigue-resistant microstructure than those associated with more slowly cooled reflow techniques (see section 11.4.1, "Solder Microstructure, Deformation, and Failure," on page 819). Another advantage is the ease with which an in situ thermal inspection system to monitor joint quality can be coupled with the laser reflow optics [165], in a manner similar to earlier IR inspection approaches [166].

In summary, regarding solder joining, several approaches are available that have been shown to be sufficiently adaptable to accommodate most, if not all, soldering requirements. It is likely that as long as PTH and SMT components are juxtaposed on many boards, a hybrid or duplex procedure will be used, which is tailored to customized requirements.

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11.4.3 Solderability

Solderability is a relatively practical descriptor for the ease with which a continuous solder bridge can be established between metallized contacts. The formation of this solder joint usually requires (1) removal of oxide or other surface corrosion layer from both metal contacts and solder, (2) flow of the liquid solder along the wettable surfaces, and (3) formation of an intermetallic layer at the solder-to-contact metal interface (this is a beneficial but not a mandatory aspect of solder-joint formation). The first two aspects of the process are briefly considered in this section; the third was discussed in section 11.3.3, "SMT Solder Joints," on page 814.

Flux: The generic term, **flux**, refers to any of a wide range of organic or inorganic chemical mixtures used to facilitate the soldering process. The normal function of flux is to remove surface corrosion layers from the metals to be joined and to promote wetting of the metallic contacts by the solder. A historically predominate class of fluxes is that based on rosin, a steam distillate of pine trees. These rosin fluxes are primarily categorized by their degree of chemical activity for removing the corrosion products (notably copper oxide). There is strong evidence that conventional rosin fluxes do not interact chemically with tin, tin oxide, or other tin and lead compounds [167]. The following groupings are commonly recognized in the United States: (1) R — rosin flux, containing no added activators; (2) RMA — rosin, mildly activated flux, containing a small amount of nonhalide activator, such as organic acids; (3) RA — rosin, activated, containing chemically active compounds, such as organic chlorides (e.g., amine hydrochloride) or inorganic chlorides (e.g., $ZnCl_2$). A large number of fluxes are commercially available that are not rosin-based, and include water-soluble fluxes, entirely synthesized mixtures, and various specialized fluxes. In general, the rosin fluxes consist of 20 to 40% solids carried in an alcohol vehicle, usually isopropanol. The primary constituents of rosin as well as their thermal stability have been analyzed in detail [168]. Rosin consists mainly of abietic acid (80–90%), plus two similar organic acids. This acid has the ability to react with copper oxide or sulfide to form copper abiet but does not react with bare copper. Abietic acid becomes activated above its melting point of 174°C and increases in activity as the temperature is raised until a point is reached at which this activity is irreversibly reduced through chemical breakdown. Rosin may become charred at high temperature, leaving a residue which cannot be removed with conventional techniques. This has motivated the preparation of fluxes using high-boiling-point polymers and "unzippable" polymers [169], which do not char. Other residuals from RMA, RA, or other activated flux may include the chemically active species, such as chlorine, which can induce corrosion in joints or in the electrical devices themselves. This has required that the development of fluxes be coupled with cleaning agents and techniques for re-

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moving all active elements [170]. An extensive study has recently been published that evaluates many commercially available fluxes along with their ability to be removed during cleaning [171]. In this study the nonrosin fluxes chosen exhibited better solderability than the rosin fluxes. A final note on fluxes: soldering applications span a broad range of contact metal and solder (both of which vary in composition, form, and surface condition), reflow time, and temperature. It is therefore necessary to consider the metallic surface layers to be cleaned or deoxidized, the temperature to which the flux will be exposed, and the time during which the flux must spread and perform the surface preparation, before choosing the optimum flux-plus-activator.

Wetting: Wetting is the process by which surface tension causes liquid solder to spread across the solid metal contacts to be joined. The basic aspects of wetting were described almost 200 years ago, given in terms of interfacial energies and wetting angle. The driving force promoting wetting is the overall reduction in interfacial energies, quantities that are normally defined for equilibrium conditions. A recent review of the subject [172] gives many of the practical and fundamental factors, such as surface roughness, temperature, and composition. which may affect the equilibrium of wetting. However, the wetting process is a highly nonequilibrium one, exhibiting complex phenomenology [173] in which the kinetics of flux motion, surface-layer reaction and by-product removal, solder motion, intermetallic formation, etc., require that it be evaluated using transient measurement techniques. Although several techniques are available [174], one general approach has become an accepted starting point for solder-wetting comparisons. This is the use of a modified Wilhelmy Balance test (sometimes called a meniscograph). In this test the forces imposed by a molten solder bath onto a metallic test specimen (e.g., plate or wire, usually prefluxed) are measured with time, as the specimen is dipped into and held in the bath. A diagram of the force versus time curve obtained during a wetting experiment is shown in Figure 11-47, which indicates the stages of the wetting process. First, a buoyancy force (<0) is observed, arising from the displacement of the molten solder by the specimen and from forces associated with nonwetting. After a short time the buoyancy forces are reduced as wetting begins. As wetting proceeds, the force becomes more positive, indicating, qualitatively, the wettability of the contact metal/flux/solder system. Attempts continue to be made to evaluate the wetting process more quantitatively from this sort of experiment, using parameters such as the overall weight change, rate of weight change and/or time to an equilibrium weight change [86, 174, 175, 176, 177, 178, 179]. In general, the precision of these efforts is limited by the lack of detailed analytical work to determine the physical properties, chemical reactions, and physical mechanisms that impact the wetting processes, although comparative evaluations, e.g., for varying solder compositions [177], are effective.

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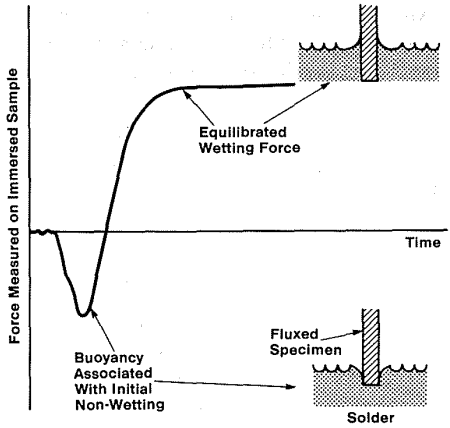


Figure 11-47. Meniscograph Testing for Solderability.

Lead and Contact Conditions: The conditions of the leads and contacts to be joined are two elements that may independently dominate solderability. Although the package leads, particularly of SMT devices, are most often solder-dipped with eutectic or near-eutectic solder, many other as-plated or tinned preparations are also used. Because the packages are commonly subjected to more stringent burn-in conditions (higher temperature, longer time) than the unpopulated or populated boards, the solderability of packages is normally a key manufacturing issue. Furthermore, the package leads must be formed prior to burn-in, thereby subjecting the relatively brittle, protective, plated layers to large plastic strains. This can lead to unacceptable cracking in these layers, whose integrity is necessary to prevent localized pitting or corrosion during subsequent processing [103]. A screening procedure is often used to evaluate the solderability of incoming packages; frequently the evaluation test used is the meniscograph tester [175, 180], described previously. This screening approach is used to gauge, for groups of incoming packages, the immediate solderability or the projected solderability after an extended holding period prior to joining [175, 181]. It is argued, for example, that a 20- to 24-hour period of steam aging generates the same relative decrease in solderability as does a year of storage under typical conditions [182]. Other aging conditions, having different time, temperature, and relative humidity are also advocated [86]. Given the range of lead frame materials, protective plated layers, and solder coatings, a single screening procedure, having mechanistic validity, will necessarily have a limited range

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of applicability. It should be noted that, although solder dipping of package leads is often chosen as a technique to promote solderability this can have a substantial adverse impact on device reliability [142, 183], mainly through thermally induced polymer-to-leadframe delamination. Two other issues that may influence the choice of lead coating are (1) tin-whisker formation [184, 185] in plated tin, which may cause shorting during operations preceding general reflow, such as burn-in, and (2) dewetting [181], caused by gas evolution from constituents within the plated layer.

Boards, on which packaged chips are joined, are also prepared in many ways. The board contacts may be bare, chemically treated, solder-paste-coated, solder-plated, tinned, solder-leveled, reworked, etc. In recent years it has been argued that for presoldered boards, a minimum solder thickness of about 8 μm of solder is necessary, with a tin concentration near the eutectic composition, for optimized solderability (see [86, 186]). For thinner solder layers growth of the copper–tin intermetallic layer will deplete the solder of tin, thereby reducing wettability. Furthermore, this condition promotes the formation of the Cu_3Sn intermetallic, rather than the much more solderable Cu_6Sn_5 (see earlier discussions on intermetallic formation). Exposure of the intermetallic layer to oxidation can seriously reduce solderability [186], expecially for rework operations; this again favors increased solder thickness.

11.5 EVOLVING INTERCONNECTION APPROACHES

Several new concepts for package-to-board interconnections are finding increasing application. These include elastomeric interconnections and electrically conductive adhesives, and are briefly described in this section.

Pressure Interconnections: This interconnection approach is being applied to an increasingly broad range of structures. The initial, major implementation utilized a filled elastomeric interposer as an interconnection for digital-watch display applications. This connector, which commonly consists of a thin block of silicone rubber with alternating pure rubber and conductor-filled (usually with graphite) rubber layers, is pressed between package leads and board contacts. Given the relatively high electrical resistance of this solderless connection, it is best suited for low-current applications, such as LCD displays. Other, lower-resistance, metal-filled or metal-coated elastomeric interposers are also commercially available (see, e.g., [188, 189]). In these metal/elastomer designs the elastomer provides the support, spring, and sealing action. Contact resistance of the elastomeric connectors depends mainly on the contact size, the thickness of the anisotropic sheet, and the resilience of the elastomer. A primary concern is the amount of pressure required to achieve acceptable resistance levels, and eventual relaxation of the elastomer core. Figure 11-48 shows several of the generic forms of pressure interconnections used commercially.

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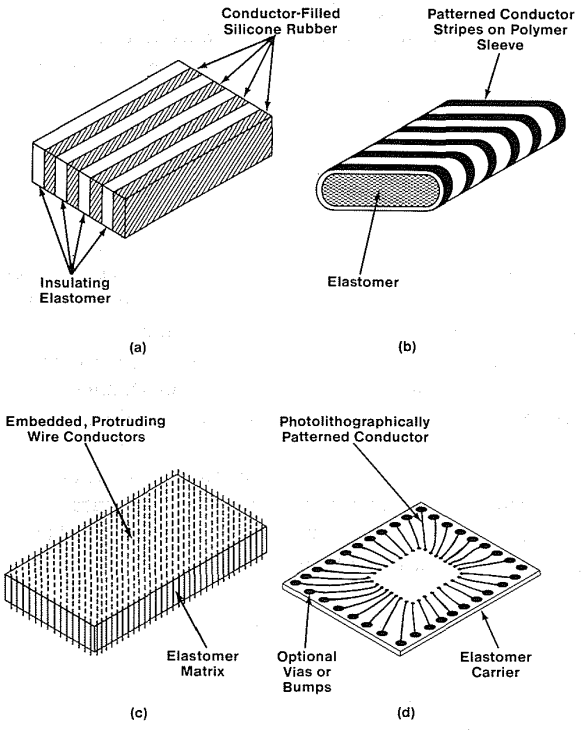


Figure 11-48. Generic Forms of Pressure Interconnections.

Beyond the relatively straightforward structures in current use, which are essentially anisotropically conducting interposers, a new method of providing pressure-induced conduction has been reported [187]. In this case, an interposer is prepared which is homogeneously filled with small, conductive particles. Through careful control of the volume fraction of metal particles, as well as conductive length, a uniformly doped composite can be conductive when the distance between two points is below the percolation threshold. On the other hand, when the distance between two points is increased beyond this given distance, the electrical resistance increases by several orders of magnitude; this is shown in Figure 11-49. This approach to pressure interconnection shows potential for certain high-density packaging applications.

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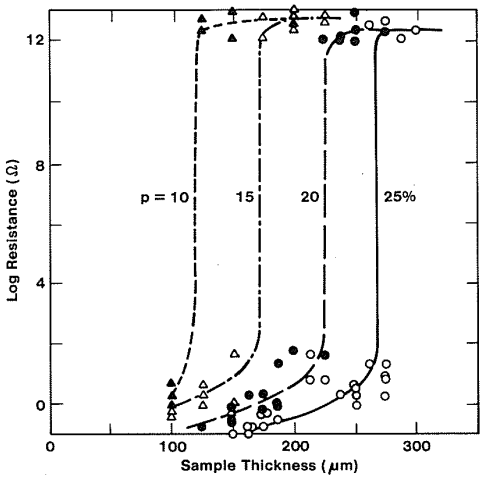


Figure 11-49. Resistance vs. Conductor Length for New Pressure Interconnection. The interconnection structure consists of a silicone rubber elastomer in which is embedded silver-coated glass spheres having a diameter of 25 μm. The electrical resistance is measured through the thickness at a particle loading given as that percentage of the fully conductive loading (percolation threshold). After Etemad et al., Ref. [187], 1986.

Conductive Adhesives: Another approach to package/board interconnection is the use of conductive adhesives. The primary approach, which has received limited application during the last several years, is the use of an organic carrier (usually epoxy) containing conducting, metallic particles (usually silver). With this technique a one- or two-component paste is mixed and applied to a circuit board using a patterned stencil or a dispensing nozzle approach. The component is attached and the organic is cured, usually at a temperature less than 200°C. As-cured bulk resistivities are available in the range of 10^{-5} to 10^{-6} Ω·m, a value which allows sufficiently low interconnection resistance to be acceptable for virtually all packaged devices. An argument that strongly supports the use of a conductive adhesive with respect to solder is the reduction in the number of process steps necessary to form the interconnection. The major argument against it has been the cost of the material, primarily arising from the cost of the silver, which is commonly chosen for increased resistance stability. Other conductive fillers (e.g., *Ag-Pd* or *Cu*) are potentially available that would reduce this concern; however, these materials are in the early stages of evaluation. Another positive aspect of this

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Table 11-4. Conducting Polymers. After Reynolds, Ref. [190], reprinted by permission of John Wiley and Sons, Inc.

Polymer	Resistivity (Ω·m)
Polyacetylene	10^{-5}
Poly(p-phenylene)	10^{-5}
Poly(p-phenylene vinylene)	10^{-5}
Poly(p-phenylene sulfide)	10^{-4}
Polypyrrole	10^{-4}
Polythiophene	10^{-4}
Polyfuran	10^{-4}
Polyazulene	10^{-2}
Polyaniline	10^{-2}
Poly (1,6-heptadiyne)	10^{-1}

class of conductive adhesives is the generally successful (although not universal) "wetting," behavior for most interconnection pads and leads.

Another similar but rather more advanced approach to package/board interconnection is the use of conductive organics, of the sort listed in Table 11-4. The limitations with many of these materials with regard to resistivity, thermal stability, or stability in air have prevented their serious industrial consideration; however, given the potentially low resistivity [190], they show promise as new polymeric blends or composite materials are introduced.

11.6 REFERENCES

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