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Peter Elenius

Work Experience

April 2002 – Present E&G Technology Partners Young, AZ

Managing Partner

Development of comprehensive strategies to protect the Intellectual Property (IP) of clients.
Consulting with clients in the selection of IC packaging technologies from solder bumping through assembly.
Development of advanced packaging technologies and processes for clients.
Providing failure analysis and corrective actions for flip chip and WLP related issues ranging from the IC's final metal through assembly.
Expert witness for semiconductor packaging IP issues.

April 2012 – Present Options for Boomers Young, AZ

Managing Partner

Expert witness for semiconductor packaging IP issues.
Residential on-grid and off-grid solar system design, procurement, installation support and maintenance.
Cattle ranching and beef sales to consumers.

July 2022 – Present Revolution Auto Parts & Hardware Young, AZ

Managing Partner

Retail auto parts and hardware store.

2008 – December 2014 OptoPAC, Inc Oksan-Myun, Korea

Executive Advisor - May 2011 to December 2014

Client of E&G Technology Partners
Market development responsibilities for USA and European customers.

Vice President and CTO - March 2008 to April 2011

Client of E&G Technology Partners
Lead all R&D in image sensor packaging and future technologies.
Established and managed IP strategy for the company.

March 1996–Mar 2002 Flip Chip Technologies, LLC Phoenix, AZ
(became Flip Chip International in 2003)

Vice President Technology and CTO - 1997 to Mar 2002

Led all R&D in Flip Chip (FC) Bumping, WLP and future technologies.
Established and managed IP strategy for the company. This included the licensing of the IP to major semiconductor and IC assembly companies.
Recognized world-wide as industry expert in both FC Bumping and WLP technologies and their associated assembly processes.
Instrumental in growing Flip Chip Technologies to a 60% share of the foundry market for both FC bumping and WLP technologies.

Vice President Marketing and Sales - 1996

Developed initial marketing and sales strategies for Flip Chip Technologies

January 1995 – March 1996 Kulicke and Soffa, Industries Willow Grove, PA
Flip Chip Product Manager

Launched K&S's first flip chip placement equipment to the market
Lead role in the team that formed Flip Chip Technologies, LLC as a JV with Delco Electronics. Included negotiation of the IP that was transferred from Delco Electronics as part of the JV.

July 1982 – December 1994 IBM Microelectronics East Fishkill, NY

Advisory Engineering Manager Poughkeepsie, NY

Responsible for all flip chip equipment and process engineering for 100 to 121 flip chip devices in Multi Chip Modules used in IBM mainframes.

Staff Engineering Manager Manassas, VA

Flip chip equipment and process engineering for module assembly process
Test engineering manager for custom MCM test equipment development

Staff Engineer East Fishkill, NY and Manassas, VA

Responsible for the design, development and process engineering of flip chip placement equipment used to assemble single and multi-chip modules.

Education

1989–1990 University of Wisconsin - Madison Madison, WI

Master of Science in Manufacturing Systems
Selected by IBM for this program and remained full time IBM employee

1977–1982 University of Wisconsin - Madison Madison, WI

Bachelor of Science in Mechanical Engineering

Industry Activities

1998-2001

Semiconductor Research Corporation

Active in the Packaging and Nanostructures & Integration Sciences (NIS)
Served as Vice Chair of NIS in 2000 and Chair of NIS in 2001

1999-2001

International Technology Roadmap for Semiconductors (ITRS)

Active in the Packaging and Assembly Technical Working Group

2000-2013

IMAPS Flip Chip Workshop and Device Packaging Conference

General Chair & organizer for first IMAPS FC Workshops from 2000-2002
Technical Chair for 2011 Device Packaging Conference
General Chair for 2012 Device Packaging Conference
Received the IMAPS President's Award in 2013

2001-present

IEEE Paper Reviewer

Review of refereed papers for IEEE Transactions on Electronics Packaging
Manufacturing, IEEE Transactions on Electronics Packaging Manufacturing,
and IEEE Transactions on Advanced Packaging.

Expert Witness

Litigation Experience

Depositions – 12
ITC Trial Testimony – 3

Federal District and ITC Experience

1. Tessera Inc. v. Elpida Memory Inc. (Japan) & Elpida Memory Inc. (U.S.A.)
Investigation No. 337-TA-630, U.S. International Trade Commission.,
Washington, D.C., Retained by Foley & Lardner LLP, Washington DC, March
2008-October 2008 for the respondents. Prepared initial and rebuttal non-
infringement expert reports. Was deposed once and testified at trial.
Disposition: After the trial the Administrative Law Judge, U.S. ITC Commission,
Federal District and Supreme Court found no violation of section 337 by
respondents.
2. Tessera Inc. v. Advanced Semiconductor Engineering (Taiwan), Silicon
Precision Industries Limited (Taiwan) & ChipMOS (Taiwan); collectively
Respondents. Investigation No. 337-TA-649, U.S. International Trade
Commission., Washington, D.C., Retained by Orrick, Herrington & Sutcliffe,
LLP, Menlo Park, CA, February 2009 for the respondents. Prepared expert
report on invalidity. Disposition: Tessera withdrew the litigation just prior to
submission of the completed initial expert report.
3. UPEK Inc. v. AuthenTec Inc., Case No. 5:10-CV-00424-JF-PAT, U.S. District
Court, Northern District of California, San Jose Division. Retained by Orrick,
Herrington & Sutcliffe, LLP, Menlo Park, CA. February 2010 – March 2010.
Patent litigation for the Plaintiffs. Hired to provide expert technical advice
concerning semiconductor packaging technology; filed one declaration and
expected to testify regarding early summary judgment motions filed by
AuthenTec attacking the patent and the infringement claims that UPEK had
asserted. AuthenTec's motions were denied without a hearing. The case was
later dismissed when the parties merged.

4. Freescale Inc. v. Panasonic Corporation (Japan) and Panasonic Corporation of North America, Investigation No. 337-TA-709, U.S. International Trade Commission., Washington, D.C., Retained by White & Case LLP, Washington DC, May 2010-January 2011 for the respondents. Prepared invalidity and non-infringement expert reports and a supplemental expert report regarding invalidity. Was deposed one time. Disposition: Prior to the trial the parties settled with a favorable outcome for respondents.
5. Altera Corporation v. LSI Corporation et al., Case No. 4:11-cv-03139-CW, U.S. District Court, Northern District of California, San Jose Division. Retained by Morrison & Foerster LLP, Palo Alto, CA, July 2011-December 2011 for the plaintiffs. Patent Litigation. Prepared invalidity, infringement and non-infringement expert reports. Was deposed one time. Disposition: Prior to the trial the parties settled with a favorable outcome for the plaintiffs.
6. Knowles Electronics LLC. v. Analog Devices Inc. Case No. 1:11-cv-06804, U.S. District Court, Northern District of Illinois, Eastern Division, Retained by Covington & Burling, Washington DC, March 2012 for the complainant. Prepared initial and rebuttal expert reports on claim construction. Was deposed one time. Disposition: Prior to the trial the parties settled with a favorable outcome for the plaintiff.
7. Knowles Electronics LLC. v. Analog Devices Inc. Investigation No. 337-TA-825, U.S. International Trade Commission., Washington, D.C., Retained by Covington & Burling, Washington DC, March 2012 for the complainant. Prepared initial and rebuttal expert reports on claim construction, priority date, infringement, domestic industry, and copying. Was deposed two times and testified two times. Disposition: Prior to the ALJ's initial determination the parties settled with a favorable outcome for the plaintiff.
8. Powertech Technology Inc. v. Tessera, Inc. Case No. 4:11-cv-06121-CW, U.S. District Court, Northern District of California, Oakland Division., Retained by Baker Botts LLP, December 2012 for Powertech Technology. Contract Litigation. Prepared initial and rebuttal expert reports on technical aspects of contract, business practices and prior litigation in ITC-630 and was deposed one time. Disposition: Prior to the trial the parties settled with a favorable outcome for plaintiff.
9. Infineon Technologies Austria AG v. Volterra Semiconductor Corporation and Volterra Asia PTE. LTD. Case No. 2:13-cv-684, U.S. District Court, Eastern District of Texas, Marshall Division. Retained by Baker Botts LLP, July 2014 for Infineon Technologies. Prepared three declarations regarding claim construction and was deposed one time. Disposition: Prior to the trial the parties settled with a favorable outcome for plaintiff.
10. Infineon Technologies Austria AG v. Volterra Semiconductor Corporation. Case No. 3:11-cv-11-06239, U.S. District Court, Northern District of California, San Francisco Division. Retained by Baker Botts LLP, July 2014 for Infineon Technologies. Began analysis of products to show infringement in preparation for expert report(s) and testimony. Disposition: Prior to the trial the parties settled with a favorable outcome for plaintiff.
11. Tessera, Inc v. Toshiba Corporation. Case No. 5:15-cv-02543 U.S. District Court, Northern District of California, San Jose Division. Retained by Baker Botts, LLP, October 2015 for Toshiba Corporation. Submitted rebuttal expert report. In March 2020 the case was settled with a favorable outcome for Toshiba.

12. ON Semiconductor Corporation and Semiconductor Components Industries, LLC v. Power Integrations, Inc. Case No. 1:17-cv-00247-LPS U.S. District Court for the District of Delaware. Retained by Shaw Keller LLP, December 2018 for Power Integrations. Submitted three expert reports and was deposed one time. Disposition: This case and several others were settled in October 2019 on very favorable terms for Power Integrations.
13. Bell Semiconductor, LLC v. Texas Instruments, Inc. Case No 2:20-cv-00048-JRG U.S. District Court for the Eastern District of Texas, Marshall Division. Retained by Skiermont Derby LLP, April 2020 for Bell Semiconductor. Infringement expert report was ready to be submitted when case settled in March 2021.
14. MyPAQ Holdings Ltd. v. Samsung Electronics Co., Ltd. et al. Case No. 6:21-cv-00398-ADA (W.D. Tex.). Retained by Baker Botts, September 2021 for Samsung Electronics. This case was dismissed based on results of (IPR Experience #13) Patent Trial and Appeal Board finding that all the challenged claims were unpatentable.
15. Katana Silicon Technologies v. GlobalFoundries, Inc. Case No AU:22-CV-00852-RP, U.S. District Court for the Western District of Texas, Austin Division. Retained by Carter Arnett PLLC, August 2022 for Katana Silicon Technologies. A declaration and infringement expert report were submitted. Was deposed one time. Case settled in April 2025.

IPR Experience

1. U.S. Patent 6,747,350 re-exam application 95/001,551. Retained by Jones Day LLP, July 2011 and Slater & Matsil LLP, May 2012 for Xilinx, Inc. Prepared two declarations. Disposition: Xilinx achieved a favorable outcome as the result of Case No. 5:11-cv-00671 and Case No. 5:11-cv-04407, U.S. District Court, Northern District of California, San Jose Division.
2. U.S. Patent 6,969,915, AIA Review # IPR2017-00843. Retained by Slater & Matsil LLP, January 2017 for Xilinx, Inc. Prepared one declaration. Patent owner filed a Statutory Disclaimer prior to the institution of a trial for the five claims in question and the IPR was terminated in May 2017.
3. U.S. Patent 6,653,731, AIA Review # IPR2017-00844. Retained by Slater & Matsil LLP, January 2017 for Xilinx, Inc. Prepared one declaration. Patent owner filed a Statutory Disclaimer for the claim in question and the IPR was terminated in October 2017.
4. U.S. Patent 7,102,211, AIA Review # IPR2018-00399. Retained by Shaw Keller LLP, December 2017 for Power Integrations, Inc. Prepared one declaration. Petition filed 1/04/2018.
5. U.S. Patent 7,389,905, AIA Review # IPR2018-00524. Retained by Morrison & Foerster LLP, August 2017 for Xilinx, Inc. Prepared one declaration. Petition filed 1/25/2018. The parties settled their litigation and terminated this IPR, July 2018 through a Settlement and License Agreement for a nominal amount.
6. U.S. Patent 6,935,548, AIA Review numbers IPR2018-00525 and IPR2018-00526. Retained by Morrison & Foerster LLP, August 2017 for Xilinx, Inc. Prepared one declaration. Petition filed 1/25/2018. The parties settled their litigation and terminated this IPR, July 2018 through a Settlement and License Agreement for a nominal amount.

7. U.S. Patent 6,354,479, AIA Review numbers IPR2018-00527 and IPR2018-00527. Retained by Morrison & Foerster LLP, August 2017 for Xilinx, Inc. Prepared one declaration. Petition filed 1/25/2018. The parties settled their litigation and terminated this IPR, July 2018 through a Settlement and License Agreement for a nominal amount.
8. U.S. Patent 6,566,167, AIA Review number IPR2018-01266. Retained by O'Melveny & Myers LLP, March 2018 for Samsung Electronics. Prepared one declaration. Petition filed 6/15/2018. The parties settled their litigation and terminated this IPR, December 2018.
9. U.S. Patent 6,825,554, AIA Review numbers IPR2018-01267. Retained by O'Melveny & Myers LLP, March 2018 for Samsung Electronics. Prepared one declaration. Petition filed 6/15/2018. The parties settled their litigation and terminated this IPR, December 2018.
10. U.S. Patent 8,049,340, AIA Review number IPR2020-01692. Retained by Skiermont Derby, April 2021 for Bell Semiconductor. Prepared one declaration which was filed 2/17/2021. The parties settled their litigation and terminated this IPR, April 2021.
11. U.S. Patent 8,288,269, AIA Review number IPR2021-00147. Retained by Skiermont Derby, April 2021 for Bell Semiconductor. Prepared one declaration which was filed 2/17/2021. The parties settled their litigation and terminated this IPR, October 2021.
12. U.S. Patent 8,049,340, AIA Review number IPR2021-00148. Retained by Skiermont Derby, April 2021 for Bell Semiconductor. Prepared one declaration which was filed 2/17/2021. The parties settled their litigation and terminated this IPR, October 2021.
13. U.S. Patent 7,403,399, AIA Review Number IPR2022-00307. Retained by Baker Botts, September 2021 for Petitioner Samsung Electronics, challenging claims asserted by MyPAQ Holdings. Prepared one declaration which was filed December 2021 and was depose one time. Patent Trial and Appeal Board found that all the challenged claims are unpatentable.
14. U.S. Patent RE38,806, AIA Review Number IPR2023-00071. Retained by Carter Arnett PLLC, August 2022 for Patent Owner Katana Silicon Technologies vs Petitioner Micron Technology. Prepared one declaration. Patent Trial and Appeal Board decided to institute an inter partes review, with one Administrative Patent Judge dissenting.
15. U.S. Patent 7,402,903, AIA Review Number IPR2022-01083. Retained by Carter Arnett PLLC, August 2022 for Patent Owner Katana Silicon Technologies vs Petitioner GlobalFoundries. Prepared one declaration. Patent Trial and Appeal Board decided to not institute an inter partes review.
16. U.S. Patent RE38,806, AIA Review Number IPR2023-00071, IPR2023-00072 and IPR2023-00073. Retained by Carter Arnett PLLC, August 2022 for Patent Owner Katana Silicon Technologies vs Petitioner Micron Technology. Prepared three declarations and was depose one time. Patent Trial and Appeal Board found the cited claims were unpatentable.
17. U.S. Patent 6,731,013, AIA Review Number IPR2023-00105. Retained by Carter Arnett PLLC, August 2022 for Patent Owner Katana Silicon Technologies vs Petitioner Micron Technology. Prepared one declaration. Patent Trial and Appeal Board decided not to institute an inter partes review.

Patents

Issued United States of America Patents

1. US5373893 - Method and apparatus for cooling thermally massive parts in a continuous furnace
2. US5397604 - Non-contact fluid applicator apparatus and method
3. US5838545 - High performance, low-cost multi-chip module package
4. US6287893 - Method for forming chip scale package
5. US6441487 - Chip scale package using large ductile solder balls
6. US6578755 - Polymer collar for solder bumps
7. US6750135 - Method for forming chip scale package
8. US7057292 - Solder bar for high power flip chips
9. US7118833 - Forming partial-depth features in polymer film
10. US7126164 - Wafer-level moat structures
11. US7485812 - Single or multi-layer PCB with improved via design
12. US8141245 - Single or Multi-Layer PCB with improved via
13. US8487437 – Electronic Device Package and Method for Fabricating the same

Publications

Partial list of Publications

1. "Rework of Wire Bonded Devices on MCMs," Multichip Modules, 1994. Proceedings of the 1994 International Conference on, pp.61-66, 13-15 Apr 1994
2. "Au Bumped Known Good Die," Electro/94 International. Conference Proceedings. Combined Volumes. pp.820-825, Boston 10-12 May 1994
3. "Flex on Cap-Solder Paste Bumping," Advanced Packaging Materials. Proceedings., 3rd International Symposium on, pp.115-116, 9-12 Mar 1997
4. "Flex on cap-solder paste bumping," Electronic Components and Technology Conference, 1997. Proceedings., 47th, pp.248-253, 18-21 May 1997
5. "Flip Chip Solder Bumping Using Solder Pastes," IEMT/IMC Symposium, 1997., 1st Joint International Electronic Manufacturing Symposium and the International Microelectronics Conference, pp.116-121, 16-18 Apr 1997
6. "Wafer Bumping Technologies – A Comparative Analysis for Solder Deposition Processes and Assembly Considerations", INTERPack '97, EEP-Vol. 19-1, Advances in Electronic Packaging – 1997, ASME 1997, pp. 337-351.
7. "Flip Chip Bumping for IC Packaging Contractors", Flip Chip Technologies White Paper, March 1998.
8. "A Comparative Analysis – Solder Deposition Process and Assembly Wafer Bumping – Part I", EPP Printed Circuit Board, March 1998, pp. 40-41.
9. " A Comparative Analysis – Solder Deposition Process and Assembly Wafer Bumping – Part II", EPP Printed Circuit Board, May 1998, pp. 30-36.
10. " A Comparative Analysis – Solder Deposition Process and Assembly Wafer Bumping – Part III", EPP Printed Circuit Board, August 1998, pp. 29-31.
11. "Flex-On-Cap Solder Bump for Manufacturability and High Reliability", IMAPS Nordic '98, Stockholm, 20-23 September, 1998.
12. "Reliability of Fine Pitch Solder Bump Flip-Chip-on-Flex: Design and Assembly Techniques, Part 1", GlobalTRONICS 1998, Singapore, 5-9 October, 1998.

13. "The Ultra CSP Wafer Scale Package," Electronics Packaging Technology Conference, 1998. Proceedings of 2nd, pp.83-88, 8-10 Dec 1998
14. "Ultra CSP: A Wafer Level Package," Advanced Packaging Materials: Processes, Properties and Interfaces, 1999. Proceedings. International Symposium on, pp.241-245, 14-17 Mar 1999
15. "Recent Advances in Flip Chip Wafer Bumping using Solder Paste Technology," Electronic Components and Technology Conference, 1999. 1999 Proceedings. 49th, pp.260-265, 1999
16. "Electron Microscopy Study of Interfacial Reaction Between Eutectic SnPb and Cu/Ni(V)/Al Thin Film Metallization," Journal of Applied Physics, vol.87, no.2, pp.750-754, Jan 2000
17. "Ultra CSP Bump on Polymer Structure," Advanced Packaging Materials: Processes, Properties and Interfaces, 2000. Proceedings. International Symposium on, pp.211-215, 2000
18. "Ultra CSP – A Wafer Level Package," Advanced Packaging, IEEE Transactions on, vol.23, no.2, pp.220-226, May 2000
19. "Flip Chip Processing of Lead-free Solders and Halogen-free High Density Microvia Substrates," Electronic Components and Technology Conference, 2000. 2000 Proceedings. 50th, pp.1101-1105, 2000
20. "Reliability Characterization in Ultra CSP Package Development," Electronic Components and Technology Conference, 2000. 2000 Proceedings. 50th, pp.1376-1383, 2000
21. "Solder Bars - A Novel Flip Chip Application for High Power Devices," Electronic Components and Technology Conference, 2000. 2000 Proceedings. 50th, pp.697-701, 2000
22. "Comparing Flip-Chip and Wire-Bond Interconnect Technologies," Chip Scale Review, July-August 2000
23. "Lead Free Solder for Flip Chips," Proceedings of the 37th IMAPS Nordic Conference, Helsingor, Denmark, 10-13 September, 2000, pp. 117-112.
24. "Lead-free Flip Chip Processing with Halogen-free High Density Microvia Substrates," Electronics Manufacturing Technology Symposium, 2000. Twenty-Sixth IEEE/CPMT International, pp.263-269, 2000
25. Co-author "Chapter 2 - Wafer Bumping", Area Array Interconnection Handbook", Kluwer Academic Publishers, 2001 pp. 770-81
26. "A Polymer Reinforced WLP / Why It Has Superior Solder Joint Reliability", IMAPS 2001 – Baltimore 10/15/2001
27. "WLP Technology Fiction Reality and Potential" - *SECAP Asia Series* 11/4 to 11/15/2001
28. "Current-Crowding-Induced Electromigration Failure in Flip Chip Solder Joints," *Applied Physics Letters*, vol.80, no.4, pp.580-582, Jan 2002
29. "Wafer Level Packaging", *APACK Keynote Address* Singapore 12/5/2001
30. "WLP Technology" - Keynote Address at The International Conference of Advanced Electronic Manufacturing Technology and Equipment in Shanghai
31. "Flex-On-Cap Solder Bump for 300mm Wafer", Semicon Singapore 2002

32. "Solder Joint Reliability and Characteristics of Deformation and Crack Growth of Sn-Ag-Cu vs Eutectic Sn-Pb on a WLP in a Thermal Cycling Test" *Electronics Packaging Manufacturing, IEEE Transactions on*, vol.25, no.2, pp. 84- 90, Apr 2002
33. "Interfacial Microstructure Evolution Between Eutectic SnAgCu solder and Al/Ni(V)/Cu thin films," *J. Mater. Res.*, 17, 1612-1621 (2002)
34. "Packaging Assessment of Porous Ultra Low-k Materials", *Interconnect Technology Conference, 2002. Proceedings of the IEEE 2002 International*, pp. 113-115, 2002
35. "Electromigration of Flip Chip Solder Bump on Cu/Ni(V)/Al Thin Film Under Bump Metallization," *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, pp. 1201- 1205, 2002
36. "Direct Bump-on-Copper Process for Flip Chip Technologies," *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, pp. 704-710, 2002
37. "Flip-Chip Reliability: Comparative Characterization of Lead Free (Sn/Ag/Cu) and 63Sn/Pb Eutectic Solder", *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, pp. 1263- 1269, 2002
38. "Solder Joint Reliability of a Polymer Reinforced Wafer Level Package", *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, pp. 1347- 1354, 2002
39. "Flip Chip Solder Bumping Compatibility on Cu / Low-k Devices", *IMAPS Flip Chip 2003 Workshop*, June 16-18, 2003
40. "Wafer-Level: Advanced Packaging Technology", *Semiconductor International*, February 2004
41. Post-Passivation Layers: Device Enhancement At The Wafer Level, *Pan Pacific 2004*, February 2004
42. "Advanced Wafer-Level Cleaning for Advanced WLP and Flip Chip", *IMAPS Flip Chip 2004 Workshop*, June 21-24, 2004
43. "Evolution of Wafer-level Packaging", *Advanced Packaging Magazine*, July 2004
44. "Where Does 3D IC Packaging Fit" – *Peaks in Packaging 2005* – Whitefish, MT
45. "Wafer Level Packaging Past, Present and Future", Invited presentation for *Wafer Level Packaging Executive Forum at ICEPT-HDP Xian, China 2010*.
46. "Flip Chip and Wafer Level Packaging - Past, Present and Future", Invited Keynote for IMAPS Device Packaging Conference, Fountain Hills AZ, March 8-10, 2011.
47. "Flip Chip for Image Sensor Packaging", IMAPS Device Packaging Conference, Fountain Hills AZ, March 8-10, 2011.

Clients

Semiconductor Clients from 2015 thru 2025

Bell Semiconductor
Boston Scientific
CoreSEM
Honeywell
IEM
Infineon
Johnstech
Katana Silicon Technologies
Knowles
Kulicke and Soffa Industries
Melexis
Microsemi
OptoPAC
Panasonic
Powertech Technology Inc.
Power Integrations
Samsung Electronics
Toshiba
Xilinx