

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.

Petitioners

v.

TOPWIRE LLC,
Patent Owner

Case No. IPR2026-00324
U.S. Patent No. 9,859,202

DECLARATION OF PETER ELENIOUS

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Declaration of Peter Elenius

I. INTRODUCTION

1. I, Peter Elenius, make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

2. I have been retained by counsel for Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Samsung” or “Petitioners”) in connection with the above-captioned request for *inter partes* review of claims 1–9 of U.S. Patent No. 9,859,202 (the “’202 Patent”), entitled “Spacer Connector,” by named inventor Dyi-Chung Hu. I understand that the ’202 Patent is assigned to Topwire LLC (the “Patent Owner”). I have been asked to provide technical review, analysis, insights, and opinions regarding the ’202 Patent and the prior art references that form the basis for the grounds of invalidity set forth in the Petition for *inter partes* review of the ’202 Patent (the “Petition”). This declaration is a statement of my opinions on issues related to the unpatentability of claims 1–9 of the ’202 Patent.

3. I am being compensated at my normal rate, plus reimbursement for expenses, for my analysis. My compensation does not depend on the content of my opinions or the outcome of this proceeding. I have no other interests in this proceeding or with Petitioners or Patent Owner.

II. EXPERIENCE AND QUALIFICATIONS

4. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae, which has been provided as EX1030. Here, I provide a brief summary of my qualifications and relevant information regarding my education, technical experience, and publications.

5. I have forty-four years of experience in semiconductor packaging technology. I am presently the Managing Partner of E&G Technology Partners (“E&G”). As Managing Partner at E&G, I provide technology and business consulting services for the advanced integrated circuit (IC) packaging industry.

6. From March 1996 to March 2002, I was Vice President of Technology and CTO for Flip Chip Technologies LLC. From January 1995 to February 1996, I was the Flip-Chip Product Manager for Kulicke and Soffa Industries Inc. From July 1982 to December 1994, I worked for IBM Inc. in the areas of flip-chip equipment and process engineering with my last position being an Advisory Engineering Manager.

7. I am the co-inventor of thirteen United States patents, all related to semiconductor packaging technology.

8. I am the author and co-author of forty-six technical publications, all related to semiconductor packaging technology.

9. I am currently a member of the Institute of Electrical and Electronic Engineers (IEEE) and the International Microelectronic and Packaging Society (IMAPS). I am also a member of the IEEE Electronics Packaging Society.

10. I have been an invited speaker at many semiconductor industry conferences and have taught short courses related to both flip chip and wafer level packaging at conferences and corporations. From 2000-2002, I was the General Chair for the first IMAPS Flip Chip Workshops. In 2012, I was the General Chair for the IMAPS Device Packaging Conference.

11. I have worked on a wide variety of semiconductor packages throughout my career, including Package on Package (POP) devices in the 2004 to 2018 time period.

12. I received my Bachelor of Science degree in mechanical engineering from the University of Wisconsin, Madison in 1982. I received my Master of Science degree in manufacturing systems from the University of Wisconsin, Madison in 1990.

13. My analyses set forth in this declaration are informed by my experience in the field of semiconductor packaging. Based on my above-described experience, I am an expert in the field relevant to the '202 Patent at issue here and have been an expert in the relevant field since before the claimed priority date of the '202 Patent. I am familiar with how a person of ordinary skill in the art ("POSITA") would have

understood and used the terminology found in the '202 Patent before and at the time of its filing.

III. MATERIALS CONSIDERED

14. The analysis that I provide in this declaration is based on my education and professional experience, as well as the documents I have considered, including the '202 Patent (EX1001) and its prosecution history (EX1002). I have reviewed and am familiar with the specification of the '202 Patent. I have reviewed and am familiar with the prosecution history of the '202 Patent.

15. In preparing this declaration, I have also reviewed and am familiar with the following prior art used in the Petition and this declaration. I have considered the following documents, and have also considered any other documents that are otherwise discussed in this declaration:

Exhibit	Description of Documents
EX1001	U.S. Patent No. 9,859,202
EX1002	Prosecution History of U.S. Patent No. 9,859,202
EX1003	Declaration of Peter Elenius in support of petition for <i>inter partes</i> review of U.S. Patent No. 9,859,202
EX1004	<i>TopWire LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.</i> , No. 2:25-cv-01183, Dkt. 1 (“Complaint”) (E.D. Tex. Dec. 1, 2025)
EX1005	U.S. Patent Publication No. 2011/0147908 (“ <i>Sun</i> ”), published June 23, 2011
EX1006	U.S. Patent Publication No. 2013/0182402 (“ <i>Chen</i> ”), published July 18, 2013
EX1007	U.S. Patent No. 5,334,804 (“ <i>Love</i> ”), granted Aug. 2, 1994

EX1008	U.S. Patent Publication No. 2013/0249083 (“Hu”), published Sept. 26, 2013
EX1009	Benson, et al., <i>Polymer Adhesives and Encapsulants for Microelectronic Applications</i> , Johns Hopkins APL Technical Digest, Volume 28, Number 1 (“Benson”) (2008)
EX1010	U.S. Patent No. 8,379,403 (“Waite”), granted Feb. 19, 2013
EX1011	IPC, <i>IPC-4761 Design Guide for Protection of Printed Board Via Structures</i> (“IPC-4761”) (July 2006)
EX1012	Declaration of Sylvia D. Hall-Ellis, Ph.D. in support of authenticity and public availability of documents for <i>inter partes</i> review of U.S. Patent No. 9,859,202
EX1013	U.S. Patent Publication No. 2008/0155820 (“Arai”), published July 3, 2008
EX1014	Osborn, <i>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices</i> , Georgia Institute of Technology (May 2009)
EX1015	Henderson, <i>Copper Pillar Bumping Technology</i> , Info Tracks (Semitracks Monthly Newsletter), Issue 36 (June 2012)
EX1016	Kreidl, <i>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module</i> , Universität Mannheim (2011)
EX1017	IPC, <i>IPC-T-50M Terms and Definitions for Interconnecting and Packaging Electronic Circuits</i> (May 2015)
EX1018	Cohn, et al., <i>Electronic Packaging and Interconnection Handbook, Packaging and Interconnection of Integrated Circuits</i> , Chapter 7, McGraw-Hill (2000)
EX1019	Vintage Computer, <i>IBM PC/AT</i> (first archived on Mar. 5, 2021) https://vintage-computer.com/machines.php?ibmpcat [https://web.archive.org/web/20210305084621/vintage-computer.com/machines.php?ibmpcat]
EX1020	Mangrum, <i>Packaging Technologies for Mobile Platforms</i> , 2006 Electronics Packaging Technology Conference (2006)
EX1021	ICE, <i>Roadmaps of Packaging Technology, Interconnect Substrate Technologies</i> , Chapter 11 (1997)
EX1022	Kenny, et al., <i>From Thin Cores to Outer Layers: Filling through Holes and Blind Micro Vias with Copper by Reverse Pulse Plating</i> , 2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP) (2009).

EX1023	JEDEC, <i>JESD47F Stress-Test-Driven Qualification of Integrated Circuits</i> (Dec. 2007)
EX1024	IPC, <i>IPC-TM-650 Test Methods Manual</i> (May 2004)
EX1025	Koide, et al., <i>High-performance Flip-Chip BGA Technology Based on Thin-core and Coreless Package Substrate</i> , 2006 Electronic Components and Technology Conference (2006)
EX1026	Graf, <i>Modern Dictionary of Electronics</i> , Newnes, Seventh Edition (1999)
EX1027	Tummala, et al., <i>Microelectronics Packaging Handbook</i> , Van Nostrand Reinhold (1989)
EX1028	Baldwin, <i>Fundamentals of Microsystem Packaging, Fundamentals of IC Assembly</i> , Chapter 9, McGraw-Hill (2001)
EX1029	Wang, et al., <i>Studies on A Novel Flip-Chip Interconnect Structure – Pillar Bump</i> , 2001 Electronic Components and Technology Conference (2001)
EX1030	CV of Peter Elenius
EX1031	Petitioners' Stipulation

IV. LEGAL STANDARDS

16. My opinions are also informed by my understanding of the relevant law. I understand that the patentability analysis is conducted on a claim-by-claim and element-by-element basis, and that there are several possible reasons that a patent claim may be found to be unpatentable.

17. I understand that earlier publications and patents may act to render a patent unpatentable for one of two reasons: (1) anticipation and (2) obviousness.

B. Anticipation

18. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly

or inherently in a single prior art reference or system. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference, and that it would have been so recognized by a POSITA. In addition, I understand that an enabling disclosure is a disclosure that allows a POSITA to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

C. Obviousness

19. I understand that the prior art may render a patent claim “obvious.” I understand that two or more prior art references (e.g., prior art articles, patents, or publications) that each disclose fewer than all elements of a patent claim may nevertheless be combined to render a patent claim obvious if the combination of the prior art collectively discloses all elements of the claim and one of ordinary skill in the art at the time would have been motivated to combine the prior art in such a way. I understand that this motivation to combine need not be explicit in any of the prior art, but may be inferred from the knowledge of one of ordinary skill in the art at the time the patent was filed. I also understand that one of ordinary skill in the art is not

an automaton, but is a person having ordinary creativity. I further understand that one or more prior art references, articles, patents or publications that disclose fewer than all of the elements of a patent claim may render a patent claim obvious if including the missing element would have been obvious to one of skill in the art (e.g., the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system).

20. Under the doctrine of obviousness, a claim may be invalid if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA to which the subject matter pertains.

21. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any secondary considerations to the extent they exist.

22. I understand that any evidence of secondary indicia of non-obviousness should be considered when evaluating whether a claimed invention would have been obvious to one of ordinary skill at the time of invention. These secondary indicia of non-obviousness may include, for example:

- a long felt but unmet need in the prior art that was satisfied by the claimed invention;
- commercial success of processes claimed by the patent;

- unexpected results achieved by the invention;
- praise of the invention by others skilled in the art;
- the taking of licenses under the patent by others; and
- deliberate copying of the invention.

23. I understand that there must be a nexus between any such secondary indicia and the claimed invention.

24. It is also my understanding that there are additional considerations that may be used as further guidance as to when the above factors will result in a finding that a claim is obvious, including the following:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;
- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;
- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;
- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a POSITA;
- there existed at the time of conception and reduction to practice a known problem for which there was an obvious solution encompassed by the patent's claims; and
- there is some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed subject matter.

25. Finally, I understand that a claim may be deemed invalid for obviousness in light of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art.

D. Claim Construction

26. I understand that “claim construction” is the process of determining a patent claim’s meaning. I also understand that, during an *inter partes* review, claims are given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. I also understand that the claims of a patent must be interpreted in light of the specification—that is, the claim

language itself, the written description, and the figures in the patent—as well as the patent’s prosecution history and/or any reexamination history. I understand that a patentee may act as his own lexicographer and clearly set forth a definition of the claim term in the specification. In such a case, the claim term will receive the definition set forth in the patent.

V. OVERVIEW OF THE ’202 PATENT

27. I have reviewed the ’202 Patent, which is entitled “Spacer Connector.” EX1001 at Cover. I understand that the ’202 Patent was filed on June 23, 2016 and issued on January 2, 2018. *Id.* For purposes of this declaration, I have been asked to assume that the ’202 Patent has a priority date of June 24, 2015 based on a provisional application filed on that date.

28. I provide the following technology overview for context, the subject matter of which was well-known to persons of ordinary skill in the art before the time of the alleged invention of the ’202 Patent.

A. Subject Matter of the ’202 Patent

29. The ’202 Patent is directed to a semiconductor packaging structure including spacer connectors 10 placed between a top package (substrate 1) and bottom package (substrate 2). EX1001 at FIG. 8 (below), 11, 14. As I explained in detail below, semiconductor packaging, *see* §V.E (“Semiconductor Packaging”) is in a different technical field than PCB assemblies, *see* §V.G (“Printed Circuit

Board”), and the ’202 Patent is specially directed to semiconductor packaging involving what is commonly called PoP (Package on Package) in the industry. See EX1001 at Background.

30. Spacer connectors 10 include a core substrate 11 and metal pillars 15, which may be “protruded below a bottom surface of the core substrate 11.” EX1001 at 2:51–53, FIGs. 7B (below), 10A. Metal pillars 15 are connected to bottom metal pillars 101B on the top package substrate and to top metal pillars 201 on the bottom package substrate. *Id.* at 2:36–42, FIGs. 8, 11, 14. In connecting those metal pillars, metal pads 152 may also be used. *Id.* Further, a top (chip 1) and bottom chip (chip 2) may be mounted on the top and bottom package substrate, respectively, while two spacer connectors 10 are arranged on opposite sides of the bottom chip. *Id.* at FIGs. 8, 11, 14.

Fig.8

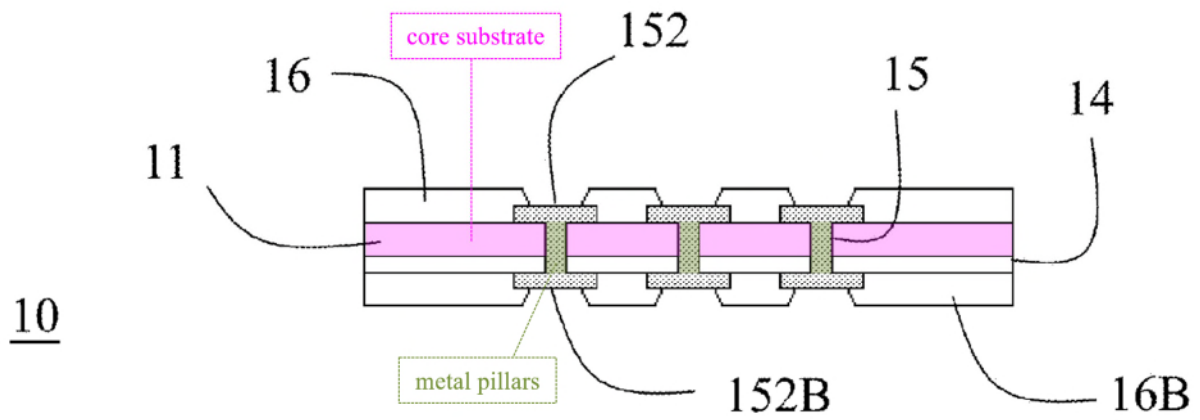
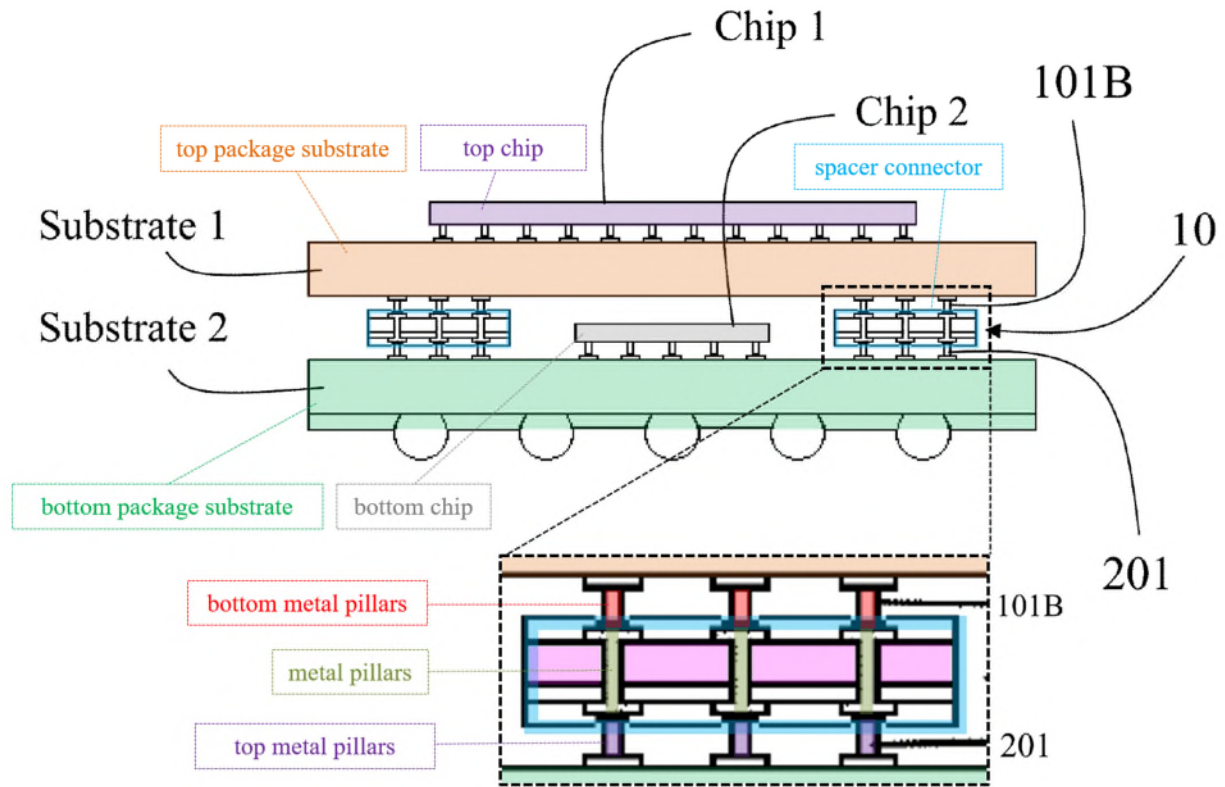


Fig.7B

EX1001 at FIGs. 8 (modified with adding a zoom-in view of spacer connectors 10)¹, 7B.

B. Prosecution History of the '202 Patent

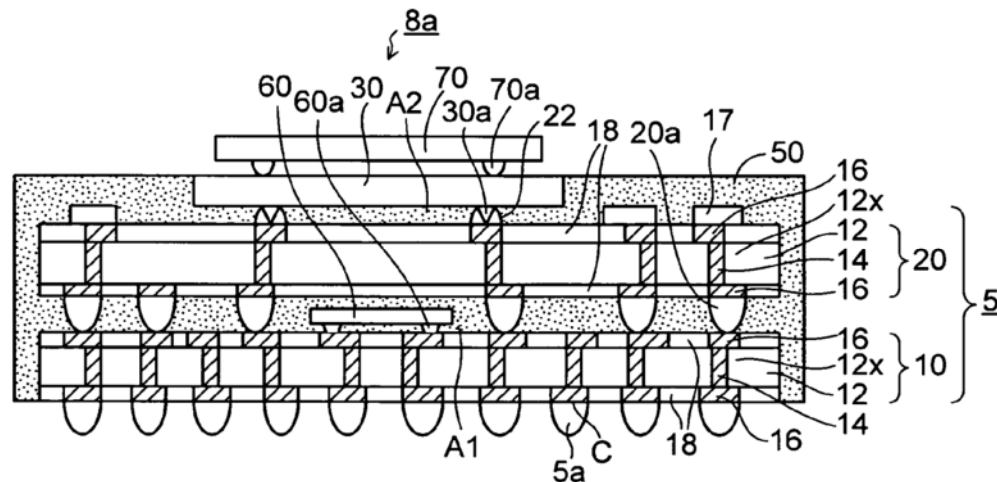
31. The '202 Patent was filed on June 23, 2016 (Application No. 15/190,695), originally with 8 claims, directed to the structure of “spacer connector” and its “process.” EX1001 at Cover; EX1002 at 8–30. It claims priority to provisional application filed on June 24, 2015 (Application No. 62/184,034). EX1001 at Cover.

32. After the Applicant added 12 more claims and the Examiner issued a restriction/election requirement, EX1002 at 64–65, 70–74, on July 10, 2017, the Applicant withdrew Claims 1–10 and elected Claims 11–20, leaving claims directed to the structure of “spacer connector.” EX1002 at 84–92.

33. On July 21, 2017, the Examiner rejected Claims 11, 15, and 17–20 as being anticipated by U.S. Patent Publication No. 2008/0155820 to Arai, et al. (“*Arai*”) (EX1013). EX1002 at 97, 100–103. Claim 11 (issued as Claim 1) included the same claim limitations as issued Claim 1 except that Claim 11 did not include limitations 1[k]–[m], which recite the “bottom chip” and “two spacer connectors” limitations the Applicant added to overcome *Arai*. *Id.* at 113, 117–18. Among other

¹ All colored text/annotations in figures and emphasis in quotes are added unless noted otherwise.

things, the Examiner found that *Arai*’s “silicon interposer 30” and “wiring board 10” disclosed “top package substrate” and “bottom package substrate,” respectively, and that *Arai*’s “wiring board 20” disclosed “at least one spacer connector” disposed between the top and bottom package substrate. *Id.* at 100–01 (citing *Arai*’s FIG. 11 below). The Applicant did not dispute this finding. *Id.* at 113.



EX1013 at FIG. 11.

conductive layer] 14 with 16 [in wiring board 10]” disclosed “top metal pillars of the bottom package.” *Id.* According to the Examiner, the metal pillars and the top metal pillars are connected “***in an end-to-end manner***,” when the two sets of metal pillars are connected via 20a, which the Examiner mapped to “bottom metal pads.” *Id.* Again, the Applicant did not dispute this finding. *Id.* at 113.

35. The Examiner also found, and the Applicant did not dispute, that *Arai*’s “solder resists 18” disclosed “dielectric layer” and that the “solder resists 18” are “dielectric adhesive into which the core substrate is pasted” because the “solder resists 18” are “adhered to core 12, [in] fig. 11.” EX1002 at 102, 113.

36. On October 19, 2017, the Applicant, while not disputing all the findings above, amended Claim 11 to add limitations 1[k]–[m], which recite the “bottom chip” and “two spacer connectors” limitations the Examiner found allowable subject matter. EX1002 at 113, 117–18.

37. On November 7, 2017, the amended claims were allowed without further rejection. EX1002 at 151.

C. Error During Prosecution of the ’202 Patent

38. Based on my assessment of the prosecution record, it is my opinion that the Examiner erred in allowing the claims because *Arai* at least renders obvious the additional limitations 1[k]–[m], which the Examiner found to be allowable subject matter.

to the increasing use of stacked dies with expanded functionality, driving the need to accommodate thicker chips in PoP structures. *See, e.g.*, EX1005 at [0058] (“two chips 200, 200a stacked one on top of the other”), [0060] (“A pair of chips 200, 200a may be memory chips or a processor.”); EX1006 at [0009] (“a plurality of memory dies stacked together”). Accordingly, a POSITA would have been motivated to modify *Arai*’s structure by separating the two spacer connectors rather than implementing them as a continuous structure illustrated in FIG. 11. As no functional component (such as through-hole-conductive layer 14 with 16 (metal pillars) for electrical connections) is present in the connection between *Arai*’s two spacer connectors, a POSITA would have easily divided the spacer connectors into two segments on either side of the chip 60, allowing additional clearance above chip 60.

42. Indeed, it was well known in the art that a PoP structure like *Arai*’s has two ***separate*** spacer connectors that provide enough space for a bottom chip. For example, *Sun* (EX1005) teaches “**second substrate** [spacer connector] has an opening therein [thus being divided into two separate spacer connectors] for accommodating” “two chips 200, [where] 200a stacked one on top of the other.” EX1005 at [0048], [0058], [0060] (“A pair of chips 200, 200a may be memory chips or a processor.”), FIG. 12 (below):

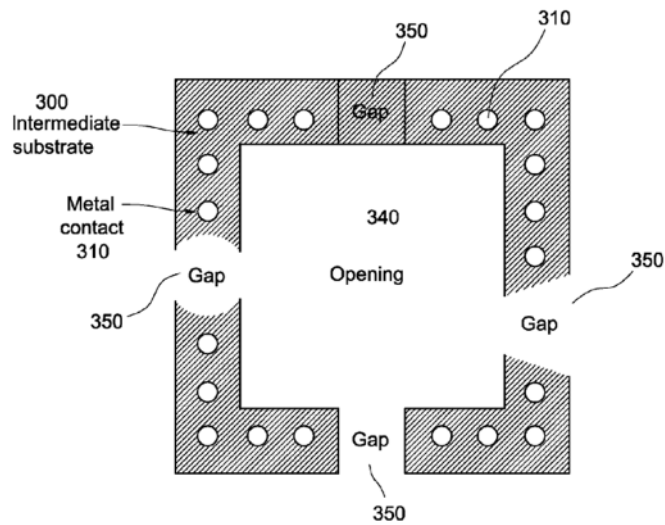


FIG.9

43. Similarly, the PoP disclosed in *Chen* (EX1006) includes two “TAV modules 28 [spacer connectors] [] disposed on opposite sides of package component 24 [bottom chip]” to provide enough headroom for package component 24, which includes “stacked dies.” EX1006 at [0012], FIGs. 2, 9–11:

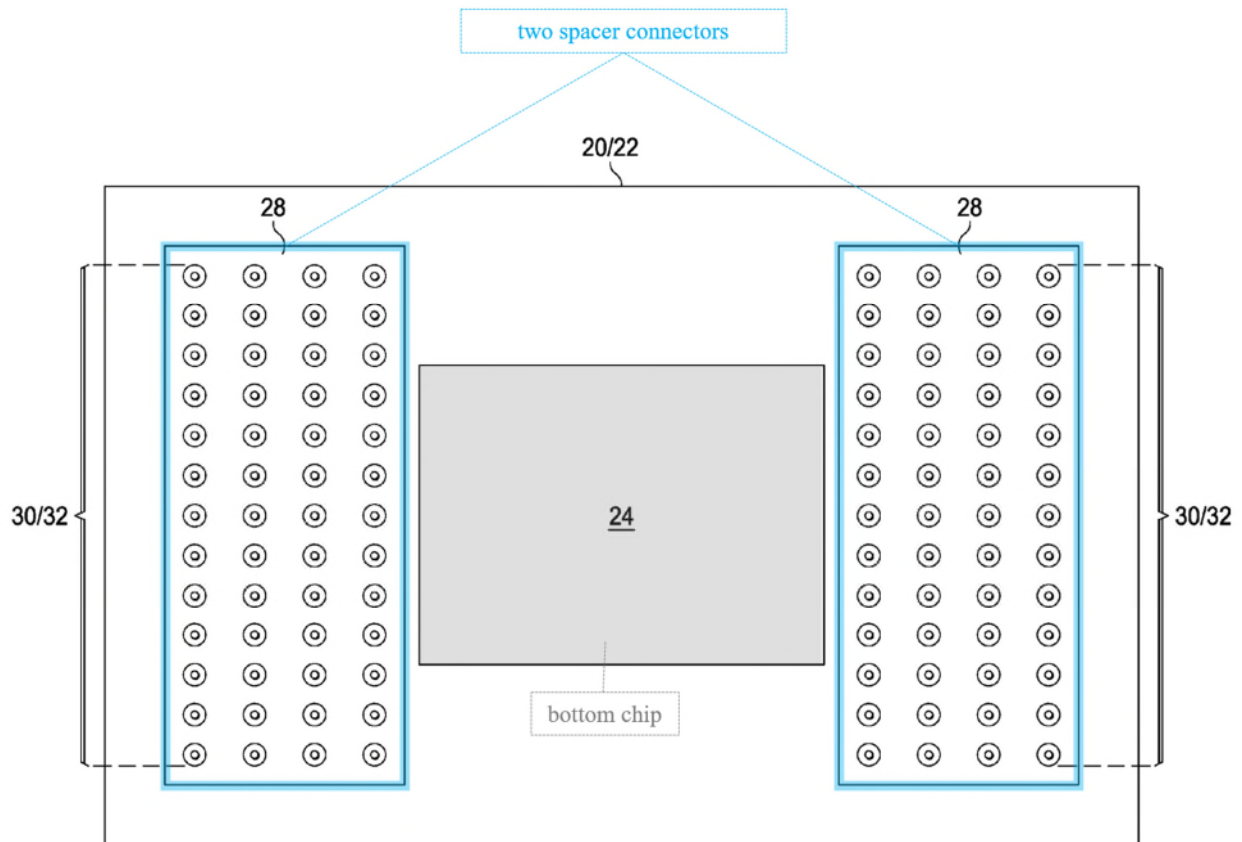


FIG. 2

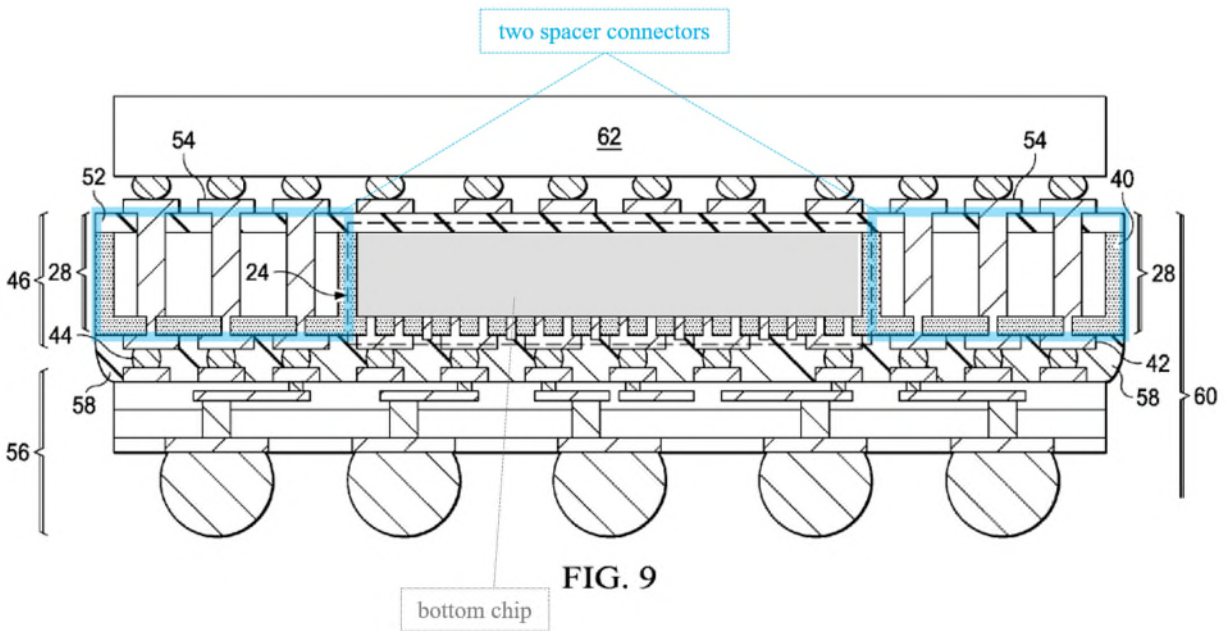


FIG. 9

44. Accordingly, it is my opinion that the Examiner erred by failing to

consider the obviousness of “two spacer connectors arranged on opposite sides of the bottom chip” in view of *Arai*, POSITA’s knowledge, and other similar references.

D. Semiconductor Device Fabrication

45. Based on my experience in the industry, I am familiar with the design of semiconductor devices of the type relevant to the ’202 patent.

46. Generally, the process of forming semiconductor devices starts with a semiconductor wafer. Silicon is most commonly used for the wafer, but other types of semiconductor materials may be used. Electronic devices, *e.g.*, transistors, capacitors, diodes, resistors, etc., are formed on the silicon wafer and metallization layers are formed over these electronic devices. The metallization layers are used to interconnect the electronic devices to form a semiconductor device. When multiple electronic devices are interconnected to form an electronic circuit function, the semiconductor device is called an integrated circuit (IC). Examples of integrated circuits include microprocessors, power transistors, memory, and ASICs (Application Specific Integrated Circuits). These semiconductor devices are referred to as dies (and sometimes loosely as chips); as fabricated, these dies must be properly packaged to interact and connect to the external circuitry.

E. Semiconductor Packaging

47. Semiconductor packaging technology refers to processes and structures that provide for connecting a semiconductor device to the next level of assembly,

such as a printed circuit board (PCB), which is also referred to as a printed wiring board (PWB). *See* EX1018 at 4 (“An IC package is the housing, which assures environmental protection to the IC chip and provides for complete testing and high-yield assembly to the next level of interconnection.”); *see also* EX1028 at 13. Semiconductor packages provide four major functions: protecting the semiconductor device from environmental and mechanical damage, transforming the fine pitch of the device’s connection pads to a coarser pitch, providing adequate power/ground delivery and signal integrity, and providing a cooling method, if required, for thermal management. Encapsulating materials have been used since the 1950s to protect integrated circuits from environmental and mechanical damage.

48. Semiconductor packages have evolved over the last sixty-five years from relatively large hermetic ceramic packages to today’s wafer level packaging (WLP) to meet the needs of the market. Today, as was true at the time of the ’202 Patent’s filing, no single packaging technology dominates the market. Rather, there are a variety of choices, and an engineer will select the appropriate packaging technology for the desired application.

F. Package on Package (PoP)

49. Package on Package (PoP) technology goes back to at least 1982 with the stacking of two DRAM DIP (Dual Inline Packages) in the IBM PC/AT as shown in the following image.

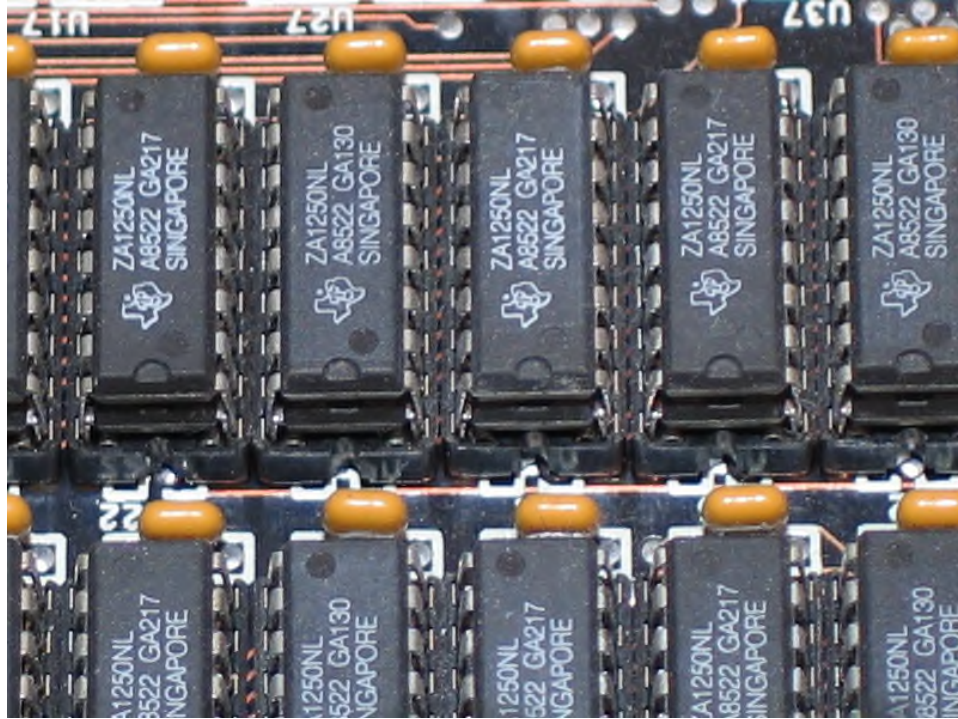


Figure 1 - IBM Stacked DRAM Packages in the IBM PC/AT

EX1019 at 4.

50. In the 2004-to-2005-time frame PoP technology adoption started at the cell phone OEMs. The most common form of PoP was stacking a BGA (Ball Grid Array) module on top of another BGA module that would be attached to the cell phone's motherboard. This structure is shown in the following image.

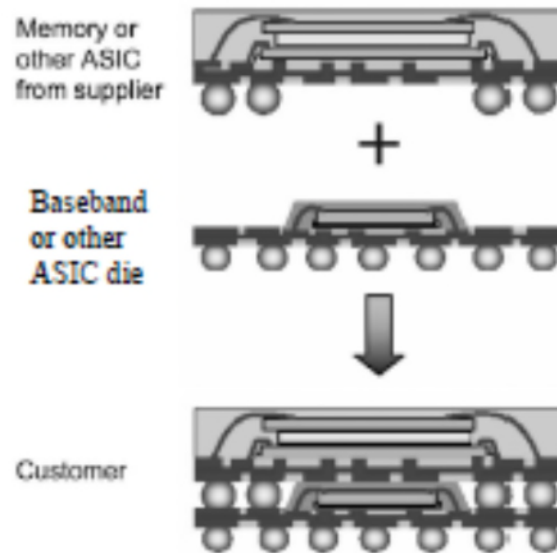


Figure 2 - Typical PoP Structure in 2005

EX1020 at 1.

51. The cell phone industry adopted PoP to allow supply chain flexibility and enable phone customization. Because package footprints were standardized, the cell phone OEM could now use multiple memory suppliers and produce phones with varying amounts of memory to meet customer's requirements. *Id.*

G. Printed Circuit Board

52. The printed circuit board (PCB) is also often referred to as a motherboard. The motherboard's function is to mount and electrically connect multiple first level semiconductor packages together, along with capacitors, resistors, connectors, sockets, etc. to make a higher-level functional product and to connect with a power source. This creation of a higher-level functional product is one characteristic that distinguishes a PCB/motherboard from a packaged IC. A

standalone IC package or PoP assembly cannot properly function or operate as needed without first being connected to memories, expansion slots on motherboard, connectors, interface logic, passives, displays, charging port, keypad, etc. through a PCB.

53. The basic process of creating a PCB through hole via is shown and annotated in the following figure. After fabricating the through hole vias additional processes such as applying a solder mask, HASL (Hot Air Solder Leveling), ENIG (Electroless Nickel Immersion Gold), via plugging, via capping and buildup layers may be added. Via plugging, via capping and buildup layers will be covered in the following paragraphs and sections.

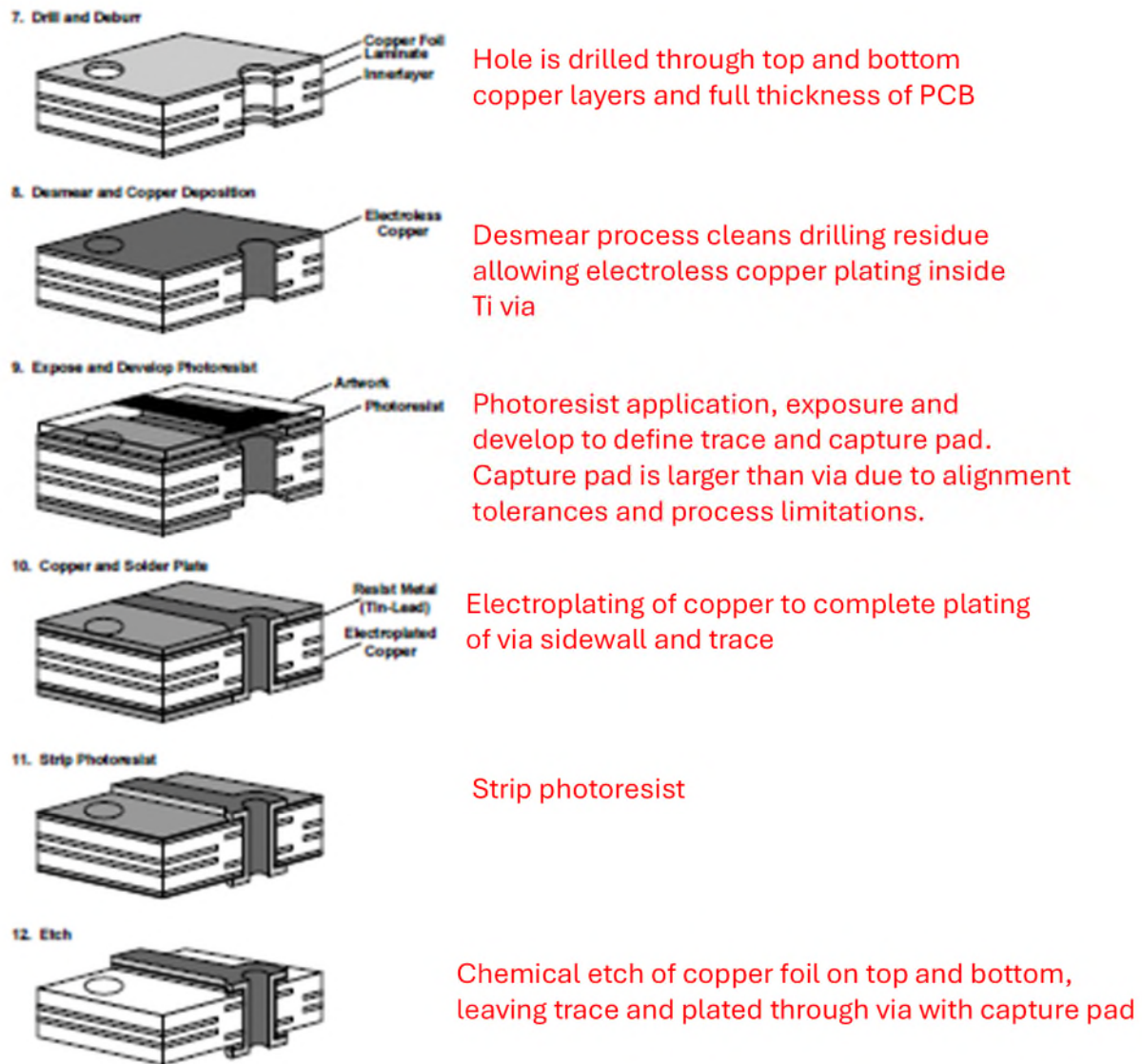


Figure 3 - How to Build a Circuit Board

EX1021 at 5 (annotated).

54. Via plugging is done to prevent solder from wetting down or up the through plated via and/or to enable the addition of buildup layers on the PCB. In the following paragraphs, three different types of via plugging structure are shown.

55. In the figure below the process of filling a via in the PCB with a

polymer material is shown. In this case the polymer fills the via and creates a small bump above the via. This type of plug is used to prevent solder wetting of the through via and when a buildup layer is not required to connect to the through via capture pad.

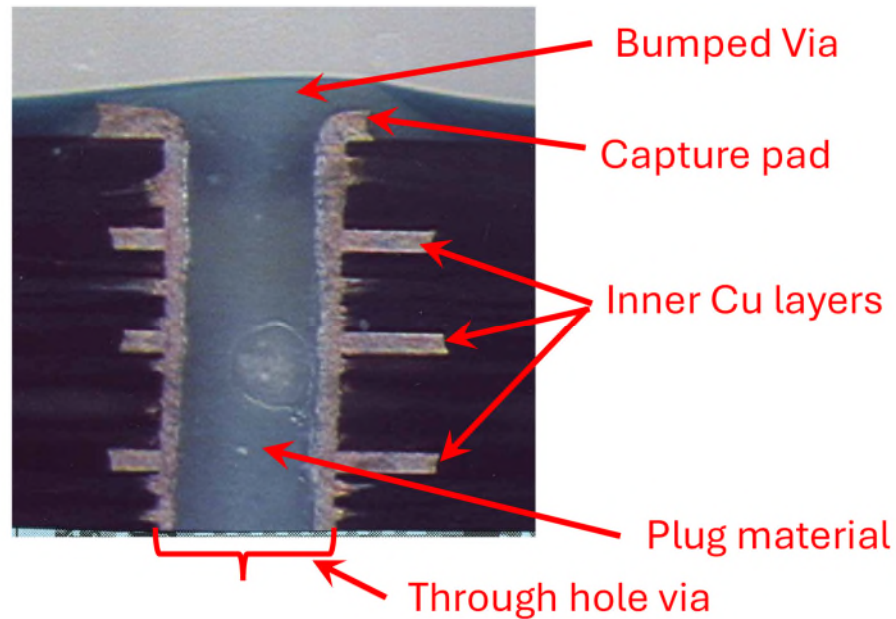


Figure 4 - Bumped Via Structure

EX1011 at 7 (annotated).

56. In the figure below, a non-conductive past material is used to fill the via and then this material is planarized. The copper cap on both the top and bottom surfaces of the via are done with a buildup process as detailed in the next section.

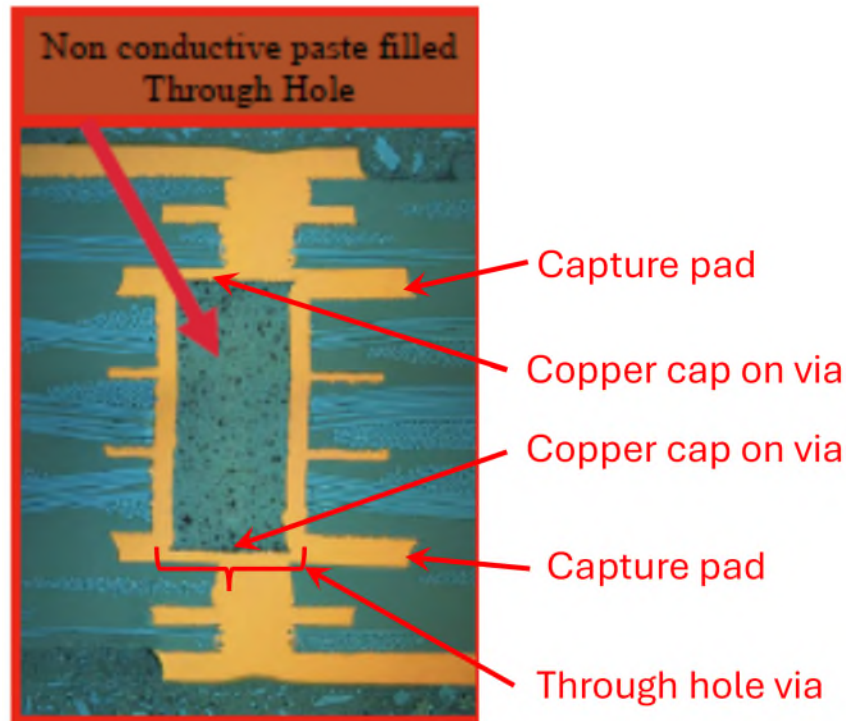


Figure 5 - Planarized and Capped Via Structure

EX1022 at 1 (annotated).

57. In the figure below is another example of a filled through hole via. In this case the via has been filled with copper by an electroplating process. While this figure shows a cross-section of a through hole via, the via has been drilled, creating a round hole, that when filled with copper makes a copper pillar or column.

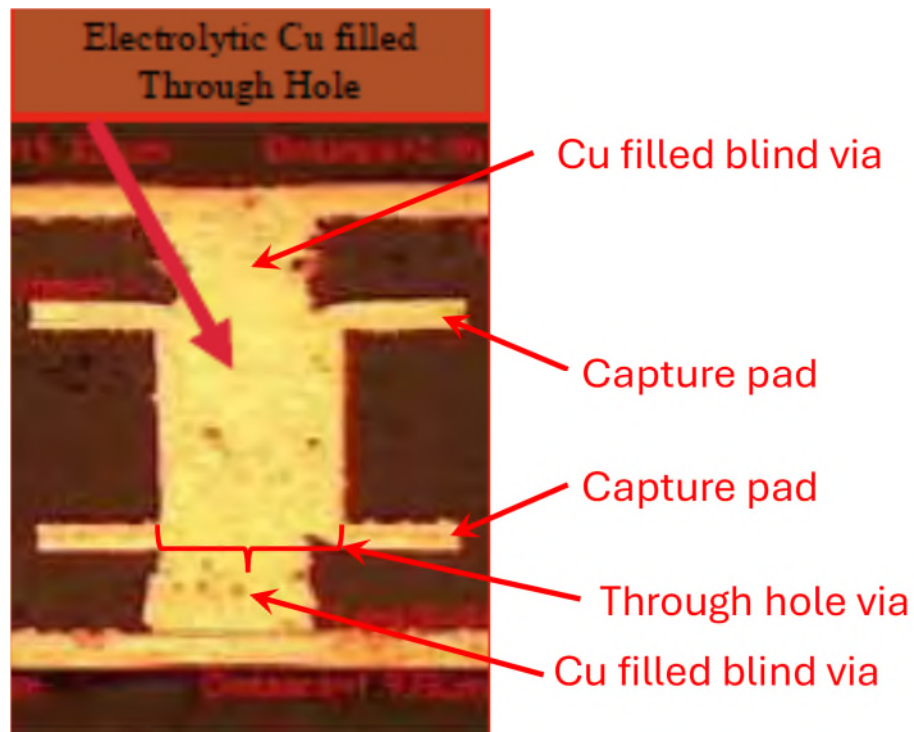


Figure 6 - Planarized and Capped Via Structure

EX1022 at 1 (annotated)

H. Substrates used for Semiconductor Packaging

58. Both laminate (*i.e.*, organic) IC package substrates and PCBs utilize multiple organic dielectric layers and copper wiring layers. There are substantial differences in materials, processes, capabilities and factories used to produce IC package substrates and PCBs.

59. The organic IC package substrates must survive a variety of reliability tests that include temperature and humidity testing for up to 1,000 hours, autoclave testing, moisture sensitivity level (MSL) testing, high temperature operating life (HTOL) at 125 to 150 C for 500 to 1,000 hours, package level thermal cycling and

thermal shock testing. These tests are done by the IC manufacturer to ensure that when assembled to a PCB, the product will be reliable. EX1023 at 16 (Table 2). The PCB reliability testing is less stringent, looking at PTH (Plate Through Hole) integrity by laying the PCB one time on a molten solder for ten seconds. EX1024 at 1.

60. To meet the IC package reliability requirements, the materials for the IC package substrates must be capable of withstanding higher temperatures, have less moisture sensitivity and have excellent adhesion. These materials, such as bismaleimide triazine (BT) resin material and Ajinomoto Buildup Film (ABF), are too expensive to use for a large motherboard/PCB and are overkills for the less stringent reliability requirements or the process capabilities of the motherboard/PCB.

61. The wiring line and space requirements are also significantly different. An IC BGA package substrate must route hundreds to thousands of I/O from under a flip chip die and fan out these I/O to the pads or solder balls of a suitable pitch for joining to the PCB while maintaining the required power and ground distribution to the die. This requires wiring line widths and spaces that are much smaller than the requirements for the PCB.

62. The picture below is a cross-section of a 5-2-5 substrate that is fabricated with five buildup layers on each side. In the 5-2-5 nomenclature the "2"

refers to the core with two copper layers. Buildup substrate structures start at 1-2-1 and can have many buildup layers. The core substrate can also have more than two layers. A 4-4-4 substrate would have four buildup layers on either side of a core substrate that has four copper layers.

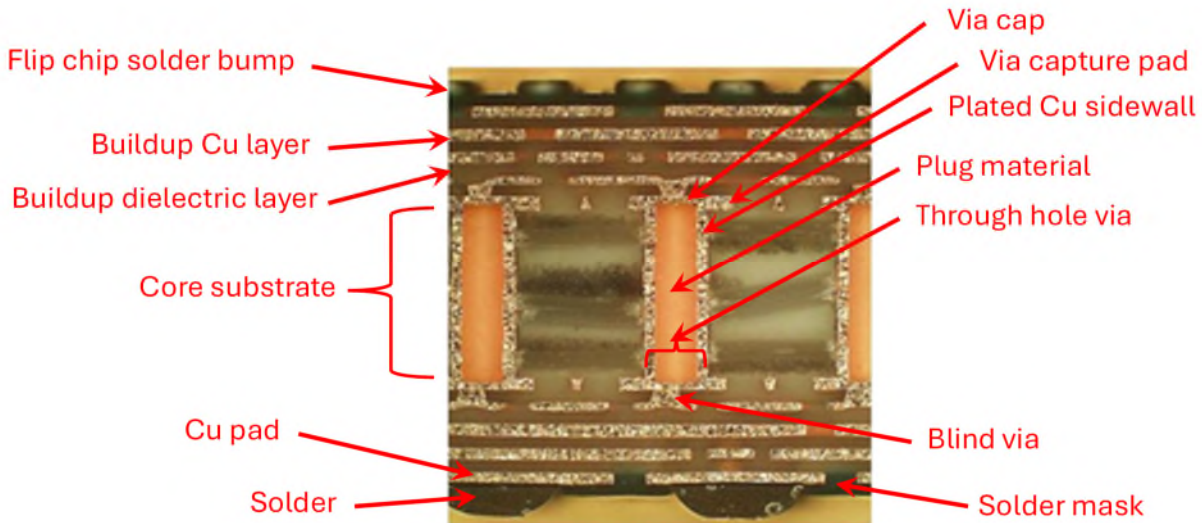


Figure 7 - 4-2-4 Substrate with 4 Buildup Layers Each on Top and Bottom

EX1025 at 1 (annotated).

I. Solder Mask

63. Prior to soldering, a solder mask is applied to the semiconductor substrate, on top of a patterned copper wiring layer. To do so, a dry film with adhesive properties is laminated on the semiconductor substrate, or a liquid with adhesive properties is coated thereon, and cured. The solder mask both protects the copper wiring layer and defines the solderable areas on the copper.

J. Soldering

64. The Modern Dictionary of Electronics defines soldering as: “A process of joining metallic surfaces with solder, without the melting of the base metals.” EX1026 at 58.

65. As an initial step, solder in the form of solder paste or solder balls are attached to contact surfaces of a component or substrate.

66. The metallic surfaces of corresponding contact surfaces, such as Cu pads to be joined with the component or substrate, have a Cu oxide layer that impedes the wetting of the solder to the Cu. In the soldering process a flux is used to reduce (remove) the oxides prior to the wetting of the solder to metallic surfaces during the reflow process in which the solder is melted. EX1027 at 146–149.

67. For a BGA (Ball Grid Array) package the solder balls are then aligned with the corresponding contact surfaces (e.g., Cu pads), and the aligned structure is passed through a reflow oven, which heats the solder balls past their melting point. During this reflow stage, the solder balls liquify and melt onto the corresponding contact surfaces, to join the two surfaces.

68. The joining of the two metallic surfaces with the solder results in the formation of intermetallic layers at the interface of the bulk metallic surface and the solder. For a Cu surface joined with a solder containing Sn, intermetallic compounds will be formed including Cu_6Sn_5 and Cu_3Sn_4 .

K. Electrolytic Plating Process

69. There are three basic types of metal plating processes: immersion, electroless and electrolytic. Both immersion and electroless plating processes result in relatively thin coating. The '202 patent describes the use of electrolytic copper plating to create the claimed pillars.

70. Electroplating requires a conductive metal layer to uniformly distribute electrical current to the areas to be plated. For plating a copper pillar, a sputtered copper layer is commonly used. Features are formed by coating the conductive metal layer with a photoresist and patterning the resist to open the areas to be plated. The item to be plated is then immersed in the electrolyte bath and a current and voltage are applied to plate the metal into the open resist areas.

71. The following image on the left is for an electroplating process that fabricates a copper pillar with a solder cap. This solder capped copper pillar is shown joined to a substrate pad on the right. The solder capped copper pillar structure has been adopted as it allows finer pitches, increases the standoff height and improves the electromigration performance of the interconnect.

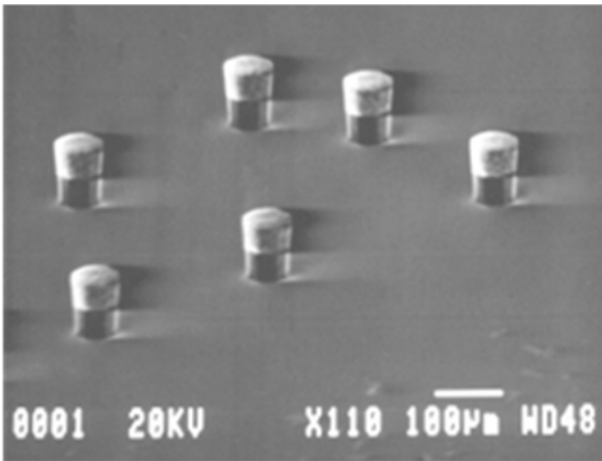


Figure 8 – Cu Pillar with Solder Cap

EX1029 at 1.

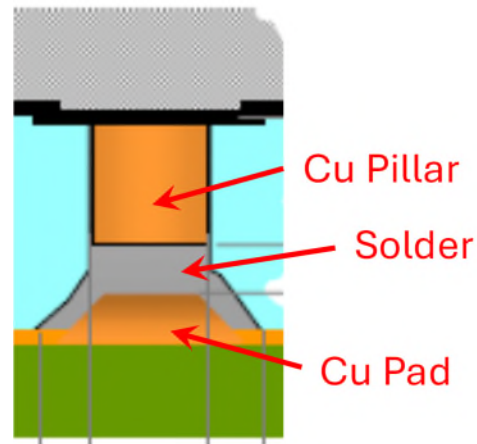


Figure 9 - Pillar Bump Joined to Pad with Solder

EX1029 at 4 (annotated).

72. In 1992, Love, et.al. patented a spacer technology that had a plugged through via and a copper pillar on the top and bottom surfaces. EX1007. This structure is shown in the figure below. In addition to the electrolytically plated Cu plug 224 and Cu base pads 20 and Cu posts/pillars 14 they also disclosed an electroless Ni layer 25.

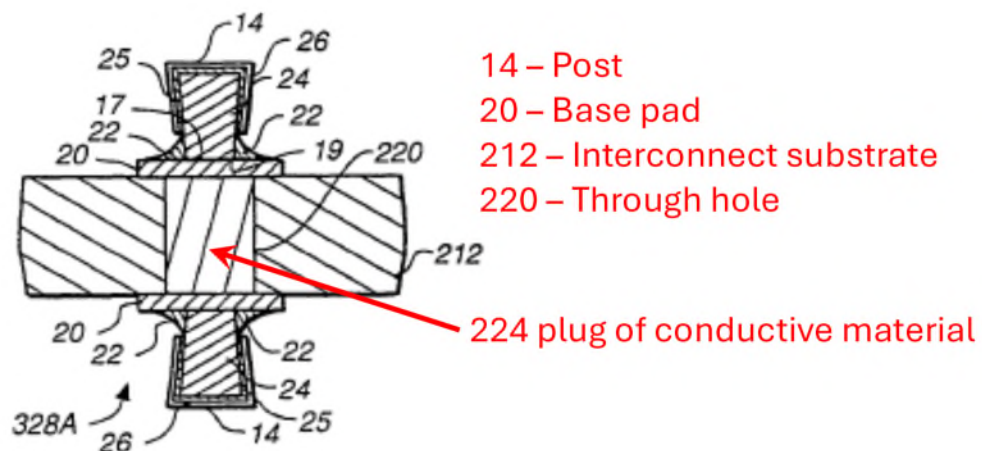


Figure 10 - Spacer Substrate with Cu Pillars on Top and Bottom

EX1007 at FIG. 6C-3 (annotated).

73. This structure became known in the industry as the Wire Interconnect Technology (WIT). As shown in the following figure, one use was for joining an IC chip through the WIT structure to a substrate.

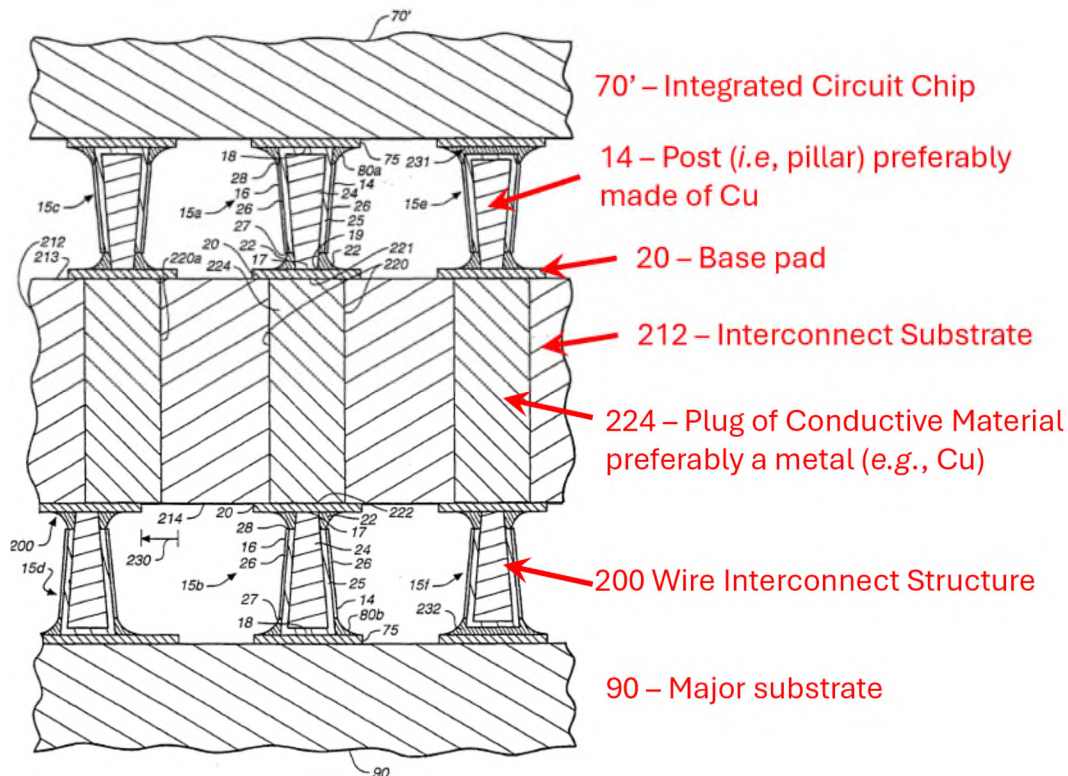


Figure 11 - Spacer Substrate with Cu Pillars Joining IC Chip to Substrate

EX1005 at FIG. 5 (annotated).

VI. LEVEL OF ORDINARY SKILL IN THE ART

74. I am informed and understand that the person having ordinary skill in the art (“POSITA”) is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor’s skill is not determinative of the level

of ordinary skill. I further understand that factors that may be considered in determining level of skill include: (i) type of problems encountered in art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or more of them may predominate. In a given case, every factor may not be present, and one or more factors may predominate.

75. In my opinion, a POSITA at the time of the alleged invention of the '202 Patent would have either (i) a Master of Science in Electrical Engineering, Materials Science, Mechanical Engineering, or an equivalent field, or (ii) a Bachelor of Science in Electrical Engineering, Materials Science, Mechanical Engineering, or an equivalent field and two years of experience in the field of semiconductor packaging. Before the priority date of the '202 Patent, I had this level of skill. Indeed, around the time of the alleged invention, I was familiar with this level of skill for semiconductor packages using laminate, ceramic and glass substrates and Package on Package (PoP) constructions. This is the education and experience level that I encountered for people working in the field at the time.

VII. CLAIM CONSTRUCTION

76. I understand that “claim construction” is the process of determining a patent claim’s meaning. I also understand that, during an *inter partes* review, a claim

construction analysis begins with the plain meaning of the claim term, which is the ordinary and customary meaning given to the term by those of ordinary skill in the art at the time of the invention. I also understand that the claims of a patent must be interpreted in light of the specification—that is, the claim language itself, the written description, and the figures in the patent—as well as the patent’s prosecution history and/or any reexamination history.

A. “metal pillar” (1[e]–[j], 4–7, 9)

77. It is my opinion that a POSITA would have understood “metal pillar” as a columnar metal structure, such as a metal post or via. Claims of the ’202 Patent recite “metal pillars” “passing through the core substrate” and “protrud[ing] downwardly from ... the core substrate” (EX1001 at 3:42–43, 47–49). This description of “metal pillars” indicates that they have a columnar structure, and the feature of “passing through the core substrate” cannot be realized by solder balls or other solder structures. Consistent with the claim language, all metal pillars in the specification are illustrated as columnar metal posts or vias without a spherical/round shape, as typically used in the art to represent solder balls. *See, e.g., id.* at FIGs. 7A–B (copper pillar 15 acting as a metal via penetrating a substrate), 8 (bottom/top metal pillars 101B/201). The specification further teaches “metal pillars” are formed by an “electric plating process.” *Id.* at Abstract. As explained in detail above in §V.K, an “electric plating process” is a distinct process to form

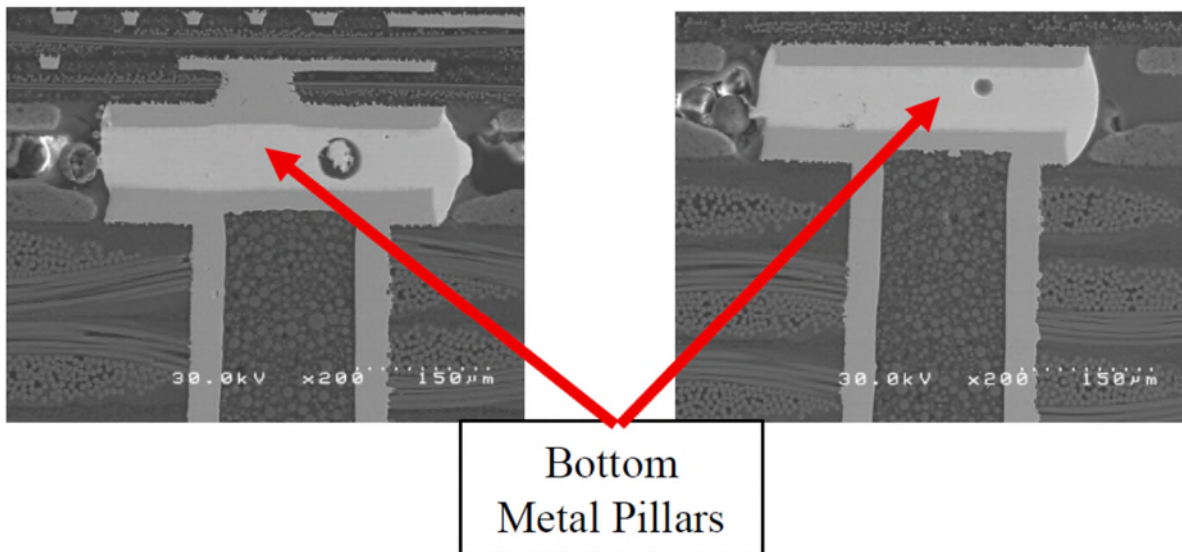
column-shaped metal pillar in semiconductor process that is different from processes for forming solder connections. *See also* EX1006 at [0014] (“metal pillars, or metal pillars and solder caps ... formed through plating”); EX1008 at [0008] (“[M]etal posts are formed by electroplating.”).

78. In the field of semiconductor process and packaging, “metal pillar” interconnects refer to a different type of conductive interconnects than solder structures. In fact, metal pillars are used in advanced semiconductor packaging to overcome various drawbacks of solder balls. *See e.g.*, EX1008 at [0004]–[0005] (explaining “metal posts ... are used ... so as to overcome the [] drawbacks” of “solder balls”); EX1014 at 23–24, 31–33 (providing “solid metal pillar connections” to overcome the limitations of “solder balls”); EX1015 at 2 (“Copper pillar bumping is intended as a replacement to traditional solder bumping.”); EX1006 at [0014] (distinguishing “solder balls” and “metal pillars” as two different types of interconnects implemented as connectors 44).

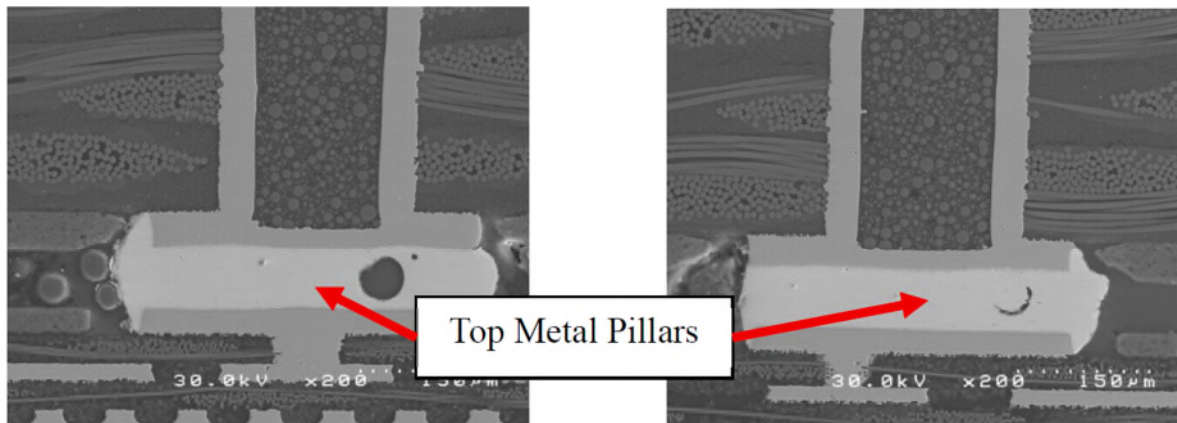
79. Thus, it is my opinion that the term “metal pillars” recited in claims 1, 4–7, and 9 should be interpreted as a columnar metal structure, such as a metal post or via.

80. Patent Owner appears to have taken a broad and unsupported construction of “metal pillar,” reading on any conductive interconnects, including solder structures on accused products, according to in its complaint. EX1004 at

¶¶45–46. As shown in the figures below, Patent Owner maps the claimed “bottom metal pillar” and “top metal pillar” in its complaint to structures visible in the SEM images that are, in fact, reflowed solder connections, as reflected by the SEM contrast. The structure appears brighter in the SEM image, confirming to a POSITA that the corresponding material has a higher atomic number than the nearby copper vias and pads and therefore likely comprises a solder composed of tin (Sn) and silver (Ag) as is common in the industry. These solder interconnects are formed between substrate pads and via caps to provide electrical and mechanical connections of the type commonly used in PCB assemblies, which generally do not require fine-pitch or micro-processing.



SEM images of the bottom metal pillars



SEM images of the top metal pillars

EX1004 at ¶¶45–46.

81. While all grounds in my declaration satisfy the correct construction, alternative disclosures of the prior art are identified, where applicable, as meeting this claim limitation under Patent Owner’s broad interpretation of this term.

B. “package substrate” (1[a]–[c], 1[h]–[l], 2–4, 6, 9)

82. As explained in detail above in §V.E (“Semiconductor Packaging”) and §V.G (“Printed Circuit Board”), and consistent with the understanding of a POSITA, “package substrate” refers to a substrate used for semiconductor die-level packaging. *See, e.g.*, EX1006 at [0019] (“a device die ... bonded to a package substrate”).

83. This interpretation is supported by the ’202 Patent. For example, “Description of Related Art” identifies the subject matter of the invention:

“One of the traditional processes for fabricating metal circuitry, a seed layer is often applied before electric plating. In a later process, the seed layer needs to be stripped. However, the stripping of the seed layer reduces the size of the circuits. Although such a circuit reduction is tiny, it is critical when it comes

to nanotechnology. A fabricating process without reducing the dimension of a circuitry is one of the popular topics to study for a long time in the semiconductor industry.”

EX1001 at 1:16–25. This passage emphasizes that stripping a seed layer causes a tiny but critical reduction in circuit dimensions and explicitly notes that this is important “when it comes to nanotechnology.” Dimensional loss at the micron scale is a core concern in semiconductor interconnect fabrication, where line widths and spaces are measured in microns. By contrast, PCB traces are larger (typically tens of microns), and minor material loss during processing is not described or treated as “critical” in this way. The ’202 Patent does disclose through its figures and explanatory text a standard interpretation of what a package substrate is. For example, Fig. 8 is described as having a package substrate 1 stacked on top of a package substrate 2. Chip 1 is located on the top of package substrate 1 and Chip 2 is located on top of package substrate 2. EX1001 at 2:30-35. Package substrate 1 has a plurality of bottom metal pillars which function as terminals for electrical connection as are common to all semiconductor packages. *Id.* at 2:36-39.

84. Thus, it is my opinion that the term “package substrate” recited in claims 1, 2–4, 6, and 9 should be interpreted as a substrate that is part of a semiconductor package, that provides mechanical support and electrical interconnection with a semiconductor die, rather than a printed circuit board that assembles packaged chips and discrete electronic components.

85. Patent Owner appears to have taken a broad construction of “package substrate,” reading on printed circuit board assemblies of the accused products, according to its Complaint, EX1004 at ¶¶41–42, despite the clear technical difference of semiconductor packaging (which involves package substrate), §V.E (“Semiconductor Packaging”), and printed circuit board assemblies, §V.G (“Printed Circuit Board”). In my declaration, Ground 9 specifically addresses the invalidity of the ’202 Patent claims under Patent Owner’s broad construction of this term. See §VIII.XVI.

C. “bottom metal pillars of the top package substrate” and “top metal pillars of the bottom package substrate” (1[h]–[j], 4, 6, 9)—“of” terms

86. In my opinion, a POSITA would have understood the preposition “of” in the above terms indicates an association between the metal pillars and the package substrates, and thus the claim limitations are met as long as the bottom metal pillars are located on the bottom side of the top package substrate and the top metal pillars are located on the top side of the bottom package substrate. These terms do not require the metal pillars to be first constructed as part of the respective substrates. EX1001 at 2:1–5, 2:36–42, FIGs. 8, 11, 14; EX1004 at ¶¶45–46.

87. The claims of the ’202 Patent are directed to a “structure,” EX1001 at 3:32, and as I understand when a claim is directed to an apparatus and merely recites a final structure, it does not require any manufacturing process or intermediate steps

for the structure. Further, the claim language of the '202 Patent specifies the association between the metal pillars and respective substrates. EX1001 at 3:49–51 (describing “bottom metal pillars” “on a bottom surface” of “the top package substrate”), 3:54–55 (describing “top metal pillars” “on a top surface” of “the bottom package substrate”). Finally, the specification, which primarily relies on various figures, does not show or suggest the metal pillars are pre-assembled with the top or bottom substrates.

88. Regardless, my declaration presents invalidity positions under both the correct construction (Grounds 1–9) and a narrower construction that requires the pre-assembling of the metal pillars and respective substrates (Grounds 4, 7–8).

VIII. SUMMARY OF PRIOR ART

A. *Sun* (EX1005)

89. *Sun* was filed on December 17, 2009 and published on June 23, 2011. EX1005. The '202 Patent was filed on June 23, 2016 and claims priority to US Provisional Patent Application No. 62/184,034, dated June 24, 2015. *Sun* thus predates the '202 Patent by over a year.

90. *Sun* discloses a PoP assembly having two substrates interposed by a spacer connector. EX1005 at [0061], Fig. 12. In particular, *Sun*'s third substrate 20 is stacked onto a first substrate 100 via second substrate 300. *Id.* *Sun* further discloses that chips 200, 200a can be mounted on the first substrate 100, such that

they are disposed between the third substrate 20 and first substrate 100. *Id.* *Sun*'s electrical connections are routed via second metal connectors 310 (in contact with the third substrate 20 and vias 390), vias 390 (within second substrate 300), and first metal connectors 320 (in contact with vias 390 and the first substrate 110). *Id.* As I describe in § X.A, a POSITA would have recognized the second metal connectors 310, vias 390, and first metal connectors 320 as “metal pillars.”

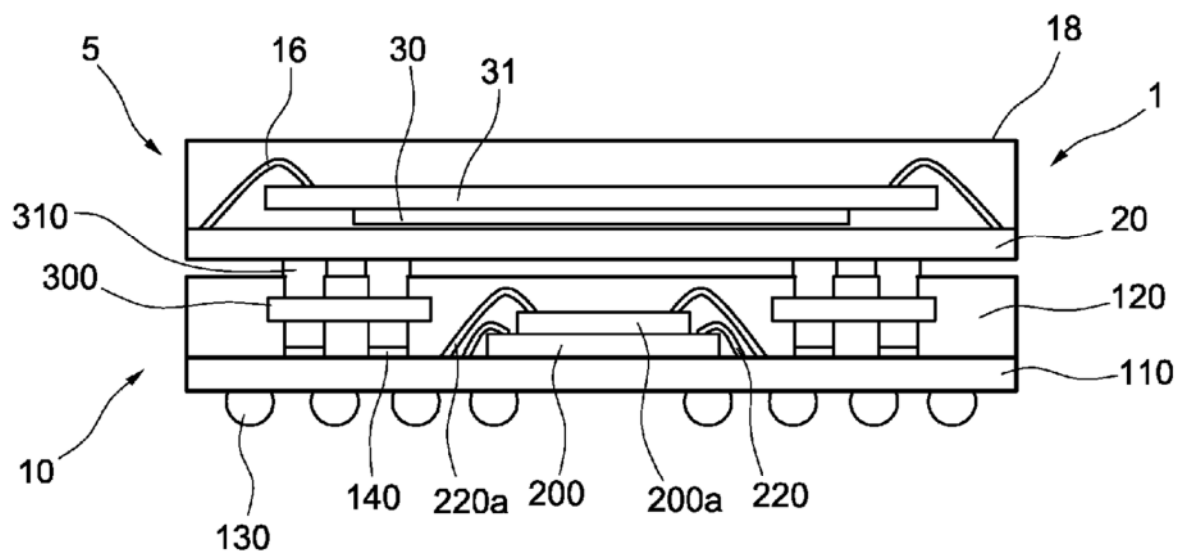


FIG.12

EX1005 at FIG. 12.

91. *Sun* is in the same field of endeavor as the '202 Patent—package-on-package assemblies—and in my opinion, *Sun* provides an alternative design that would have been available to a POSITA at the time of invention.

B. *Chen* (EX1006)

92. *Chen* was filed on January 18, 2012 and published on July 18, 2013. EX1006. The '202 Patent was filed on June 23, 2016 and claims priority to US Provisional Patent Application No. 62/184,034, dated June 24, 2015. *Chen* thus predates the '202 Patent by over a year.

93. Similar to *Sun*, *Chen* discloses a PoP assembly having two substrates interposed by TAV modules. EX1006 at [0008], [0014], [0018]–[0019], Fig. 9. Specifically, *Chen*'s top package component 62 is stacked onto package component 56 via two TAV modules 28. *Id.* *Chen* also discloses that one or more “device dies” can be mounted on the package component 56. EX1006 at [0009], [0012]. *Chen*'s packages are electrically connected via connectors 44 (in contact with package component 62, package component 56, and the TAV modules) and metal posts 30 and through-substrate vias 32 (disposed within the TAV modules 28). EX1006 at [0014], [0019]. As I describe in § XIII.A, a POSITA would have recognized the connectors 44, and metal posts 30 and through-substrate vias 32 as “metal pillars.”

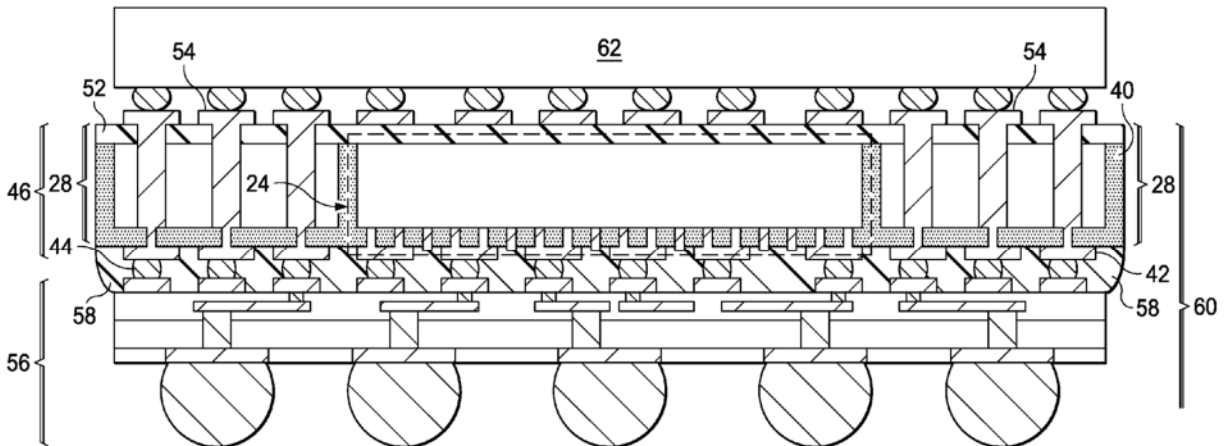


FIG. 9

EX1006 at FIG. 9.

94. *Chen* is in the same field of endeavor as the '202 Patent—package-on-package assemblies—and in my opinion, *Sun* provides an alternative design that would have been available to a POSITA at the time of invention.

C. Love (EX1007)

95. *Love* was filed on November 17, 1992 and issued on August 2, 1994. EX1007. The '202 Patent was filed on June 23, 2016 and claims priority to US Provisional Patent Application No. 62/184,034, dated June 24, 2015. *Love* thus predates the '202 Patent by over a year.

96. *Love* discloses an “interconnect structure[] for electrically and mechanically connecting an integrated circuit (IC) chip to a supplying substrate, which serve[s] to communicate signals between the IC chip and the ‘outside world.’” EX1007 at 4:51–61. While *Love*’s interconnect structure connects a “supplying

substrate” (i.e., package substrate) to an integrated circuit (i.e., chip), in my opinion, a POSITA would have understood that certain techniques taught by *Love* could be applied to a PoP structure. For example, *Love* discloses that conductive material 224 of an interconnect substrate 212 can be connected to upper posts 14 of an integrated circuit 70 and lower posts 14 of a major substrate 90 to facilitate an electrical connection between the integrated circuit 70 and major substrate 90. EX1007 at 12:34–60, FIG. 5. As I describe in § XI.A, a POSITA would have recognized the conductive material 224 and posts 14 as “metal pillars.” As I discuss below, these same components could be applied to a PoP structure, which has a similar pitch to chip-on-substrate structures, similar to that disclosed by *Love*. Additionally, *Love* teaches that its design has the advantages of reducing mechanical stress due to product warping, EX1007 at 10:5–23, and reducing required alignment tolerances when stacking pillars, EX1007 at 13:16–37.

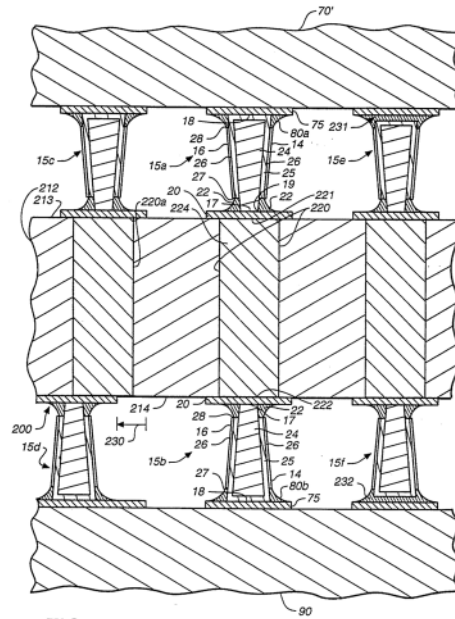


FIG. 5

EX1007 at FIG. 5.

97. Accordingly, *Love* is in the same field of endeavor as the '202 Patent—interconnect structures having a stacked pillar design—as the '202 Patent, and in my opinion a POSITA would have understood that *Love* provides an alternative design that would have been available to a POSITA at the time of invention, which provides the advantages discussed above.

D. *Hu* (EX1008)

98. *Hu* was filed on January 30, 2013 and published on September 26, 2013. EX1008. The '202 Patent was filed on June 23, 2016 and claims priority to US Provisional Patent Application No. 62/184,034, dated June 24, 2015. *Hu* thus predates the '202 Patent by over a year.

99. *Hu* discloses a PoP structure where two package substrates are

interconnected by stacked metal pillars. EX1008 at [0001], [0010]–[0011], FIG. 3. In particular, *Hu* discloses that packaging substrates 30 can be stacked and spaced apart by external connection structures 27a-b, which comprise “metal posts.” *Id.* As I describe in § XIV.A, a POSITA would have recognized the external connection structures 27a-b, 300 as “metal pillars.” Additionally, *Hu* teaches that its design provides the benefit of improving the uniformity of metal posts, such that they have similar heights. EX1008 at [0030].

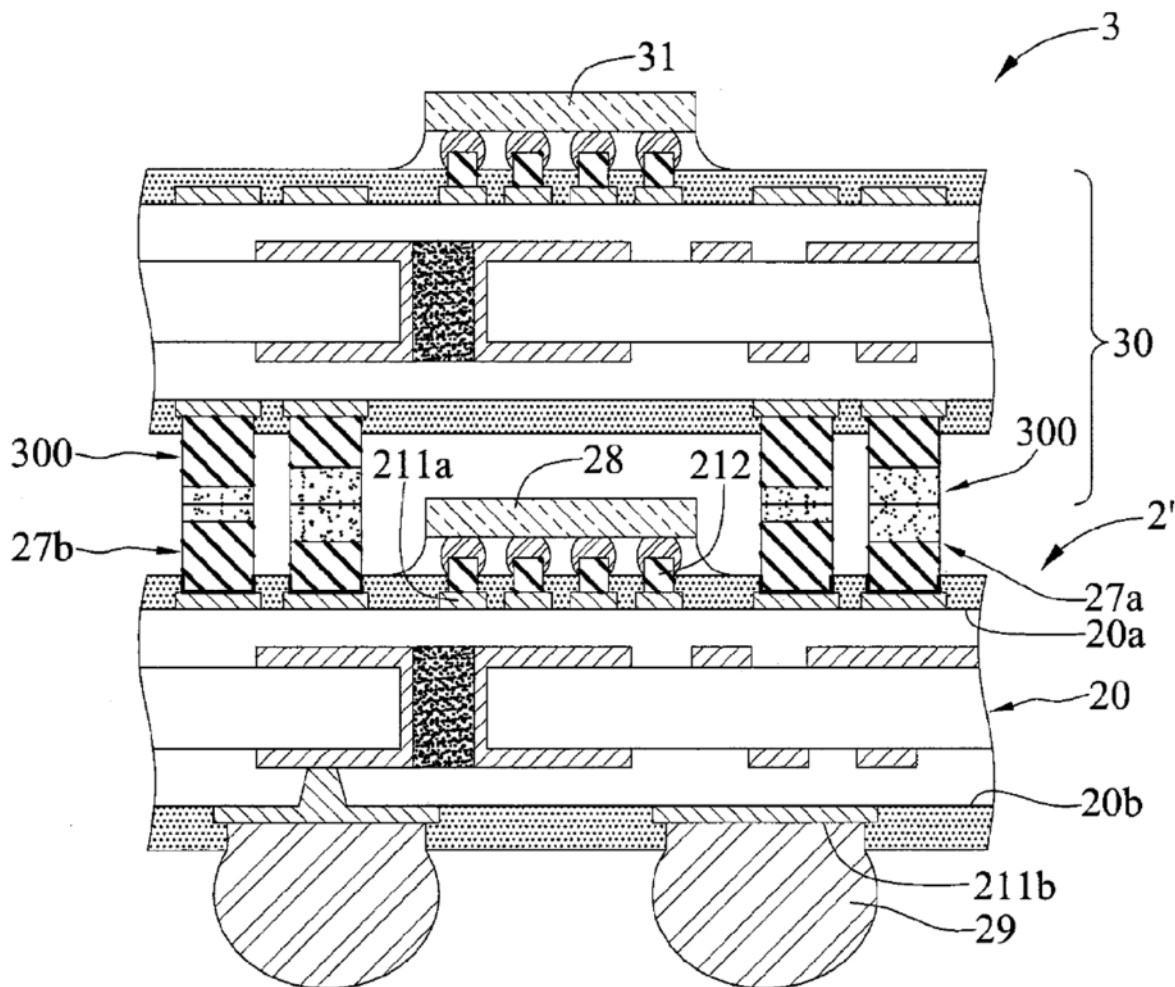


FIG.3

EX1008 at FIG. 3.

100. Accordingly, *Hu* is in the same field of endeavor as the '202 Patent—PoP structures having stacked metal pillars—as the '202 Patent, and in my opinion a POSITA would have understood that *Hu* provides an alternative design that would have been available to a POSITA at the time of invention, which provides the advantages discussed above.

E. *Benson* (EX1009)

101. *Benson* is an academic article titled “Polymer Adhesives and Encapsulants for Microelectronic Applications,” which was published in 2008 by Johns Hopkins APL Technical Digest. EX1012 at ¶¶48-56. The ’202 Patent was filed on June 23, 2016 and claims priority to US Provisional Patent Application No. 62/184,034, dated June 24, 2015. *Benson* thus predates the ’202 Patent by over a year.

102. *Benson* discloses the use of polymer adhesives in “microelectronic packaging” EX1009 at 1. *Benson* discloses “the general types of materials used to formulate polymer adhesives for die attachment, underfills, and encapsulants, along with their properties.” EX1009 at 13. *Benson* discloses various “underfills” applications of “polymer adhesives,” *id.* at 6–7, and also teaches “[w]hen thermal or electrical conductivity is not required, insulating polymer adhesives are used for bonding... semiconductor die to substrates,” *id.* at 3.

103. *Benson* is in the same field of endeavor—microelectronic packaging—as the ’202 Patent, and in my opinion a POSITA would have understood that *Benson* provides specific guidance regarding the use of adhesives and underfills in such applications.

F. *Waite* (EX1010)

104. *Waite* was filed on March 30, 2010, issued on February 29, 2013.

EX1010. The '202 Patent was filed on June 23, 2016 and claims priority to US Provisional Patent Application No. 62/184,034, dated June 24, 2015. *Waite* thus predates the '202 Patent by over a year.

105. *Waite* discloses a stacked PCB design, which includes a spacer connector interposed between two boards. EX1010 at 4:19–26. In particular, *Waite* discloses that its spacer connector “interfaces between daughter boards connected to printed circuit boards and test equipment interfaces.” *Id.* *Waite*’s daughter board 202 is stacked onto a spacer connector 204, which is further stacked onto a motherboard 200. EX1010 at 6:25–28, FIG. 7. The electrical connections between the daughter board 202 and motherboard 200 are routed through conductive elements 302 and vias 402, 428. EX1010 at 4:19–26. As I describe in § XVI.B, a POSITA would have recognized the conductive elements 302 and vias 402, 428 as “metal pillars.”

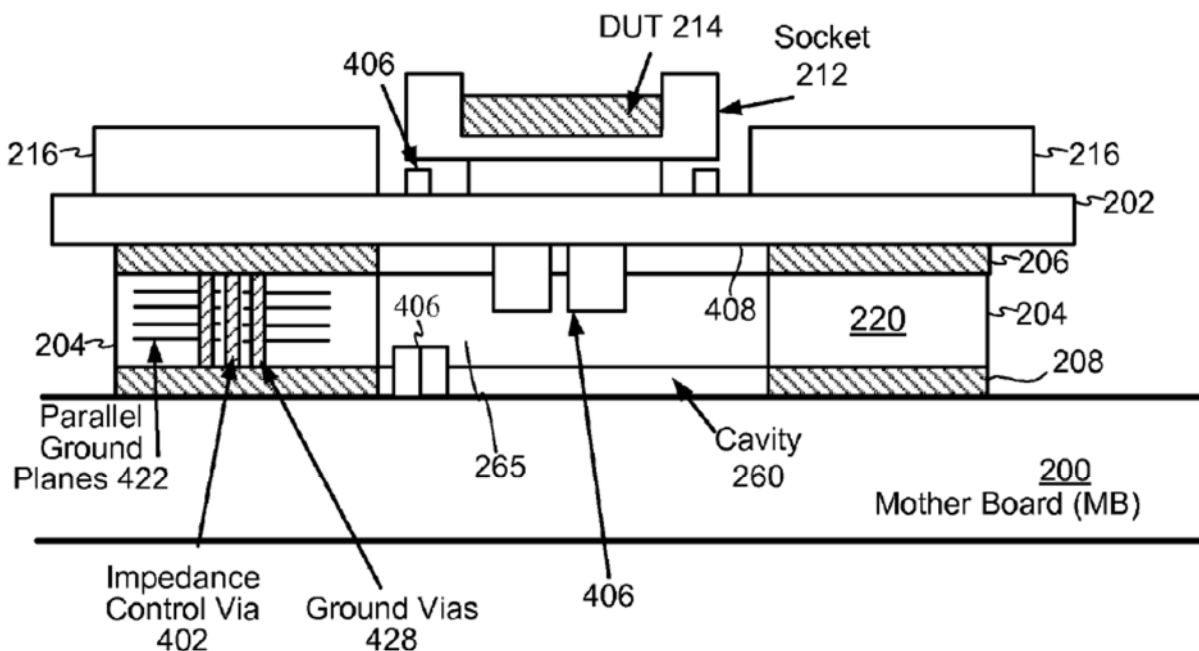


FIG. 4A

EX1010 at FIG. 4A, 4:12–19.

106. According to Patent Owner’s apparent construction, which reads the terms “package substrate” to include logic boards (i.e., PCBs) of the accused device, *Waite* is in the same field of endeavor—PCB stacking designs utilizing spacer connectors, and in my opinion a POSITA would have understood that *Waite* provides an alternative design that would have been available to a POSITA at the time of invention. See EX1004 at ¶¶41, 42.

G. IPC-4761 (EX1011)

107. *IPC-4761* is titled “Design Guide for Protection of Printed Board Via Structures,” and was published in July 2006 by the IPC Global Electronics Association. EX1012 at ¶¶57-63. *IPC-4761* “provides [printed wiring board]

designers, fabricators, and/or users with information on existing methods for the protection of vias on printed boards.” EX1011 at 1. *IPC-4761* discloses that a metal cap can be applied to the top and bottom of metal vias, which will prevent solder, solder resist, or other contaminants from entering or flowing through the vias. EX1011 at 2, 7, 9–10. As I describe in § XVI.B, a POSITA would have recognized the vias as “metal pillars.”

108. *IPC-4761* is in the same field of endeavor—metal pillar applications—as the ’202 Patent, and in my opinion a POSITA would have understood that *IPC-4761* provides a standard design that would have been available to a POSITA at the time of invention, which provides the advantages discussed above.

IX. SUMMARY OF PRIOR ART GROUNDS

Petitioner’s or Patent Owner’s Claim Interpretations			
Ground	Claims	Basis	Prior Art
1	1–4, 6–9	Anticipation	<i>Sun</i>
2	1–4, 6–9	Obviousness	<i>Sun</i>
3	1–4, 6–9	Obviousness	<i>Sun with Love</i>
4	1–4, 6–9	Obviousness	<i>Sun with Hu</i>
5	1–2, 4–9	Anticipation	<i>Chen</i>
6	1–9	Obviousness	<i>Chen</i>
7	1–9	Obviousness	<i>Chen with Hu</i>

8	8	Obviousness	<i>Chen with Hu and Benson</i>
Patent Owner's Potential Claim Interpretations			
Ground	Claims	Basis	Prior Art
9	1–2, 4, 6, 9	Obviousness	<i>Waite with IPC-4761</i>

X. GROUND 1–2: *SUN* ANTICIPATES AND/OR RENDERS OBVIOUS CLAIMS 1–4 AND 6–9

109. In my opinion, *Sun* anticipates and/or renders obvious claims 1–4 and 6–9.

A. Claim 1

i. 1[pre]: A structure

110. *Sun* discloses “a structure.” *Sun* discloses a “PoP assembly 1,” which corresponds to a semiconductor packaging “structure.” EX1005 at [0058]. *Sun*’s PoP assembly 1 is very similar to the claimed “structure,” which includes a bottom package substrate, top package substrate, spacer connector, metal pillars, bottom metal pillars, and top metal pillars, as shown below. EX1001 at 3:32–4:64. For example, as shown below, *Sun*’s Figure 12 is similar to Figure 11 of the ’202 Patent.

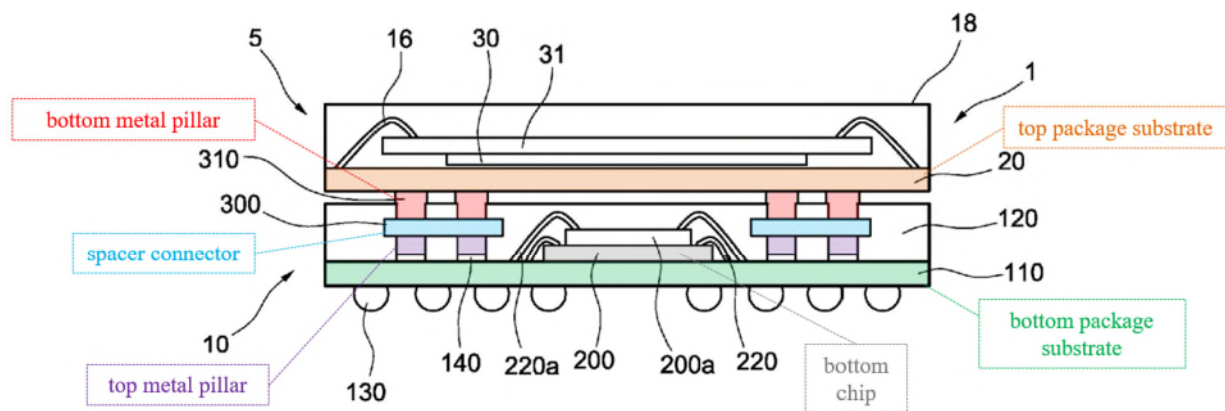
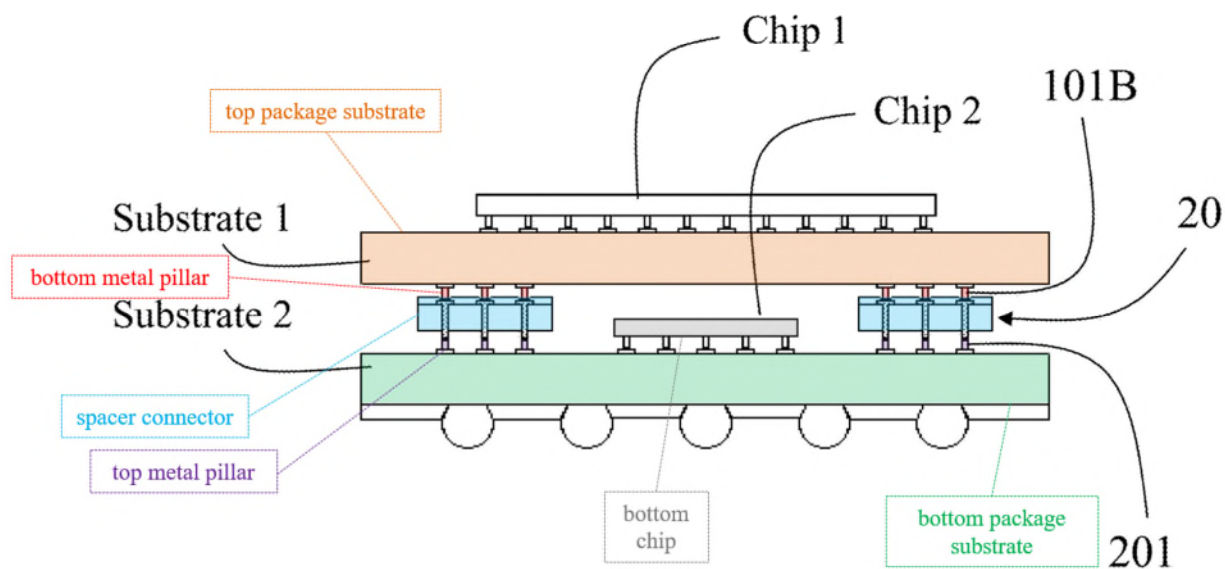


FIG.12

EX1005 at FIG. 12.

Fig.11



EX1001 at FIG. 11

111. Thus, in my opinion, *Sun* discloses each limitation of claim 1[pre].

ii. 1[a]: a bottom package substrate

112. *Sun* discloses “a bottom package substrate.” *Sun* discloses a first substrate 110 of PoP assembly 1, which corresponds to the claimed bottom package substrate. EX1005 at [0047]–[0048]. In particular, *Sun*’s first substrate 110 (bottom package substrate) is a “package substrate.” It interfaces directly with a chip 200 (bottom chip) and a motherboard, consistent with the function of a semiconductor package substrate. EX1005 at [0047]–[0048] (“Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A chip 200, which may be a memory chip or a processor, is mounted to the first substrate 110.”), FIG. 12 (the motherboard is omitted from FIG. 12, but would be disposed on the bottom surface of solder balls 130); *see also* my prior discussion regarding package substrates in §V.H. Additionally, the first substrate 110 is a “bottom” package substrate, arranged at the bottom of the PoP assembly 1, as shown in Figure 12 of *Sun*.

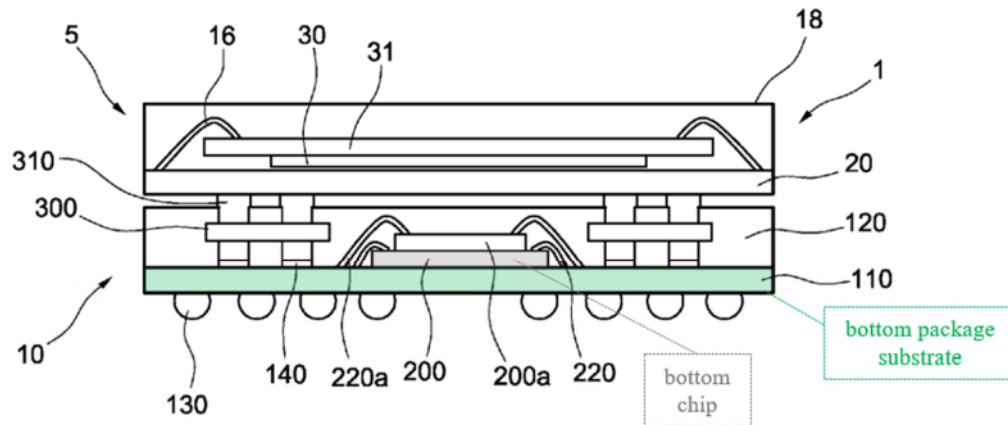


FIG.12

EX1005 at FIG. 12.

113. Thus, in my opinion, *Sun* discloses each limitation of claim 1[a].

iii. 1[b]: a top package substrate stacked on top of the bottom package substrate

114. *Sun* discloses “a top package substrate stacked on top of the bottom package substrate.” *Sun* discloses a third substrate 20 (top package substrate) stacked on top of the first substrate 110 (bottom package substrate). EX1005 at [0059], FIG. 12. Similar to first substrate 110 (bottom package substrate), the third substrate 20 (top package substrate) is also a “package substrate.” It interfaces directly with chips 30, 31 (top chips) and second substrates 300 (spacer connectors), consistent with the role of semiconductor package substrates. EX1005 at [0059] (“a pair of chips 30, 31 [are] mounted to a first (upper) side of a third substrate 20.... The second (lower) side of the third substrate 20 is mounted to the first module 10 [(which includes second substrates 300 and first substrate 110)].”), FIG. 12.

Additionally, **third substrate 20** is a “top” package substrate, arranged at the top of PoP assembly 1, as shown in Figure 12 of *Sun*.

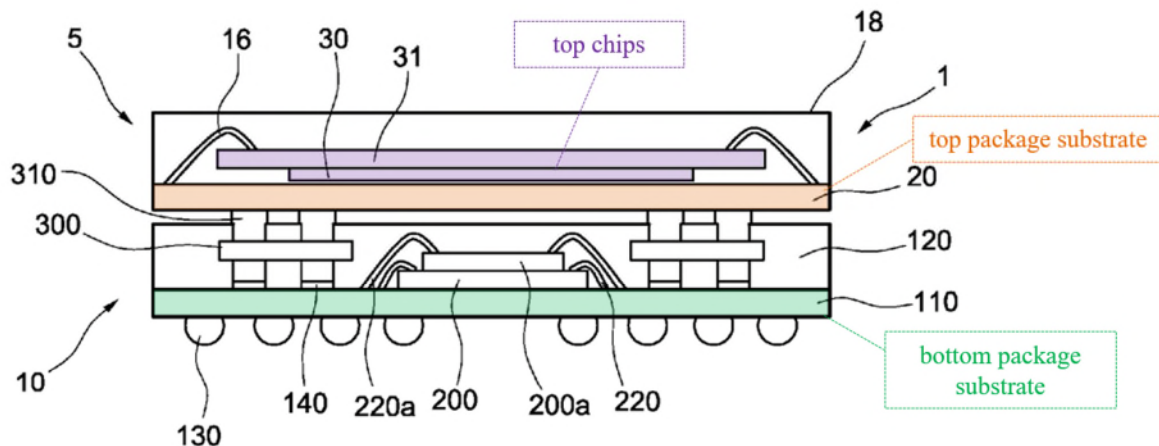


FIG.12

EX1005 at FIG. 12.

115. Thus, in my opinion, *Sun* discloses each limitation of claim 1[b].

- iv. **1[c]: at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate**

116. *Sun* discloses “at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.” *Sun* discloses **second substrates 300** (spacer connectors) interposed between **first substrate 110** (bottom package substrate) and **third substrate 20** (top package substrate) to define a space between **first substrate 110** and **third substrate 20**. As an initial matter, a POSITA

would have understood that the term “interposed,” as used in limitation 1[c], requires the spacer connector to “be between” the bottom package substrate and the top package substrate. Merriam Webster, *Interposed*, <https://www.merriam-webster.com/dictionary/interposed> (last visited Mar. 10, 2026) (defining “interpose” as “to be or come between”). Indeed, as shown below, Sun’s **second substrates 300** (spacer connectors) are between the **third substrate 20** (top package substrate) and the **first substrate 110** (bottom package substrate), and thus interpose these substrates. EX1005 at FIG. 12. Additionally, as shown below, the **second substrates 300** (spacer connectors) define a space between the **third substrate 20** (top package substrate) and the **first substrate 110** (bottom package substrate). Sun identifies the problem in the prior art that “the space between the upper and lower packages is limited,” and notes that “[i]t would be desirable to increase the vertical separation (stand off height) in order to make room for more and larger chips and enable stacking of chips on the lower substrate.”). EX1005 at [0010]. Additionally, Sun discloses that “[a]s the lower module has a second substrate with electrical connectors on either side, the stand off height may be increased.” *Id.* at [0014]. As shown in Figure, 12, this increased stand off height is accomplished by implementing **second substrates 300** (spacer connectors).

“insulating layer,” which a POSITA would have understood is commonly used as a core substrate in semiconductor package. EX1005 at [0065].

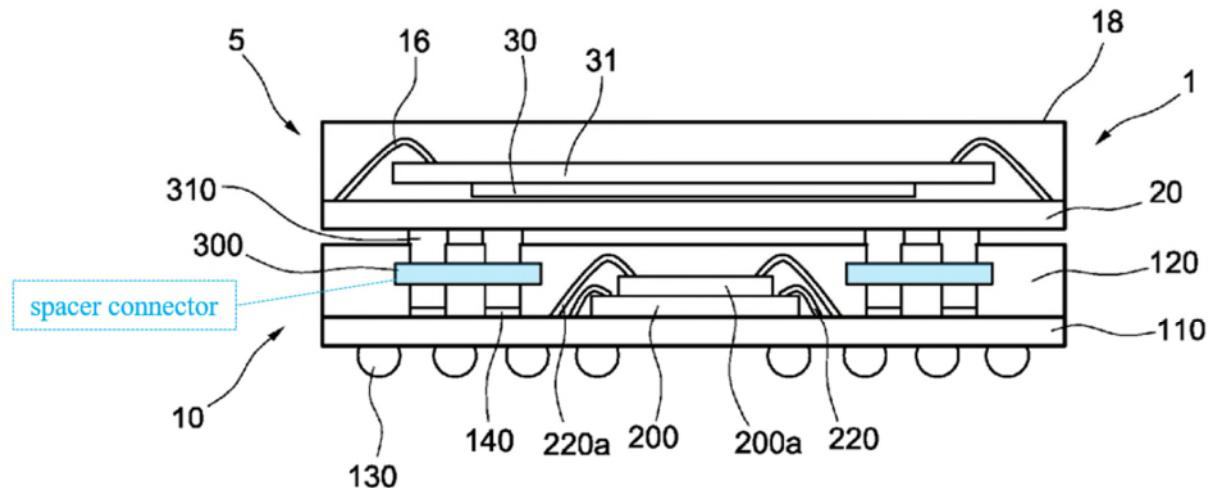


FIG.12

EX1005 at FIG. 12.

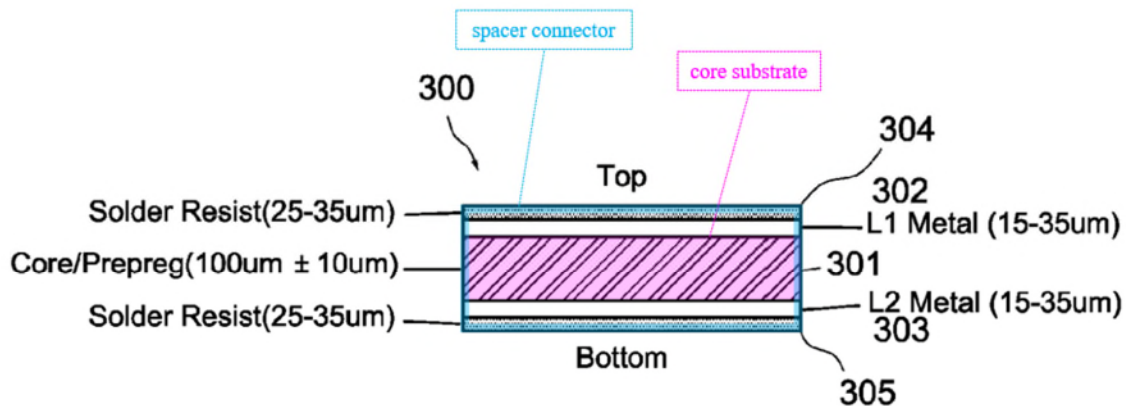


FIG.15

EX1005 at FIG. 15.

119. Thus, in my opinion, *Sun* discloses each limitation of claim 1[d].

vi. 1[e]: a plurality of metal pillars, each passing through the core substrate

120. *Sun* discloses “a plurality of metal pillars, each passing through the core substrate.” *Sun*’s second substrates 300 (spacer connectors) include a plurality of vias 390 (metal pillars), each passing through the core/prepreg insulating layer 301 (core substrate). EX1005 at [0062]–[0063] (“Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320. The vias extend through the second substrate 300.”). A POSITA would have understood that *Sun*’s “vias” are metal pillars (i.e., pillars made of metal), as they are metal structures extending through the substrate. For example, *Sun* teaches that “[e]ach via typically comprises first and second electrically conductive side walls. The first and second side walls are electrically connected to each other by the first electrical connector and said second electrical connector (at either end of the via). The term side walls as used herein includes the situation where the two ‘side walls’ are part of the same wall, e.g. different parts of a circular wall.” EX1005 at [0017]–[0018]. Additionally, *Sun* discloses that “the side walls 391, 392 are electrically conductive (e.g. made of metal).” *Id.* at [0063]–[0064]. As shown in Figure 13, the vias 390 extend vertically, and take on a “pillar” shape. As shown below, the vias 390 (metal pillars) pass through the core/prepreg insulating layer 301 (core substrate). EX1005 at [0062]–[0063] (“vias 390 extend through the second substrate 300”), [0065], FIG. 13 (showing that the vias 390 extend entirely through the second substrate 300, which

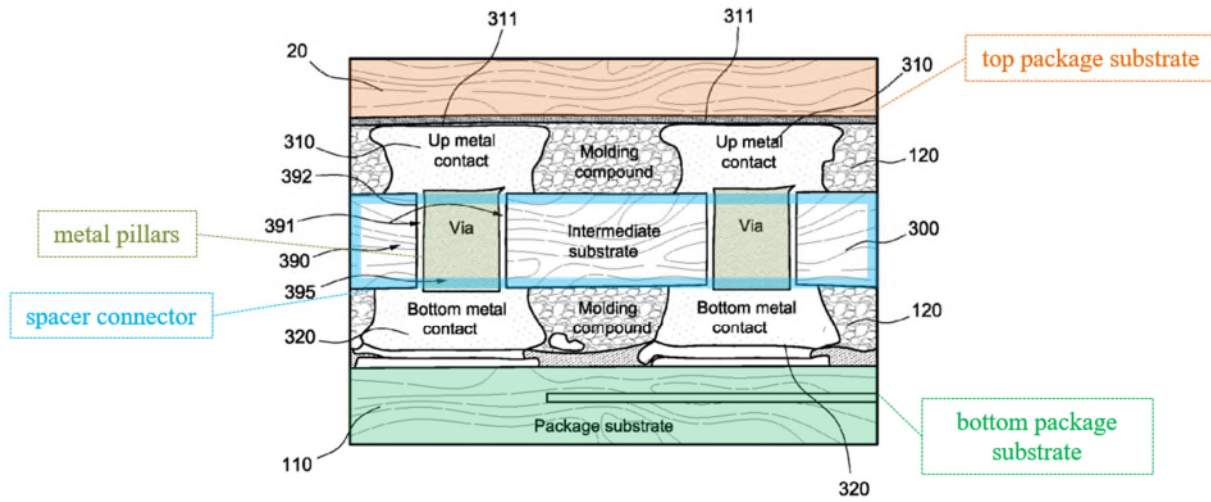


FIG.13

EX1005 at FIG. 13.

121. Thus, in my opinion, *Sun* discloses each limitation of claim 1[e].

vii. **1[f]: a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars**

122. *Sun* discloses and/or renders obvious “a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.” *Sun*’s **second substrates 300** (spacer connectors) include a plurality of **bonding pads** (top metal pads), each on a top end of a corresponding **via 390** (metal pillar) among the plurality of **vias 390**.

123. For example, paragraph [0066] of *Sun* addresses the connection between *Sun*'s third substrate 20 (top package substrate) and second substrates 300

(spacer connectors). In this paragraph, *Sun* discloses that “bonding pads may [be] used to connect the metal pillars to the respective other substrates.” EX1005 at [0066]. Here, *Sun* does not limit the application of the bonding pads to any particular metal pillar or substrate. A POSITA would have understood that *Sun* provides a general teaching for applying bonding pads to facilitate metal pillar-substrate connection, as is commonly done in the art. For example, a POSITA would have understood bonding pads are metal pads, which are often deposited over a via for solder connections. EX1005 at [0048] (the metal connectors can be connected to the first substrate 110 via “solder bonding or intermetallic bonding”), [0074] (a bonding pad can be an electrical contact).

124. The specification and figures of *Sun* make it clear to a POSITA that the bonding pads can be and are applied to the top ends of each **via 390** (metal pillar). Figure 14(a) shows **bonding pads** disposed on top of the **vias 390** (metal pillars) to facilitate the electrical connection between the **vias 390** and the **third substrate 20** (top package substrate). In particular, Figure 14(a), which “shows a pair of metal pillars used as electrical connectors between two substrates,” includes a solid black line bisecting the electrical connection between the **second substrate 300** (spacer connector) and **third substrate 20** (top package substrate). EX1005 at [0043], Figure 14(a). In reference to this figure, *Sun* explains that “bonding pads may used to connect the metal pillars to the respective other substrates.” *Id.* at [0066]. While the

vias 390 (metal pillars) are omitted from Figure 14(a), it is clear from other figures (e.g., Figure 13) and the specification that the electrical connection interfaces with vias 390 (metal pillars), which extend through the second substrates 300 (spacer connectors) and connects first substrate 110 (bottom package substrate). EX1005 at [0062].

125. The solid black line in Figure 14(a) separates the second metal connectors 310 (bottom metal pillars) from the bonding pads (top metal pads). EX1005 at [0066]. Specifically, as shown below, the portion of the electrical connection below this line corresponds to bonding pads (top metal pads), which are disposed on the top end of each via 390 (metal pillar). EX1005 at [0066].

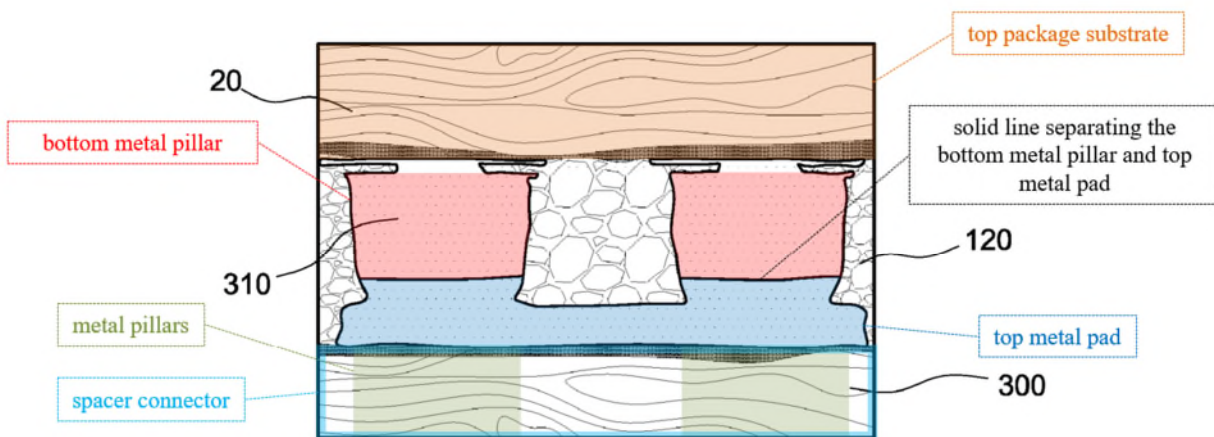


FIG.14(a)

EX1005 at FIG. 14(a).

126. However, if the Board finds that *Sun* may not explicitly disclose or illustrate that the bonding pads (top metal pads) are be applied to the top ends of

each **via 390** (metal pillar), there are several reasons for which a POSITA would have found it obvious to do so.

127. First, certain embodiments of *Sun*'s **vias 390** would require a top metal pad to facilitate a reliable electrical connection to the **second metal connectors 310** (bottom metal pillars). In particular, *Sun* discloses that **vias 390** (metal pillars) have sidewalls 310, 320 and a core 395. EX1005 at [0063]–[0064], FIG. 13. *Sun* teaches, in some embodiments, the core 395 can be a void, and thus the **vias 390** (metal pillars) are hollow. EX1005 at [0064] (“In alternative embodiments the core could instead b[e] a... void.”). In other embodiments, however, “[t]he core 395 of the via is an insulator.” EX1005 at [0064]. In both cases, the only conductive surface of the **vias 390** (metal pillars) would be the sidewalls 310. EX1005 at [0064] (stating “side walls 391, 392 are electrically conductive (e.g. made of metal)”). Here, the cross-sectional area of the sidewalls 310 would be small as they are walls of a small hollow cylinder (i.e., a via with a center void). Since the insulator or void core 395 is neither solder-wettable nor conductive, it would not provide a desirable surface for connecting to another metal pillar. Accordingly, a POSITA would have found it obvious to apply metal pads to the top ends of **vias 390** (metal pillars) to provide a suitable surface area to facilitate a reliable electrical connection between the **vias 390** (metal pillars) and **second metal connectors 310** (bottom metal pillars). EX1016 at 95 (“[a] solder wettable surface like copper or nickel is needed to place solder

bumps on”); EX1014 at 33.

128. Second, *Sun* teaches that the **second metal connectors 310** (bottom metal pillars) are stacked on top of **vias 390** (metal pillars), and thus a POSITA would have found it obvious to apply top metal pads to reduce the complexity of stacking two sets of narrow metal pillars. For example, top metal pads disposed on the top ends of **vias 390** (metal pillars) would provide a wider landing area for the **second metal connectors 310** (bottom metal pillars), such that misalignment errors during the manufacturing and assembly processes would not impact the reliability of the PoP assembly. This technique was well-known in the prior art. *See, e.g.*, EX1007 at 13:12–41 (teaching that wide pads can be applied to stacked metal pillars to allow for misalignment errors).

129. Third, a POSITA would have found it obvious to apply top metal pads to **vias 390** (metal pillars) to prevent other materials from flowing into or through the metal pillars during the manufacturing process. In particular, it was well-known at the time of invention that metal pillar designs having no top metal pad suffer from the problem that solder, solder resist, or contaminants can flow into or through the metal pillar. EX1011 at 7, 10 (noting “this document does recognize manufacturing processes where solder mask flows into the hole during liquid solder mask application, without intending to provide complete coverage or protection, and may result in partial plugging. This is not acceptable with bare copper surface finishes.”).

This problem would be especially applicable to *Sun*'s **vias 390** (metal pillars), which as discussed above, can be hollow. EX1005 at [0064]. A POSITA would therefore have found it obvious to apply top metal pads to the top ends of the **vias 390** (metal pillars) to provide adequate protection during manufacturing and assembly by preventing solder, solder resist, or contaminants from entering or passing through the **vias 390** (metal pillars). *See also* EX1011 at 7, 10, Table 5-1 (showing that “capped” vias provide such protective benefits).

130. Thus, in my opinion, *Sun* discloses and/or renders obvious each limitation of claim 1[f].

viii. 1[g]: wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate

131. *Sun* discloses “wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.” *Sun* discloses the bottom end of each **via 390** (metal pillar) among the plurality of **vias 390** protrudes downwardly from a bottom surface of the **core/prepreg insulating layer 301** (core substrate). For example, *Sun* teaches that “[t]he vias 390 extend through the second substrate 300.” EX1005 at [0063]. As shown in *Sun*'s FIG. 13, the **vias 390** extend all the way through the **second substrate 300** (spacer connector). Accordingly, *Sun*'s **vias 390** protrude below the **core/prepreg insulating layer 301** (core substrate), which is a middle layer of the

second substrate 300 and is disposed above its bottom surface, as shown below.

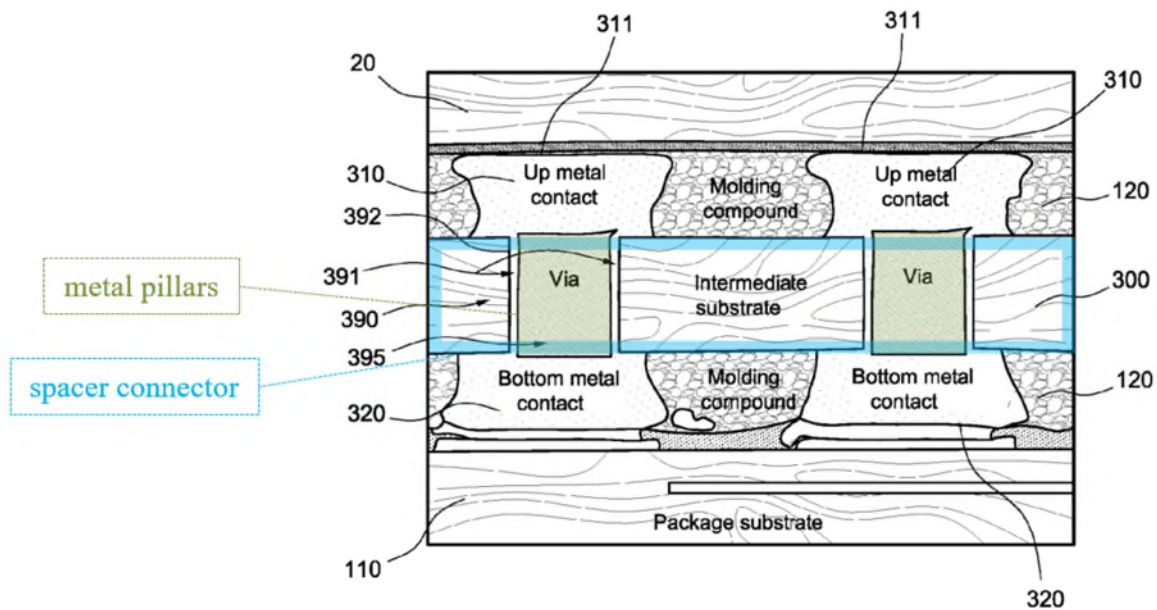


FIG.13

EX1005 at FIG. 13 (showing vias 390 extend all the way through the second substrate 300).

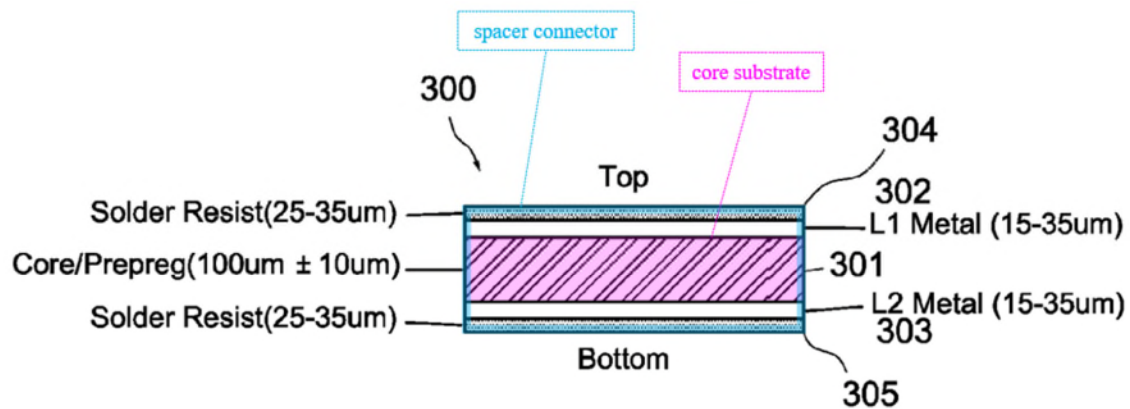


FIG.15

EX1005 at FIG. 15 (showing core/prepreg insulating layer 301 as a middle layer of the second substrate 300).

of **second substrate 300** (spacer connector). For example, *Sun* discloses “[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” EX1005 at [0063]. *Sun* further states “[p]referably the first and second electrical connectors are metal pillars, e.g. copper pillars...[and] solder joints may be used to join the metal pillars to a substrate above or below.” *Id.* at [0015]. Limitation 1[h] is clearly shown in Figure 13, which illustrates that a top end of each **second metal connector 310** (bottom metal pillar) is electrically connected to the bottom surface of the **third substrate 20** (top package substrate), and a bottom end is electrically connected to **vias 390** (metal pillars).

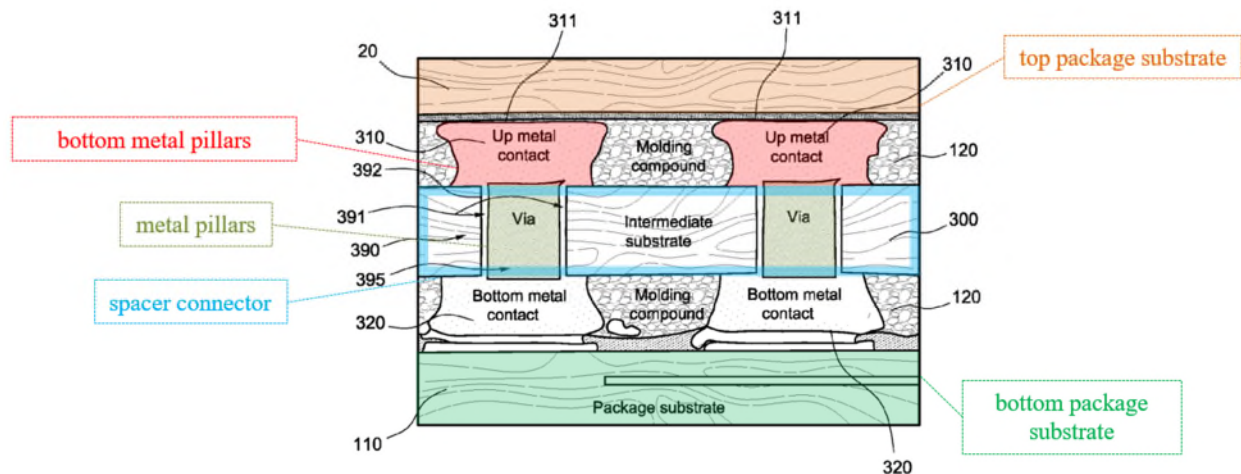


FIG.13

EX1005 at FIG. 13.

134. Thus, in my opinion, *Sun* discloses each limitation of claim 1[h].

- x. **1[i]: the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a**

corresponding metal pillar among the plurality of metal pillars of the spacer connector

135. *Sun* discloses “the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.” *Sun* discloses the **first substrate 110** (bottom package substrate) has, on a top surface thereof, a plurality of **first metal connectors 320** (top metal pillars) each coupled to a corresponding **via 390** (metal pillar) among the plurality of **vias 390** (metal pillars) of **second substrate 300** (spacer connector). *Sun* discloses that “[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320” on opposite sides of the second substrates 300 (spacer connector). EX1005 at [0063]; *see also id.* at [0015] (“Preferably there are a plurality of first electrical connectors and a plurality of second electrical connectors. For example, there may be four or more first electrical connectors on the underside of the second substrate and four or more second electrical connectors on the top side of the second substrate”). Similar to the bottom metal pillars, Figure 13 shows that a bottom end of each **first metal connector 320** (top metal pillar) is electrically connected to the top surface of the **first substrate 110** (bottom package substrate), and a top end of the **first metal connector 320** is electrically connected to **vias 390** (metal pillars).

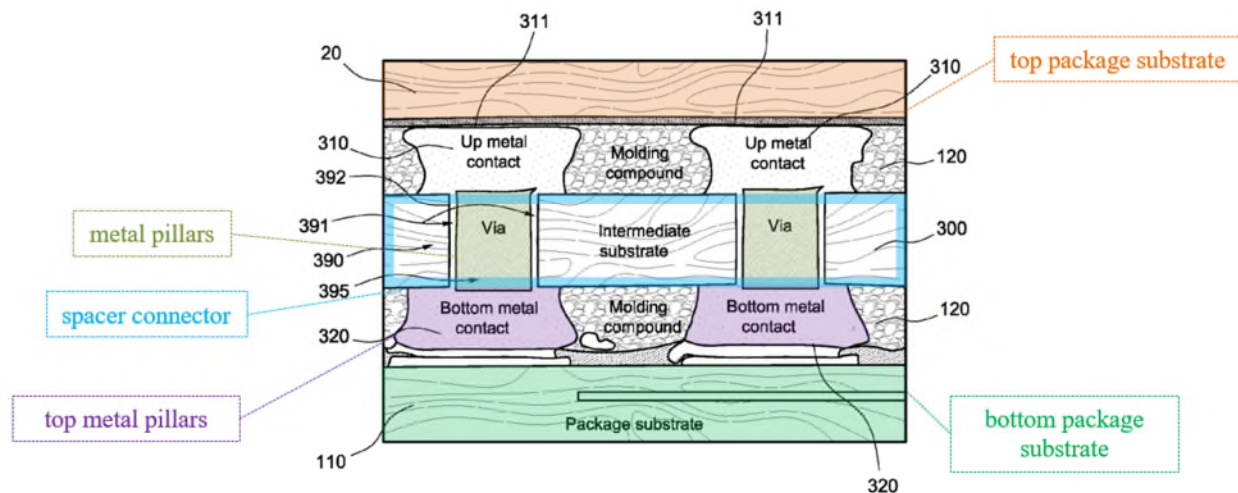


FIG.13

EX1005 at FIG. 13.

136. Thus, in my opinion, *Sun* discloses each limitation of claim 1[i].

- xi. 1[j]: the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate

137. *Sun* discloses “the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.” *Sun* discloses the third substrate 20 (top package substrate) is electrically coupled to the first substrate 110 (bottom package substrate) through the plurality of the second metal connectors 310 (bottom metal pillars) of the third substrate 20 (top package substrate), the

plurality of **vias 390** (metal pillars) of **second substrate 300** (spacer connector), and the plurality of the **first metal connectors 320** (top metal pillars) of the **first substrate 110** (bottom package substrate).

138. For example, *Sun* discloses “the first substrate being electrically connected to the second substrate by at least one first electrical connector; and at least one second electrical connector extending from the second substrate through the overmold and having an exposed end for electrical connection to an external module.” EX1005 at [0012]–[0013]. *Sun* further discloses that “[p]referably there are a plurality of first electrical connectors and a plurality of second electrical connectors. For example, there may be four or more first electrical connectors on the underside of the second substrate and four or more second electrical connectors on the top side of the second substrate.” *Id.* at [0015]. Further, “[t]he second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110” (*Id.* at [0015]), and “[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” *Id.* at [0063]. “[E]lectrical contacts (e.g. bonding pads or lands) present on the second (lower) side of the third substrate are placed in contact with the exposed ends of the second electrical connectors 310 of the first module 10.” *Id.* at [0074].

139. This connection structure is further illustrated in Figure 13, which shows that the **third substrate 20** (top package substrate) is electrically coupled to

the first substrate 110 (bottom package substrate) through vertically stacked second metal connectors 320 (bottom metal pillars), vias 390 (metal pillars), and first metal connectors 320 (bottom metal pillars).

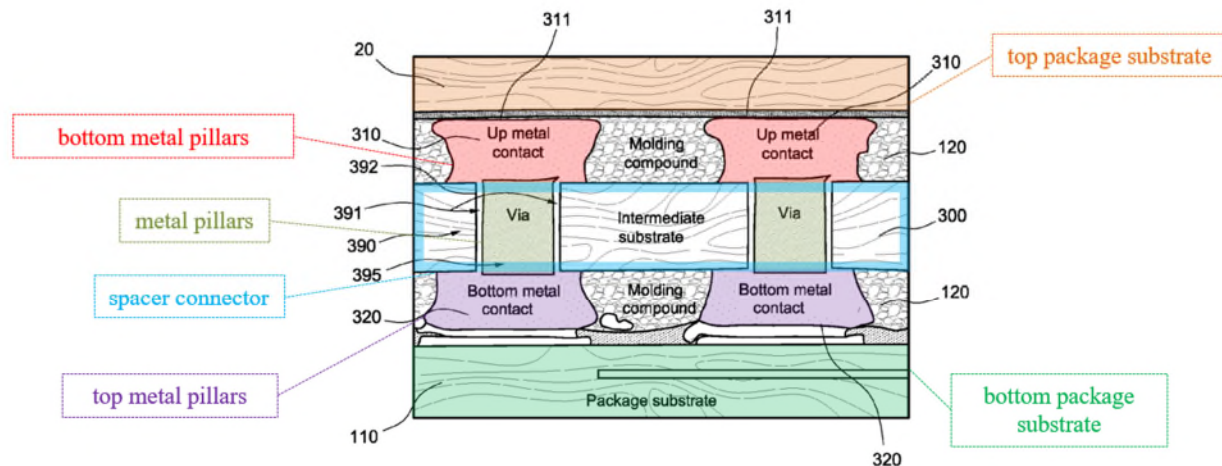


FIG.13

EX1005 at FIG. 13.

140. I note that limitation 1[j] recites “bottom metal pillars *of* the top package substrate” and “top metal pillars *of* the bottom package substrate.” As I explained above, the preposition “of” in the above terms indicates an association between the metal pillars and the package substrates. A POSITA would have understood that the bottom pillars are located on the bottom of the top package substrate, and are thus “bottom metal pillars of the top package structure.” Similarly, the top pillars are located on the top of the bottom package substrate, and are thus “top metal pillars of the bottom package substrate.” This is consistent with

limitations 1[h] and 1[i], as discussed above, as well as Figures 8, 11, and 14 of the '202 Patent.

141. Thus, in my opinion, *Sun* discloses each limitation of claim 1[j].

xii. 1[k]: a bottom chip arranged in the space between the bottom package substrate and the top package substrate

142. *Sun* discloses “a bottom chip arranged in the space between the bottom package substrate and the top package substrate.” *Sun* discloses a chip 200 (bottom chip) arranged in the space between the first substrate 110 (bottom package substrate) and the third substrate 20 (top package substrate). For example, *Sun* discloses that “[a] pair of chips 200, 200a... are mounted to the first substrate 110.” EX1005 at [0060]–[0061]. As shown in Figure 12, chip 200 (bottom chip) is mounted on the first substrate 110 (bottom package substrate), such that it is arranged in a space between the first substrate 110 (bottom package substrate) and the third substrate 20 (top package substrate).

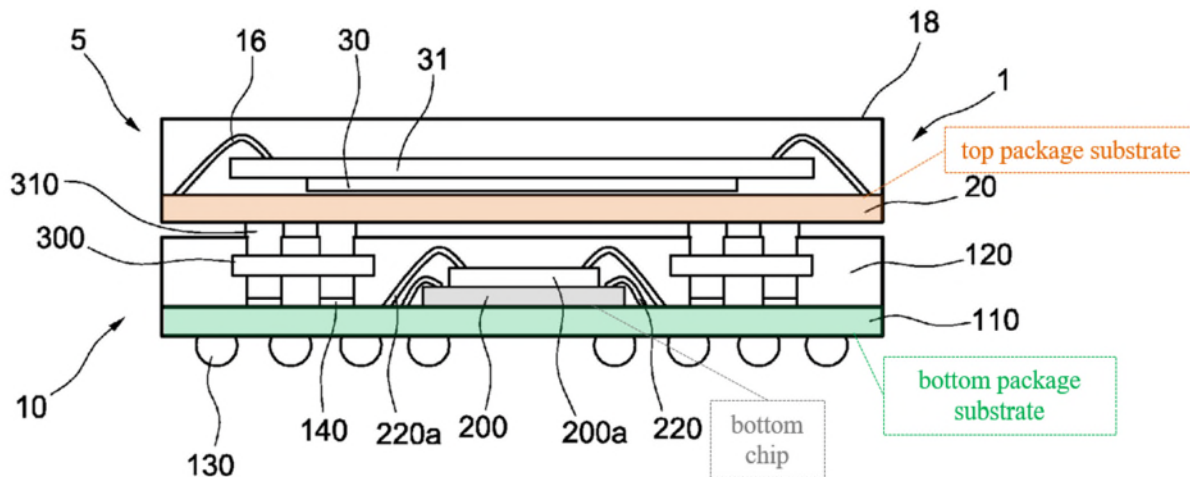


FIG.12

EX1005 at FIG. 12.

143. Thus, in my opinion, *Sun* discloses each limitation of claim 1[k].

xiii. 1[l]: the bottom chip is mounted to the top surface of the bottom package substrate

144. *Sun* discloses “the bottom chip is mounted to the top surface of the bottom package substrate.” *Sun* discloses the chip 200 (bottom chip) is mounted to the top surface of the first substrate 110 (bottom package substrate). EX1005 at [0060] (chip 200 is “mounted to the first substrate 110”). This is further illustrated in Figure 12 below, which shows “two chips 200, 200a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220a respectively. EX1005 at [0058].

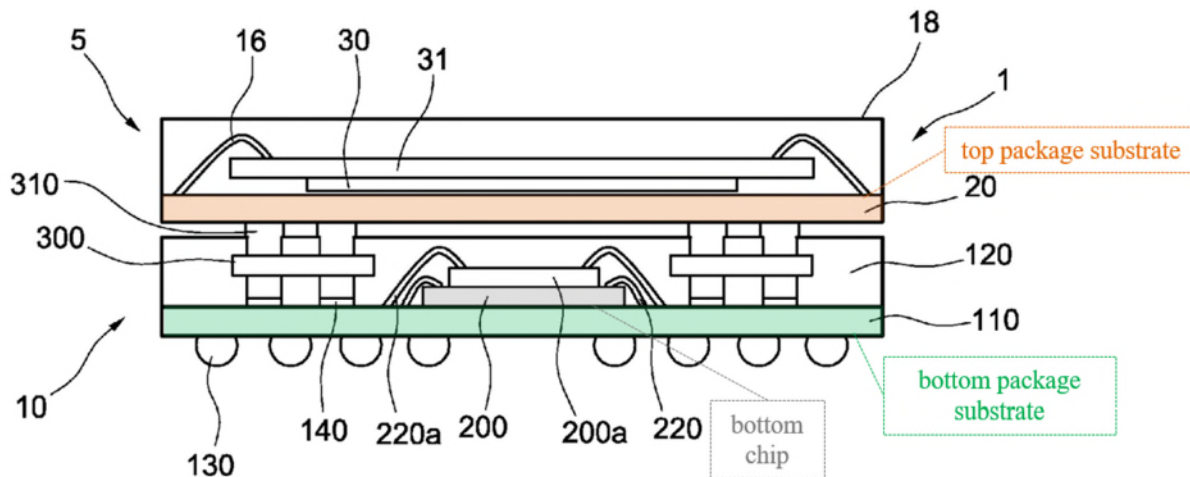


FIG.12

EX1005 at FIG. 12.

145. Thus, in my opinion, *Sun* discloses each limitation of claim 1[l].

xiv. 1[m]: the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip

146. *Sun* discloses “the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.” *Sun* discloses two **second substrates 300** (spacer connectors) arranged on opposite sides of chip 200 (bottom chip). For example, *Sun* teaches that “[t]he second substrate 300 has an opening therein for accommodating the chips 200, 200a,” and each side of the second substrate (spacer connector) “has a gap” “join[ing] the central opening.” EX1005 at [0061], [0055], [0059], FIGs. 9, 12. *Sun* further discloses that “the opening in the second substrate makes room for one or more chips mounted to the first substrate.” EX1005 at [0014]. As illustrated in *Sun*’s Figures 9 and 12, the “opening” and

“gaps” separate two spacer connectors, which are arranged on opposite sides of the bottom chip.

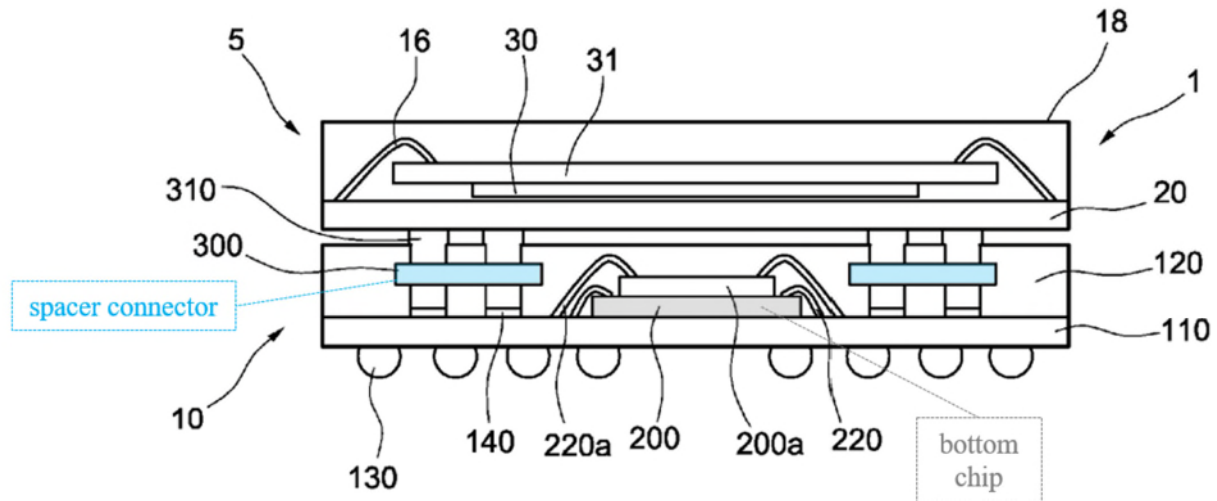


FIG.12

EX1005 at FIG. 12.

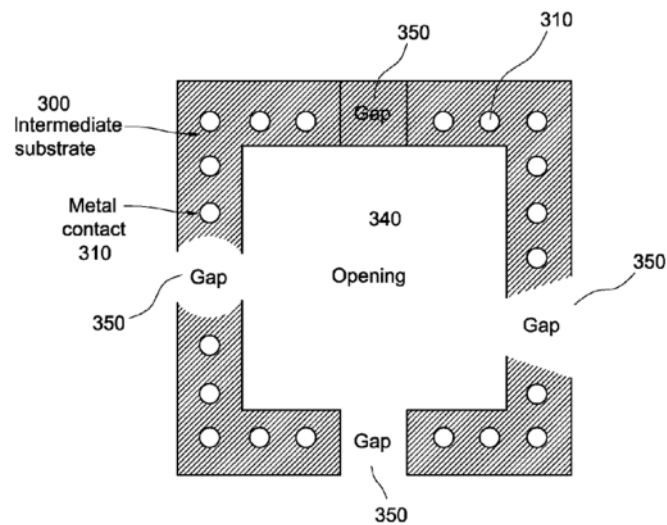


FIG.9

EX1005 at FIG. 9.

147. Thus, in my opinion, *Sun* discloses each limitation of claim 1[m].

B. Claim 2

i. the structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate

148. *Sun* discloses “the structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.” *Sun* discloses the top surface of chip 200 (bottom chip) is spaced downwardly from the bottom surface of third substrate 20 (top package substrate). *Sun* teaches that the “pair of chips 200, 200a may be memory chips or a processor, are mounted to the first substrate 110.” EX1005 at [0060]–[0061], FIG. 12. For example, Figure 12 shows that chip 200 (bottom chip) is disposed entirely below third substrate 20 (top package substrate). Indeed, *Sun* teaches that “[i]t would be desirable to increase the vertical separation (stand off height) in order to make room for more and larger chips and enable stacking of chips on the lower substrate” (EX1005 at [0010]), and “[a]s the lower module has a second substrate with electrical connectors on either side, the stand off height may be increased. Further, the opening in the second substrate makes room for one or more chips mounted to the first substrate,” EX1005 at [0014].

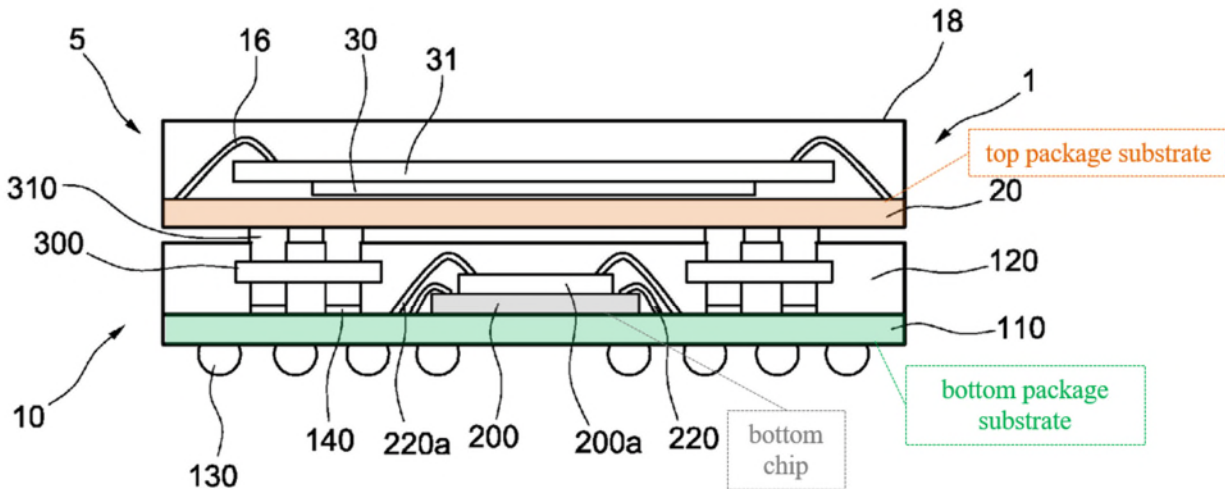


FIG.12

EX1005 at FIG. 12.

149. Thus, in my opinion, *Sun* discloses each limitation of claim 2.

C. Claim 3

i. 3[a]: The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate

150. *Sun* discloses “the structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate.” *Sun* discloses chips 30, 31 (top chips) mounted to the top surface of the third substrate 20 (top package substrate). For example, *Sun* provides that chips 30, 31 (top chips) are “mounted to a first (upper) side of a third substrate 20.” EX1005 at [0059]. The chips 30, 31 (top chips) are connected to the third substrate 20 (top package substrate) via wire bonding. EX1005 at [0059] (“The chips 30, 31 are electrically connected to the third substrate 20 by wires 16 or any other suitable means.”).

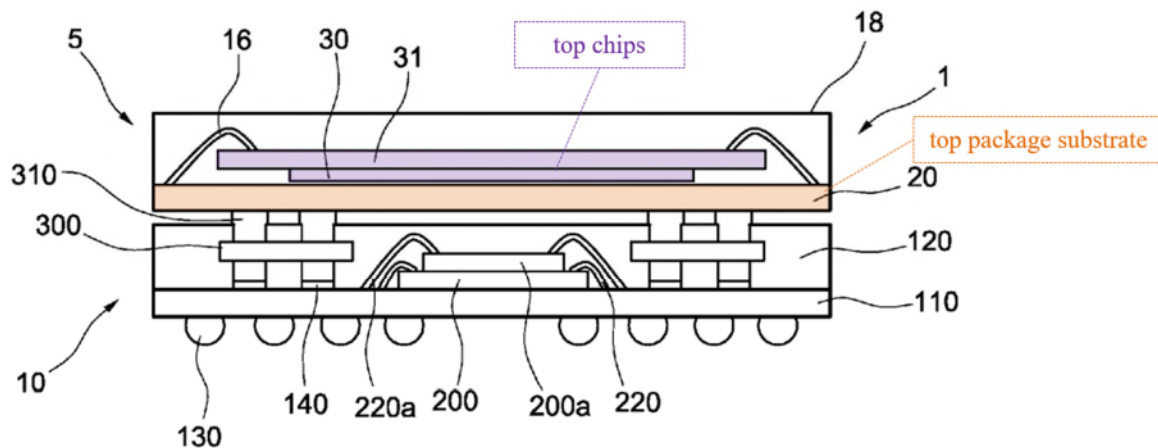


FIG.12

EX1005 at FIG. 12.

151. Thus, in my opinion, *Sun* discloses each limitation of claim 3[a].

ii. 3[b]: wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors

152. *Sun* discloses “wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.” *Sun* discloses that in a direction in which the **third substrate 20** (top package substrate) is stacked on top of the **first substrate 110** (bottom package substrate), **chips 30, 31** (top chips) overlaps **chip 200** (bottom chip) and each of the two **second substrates 300** (spacer connectors). For example, Figure 12 shows that the **third substrate 20** (top package substrate) and **first substrate 110** (bottom package substrate) are stacked in a vertical direction, and in

this vertical direction, the chips 30, 31 (top chips) overlaps with the chip 200 (bottom chip) and both second substrates 300 (spacer connectors), as shown below.

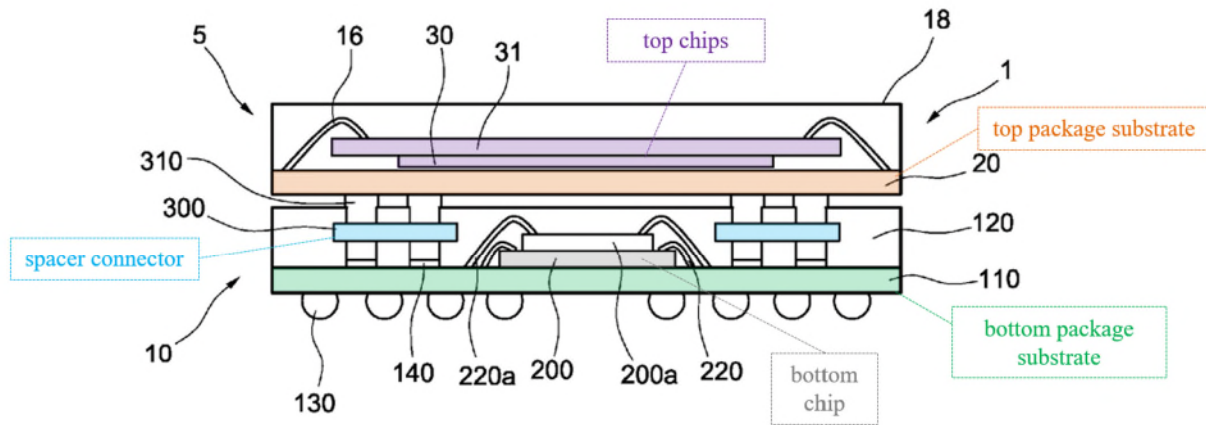


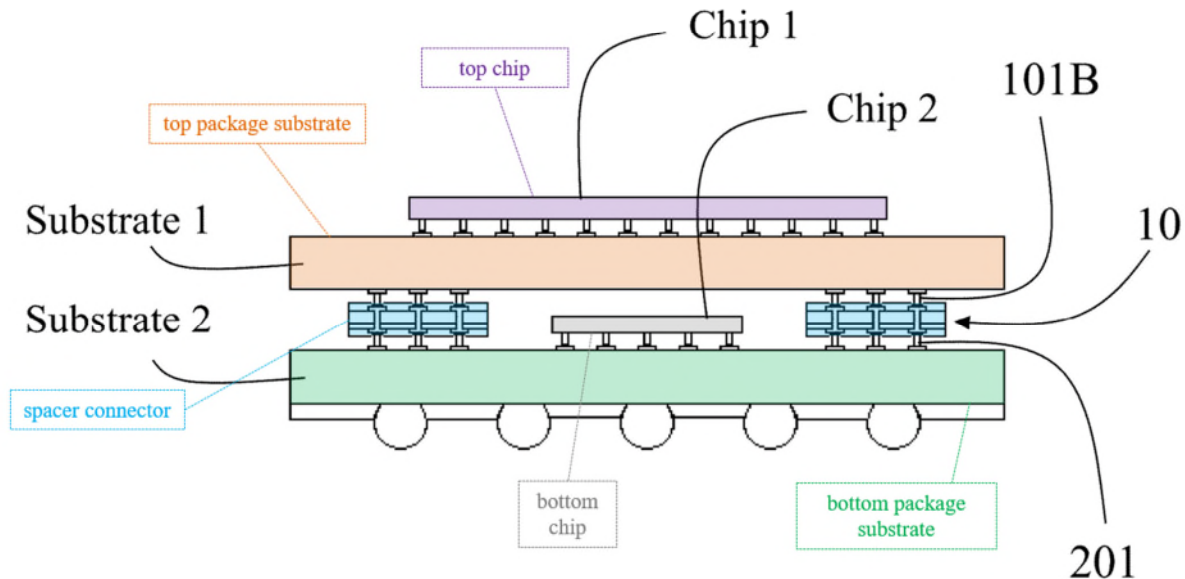
FIG.12

EX1005 at FIG. 12.

153. This overlap is similar to that shown in the figures of the '202 Patent.

EX1001 at FIGs. 8, 11, 14.

Fig.8



EX1001 at FIG. 8.

154. Thus, in my opinion, *Sun* discloses each limitation of claim 3[b].

D. Claim 4

- i. The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate**

155. *Sun* discloses “the structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the

spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.” *Sun* discloses each **second metal connector 310** (bottom metal pillar) among the plurality of **second metal connectors 310** of the **third substrate 20** (top package substrate) is aligned with a corresponding **via 390** (metal pillar) among the plurality of **vias 390** of the **second substrate 300** (spacer connector), and with a corresponding **first metal connector 320** (top metal pillar) among the plurality of **first metal connectors 320** of the **first substrate 110** (bottom package substrate). For example, *Sun* teaches that “[t]he second metal connectors 310 are aligned with corresponding [first metal connectors 320] on the opposite side of the substrate 300.” EX1005 at [0062]². Further, the “[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” EX1005 at [0063]. Here, to make this electrical connection between the **vias 390** (metal pillars) and the aligned **second metal connectors 310** (bottom metal pillars) and **first metal connectors 320** (top metal pillars), each **via 390** (metal pillar) must also be aligned with a corresponding **second metal connector 310** (bottom metal pillar) and **first metal connector 320** (top metal pillar), as illustrated in *Sun*’s Figure 13 below. EX1005 at [0062], FIG. 13.

² Here, “second metal connectors 310” in [0062] is an apparent typo and should have been “first metal connectors 320,” considering the illustration in FIG. 13 and other portions of the specification.

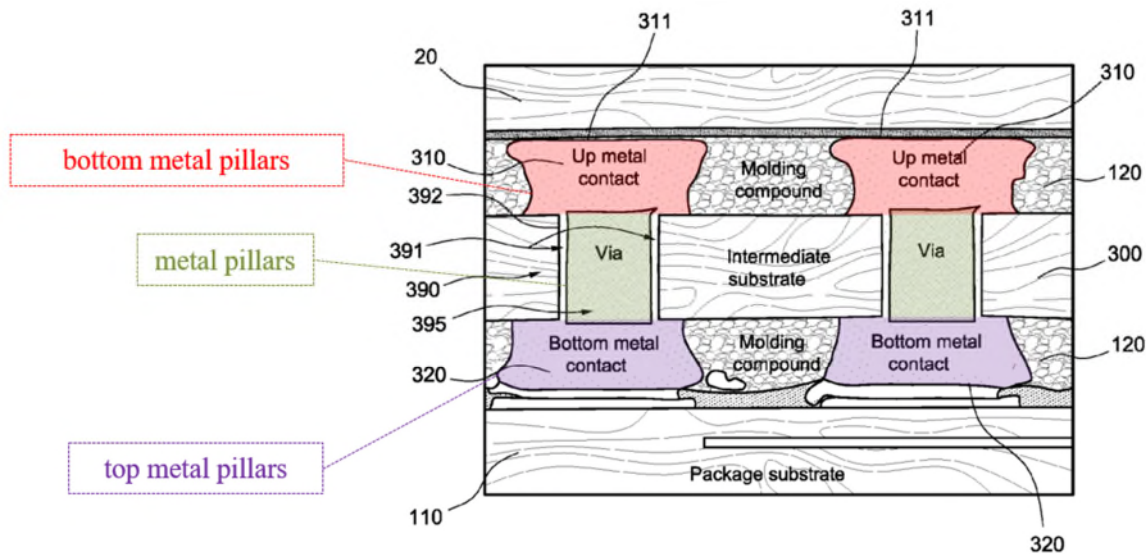


FIG.13

EX1005 at FIG. 13 (showing the alignment of the three sets of metal pillars).

156. Thus, in my opinion, *Sun* discloses each limitation of claim 4.

E. Claim 6

- i. **6[a]: The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate**

157. *Sun* discloses “the structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate.” *Sun* discloses the bottom ends of the plurality of vias 390 (metal pillars)

protruding downwardly from the bottom surface of the core/prepreg layer 301 (core substrate) of the second substrate 300 (spacer connector) are connected, in an end-to-end manner, to corresponding top ends of the plurality of first metal connectors 310 (top metal pillars) of the first substrate 100 (bottom package substrate). For example, as discussed above, *Sun* discloses the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector. §X.A.viii. *Sun* further discloses that “[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” EX1005 at [0062]. As shown in *Sun*’s Figure 13, such an electrical connection requires that these pillars are connected in an end-to-end manner, as the bottom **ends** of the metal pillars are connected to corresponding top **ends** of the plurality of first metal connectors 320 (top metal pillars) of the first substrate 110 (bottom package substrate).

connected to the corresponding top ends of the plurality of **vias 390** (metal pillars) of the **second substrate 300** (spacer connector) via the corresponding **bonding pads** (top metal pads) of the **second substrate 300**. As discussed above in §X.A.vii, *Sun* discloses and/or renders obvious **bonding pads** (top metal pads) on the top end of each **via 390** (metal pillar). Figure 14(a) shows the bottom end of each **second metal connector 310** (bottom metal pillar) is connected to a **bonding pad** (top metal pad) disposed on a top end of each corresponding **via 390** (while Figure 14(a) omits **vias 390** (metal pillars), Figure 13 illustrates that the **second metal connectors 310** (bottom metal pillars) are connected to the corresponding top ends of **vias 390** (metal pillars)).

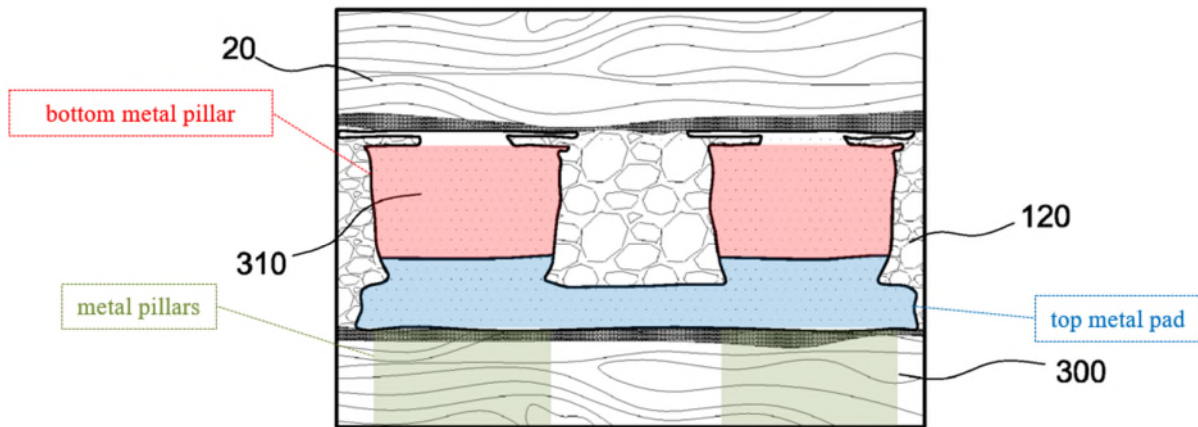


FIG.14(a)

EX1005 at FIG. 14(a) (superimposed with vias 390 (metal pillars), as taught in Figure 13).

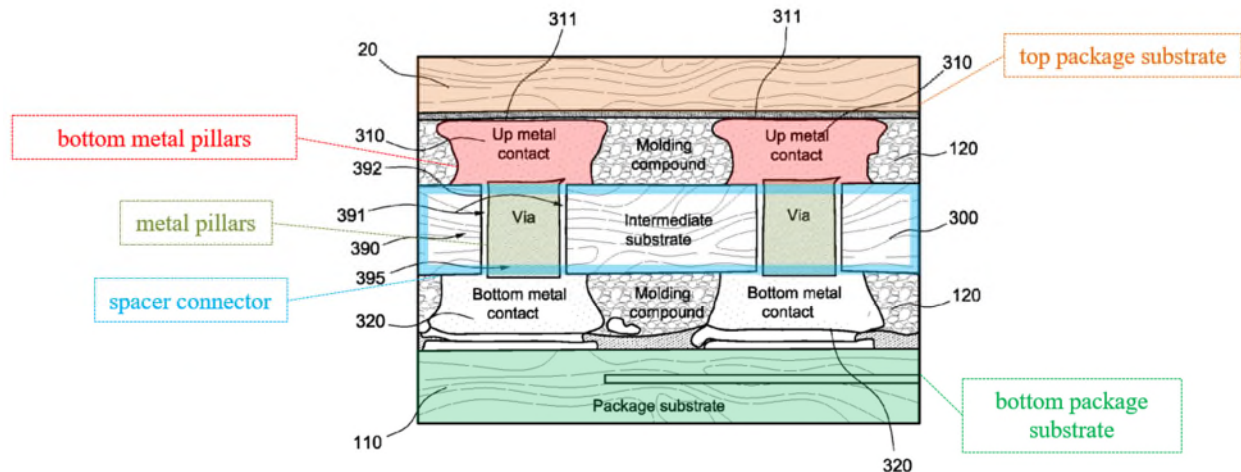


FIG.13

EX1005 at FIG. 13.

160. Thus, in my opinion, *Sun* discloses and/or renders obvious each limitation of claim 6[b].

F. Claim 7

- i. **7[a]: The structure of claim 4, wherein the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate**

161. *Sun* discloses “the structure of claim 4, wherein the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate.” *Sun*’s second substrates 300 (spacer connectors) include a solder resist layer 305 (dielectric layer) on a bottom surface of the core/prepreg insulating layer 301 (core substrate). For example, *Sun* teaches that “the second substrate 300 comprises a core/prepreg insulating layer 301, a metal layer 302, 303 on either side of the core

layer and an insulating solder resist layer 304, 305 on either side of the metal layers.”). EX1005 at [0065]. Additionally, as illustrated in Figure 15, the **solder resist layer 305** (dielectric layer) is disposed on a bottom surface of the **core/prepreg insulating layer 301** (core substrate). It is my opinion that the resist layer need not be **directly** on, or in contact with, the bottom surface of the core/prepreg insulating layer to satisfy this limitation.

162. However, even if direct contact is required, this limitation is still satisfied. As I explained above, Sun’s **solder resist layer 305** (dielectric layer) would be applied after the metal layer 303 is patterned. See EX1005 at [0065]; §V.I. A POSITA would have understood that the **solder resist layer 305** (dielectric layer) protects the metal layer 303 and defines the solderable areas on the metal layer 303. The **solder resist layer 305** (dielectric layer) is therefore in contact with the **core/prepreg insulating layer 301** (core substrate) in all areas where the metal layer 303 has been etched away during the patterning process.

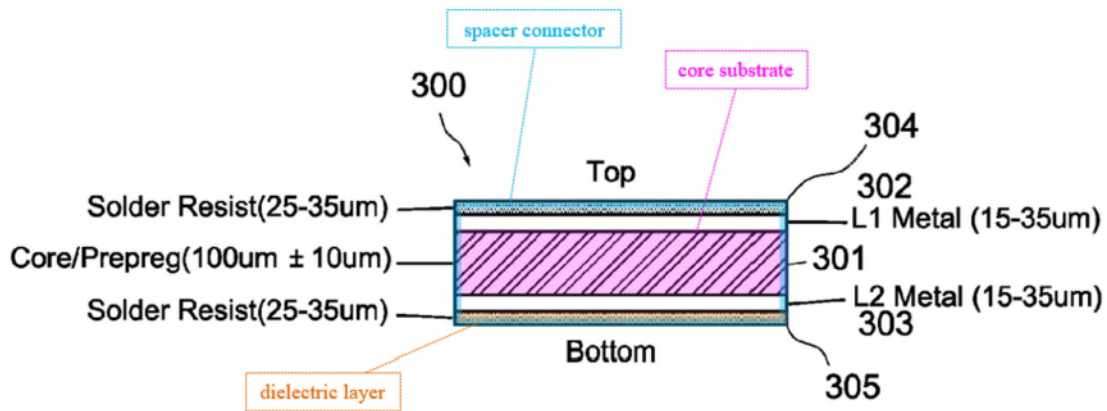


FIG.15

EX1005 at FIG. 15.

163. Thus, in my opinion, *Sun* discloses each limitation of claim 7[a].

ii. 7[b]: the plurality of metal pillars pass through the core substrate and the dielectric layer

164. *Sun* discloses “the plurality of metal pillars pass through the core substrate and the dielectric layer.” *Sun*’s plurality of **vias 390** (metal pillars) pass through the **core/prepreg insulating layer 301** (core substrate) and the **solder resist layer 305** (dielectric layer). For example, *Sun* teaches that its “vias 390 extend through the second substrate 300.” EX1005 at [0063]. **Second substrate 300** (spacer connector) includes both the **core/prepreg insulating layer 301** (core substrate) and the solder resist layer 305 (dielectric layer). EX1005 at [0063]. Accordingly, *Sun*’s **vias 390** (metal pillars) pass through the **second substrate 300** (spacer connector), thus they also pass through the **core/prepreg insulating layer 301** (core substrate) and the **solder resist layer 305** (dielectric layer). EX1005 at [0063]. This is illustrated in

110

120

120

310

310

311

311

320

320

390

391

392

395

300

310

310

Up metal contact

Molding compound

Up metal contact

Bottom metal contact

Molding compound

Bottom metal contact

Via

Via

Package substrate

Package substrate

dielectric layer

spacer connector

metal pillars

core substrate

EX1005 at FIG. 13 (annotated with FIG. 15 superimposed thereon).

G. Claim 8

166. Sun discloses “the structure of claim 7, wherein the dielectric layer is a dielectric adhesive in which the core substrate is pasted.” Sun’s solder resist layer 305 (dielectric layer) is a dielectric adhesive in which the core/prepreg insulating layer 301 (core substrate) is pasted. I understand that claim 8 is an apparatus claim, which does not include any limitations requiring the act of “pasting,” but merely

requires that the solder resist layer 305 (dielectric layer) be adhered to the core/prepreg insulating layer 301 (core substrate). For example, Sun's solder resist layer 305 (dielectric layer) is adhered to the bottom of second substrate 300 (spacer connector) below the L2 Metal layer. EX1005 at [0065], FIG. 15. Accordingly, a POSITA would have understood that the insulating solder resist layer 305 (dielectric layer) is a dielectric adhesive, as it must necessarily have adhesive properties, such that it can adhere to the L2 Metal layer. EX1005 at [0065], FIG. 15; §V.I. Accordingly, given that the solder resist layer 305 (dielectric layer) is adhered on the top and bottom of the core/prepreg insulating layer 301 (core substrate) the core/prepreg insulating layer 301 (core substrate) is “pasted” in the solder resist layer 305 (dielectric layer). EX1005 at [0065], FIG. 15.

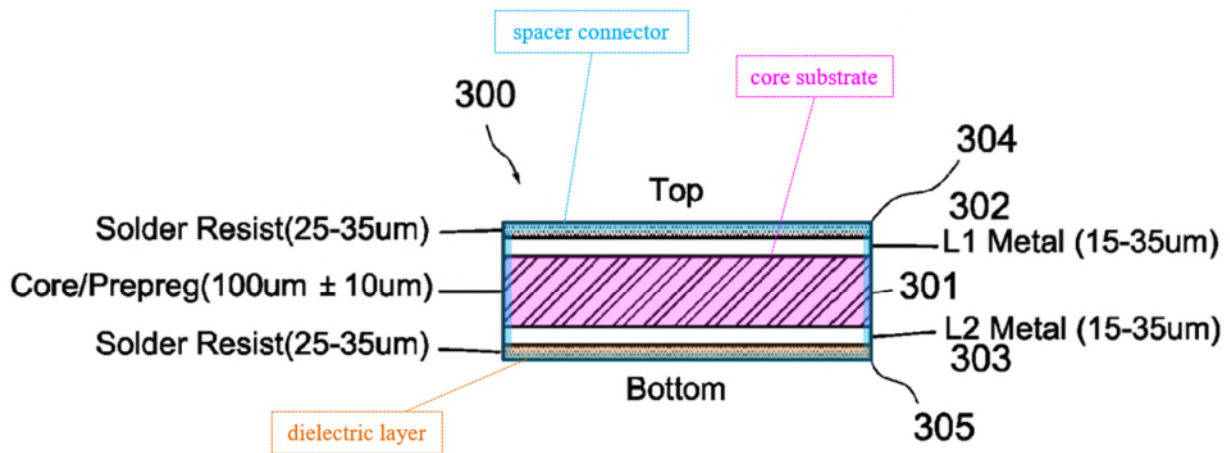


FIG.15

EX1005 at FIG. 15.

167. Thus, in my opinion, *Sun* discloses each limitation of claim 8.

H. Claim 9

- i. **9[a]: The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars**

168. *Sun* discloses and/or renders obvious “the structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars.” *Sun* discloses and/or renders obvious the bottom ends of the plurality of **vias 390** (metal pillars) are connected to corresponding top ends of the plurality of **first metal connectors 320** (top metal pillars) of the **first substrate 110** (bottom package substrate) via the corresponding **bonding pads** (bottom metal pads) of the **second substrate 300** (spacer connector), for the same reasons discussed above, with reference to limitation 1[f]. §§X.A.vii, X.E.ii.

169. Thus, in my opinion, *Sun* discloses and/or renders obvious each limitation of claim 9[a].

- ii. **9[b]: the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector**

170. *Sun* discloses and/or renders obvious “the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal

pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector.” *Sun* discloses the bottom ends of the plurality of **vias 390** (metal pillars) are connected to corresponding top ends of the plurality of **first metal connectors 320** (top metal pillars) of the **first substrate 110** (bottom package substrate) via the corresponding **bonding pads** (bottom metal pads) of the **second substrate 300** (spacer connector). For example, as discussed above with reference to limitation 1[i], *Sun* discloses that the bottom ends of **vias 390** (metal pillars) are connected to top ends of the **first metal connectors 320** (top metal pillars). §X.A.x. Additionally, as discussed above with reference to limitation 9[a], *Sun* discloses and/or renders obvious **bonding pads** (bottom metal pads) disposed on the bottom ends of **vias 390** (metal pillars). §§X.A.vii, X.E.ii, X.H.i. Accordingly, as illustrated in Figure 13, the bottom ends of **vias 390** (metal pillars) are connected to corresponding top ends of **first metal connectors 320** (top metal pillars) via the **bonding pads** (bottom metal pads) on the bottom ends of **vias 390** (metal pillars).

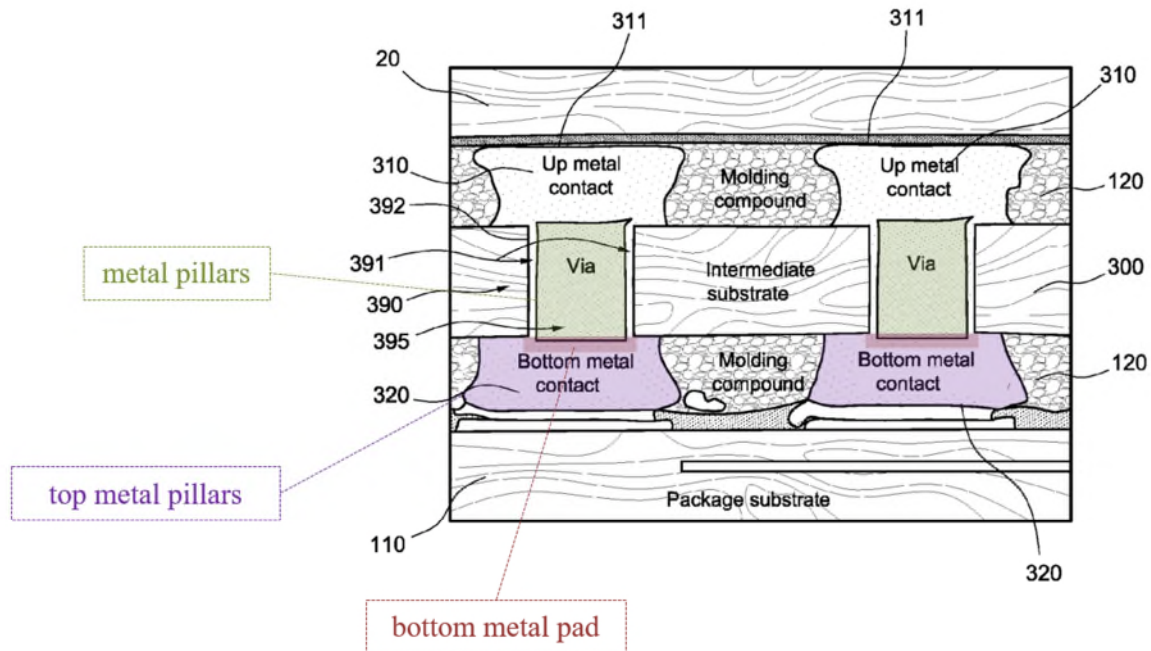


FIG.13

EX1005 at FIG. 13.

171. Thus, in my opinion, *Sun* discloses and/or renders obvious each limitation of claim 9[b].

- iii. **9[c]: bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector**

172. Limitation 9[c] is identical to limitation 6[b]. Accordingly, in my opinion, *Sun* discloses and/or renders obvious limitation 9[c], for the same reasons discussed above, with reference to limitation 6[b]. §X.E.ii.

XI. GROUND 3: *SUN* WITH *LOVE* RENDERS OBVIOUS CLAIMS 1–4 AND 6–9

173. In my opinion, combination of *Sun* and *Love* renders obvious claims 1–4 and 6–9.

A. Motivation to Combine

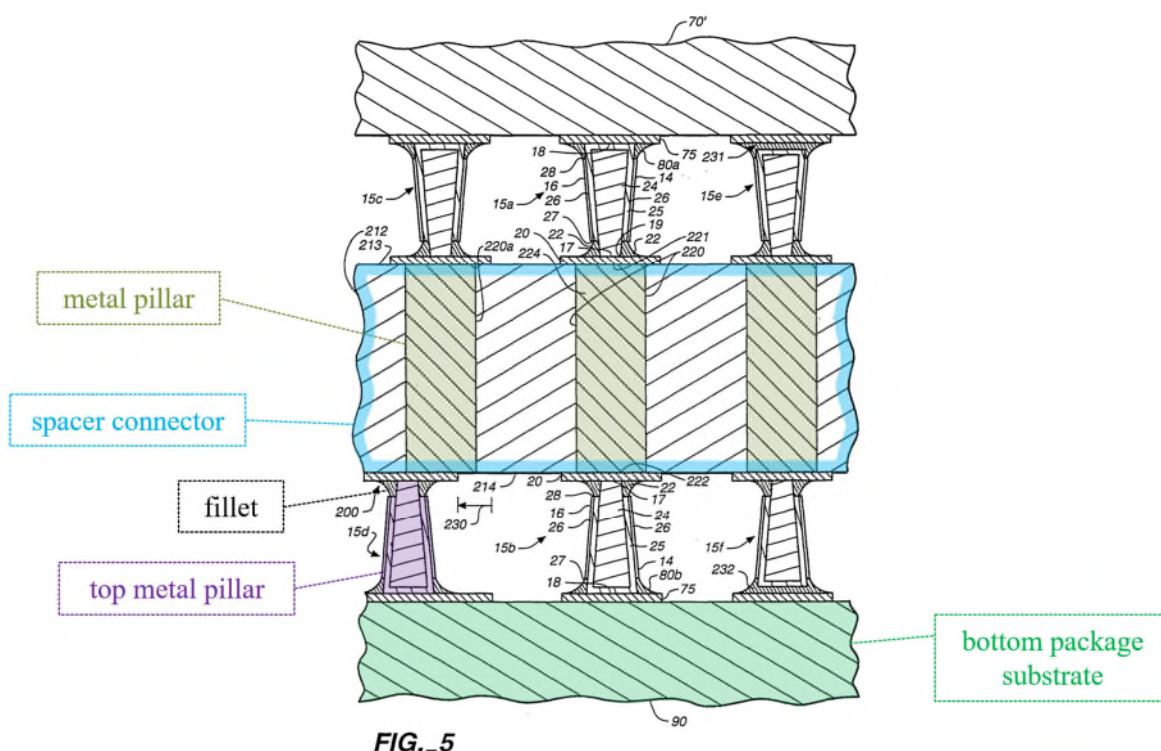
174. *Sun* and *Love* are both directed to similar semiconductor packaging structures including substrates and spacer connectors which are interconnected via metal pillars. For example, *Sun* provides that the claimed “invention relates to package on package (PoP) technology. In particular it relates to a module for use in a multi-package assembly and a method of making the module and a multi-package assembly.” EX1005 at [0001]. As discussed above, *Sun*’s design includes “[a] second substrate 300 is mounted to the first substrate 110.... The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110.... A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars.” *Id.* at [0048]. Similarly, *Love*’s design “relates to interconnect structures for electrically and mechanically connecting an integrated circuit (IC) chip to a supplying substrate, which serve to communicate signals between the IC chip and the ‘outside world,’ which may be other IC chips or other external devices, and to supply power to the IC chip. Additionally, the present invention relates to methods for constructing such

interconnect structures.” EX1007 at 1:7–15. Specifically, *Love* discloses “an interconnect structure having a substrate with a plurality of electrically conductive posts,” which is similar to *Sun. Id.* at 4:51–61 12:13–19, 15:16–23. For example, *Sun*’s Fig. 13 is similar to *Love*’s Figure 5. EX1005 at FIG. 13; EX1007 at FIG. 5.

175. Additionally, *Sun* and *Love* both identify and discuss the well-known problem that substrates may warp during operation, due to fluctuating temperatures, thereby creating mechanical stress on the interconnected semiconductor structure. For example, *Sun* teaches that “warpage of one or both substrates 20, 40 can deform the connection and solder joints between the upper and lower packages.” EX1005 at [0011]. *Love* teaches that “when the IC chip and the supporting substrate are exposed to elevated temperatures, they will expand at different rates and to different dimensions, thereby inducing mechanical stresses in the solder bump connections.” EX1007 at 1:55–59; *see also* §VIII.C (¶96).

176. In my opinion, a POSITA would look to *Love* to address warpage concerns identified in *Sun*. *Love* teaches a metal pillar design having metal pads and fillets, which provides the benefit of reducing stress on the semiconductor assembly. Specifically, *Love* teaches base pads 20 can be formed on conductive material 224 (metal pillars) by depositing a copper seed layer on interconnect substrate 212 (spacer connector), applying a photoresist layer, electroplating copper onto the exposed portions of the seed layer, and then removing the photoresist layer. EX1007

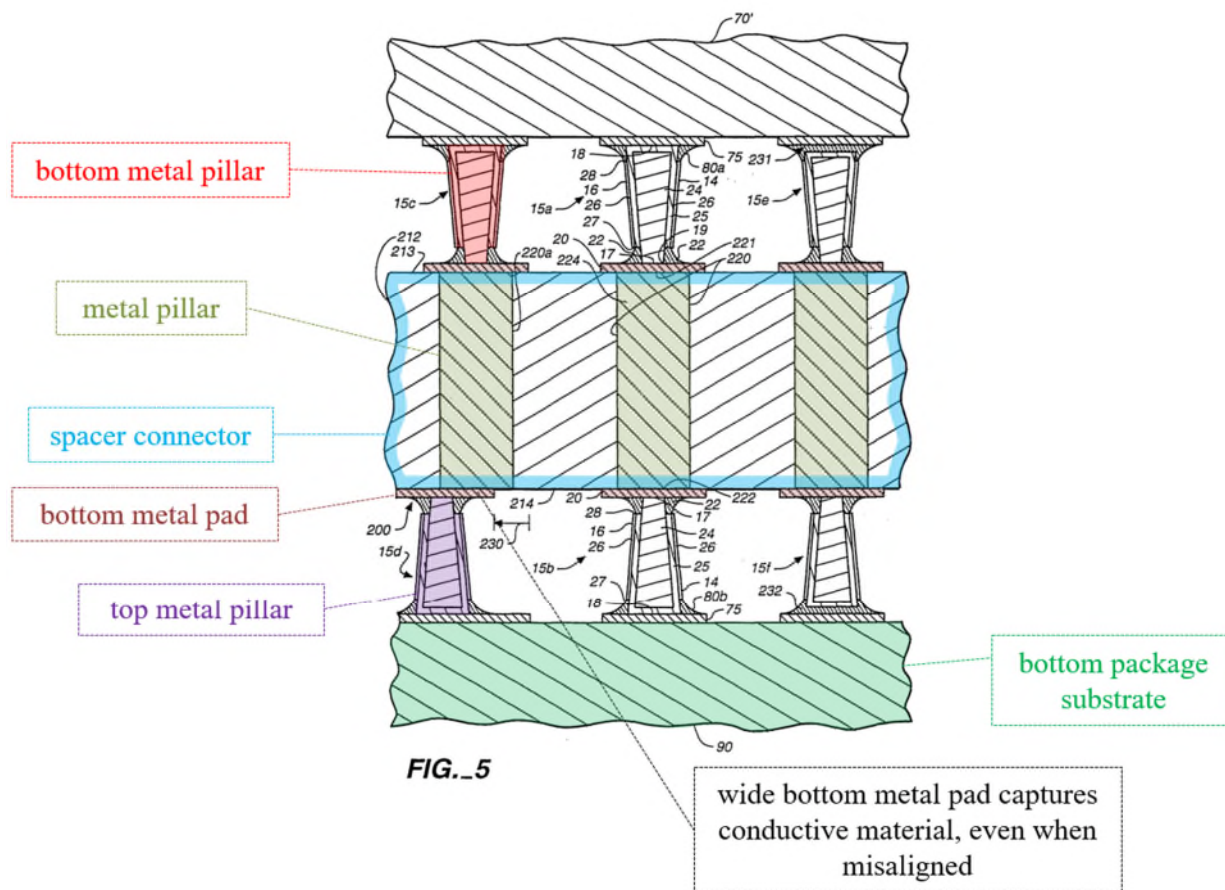
at 14:57–15:15, FIG. 6A. Posts 14 (top metal pillars) can then be connected to conductive material 224 (metal pillars) of an interconnect substrate 212 (spacer connector) via the base pads 20 (metal pads). EX1007 at 12:43–60, FIG. 5. *Love* further teaches fillet 22 can be added to the base pad 20 and post 14 to “de-concentrate any of the mechanical stress and strain at the junction of end 17 [of post 14] and base pad 20.” EX1007 at 10:5–23; *see also* §VIII.C (¶96).



EX1007 at FIG. 5.

177. *Love*’s base pads 20 provide the benefit of reducing the required alignment tolerances during assembly. For example, *Love* explains that “the interconnect columns may be somewhat offset from an exact opposing relationship,” due to misalignment during the manufacturing process, and that this problem can be

solved by applying wide base pads 20 to allow “misalignment error[s].” EX1007 at 13:16–37. See also §VIII.C (¶¶96).



EX1007 at FIG. 5.

178. Accordingly, based on these teachings of *Love*, a POSITA would have been known to apply *Love*’s interconnect columns 15 (which include fillets 22 and posts 14) to *Sun*’s second metal connectors 310 and first metal connectors 320, and add *Love*’s base pads 20 to *Sun*’s vias 390 to (1) reduce mechanical stress from warping and (2) provide a wider connection area between the metal pillars and top and bottom metal pillars, respectively, to account for alignment errors during

assembly, as taught by *Love*. EX1007 at 10:5–23, 13:32–37. This combination would preserve all other aspects of *Sun*’s design. For example, a POSITA would have arrived at the *Sun-Love* design shown below. See §VIII.C (¶96).

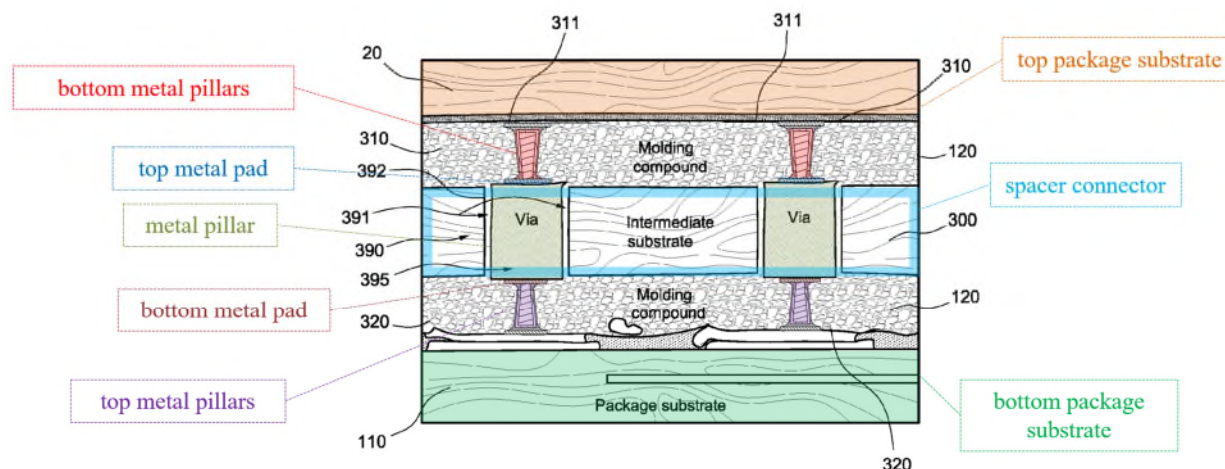


FIG.13

EX1005 at FIG. 13 (superimposed with the base pad and interconnect columns of *Love*).

179. In my opinion, a POSITA would have had a reasonable expectation of success in the proposed combination. For example, *Sun* explicitly discloses similar bonding pads 140, disposed on the bottom ends of the first metal connectors 320. EX1005 at [0066]–[0068]. *Sun* states that these bonding pads can be applied to other pillars. EX1005 at [0066]. *Sun* also discloses similar second metal connectors 310 and first metal connectors 320, which interconnect the package substrates and the spacer connector. EX1005 at [0048]. On the other hand, *Love* provides detailed working examples of how similar base pads and interconnect columns can be applied

to the top and bottom of vias 390. EX1007 at 14:57–15:15, FIG. 6A.

180. Accordingly, the *Sun-Love* combination would only require applying known elements (base pads and interconnect columns) in a known structure (vias and metal connectors) using known methods (copper electroplating) to achieve this well-understood and predictable function (reducing mechanical stress due to warpage and allowing for alignment errors during manufacturing). In my opinion, this is precisely the type of combination that a POSITA would reasonably expect to succeed without undue experimentation, as it relies on established semiconductor manufacturing techniques and addresses known, well-documented problems with interconnects.

B. Claim 1

i. 1[pre]–1[e]

181. As discussed above, the *Sun-Love* combination incorporates *Love*’s interconnect columns 15 and base pads 20 in *Sun*’s PoP structure, but otherwise preserves *Sun*’s design. In my opinion, *Sun-Love* renders obvious each limitation of claim 1[pre]–1[e], as discussed above with reference to *Sun*. §X.A.i–X.A.vi.

ii. 1[f]: a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars

182. *Sun-Love* renders obvious “a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.” For

example, *Sun-Love* renders obvious a plurality of top metal pads, each on a top end of a corresponding **via 390** (metal pillar) among the plurality of **vias 390** (metal pillars). As discussed above in §XI.A, *Love* teaches that a **base pad 20** (top metal pad) can be applied to metal pillars, such as **vias 390** (metal pillars) of *Sun*. For example, *Love* states that “a base pad 20 for each interconnect column 15a and 15b is formed.” EX1007 at 14:57–15:15, FIG. 6. *Sun*, on the other hand, teaches “[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320” and “bonding pads may [be] used to connect the metal pillars to the respective other substrates.” EX1005 at [0062]–[0063], [0066]. As discussed above, a POSITA would have been motivated to apply *Love*’s **base pads 20** (top metal pads) to *Sun*’s **vias 390** (metal pillars) to achieve the beneficial results of (1) reducing mechanical stress due to warping and (2) accommodating alignment errors, as taught by *Love*. §XI.A. Additionally, a POSITA would have had a reasonable expectation of success in making this combination. §XI.A. Accordingly, a POSITA would have arrived at the *Sun-Love* design shown below, which includes **base pads 20** (top metal pads) disposed on the top ends of **vias 390** (metal pillars).

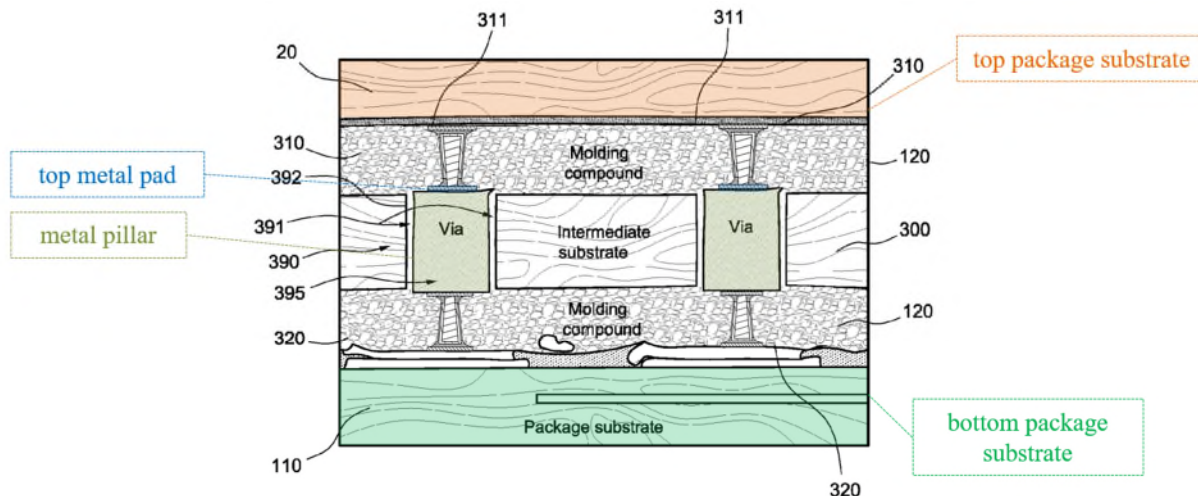


FIG.13

EX1005 at FIG. 13 (superimposed with the base pad and interconnect columns of *Love*).

183. Thus, in my opinion, *Sun-Love* renders obvious each limitation of claim 1[f].

iii. 1[g]–[m]

184. As discussed above, *Sun-Love* incorporates *Love*'s interconnect columns 15 and base pads 20 in *Sun*'s PoP structure but otherwise preserves *Sun*'s design. Accordingly, in my opinion, *Sun-Love* renders obvious limitations 1[g]–[m], in the same way as discussed above regarding *Sun*. §X.A.viii–X.A.xiv.

C. Claims 2–4

185. As discussed above, *Sun-Love* incorporates *Love*'s interconnect columns 15 and base pads 20 in *Sun*'s PoP structure but otherwise preserves *Sun*'s design. Accordingly, in my opinion, *Sun-Love* renders obvious each limitation of

claims 2–4, for the same reason discussed above regarding *Sun*. §X.B–X.D.

D. Claim 6

- i. 6[a]: The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate**

186. *Sun-Love* renders obvious “the structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate.” As discussed above, *Sun-Love* incorporates *Love*’s interconnect columns 15 and base pads 20 in *Sun*’s PoP structure but otherwise preserves *Sun*’s design. Accordingly, in my opinion, *Sun-Love* renders obvious limitation 6[a], for the same reasons discussed above regarding *Sun*. §X.E.i.

- ii. 6[b]: bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector**

187. *Sun-Love* renders obvious “bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.” For the reasons discussed above regarding limitation

1[f], *Sun-Love* renders obvious base pads 20 (top metal pads) on the top of each via 390 (metal pillar). §XI.B.ii; §XI.A. And for the additional reasons discussed above with reference to *Sun*, *Sun-Love* also renders obvious 6[b]. §X.E.ii.

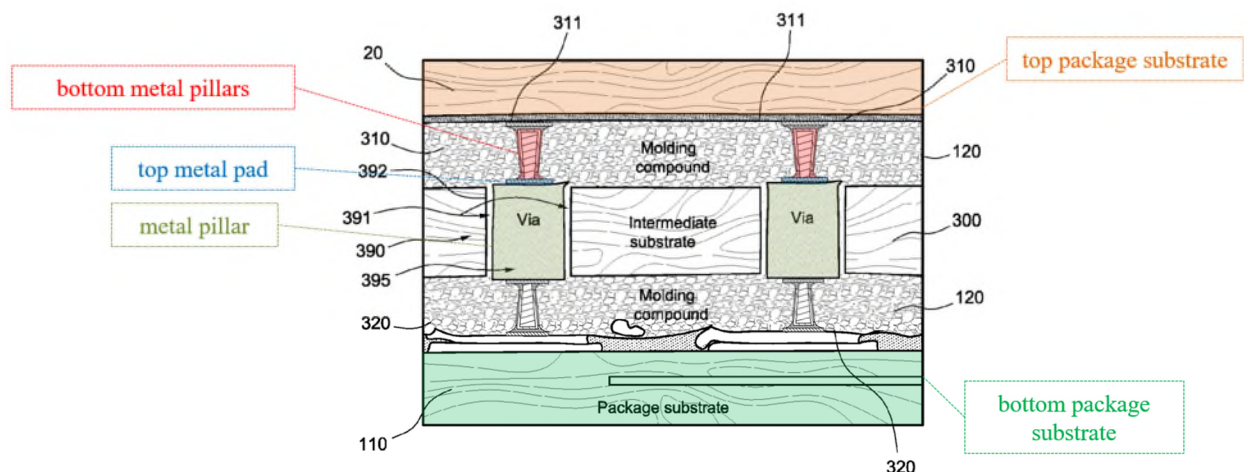


FIG. 13

EX1005 at FIG. 13 (superimposed with the base pad and interconnect columns of *Love*).

188. Thus, in my opinion, *Sun-Love* renders obvious each limitation of claim 6[b].

E. Claims 7–8

189. As discussed above, *Sun-Love* incorporates *Love*'s interconnect columns 15 and base pads 20 in *Sun*'s PoP structure but otherwise preserves *Sun*'s design. Accordingly, *Sun-Love* renders obvious the limitations of claims 7–8, for the same reasons discussed above with respect to *Sun*. §X.F–X.G.

190. Thus, in my opinion, *Sun-Love* renders obvious claims 7–8.

F. Claim 9

- i. **9[a]: The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars**

191. *Sun-Love* renders obvious “the structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars.” *Sun-Love* discloses the **second substrate 300** (spacer connector) includes a plurality of **base pads 20** (bottom metal pads), each on the bottom end of a corresponding **via 390** (metal pillar) among the plurality of **vias 390** (metal pillars). For the same reasons discussed above regarding the top metal pads, *Sun-Love* similarly renders obvious bottom metal pads on the bottom ends of the **vias 390** (metal pillars), which are implemented in *Sun-Love* as shown below. §X.A.vii.

reasons discussed above regarding *Sun*, *Sun-Love* renders obvious limitation 9[b].

§X.H.ii.

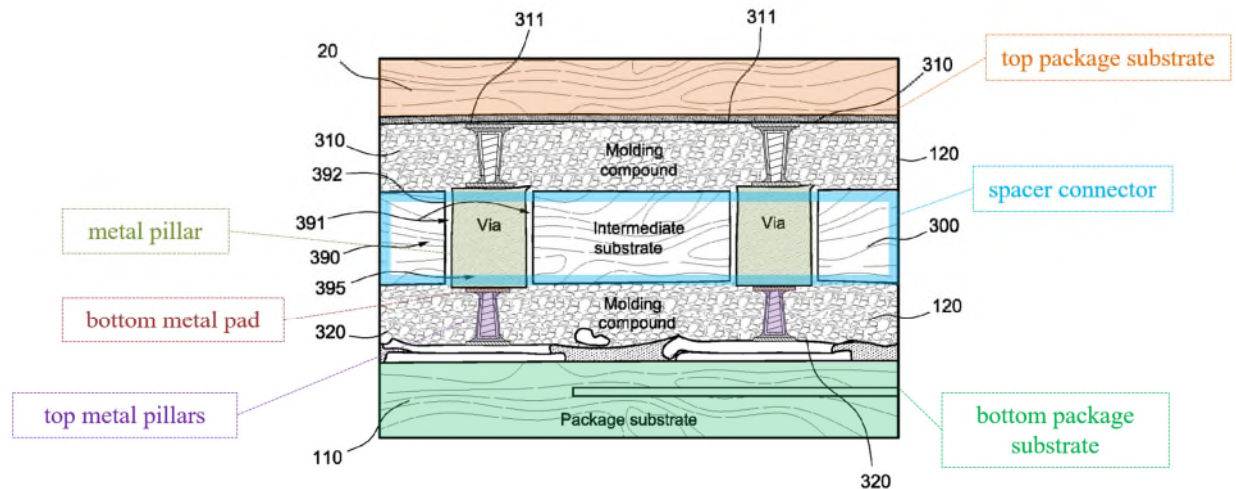


FIG.13

EX1005 at FIG. 13 (superimposed with the base pad and interconnect columns of *Love*).

194. Thus, in my opinion, *Sun-Love* renders obvious each limitation of claim 9[b].

iii. **9[c]: bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector**

195. Limitation 9[c] is identical to limitation 6[b]. Accordingly, in my opinion, *Sun-Love* renders obvious limitation 9[c], for the same reasons discussed above regarding limitation 6[b]. §XI.D.ii.

XII. GROUND 4: *SUN* WITH *HU* RENDERS OBVIOUS CLAIMS 1–4 AND 6–9

196. In my opinion, combination of *Sun* and *Hu* renders obvious claims 1–4 and 6–9.

A. Motivation to Combine

197. *Sun* and *Hu* are both directed to a PoP assembly, including stacked semiconductor packages. EX1005 at [0002] (“A package on package (PoP) comprises two electronic packages assembled in a vertical stack”); EX1008 at [0001] (“The present invention relates to packaging substrates, and more particularly, to a packaging substrate used in a package on package (PoP) structure”), [0003] (“To improve electrical performance and save space, a plurality of packages are stacked on one another so as to form a PoP structure.”). Both *Sun* and *Hu* recognize that PoP assemblies can be improved by replacing conventional solder balls with metal pillars. EX1005 at [0015], [0066]; EX1008 at [0004]–[0005].

198. In particular, *Sun* explains that “solder balls have a less fine pitch and less well defined shape than the metal pillars. Furthermore, at typical processing temperatures (e.g. around 260 degrees Celsius) the solder balls will melt and collapse down, while the metal (e.g. copper) pillars will remain solid and well defined.” EX1005 at [0066].

199. As discussed above, *Sun* teaches a PoP structure, where **first connectors 320** and **second connectors 310** (top and bottom metal pillars) can be stacked with

vias 390 to connect a first substrate 110 and a third substrate 20. EX1005 at [0061], [0063]. Similar to *Hu, Sun*'s "first and second connectors preferably take the form of metal pillars, for example copper pillars." *Id.* at [0063].

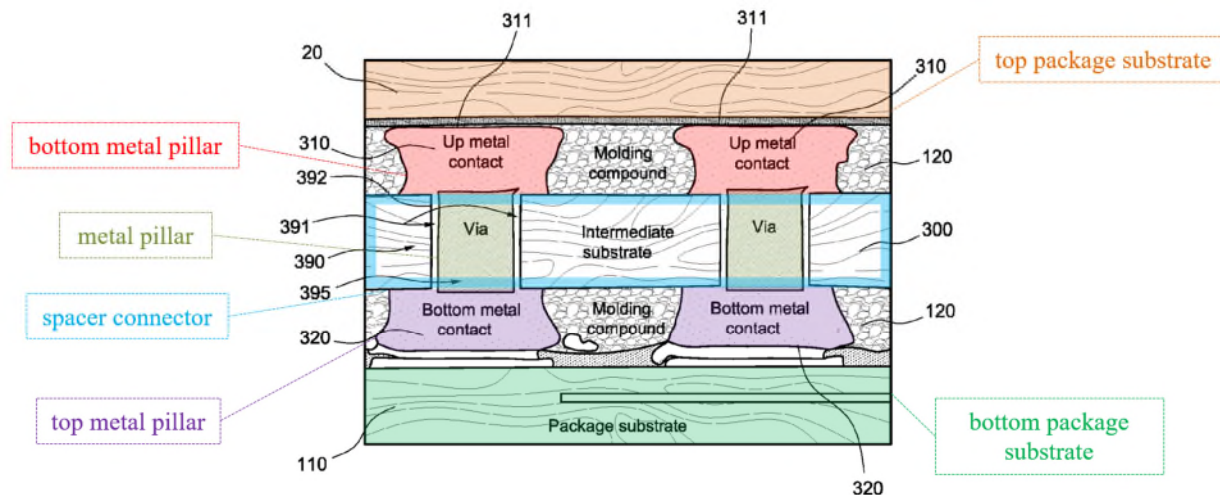


FIG.13

EX1005 at FIG. 13.

200. *Hu* provides teachings related to *Sun*'s. For example, *Hu* explains that when conventional solder balls are used in PoP assemblies, "it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity." EX1008 at [0004]. To solve this well-known problem, *Hu* teaches using "metal posts in combination with a solder material." EX1008 at [0005].

201. *Hu* also identifies certain technical challenges associated with metal pillars. For example, *Hu* explains that "it is not easy to control the uniformity of the

height of the metal posts.” EX1008 at [0008], FIG. 1 (showing metal posts with non-uniform height). *Hu* provides a detailed solution to this uniformity problem of metal pillar structures, which involves placing “conductive bonding layers” on metal posts, which are initially formed on the top and bottom substrates so that the resulting metal posts have the same “height.” EX1008 at [0030], FIG. 2E. *Hu* further teaches specific process-level details for implementing such uniform metal pillars on a package substrate. EX1008 at [0013], [0028]–[0035], FIGs. 2C–2F.

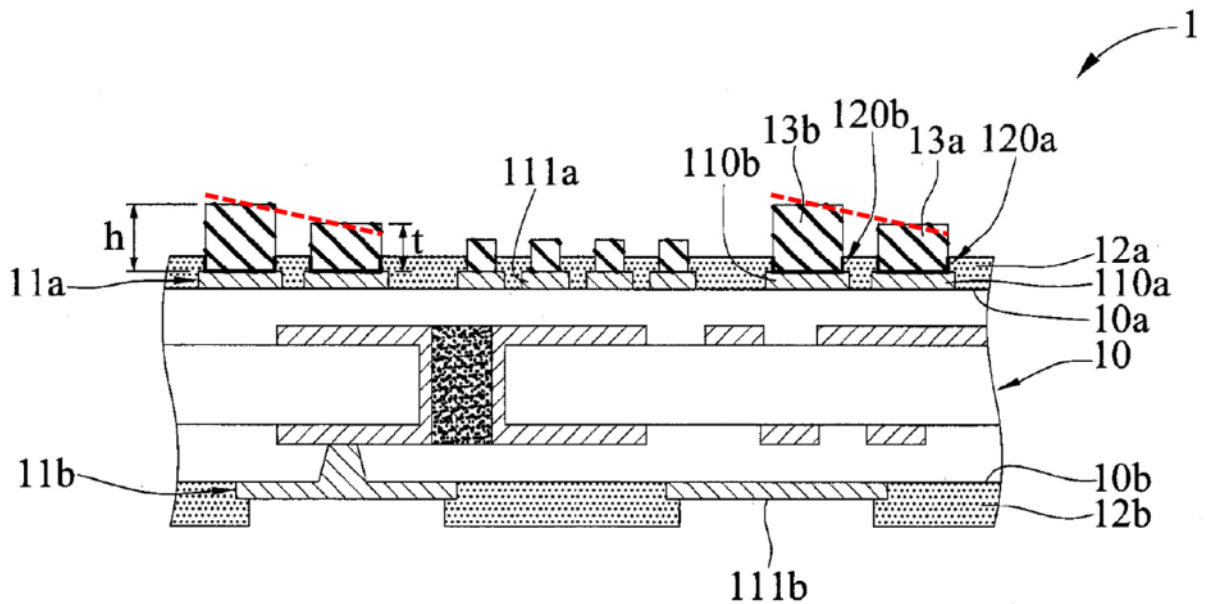


FIG. 1 (PRIOR ART)

EX1008 at FIG. 1 (red dashed line illustrating a mismatch between the metal pillars).

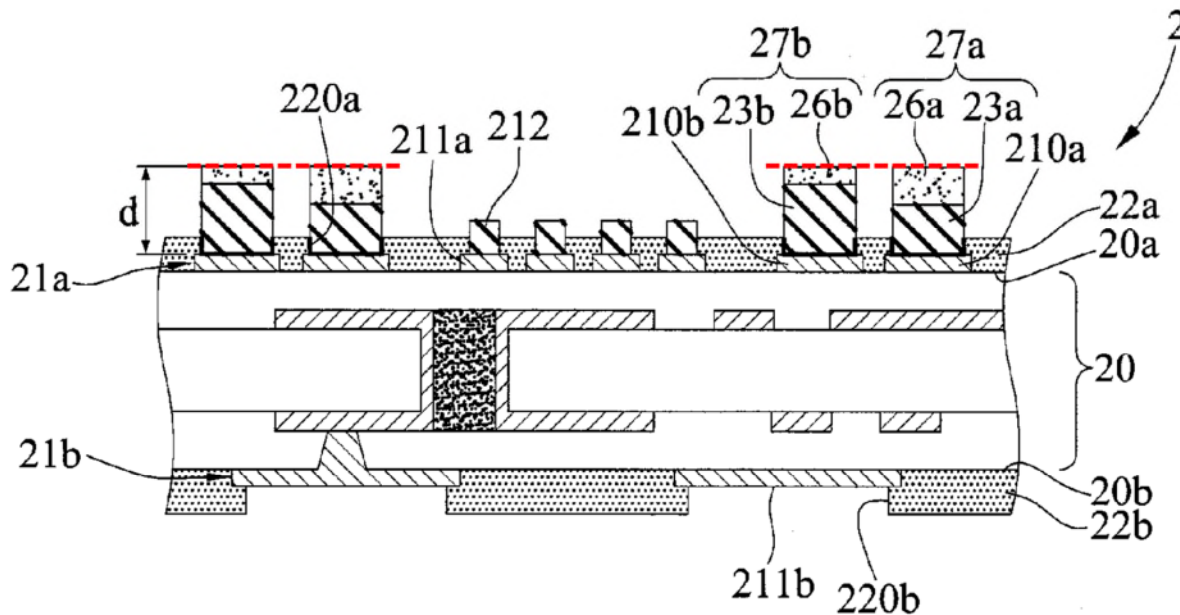


FIG. 2E

EX1008 at FIG. 2E (red dashed line illustrating matching metal pillars in an embodiment example of *Hu*).

202. Accordingly, when implementing *Sun*'s design, a POSITA would have been motivated to look to *Hu* for guidance on how to construct *Sun*'s first connectors 320 and second connectors 310 as metal pillars, to achieve uniform pillar height in a practical and reliable manner. A POSITA would therefore have been motivated to apply *Hu*'s techniques to *Sun*'s metal pillar design, to "prevent tilted stack structures and poor coplanarity in a... stacking process... to improve the product reliability." EX1008 at [0013].

203. Specifically, in my opinion, a POSITA would have found it obvious to implement *Hu*'s metal pillar processing steps to fabricate *Sun*'s first connectors 320 and second connectors 310. As taught by *Hu*, POSITA would initially form metal

pillars on the bonding pads 140 on top of Sun's **first substrate 110** (bottom package substrate) and bottom of **third substrate 20** (top package substrate), prior to assembling them with the **second substrates 300** (spacer connectors) (EX1005 at [0061], [0066], [0068]; EX1008 at [0025]–[0028]), so that the height of the metal pillars can be adjusted using conductive bonding layers to achieve good coplanarity. EX1008 at [0008], [0029]–[0030]; EX1005 at FIG. 12.

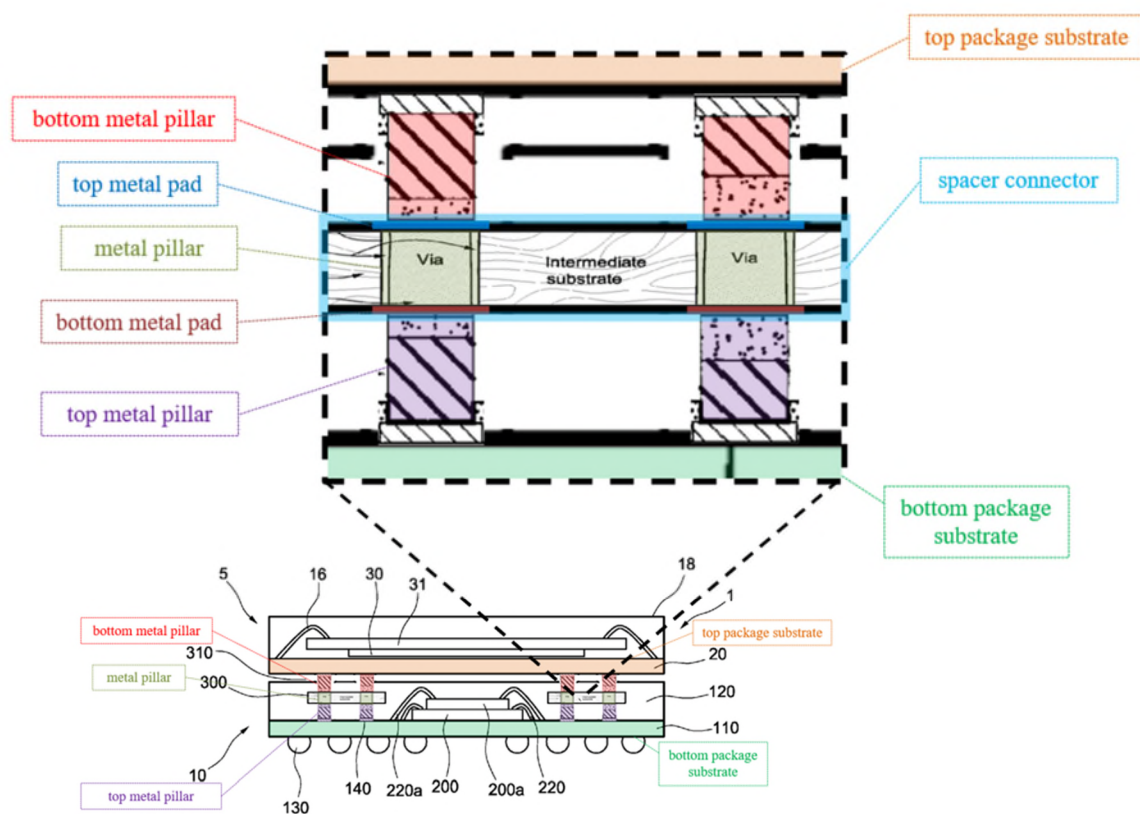


FIG.12

EX1005 at FIG. 12 (modified in view of *Hu* to illustrate the *Sun-Hu* device).

204. Accordingly, *Sun-Hu* preserves *Sun*'s structural design and only varies the fabrication steps of the metal pillars, as taught by *Hu*, such that metal pillars (first

connectors 320 and second connectors 310) are first built on *Sun*'s bonding pads 140 (equivalent to *Hu*'s "conductive pads" 210 on which metal pillars are formed) on the bottom package substrate and the top package substrate, respectively. In my opinion, this combination would predictably yield the same electrical interconnectivity between package substrates, while providing the benefits of improved coplanarity and mechanical stability. Additionally, *Sun-Hu* satisfies not only the correction construction but also the narrow construction of bottom and top metal pillars discussed above, where the metal pillars are built as "part of" the top and bottom package substrates.

205. In my opinion, a POSITA would have had a reasonable expectation of success in achieving this *Sun-Hu* combination. For example, *Sun* already provides the teachings of forming first connectors 320 and second connectors 310 as metal pillars. EX1005 at [0061]. In the same line of teaching, *Hu* further provides detailed, working examples of metal pillars formed by an "electroplating process" for PoP interconnections to achieve improved coplanarity, which a POSITA would use to determine how to construct *Sun*'s metal pillars. EX1008 at [0028]–[0035], FIGs. 2C–2F. The *Sun-Hu* combination therefore requires only applying known elements (metal pillars) in a known structure (PoP) using known methods (electroplating) to achieve a well-understood and predictable function (providing reliable electrical and mechanical connections). In my opinion, this is the type of combination that a

POSITA would reasonably expect to succeed without undue experimentation, as it relies on established semiconductor packaging techniques and addresses known, well-documented problems with PoP connectors.

B. Claims 1–4 and 6–9

206. As discussed above, the *Sun-Hu* design does not materially alter the final package structure of *Sun*. §XII.A. *Sun-Hu* merely changes the processing step of *Sun*'s top and bottom metal pillars according to *Hu*'s teachings. Specifically, the first connectors 320 and second connectors 310 (top and bottom metal pillars) of *Sun-Hu* are first formed on the first substrate 110 (bottom package substrate) and third substrate 20 (top package substrate), respectively, and are then joined to the vias 390 (metal pillars) of *Sun*'s second substrates 300 (spacer connectors). §XII.A. As discussed above, this design joins the first substrate 110 (bottom package substrate) and third substrate 20 (top package substrate) with the second substrates 300 (spacer connectors), to form a package stack with minimal tilt. §XII.A.

207. Accordingly, even if the terms “bottom metal pillars of the top package substrate” and “top metal pillars of the bottom package substrate” require that the bottom metal pillars and top metal pillars be built as part of the top package substrate and bottom package substrate, respectively, prior to assembling the PoP structure, *Sun-Hu* suggests to a POSITA this process. §XII.A. Accordingly, in my opinion, *Sun-Hu* renders obvious claims 1–4 and 6–9 for the same reasons discussed above,

with reference to Grounds 1–2, even under this narrow construction, because the structural design of *Sun-Hu* is materially identical to *Sun*. §X.

XIII. GROUND 5–6: *CHEN* ANTICIPATES AND/OR RENDERS OBVIOUS CLAIMS 1–9

208. In my opinion, *Chen* anticipates and/or renders obvious claims 1–9.

A. Claim 1

i. 1[pre]: A structure

209. *Chen* discloses “a structure.” For example, *Chen* teaches “[a] Package-on-Package (PoP) structure and the methods of forming the same.” EX1006 at [0008]. The PoP structure includes top package component 62, package component 56, and “Through-Assembly Via (TAV) Module [28], which includes a substrate [and] a plurality of through-vias penetrating through the substrate.” *Id.* at Abstract, [0010] (“substrate 34, which may be a semiconductor substrate such as a silicon substrate.”), FIG. 9 (below). TAV Module 28 is electrically coupled to the bottom and top package component via connectors 44 as shown in Figure 9. *Id.* at [0014], [0019] (“TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.”), FIGs. 4, 9.

210. *Chen*’s PoP structure also include “two TAV modules” “disposed on opposite sides of package component 24,” including “one or a plurality of device dies” mounted on the bottom package component. *Id.* at [0012], [0009] (“In some embodiments, package component 24 includes one or a plurality of device dies.”),

[0020] (“FIG. 11 illustrates alternative embodiments, wherein the positions of stacked dies 64 and package component 24 are swapped as compared to FIG. 10.”), FIGs. 2, 11. As shown in figures below and further explained below, *Chen’s* PoP structure (FIG. 9) is substantially similar to the ’202 Patent’s structure (FIG. 8).

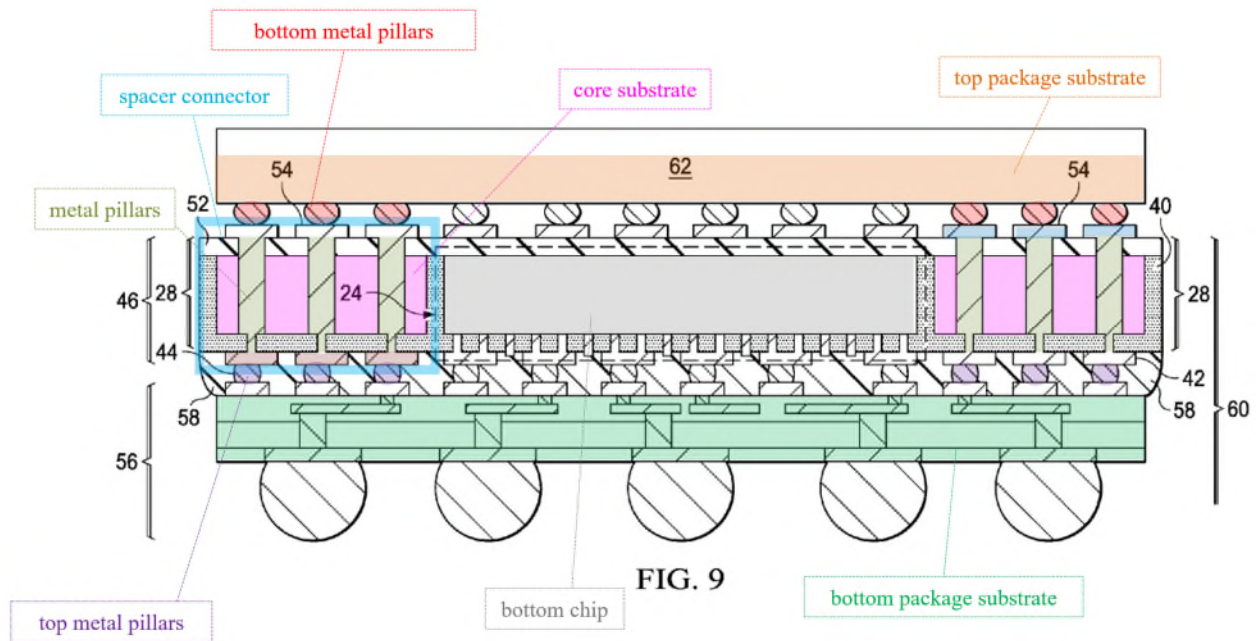
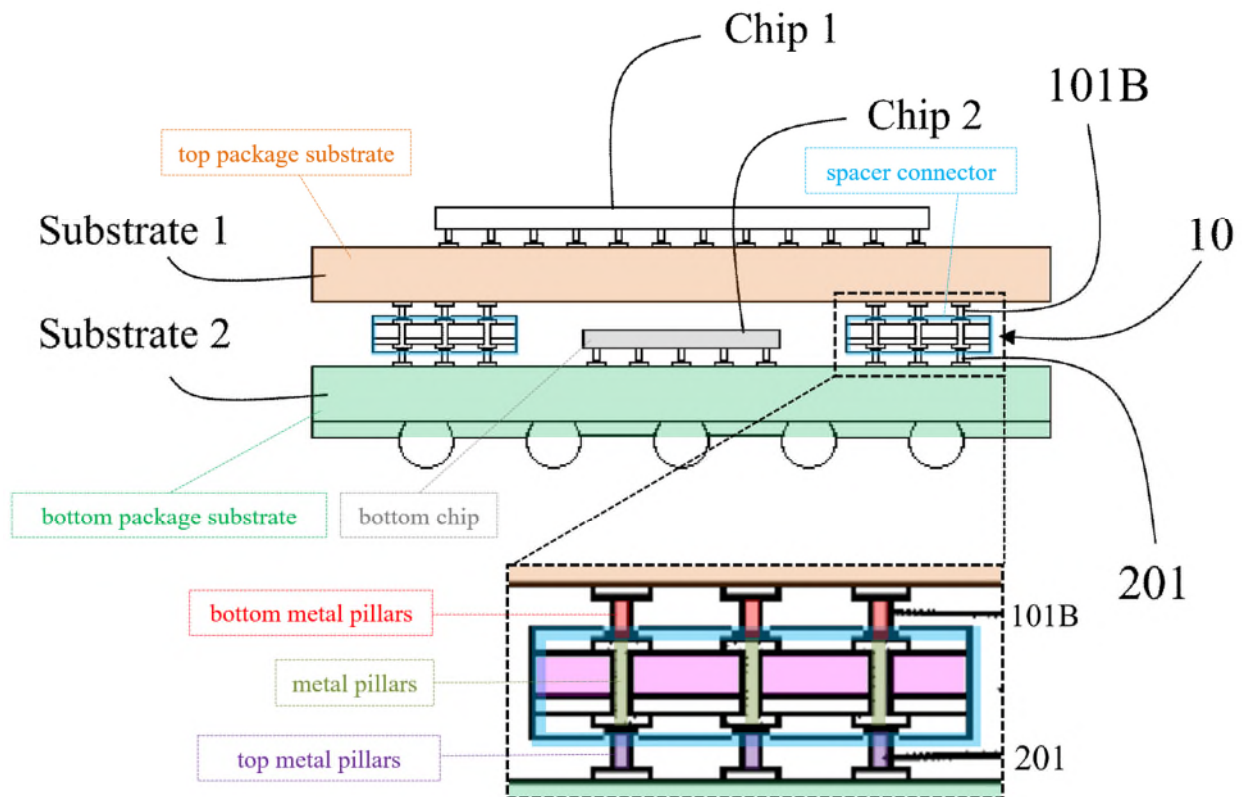


Fig.8



EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

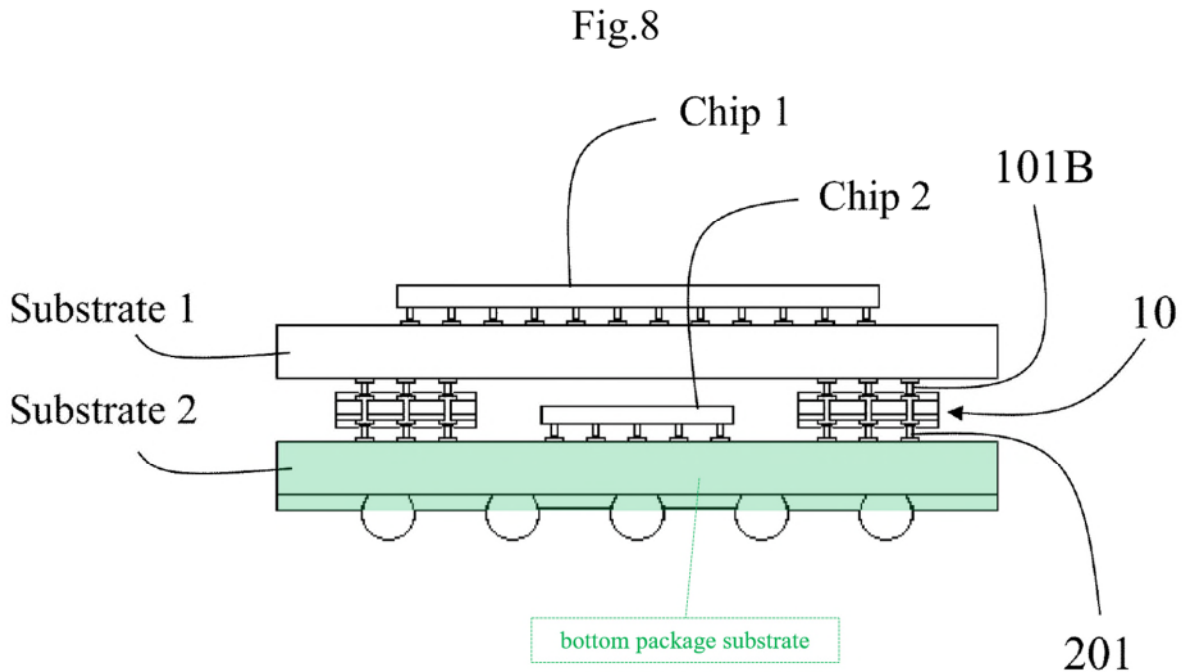
211. Thus, in my opinion, *Chen* discloses each limitation of claim 1[pre].

ii. 1[a]: a bottom package substrate

212. *Chen* discloses “a bottom package substrate.” *Chen* discloses **package component 56** (bottom package substrate). *Chen* explains “[p]ackage component 56 may be a **package substrate**, an interposer, a device die, a Printed Circuit Board (PCB), or the like.” EX1006 at [0018], [0024] (“a package substrate”), FIGs. 8–10. *Chen*’s package component 56 is “electrically couple[d] [to] the circuit devices in package component 62” via “TAV modules 28.” *Id.* at [0019], [0020] (In “an

56.”). As shown in figures below, *Chen’s* bottom package substrate in the PoP is very similar to that of the ’202 Patent.





EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

213. Thus, in my opinion, *Chen* discloses each limitation of claim 1[a].

iii. 1[b]: a top package substrate stacked on top of the bottom package substrate

214. *Chen* discloses “a top package substrate stacked on top of the bottom package substrate.” *Chen* discloses package substrate within top package component 62 (top package substrate) stacked on top of package component 56 (bottom package substrate). Similar to package component 56, *Chen* explains “package component 62 is a package that includes a device die (not shown) bonded to a **package substrate** (not shown), an interposer (not shown), or the like.” EX1006 at [0019]. Accordingly, *Chen* teaches top package component 62 includes a top package substrate upon which a device die is mounted. In this way, the device die is

electrically and mechanically connected to the overall package through the top package substrate, which serves as an interface. *Chen* also teaches the package component 62 (including the top package substrate) is stacked on top of package component 56 (bottom package substrate) as shown in FIG. 9 below. *See also* EX1006 at [0024] (“[*Chen’s* PoP] device includes a bottom package, and a top package component bonded to the bottom package. The bottom package includes a package substrate, a plurality of connectors over the package substrate.”), [0018] (“package 46 [] bonded to package component 56 to form bottom package 60”), FIGs. 9–11. As shown in figures below, *Chen’s* top package substrate stacked on top of the bottom package substrate is very similar to that of the ’202 Patent.

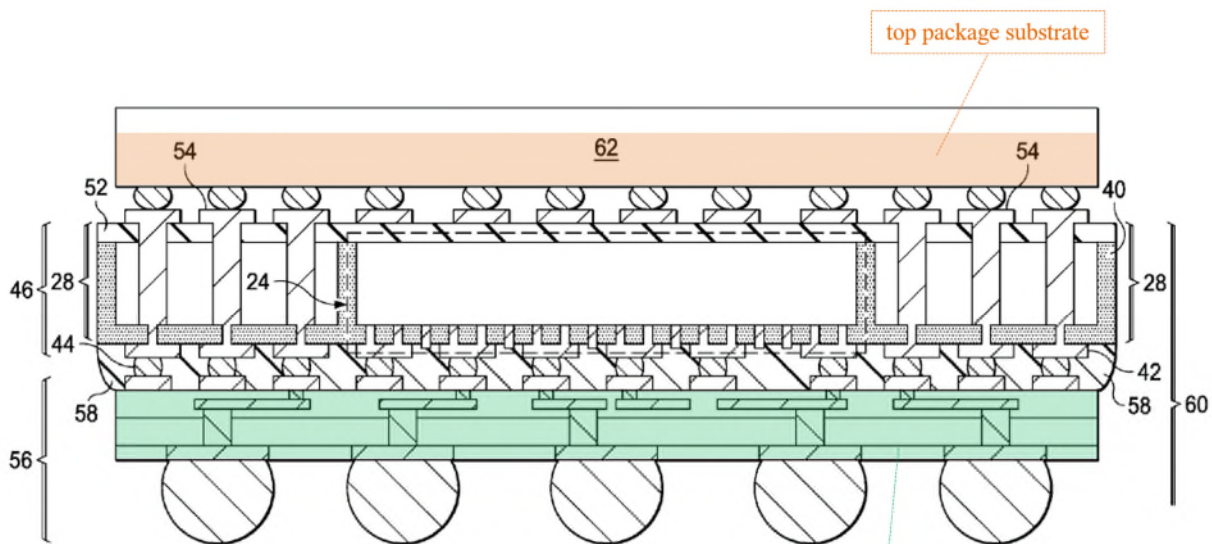
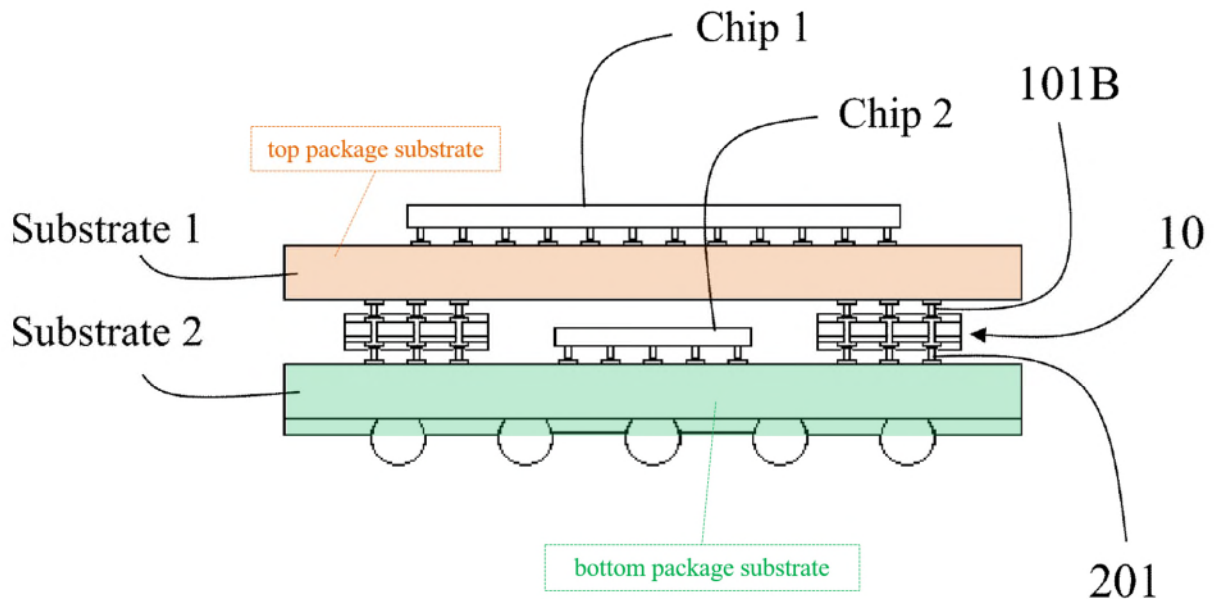


FIG. 9

Fig.8



EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

215. Thus, in my opinion, *Chen* discloses each limitation of claim 1[b].

- iv. **1[c]: at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate**

216. *Chen* discloses “at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.” *Chen*’s **Through-Assembly Via (TAV) modules 28** (spacer connector) are interposed between **package substrate in top package component 62** (top package substrate) and **package component 56** (bottom package substrate) and “TAV modules 28 are used to electrically couple” the two substrates. EX1006 at [0019], [0021] (“In the

embodiments, the connection between top package component 62 and bottom package 60 is through TAV modules 28, rather than large solder balls.”). “TAV modules 28 are integrated modules that are pre-formed” and “include substrate 34, which may be a semiconductor substrate such as a silicon substrate.” *Id.* at [0010]. As shown in FIG. 9 below, TAV modules 28 also define a space between *Chen’s* top and bottom package substrates, so that “package component 24 includ[ing] one or a plurality of device dies” can be placed between the two substrates. *Id.* at [0009]; FIGs. 9–11. As shown in figures below, the way that *Chen’s* spacer connectors interposed between the bottom package substrate and the top package substrate is very similar to that of the ’202 Patent.

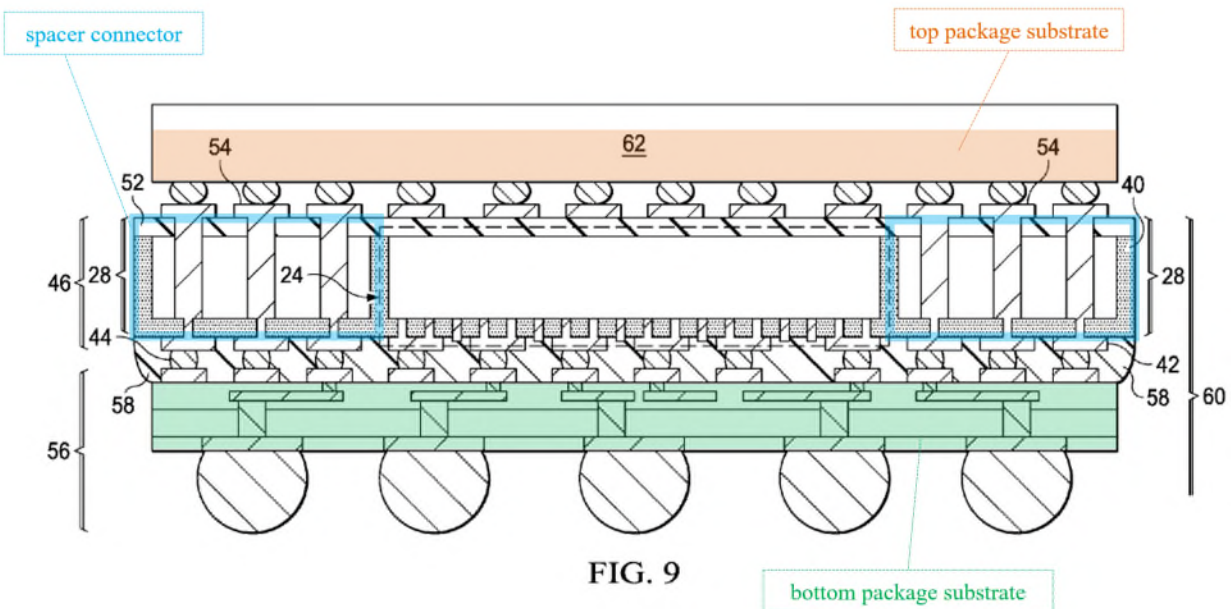
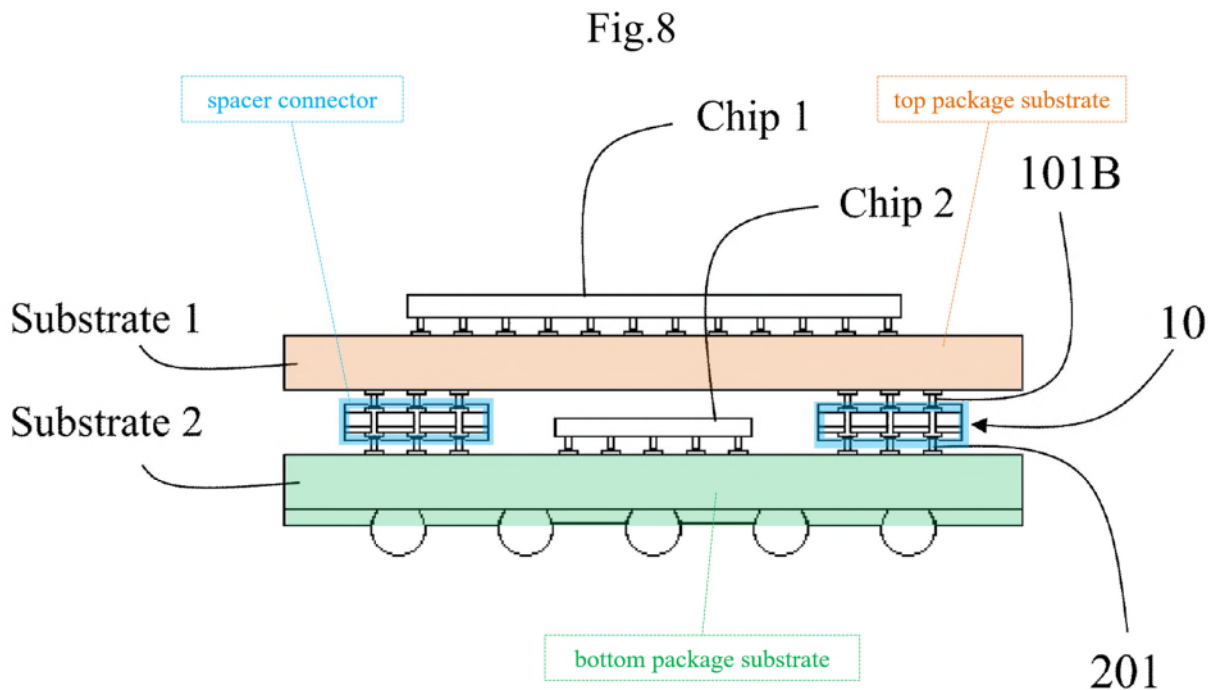


FIG. 9



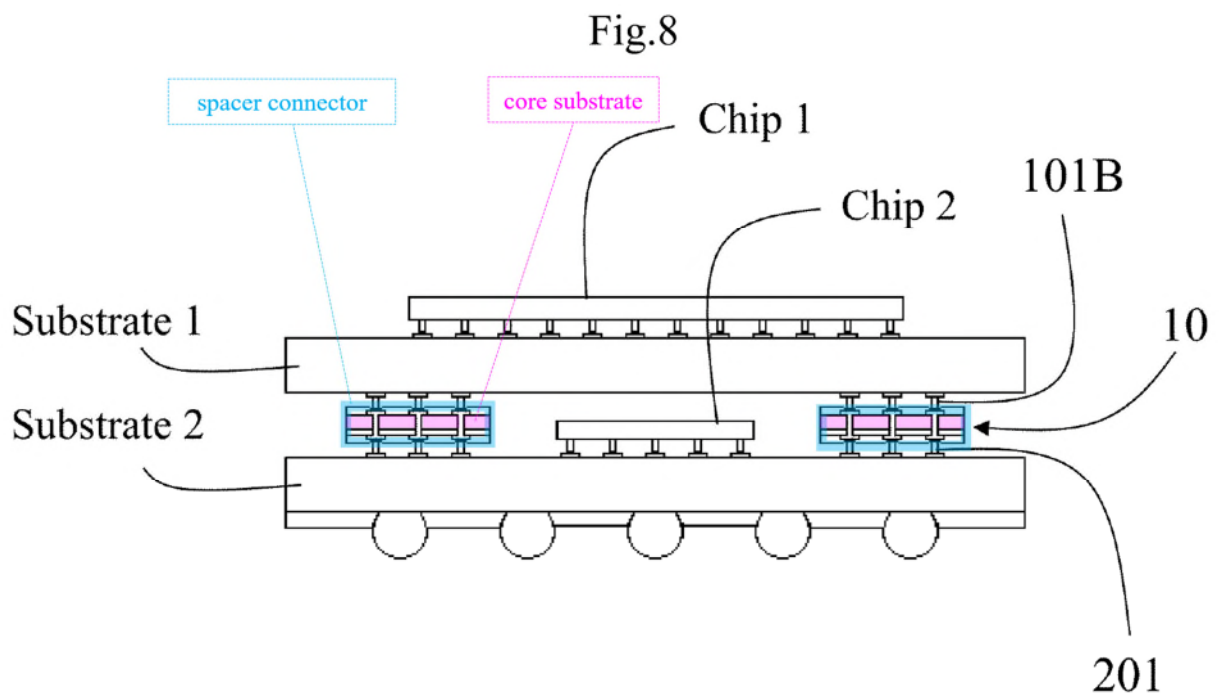
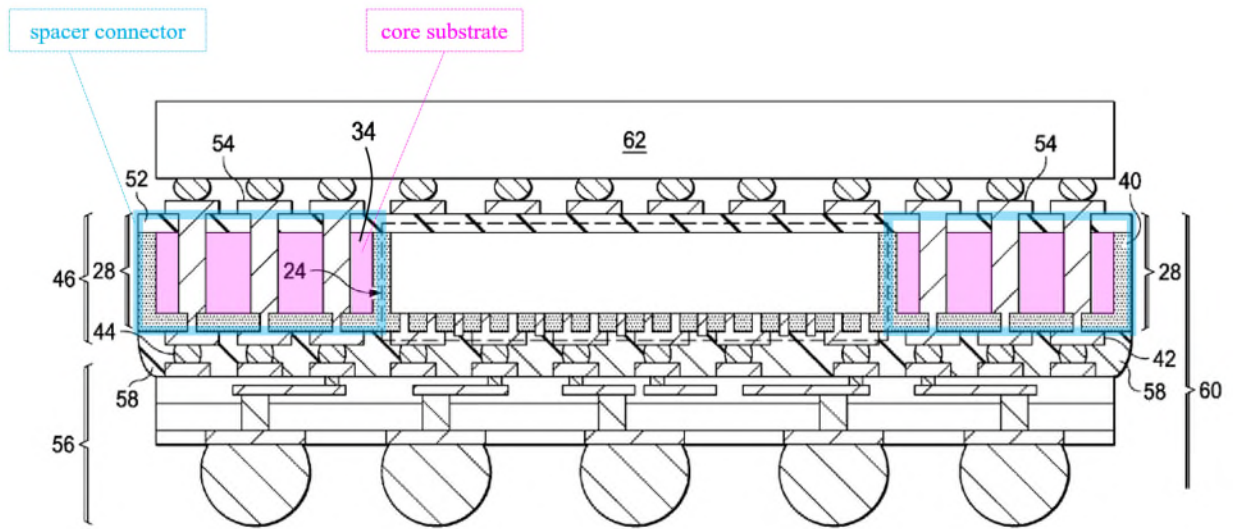
EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

217. Thus, in my opinion, *Chen* discloses each limitation of claim 1[c].

v. 1[d]: the spacer connector comprises a core substrate

218. *Chen* discloses “the spacer connector comprises a core substrate.” *Chen* discloses “TAV modules 28 [spacer connector] include substrate 34 [core substrate],” “which may be a semiconductor substrate such as a silicon substrate.” EX1006 at [0010]. *Chen* also discloses “TAV Module ... includes a substrate” (*id.* at [0023]), and “may be formed using lithography processes and/or other processes that are used on silicon substrates” (*id.* at [0021]). *See also id.* at [0024] (“The TAV module ... includes a substrate.”), FIGs. 1, 6, 9. As shown in figures below, *Chen*’s spacer connector comprising a core substrate that is very similar to that of the ’202

Patent.



EX1006 at FIG. 9 (top)³; EX1001 at FIG. 8 (bottom).

219. Thus, in my opinion, *Chen* discloses each limitation of claim 1[d].

vi. 1[e]: a plurality of metal pillars, each passing through the core substrate

220. *Chen* discloses “a plurality of metal pillars, each passing through the core substrate.” *Chen* explains TAV modules 28 (spacer connector) include “[t]hrough-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34. Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like.” EX1006 at [0010]. “Through-substrate vias 32” are further “connected to, and are aligned to” “metal posts 30.” *Id.* at [0011]. Like through-substrate vias 32, metal posts 30, may be formed as “copper posts.” *Id.* at [0010] (“TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions⁴ of TAV modules 28”), FIG. 9 (below). Accordingly, *Chen*’s through-substrate vias 32 and metal posts 30 together form the metal pillars, each passing through substrate 34 (core substrate). *Chen*’s metal pillars “electrically connect[] the features on opposite sides of TAV modules 28.” *Id.* at [0022], FIGs. 9,

³ Unless otherwise noted, numerical references 30, 32, and/or 34 annotated in FIGs. 6–7, 9 of *Chen* are added in view of FIGs. 1, 4, 6.

⁴ This refers to FIG. 1 before TAV module 28 is flipped upside down during “carrier switch,” EX1006 at [0015]. In the final structure as shown in FIG. 9 metal posts 30 are placed at the bottom side of TAV module 28.

EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

spacer connector

core substrate

metal pillars

60

62

54

32

34

52

40

28

24

46

44

58

56

30

42

Fig. 8

Substrate 1

Substrate 2

Chip 1

Chip 2

core substrate

spacer connector

metal pillars

10

101B

201

EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

221. Thus, in my opinion, *Chen* discloses each limitation of claim 1[e].

vii. 1[f]: a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars

222. *Chen* discloses and/or renders obvious “a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.” *Chen* discloses multiple [Redistribution Lines \(RDLs\) 54](#) (top metal pads), each on a top end of a corresponding [through-substrate via 32](#) and [metal post 30](#) (together, metal pillars) among the metal pillars. *Chen* explains that “TAV modules 28 may include redistribution layer(s) [RDLs] that include redistribution lines and **metal pads** on the top sides of TAV modules 28.” EX1006 at [0011]. It goes on to state: “Alternatively, no redistribution layer is formed on either side of one or each of TAV modules 28, metal posts 30 are connected to, and are aligned to, through-substrate vias 32, with no redistribution lines between metal posts and through-substrate vias 32.” *Id.* *Chen* made it clear that RDLs, including redistribution lines and metal pads, can be located on both sides of a TAV module. *See also id.* at [0014] (“RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer.”).

223. RDLs, also referred to as redistribution layers, are standard structures in semiconductor packaging technology, used to reroute I/O of a chip. It was well-known in the art that RDLs include both metal lines and metal pads. *See* EX1006 at [0011]. I have used RDLs in WLPs as documented in US Patent No. 6,441,487 as

shown in my CV. EX1030 at 7. The metal lines are elongated features patterned in the RDLs, serving as a routing element providing an electrical connection between one or more points, whereas the metal pads are enlarged metal regions of the RDLs, serving as interface or termination points. In my opinion, a POSITA would have recognized the portions of RDLs 54 shown in FIG. 9 are enlarged regions of the RDLs, i.e., contact pads, for the connectors between substrates. These are metal pads, not metal lines, which would not be able to facilitate the connection with the connectors. Indeed, the '202 Patent discloses its own “metal pads” with the same shape as RDLs 54 in FIG. 9. *See e.g.*, EX1001 at FIG.s 5A–B (top metal pads 152).

224. As shown in FIG. 9 below, each of the top metal pads of the RDLs 54 is disposed on a top end of a corresponding through-substrate via 32 and metal post 30 for electrical connection of TAV modules 24 to package component 62. EX1006 at [0017] (“RDLs 54 are then formed on dielectric layer 52.”), FIGs. 6–7, 9 (below).

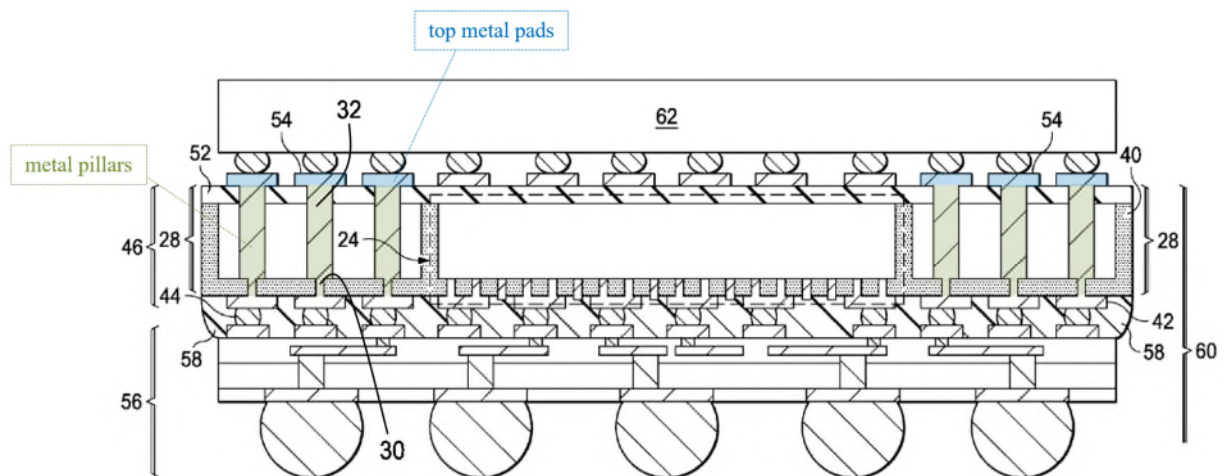


FIG. 9

EX1006 at FIG. 9.

225. To the extent that Patent Owner argues *Chen*'s reference to "metal pads on the top sides of TAV modules 28" is limited to RDLs 42⁵ below TAV modules 28 (but not RDLs 54) in FIG. 9, as explained above, such an interpretation directly contradicts the express disclosures in paragraph [0011] and is inconsistent with a POSITA's understanding of RDLs.

226. Even assuming that *Chen* only expressly discloses RDLs 42 include metal pads, *Chen* still discloses and/or renders obvious this limitation. *Chen* uses the same term "Redistribution Lines (RDLs)" for both RDLs 54 and RDLs 42, which share the exact same shape/shade in FIG. 9. EX1006 at [0014], FIG. 9. *Chen* also teaches "RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer," expressly disclosing RDLs 42 include metal pads. *Id.* at [0014], [0011]. There is, in my opinion, no practical reason to use different materials to construct RDLs on top and bottom sides of the TAV modules. Accordingly, *Chen*'s RDLs 54, which share the same term, shape, and shade as RDLs 42, also include "metal pads," as shown in FIG. 9.

⁵ If the reference to "metal pads on the top sides of TAV modules 28" in [0011] was based on FIG. 1, "the top sides" would become the bottom sides of TAV modules 28 in the final PoP structure because TAV modules 28 are flipped upside down after "a carrier switch is performed." EX1006 at [0015], FIG. 5. Regardless, as I further explained, a POSITA would have understood that RDLs 54, just like RDLs 42, include metal pads.

227. It would have been also obvious for a POSITA to implement RDLs 54 as metal pads as well known in the art. As explained above §X.A.vii, metal pads are widely used in micro-packaging process for reliable electrical connection of metal pillars, like *Chen*'s through-substrate vias 32 and metal posts 30. §X.A.vii. Metal pads provide a wider landing area for metal pillar connections, thus misalignment errors during the manufacturing processes are minimized. EX1007 at 13:12-41; §X.A.vii. Further, utilizing metal pads on top of metal pillars may prevent contaminants from flowing into or through (in case of using hollow metal pillars) the metal pillars during the manufacturing process. EX1011 at 7, 10 (explaining the problem of contaminants, such as solder and solder resist, flown into metal pillars when no metal pads are used); §X.A.vii.

228. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of claim 1[f].

viii. 1[g]: wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate

229. *Chen* discloses “wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.” *Chen* discloses a bottom end of each of through-substrate vias 32 and metal posts 30 (metal pillars) protrudes downwardly from a bottom surface of substrate 34 (core substrate). As explained above for §XIII.A.vii, through-substrate

vias 32 and metal posts 30 “connected to, and are aligned to” the bottom of through-substrate vias 32 together form the claimed metal pillars within TAV modules 28 (spacer connector). EX1006 at [0010]–[0011] (“[M]etal posts 30 are connected to, and are aligned to, through-substrate vias 32.”), FIGs. 1, 4. And, as shown in FIGs. 5–6, 9 (below), portions of the metal pillars (metal posts 30) protrude downwardly from a bottom surface of substrate 34. *Id.*; *see also id.* at FIG. 1 (showing metal posts 30 protruding above substrate 34 before “carrier switch,” where TAV modules 24 are flipped upside down.), [0009] (Referring to FIG. 1 before a carrier switch, “Through-Assembly Via (TAV) modules 28 are then placed on release layer 22.”), [0015] (“Referring to FIG. 5, a carrier switch is performed.”).

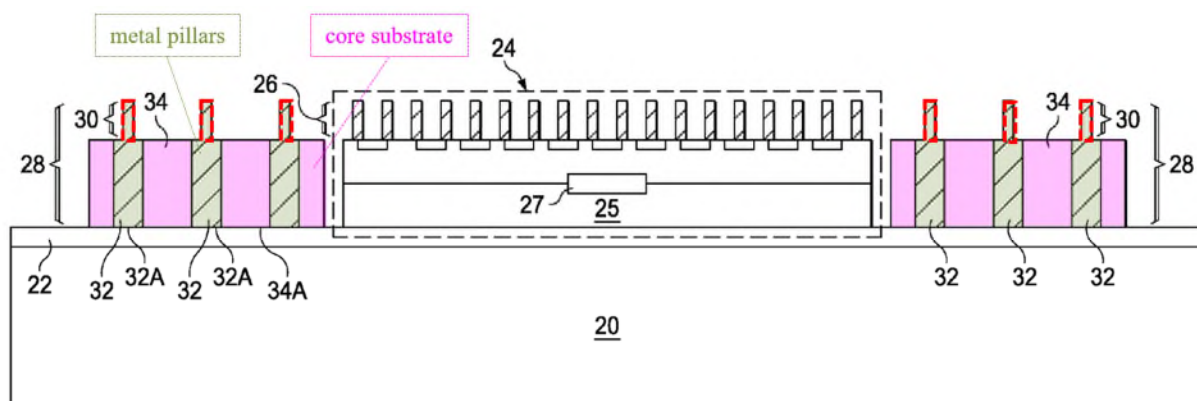


FIG. 1

Id. at FIG. 1 (showing metal posts 30 protruding above substrate 34 before “carrier switch,” where TAV modules 24 are flipped upside down.)

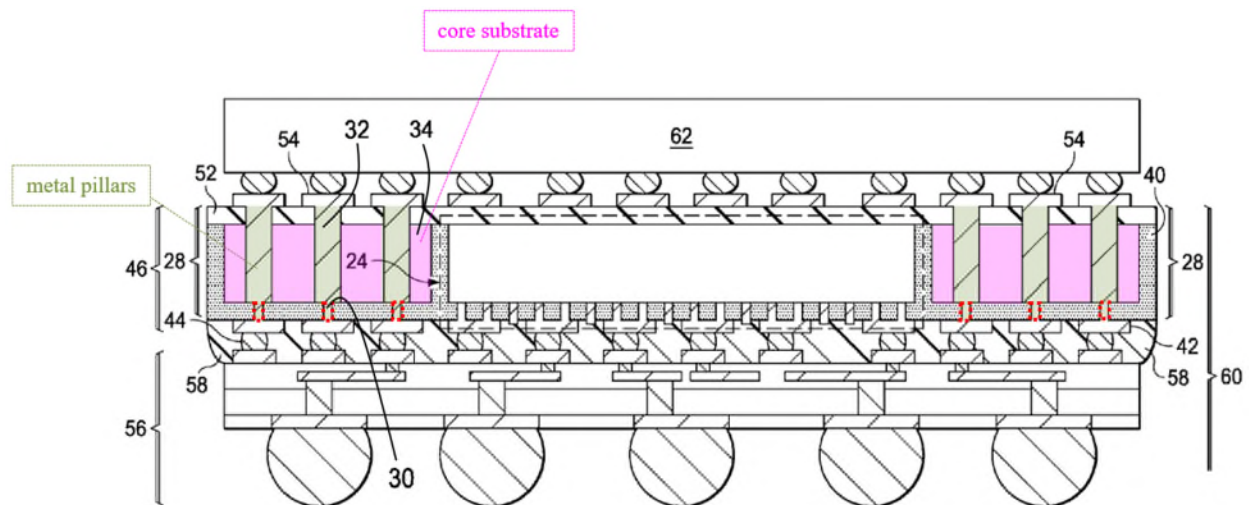


FIG. 9

EX1006 at FIG. 9 (dashed red lines showing metal posts 30 protruding downwardly from substrate 34 in the final PoP structure).

230. Thus, in my opinion, *Chen* discloses each limitation of claim 1[g].

- ix. **1[h]: the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector**

231. *Chen* discloses and/or renders obvious “the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.” *Chen* discloses package substrate in top package component 62 (top package substrate) has, on a bottom surface thereof, multiple (upper) connectors 44 (bottom metal pillars) each coupled to a corresponding through-substrate via 32 and

metal post 30 (together, metal pillars) of TAV modules 28 (spacer connectors).

EX1006 at FIG. 9:

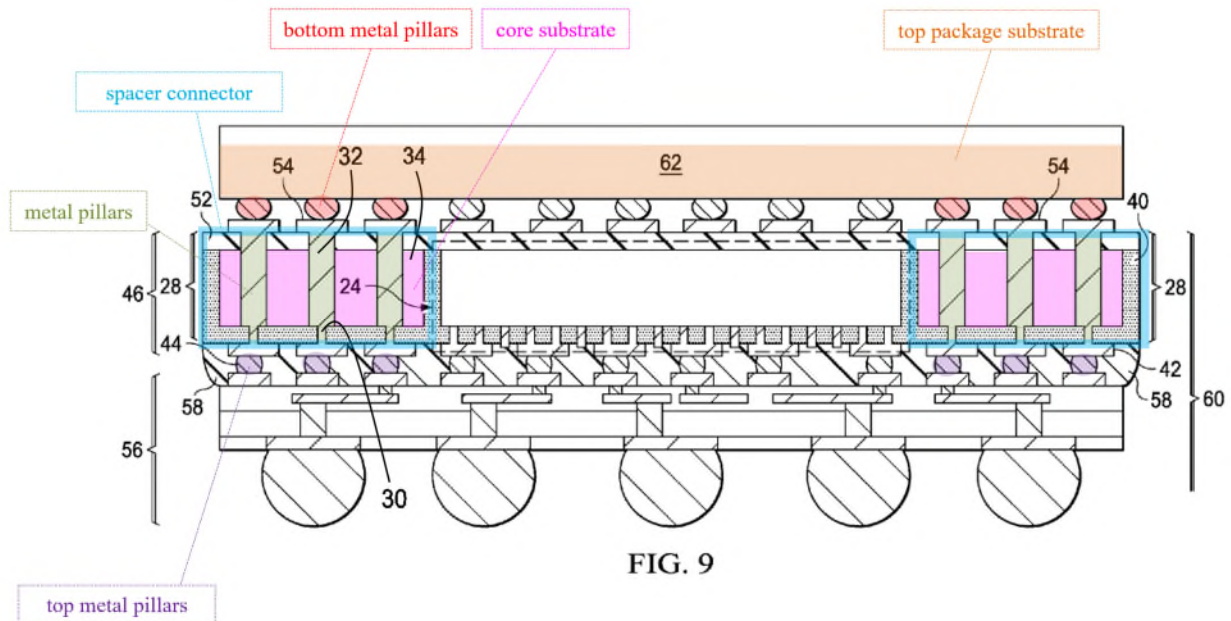


FIG. 9

232. While not all of connectors in FIG.9 are specifically identified as connectors 44 (e.g., the connectors between the top package substrate and bottom package 60), a POSITA would have understood connectors 44 refer to both the upper and lower connectors that connect TAV modules and package component 24 to the top and bottom package substrates, respectively, given the same cross-hatching applied to all connectors and the same function served by both sets of connectors. EX1006 at FIG. 9.

233. Each of (upper) connectors 44, as shown in FIG. 9 above, is coupled to a corresponding through-substrate via 32 and metal post 30 (together, metal pillars) in order to electrically connect TAV modules 28 and package component 62.

EX1006 at [0019] (“TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.”).

234. *Chen* expressly teaches connectors 44 may “include **solder balls** ... **metal pillars**, or **metal pillars** and solder caps, which may also be formed through plating.” EX1006 at [0014], FIGs. 4, 9. As discussed above in §VII.A, while the correct construction requires a columnar structure, Patent Owner appears to broadly interpret the claimed metal pillar to include any metal structures, including solder structures, EX1004 at ¶¶45–46; §VII.A. *Chen*’s (upper) connectors 44 disclose “bottom metal pillars” under Patent Owner’s broad interpretation (which includes “solder balls”) and Petitioner’s correct construction (“metal pillars”).

235. If the Board, however, finds that *Chen* does not expressly disclose bottom metal pillars under the correct construction of metal pillars in §VII.A, *Chen* at least renders 1[h] obvious.

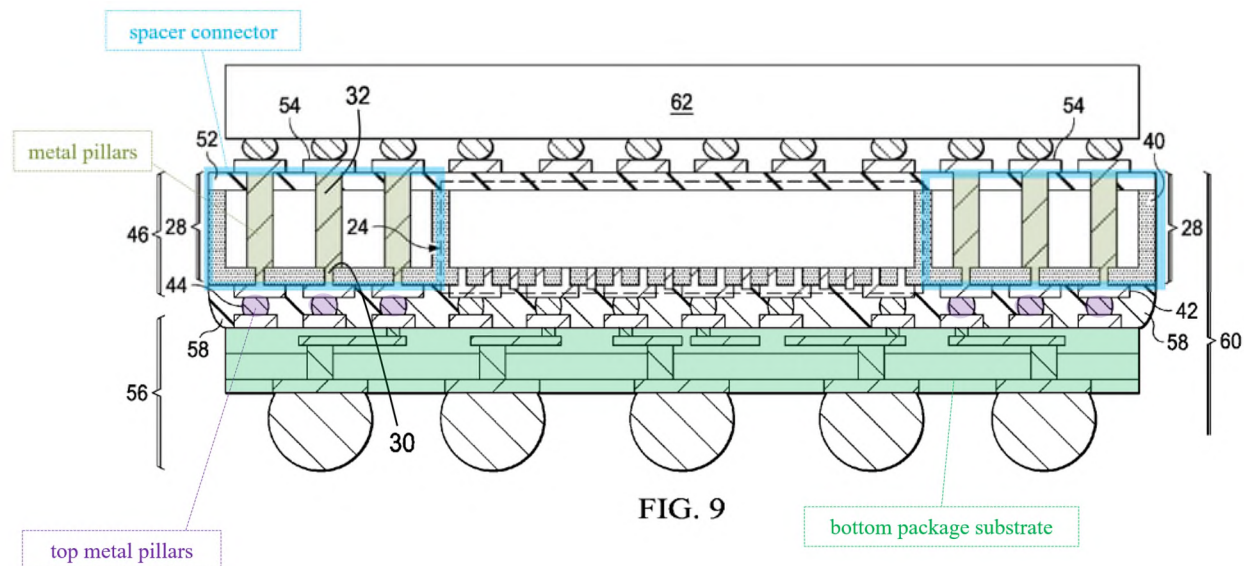
236. *Chen* recognizes the drawbacks of using “solder balls” in microelectronic PoP packaging and the benefit of metal pillars as a more favorable replacement of “solder balls.” For example, *Chen* explains that “the amount of the solder balls that can be used in a PoP structure is limited” because “the lateral sizes of the solder balls are [] large.” EX1006 at [0002]. *Chen* further explains that metal pillars are a favorable interconnect structure for PoP assemblies because “the pitches and the sizes of [metal pillars] may be very small.” EX1006 at [0021]. Accordingly,

Chen expressly recommends “[c]onnectors 44 may also include metal pillars, or metal pillars and solder caps, which may also be formed through plating.” *Id.* at [0014]. Notably, (upper) connectors 44 are disposed in the narrow region that connects top package component 62 and TAV modules 28. This region is spatially constrained and must accommodate multiple vertical electrical interconnects within a limited lateral footprint, which makes “metal pillars” with fine pitches favorable interconnects. *See also* EX1008 at [0004]-[0005] (“[M]etal posts ... are used in stack structures so as to overcome the above-described drawbacks” of solder balls, including “a tilted stack structure,” “poor coplanarity,” “positional deviation of solder joints between the packages,” and “solder bridge.”); EX1005 at [0015] (“[T]he first and second electrical connectors [connecting package substrates and spacer connectors in a similar PoP structure] are metal pillars, e.g. copper pillars.”).

237. In my opinion, a POSITA would have found it obvious to implement (upper) connectors 44 as metal pillars to address the drawbacks of solder balls, such as “a tilted stack structure,” “poor coplanarity,” “positional deviation of solder joints between the packages,” and “solder bridge,” EX1008 at [0004], and to realize the fine-pitch interconnects as required by *Chen*’s PoP structure in light of the teachings of *Chen* itself and/or the knowledge of a POSITA. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of claim 1[h].

- x. **1[i]: the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector**

238. *Chen* discloses and/or renders obvious “the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.” *Chen* discloses package component 56 (bottom package substrate) has, on a top surface thereof, multiple (lower) connectors 44 (top metal pillars), each “formed to connect to [corresponding] metal posts...30” and through-substrate vias 32 (together, metal pillars) of TAV modules 28 (spacer connector). EX1006 at [0014], FIGs. 8–9 (showing lower connectors 44 on package component 56 are connected to corresponding metal posts 30 and through-substrate vias 32 via metal pads 42):



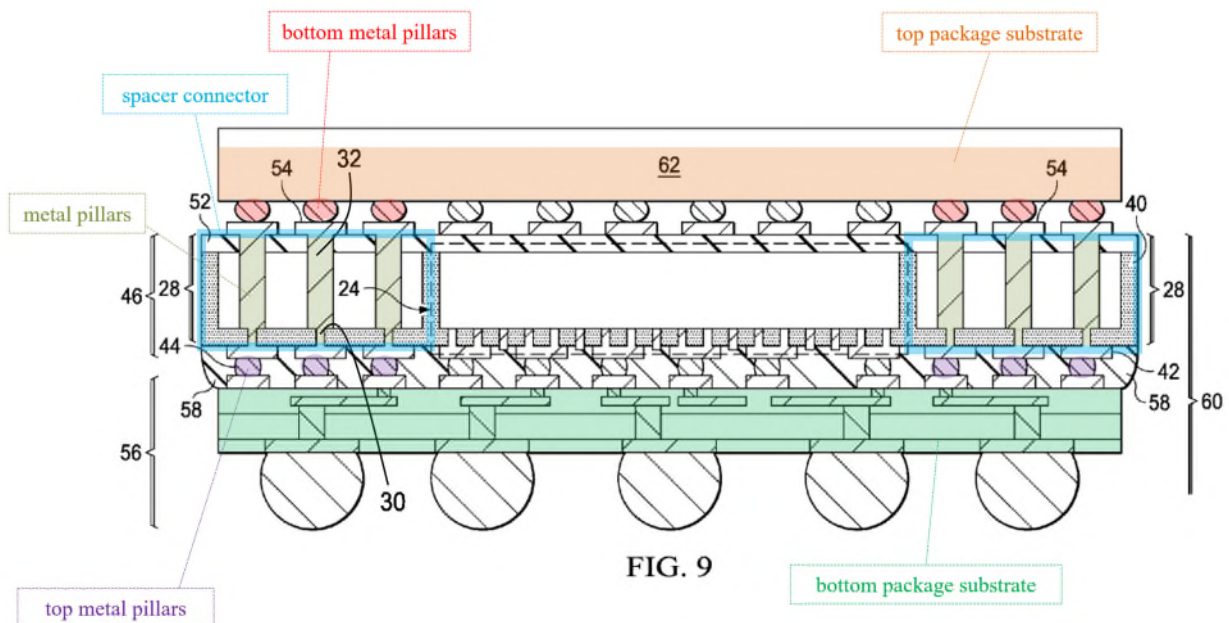
239. As explained above, *Chen* teaches connectors 44 may “include **solder balls...**[or] **metal pillars**,” EX1006 at [0014], and Patent Owner appears to broadly interpret the claimed metal pillar to include any metal structures, including “solder balls,” EX1004 at ¶¶45–46. Thus, like *Chen*’s bottom metal pillars, *Chen*’s (lower) connectors 44 disclose “top metal pillars” under both Patent Owner’s broad construction and Petitioner’s correct construction of “metal pillars.” EX1006 at [0014]; §VII.A.

240. If the Board finds that *Chen* does not expressly disclose top metal pillars, *Chen* renders 1[i] obvious for the same reasons discussed above for 1[h]. See §XIII.A.ix. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of claim 1[i].

- xi. 1[j]: the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate**

241. *Chen* discloses “the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.” The package substrate in top package component 62 (top package substrate) is electrically coupled to package component 56 (bottom package substrate) through (upper) connectors 44 (bottom metal pillars) of package substrate in top package component 62, through-substrate vias 32 and metal posts 30 (together, metal pillars) of TAV modules 28 (spacer connector), and (lower) connectors 44 (top metal pillars) of package component 56. EX1006 at FIG. 9. For example, *Chen* discloses “TAV modules 28 [spacer connector] are used to electrically couple ... package component 62 to package component 56.” EX1006 at [0019]; *see also id.* at [0021] (“[T]he connection between top package component 62 and bottom package 60 [including package component 56] is through TAV modules 28”), FIG. 9. The electrical connection between *Chen*’s top and bottom package substrate is formed with “through-substrate vias 32, which are used for electrically connecting the features on opposite sides of TAV modules 28.” *Id.* at [0022]. As shown FIG. 9, the top side

of through-substrate vias 32 is electrically coupled to package substrate in top package component 62 (top package substrate) via (upper) connectors 44 (bottom metal pillars). *Id.* at FIG. 9. Also, the bottom side “connected to, and [] aligned to” metal posts 30, is electrically coupled to package component 56 (bottom package substrate) via (lower) connectors 44 (top metal pillars). *Id.* at [0011], [0014] (“[C]onnectors 44 are formed to connect to metal posts 26 and 30.”), FIG. 9. Accordingly, in *Chen’s* PoP structure, top package component 62 and package component 56 are electrically coupled to one another through a series of metal pillars, including (upper) connectors 44 (connecting top package component 62 and TAV modules 28), through-substrate vias 32 and metal posts 30 (connecting opposite sides of TAV modules 28), and (lower) connectors 44 (connecting TAV modules 28 to package component 56).



EX1006 at FIG. 9.

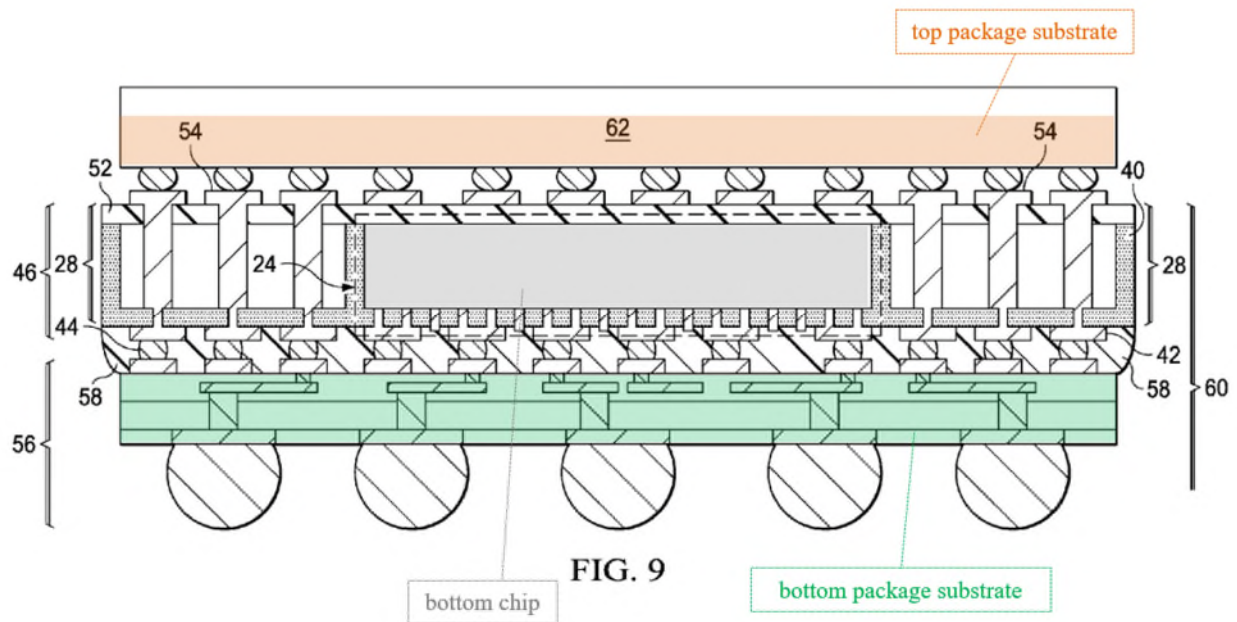
242. Additionally, limitation 1[j] requires “bottom metal pillars **of** the top package substrate” and “top metal pillars **of** the bottom package substrate.” I understand that under Samsung’s claim construction (see §VII.C above), the bottom and top metal pillars are “of” the top and bottom package substrates, respectively, because they are located on the respective package substrates. This is consistent with limitations 1[h] and 1[i], as discussed above, as well as Figures 8, 11, and 14 of the ’202 Patent. EX1001 at FIGs. 8, 11, 14.

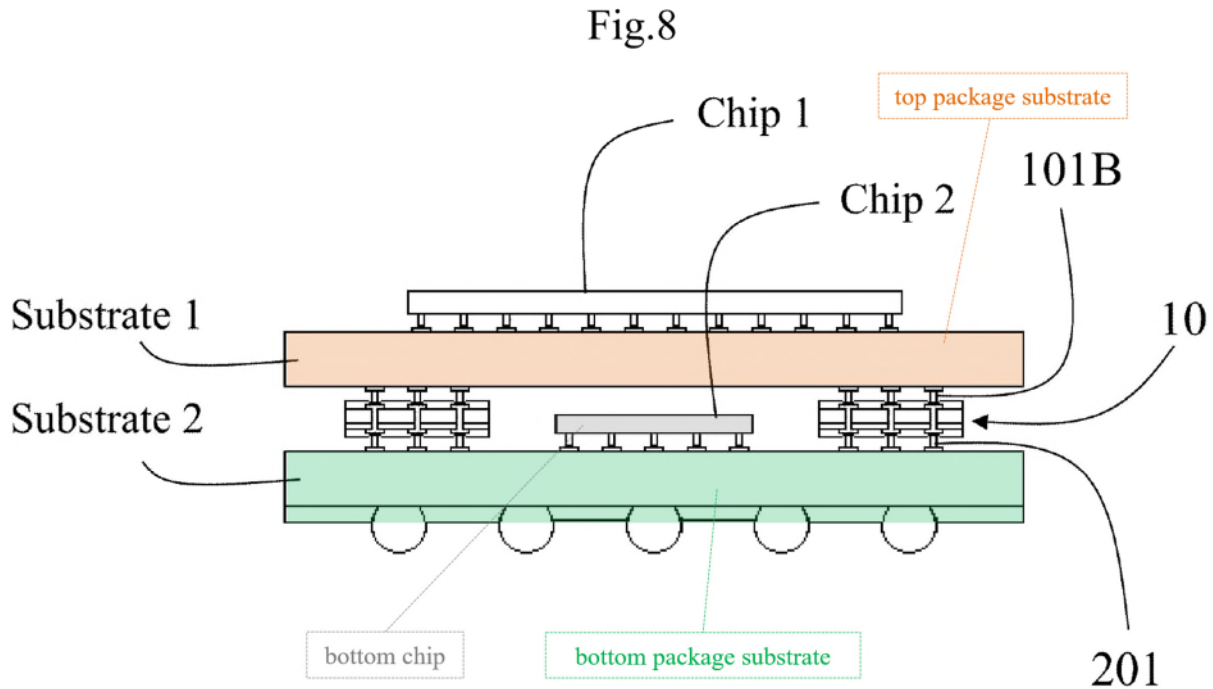
243. Thus, in my opinion, *Chen* discloses each limitation of claim 1[j].

xii. 1[k]: a bottom chip arranged in the space between the bottom package substrate and the top package substrate

244. *Chen* discloses “a bottom chip arranged in the space between the bottom package substrate and the top package substrate.” “For example, package component 24 may include a Central Computing Unit (CPU) **die** or another type of **logic die** having logic circuits. In alternative embodiments, package component 24 includes a plurality of memory dies stacked together.” EX1006 at [0009]. Thus, package component 24 including “one or a plurality of device dies [bottom chip]” is arranged in the space between package substrate in top package component 62 (top package substrate) and package component 56 (bottom package substrate) as shown in FIG. 9 below. *Id.* at FIG.9, [0020] (explaining package component 24 is placed under and “aligned to” top package component 62), FIGs. 10–11 (showing package

component 24 arranged between top package component 62 and package component 56). As shown in figures below, *Chen's* bottom chip arranged in the space between the bottom package substrate and the top package substrate in a way similar to that of the '202 Patent.





EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

245. Thus, in my opinion, *Chen* discloses each limitation of claim 1[k].

xiii. 1[l]: the bottom chip is mounted to the top surface of the bottom package substrate

246. *Chen* discloses “the bottom chip is mounted to the top surface of the bottom package substrate.” As shown in FIG. 9, package component 24 including one or more device dies (bottom chip) is mounted on package component 56 (bottom package substrate) via connectors 44. EX1006 at FIG. 9, *see also id.* at [0018] (“[P]ackage 46 [including package component 24] is bonded to package component 56 to form bottom package 60.”), FIG. 8 (similarly showing package component 24 mounted to the top surface of package component 56 via connectors 44), [0024] (“The package includes a device die, and a TAV Module substantially level with the

device die.”). This configuration is similar to Chip 2 (bottom chip) in the '202 Patent being mounted to the top surface of Substrate 2 (bottom package substrate) via metal connectors. EX1001 at FIG. 8.

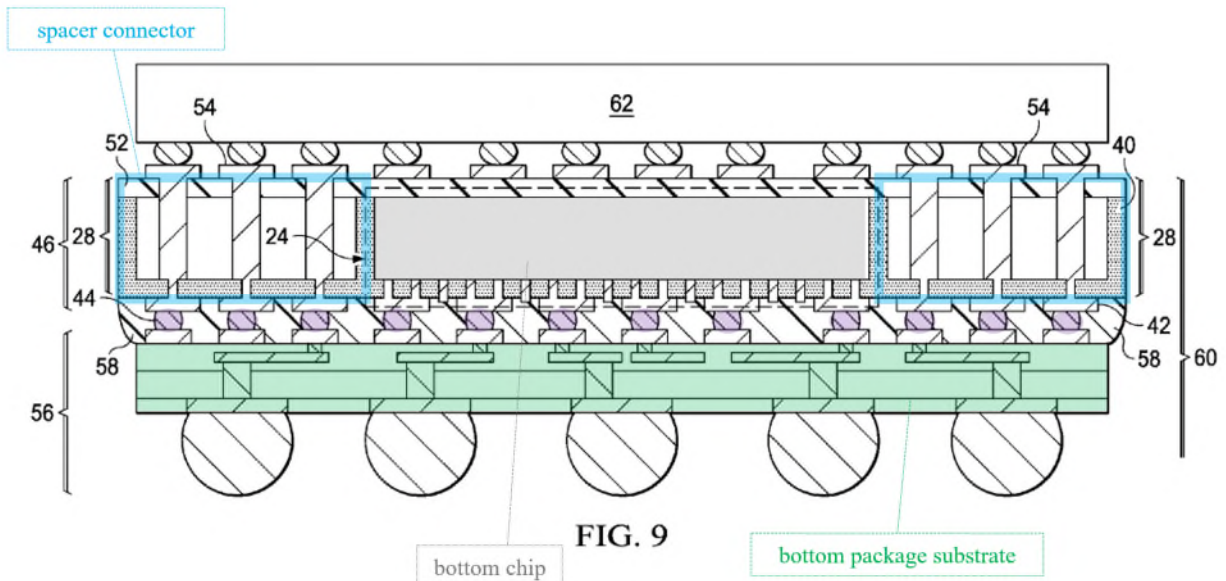
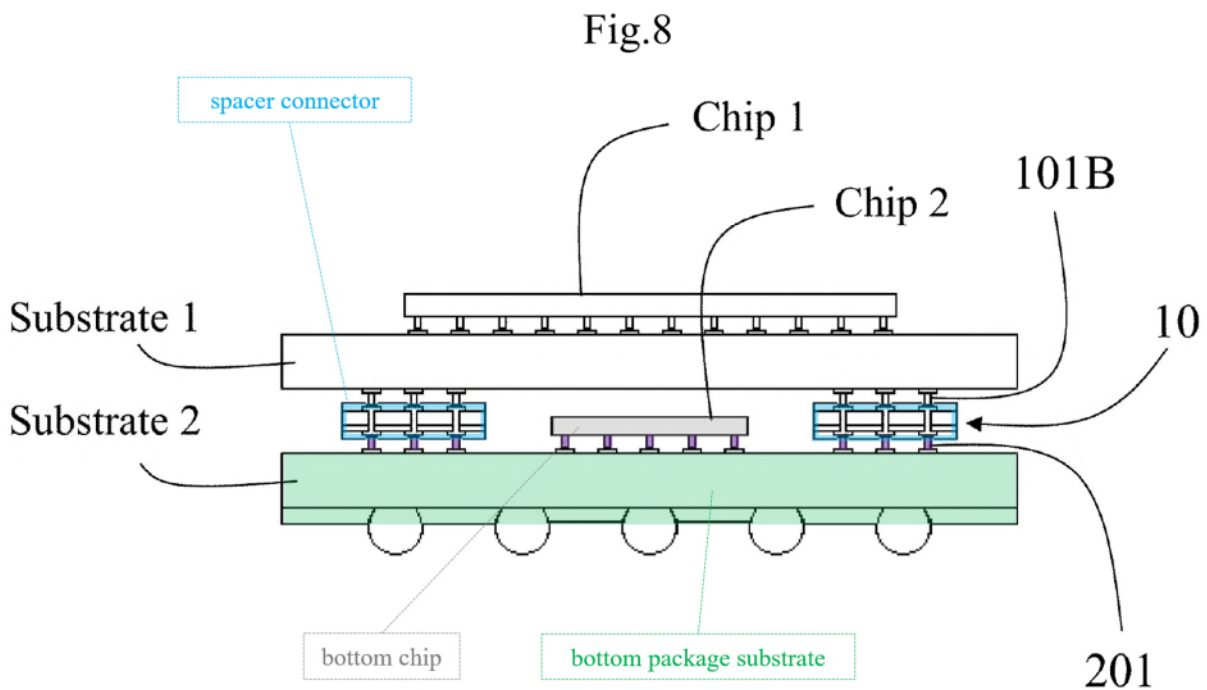


FIG. 9



EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

247. Thus, in my opinion, *Chen* discloses each limitation of claim 1[l].

xiv. 1[m]: the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip

248. *Chen* discloses “the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.” *Chen* expressly discloses “**two TAV modules 28**” (spacer connectors) “disposed on opposite sides of package component 24” (bottom chip). EX1006 at [0012], [0022] (“FIG. 12 illustrates a top view of the structure in FIG. 1 in accordance with alternative embodiments.”), FIGs. 2, 9, 12.

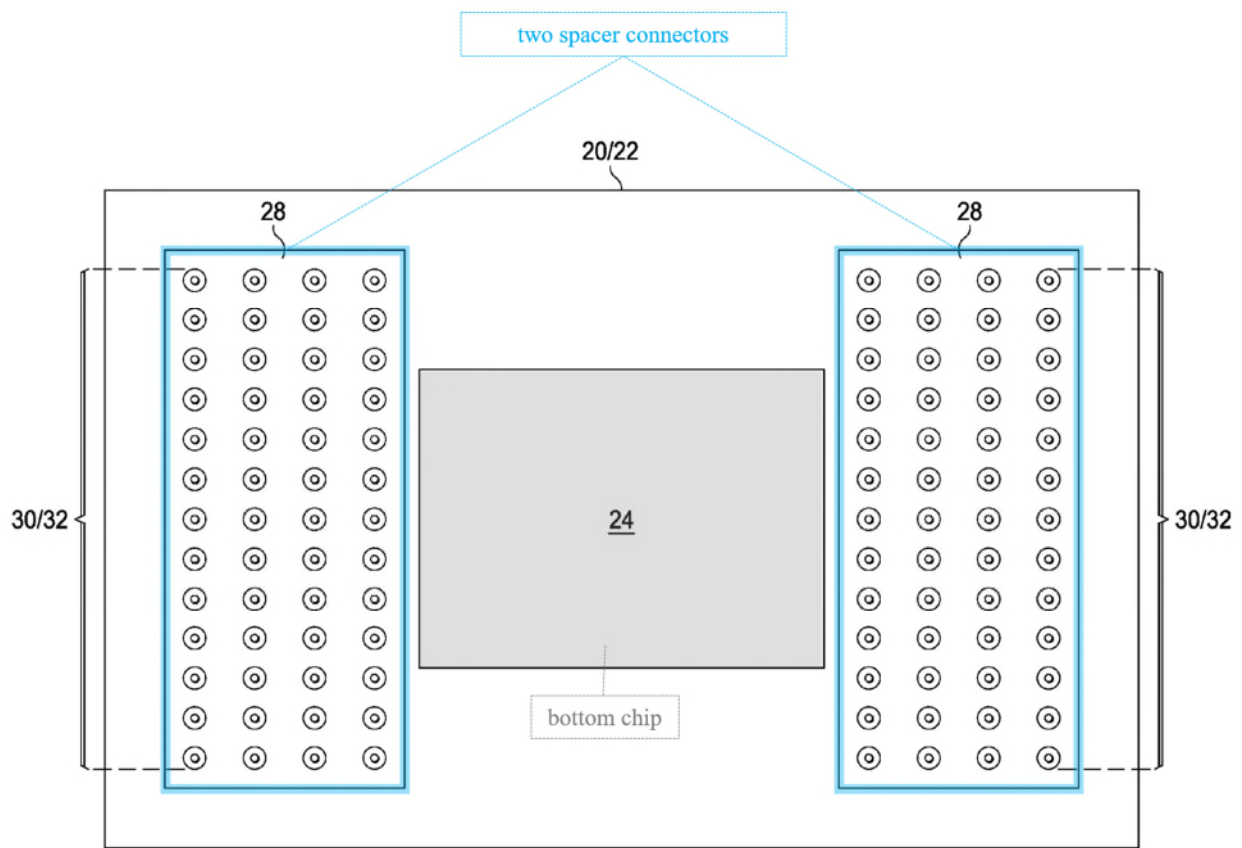
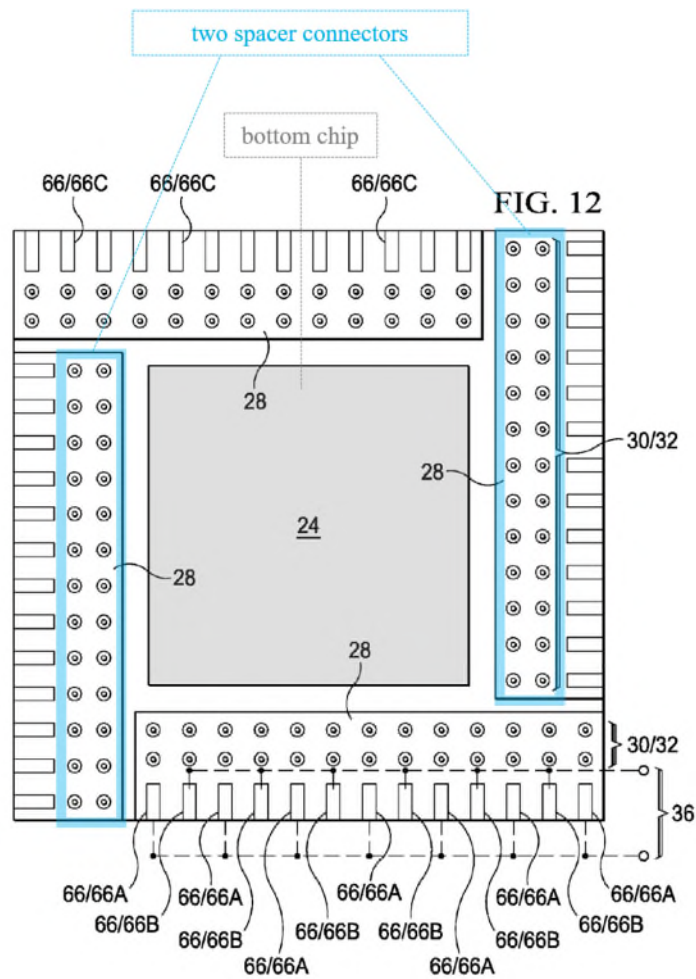


FIG. 2



EX1006 at FIGs. 2, 12 (both top view and FIG. 12 illustrating an alternative embodiment that TAV modules 28 additionally use “strip-shaped vias 66” for dissipating the heat generated from package component 24).

249. As shown in figures below, *Chen’s* two spacer connectors are arranged on opposite sides of the bottom chip in a way similar to that of the ’202 Patent.

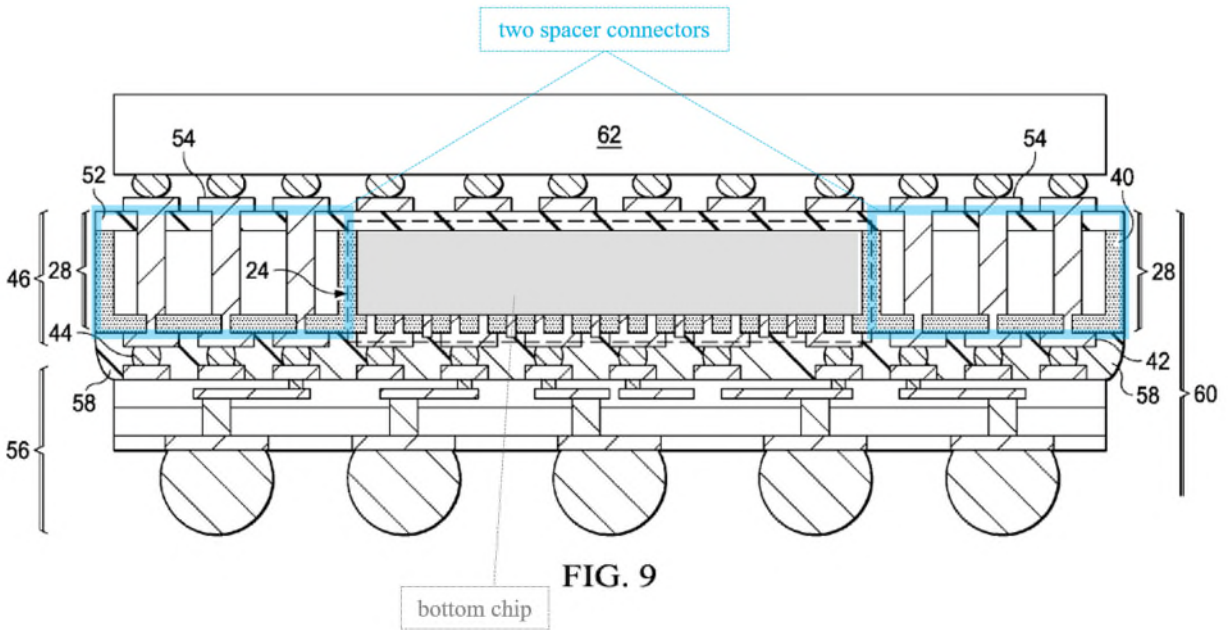
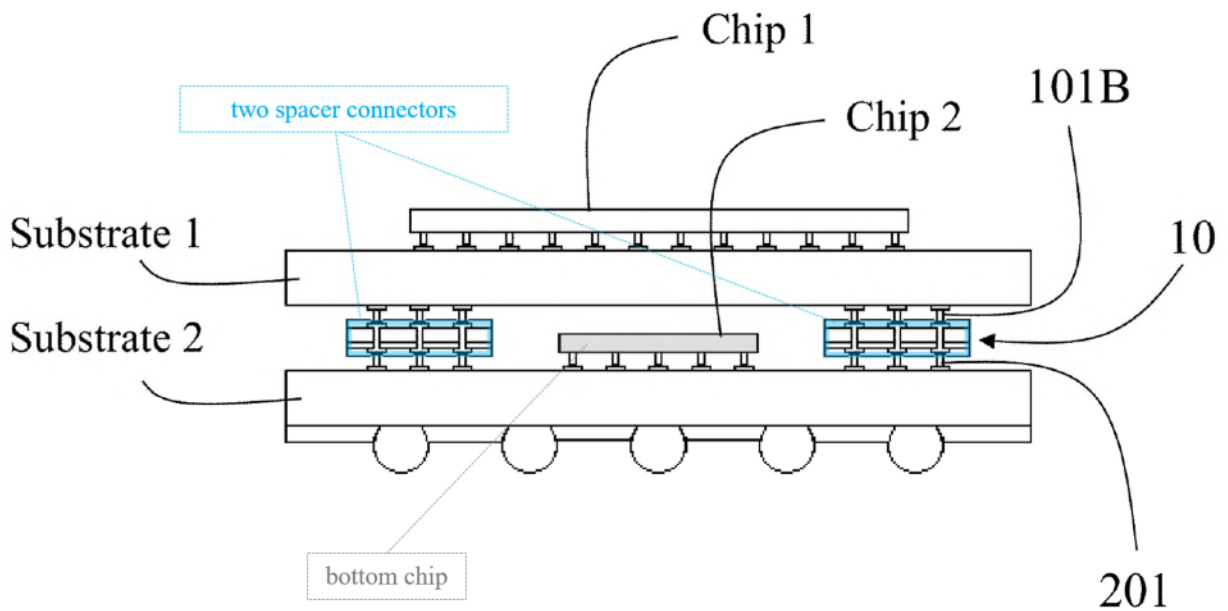


Fig.8



EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

250. Thus, in my opinion, *Chen* discloses each limitation of claim 1[m].

B. Claim 2

- i. the structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate**

251. *Chen* discloses “the structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.” As discussed in §XIII.A.xii–XIII.Axiii and as shown in FIG. 9, *Chen*’s package component 24 (bottom chip) is placed below package substrate in top package component 62 (top package substrate), and thus a top surface of package component 24 is spaced downwardly from the bottom surface of the top package substrate. EX1006 at [0019] (“[P]ackage component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown).”), [0020] (“[P]ackage component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56.”), [0024] (“The package includes a device die, and a TAV Module substantially level with the device die.”), FIG. 9. As shown in figures below, a top surface of *Chen*’s bottom chip is spaced downwardly from the bottom surface of the top package substrate in a way similar to that of the ’202 Patent.

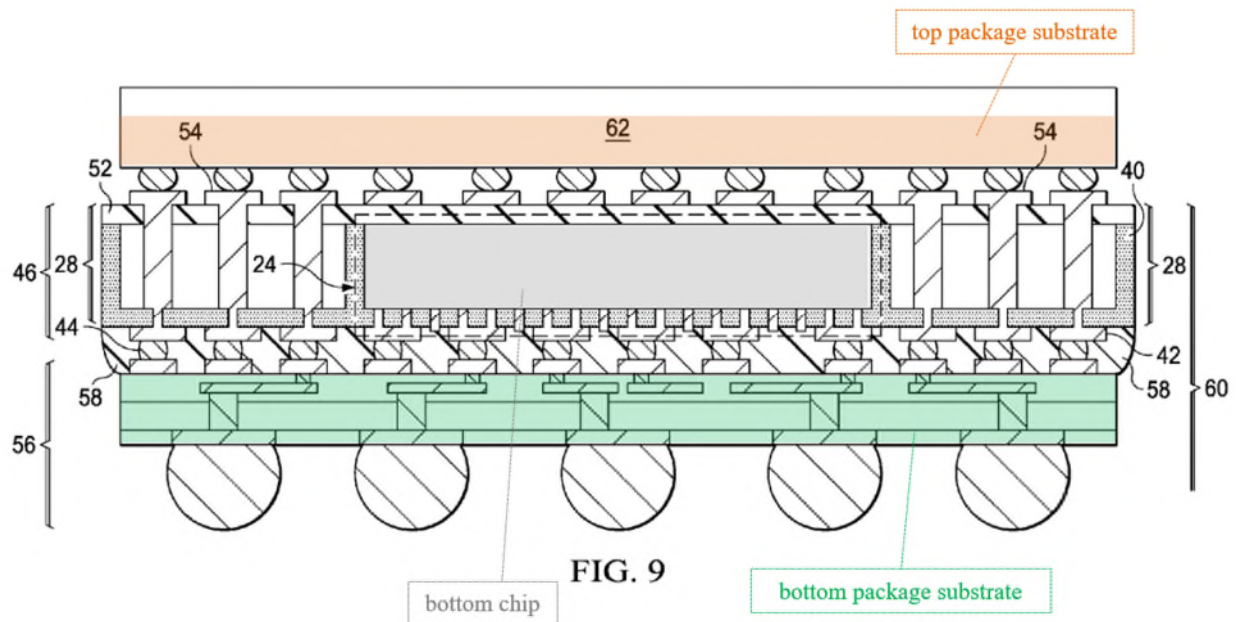
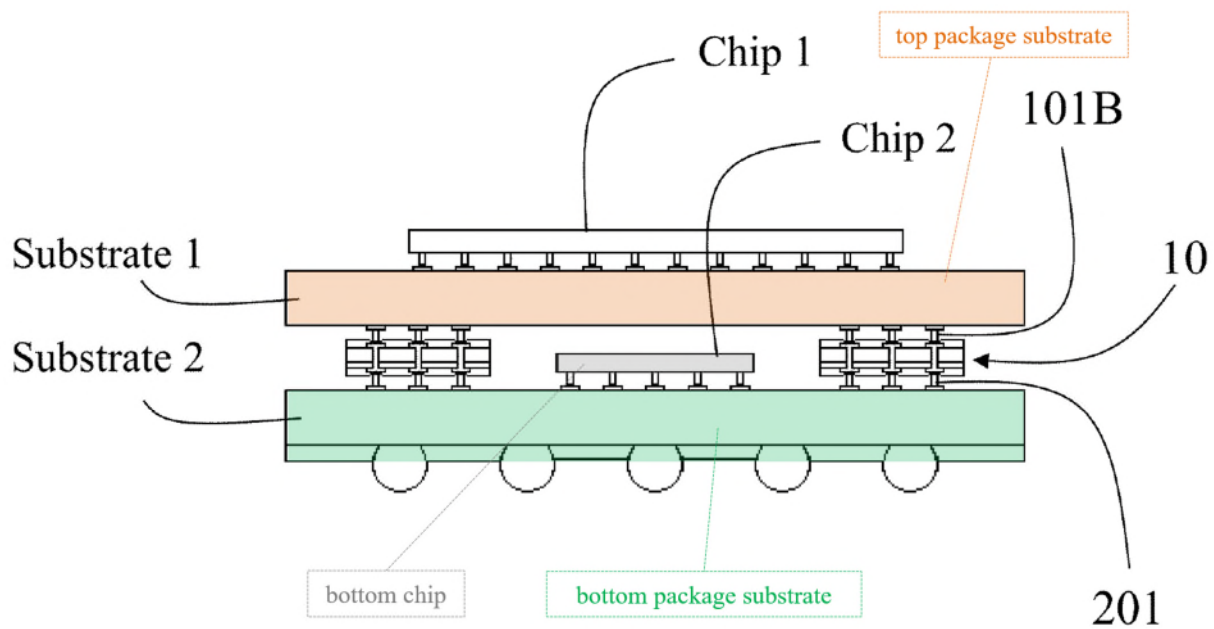


Fig.8



EX1006 at FIG. 9 (top); EX1001 at FIG. 8 (bottom).

252. Thus, in my opinion, *Chen* discloses each limitation of claim 2.

C. **Claim 3**

- i. **3[a]: The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate**

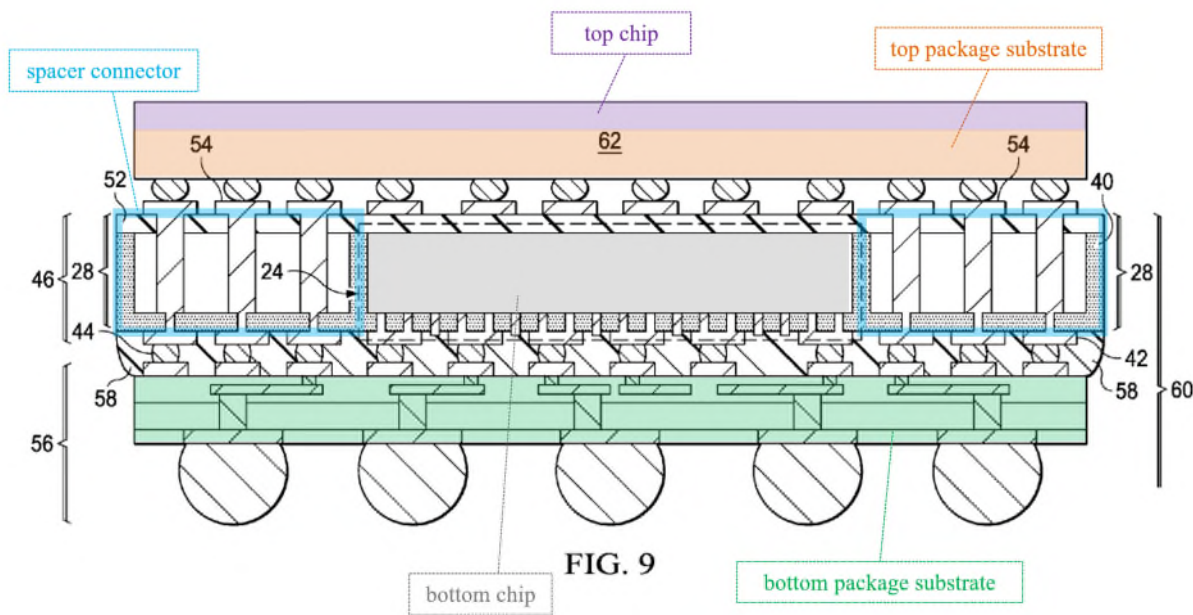
253. *Chen* discloses “[t]he structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate.” *Chen* discloses a top chip (in top package component 62) mounted to the top surface of the top package substrate (also in top package component 62). *Chen* teaches top package component 62 may be “a package that includes a device die (not shown) bonded to a package substrate (not shown).” EX1006 at [0019]. In a PoP structure, when a “device die ... bonded to a package substrate,” the device die is mounted to the top surface of the package substrate, which further interfaces with the spacer connector and the bottom package substrate as discussed above for §XIII.A.xi and as shown in the annotated FIG. 9. *Id.* at FIG. 9 (illustrating a “device die ... bonded to a package substrate” in top package component 62); *see also id.* at FIG. 8, [0009] (explaining in case of “semiconductor substrate,” “active devices (such as transistors)” are disposed “at a top surface of semiconductor substrate”).

254. Thus, in my opinion, *Chen* discloses each limitation of claim 3[a].

- ii. **3[b]: wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors**

255. *Chen* renders obvious “wherein in a direction in which the top package

substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.” As explained directly above for 3[a], *Chen*’s top package component 62 “include[s] a device die [top chip] bonded to a package substrate [top package substrate].” EX1006 at [0019]. *Chen* also teaches that “[i]n some embodiments, top package component 62 [itself] is a device die.” From these disclosures a POSITA would have it found obvious that *Chen*’s device die (top chip), as large as top package component 62 itself in FIG. 9, would have been mounted on the top package substrate in top package component 62 and overlaps package component 24 (bottom chip) and each of the two TAV modules 28 (spacer connectors) in a direction in which the top package substrate is stacked on top of the bottom package substrate as shown in FIG. 9 below. *Id.* at FIG. 9.



EX1006 at FIG. 9 (annotated to illustrate top chip and top package substrate).

256. First, a POSITA would have found it obvious to combine the two embodiments of “top package component 62” disclosed by *Chen*. As discussed, in a first embodiment, *Chen* teaches “[i]n some embodiments, top package component 62 [itself] is a device die” (as large as “top package component 62” in FIG. 9), directly interfacing with bottom package 60. EX1006 at [0019], FIG.9. In a second embodiment, *Chen* discloses package component 62 can be “a package that includes a device die...bonded to a package substrate,” reflecting an alternative arrangement of first mounting the die on a substrate, which then interfaces with bottom package 60. EX1006 at [0019], FIG. 9. This latter approach is generally more preferable and common in semiconductor packaging, as the package substrate offers flexibility in arranging the I/O appropriately to optimize the use of ICs for the PoP assembly. See §V.F. Based on these two embodiments, a POSITA would have found it obvious to mount the device die—“top package component 62”—on a substrate to interface with bottom package 60. Direct interface and through-substrate interface with bottom package 60 are two alternatives taught by *Chen* and also well-known alternatives in the art. Thus, in this case of combining the two embodiments of *Chen*, the device die (top chip), as large as package component 62 itself in FIG. 9, overlaps the bottom chip and each of the two spacer connectors as shown in FIG. 9 above.

257. Moreover, even just considering the second embodiment by itself,

where the device die is mounted on a top package substrate stacked on a bottom substrate, this limitation is obvious. Mounting a top and bottom chip on a top and bottom package substrate, respectively, was a common feature in stacked PoP structure. See, e.g., EX1005 at FIG. 12. When doing so, it was also a well-known design choice to place a top chip larger than a bottom chip. In PoP structure like *Chen's*, where spacer connectors are inserted between a top and bottom package substrate, the top package substrate typically has more space to accommodate a larger chip because the space for the bottom chip is limited by the spacer connectors.

258. For example, as discussed above for §X.C.ii, *Sun* having a PoP structure similar to *Chen's* discloses chips 30, 31 (top chips) overlapping each of second substrate 300 (spacer connector) and chip 200 (bottom chip) as shown in FIG. 12 below. EX1005 at [0059] (“The upper module 5 comprises a pair of chips 30, 31 mounted to a first (upper) side of a third substrate 20. ... The chips 30, 31 are electrically connected to the third substrate 20 by wires or any other suitable means.”), FIG. 12:

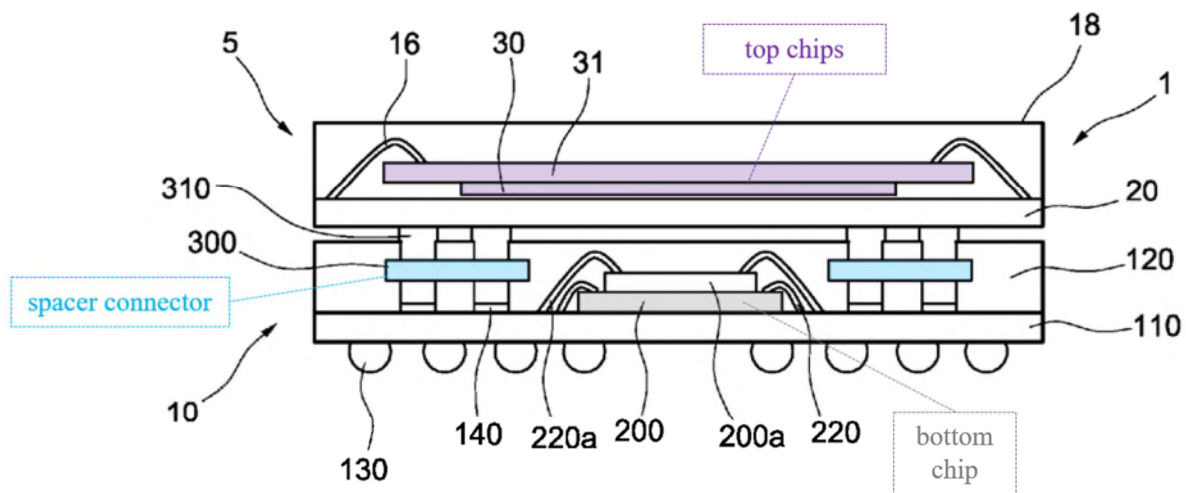


FIG. 12

Accordingly, a POSITA would have found it obvious to accommodate a larger top chip in *Chen*'s PoP, which overlaps the bottom chip and each of the two spacer connectors, to maximize the use of space on the top package substrate.

259. Thus, in my opinion, *Chen* renders obvious each limitation of 3[b].

D. Claim 4

- i. The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate**

260. *Chen* discloses "[t]he structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the

spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.” As discussed above in §XIII.A.xi, (1) (upper) connectors 44 (bottom metal pillars) of package substrate in top package component 62 (top package substrate), (2) through-substrate vias 32 and metal posts 30 (together, metal pillars) of TAV modules 28 (spacer connector), (3) and (lower) connectors 44 (top metal pillars) of package component 56 (bottom package substrate) are used to electrically couple the top and bottom package substrate. EX1006 at [0011] (“[M]etal posts 30 are connected to, and are aligned to, through-substrate vias 32.”), [0014] (“[C]onnectors 44 are formed to connect to metal posts 26 and 30.”), [0019] (top package component 62 including “a package that includes a device die (not shown) bonded to a package substrate (not shown).”), [0021] (“[T]he connection between top package component 62 and bottom package 60 [including package component 56] is through TAV modules 28.”), [0022] (“through-substrate vias 32, which are used for electrically connecting the features on opposite sides of TAV modules 28”), FIG. 9. For the electrical connection, each of (upper) connectors 44 is aligned with a corresponding through-substrate via 32 and metal post 30, and also with a corresponding (lower) connector 44 as shown in FIG. 9 (indicated in a dashed red line).

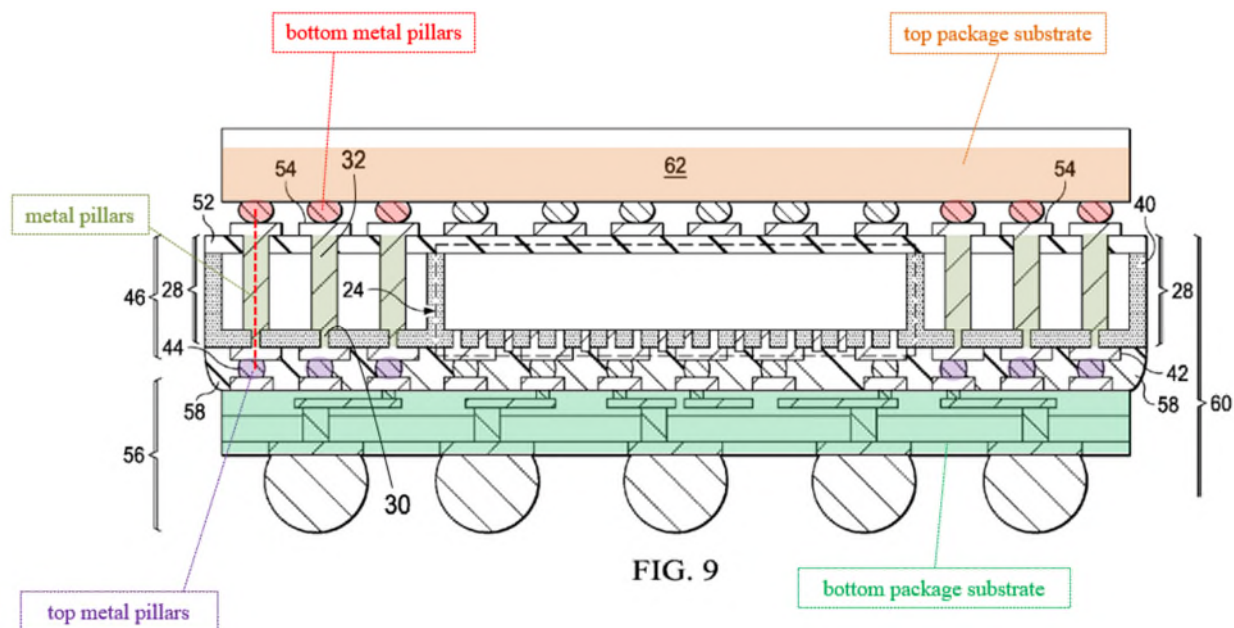


FIG. 9

EX1006 at FIG. 9.

261. Thus, in my opinion, *Chen* discloses each limitation of claim 4.

E. Claim 5

- i. **5[a]–[b]: The structure of claim 4, wherein the spacer connector is free of metal pads on the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate, and each metal pillar among the plurality of metal pillars and the corresponding top metal pad of the spacer connector form a T shape**

262. *Chen* discloses and/or renders obvious “[t]he structure of claim 4, wherein the spacer connector is free of metal pads on the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate, and each metal pillar among the plurality of metal pillars and the corresponding top metal pad of the spacer connector form a T shape.” *Chen* discloses [TAV modules 28](#) (spacer connector) may **not** have a metal pad on the

bottom ends of through-substrate vias 32 and metal posts 30 (together, metal pillars), which protrude downwardly from the bottom surface of substrate 34 (core substrate). Specifically, *Chen* teaches “[a]lternatively, no redistribution layer is formed on either side of one or each of TAV modules 28,” EX1006 at [0011]. This means TAV modules 28 may omit “Redistribution Lines (RDLs) 42” on their bottom side (i.e., on the bottom ends of metal posts 30) as the claim requires.

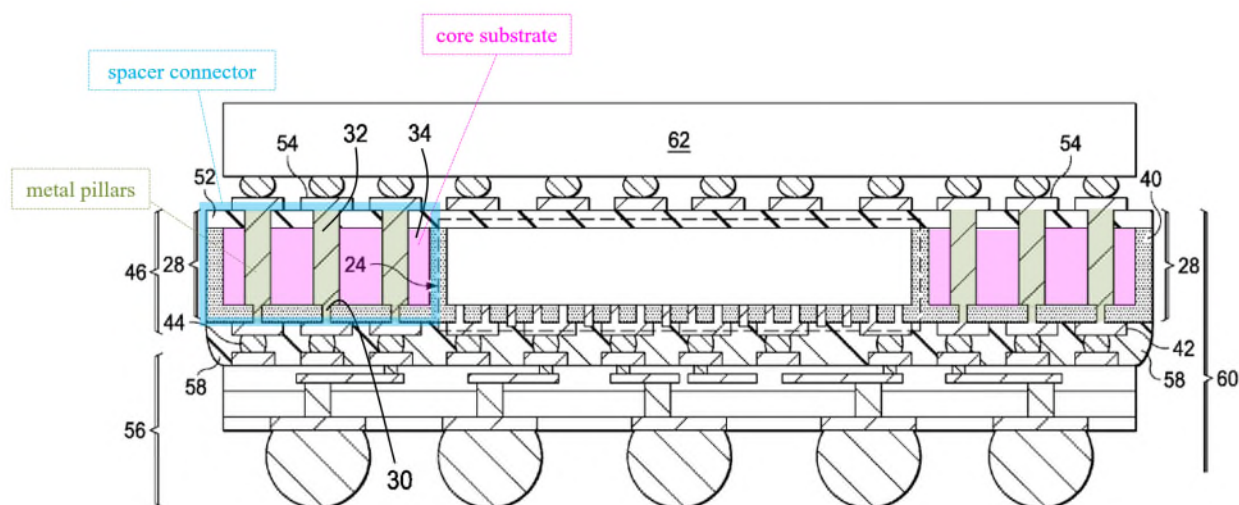


FIG. 9

EX1006 at FIG. 9. When TAV modules 28 do not have RDLs 42 on their bottom side and on the bottom side of metal posts 30, through-substrate vias 32 and metal posts 30 (together, metal pillars) and the corresponding RDLs 54 (top metal pads) of TAV modules 28 (spacer connector) “form a T shape.” Accordingly, *Chen* anticipates claim 5.

263. If the Board finds *Chen* does not expressly teach the absence of metal pads on the bottom ends of the plurality of metal pillars, a POSITA would have

found this limitation obvious because *Chen* provides excluding RDLs 42 as one of finite design options. EX1006 at [0011] (“Alternatively, no redistribution layer is formed on either side of one or each of TAV modules 28.”). Furthermore, it was well known in the art that two sets of metal pillars (e.g., *Chen*’s metal posts 30 and top connectors 44, which “may also include metal pillars,” EX1006 at [0014]) can be directly bonded together without using an intermediate metal pad. Given that forming metal pads require additional process steps, such as “depositing a metal layer, and then patterning the metal layer,” *id.*, removing metal pads while connecting two metal pillars would minimize process steps and reduce assembly costs, for devices where the alignment precision is less stringent. *See, e.g.*, EX1008 at FIG. 3 (below showing two sets of metal pillars 300 and 27 are directly bonded without a metal pad). Accordingly, a POSITA would have found it obvious that metal posts 30 and top connectors 44 (both of which are metal pillars) may also be directly connected without using RDLs 42 between them.

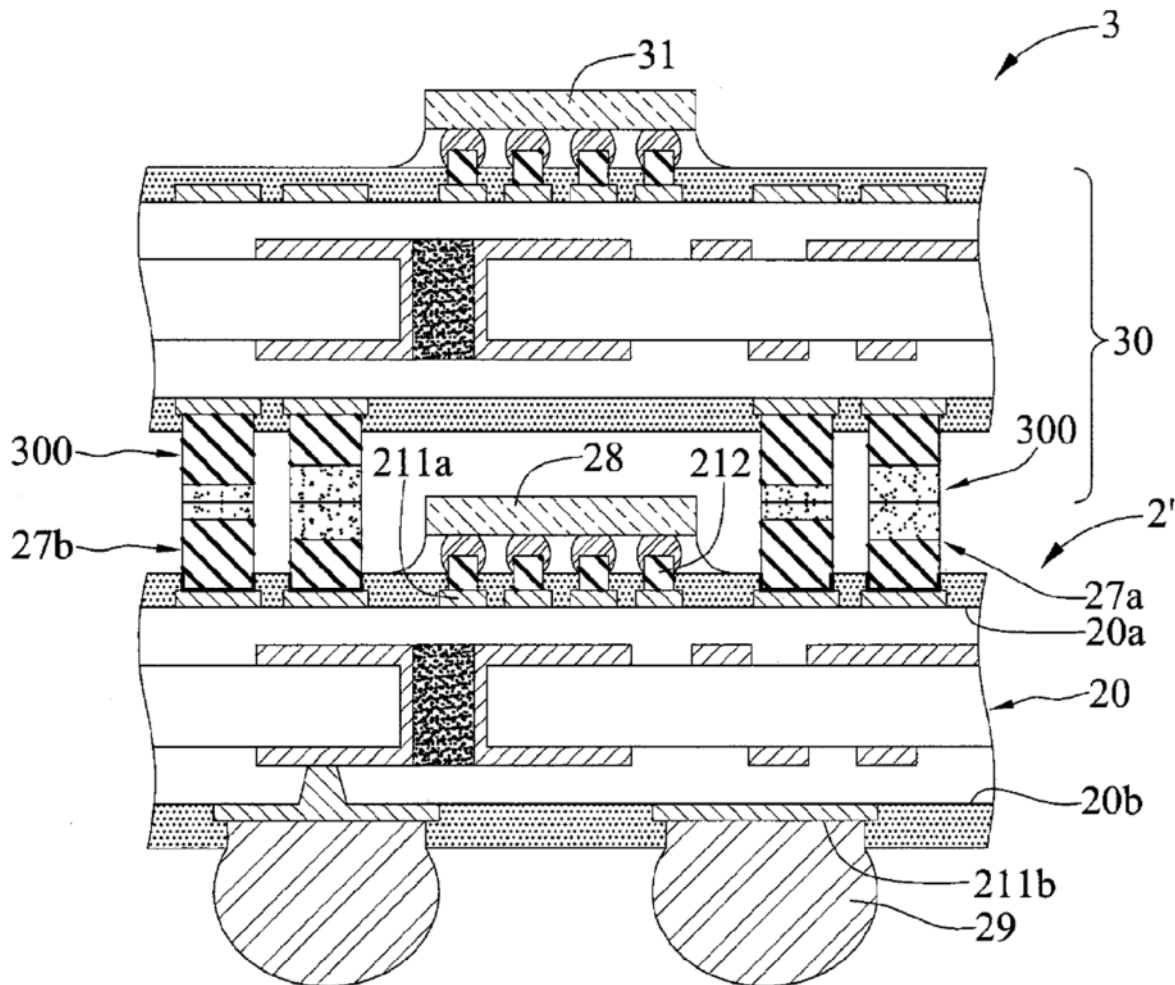


FIG.3

EX1008 at FIG. 3.

264. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of claim 5.

F. Claim 6

- i. **6[a]: The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector**

are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate

265. *Chen* discloses and/or renders obvious “[t]he structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate.” As discussed in §XIII.A.viii, *Chen* discloses a bottom end of each of through-substrate vias 32 and metal posts 30 (metal pillars) protrudes downwardly from a bottom surface of substrate 34 (core substrate). As shown in FIG. 9 below and as discussed above for §XIII.A.x, through-substrate vias 32 and metal posts 30 (together, metal pillars) are directly stacked on (lower) connectors 44 (top metal pillars) to form a conductive path through package component 56 (bottom package substrate). EX1006 at [0014], FIGs. 8–9.

266. Accordingly, the bottom ends of through-substrate vias 32 and metal posts 30 are connected, in “an end-to-end manner,” to corresponding top ends of top connectors 44. Although RDLs 42 are present between these metal pillars, they merely function as an intermediate routing feature that facilitates electrical continuity and simply provides a conductive bridge allowing the electrical signal to pass from the end of one metal pillar to the end of another. See §V.B (The Examiner found and the Applicant did not dispute that *Arai*’s metal pillars and top metal pillars

are connected “in an end-to-end manner,” when the two sets of metal pillars are connected via 20a, which the Examiner mapped to bottom metal pads.).

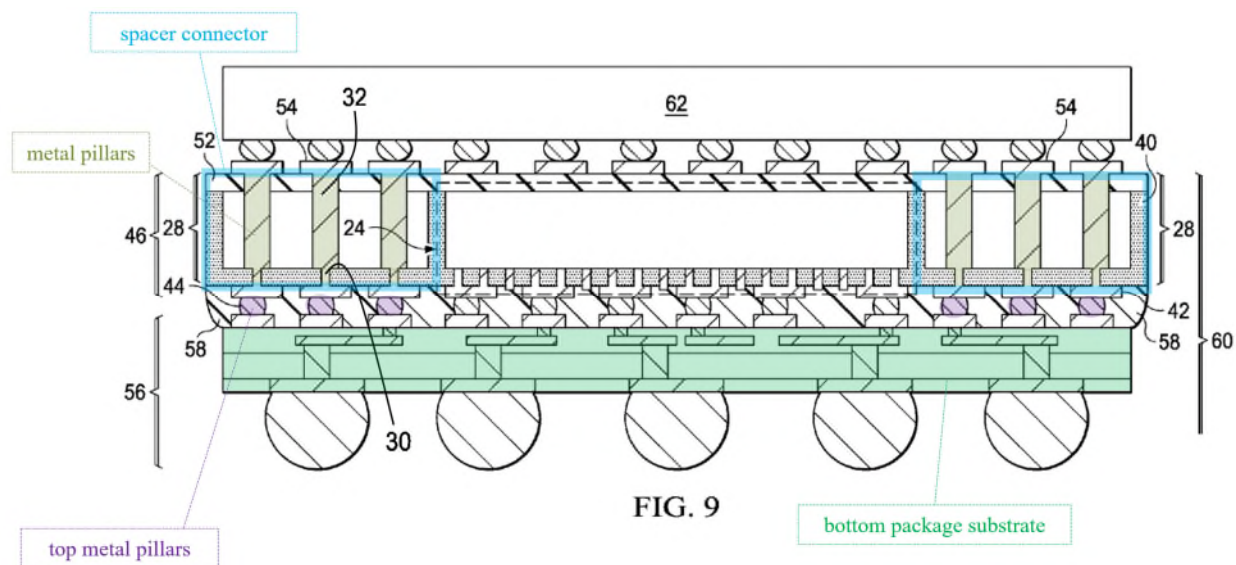


FIG. 9

EX1006 at FIG. 9.

267. If, however, the Board finds that “an end-to-end manner” requires direct connection between the bottom ends of metal pillars and the corresponding top ends of the top metal pillars, *Chen* still discloses and/or renders this limitation obvious. As discussed above for §XIII.E, *Chen* teaches RDLs 42 may be omitted, resulting in two metal pillars (i.e., metal posts 30 and top connectors 44) that are connected in “an end-to-end manner” without intervening metal pads—an alternative and well known approach in the art. EX1006 at [0011]; EX1008 at FIG. 3. In this configuration, the bottom ends of metal posts 30 are directly connected to the top ends of top connectors 44.

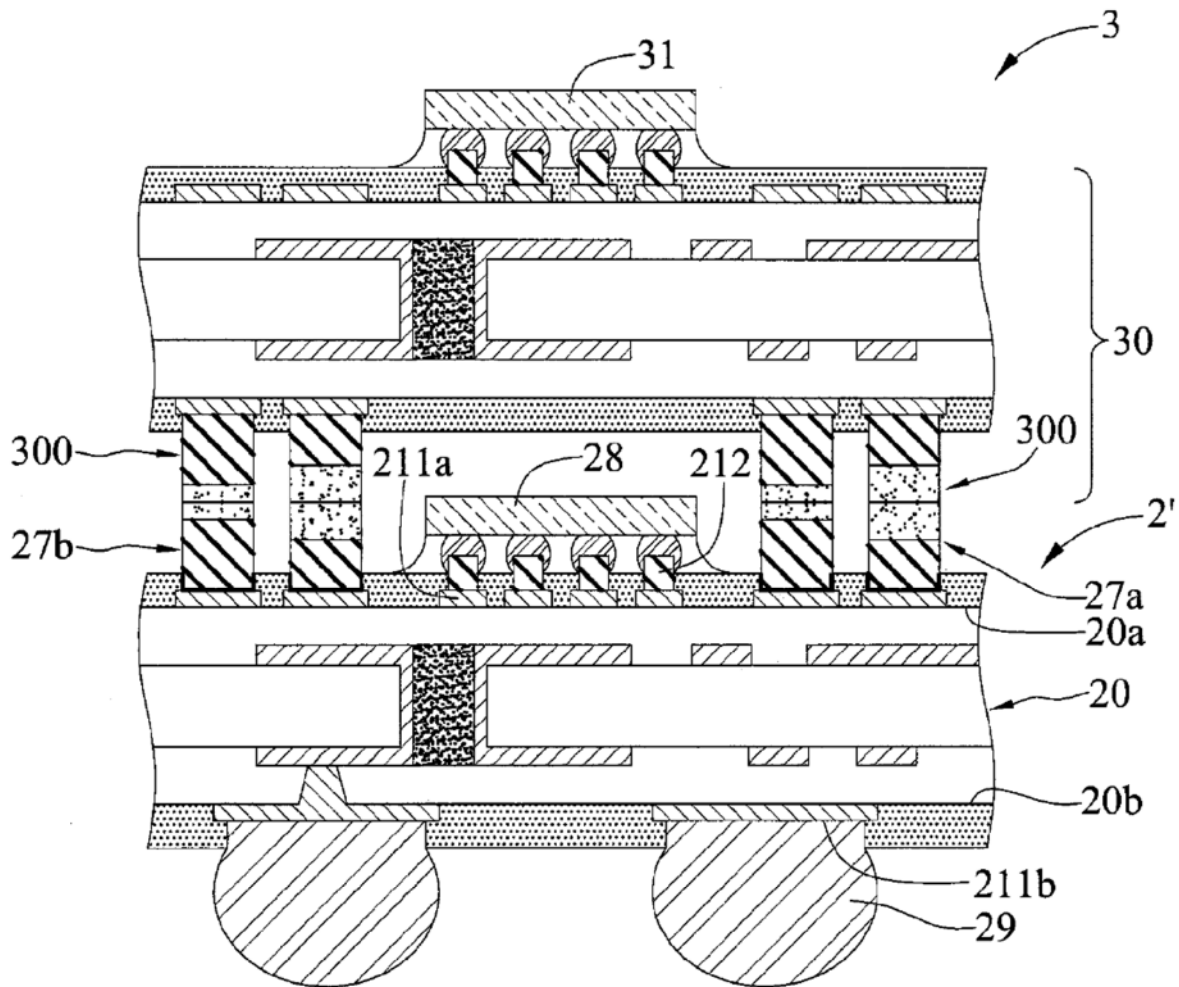


FIG.3

EX1008 at FIG. 3.

268. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of claim 6[a].

- ii. **6[b]: bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer**

connector via the corresponding top metal pads of the spacer connector

269. *Chen* discloses and/or renders obvious “bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.” As discussed above in §XIII.A.vii, ix and as shown in FIG. 9 below, bottom ends of (upper) connectors 44 (bottom metal pillars) of package substrate in top package component 62 (top package substrate) are connected to the corresponding top ends of through-substrate vias 32 and metal posts 30 (together, metal pillars) of TAV modules 28 (space connectors) via the corresponding RDLs 54 (top metal pads). *See also* EX1006 at [0017] (“RDLs 54 are then formed on dielectric layer 52.”), [0018] (“RDLs 54 are exposed through the respective molding compound (not shown).”), FIGs. 7–9 (below):

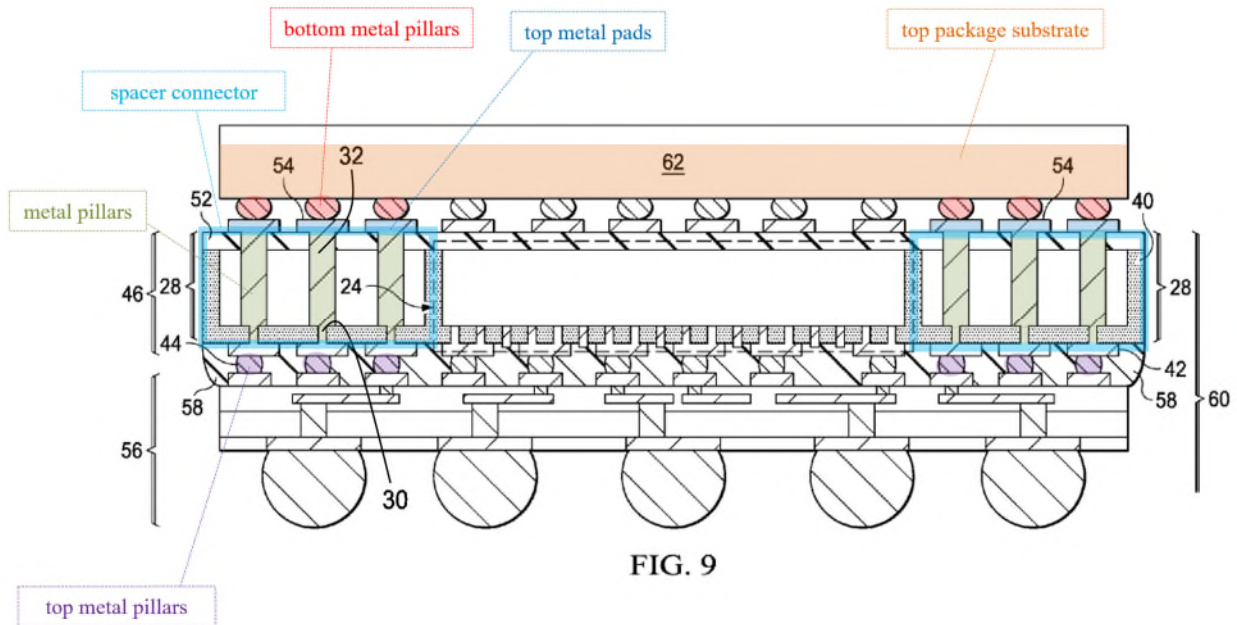


FIG. 9

270. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of 6[b].

G. Claim 7

- i. **7[a]–[b]: The structure of claim 4, wherein the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate, and the plurality of metal pillars pass through the core substrate and the dielectric layer**

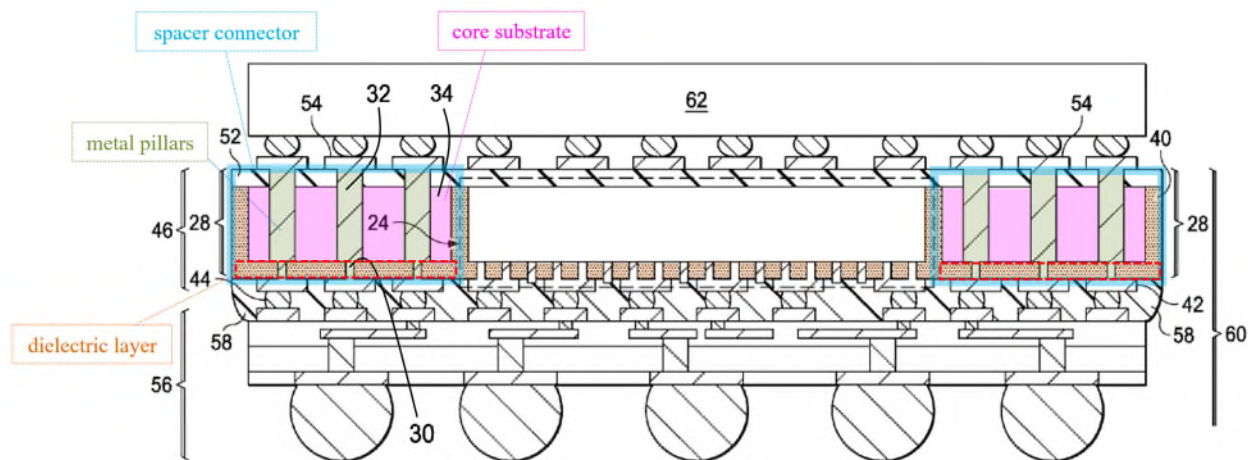
271. *Chen* discloses “[t]he structure of claim 4, wherein the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate, and the plurality of metal pillars pass through the core substrate and the dielectric layer.” *Chen* discloses TAV modules 28 (spacer connector) include polymer 40 (dielectric layer), a layer disposed on the bottom surface of substrate 34 (core substrate) as shown in FIG. 9. EX1006 at FIG. 9. *Chen* explains “polymer 40 is filled ... into the

gaps between metal posts 30,” which protrude below substrate 34 as explained above for §XIII.A.viii. *Id.* at [0013], [0023] (“A polymer includes a first portion between and contacting sidewalls of the first package component and the TAV module, a second portion disposed between the first plurality of metal posts, and a third portion disposed between the second plurality of metal posts.”). In effect, polymer 40 is disposed on the bottom surface of substrate 34 as shown in FIG. 9. *See also, id.* at [0025] (“The polymer is ground to expose ... metal posts [30] of the TAV module.”).

272. *Chen* also teaches polymer 40 is a dielectric layer as consistent with a POSITA’s understanding. *Id.* at [0013] (“Polymer 40 may include a molding compound, a molding underfill, or a kind of epoxy.”), [0017] (“dielectric layer 52 include[ing] a polymer, which may be polyimide, benzocyclobutene (BCB), or the like”), FIG. 3 (showing polymer 40 molded during the fabrication of *Chen*’s PoP). Indeed, given the contact between polymer 40 and metal posts 30, polymer 40 would necessarily be electrically insulating (a dielectric) to prevent shorting between the metal posts.

273. Furthermore, as discussed above for §XIII.A.vi, *Chen*’s metal pillars, including through-substrate vias 32 and metal posts 30, pass through substrate 34 (core substrate) for electrical connections of TAV modules 28. The metal pillars also pass through polymer 40 (dielectric layer), which “fill[s] ... gaps between metal posts 30.” EX1006 at [0013], FIG. 9 (showing metal posts 30 pass through polymer

40 in dashed red line).



274. Thus, in my opinion, *Chen* discloses each limitation of claim 7.

H. Claim 8

i. The structure of claim 7, wherein the dielectric layer is a dielectric adhesive in which the core substrate is pasted

275. *Chen* discloses and/or renders obvious “[t]he structure of claim 7, wherein the dielectric layer is a dielectric adhesive in which the core substrate is pasted.” *Chen*’s polymer 40 (dielectric layer) is a dielectric adhesive where substrate 34 (core substrate) is pasted. *Chen* discloses “[p]olymer 40 may include...a molding *underfill*, or a kind of *epoxy*,” EX1006 at [0013], and the underfill or epoxy is “adhesive” because in “microelectronic packaging” “[p]olymer adhesives are commonly used as underfills” and “[t]he materials used are typically unfilled epoxies.” EX1009 at 1, 3 (“insulating polymer adhesives,” such as “unfilled epoxies”).

276. If the Board, however, finds that *Chen* does not explicitly disclose polymer 40 as a dielectric adhesive, a POSITA would have also found it an obvious design choice. To have polymer 40 disposed or “pasted” underneath core substrate 34, a POSITA would have readily understood that polymer 40 is not only a dielectric layer, but also has adhesive properties. In semiconductor packaging, adhesive insulating polymer materials are widely used not only to fill the gap but also to bond adjacent components together. EX1009 at 1, 3 (“insulating polymer adhesives,” such as “unfilled epoxies”). Thus, a POSITA would have recognized that polymer 40 is intended to adhere to the underside of core substrate 34, thereby securing the components in place without the need for separate bonding materials. Indeed, insulating polymer adhesives are commonly used as underfills in applications like *Chen*’s polymer 40 to provide known benefits including “stress relief.” EX1009 at 3 (“A major application involves the use of adhesives as underfills for flip-chip devices to provide some stress relief of the solder joints during temperature cycling.”), 6 (“These materials fill the gap between the chip and substrate and surround the solder joints, thereby reducing any thermal stress.”), 13 (“the general types of materials used to formulate polymer adhesives for die attachment, underfills, and encapsulants, along with their properties.”).

277. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of claim 8.

I. Claim 9

- i. **9[a]: The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars**

278. *Chen* discloses and/or renders obvious “[t]he structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars.” *Chen* teaches TAV modules 28 (spacer connector) include multiple Redistribution Lines (RDLs) 42 (bottom metal pads), each “formed” on the bottom end of a corresponding through-substrate via 32 and metal post 30 (together, metal pillars). EX1006 at [0014] (“Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts ... 30.”). *Chen* also teaches RDLs 42 including metal pad portions, as shown in FIG. 9. *Id.* at [0014] (“RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer.”), [0011] (“TAV modules 28 may include redistribution layer(s) that include redistribution lines and **metal pads**,” such as RDLs 42.). As explained above, it was well-known in the art that RDLs include both metal lines and metal pads as *Chen* explains, see EX1006 at [0011], and a POSITA would have understood the portions of RDLs 42 shown in FIG. 9 are metal pads for the connectors between substrates. §XIII.A.vii. *Chen*’s RDLs 42 discloses and/or renders obvious metal pads for the same reasons discussed above in §XIII.A.vii. *Id.*

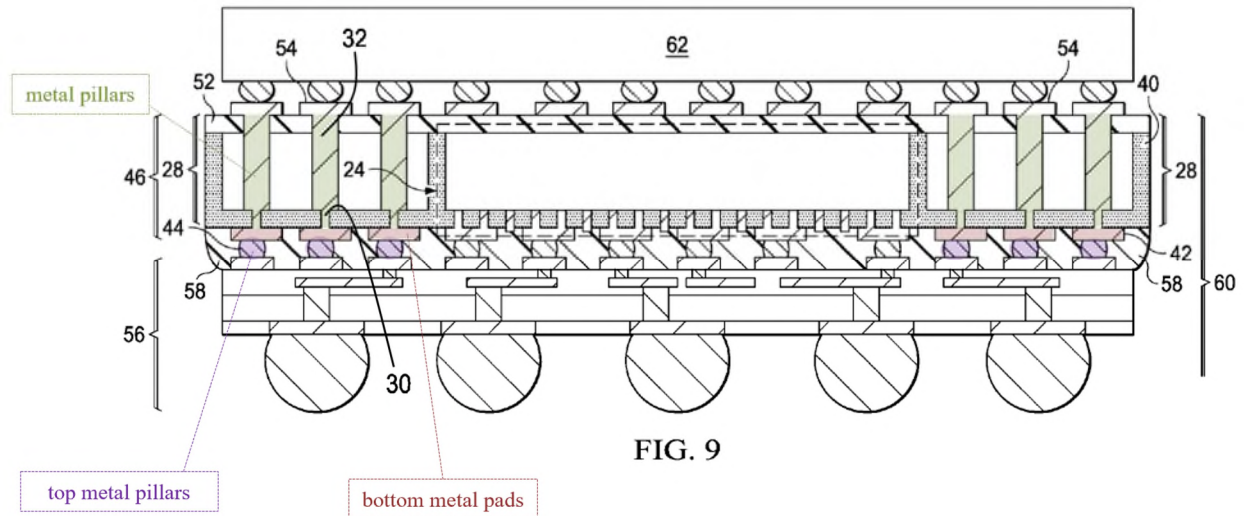


FIG. 9

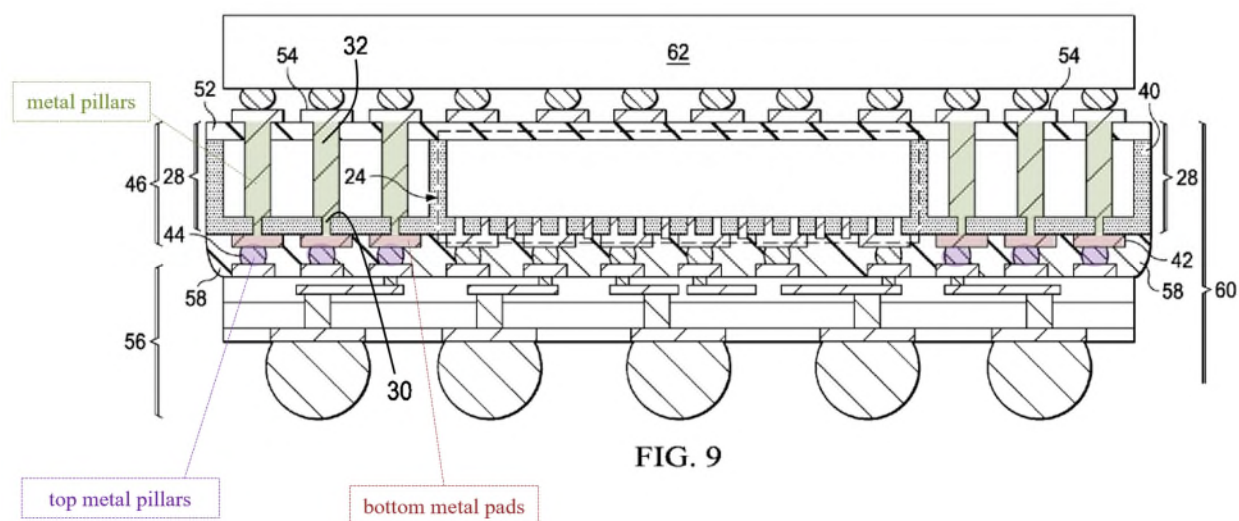
EX1006 at FIG. 9.

279. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of claim 9[a].

- ii. **9[b]: the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector**

280. *Chen* discloses and/or renders obvious “the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector.” As shown in FIG. 9 below, the bottom ends of through-substrate vias 32 and metal posts 30 (together, metal pillars) are connected to corresponding top ends of (lower) connectors 44 (top metal pillars) of package component 56 (bottom package substrate) via the corresponding RDLs 42 (bottom metal pads) of TAV modules 28 (spacer connector). EX1006 at [0014]

(“Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts ... 30.”), [0011] (“[M]etal posts 30 are connected to, and are aligned to, through-substrate vias 32.”).



EX1006 at FIG. 9.

281. Thus, in my opinion, *Chen* discloses and/or renders obvious each limitation of claim 9[b].

iii. 9[c]

282. Limitation 9[c] is identical to limitation 6[b]. Accordingly, *Chen* discloses and/or renders obvious each limitation of 9[c], for the same reasons discussed above, with reference to limitation 6[b]. §XIII.F.ii.

XIV. GROUND 7: *CHEN* WITH *HU* RENDERS OBVIOUS CLAIMS 1–9

283. In my opinion, combination of *Chen* and *Hu* renders obvious claims 1–9.

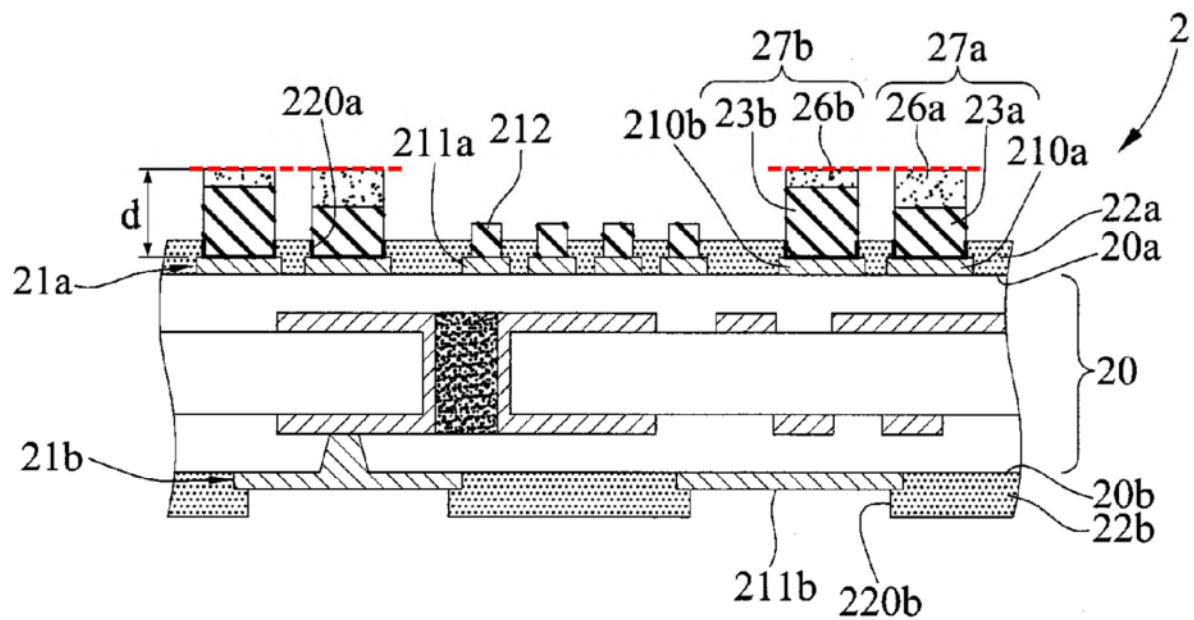
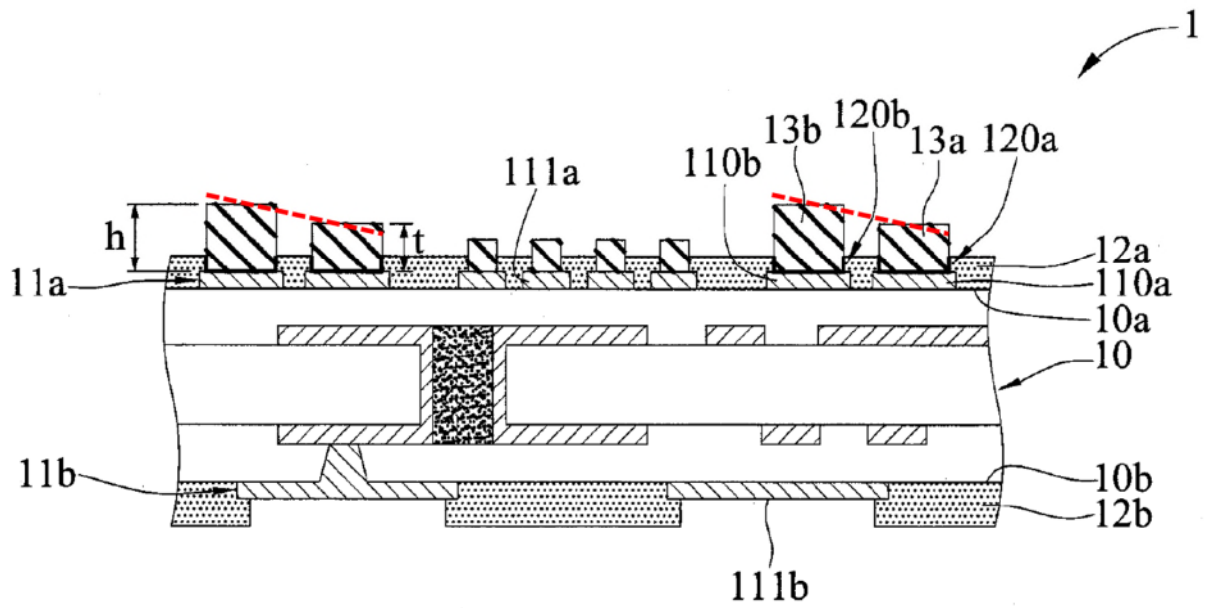
A. Motivation to Combine

284. Both *Chen* and *Hu* are directed to the structure and process of “Package-on-Package (POP),” where “a top package is bonded to a bottom package.” EX1006 at [0001]; EX1008 at [0001] (“The present invention relates to packaging substrates, and more particularly, to a packaging substrate used in a package on package (PoP) structure.”).

285. Each reference identifies shortcomings of using solder balls in PoP structures well-known in the art, such as limited space and coplanarity and reliability issues. For example, *Chen* explains that, in conventional PoP processes, “solder balls are used” to connect package substrates, but “the amount of the solder balls that can be used in a PoP structure is limited” because “the lateral sizes of the solder balls are [] large.” EX1006 at [0002]. *Hu* similarly identifies fundamental drawbacks of solder balls, explaining that “[g]enerally, solder balls are formed between packages to achieve a PoP structure,” but that “it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity, and even causing positional deviation of solder joints between the packages.” EX1008 at [0004]. *Hu* further explains that a large “diameter of the solder balls” requires “more space ... leaving less available space for circuits and electronic elements and adversely affecting continuous reduction of pitches between PoP pads.” *Id.* Also, “an increase in the volume of the solder balls

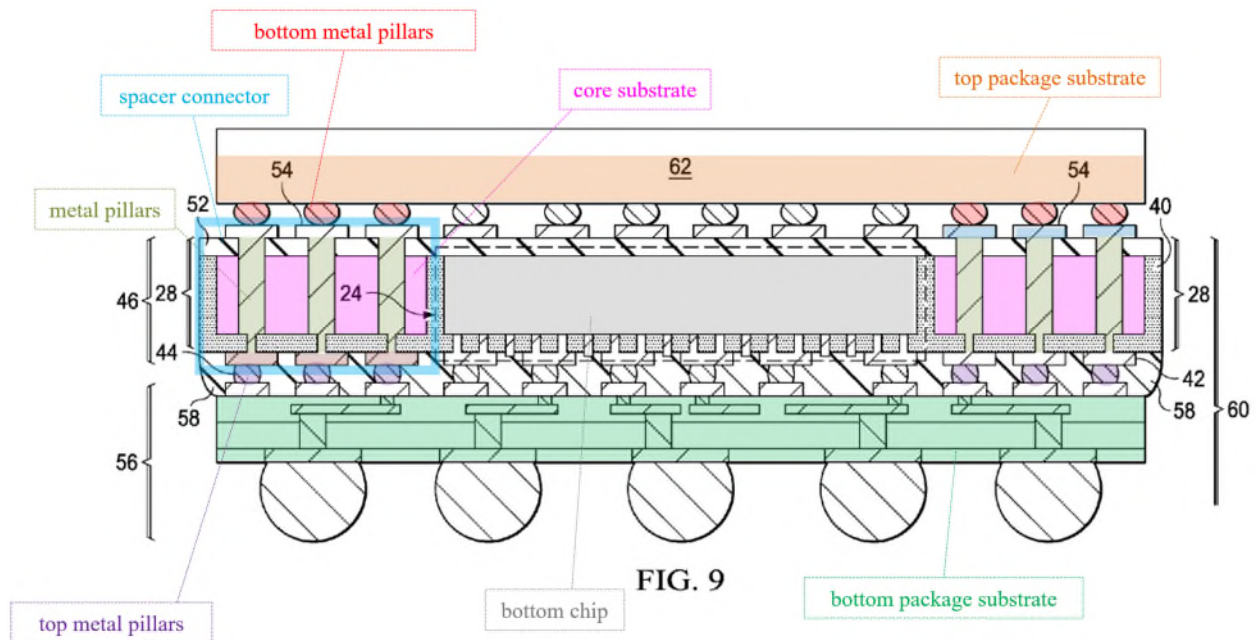
can easily cause a solder bridge between the solder balls.” *Id.*

286. *Hu* then expressly teaches “metal posts ... are used in stack structures so as to overcome the above-described drawbacks” of solder balls. EX1008 at [0005], [0007] (“Since ... metal posts ... are not likely to deform during a reflow process, the above-described drawbacks can be overcome.”). While acknowledging that “it is not easy to control the uniformity of the height of the metal posts” because “the metal posts are formed by electroplating,” EX1008 [0008] at FIG. 1 (below, dashed red lines), *Hu* provides a detailed solution to the uniformity problem. For example, *Hu* teaches placing “conductive bonding layers” 26a-b on initially formed metal posts 23a-b, so that the resulting metal posts 27a-b have the same “height,” *id.* at [0030], FIG. 2E (below, dashed red lines), and teaches specific process-level details for implementing such uniform metal posts on a package substrate, *id.* at [0028]–[0035], FIGs. 2C–2F. *See also id.* at [0013] (“According to the present invention, the conductive posts together with the conductive bonding layer formed thereon form a plurality of external connection structures with the same height.”).



EX1008 at FIGs. 1, 2E.

287. As discussed above in §XIII.A.i, *Chen* teaches a PoP structure that includes top package component 62, package component 56, and “Through-Assembly Via (TAV) Module [28].” EX1006 at Abstract, [0010] (“TAV modules 28 include substrate 34, which may be a semiconductor substrate such as a silicon substrate.”), [0019] (“In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.”), FIG. 9 (below). Each of top package component 62 and package component 56 includes “a package substrate.” *Id.* at [0019], [0018] (“Package component 56 may be a package substrate.”). TAV Module 28 further includes “a substrate [and] a plurality of through-vias penetrating through the substrate,” *id.* at Abstract, and is electrically coupled to top package component 62 and package component 56 via connectors 44, *id.* at [0019], FIGs. 4, 9. With respect to connectors 44, *Chen* teaches the use of “metal pillars” as alternatives to solder balls, although it does not provide the same level of fabrication detail as *Hu*. For example, *Chen* explains that connectors 44 may be “solder balls,” but they alternatively “include metal pillars, or metal pillars and solder caps, which may also be formed through plating.” *Id.* at [0014].



EX1006 at FIG. 9.

288. Given these disclosures, a POSITA would have been motivated to look to *Hu* for guidance on how to implement *Chen*’s interconnects as metal pillars (posts) in a practical and reliable manner. As explained above, *Hu* not only teaches the use of metal pillars in PoP structures but also addresses the fabrication challenge—controlling height uniformity—that a POSITA would reasonably anticipate when forming “metal pillars ... formed through plating” process as taught by *Chen*. EX1006 at [0014]; EX1008 at [0008] (“metal posts [] formed by electroplating”). Applying *Hu*’s detailed metal-pillar implementation to *Chen*’s interconnectors, such as connectors 44, to provide uniform metal pillars would therefore have been a logical and predictable design choice, “preventing tilt of the packaging substrate [] during a subsequent stacking process, improving the coplanarity and consequently

effectively improving the product reliability.” EX1008 at [0038].

289. Specifically, a POSITA would have implemented *Hu*’s metal pillars on each of *Chen*’s top (within top package component 62) and bottom package substrate (package component 56) before connecting them with TAV modules 28. As explained above and shown in FIG. 3 below, *Hu* teaches forming uniform metal pillars (300) on a package substrate, EX1008 at [0028]–[0035] (describing detailed steps of forming uniform metal pillars on a package substrate), FIGs. 2C–2F, and placing the package substrate on another one in a way that the uniform metal pillars (300) contact with other metal pillars below (27), EX1008 at [0037].

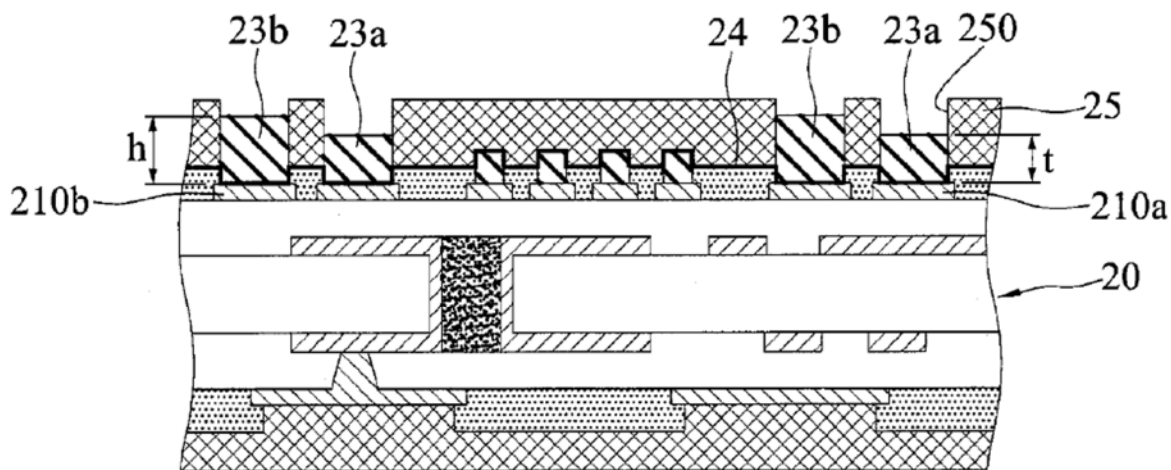


FIG.2C

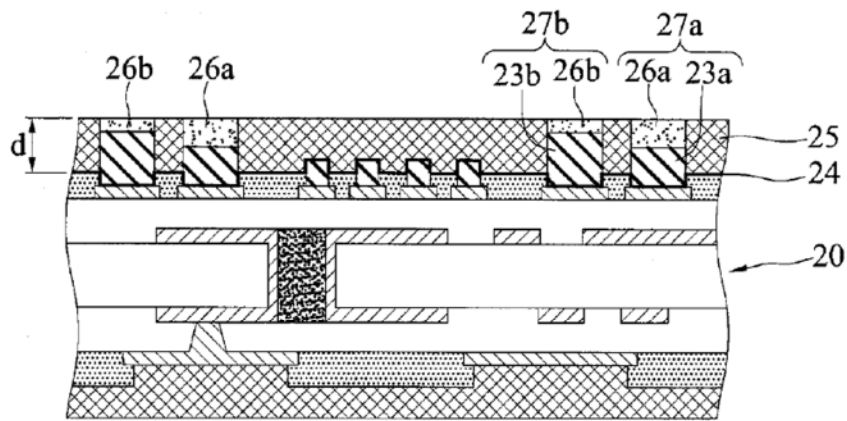


FIG. 2D

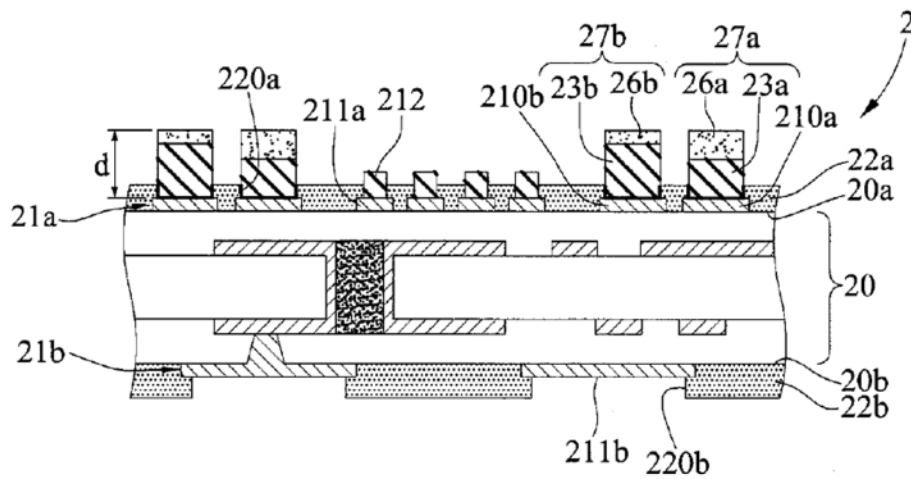


FIG. 2E

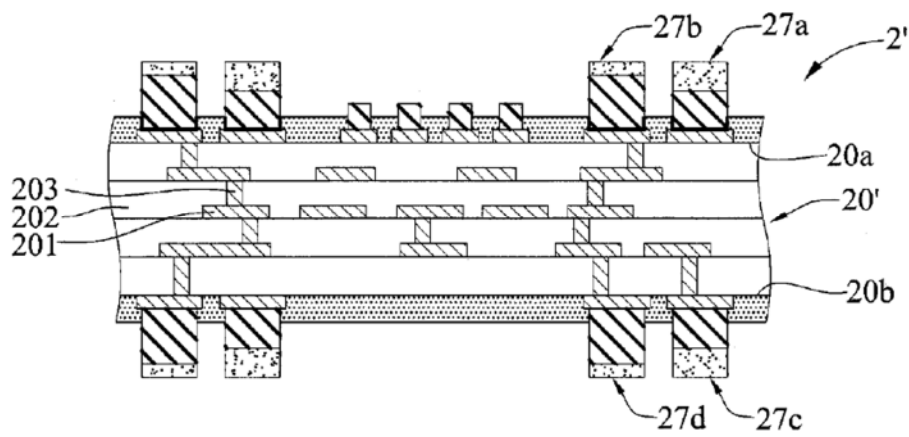
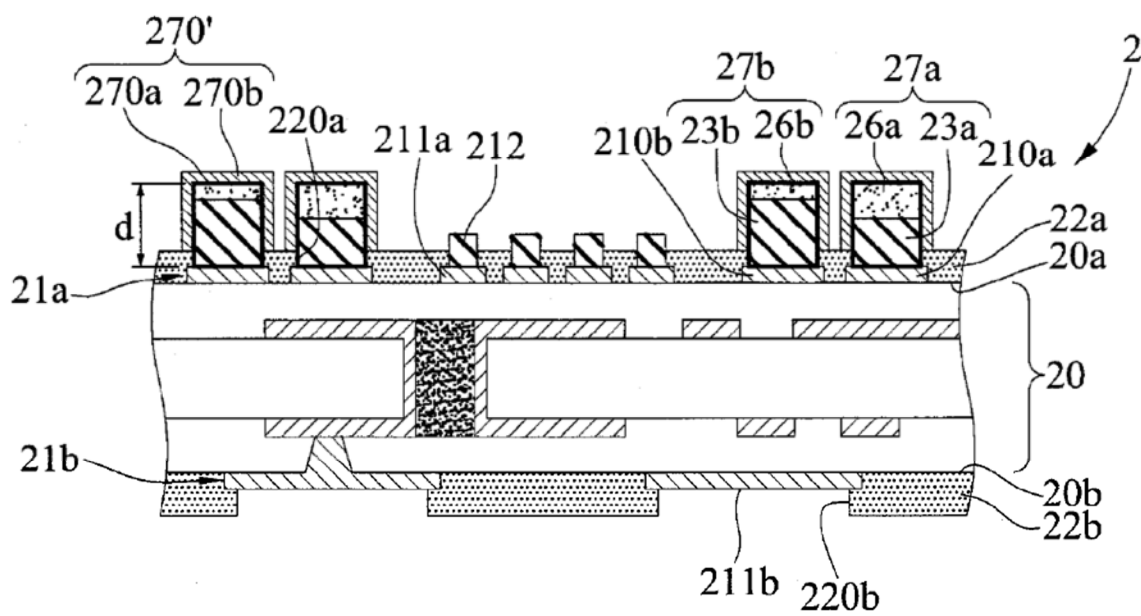
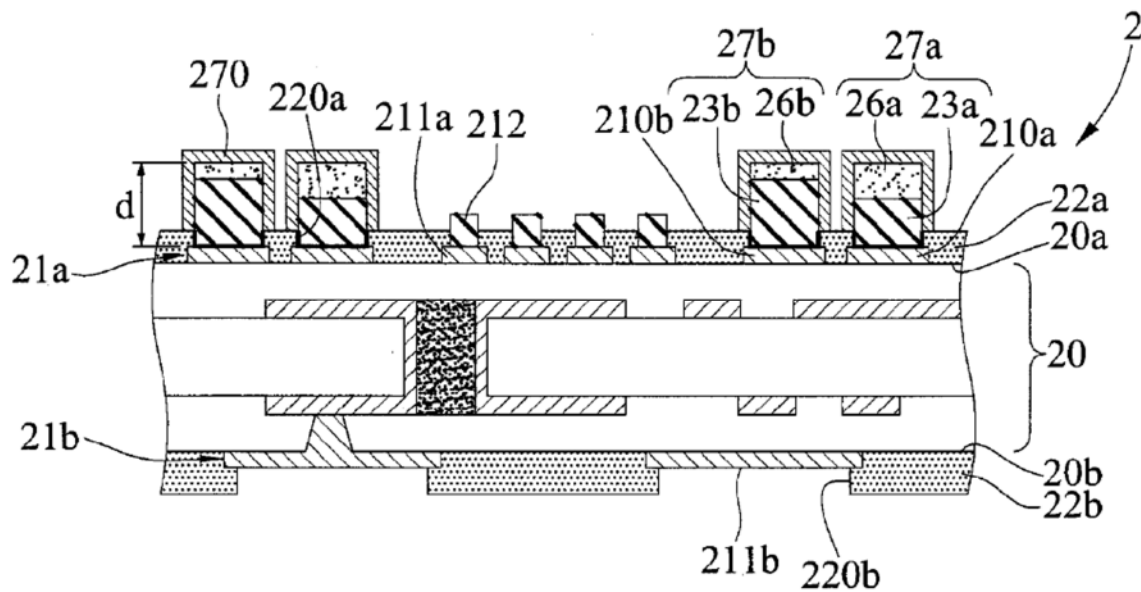


FIG. 2E'



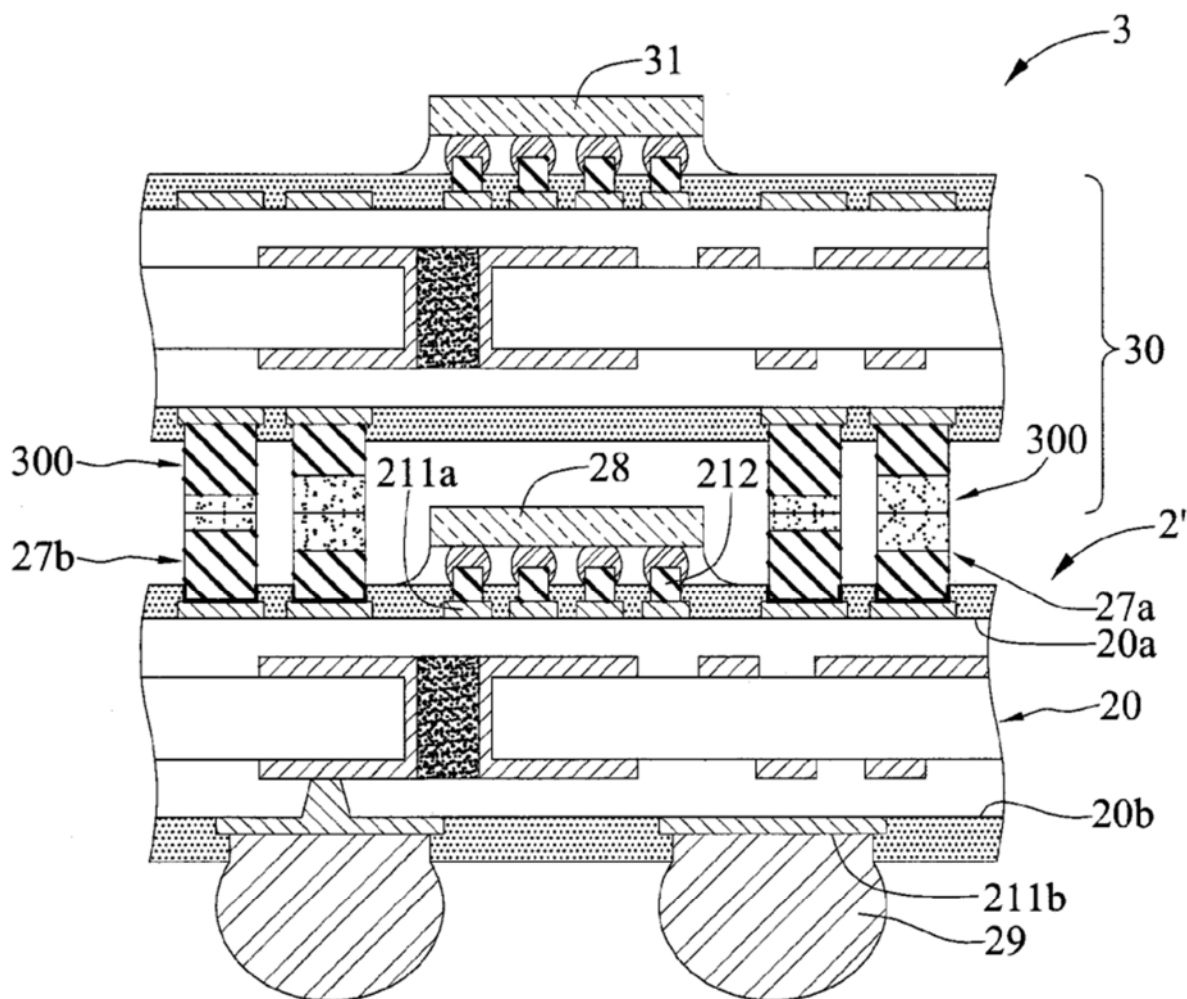


FIG.3

EX1008 at FIGs. 2C–F, 3.

290. Thus, a POSITA would have recognized that *Hu's* (upper) metal pillars (annotated FIG. 9 below) could be grown on the bottom-side of *Chen's* top package substrate (in package component 62), which is then placed on TAV modules 28 in a way that the (upper) metal pillars contact with through-substrate vias 32 (other metal

pillars below) through RDLs 54 as illustrated in FIG. 9 below. Similarly, *Hu's* (lower) metal pillars could be grown on the top-side of *Chen's* bottom package substrate (package component 56) before the metal pillars are bonded with metal posts 30 in TAV modules.

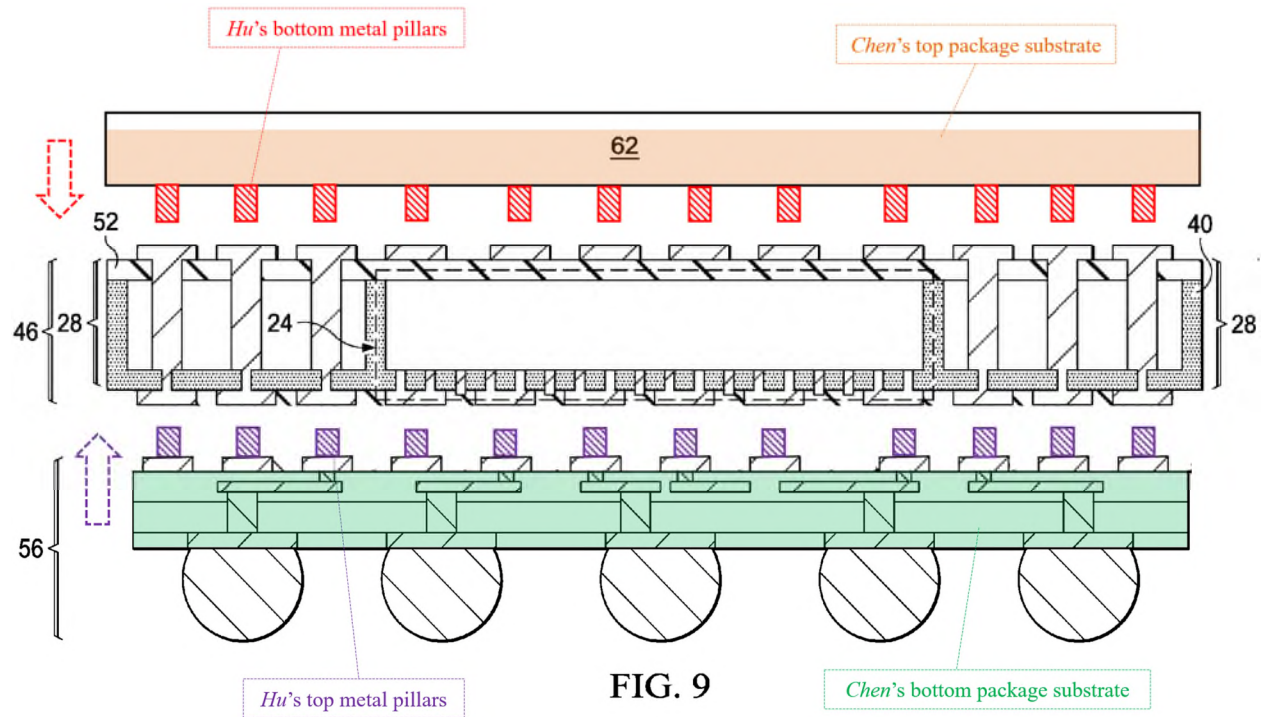


FIG. 9

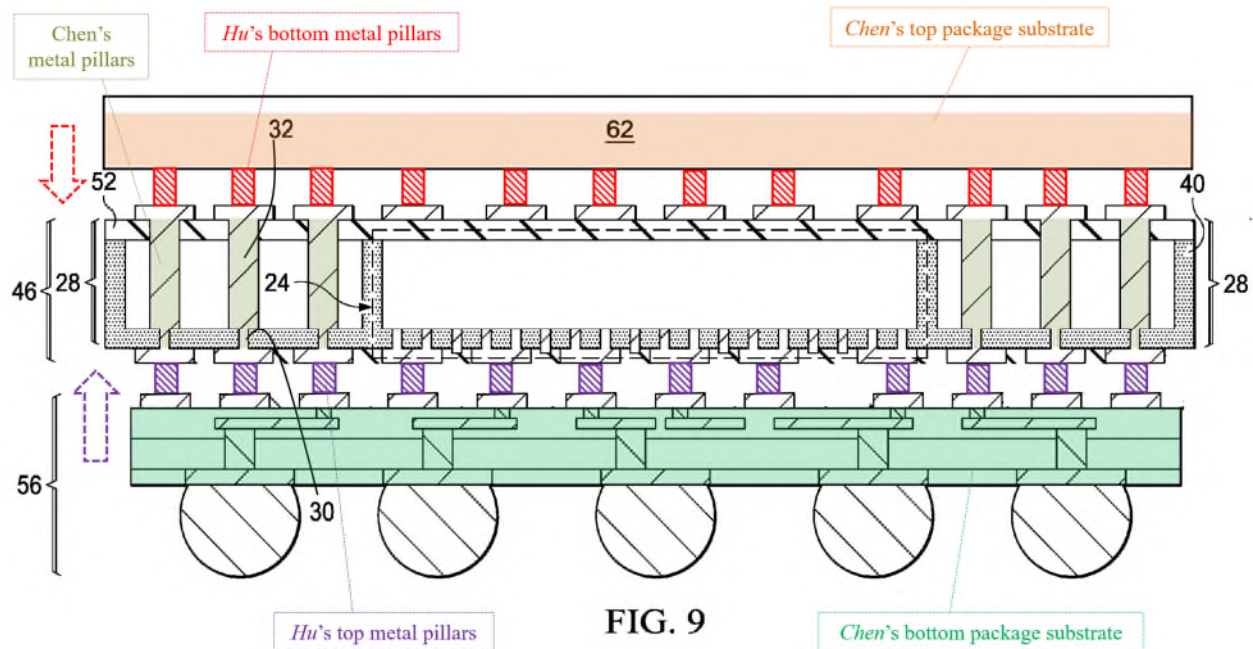


FIG. 9

EX1006 at FIG. 9 (modified to illustrate the *Chen-Hu* device)

291. This way, *Chen-Hu* PoP avoids “tilted stack structure and poor coplanarity” caused by solder balls, EX1008 at [0004], and the metal pillars can be adjusted using conductive bonding layers to achieve good coplanarity as taught by *Hu*. EX1008 at [0008] (“[S]ince the metal posts are formed by electroplating, it is not easy to control the uniformity of the height of the metal posts.”), [0029] (“In an embodiment, the first and second conductive posts 23a, 23b are metal posts such as copper posts.”), [0030] (“The height d of the first external connection structures 27a is equal to the height d of the second external connection structures 27b.”). This approach would also have saved overall process time by removing metal plating steps for TAV modules 28, which are separately fabricated and “pre-formed” before being assembled with other components. EX1006 at [0010]. Instead, the metal

pillars could be fabricated in parallel during the manufacture of top and bottom package substrates.

292. Finally, a POSITA would have had a reasonable expectation of success in making the proposed combinations. *Chen* already teaches forming “metal pillars ... through plating” for connectors 44. EX1006 at [0014]. Further to that teaching, *Hu* provides detailed, working examples of metal pillars formed by the same “electroplating process” and used as PoP interconnections, along with solutions for achieving uniform height and improved coplanarity. EX1008 [0028]–[0035], FIGs. 2C–2F. The combination therefore involves nothing more than applying known elements (metal pillars) in a known structure (PoP) using known methods (electroplating) to achieve their well-understood and predictable function (providing reliable electrical and mechanical connections). This is the type of combination that a POSITA would reasonably expect to succeed without undue experimentation, as it relies on established semiconductor packaging techniques and addresses known, well-documented problems with solder-ball-based PoP connectors.

B. Claims 1–9

293. As discussed above, the *Chen-Hu* design does not materially alter the final package structure of *Chen*. §XIV.A. *Chen-Hu* merely implements *Chen*’s connectors with *Hu*’s metal pillars with the processing steps taught by *Hu*, by first forming the bottom metal pillars and the top metal pillars on the top and bottom

package substrates, respectively, prior to joining the two substrates with the spacer connectors to avoid tilted package stack. §XIV.A. Accordingly, *Chen-Hu* renders obvious “bottom” and “top metal pillars” the reasons discussed in §§XIII.A.ix-x(1[h]–[i]), XIV.A. and thus renders obvious claims 1–9 for the same reasons discussed above in Grounds 5–6.

294. If the terms “bottom metal pillars of the top package substrate” and “top metal pillars of the bottom package substrate” require that the bottom metal pillars be built as part of the top package and the top metal pillars as part of the bottom package prior to assembling the PoP assembly, *Chen-Hu* suggests to a POSITA this process. Accordingly, in my opinion, *Chen-Hu* renders obvious claims 1–9 for the same reasons discussed above, with reference to Grounds 5–6, even under this narrow construction, because the structural design of *Chen-Hu* is materially identical to *Chen*. §XIII.

XV. GROUND 8: CHEN WITH HU AND BENSON RENDERS OBVIOUS CLAIM 8

295. In my opinion, combination of *Chen*, *Hu*, and *Benson* renders obvious claim 8.

A. Motivation to Combine

296. As explained in §XIV.A, a POSITA would have been motivated to combine *Chen* and *Hu* to use *Hu*’s metal pillars for *Chen*’s connectors 44 in order to achieve good coplanarity and avoid tilted structure. Accordingly, other than the

structure of connectors 44, *Chen-Hu's* PoP is identical to *Chen's* PoP structure, including using “polymer 40” as “underfill.” EX1006 at [0013].

297. In my opinion, a POSITA would have been motivated to implement **polymer 40** (dielectric layer) as “adhesives” in *Chen-Hu's* PoP structure in view of *Benson's* teaching about “the use of polymer adhesives in microelectronic packaging.” EX1009 at 1; *see also id.* (“Polymer adhesives are commonly used as underfills.”)

298. *Chen-Hu* teaches a PoP structure where “polymer 40 is filled into the gaps between metal posts 26, and into the gaps between **metal posts 30** [part of metal pillars]” and specifically provides “[p]olymer 40 may include a molding compound, a molding **underfill**, or a kind of **epoxy**.” EX1006 at [0013].

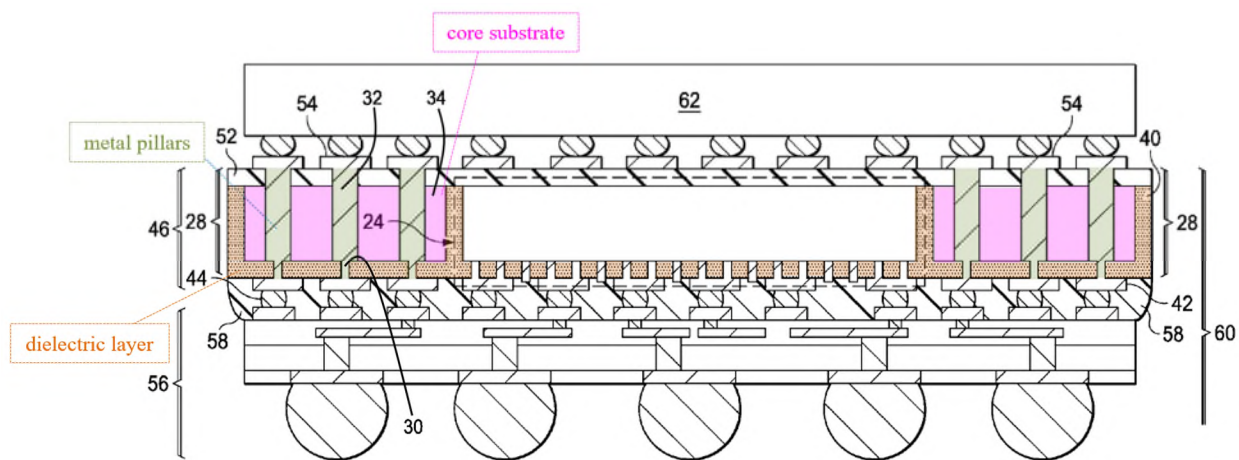


FIG. 9

EX1006 at FIG. 9.

299. Meanwhile, *Benson* teaches, in “microelectronic packaging,” like *Chen-Hu's* PoP, “[p]olymer adhesives have been widely used.” EX1009 at 1. *Benson*

also discloses “the general types of materials used to formulate polymer adhesives for die attachment, underfills, and encapsulants, along with their properties.” EX1009 at 13. Moreover, *Benson* teaches “[p]olymer adhesives are commonly used as **underfills** in larger eutectic-bonded flip-chip devices in order to distribute stress in the solder/eutectic joints that occurs during temperature cycling and results from coefficient of thermal expansion (CTE) mismatches at interfaces.” *Id.*; see also EX1006 at [0013] (“Polymer 40 may include ... a molding **underfill**.”). The same benefits of stress distribution and relief are expected in applying the adhesive underfill to the *Chen-Hu* device, which includes various materials with different CTEs. *Benson* further teaches that “[w]hen thermal or electrical conductivity is not required [like Chen’s polymer 40], insulating polymer adhesives are used for bonding ... semiconductor die to substrates” and that “[t]he materials used are typically unfilled **epoxies**.” *Id.* at 60, see also EX1006 at [0013] (“Polymer 40 may include ... a kind of **epoxy**.”). This further confirms the applicability of polymer adhesives, such as epoxy, as polymer 40 of the *Chen-Hu* device. *Benson* also provides extensive technical details about “polymer adhesives” used as “underfills,” including their various types (e.g., “capillary flow underfills” and “no-flow underfills”), processing conditions, and relative advantages and disadvantages. See, *id.* at 63 (“Capillary Flow Underfills”), 64 (“No-Flow Underfills,” “Disadvantages/Limitations of Underfill Materials”).

300. Based on these disclosures, a POSITA would have been motivated to implement polymer 40 in *Chen-Hu's* PoP structure with *Benson's* “polymer adhesives,” especially given *Chen's* express teaching of “a molding underfill” as an example of polymer 40, EX1006 at [0013], and *Benson's* technical details of “polymer adhesives ... commonly used as underfills,” EX1009 at 1, as discussed above. Further, *Benson* teaches “unfilled epoxies” are typically used for “insulating polymer adhesives,” which bond “substrates,” *id.* at 3, while *Chen* provides “a kind of epoxy” as another example of his polymer 40, which also serves as an insulating layer attached to substrate 34 (core substrate). Moreover, *Benson's* description of “polymer adhesives” used to “fill the gap” and “surround” metal interconnectors, such as “solder joints,” EX1009 at 6, is very similar to how *Chen's* polymer 40 “is filled into the gaps between ... metal posts 30,” EX1006 at [0013]. Accordingly, a POSITA would have applied *Benson's* teaching of “polymer adhesives,” when forming polymer 40 in *Chen-Hu's* PoP to be pasted to substrate 34 and “filled into” the metal post gaps. A POSITA would have been further motivated to do so in light of “an advantage [of Ben's polymer adhesives]” involving “lower temperature processing (typically <150°C), lower cost, and lower stress (attributable to lower rigidity).” EX1009 at 1.

301. In addition, a POSITA would have had a reasonable expectation of success in this implementation. The proposed modification involves nothing more

than applying known materials of “insulating polymer adhesives,” such as “unfilled epoxies,” EX1009 at 3; EX1006 at [0013] (“underfill” or “epoxy”), in a known PoP structure, like *Chen-Hu*’s PoP. These adhesive materials were widely used in semiconductor packaging to achieve the predictable functions of mechanically attaching substrates and filling gaps between metal components to stabilize the assembly. Because the use of epoxy-based underfill materials to secure components and to fill the gap between conductive elements was well understood in the art, a POSITA would have reasonably expected that incorporating such materials into the *Chen-Hu* structure would function as intended without undue experimentation. Moreover, as explained above, *Benson* provides detailed guidance on materials and implementations of “polymer adhesives” used for “underfills,” EX1009 at 6–7, as taught by *Chen*, EX1006 at [0013] (“Polymer 40 may include a molding compound, a molding underfill, or a kind of epoxy.”), further confirming the expectation of success.

B. Claim 8

i. The structure of claim 7, wherein the dielectric layer is a dielectric adhesive in which the core substrate is pasted

302. As discussed above §XV.A, *Benson* combined with *Chen-Hu* PoP structure renders obvious that polymer 40 (dielectric layer) is a dielectric adhesive where substrate 34 (core substrate) is pasted.

303. Thus, in my opinion, the combination of *Chen*, *Hu*, and *Benson* renders

obvious each limitation of claim 8.

XVI. GROUND 9: WAITE AND IPC-4761 RENDERS OBVIOUS CLAIMS 1–2, 4, 6, AND 9.

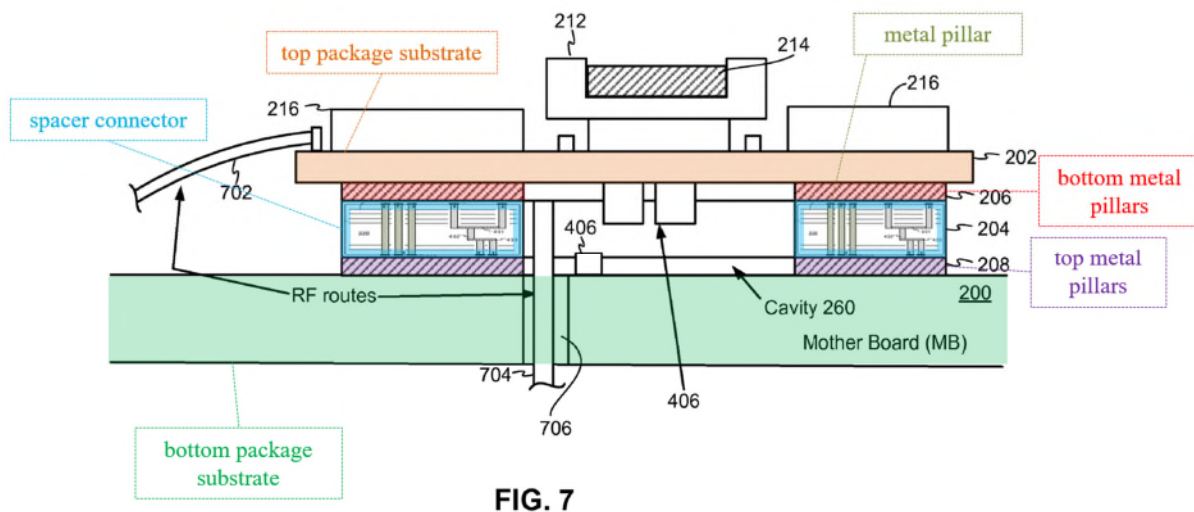
304. In my opinion, the combination of *Waite* and *IPC-4761* renders obvious claims 1–2, 4, 6, and 9, according to PO’s apparent claim interpretation. See §VII.B.

A. Motivation to Combine

305. Both *Waite* and *IPC-4761* are directed to printed circuit board assemblies. For example, *Waite* is related to “spacer/connector interfaces between daughter boards connected to printed circuit boards and test equipment interfaces.” EX1010 at 1:16–18, 4:19–26, 10:3–5, 4:18–4:61. Similarly, *ICP-4761* is a “guideline,” which “provides PWB designers, fabricators, and/or users with information on existing methods for the protection of vias on printed boards.” EX1011 at 7. The term “PWB” is well-known in the electronics industry to refer to “printed wiring board.” In the semiconductor industry, term “printed circuit board is often used interchangeably with “printed wiring board.” See §V.E.

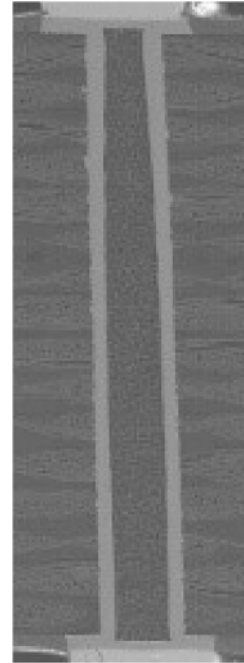
306. Specifically, *Waite* discloses a circuit board assembly including a daughter board 202, which is stacked onto motherboard 200. EX1010 at 6:25–28, FIG. 7. *Waite*’s boards are interposed by spacer connector 204, which includes a plurality of signal vias 402 and ground vias 428 (metal pillars) within spacer connector 204. EX1010 at 6:25–28, 6:59–61, FIG.9. However, *Waite* does not provide a detailed design for the vias 402, 428, and does not disclose whether they

should protrude below the spacer connector 204.



EX1010 at FIG. 7.

307. While a POSITA would have had knowledge of standard designs of via structures, *IPC-4761* nevertheless fills this knowledge gap of *Waite*. Specifically, *IPC-4761* provides a known industry standard design for vias (metal pillars). EX1010 at 10. *IPC-4761*'s vias are similar to the vias of the accused product, as alleged in Patent Owner's Complaint.



EX1011 at 16 (left, optical images of a cross-section view of a standard via); EX1004 at ¶44 (right, SEM images of a cross-section view of the accused via structure).

308. In my opinion, *IPC-4761*'s via design would have been an obvious design choice, as a POSITA would have consulted *IPC-4761*, which is an industry standard, to construct *Waite*'s vias 402, 428. EX1011 at 1. Moreover, in my opinion, a POSITA would have had a reasonable expectation of success when applying *IPC-4761*'s teachings, which embody an industry standard technique, to *Waite*'s well-known via structure.

B. Claim 1

i. 1[pre]: A structure

309. *Waite* discloses “a structure.” For example, *Waite* discloses a circuit board assembly structure. EX1010 at 2:10–11.

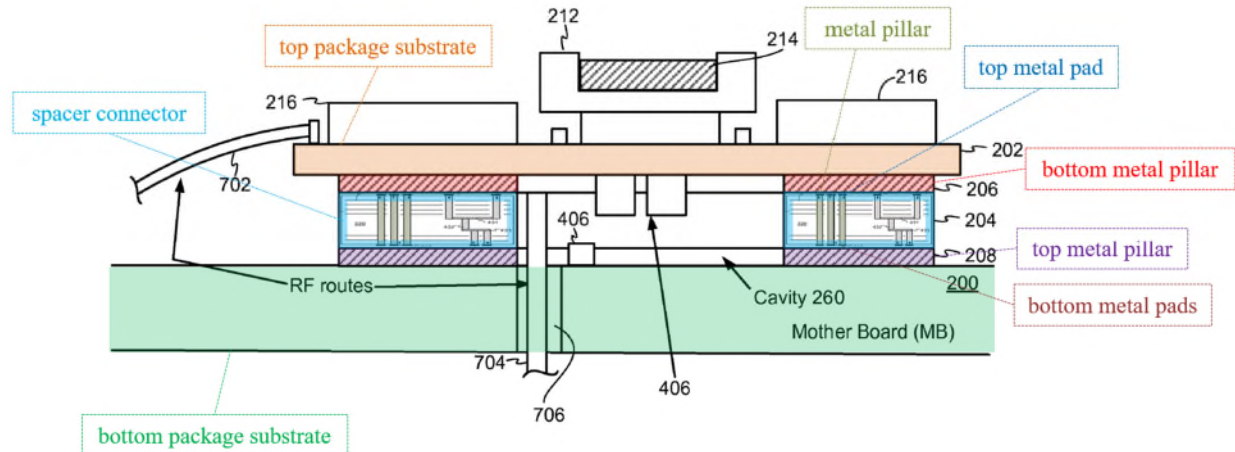


FIG. 7

EX1010 at FIG. 7.

310. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[pre].

ii. 1[a]: a bottom package substrate

311. *Waite* discloses “a bottom package substrate.” *Waite* discloses a **motherboard 200** (bottom package substrate). EX1010 at 9:24–25 (“A variety of RF connections can be made when using one or more connectors of spacer-connector 204 to elevate a daughter board 202 above a motherboard 200”). I understand that according to Patent Owner’s interpretation, a “bottom package substrate” can correspond to a PCB board, such as a motherboard. EX1004 at ¶41 (reading “bottom package substrate” on a “logic board”).

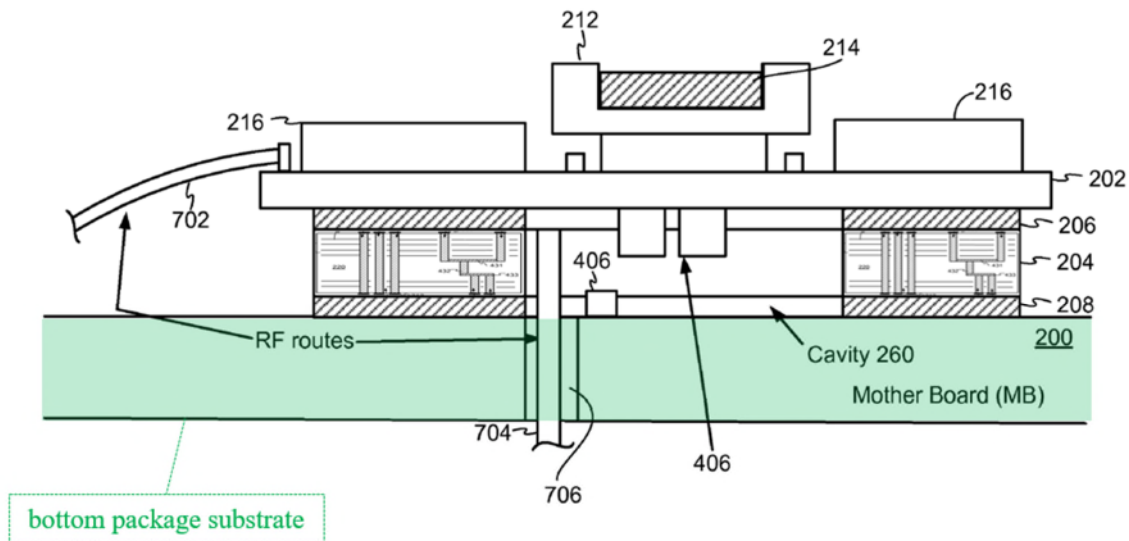


FIG. 7

EX1010 at FIG. 7.

312. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[a].

iii. 1[b]: a top package substrate stacked on top of the bottom package substrate

313. *Waite* discloses “a top package substrate stacked on top of the bottom package substrate.” *Waite* discloses a daughter board 202 (top package substrate) stacked on top of motherboard 200 (bottom package substrate). EX1010 at 9:24–25 (“A variety of RF connections can be made when using one or more connectors of spacer-connector 204 to elevate a daughter board 202 above a motherboard 200”). Similar to the bottom package substrate, I understand that according to Patent Owner’s interpretation, a “top package substrate” can correspond to a PCB board, such as a daughter board. EX1004 at ¶42 (reading “top package substrate” on a

“logic board”).

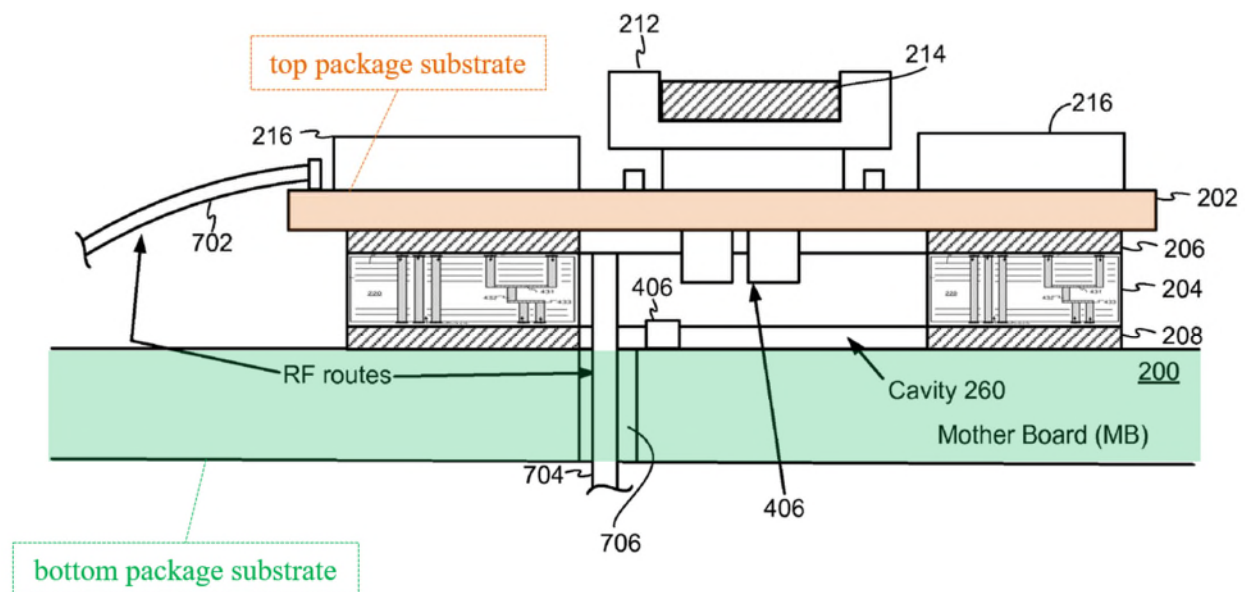


FIG. 7

EX1010 at FIG. 7.

314. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[b].

- iv. **1[c]: at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate**

315. *Waite* discloses “at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.” *Waite* discloses two **spacer connectors 204** interposed between **daughter board 202** (top package substrate) and **motherboard 200** (bottom package substrate) to define a space between **daughter board 202** (top package substrate) and **motherboard 200** (bottom

package substrate). EX1010 at 4:3-11 (“motherboard 200 on which a daughter board 202 is mounted. Daughter board 202 is supported on the motherboard 200 by first and second spacer-connectors 204”), FIGs. 2A, 7.

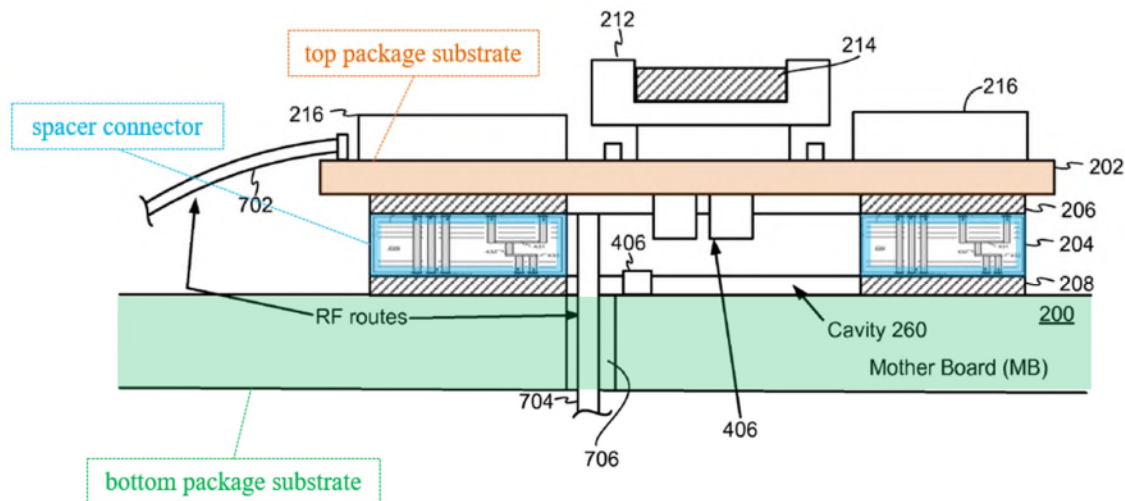


FIG. 7

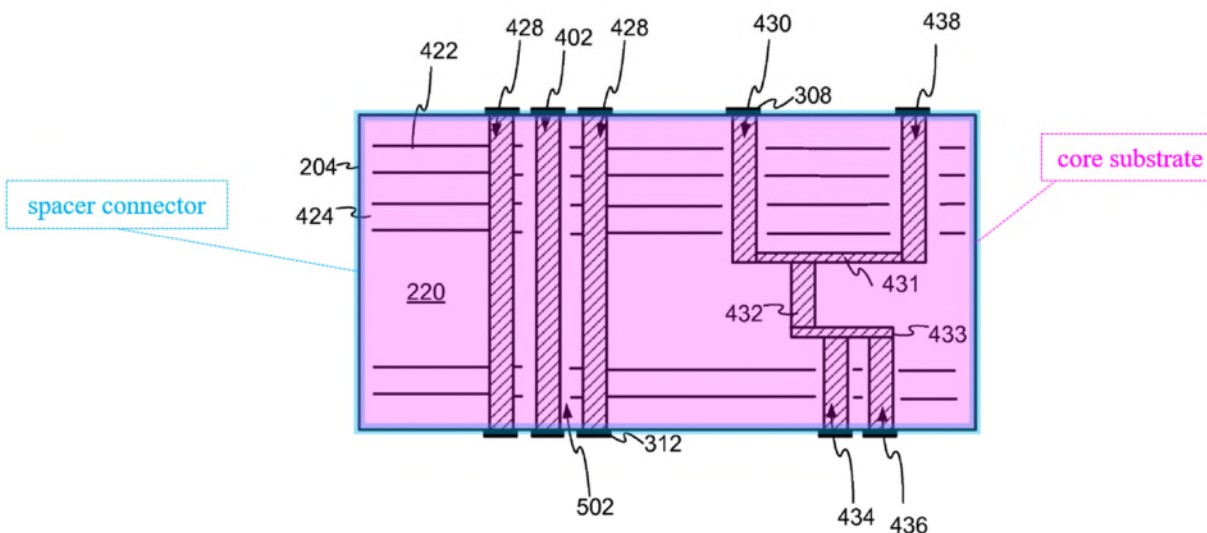
EX1010 at FIG. 7.

316. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[c].

v. 1[d]: the spacer connector comprises a core substrate

317. *Waite* discloses “the spacer connector comprises a core substrate.” *Waite*’s **spacer connectors 204** include a **material 220** (core substrate). EX1010 at 6:59–60. *Waite* teaches that **material 220** (core substrate) includes PCB material, which is “any form of multilayer laminated, case or molded circuit board component.” EX1010 at 2:14–15, 6:28–30. Accordingly, **material 220** (core substrate) is a substrate. As shown in Figure 8, **material 220** (core substrate) forms

the core of each [spacer connector 204](#). EX1010 at 2:14–15, FIG. 8.



EX1010 at FIG. 8.

318. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[d].

vi. 1[e]: a plurality of metal pillars, each passing through the core substrate

319. *Waite* discloses “a plurality of metal pillars, each passing through the core substrate.” *Waite*’s [spacer connectors 204](#) include a plurality of [vias 402, 428](#) (metal pillars), each passing through [material 220](#) (core substrate). For example, *Waite* teaches that [vias 402, 428](#) (metal pillars) pass through [material 220](#) (core substrate) to interface with contact pads [308, 312](#) (top and bottom metal pads), which are disposed on either side of the [material 220](#) (core substrate). Specifically, *Waite*

discloses that “spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428” and “[e]ach via is connected to contact pads (308,312) affixed to it at each PCB surface.” EX1010 at 6:59–61, 10:3–5.

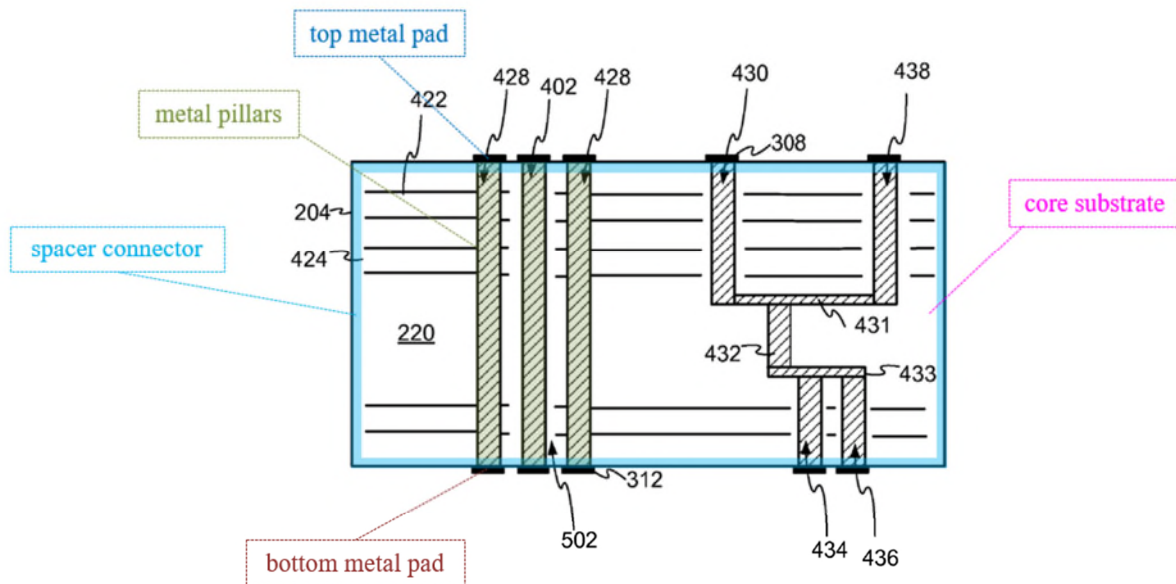


FIG. 8

EX1010 at FIG. 8.

320. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[e].

vii. 1[f]: a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars

321. *Waite* discloses “a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.” *Waite* includes

contact pads 308 (top metal pads), each on a top end of a corresponding via 402, 428 (metal pillar) among the plurality of vias 402, 428 (metal pillars). For example, *Waite* discloses that “[e]ach via is connected to contact pads (308, 312) affixed to it at each PCB surface.” EX1010 at 10:3–5. As shown in Figures 7 and 8, the “PCB surfaces” include a top surface, where a top contact pad 308 (top metal pad) is disposed.

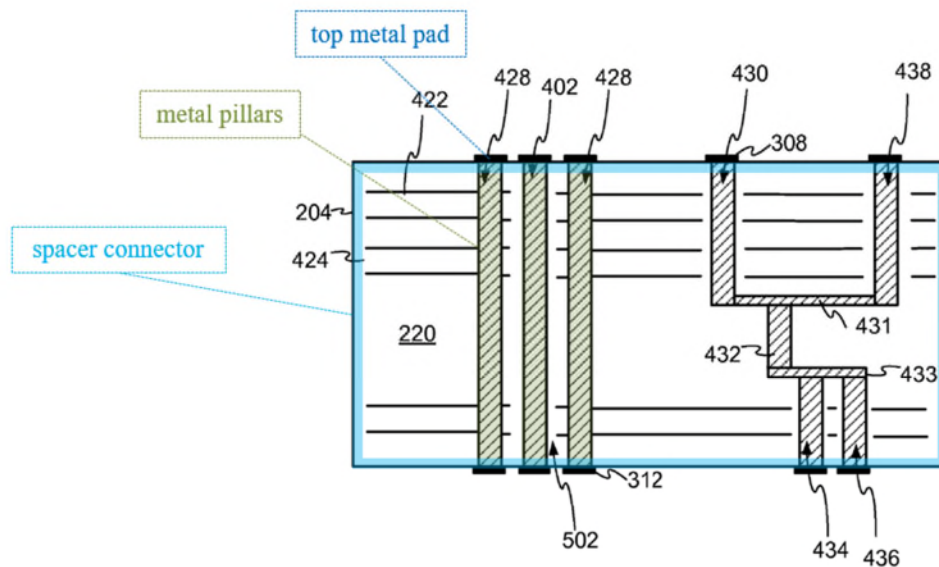


FIG. 8

EX1010 at FIG. 8.

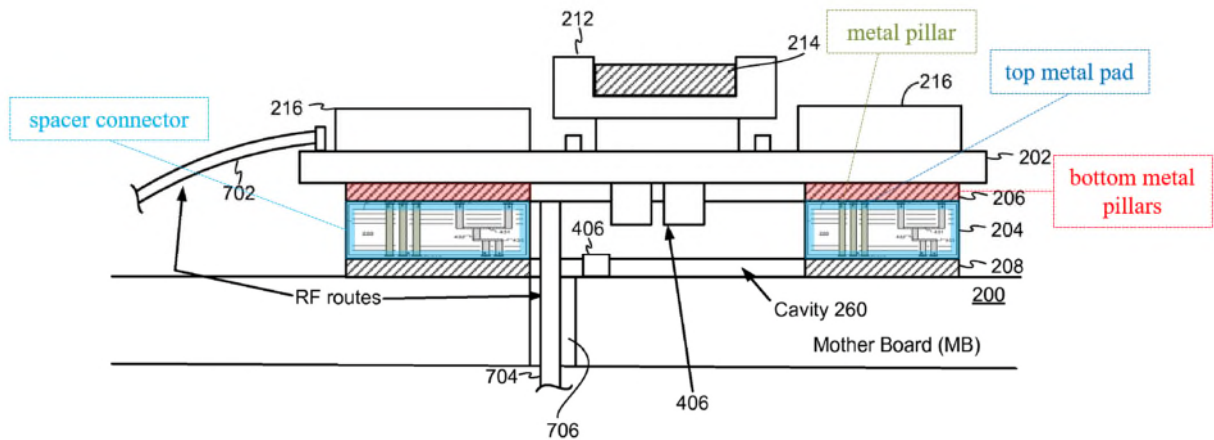


FIG. 7

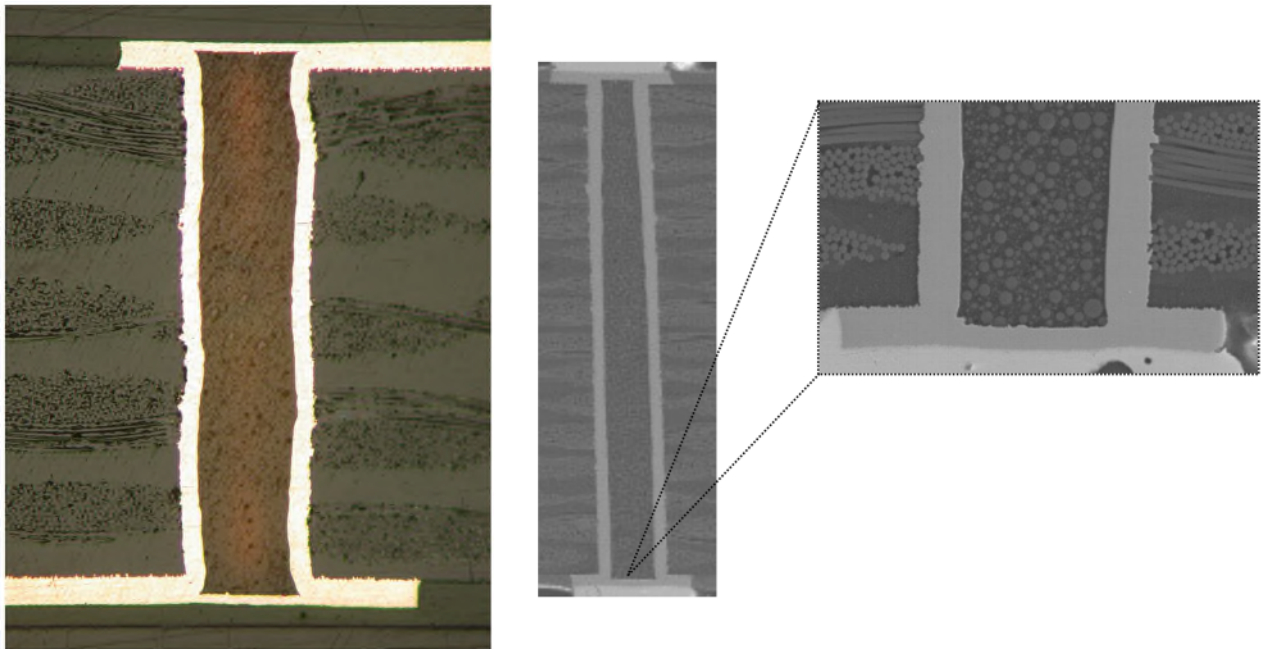
EX1010 at FIG. 7 (FIG. 8 superimposed thereon).

322. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[f].

viii. 1[g]: wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate

323. *Waite* discloses “wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.” Consistent with Patent Owner’s apparent interpretation, the bottom end of each **via 402, 428** (metal pillar) among the plurality of **vias 402, 428** (metal pillars) protrudes downwardly from a bottom surface of **material 220** (core substrate). As discussed above, a POSITA would have been motivated to apply *IPC-4761*’s teachings of its metal pillar design to *Waite*’s **vias 402, 428**. §XVI.A. This design is similar to the accused product, as cited in Patent Owner’s Complaint. EX1004 at ¶¶44, 46. Nearly identical to the via structures accused in Patent Owner’s Complaint

as protruding downwardly from a bottom surface of the core substrate, the *IPC-4761* via structures include metal sidewalls that wrap under the core substrate of a spacer connector, and are covered with an additional layer of conductive material (bottom metal pad). EX1011 at 16; EX1004 at ¶¶44, 46. Thus, *Waite*'s metal pillars, when constructed according to *IPC-4761*'s design, satisfy limitation 1[g], according to Patent Owner's apparent infringement read.



EX1011 at 16 (left, an optical image of a cross-section view of a standard via); EX1004 at ¶¶44, 46 (right, cross-section SEM images of the accused via structure).

324. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[g].

- ix. **1[h]: the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector**

325. *Waite* discloses “the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.” The daughter board 202 (top package substrate) has, on a bottom surface thereof, a plurality of conductive elements 302 (bottom metal pillars) each coupled to a corresponding via 402, 428 (metal pillar) among the plurality of vias 402, 428 (metal pillars) of the spacer connector 204. EX1010 at FIG. 3. In particular, “each” “bottom metal pillar” corresponds to the conductive elements 302 (bottom metal pillars) of *Waite*, which are coupled to vias 402, 428 (metal pillars) in *Waite*’s Figure 3, as shown below. EX1010 at FIG. 3. Further, Figure 3 includes several ellipses associated with the conductive elements 302 (bottom metal pillars), indicating that additional bottom metal pillars and top metal pillars are included in *Waite*’s design, but are omitted from Figure 3. EX1010 at FIG. 3. Thus, *Waite* can include additional conductive elements 302 (top/bottom metal pillars), which align with corresponding conductive elements 302 (top/bottom metal pillars) that are not illustrated in Figure 3. *Waite* further discloses that conductive elements 302 (bottom metal pillars) are disposed within conductive elastomer 206, which interfaces with daughter board 202 (top package substrate) and vias 402, 428 (metal pillars) disposed within the spacer connector 204. EX1010 at 4:12–16 (“the first and second conductive elastomers 206, 208 each include vertically coupled conductive elements 302 in a high density grid

that provide high quality coupling (e.g., low parasitic (e.g., resistance, capacitance, inductance), low noise and cross-talk, wide band path.”). *Waite* teaches that the **conductive elements 302** (bottom metal pillars) can be conductive cubes, segments, spring pins, or formed pin type connectors. EX1010 at 4:18, 4:61. Any of these configurations can correspond to the claimed “metal pillars.”

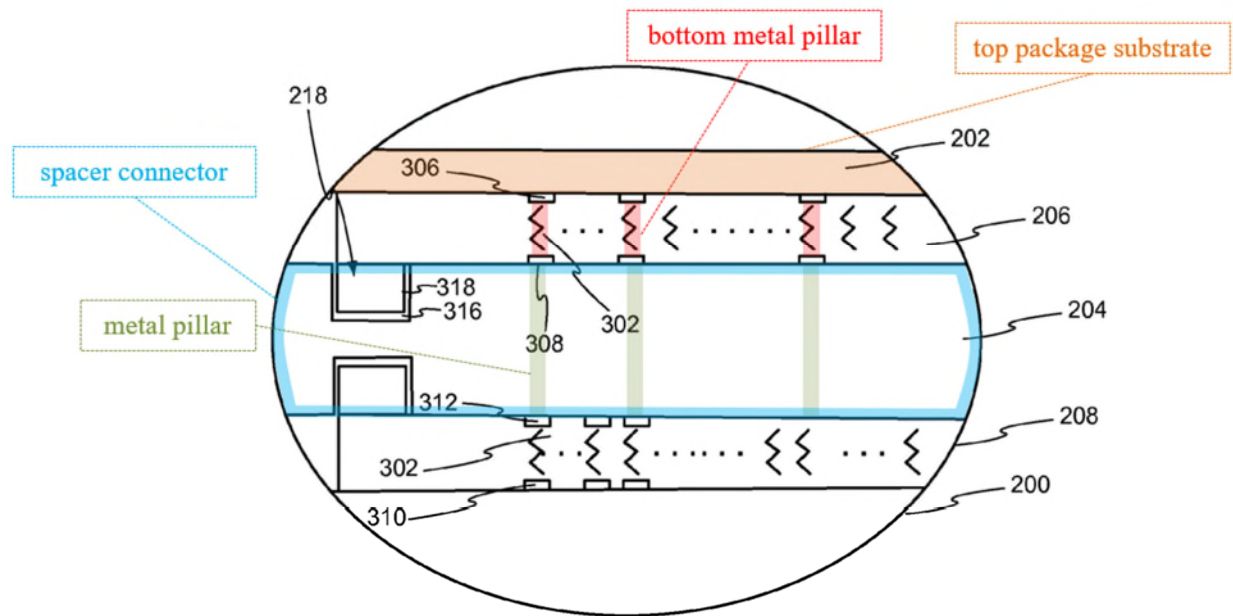


FIG. 3

EX1010 at FIG. 3.

326. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[h].

- x. **1[i]: the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector**

327. *Waite* discloses “the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.” The motherboard 200 (bottom package substrate) has, on a top surface thereof, a plurality of conductive elements 302 (top metal pillars) each coupled to a corresponding via 402, 428 (metal pillar) among the plurality of vias 402, 428 (metal pillars) of the spacer connector 204. EX1010 at FIG. 3. *Waite* teaches that the conductive elements 302 (top metal pillars) are disposed within conductive elastomer 208, which interfaces with motherboard 200 (bottom package substrate) and vias 402, 428 (metal pillars) (disposed within spacer connector 204). EX1010 at 4:12–16 (“the first and second conductive elastomers 206, 208 each include vertically coupled conductive elements 302 in a high density grid that provide high quality coupling (e.g., low parasitic (e.g., resistance, capacitance, inductance), low noise and cross-talk, wide band path.”). As discussed above, the conductive elements 302 (top metal pillars) can be conductive cubes, segments, spring pins, or formed pin type connectors, which correspond to the claimed “metal pillars.” EX1010 at 4:17-19, 4:56-63.

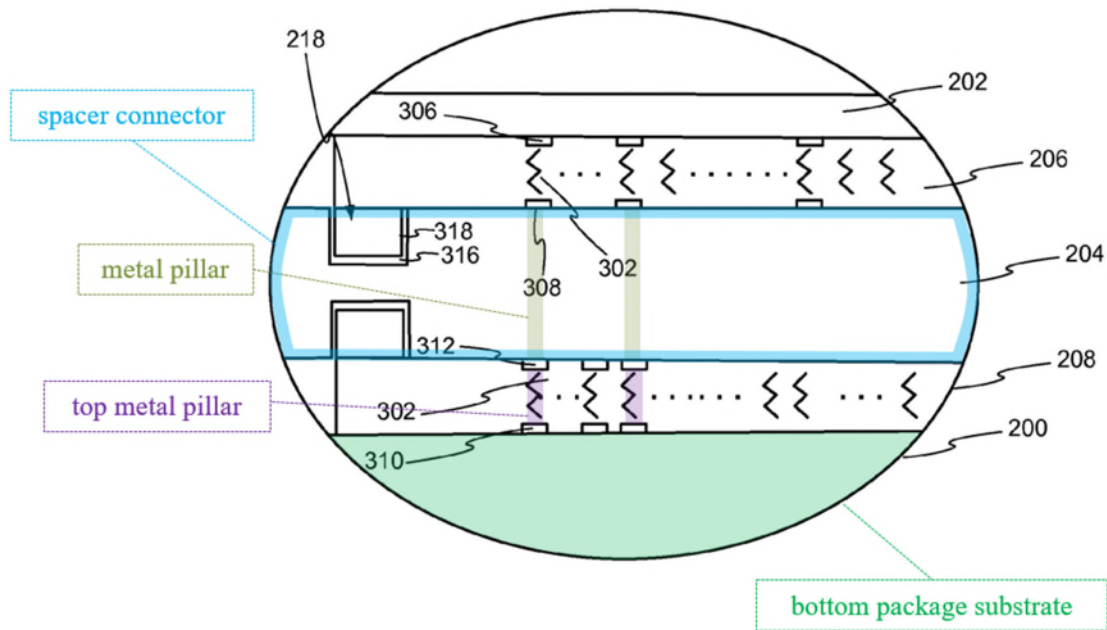


FIG. 3

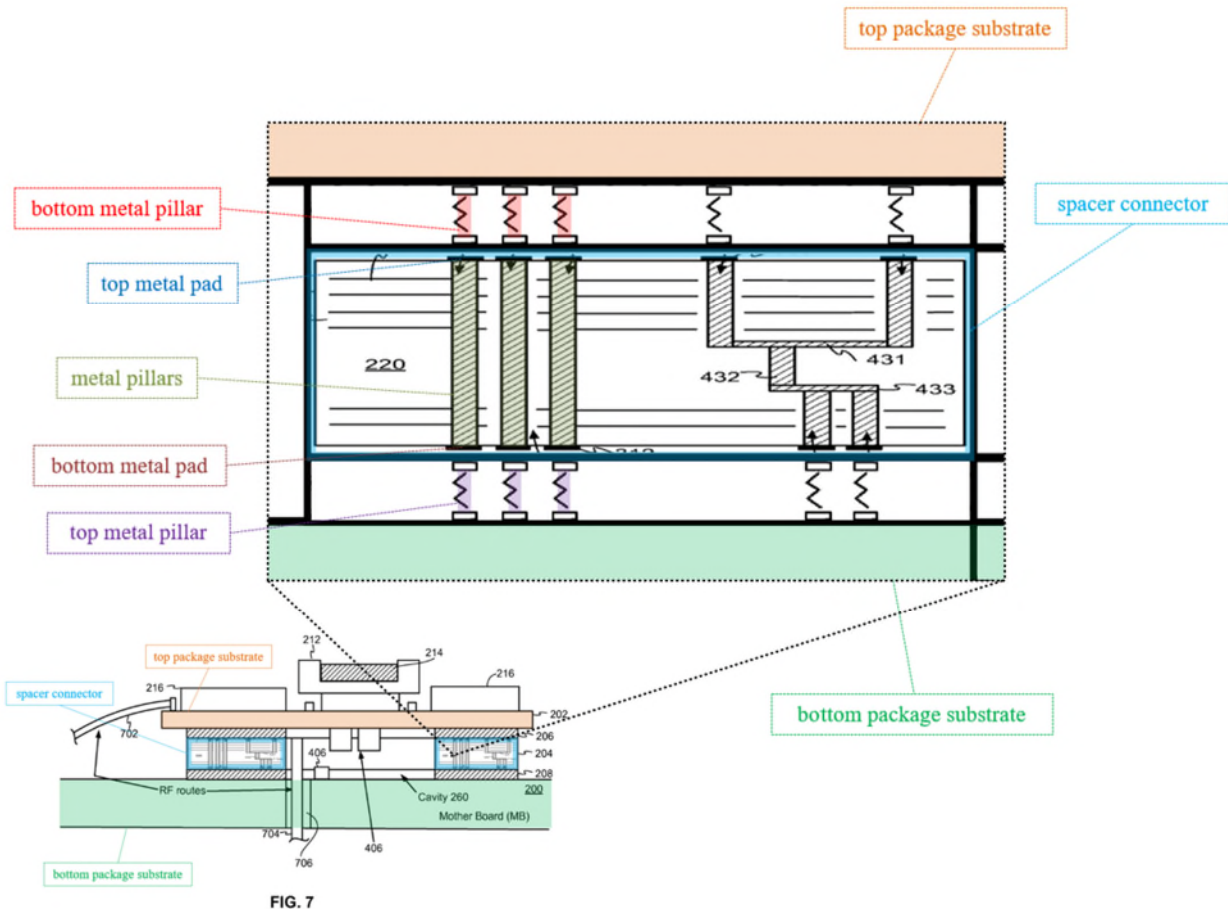
EX1010 at FIG. 3.

328. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[i].

- xi. **1[j]: the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate**

329. *Waite* discloses “the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.” Daughter board 202 (top package substrate) is electrically coupled to motherboard 200 (bottom package

substrate) through the plurality of **conductive elements 302** (bottom metal pillars) of the **daughter board 202** (top package substrate), the plurality of **vias 402, 428** (metal pillars) of the **spacer connector 204**, and the plurality of **conductive elements 302** (top metal pillars) of the motherboard 200 (bottom package substrate). EX1010 at FIGs. 3, 7, 8. According to *Waite*, the **contact pads 308** (top metal pads) of **vias 402, 428** (metal pillars) are coupled to **conductive elements 302** (bottom metal pillars), and **contact pads 312** (bottom metal pads) of **vias 402, 428** (metal pillars) are coupled to **conductive elements 302** (top metal pillars). EX1010 at 4:19–26 (“Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the mother board 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.”), 10:3–5. Thus, the daughter board 202 (top package substrate) is electrically connected to the **motherboard 200** (bottom package substrate) through the **conductive elements 302** (bottom metal pillars) of the **daughter board 202** (top package substrate), **vias 402, 428** (metal pillars), and **conductive elements 302** (top metal pillars) of the **motherboard 200** (bottom package substrate), as shown below.



EX1010 at FIG. 7 (FIGs. 3 and 8 superimposed thereon).

330. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[j].

xii. 1[k]: a bottom chip arranged in the space between the bottom package substrate and the top package substrate

331. *Waite* discloses “a bottom chip arranged in the space between the bottom package substrate and the top package substrate.” *Waite* discloses component 406 (bottom chip) arranged in the space between motherboard 200 (bottom package substrate) and daughter board 202 (top package substrate). Specifically, *Waite* teaches component 406 (bottom chip) is mounted on motherboard 200 (bottom

package substrate), between two [spacer connectors 204](#) (spacer connectors). EX1010 at 7:1–6 (“The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”), 7:31–34. *Waite’s* component 406 (bottom chip) corresponds to a “RF tuning component” or “RF tuning circuitry.” For example, *Waite* teaches that “[t]he cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200” and “tuning components 406 to be located near the DUT 214 on the underside of the daughter board 202 and/or on the mother board 200.” EX1010 at 7:1–6, 9:29–30. *Waite* further discloses that “it may be desirable to place RF tuning circuitry and RF-related components close to the device under test.” EX1010 at 6:14–16. Both an RF tuning component and RF tuning circuitry correspond to a “chip,” because these can be discrete integrated circuit components. For example, IPC-T-50, which is a standards document that provides a list of definitions accepted in the semiconductor packaging industry, defines the terms “chip” and “die” as “[s]eparated piece(s) of semiconductor wafer that constitute a discrete semiconductor or integrated circuit.” EX1017 at 26, 41. Both “RF tuning components” and “RF tuning circuitries” fall

within this definition. In any case, it would be obvious to implement RF tuning circuitries in a discrete die, as is commonly done in the industry.

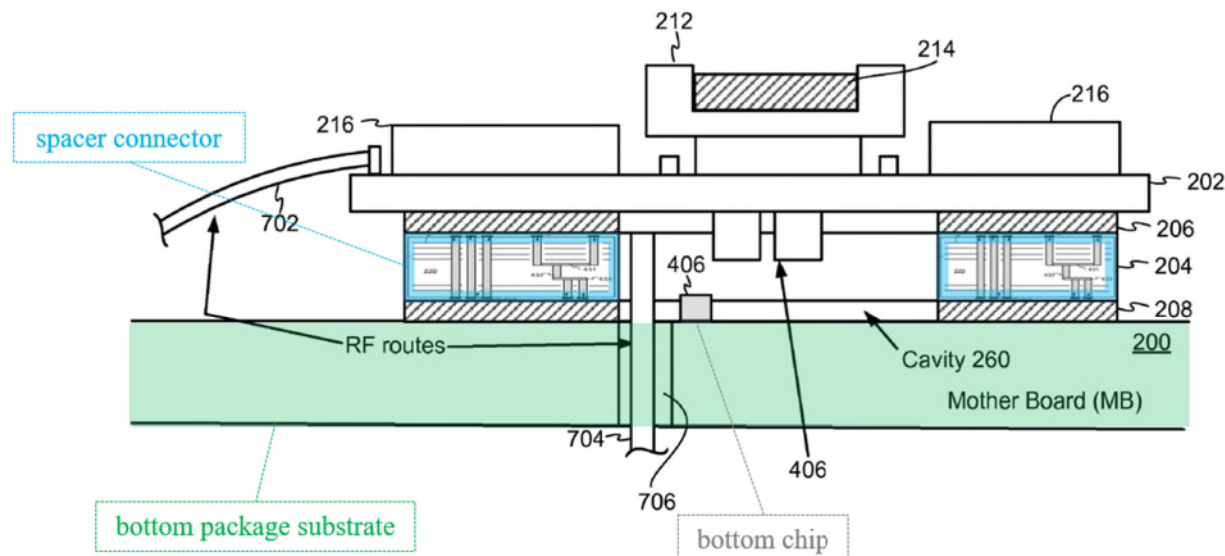


FIG. 7

EX1010 at FIG. 7.

332. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[k].

xiii. 1[l]: the bottom chip is mounted to the top surface of the bottom package substrate

333. *Waite* discloses “the bottom chip is mounted to the top surface of the bottom package substrate.” *Waite*’s component 406 (bottom chip) is mounted to the top surface of motherboard 200 (bottom package substrate). EX1010 at 7:1–6 (component 406 can be located “on the top side of the motherboard 200”).

elements 406 and the DUT 214.”). Thus, *Waite* teaches two spacer connectors 204 are arranged on opposite sides of the component 406 (bottom chip), as shown below.

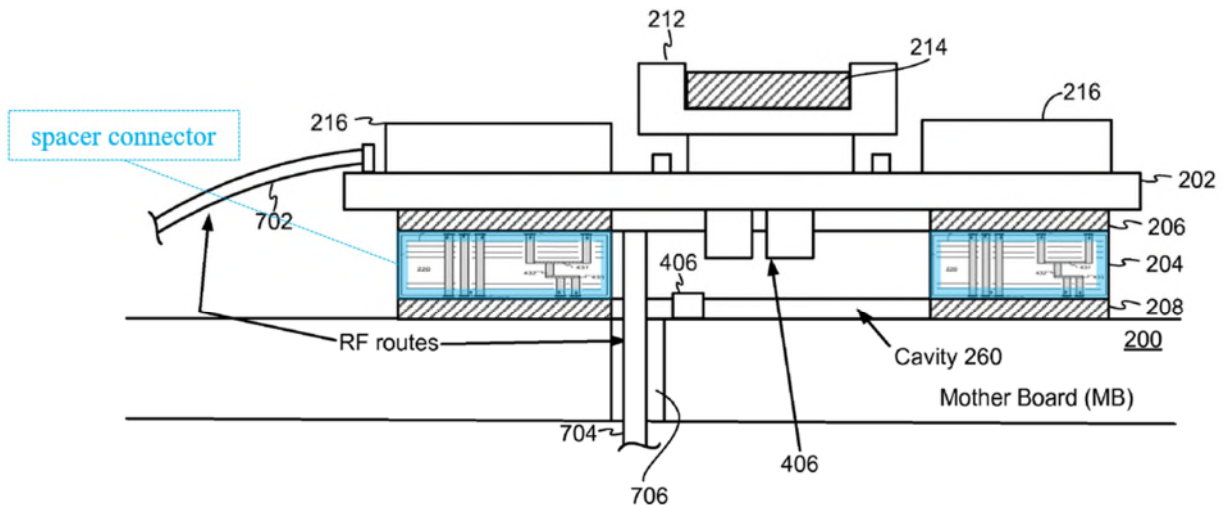


FIG. 7

EX1010 at FIG. 7.

336. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of limitation 1[m].

C. Claim 2

- i. the structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate**

337. *Waite* discloses “the structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.” The top surface of component 406 (bottom chip) is spaced downwardly from the bottom surface of daughter board 202 (top package substrate). As discussed above, *Waite* discloses that component 406 (bottom chip) is disposed within a cavity

260, which is formed below daughter board 202 (top package substrate), as shown below. EX1010 at 6:66-7:6 (“The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”).

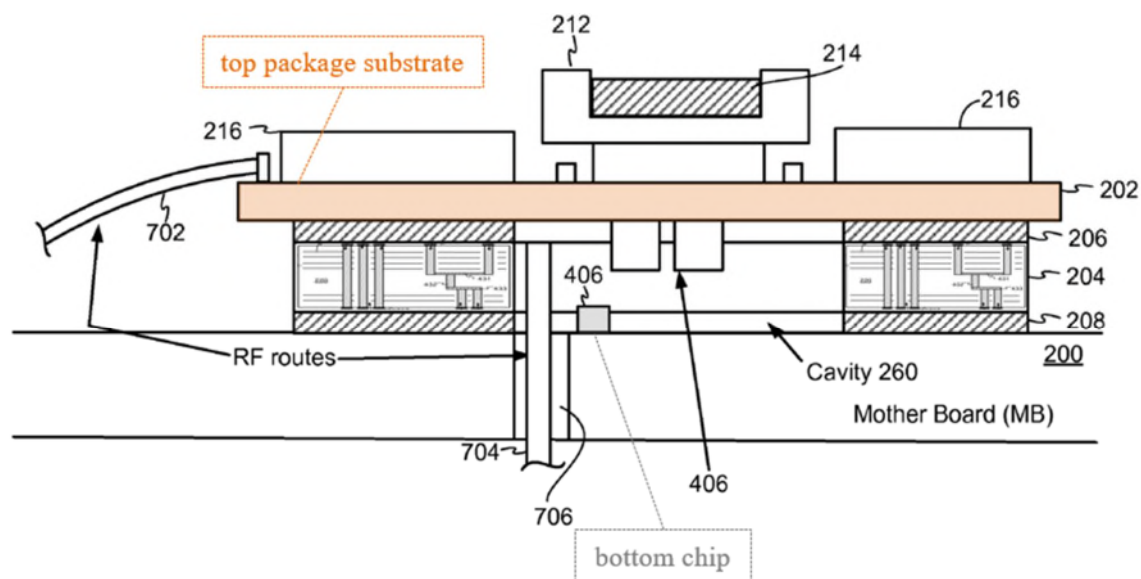


FIG. 7

EX1010 at FIG. 7.

338. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of claim 2.

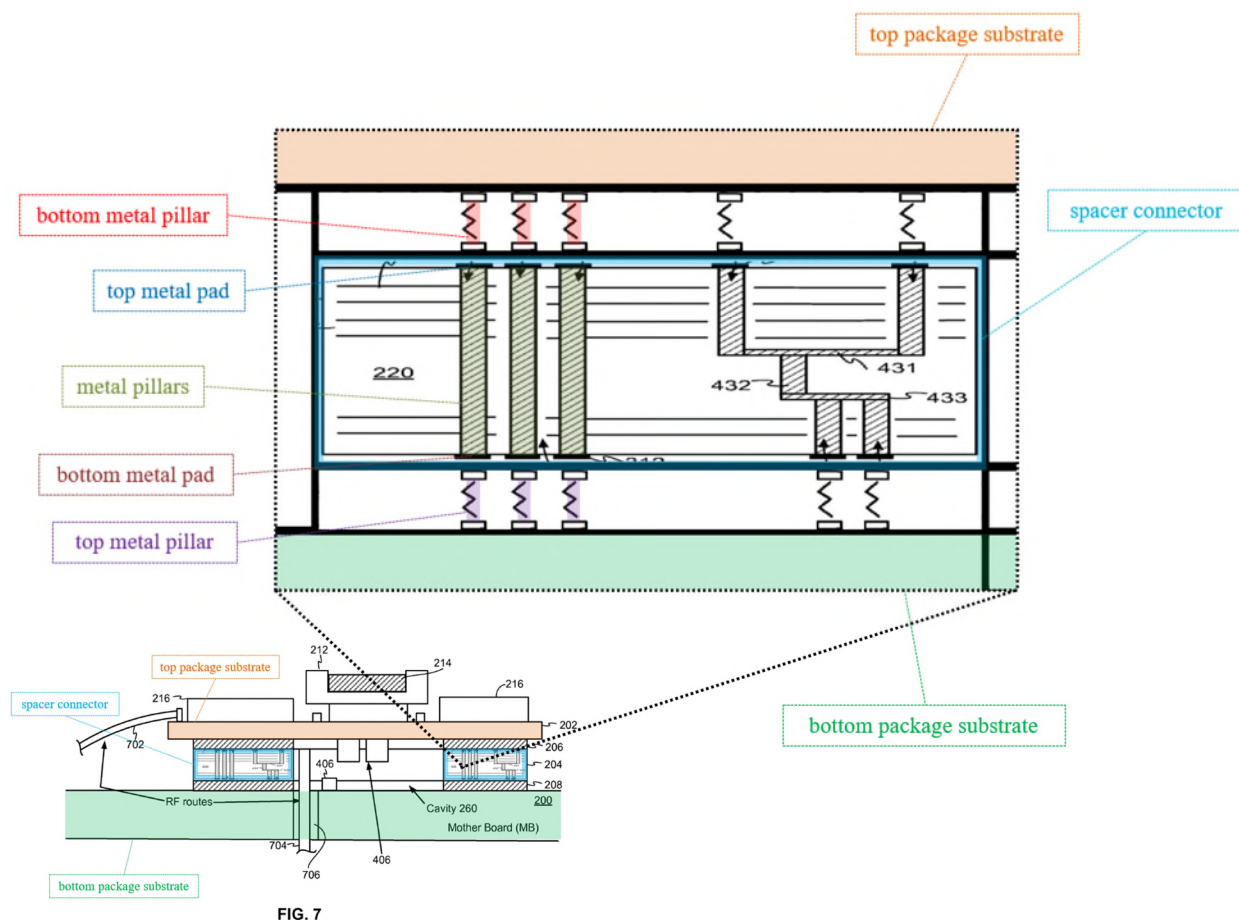
D. Claim 4

- i. **The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among**

the plurality of top metal pillars of the bottom package substrate

339. *Waite* discloses “the structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.” Each conductive element 302 (bottom metal pillar) among the plurality of **conductive elements 302** (bottom metal pillars) of **daughter board 202** (top package substrate) is aligned with a corresponding **via 402, 428** (metal pillar) among the plurality of **vias 402, 428** (metal pillars) of **spacer connector 204**, and with a corresponding **conductive element 302** (top metal pillar) among the plurality of **conductive elements 302** (top metal pillars) of **motherboard 200** (bottom package substrate). Specifically, *Waite* teaches that (1) **contact pads 308** (top metal pads) of **vias 402, 428** (metal pillars) are coupled to **conductive elements 302** (bottom metal pillars), and (2) **contact pads 312** (bottom metal pads) of **vias 402, 428** (metal pillars) are coupled to **conductive elements 302** (top metal pillars). For example, *Waite* teaches that “[l]ower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the mother board 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the

conductive elements 302 of the second conductive elastomer 208.” EX1010 at 4:19–26. Further, “[e]ach via is connected to contact pads (308, 312) affixed to it at each PCB surface.” *Id.* at 10:3-5. Thus, the conductive elements 302 (top and bottom metal pads) are connected to the **vias 402, 428** (metal pillars) via the **contact pads 308** (top metal pads) and **contact pads 312** (bottom metal pads). As shown below, such a configuration includes aligned metal pillars. Additionally, as shown below, “each bottom metal pillar among the plurality of bottom metal pillars,” corresponds to the three leftmost pillars illustrated in *Waite*’s Figure 8. EX1010 at FIG. 8.



EX1010 at FIG. 7 (FIGs. 3 and 8 superimposed thereon).

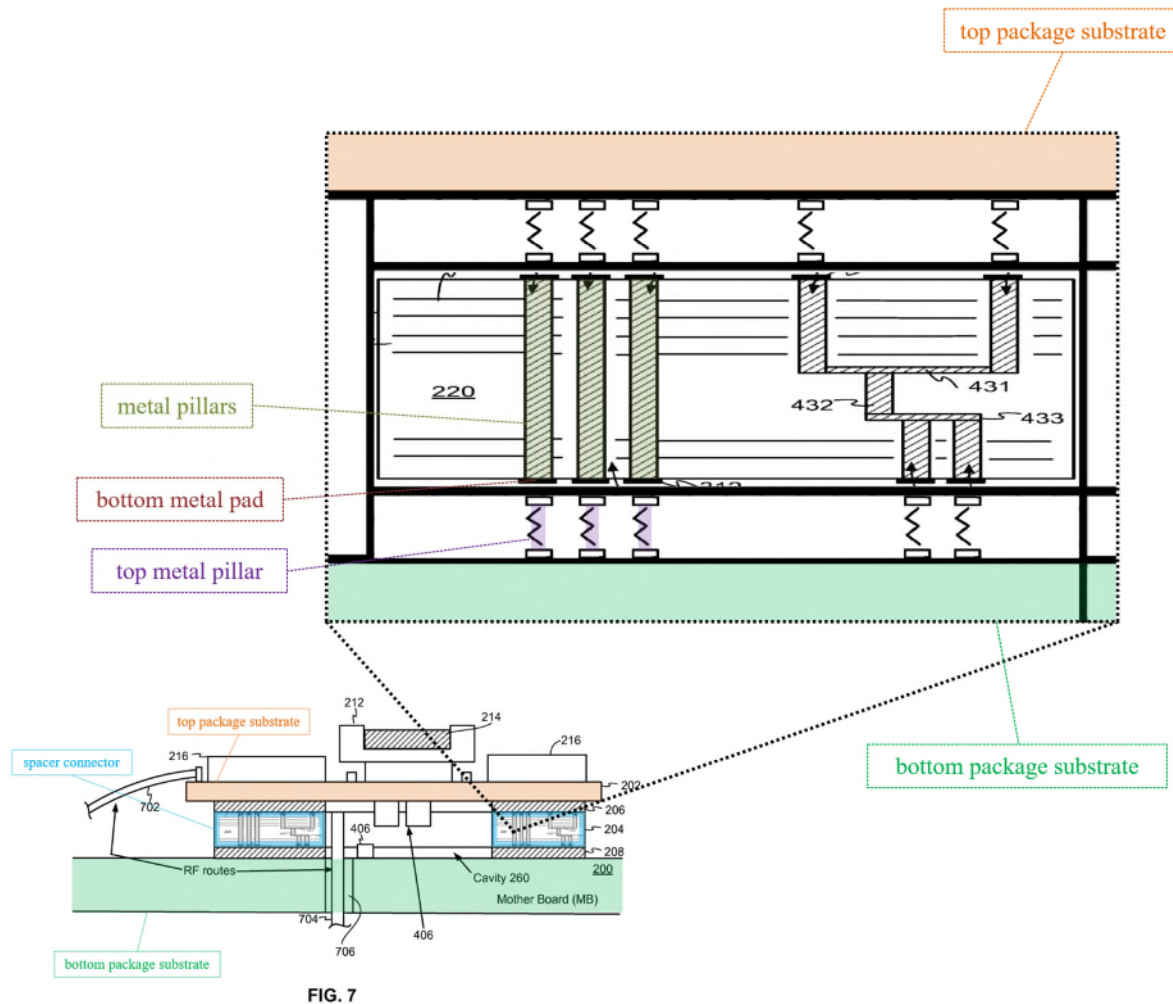
340. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious each limitation of claim 4.

E. Claim 6

- i. **6[a]: The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate**

341. *Waite* discloses “the structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate.” The bottom ends of the plurality of **vias 402, 428** (metal pillars) protruding downwardly from the bottom surface of **material 220** (core substrate) of **spacer connector 204** are connected, in an end-to-end manner, to corresponding top ends of the plurality of **conductive elements 302** (top metal pillars) of **motherboard 200** (bottom package substrate). Specifically, *Waite* teaches that **contact pads 312** (bottom metal pads) are disposed on the bottom ends of **vias 402, 428** (metal pillars), and are electrically connected to the **conductive elements 302** (top metal pillars). EX1010 at 4:23–26. The **contact pads 312** (bottom metal pads) and **conductive elements 302** (top metal pillars) are connected in an end-to-end manner, because the bottom **ends** of **vias 402, 428** (metal pillars) are connected to the top **ends** of

conductive elements 302 (top metal pillars), as shown below. EX1010 at FIGs. 3, 7, 8.



EX1010 at FIG. 7 (FIGs. 3 and 8 superimposed thereon). This interpretation of “end-to-end manner” is consistent with Patent Owner’s infringement allegations, which rely on vias with capped bottom ends in meeting the “end-to-end” requirement. *See, e.g.*, EX1004 at 16.

342. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious limitation

6[a].

- ii. **6[b]: bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector**

343. *Waite* discloses “bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.” The bottom ends of the plurality of **conductive elements 302** (bottom metal pillars) of the **daughter board 202** (top package substrate) are connected to the corresponding top ends of the plurality of **vias 402, 428** (metal pillars) of the **spacer connector 204** via corresponding **contact pads 308** (top metal pads) of the **spacer connector 204**. For example, *Waite* teaches that the daughter board 202 is “coupled to upper contact pads 308 of the first spacer-connector 204, through... conductive elements 302.” EX1010 at 4:19–23, FIG. 7.

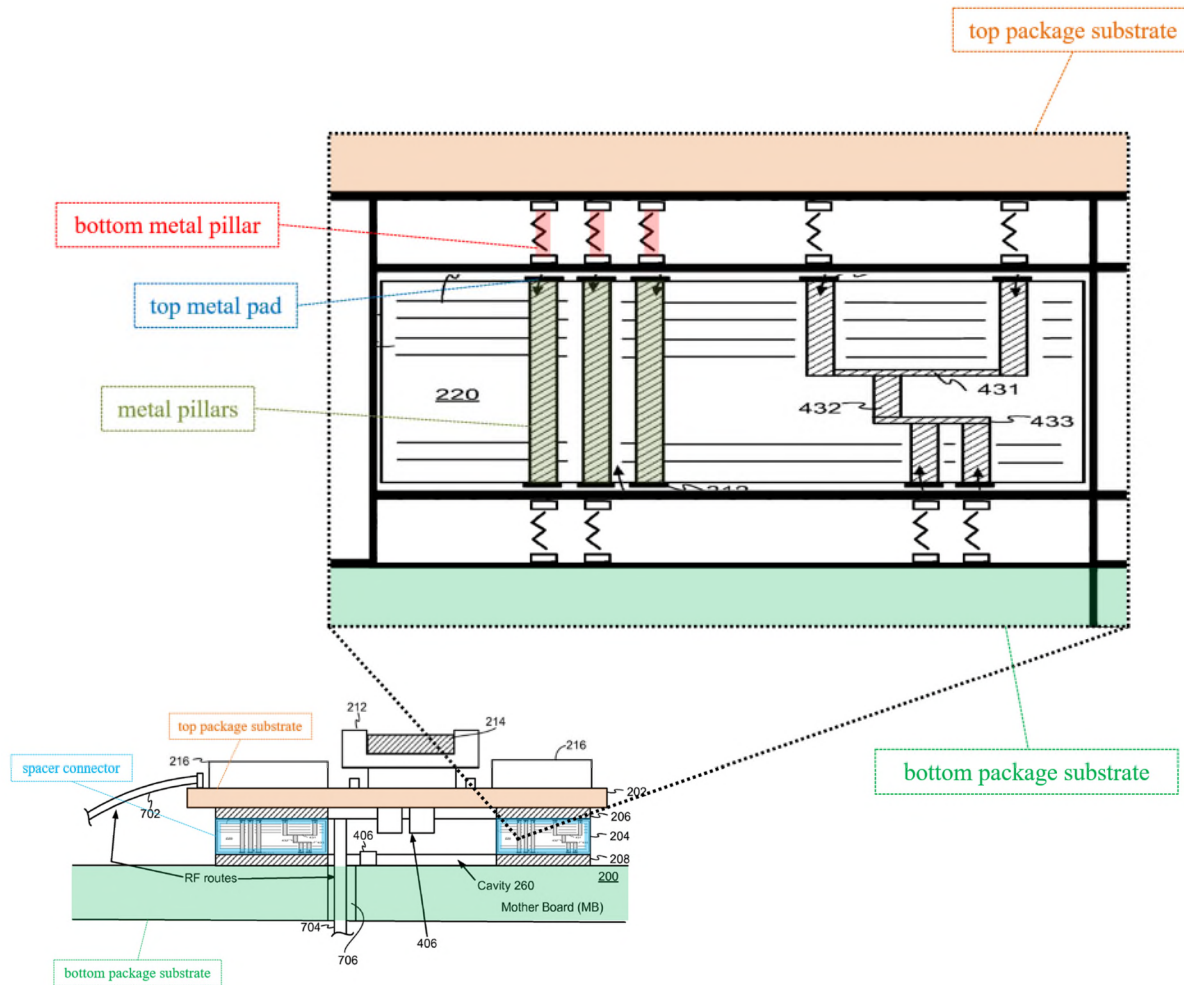


FIG. 7

EX1010 at FIG. 7 (FIGs. 3 and 8 superimposed thereon).

344. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious limitation 6[b].

F. Claim 9

- i. **9[a]: The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars**

345. *Waite* discloses “the structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a

corresponding metal pillar among the plurality of metal pillars.” The [spacer connector 204](#) includes a plurality of bottom metal pads, each on the bottom end of a corresponding [via 402, 428](#) (metal pillar) among the plurality of [vias 402, 428](#) (metal pillars). As discussed above with reference to limitation 1[f], *Waite and IPC-4761 renders obvious top metal pads*. §XVI.B.vii. For at least the same reasons as discussed with reference to the top metal pads, *Waite* similarly renders obvious bottom metal pads on the bottom ends of the [vias 402, 428](#) (metal pillars). §XVI.B.vii.

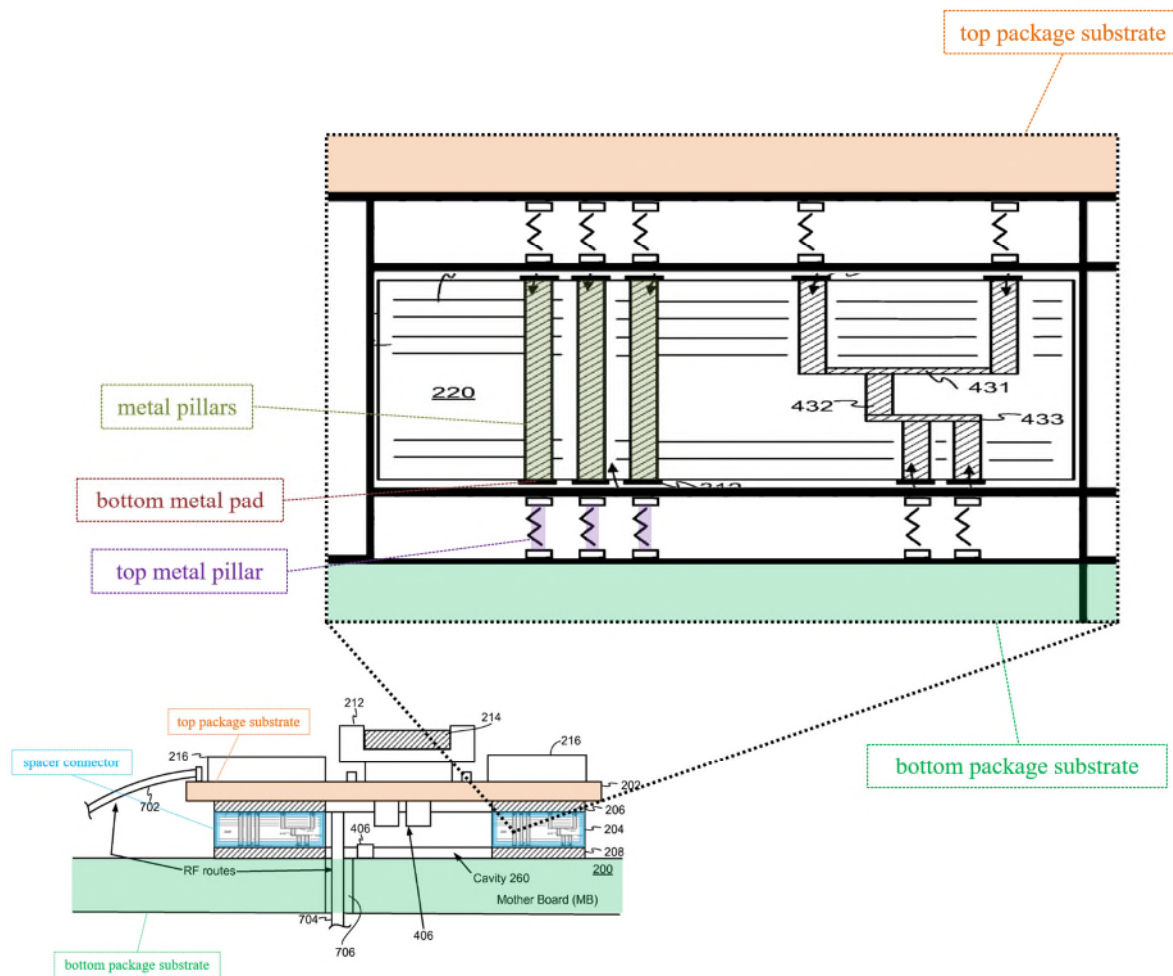


FIG. 7

EX1010 at FIG. 7 (FIGs. 3 and 8 superimposed thereon).

346. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious limitation 9[a].

- ii. **9[b]: the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector**

347. *Waite* discloses “the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector.” The bottom ends of *vias 402, 428* (metal pillars) are connected to corresponding top ends of *conductive elements 302* (top metal pillars) of the *motherboard 200* (bottom package substrate) via *contact pads 312* (bottom metal pads). For example, *Waite* teaches that the motherboard 200 is “coupled to lower contact pads 312 of the first [spacer-]connector 204, through... conductive elements 302”). EX1010 at 4:23–26, FIG. 7.

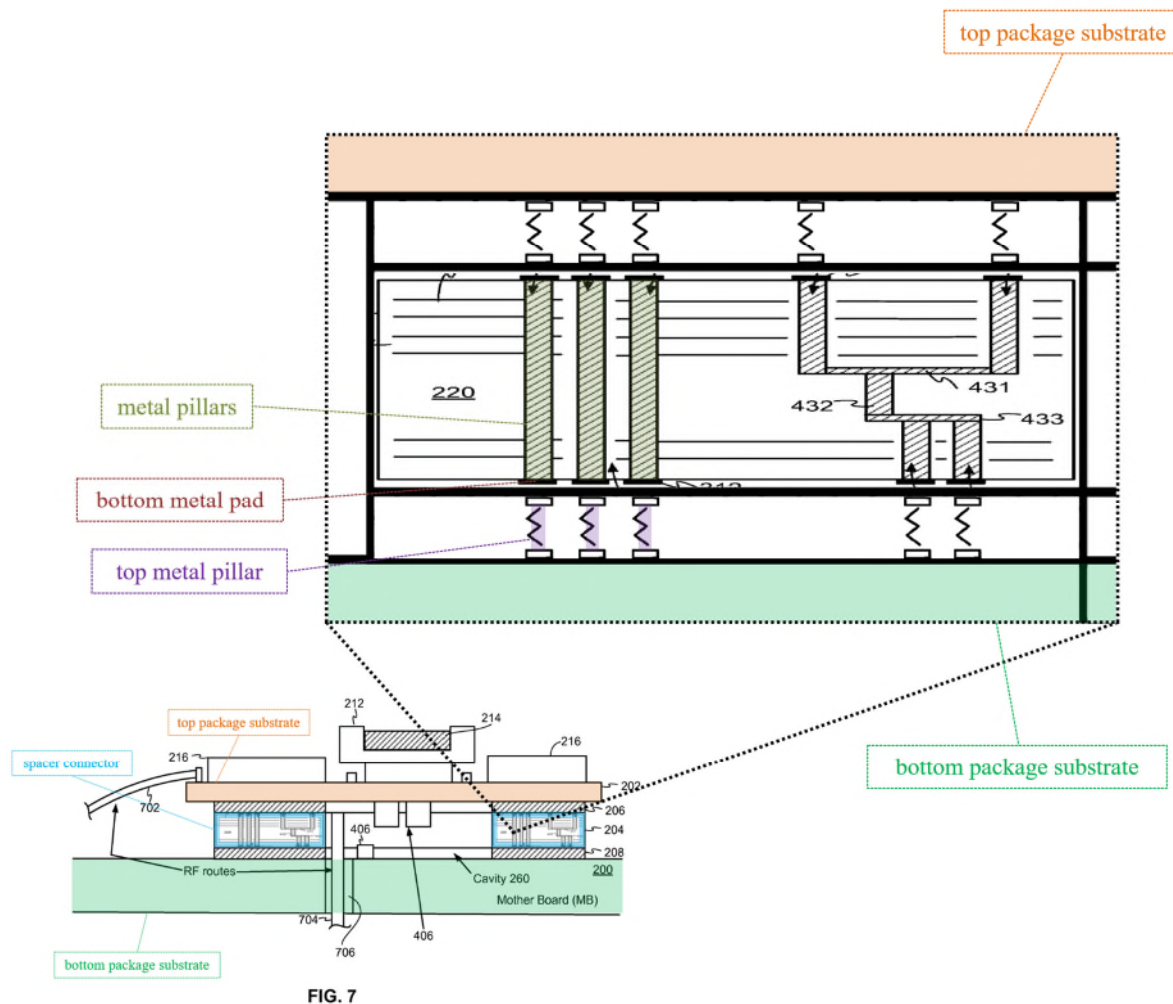


FIG. 7

EX1010 at FIG. 7 (FIGs. 3 and 8 superimposed thereon).

348. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious limitation 9[b].

- iii. **9[c]: bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector**

349. Limitation 9[c] is identical to limitation 6[b]. Accordingly, in my opinion, *Waite* discloses limitation 9[c], for the same reasons discussed above, with

reference to limitation 6[b]. §XVI.E.ii.

350. Thus, in my opinion, *Waite* and *IPC-4761* renders obvious limitation 9[c].

XVII.CONCLUSION

351. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. I further understand that willful false statements and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Executed on March 31, 2026.

By: 
Peter Elenius