UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.

Petitioners

v.

TOPWIRE LLC,
Patent Owner

Case No. IPR2026-00324
U.S. Patent No. 9,859,202

PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 9,859,202

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PETITIONERS' EXHIBIT LIST[1]

Exhibit	Description of Documents
EX1001	U.S. Patent No. 9,859,202
EX1002	Prosecution History of U.S. Patent No. 9,859,202
EX1003	Declaration of Peter Elenius in support of petition for *inter partes* review of U.S. Patent No. 9,859,202
EX1004	*TopWire LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.*, No. 2:25-cv-01183, Dkt. 1 ("Complaint") (E.D. Tex. Dec. 1, 2025)
EX1005	U.S. Patent Publication No. 2011/0147908 ("*Sun*"), published June 23, 2011
EX1006	U.S. Patent Publication No. 2013/0182402 ("*Chen*"), published July 18, 2013
EX1007	U.S. Patent No. 5,334,804 ("*Love*"), granted Aug. 2, 1994
EX1008	U.S. Patent Publication No. 2013/0249083 ("*Hu*"), published Sept. 26, 2013
EX1009	Benson, et al., *Polymer Adhesives and Encapsulants for Microelectronic Applications*, Johns Hopkins APL Technical Digest, Volume 28, Number 1 ("*Benson*") (2008)
EX1010	U.S. Patent No. 8,379,403 ("*Waite*"), granted Feb. 19, 2013
EX1011	IPC, *IPC-4761 Design Guide for Protection of Printed Board Via Structures* ("*IPC-4761*") (July 2006)
EX1012	Declaration of Sylvia D. Hall-Ellis, Ph.D. in support of authenticity and public availability of documents for *inter partes* review of U.S. Patent No. 9,859,202
EX1013	U.S. Patent Publication No. 2008/0155820 ("*Arai*"), published July 3, 2008
EX1014	Osborn, *All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices*, Georgia Institute of Technology (May 2009)
EX1015	Henderson, *Copper Pillar Bumping Technology*, Info Tracks (Semitracks Monthly Newsletter), Issue 36 (June 2012)

[1] Unless otherwise indicated, U.S. patents are cited by column:line, U.S. patent application publications, complaints, and declarations by paragraph number, patent figures by figure number, and all other materials by Bates number.

EX1016	Kreidl, *Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module*, Universität Mannheim (2011)
EX1017	IPC, *IPC-T-50M Terms and Definitions for Interconnecting and Packaging Electronic Circuits* (May 2015)
EX1018	Cohn, et al., *Electronic Packaging and Interconnection Handbook, Packaging and Interconnection of Integrated Circuits*, Chapter 7, McGraw-Hill (2000)
EX1019	Vintage Computer, *IBM PC/AT* (first archived on Mar. 5, 2021) https://vintage-computer.com/machines.php?ibmpcat [https://web.archive.org/web/20210305084621/vintage-computer.com/machines.php?ibmpcat]
EX1020	Mangrum, *Packaging Technologies for Mobile Platforms*, 2006 Electronics Packaging Technology Conference (2006)
EX1021	ICE, *Roadmaps of Packaging Technology*, *Interconnect Substrate Technologies*, Chapter 11 (1997)
EX1022	Kenny, et al., *From Thin Cores to Outer Layers: Filling through Holes and Blind Micro Vias with Copper by Reverse Pulse Plating*, 2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP) (2009).
EX1023	JEDEC, *JESD47F Stress-Test-Driven Qualification of Integrated Circuits* (Dec. 2007)
EX1024	IPC, *IPC-TM-650 Test Methods Manual* (May 2004)
EX1025	Koide, et al., *High-performance Flip-Chip BGA Technology Based on Thin-core and Coreless Package Substrate*, 2006 Electronic Components and Technology Conference (2006)
EX1026	Graf, *Modern Dictionary of Electronics*, Newnes, Seventh Edition (1999)
EX1027	Tummala, et al., *Microelectronics Packaging Handbook*, Van Nostrand Reinhold (1989)
EX1028	Baldwin, *Fundamentals of Microsystem Packaging*, *Fundamentals of IC Assembly*, Chapter 9, McGraw-Hill (2001)
EX1029	Wang, et al., *Studies on A Novel Flip-Chip Interconnect Structure – Pillar Bump*, 2001 Electronic Components and Technology Conference (2001)
EX1030	CV of Peter Elenius
EX1031	Petitioners' Stipulation

MANDATORY NOTICES UNDER 37 C.F.R 42.8(A)(1)

Real Party in Interest: The real parties in interest are Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc., Petitioners.

Related Matters: U.S. Patent No. 9,859,202 ("'202 patent") is currently asserted by Patent Owner ("PO") against Petitioners in the case styled: *Topwire LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics Am., Inc.*, 2:25-cv-01183 (E.D. Tex.), which was originally filed on December 1, 2025.

Lead Counsel and Back-Up Counsel: Petitioners designate lead and back-up counsel as noted below. Powers of Attorney are filed concurrently herewith under 37 C.F.R. § 42.10(b).

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Service Information: Correspondence to lead and back-up counsel can be provided at the postal and electronic addresses above. Petitioners also consent to service by electronic mail at DLSamsung202IPR@BakerBotts.com.

CLAIMS LISTING

Claim 1:

1[pre]	A structure, comprising:
1[a]	a bottom package substrate;
1[b]	a top package substrate stacked on top of the bottom package substrate;
1[c]	at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein
1[d]	the spacer connector comprises a core substrate;
1[e]	a plurality of metal pillars, each passing through the core substrate; and
1[f]	a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;
1[g]	wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,
1[h]	the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,
1[i]	the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and
1[j]	the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and
1[k]	a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein
1[l]	the bottom chip is mounted to the top surface of the bottom package substrate, and
1[m]	the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

Claim 2:

2	The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

Claim 3:

3[a]	The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate,
3[b]	wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

Claim 4:

4	The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

Claim 5:

5[a]	The structure of claim 4, wherein the spacer connector is free of metal pads on the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate, and
5[b]	each metal pillar among the plurality of metal pillars and the corresponding top metal pad of the spacer connector form a T shape.

Claim 6:

6[a]	The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and
6[b]	bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of

	metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Claim 7:

7[a]	The structure of claim 4, wherein the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate, and
7[b]	the plurality of metal pillars pass through the core substrate and the dielectric layer.

Claim 8:

8	The structure of claim 7, wherein the dielectric layer is a dielectric adhesive in which the core substrate is pasted.

Claim 9:

9[a]	The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars,
9[b]	the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and
9[c]	bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

I. INTRODUCTION

The Office materially erred in granting U.S. Patent No. 9,859,202 ("the '202 Patent"). As Petitioners will address in detail in their brief regarding the discretionary institution factors, the Examiner overlooked the obviousness of "two spacer connectors" in a package-on-package ("PoP") structure, and the search was insufficient to locate highly relevant references. Grounds 1-9 teach every element of at least claim 1 of the '202 Patent, including the "two spacer connectors" limitation, either under Petitioners' construction (Grounds 1-8) or PO's overbroad construction (Ground 9).

II. REQUIREMENTS UNDER 37 C.F.R. 42.104

A. GROUNDS FOR STANDING

Petitioners certify under 37 C.F.R. § 42.104(a) that the '202 Patent is eligible for IPR and that Petitioners are not barred or estopped from requesting IPR on Grounds 1-9.

B. IDENTIFICATION OF CHALLENGE AND STATEMENT OF PRECISE RELIEF REQUESTED

This IPR, supported by the declaration of Mr. Peter Elenius (EX1003), asserts the following grounds of unpatentability:

Petitioners' or PO's Claim Interpretations	
Ground 1	*Sun* anticipates claims 1-4, 6-9
Ground 2	*Sun* renders obvious claims 1-4, 6-9
Ground 3	*Sun* with *Love* renders obvious claims 1-4, 6-9
Ground 4	*Sun* with *Hu* renders obvious claims 1-4, 6-9

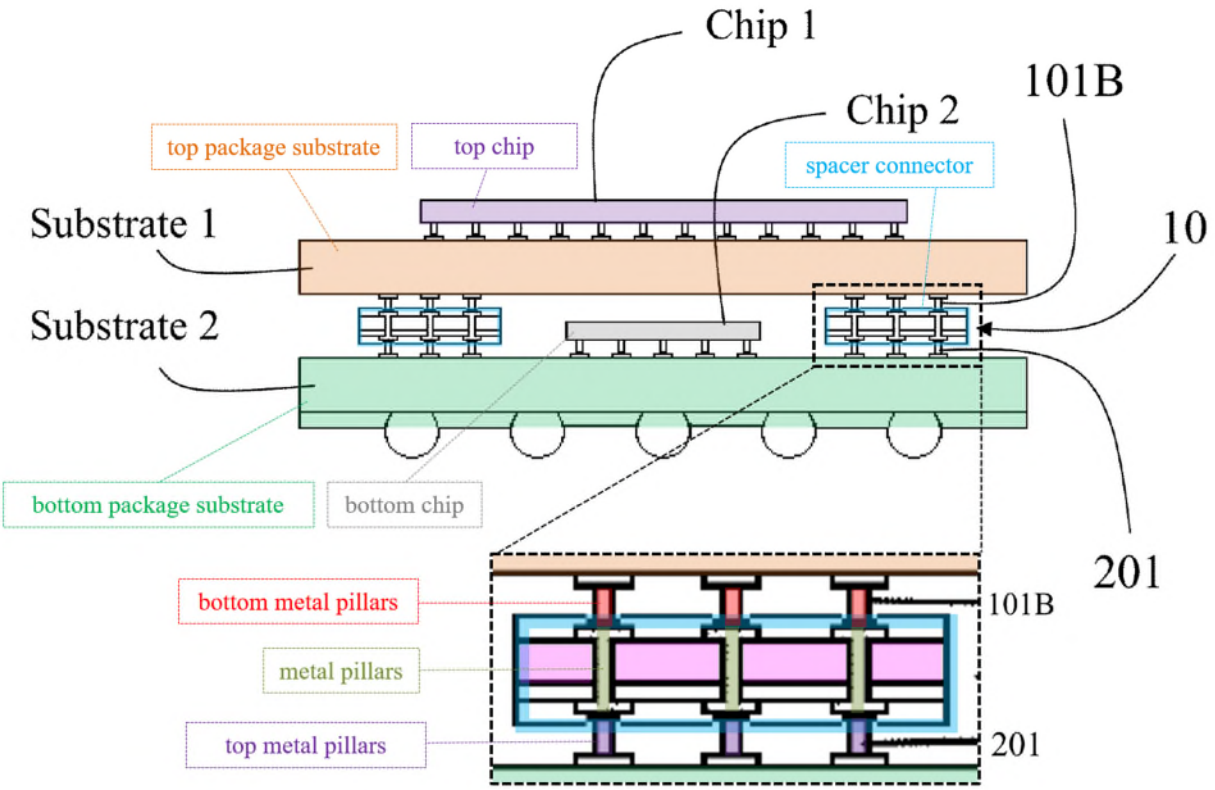
Ground 5	*Chen* anticipates claims 1-2, 4-9
Ground 6	*Chen* renders obvious claims 1-9
Ground 7	*Chen* with *Hu* renders obvious claims 1-9
Ground 8	*Chen* with *Hu* and *Benson* renders obvious claim 8
PO's Potential Claim Interpretations	
Ground 9	*Waite* with *IPC-4761* renders obvious claims 1-2, 4, 6, 9

III. '202 PATENT

A. SPECIFICATION

The '202 Patent shows a semiconductor packaging structure including spacer connectors 10 between a top (substrate 1) and bottom package substrate (substrate 2). EX1001, FIGs. 8, 11, 14; EX1003, ¶¶29, 47-62. Spacer connectors 10 include a core substrate 11 and metal pillars 15, which may protrude "below a bottom surface of the core substrate 11." EX1001, 2:51-53, FIGs. 7B, 10A. Metal pillars 15 are connected to bottom metal pillars 101B on the top package substrate and top metal pillars 201 on the bottom package substrate. *Id.*, 2:36-42, FIGs. 8, 11, 14. Metal pads 152 may also be used to connect these metal pillars. *Id*. Further, a top (chip 1) and bottom chip (chip 2) may be mounted on the top and bottom package substrates, respectively, while two spacer connectors 10 are arranged on opposite sides of the bottom chip. *Id.*, FIGs. 8, 11, 14.

Fig.8


Chip 1
101B
Chip 2
top package substrate
top chip
spacer connector
Substrate 1
10
Substrate 2
bottom package substrate
bottom chip
201
bottom metal pillars
101B
metal pillars
top metal pillars
201

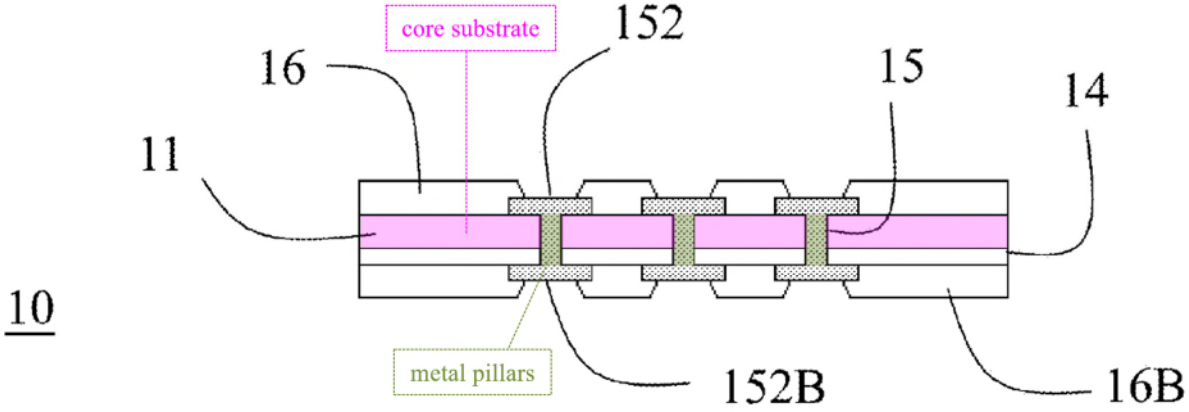

core substrate
152
16
15
14
11
10
metal pillars
152B
16B

Fig.7B

EX1001, FIGs. 8,[2] 7B.

B. FILE HISTORY

The ’202 Patent was filed on June 23, 2016 (Application No. 15/190,695), claiming priority to a provisional application filed on June 24, 2015. EX1001, Cover.

The Examiner rejected pending claims, finding U.S. Patent Publication No. 2008/0155820 to *Arai* (“*Arai*,” EX1013) disclosed many limitations ultimately included in the issued claims. EX1002, 100-04. For example, the Examiner determined *Arai*’s wiring board 20 disclosed “at least one spacer connector” (limitation 1[c]). *Id*., 100. The Examiner also found that *Arai*’s metal pillars (through-hole-conductive layer 14 with 16) connected via connection terminal 20a disclosed “metal pillars” being “connected, in an end-to-end manner, to…top metal pillars,” (limitation 6[a]) and that *Arai*’s “solder resists 18” were a “dielectric adhesive” (claim 8). EX1002, 101-02.

The applicant did not dispute these findings and the claims were allowed after adding the “bottom chip” ([1.k]-[1.l]) and “two spacer connectors” (1[m]) limitations that the Examiner deemed allowable over *Arai*. *Id*., 123-24, 151.

[2] All colored text/annotations in figures and emphasis in quotes are added unless noted.

IV. LEVEL OF ORDINARY SKILL IN THE ART

A Person of Ordinary Skill in the Art ("POSITA") at the time of the '202 Patent would have had either (i) a Master of Science in Electrical Engineering, Materials Science, Mechanical Engineering, or an equivalent field, or (ii) a Bachelor of Science in Electrical Engineering, Materials Science, Mechanical Engineering, or an equivalent field and two years of experience in the field of semiconductor packaging. EX1003, ¶¶74-75.

V. CLAIM CONSTRUCTION

Petitioners propose that all terms be given their ordinary and customary meaning and identify the following terms for construction, in view of potential differing interpretations.

A. "metal pillar" (1[e]-[j], 4-7, 9)

A POSITA would have understood "metal pillar" as "a columnar metal structure, such as a metal post or via." EX1003, ¶77. The claims recite "metal pillars" "passing through the core substrate" and "protrud[ing] downwardly from…the core substrate" indicating a columnar structure. EX1001, 3:42-43, 47-49. This structure cannot be realized by solder balls or other solder structures. EX1003, ¶77. Similarly, all metal pillars in the specification are illustrated as columnar metal posts or vias without a spherical/round shape of solder balls. *Id*.; EX1001, FIGs. 7A-B (copper pillar 15 as a via), 8 (bottom/top metal pillars 101B/201). These "metal pillars" are formed by an "electric plating process" (*id*., Abstract)—distinct from processes for

solder connections. EX1003, ¶¶77, 69-73. Prior art in the same field also identifies plating as a means to form metal pillars and distinguishes metal pillars from solder structures. EX1008, [0008] ("[M]etal posts are formed by electroplating."), [0004]-[0005] (explaining "metal posts…are used…to overcome the[] drawbacks" of "solder balls"); EX1006, [0014] (distinguishing "solder balls" and "metal pillars" as different types of interconnects); EX1014, 23-24, 31-33 (providing "solid metal pillar connections" to overcome the limitations of "solder balls"); EX1015, 2; EX1003, ¶¶77-79.

PO appears to take a broad and unsupported construction of "metal pillar," reading on solder structures on accused products, according to its Complaint. EX1004, ¶¶45-46; EX1003, ¶80. While all grounds in this Petition satisfy Petitioners' correct construction, alternative disclosures of the prior art are identified, where applicable, as meeting this claim limitation under PO's broad interpretation.

B. "package substrate" (1[a]-[c], 1[h]-[l], 2-4, 6, 9)

A POSITA would have understood "package substrate" to refer to a substrate that is part of a semiconductor package, that provides mechanical support and electrical interconnection with a semiconductor die, rather than a printed circuit board that assembles packaged chips and discrete electronic components. EX1003, ¶¶82-84. This interpretation is consistent with the '202 Patent's "Description of Related Art," identifying the subject as a popular topic "in the semiconductor

industry," relating to "nanotechnology." EX1001, 1:16-25. This description addresses die/chip level packaging and not a board-level assembly. EX1003, ¶¶82-83 (citing the usage of this term in the prior art); EX1006, [0019] ("a device die…bonded to a package substrate").

PO appears to take a broad and unsupported construction of "package substrate," reading on printed circuit board assemblies of the accused products, according to its Complaint. EX1004, ¶¶41-42; EX1003, ¶85. Ground 9 specifically addresses the invalidity of the '202 Patent claims under PO's broad construction. *See infra* §VII.G.

C. "bottom metal pillars of the top package substrate" and "top metal pillars of the bottom package substrate" (1[h]-[j], 4, 6, 9)—"of" terms

A POSITA would have understood the preposition "of" in the above terms indicates an association between the metal pillars and the package substrates—specifically, the bottom metal pillars are located on the bottom side of the top package substrate, and the top metal pillars are located on the top side of the bottom package substrate—but does not require the metal pillars be first constructed as part of the respective substrates.[3] EX1003, ¶86; EX1001, 2:1-5, 2:36-42, FIGs. 8, 11, 14. First, the '202 Patent claims are directed to a "structure," the limitations of which do

[3] This interpretation is consistent with PO's infringement read, which does not refer to any process steps of the accused products. EX1004, ¶¶45-46.

not require any manufacturing process or intermediate steps. EX1001, 3:32. Second, the claim language specifies the association between the metal pillars and respective substrates. EX1001, 3:49-51 (describing "bottom metal pillars" "on a bottom surface" of "the top package substrate"), 3:54-55 (describing "top metal pillars" "on a top surface" of "the bottom package substrate"). Third, the specification does not show or suggest the metal pillars are pre-assembled with the top or bottom substrates. EX1003, ¶87.

Petitioners present invalidity positions under both Petitioners' construction (Grounds 1-9) and a narrower construction that requires the pre-assembling of the metal pillars and respective substrates (Grounds 4, 7-8).

VI. SUMMARY OF PRIOR ART

Petitioners assume, without conceding, that claims 1-9 of the '202 Patent ("Challenged Claims") are entitled to a June 24, 2015 priority date and are subject to the AIA.

A. *SUN* (EX1005)

Sun was filed Dec. 17, 2009 and published June 23, 2011, and is prior art under 35 U.S.C. § 102(a)(1). *Sun* discloses a PoP assembly 1 in which second substrates 300 are disposed between a first substrate 110 and a third substrate 20, with chips 200/200a mounted on the first substrate, and the second substrates are disposed opposite sides of chips 200/200a. EX1005, [0061], FIG. 12.

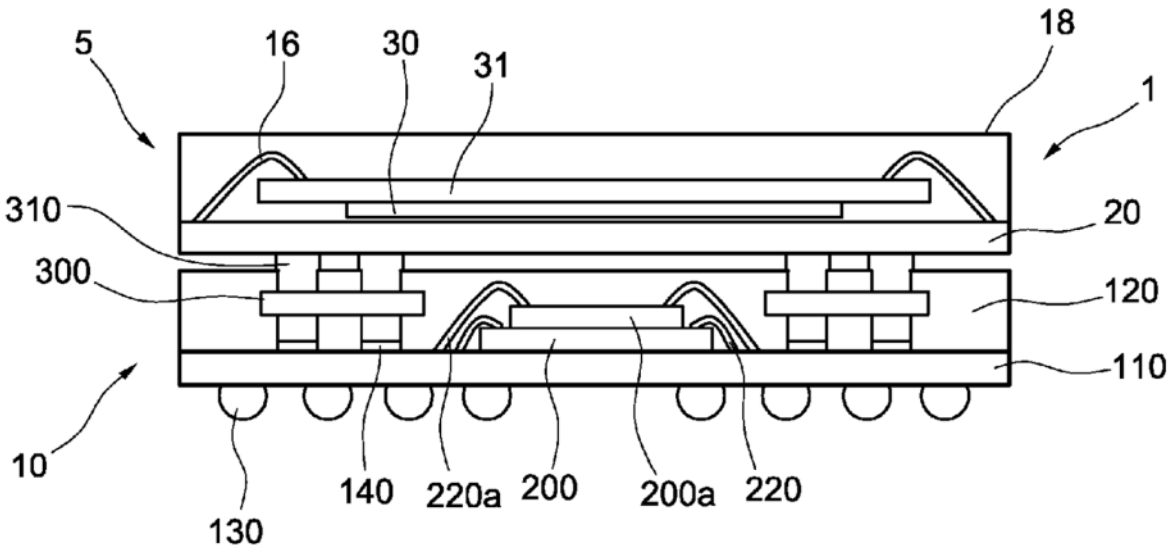


FIG.12

EX1005, FIG. 12.

B. *CHEN* (EX1006)

Chen was filed Jan. 18, 2012 and published July 18, 2013, and is prior art under 35 U.S.C. § 102(a)(1). *Chen* discloses a PoP structure in which top package component 62 is stacked on bottom package component 56 and electrically coupled through two TAV (Through-Assembly Via) modules 28 placed between the packages; package component 24 (including one or more device dies) is disposed between the packages. EX1006, [0008]-[0009], [0014], [0018]-[0019], FIG. 9:

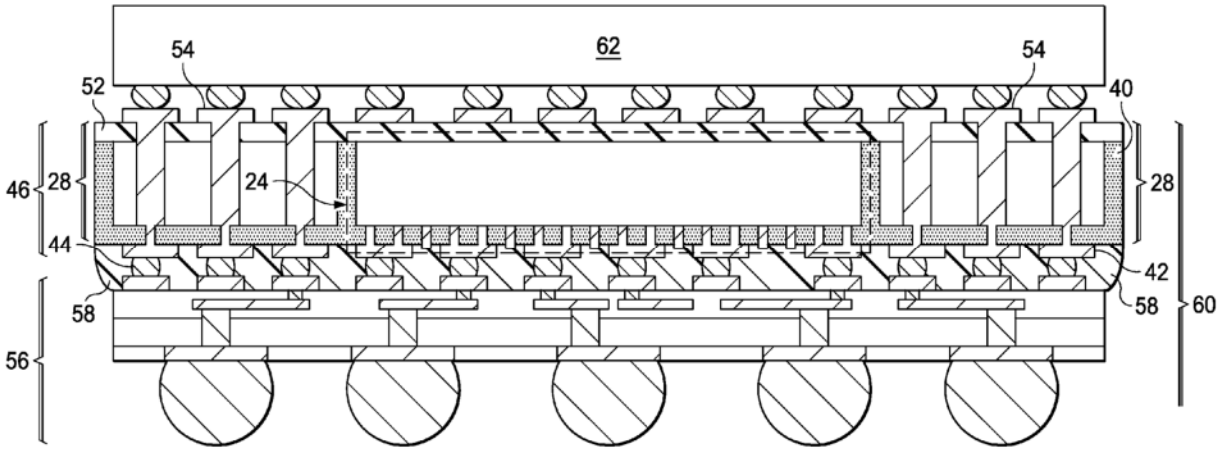


FIG. 9

C. *LOVE* (EX1007)

Love was filed Nov. 17, 1992 and issued Aug. 2, 1994, and is prior art under 35 U.S.C. § 102(a)(1). *Love* discloses interconnect structures for electrically and mechanically connecting an IC chip to a substrate, including conductive posts/pillars used to communicate signals and supply power. EX1007, 1:8-13, FIG. 5:

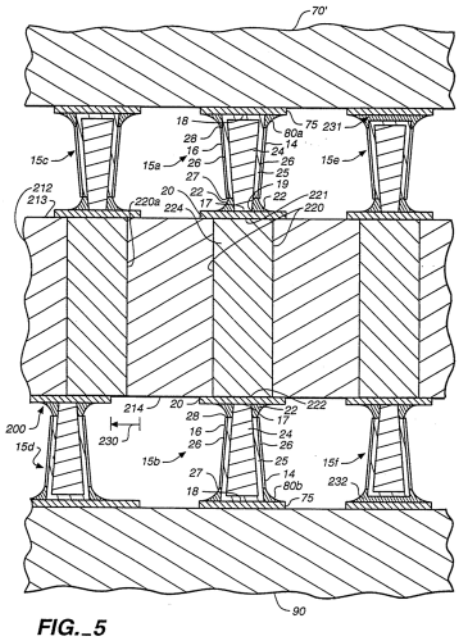


FIG._5

D. *HU* (EX1008)

Hu was filed Jan. 30, 2013 and published Sept. 26, 2013, and is prior art under 35 U.S.C. § 102(a)(1). *Hu* discloses a PoP structure using packaging substrates and external connection structures that include "metal posts," and teaches using metal posts in stack structures to overcome drawbacks of solder balls. EX1008, [0001], [0004]-[0005], [0010]-[0011], FIG. 3:

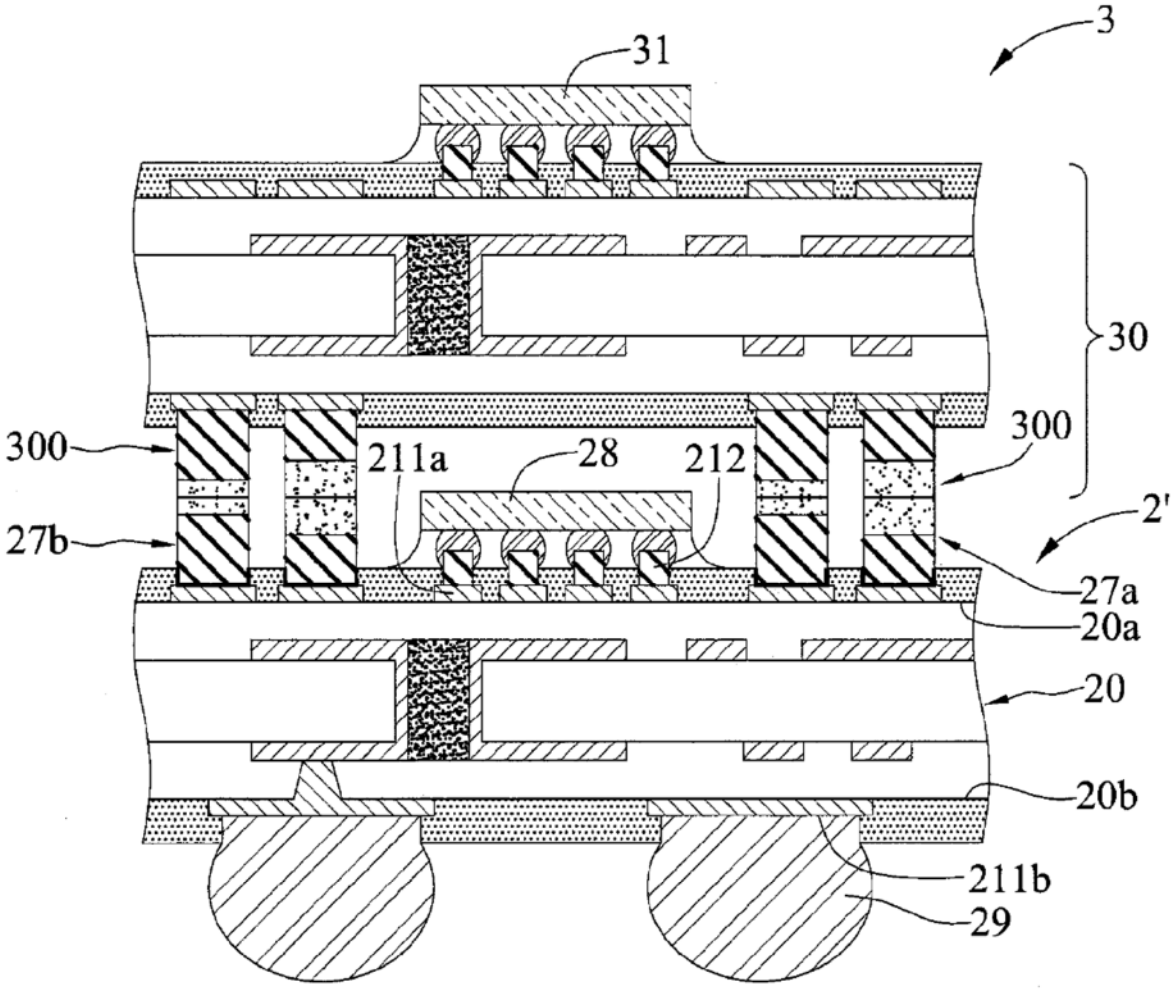


FIG.3

E. *BENSON* (EX1009)

Benson ("Polymer Adhesives and Encapsulants for Microelectronic Applications") was published in 2008 and is prior art under 35 U.S.C. § 102(a)(1). EX1012, ¶¶48-56. *Benson* discusses polymer materials used for die attachment, underfills, and encapsulants, and their properties. EX1009, 13.

F. *WAITE* (EX1010)

Waite was filed Mar. 30, 2010 and issued Feb. 19, 2013, and is prior art under 35 U.S.C. § 102(a)(1). *Waite* discloses a circuit board assembly including a spacer connector that interfaces between daughter boards and printed circuit boards. EX1010, 4:12-19, FIG. 4A:

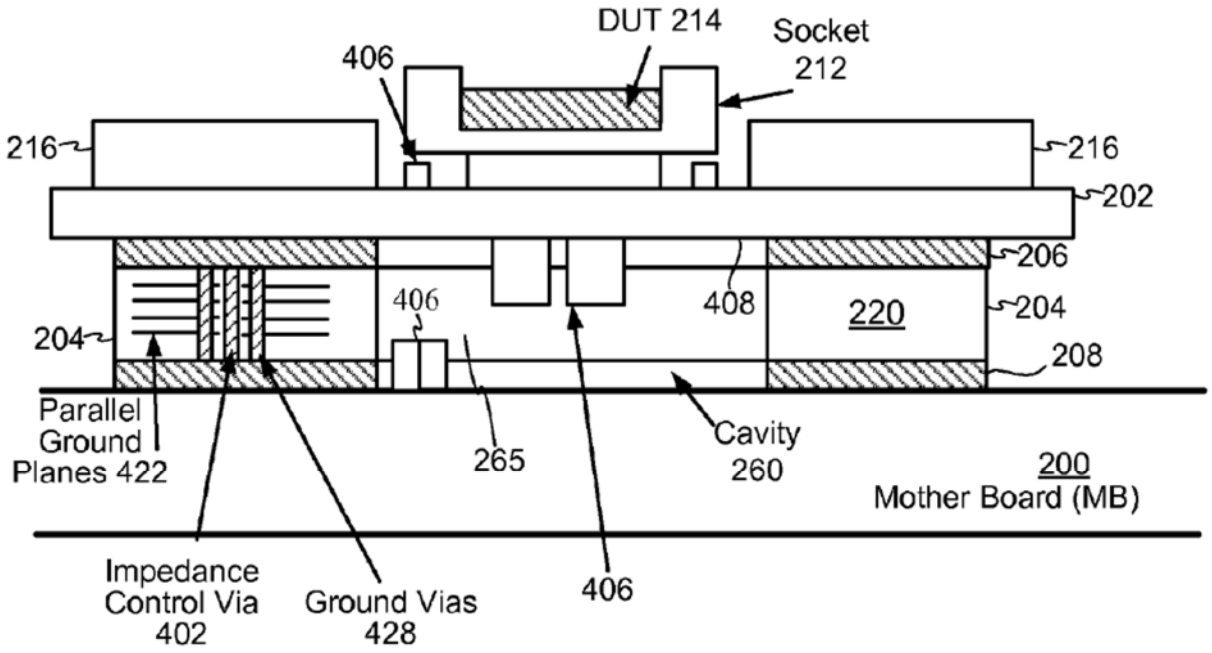


FIG. 4A

G. *IPC-4761* (EX1011)

IPC-4761 ("Design Guide for Protection of Printed Board Via Structures") was published July 2006 and is prior art under 35 U.S.C. § 102(a)(1). EX1012, ¶¶57-63. It is an IPC design guide providing printed wiring board designers/fabricators/users information on methods for protecting vias on printed boards. EX1011, 1, 7.

VII. INVALIDITY

A. GROUNDS 1-2: *SUN*

Sun anticipates and/or renders obvious claims 1-4 and 6-9.

i. Independent Claim 1

1[pre]

Sun discloses a "structure." *Sun*'s PoP assembly 1 is a semiconductor packaging structure, like that of the '202 Patent. EX1003, ¶¶110-11; EX1005, [0058], FIG. 12.

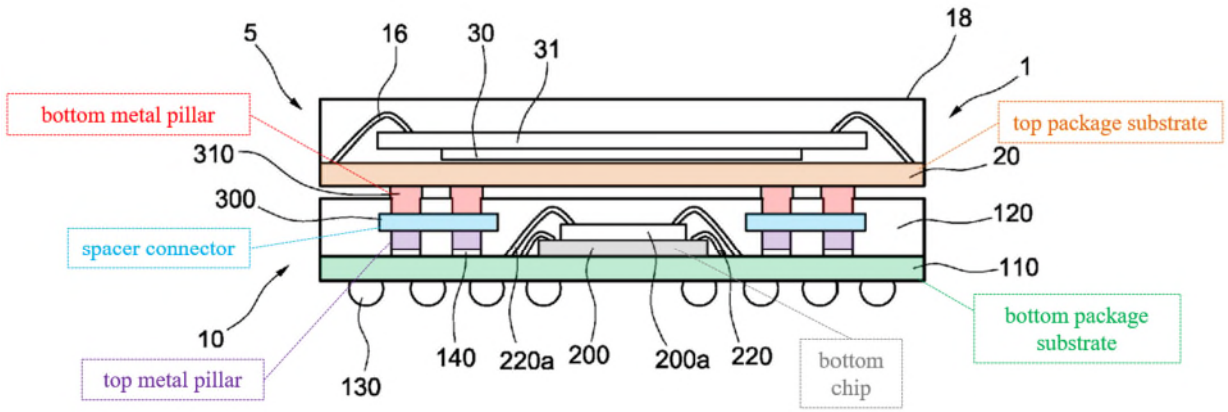
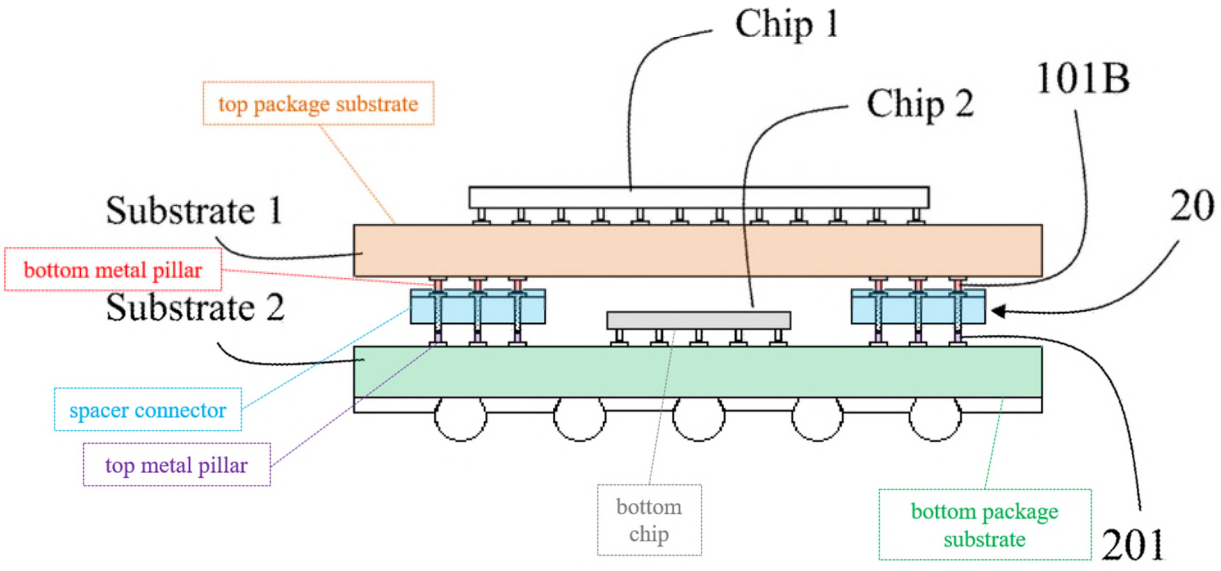


FIG.12

Fig.11



Compare EX1005, FIG. 12 (top) *with* EX1001, FIG. 11 (bottom).

1[a]

Sun discloses a first substrate 110 (bottom package substrate) of PoP assembly 1. EX1003, ¶¶112-13. The first substrate 110 directly interfaces with chip 200 (bottom chip) and a motherboard (not illustrated). EX1005, [0047]-[0048], FIG. 12:

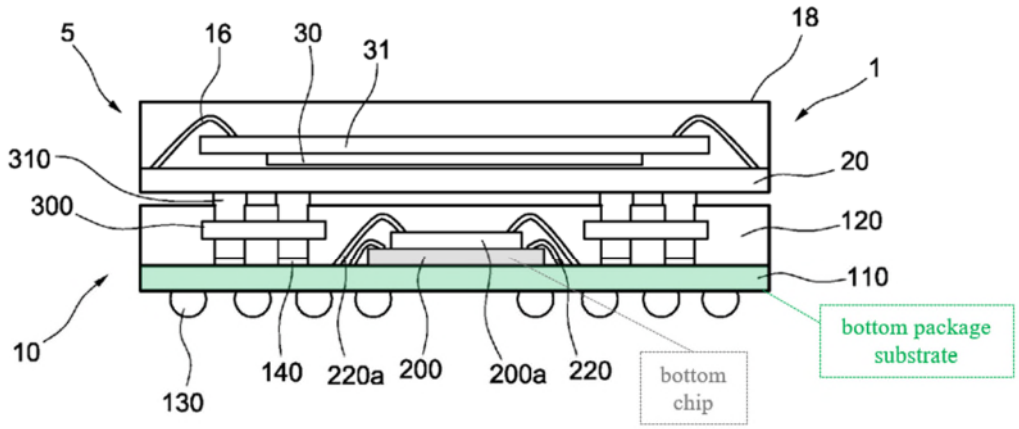


FIG.12

1[b]

Sun discloses a third substrate 20 (top package substrate) stacked on top of the first substrate 110 (bottom package substrate). EX1003, ¶¶114-15; EX1005, [0059], FIG. 12. The third substrate 20 interfaces with chips 30, 31 (top chips) and second substrates 300 (spacer connector). EX1005, [0059], FIG. 12:

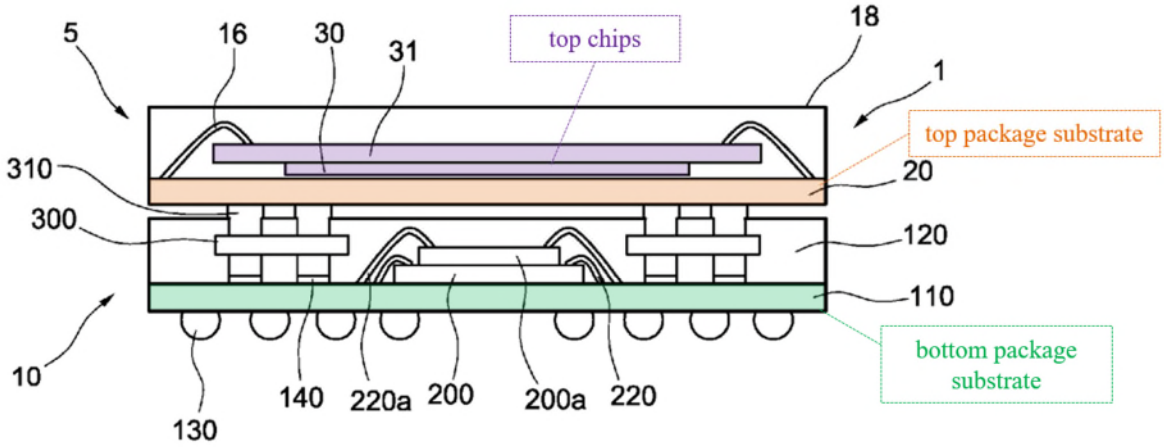


FIG.12

1[c]

Sun discloses second substrates 300 (spacer connectors) interposed between first substrate 110 (bottom package substrate) and third substrate 20 (top package substrate) to define a space between first substrate 110 and third substrate 20. EX1003, ¶¶116-17; EX1005, [0010], [0048], [0060]-[0061], FIG. 12:

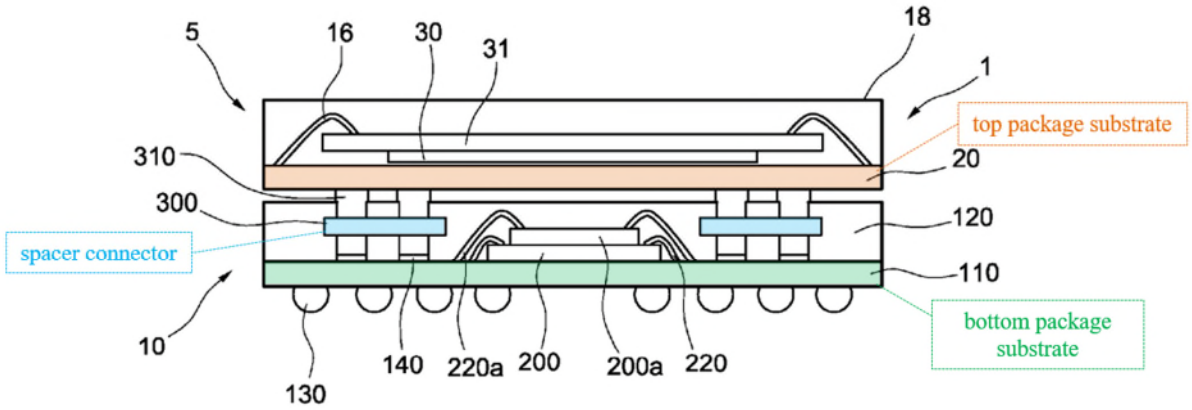


FIG.12

1[d]

Sun's second substrates 300 (spacer connectors) include a core/prepreg insulating layer 301 (core substrate). EX1005, [0016], [0065] ("the second substrate 300 comprises a core/prepreg insulating layer 301"), FIGs. 12, 15; EX1003, ¶¶118-19. The core/prepreg insulating layer 301 is an "insulating layer" which forms the core of the second substrate 300 (spacer connector). EX1003, ¶118; EX1005, [0016], [0065].

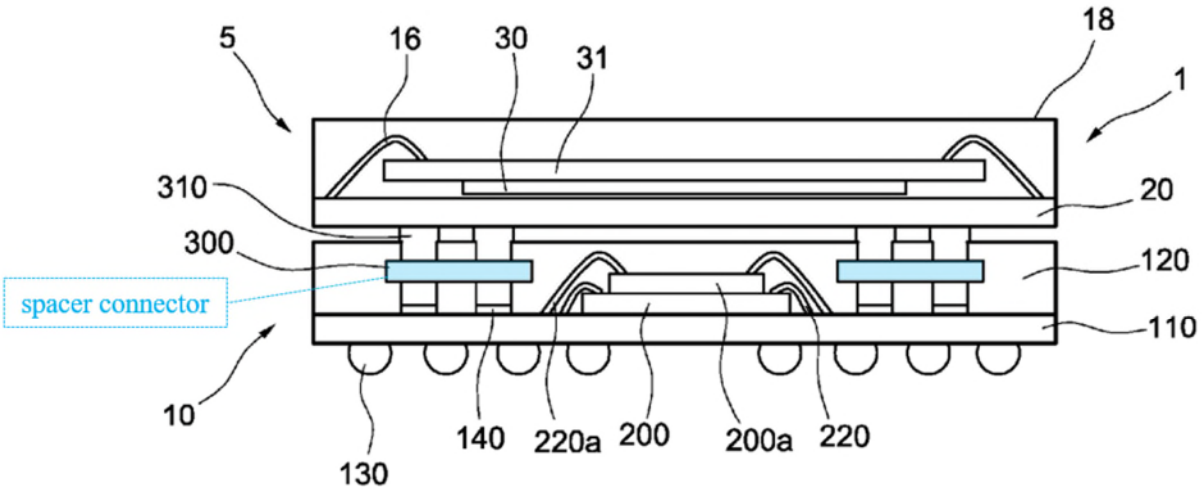


FIG.12

EX1005, FIG. 12.

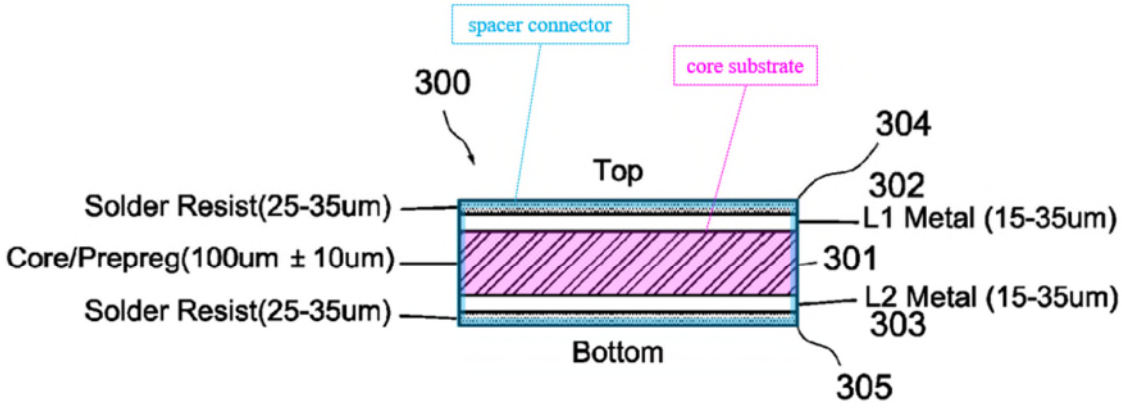


FIG.15

EX1005, FIG. 15.

1[e]

Sun's second substrates 300 (spacer connectors) include a plurality of vias 390 (metal pillars), each passing through the core/prepreg insulating layer 301 (core

substrate). EX1003, ¶¶120-21; EX1005, [0062]-[0063] ("vias 390 extend through the second substrate 300"), [0065], FIG. 13. Vias 390 are metal pillars (columnar metal structures) configured to electrically connect the third substrate 20 (top package substrate) and first substrate 110 (bottom package substrate). EX1003, ¶120; EX1005, [0017]-[0018], [0063]-[0064], FIG. 13[4]; *see also* §V.A.

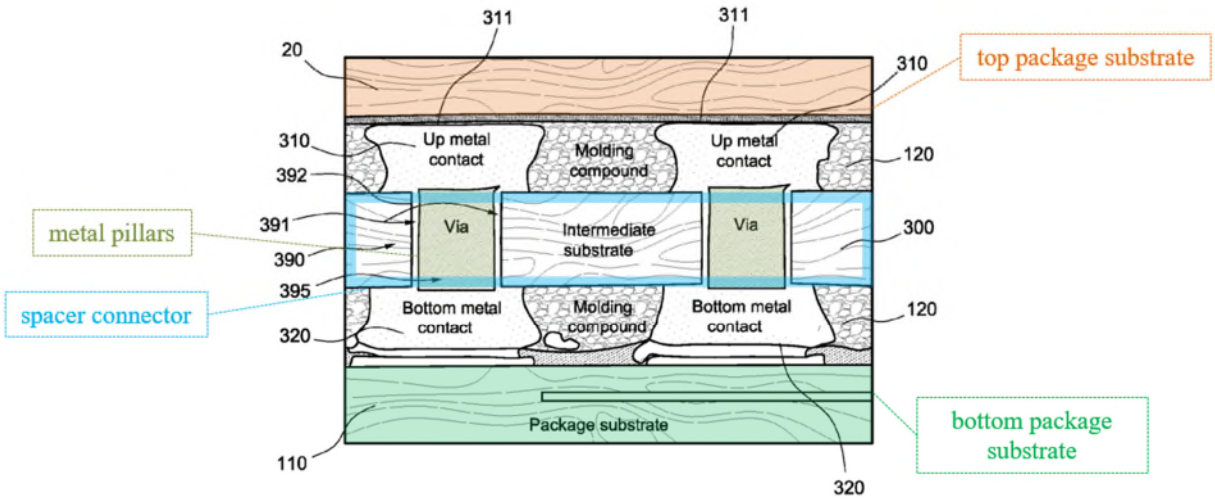


FIG.13

EX1005, FIG. 13.

1[f]

Sun's second substrates 300 (spacer connectors) include a plurality of bonding pads (top metal pads), each on a top end of a corresponding via 390 (metal pillar)

[4] *Sun*'s Figure 13 identifies first substrate 110 as "Package substrate" and second substrate 300 as "Intermediate substrate." EX1005, FIG. 13.

among the plurality of vias 390. EX1003, ¶¶122-30; EX1005, [0066], FIG. 14(a)[5]. Regarding the connection between third substrate 20 (top package substrate) and second substrates 300 (spacer connectors), *Sun* discloses that "bonding pads may [be] used to connect the metal pillars to the respective other substrates." EX1005, [0066]. These bonding pads are metal pads. EX1005, [0048] (stating that the metal connectors can be electrically connected to the substrates via "solder bonding or intermetallic bonding"), [0074] (identifying "bonding pads" as "electrical contacts"); EX1003, ¶123.

Figure 14(a) further illustrates this with a solid line highlighting the interface between the second metal connectors 310 (bottom metal pillars) and the bonding pads, which extend laterally over the second substrate 300 (spacer connector). EX1003, ¶¶124-25; EX1005, [0043], [0066], FIG. 14(a). The portion below this line corresponds to bonding pads disposed on the top end of each via 390. EX1003, ¶125.

[5] Vias 390 are omitted from Figure 14(a).

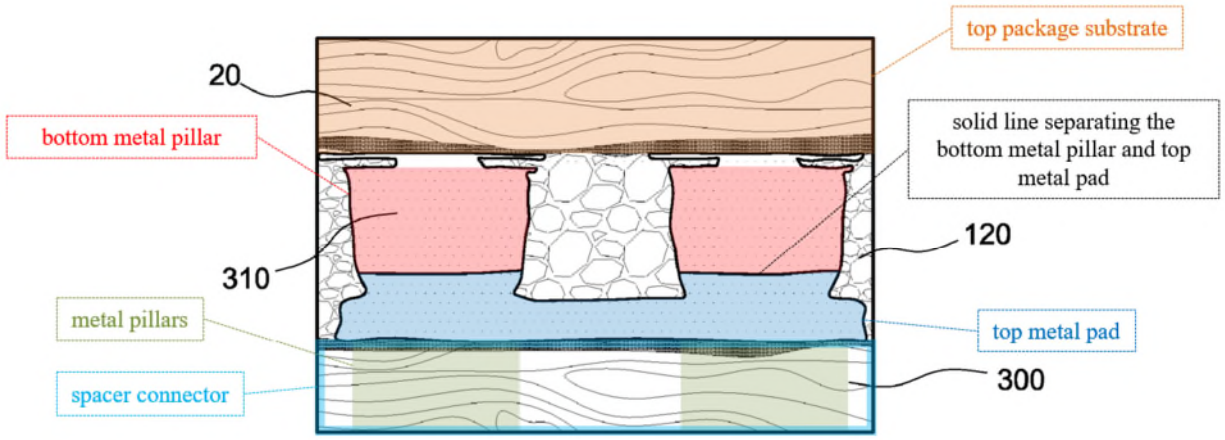


FIG.14(a)

EX1005, FIG. 14(a).

To the extent the Board disagrees that *Sun* explicitly discloses the claimed top metal pads, *Sun* renders this limitation obvious to a POSITA. EX1003, ¶¶126-29.

First, the structure of vias 390 requires a top metal pad to facilitate electrical connections, and a POSITA would have found it obvious to apply such pads. EX1003, ¶127. For example, vias 390 have sidewalls 310, 320 and a core 395. EX1005, [0063]-[0064], FIG. 13. The sidewalls are electrically conductive whereas the core can be an insulator or a void. EX1005, [0064]. As an insulator or void, core 395 is not solder-wettable and would not provide a suitable contact surface to facilitate an electrical connection between vias 390 and second metal connectors 310. EX1003, ¶127. It would have been obvious to apply metal pads to the top ends of vias 390 to connect to the conductive sidewalls and to provide a suitable surface to

facilitate an electrical connection between vias 390 and second metal connectors 310. EX1003, ¶127; *see also* EX1016, 95 ("[a] solder wettable surface like copper or nickel is needed to place solder bumps on"); EX1014, 33.

Second, applying metal pads on top of narrow vias 390 was known to provide the advantage of alleviating the need for precise alignment, and thus was an obvious design choice. EX1003, ¶128; EX1007, 13:12-41 (teaching wide pads can be applied to metal pillars to allow for misalignment errors).

Third, applying metal pads over vias was known to provide the benefit of preventing solder, solder resist, and other contaminants from flowing into the vias, which could inhibit the curing of bonding adhesives or result in corrosion of metal pillar sidewalls. EX1003, ¶129; EX1011, 8, 10, 13, 16; EX1005, [0064].

Accordingly, A POSITA would have found it obvious to apply top metal pads to the top ends of the metal pillars. EX1003 ¶¶126-30.

1[g]

Sun discloses the bottom end of each via 390 (metal pillar) protrudes downwardly from a bottom surface of the core/prepreg insulating layer 301 (core substrate). EX1003, ¶¶131-32. *Sun* teaches vias 390 "extend through" second substrate 300 (spacer connector), which includes core/prepreg insulating layer 301. EX1005, [0062]-[0063], [0065].

Additionally, *Sun*'s Figures 13 shows the vias 390 extend below the bottom surface of second substrate 300.

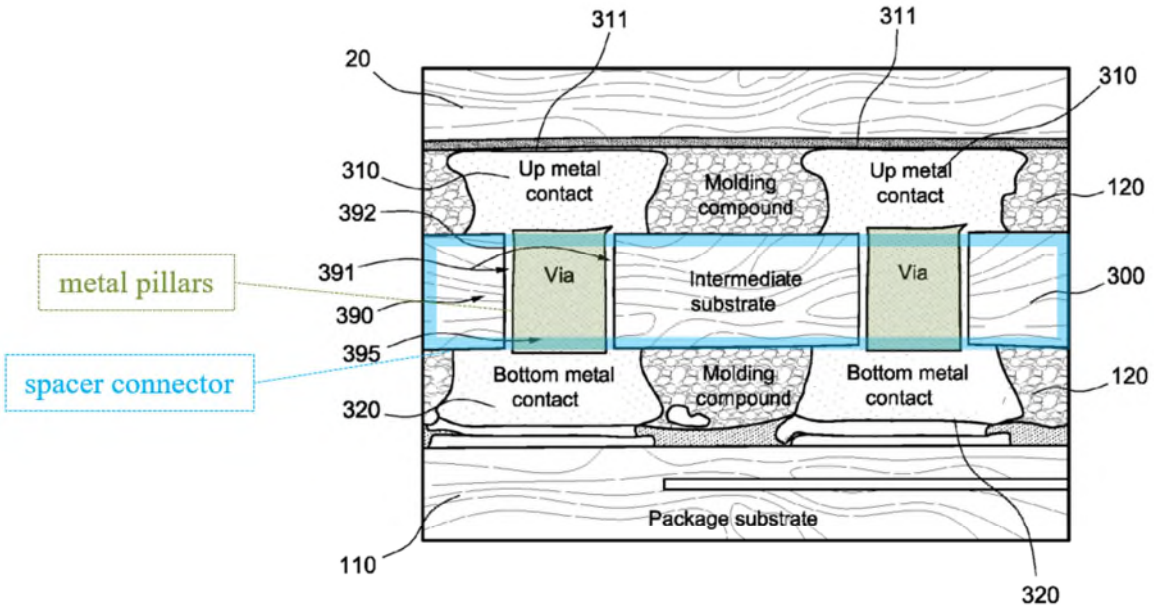


FIG.13

EX1005, FIG. 13.

Furthermore, given core/prepreg insulating layer 301 (core substrate) is a middle layer within second substrate 300, vias 390 must also protrude downwardly from a bottom surface of the core/prepreg insulating layer 301, as shown in FIGs. 13, 15 below. EX1005, [0065]; EX1003, ¶131; *see also In re Mraz*, 455 F.2d 1069 (CCPA 1972) ("[d]rawings and pictures can anticipate claims if they clearly show the structure which is claimed"); MPEP §2125.

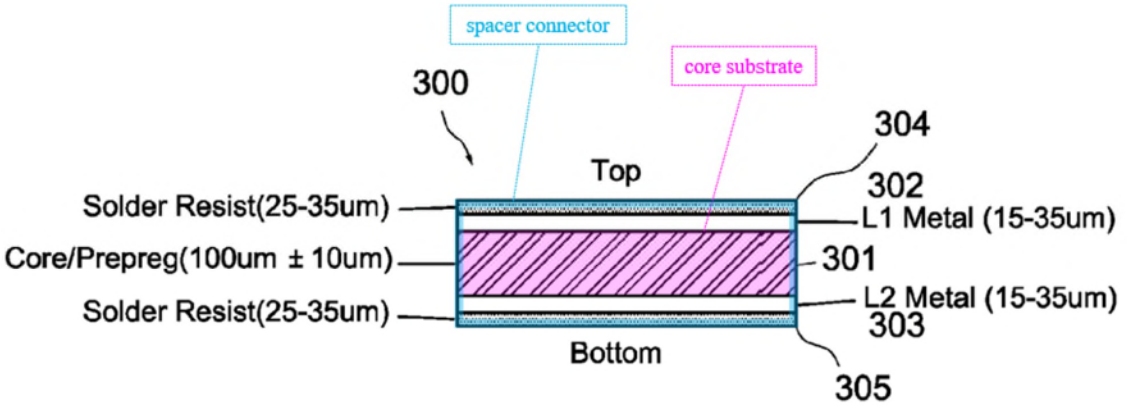


FIG.15

EX1005, FIG. 15.

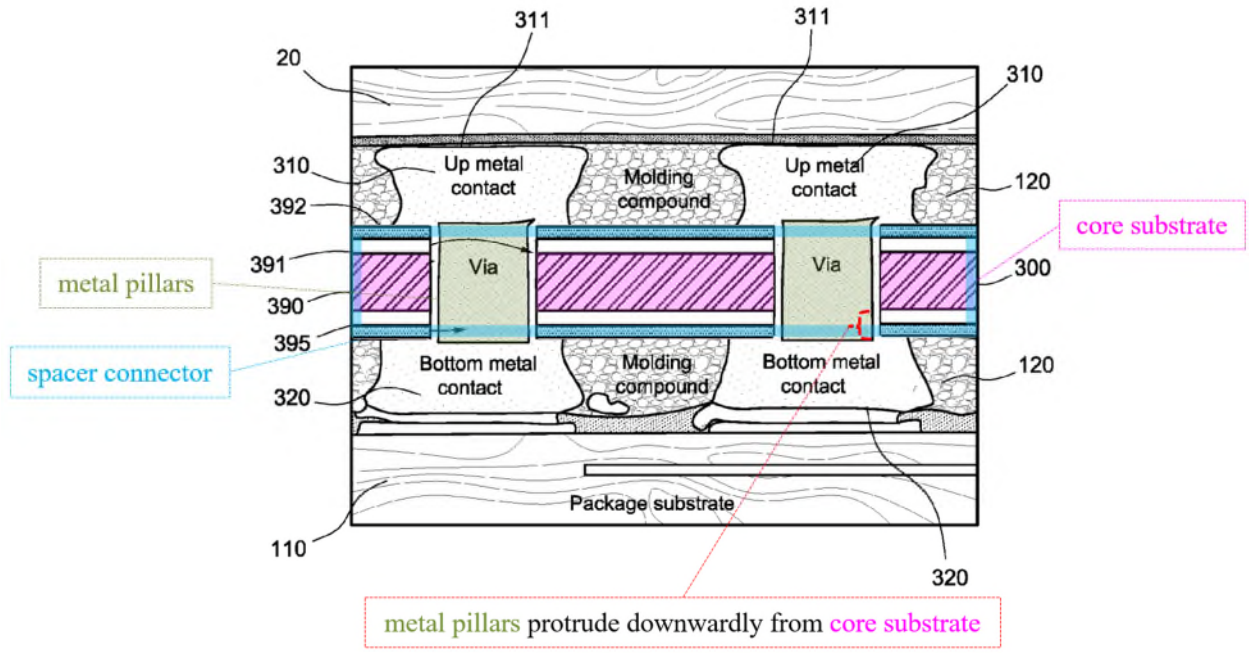


FIG.13

EX1005, FIG. 13 (FIG. 15 superimposed thereon).

1[h]

Sun discloses the third substrate 20 (top package substrate) has, on a bottom surface thereof, a plurality of second metal connectors 310 (bottom metal pillars), each coupled to a corresponding via 390 (metal pillar) among the plurality of vias 390 of second substrate 300 (spacer connector). EX1003, ¶¶133-34; EX1005, [0063] ("Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320."), [0015] ("Preferably the first and second electrical connectors are metal pillars, e.g. copper pillars…[and] solder joints may be used to join the metal pillars to a substrate above or below."), FIG. 13:

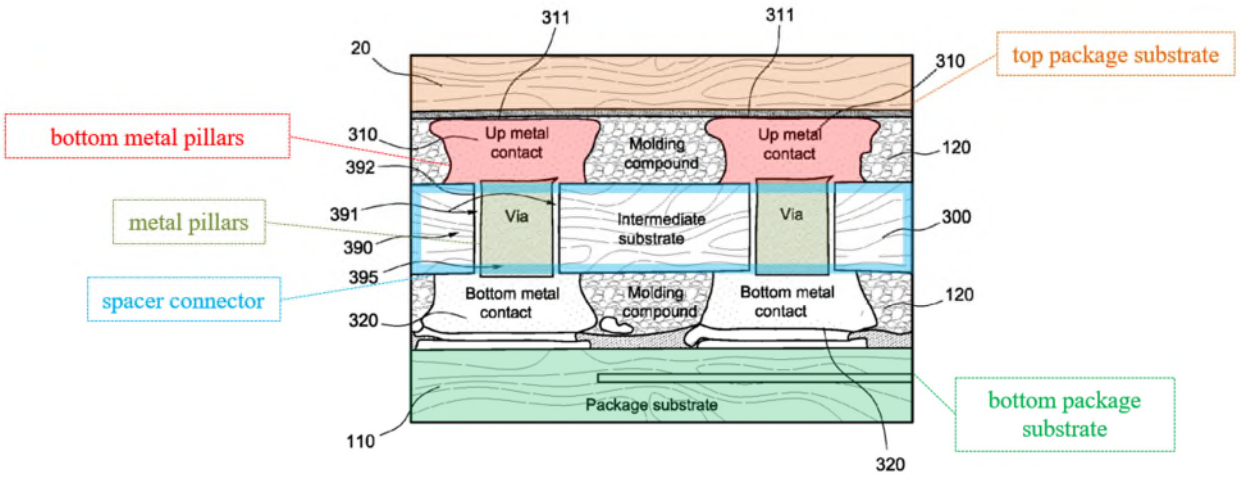


FIG.13

1[i]

Sun discloses the first substrate 110 (bottom package substrate) has, on a top surface thereof, a plurality of first metal connectors 320 (top metal pillars) each coupled to a corresponding via 390 (metal pillar) among the plurality of vias 390 of second substrate 300 (spacer connector). EX1003, ¶¶135-36; EX1005, [0063], [0015], FIG. 13:

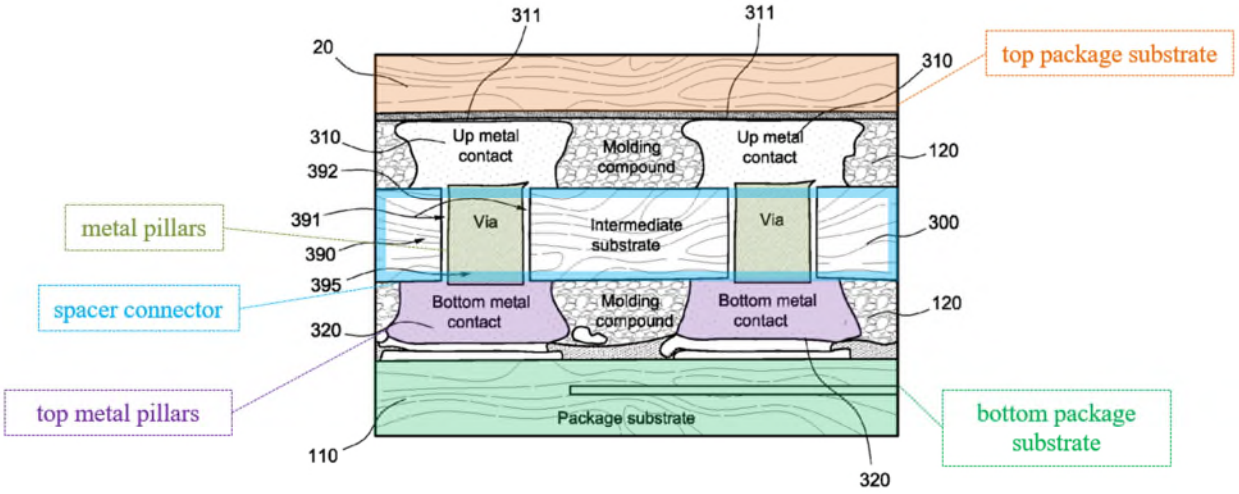


FIG.13

1[j]

Sun discloses the third substrate 20 (top package substrate) is electrically coupled to the first substrate 110 (bottom package substrate) through the plurality of the second metal connectors 310 (bottom metal pillars) of the third substrate 20, the plurality of vias 390 (metal pillars) of second substrate 300 (spacer connector), and

the plurality of the first metal connectors 320 (top metal pillars) of the first substrate 110. EX1003, ¶¶137-41; EX1005, [0013], [0015], [0061] ("The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110."), [0063] ("Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320."), [0074] ("[E]lectrical contacts (e.g. bonding pads or lands) present on the second (lower) side of the third substrate are placed in contact with the exposed ends of the second electrical connectors 310 of the first module 10."), FIG. 13:

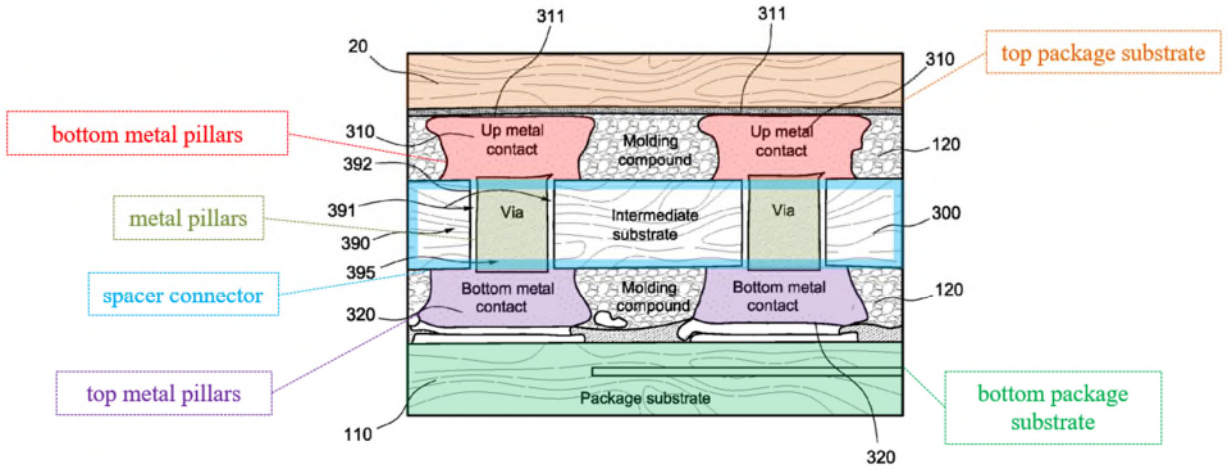


FIG.13

As discussed in §V.C above, because first metal connector 320 (top metal pillars) and second metal connector 310 (bottom metal pillars) are associated with (on the surface of) the bottom package substrate and the top package substrate,

respectively, the "bottom metal pillars of the top package substrate" and "top metal pillars of the bottom package substrate" limitations are both met. EX1003, ¶140.

1[k]

Sun discloses a chip 200 (bottom chip) arranged in the space between the first substrate 110 (bottom package substrate) and the third substrate 20 (top package substrate). EX1003, ¶¶142-43; EX1005, [0060]-[0061] ("A pair of chips 200, 200a…are mounted to the first substrate 110…."), FIG. 12:

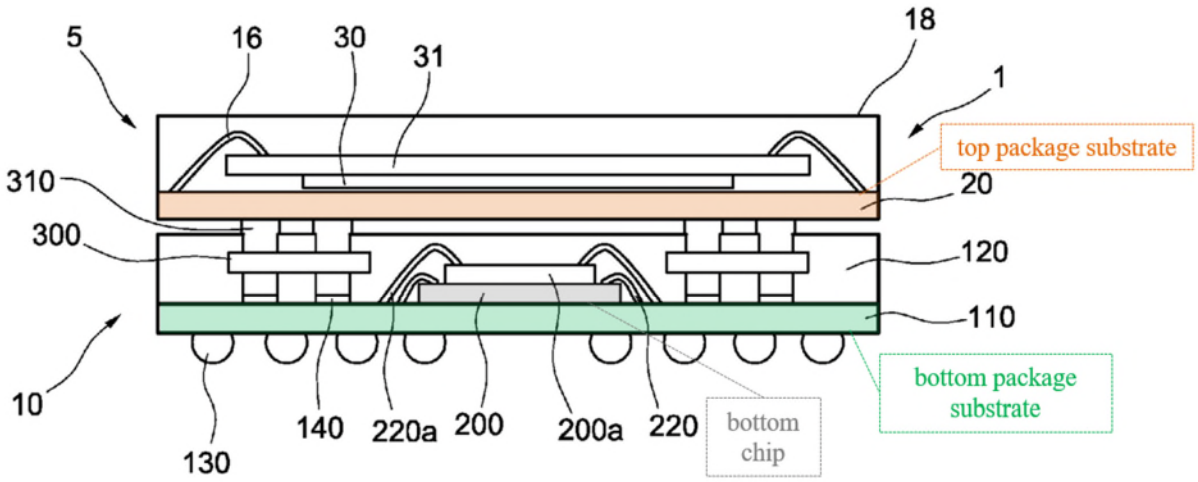


FIG.12

1[l]

Sun discloses chip 200 (bottom chip) is mounted to the top surface of first substrate 110 (bottom package substrate). EX1003, ¶¶144-45; EX1005, [0060] (chip 200 is "mounted to the first substrate 110"), FIG. 12:

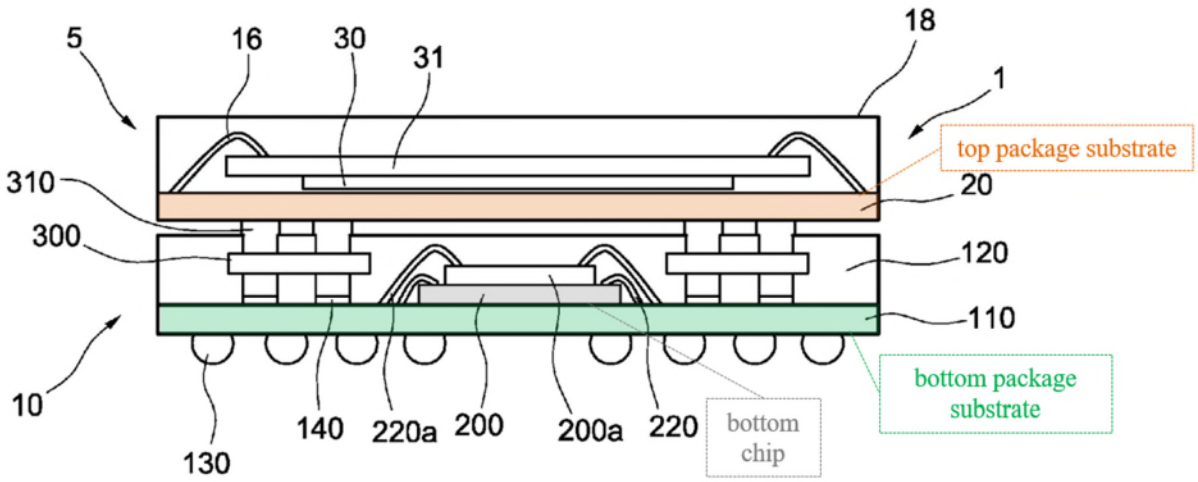


FIG.12

1[m]

Sun discloses two second substrates 300 (spacer connector) arranged on opposite sides of chip 200 (bottom chip). EX1003, ¶¶146-47. *Sun* teaches "[t]he second substrate [300] has an opening therein for accommodating the chips 200, 200a," and each side of the second substrate (spacer connector) "has a gap" "join[ing] the central opening." EX1005, [0061], [0055], [0059], FIGs. 9, 12. As illustrated in *Sun*'s Figures 9 and 12, these "opening" and "gaps" lead to two spacer connectors arranged on opposite sides of the bottom chip. EX1003, ¶146.

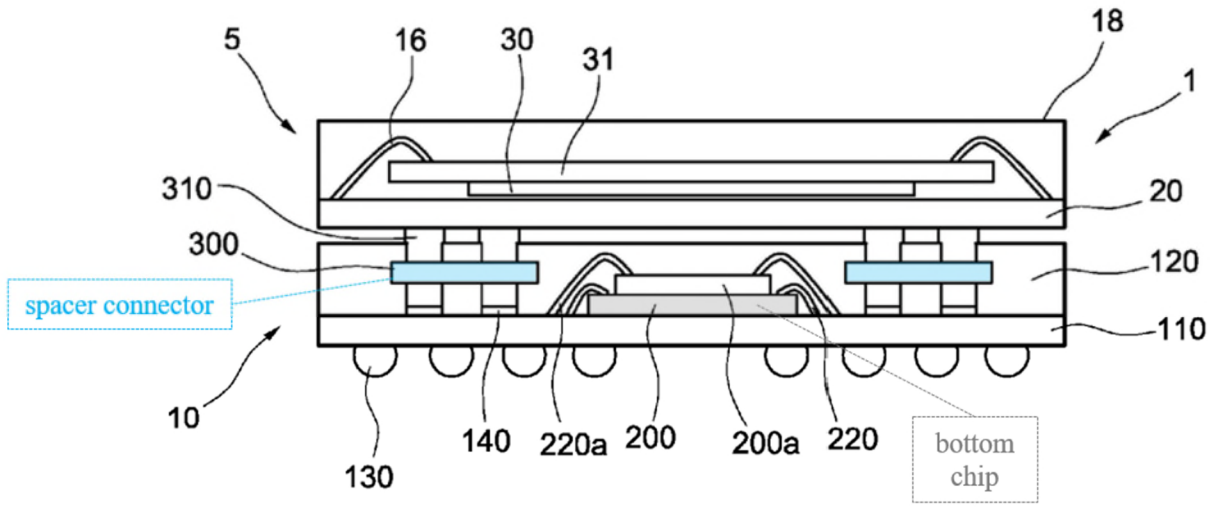


FIG.12

EX1005, FIG. 12.

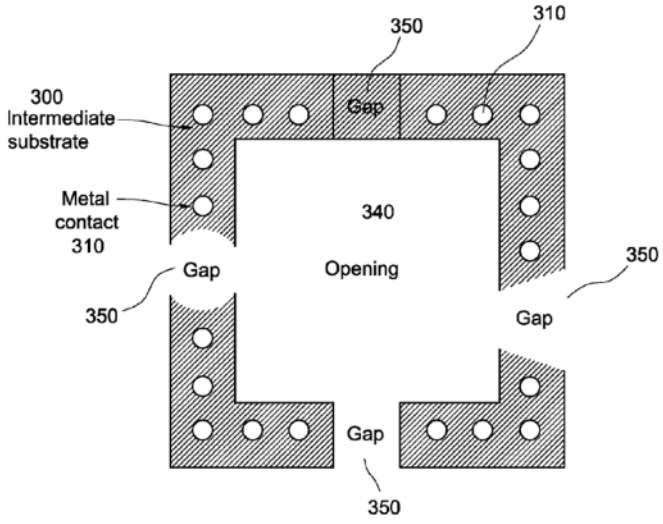


FIG.9

EX1005, FIG. 9.

ii. Dependent Claims 2-4 and 6-9

Claim 2

Sun discloses the top surface of chip 200 (bottom chip) is spaced downwardly from the bottom surface of third substrate 20 (top package substrate). EX1003, ¶¶148-49; EX1005, [0060]-[0061], FIG. 12:

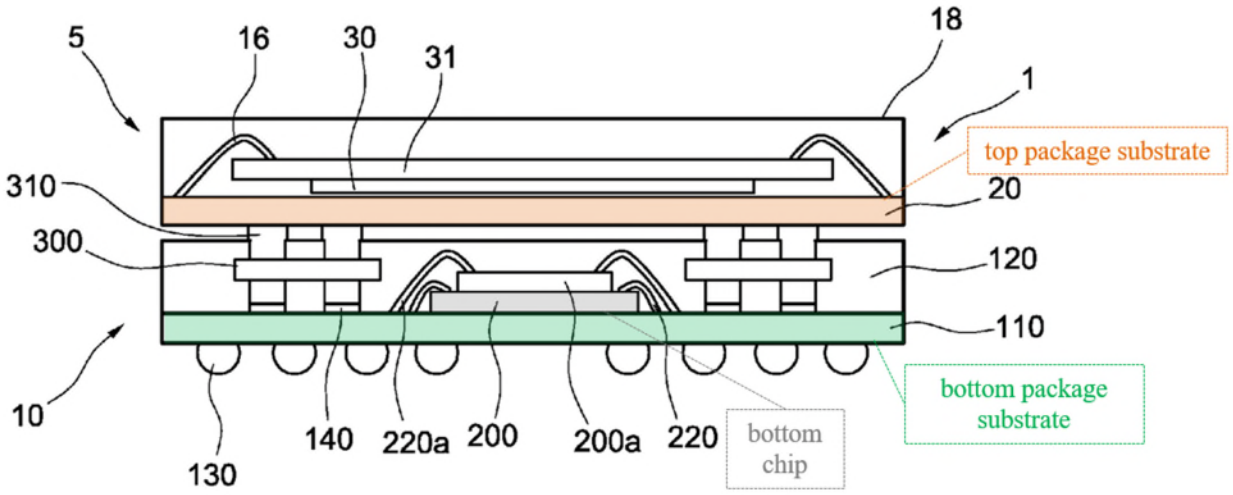


FIG.12

Claim 3[a]

Sun discloses chips 30, 31 (top chips) mounted to the top surface of the third substrate 20 (top package substrate). EX1003, ¶¶150-51; EX1005, [0059] (chips 30, 31 are "mounted to a first (upper) side of a third substrate 20."), FIG. 12:

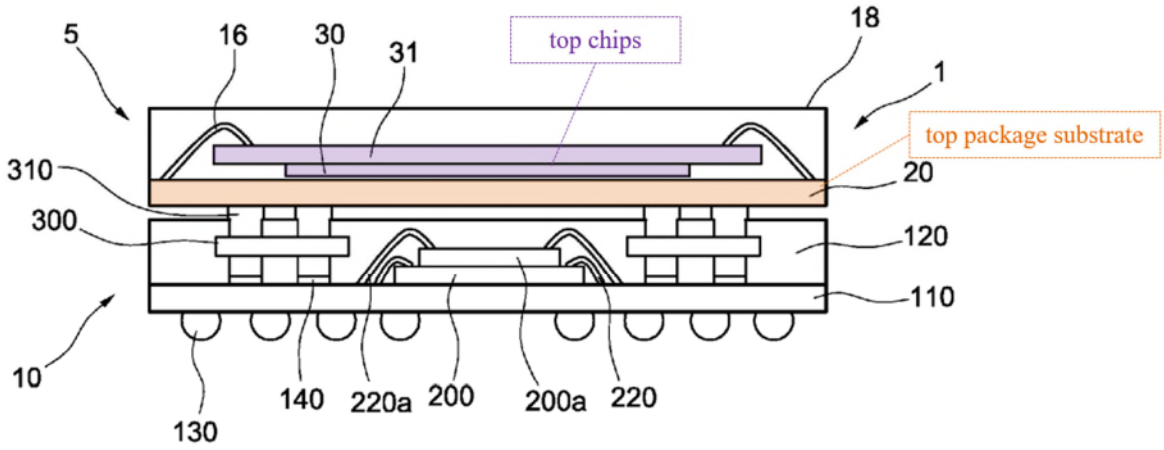


FIG.12

Claim 3[b]

Sun discloses that in a vertical direction in which the third substrate 20 (top package substrate) is stacked on top of the first substrate 110 (bottom package substrate), chips 30, 31 (top chips) overlap chip 200 (bottom chip) and each of the two second substrates 300 (spacer connector). EX1003, ¶¶152-54; EX1005, FIG. 12.

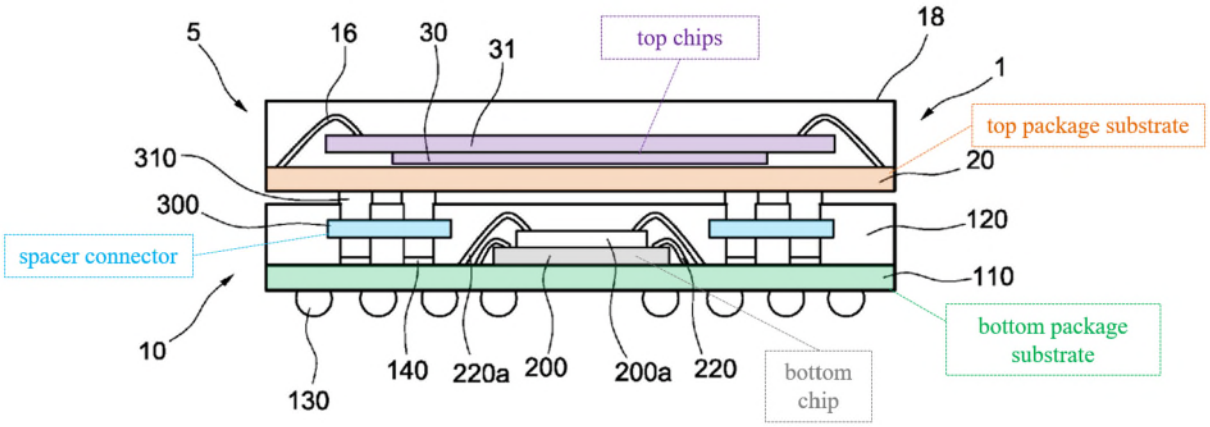
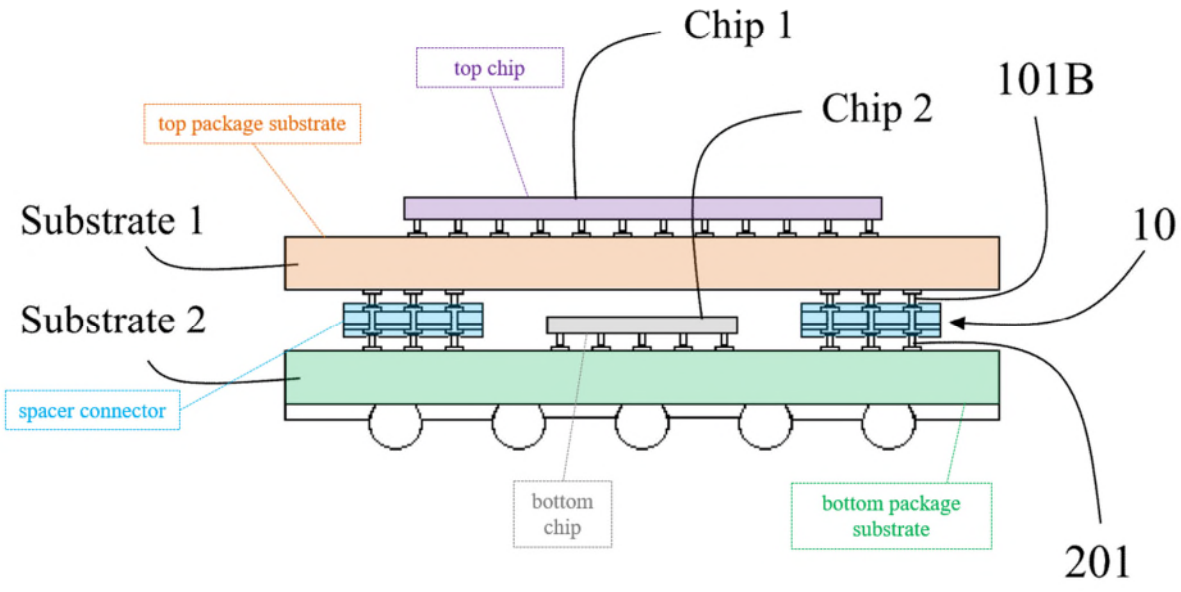


FIG.12

Compare EX1005, FIG. 12 *with* EX1001, FIG. 8:

Fig.8



Claim 4

Sun discloses each second metal connector 310 (bottom metal pillar) among the plurality of second metal connectors 310 of the third substrate 20 (top package substrate) is aligned with a corresponding via 390 (metal pillar) among the plurality of vias 390 of the second substrate 300 (spacer connector), and with a corresponding first metal connector 320 (top metal pillar) among the plurality of first metal connectors 320 of the first substrate 110 (bottom package substrate). EX1003, ¶¶155-56; *see also* §VII.A.i.(1[j]).

Sun teaches that "[t]he second metal connectors 310 are aligned with corresponding [first metal connectors 320] on the opposite side of the substrate 300"[6] and the "[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320." EX1005, [0062]-[0063]. For this electrical connection, each via 390 is aligned with a corresponding second metal connector 310 and first metal connector 320. EX1003, ¶155; EX1005, [0062]-[0063], FIG. 13:

[6] Corrected an apparent typo. EX1003, ¶155; EX1005, FIG. 12.

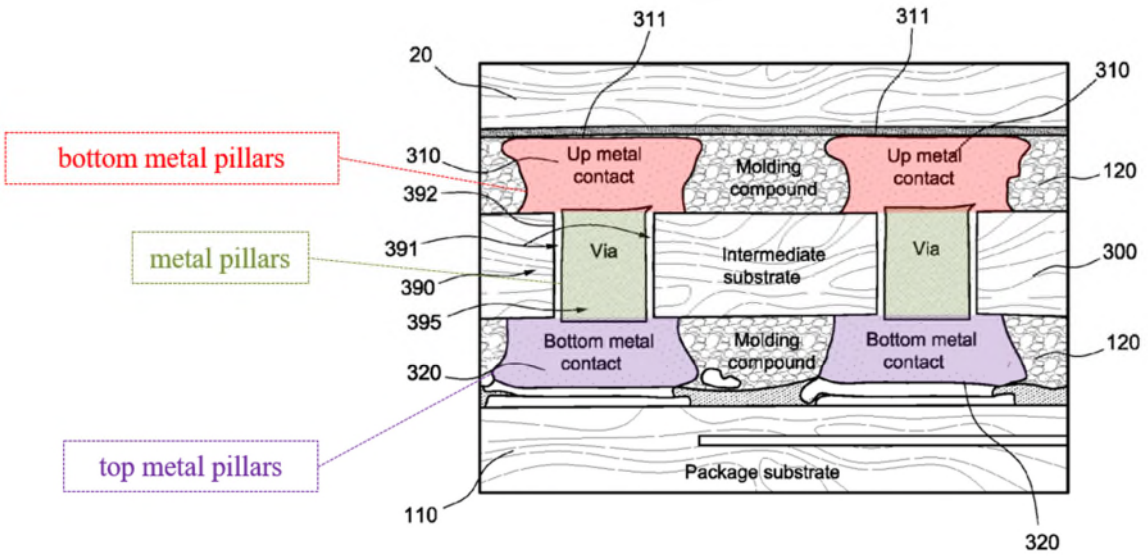


FIG.13

Claim 6[a]

As discussed above, *Sun* discloses the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector. §VII.A.i.(1[g]). Additionally, *Sun* discloses the bottom ends of vias 390 (metal pillars) are connected, in an end-to-end manner, to corresponding top ends of the plurality of first metal connectors 320 (top metal pillars) of first substrate 110 (bottom package substrate).[7] EX1003, ¶¶157-58; EX1005, [0063] ("Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320."), FIG. 13:

[7] This interpretation is consistent with PO's infringement allegations, which rely on vias with capped bottom ends to meet the "end-to-end" requirement. *See, e.g.*, EX1004, ¶44 (p.16).

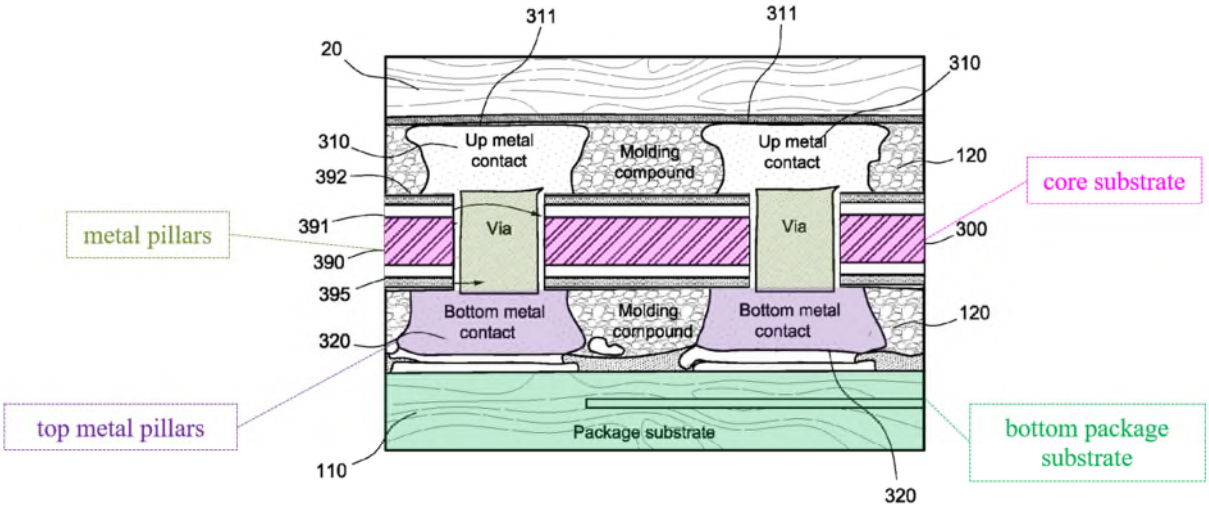


FIG.13

Claim 6[b]

Sun discloses and/or renders obvious the bottom ends of the plurality of second metal connectors 310 (bottom metal pillars) of third substrate 20 (top package substrate) are connected to the corresponding top ends of the plurality of vias 390 (metal pillars) of second substrate 300 (spacer connector) via the corresponding bonding pads (top metal pads) of second substrate 300. EX1003, ¶¶159-60; *see also* §§VII.A.i.(1[f]), VII.A.i.(1[j]). As discussed in §VII.A.i.(1[f]), *Sun* discloses or otherwise renders obvious bonding pads (top metal pads) on the top end of each via 390. Figure 14(a) shows the bottom end of each second metal

connector 310 is connected to a bonding pad disposed on a top end of each corresponding via 390.[8] EX1003, ¶159; EX1005, FIG. 14(a):

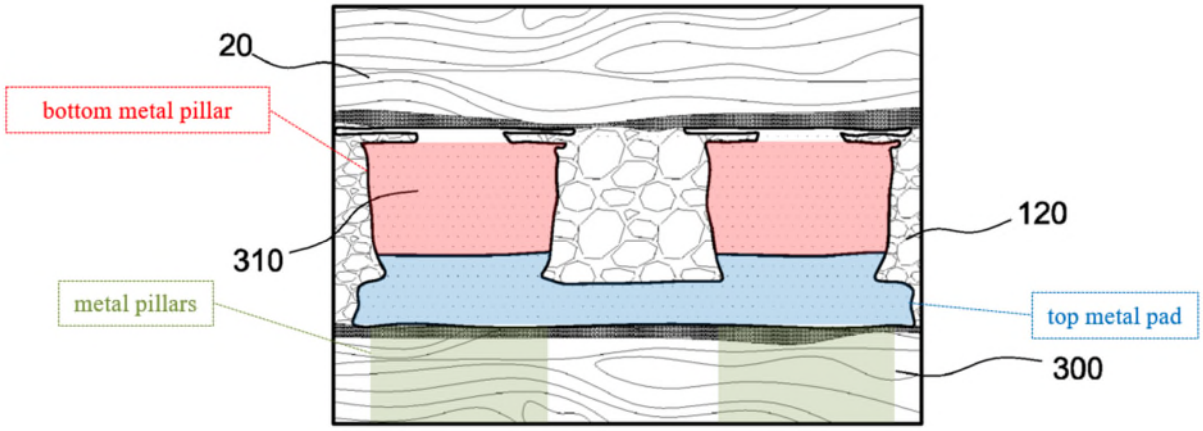


FIG.14(a)

Claim 7[a]

Sun's second substrates 300 (spacer connectors) include a solder resist layer 305 (dielectric layer) on a bottom surface of the core/prepreg insulating layer 301 (core substrate). EX1003, ¶¶161-63; EX1005, [0065] ("the second substrate 300 comprises a core/prepreg insulating layer 301, a metal layer 302, 303 on either side of the core layer and an ***insulating*** solder resist layer 304, 305 on either side of the

[8] While FIG. 14(a) does not show vias 390, they are illustrated in FIG. 13, showing the bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector. EX1003, ¶159; EX1005, FIG. 13.

metal layers."), FIG. 15 (showing solder resist layer 305 is disposed on a bottom surface of core/prepreg insulating layer 301):[9]

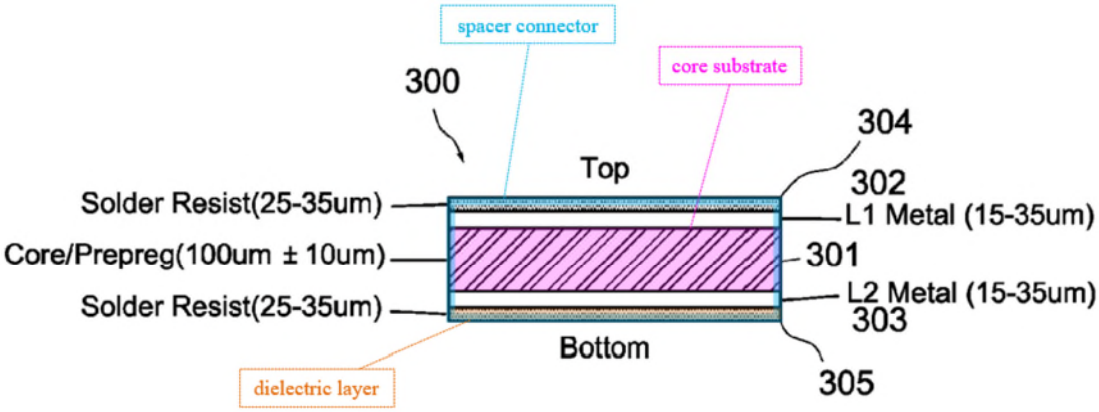


FIG.15

Claim 7[b]

The plurality of vias 390 (metal pillars) pass through the core/prepreg insulating layer 301 (core substrate) and the solder resist layer 305 (dielectric layer). EX1003, ¶¶164-65. *Sun*'s "vias 390 extend through the second substrate 300," which includes both core/prepreg insulating layer 301 and solder resist layer 305. EX1005, [0063], [0065]; *see also id.*

[9] The claim does not require the dielectric layer to be "directly on" the bottom surface of the core substrate. Accordingly, *Sun*'s solder resist layer 305 is "on" the bottom surface of core/prepreg insulating layer 301, as required by limitation 7[a]. EX1003, ¶¶162-63 (noting that at least a portion of the solder resist will be directly on the core substrate).

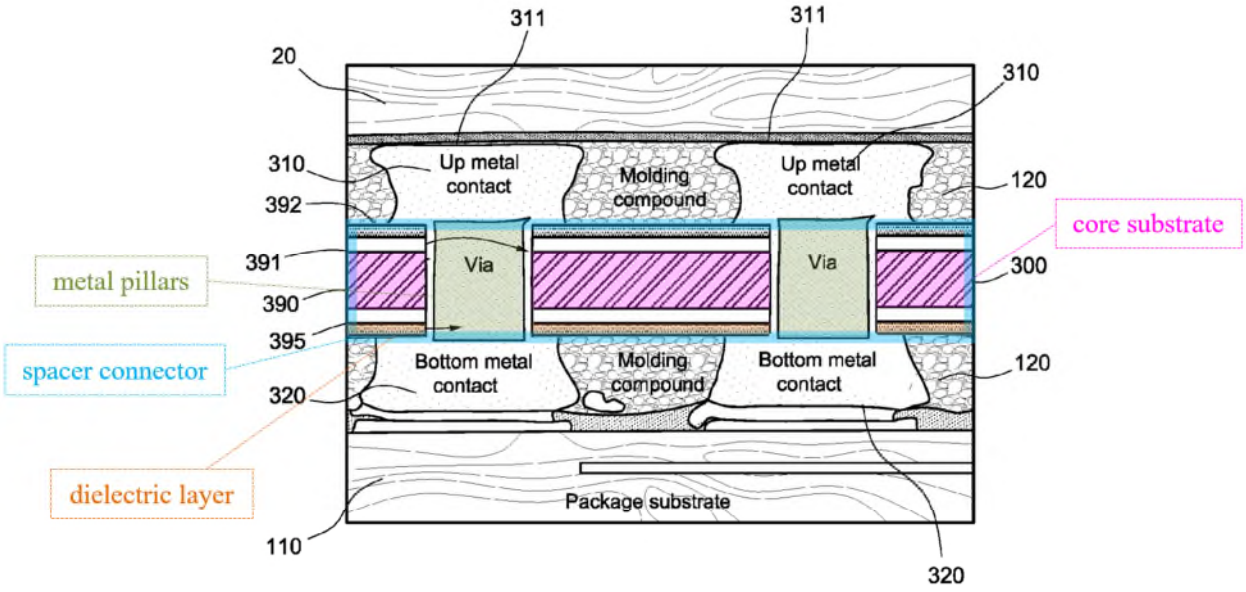


FIG.13

EX1005, FIG. 13 (annotated with FIG. 15 superimposed thereon).

Claim 8

Sun's solder resist layer 305 (dielectric layer) is a dielectric adhesive in which the core/prepreg insulating layer 301 (core substrate) is pasted.[10] EX1003, ¶¶166-67. The solder resist layer 305 (dielectric layer) is adhered to the bottom of second substrate 300 (spacer connector) below L2 Metal and core/prepreg insulating layer 301. EX1003, ¶¶162, 166; EX1005, [0065], FIG. 15. A POSITA would have

[10] Since claim 8 is an apparatus claim, the phrase "pasted" does not require the act of pasting but merely requires that the adhesive adhere to the core substrate. EX1003, ¶166.

recognized the insulating solder resist layer as a dielectric adhesive, as it necessarily has adhesive properties to adhere to a metal surface. EX1003, ¶¶162, 166; EX1005, [0065], FIG. 15:

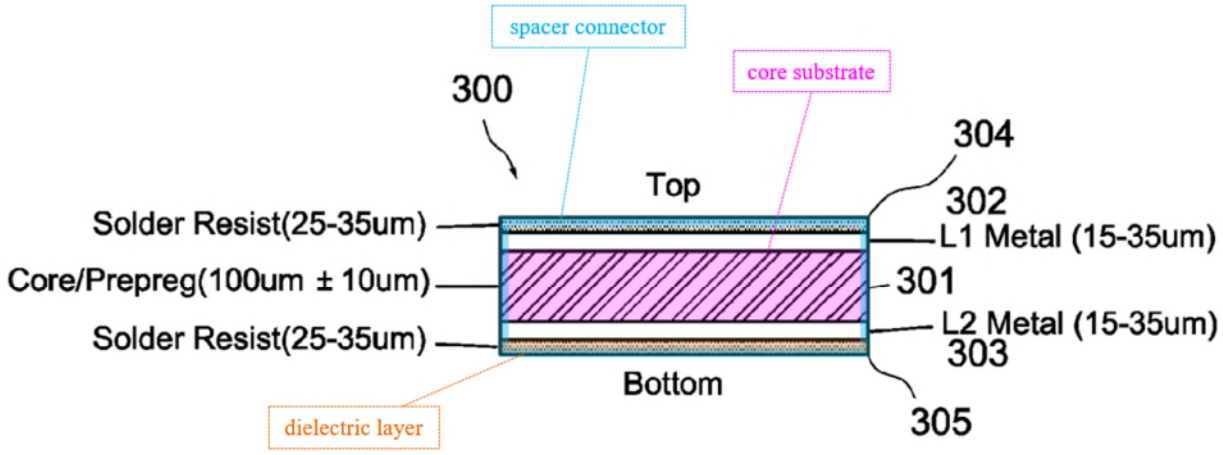


FIG.15

Claim 9[a]

For the same reasons discussed above regarding the top metal pads, *Sun* similarly discloses and/or renders obvious bottom metal pads on the bottom ends of the vias 390 (metal pillars). EX1003, ¶¶168-69; §§VII.A.i.(1[f]), VII.A.ii.(6[b]).

Claim 9[b]

As discussed above regarding 1[i], *Sun* discloses the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate. EX1003, ¶¶170-71; §VII.A.i.(1[i]). As discussed above, *Sun* also discloses or renders obvious bottom metal pads on the

bottom ends of the vias 390 (metal pillars). EX1003, ¶170; §§VII.A.i.(1[f]), VII.A.ii.(9[a]). Accordingly, the bottom ends of vias 390 (metal pillars) are connected to corresponding top ends of first metal connectors 320 (top metal pillars) via the bonding pads (bottom metal pads). EX1003, ¶¶170-71; *see also* §§VII.A.ii.(6[b]), VII.A.ii.(9[a]); EX1005, FIG. 13:

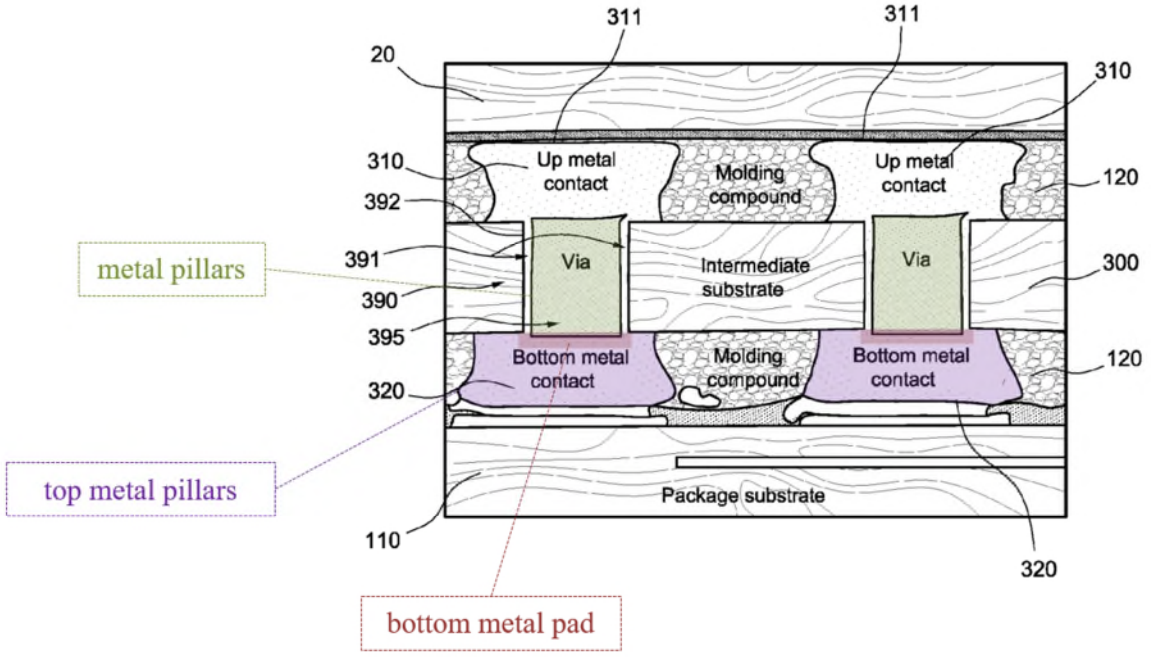


FIG.13

Claim 9[c]

Limitation 9[c] is identical to limitation 6[b] and is thus disclosed or rendered obvious for the same reasons. *See* §VII.A.ii.(6[b]); EX1003, ¶172.

B. GROUND 3: *SUN* WITH *LOVE*

Sun with *Love* renders obvious claims 1-4 and 6-9.

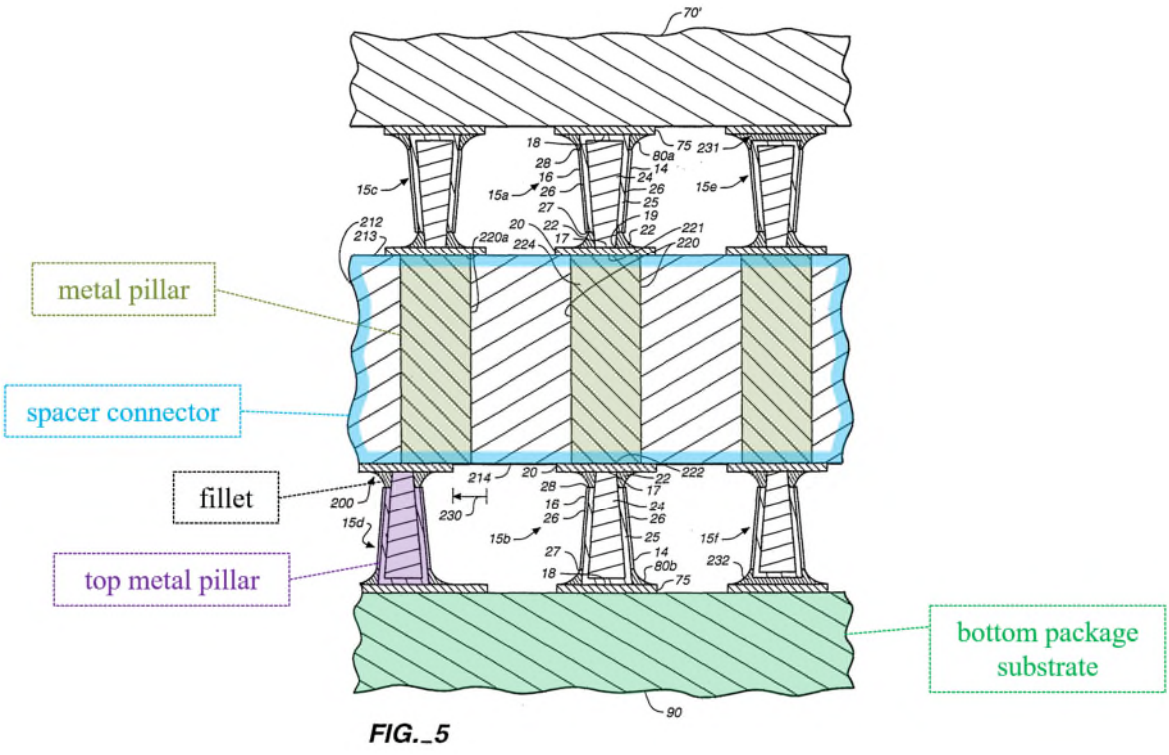
i. Motivation to Combine

Both *Sun* and *Love* are directed to similar semiconductor packaging structures where substrates and spacer connectors are interconnected via metal pillars. EX1003, ¶174; EX1005, [0001], [0048]; EX1007, 1:7-15, 4:51-61 (disclosing "an interconnect structure having a substrate with a plurality of electrically conductive posts"), 12:13-19, 15:16-23; c*ompare* EX1005, FIG. 13 *with* EX1007, FIG. 5.

Both *Sun* and *Love* identify a problem that substrates may warp during operation, due to fluctuating temperatures, creating mechanical stress on the interconnected structure. EX1003, ¶¶175, 96; EX1005, [0011] ("warpage of one or both substrates 20, 40 can deform the connection and solder joints between the upper and lower packages."); EX1007, 1:55-59 ("when the IC chip and the supporting substrate are exposed to elevated temperatures, they will expand at different rates and to different dimensions, thereby inducing mechanical stresses in the solder bump connections."). Accordingly, a POSITA would look to *Love* to address warpage concerns identified in *Sun*. EX1003, ¶¶176, 96.

Love teaches a metal pillar design having metal pads and fillets, which reduces stress on the assembly. EX1003, ¶¶176, 96. *Love* teaches base pads 20 can be formed on conductive material 224 (metal pillars) by depositing a copper seed layer on interconnect substrate 212 (spacer connector), applying a photoresist layer, electroplating copper onto the exposed portions of the seed layer, and then removing

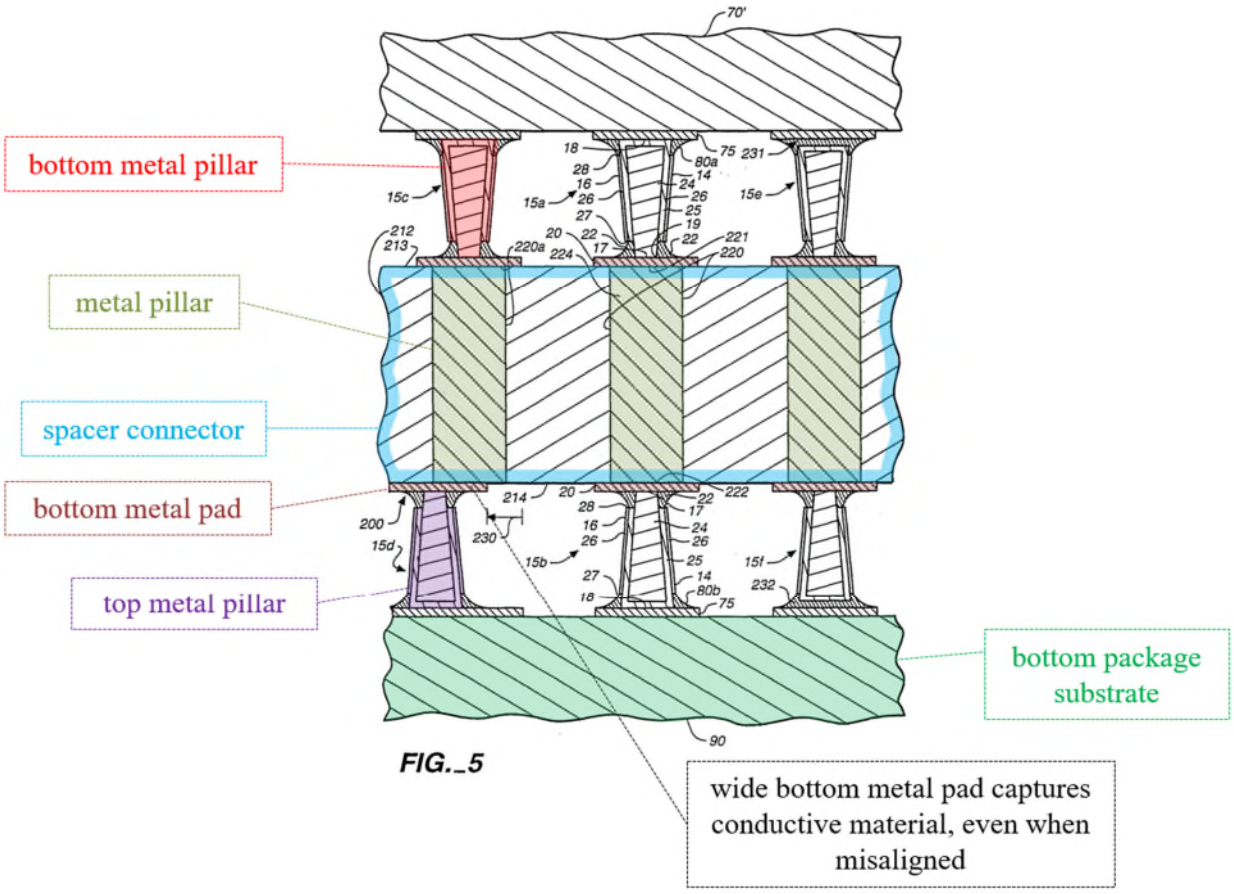
the photoresist layer. EX1007, 14:57-15:15, FIG. 6A. Posts 14 can then be connected to conductive material 224 (metal pillars) of an interconnect substrate 212 via base pads 20 (metal pads). EX1007, 12:43-60, FIG. 5. *Love* further teaches fillet 22 can be added to base pad 20 and post 14 to "de-concentrate any of the mechanical stress and strain at the junction of end 17 [of post 14] and base pad 20." EX1007, 10:5-23.



EX1007, FIG. 5.

Love also teaches base pads 20 provide the benefit of reducing the required alignment tolerances during assembly. EX1003, ¶¶177, 96; EX1007, 13:16-37 (explaining that "the interconnect columns may be somewhat offset from an exact

opposing relationship," due to misalignment during the manufacturing process, and that applying wide base pads 20 allows "misalignment error[s]").



EX1007, FIG. 5.

Based on the teachings of *Love*, a POSITA would have been motivated to apply *Love*'s interconnect columns 15 (which include fillets 22 and posts 14) to *Sun*'s second metal connectors 310 and first metal connectors 320, and add *Love*'s base pads 20 to *Sun*'s vias 390 to (1) reduce mechanical stress from warping and (2) provide a wider connection area between the metal pillars and top and bottom metal pillars, respectively, to account for alignment errors during assembly. EX1003,

¶¶178, 96; EX1007, 10:5-23, 13:32-37. This combination would not require alteration to any other aspect of *Sun*'s design. EX1003, ¶178.

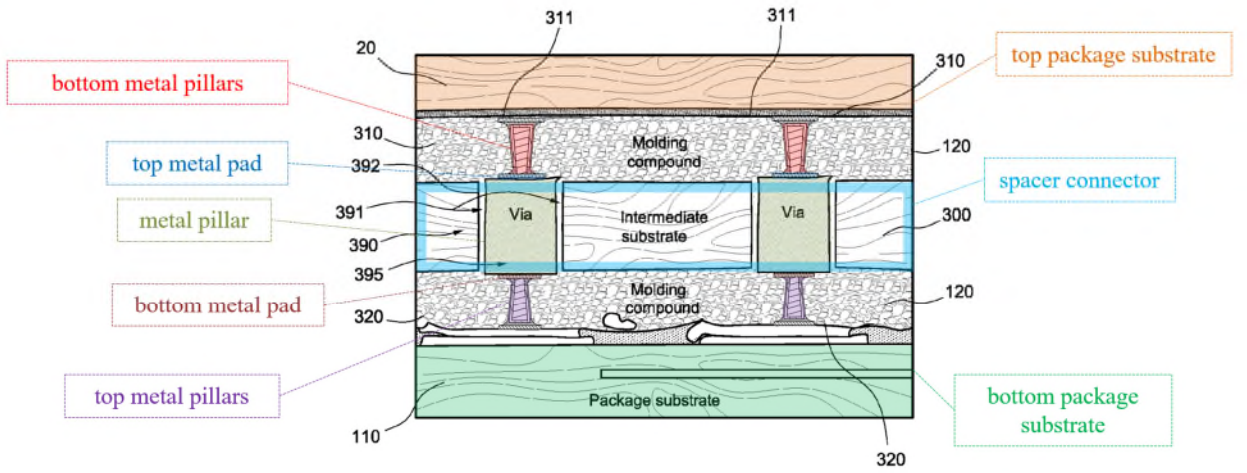


FIG.13

EX1005, FIG. 13 (superimposed with the base pad and interconnect columns of *Love*).

Moreover, a POSITA would have had a reasonable expectation of success in the proposed combination. EX1003, ¶179. For example, *Sun* discloses similar bonding pads 140, disposed on the bottom ends of the first metal connectors 320. EX1005, [0066]-[0068]. *Sun* states these bonding pads can be applied to other pillars. EX1005, [0066]. *Sun* also discloses similar second metal connectors 310 and first metal connectors 320, which interconnect a package substrate and spacer connector. EX1005, [0048]. Meanwhile, *Love* provides detailed working examples of how

similar base pads and interconnect columns can be applied to the top and bottom of vias. EX1003, ¶179; EX1007, 14:57-15:15, FIG. 6A.

The *Sun-Love* combination therefore involves nothing more than applying known elements (base pads and interconnect columns) in a known structure (vias and metal connectors) using known methods (copper electroplating) to achieve this well-understood and predictable benefit (reducing mechanical stress due to warpage and allowing for alignment errors during manufacturing). EX1003, ¶180. This is the type of combination that a POSITA would reasonably expect to succeed without undue experimentation, as it relies on established semiconductor manufacturing techniques and addresses known, well-documented problems with interconnects. EX1003, ¶180.

ii. Independent Claim 1

1[pre]-[e]

Sun-Love renders obvious limitations 1[pre]-[e] for the same reasons discussed above in Grounds 1-2. EX1003, ¶181; §VII.A.i.

1[f]

Sun-Love renders obvious a plurality of top metal pads, each on a top end of a corresponding via 390 (metal pillar) among the plurality of vias 390. EX1003, ¶¶182-83. As discussed above in §VII.B.i, *Love* discloses a base pad 20 (top metal pad) can be applied to metal pillars, such as vias 390 of *Sun*. EX1007, 14:57-15:15, FIG. 6A; EX1005, [0062]-[0063], [0066]. A POSITA would have been motivated

to apply *Love*'s base pads 20 to *Sun*'s vias 390 to achieve the benefits of reducing mechanical stress from warping and accommodating alignment errors as taught by *Love*. EX1003, ¶182; §VII.B.i. Furthermore, a POSITA would have a reasonable expectation of success in doing so. EX1003, ¶182; §VII.B.i. Accordingly, a POSITA would arrive at the *Sun-Love* design shown below, which includes base pads 20 (top metal pads) disposed on the top ends of vias 390 (metal pillars). EX1003, ¶182.

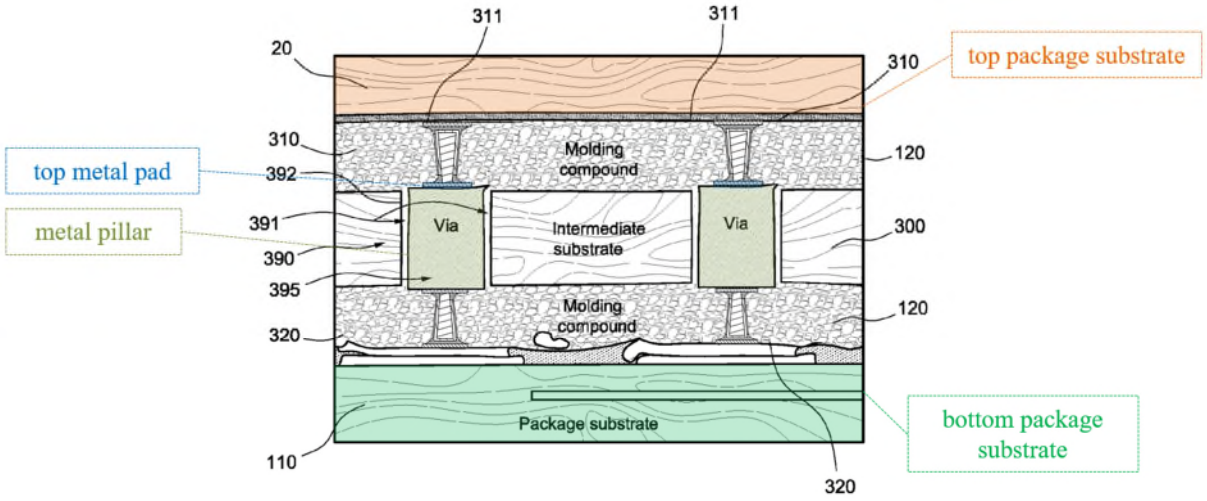


FIG.13

EX1005, FIG. 13 (superimposed with the base pad and interconnect columns of *Love*).

1[g]-[m]

As discussed above, the *Sun-Love* design is similar to *Sun*, except *Love*'s base pads 20 are applied to *Sun*'s vias 390, and *Sun*'s first metal connectors 320 and second connectors 310 are replaced with *Love*'s interconnect structures 15. EX1003,

¶184; §VII.B.i. The remaining claim elements are met in the *Sun-Love* combination for the same reasons as Ground 1-2. EX1003, ¶184; §VII.A.i.

iii. Dependent Claims 2-4 and 6-9

Claims 2-4

Sun-Love renders obvious claims 2-4 for the same reasons as Grounds 1-2 above. EX1003, ¶185; §VII.A.ii-B.i.

Claim 6[a]

Sun-Love renders obvious 6[a] for the same reasons as Grounds 1-2 above. EX1003, ¶186; §VII.A.ii-B.i.

Claim 6[b]

As discussed above regarding 1[f], *Sun-Love* renders obvious base pads 20 (top metal pads) on the top of each via 390 (metal pillar). §VII.B.ii.(1[f]). For the additional reasons discussed above regarding *Sun*, *Sun-Love* renders obvious 6[b]. §VII.A.ii.(6[b]); EX1003, ¶¶187-88.

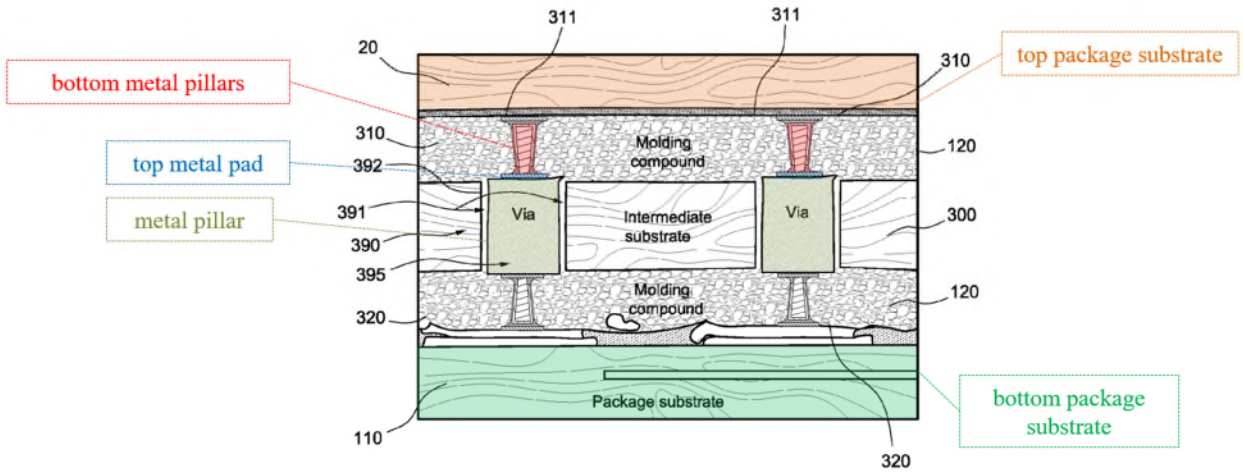


FIG.13

EX1005, FIG. 13 (superimposed with the base pad and interconnect columns of *Love*).

Claims 7-8

Sun-Love renders claims 7-8 for the same reasons as Grounds 1-2. EX1003, ¶¶189-90; §§VII.A.ii-B.i.

Claim 9[a]

Sun-Love renders obvious the second substrates 300 (spacer connectors) include a plurality of base pads 20 (bottom metal pads), each on the bottom end of a corresponding via 390 (metal pillar). EX1003, ¶¶191-92. For the same reasons discussed above regarding the top metal pads, *Sun-Love* similarly renders obvious bottom metal pads on the bottom ends of the vias. EX1003, ¶191; §VII.B.ii.(1[f]);

see also EX1005, FIG. 13 (superimposed with the base pad and interconnect columns of *Love*):

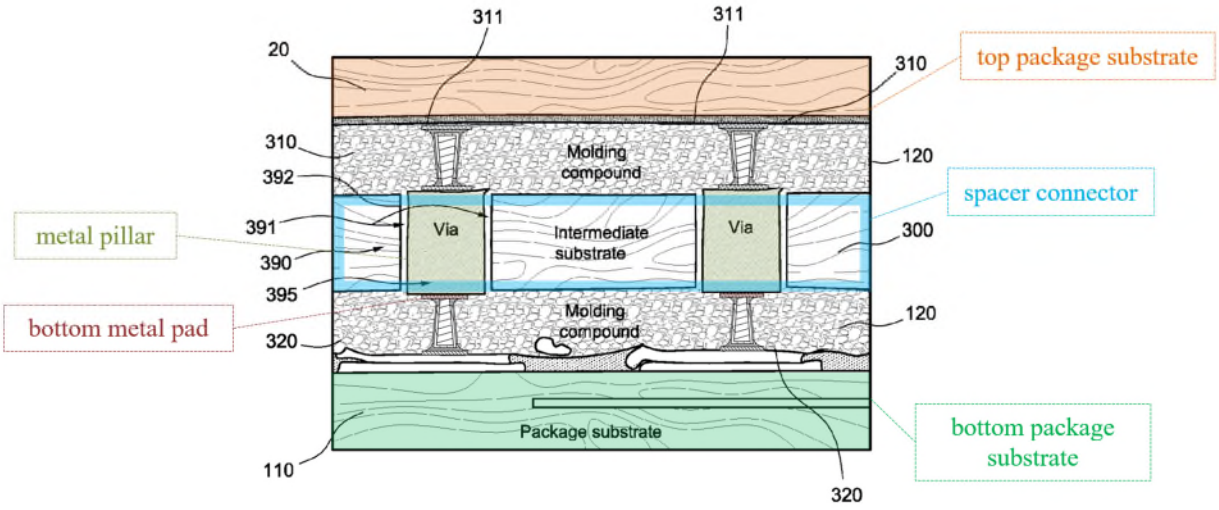


FIG.13

Claim 9[b]

As discussed above, *Sun* discloses or renders obvious bottom metal pads on the bottom ends of the vias 390 (metal pillars). EX1003, ¶¶193-94; §§VII.A.i.(1[f]), VII.A.ii.(9[b]). For the same reasons discussed above regarding *Sun*, *Sun-Love* also renders obvious 9[b]. EX1003, ¶193; §§VII.A.i.(1[f]), VII.A.ii.(9[b]).

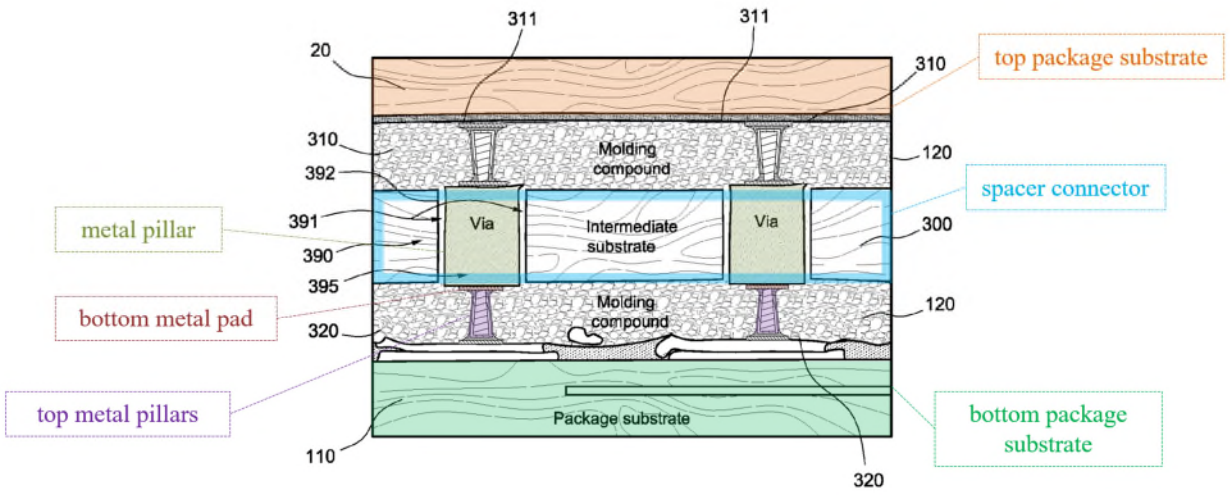


FIG.13

EX1005, FIG. 13 (superimposed with the base pad and interconnect columns of *Love*).

Claim 9[c]

Limitation 9[c] is identical to limitation 6[b] and is thus rendered obvious for the same reasons. *See* §VII.B.iii.(6[b]); EX1003, ¶195.

C. GROUND 4: *SUN* WITH *HU*

Sun with *Hu* renders obvious claims 1-4 and 6-9.

i. Motivation to Combine

Sun and *Hu* are both directed to a PoP assembly, where a plurality of semiconductor packages are stacked. EX1003, ¶197; EX1005, Abstract; EX1008, [0001], [0003]. Both recognize the need to replace conventional solder balls with

metal pillars for interconnect packages. EX1003, ¶197; EX1005, [0015], [0066]; EX1008, [0004]-[0005].

Sun explains "solder balls have a less fine pitch and less well defined shape than the metal pillars. Furthermore, at typical processing temperatures (e.g. around 260 degrees Celsius) the solder balls will melt and collapse down, while the metal (e.g. copper) pillars will remain solid and well defined." EX1005, [0066].

As discussed above, *Sun* teaches a PoP structure, where first connectors 320 and second connectors 310 (top and bottom metal pillars) can be stacked with vias 390 to connect a first substrate 110 and a third substrate 20. EX1005, [0061], [0063], FIG. 13:

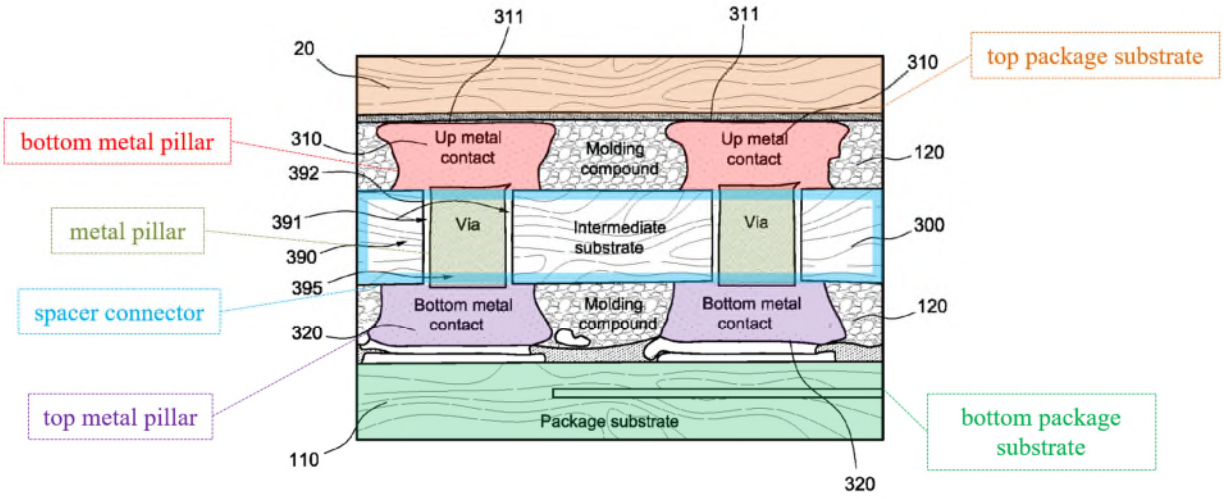


FIG.13

Hu explains "it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity." EX1008, [0004]. To solve this, *Hu* teaches using "metal posts in combination with a solder material." EX1008, [0005]; EX1003, ¶200.

Hu identifies a challenge with metal pillars, explaining that "it is not easy to control the uniformity of the height of the metal posts." EX1008, [0008], FIG. 1 (showing metal posts with non-uniform height). *Hu* addresses the uniformity problem by placing "conductive bonding layers" of varying offsetting heights on initially formed metal posts, so the resulting metal posts have the same "height." *Id*., [0030], FIG. 2E. *Hu* further teaches process-level details for implementing such uniform metal pillars on a package substrate. *Id*., [0013], [0028]-[0035], FIGs. 2C-2F; EX1003, ¶201.

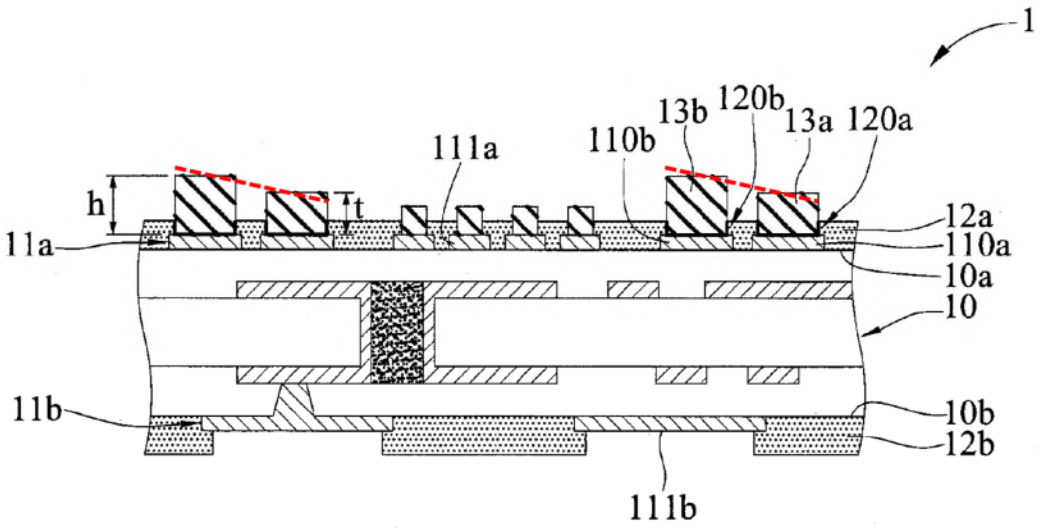


FIG. 1 (PRIOR ART)

EX1008, FIG. 1 (illustrating mismatched metal pillar heights).

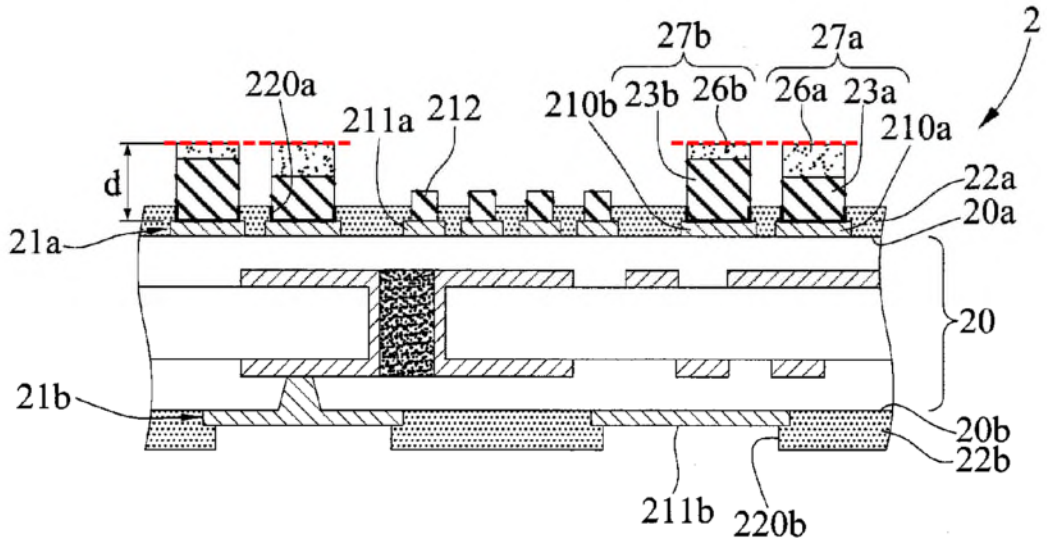


FIG.2E

EX1008, FIG. 2E (illustrating matched metal pillar heights).

A POSITA would have been motivated to look to *Hu* for guidance on how to implement *Sun*'s first connectors 320 and second connectors 310 as metal pillars, to achieve uniform pillar height in a practical and reliable manner. EX1003, ¶202. A POSITA would therefore have been motivated to apply *Hu*'s techniques to *Sun* to "prevent tilted stack structures and poor coplanarity in a… stacking process…to improve the product reliability." EX1008, [0013], [0038]; EX 1003, ¶202.

Accordingly, a POSITA would have found it obvious to implement the processing steps of the metal pillars of *Hu* to fabricate *Sun*'s first connectors 320 and second connectors 310. EX1003, ¶203. A POSITA would first form metal pillars on the bonding pads 140 on top of *Sun*'s first substrate 110 (bottom package substrate) and bottom of third substrate 20 (top package substrate), prior to assembling them with the second substrates 300 (spacer connector) (EX1005, [0061], [0066], [0068]; EX1008, [0025]-[0028]), so that the height of the metal pillars can be adjusted using conductive bonding layers to achieve good coplanarity as taught by *Hu*. EX1003, ¶203; EX1008, [0008], [0029]-[0030]; EX1005, FIG.12 (modified to illustrate the *Sun-Hu* device):

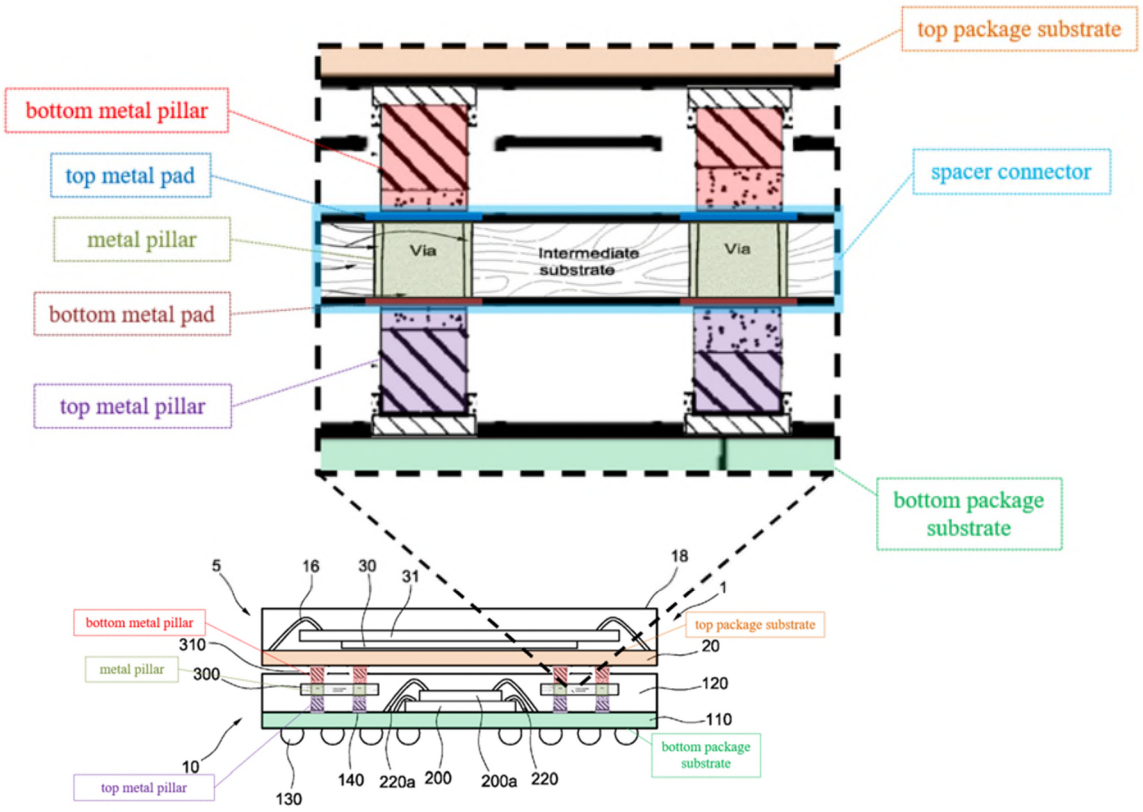


FIG.12

This approach retains *Sun*'s structural design but varies the fabrication steps in view of *Hu*, such that metal pillars (first connectors 320 and second connectors 310) are first built on *Sun*'s bonding pads 140 (equivalent to *Hu*'s "conductive pads 210") on the bottom package substrate and the top package substrate, respectively. EX1003, ¶204. This combination would predictably yield the same electrical interconnectivity while improving coplanarity and mechanical stability. EX1003, ¶204.

A POSITA would have had a reasonable expectation of success in the proposed combination. EX1003, ¶205. *Sun* already teaches forming first connectors

320 and second connectors 310 as metal pillars. EX1005, [0061]. Meanwhile, *Hu* provides detailed, working examples of metal pillars formed by an "electroplating process" for PoP interconnections to achieve improved coplanarity. EX1008, [0028]-[0035], FIGs. 2C-2F. The combination involves nothing more than applying known elements (metal pillars) in a known structure (PoP) using known methods (electroplating) to achieve a well-understood and predictable function (providing reliable electrical and mechanical connections). EX1003, ¶205. A POSITA would reasonably expect this combination to succeed without undue experimentation. *Id*.

ii. Claims 1-4 and 6-9

As discussed above, the combination of *Sun* and *Hu* does not materially alter the final package structure of *Sun* but merely changes the processing steps, by first forming the bottom metal pillars and the top metal pillars on the top and bottom package substrates, respectively, prior to joining the two substrates with the spacer connectors to avoid a tilted package stack, as taught by *Hu*. EX1003, ¶206.

To the extent the Board disagrees with Petitioners' proposed construction for the "of" terms—i.e., "bottom metal pillars of the top package substrate" and "top metal pillars of the bottom package substrate" (1[h]-[j], 4, 6, 9)—and instead requires the bottom metal pillars be built as part of the top package and the top metal pillars as part of the bottom package prior to assembling the PoP assembly, *Sun-Hu* renders obvious claims 1-4 and 6-9 for the same reasons discussed above in Grounds

1-2, even under that narrow construction, because the resulting structure of *Sun-Hu* is materially identical to *Sun*. EX1003, ¶207; §VII.A.

D. GROUNDS 5-6: *CHEN*

Chen anticipates and/or renders obvious claims 1-9.

i. Independent Claim 1

1[pre]

Chen discloses a "structure." EX1003, ¶¶209-11; EX1006, [0008] (disclosing "[a] Package-on-Package (PoP) structure and the methods of forming the same"). *Chen*'s PoP structure (FIG. 9) is substantially similar to the '202 Patent's structure (FIG. 8).

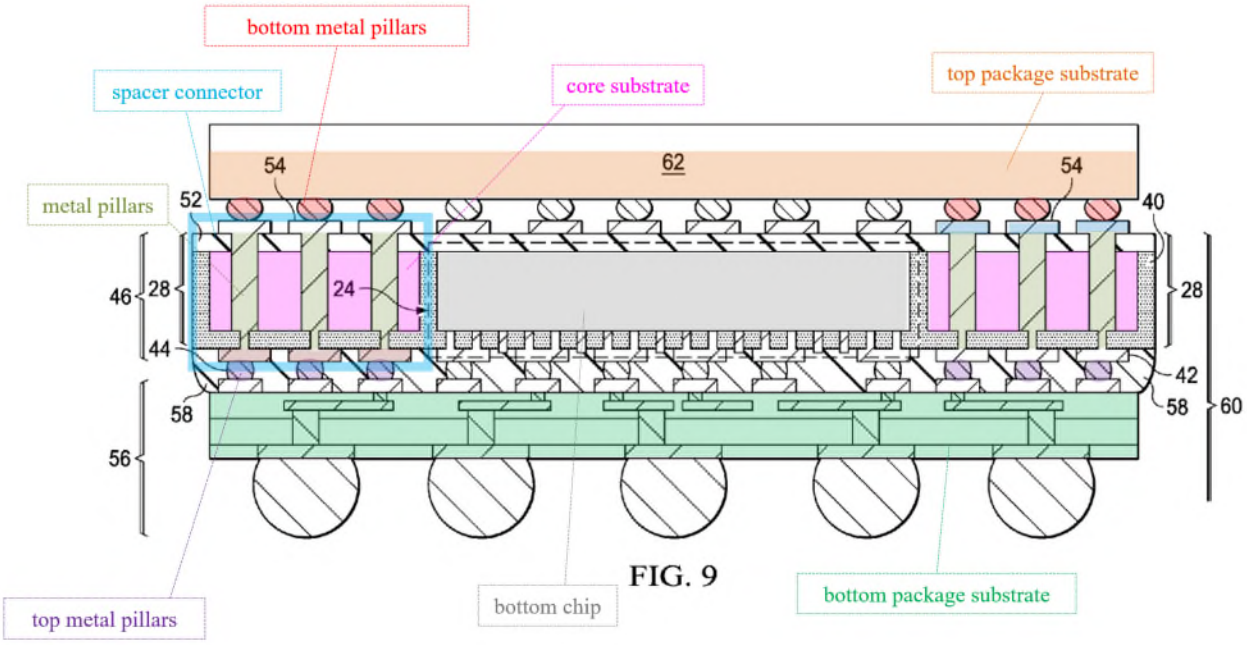
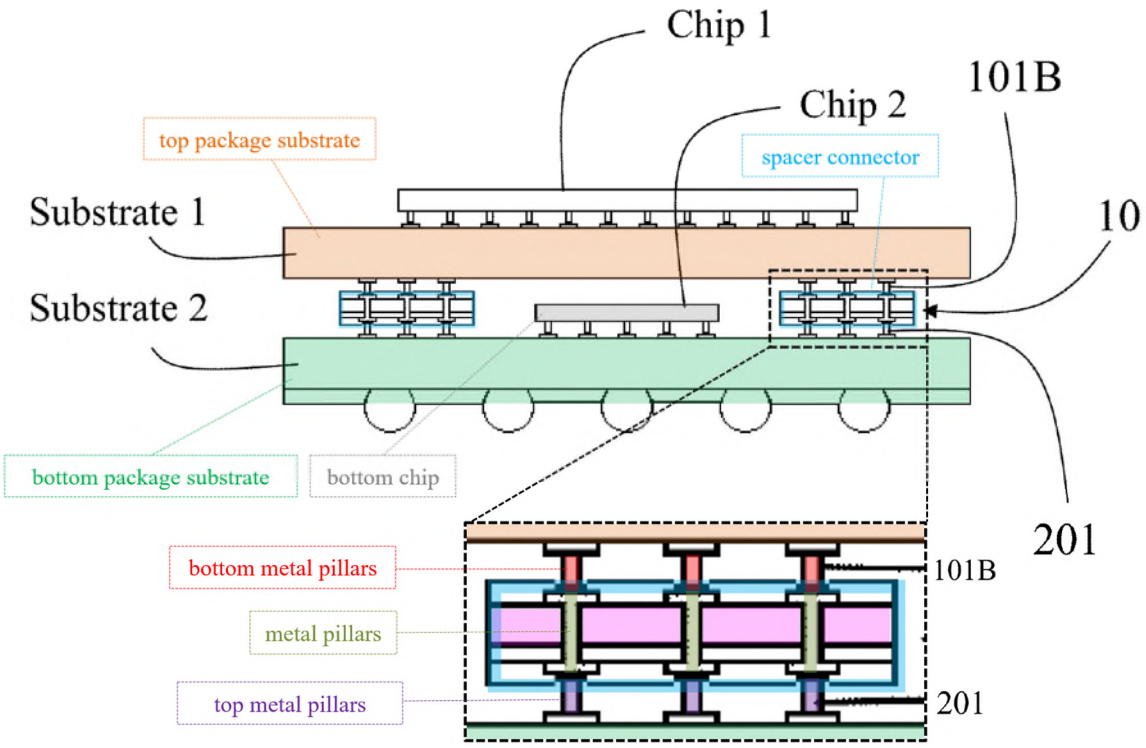


FIG. 9

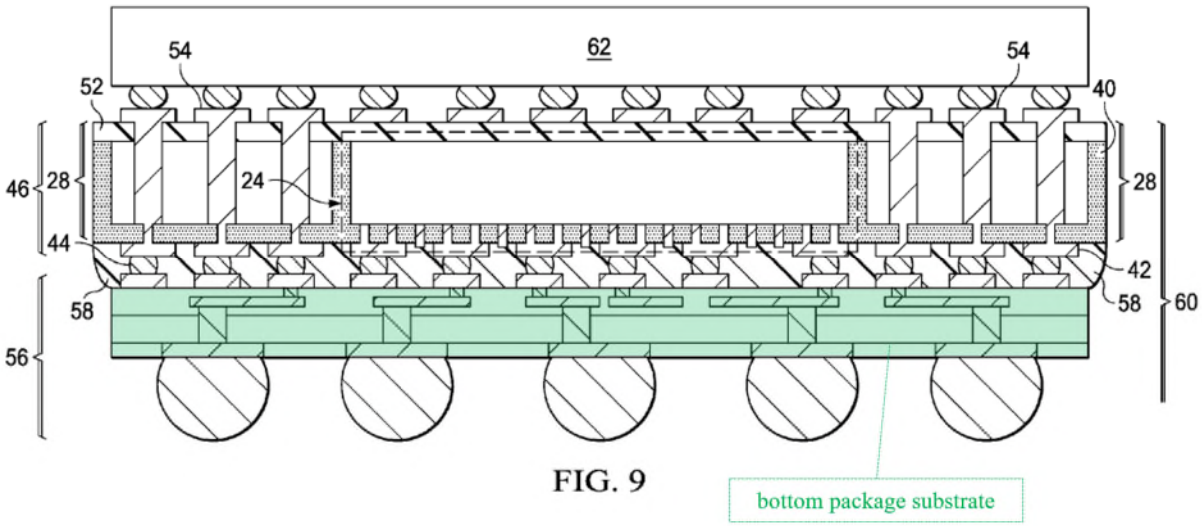
Fig.8



Compare EX1006, FIG. 9 (top) *with* EX1001, FIG. 8 (bottom).

1[a]

Chen discloses package component 56 (bottom package substrate), which "may be a ***package substrate***." EX1006, [0018], [0019], [0020], [0024] ("The bottom package includes a package substrate."), FIGs. 8-10; EX1003, ¶¶212-13.



EX1006, FIG. 9.

1[b]

Chen discloses package substrate within top package component 62 (top package substrate) stacked on top of package component 56 (bottom package substrate). EX1003, ¶¶214-15; EX1006, [0019] (teaching "bonding of top package component 62 to bottom package 60" and explaining "[top] package component 62 is a package that includes a device die (not shown) bonded to ***a package substrate*** (not shown)"), [0024], [0018] ("package 46 [] bonded to package component 56 to form bottom package 60"), FIGs. 9-11.

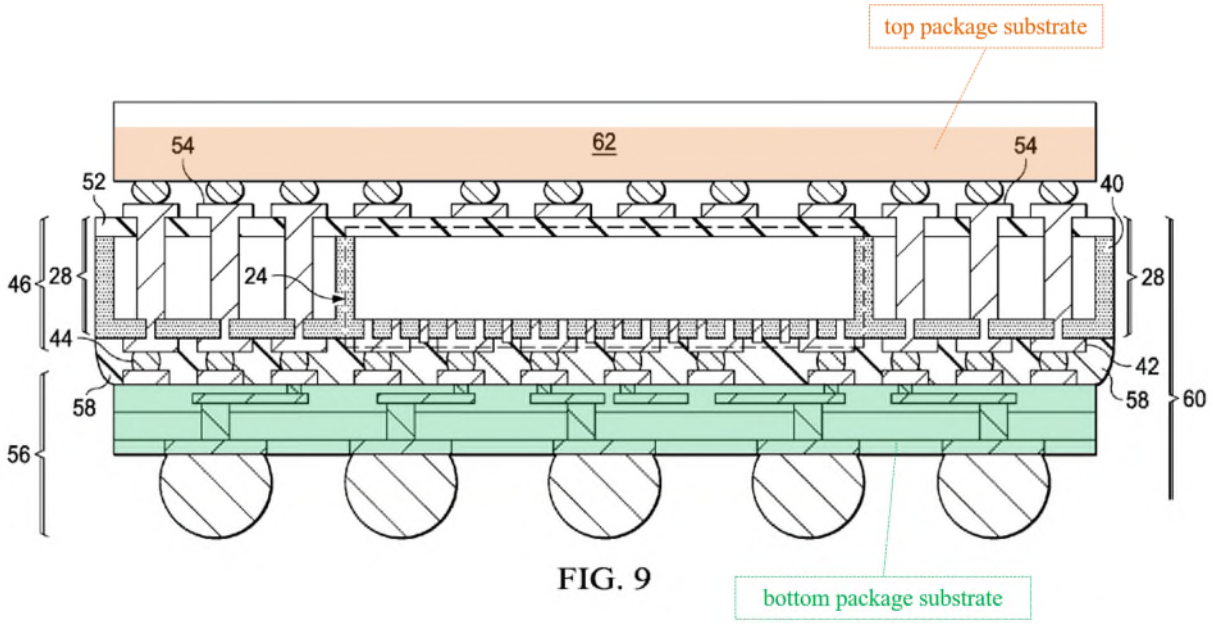


FIG. 9

EX1006, FIG. 9.

1[c]

Chen's Through-Assembly Via (TAV) modules 28 (spacer connector) interposed between package substrate in top package component 62 (top package substrate) and package component 56 (bottom package substrate) "are used to electrically couple" the two substrates. EX1006, [0019], [0021], [0010], FIGs. 9-11; EX1003, ¶¶216-17. As shown in FIG. 9 below, TAV modules 28 also define a space between *Chen*'s top and bottom package substrates, so that "package component 24 includ[ing] one or a plurality of device dies" can be placed between the two substrates. EX1006, [0009]; EX1003, ¶216.

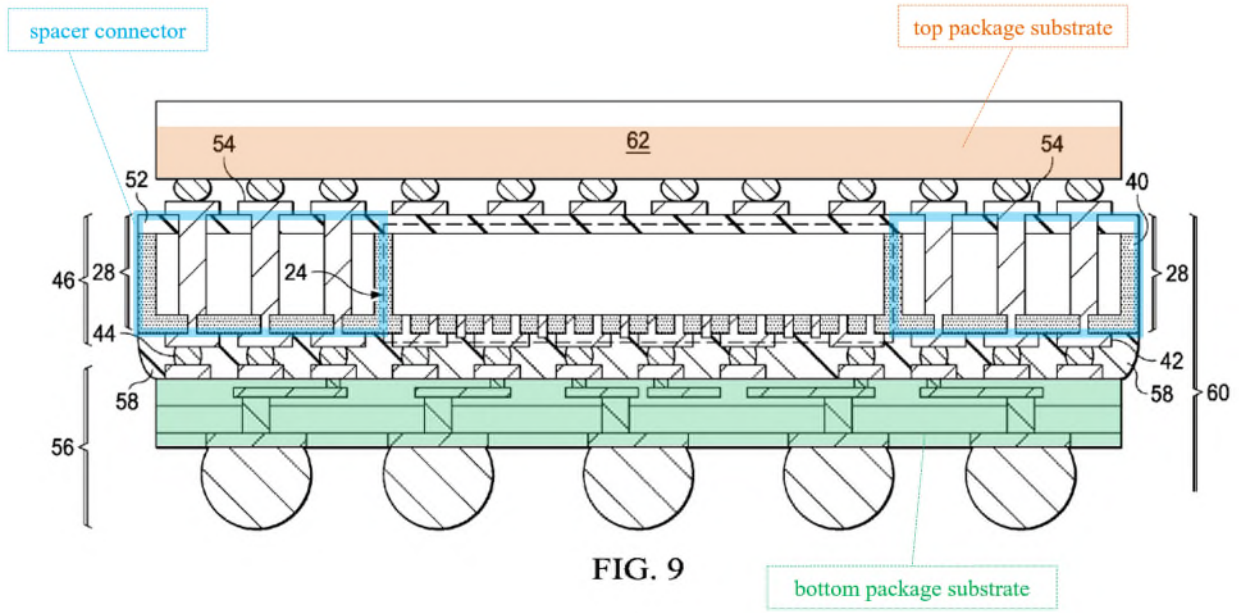


FIG. 9

EX1006, FIG. 9.

1[d]

Chen discloses "TAV modules 28 [spacer connector] include ***substrate*** 34 [core substrate]," "which may be a semiconductor substrate such as a silicon substrate." EX1006, [0010], [0021], [0023] ("In accordance with embodiments, a device includes a TAV Module, which includes a ***substrate***."), [0024], FIGs. 1, 6, 9; EX1003, ¶¶218-19.

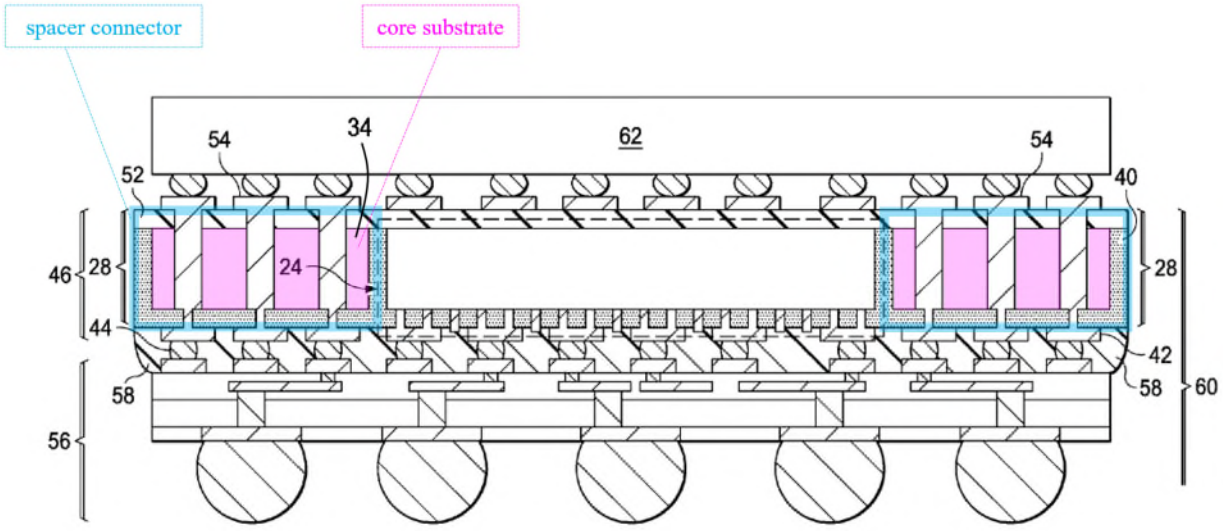


FIG. 9

EX1006, FIG. 9[11].

1[e]

Chen's TAV modules 28 (spacer connector) include "[t]hrough-substrate vias 32 [] formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34." EX1006, [0010]. "Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like." *Id*. Further, "metal posts 30 are connected to, and are aligned to, through-substrate vias 32," together[12] forming the metal pillars, each passing through the substrate 34 (core substrate). EX1006, [0011], [0010] ("TAV modules 28 may also include metal

[11] Unless otherwise noted, numerical references 30, 32, and/or 34 annotated in FIG. 9 of *Chen* are added in view of FIGs. 1, 4, 6.

[12] For avoidance of doubt, Petitioners map "through-substrate vias 32" and "metal posts 30" jointly as the claimed metal pillars of 1[e].

posts 30 (such as copper posts)...."); EX1003, ¶¶220-21; EX1006, [0022], FIGs. 9, 12.

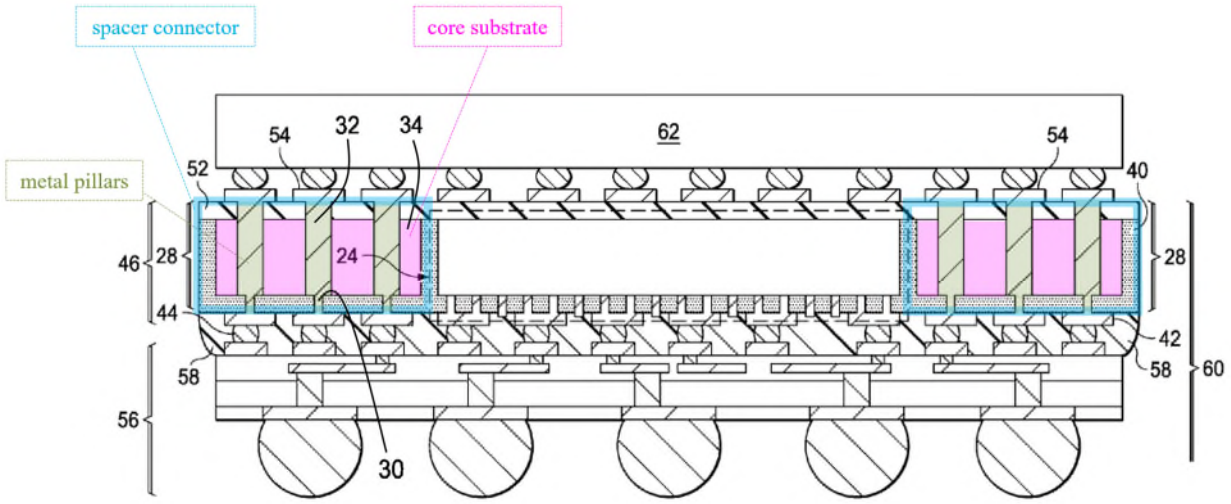


FIG. 9

EX1006, FIG. 9.

1[f]

Chen discloses multiple Redistribution Lines (RDLs) 54[13] (top metal pads), each on a top end of a corresponding through-substrate via 32 (metal pillars) for electrical connection. EX1003, ¶¶222-28; EX1006, [0011] ("TAV modules 28 may include redistribution layer(s) that include redistribution lines and ***metal pads*** on the top sides of TAV modules 28"), [0014] ("RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer."), [0017], FIGs. 6-7, 9.

[13] For avoidance of doubt, Petitioners map the "metal pads" to RDL features shown and highlighted in *Chen*'s corresponding figures herein.

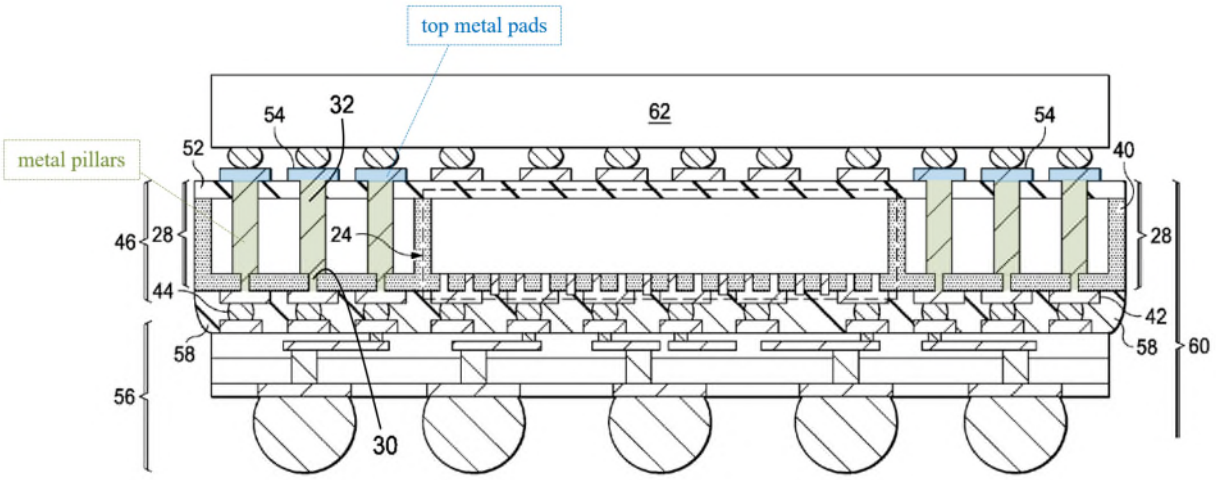


FIG. 9

EX1006, FIG. 9. It was well-known in the art that RDLs include both metal lines and metal pads. EX1003, ¶223. The metal lines are elongated features patterned in the RDLs, serving as a routing element, whereas the metal pads are enlarged metal regions of the RDLs, serving as interface or termination points. *Id*. The portions of RDLs 54 shown in FIG. 9 have enlarged regions, serving as contact pads for connectors between substrates, and are therefore metal pads. EX1003, ¶¶223-24.

To the extent *Chen*'s RDLs 54 do not explicitly disclose metal pads, *Chen* renders obvious this limitation for the same reasons. EX1003, ¶¶225-27; *see also* EX1007, 13:12-41 (teaching metal pads allowing for misalignment errors); EX1011, 13, 16 (explaining metal pads prevent contaminants flow-in); *see also* §VII.A.i.(1[f]).

1[g]

Chen discloses a bottom end of each of metal posts 30 (metal pillars) protrudes downwardly from a bottom surface of substrate 34 (core substrate). EX1003, ¶¶229-30; EX1006, [0010]-[0011], FIGs. 1, 4.

As shown in FIGs. 5-6, 9, portions of the metal pillars (metal posts 30) protrude ***downwardly*** from a bottom surface of substrate 34.

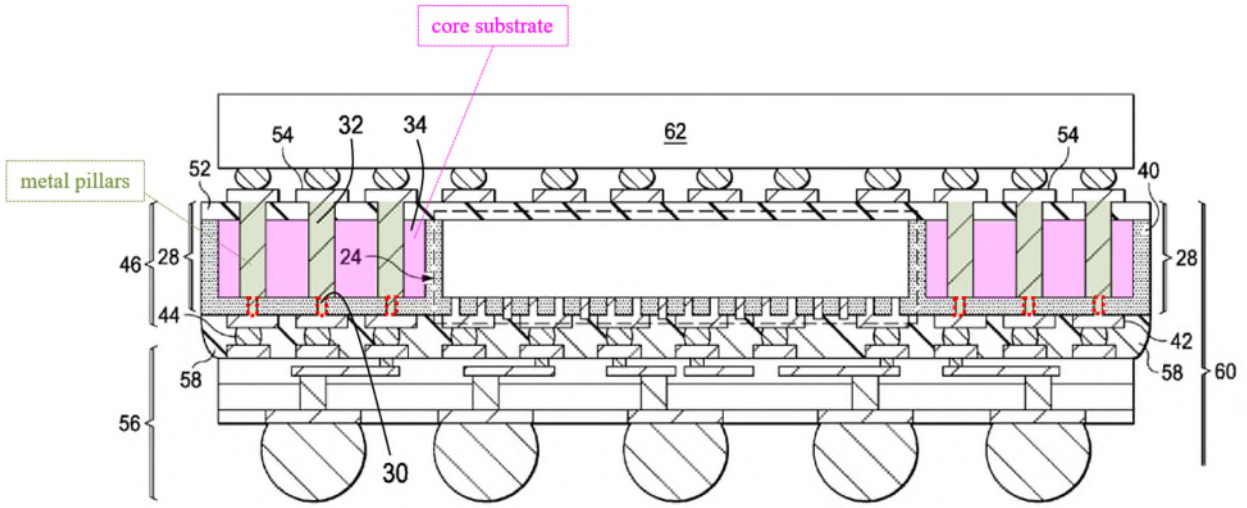


FIG. 9

EX1006, FIG. 9 (dashed red lines showing metal posts 30 protruding downwardly from substrate 34).

1[h]

Chen discloses package substrate in top package component 62 (top package substrate) has, on a bottom surface thereof, multiple (upper) connectors 44[14] (bottom

[14] While not all of connectors in FIG.9 are specifically identified as connectors 44, a POSITA would have understood connectors 44 refer to both the upper and lower

metal pillars) each coupled to a corresponding through-substrate via 32 and metal post 30 (metal pillars) of TAV modules 28 (spacer connector). EX1003, ¶¶231-34; EX1006, FIG. 9. *Chen* teaches connectors 44 may "include ***solder balls***… ***metal pillars***, or ***metal pillars*** and solder caps, which may also be formed through plating." EX1006, [0014], FIGs. 4, 9. As discussed in §V.A, PO broadly interprets the claimed metal pillar to include solder structures, EX1004, ¶¶45-46. *Chen*'s (upper) connectors 44 disclose "bottom metal pillars" under PO's broad interpretation (which includes "solder balls") and Petitioners' correct construction ("metal pillars"). EX1006, [0014]; EX1003, ¶¶233-34.

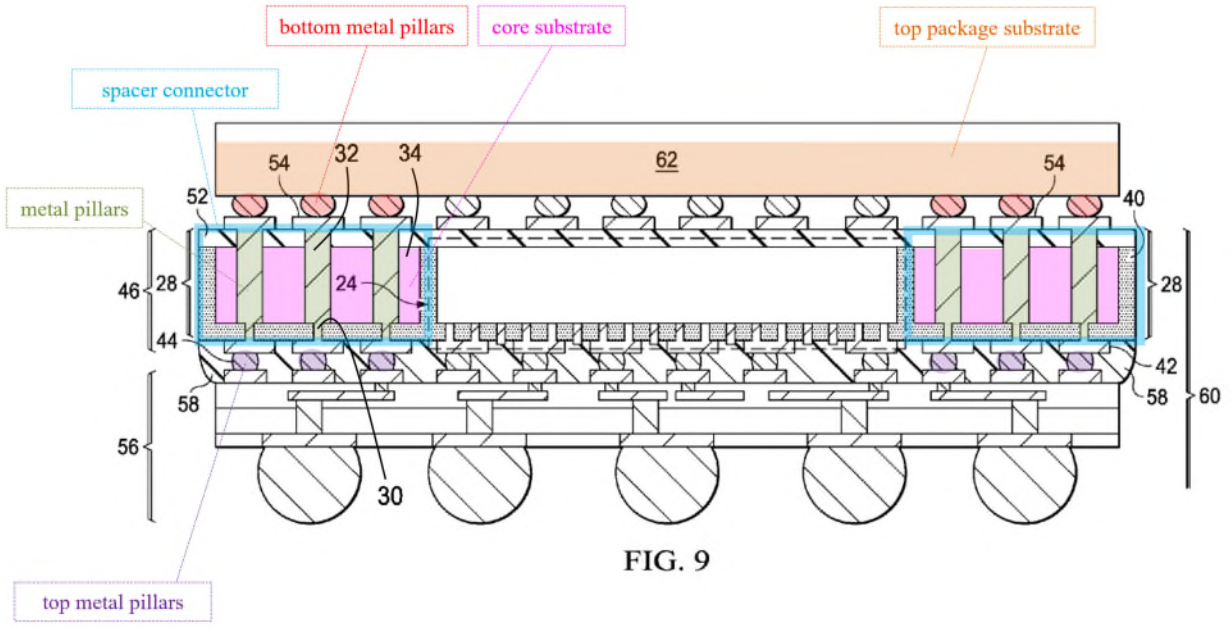


FIG. 9

connectors that connect TAV modules and package component 24 to the top and bottom package substrates, respectively, given the same shading applied to all connectors and the same function served by both sets of connectors. EX1003, ¶232; EX1006, FIG. 9.

EX1006, FIG. 9.

To the extent *Chen* does not expressly disclose bottom metal pillars under Petitioners' construction of metal pillars in §V.A, *Chen* at least renders 1[h] obvious. EX1003, ¶¶235-37. While Figure 9 illustrates (upper) connectors 44 with rounded shapes resembling "solder balls," *Chen* explains that "the amount of the solder balls that can be used in a PoP structure is limited" because "the lateral sizes of the solder balls are [] large." EX1006, [0002]. *Chen* teaches metal pillars are favorable interconnect structure for PoP assemblies because "the pitches and the sizes of [metal pillars] may be very small." EX1006, [0021]; *see also* EX1008, [0004]-[0005] ("[M]etal posts … are used in stack structures so as to overcome the above-described drawbacks" of solder balls, including "a tilted stack structure," "poor coplanarity," "positional deviation of solder joints between the packages," and "solder bridge."); EX1005, [0015] ("[T]he first and second electrical connectors [in a similar PoP structure] are metal pillars, e.g. copper pillars."); EX1003, ¶236. Accordingly, a POSITA would have found it obvious to implement (upper) connectors 44 as metal pillars to address the drawbacks of solder balls and to realize the fine-pitch PoP fabrication according to the teachings of *Chen* itself and/or the knowledge of a POSITA. EX1003, ¶237.

1[i]

Chen discloses package component 56 (bottom package substrate) has, on a top surface thereof, multiple (lower) connectors 44 (top metal pillars), each "formed to connect to [corresponding] metal posts…30" and through-substrate vias 32 (metal pillars) of TAV modules 28 (spacer connector). EX1006, [0014], FIGs. 8-9 (showing lower connectors 44 on package component 56 are connected to corresponding metal posts 30 via metal pads 42); EX1003, ¶¶238-39.

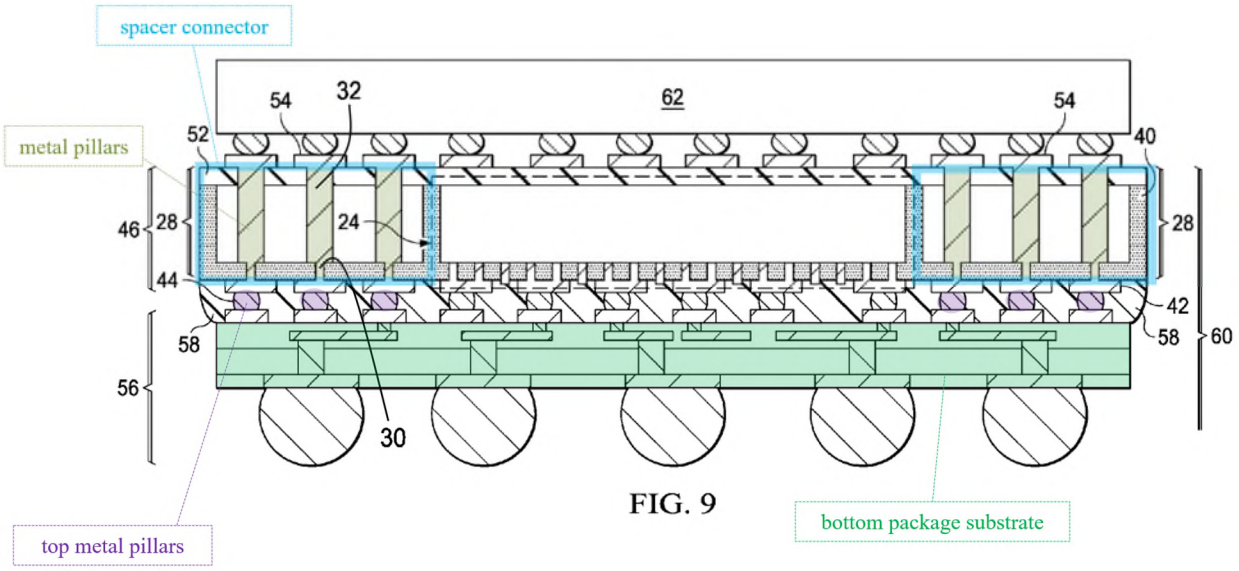


FIG. 9

EX1006, FIG. 9. *Chen* teaches connectors 44 may "include ***solder balls***…[or] ***metal pillars***." *Id*., [0014]. Thus, Chen's (lower) connectors 44 disclose "top metal pillars" under both PO's broad construction and Petitioners' correct construction of "metal pillars." EX1006, [0014]; *supra*, §§V.A, VII.D.i.(1[h]); EX1003, ¶239.

To the extent *Chen* does not expressly disclose top metal pillars, *Chen* renders 1[i] obvious for the same reasons discussed in §VII.D.i.(1[h]). EX1003, ¶240.

1[j]

Chen discloses package substrate in top package component 62 (top package substrate) is electrically coupled to package component 56 (bottom package substrate) through (upper) connectors 44 (bottom metal pillars), through-substrate vias 32 and metal posts 30 (metal pillars), and (lower) connectors 44 (top metal pillars). EX1003, ¶¶241-43; EX1006, FIG. 9. For example, "TAV modules 28 [spacer connector] are used to electrically couple…package component 62 to package component 56." EX1006, [0019]; *see also id.*, [0021], FIG. 9. This electrical connection is formed with "through-substrate vias 32, which are used for electrically connecting the features on opposite sides of TAV modules 28." *Id.*, [0022]. The top side of through-substrate vias 32 is electrically coupled to top package component 62 via (upper) connectors 44 while the bottom side, "connected to, and are aligned to" metal posts 30, is electrically coupled to package component 56 via (lower) connectors 44. *Id.*, [0011], [0014] ("connectors 44…formed to connect to metal posts…30"), FIG. 9:

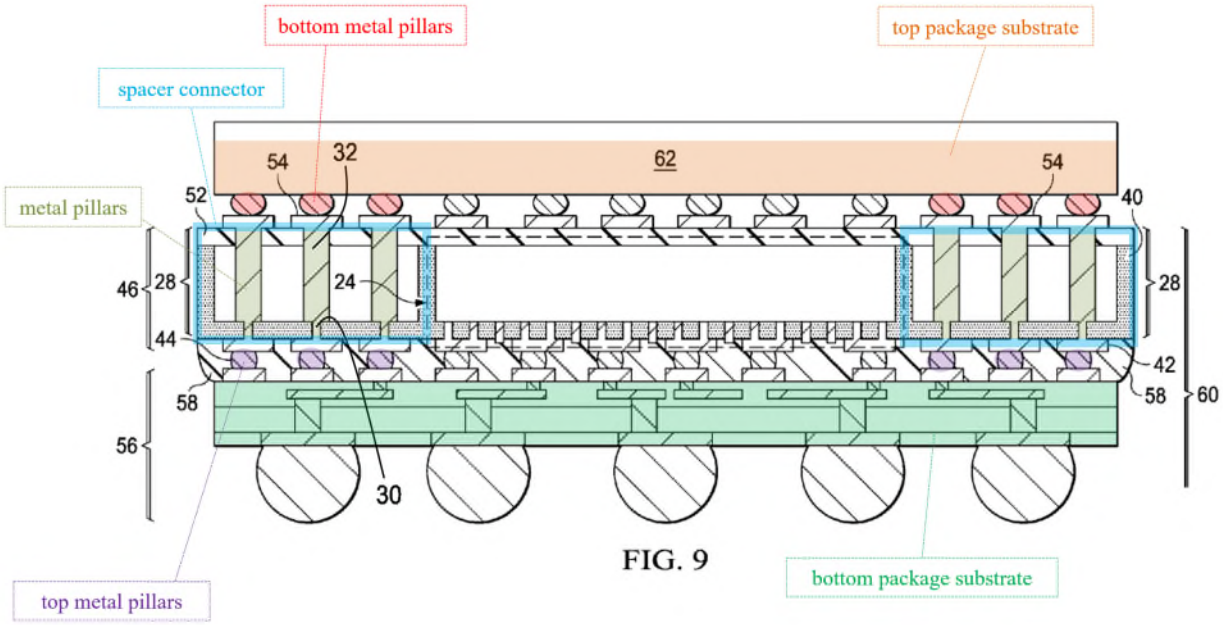


FIG. 9

As discussed in §V.C, because (upper) connectors 44 (bottom metal pillars) and (lower) connectors 44 (top metal pillars) are associated with (on the surface of) *Chen*'s top and bottom package substrate, respectively, a POSITA would have recognized that "bottom metal pillars of the top package substrate" and "top metal pillars of the bottom package substrate" are met. EX1003, ¶242.

1[k]

Chen discloses "package component 24 includ[ing] one or a plurality of device dies [bottom chip]," arranged in the space between package substrate in top package component 62 (top package substrate) and package component 56 (bottom package substrate). EX1006, [0009]("Package component 24 may include a Central Computing Unit (CPU) ***die*** or another type of ***logic die*** having logic circuits."),

[0020], FIGs. 9-11(showing package component 24 arranged between top package component 62 and package component 56); EX1003, ¶¶244-45.

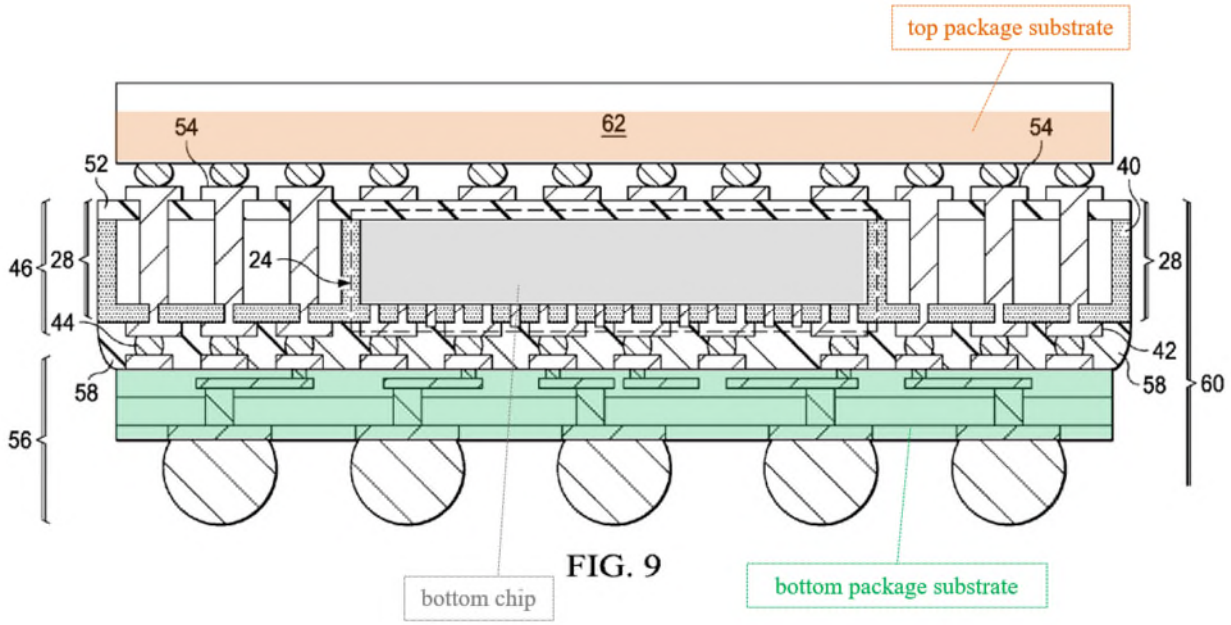


FIG. 9

EX1006, FIG. 9.

1[l]

Chen discloses package component 24 (bottom chip) is mounted on the top surface of package component 56 (bottom package substrate). EX1003, ¶¶246-47; EX1006, FIG. 9; *see also id.*, [0018], FIG. 8 (showing package component 24 mounted to the top surface of package component 56 via connectors 44), [0024]; §VII.D.i.(1[k]).

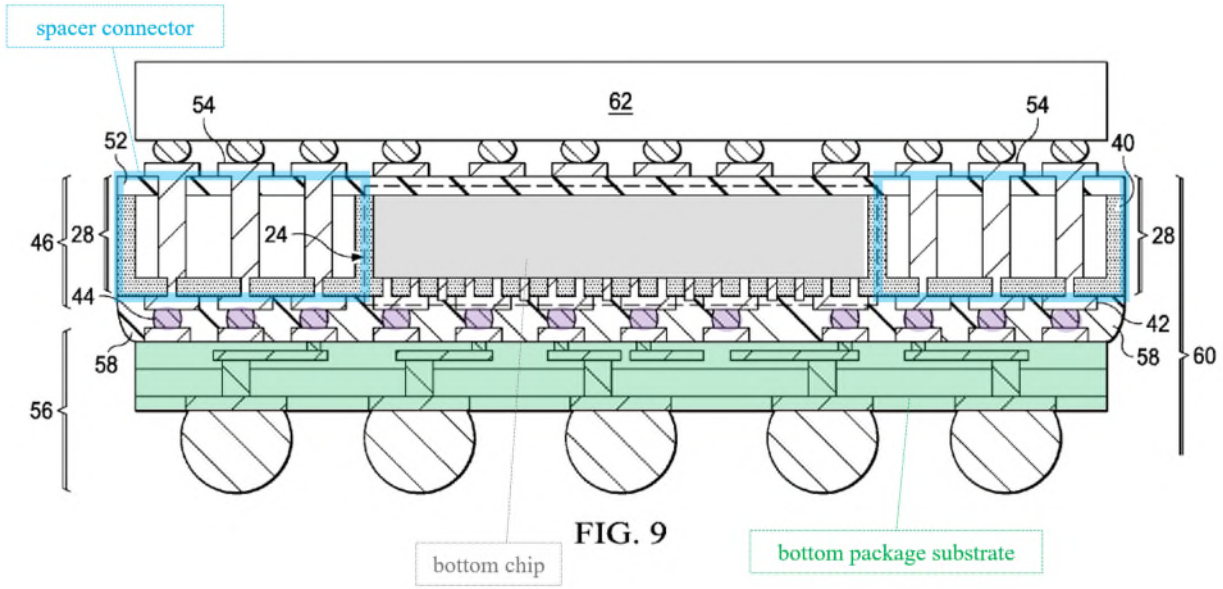


FIG. 9

EX1006, FIG. 9.

1[m]

Chen discloses "***two*** TAV modules 28" (spacer connector) "disposed on ***opposite sides*** of package component 24" (bottom chip). EX1006, [0012], [0022], FIGs. 2, 9, 12; EX1003, ¶¶248-50.

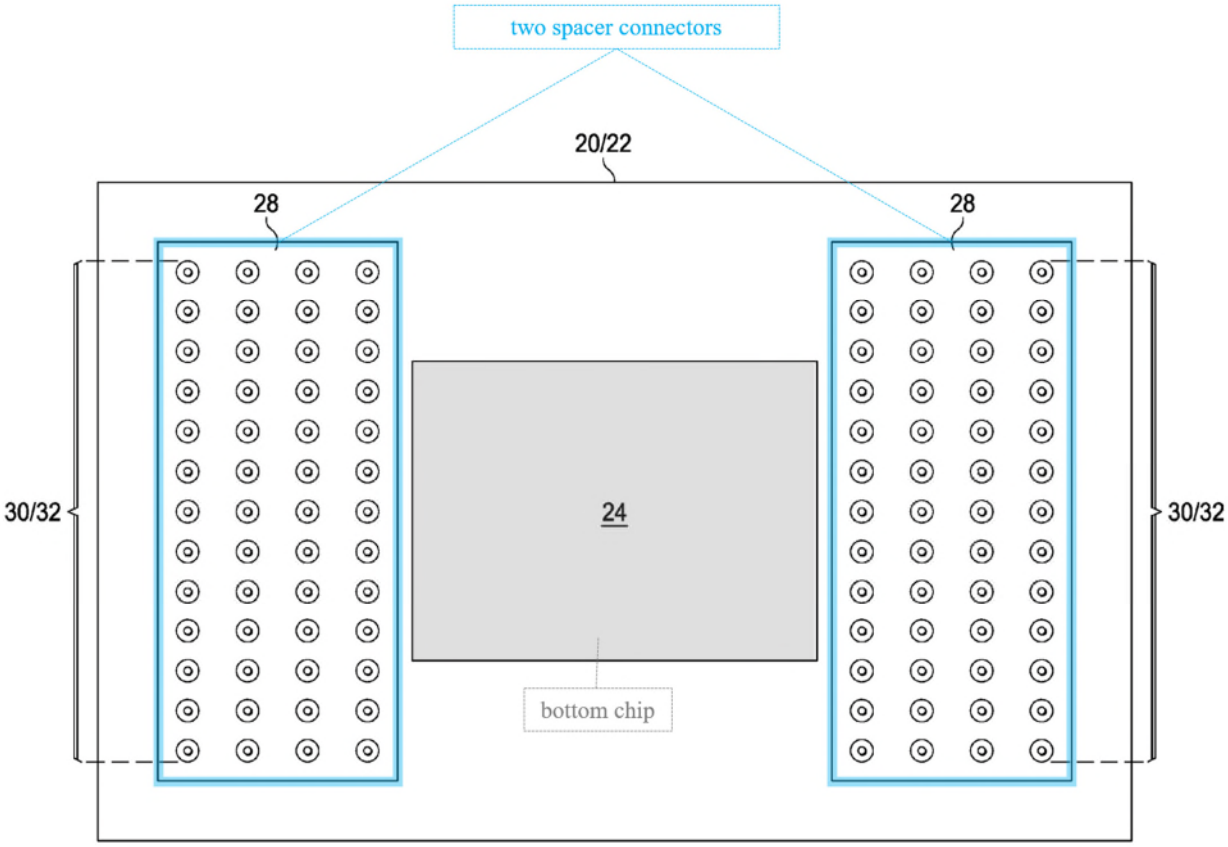


FIG. 2

EX1006, FIG. 2 (top view).

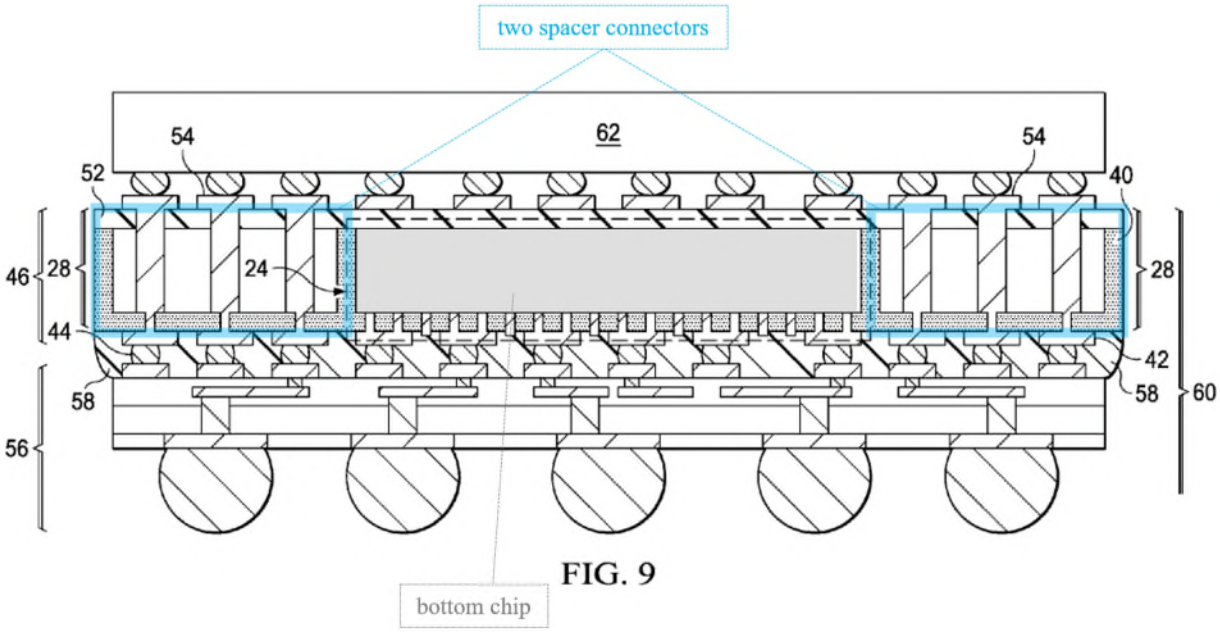


FIG. 9

EX1006, FIG. 9.

ii. Dependent Claims 2-9

Claim 2

As discussed in §VII.D.i.(1[k]-[l]), *Chen*'s package component 24 (bottom chip) is placed below package substrate in top package component 62 (top package substrate), and thus a top surface of package component 24 is spaced downwardly from the bottom surface of the top package substrate. EX1003, ¶¶251-52; EX1006, [0019], [0020], [0024], FIG. 9:

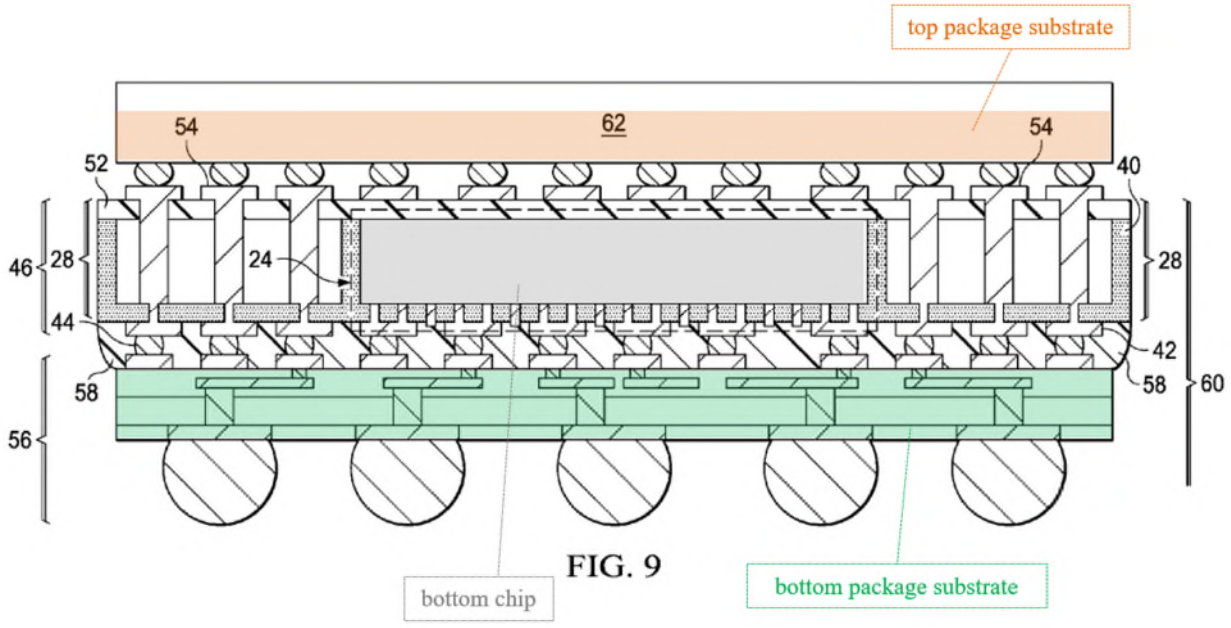


FIG. 9

Claim 3[a]

Chen discloses a top chip (in top package component 62) mounted to the top surface of the top package substrate (also in top package component 62). EX1003, ¶¶253-54. *Chen*'s top package component 62 may be "a package that includes a

device die (not shown) bonded to a ***package substrate*** (not shown)." EX1006, [0019]. When a device die is "bonded to" a package substrate, the device die is mounted to the top of the package substrate, which in turn interfaces with the spacer connector as discussed in §VII.D.i.(1[j]). EX1003, ¶253; *see also*, *e.g.*, EX1006, [0009], FIGs. 8-9.

Claim 3[b]

Chen's top package component 62 "include[s] a device die [top chip] bonded to a package substrate [top package substrate]." EX1006, [0019]. A POSITA would have found it obvious to include a device die that overlaps both package component 24 (bottom chip) and two TAV modules 28 (spacer connector) in a vertical direction in which *Chen*'s top package substrate is stacked on top of bottom package substrate. EX1006, [0019], FIG. 9; EX1003, ¶¶255-59.

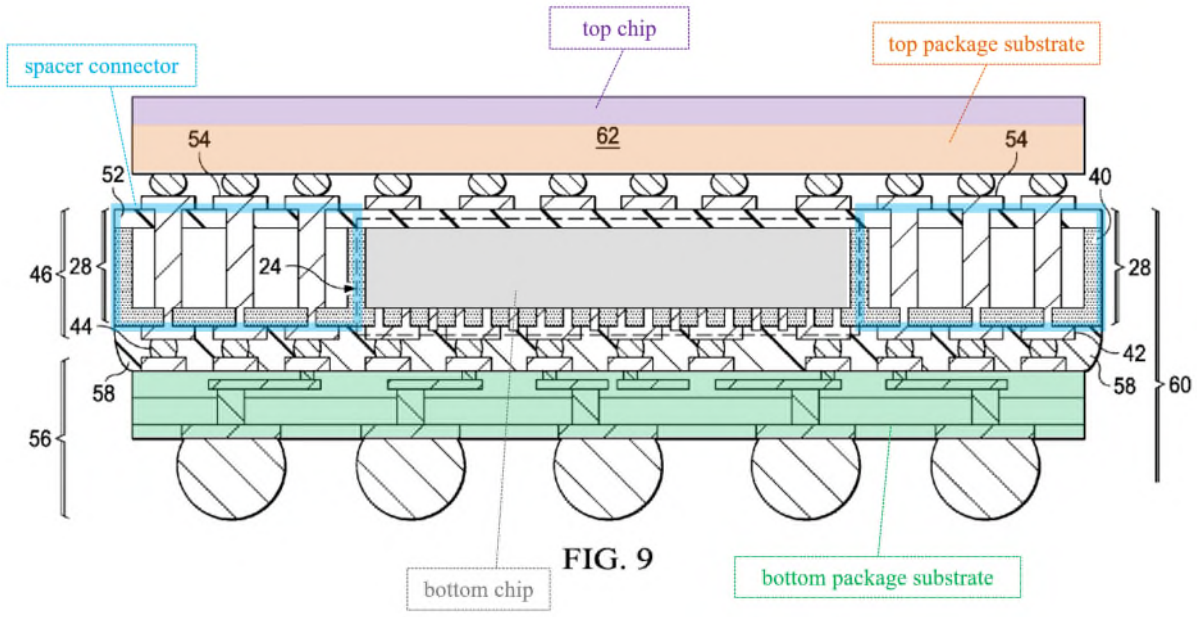


FIG. 9

EX1006, FIG. 9.

First, a POSITA would have found it obvious to combine embodiments of "top package component 62." EX1003, ¶256. In a first embodiment, *Chen* teaches "top package component 62" can be "a device die," directly interfacing with bottom package 60. EX1006, [0019], FIG.9; EX1003, ¶256. In a second embodiment, *Chen* discloses package component 62 as "a package that includes a device die…bonded to a package substrate," reflecting an alternative arrangement of mounting the die on a substrate, which interfaces with bottom package 60. EX1006, [0019], FIG. 9; EX1003, ¶256. A POSITA would have found it obvious to mount the device die—"top package component 62"—on a substrate to interface with bottom package 60, as direct interface and through-substrate interface are two alternatives taught by *Chen*. EX1003, ¶256. So mounted, the device die—package component 62—overlaps the bottom chip and each of the two spacer connectors. EX1003, ¶256.

Second, even just considering the second embodiment by itself, a POSITA would have found it obvious to include a top chip that overlaps the bottom chip and each of the two spacer connectors, as the top package substrate has more space for a larger chip than the bottom one, which is limited by the spacer connectors. EX1003, ¶¶257-58; *see, e.g.*, EX1005, FIG. 12 (showing top chips 30, 31 larger than bottom chip 200 are mounted on top package substrate 20). The size of the top die is no more than an obvious design choice for an application. EX1003, ¶¶257-58.

Accordingly, *Chen* renders obvious claim 3.

Claim 4

As discussed above in §VII.D.i.(1[j]), (upper) connectors 44 (bottom metal pillars), through-substrate vias 32 and metal posts 30 (metal pillars), and (lower) connectors 44 (top metal pillars) are used to electrically couple package substrate in top package component 62 (top package substrate) and package component 56 (bottom package substrate). EX1006, [0011], [0014], [0019], [0021], [0022], FIG. 9; EX1003, ¶¶260-61. For the electrical connection, each of (upper) connectors 44 is aligned with a corresponding through-substrate via 32 and metal post 30, and also with a corresponding (lower) connector 44 as shown in FIG. 9 (illustrated in a dashed red line).

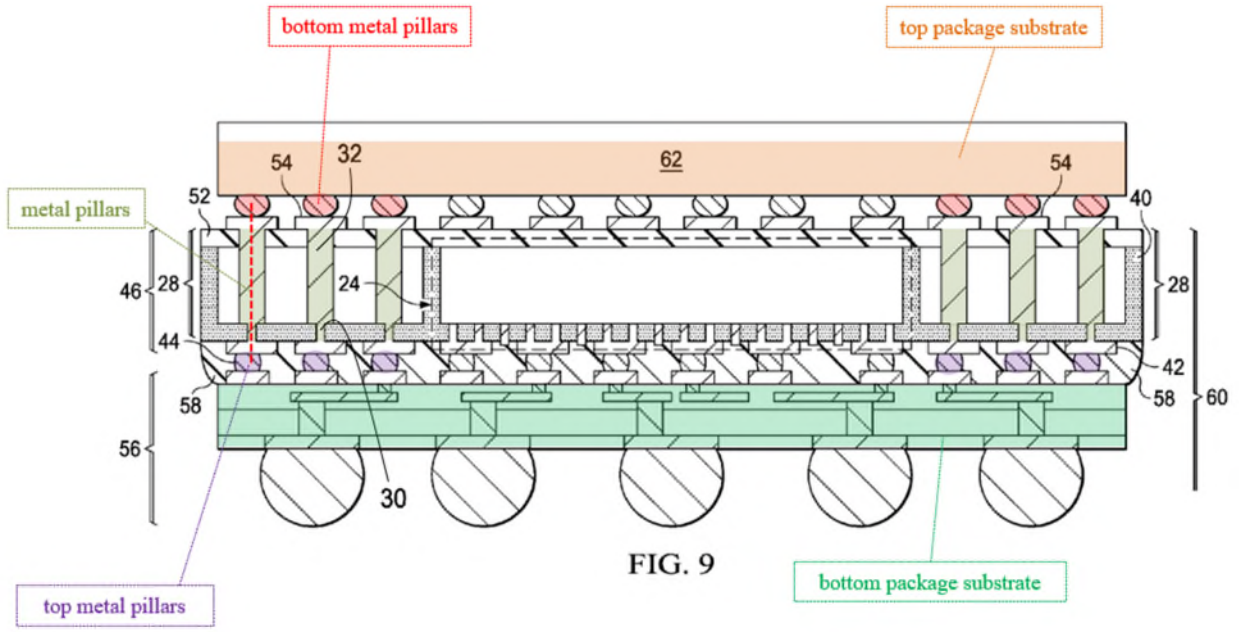


FIG. 9

EX1006, FIG. 9.

Claim 5[a]-[b]

Chen teaches TAV modules 28 (spacer connector) may ***not*** have a metal pad on the bottom ends of through-substrate vias 32 and metal posts 30 (metal pillars), which protrude downwardly from the bottom surface of substrate 34 (core substrate). EX1003, ¶¶262-64; *supra*, §VII.D.i.(1[g]). Specifically, *Chen* teaches "[a]lternatively, ***no*** redistribution layer is formed on ***either*** side of one or each of TAV modules 28," disclosing the option of omitting "Redistribution Lines (RDLs) 42" on the bottom surface of the core substrate. EX1006, [0011]; EX1003, ¶262.

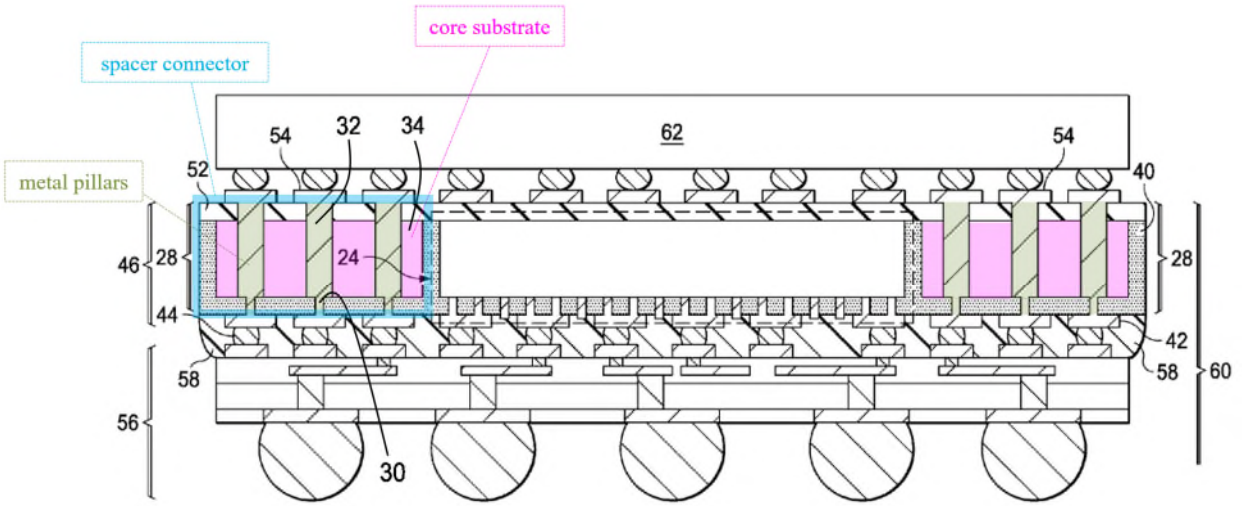


FIG. 9

EX1006, FIG. 9. In this design, the metal pillar and the corresponding top metal pad of the spacer connector form a T shape. EX1003, ¶262. Accordingly, *Chen* anticipates claim 5. EX1003, ¶262; *In re Petering*, 301 F.2d 676, 681 (C.C.P.A. 1962); *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed.

Cir. 2015) (holding "a reference can anticipate," when the reference discloses limited options, and thus a POSITA "would 'at once envisage' the claimed arrangement or combination."); *see also Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1344 (Fed. Cir. 2016) ("[A] reference need not always include an express discussion of the actual combination to anticipate.").

To the extent *Chen* does not expressly teach the absence of metal pads on the bottom ends of the plurality of metal pillars, a POSITA would have found it obvious not to include them as it is among the finite design options *Chen* discloses. EX1003, ¶¶263-64. Furthermore, it was well known in the art that two sets of metal pillars—e.g., metal posts 30 and (lower) connectors 44—can be directly bonded together without using an intermediate metal pad to minimize process steps and assembly costs. EX1003, ¶263; *see*, *e.g.*, EX1008, FIG. 3 (showing two sets of metal pillars 300 and 27 are directly bonded without a metal pad).

Claim 6[a]

As discussed in §VII.D.i.(1[g]), *Chen* discloses a bottom end of each of metal posts 30 (metal pillars) protrudes downwardly from a bottom surface of substrate 34 (core substrate). As discussed in §VII.D.i.(1[i]), through-substrate vias 32 and metal posts 30 are directly stacked on (lower) connectors 44 (top metal pillars) to form a conductive path to package component 56 (bottom package substrate). EX1006, [0014], FIGs. 8-9. Accordingly, the bottom ends of metal posts 30 are connected, in

"an end-to-end manner," to corresponding top ends of (lower) connectors 44, while RDLs 42 merely serve as an intermediate interconnect feature that facilitates electrical continuity between those metal pillars.[15] EX1003, ¶¶265-66, 268.

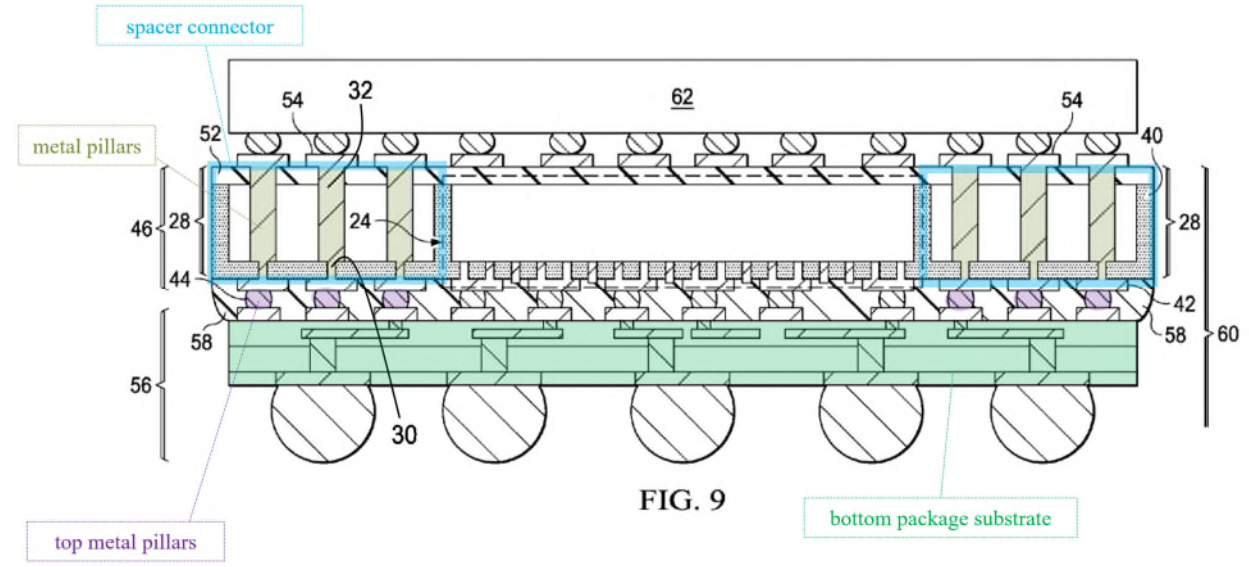


FIG. 9

EX1006, FIG. 9.

To the extent "an end-to-end manner" requires ***direct*** connection between the bottom ends of metal pillars ***without a metal pad*** and the corresponding top ends of top metal pillars, *Chen* still discloses and/or renders this limitation obvious. EX1003, ¶267. As discussed above for §VII.D.ii.(5[a]-[b]), *Chen* teaches RDLs 42 may be omitted, when two metal pillars (i.e., metal posts 30 and (lower) connectors 44) are connected in "an end-to-end manner," as well known in the art. EX1003, ¶267; EX1006, [0011]; EX1008, FIG. 3.

[15] *See also supra* n.7.

Claim 6[b]

As discussed above in §VII.D.i.(1[f], [h]), bottom ends of (upper) connectors 44 (bottom metal pillars) of package substrate in top package component 62 (top package substrate) are connected to the corresponding top ends of through-substrate vias 32 (metal pillars) of TAV modules 28 (spacer connector) via the corresponding RDLs 54 (top metal pads). EX1003, ¶¶269-70; *see also* EX1006, [0017] ("RDLs 54 are then formed on dielectric layer 52."), [0018] ("RDLs 54 are exposed through the respective molding compound (not shown)."), FIGs. 7-9.

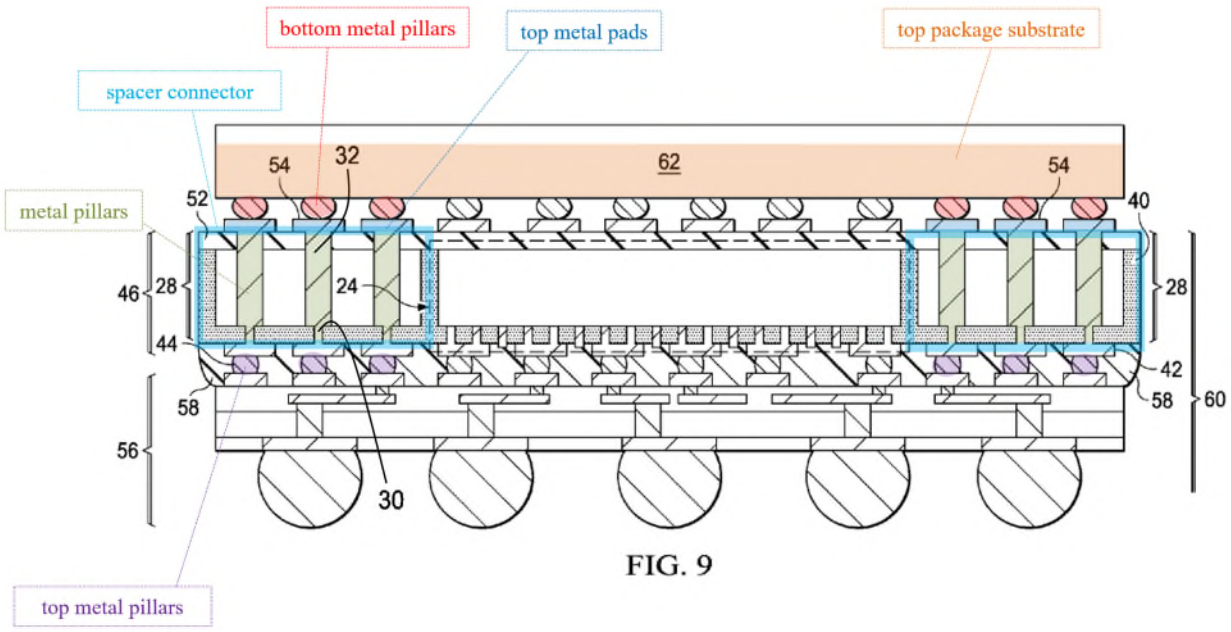


FIG. 9

EX1006, FIG. 9.

Claim 7[a]-[b]

Chen discloses TAV modules 28 (spacer connector) include polymer 40 (dielectric layer) on the bottom surface of substrate 34 (core substrate). EX1003, ¶¶271-74; EX1006, FIG. 9; *see also id.*, [0013](noting "polymer 40 is filled…into the gaps between metal posts 30"), [0017]("***dielectric layer*** 52 include[ing] a ***polymer***, which may be polyimide, benzocyclobutene (BCB), or the like"), [0023], [0025]("The polymer is ground to expose…metal posts [30] of the TAV module."), FIG. 3. Moreover, through-substrate vias 32 and metal posts 30 (metal pillars) pass through substrate 34 (core substrate), *supra*, §VII.D.i.(1[e]), and polymer 40 (dielectric layer), which "fill[s]…gaps between metal posts 30." EX1006, [0013], FIG. 9 (showing metal posts 30 pass through polymer 40 in dashed red line).

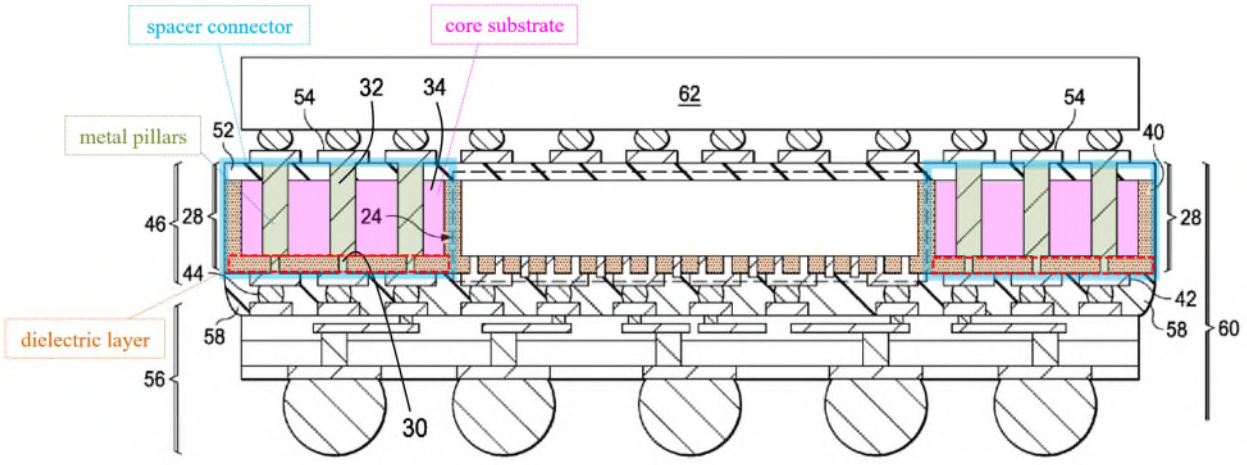


FIG. 9

EX1006, FIG. 9.

Claim 8

Chen's polymer 40 (dielectric layer) is a dielectric ***adhesive*** in which substrate 34 (core substrate) is pasted. EX1003, ¶¶275-77. *Chen* discloses polymer 40 is "adhesive" because "[p]olymer 40 may include…a molding ***underfill***, or a kind of ***epoxy***," EX1006, [0013], and in "microelectronic packaging" "[p]olymer ***adhesives*** are commonly used as ***underfills***" and "[t]he materials used are typically unfilled ***epoxies***." EX1009, 1, 3; EX1003, ¶275.

To the extent *Chen* does not explicitly disclose polymer 40 as a dielectric adhesive, a POSITA would have also found it an obvious design choice. EX1003, ¶276-77. It would have been desirable for polymer 40 to have adhesive properties to be pasted underneath core substrate 34, as insulating polymer ***adhesives*** are commonly used as underfills in applications like *Chen*'s polymer 40 to provide known benefits including stress relief. EX1003, ¶276; *see also* EX1009, 3, 6, 13.

Claim 9[a]

Chen discloses TAV modules 28 (spacer connector) include multiple Redistribution Lines (RDLs) 42 (bottom metal pads), each "formed" on the bottom end of a corresponding metal post 30 (metal pillar). EX1006, [0014], FIG. 9; EX1003, ¶¶278-79. "RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer." EX1006, [0014], [0011] ("TAV modules 28 may include redistribution layer(s) that include redistribution lines and ***metal pads***," such as

RDLs 42.). Moreover, *Chen* discloses and/or renders obvious "bottom metal pads" for the same reasons discussed above for VII.D.i.(1[f]). EX1003, ¶278.

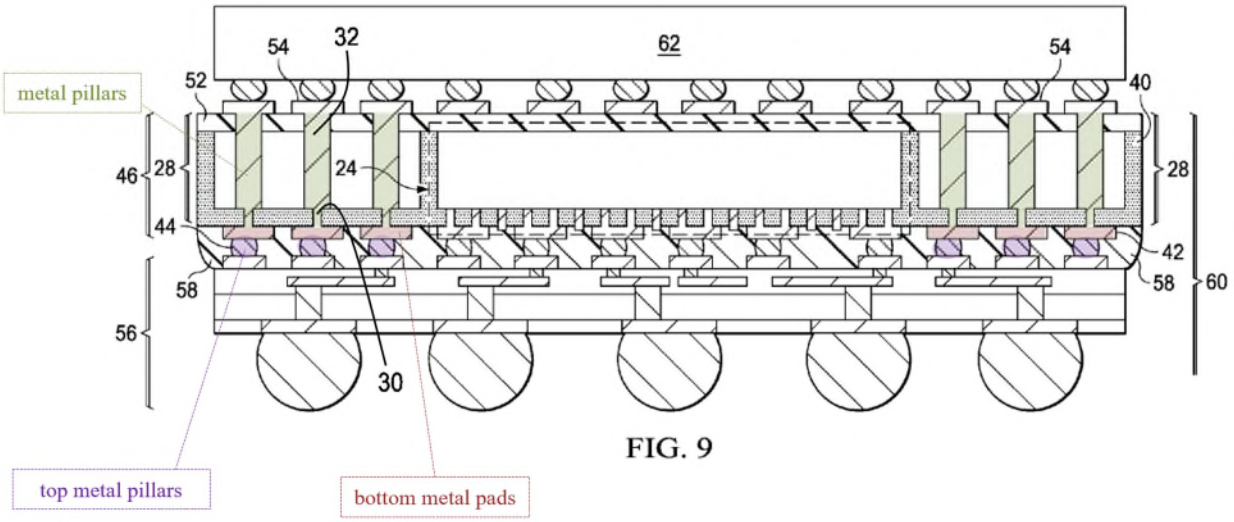


FIG. 9

EX1006, FIG. 9.

Claim 9[b]

Chen discloses and/or renders obvious, as shown in FIG. 9 below, the bottom ends of metal posts 30 (metal pillars) are connected to corresponding top ends of (lower) connectors 44 (top metal pillars) via the corresponding RDLs 42 (bottom metal pads). EX1003, ¶¶280-81; EX1006, [0014] ("Redistribution Lines (RDLs) 42 and [lower] connectors 44 are formed to connect to metal posts…30."), [0011].

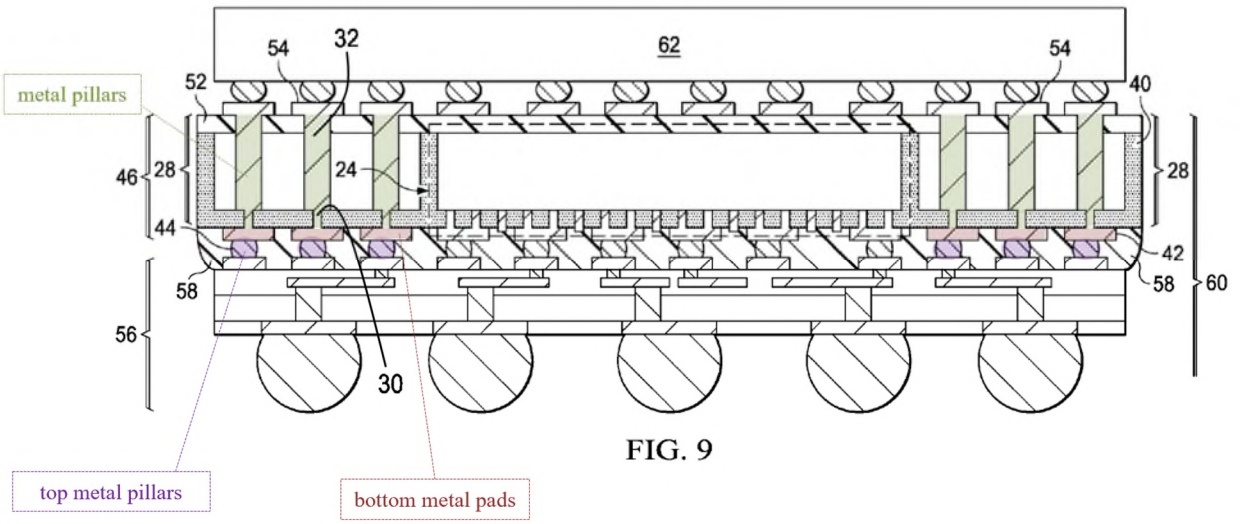


FIG. 9

EX1006, FIG. 9.

Claim 9[c]

Limitation 9[c] is identical to limitation 6[b], and thus disclosed and/or rendered obvious for the same reason. §VII.D.ii.(6[b]); EX1003, ¶282.

E. GROUND 7: *CHEN* WITH *HU*

Chen with *Hu* renders obvious claims 1-9.

i. Motivation to Combine

Both *Chen* and *Hu* are directed to the structure and process of "Package-on-Package (POP)," where "a top package is bonded to a bottom package." EX1006, [0001]; EX1008 [0001] ("package on package (PoP) structure"); EX1003, ¶284.

Each identifies shortcomings of using solder balls in PoP structures. EX1003, ¶285. *Chen* explains that, in conventional PoP processes, "solder balls are used" to connect package substrates, but "the amount of the solder balls that can be used in a

PoP structure is limited" because "the lateral sizes of the solder balls are [] large." EX1006, [0002]. As discussed above in §VII.C.i, *Hu* similarly identifies drawbacks of solder balls. EX1008, [0004] ("a tilted stack structure," "poor coplanarity," "positional deviation," and "solder bridge"); *supra*, §VII.C.i.

As discussed in §§VI.B, VII.A.i, *Chen* teaches a PoP structure that includes top package component 62, package component 56, and "Through-Assembly Via (TAV) Module [28], which includes a substrate [and] a plurality of through-vias penetrating through the substrate." EX1006, Abstract, [0010], [0019], FIG. 9 (below). TAV Module 28 is electrically coupled to the bottom and top package component via connectors 44. *Id*., [0014], [0019], FIGs. 4, 9.

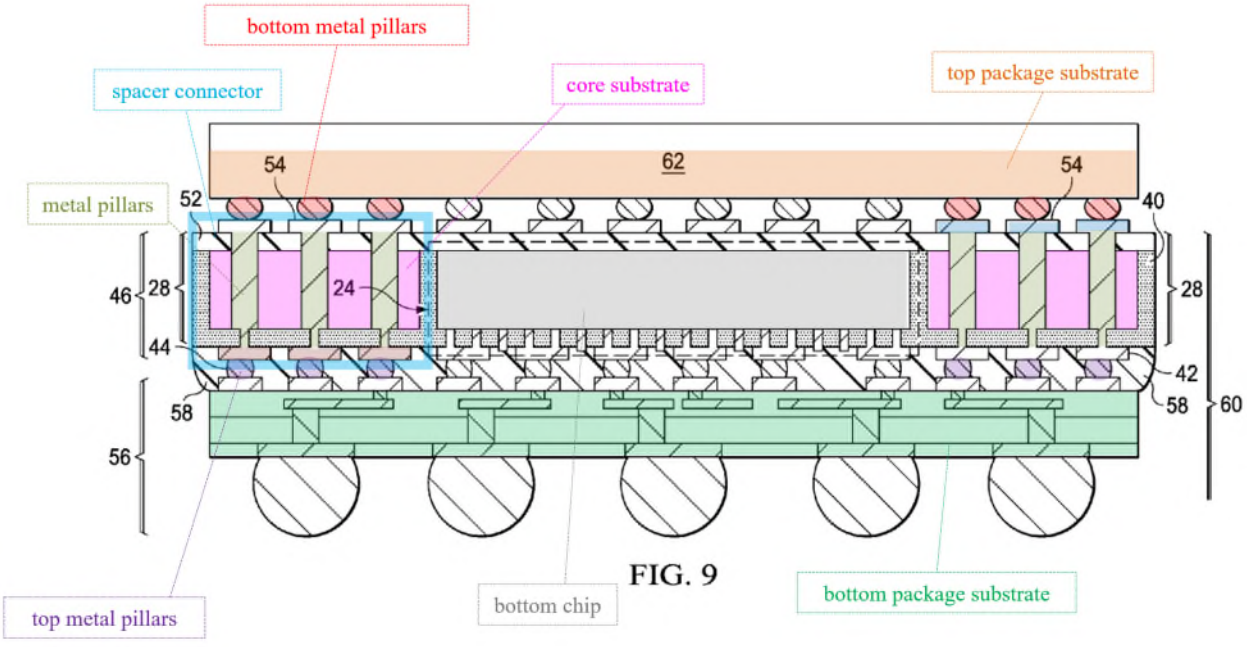


FIG. 9

EX1006, FIG. 9.

While *Chen* teaches the use of "metal pillars" as alternatives to solder balls for connectors 44, it does not provide fabrication details. EX1006, [0014], FIGs. 4, 8-9; EX1003, ¶287.

A POSITA would have been motivated to look to *Hu* for guidance on how to implement *Chen*'s connectors 44 as metal pillars (posts) in a practical and reliable manner. EX1003, ¶288. *Hu* expressly teaches "metal posts…are used in stack structures so as to overcome the above-described drawbacks" of solder balls (EX1008, [0005], [0007]) and further provides detailed process steps to form metal pillars with improved uniformity. EX1008, [0008] (explaining the difficulty of controlling metal pillars' "uniformity"), FIG. 1, [0028]-[0035] (process steps to form uniform metal pillars), FIGs. 2C-2F, [0013] (resulting metal pillars with "same height"); *supra*, §VII.C.i. Applying *Hu*'s detailed metal-pillar implementation to *Chen*'s interconnects, such as connectors 44, would have been a logical and predictable design choice to "prevent[] tilt of the packaging substrate [] during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability," as taught by *Hu*. EX1008, [0038]; EX1003, ¶288.

Specifically, a POSITA would have followed the process steps of *Hu* to first prepare bottom and top metal pillars on *Chen*'s top and bottom package substrates, respectively, before bonding these package substrates with TAV modules 28 via the bottom/top metal pillars. EX1003, ¶¶289-90; EX1006, [0014], [0019]; EX1008,

[0025]-[0028]. This way, the height of the metal pillars can be adjusted using conductive bonding layers to achieve good coplanarity as taught by *Hu*. EX1003, ¶291; EX1008, [0008], [0029]-[0030], EX1006, FIG. 9 (modified to illustrate the *Chen-Hu* device):

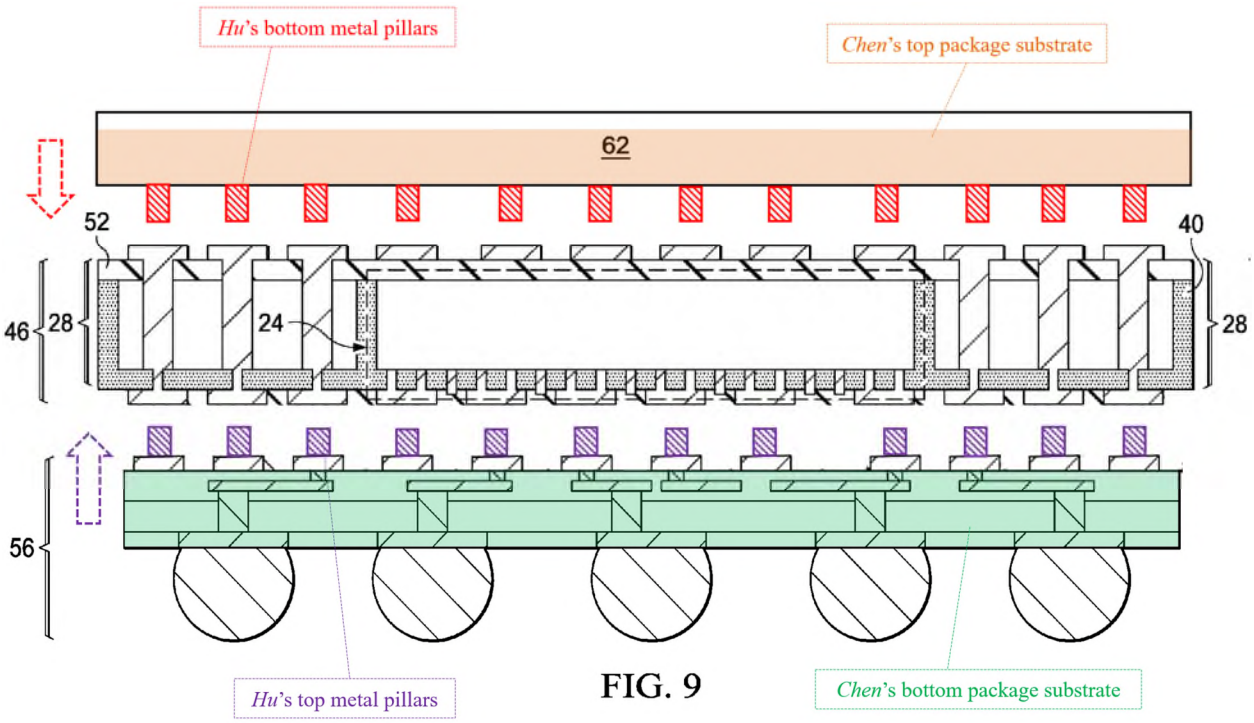


FIG. 9

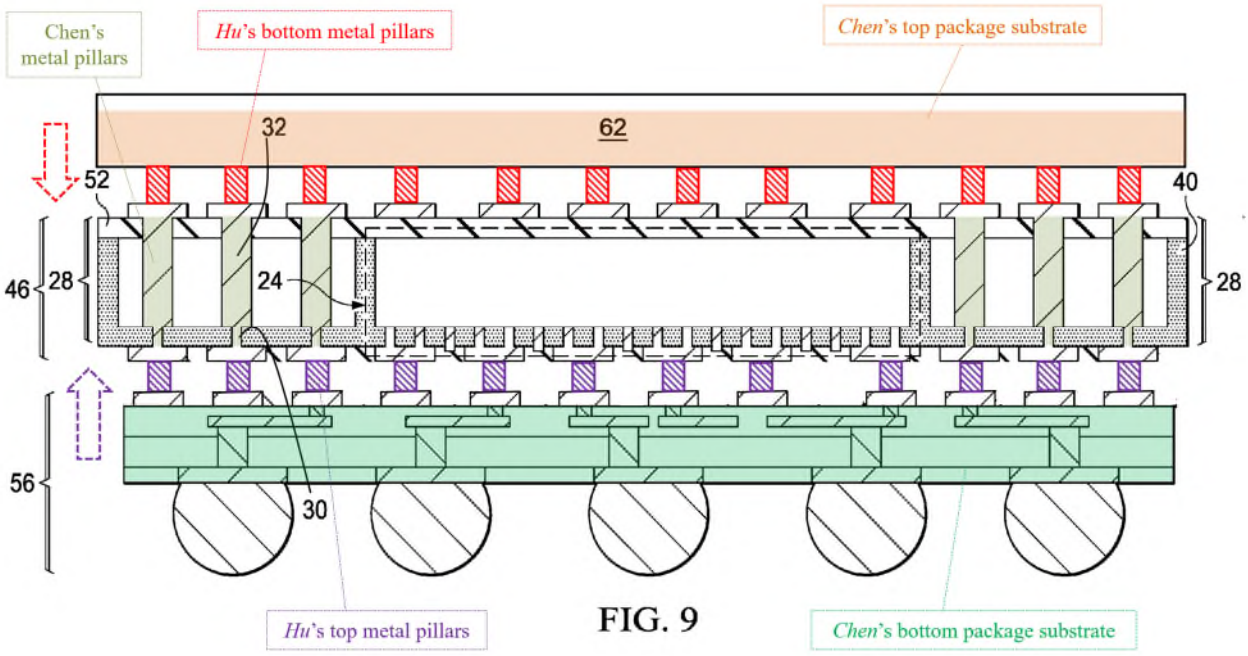


FIG. 9

A POSITA would have had a reasonable expectation of success in making the proposed combinations. EX1003, ¶292. *Chen* contemplates using "metal pillars" for connectors 44. EX1006, [0014]. Meanwhile, *Hu* provides detailed, working examples of metal pillars formed by the "electroplating process" and used as PoP interconnects, along with solutions for achieving uniform height and improved coplanarity. EX1008 [0028]-[0035], FIGs. 2C-2F. The *Chen-Hu* combination therefore involves nothing more than applying known elements (metal pillars) in a known structure (PoP) using known methods (electroplating) to achieve their well-understood and predictable function (providing reliable electrical and mechanical connections). EX1003, ¶292. This is the type of combination that a POSITA would reasonably expect to succeed without undue experimentation, as it relies on

established semiconductor packaging techniques and addresses known, well-documented problems of solder-ball-based PoP connectors. *Id*.

ii. Claims 1-9

As discussed above, the combination of *Chen* and *Hu* does not materially alter the final package structure of *Chen* but merely implement *Chen*'s connectors with *Hu*'s metal pillars and processing steps, by first forming the bottom and top metal pillars on the top and bottom package substrates, respectively, before bonding the substrates with the spacer connectors (TAV modules 28) to avoid tilted package stack as taught by *Hu*. EX1003, ¶293. Accordingly, *Chen-Hu* renders obvious "bottom" and "top metal pillars" for the reasons discussed in §§VII.D.i.(1[h]-[i]), VII.E.i., and thus renders obvious claims 1-9 for the same reasons discussed above in Grounds 5-6.

To the extent that the Board disagrees with Petitioners' proposed construction for the "of" terms—i.e., "bottom metal pillars of the top package substrate" and "top metal pillars of the bottom package substrate" (1[h]-[j], 4, 6, 9) and instead requires the bottom metal pillars be built as part of the top package and the top metal pillars as part of the bottom package prior to assembling the PoP assembly, *Chen-Hu* renders obvious claims 1-9 for the same reasons discussed above, even under that narrow construction, because the structural design of *Chen-Hu* is materially identical to *Chen*. EX1003, ¶294; §§VII.D., VII.E.i.

F. GROUND 8: *CHEN* WITH *HU* AND *BENSON*

Chen with *Hu* and *Benson* renders obvious claim 8.

i. Motivation to Combine

As discussed in §VII.E.i, *Chen-Hu*'s PoP structure only implements *Chen*'s connectors 44 as *Hu*'s metal pillars, and is otherwise identical to *Chen*'s PoP structure, including using "polymer 40" as "underfill." EX1006, [0013]; EX1003, ¶296.

A POSITA would have been motivated to implement polymer 40 (dielectric layer) as "adhesives" in *Chen-Hu*'s PoP structure in view of *Benson*'s teaching about "the use of ***polymer adhesives*** in microelectronic packaging." EX1009, 1; EX1003, ¶¶297-300.

Chen-Hu teaches a PoP structure where "polymer 40 is filled into the gaps between metal posts 26, and into the gaps between metal posts 30" and "[p]olymer 40 may include a molding compound, a molding ***underfill***, or a kind of ***epoxy***." EX1006, [0013].

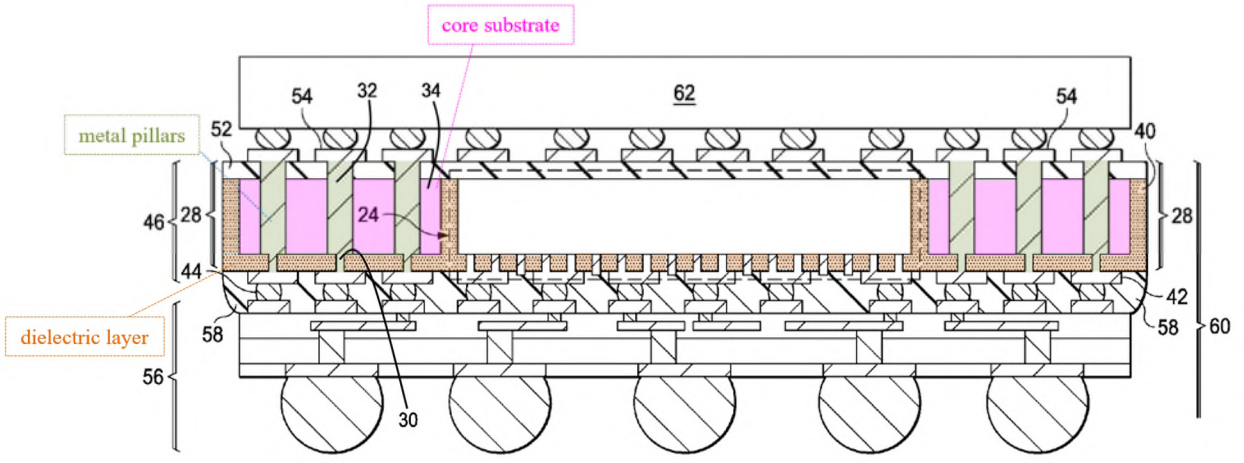


FIG. 9

EX1006, FIG. 9.

Benson teaches, in "microelectronic packaging," like *Chen-Hu*'s PoP, "***[p]olymer adhesives*** have been widely used." EX1009, 1. *Benson* also discloses "the general types of materials used to formulate polymer adhesives for die attachment, underfills, and encapsulants, along with their properties." *Id*., 13. Moreover, "[p]olymer adhesives are commonly used as ***underfills***," which *Chen* provides as an example of its polymer 40, "in order to distribute stress" that may occur during packaging process and testing, such as "temperature cycling." *Id*., 1. *Benson* further teaches that "[w]hen thermal or electrical conductivity is not required [like *Chen*'s polymer 40], insulating polymer adhesives are used for bonding…semiconductor die to substrates" and that "[t]he materials used are typically unfilled ***epoxies***." *Id*., 3. *Benson* also provides technical details about "polymer adhesives" used as "underfills," including their types (e.g., "capillary flow

underfills" and "no-flow underfills"), processing conditions, and relative advantages and disadvantages. *See, id*., 6-7.

Moreover, a POSITA would have had a reasonable expectation of success in implementing *Chen-Hu*'s polymer 40 with *Benson*'s polymer dielectric adhesives, which involves nothing more than applying known materials of "insulating polymer adhesives," such as "underfills" (EX1009, 3; EX1006, [0013]), in a known PoP structure, like *Chen-Hu*'s, to achieve their well-understood and predictable function of attaching a substrate and filling gaps between metal components. EX1003, ¶301.

ii. Claim 8

As discussed above in §VII.F.i, *Chen-Hu* in view of *Benson* renders obvious that polymer 40 is a dielectric adhesive where substrate 34 (core substrate) is pasted. EX1003, ¶¶302-03.

G. GROUND 9: *WAITE* WITH *IPC-4761*

Waite with *IPC-4761* renders obvious claims 1-2, 4, 6, 9, according to PO's apparent claim interpretations. *See* §V.B.

i. Motivation to Combine

Both *Waite* and *IPC-4761* are directed to printed circuit board assemblies. EX1003, ¶305; EX1010, 1:16-18 ("Embodiments of the invention are related [to] spacer/connector interfaces between daughter boards connected to printed circuit boards and test equipment interfaces"), 4:19-26, 10:3-5, 4:18-4:61; EX1011, 7

("This guideline provides [printed wiring board] designers, fabricators, and/or users with information on existing methods for the protection of vias on printed boards.").

Waite discloses a circuit board assembly wherein daughter board 202 is stacked onto motherboard 200, and the boards are interposed by spacer connector 204. EX1010, 6:25-28, FIG. 7. *Waite* further discloses a plurality of signal vias 402 and ground vias 428 (metal pillars) within spacer connector 204. EX1010, 6:59-61. However, *Waite* does not provide a detailed design for vias 402, 428, and is silent on whether they protrude below a bottom surface of the spacer connector 204. EX1003, ¶306.

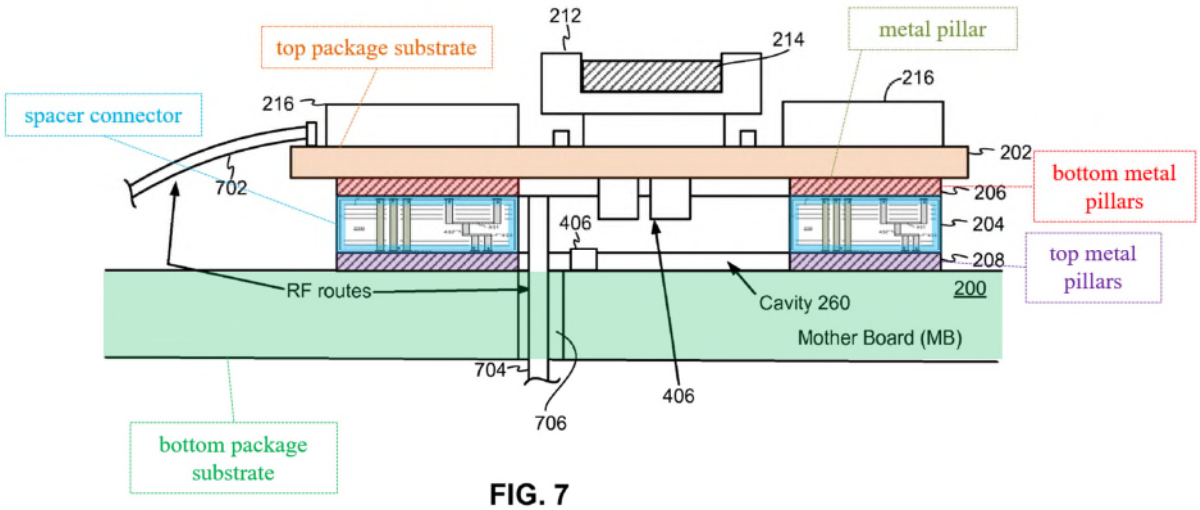
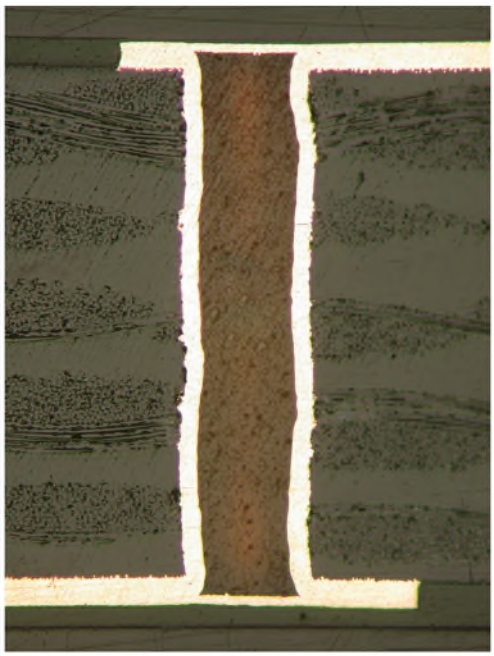


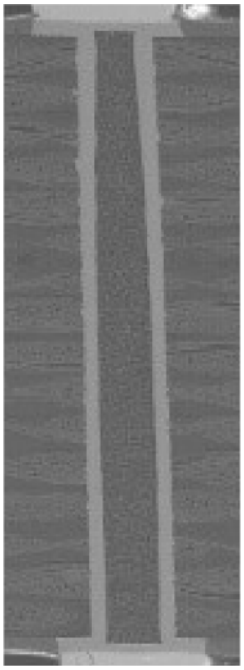
FIG. 7

EX1010, FIG. 7.

IPC-4761, however, provides such guidance, filling the gap in *Waite*'s disclosures. *IPC-4761* provides a known standard design for vias (metal pillars) that

are similar to the design of the products accused in PO's Complaint. EX1011, 16; EX1004, ¶44.





Compare EX1011, 16 *with* EX1004, ¶44.

This via structure would have been an obvious design choice, as a POSITA would have consulted *IPC-4761*, an industry standard, to construct *Waite*'s vias 402, 428. EX1003, ¶308; EX1011, 1. Moreover, a POSITA would have had a reasonable expectation of success to apply *IPC-4761*'s teachings, a standard technique, to a well-known via structure. EX1003, ¶308.

ii. Independent Claim 1

1[pre]

Waite discloses a circuit board assembly structure. EX1010, 2:10-11; EX1003, ¶¶309-10.

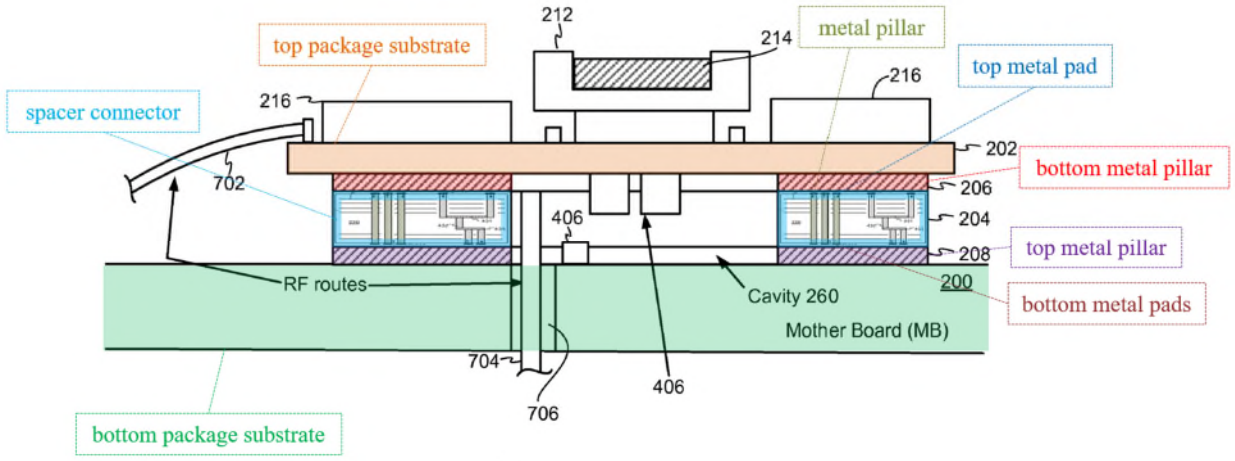


FIG. 7

EX1010, FIG. 7.

1[a]

According to PO's apparent interpretation, *Waite* discloses a motherboard 200 (bottom package substrate). EX1003, ¶¶311-12; EX1010, 9:24-25; EX1004, ¶41 (reading "bottom package substrate" on a "logic board").

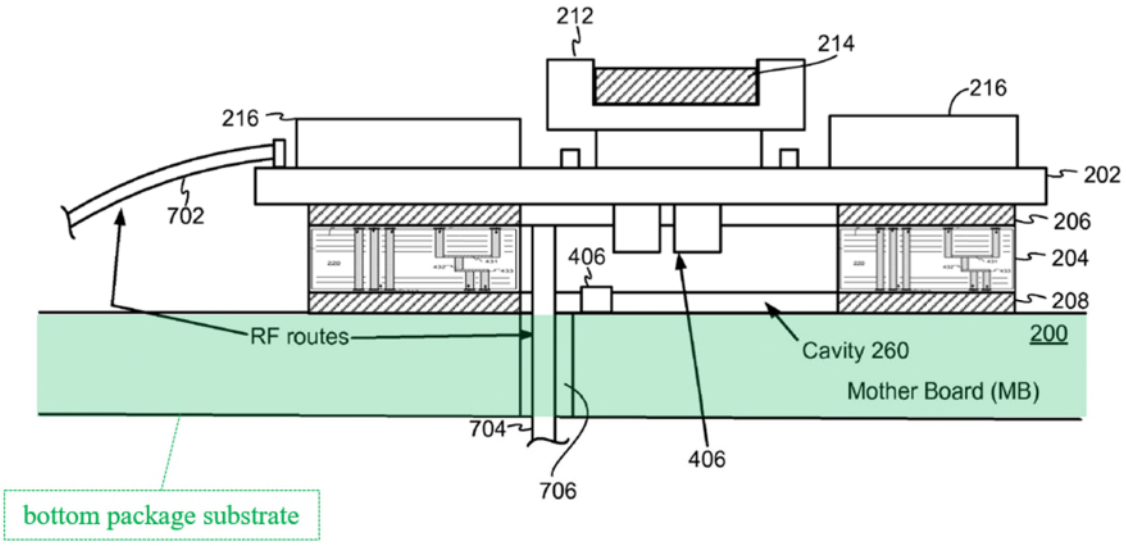


FIG. 7

EX1010, FIG. 7.

1[b]

According to PO's apparent interpretation, *Waite* discloses a daughter board 202 (top package substrate) stacked on top of motherboard 200 (bottom package substrate). EX1003, ¶¶313-14; EX1010, 9:24-25; EX1004, ¶42 (reading "top package substrate" on a "logic board").

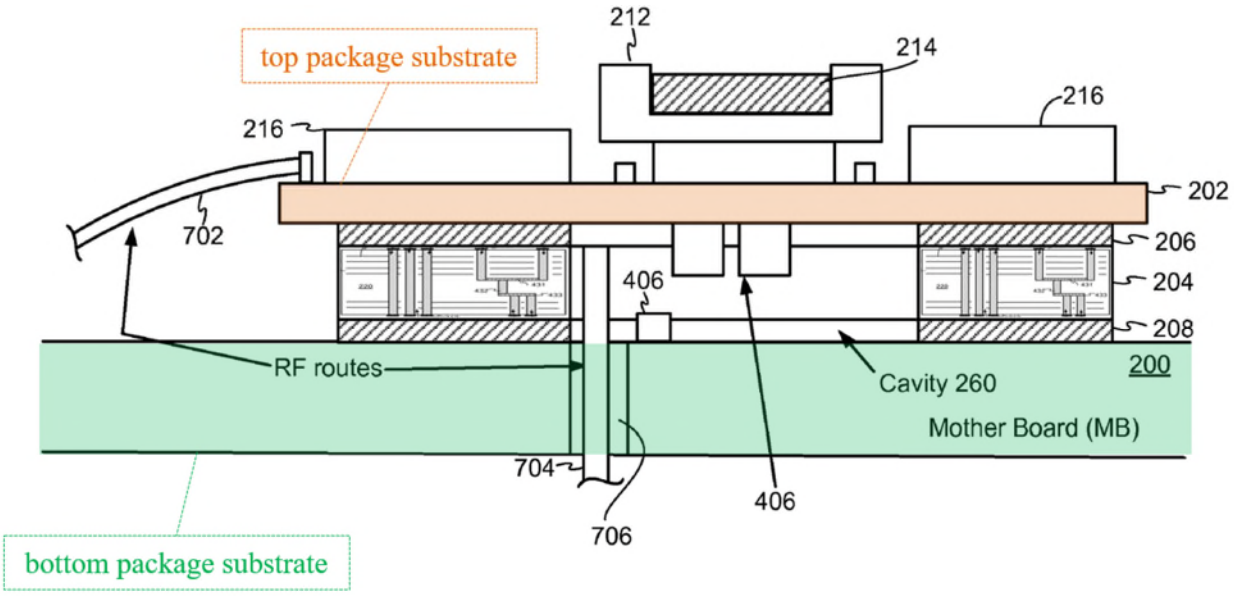


FIG. 7

EX1010, FIG. 7.

1[c]

Waite discloses two spacer connectors 204 interposed between daughter board 202 (top package substrate) and motherboard 200 (bottom package substrate) to define a space between daughter board 202 and motherboard 200. EX1003, ¶¶315-16; EX1010, 4:3-11, FIGs. 2A, 7.

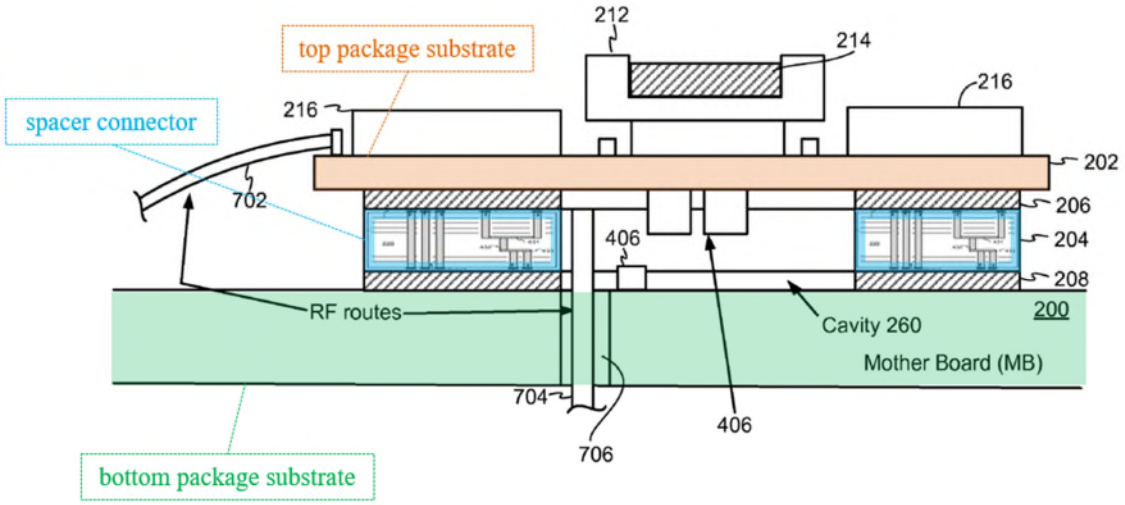


FIG. 7

EX1010, FIG. 7.

1[d]

Waite's spacer connectors 204 include a material 220 (core substrate). EX1010, 6:59-60; EX1003, ¶¶317-18. *Waite*'s material 220 includes PCB material (a substrate), which forms the core of spacer connector 204. EX1010, 2:14-15, 6:28-30 ("PCB can be any form of multilayer laminated, case or molded circuit board component"), FIG. 8.

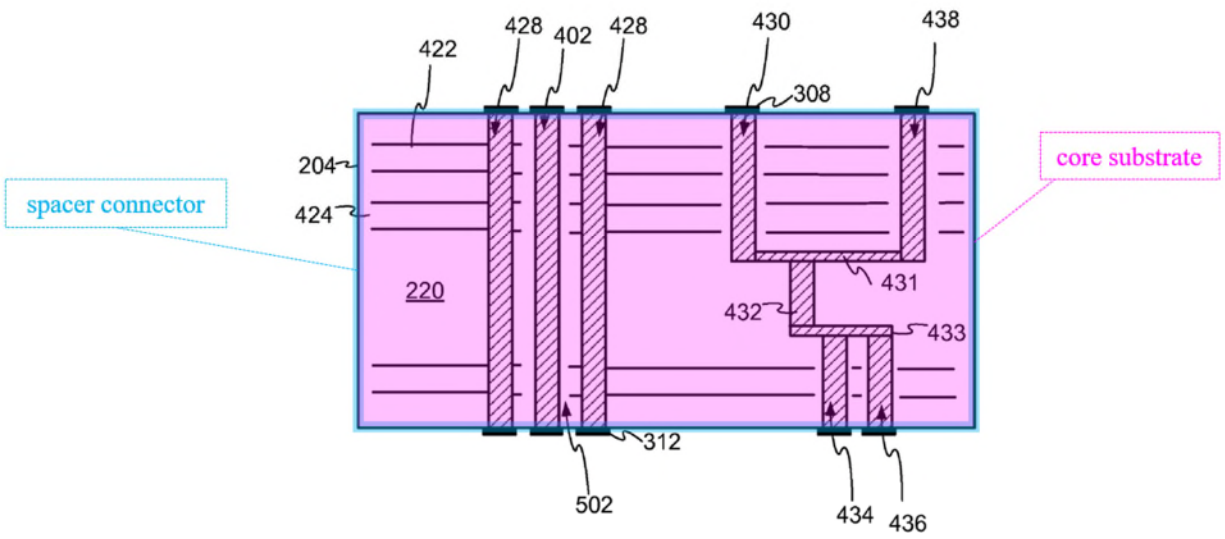


FIG. 8

EX1010, FIG. 8.

1[e]

Waite's spacer connectors 204 include a plurality of vias 402, 428 (metal pillars), each passing through material 220 (core substrate). EX1003, ¶¶319-20. *Waite*'s vias 402, 428 pass through material 220 to interface with contact pads 308, 312 (top and bottom metal pads) disposed on either side thereof. EX1010, 6:59-61 (stating "spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428"), 10:3-5 ("Each via is connected to contact pads (308,312) affixed to it at each PCB surface.").

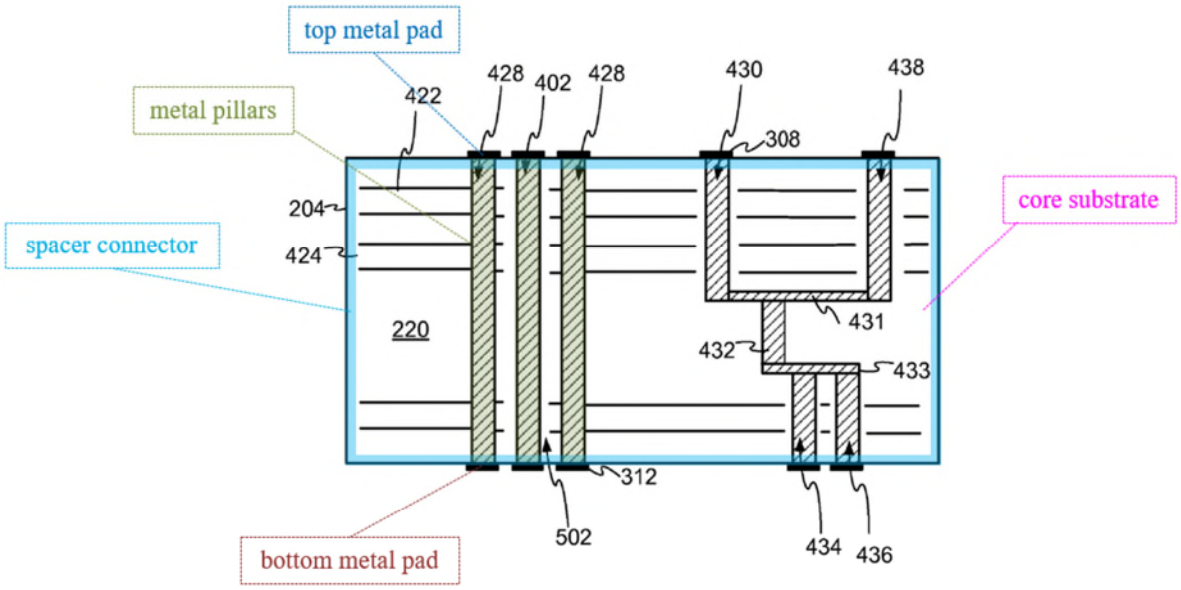


FIG. 8

EX1010, FIG. 8.

1[f]

Waite includes contact pads 308 (top metal pads), each on a top end of a corresponding via 402, 428 (metal pillar) among the plurality of vias 402, 428. EX1003, ¶¶321-22; EX1010, 10:3-5 ("Each via is connected to contact pads (308, 312) affixed to it at each PCB surface."), FIGs. 7, 8.

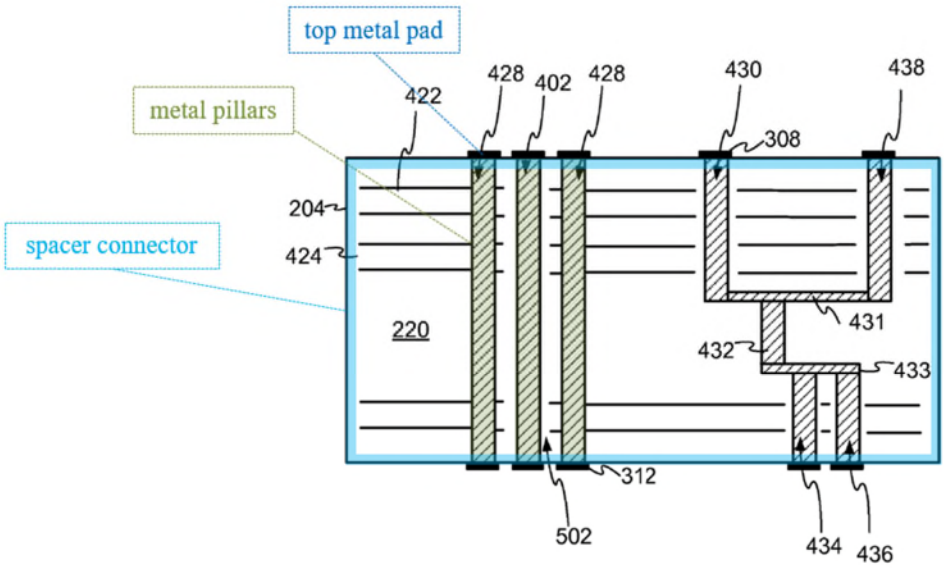


FIG. 8

EX1010, FIG. 8.

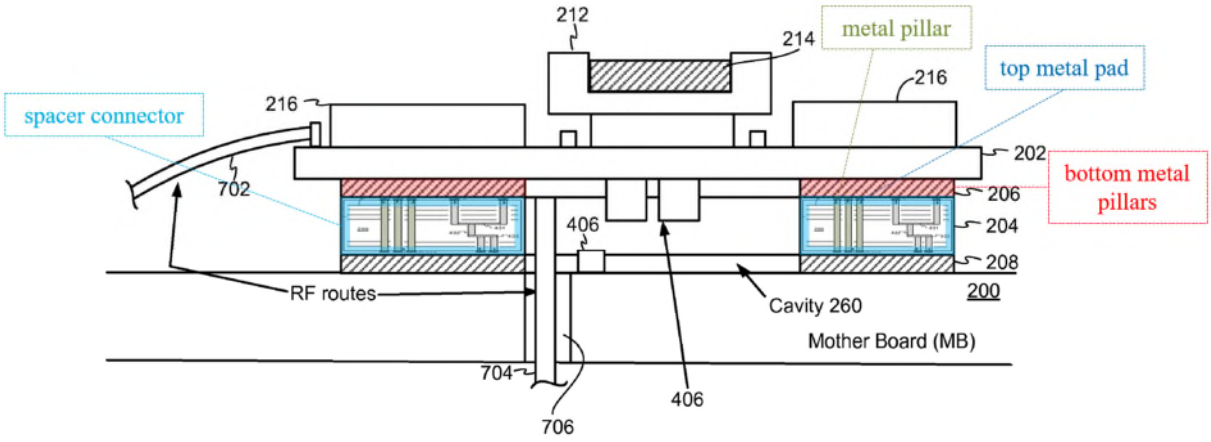
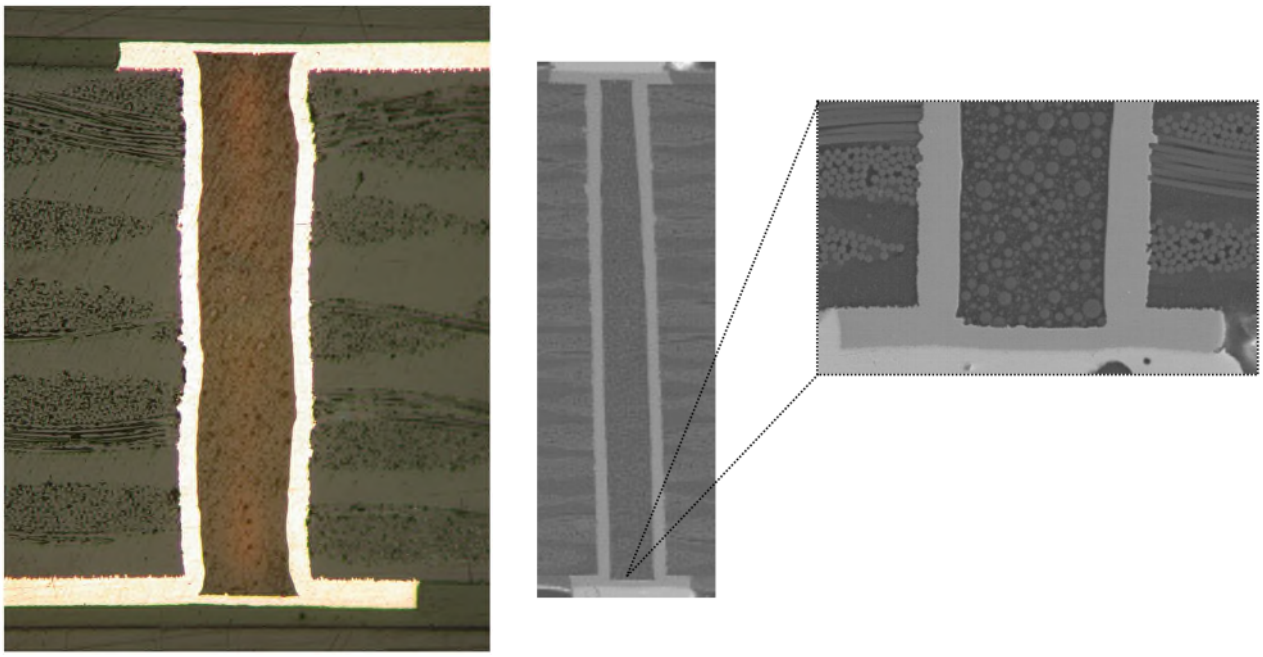


FIG. 7

EX1010, FIG. 7 (FIG. 8 superimposed thereon).

1[g]

According to PO's apparent interpretation, the bottom end of each via 402, 428 (metal pillar) among the plurality of vias 402, 428 protrudes downwardly from a bottom surface of material 220 (core substrate). EX1003, ¶¶323-24. As discussed above, a POSITA would have been motivated to apply *IPC-4761*'s via design to *Waite*'s vias 402, 428. §VII.G.i. This design is similar to the accused product; both show that the sidewalls of the vias wrap under the core substrate, and are covered with an additional layer of conductive material (bottom metal pad). EX1003, ¶323; EX1011, 16; EX1004, ¶¶44, 46. Thus, *Waite*'s metal pillars, when constructed according to the design disclosed by *IPC-4761*, satisfies 1[g], according to PO's apparent interpretation. EX1004, ¶44; EX1003, ¶323.



Compare EX1011, 16 (left) *with* EX1004, ¶¶44, 46 (right).

1[h]

The daughter board 202 (top package substrate) has, on a bottom surface thereof, a plurality of conductive elements 302 (bottom metal pillars) each coupled to a corresponding via 402, 428 (metal pillar) among the plurality of vias 402, 428 of the spacer connector 204.[16] EX1010, FIG. 3; EX1003, ¶¶325-26. *Waite* discloses that conductive elements 302 are disposed within conductive elastomer 206, which interfaces with daughter board 202 and vias 402, 428 disposed within the spacer connector 204. EX1010, 4:12-16. *Waite* further discloses conductive elements 302 can be conductive cubes, segments, spring pins, or formed pin type connectors. EX1010, 4:17-19, 4:61. These configurations correspond to "metal pillars," as required by 1[h]. EX1003, ¶325, §V.A.

[16] For avoidance of doubt, "each" "bottom metal pillar" as mapped herein, corresponds to the bottom metal pillars that are coupled to metal pillars in *Waite*'s Figure 3. EX1010, FIG. 3; *see also* EX1003, ¶325.

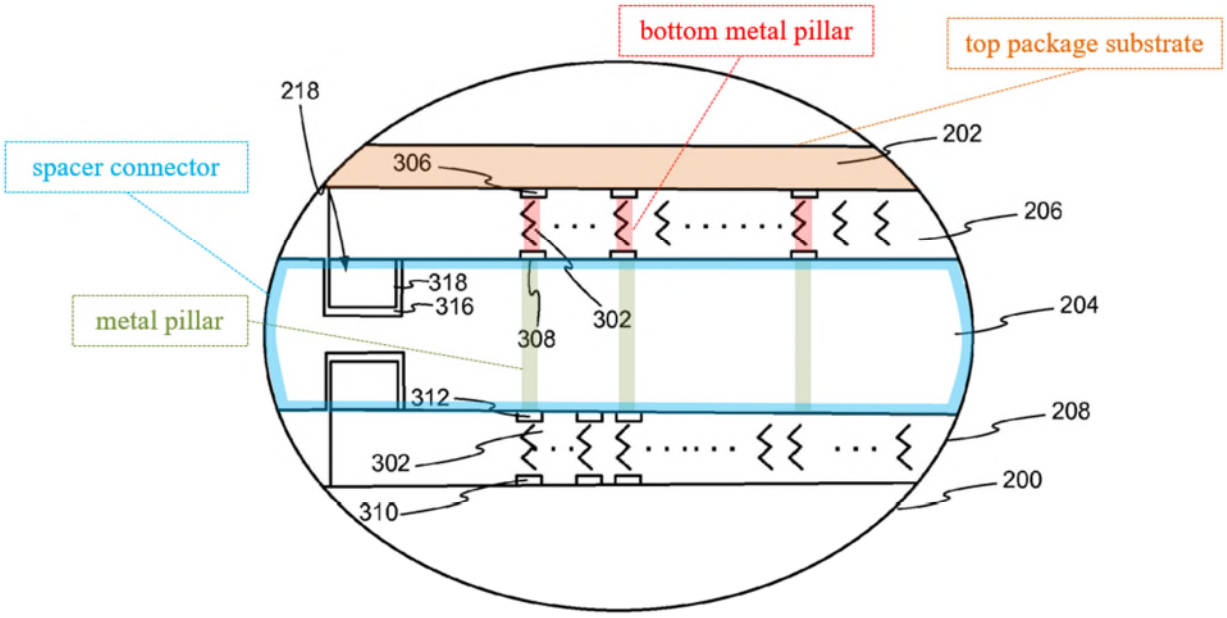


FIG. 3

EX1010, FIG. 3.

1[i]

The motherboard 200 (bottom package substrate) has, on a top surface thereof, a plurality of conductive elements 302 (top metal pillars) each coupled to a corresponding via 402, 428 (metal pillar) among the plurality of vias 402, 428 of the spacer connector 204. EX1010, FIG. 3; EX1003, ¶¶327-28. *Waite* discloses conductive elements 302 are disposed within conductive elastomer 208, which interfaces with motherboard 200 and vias 402, 428 (within spacer connector 204). EX1010, 4:12-16. Conductive elements 302 can be conductive cubes, segments,

spring pins, or formed pin type connectors, which are "metal pillars," as required by 1[i]. EX1010, 4:17-19, 4:56-63; EX1003, ¶327, §V.A.

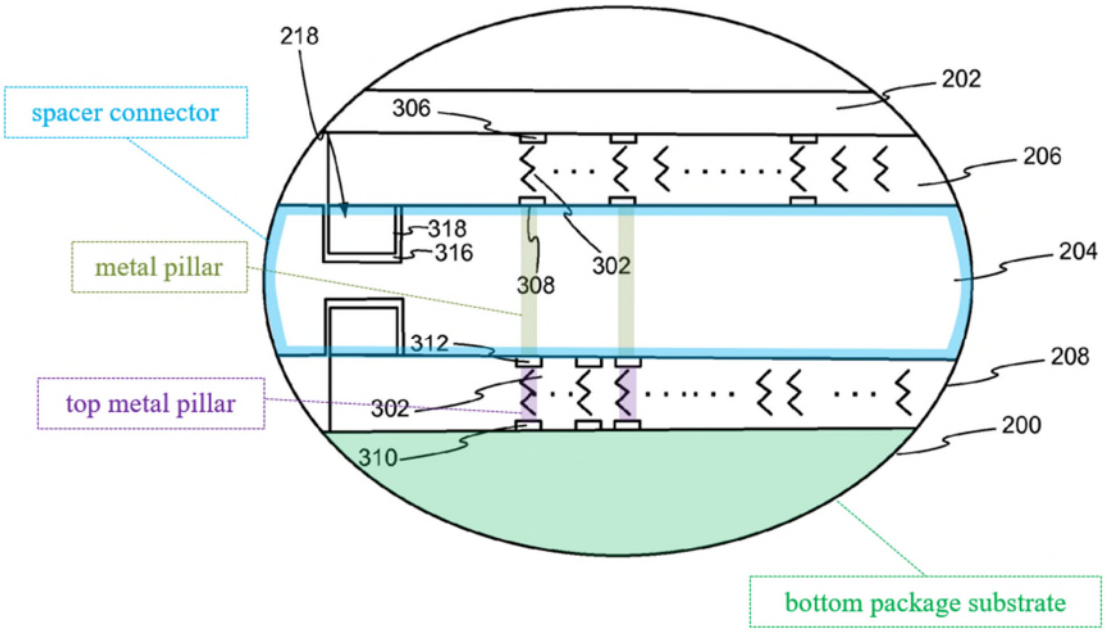


FIG. 3

EX1010, FIG. 3.

1[j]

Daughter board 202 (top package substrate) is electrically coupled to motherboard 200 (bottom package substrate) through the plurality of conductive elements 302 (bottom metal pillars) of daughter board 202, the plurality of vias 402, 428 (metal pillars) of spacer connector 204, and the plurality of conductive elements 302 (top metal pillars) of motherboard 200. EX1010, FIGs. 3, 7, 8; EX1003, ¶¶329-30. *Waite* teaches that contact pads 308 (top metal pads) of vias 402, 428 are coupled

to conductive elements 302, and contact pads 312 (bottom metal pads) of vias 402, 428 are coupled to conductive elements 302. EX1010, 4:19-26, 10:3-5.

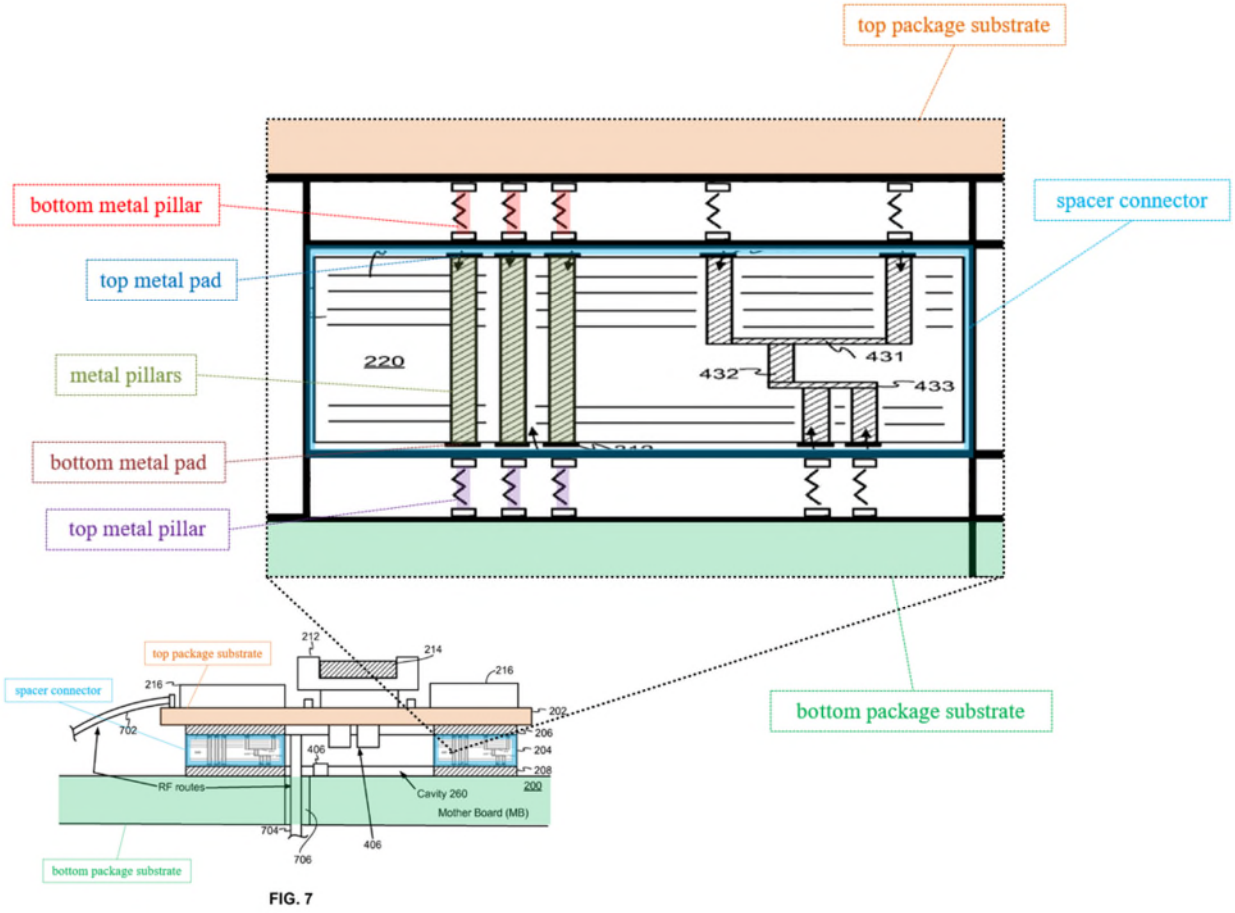


FIG. 7

EX1010, FIG. 7 (incorporating FIGs. 3 and 8).

1[k]

Waite discloses component 406 (bottom chip) arranged in the space between motherboard 200 (bottom package substrate) and daughter board 202 (top package substrate). EX1003, ¶¶331-32. *Waite* teaches component 406 (bottom chip) mounted on motherboard 200 between two spacer connectors 204. EX1010, 7:1-6, 7:31-34. Component 406 (bottom chip) can be a "RF tuning component" or "RF tuning

circuitry." EX1010, 7:1-6 ("The cavity 260 provides room for RF tuning components 406 and/or other components…on the top side of the motherboard 200…."), 9:29-30, 6:15; EX1003, ¶331. Both an RF tuning component and RF tuning circuitry correspond to a "chip," because these are often implemented as discrete integrated circuit components. EX1003, ¶331; EX1017, 26, 41. To the extent the RF tuning circuitry is not explicitly identified as a chip, it would have been obvious to implement it as such. EX1003, ¶331.

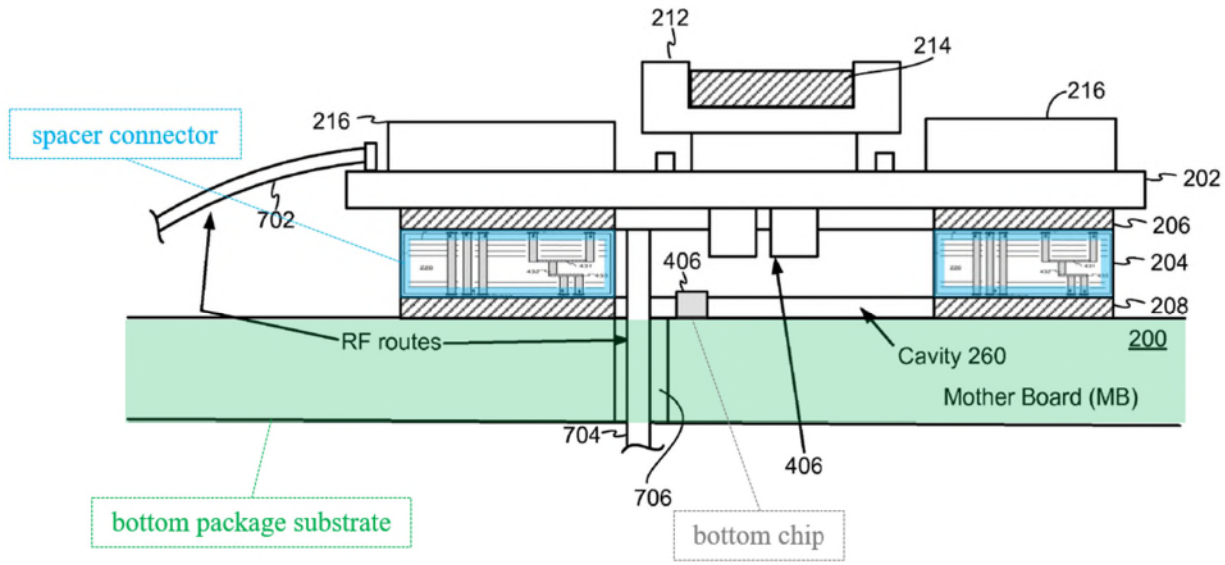


FIG. 7

EX1010, FIG. 7.

1[l]

Component 406 (bottom chip) is mounted to the top surface of motherboard 200 (bottom package substrate). EX1003, ¶¶333-34; EX1010, 7:1-6 (component 406 can be located "on the top side of the motherboard 200").

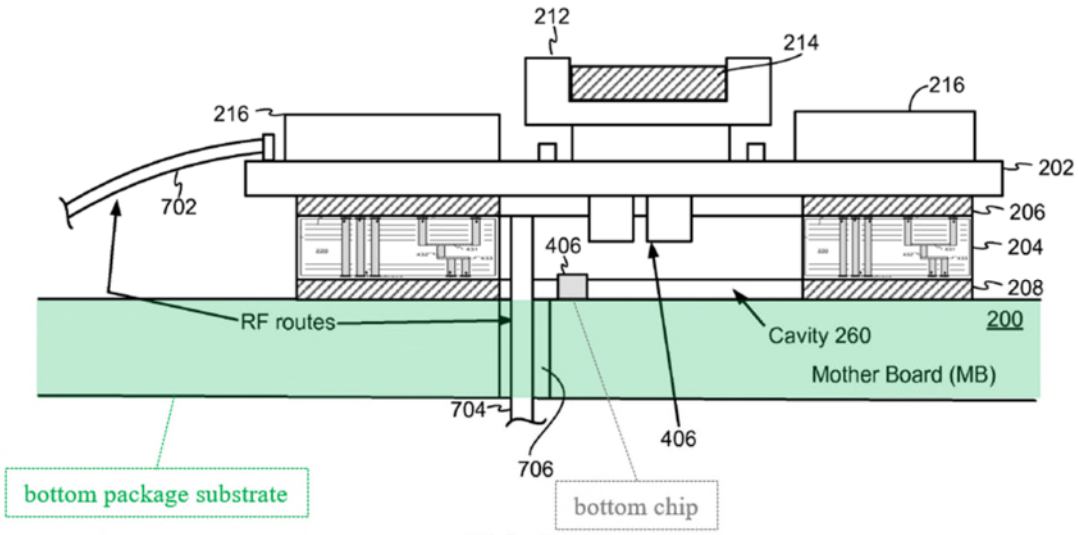


FIG. 7

EX1010, FIG. 7.

1[m]

Waite discloses two spacer connectors 204 arranged on opposite sides of component 406 (bottom chip). EX1003, ¶¶335-36. *Waite* discloses that component 406 (bottom chip) is disposed within a cavity 260 that is formed between two spacer connectors 204. EX1010, 6:66-7:6. The two spacer connectors 204 are arranged on opposite sides of component 406, as shown below.

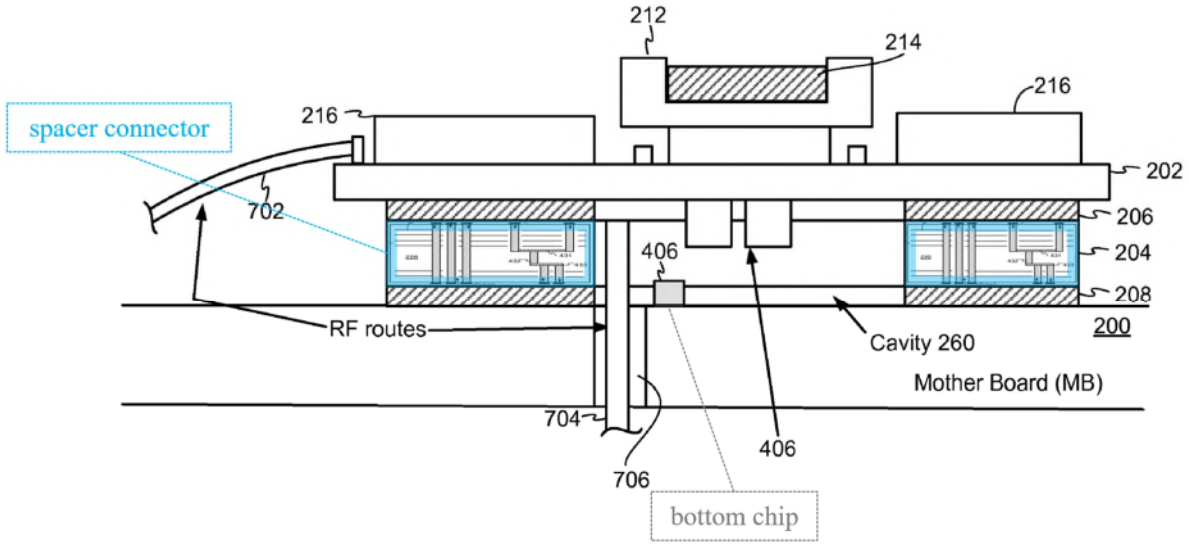


FIG. 7

EX1010, FIG. 7.

iii. Dependent Claims 2, 4, 6, and 9

Claim 2

The top surface of component 406 (bottom chip) is spaced downwardly from the bottom surface of daughter board 202 (top package substrate). EX1003, ¶¶337-38. *Waite* discloses that component 406 (bottom chip) is disposed within a cavity 260 formed below daughter board 202 (top package substrate). EX1010, 6:66-7:6, FIG. 7:

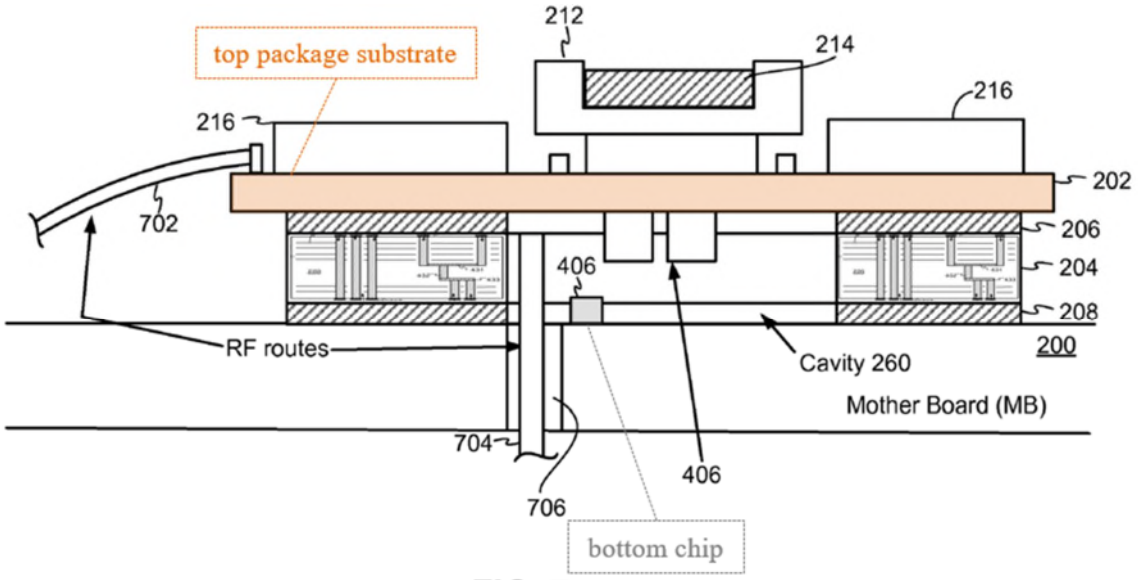
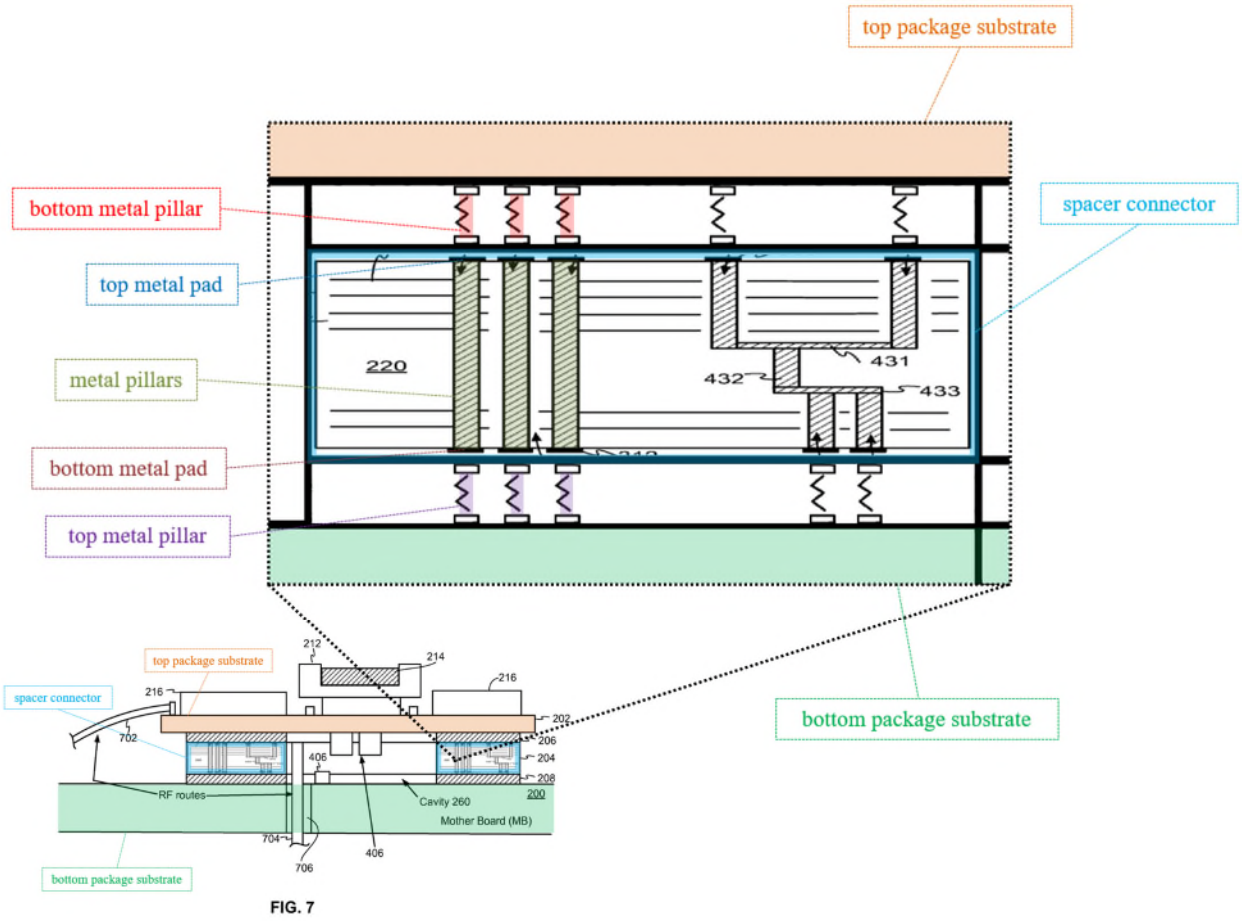


FIG. 7

Claim 4

Each conductive element 302 (bottom metal pillar) among the plurality of conductive elements 302 of daughter board 202 (top package substrate) is aligned with a corresponding via 402, 428 (metal pillar) among the plurality of vias 402, 428 of spacer connector 204, and with a corresponding conductive element 302 (top metal pillar) among the plurality of conductive elements 302 of motherboard 200 (bottom package substrate). EX1003, ¶339-40. *Waite* teaches that contact pads 308 (top metal pads) of vias 402, 428 are coupled to conductive elements 302, and contact pads 312 (bottom metal pads) of vias 402, 428 are coupled to conductive

elements 302. EX1010, 4:19-26, 10:3-5. As shown below, *Waite* illustrates that such a configuration can include aligned metal pillars.[17]



EX1010, FIG. 7 (FIGs. 3 and 8 superimposed thereon).

Claim 6[a]

The bottom ends of the plurality of vias 402, 428 (metal pillars) protruding downwardly from the bottom surface of material 220 (core substrate) of spacer connector 204 are connected, in an end-to-end manner, to corresponding top ends of

[17] For avoidance of doubt, "each bottom metal pillar among the plurality of bottom metal pillars," as mapped herein, corresponds to the three leftmost pillars illustrated in *Waite*'s Figure 8. EX1010, FIG. 8.

the plurality of conductive elements 302 (top metal pillars) of motherboard 200 (bottom package substrate). EX1003, ¶¶341-42. As discussed in §VII.G.ii.(1[g]), the bottom end of each via 402, 428 protrudes downwardly from a bottom surface of material 220. *Waite* further teaches that contact pads 312 (bottom metal pads), disposed on the bottom ends of vias 402, 428, are connected to the conductive elements 302. EX1010, 4:23-26. This connection is made in an end-to-end manner, as the bottom ***ends*** of vias 402, 428 are in communication with the top ***ends*** of conductive elements 302. EX1010, FIGs. 3, 7, 8; *see also supra* n.7.

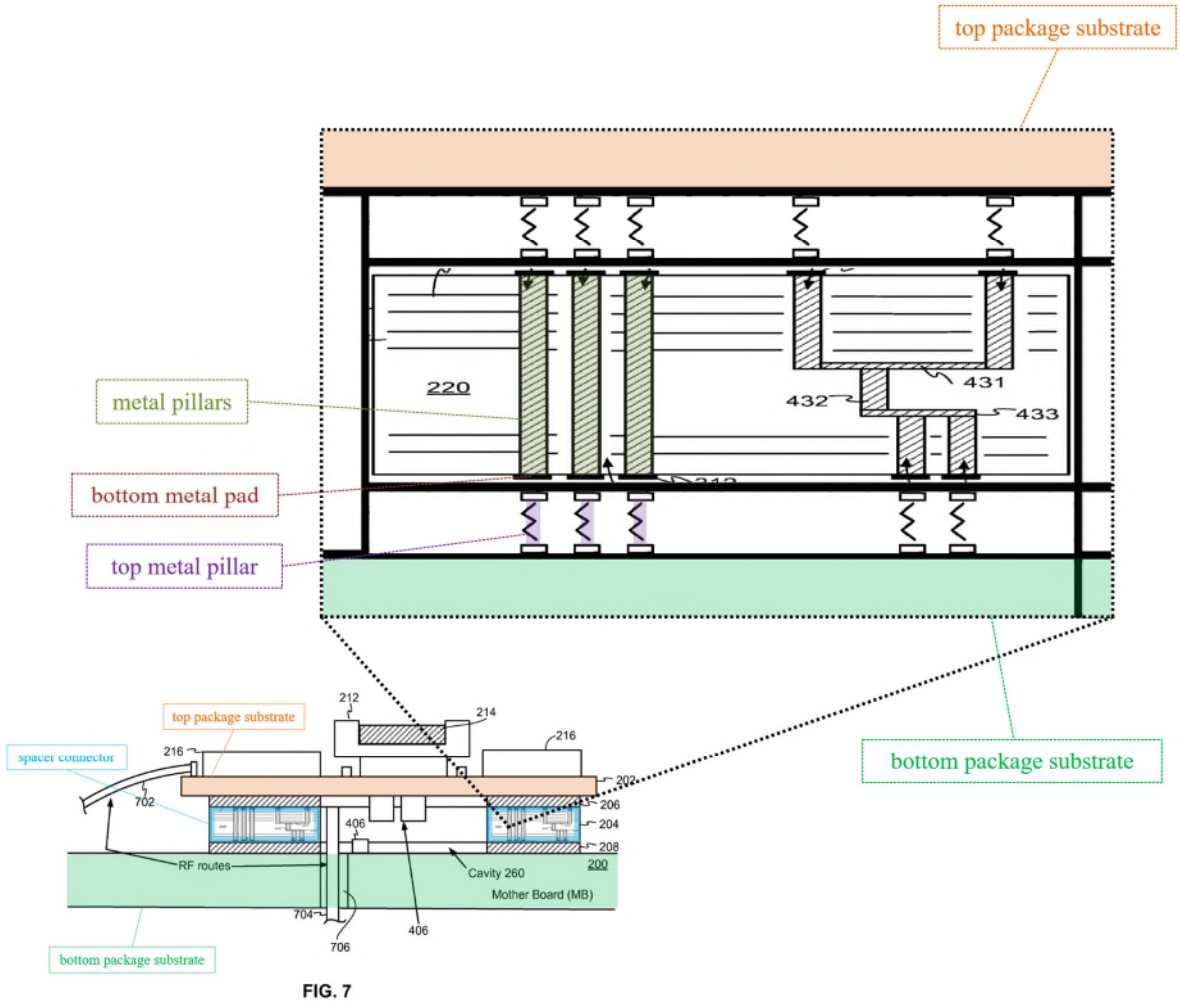


FIG. 7

EX1010, FIG. 7 (FIGs. 3 and 8 superimposed thereon).

Claim 6[b]

The bottom ends of the plurality of conductive elements 302 (bottom metal pillars) of the daughter board 202 (top package substrate) are connected to the corresponding top ends of the plurality of vias 402, 428 (metal pillars) of the spacer connector 204 via corresponding contact pads 308 (top metal pads) of the spacer connector 204. EX1003, ¶¶343-44; EX1010, 4:19-23 (daughter board 202 is

"coupled to upper contact pads 308 of the first spacer-connector 204, through…conductive elements 302"), FIG. 7.

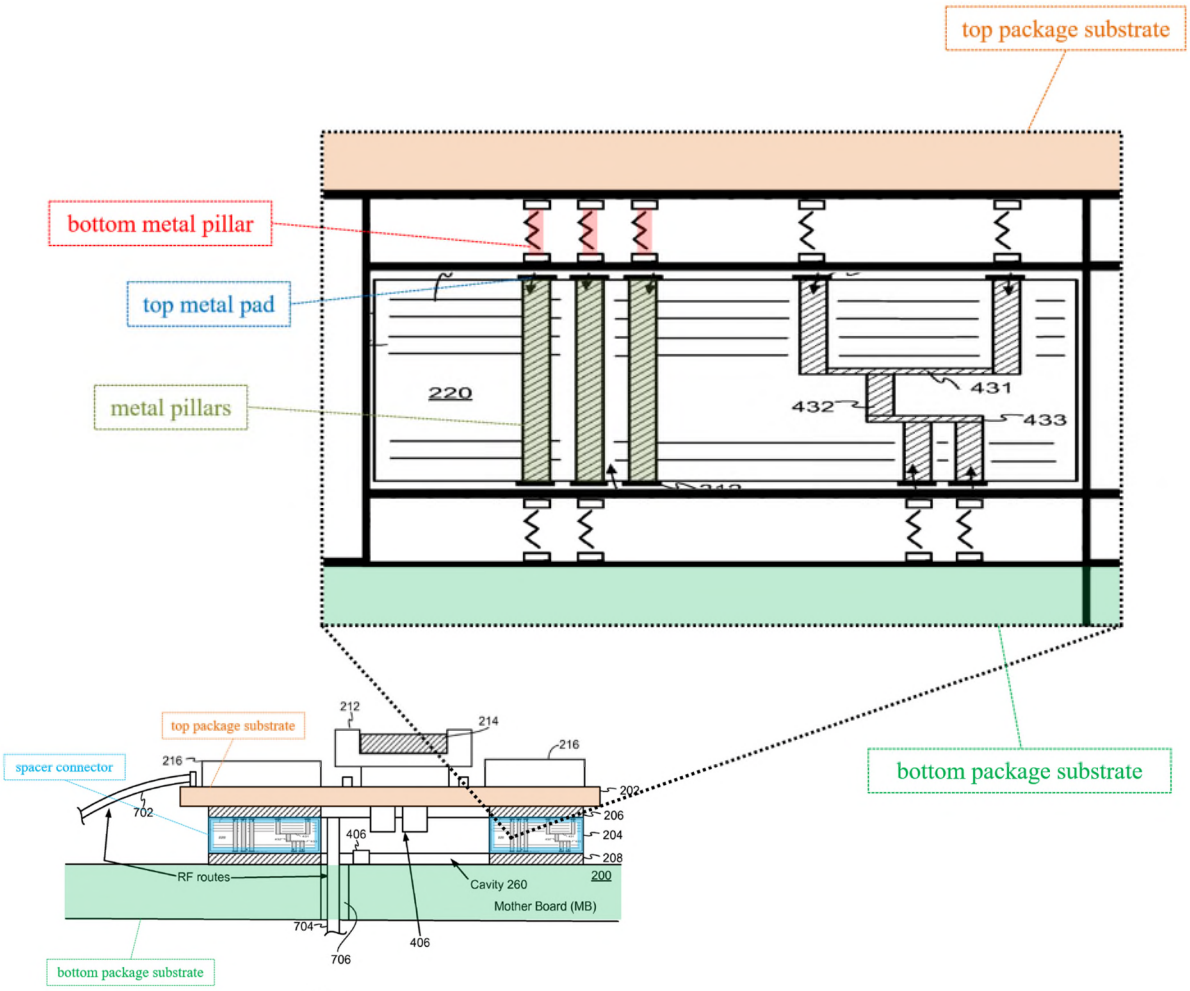


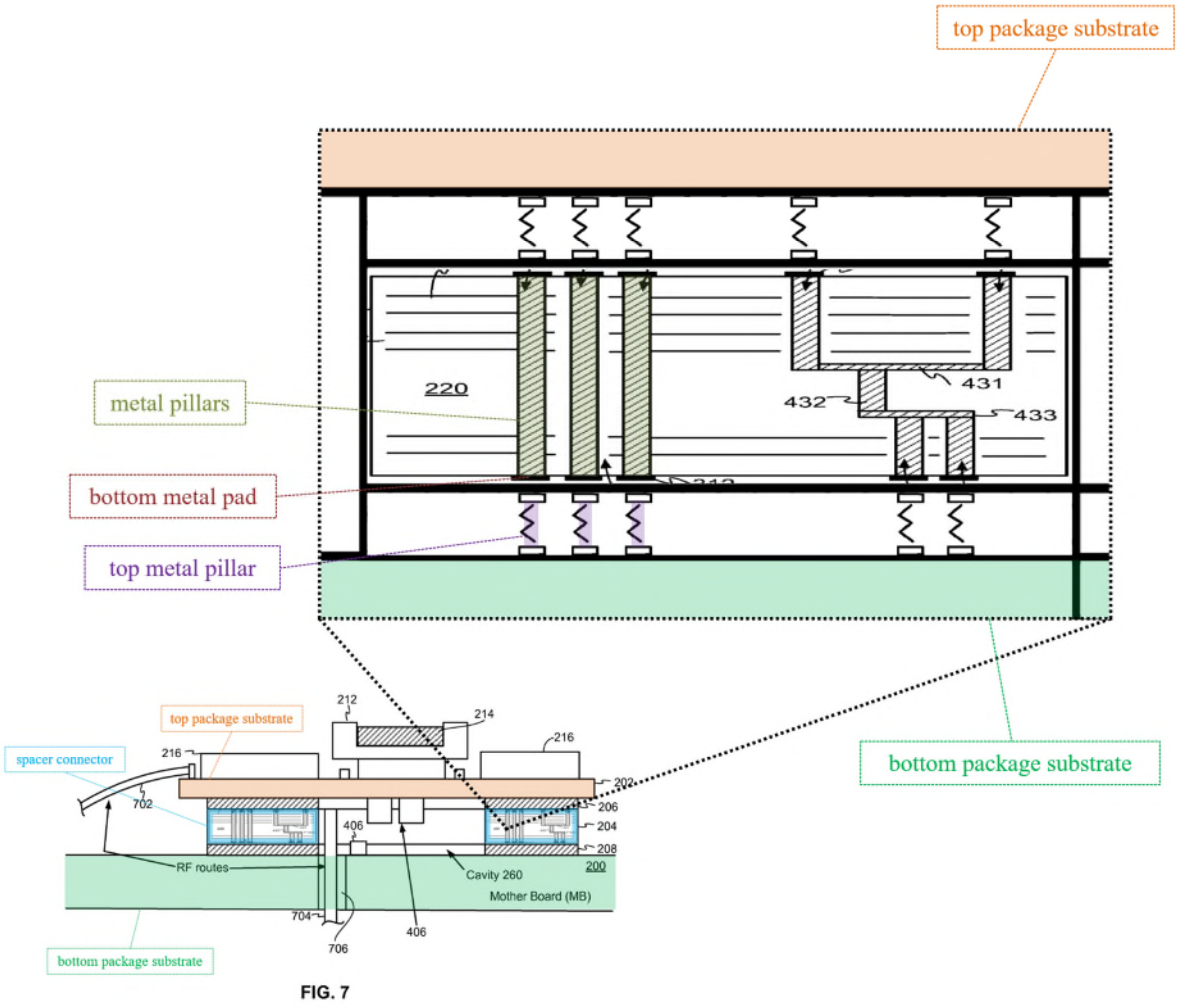
FIG. 7

EX1010, FIG. 7 (FIGs. 3 and 8 superimposed thereon).

Claim 9[a]

The spacer connector 204 includes a plurality of bottom metal pads, each on the bottom end of a corresponding via 402, 428 (metal pillar) among the plurality of vias 402, 428. EX1003, ¶¶345-46. For the same reasons discussed above regarding

the top metal pads, *Waite* similarly discloses bottom metal pads on the bottom ends of the vias. EX1003, ¶45; §VII.G.i.(1[f]).



EX1010, FIG. 7 (FIGs. 3 and 8 superimposed thereon).

Claim 9[b]

The bottom ends of vias 402, 428 (metal pillars) are connected to corresponding top ends of conductive elements 302 (top metal pillars) of the motherboard 200 (bottom package substrate) via contact pads 312 (bottom metal pads). EX1003, ¶¶347-48; EX1010, 4:23-26 (motherboard 200 is "coupled to lower

contact pads 312 of the first [spacer-]connector 204, through…conductive elements 302"), FIG. 7.

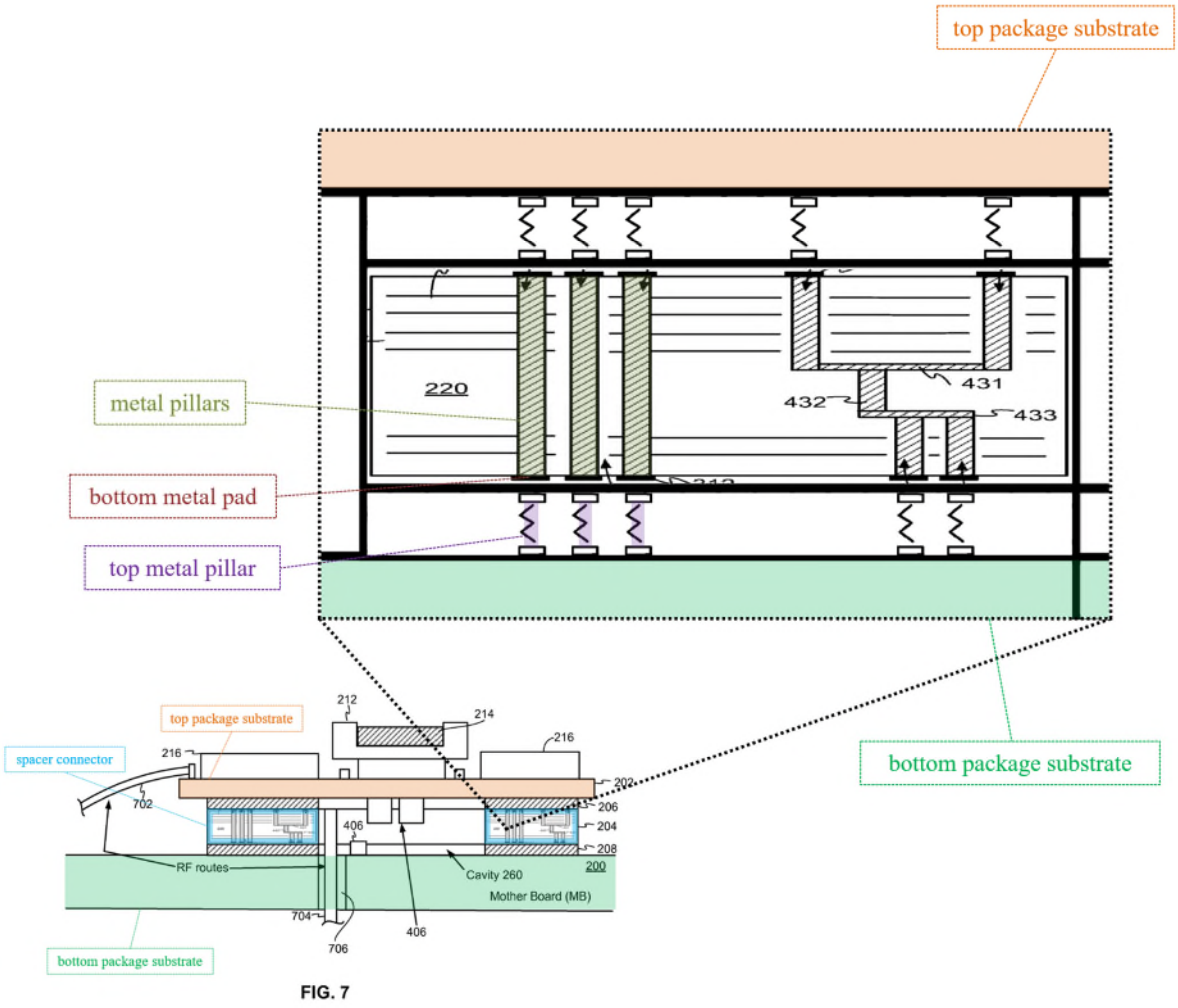


FIG. 7

EX1010, FIG. 7 (FIGs. 3 and 8 superimposed thereon).

Claim 9[c]

Limitation 9[c] is identical to limitation 6[b] and is thus obvious for the same reason. EX1003, ¶¶349-50; *see* §VII.G.iii.(6[b]).

VIII. SECONDARY CONSIDERATIONS

Petitioners are aware of no evidence of secondary considerations that would rebut a finding of obviousness and reserve the right to rebut any purported evidence raised by PO.

IX. CONCLUSION

Petitioners respectfully request that IPR be instituted and the Challenged Claims be cancelled.

Respectfully submitted,

Dated: March 31, 2026

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CERTIFICATION UNDER 37 C.F.R. §42.24(d)

Pursuant to 37 C.F.R. §42.24(d), the undersigned hereby certifies that the word count under §42.24(a)(1) for the foregoing Petition for *Inter Partes* Review totals 13,915 words, within the 14,000 word limit allowed under §42.24(a)(1)(i).

Dated: March 31, 2026

/ Eliot D. Williams /
Eliot D. Williams

CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§42.6(e) and 42.105, the undersigned certifies that, on this date, the foregoing was served via FedEx Overnight Delivery on the Patent Owner at the correspondence addresses of record (as listed in Patent Center and on the Patent Assignment Cover Sheet) for the subject patent at:

Patent Center	Patent Assignment Cover Sheet
JCIPRNET 8F-1, No. 100, Roosevelt Rd. Sec. 2, Taipei, TAIWAN	Robert D Katz 8350 N. Central Expressway Suite 1900 Dallas, TEXAS 75206

A complete copy was also served via electronic mail to counsel of record for Patent Owner in the litigation pending before the U.S. District Court for the Eastern District of Texas entitled *Topwire LLC v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc.*, Civil Action No. 2:25-cv-01183-JRG-RSP at:

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Dated: March 31, 2026

/ Eliot D. Williams /
Eliot D. Williams