UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.
Petitioner

v.

TOPWIRE LLC
Patent Owner

Case No. IPR2026-00303
U.S. Patent No. 9,859,202

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,859,202

CHALLENGING CLAIMS 1–9
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

TABLE OF CONTENTS

Page

I. MANDATORY NOTICES 1

A. Real Party-In-Interest (37 C.F.R. § 42.8(b)(1)) 1

B. Related Matters (37 C.F.R. § 42.8(b)(2)) 1

C. Lead And Back-up Counsel (37 C.F.R. § 42.8(b)(3)) 1

D. Service Information (37 C.F.R. § 42.8(b)(4)) 2

II. FEES 2

III. CERTIFICATION OF GROUNDS FOR STANDING 2

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED 3

A. Identification of Prior Art 3

B. Statutory Grounds of Unpatentability 3

V. OVERVIEW OF THE ’202 PATENT 4

A. Summary Of Claimed Embodiments 4

B. Prosecution History 7

VI. LEVEL OF ORDINARY SKILL IN THE ART 7

VII. CLAIM CONSTRUCTION 8

VIII. GROUNDS 9

A. Ground I: Claims 1–4 and 7–9 Are Rendered Obvious By Chen In View Of Sun 9

1. Independent Claim 1 9

2. Dependent Claim 2 32

3. Dependent Claim 3 33

4. Dependent Claim 4 38

5. Dependent Claim 7 39

6. Dependent Claim 8 41

7. Dependent Claim 9 43

B. Ground II: Claims 5–6 Are Rendered Obvious By Chen In View Of Sun And Furuta 47

1. Dependent Claim 5 47

2. Dependent Claim 6 54

C. Ground III: Claims 1–4 and 7–9 Are Rendered Obvious By Chen In View Of Wu 55

1. Independent Claim 1 55

2. Dependent Claim 2 70

3. Dependent Claim 3 70

4. Dependent Claim 4 77

5. Dependent Claim 7 78

6. Dependent Claim 8 79

7. Dependent Claim 9 79

D. Ground IV: Claims 5–6 Are Rendered Obvious By Chen In View Of Wu And Furuta 81

1. Dependent Claim 5 81

2. Dependent Claim 6 82

IX. CONCLUSION 83

TABLE OF AUTHORITIES

Page(s)

Cases

Nidec Motor Corp. v. Zhongshan Broad Ocean Motor, Co.,
868 F.3d 1013 (Fed. Cir. 2017) 8

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005) 8

Regents of the Univ. of Cal. v. Satco Prods., Inc.,
No. 2023-1356, 2024 WL 7311186 (Fed. Cir. Dec. 4, 2024) 36, 74

Statutes

35 U.S.C. § 102 3

35 U.S.C. § 103 3

35 U.S.C. § 314(a) 4

Rules

37 C.F.R. § 42.100(b) 8

37 C.F.R. § 42.104(b)(1)–(2) 3

37 C.F.R. § 42.22(a)(1) 3

PETITIONER'S TABLE OF EXHIBITS

Exhibit No.	DESCRIPTION
1001	U.S. Patent No. 9,859,202 ("'202 Patent")
1002	Declaration of Dr. Stanley Shanfield
1003	U.S. Patent Application Publication No. 2013/0182402 ("Chen")
1004	U.S. Patent Application Publication No. 2011/0147908 ("Sun")
1005	U.S. Patent Application Publication No. 2016/0056087 ("Wu")
1006	U.S. Patent Application Publication No. 2009/0140415 ("Furuta")
1007	Prosecution History of U.S. Patent No. 9,859,202 ("'202 Patent FH")
1008	U.S. Patent Application Publication No. 2014/0248742
1009	U.S. Patent Application Publication No. 2011/0159284
1010	U.S. Patent Application Publication No. 2008/0155820 ("Arai")
1011	U.S. Patent Application Publication No. 2015/0001708

Throughout the Petition, all annotations, coloring, and emphases have been added unless indicated otherwise.

LISTING OF CLAIMS

[1Pre] A structure, comprising

[1A] a **bottom package substrate**;

[1B] a **top package substrate** stacked on top of the **bottom package substrate**;

[1C] at least one **spacer connector** interposed between the **bottom package substrate** and the **top package substrate** to define a space between the **bottom package substrate** and the **top package substrate**,

[1D] wherein the **spacer connector** comprises a **core substrate**;

[1E] a **plurality of metal pillars**, each passing through the **core substrate**;

[1F] a **plurality of top metal pads**, each on a top end of a corresponding **metal pillar** among the **plurality of metal pillars**;

[1G] wherein a bottom end of each **metal pillar** among the **plurality of metal pillars** protrudes downwardly from a bottom surface of the **core substrate**;

[1H] the **top package substrate** has, on a bottom surface thereof, a **plurality of bottom metal pillars** each coupled to a corresponding **metal pillar** among the **plurality of metal pillars** of the **spacer connector**,

[1I] the **bottom package substrate** has, on a top surface thereof, a **plurality of top metal pillars** each coupled to a corresponding **metal pillar** among the **plurality of metal pillars** of the **spacer connector**,

[1J] the **top package substrate** is electrically coupled to the **bottom package substrate** through the **plurality of bottom metal pillars** of the **top package substrate**, the **plurality of metal pillars** of the **spacer connector**, and the **plurality of top metal pillars** of the **bottom package substrate**; and

[1K] a **bottom chip** arranged in the space between the **bottom package substrate** and the **top package substrate**,

[1L] wherein the **bottom chip** is mounted to the top surface of the **bottom package substrate**,

[1M] the at least one **spacer connector** comprises two spacer connectors arranged on opposite sides of the **bottom chip**.

[2Pre] The structure of claim 1, wherein

[2A] a top surface of the **bottom chip** is spaced downwardly from the bottom surface of the **top package substrate**.

[3Pre] The structure of claim 2, further comprising:

[3A] a **top chip** mounted to the top surface of the **top package substrate**,

[3B] wherein in a direction in which the **top package substrate** is stacked on top of the **bottom package substrate**, the **top chip** overlaps the **bottom chip** and each of the two **spacer connectors**.

[4Pre] The structure of claim 1, wherein

[4A] each **bottom metal pillar** among the **plurality of bottom metal pillars** of the **top package substrate** is aligned with a corresponding **metal pillar** among the **plurality of metal pillars** of the **spacer connector**, and with a corresponding **top metal pillar** among the **plurality of top metal pillars** of the **bottom package substrate**.

[5Pre] The structure of claim 4, wherein

[5A] the **spacer connector** is free of **metal pads** on the bottom ends of the **plurality of metal pillars** protruding downwardly from the bottom surface of the **core substrate**, and each **metal pillar** among the **plurality of metal pillars** and the corresponding **top metal pad** of the **spacer connector** form a T shape.

[6Pre] The structure of claim 4, wherein

[6A] the bottom ends of the **plurality of metal pillars** protruding downwardly from the bottom surface of the **core substrate** of the **spacer connector** are connected, in an end-to-end manner, to corresponding top ends of the **plurality of top metal pillars** of the **bottom package substrate**, and bottom ends of the **plurality of bottom metal pillars** of the **top package substrate** are connected to the corresponding top ends of the **plurality of metal pillars** of the **spacer connector** via the corresponding **top metal pads** of the **spacer connector**.

[7Pre] The structure of claim 4, wherein

[7A] the **spacer connector** further comprises a **dielectric layer** on the bottom surface of the **core substrate**, and

[7B] the **plurality of metal pillars** pass through the **core substrate** and the **dielectric layer**.

[8Pre] The structure of claim 7, wherein

[8A] the **dielectric layer** is a dielectric adhesive in which the **core substrate** is pasted.

[9Pre] The structure of claim 4, wherein

[9A] the **spacer connector** further comprises a **plurality of bottom metal pads**, each on the bottom end of a corresponding **metal pillar** among the **plurality of metal pillars**,

[9B] the bottom ends of the **plurality of metal pillars** are connected to corresponding top ends of the **plurality of top metal pillars** of the **bottom package substrate** via the corresponding **bottom metal pads** of the **spacer connector**, and

[9C] bottom ends of the **plurality of bottom metal pillars** of the top package substrate are connected to the corresponding top ends of the **plurality of metal pillars** of the **spacer connector** via the corresponding **top metal pads** of the **spacer connector**.

Petitioner respectfully requests *inter partes* review and cancellation of claims 1–9 in U.S. Patent No. 9,859,202 ("'202 Patent").

I. MANDATORY NOTICES

A. Real Party-In-Interest (37 C.F.R. § 42.8(b)(1))

Apple Inc., the Petitioner, identifies itself as a real party-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

On December 1, 2025, Patent Owner TopWire, LLC filed a patent infringement suit against Petitioner, asserting U.S. Patent No. 9,859,202. *TopWire, LLC v. Apple Inc.*, No. 7:25-cv-00551 (W.D. Tex.).

C. Lead And Back-up Counsel (37 C.F.R. § 42.8(b)(3))

Petitioner is filing a Power of Attorney appointing the practitioners associated with Customer Number 132,593. Petitioner designates the following lead and back-up counsel:

Lead Counsel	First Back-up Counsel
Yung-Hoon Ha (Reg. No. 56,368) Desmarais LLP 230 Park Ave New York, NY 10169 Telephone: (212) 351-3400 Email: yha@desmaraisllp.com	Cosmin Maier (Reg. No. 75,387) Desmarais LLP 230 Park Ave New York, NY 10169 Telephone: (212) 351-3400 Email: cmaier@desmaraisllp.com

D. Service Information (37 C.F.R. § 42.8(b)(4))

Post and hand delivery: Desmarais LLP

230 Park Ave, New York, NY 10169

Telephone: 212-351-3400

Email: AppleTopWireService@desmaraisllp.com

Please address all correspondence to counsel identified above. Petitioner consents to electronic service by email at:

AppleTopWireService@desmaraisllp.com

II. FEES

Petitioner is concurrently electronically submitting the required fees for this Petition. The Board is authorized to charge Desmarais LLP's deposit account, No. 50-6822, for any fee deficiency.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies that the '202 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review.

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Under 37 C.F.R. §§ 42.22(a)(1) and 42.104(b)(1)–(2), Petitioner requests *inter partes* review and cancellation of claims 1–9 of the ’202 Patent.

A. Identification of Prior Art

The ’202 Patent claims priority to U.S. provisional application No. 62/184,034, filed on June 24, 2015. EX1001, Cover. Accordingly, this Petition applies AIA provisions of 35 U.S.C. §§ 102 and 103. The below references are pertinent to the grounds of unpatentability.

Prior Art Reference	Prior Art Date	Prior Art Under 35 U.S.C. §
U.S. Patent Application Publication 2013/0182402 (“Chen”) (EX1003)	Published: July 18, 2013	102(a)(1)
U.S. Patent Application Publication 2011/0147908 (“Sun”) (EX1004)	Published: June 23, 2011	102(a)(1)
U.S. Patent Application Publication 2016/0056087 (“Wu”) (EX1005)	Filed: August 22, 2014 Published: February 25, 2016	102(a)(2)
U.S. Patent Application Publication 2009/0140415 (“Furuta”) (EX1006)	Published: June 4, 2009	102(a)(1)

B. Statutory Grounds of Unpatentability

Petitioner requests cancellation of Claims 1–9 under 35 U.S.C. §103 based on the following Grounds.

Ground	Statutory Ground 35 U.S.C.	Claims	Prior Art References
I	103	1–4, 7–9	Chen in view of Sun
II	103	5–6	Chen in view of Sun and Furuta
III	103	1–4, 7–9	Chen in view of Wu
IV	103	5–6	Chen in view of Wu and Furuta

This Petition demonstrates that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. 35 U.S.C. § 314(a).

V. OVERVIEW OF THE '202 PATENT

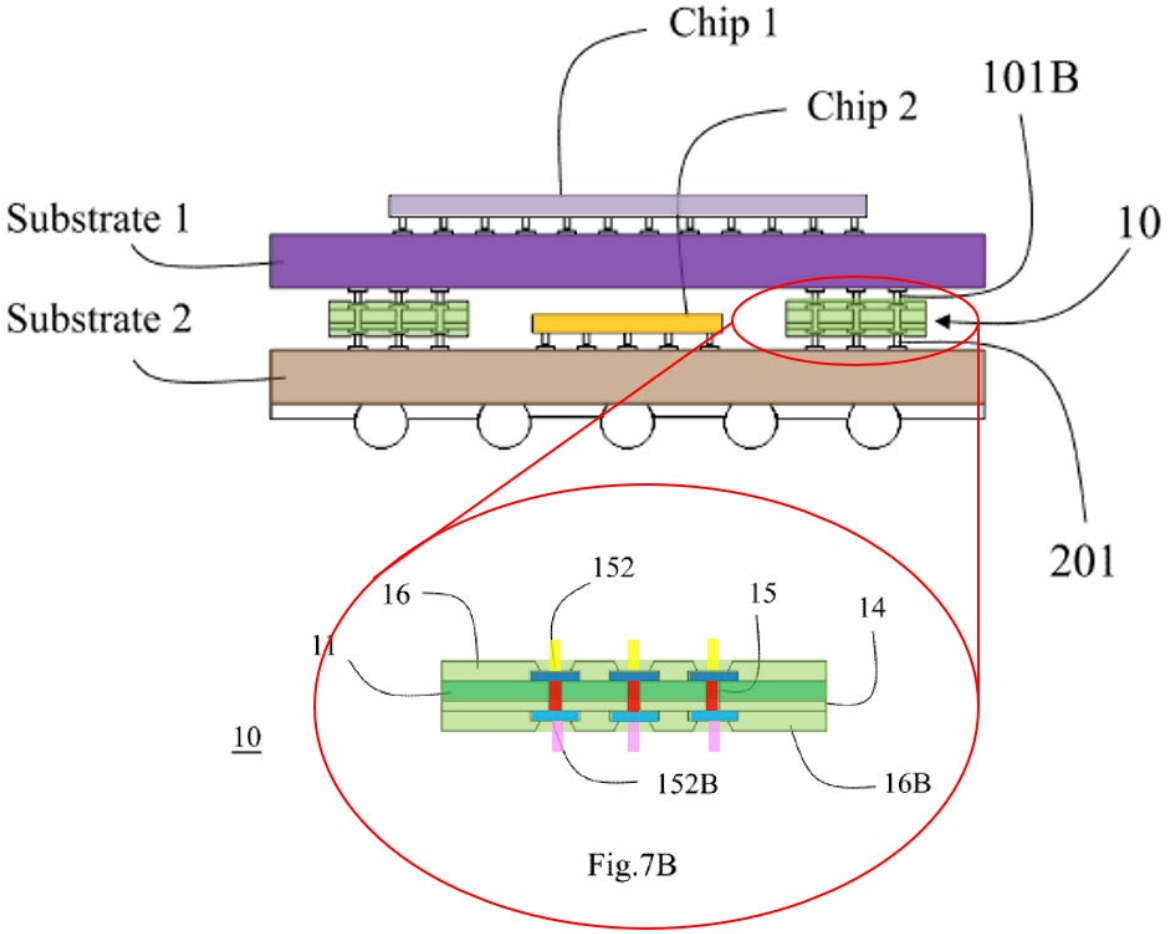
A. Summary Of Claimed Embodiments

The '202 Patent—titled "Spacer Connector"—provides three embodiments for making a spacer connector—only two of which are claimed because the third embodiment does not meet the claimed "wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate." EX1001, claim 1. EX1002, ¶¶ 37–41.

The first claimed embodiment is illustrated with Figures 7B and 8, which show two substrates—**substrate 1** and **substrate 2**—each having a chip 1 and chip 2 thereon, respectively. As shown in Figures 7B and 8 below, two distinct **spacer connectors 10** separate **substrate 1** and **substrate 2**. Each **spacer connector 10** includes **metal pillars 15** that penetrate through the **core substrate 14**, passivation 16, and dielectric adhesive 14 of the **spacer connector 10** that terminates with **top**

metal pad 152 and **bottom metal pad 152B**. The **top metal pads 152** are electrically coupled to **metal pillars 101B** at the bottom of **substrate 1** and **bottom metal pads 152B** are electrically coupled to **metal pillars 201** at the top of the **substrate 2**. *See* EX1001, 2:1–27.

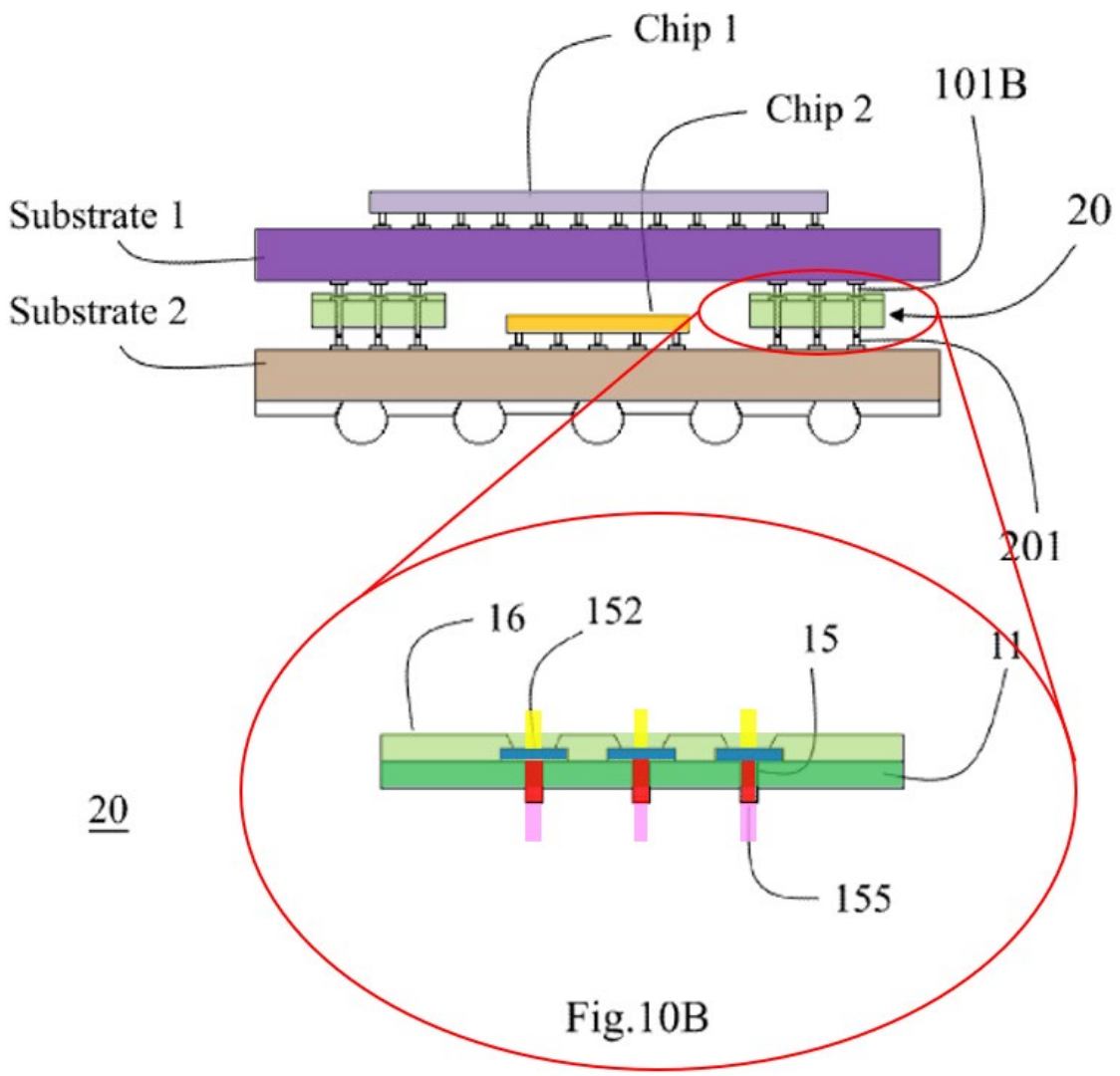
Fig.8



EX1001, Figures 7B and 8. EX1002, ¶39.

The second claimed embodiment is nearly identical to the first embodiment, except that the **bottom metal pads 152B** have been removed and the **metal pillars 15** connect directly to **metal pillars 201**. *See* EX1001, 2:66–3:23.

Fig.11



EX1001, Figures 10B and 11. EX1002, ¶40.

B. Prosecution History

The ’202 Patent was filed on June 23, 2016, claiming priority to U.S. provisional application No. 62/184,034, filed on June 24, 2015. EX1007, 4, 33. EX1002, ¶11.

On July 21, 2017, the Examiner rejected the then-pending claims over U.S. Patent Application Publication No. 2008/0155820 (“Arai”). *See* EX1007, 100–104. The Examiner, however, indicated that then-pending claim 12, which recites “further comprising: a bottom chip arranged in the space between the bottom package substrate and the top package substrate, and the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip” contained allowable subject matter. EX1007, 104. EX1002, ¶46.

On October 19, 2017, Applicant amended the independent claim to incorporate the subject matter recited in then-pending claim 12. EX1007, 117–125.

On November 7, 2017, a Notice of Allowance was mailed. EX1007, 129–137. The ’202 Patent issued on January 2, 2018. EX1007, 151. EX1002, ¶49.

VI. LEVEL OF ORDINARY SKILL IN THE ART

A Person of Ordinary Skill in the Art (“POSITA”), as of the claimed priority date of June 24, 2015, would have had: (1) a bachelor’s degree in materials science, mechanical engineering, electrical engineering, physics or an equivalent engineering discipline, and (2) approximately two years of experience working in the field of

integrated circuit processing, fabrication, and packaging. A higher level of education may make up for less experience and vice versa. EX1002, ¶51.

VII. CLAIM CONSTRUCTION

The claims should be construed "in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b); *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Moreover, the Board "need[s] only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor, Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

In view of the '202 Patent and the file history of the '202 Patent (EX1007) and its claimed priority application—U.S. Provisional Application No. 62/184,034—Petitioner submits that no terms require explicit construction and should be given their plain and ordinary meaning. EX1002, ¶¶54–55.

VIII. GROUNDS

A. Ground I: Claims 1–4 and 7–9 Are Rendered Obvious By Chen In View Of Sun

1. Independent Claim 1

a) [1Pre] A structure, comprising:

Chen discloses [1Pre]. Chen, like the ’202 Patent, is directed to a package-on-package structure.[1] *See, e.g.,* EX1003, [0004] (discussing Figures 1–9 are directed to “manufacturing of a Package-on-Package (PoP) structure”); EX1001, claim 1. Chen discloses a structure that includes a **top package component 62** electrically coupled to a **bottom package component 56** through two **Through-Assembly Via (TAV) Modules 28**. EX1003, [0019] (“FIG. 9 illustrates the bonding of **top package component 62** to bottom package 60. In some embodiments, …

[1] Chen is therefore analogous art for this reason alone because Chen is in the same field of endeavor as the ’202 Patent. Independently, Chen is analogous art because a POSITA would have also found Chen to be reasonably pertinent to the ’202 Patent because it deals with the same problem of electrically coupling a top package substrate to a bottom package substrate through the use of two intermediate substrates. *See* EX1001, claim 1 (“the top package substrate is electrically coupled to the bottom package substrate through… the spacer connector…”); EX1002, ¶62.

package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown)…. In the resulting package, **TAV modules 28** are used to electrically couple the circuit devices in **package component 62** to **package component 56**."), [0018], EX1003, [0012] ("FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, **TAV modules 28** are disposed on opposite sides of **package component 24**. Although two **TAV modules 28** are illustrated, there may be one or more than two **TAV modules 28**."), Abstract.

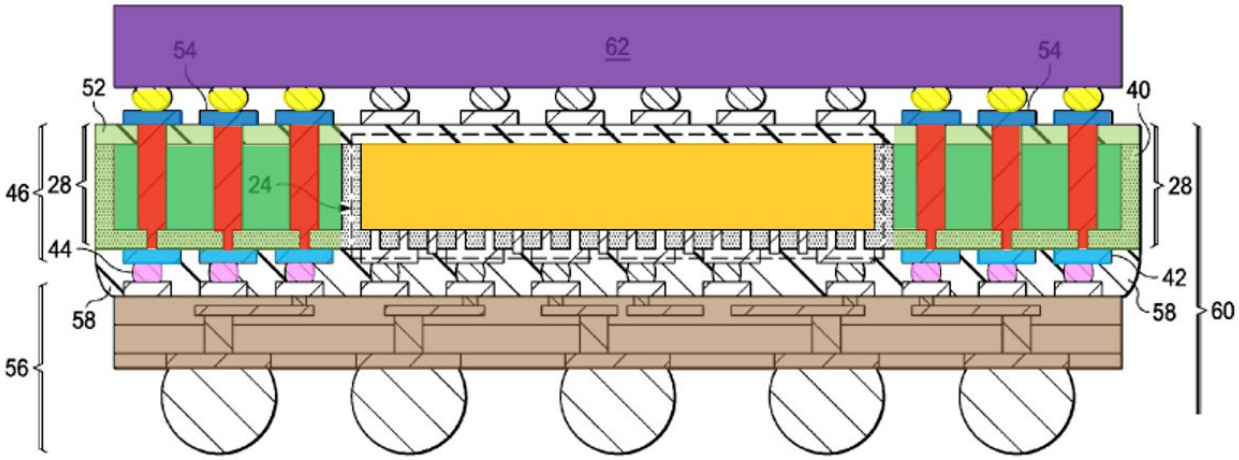


FIG. 9

EX1003, Figure 9.

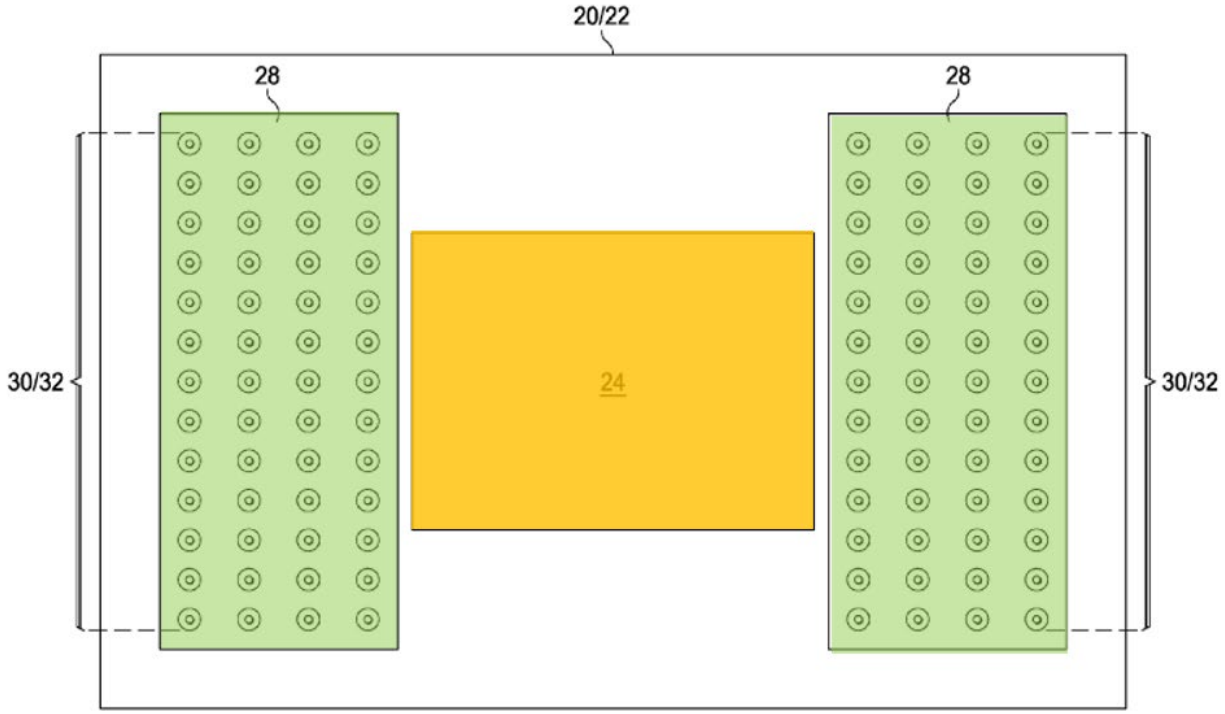
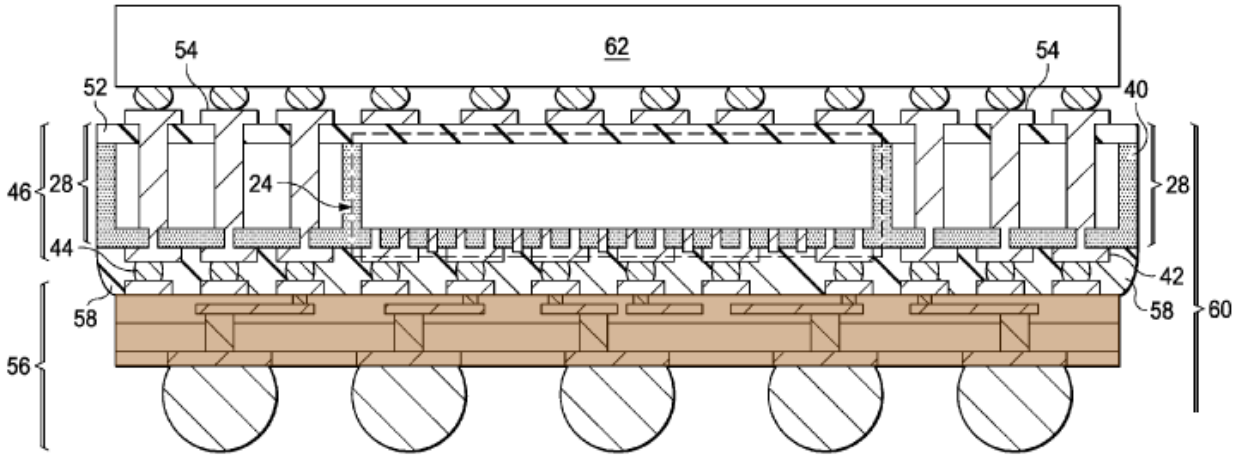


FIG. 2

EX1003, Figure 2. EX1002, ¶¶ 61–63.

b) [1A] a bottom package substrate;

Chen discloses [1A]. Chen discloses **package component 56** located on the bottom of Figure 9, which may be a "**package substrate**." EX1003, [0018] ("Referring to FIG. 8, package 46 is bonded to **package component 56** to form bottom package 60. **Package component 56** may be a **package substrate**, an interposer, a device die, a Printed Circuit Board (PCB), or the like.").



EX1003, Figure 9. EX1002, ¶¶ 64–65.

c) [1B] a top package substrate stacked on top of the bottom package substrate;

Chen discloses [1B]. Chen discloses a **top package component 62** (which includes a **package substrate**) stacked on top of the **package component 56**. EX1003, [0019] ("FIG. 9 illustrates the bonding of **top package component 62** to **bottom** package 60. In some embodiments, … **package component 62** is a package that includes **a device die (not shown) bonded to a package substrate (not shown)** … . In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in **package component 62** to **package component 56**.").

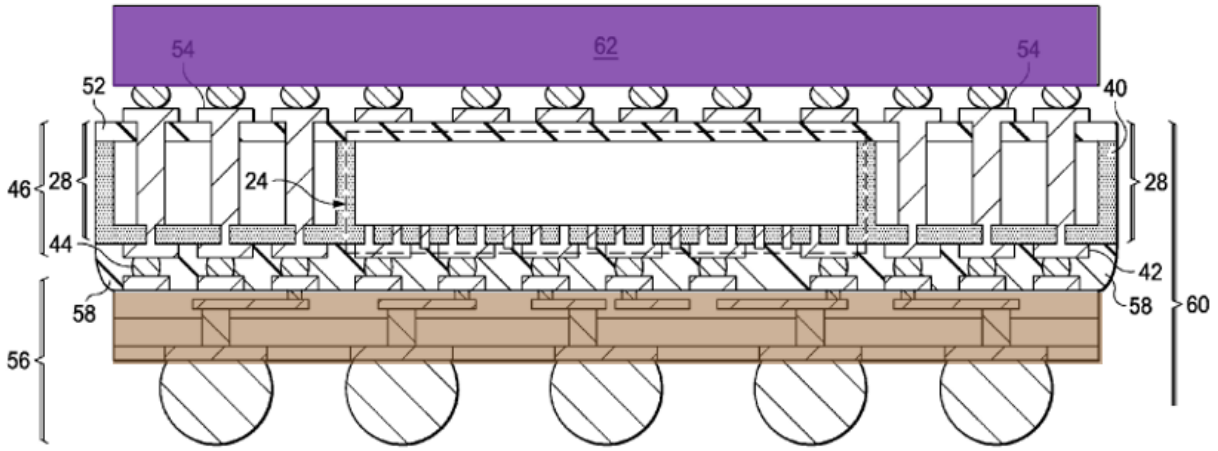


FIG. 9

EX1003, Figure 9. EX1002, ¶¶ 66–67.

d) [1C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate,

Chen discloses [1C]. As shown in Figures 2 and 9 below, Chen discloses two (or more) **Through-Assembly Via (TAV) modules 28** that are interposed between the **top package component 62** and the **bottom package component 56**. *See* EX1003, [0012] ("FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, **TAV modules 28** are disposed on opposite sides of package component 24. Although two **TAV modules 28** are illustrated, there may be one or more than two TAV modules 28.").

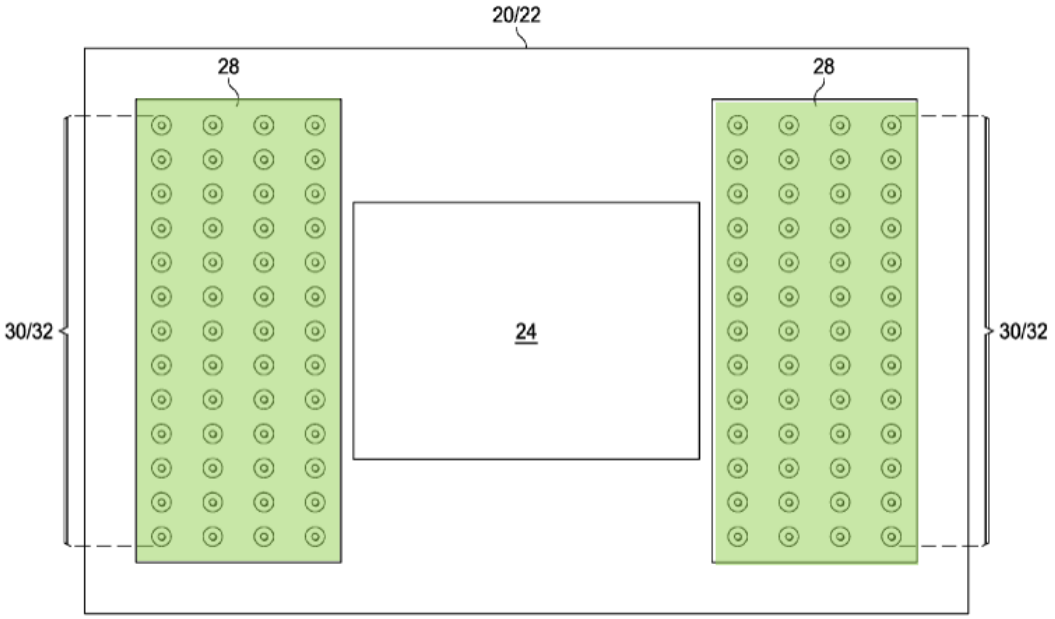


FIG. 2

EX1003, Figure 2. EX1003, [0019] ("In the resulting package, **TAV modules 28** are used to electrically couple the circuit devices in **package component 62** to **package component 56**.").

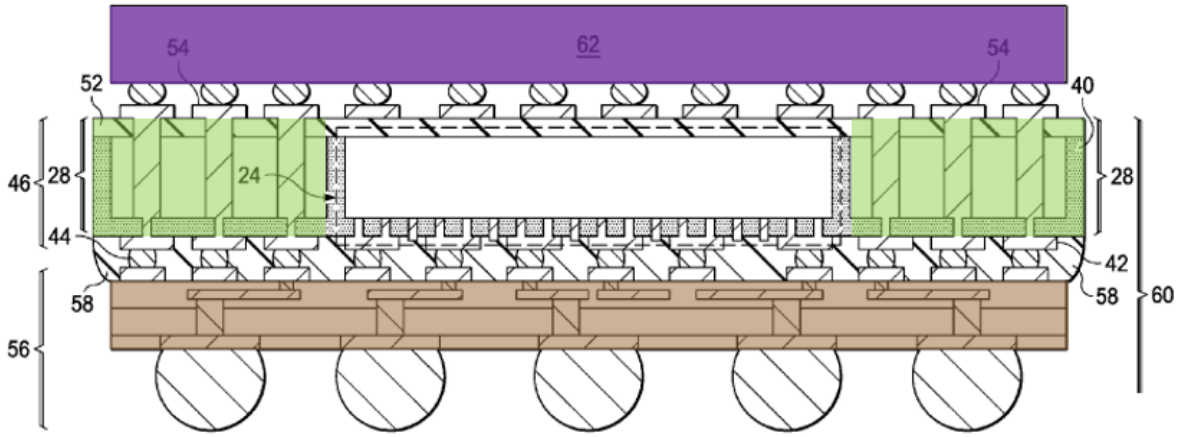


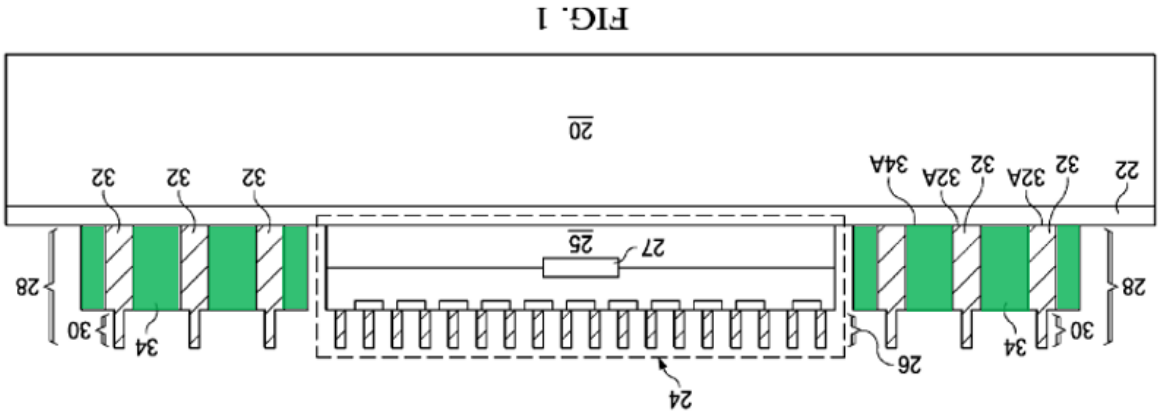
FIG. 9

EX1003, Figure 9. EX1002, ¶68–70.

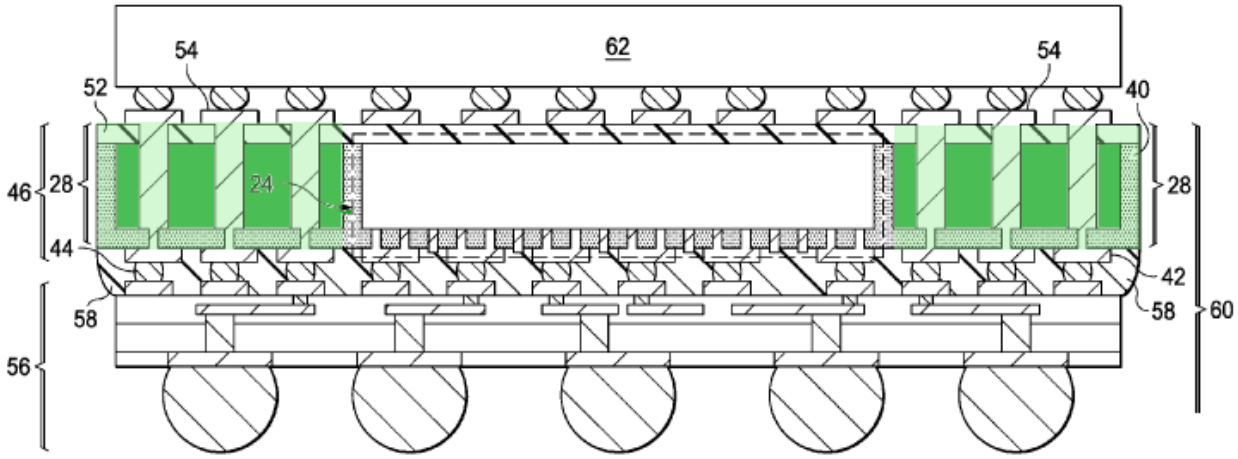
As shown above in Figure 9, the placement of the two **TAV modules 28** that are level with each other defines a space (in which a package component 24 resides) between the **top package component 62** and the **bottom package component 56**. *See* EX1003, [0009] ("Package component 24 and **Through-Assembly Via (TAV) modules 28** are then placed on release layer 22. The bottom surfaces of package component 24 and **TAV modules 28** are in contact with the top surface of release layer 22, and are level with each other. … In some embodiments, a package component 24 includes one or a plurality of device dies. For example, package component 24 may include a Central Computing Unit (CPU) die or another type of logic die having logic circuits."), [0023]. EX1002, ¶71.

e) [1D] wherein the spacer connector comprises a core substrate;

Chen discloses [1D]. Chen discloses that each of the **TAV modules 28** includes a **substrate 34**. *See* EX1003, [0010] ("**TAV modules 28** include **substrate 34**, which may be a semiconductor substrate such as a silicon substrate.").



EX1003, Figure 1 (rotated 180 degrees to be in the same orientation as Figure 9).

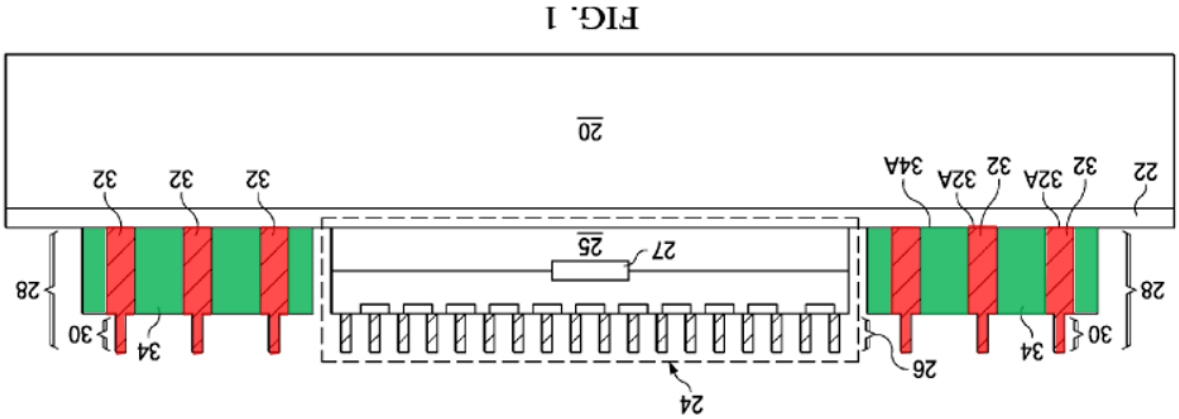


EX1003, Figure 9. EX1002, ¶¶ 72–74.

f) [1E] a plurality of metal pillars, each passing through the core substrate;

Chen discloses [1E]. Chen discloses a number of different **through substrate vias 32** and **metal posts 30** made of metals (*e.g.*, copper), each of which pass through **substrate 34** of the TAV modules 28. *See* EX1003, [0010] ("**Through-substrate vias 32** are formed in **substrate 34** for inter-coupling the conductive features on

opposite sides of **substrate 34**. **Through-substrate vias 32** are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like.… TAV modules 28 may also include **metal posts 30** (such as copper posts).…”).



EX1003, Figure 1 (rotated 180 degrees to be in the same orientation as Figure 9).

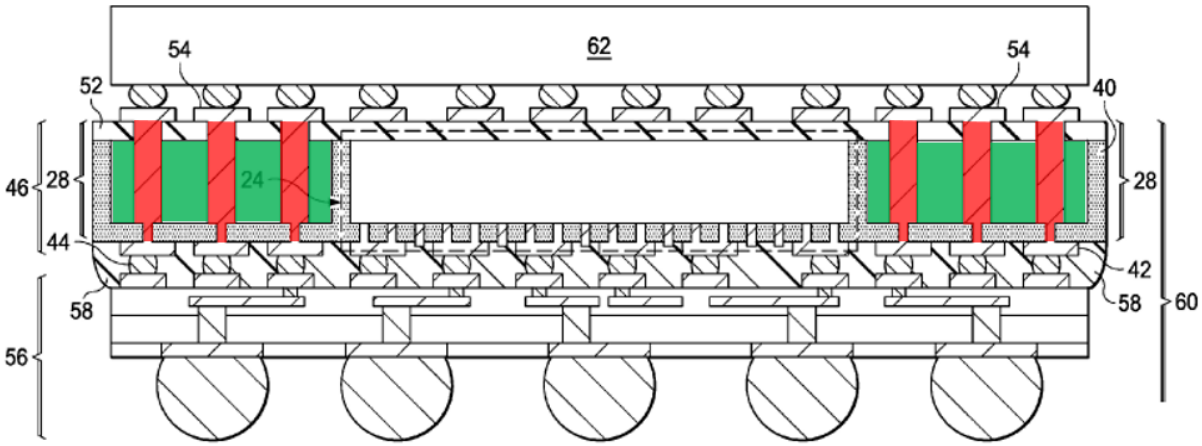


FIG. 9

EX1003, Figure 9. EX1002, ¶¶ 75–77.

g) [1F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;

Chen discloses, or at least renders obvious, [1F]. Chen discloses a number of **redistribution layers (RDLs) 54**, each of which are formed on top end of the **through-substrate vias 32**. EX1003, [0017] ("**RDLs 54** are then formed on dielectric layer 52 and connected to RDLs [42]."), claim 15 ("forming a first plurality of Redistribution Lines (RDLs) over the polymer and connected to the metal posts of the device die and the metal posts of the TAV module, wherein the device die, the TAV module, and the first plurality of RDLs form a package; … forming a **second plurality of RDLs** coupled to the **plurality of through-vias**, wherein the first and the second plurality of RDLs are on opposite sides of the package."), claim 17 ("wherein the **second plurality of RDLs** is electrically coupled to the **plurality of through-vias** through openings in the dielectric layer."). **RDLs 54** provide the same functionality as the claimed **metal pads** and therefore meet the claimed "**plurality of metal pads**." *See, e.g.,* EX1001, 2:36–39 ("The package substrate 1 has a plurality of bottom metal pillars 101B, each metal pillar 101B is electrically coupled to a corresponding **top metal pad 152** of the spacer connector 10.")

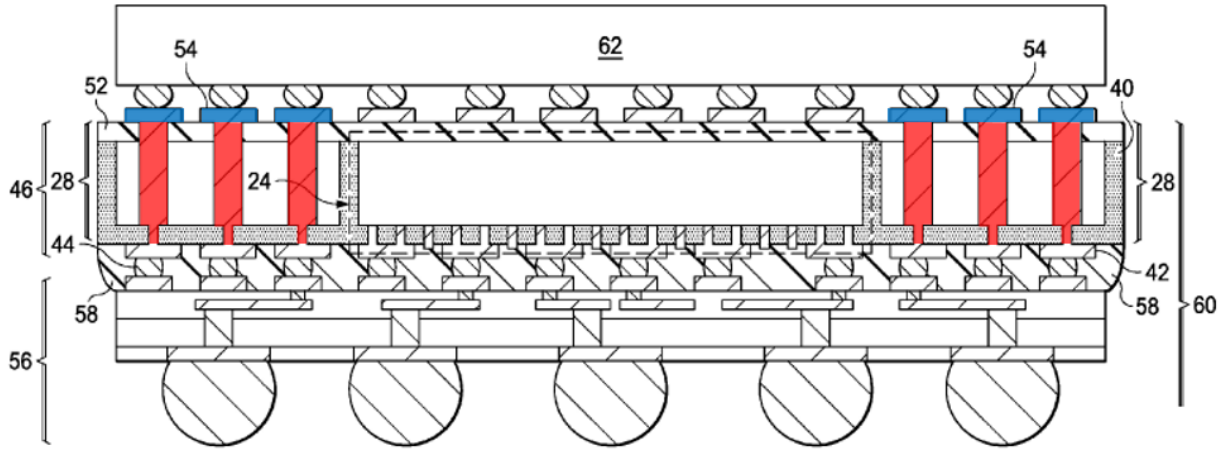


FIG. 9

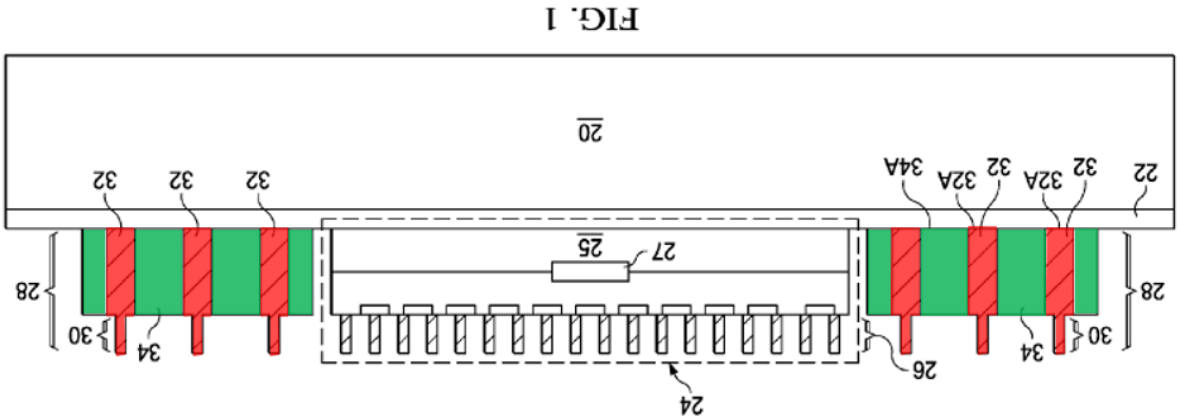
EX1003, Figure 9. EX1002, ¶¶ 78–79.

To the extent Chen does not explicitly describe **RDLs 54** being formed of **metal**, it would have been obvious to form **RDLs 54** as **metal pads** because Chen describes that the same corresponding ***RDLs 42*** on the opposite side of the **TAV modules 28** are deposited as a metal layer and patterned. *See* EX1003, [0014] ("***RDLs 42*** may be formed by depositing a ***metal layer***, and then patterning the ***metal layer***."). The modification amounts to nothing more than the use of a known technique in the same way (depositing and patterning a metal layer to form metal pads) to form the same type of structures (***RDLs 42*** and **RDLs 54**). Metal is often utilized for electrical coupling because it is well-known to have low electrical resistance and therefore a POSITA would have been motivated to lower the electrical resistance of the overall structure by utilizing low resistance materials, such as **metals**, as **RDLs 54**. Accordingly, a POSITA would have been able to readily

apply the teachings related to the formation of ***RDLs 42*** to that of **RDLs 54** with a reasonable expectation of success. EX1002, ¶¶ 80–81.

h) [1G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate;

Chen discloses [1G]. Chen discloses that the **through-substrate vias 32** have **metal posts 30** that protrude down from a bottom surface of **substrate 34**. *See* EX1003, [0010] ("**Through-substrate vias 32** are formed in **substrate 34** for inter-coupling the conductive features on opposite sides of **substrate 34**. **Through-substrate vias 32** are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like. … **TAV modules 28** may also include **metal posts 30** (such as copper posts) formed as top portions of **TAV modules 28**."), [0011],



EX1003, Figure 1 (rotated 180 degrees to be in the same orientation as Figure 9).

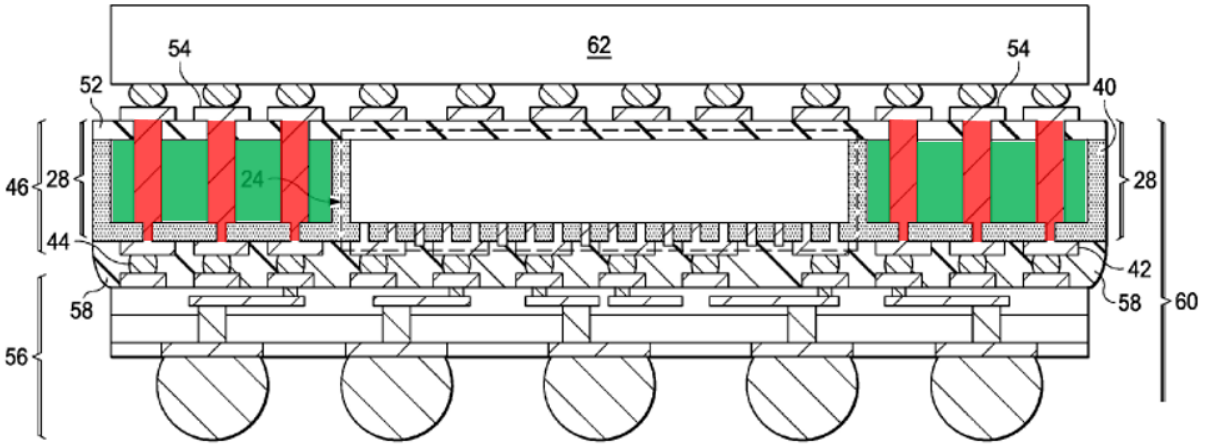


FIG. 9

EX1003, Figure 9. EX1002, ¶¶ 82–84.

i) [1H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,

Chen and Sun render obvious [1H]. First, Chen discloses the **package component 62** and **package component 56** that are **electrically coupled** to each other by (from top to bottom) unlabeled **connectors**[2] (that appear nearly identical to connectors 44 on the opposite side of the TAV modules 28), **RDLs 54**, **through-substrate vias 32**, **metal posts 30**, **RDLs 42**, and connectors 44. *See* EX1003, [0019] ("FIG. 9 illustrates the bonding of **top package component 62** to bottom

[2] Petitioner specifically relies on the six unlabeled **connectors** colored in Figure 9 of Chen below as rendering obvious the claimed "**plurality of bottom metal pillars**."

package 60. … In the resulting package, **TAV modules 28** are used to **electrically couple** the circuit devices in **package component 62** to **package component 56**.”), [0014] (“Next, referring to FIG. 4, **Redistribution Lines (RDLs) 42** and **connectors 44** are formed to connect to **metal posts** 26 and **30**.”), [0017] (“**RDLs 54** are then formed on dielectric layer 52 and connected to **RDLs [42]**.”), claim 1 (“wherein the **first plurality of RDLs** is electrically coupled to the **second plurality of RDLs** through the plurality of **through-vias** in the **TAV module**”), claim 15 (“forming a **first plurality of Redistribution Lines (RDLs)** over the polymer and connected to the metal posts of the device die and the **metal posts** of the **TAV module**, wherein the device die, the TAV module, and the first plurality of RDLs form a package; … forming a **second plurality of RDLs** coupled to the **plurality of through-vias**, wherein the **first [plurality of RDLs]** and the **second plurality of RDLs** are on opposite sides of the package.”).

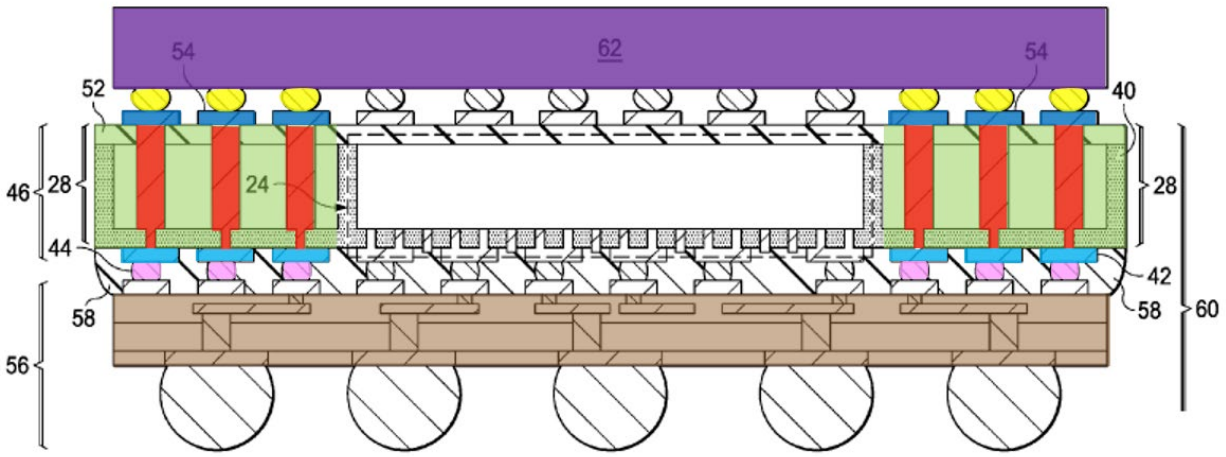


FIG. 9

EX1003, Figure 9. EX1002, ¶¶ 85–87.

Chen discloses that "**[c]onnectors 44** may also include **metal pillars**, or **metal pillars** and solder caps."[3] EX1003, [0014]. Chen does not explicitly state that the unlabeled **connectors**—that appear nearly identical to **connectors 44** on the opposite side of the **TAV modules 28**—are metal. But like **connectors 44**, a POSITA would have readily recognized that it would have been obvious to utilize **metal pillars** as the unlabeled **connectors**. EX1002, ¶88.

Sun, like the '202 Patent, is directed to a package-on-package structure.[4] *See, e.g.,* EX1004, [0002] ("A package on package (PoP) comprises two electronic packages assembled in a vertical stack."), [0041] ("FIG. 12 is a schematic view of a

[3] To be clear, solder and metal pillars are two distinct structures and are not equivalent to one another.

[4] Sun is therefore analogous art for this reason alone because Sun is in the same field of endeavor as the '202 Patent. Independently, Sun is analogous art because a POSITA would have also found Sun to be reasonably pertinent to the '202 Patent because it deals with the same problem of electrically coupling a top package substrate to a bottom package substrate through the use of an intermediate second substrate. *See* EX1001, claim 1 ("the top package substrate is electrically coupled to the bottom package substrate through… the spacer connector…"). EX1002, ¶89.

PoP assembly comprising first and second modules."); EX1001, claim 1. Moreover, Sun, like Chen, describes a structure having a **first substrate 110** electrically coupled to a **third substrate 20** via an intermediate **second substrate 300**. *See* EX1004, [0012] ("In one aspect of the present invention a (first) module is proposed comprising a **first substrate** and at least one chip mounted on the first substrate; a **second substrate** mounted to the **first substrate** …; the **first substrate** being electrically connected to the **second substrate** by at least one **first electrical connector**; and at least one **second electrical connector** extending from the **second substrate** through the overmold and having an exposed end for electrical connection to an external module."), [0022] ("Preferably the at least one **second electrical connector** is in electrical contact with a conducting contact of the **third substrate**.").

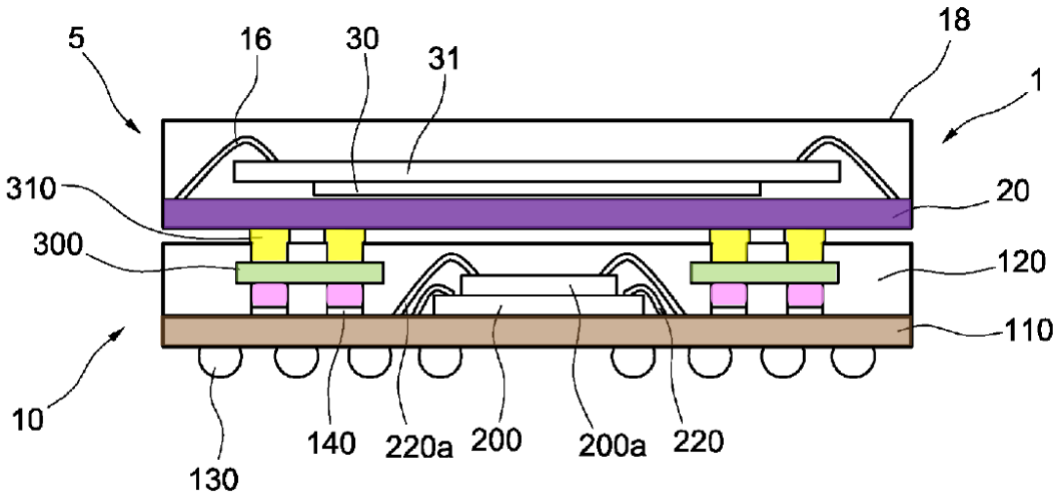


FIG.12

EX1004, Figure 12. The details of the **connection 310** between the **third substrate 20** and the **second substrate 300** is shown below in Figure 14.

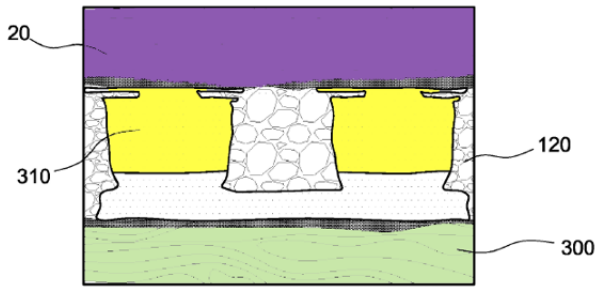


FIG.14(a)

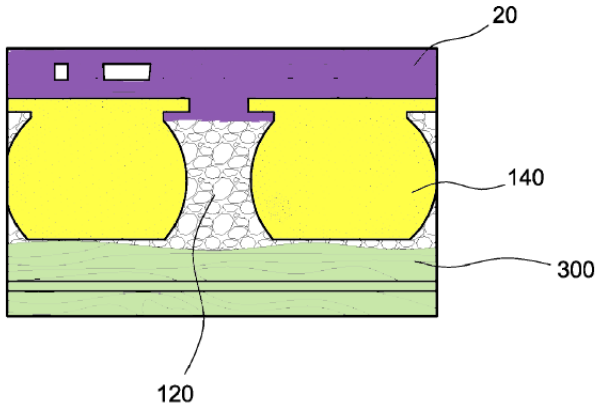


FIG.14(b)

EX1004, Figure 14. Sun teaches that the **connection 310** can be formed of **metal pillars**. *See* EX1004, [0066] ("FIG. 14 (a) illustrates a pair of **second connectors 310**. They have the same structure as the first connectors 320. They are formed of **metal pillars**, preferably **copper pillars**."). This is contrasted with Figure 14(b), which utilizes **solder balls 140** instead. *See* EX1004, [0066] ("By way of contrast FIG. 14(b) shows an arrangement with a pair of **solder balls 140** between a **substrate 20** and a **substrate 300**."). EX1002, ¶¶ 89–91.

It would have been obvious to combine Chen with Sun to connect the **TAV modules 28** to the **top package component 62** with **metal pillars** with a reasonable expectation of success. Indeed, a POSITA would have been motivated to make such a modification because Sun teaches the benefits of utilizing pillars, instead of other

connector structures such as solder. *See* EX1004, [0066] ("FIG. 14 (a) illustrates a pair of **second connectors 310**. They have the same structure as the first connectors 320. They are formed of **metal pillars**, preferably copper pillars. It can be seen that the pillars have fine pitch and a well defined shape. By way of contrast FIG. 14(b) shows an arrangement with a pair of solder balls 140 between a substrate 20 and a substrate 300. It can be seen that the solder balls have a less fine pitch and less well defined shape than the metal pillars. Furthermore, at typical processing temperatures (e.g. around 260 degrees Celsius) the solder balls will melt and collapse down, while the metal (e.g. copper) pillars will remain solid and well defined. ***As a result, for a given stand off height,* metal pillars *provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates***. The **metal pillars** allow finer pitch and thus denser electrical connections. A small amount of solder or bonding pads may used to connect the **metal pillars** to the respective other substrates."). EX1002, ¶92.

j) [1I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,

Chen discloses [1I]. Chen discloses **connectors 44** that include **metal pillars** on the top surface of the **bottom package component 56** that are coupled to the **through-substrate vias 32** and **metal posts 30** in the **TAV modules 28**. EX1003,

[0014] ("Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and **connectors 44** are formed to connect to **metal posts** 26 and **30**. … **Connectors 44** may also include **metal pillars**, or **metal pillars** and solder caps, which may also be formed through plating.").

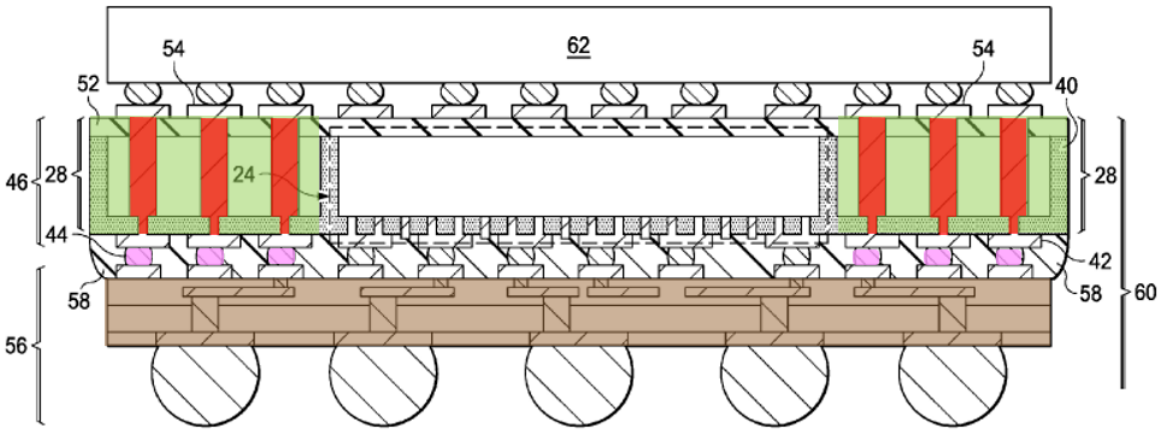


FIG. 9

EX1003, Figure 9. EX1002, ¶¶ 93–96.

k) [1J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and

Chen and Sun render obvious [1J] for at least the reasons explained in [1H]. *See* Section VIII.A.1.i) [Ground I, [1H]].

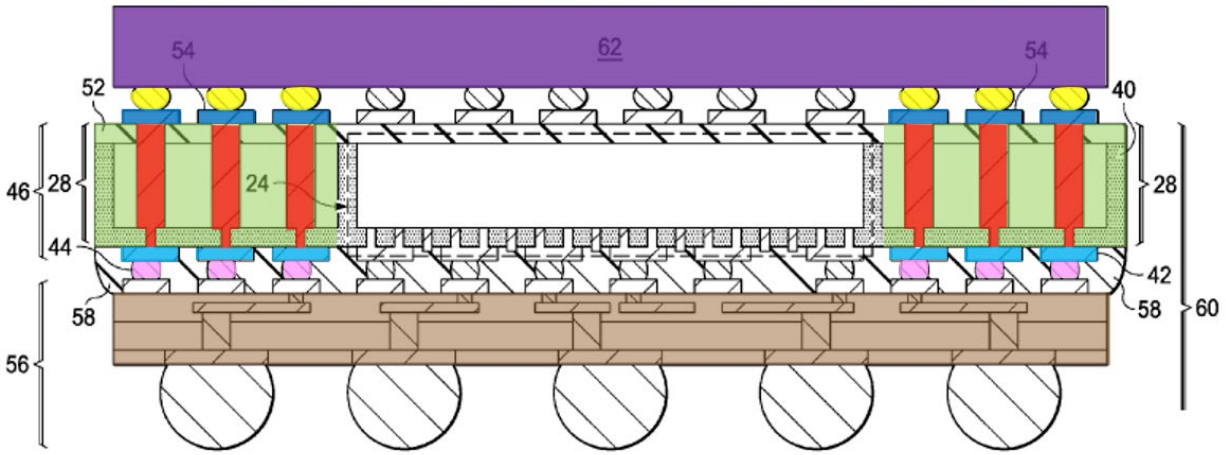


FIG. 9

EX1003, Figure 9. EX1002, ¶¶ 97–98.

l) [1K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate,

Chen discloses [1K]. Chen discloses a **package component 24 (*e.g.*, CPU die, memory die, device die, etc.)** that is arranged in the space between the **bottom package component 56** and the **top package component 62**. *See* EX1003, [0009] ("In some embodiments, **package component 24** includes one or a plurality of **device dies**. For example, **package component 24** may include a **Central Computing Unit (CPU) die** or another type of logic die having logic circuits. In alternative embodiments, **package component 24** includes a plurality of **memory dies** stacked together (please refer to FIG. 11). In the embodiments wherein **package component 24** is a **device die**, package component 24 may include semiconductor substrate 25 and active devices (such as transistors) 27 at a top surface of

semiconductor substrate 25."), [0019] ("In the resulting package, **TAV modules 28** are used to electrically couple the circuit devices in **package component 62** to **package component 56**."). It is well-known that the terms "die" and "chip" are synonymous with one another. *See, e.g.,* EX1008, [0007] (using the terms "integrated circuit (IC) **chip *or* die**" interchangeably).

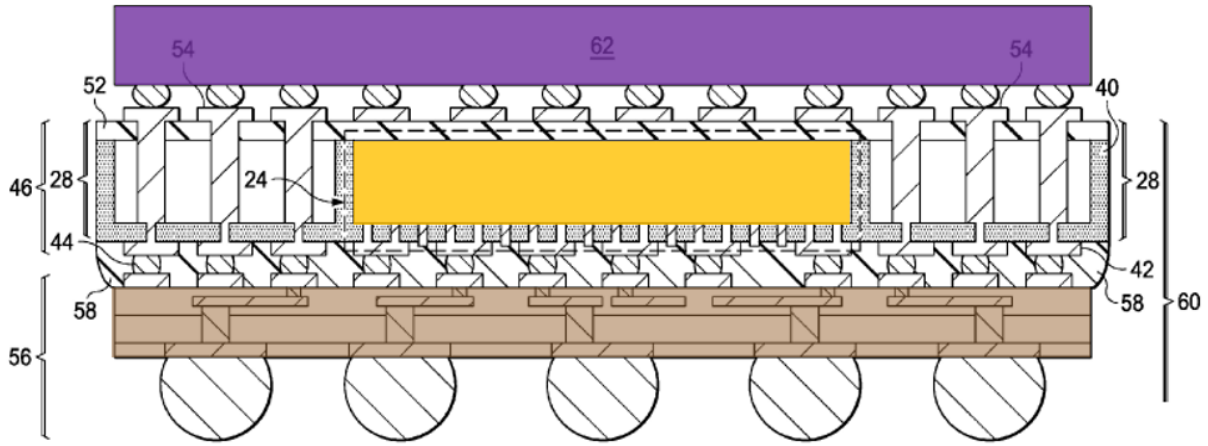


FIG. 9

EX1003, Figure 9. EX1002, ¶¶99–102.

m) [1L] wherein the bottom chip is mounted to the top surface of the bottom package substrate,

Chen discloses [1L]. As shown in Figure 9, Chen discloses that the **package component 24** is mounted on the top surface of the **bottom package component 56**. *See* EX1003, [0014] ("Throughout the description, the structure including **package component 24**, TAV modules 28, and polymer 40 is referred to as **package 46**."), [0018] ("Referring to FIG. 8, **package 46** is bonded to **package component**

56 to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like.”).

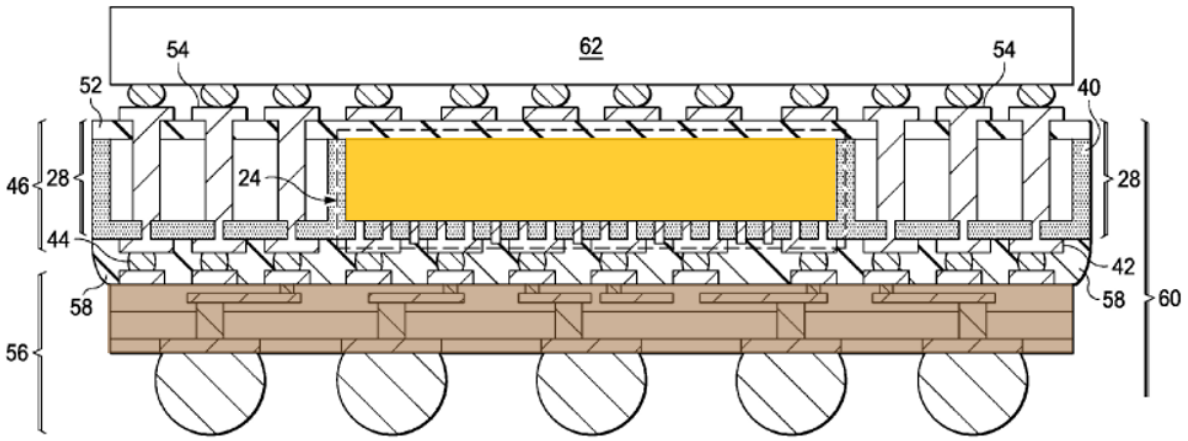


FIG. 9

EX1003, Figure 9. EX1002, ¶¶ 103–104.

n) [1M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

Chen discloses [1M]. Chen discloses two **TAV modules 28** arranged on opposite sides of **package component 24**. *See* EX1003, [0012] (“FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, **TAV modules 28** are disposed on opposite sides of **package component 24**. Although two **TAV modules 28** are illustrated, there may be one or more than two **TAV modules 28**.”).

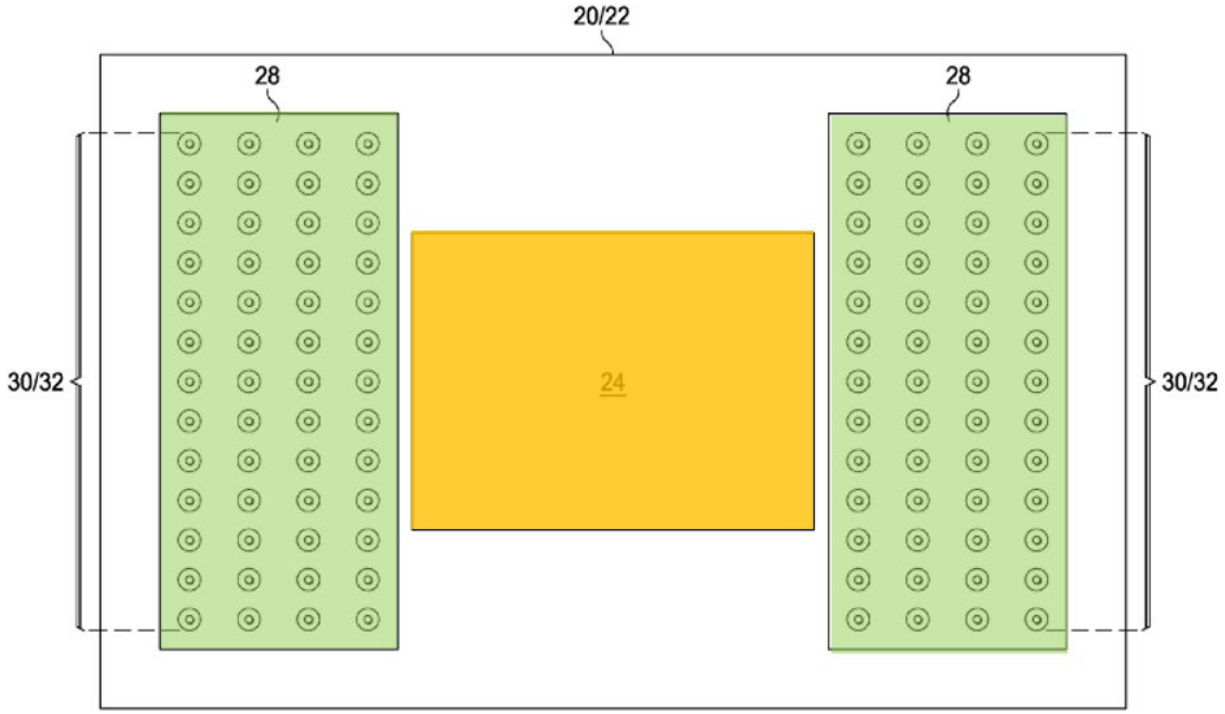


FIG. 2

EX1003, Figure 2.

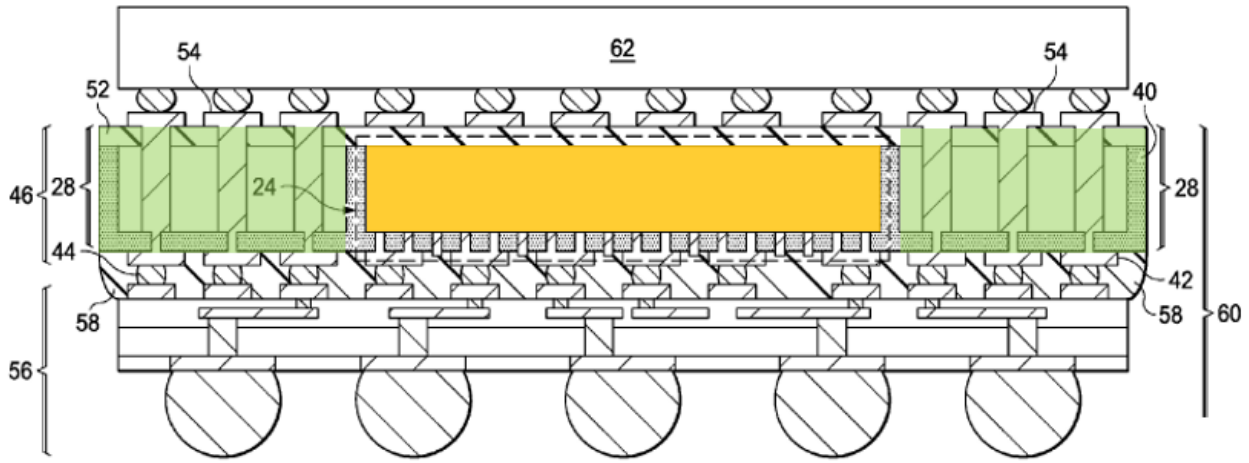


FIG. 9

EX1003, Figure 9. EX1002, ¶¶105–106.

2. Dependent Claim 2

a) [2Pre] The structure of claim 1, wherein

See Section VIII.A.1 [Ground I, claim 1]. EX1002, ¶107.

b) [2A] a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

Chen discloses [2A]. As shown in Figure 9, Chen discloses that the top surface of the **package component 24** is spaced downwardly from the bottom surface of **top package component 62**.

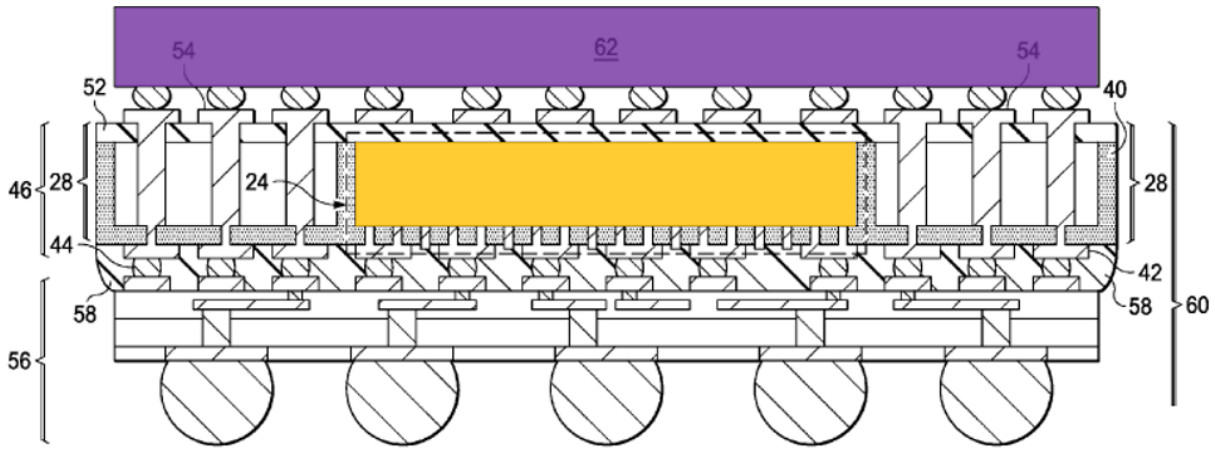


FIG. 9

EX1003, Figure 9. *See also* EX1003, [0020] ("FIG. 10 illustrates an exemplary embodiment wherein **package component 62** includes a plurality of stacked dies 64. … Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to **package component 24**, which are further connected to the RDLs 54 over and aligned to TAV modules 28."), [0014], [0018], [0019]. EX1002, ¶¶108–109.

3. Dependent Claim 3

a) [3Pre] The structure of claim 2, further comprising:

See Section VIII.A.2 [Ground I, claim 2]. EX1002, ¶110.

b) [3A] a top chip mounted to the top surface of the top package substrate,

Chen and Sun render obvious [3A]. First, Chen discloses **a device die (not shown)** mounted to (i.e., bonded to) the **package substrate (not shown)** of **package component 62**. *See* EX1003, [0019] ("Alternatively, **package component 62** is a package that includes a **device die (not shown)** bonded to a **package substrate (not shown)**, an interposer (not shown), or the like.").

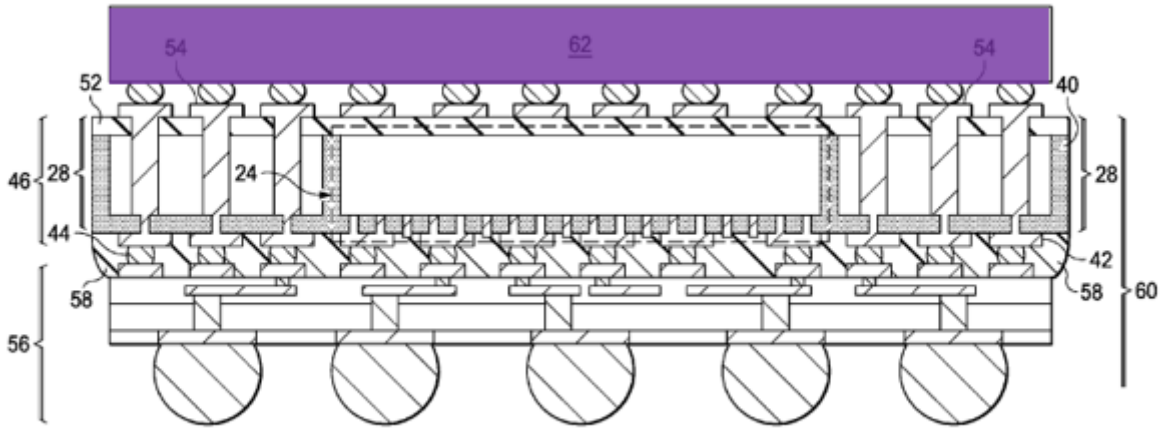


FIG. 9

EX1003, Figure 9. EX1002, ¶¶111–112.

Although Chen does not explicitly disclose whether the **device die (not shown)** is bonded to the ***top surface*** of the **package substrate (not shown)**, such a configuration was well-known. As explained in [1H], Sun, like Chen, describes a

structure having a **first substrate 110** electrically coupled to a **third substrate 20** via an intermediate **second substrate 300**. *See* Section VIII.A.1.i) [Ground I, [1H]].

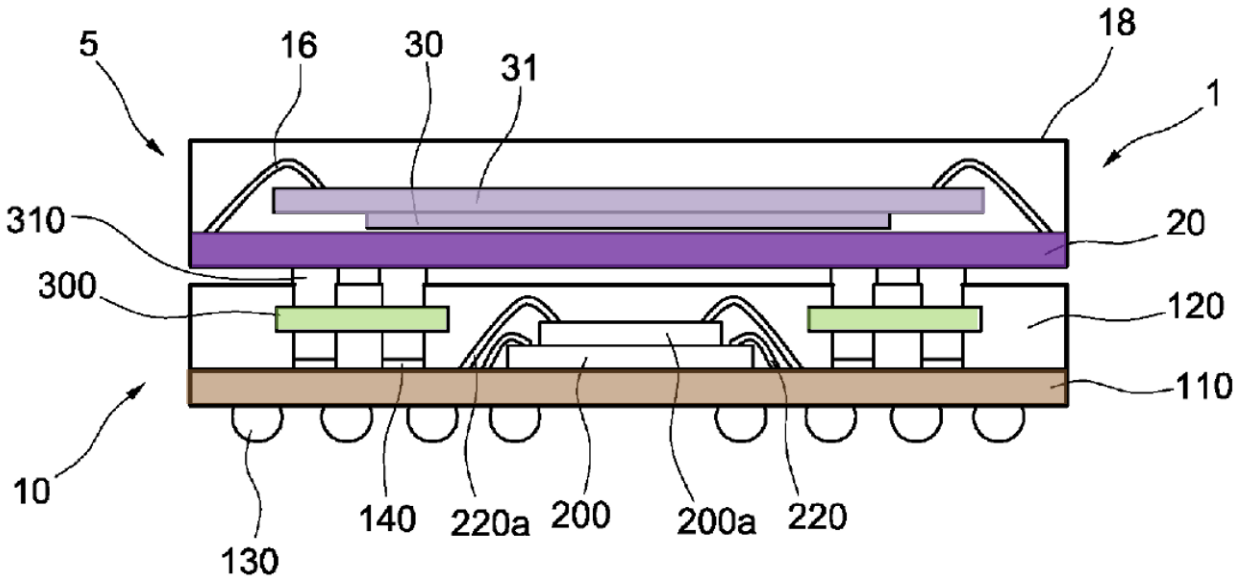


FIG.12

EX1004, Figure 12. As shown above, **chips 30 and 31** are mounted to the top surface of the **third substrate 20**. *See* EX1004, [0059] ("The upper module 5 comprises a **pair of chips 30, 31** mounted to a first (upper) side of a **third substrate 20**. The **third substrate** may be a PCB, preferably a BT core substrate. The **chips 30, 31** are electrically connected to the **third substrate 20** by wires or any other suitable means."). EX1002, ¶¶113–114.

A POSITA would have been able to make the modification with a reasonable expectation of success. Chen already teaches that "**package component 62** is a package that includes a **device die (not shown)** bonded to a **package substrate (not**

shown)." EX1003, [0019]. It would have been obvious for a POSITA to place Chen's **device die (not shown)** or Sun's **chips 30 and 31** on Chen's **package substrate (not shown)** in the manner shown in Figure 12 of Sun with a reasonable expectation of success because it merely provides one known technique of mounting **device die(s)** on Chen's **package substrate (not shown)**. Mounting Chen's **device die (not shown)** or Sun's **chips 30 and 31** on the top surface of Chen's **package substrate (not shown)** merely amounts to combining known prior art elements (Chen's **device die (not shown)** or Sun's **chips 30 and 31** with Chen's **package substrate (not shown)**) according to known methods (by placing Chen's **device die (not shown)** or Sun's **chips 30 and 31** on a readily available top surface of Chen's **package substrate (not shown)**) to yield the predictable results of a **die/chip** sitting on the top surface of a **package substrate** for electrical coupling to another chip on another substrate. At a minimum, it would have been obvious to try from the finite number of possible places for mounting the **dies** (either the top or bottom surface of the **package substrate** because a POSITA would have readily recognized that mounting to the side surfaces of the **package substrate** would not be an efficient approach) that a POSITA would have reasonably expected to have succeeded. EX1002, ¶¶114–115.

c) [3B] wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

Chen and Sun render obvious [3B]. As shown below in Figure 12 of Sun, **chips 30 and 31** overlap the **chip 200** and each of the **second substrates 300**. *See Regents of the Univ. of Cal. v. Satco Prods., Inc.,* No. 2023-1356, 2024 WL 7311186 (Fed. Cir. Dec. 4, 2024) ("[P]atent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their spatial relations to one another.").

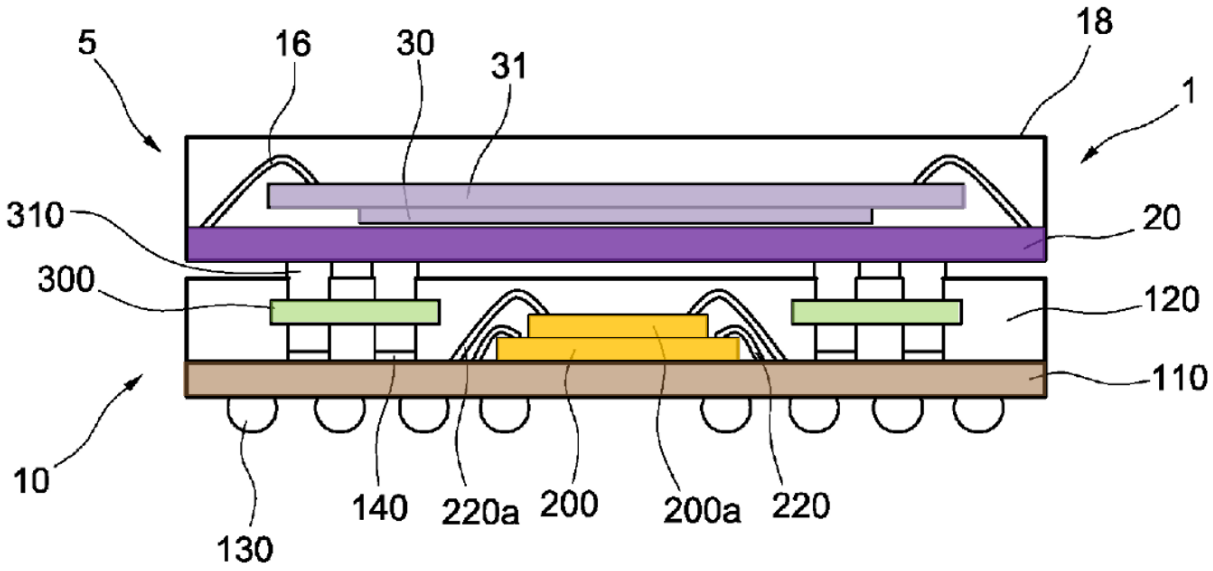


FIG.12

EX1004, Figure 12. EX1002, ¶¶116–117.

Chen similarly teaches that the **package component 62** depicted in Figure 9 itself can be a **device die** that is over the **package component 24** and the **TAV modules 28**. *See* EX1003, [0019] ("In some embodiments, **top package component 62** is a **device die**. Alternatively, **package component 62** is a package that includes a **device die (not shown)** bonded to a **package substrate (not shown)**, an interposer (not shown), or the like."). EX1003, [0020] ("FIG. 10 illustrates an exemplary embodiment wherein **package component 62** includes a plurality of stacked dies 64. … Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to **package component 24**, which are further connected to the RDLs 54 over and aligned to **TAV modules 28**."), [0014], [0018].

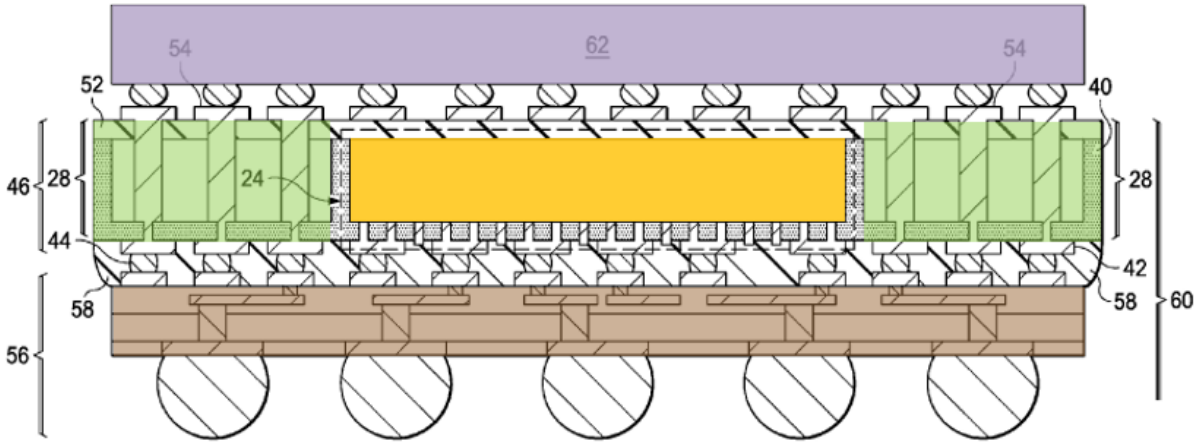


FIG. 9

EX1003, Figure 9. EX1002, ¶118.

It would have been obvious to bond Chen's **device die (not shown)** or Sun's **chips 30 and 31** to the top surface of Chen's **package substrate (not shown)** such

that Chen's **device die** or Sun's **chips 30 and 31** overlaps Chen's **package component 24** and each of the two **TAV modules 28**, for at least the same reasons explained above in [3A]. *See also* Section VIII.A.3.b) [Ground I, [3A]]. EX1002, ¶119.

4. Dependent Claim 4

a) [4Pre] The structure of claim 1, wherein

See Section VIII.A.1 [Ground I, claim 1]. EX1002, ¶120.

b) [4A] each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

Chen and Sun render obvious [4A] for at least the reasons discussed in [1H] and [1I]. *See* Sections VIII.A.1.i) [Ground I, [1H]] and VIII.A.1.j) [Ground I, [1I]].

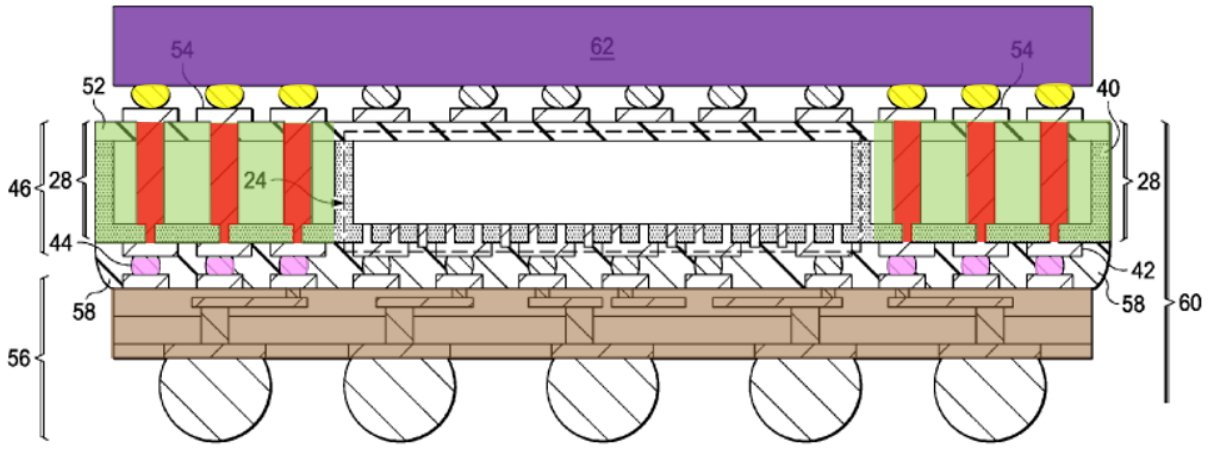


FIG. 9

EX1003, Figure 9. EX1002, ¶¶121–122.

5. Dependent Claim 7

a) [7Pre] The structure of claim 4, wherein

See Section VIII.A.4 [Ground I, claim 4]. EX1002, ¶123.

b) [7A] the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate, and

Chen discloses [7A]. Chen discloses that the **TAV modules 28** include a **layer of polymer 40** on the bottom surface of the **substrate 34**. *See* EX1003, [0013] ("Referring to FIG. 3, **polymer 40** is molded on package component 24 and **TAV modules 28**. **Polymer 40** fills the gaps between package component 24 and **TAV modules 28**, and may be in contact with release layer 22. Furthermore, **polymer 40** is filled into the gaps between metal posts 26, and into the gaps between metal posts 30. **Polymer 40** may include a molding compound, a molding underfill, or a kind of epoxy. The top surface of **polymer 40** may be level with or higher than the top surfaces of metal posts 26 and 30."). Polymers are well-known to be dielectric. *See, e.g.,* EX1011, [0056] (discussing an "insulating layer 144 contain[ing] … polymer dielectric").

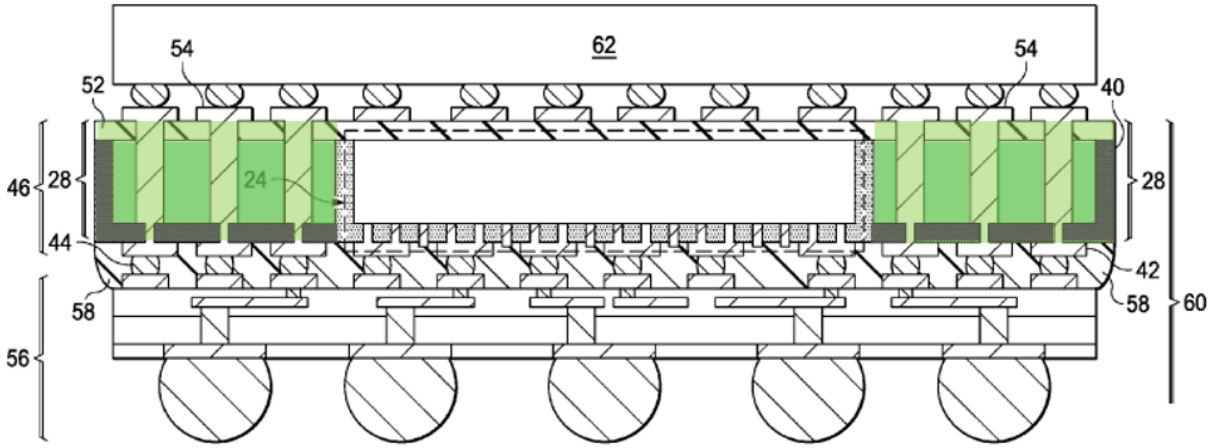


FIG. 9

EX1003, Figure 9. EX1002, ¶¶124–125.

c) [7B] the plurality of metal pillars pass through the core substrate and the dielectric layer.

Chen discloses [7B]. Chen discloses that the **through-substrate vias 32** and **metal posts 30** pass through the **substrate 34** and **polymer 40**. *See* EX1003, [0010] ("**Through-substrate vias 32** are formed in **substrate 34** for inter-coupling the conductive features on opposite sides of **substrate 34**. **Through-substrate vias 32** are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like. In some embodiments, bottom ends 32A of **through-substrate vias 32** are level with the bottom surface 34A of **substrate 34**. Accordingly, bottom ends 32A of **through-substrate vias 32** may be in contact with release layer 22. TAV modules 28 may also include **metal posts 30** (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of **metal post** 26 and **30** are

substantially level with each other."), [0013] ("Referring to FIG. 3, **polymer 40** is molded on package component 24 and TAV modules 28. **Polymer 40** fills the gaps between package component 24 and TAV modules 28, and may be in contact with release layer 22. Furthermore, **polymer 40** is filled into the gaps between metal posts 26, and into the gaps between **metal posts 30**. **Polymer 40** may include a molding compound, a molding underfill, or a kind of epoxy. The top surface of **polymer 40** may be level with or higher than the top surfaces of **metal posts** 26 and **30**. A grinding step may be performed to grind **polymer 40**, until **metal posts** 26 and **30** are exposed.").

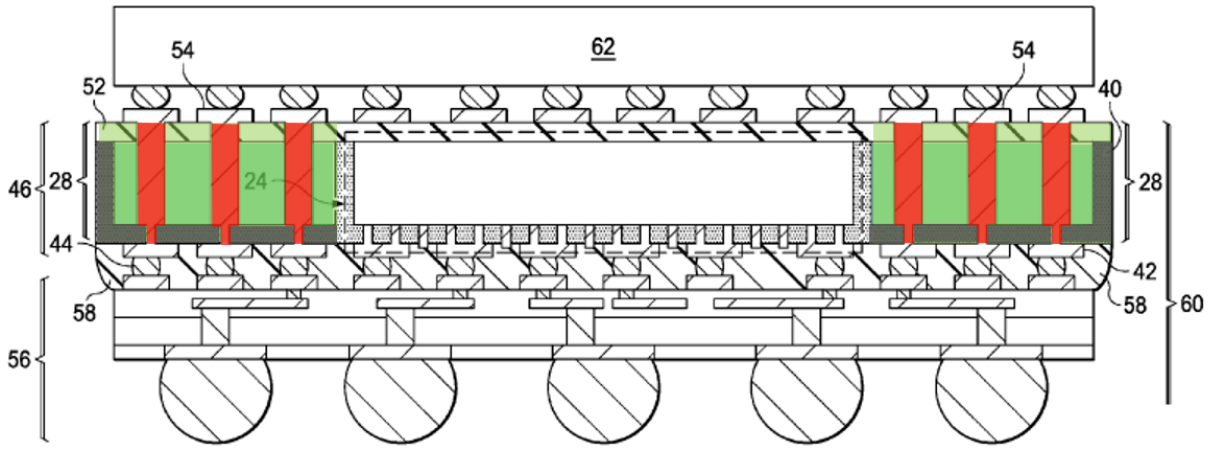


FIG. 9

EX1003, Figure 9. EX1002, ¶¶126–127.

6. Dependent Claim 8

a) [8Pre] The structure of claim 7, wherein

See Section VIII.A.5 [Ground I, claim 7]. EX1002, ¶128.

b) [8A] the dielectric layer is a dielectric adhesive in which the core substrate is pasted.

Chen discloses [8A]. Chen's **polymer 40** includes an epoxy, which is well-known to be a dielectric adhesive. *See* EX1003, [0013] ("**Polymer 40** may include a molding compound, a molding underfill, or **a kind of epoxy**."); *see also* EX1009, [0036] ("The **epoxy** resin may have a high cross-linking density, e.g., sufficient to exhibit strong curing and **adhesive** functions."), [0037] (listing out well-known **dielectric** materials as suitable examples of an epoxy resin, such as "bisphenol F, bisphenol A, and/or bisphenol AD epoxy resins"). EX1002, ¶130.

Moreover, Chen's **polymer 40** meets "in which the **substrate 34** is pasted"[5] because **polymer 40** is ***molded on*** the **TAV modules 28**, which includes **substrate 34**. EX1003, [0013] ("Referring to FIG. 3, **polymer 40 is molded on** package component 24 and **TAV modules 28**. **Polymer 40** fills the gaps between package

[5] During prosecution, the Examiner merely pointed to the final structure of the prior art reference as meeting this limitation. *See* EX1007, 102 ("Re Claim 19 Arai show and disclose … wherein the dielectric layer is a dielectric adhesive (dielectric layer 18 ***adhered to*** core 12, fig. 11) into which the core substrate is pasted."). And the Patent Owner acquiesced to that rejection. *See* EX1007, 113–125. EX1002, ¶XXXX.

component 24 and **TAV modules 28**, and may be in contact with release layer 22. Furthermore, **polymer 40** is filled into the gaps between metal posts 26, and into the gaps between metal posts 30.”), [0010] (“**TAV modules 28** include **substrate 34**, which may be a semiconductor substrate such as a silicon substrate. Alternatively, substrate 34 is a dielectric substrate such as a glass substrate.”).

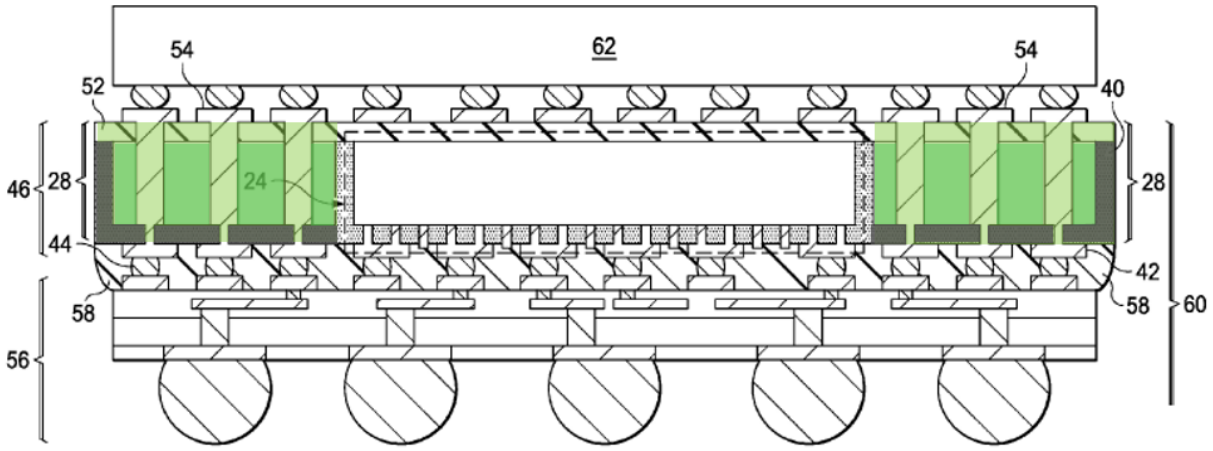


FIG. 9

EX1003, Figure 9. EX1002, ¶¶138–139.

7. Dependent Claim 9

a) [9Pre] The structure of claim 4, wherein

See Section VIII.A.4 [Ground I, claim 4]. EX1002, ¶133.

b) [9A] the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars,

Chen discloses [9A]. Chen discloses that the **TAV modules 28** include **RDLs 54**, each on the bottom end of a corresponding **metal post 30**. *See* EX1003, [0014] ("Next, referring to FIG. 4, **Redistribution Lines (RDLs) 42** and connectors 44 are formed to connect to **metal posts** 26 and **30**. As indicated by dashed lines, **RDLs 42** may also interconnect **metal posts** 26 and **30**. **RDLs 42** may be formed by depositing a metal layer, and then patterning the metal layer.").

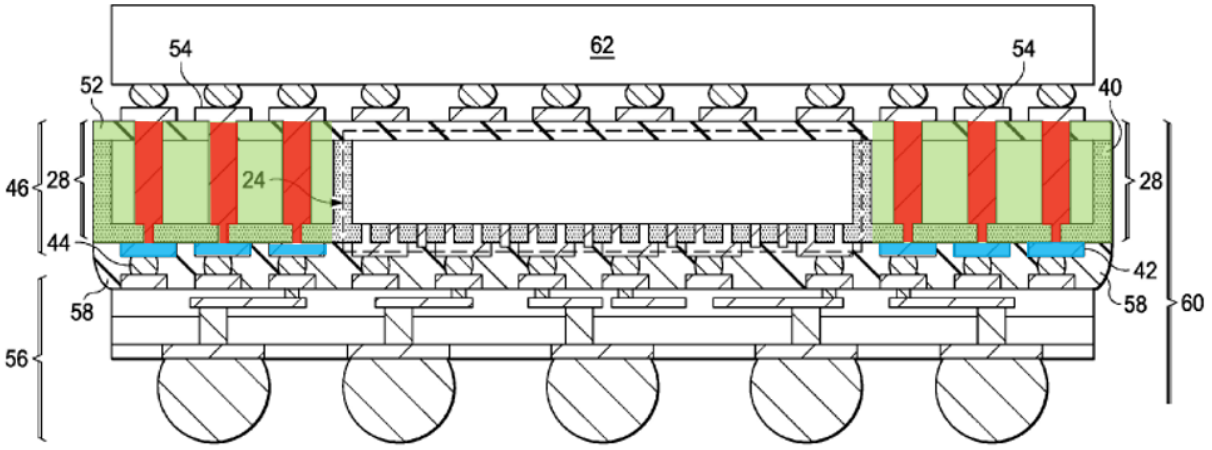


FIG. 9

EX1003, Figure 9. EX1002, ¶¶134–135.

c) [9B] the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and

Chen discloses [9B]. Chen discloses that the bottom ends of the **metal posts 30** are connected to corresponding top ends of the plurality of **connectors 44** (which may include **metal pillars**) of the **package component 56** via the corresponding **RDLs 42** of the **TAV modules 28**. EX1003, [0014] ("Next, referring to FIG. 4, **Redistribution Lines (RDLs) 42** and **connectors 44** are formed to connect to **metal posts** 26 and **30**. As indicated by dashed lines, **RDLs 42** may also interconnect **metal posts** 26 and **30**. **RDLs 42** may be formed by depositing a metal layer, and then patterning the metal layer. In some exemplary embodiments, the formation of **connectors 44** includes placing solder balls on the exposed portions of **RDLs 42**, and then reflowing the solder balls. … **Connectors 44** may also include **metal pillars**, or **metal pillars** and solder caps, which may also be formed through plating."), [0019] ("FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. … In the resulting package, **TAV modules 28** are used to electrically couple the circuit devices in package component 62 to **package component 56**.").

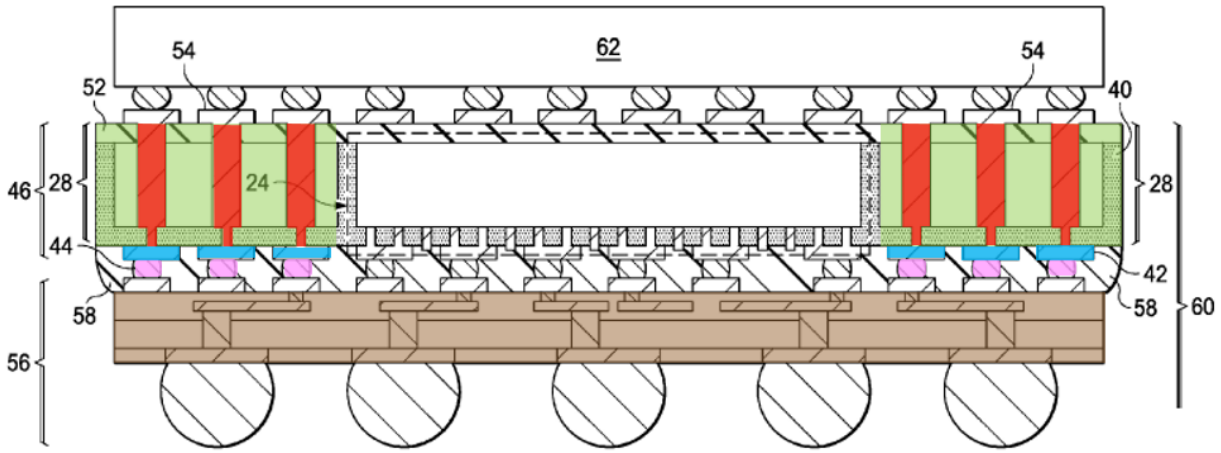


FIG. 9

EX1003, Figure 9. EX1002, ¶¶136–138.

d) [9C] bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Chen and Sun render obvious [9C] for at least the reasons described in [1F] and [1H]. *See* Sections VIII.A.1.g) [Ground I, [1F]] and VIII.A.1.i) [Ground I, [1H]].

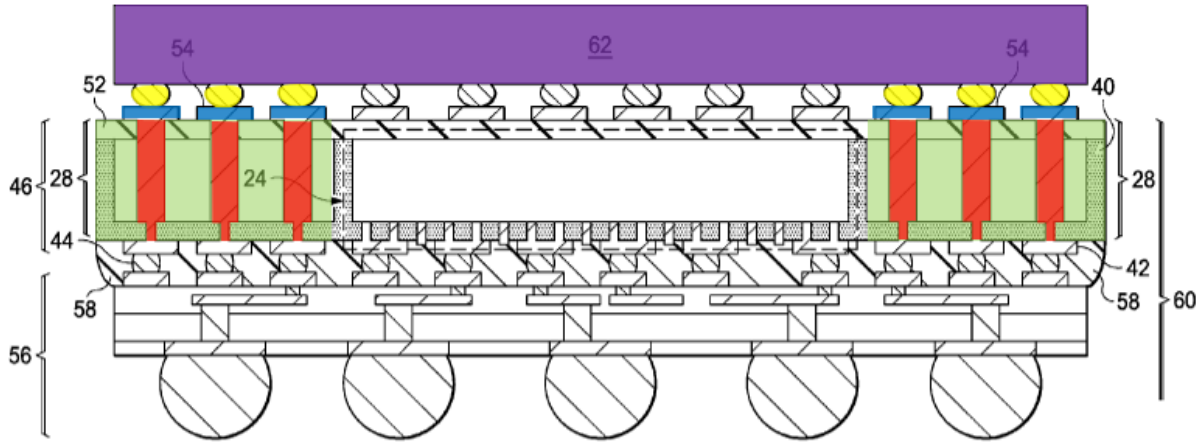


FIG. 9

EX1003, Figure 9. EX1002, ¶¶139–140.

B. Ground II: Claims 5–6 Are Rendered Obvious By Chen In View Of Sun And Furuta

1. Dependent Claim 5

a) [5Pre] The structure of claim 4, wherein

See Section VIII.A.4 [Ground I, claim 4]. EX1002, ¶141.

b) [5A] the spacer connector is free of metal pads on the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate, and each metal pillar among the plurality of metal pillars and the corresponding top metal pad of the spacer connector form a T shape.

Chen, Sun, and Furuta render obvious [5A]. First, as shown below, Chen teaches **RDLs 42** that are used to make an electrical connection between the **connectors 44** and **through substrate vias 32** and **metal posts 30** that protrude downwardly from the bottom surface of **substrate 34**.

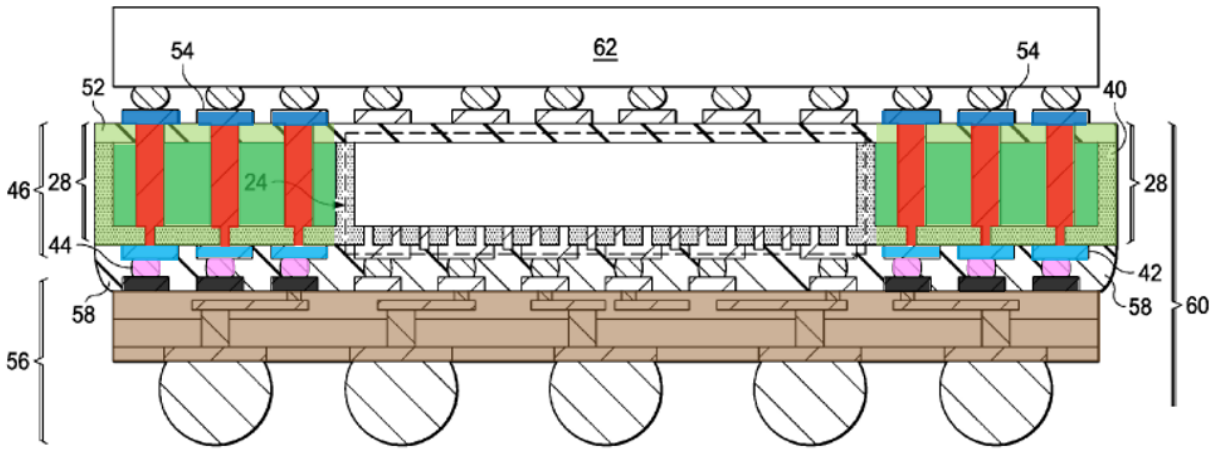


FIG. 9

EX1003, Figure 9. EX1002, ¶¶142–143.

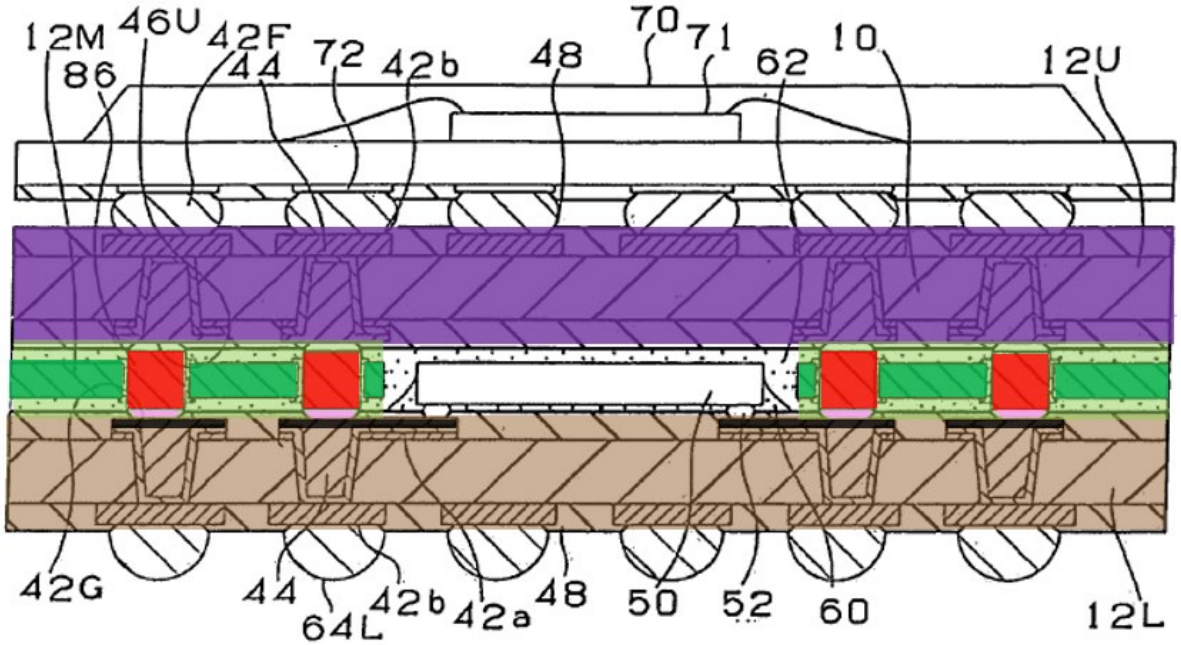
Nevertheless, it would have been obvious to make an electrical connection between **metal posts 30** and **connectors 44** without the use of **RDLs 42**. Furuta discloses a similar structure used to connect an **upper substrate 12U** with **lower substrate 12L** using an **interposer 12M**. *See* EX1006, [0020] ("FIG. 6(A) shows a cross-sectional view of combination substrate 10 according to Example 1. Combination substrate 10 is structured with **upper substrate (12U)**, **interposer (12M)** as an intermediate and **lower substrate (12L)**."). In other words, Furuta, like the '202 Patent, is directed to a package-on-package structure.[6] *See*, *e.g.*, EX1006 at [0003] ("The present invention relates to a combination substrate… where the package substrate and a substrate are electrically connected in a POP (Package On Package) structured with at least two substrates.").

---

[6] Furuta is therefore analogous art for this reason alone because Furuta is in the same field of endeavor as the '202 Patent. Independently, Furuta is analogous art because a POSITA would have also found Furuta to be reasonably pertinent to the '202 Patent because it deals with the same problem of electrically coupling a top package substrate to a bottom package substrate through the use of an interposer. *See* EX1001, claim 1 ("the top package substrate is electrically coupled to the bottom package substrate through… the spacer connector…"). EX1002, ¶144.

FIG. 6

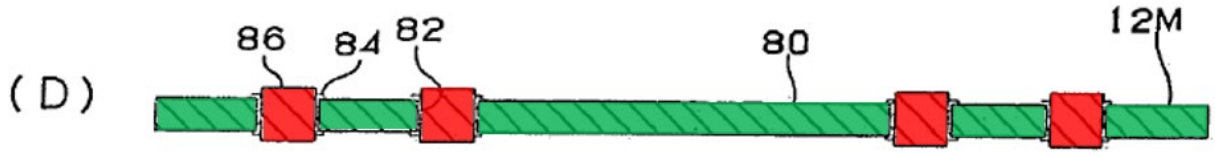
(A)



EX1006, Figure 6. EX1002, ¶¶142–144.

As shown above, the **interposer 12M** includes **metal posts 86** that electrically couple the **upper substrate 12U** and **lower substrate 12L**. *See* EX1006, [0021] ("**Metal posts 86** are formed, for example, of copper or copper alloy."), [0023] ("In combination substrate 10 according to Example 1, through **posts 86** fitted into through-holes 82 in **interposer (12M)**, connection pads (42G) on **lower substrate (12L)** and connection pads (42F) on **upper substrate (12U)** are electrically connected."). EX1002, ¶¶145–146.

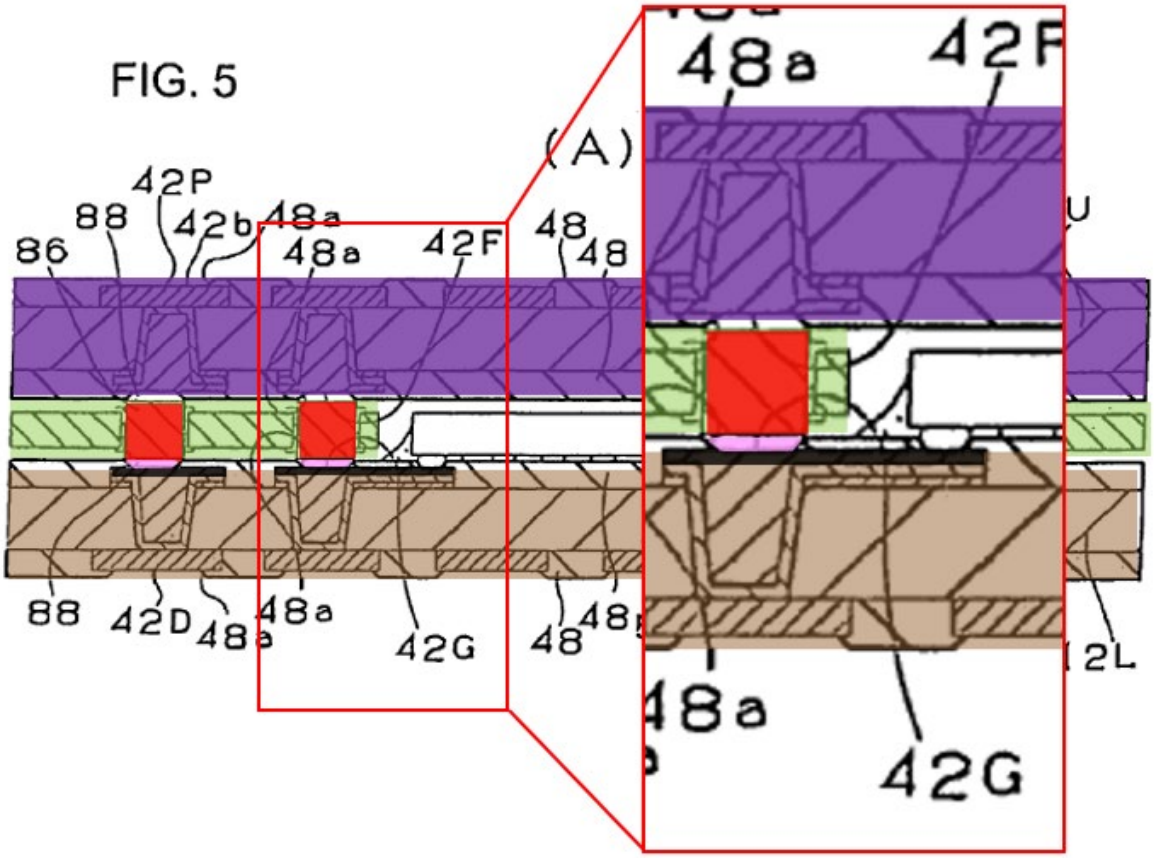
These **metal posts 86** protrude beyond the **insulative substrate 80**. *See* EX1006, [0037] ("The pierced implant material is inserted in openings 82 of **insulative substrate 80** prepared above, then pounded in. Accordingly, **conductive members (metal posts) 86** penetrating the **insulative substrate** are formed (FIG. 4(D)). Then, the implant material is separated and the height of **posts 86** protruding beyond **insulative substrate 80** is aligned. In doing so, **insulative substrate 80**, which is **interposer (12M)**, obtains **conductive members (posts) 86**, ***which enable electrical connection between the top and bottom***, and whose heights protruding beyond **insulative substrate 80** are substantially the same.").



EX1006, Figure 4D. EX1002, ¶147.

In making the "electrical connection between the **top** and **bottom**" substrates, Furuta teaches using **adhesive agent 88** that may be a "**solder or the like**" directly to **pads (42G)** on the top surface of the **lower substrate (12L)**, without the use of a corresponding **metal pad** on the bottom of **metal posts 86**. *See* EX1006, [0038] ("**Circuit (pads) (42G)** of **lower substrate (12L)**, **posts 86** of **interposer (12M)** and circuit (pads) (42F) of upper substrate (12U) are aligned (FIG. 5(A)). Here, **circuit portions (42G)** of **lower substrate (12L)** come in contact with **posts 86** of

interposer (12M); … . **Posts 86** of **interposer (12M)** and **conductive layers** (**42G**, 42F) of each substrate may be connected using **solder or the like as conductive adhesive agent 88**.”).



EX1006, Figure 5A. EX1002, ¶148.

Furuta’s **circuit pads 42G** are just like Chen’s **unlabeled pads** formed on the **bottom package component 56** that electrically couple to **connectors 44**.

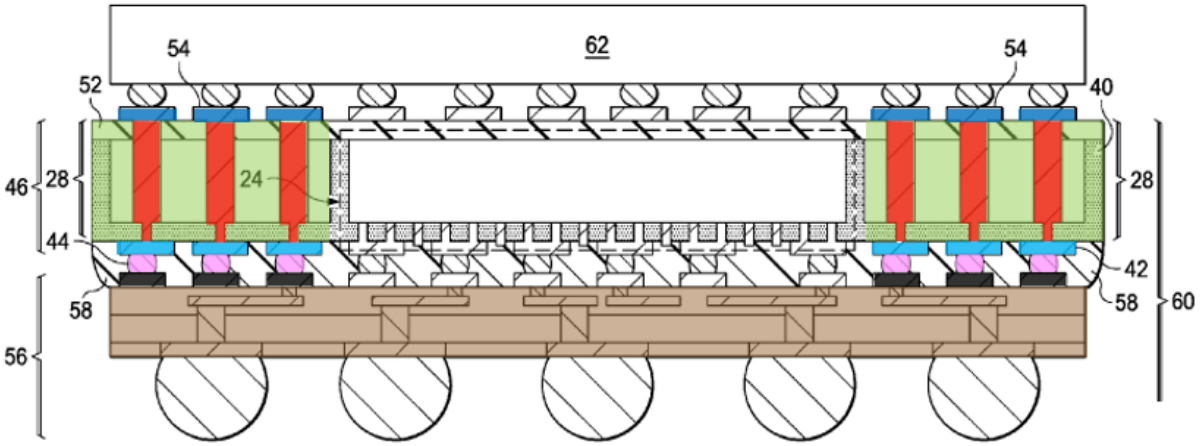


FIG. 9

EX1003, Figure 9. EX1002, ¶148.

A POSITA would have been motivated to remove the **RDLs 42** in Chen because Furuta teaches the desirability of making such direct electrical connections between **metal posts** and **connectors 44** because the **metal posts** can be uniformly manufactured with smaller pitch sizes, is less prone to uneven heating problems, and can be utilize to control the height between the upper substrate (12U) and lower substrate (12L) more precisely and reliably. *See* EX1006, [0023] ("Accordingly, it is possible to obtain connection through **posts 86** with a smaller diameter than solder bumps, and thus wiring may be arranged with a **fine pitch**. Also, since **uniformly manufactured posts 86** are used, unlike solder bumps of varying sizes, **heat is generated uniformly, thus high temperatures in spots may seldom be generated**. Moreover, since **interposer (12M)** lies in between, the height between **upper**

substrate (12U) and **lower substrate (12L)** may be adjusted, **making it easier to secure electrical connectivity and reliability**."). EX1002, ¶149.

Hence, it would have been obvious to modify Chen with Sun and Furuta to arrive at a structure that appears as shown below, in which each **through substrate vias 32**, **metal posts 30**, and the corresponding **RDLs 54** of the **TAV modules 28** form a T shape.

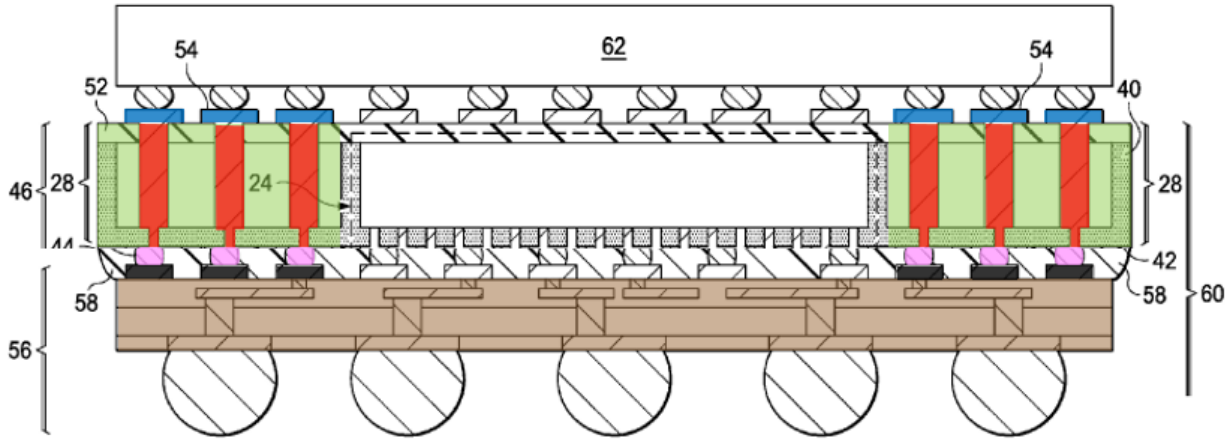


FIG. 9

EX1003, Figure 9 (as modified with Sun and Furuta). At a minimum, a POSITA would have found it obvious to try to removing **RDLs 42** that were present on the bottom of the **TAV modules 28** because the **metal posts 30** of Chen are significantly thinner than the **through substrate vias 32**, necessitating methods to further improve on the manufacturability and reliability, which Furuta teaches can be achieved by making a direct connection from **metal posts 30** to **connectors 44**.

Accordingly, a POSITA would have been able to readily make the modification with a reasonable expectation of success. EX1002, ¶¶150–151.

2. Dependent Claim 6

a) [6Pre] The structure of claim 4, wherein

See Section VIII.A.4 [Ground I, claim 4]. EX1002, ¶152.

b) [6A] the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Chen, Sun, and Furuta render obvious [6A] for at least the reasons stated in [5A] and [1H]. *See* Sections VIII.B.1.b) [Ground II, [5A]] and VIII.A.1.i) [Ground I, [1H]]. Hence, it would have been obvious to modify Chen with Sun and Furuta to arrive at a structure that appears as shown below.

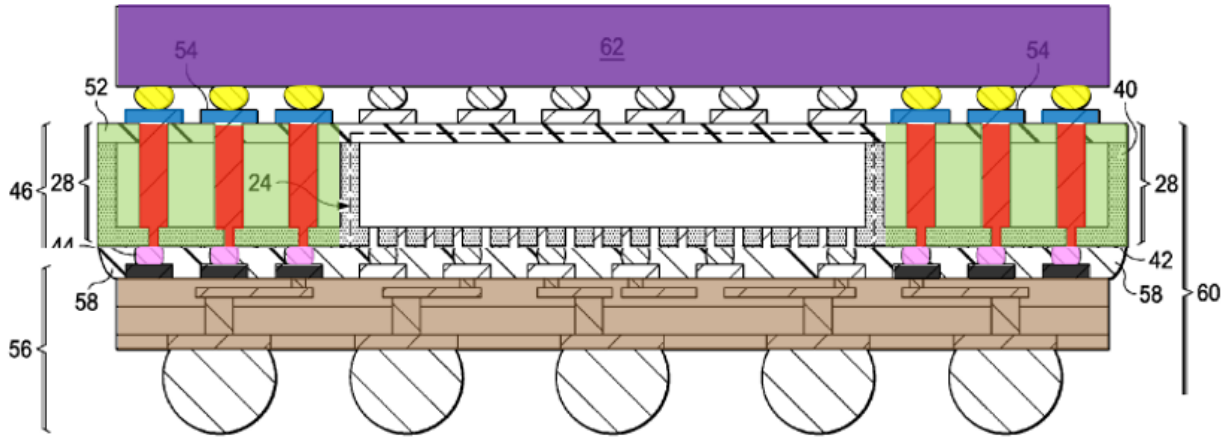


FIG. 9

EX1003, Figure 9 (as modified with Sun and Furuta). EX1002, ¶153.

C. Ground III: Claims 1–4 and 7–9 Are Rendered Obvious By Chen In View Of Wu

1. Independent Claim 1

a) [1Pre] A structure, comprising:

Chen discloses [1Pre]. *See* Section VIII.A.1.a) [Ground I, [1Pre]]. EX1002, ¶154.

b) [1A] a bottom package substrate;

Chen discloses [1A]. *See* Section VIII.A.1.b) [Ground I, [1A]]. EX1002, ¶155.

c) [1B] a top package substrate stacked on top of the bottom package substrate;

Chen discloses [1B]. *See* Section VIII.A.1.c) [Ground I, [1B]]. EX1002, ¶156.

d) [1C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate,

Chen discloses [1C]. *See* Section VIII.A.1.d) [Ground I, [1C]]. EX1002, ¶157.

e) [1D] wherein the spacer connector comprises a core substrate;

Chen discloses [1D]. *See* Section VIII.A.1.e) [Ground I, [1D]]. EX1002, ¶158.

f) [1E] a plurality of metal pillars, each passing through the core substrate;

Chen discloses [1E]. *See* Section VIII.A.1.f) [Ground I, [1E]]. EX1002, ¶159.

g) [1F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;

Chen discloses, or at least renders obvious, [1F]. *See* Section VIII.A.1.g) [Ground I, [1F]]. EX1002, ¶¶160–161.

h) [1G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate;

Chen discloses [1G]. *See* Section VIII.A.1.h) [Ground I, [1G]]. EX1002, ¶162.

i) [1H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,

Chen and Wu render obvious [1H]. First, as explained above in Ground I [1H], Chen discloses **package component 62** and **package component 56** that are **electrically coupled** to each other by (from top to bottom) unlabeled **connectors**[7] (that appear nearly identical to connectors 44 on the opposite side of the TAV modules 28), **RDLs 54**, **through-substrate vias 32**, **metal posts 30**, **RDLs 42**, and connectors 44. *See* EX1003, [0019], [0014], [0017], claim 1, claim 15; *see also* Section VIII.A.1.i) [Ground I, [1H]].

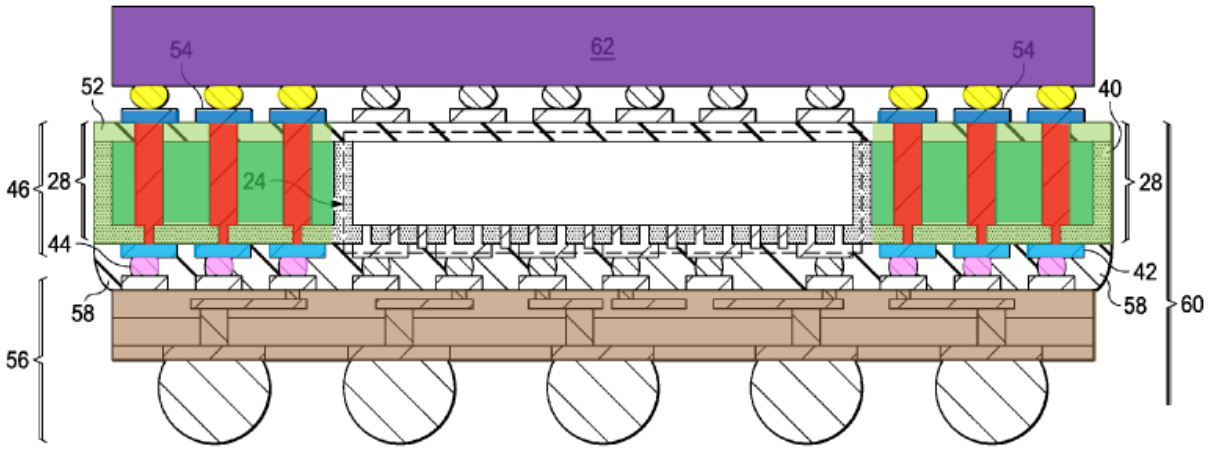


FIG. 9

[7] Petitioner specifically relies on the six unlabeled **connectors** colored in Figure 9 of Chen below as rendering obvious the claimed "**plurality of bottom metal pillars**."

EX1003, Figure 9. EX1002, ¶¶163–164.

Chen discloses that "**[c]onnectors 44** may also include **metal pillars**, or **metal pillars** and solder caps." EX1003, [0014]. Chen does not explicitly state that the unlabeled **connectors**—that appear nearly identical to **connectors 44** on the opposite side of the **TAV modules 28**—are metal. But like **connectors 44**, a POSITA would have readily recognized that it would have been obvious to utilize **metal pillars** as the unlabeled **connectors**. EX1002, ¶165.

Wu, like the '202 Patent, is directed to a package-on-package structure.[8] *See, e.g.,* EX1005, Title ("Package-on-package structure with organic interposer."), [0005] ("FIGS. 1 through 7 are cross-sectional views illustrating intermediate steps of a process for forming package-on-package structures"); EX1001, claim 1. Moreover, Wu, like Chen, describes a structure used to stack two packages on top

[8] Wu is therefore analogous art for this reason alone because Wu is in the same field of endeavor as the '202 Patent. Independently, Wu is analogous art because a POSITA would have also found Wu to be reasonably pertinent to the '202 Patent because it deals with the same problem of electrically coupling a top package substrate to a bottom package substrate through the use of an interposer. *See* EX1001, claim 1 ("the top package substrate is electrically coupled to the bottom package substrate through… the spacer connector…"). EX1002, ¶166.

of each other using an **interposer 402** and teaches that **vias 410** in the **interposer 402** were well-known to be coupled to **package connectors 704** formed on **package 702**. For example, in Figure 7, the top **package 702** (having **package substrate 706**) is mounted onto the **interposer 402** by way of **package connectors 704**. *See* EX1005, [0030] ("FIG. 7 is a cross-sectional view illustrating mounting a **package 702** on the **interposer 402** according to some embodiments. … The **connectors 704** electrically connect the lands 412 on the top surface of the **interposer 402** to the lands 716 on the bottom surface of the **package 702**."), [0021] ("In an interposer first process, an **interposer 402** is initially provided and mounted over the substrate 110 by attaching **pillars 416** on the **interposer 402** to the **pillars 202** on the **substrate 110**. The **interposer 402** has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. **Vias 410** in the **interposer substrate 408** connect the bottom RDL 406 to the top RDL 404.").

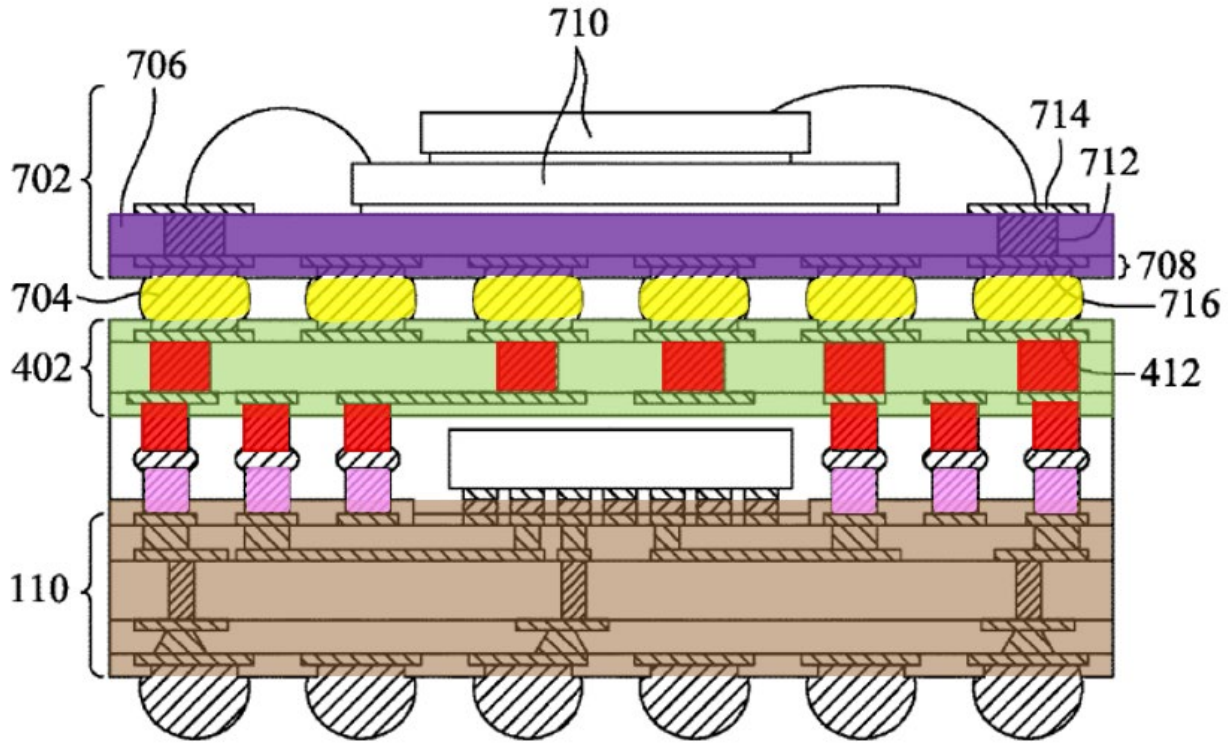


Fig. 7

EX1005, Figure 7. EX1002, ¶166–167.

Wu explains that **connectors 704** can be pillars and that pillars can be made of **metal**. *See* EX1005, [0030] ("**Package connectors 704** such as, for example, solder balls, **pillars**, studs, conductive bumps, or the like bond the package 702 to the interposer 402."), [0017] ("In some embodiments, the **pillars** 202 are formed by initially depositing a seed layer over the lands 106. … A mask layer is formed over the seed layer … . A **metal layer** is formed over the patterned mask layer … the **deposited metal layer** is planarized … . The planarization step removes excess

deposited metal from over the patterned mask layer, leaving **pillars** 202."). EX1002, ¶168.

Wu further explains that **connector 704** is part of the **package 702** (having **package substrate 706**). *See* EX1005, [0031] ("While the **package 702** is illustrated herein as having a substrate 706 with dies 710 disposed thereon, the structure is not limited to having such a **package 702** with such an arrangement. In other embodiments, the **package 702** is a die or chip ***mounted directly on the connectors 704***, ***multiple dies or packages on the connectors 704*** or another arrangement."). EX1002, ¶169.

The fabrication steps, described in Figures 5 through 7 of Wu, make this clear. As shown below, Figure 5 shows a stage of assembly in which **interposer 402** has been mounted on the **substrate 110** and moldable underfill (MUF) 502 has been applied. *See* EX1005, [0021] ("FIG. 4 is a cross-sectional view illustrating mounting an **interposer 402** on the **substrate 110** according to some embodiments."), [0028] ("FIG. 5 is a cross-sectional view illustrating application of a moldable underfill (MUF) 502 according to some embodiments.").

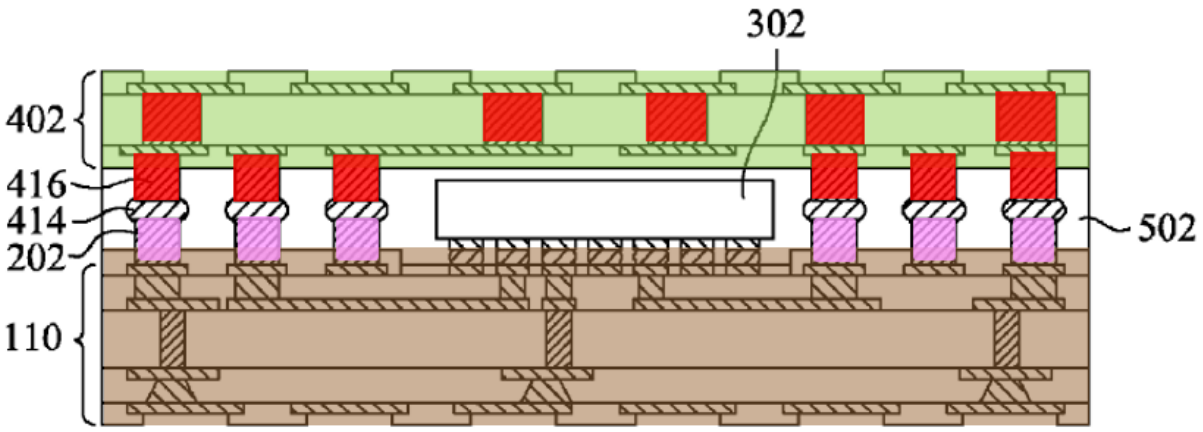


Fig. 5

EX1005, Figure 5. EX1002, ¶170.

Figure 6 then shows the addition of **connector 602 (see blue arrow)** to the bottom of the **substrate 110**, but ***not*** to the top surface of **interposer 402**. *See* EX1005, [0029] ("FIG. 6 is a cross-sectional view illustrating mounting **connectors 602** on the **substrate 110** according to some embodiments. **Connectors 602**, such as, for example, solder balls, are mounted on the lands 114. In other embodiments, the **connectors 602** are conductive bumps, pillars, studs, or another conductive structure.").

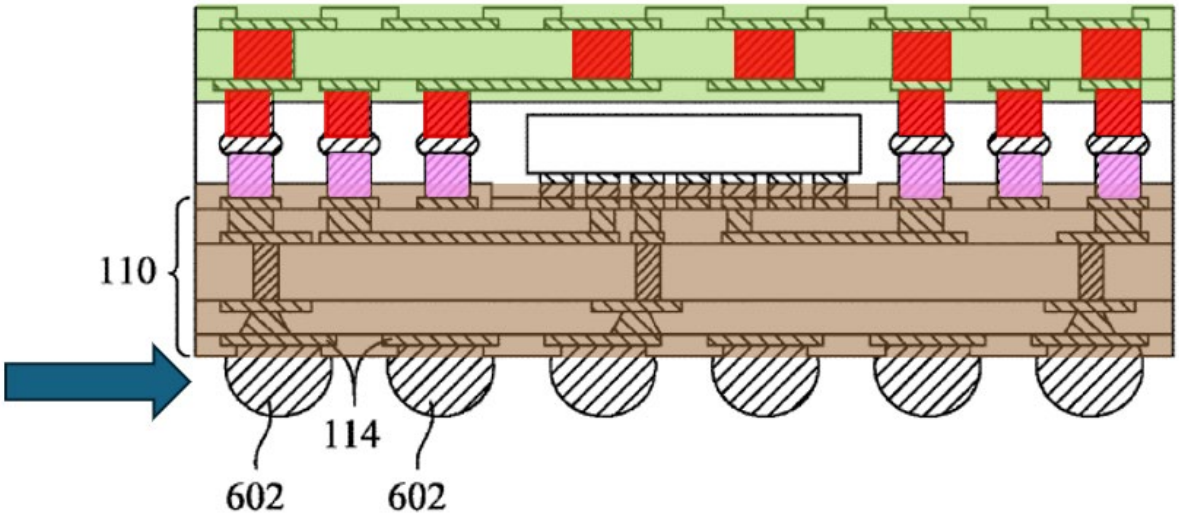


Fig. 6

EX1005, Figure 6. EX1002, ¶171.

Finally, the structure shown in Figure 7 is obtained.

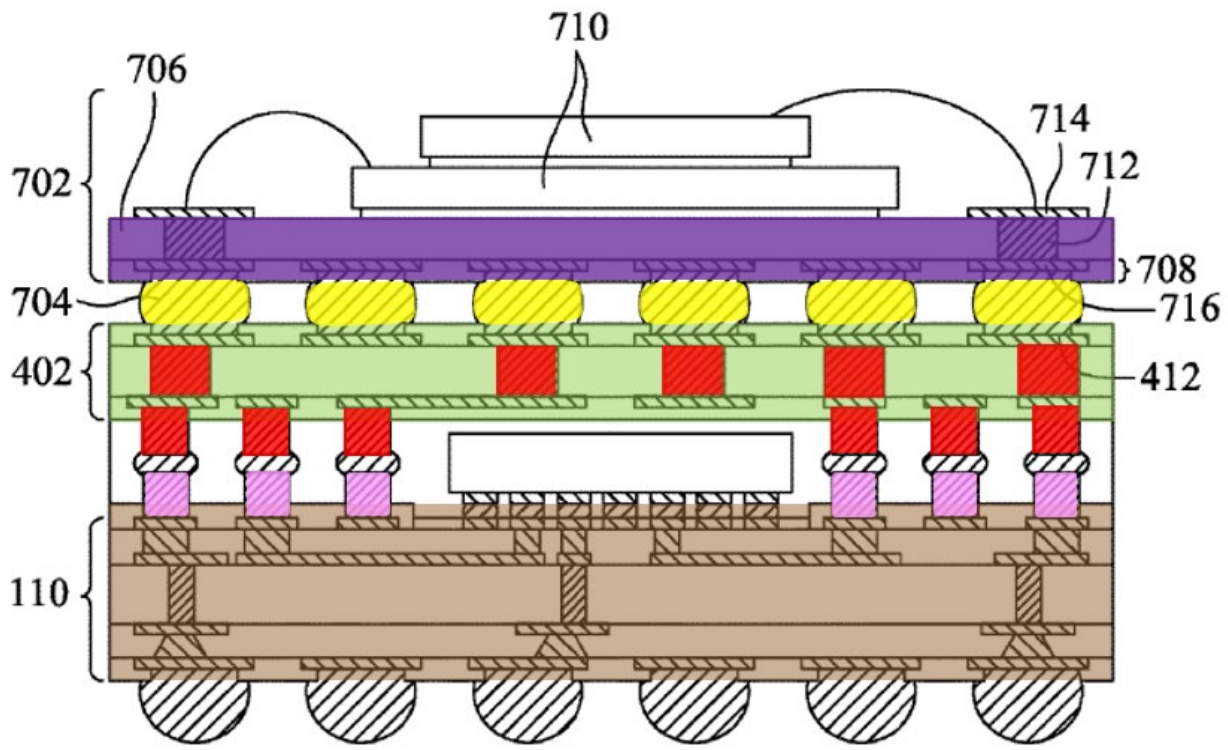


Fig. 7

EX1005, Figure 7. EX1002, ¶172.

It would have been obvious to combine Chen with Wu to place **metal pillars** on the bottom surface of the **top package component 62** for electrical coupling to Chen's **TAV modules 28**. First, a POSITA would have found it obvious to utilize **metal pillars** as suitable connectors between **TAV modules 28** to the **top package component 62** because Wu teaches it is merely one well-known methods to electrically couple one substrate to another. The modification amounts to nothing more than simple substitution of one well-known connector (i.e., **metal pillars** of

Wu) instead of the unlabeled **connector** shown in Chen that would have led to the predictable result of electrically coupled substrates. EX1002, ¶¶173–174.

Moreover, placing such **metal pillars** on the **top package component 62** for electrical coupling to the **TAV modules 28** is a routine design choice that would have been obvious to a POSA. For example, as more fully explained in [1I] below, Wu describes placing **pillars 202** on a **bottom substrate 110** for electrical coupling to **interposer 402**. Section VIII.C.1.j) [Ground III, [1I]]. Placing **metal pillars** on **top package component 62** to electrically couple those **pillars** to the **TAV modules 28** amounts to nothing more than combining prior art elements (**metal pillars**) according to known methods (placing **metal pillars** onto **top package component 62**) to yield predictable results (structure having **TAV modules 28** electrically coupled to **top package component 62**). And a POSITA would have been able to make such a modification with a reasonable expectation of success because it would be a simple substitution of two known elements. EX1002, ¶175.

j) [1I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,

Chen discloses [1I] for at least the reasons stated in Ground I, [1I]. *See* Section VIII.A.1.j) [Ground I, [1I]]. EX1002, ¶176.

Alternatively, Chen and Wu render obvious [1I]. Wu, like Chen, describes a structure used to stack two packages (i.e., **package 702** and **substrate 110**) on top of each other using an **interposer 402** and teaches that **pillars 416** of the **interposer 402** are coupled to **pillars 202** that have already been formed on the **substrate 110**.

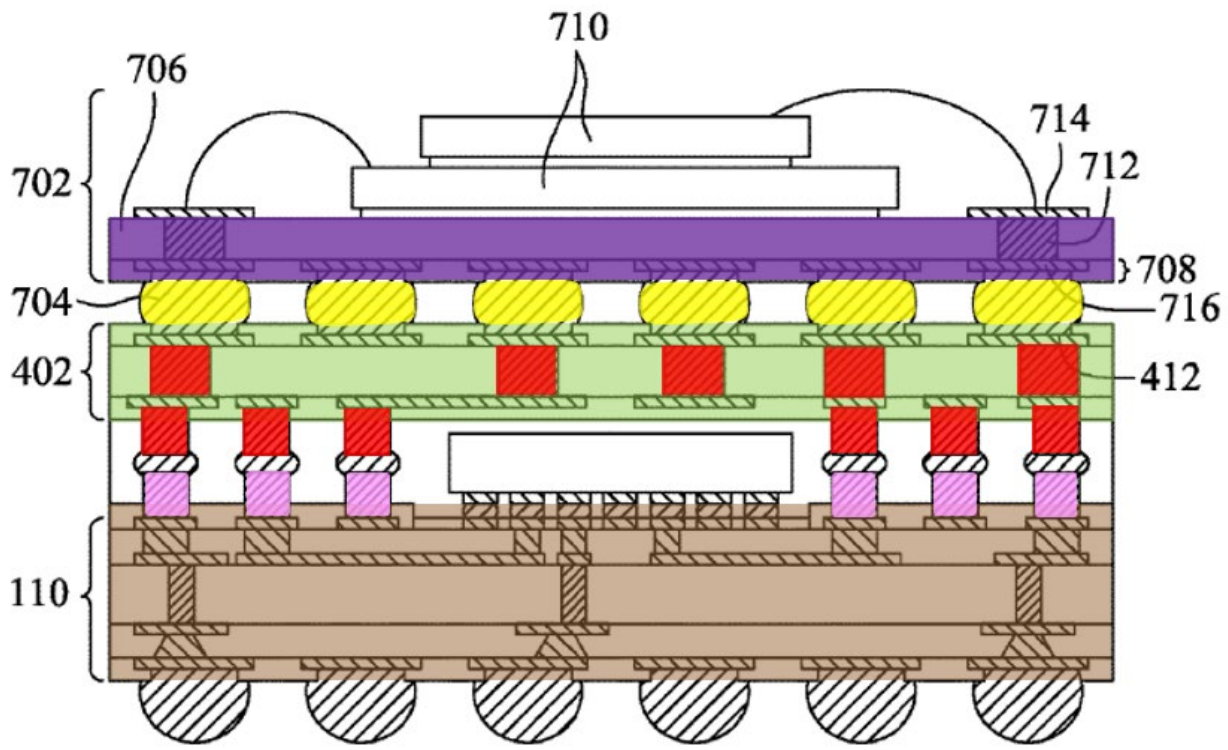


Fig. 7

EX1005, Figure 7. EX1002, ¶177.

For example, Figures 2 through 4 show three intermediate steps of assembly for Wu's package-on-package structure. As shown, Figure 2 shows the addition of **pillars 202** to the top surface of **substrate 110**. EX1005, [0017] ("FIG. 2 is a cross-

sectional view illustrating formation of **pillars 202** on the **substrate 110** according to some embodiments.”).

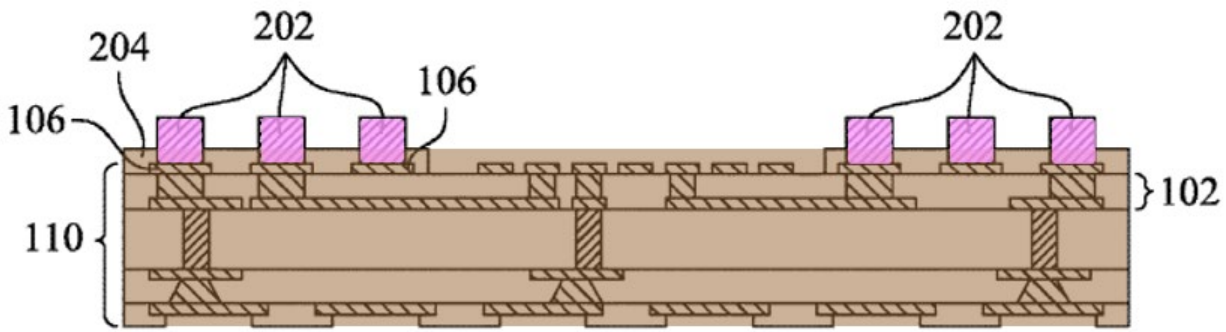


Fig. 2

EX1005, Figure 2. EX1002, ¶178.

Then, in FIG. 4, the **interposer 402** is mounted to the **substrate 110** by way of **pillars 202** that have already been formed on **substrate 110**. EX1005, [0021] (“FIG. 4 is a cross-sectional view illustrating mounting an **interposer 402** on the **substrate 110** according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the **pillars 202** **on the** **substrate 110**.”), [0027] (“The **interposer 402** is mounted to the **substrate 110** by aligning the **pillars 416** over the **pillars 202** and bonding the aligned pairs of **pillars 202** and **416** to each other.”).

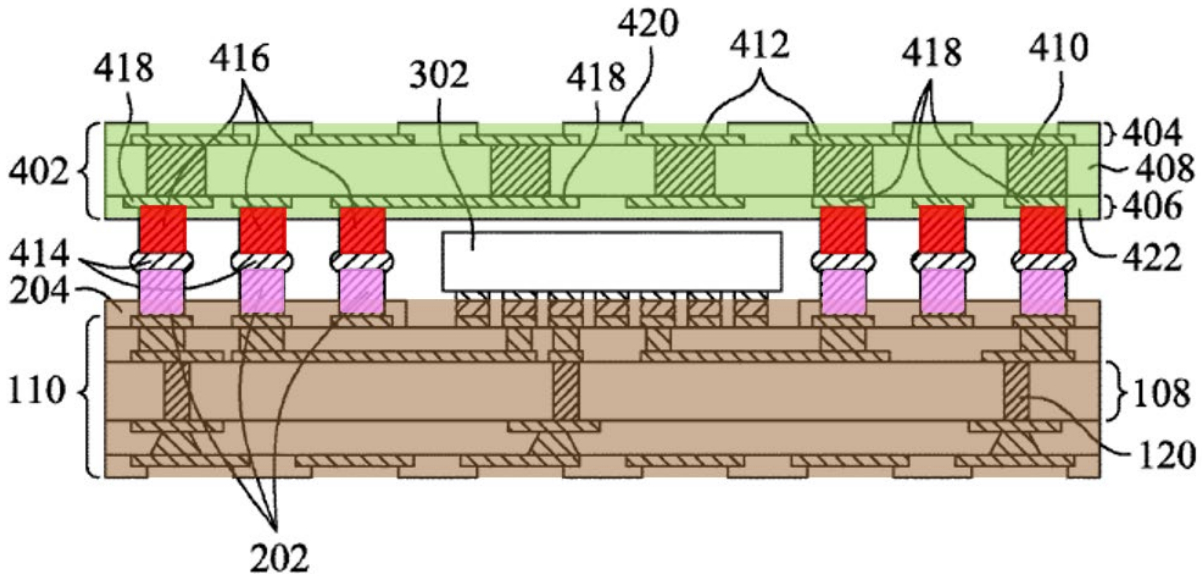


Fig. 4

EX1005, Figure 4. EX1002, ¶179.

Wu further explains that **pillars 202** are made of **metal**. *See* EX1005, [0017] ("In some embodiments, the **pillars 202** are formed by initially depositing a seed layer over the lands 106. … A mask layer is formed over the seed layer … . A **metal layer** is formed over the patterned mask layer … the **deposited metal layer** is planarized … . The planarization step removes excess deposited metal from over the patterned mask layer, leaving **pillars 202**."). EX1002, ¶180.

It would have been obvious to combine Chen with Wu to place **metal pillars** onto the **bottom package component 56** for electrical coupling to **TAV modules 28**. Placing **metal pillars** on **bottom package component 56** for electrical coupling to **TAV modules 28** amounts to nothing more than combining prior art elements

(**metal pillars**) according to known methods (placing **metal pillars** onto **bottom package component 56**) to yield predictable results (device that has **TAV modules 28** electrically coupled to **bottom package component 56**). And a POSITA would have been able to make such a modification with a reasonable expectation of success because it would be a simple substitution of two known elements. EX1002, ¶181.

k) [1J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and

Chen and Wu render obvious [1J] for at least the reasons explained in [1H]. *See* Section VIII.C.1.i) [Ground III, [1H]. EX1002, ¶182.

l) [1K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate,

Chen discloses [1K]. *See* Section VIII.A.1.l) [Ground I, [1K]]. EX1002, ¶183.

m) [1L] wherein the bottom chip is mounted to the top surface of the bottom package substrate,

Chen discloses [1L]. *See* Section VIII.A.1.m) [Ground I, [1L]]. EX1002, ¶184.

n) [1M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

Chen discloses [1M]. *See* Section VIII.A.1.n) [Ground I, [1M]]. EX1002, ¶186.

2. Dependent Claim 2

a) [2Pre] The structure of claim 1, wherein

See Section VIII.C.1 [Ground III, claim 1]. EX1002, ¶186.

b) [2A] a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

Chen discloses [2A]. *See* Section VIII.A.2.b) [Ground I, [2A]]. EX1002, ¶187.

3. Dependent Claim 3

a) [3Pre] The structure of claim 2, further comprising:

See Section VIII.C.2 [Ground III, claim 2]. EX1002, ¶188.

b) [3A] a top chip mounted to the top surface of the top package substrate,

Chen and Wu render obvious [3A]. First, Chen discloses **a device die (not shown)** mounted to (i.e., bonded to) the top surface of the **package substrate (not shown)** of **package component 62**. *See* EX1003, [0019] ("Alternatively, **package component 62** is a package that includes a **device die (not shown)** bonded to a **package substrate (not shown)**, an interposer (not shown), or the like.").

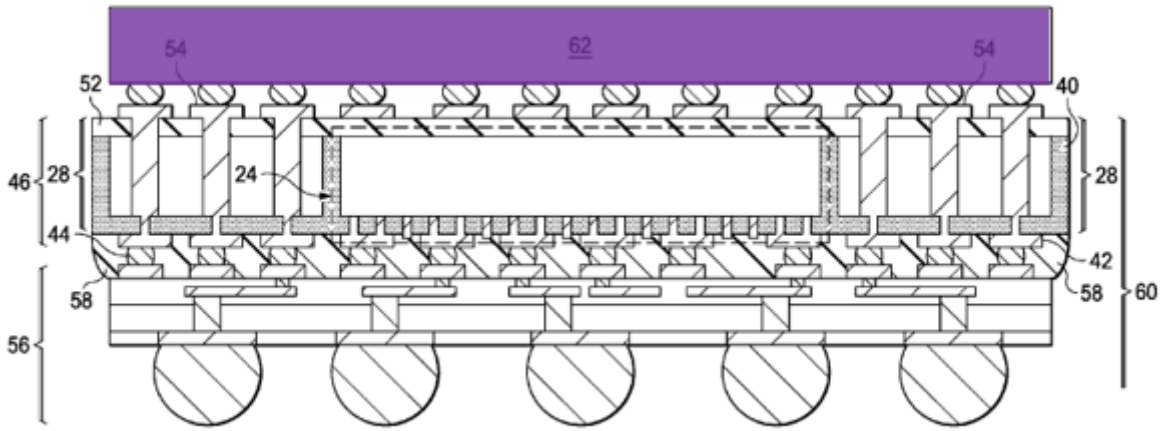


FIG. 9

EX1003, Figure 9. EX1002, ¶¶189–190.

Although Chen does not explicitly disclose whether the **device die (not shown)** is bonded to the ***top surface*** of the **package substrate (not shown)**, such a configuration was well-known. As explained in [1H], Wu, like Chen, describes a structure having a **substrate 110** electrically coupled to a **package substrate 706** via an intermediate **interposer 300**. *See* Section VIII.A.1.i) [Ground I, [1H]].

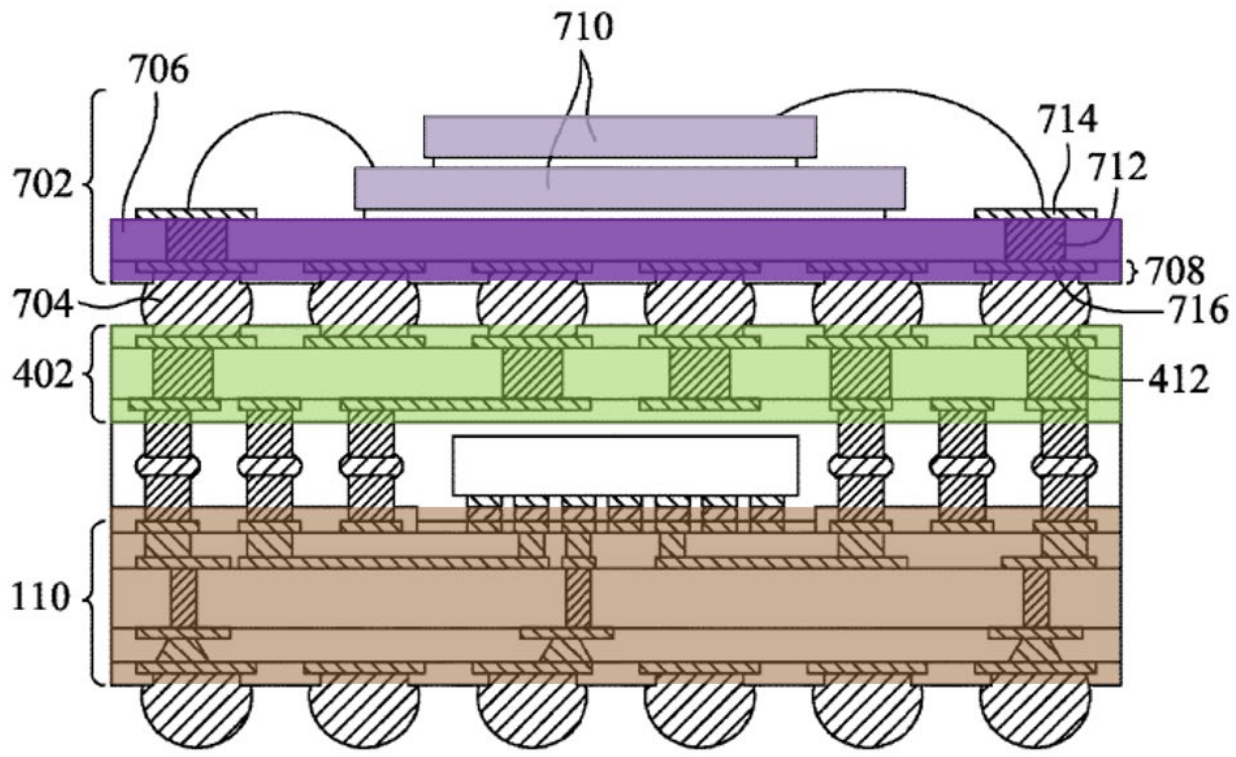


Fig. 7

EX1005, Figure 7. As shown above, **dies 710** are mounted to the top surface of the **package substrate 706**. *See* EX1005, [0030] ("In some embodiments, the **package 702** has **one or more dies 710** electrically connected to conductive features 714 that are in turn electrically connected to the lands 716 by way of vias 712 disposed in a **package substrate 706**."). EX1002, ¶191.

A POSITA would have been able to make the modification with a reasonable expectation of success. Chen already teaches that "**package component 62** is a package that includes a **device die (not shown)** bonded to a **package substrate (not**

shown)." EX1003, [0019]. It would have been obvious for a POSITA to place Chen's **device die (not shown)** or Wu's **dies 710** on Chen's **package substrate (not shown)** in the manner shown in Figure 7 of Wu with a reasonable expectation of success because it merely provides one particular configuration of mounting **device die(s)** on a Chen's **package substrate (not shown)**. Mounting Chen's **device die (not shown)** or Wu's **dies 710** on the top surface of Chen's **package substrate (not shown)** merely amounts to combining known prior art elements (Chen's **device die (not shown)** or Wu's **dies 710** with Chen's **package substrate (not shown)**) according to known methods (by placing Chen's **device die (not shown)** or Wu's **dies 710** on a readily available top surface of Chen's **package substrate (not shown)**) to yield the predictable results of a **die/chip** sitting on the top surface of a **package substrate** for electrical coupling to another chip on another substrate. At a minimum, it would have been obvious to try from the finite number of possible places for mounting the dies (either the top or bottom surface of the package substrate because a POSITA would have readily recognized that mounting to the side surfaces of the package substrate would not be an efficient approach) that a POSITA would have reasonably expected to have succeeded. EX1002, ¶¶192–193.

c) [3B] wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

Chen and Wu render obvious [3B]. As shown below in Figure 7 of Wu, two **dies 710** mounted on **package substrate 706**. The **lower die 710**, relative to the **upper die 710** and **die 110** on the **bottom substrate 110**, is larger such that the **lower die 710** extends over the **pillars 416** that are adjacent to the **die 302**. *See Regents of the Univ. of Cal. v. Satco Prods., Inc.,* No. 2023-1356, 2024 WL 7311186 (Fed. Cir. Dec. 4, 2024) ("[P]atent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their spatial relations to one another.").

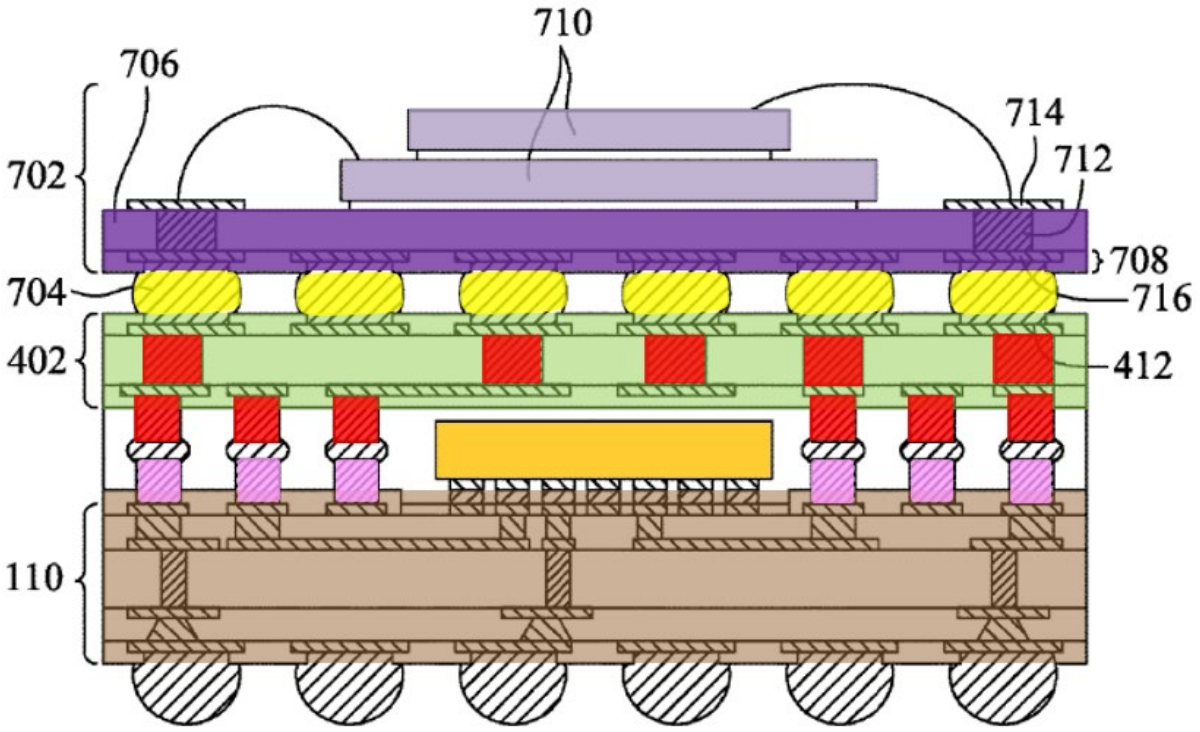


Fig. 7

EX1005, Figure 7. EX1002, ¶¶194–195.

Chen similarly teaches that the **package component 62** depicted in Figure 9 itself can be a **device die** that is over the **package component 24** and the **TAV modules 28**. *See* EX1003, [0019] ("In some embodiments, **top package component 62** is a **device die**. Alternatively, **package component 62** is a package that includes a **device die (not shown)** bonded to a **package substrate (not shown)**, an interposer (not shown), or the like."). EX1003, [0020] ("FIG. 10 illustrates an exemplary embodiment wherein **package component 62** includes a plurality of

stacked dies 64. … Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to **package component 24**, which are further connected to the RDLs 54 over and aligned to **TAV modules 28**.”), [0014], [0018].

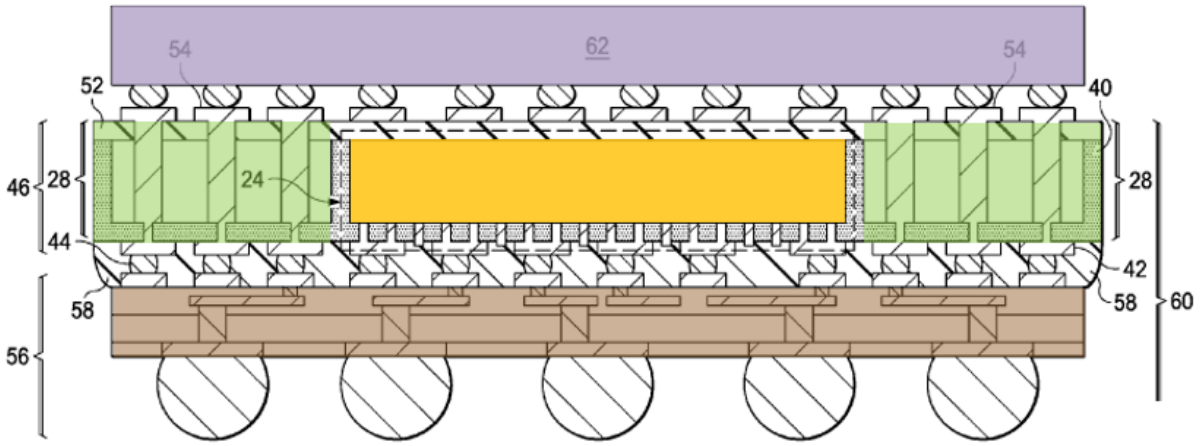


FIG. 9

EX1003, Figure 9. EX1002, ¶195.

It would have been obvious to replace with a reasonable expectation of success Chen’s **device die (not shown)** in Chen’s **package component 62** with Wu’s **dies 710** to obtain a configuration shown below, such that the **die 710** overlaps the **package component 24** and each of the two **TAV modules 28** (*i.e.,* over the **through-substrate vias 32** that are adjacent to the **package component 24**) in a direction in which the **package component 702** is stacked on top of the **bottom package component 56**.

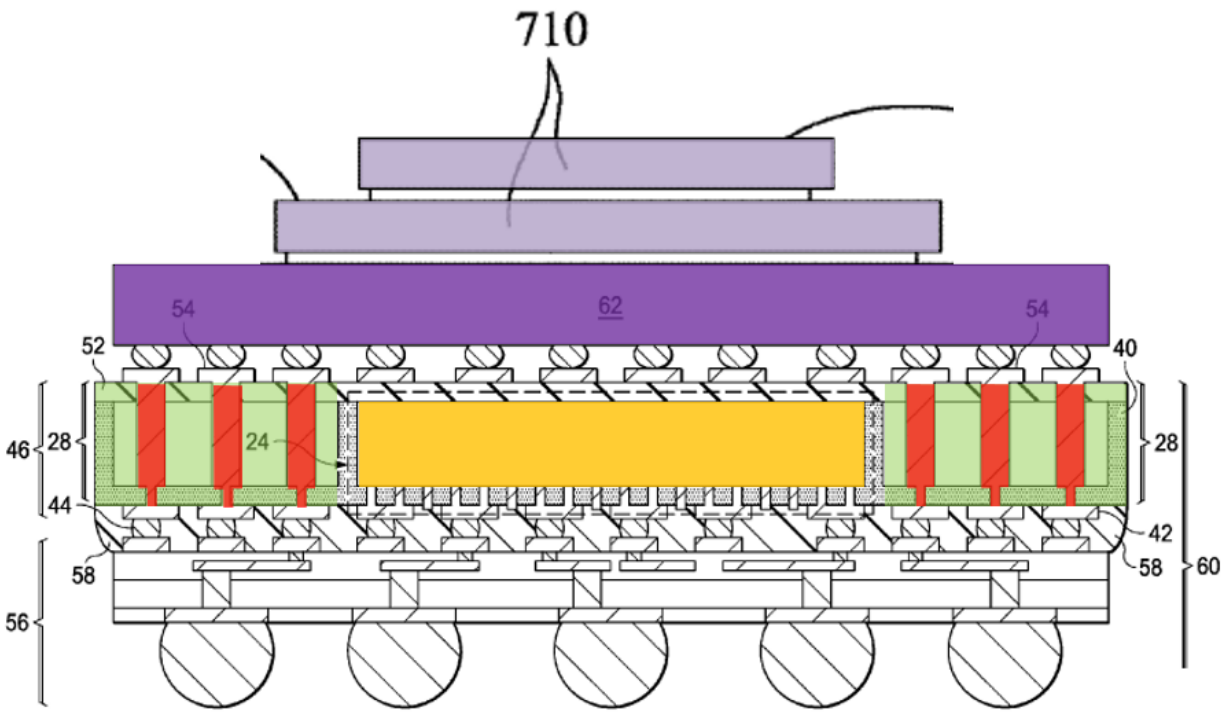


FIG. 9

EX1003, Figure 9 (as modified with Wu). *See also* Section VIII.C.3.b) [Ground III, [3A]]. EX1002, ¶196.

4. Dependent Claim 4

a) [4Pre] The structure of claim 1, wherein

See Section VIII.C.1 [Ground III, claim 1]. EX1002, ¶197.

b) [4A] each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

Chen and Wu render obvious [4A] for at least the reasons discussed in [1H] and [1I]. *See* Sections VIII.C.1.i) [Ground III, [1H]] and VIII.C.1.j) [Ground III, [1I]].

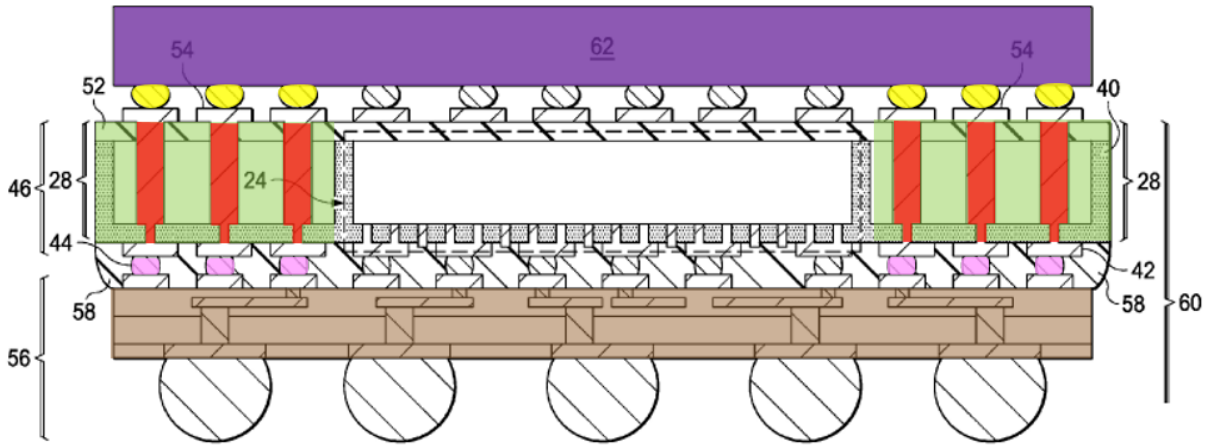


FIG. 9

EX1003, Figure 9. EX1002, ¶198.

5. Dependent Claim 7

a) [7Pre] The structure of claim 4, wherein

See Section VIII.C.4 [Ground III, claim 4]. EX1002, ¶199.

b) [7A] the spacer connector further comprises a dielectric layer on the bottom surface of the core substrate, and

Chen discloses [7A]. *See* Section VIII.A.5.b) [Ground I, [7A]]. EX1002, ¶200.

c) [7B] the plurality of metal pillars pass through the core substrate and the dielectric layer.

Chen discloses [7B]. *See* Section VIII.A.5.c) [Ground I, [7B]]. EX1002, ¶201.

6. Dependent Claim 8

a) [8Pre] The structure of claim 7, wherein

See Section VIII.C.5 [Ground III, claim 7]. EX1002, ¶202.

b) [8A] the dielectric layer is a dielectric adhesive in which the core substrate is pasted.

Chen discloses [8A]. *See* Section VIII.A.6.b) [Ground I, [8A]]. EX1002, ¶203.

7. Dependent Claim 9

a) [9Pre] The structure of claim 4, wherein

See Section VIII.C.4 [Ground III, claim 4]. EX1002, ¶204.

b) [9A] the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars,

Chen discloses [9A]. *See* Section VIII.A.7.b) [Ground I, [9A]]. EX1002, ¶205.

c) [9B] the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and

Chen discloses [9B]. *See* Section VIII.A.7.c) [Ground I, [9B]]. EX1002, ¶206.

d) [9C] bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Chen and Wu render obvious [9C] for at least the reasons described in [1F] and [1H]. *See* Sections VIII.C.1.g) [Ground III, [1F]] and VIII.C.1.i) [Ground III, [1H]].

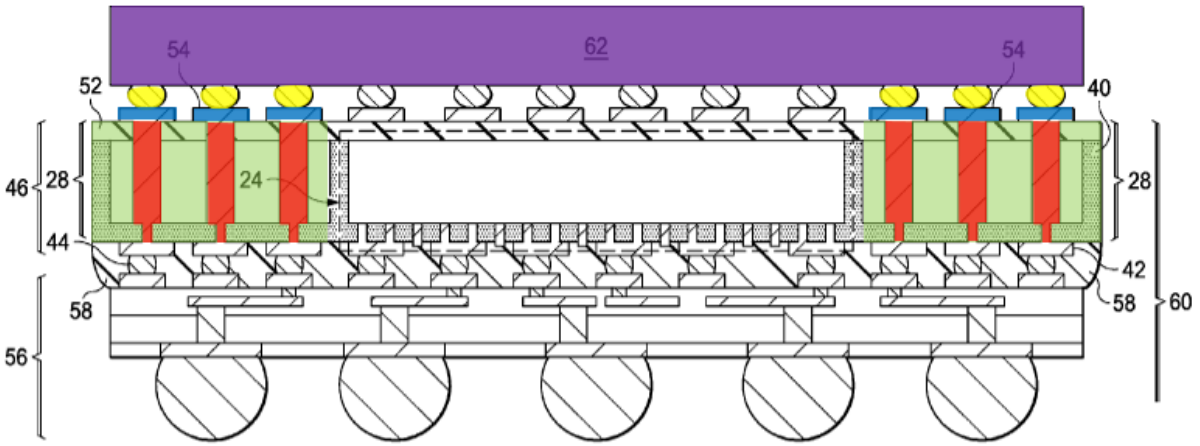


FIG. 9

EX1003, Figure 9. EX1002, ¶207.

D. Ground IV: Claims 5–6 Are Rendered Obvious By Chen In View Of Wu And Furuta

1. Dependent Claim 5

a) [5Pre] The structure of claim 4, wherein

See Section VIII.C.4 [Ground III, claim 4]. EX1002, ¶208.

b) [5A] the spacer connector is free of metal pads on the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate, and each metal pillar among the plurality of metal pillars and the corresponding top metal pad of the spacer connector form a T shape.

Chen, Wu, and Furuta render obvious [5A] for at least the reasons stated in Ground II, [5A]. *See* Section VIII.D.1.b) [Ground II, [5A]]. Specifically, the proposed modifications discussed in Ground II, [5A] based on Furuta apply equally well to the teachings of Chen and Wu. And a POSITA would have found it obvious

to remove **RDLs 42** from the modified system based on the teachings of Chen in combination with Wu for the same reasons stated in Ground II, [5A]. EX1002, ¶¶209–210.

2. Dependent Claim 6

a) [6Pre] The structure of claim 4, wherein

See Section VIII.C.4 [Ground III, claim 4]. EX1002, ¶211.

b) [6A] the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Chen, Wu, and Furuta render obvious [6A] for at least the reasons stated in [5A] and [1H]. *See* Sections VIII.D.1.b) [Ground IV, [5A]] and VIII.C.1.i) [Ground III, [1H]]. Hence, it would have been obvious to modify Chen with Wu and Furuta to arrive at a structure that appears as shown below.

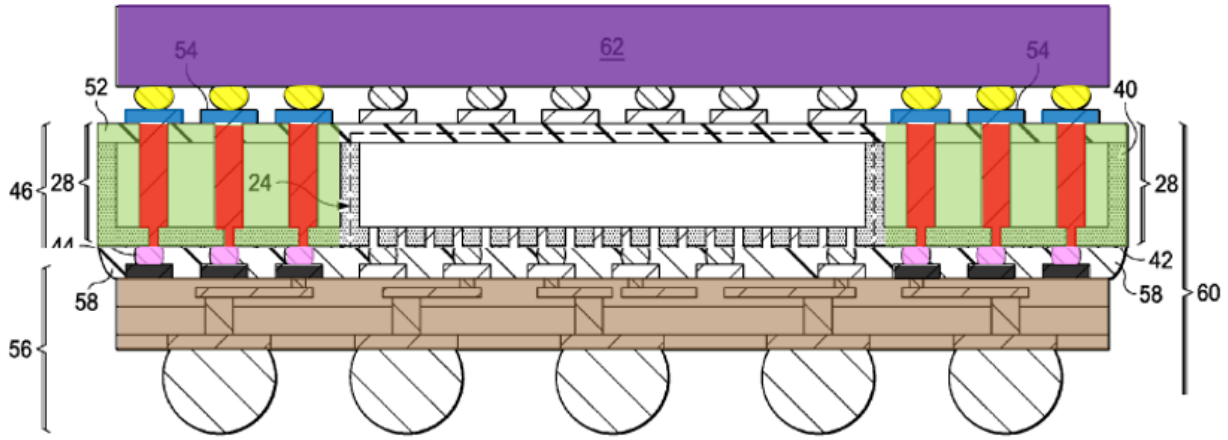


FIG. 9

EX1003, Figure 9 (as modified with Wu and Furuta). EX1002, ¶212.

IX. CONCLUSION

Petitioner respectfully requests that the Director institute *inter partes* review and the Board cancel the challenged claims.

Dated: March 16, 2026

Respectfully submitted,

/Yung-Hoon Ha/
Yung-Hoon Ha (Reg. No. 56,368)
yha@desmaraisllp.com
DESMARAIS LLP
230 Park Avenue
New York, NY 10169
212-351-3400 (telephone)
212-351-3401 (facsimile)

Lead Counsel for Petitioner

CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

I hereby certify that this Petition for *Inter Partes* Review of U.S. Patent No. 9,859,202 has, excluding the portions exempted under 37 C.F.R. § 42.24(a), 11,389 words as counted by the word-processing system used to prepare this document, in compliance with 37 C.F.R. § 42.24(d).

Dated: March 16, 2026

Respectfully submitted,

/Yung-Hoon Ha/
Yung-Hoon Ha (Reg. No. 56,368)
yha@desmaraisllp.com
DESMARAIS LLP
230 Park Avenue
New York, NY 10169
212-351-3400 (telephone)
212-351-3401 (facsimile)

Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

Under 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on March 16, 2026 complete copies of the foregoing and any accompanying exhibits were caused to be served by sending them via Federal Express Priority Overnight shipping, which is at least as fast and reliable as U.S. Priority Mail Express, to the correspondence address of record for U.S. Patent No. 9,859,202 as indicated in Patent Center:

JCIPRNET
8F-1, No. 100, Roosevelt Rd. Sec. 2,
Taipei, TAIWAN

Petitioner is also serving a courtesy copy to Patent Owner's litigation counsel of record at topwire_aza@azalaw.com.

Dated: March 16, 2026

Respectfully submitted,

/Yung-Hoon Ha/
Yung-Hoon Ha (Reg. No. 56,368)
yha@desmaraisllp.com
DESMARAIS LLP
230 Park Avenue
New York, NY 10169
212-351-3400 (telephone)
212-351-3401 (facsimile)

Lead Counsel for Petitioner