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Jefferson IP Law, LLP 1130 Connecticut Ave., NW, Suite 420 Washington, DC 20036			EXAMINER DINH, TUAN T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Objections

Claims 6, 15 are objected to because of the following informalities:

Regarding claims 6 and 15, each in line 2, please, change “an lower surface” to - a lower surface - - for proper reading.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, and 3-10 is/are rejected under 35 U.S.C. 103 as being unpatentable over Lim in view of Casto et al. (both references as in the record), and further in view of Asahi et al. (U.S. 2005/0184381)

As to claim 1, Lim discloses an electronic device (100) as shown in figures 4-7 comprising:

a first circuit board (210) having a first connection terminal (240) formed thereon;
a first electronic component (211) (electrically) connected to the first connection terminal (240) and disposed on the first circuit board;

an interposer (220) having first and second vias (225) formed therein and having a first surface attached to the first circuit board (210), the interposer at least partly surrounding at least a partial region of the first circuit board (see figure 7) and a first ending portion of the first via being electrically connected to the first connection terminal (240);

a second circuit board (230) having a second connection terminal (250) formed thereon and attached to a second surface of the interposer that is opposite to the first surface, the second connection terminal (250) being electrically connected to a second ending portion of the first via (225) and the second circuit board forming an inner space together with the first circuit board (210) and the interposer (220);

a second electronic component (231) electrically connected to the second connection terminal and disposed on the second circuit board; and

an antenna (116) electrically connected to the second electronic component (231), a plating member (323, see figures 8-9) formed on upper, lower, and side surfaces of the interposer (220).

Lim does not specifically disclose the first component which is an application processor, and the second component which is a communication processor.

Casto teaches system as shown in figures 1A-1C comprising the first and second electrical components (25) mounted on a stacked (10) of the second circuit board mounted on the first circuit board (22), the components are processors.

It would have been obvious to one having ordinary skill in the art before the effective filing date to have a teaching of Casto employed in the electronic device of Lim in order to perform the basic arithmetical, logical, and input/output operations of a computer system.

Lim and Casto do not specifically disclose a plating member including a first portion, a second portion and a third portion, the first portion attached to the first surface of the interposer, the second portion attached to the second surface of the interposer, and the third portion attached to a third surface of the interposer substantially perpendicular to the first surface and the second surface such that the third portion is extended over an entire height of the third surface, an ending portion of the first portion or an ending portion of the second portion connected to an ending portion of the second via.

Asahi teaches a connector member (100 or 200) as shown in figures 1-8 comprising a plating member (20) including a first portion (top portion, hereafter called TP), a second portion (bottom portion, BP) and a third portion (side portion formed on the side surface 10c, called SP), the first portion attached to the first surface of the interposer, the second portion attached to the second surface of the interposer, and the third portion attached to a third surface of the interposer substantially perpendicular to the first surface and the second surface such that the third portion is extended over an entire height of the third surface, an ending portion of the first portion or an ending portion of the second portion connected to an ending portion of the second via (or through holes 510, figures 3-8, the through hole or via connected to the first and second lands 20a, 20b), see para-0026+.

It would have been obvious to one having ordinary skill in the art before the effective filing date to have a teaching of Asahi employed in the electronic device of Lim and Casto in order to provide internal electrical connections.

Regarding claim 3, Lim as modified by Casto and Asahi teaches the plating member includes a first plating member, a second plating member and a third plating member.

Regarding claim 4, Lim as modified by Casto and Asahi teaches a portion of the first plating member and a portion of the second plating member are attached to an outer side of the third surface, and a portion of the third plating as shown in figure 8 is attached to an inner side of the third surface.

Regarding claim 5, Lim as modified by Casto and Asahi teaches the first plating member, the second plating member and the third plating member comprise a C shape.

As to claims 6-7, Lim as modified by Casto and Asahi discloses in figure 4 that a first shielding member (rear cover 102) is disposed on a lower surface of the first circuit board (210), and a second shielding member (rear cover 102) is disposed on an upper surface of the first circuit board (210).

As to claims 8-9, Lim as modified by Casto and Asahi discloses a first pad (not shown but the element 220 must or have to have the pad for solder to the element 240) electrically connected to the first connection terminal (240) of the first circuit board (210) is formed on a lower portion of the via (225), and wherein a second pad (not shown, same as the first pad) electrically connected to the second connection terminal (250) of the second circuit board (220) is formed on an upper portion of the via (225).

As to claim 10, Lim as modified by Casto and Asahi teaches the interposer (200) as shown in figure 6 that is separated through at least one slit.

As to claim 11, Lim as modified by Casto and Asahi discloses the interposer comprises a ground region (at the ground unit 232 or 323) surrounding at least a part of the first and second vias (225).

Claims 12-20 is/are rejected under 35 U.S.C. 103 as being unpatentable over Lim in view of Liao et al. (465), and further in view of Asahi et al. (U.S. 2005/0184381)

As to claim 12, Lim discloses an electronic device (100) as shown in figures 4-7 comprising:

- a first circuit board (210) having a first connection terminal (240) formed thereon;
- a first electronic component (211) (electrically) connected to the first connection terminal (240) and disposed on the first circuit board;

- an interposer (220) having first and second vias (225) formed therein and having a first surface attached to the first circuit board (210), the interposer at least partly surrounding at least a partial region of the first circuit board (see figure 7) and a first ending portion of the first via being electrically connected to the first connection terminal (240);

- a second circuit board (230) having a second connection terminal (250) formed thereon and attached to a second surface of the interposer that is opposite to the first surface, the second connection terminal (250) being electrically connected to a second ending portion of the first via (225) and the second circuit board forming an inner space together with the first circuit board (210) and the interposer (220);

a second electronic component (231) electrically connected to the second connection terminal and disposed on the second circuit board.

Lim does not specifically disclose an antenna array to be used for forming a beam disposed on a second surface of the second circuit board that is opposite to the first surface of the second circuit board.

Liao teaches an antenna cavity structure (300) as shown in figures 13-16 comprising an antenna array (427, figure 14) to be used for forming a beam disposed on a second surface of the second circuit board (420, 430) that is opposite to the first surface of the second circuit board.

It would have been obvious to one having ordinary skill in the art before the effective filing date to have a teaching of Liao employed in the electronic device of Lim in order to provide excellent in high frequency transceivers in mobile communication applications.

Lim and Liao do not disclose a plating member including a first portion, a second portion and a third portion, the first portion attached to the first surface of the interposer, the second portion attached to the second surface of the interposer, and the third portion attached to a third surface of the interposer substantially perpendicular to the first surface and the second surface such that the third portion is extended over an entire height of the third surface, an ending portion of the first portion or an ending portion of the second portion connected to an ending portion of the second via,

wherein the plating member includes first plating member, second plating member and third plating member, a portion of the first plating member and a portion of

the second plating member attached to an outer side of the third surface, and a portion of the third plating attached to an inner side of the third surface.

Asahi teaches a connector member (100 or 200) as shown in figures 1-8 comprising a plating member (20) including a first portion (top portion, hereafter called TP), a second portion (bottom portion, BP) and a third portion (side portion formed on the side surface 10c, called SP), the first portion attached to the first surface of the interposer, the second portion attached to the second surface of the interposer, and the third portion attached to a third surface of the interposer substantially perpendicular to the first surface and the second surface such that the third portion is extended over an entire height of the third surface, an ending portion of the first portion or an ending portion of the second portion connected to an ending portion of the second via (or through holes 510, figures 3-8, the through hole or via connected to the first and second lands 20a, 20b), see para-0026+, and wherein the plating member includes first to third plating members (20), a portion of the first plating member and a portion of the second plating member attached to an outer side of the third surface, and a portion of the third plating see figure 8, attached to an inner side of the third surface.

It would have been obvious to one having ordinary skill in the art before the effective filing date to have a teaching of Asahi employed in the electronic device of Lim and Liao in order to provide internal electrical connections.

Regarding claim 13, Lim as modified by Liao and Asahi, Lao teaches the antenna array (427, figure 14) to be used for forming a beam corresponding to 5th generation communication (column 10, lines 32-40).

Regarding claim 14, Lim as modified by Liao and Asahi teaches the first plating member, the second plating member and the third plating member comprise a C shape.

As to claims 15-16, Lim as modified by Liao and Asahi discloses in figure 4 that a first shielding member (rear cover 102) is disposed on an a lower surface of the first circuit board (210), and a second shielding member (rear cover 102) is disposed on an upper surface of the first circuit board (210).

As to claims 17 and 19, Lim as modified by Liao and Asahi discloses a first pad (not shown but the element 220 must or have to have the pad for solder to the element 240) electrically connected to the first connection terminal (240) of the first circuit board (210) is formed on a lower portion of the via (225), and wherein a second pad (not shown, same as the first pad) electrically connected to the second connection terminal (250) of the second circuit board (220) is formed on an upper portion of the via (225).

As to claim 18, Lim as modified by Liao and Asahi teaches the interposer (200) as shown in figure 6 that is separated through at least one slit.

As to claim 20, Lim as modified by Liao and Asahi discloses the interposer comprises a ground region (at the ground unit 232 or 323) surrounding at least a part of the first and second vias (225).

Claim 2 is/are rejected under 35 U.S.C. 103 as being unpatentable over Lim in view of Casto and Asahi as applied to claims above, and further in view of Liao et al. (U.S. Patent 9,711,465).

Regarding claim 2, Lim as modified by Casto and Asahi discloses all of the limitations of claimed invention except for the antenna includes an antenna array to be used for forming a beam corresponding to 5th generation communication.

Liao teaches an antenna cavity structure (300) as shown in figures 13-16 comprising an antenna (427) includes an antenna array (figure 14) to be used for forming a beam corresponding to 5th generation communication (column 10, lines 32-40).

It would have been obvious to one having ordinary skill in the art before the effective filing date to have a teaching of Liao employed in the electronic device of Lim, Casto, and Asahi in order to provide excellent in high frequency transceivers in mobile communication applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TUAN T DINH whose telephone number is (571)272-1929. The examiner can normally be reached MON-FRI: 8AM-4:30PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Dole can be reached on 571-272-2229. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/TUAN T DINH/
Primary Examiner, Art Unit 2848