

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

TOPWIRE LLC

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD.
AND SAMSUNG ELECTRONICS
AMERICA, INC.,

Defendants.

Civil Action No. 2:25-cv-01183

JURY TRIAL DEMANDED

DEFENDANTS' INITIAL INVALIDITY CONTENTIONS

APPENDICES

Appendices A-1 through A-54

Invalidity claim charts for U.S. 9,859,202

I. INTRODUCTION

Pursuant to the Court’s Docket Control Order (Dkt. No. 21) and Patent Local Rules 3-3 and 3-4, Defendants Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively, “Samsung” or “Defendants”) provide these initial invalidity contentions (“Invalidity Contentions”) to Plaintiff TopWire LLC (“TopWire” or “Plaintiff”) for Claims 1–4, 6, and 9 (collectively, “Asserted Claims”) of U.S. Patent No. 9,859,202 (“the ’202 patent” or “Asserted Patent”). These Invalidity Contentions are based on Samsung’s current knowledge of the Asserted Patent and prior art, along with its understanding of TopWire’s infringement allegations set forth in its Disclosure of Asserted Claims and Infringement Contentions (“Infringement Contentions”), served on March 12, 2026. Samsung’s investigation of the prior art and other grounds of invalidity is ongoing, and Samsung expressly reserves the right to supplement these Invalidity Contentions as the case proceeds.

Samsung filed a Petition for *inter partes* review proceeding (“IPR”) at the Patent Trial and Appeal Board (“PTAB”), challenging the validity of each claim of the ’202 patent, which includes all Asserted Claims set forth in TopWire’s Infringement Contentions. *See* IPR2026-00324 (hereinafter “the ’202 IPR”), Paper 1 (March 31, 2026). Samsung hereby incorporates by reference the Petition in the ’202 IPR, including the exhibits thereto, as if set forth fully in these Invalidity Contentions. To the extent the ’202 IPR is instituted, Samsung will abide by the stipulation attached to the Petition. ’202 IPR, Paper 1, EX1031.

Nothing in these Invalidity Contentions is intended, nor should be construed, as a waiver of any claim construction argument or noninfringement position. Samsung’s statements herein (including the accompanying claim charts) reflect in certain places Samsung’s present understanding of the purported potential scope of the claims that TopWire appears to be advocating by way of its Infringement Contentions and are not to be seen as any acquiescence to TopWire’s

interpretation of any claims. To the extent that TopWire's Infringement Contentions imply or define a scope or construction of the Asserted Claims, Samsung disagrees that any such claim scope or construction is proper. To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases at this time. The Court established separate deadlines for the parties' proposed claim constructions, and Samsung will disclose its proposed constructions accordingly. For purposes of these Invalidity Contentions, Samsung may adopt alternative claim construction positions. Samsung reserves the right to supplement, modify, or otherwise amend these Invalidity Contentions, particularly to the extent that TopWire is allowed to assert any additional Asserted Claims or theories or to amend its contentions or otherwise attempt to correct the deficiencies in its Infringement Contentions or supplement them in any way.

Nothing herein shall be interpreted as an admission that: (1) the Asserted Claims are infringed by any of Samsung's products or instrumentalities, (2) any particular feature or aspect of any of the accused instrumentalities practices any limitation of the Asserted Claims, (3) there is 35 U.S.C. § 112 support for any limitation of the Asserted Claims, or (4) any of TopWire's proposed or implied constructions are supportable or proper.

Consistent with the Local Patent Rules and the Federal Rules of Civil Procedure, Samsung reserves the right to amend these Invalidity Contentions. The information and documents that Samsung produced with these Invalidity Contentions are provisional and subject to further revision as follows. Samsung expressly reserves the right to amend its disclosures and document production referenced herein should TopWire provide any information that it failed to provide in its Local Patent Rule 3-1 and 3-2 disclosures or should TopWire amend its disclosures in any way, whether

explicitly (*i.e.*, via moving for leave to amend or supplement) or implicitly. Further, because discovery has only recently begun, Samsung reserves the right to amend the information provided herein. Such amendments include, for example, identifying and relying on additional references, should Samsung's further analysis yield additional information or references, consistent with the Patent Rules or the Federal Rules of Civil Procedure. Samsung reserves the right to supplement these contentions in light of any additional prior art of which TopWire is aware and did not disclose to Samsung in discovery. Also, because third-party discovery is not yet complete, Samsung reserves the right to supplement these contentions in light of any newly discovered information or documentation produced by any third-parties with relevant information from whom Samsung may seek discovery via subpoenas. For example, Samsung expects to issue subpoenas to, and receive information from, third-parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed below and/or additional prior art. These third-parties include, without limitation, the authors, inventors, vendors, or assignees of the references listed in these disclosures.

Samsung also reserves the right to revise its ultimate contentions concerning the invalidity of the Asserted Claims based upon the Court's construction of the claim terms, any findings as to the priority dates of the Asserted Claims, and/or positions that TopWire, Samsung, or any expert witness may take concerning claim interpretation, infringement, and/or invalidity issues.

Prior art not included in this disclosure, whether known or not known to Samsung, may become relevant. In particular, Samsung is currently unaware of the extent, if any, to which TopWire will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Samsung. To the extent that such an issue arises, Samsung reserves the right to identify other references that would have made the addition of the allegedly missing limitation to

the disclosed device obvious or show that the allegedly missing limitation would have been known or readily apparent to a POSITA at the time of the invention in light of the disclosure of the prior art at issue.

For prior art patents and prior art publications identified in these Invalidity Contentions, Samsung reserves the right to rely on the public use, offer for sale, sale, and/or actual products embodying the methods and systems described therein uncovered during discovery. Samsung also reserves the right to rely upon any related patents and patent applications, foreign patent counterparts and foreign patent applications of U.S. patents identified in these Invalidity Contentions, and U.S. counterparts of foreign patents and foreign patent applications identified in these Invalidity Contentions.

Samsung's claim charts in Appendices A-1 through A-54 cite to or reference particular teachings and disclosures of the prior art as applied to features of the Asserted Claims, but a POSITA in the art generally may view an item of prior art in the context of other publications, literature, products, and understanding. As such, the cited portions are only examples, and Samsung reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation. Samsung further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony to establish reasons for combining certain cited references that render the Asserted Claims obvious. Where Samsung cites to a particular figure in a reference, the citation should be understood to encompass the caption and description of the figure and any text relating to the figure. Conversely, where Samsung cites to particular text referring to a figure, the citation should be understood to include the figure as well.

The references discussed in the claim charts in Appendices A-1 through A-54 may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the State of the Art in the relevant time frame or the foreseeability from a technical perspective of a POSITA at the time of the alleged invention and/or marketing and/or natural and expected evolution of the art. The suggested obviousness combinations are provided in the alternative to Samsung’s anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory.

II. ’202 PATENT AND ASSERTED CLAIMS

In its Infringement Contentions, TopWire asserts Claims 1–4, 6, and 9 (*i.e.*, “Asserted Claims”) of the ’202 patent (*i.e.*, “Asserted Patent”). Among the Asserted Claims, Claim 1 is an independent claim.

For the purposes of these contentions, Samsung only addresses those claims specifically asserted by TopWire in its March 12, 2026 Infringement Contentions. Samsung reserves the right to amend or supplement this disclosure as needed in light of any changes or amendments made, for any reason, to TopWire’s infringement theories, Infringement Contentions, or Asserted Claims.

III. PERSON OF ORDINARY SKILL IN THE ART

These Invalidity Contentions use the acronym “POSITA” to refer to a person of ordinary skill in the art at the time of the Asserted Patent.

Samsung contends that a POSITA in this case would have had either (i) a Master of Science in Electrical Engineering, Materials Science, Mechanical Engineering, or an equivalent field, or (ii) a Bachelor of Science in Electrical Engineering, Materials Science, Mechanical Engineering, or an equivalent field and two years of experience in the field of semiconductor packaging.

Samsung reserves the right to modify and/or supplement this contention as the case proceeds, including during expert discovery and/or after receiving TopWire’s contentions on this issue.

IV. PRIORITY DATE

The Plaintiff bears the burden of establishing the priority date to which each claim of the Asserted Patents is entitled. *See, e.g., In re NTP, Inc.*, 654 F.3d 1268, 1276 (Fed. Cir. 2011) (“[F]or a patent’s claim to be entitled to an earlier priority date, the patentee must *demonstrate* that the claims meet the requirements of 35 U.S.C. § 120.”); *Natural Alternatives Int’l, Inc. v. Iancu*, 904 F.3d 1375, 1380 (Fed. Cir. 2018) (“Accordingly, claims in a patent or patent application are not entitled to priority under § 120 at least until the patent owner *proves* entitlement to the PTO, the Board, or a federal court.”).

The ’202 patent claims priority on its face to U.S. Provisional Patent Application No. 62/184,034, filed on June 24, 2015.

TopWire’s Infringement Contentions allege that “the Asserted Claims of the Asserted Patent are entitled to a priority date of June 24, 2015.” *See* Infringement Contentions at 7. For the purposes of these Invalidity Contentions, Samsung assumes that post-AIA patent statutes apply based on TopWire’s claimed priority date of June 24, 2015, for all Asserted Claims. *Id.* This is in no way a concession that TopWire is entitled to that priority date.

Samsung specifically does not concede that the June 24, 2015 priority date is accurate. TopWire has not provided sufficient evidence to support its contention that the Asserted Claims of the ’202 patent are entitled to the priority dates of the provisional application.

In the event that TopWire seeks leave to amend its priority date or conception/reduction to practice contentions, Samsung reserves the right to supplement these Invalidity Contentions in light of those amendments. To the extent TopWire alleges that any prior art relied on in these

Invalidity Contentions does not actually qualify as prior art to the Asserted Patent, Samsung reserves the right to rebut those allegations (*e.g.*, by demonstrating an earlier critical date for the challenged prior art and/or a later priority date for the Asserted Patent and/or Asserted Claims) with additional evidence.

V. IDENTIFICATION OF PRIOR ART

Subject to Samsung's reservations of rights, Samsung identifies each item of prior art that anticipates or renders obvious one or more of the Asserted Claims, either expressly or inherently as understood by a POSITA, or based on TopWire's apparent interpretation of the claims. Samsung may also use the prior art identified to form the basis of the knowledge of a POSITA, in the sections that follow and/or in the claim chart appendices to these Invalidity Contentions. To the extent any references identified below and/or in the claim charts is not identified as an item of prior art that anticipates or renders obvious an Asserted Claim, Samsung intends to rely on such references as background and evidence of the state of the art at the time of the alleged inventions of the Asserted Patent. Samsung reserves the right to rely on additional prior art that may be uncovered during its continuing investigation and discovery.

In addition, many of the prior art references have related patent applications, publications, or issued patents that contain the same or materially the same subject matter (*e.g.*, published U.S. patent applications and publications, issued U.S. patents, and foreign applications or issued patents). Any citation to or quotation from any of these applications, publications, or patents, therefore, should be understood as encompassing any parallel citation to the same subject matter in other related or corresponding patent applications, publications, or issued patents. Moreover, Samsung relies on machine translations for various foreign prior art identified herein. Samsung reserves the right to update or amend these translations at a later time.

Also, to the extent not expressly stated herein, Samsung incorporates by reference any and all prior art contained or identified in documents produced thus far by TopWire in this case, each reference identified in all Appendices to these Invalidity Contentions, and any and all materials regarding invalidity that should have been timely produced by TopWire previously.

A. Prior Art Patents and Publications

The table below identifies patents and patent publications now known to Samsung that qualify as prior art to the Asserted Patent under at least 35 U.S.C. §§ 102(a)(1) and/or 102(a)(2). Invalidity claim charts for these references are attached as Appendices A-1 through A-54. Each listed reference became prior art at least as early as the dates provided on the face of the document, as indicated in the chart below, and/or as indicated in the corresponding Appendix. Samsung reserves the right to rely upon earlier dates of publication or public availability to the extent such information is uncovered during discovery. Samsung also reserves the right to rely on fact or expert witness testimony to establish the publication and/or public availability of any publications described below.

Table 1: Prior Art Patents and Published Patent Applications				
Patent Number	Title	Date(s)	Short Name	Appendix
US 2008/0155820	Wiring Substrate, Manufacturing Method Thereof, and Semiconductor Device	Pub: July 3, 2008	Arai	A-1
US 7,687,899	Dual Laminate Package Structure with Embedded Elements	Issued: Mar. 30, 2010	Berry	A-2
US 2013/0182402	PoP Structures Including Through-Assembly Via Modules	Pub: July 18, 2013	Chen '402	A-3
US 2015/0102484	Package Structure and Fabrication Method Thereof	Pub: April 16, 2015	Chen '484	A-4

Table 1: Prior Art Patents and Published Patent Applications				
Patent Number	Title	Date(s)	Short Name	Appendix
		Filed: Dec. 20, 2013		
US 9,401,320	Combined Substrate	Issued: July 26, 2016 Pub: Sept. 10, 2015 Filed: Mar. 4, 2015	Daizo	A-5
US 8,436,475	IC Device Having Low Resistance TSV Comprising Ground Connection	Issued: May 7, 2013	Dunne	A-6
US 8,618,669	Combination Substrate	Issued: Dec. 31, 2013	Furuta '669	A-7
US 2009/0140415	Combination Substrate	Pub: June 4, 2009	Furuta '415	A-8
US 8,513,792	Package-on-Package Interconnect Stiffener	Issued: Aug. 20, 2013	Ganesan	A-9
US 2015/0061142	Ultra Fine Pitch PoP Coreless Package	Pub: Mar. 5, 2015	Hsu '142	A-10
US 8,981,559	Package on Package Devices and Methods of Packaging Semiconductor Dies	Issued: Mar. 17, 2015	Hsu '559	A-11
US 2013/0175687	Package Stack Device and Fabrication Method Thereof	Pub: July 11, 2013	Hu '687	A-12
US 2013/0249083	Packaging Substrate	Pub: Sept. 26, 2013	Hu '083	A-13
US 9,357,659	Packaging Substrate Having Embedded Through-Via Interposer	Issued: May 31, 2016 Pub: May 14, 2015	Hu '659	A-14
US 8,017,436	Thin Substrate Fabrication Method and Structure	Issued: Sept. 13, 2011	Huemoeller	A-15
US 2015/0132950	Semiconductor Packages, Methods of Manufacturing the Same, and	Pub: May 14, 2015	Jung	A-16

Table 1: Prior Art Patents and Published Patent Applications				
Patent Number	Title	Date(s)	Short Name	Appendix
	Semiconductor Package Structures Including the Same			
US 2015/0061093	Interposer and Semiconductor Package Using the Same, and Method of Manufacturing Interposer	Pub: Mar. 5, 2015	Kim	A-17
US 2014/0054773	Electronic Component Built-In Substrate and Method of Manufacturing the Same	Pub: Feb. 27, 2014	Kurashima	A-18
US 9,368,566	Package on Package (PoP) Integrated Device Comprising a Capacitor in a Substrate	Issued: June 14, 2016 Pub: Jan. 21, 2016 Filed: Jul. 17, 2014	Lee	A-19
US 7,514,774	Stacked Multi-Chip Package with EMI Shielding	Issued: April 7, 2009	Leung	A-20
US 10,418,298	Semiconductor Device and Method of Forming Dual Fan-Out Semiconductor Package	Issued: Sept. 17, 2019 Pub: Mar. 26, 2015 Filed: Sept. 24, 2013	Lin	A-21
US 2014/0252561	Via-Enabled Package-on-Package	Pub: Sept. 11, 2014	Lisk	A-22
TW 2006/01516	Stacked Multi-Package Module	Filed: June 25, 2004	Liu	A-23
US 5,334,804	Wire Interconnect Structures for Connecting an Integrated Circuit to a Substrate	Issued: Aug. 2, 1994	Love	A-24
US 2013/0127054	Stacked-Chip Packages in Package-on-Package Apparatus, Methods of	Pub: May 23, 2013	Muthukumar	A-25

Table 1: Prior Art Patents and Published Patent Applications				
Patent Number	Title	Date(s)	Short Name	Appendix
	Assembling Same, and Systems Containing Same			
US 2004/0227258	Electronic Component Packaging Structure and Method for Producing the Same	Pub: Nov. 18, 2004	Nakatani	A-26
US 6,521,530	Composite Interposer and Method for Producing a Composite Interposer	Issued: Feb. 18, 2003	Peters	A-27
US 7,049,170	Integrated Circuits and Packaging Substrates with Cavities, and Attachment Methods Including Insertion of Protruding Contact Pads into Cavities	Issued: May 23, 2006	Savastiouk '170	A-28
US 2005/0189636	Packaging Substrates for Integrated Circuits and Soldering Methods	Pub: Sept. 1, 2005	Savastiouk '636	A-29
US 9,685,414	Package Assembly for Embedded Die and Associated Techniques and Configurations	Issued: June 20, 2017 Filed: June 26, 2013	Shuto	A-30
US 2011/0147908	Module for Use in a Multi Package Assembly and a Method of Making the Module and the Multi Package Assembly	Pub: June 23, 2011	Sun	A-31
US 2012/0139010	Interposer and Semiconductor Device	Pub: June 7, 2012	Takeda	A-32

Table 1: Prior Art Patents and Published Patent Applications				
Patent Number	Title	Date(s)	Short Name	Appendix
US 8,379,403	Spacer-Connector and Circuit Board Assembly	Issued: Feb. 19, 2013	Waite	A-33
US 10,319,607	Package-on-Package Structure with Organic Interposer	Issued: June 11, 2019 Pub: Feb. 25, 2016 Filed: Aug. 22, 2014	Wu	A-34
US 2012/0119370	Semiconductor Package and Semiconductor System Including the Same	Pub: May 17, 2012	Yoo	A-35
US 10,026,671	Substrate Design for Semiconductor Packages and Method of Forming Same	Issued: July 17, 2018 Pub: Aug. 20, 2015 Filed: Aug. 29, 2015 Priority: Feb. 14, 2014	Yu '671	A-36
US 11,107,798	Semiconductor Packages and Methods of Forming the Same	Issued: Aug. 31, 2021 Pub: Sept. 3, 2020 Filed: May 18, 2020 Priority: Aug. 22, 2014	Yu '798	A-37

Samsung's investigation into prior art patent and publication references remains ongoing, and Samsung reserves the right to identify and rely upon additional patent or publication references.

B. Prior Art Non-Patent Publications

The table below identifies non-patent printed publications now known to Samsung that qualify as prior art to the Asserted Patent under at least 35 U.S.C. §§ 102(a)(1) and/or 102(a)(2). Each listed reference became prior art at least as early as the dates provided on the face of the document, as indicated in the chart below, and/or as indicated in the corresponding Appendix.

Samsung reserves the right to rely upon earlier dates of publication or public availability to the extent such information is uncovered during discovery. Samsung also reserves the right to rely on fact or expert witness testimony to establish the publication and/or public availability of any publications described below.

Table 2: Prior Art Printed Publications			
Title	Author/Publisher	Date	Appendix
Polymer Adhesives and Encapsulants for Microelectronic Applications	Richard C. Benson, et al.	January 1, 2008	A-38
Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration	Rabindra N. Das, et al. 25th International Symposium on Microelectronics	Sept. 13, 2012	A-39
Copper Pillar Bumping Technology	Christopher Henderson InfoTracks Semitracks Monthly Newsletter	June 27, 2012	A-40
Embedded Glass Interposer for Heterogeneous Multi-Chip Integration	Dyi-Chung Hu, et al. Institute of Electrical and Electronics Engineers (IEEE)	May 29, 2015	A-41
The Requirement of Future Substrate - Maker Point of View -	Dyi-Chung Hu Unimicron	April 22, 2014	A-42
IPC-4761 Design Guide for Protection of Printed Board Via Structures	Associate Connecting Electronics Industries (IPC)	May 7, 2008	A-43
Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module	Christian Kriedl	December 31, 2011	A-44
All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices	Tyler N. Osborn	April 2, 2009	A-45
Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects	Aibin Yu, et al. Institute of Electrical and Electronics Engineers (IEEE)	July 18, 2011	A-46

Samsung's investigation into non-patent printed publications remains ongoing, and Samsung reserves the right to identify and rely upon additional non-patent printed publications.

C. Prior Art Systems on Sale and/or Publicly Used

The table below identifies systems and products that were publicly available and/or used, offered for sale, or sold and qualify as prior art to the Asserted Patent under 35 U.S.C. §§ 102(a)(1) and/or 102(a)(2). Some or all of the supporting references for these systems, as cited below and in the corresponding Appendices, may also qualify as prior art publications under 35 U.S.C. §§ 102, such as manuals, patents, and other information intended to cover these products and systems, and may be used as invalidating prior art under 35 U.S.C. §§ 102 and 103. In addition, Samsung incorporates by reference the individuals identified in its initial disclosures, and Samsung also continues to investigate the systems and products and reserves the right to supplement the contentions and accompanying claim charts after further discovery and investigation. Samsung also reserves the right to rely on fact or expert witness testimony to establish the public knowledge, use, availability, sale, or offer for sale of any systems described below. Although additional information and prior art systems may be obtained through discovery, such prior art systems include at least the following:

Table 3: Prior Art Systems			
System/Item	Date(s)	Person/Entity	Appendix
Teensy Board	Dec. 21, 2014	PJRC, LLC	A-47
Seeed Board	Dec. 14, 2014	Seeed Technology Limited	A-48
SainSmart Board	Feb. 9, 2014	SainSmart	A-49
Apple iPhone 1	2007	Apple Inc.	A-50
Through Mold Via (TMV) PoP	2011	Amkor Technology, Inc.	A-51

MCeP	2013	Shinko Electric Industries Co., Ltd.	A-52
Apple iPhone 4–6	2014	Apple Inc.	A-53
EIT Package-Interposer-Package (PIP) Test Vehicle	Sept. 2012	Endicott Interconnect Technologies, Inc.	A-54
Preci-Dip PCB Connectors	2014 ¹	Preci-Dip SA	N/A
Mill-Max PCB Connectors	2013 ²	Mill-Max Mfg. Corp	N/A

Samsung’s investigation into prior art systems is ongoing and discovery is only in its early stages. Samsung will amend or supplement its disclosures of these systems, as its investigation and discovery continue, including third-party discovery. Samsung also reserves the right to rely on fact or expert witness testimony to establish the public knowledge, use, availability, sale, or offer for sale of any systems described above and in the accompanying claim charts.

D. Admitted Prior Art

Statements made by the Applicant in the specification and/or during prosecution of the Asserted Patent and any related patents/applications, such as in the “Background of the Invention” section that describes the related art known to the Applicant, are admissions that can be relied upon for both anticipation and obviousness determinations, regardless of whether the admitted prior art would otherwise qualify as prior art under the statutory categories set forth in 35 U.S.C. § 102. *See* MPEP §§ 2129 and 608.01(c). To the extent TopWire contends that the Asserted Claims are not invalid as anticipated by and/or obvious in view of the prior art under 35 U.S.C. §§ 102 and 103,

¹ *See, e.g.*, <https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html>

² *See, e.g.*, <https://web.archive.org/web/20130827161228/http://www.mill-max.com/>

Samsung reserves the right to rely on Applicant's "Admitted Prior Art" to demonstrate the invalidity of the Asserted Claims.

For example, the Asserted Patent and/or the alleged inventor(s) thereof admit that all of the following was prior art. Samsung reserves the right to supplement the list of admitted prior art to refer to additional admissions:

- Spacer connectors deposited between a top and bottom package substrate. *See, e.g.*, '202 patent at 1:12–15 ("Technical Field The present invention relates to a fabricating process for making a *spacer connector*, especially using a conductive carrier in an initial step of the fabrication process.").
- Metal pillars on a substrate, such as "a plurality of bottom metal pillars" on "a top package substrate" and "a plurality of top metal pillars" on "a bottom package substrate. *See, e.g.*, '202 patent at 1:16–18 ("One of the traditional processes for fabricating metal circuitry, a seed layer is often applied before *electric plating*," which was a well-known process to form metal pillars/posts on a substrate); Hu '083 (A-13) at [0008] ("[M]etal posts are formed by electroplating.").

VI. GROUNDS FOR INVALIDITY UNDER 35 U.S.C. §§ 102, 103

Samsung contends that all Asserted Claims of the Asserted Patent are invalid under 35 U.S.C. §§ 102, 103, and/or 112. The Appendices to these Invalidity Contentions contain claim charts for prior art references selected by Samsung. Specifically, the claim chart Appendices to these Invalidity Contentions set forth how the prior art identified by Samsung anticipates either expressly or inherently, or renders obvious, each Asserted Claim. Samsung cites exemplary relevant portions of the identified prior art references to provide notice of its theories of invalidity. However, other portions of the identified reference may additionally anticipate, either expressly or inherently, or render obvious one or more of the Asserted Claims. In addition, a POSITA generally would view each prior art reference in the context of other publications, literature, products, systems, and understanding. As such, the cited portions are merely exemplary, and Samsung

reserves the right to rely on uncited portions of the prior art references and on other publications, expert testimony, and other evidence as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation or any of the Asserted Claims as whole. Samsung further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony, including expert testimony, to establish bases for combinations of certain cited references that render the Asserted Claims obvious. Further, as a general matter, all portions of each prior art reference are relied upon to support the disclosure of each patent claim limitation, as all portions provide general support. Supporting citations are still provided, but do not necessarily represent every location where a particular claim limitation may be found in the prior art reference.

Where Samsung cites a particular drawing or figure in the accompanying charts, the citation encompasses the description of the drawing or figure, as well as any text associated with the drawing or figure (even if the associated text is not itself expressly cited). Similarly, where Samsung cites particular text concerning a drawing or figure in the accompanying charts, the citation encompasses that drawing or figure as well (even if the associated drawing or figure is not expressly cited). Samsung further incorporates by reference the prior art references cited during prosecution of the Asserted Patent, any patents or patent applications related to the Asserted Patent, and any patent or patent application sharing a common inventor with the Asserted Patent. This includes without limitation those identified in any other proceeding involving the Asserted Patent or related U.S. or foreign patents. Samsung additionally incorporates by reference all prior art produced or otherwise known to Plaintiff and all prior art known to the named inventors, any past or current owner, or any individual substantively involved in the prosecution of the Asserted Patent.

Samsung contends that at least some of the systems and products disclosed in one or more of the prior art references identified here or in the attached Appendices are prior art under 35 U.S.C. §§ 102(a)(1) and/or 102(a)(2), and/or 103. Samsung's reference to any particular component, device, machine, or other product herein should also be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited here or in the attached Appendices that relate to the cited component, device, machine, or other product. Samsung's reliance on each prior art reference identified throughout these Invalidity Contentions includes the reference itself, anything incorporated by the reference or described as relevant technology by the reference, any system embodying the reference, and any testimony by those with knowledge of the reference, such as named authors and inventors. All such documents and information shall be considered one prior art reference to the extent they describe a single prior art system, technology or solution. Moreover, while some prior art may be charted separately, Samsung reserves the right to show that combinations of individual charts describe a portion of single prior art system or solution.

Samsung does not yet have complete information regarding the dates by which some of the cited products were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. Samsung reserves the right to amend these Invalidity Contentions upon obtaining further information related to the cited products herein, including information obtained relating to any Samsung products or third-party products obtained through subpoenas as this case progresses through discovery.

It is understood that a POSITA reads a prior art reference as a whole and in the context of

other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a POSITA also relies upon other information including other publications and general scientific, engineering or other relevant knowledge. Samsung reserves the right to rely upon the general scientific, engineering or other relevant knowledge in the field in interpreting the disclosure of the prior art references. In addition, Samsung reserves the right to rely upon other publications and on expert testimony to provide context and to aid in the understanding of the prior art references. Samsung also reserves the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a POSITA, including the basis for modifying or combining the prior art references. Furthermore, Samsung reserves the right to rely upon any admissions relating to prior art found in the intrinsic evidence for the Asserted Patent.

Certain pieces of identified prior art inherently disclose features of the Asserted Claims. Samsung may rely on inherency to demonstrate the invalidity of the Asserted Claims. Moreover, certain prior art references and solutions may inherently anticipate certain features of the Asserted Claims as construed by Plaintiff. Samsung may rely on other portions of the prior art, other documents, and expert testimony to establish the inherency of certain features of the prior art to invalidate the Asserted Claims. Samsung also may rely on any reference identified in these invalidity contentions or any other reference to prove that the references are enabled or to explain the meaning of a term used in the solutions or any reference.

Whether a prior art reference anticipates or renders obvious the Asserted Claims may depend on claim construction. To the extent any limitation is deemed not to be met exactly by an item of prior art, Samsung contends that the difference would have been obvious to a POSITA and

within the knowledge of one skilled in the art at the time of the alleged invention, such that the claimed invention would have been obvious both in light of the single reference alone and/or in light of combined references.

To the extent that prior art cited for a particular limitation discloses functionality that is the same or similar in some respect to the alleged functionality in the accused products as set forth in TopWire's Infringement Contentions (notwithstanding the deficiencies therein), Samsung does not concede that those limitations are in fact met by those accused functionalities.

Further, in the attached Appendices to these Invalidity Contentions, Samsung has identified where the prior art references disclose subject matter recited in the preambles of the Asserted Claims, without regard to whether the preambles are properly considered to be limitations of the Asserted Claims.

Samsung's proposed obviousness combinations of the prior art references are separately identified throughout these Invalidity Contentions (including in § VI.B, below).

Samsung reserves the right to further streamline and reduce the number of anticipation and/or obviousness references relied on with respect to a given Asserted Claim and to exchange or otherwise modify the specific references relied upon for anticipation and within each obviousness combination for each asserted claim. Discovery is at an early stage, and TopWire has not provided sufficient contentions or documentation with respect to any pre-filing invention dates or with respect to claim limitations that are allegedly lacking or not obvious in the prior art.

A. Anticipation

Samsung contends that the Asserted Claims of the '202 patent are anticipated by the prior art, or are obvious in view of the prior art, as set forth in the table below. Samsung provides Appendices A-1 through A-54, which contain claim charts demonstrating the invalidity of the Asserted Claims of the '202 patent.

Each Asserted Claim is anticipated or rendered obvious by the following prior art, either alone or in combination with the knowledge of a POSITA, the state of the art, admitted prior art, or in combination one or more other prior art references as described below in § VI.B:

- Arai (A-1)
- Berry (A-2)
- Chen '402 (A-3)
- Chen '484 (A-4)
- Daizo (A-5)
- Dunne (A-6)
- Furuta '669 (A-7)
- Furuta '415 (A-8)
- Ganesan (A-9)
- Hsu '142 (A-10)
- Hsu '559 (A-11)
- Hu '687 (A-12)
- Hu '083 (A-13)
- Hu '659 (A-14)
- Huemoeller (A-15)
- Jung (A-16)
- Kurashima (A-18)
- Lee (A-19)
- Leung (A-20)
- Lin (A-21)
- Lisk (A-22)
- Liu (A-23)
- Love (A-24)
- Nakatani (A-26)
- Peters (A-27)
- Savastiouk '170 (A-28)
- Savastiouk '636 (A-29)

- Shuto (A-30)
- Sun (A-31)
- Waite (A-33)
- Wu (A-34)
- Yoo (A-35)
- Yu '671 (A-36)
- Yu '798 (A-37)
- Polymer Adhesives and Encapsulants for Microelectronic Applications (A-38)
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39)
- Copper Pillar Bumping Technology (A-40)
- Embedded Glass Interposer for Heterogeneous Multi-Chip Integration (A-41)
- The Requirement of Future Substrate - Maker Point of View - (A-42)
- IPC-4761 Design Guide for Protection of Printed Board Via Structures (A-43)
- Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module (A-44)
- All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices (A-45)
- Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects (A-46)
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Apple iPhone 1 (A-50)
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- Apple iPhone 4-6 (A-53)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

B. Obviousness

A massive body of relevant, analogous prior art existed as of the earliest filing dates of the

Asserted Claims, as identified, for example, in § V, *supra*. Taken together, this prior art discloses each and every limitation of every asserted claim. Example combinations of specific prior art references that Samsung may rely on at trial to demonstrate obviousness of the Asserted Claims are set forth below. Such obviousness combinations are provided in the alternative to Samsung's anticipation contentions and are not to be construed to suggest that any references included in the combinations is not by itself anticipatory or that any particular limitation is missing from a particular reference.

Given the scope and content of these prior art references, the lack of any substantial differences between these references and the Asserted Claims, and the knowledge of a POSITA at the time of the alleged inventions, it would have been obvious to combine the specified references. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007). Moreover, a POSITA had a motivation to combine these references because—at a minimum—they all pertain to the subject of spacer connectors.

One or more combinations of the prior art references identified above would have been obvious because those references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions with a reasonable expectation of success and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. In addition, the combination of the prior art references identified above would have been obvious because the combination represents the known potential

options with a reasonable expectation of success.

These rationales would have motivated a POSITA to combine the identified prior art items and teachings. As the Supreme Court held in *KSR Int'l Co. v. Teleflex, Inc.*, “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” 550 U.S. 398, 416 (2007). The Supreme Court further held that “[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *Id.* at 418.

“[I]n many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.* at 420. For example, the Supreme Court held that it is sufficient that a combination of elements was “obvious to try,” recognizing that “[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense.” *Id.*

Patents like the Asserted Patent here are invalid, the Supreme Court explained, because “[g]ranting patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility.” *Id.* at 402. Here, each of the prior art items identified above is directed to the same field of endeavor as the Asserted Patent at least under

TopWire’s apparent interpretation³. Further, each prior art item was directed to the same problem or problems that the Asserted Patent purportedly addressed. The Asserted Claims therefore represent, at the most, mere “ordinary skill and common sense,” not innovation. In other words, the alleged inventions of the Asserted Patent are, at most, obvious combinations or adaptations of well-known technology used in predictable ways.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the invention(s); and the background knowledge that would have been possessed by a POSITA.

Thus, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of POSITAs; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known

³ As reflected in TopWire’s Infringement Contentions, TopWire broadly interprets the field of endeavor to include not only semiconductor packaging technology but also printed circuit board assembly technology. TopWire’s Infringement Contentions at 3, 5–6. In addition, TopWire appears to have also taken broad interpretations regarding certain terms. *See e.g.*, TopWire’s Infringement Contentions, Ex. A, at 8–9 (interpreting “bottom package substrate” and “top package substrate” to cover printed circuit boards), 18 (interpreting “metal pillars protrudes downwardly from a bottom surface of the core substrate” to cover metal pillars that are flush with the bottom surface of a core substrate), 19–20 (interpreting “bottom metal pillars” and “top metal pillars” to cover solder connections); Samsung’s Petition, IPR2026-00324 at 5–8 (discussing TopWire’s apparent claim constructions). For the purpose of this Invalidity Contentions only, Samsung adopts TopWire’s apparent interpretation for all relevant terms until further resolution of the disputes during the claim construction as set forth in the Court’s Docket Control Order. For avoidance of doubt, Samsung does not concede TopWire’s interpretations are correct.

technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim because every element of each dependent claim was known by a POSITA at the time of the alleged invention, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Samsung contends that each Asserted Claim would have been obvious not only by the combinations explicitly defined in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the exemplary prior art references, systems, and teachings identified herein and in the accompanying Appendices, the common knowledge of POSITAs also constitutes prior art, and may be relied on by Samsung through testimony or declarations in combination with the identified prior art. The knowledge of a POSITA at the time of the alleged invention would also include, for example, the known advantages and disadvantages of each of the limitations recited in the Asserted Claims. It would have been obvious to combine the references and teachings identified herein with one another based on the nature of the problem to be solved, the general knowledge of a person of ordinary skill in the art, the teachings of other art in existence at that time, and the recognition of similarities between the art and the claimed features. On these bases,

each identified prior art item can be combined with others if a particular prior art item lacks or does not exactly disclose a limitation or feature of an Asserted Claim.

Samsung hereby expressly incorporates by reference any statements and reasons set forth by the Examiner during prosecution of the Asserted Patent and any relevant family patents, including the First Reissue, the Parent Patent, and any continuation patents that may issue from the Asserted Patent, particularly as to why it would have been obvious to modify or combine references to achieve the limitations of the Asserted Claims. Numerous prior art references, including those identified above, reflect common knowledge and the state of the prior art before the priority date claimed on the face of each asserted patent.

For at least the reasons described above and below in the examples provided as well as in the claim chart Appendices, it would have been obvious to a POSITA to combine any of a number of prior art references, including any combination of those identified in Appendices A-1 through A-54, to meet the limitations of the Asserted Claims. Samsung provides additional motivations to combine as to specific exemplary combinations and elements, as discussed in the sections that follow. As such, Samsung's inclusion of exemplary combinations does not preclude Samsung from identifying other invalidating combinations as appropriate.

1. Top Package Substrate Stacked on Top of a Bottom Package Substrate

Claim 1 of the '202 patent recites "a top package substrate stacked on top of the bottom package substrate." *See, e.g.*, '202 patent, Claim 1. Claims 2–4, 6, and 9 each depend from Claim 1, and therefore incorporate this limitation.

Nothing about the claimed, generic "top package substrate stacked on top of the bottom package substrate," as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of "a top package substrate stacked on top of the bottom package substrate"

was well known in the art before the alleged invention of the '202 patent. To the extent any of the structural elements reciting a stacked “top package substrate” and “bottom package substrate” is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, [0043]
- Berry (A-2) at, *e.g.*, [3:15-3:24], [4:55-4:62]
- Chen '402 (A-3) at, *e.g.*, [0018-0019]
- Chen '484 (A-4) at, *e.g.*, [0050-0054]
- Daizo (A-5) at, *e.g.*, [1:26-1:32], [2:3-2:10]
- Furuta '669 (A-7) at, *e.g.*, [7:16-7:38]
- Furuta '415 (A-8) at, *e.g.*, [0020], [0040]
- Ganesan (A-9) at, *e.g.*, [2:45-2:66]
- Hsu '142 (A-10) at, *e.g.*, [0048]
- Hsu '559 (A-11) at, *e.g.*, [2:50-3:6]
- Hu '687 (A-12) at, *e.g.*, [0041]
- Hu '083 (A-13) at, *e.g.*, [0039]
- Jung (A-16) at, *e.g.*, [0265-0267]
- Kim (A-17) at, *e.g.*, [0038]
- Kurashima (A-18) at, *e.g.*, [0075-0076]
- Lee (A-19) at, *e.g.*, [5:3-5:14]
- Lisk (A-22) at, *e.g.*, [0023]
- Muthukumar (A-25) at, *e.g.*, [0035]
- Nakatani (A-26) at, *e.g.*, [0092-0093]
- Shuto (A-30) at, *e.g.*, [3:13-3:25]
- Sun (A-31) at, *e.g.*, [0047], [0058-0059]
- Takeda (A-32) at, *e.g.*, [0146-0148]
- Waite (A-33) at, *e.g.*, [6:59-7:6]

- Wu (A-34) at, *e.g.*, [2:37-2:51]
- Yu '798 (A-37) at, *e.g.*, [5:16-5:41], [7:32-7:45]
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, 4
- The Requirement of Future Substrate - Maker Point of View - (A-42) at, *e.g.*, 24
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Apple iPhone 1 (A-50)
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- Apple iPhone 4-6 (A-53)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to interconnect mounted components would have recognized that a top package substrate could be stacked on top of a bottom package substrate. Such a configuration was a well-known design choice in the semiconductor packaging art, as it allowed manufacturers to improve electrical performance, reduce the size of a semiconductor package, and decrease the interconnect length between mounted components.

The motivation to vertically stack a top package substrate and bottom package substrate to improve electrical performance, reduce the size of a semiconductor package, and decrease the interconnect length was known in the prior art at the time. *See, e.g.*, Chen '484 (A-4) at [0004] (“To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39)

at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”); Waite (A-33) at [7:1-7:6] (“cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”). Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose top package substrates stacked on top of bottom package substrates. *See, e.g.*, Chen ’402 (A-3) at [0019] (disclosing the “bonding of top package component 62 to bottom package 60”); Sun (A-31) at [0048] (disclosing an upper PoP module stacked on a first module 110, with a second substrate 300 interposed therebetween, wherein a “plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140.... For example an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.”).

As these exemplary teachings demonstrate, improving existing semiconductor packaging designs that are ready for improvement by stacking a top package substrate on top of a bottom package substrate was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any

such combination and where, as here, such combinations of references listed above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded decreased interconnection length, more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered known improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of decreasing interconnector length, improving reliability at high temperatures, and reducing solder bridging is of special interest or importance in the field. *See, e.g.,* Chen '484 (A-4) at [0004] ("To improve

electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts.”); Waite (A-33) at [7:1-7:6] (“cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”).

2. Spacer Connector Between Package Substrates

Claim 1 of the ’202 patent recites “at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.” *See, e.g.,* ’202 patent, Claim 1. Claims 2–4, 6, and 9 each depend from Claim 1, and therefore incorporate this limitation.

Nothing about the claimed, generic “spacer connector,” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of a “spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate” was well known in the art before the alleged invention of the ’202 patent. To the extent any of the structural elements reciting a “spacer connector” is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, [0043-0045]
- Berry (A-2) at, *e.g.*, [7:40-7:57]

- Chen '402 (A-3) at, *e.g.*, [0018-0019]
- Chen '484 (A-4) at, *e.g.*, [0040-0044]
- Daizo (A-5) at, *e.g.*, [2:8-2:10]
- Dunne (A-6) at, *e.g.*, [9:18-9:32]
- Furuta '669 (A-7) at, *e.g.*, [7:18-7:20]
- Furuta '415 (A-8) at, *e.g.*, [0021-0023]
- Ganesan (A-9) at, *e.g.*, [3:3-3:12]
- Hsu '142 (A-10) at, *e.g.*, [0046]
- Hsu '559 (A-11) at, *e.g.*, [2:50-2:63]
- Hu '687 (A-12) at, *e.g.*, [0037-0041]
- Hu '083 (A-13) at, *e.g.*, [0037]
- Hu '659 (A-14) at, *e.g.*, [6:18-6:26]
- Huemoeller (A-15) at, *e.g.*, [16:19-16:55]
- Jung (A-16) at, *e.g.*, [0266-0267]
- Kim (A-17) at, *e.g.*, [0035]
- Kurashima (A-18) at, *e.g.*, [0079-0080]
- Lee (A-19) at, *e.g.*, [6:1-6:27]
- Leung (A-20) at, *e.g.*, [4:36-4:54]
- Lin (A-21) at, *e.g.*, [36:57-38:6]
- Lisk (A-22) at, *e.g.*, [0033]
- Liu (A-23) at, *e.g.*, 3
- Love (A-24) at, *e.g.*, [12:13-12:25]
- Muthukumar (A-25) at, *e.g.*, [0021]
- Nakatani (A-26) at, *e.g.*, [0092-0093]
- Peters (A-27) at, *e.g.*, [12:65-13:30]
- Savastiouk '170 (A-28) at, *e.g.*, [8:20-8:25]
- Savastiouk '636 (A-29) at, *e.g.*, [0027-0028]
- Shuto (A-30) at, *e.g.*, [3:13-3:25]
- Sun (A-31) at, *e.g.*, [0048]
- Takeda (A-32) at, *e.g.*, [0035], [0146-0148]
- Waite (A-33) at, *e.g.*, [6:59-7:6]

- Wu (A-34) at, *e.g.*, [4:57-5:5]
- Yoo (A-35) at, *e.g.*, [0069-0072]
- Yu '671 (A-36) at, *e.g.*, [10:58-11:3]
- Yu '798 (A-37) at, *e.g.*, [9:4-9:28]
- Polymer Adhesives and Encapsulants for Microelectronic Applications (A-38) at, *e.g.*, 63
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, 1–4
- Copper Pillar Bumping Technology (A-40) at, *e.g.*, 1–3
- Embedded Glass Interposer for Heterogeneous Multi-Chip Integration (A-41) at, *e.g.*, 315
- The Requirement of Future Substrate - Maker Point of View - (A-42) at, *e.g.*, 23
- Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module (A-44) at, *e.g.*, 32–33
- All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices (A-45) at, *e.g.*, 16–17
- Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects (A-46) at, *e.g.*, 1337–38
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- Apple iPhone 4–6 (A-53)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to interconnect a top package substrate and a bottom package substrate would have recognized that such a goal could be accomplished with a spacer connector. Such a

configuration was a well-known design choice in the semiconductor packaging art, as it allowed manufacturers to interconnect stacked package substrates while providing room for mounted components and improving rigidity of the overall structure.

The motivation to interpose a vertically stacked top package substrate and bottom package substrate with a spacer connector to interconnect stacked package substrates while providing room for mounted components and improving rigidity of the overall structure was known in the prior art at the time. *See, e.g.*, Sun (A-31) at [0048] (“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200”). Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose spacer connectors interposed between a top package substrate and a bottom package substrate. *See, e.g.*, Chen ’402 (A-3) at [0021] (“the connection between top package component 62 and bottom package 60 is through TAV modules 28”); Sun (A-31) at [0048] (disclosing an upper PoP module stacked on a first module 110, with a second substrate 300 interposed therebetween, wherein a “plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140.... For example an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.”); Hsu ’142 (A-10), at [0029] (“The presence of reinforcement layer 128 provides rigidity and stiffness for better handling of substrate 112 in the absence of carrier 100.”).

As these exemplary teachings demonstrate, improving existing semiconductor packaging designs that are ready for improvement by interposing a spacer connector between a vertically stacked top package substrate and a bottom package substrate was known in the art and would

yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit

and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of interconnecting package substrates is of special interest or importance in the field. *See, e.g.*, Sun (A-31) at [0048] (“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200”).

3. Metal Pillars

Claim 1 of the '202 patent recites “a plurality of metal pillars, each passing through the core substrate.” *See, e.g.*, '202 patent, Claim 1. Claims 2–4, 6, and 9 each depend from Claim 1, and therefore incorporate these limitations.

Nothing about the claimed, generic “metal pillars,” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of a “metal pillar,” which appears to refer to a copper pillar structure in the specification, was well known in the art before the alleged invention of the '202 patent. To the extent any of the structural elements reciting a “metal pillar” is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, [0037]
- Berry (A-2) at, *e.g.*, [4:15-4:32]
- Chen '402 (A-3) at, *e.g.*, [0010]
- Chen '484 (A-4) at, *e.g.*, [0043-0045]
- Dunne (A-6) at, *e.g.*, [7:58-8:10]
- Furuta '669 (A-7) at, *e.g.*, [8:39-8:56]

- Furuta '415 (A-8) at, *e.g.*, [0034-0037]
- Ganesan (A-9) at, *e.g.*, [3:60-4:3]
- Hsu '142 (A-10) at, *e.g.*, [0026]
- Hsu '559 (A-11) at, *e.g.*, [3:65-4:10]
- Hu '687 (A-12) at, *e.g.*, [0038]
- Hu '083 (A-13) at, *e.g.*, [0037]
- Hu '659 (A-14) at, *e.g.*, [1:64-2:23]
- Huemoeller (A-15) at, *e.g.*, [16:19-16:55]
- Jung (A-16) at, *e.g.*, [0270-0271]
- Kim (A-17) at, *e.g.*, [0035]
- Kurashima (A-18) at, *e.g.*, [0068-0069]
- Lee (A-19) at, *e.g.*, [5:47-5:57]
- Leung (A-20) at, *e.g.*, [3:42-3:61]
- Lin (A-21) at, *e.g.*, [55:8-55:17]
- Lisk (A-22) at, *e.g.*, [0025]
- Liu (A-23) at, *e.g.*, 3
- Love (A-24) at, *e.g.*, [12:42-12:59]
- Muthukumar (A-25) at, *e.g.*, [0026]
- Nakatani (A-26) at, *e.g.*, [0081]
- Peters (A-27) at, *e.g.*, [8:20-8:34]
- Savastiouk '170 (A-28) at, *e.g.*, [4:9-4:13]
- Savastiouk '636 (A-29) at, *e.g.*, [0027]
- Shuto (A-30) at, *e.g.*, [3:13-3:25]
- Sun (A-31) at, *e.g.*, [0062-0063]
- Takeda (A-32) at, *e.g.*, [0035]
- Waite (A-33) at, *e.g.*, [6:59-6:66]
- Wu (A-34) at, *e.g.*, [3:5-3:9]
- Yoo (A-35) at, *e.g.*, [0043]
- Yu '671 (A-36) at, *e.g.*, [5:57-5:63]
- Yu '798 (A-37) at, *e.g.*, [12:61-13:2]

- Polymer Adhesives and Encapsulants for Microelectronic Applications (A-38) at, *e.g.*, 67–68
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, 3
- Copper Pillar Bumping Technology (A-40) at, *e.g.*, 1–3
- Embedded Glass Interposer for Heterogeneous Multi-Chip Integration (A-41) at, *e.g.*, 314–15
- The Requirement of Future Substrate - Maker Point of View - (A-42) at, *e.g.*, 22
- IPC-4761 Design Guide for Protection of Printed Board Via Structures (A-43) at, *e.g.*, 8
- Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module (A-44) at, *e.g.*, 96–97
- All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices (A-45) at, *e.g.*, 31, 33
- Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects (A-46) at, *e.g.*, 1336
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- Apple iPhone 4–6 (A-53)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to interconnect stacked package substrates would have recognized that such package substrates could be interconnected through metal pillars, such as metal vias, implemented in a spacer connector. Such a configuration was a well-known design choice in the semiconductor

packaging art, as it allowed manufacturers to improve electrical performance, reduce the size of a semiconductor package, decrease the interconnect length between mounted components, improve reliability at high temperatures, and reduce solder bridging.

The motivation to vertically stack a top package substrate and bottom package substrate using metal pillars, to achieve these benefits was known in the prior art at the time. *See, e.g.*, Sun (A-31) at [0015] (“Metal pillars allow for fine pitch and maintain their shape at high processing temperatures (e.g. 260° C), compared to solder joints which melt and break down at such temperatures”), [0066] (“for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections.”); Chen ’484 (A-4) at [0004] (“To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); [0005] (“as the packages tend to have smaller sizes and fine pitches, solder bridging easily occurs between the solder balls of the PoP structure, thus adversely affecting the product yield. Accordingly, copper pillars are formed to achieve a stand-off effect so as to prevent solder bridging.”); Hu ’083 (A-13) at [0004] (“it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity, and even causing position deviation of solder joints between the packages.... Furthermore, an increase in the volume of the solder balls can easily cause a solder bridge between the solder balls.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”). Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose package substrates interconnected using metal pillars implemented in a spacer connector.

See, e.g., Chen '402 (A-3) at (“Through-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34. Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like.”); Sun (A-31) at [0048], [0062], FIG. 13 (disclosing an upper PoP module stacked on a first module 110, with a second substrate 300 interposed therebetween, where the second substrate 300 includes “vias 390 extending through the second substrate 300”); Waite (A-33) at [10:2-10:5] (“Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.”); IPC-4761 Design Guide for Protection of Printed Board Via Structures (A-43) at 9 (disclosing a “via with a secondary metallized coating covering the via”).

As these exemplary teachings demonstrate, improving existing semiconductor packaging designs that are ready for improvement by interconnecting package substrates using metal pillars in a spacer connector was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way.

Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded decreased interconnection length, more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of decreasing interconnector length, improving reliability at high temperatures, and reducing solder bridging is of special interest or importance in the field. *See, e.g.*, Sun (A-31) at [0015] (“Metal pillars allow for fine pitch and maintain their shape at high processing temperatures (e.g. 260° C), compared to solder joints which melt and break down at such temperatures”), [0066] (“for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections.”); Chen ’484 (A-4) at [0004] (“To improve electrical

performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); [0005] (“as the packages tend to have smaller sizes and fine pitches, solder bridging easily occurs between the solder balls of the PoP structure, thus adversely affecting the product yield. Accordingly, copper pillars are formed to achieve a stand-off effect so as to prevent solder bridging.”); Hu ’083 (A-13) at [0004] (“it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity, and even causing position deviation of solder joints between the packages.... Furthermore, an increase in the volume of the solder balls can easily cause a solder bridge between the solder balls.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”).

4. Metal Pads

Claim 1 of the ’202 patent recites “a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.” *See, e.g.*, ’202 patent, Claim 1. Claims 2–4, 6, and 9 each depend from Claim 1, and therefore incorporate these limitations. Claim 9 of the ’202 patent recites “a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars.” *See, e.g.*, ’202 patent, Claim 9.

Nothing about the claimed, generic “top metal pads” or “bottom metal pads” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of a “metal pad” was well known in the art before the alleged invention of the ’202 patent. To the extent any of the structural elements reciting a “top metal pad” or “bottom metal pad” is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding

Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, [0038-0039]
- Berry (A-2) at, *e.g.*, [7:17-7:44]
- Chen '402 (A-3) at, *e.g.*, [0010-0011], [0017]
- Chen '484 (A-4) at, *e.g.*, [0047]
- Dunne (A-6) at, *e.g.*, [7:58-7:64]
- Furuta '669 (A-7) at, *e.g.*, [8:48-8:67]
- Furuta '415 (A-8) at, *e.g.*, [0034-0038]
- Ganesan (A-9) at, *e.g.*, [2:62-3:27], [3:60-4:3]
- Hsu '142 (A-10) at, *e.g.*, [0046-0048]
- Hsu '559 (A-11) at, *e.g.*, [6:29-6:46]
- Hu '687 (A-12) at, *e.g.*, [0034], [0036]
- Hu '083 (A-13) at, *e.g.*, [0030]
- Hu '659 (A-14) at, *e.g.*, [10:57-11:3]
- Huemoeller (A-15) at, *e.g.*, [16:19-16:55]
- Jung (A-16) at, *e.g.*, [0271-0272]
- Kurashima (A-18) at, *e.g.*, [0071]
- Lee (A-19) at, *e.g.*, [5:38-5:59], [6:48-7:8]
- Leung (A-20) at, *e.g.*, [3:56-3:61]
- Lin (A-21) at, *e.g.*, [33:50-33:59]
- Lisk (A-22) at, *e.g.*, [0032-0033]
- Liu (A-23) at, *e.g.*, 3-4
- Love (A-24) at, *e.g.*, [12:42-12:59]
- Muthukumar (A-25) at, *e.g.*, [0026]
- Nakatani (A-26) at, *e.g.*, [0081-0082], [0092-0093]
- Peters (A-27) at, *e.g.*, [9:45-9:55]
- Savastiouk '170 (A-28) at, *e.g.*, [3:57-4:8]
- Savastiouk '636 (A-29) at, *e.g.*, [0033-0035]
- Shuto (A-30) at, *e.g.*, [3:13-3:25], [7:23-7:27]

- Sun (A-31) at, *e.g.*, [0062-0063]
- Takeda (A-32) at, *e.g.*, [0035], [0043]
- Waite (A-33) at, *e.g.*, [10:2-10:5]
- Wu (A-34) at, *e.g.*, [2:38-2:45]
- Yoo (A-35) at, *e.g.*, [0043-0044]
- Polymer Adhesives and Encapsulants for Microelectronic Applications (A-38) at, *e.g.*, 62, 67–68
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, 4
- Copper Pillar Bumping Technology (A-40) at, *e.g.*, 1–3
- Embedded Glass Interposer for Heterogeneous Multi-Chip Integration (A-41) at, *e.g.*, 315
- The Requirement of Future Substrate - Maker Point of View - (A-42) at, *e.g.*, 22
- IPC-4761 Design Guide for Protection of Printed Board Via Structures (A-43) at, *e.g.*, 9
- Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module (A-44) at, *e.g.*, 55–56
- All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices (A-45) at, *e.g.*, 51–53
- Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects (A-46) at, *e.g.*, 1336
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)
- Preci-Dip PCB Connectors
- Mill-Max PCB Connectors

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to implement a metal pillar would have known that top and/or bottom metal

pads could be applied to such a metal pillar. Such a configuration was a well-known design choice in the semiconductor packaging art, as it allowed manufacturers to facilitate a reliable electrical connection between metal pillars, reduce misalignment tolerances during manufacturing, and prevent contaminants from damaging metal pillars.

The motivation to apply top metal pads to metal pillars to facilitate a reliable electrical connection between the metal pillars and bottom metal pillars and top metal pillars, reduce misalignment tolerances during manufacturing, and prevent contaminants from damaging metal pillars was known in the prior art at the time. *See, e.g.*, Love (A-24) at 13:17–37 (“interconnect columns may be somewhat offset from an exact opposing relationship... Such an offset may occur during the construction of interconnect column 15d... base pad 20 of each interconnect columns 15a–15d is approximately 40 microns wide and the bottom end 17 is approximately 10 microns in diameter, thereby allowing a 15 micron misalignment error for each of interconnect columns 15a and 15b.”); IPC-4761 Design Guide for Protection of Printed Board Via Structures (A-43) at Table 5-1 (“Filled and Capped” vias provide the benefits of “[k]eeping chemistry or solder from passing through the via,” and “[p]revent[ing] migration of solder, adhesives, or encapsulants into vias”). Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose top metal pads. *See, e.g.*, Chen ’402 (A-3) at [0011] (“TAV modules 28 may include redistribution layer(s) that include redistribution lines and metal pads on the top sides of TAV modules 28.”); Love (A-24) at [7:32-7:36] (disclosing a “base pad 20); Sun (A-31) at [0066] (“A small amount of solder or bonding pads may used to connect the metal pillars to the respective other substrates.”); Waite (A-33) at 4:20–21 (disclosing “upper contact pads 308 of the first spacer-connector 204”) IPC-4761 Design Guide for Protection of Printed Board Via Structures (A-43) at 9 (disclosing “Filled and Capped” vias).

As these exemplary teachings demonstrate, improving existing semiconductor packaging designs that are ready for improvement by applying top metal pads and/or bottom metal pads to metal pillars was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded improved reliability or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to

combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of metal pillar interconnections is of special interest or importance in the field. *See, e.g.*, Love (A-24) at 13:17–37 (“interconnect columns may be somewhat offset from an exact opposing relationship... Such an offset may occur during the construction of interconnect column 15d... base pad 20 of each interconnect columns 15a–15d is approximately 40 microns wide and the bottom end 17 is approximately 10 microns in diameter, thereby allowing a 15 micron misalignment error for each of interconnect columns 15a and 15b.”); IPC-4761 Design Guide for Protection of Printed Board Via Structures (A-43) at Table 5-1 (“Filled and Capped” vias provide the benefits of “[k]eeping chemistry or solder from passing through the via,” and “[p]revent[ing] migration of solder, adhesives, or encapsulants into vias”).

5. Metal Pillars Protrude Downwardly from Core Substrate

Claim 1 of the '202 patent recites “wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.” *See, e.g.*, '202 patent, Claim 1. Claims 2–4, 6, and 9 each depend from Claim 1, and therefore incorporate these limitations.

Nothing about the claimed, generic “metal pillars,” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of a “metal pillar” which “protrudes downwardly from a bottom surface of the core substrate” was well known in the art before the alleged invention of the '202 patent. To the extent any of the structural elements reciting a “metal pillar” which “protrudes downwardly from a bottom surface of the core substrate” is not

explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Berry (A-2) at, *e.g.*, [7:13-7:39]
- Chen '402 (A-3) at, *e.g.*, [0009-0010]
- Dunne (A-6) at, *e.g.*, [2:41-2:51]
- Furuta '669 (A-7) at, *e.g.*, [8:39-8:56]
- Furuta '415 (A-8) at, *e.g.*, [0037]
- Ganesan (A-9) at, *e.g.*, [3:25-3:37]
- Hu '659 (A-14) at, *e.g.*, [8:5-8:15]
- Savastiouk '170 (A-28) at, *e.g.*, [4:45-4:48]
- Savastiouk '636 (A-29) at, *e.g.*, [0027-0028]
- Shuto (A-30) at, *e.g.*, [3:13-3:25]
- Sun (A-31) at, *e.g.*, [0062-0065], FIG. 13
- Yoo (A-35) at, *e.g.*, [0043-0044]
- Polymer Adhesives and Encapsulants for Microelectronic Applications (A-38) at, *e.g.*, 67–68
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, 3, 5, FIGs. 4, 9.
- Embedded Glass Interposer for Heterogeneous Multi-Chip Integration (A-41) at, *e.g.*, 314–15
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Through Mold Via (TMV) PoP (A-51)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example,

a POSITA seeking to interconnect stacked package substrates would have recognized that such package substrates could be interconnected using metal pillars implemented in a spacer connector, which would protrude below the bottom surface of a core substrate of the spacer connector, such that they make contact with top metal pillars of a bottom substrate. Such a configuration was a well-known design choice in the semiconductor packaging art, as it allowed manufacturers to improve electrical performance, reduce the size of a semiconductor package, decrease the interconnect length between mounted components, and facilitate the connection between the metal pillars and the bottom substrate.

The motivation to vertically stack a top package substrate and bottom package substrate to improve electrical performance, reduce the size of a semiconductor package, decrease the interconnect length between mounted components, and facilitate the connection between the metal pillars and the bottom substrate was known in the prior art at the time. *See, e.g.*, Chen '484 (A-4) at [0004] (“To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”). Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose package substrates interconnected using metal pillars implemented in a spacer connector. *See, e.g.*, Chen '402 (A-3) at (“through-substrate vias 32 protrude above the back surface of substrate 34”); Sun (A-31) at [0048], [0062], FIGs. 13, 15 (disclosing an upper PoP module stacked on a first module 110, with a second substrate 300 interposed therebetween, where the second substrate 300 includes “vias 390 extending through the second substrate 300” and protruding below a bottom surface of a core substrate).

As these exemplary teachings demonstrate, improving existing semiconductor packaging designs that are ready for improvement by interconnecting package substrates using metal pillars implemented in a spacer connector, which protrude below the bottom surface of a core substrate, was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded decreased interconnection length, more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding

Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of decreasing interconnector length is of special interest or importance in the field. *See, e.g.*, Chen '484 (A-4) at [0004] (“To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”).

6. Bottom Metal Pillars and Top Metal Pillars

Claim 1 of the '202 patent recites “the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,” and “the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.” *See, e.g.*, '202 patent, Claim 1. Claims 2–4, 6, and 9 each depend from Claim 1, and therefore incorporate these limitations.

Nothing about the claimed, generic “bottom metal pillars” or “top metal pillars,” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of “bottom metal pillars” and “top metal pillars” was well known in the art before the alleged invention of the '202 patent. To the extent any of the structural elements reciting “bottom metal

pillars” or “top metal pillars” is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, [0045], [0058]
- Berry (A-2) at, *e.g.*, [8:29-8:41], [10:56-11:1]
- Chen '402 (A-3) at, *e.g.*, [0019]
- Chen '484 (A-4) at, *e.g.*, [0052], [0059-0063]
- Daizo (A-5) at, *e.g.*, [3:12-3:19]
- Furuta '669 (A-7) at, *e.g.*, [7:40-7:55]
- Furuta '415 (A-8) at, *e.g.*, [0020-0021]
- Ganesan (A-9) at, *e.g.*, [3:22-3:30], [3:37-3:39]
- Hsu '142 (A-10) at, *e.g.*, [0046-0048]
- Hsu '559 (A-11) at, *e.g.*, [2:50-2:63], [6:29-6:46]
- Hu '687 (A-12) at, *e.g.*, [0038]
- Hu '083 (A-13) at, *e.g.*, [0037]
- Huemoeller (A-15) at, *e.g.*, [16:19-16:55]
- Jung (A-16) at, *e.g.*, [0266-0271]
- Kim (A-17) at, *e.g.*, [0037]
- Kurashima (A-18) at, *e.g.*, [0061-0067]
- Lee (A-19) at, *e.g.*, [6:12-6:31], [9:46-9:55]
- Leung (A-20) at, *e.g.*, [3:56-3:61]
- Lisk (A-22) at, *e.g.*, [0032], [0034]
- Liu (A-23) at, *e.g.*, 3–4
- Love (A-24) at, *e.g.*, [12:4-12:28], [13:12-13:39]
- Nakatani (A-26) at, *e.g.*, [0092-0093]
- Peters (A-27) at, *e.g.*, [7:36-7:46], [12:65-13:27]
- Savastiouk '636 (A-29) at, *e.g.*, [0025-0027]
- Shuto (A-30) at, *e.g.*, [5:7-5:21], [6:8-6:24]
- Sun (A-31) at, *e.g.*, [0048], [0059]

- Waite (A-33) at, *e.g.*, [4:19-4:26]
- Wu (A-34) at, *e.g.*, [3:45-4:8], [4:58-4:67]
- Yoo (A-35) at, *e.g.*, [0069-0072]
- Yu '671 (A-36) at, *e.g.*, [13:14-13:28]
- Yu '798 (A-37) at, *e.g.*, [6:11-6:30], [9:4-9:32]
- Polymer Adhesives and Encapsulants for Microelectronic Applications (A-38) at, *e.g.*, 62, 68
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, 1–3
- Copper Pillar Bumping Technology (A-40) at, *e.g.*, 2–3
- Embedded Glass Interposer for Heterogeneous Multi-Chip Integration (A-41) at, *e.g.*, 315
- The Requirement of Future Substrate - Maker Point of View - (A-42) at, *e.g.*, 2, 23
- Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module (A-44) at, *e.g.*, 98–101
- All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices (A-45) at, *e.g.*, 50–54
- Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects (A-46) at, *e.g.*, 1336
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- Apple iPhone 4–6 (A-53)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to interconnect a top package substrate and bottom package substrate would

have recognized that metal pillars could be applied to the top package substrate and bottom package substrate, to facilitate such an interconnection. Such a configuration was a well-known design choice in the semiconductor packaging art, as it allowed for reduced pitch between electrical connectors, improved reliability at high temperatures, and reduced solder bridging.

The motivation to apply bottom metal pillars and top metal pillars to achieve these benefits was known in the prior art at the time. *See, e.g.*, Sun (A-31) at [0015] (“Metal pillars allow for fine pitch and maintain their shape at high processing temperatures (e.g. 260° C), compared to solder joints which melt and break down at such temperatures”), [0066] (“for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections.”); Chen ’484 (A-4) at [0005] (“as the packages tend to have smaller sizes and fine pitches, solder bridging easily occurs between the solder balls of the PoP structure, thus adversely affecting the product yield. Accordingly, copper pillars are formed to achieve a stand-off effect so as to prevent solder bridging.”); Hu ’083 (A-13) at [0004] (“it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity, and even causing position deviation of solder joints between the packages.... Furthermore, an increase in the volume of the solder balls can easily cause a solder bridge between the solder balls.”).

Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose bottom metal pillars and top metal pillars. *See, e.g.*, Hu ’083 (A-13) at [0037] (“package 3 is bonded to the first and second external connection structures 27 a, 27 b”); Love (A-24) at 6:63–66 (“Structure 10 comprises substrate 12 and an interconnect column 15, which includes an electrically conductive post 14 disposed on a first surface 13 of substrate 12.”); Sun (A-31) at

[0059], [0066], FIG. 14(a) (disclosing “second metal connectors 310” and “first metal connectors 320”); Waite (A-33) at [4:19-4:26] (disclosing “multiple conductive elements 302 of the first conductive elastomer 206”).

As these exemplary teachings demonstrate, improving existing semiconductor packaging designs that are ready for improvement by implementing bottom metal pillars and top metal pillars was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded decreased interconnection length, more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for

achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of metal pillar interconnects is of special interest or importance in the field. *See, e.g.*, Sun (A-31) at [0015] (“Metal pillars allow for fine pitch and maintain their shape at high processing temperatures (e.g. 260° C), compared to solder joints which melt and break down at such temperatures”), [0066] (“for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections.”); Chen ’484 (A-4) at [0005] (“as the packages tend to have smaller sizes and fine pitches, solder bridging easily occurs between the solder balls of the PoP structure, thus adversely affecting the product yield. Accordingly, copper pillars are formed to achieve a stand-off effect so as to prevent solder bridging.”); Hu ’083 (A-13) at [0004] (“it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity, and even causing position deviation of solder joints between the packages.... Furthermore, an increase in the volume of the solder balls can easily cause a solder bridge between the solder balls.”).

7. Bottom Chip

Claim 1 of the '202 patent recites “a bottom chip arranged in the space between the bottom package substrate and the top package substrate” and “the bottom chip is mounted to the top surface of the bottom package substrate.” *See, e.g.*, '202 patent, Claim 1. Claims 2–4, 6, and 9 each depend from Claim 1, and therefore incorporate these limitations.

Nothing about the claimed, generic “bottom chip” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of “a bottom chip arranged in the space between the bottom package substrate and the top package substrate,” where “the bottom chip is mounted to the top surface of the bottom package substrate” was well known in the art before the alleged invention of the '202 patent. To the extent any of the structural elements reciting such a “bottom chip” is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, [0073-0075]
- Berry (A-2) at, *e.g.*, [6:43-6:48]
- Chen '402 (A-3) at, *e.g.*, [0018], [0020]
- Chen '484 (A-4) at, *e.g.*, [0047], [0052]
- Daizo (A-5) at, *e.g.*, [2:11-2:17], [2:40-2:53]
- Dunne (A-6) at, *e.g.*, [9:19-9:34]
- Furuta '669 (A-7) at, *e.g.*, [3:1-3:6], [9:40-9:45]
- Furuta '415 (A-8) at, *e.g.*, [0020], [0040]
- Ganesan (A-9) at, *e.g.*, [1:35-1:41], [4:55-4:57]
- Hsu '142 (A-10) at, *e.g.*, [0048]
- Hsu '559 (A-11) at, *e.g.*, [2:50-2:63], [4:34-4:58]
- Hu '687 (A-12) at, *e.g.*, [0033], [0036]
- Hu '083 (A-13) at, *e.g.*, [0036-0037]

- Hu '659 (A-14) at, *e.g.*, [6:32-6:43]
- Huemoeller (A-15) at, *e.g.*, [6:53-6:63], [16:25-16:55]
- Jung (A-16) at, *e.g.*, [0266], [0270-0271]
- Kim (A-17) at, *e.g.*, [0039]
- Kurashima (A-18) at, *e.g.*, [0048], [0108-0115]
- Lee (A-19) at, *e.g.*, [6:1-6:13], [5:31-5:43]
- Leung (A-20) at, *e.g.*, [1:29-1:63], [3:24-3:28]
- Lin (A-21) at, *e.g.*, [42:48-42:62]
- Lisk (A-22) at, *e.g.*, [0031-0032]
- Liu (A-23) at, *e.g.*, 3–4
- Love (A-24) at, *e.g.*, [11:4-11:30]
- Muthukumar (A-25) at, *e.g.*, [0054]
- Nakatani (A-26) at, *e.g.*, [0092-0093]
- Peters (A-27) at, *e.g.*, [7:36-7:46]
- Savastiouk '170 (A-28) at, *e.g.*, [3:52-3:56]
- Savastiouk '636 (A-29) at, *e.g.*, [0008]
- Shuto (A-30) at, *e.g.*, [3:13-3:25]
- Sun (A-31) at, *e.g.*, [0047], [0058-0059]
- Waite (A-33) at, *e.g.*, [7:1-7:6]
- Wu (A-34) at, *e.g.*, [4:43-4:53]
- Yoo (A-35) at, *e.g.*, [0069-0072]
- Yu '671 (A-36) at, *e.g.*, [8:27-8:38]
- Yu '798 (A-37) at, *e.g.*, [3:64-3:68]
- Polymer Adhesives and Encapsulants for Microelectronic Applications (A-38) at, *e.g.*, 60
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, 2, 4
- Copper Pillar Bumping Technology (A-40) at, *e.g.*, 1–3
- Embedded Glass Interposer for Heterogeneous Multi-Chip Integration (A-41) at, *e.g.*, 315
- The Requirement of Future Substrate - Maker Point of View - (A-42) at, *e.g.*, 2, 23

- Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module (A-44) at, *e.g.*, 32–33
- All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices (A-45) at, *e.g.*, 71–72
- Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects (A-46) at, *e.g.*, 1336
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Apple iPhone 1 (A-50)
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- Apple iPhone 4–6 (A-53)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to interconnect mounted components would have recognized that a bottom chip could be mounted on a bottom package substrate and connected to a top chip mounted on a top package substrate, which is stacked on top of the bottom package substrate (i.e., the package substrates are vertically stacked). Such a configuration was a well-known design choice in the semiconductor packaging art, as it allowed manufacturers to improve electrical performance, reduce the size of a semiconductor package, and decrease the interconnect length between mounted components.

The motivation to mount a bottom chip on the bottom package substrate, such that the bottom chip is arranged in the space between the bottom package substrate and the top package substrate, to improve electrical performance, reduce the size of a semiconductor package and

decrease the interconnect length between the bottom chip and components mounted on the top package substrate (i.e., top chips) was known in the prior art at the time. *See, e.g.*, Chen '484 (A-4) at [0004] (“To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”); Waite (A-33) at [7:1-7:6] (“cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”). Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose such a configuration. *See, e.g.*, Chen (A-3) at [0009] (disclosing a “package component 24”); Hu '083 (A-13) at [0035]–[0037] (disclosing a “semiconductor chip 28”); Sun (A-31) at [0048] (“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200”); Waite (A-33) at [7:1-7:6] (“cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”).

As these exemplary teachings demonstrate, mounting a bottom chip on the bottom package substrate was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or

combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded decreased interconnection length, more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile,

and more reliable semiconductor packaging structures, and knowledge that the art of decreasing interconnection length is of special interest or importance in the field. *See, e.g.*, Chen '484 (A-4) at [0004] (“To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”); Waite (A-33) at [7:1-7:6] (“cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”).

8. Two Spacer Connectors Arranged on Opposite Sides of the Bottom Chip

Claim 1 of the '202 patent recites “the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.” *See, e.g.*, '202 patent, Claim 1. Claims 2–4, 6, and 9 each depend from Claim 1, and therefore incorporate this limitation.

Nothing about the claimed, generic “two spacer connectors arranged on opposite sides of the bottom chip,” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of “two spacer connectors arranged on opposite sides of the bottom chip” was well known in the art before the alleged invention of the '202 patent. To the extent any of the structural elements reciting “two spacer connectors arranged on opposite sides of the bottom chip” is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the

corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, [0078]
- Berry (A-2) at, *e.g.*, [7:1-7:12]
- Chen '402 (A-3) at, *e.g.*, [0012]
- Furuta '669 (A-7) at, *e.g.*, [7:17-7:39]
- Furuta '415 (A-8) at, *e.g.*, [0038]
- Ganesan (A-9) at, *e.g.*, FIG. 2
- Hsu '559 (A-11) at, *e.g.*, [6:29-6:46]
- Hu '687 (A-12) at, *e.g.*, [0037-0041]
- Hu '083 (A-13) at, *e.g.*, [0037]
- Kim (A-17) at, *e.g.*, [0039]
- Kurashima (A-18) at, *e.g.*, [0067]
- Muthukumar (A-25) at, *e.g.*, [0021]
- Sun (A-31) at, *e.g.*, [0048]
- Waite (A-33) at, *e.g.*, [6:59-7:6]
- Yoo (A-35) at, *e.g.*, [0069-0072]
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, 2, 5
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- Apple iPhone 4-6 (A-53)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to interconnect a top package substrate and a bottom package substrate would

have recognized that such a goal could be accomplished with two spacer connectors arranged on opposite sides of a bottom chip. Such a configuration was a well-known design choice in the semiconductor packaging art, as it allowed manufacturers to interconnect stacked package substrates while providing room for mounted components.

The motivation to interpose a vertically stacked top package substrate and bottom package substrate with two spacer connectors arranged on opposite sides of a bottom chip to interconnect stacked package substrates while providing room for mounted components was known in the prior art at the time. *See, e.g.*, Berry (A-2) at 13:56–61 (“the electronic component(s) 122 is/are oriented in respective voids or openings 331 of the interposer strip 330, each such opening 331 extending between the first and second segments 130a, 130b of a respective one of the interposers 130 within the interposer strip 330”); Ganesan (A-9) at 3:3–5 (“Planar interconnect stiffener 330 includes substrate 220 defining a recess 330 adapted to house die 170 of bottom device package 150.”); Sun (A-31) at [0048] (“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200”).

As these exemplary teachings demonstrate, improving existing semiconductor packaging designs that are ready for improvement by arranging two spacer connectors on opposite sides of a bottom chip was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed above involve well-established principles

of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of interconnecting package substrates is of special interest or importance in the field. *See, e.g.,* Berry (A-2) at 13:56–61 (“the electronic component(s) 122 is/are oriented in respective voids or openings 331 of the interposer strip 330, each such opening 331 extending between the first and second segments 130a, 130b of

a respective one of the interposers 130 within the interposer strip 330”); Ganesan (A-9) at 3:3–5 (“Planar interconnect stiffener 330 includes substrate 220 defining a recess 330 adapted to house die 170 of bottom device package 150.”); Sun (A-31) at [0048] (“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200”).

9. Top Chip Overlaps Bottom Chip and Spacer Connectors

Claim 3 of the ’202 patent recites “a top chip mounted to the top surface of the top package substrate” and “in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.” *See, e.g.*, ’202 patent, Claim 3.

Nothing about the claimed, generic “top chip” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of “a top chip mounted to the top surface of the top package substrate” where “in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors” was well known in the art before the alleged invention of the ’202 patent. To the extent any of the structural elements reciting such a “top chip” is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, [0078-0079], FIG. 11
- Chen ’402 (A-3) at, *e.g.*, [0019], FIG. 9
- Chen ’484 (A-4) at, *e.g.*, [0052], FIG. 3
- Furuta ’669 (A-7) at, *e.g.*, 9:40-9:45, FIG. 12
- Furuta ’415 (A-8) at, *e.g.*, [0040], FIG. 6

- Ganesan (A-9) at, *e.g.*, 1:35-1:41, FIG. 2
- Hsu '142 (A-10) at, *e.g.*, [0048], FIG. 9
- Hsu '559 (A-11) at, *e.g.*, [2:50-2:63], FIG. 1
- Kurashima (A-18) at, *e.g.*, [0108-0115], FIG. 11
- Lin (A-21) at, *e.g.*, [42:46-42:52], FIG. 12
- Muthukumar (A-25) at, *e.g.*, FIG. 1E
- Sun (A-31) at, *e.g.*, [0058-0059], FIG. 12
- SainSmart Board (A-49)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to shorten the interconnect length between mounted components would have recognized that a top chip could be mounted on a top package substrate and connected to a bottom chip mounted on a bottom package substrate, which is stacked below the top package substrate (i.e., the package substrates are vertically stacked). Such a configuration was a well-known design choice in the semiconductor packaging art, as it allowed manufacturers to improve electrical performance, reduce the size of a semiconductor package, and decrease the interconnect length between mounted components. Further, a POSITA would have recognized that a top chip could overlap a bottom chip and each of two spacer connectors. Such a configuration was a well-known design choice in the semiconductor packaging art, as larger chips can more easily be mounted on the top substrate of a semiconductor package, which has more available mounting area than the bottom substrate.

The motivation to mount a top chip on the top package substrate, such that the top chip is arranged above the bottom chip, to improve electrical performance, reduce the size of a semiconductor package, and decrease the interconnect length between the top chip and the bottom chip was known in the prior art at the time. *See, e.g.*, Chen '484 (A-4) at [0004] (“To improve

electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”); Waite (A-33) at [7:1-7:6] (“cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”). Further, the motivation to mount a large top chip on a top package substrate having sufficient mounting area, such that it overlaps a bottom chip and each of two spacer connectors on a bottom package substrate was known in the prior art at the time. *See e.g.*, Chen ’484 (A-4) at FIGs. 9, 12. Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose such a configuration. *See, e.g.*, Chen ’402 (A-3) at [0019], FIG. 9 (disclosing a “package component 62”); Sun (A-31) at [0048] (“an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.”); FIG. 12.

As these exemplary teachings demonstrate, mounting a top chip on the top package substrate and a bottom chip on the bottom package substrate was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed

above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded decreased interconnection length, more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of decreasing interconnection length is of special interest or importance in the field. *See, e.g.*, Chen '484 (A-4) at [0004] ("To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure."); Package-

Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”); Waite (A-33) at [7:1-7:6] (“cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.”).

10. Metal Pillars are Connected to Top Metal Pillars in an End-to-End Manner

Claim 6 of the '202 patent recites “the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate.” *See, e.g.*, '202 patent, Claim 6.

Nothing about the claimed, generic “metal pillars” or “top metal pillars” as recited in the above referenced claim, adds anything non-obvious over the prior art. The structure of a “metal pillar” being connected to a “top metal pillar” in an “end-to-end manner” was well known in the art before the alleged invention of the '202 patent. To the extent any of the structural elements reciting such a structure is not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Furuta '669 (A-7) at, *e.g.*, [9:1-9:15], FIG. 12
- Furuta '415 (A-8) at, *e.g.*, [0038], FIG. 6
- Hu '687 (A-12) at, *e.g.*, [0038-0039], FIG. 2E
- Hu '083 (A-13) at, *e.g.*, [0037], FIG. 3

- Sun (A-31) at, *e.g.*, [0062-0064], FIG. 13
- Waite (A-33) at, *e.g.*, [4:12-4:25], FIGs. 3, 4A
- All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices (A-45) at, *e.g.*, 53, FIG. 3.1
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)

A POSITA at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references for the reasons stated above. For example, a POSITA seeking to interconnect stacked package substrates would have recognized that such package substrates could be interconnected using metal pillars implemented in a spacer connector and top metal pillars implemented on a bottom package substrate in an end-to-end manner. Such a configuration was a well-known design choice in the semiconductor packaging art, as it allowed manufacturers to improve electrical performance, reduce the size of a semiconductor package, decrease the interconnect length between mounted components, and reduce solder bridging.

The motivation to vertically stack a top package substrate and bottom package substrate using metal pillars to achieve these benefits was known in the prior art at the time. *See, e.g.*, Sun (A-31) at [0015] (“Metal pillars allow for fine pitch and maintain their shape at high processing temperatures (*e.g.* 260° C), compared to solder joints which melt and break down at such temperatures”), [0066] (“for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections.”); Chen ’484 (A-4) at [0004] (“To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); [0005]

(“as the packages tend to have smaller sizes and fine pitches, solder bridging easily occurs between the solder balls of the PoP structure, thus adversely affecting the product yield. Accordingly, copper pillars are formed to achieve a stand-off effect so as to prevent solder bridging.”); Hu ’083 (A-13) at [0004] (“it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity, and even causing position deviation of solder joints between the packages.... Furthermore, an increase in the volume of the solder balls can easily cause a solder bridge between the solder balls.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”). Moreover, the references listed above, as demonstrated in the corresponding Appendices, disclose package substrates interconnected using metal pillars implemented in a spacer connector and top metal pillars on a bottom package substrate, wherein the metal pillars and top metal pillars are connected in an end-to-end manner. *See, e.g.*, Chen ’402 (A-3) at [0014] (“connectors 44 are formed to connect to metal posts 26 and 30”); Hu ’083 (A-13) at [0037] (“external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b”); Sun (A-31) at [0062], FIG. 13 (“[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320”); Waite (A-33) at [4:12–4:25] (“upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208”).

As these exemplary teachings demonstrate, improving existing semiconductor packaging designs that are ready for improvement by interconnecting package substrates using metal pillars in a spacer connector and top metal pillars on a bottom package substrate, in an end-to-end manner,

was known in the art and would yield predictable results. Such improvement would be a combination of prior art references according to known methods to yield predictable results. A POSITA would have had a reasonable expectation of success in making such modifications or combinations. Known techniques of semiconductor packaging design and manufacturing, such as those set forth in the prior art references cited above, would have been within the knowledge of a POSITA and would have sufficed to allow a POSITA to implement any such combination and where, as here, such combinations of references listed above involve well-established principles of semiconductor packaging in predictable, well-developed fields, thus the results of making the combinations would be predictable. Moreover, as all such systems are within the same field of endeavor, the combination would have been obvious to a POSITA because it is simply the use of a known technique to improve similar devices or systems in the same way. Moreover, such a combination would be predictable because each system and its components continue to function in the combination as it did separately.

In addition, a POSITA would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. For example, to the extent that market forces demanded decreased interconnection length, more compact form factors, improved reliability, or streamlined manufacturing processes, as discussed above, a POSITA would have thought to combine or modify references that described known techniques for achieving these objectives because such techniques offered improvements to existing semiconductor packaging structures. Further, as described above and in the corresponding Appendices, each of the references listed above describes techniques that were known to offer such improvements, and accordingly, a POSITA would have been motivated to combine the references. The teaching, suggestion, or motivation to modify or combine the references in the

manner claimed can be found in the explicit and/or implicit teachings of the references listed above, as identified in the corresponding Appendices, and the prior art as a whole, the general knowledge of POSITAs, including the knowledge of trends in the field toward faster, smaller, more versatile, and more reliable semiconductor packaging structures, and knowledge that the art of decreasing interconnector length, improving reliability at high temperatures, and reducing solder bridging is of special interest or importance in the field. *See, e.g.*, Sun (A-31) at [0015] (“Metal pillars allow for fine pitch and maintain their shape at high processing temperatures (e.g. 260° C), compared to solder joints which melt and break down at such temperatures”), [0066] (“for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections.”); Chen ’484 (A-4) at [0004] (“To improve electrical performances and save spaces, a plurality of packages can be vertically stacked on one another so as to form a package on package (PoP) structure.”); [0005] (“as the packages tend to have smaller sizes and fine pitches, solder bridging easily occurs between the solder balls of the PoP structure, thus adversely affecting the product yield. Accordingly, copper pillars are formed to achieve a stand-off effect so as to prevent solder bridging.”); Hu ’083 (A-13) at [0004] (“it is difficult to control deviation of the volume of the solder balls, thereby easily resulting in a tilted stack structure and poor coplanarity, and even causing position deviation of solder joints between the packages.... Furthermore, an increase in the volume of the solder balls can easily cause a solder bridge between the solder balls.”); Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at 5 (a “packaged die stack provides better electrical performance by reducing the interconnect length between the parts”).

11. Other Structural and Electrical Elements

In addition to the claim elements analyzed above, the Asserted Claims of the '202 patent further recite various generic structural and electrical limitations of the claimed socket structure, as summarized in the table below. Some Asserted Claims may have slight variations in claim language, which are not exhaustively listed below and do not change the analysis of the prior art.

Claim Language	Summary of Element	Asserted Claims
“A structure”	Structural – Structure	1
“the spacer connector comprises a core substrate”	Structural – Core substrate	1
“the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate”	Structural – Metal pillar connection	1
“the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip”	Structural – Spacer connector	1
“a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate”	Structural – Space between bottom chip and top package substrate	2
“each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate”	Structural – Metal pillar alignment	4
“bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector”	Structural – Metal pillar connection	6, 9
“the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package	Structural – Metal pillar connection	9

substrate via the corresponding bottom metal pads of the spacer connector”		
--	--	--

Nothing about these generic structural limitations that commonly exist in many existing semiconductor package structures at the time of the alleged invention of the '202 patent add anything non-obvious over the prior art. The basic structural configuration of package substrate interconnection using metal pillars was well-known in the field, well before the alleged inventions of the '202 patent. For example, Sun (A-31) discloses, among others things:

- “A structure” element – *see, e.g.*, Sun (A-31) at [0058] (“PoP assembly 1 comprising a second module 5 mounted on a first module 10”).
- “the spacer connector comprises a core substrate” element – *see, e.g.*, Sun (A-31) at [0016] (“the second substrate may comprise a core insulator layer and conducting layers on either side of the core layer. There may be insulating layers (e.g. solder resists) outward on either side of the conducting layers.”).
- “the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate” element – *see, e.g.*, Sun (A-31) at [0012]–[0013] (“the first substrate being electrically connected to the second substrate by at least one first electrical connector; and at least one second electrical connector extending from the second substrate through the overmold and having an exposed end for electrical connection to an external module.”); [0015] (“[p]referably there are a plurality of first electrical connectors and a plurality of second electrical connectors. For example, there may be four or more first electrical connectors on the underside of the second

- substrate and four or more second electrical connectors on the top side of the second substrate”); [0061] (“[t]he second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110”); [0063] (“[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320”); [0074] (“electrical contacts (e.g. bonding pads or lands) present on the second (lower) side of the third substrate are placed in contact with the exposed ends of the second electrical connectors 310 of the first module 10”).
- “the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip” element – *see, e.g.*, Sun (A-31) at [0061] (“[t]he second substrate 300 has an opening therein for accommodating the chips 200, 200a”); [0055] (“second substrate 300 is rectangular and has a rectangular opening 340 in the middle.... Each side has a gap 350. The gaps 350 are of different shapes and join the central opening 340.”); [0014] (“the opening in the second substrate makes room for one or more chips mounted to the first substrate.”).
 - “a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate” element – *see, e.g.*, Sun (A-31) at [0010] (“[i]t would be desirable to increase the vertical separation (stand off height) in order to make room for more and larger chips and enable stacking of chips on the lower substrate.”); [0014] (“[a]s the lower module has a second substrate with electrical connectors on either side, the stand off height may be increased. Further, the opening in the second substrate makes room for one or more chips mounted to the first substrate.”).
 - “each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of

- metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate” element – *see, e.g.*, Sun (A-31) at [0062] (“[t]he second metal connectors 310 are aligned with corresponding [first metal connectors 320] on the opposite side of the substrate 300.”); [0063] (“[v]ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.”).
- “bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector” element – *see, e.g.*, Sun (A-31) at FIG. 14(a).
 - “the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector” element – *see, e.g.*, Sun (A-31) at FIG. 13.

To the extent any of the structural elements recited in the Asserted Claims are not explicitly or inherently disclosed in a charted reference, such elements are disclosed and/or taught by each of the prior art references identified in the non-exhaustive list below and the corresponding Appendices, such that references in combination, in addition to the relevant teachings identified herein and/or charted, render the claim obvious.

- Arai (A-1) at, *e.g.*, FIG. 11
- Berry (A-2) at, *e.g.*, FIG. 1
- Chen ’402 (A-3) at, *e.g.*, FIG. 9
- Chen ’484 (A-4) at, *e.g.*, FIGs. 2F, 3
- Daizo (A-5) at, *e.g.*, FIG. 1
- Dunne (A-6) at, *e.g.*, FIG. 4

- Furuta '669 (A-7) at, *e.g.*, FIG. 12
- Furuta '415 (A-8) at, *e.g.*, FIG. 6
- Ganesan (A-9) at, *e.g.*, FIG. 2
- Hsu '142 (A-10) at, *e.g.*, FIG. 9
- Hsu '559 (A-11) at, *e.g.*, FIG. 2
- Hu '687 (A-12) at, *e.g.*, FIG. 2F
- Hu '083 (A-13) at, *e.g.*, FIG. 3
- Hu '659 (A-14) at, *e.g.*, FIG. 2I'
- Huemoeller (A-15) at, *e.g.*, FIG. 41
- Jung (A-16) at, *e.g.*, FIG. 44B
- Kim (A-17) at, *e.g.*, FIG. 3
- Kurashima (A-18) at, *e.g.*, FIG. 7B
- Lee (A-19) at, *e.g.*, FIG. 2
- Leung (A-20) at, *e.g.*, FIG. 2
- Lin (A-21) at, *e.g.*, FIG. 6
- Lisk (A-22) at, *e.g.*, FIG. 3A
- Liu (A-23) at, *e.g.*, 2–4
- Love (A-24) at, *e.g.*, FIG. 5
- Muthukumar (A-25) at, *e.g.*, FIG. 1E
- Nakatani (A-26) at, *e.g.*, FIG. 3
- Peters (A-27) at, *e.g.*, FIG. 1
- Savastiouk '170 (A-28) at, *e.g.*, FIG. 3
- Savastiouk '636 (A-29) at, *e.g.*, FIG. 3
- Shuto (A-30) at, *e.g.*, FIG. 1
- Sun (A-31) at, *e.g.*, FIGs. 12, 13, 15
- Takeda (A-32) at, *e.g.*, FIG. 11
- Waite (A-33) at, *e.g.*, FIG. 4A
- Wu (A-34) at, *e.g.*, FIG. 7
- Yoo (A-35) at, *e.g.*, FIG. 12
- Yu '671 (A-36) at, *e.g.*, FIG. 1K
- Yu '798 (A-37) at, *e.g.*, FIG. 8

- Polymer Adhesives and Encapsulants for Microelectronic Applications (A-38) at, *e.g.*, 59–63
- Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration (A-39) at, *e.g.*, FIGs. 2, 4, 6, 8
- Copper Pillar Bumping Technology (A-40) at, *e.g.*, 1–3
- Embedded Glass Interposer for Heterogeneous Multi-Chip Integration (A-41) at, *e.g.*, 314–316
- The Requirement of Future Substrate - Maker Point of View - (A-42) at, *e.g.*, 2, 22–23, 25
- IPC-4761 Design Guide for Protection of Printed Board Via Structures (A-43) at, *e.g.*, FIG. 5-8, Table 5-1
- Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module (A-44) at, *e.g.*, 32–33, 100–03, 106–07
- All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices (A-45) at, *e.g.*, 16–17, 19–20, 52–53
- Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects (A-46) at, *e.g.*, 1336–38
- Teensy Board (A-47)
- Seeed Board (A-48)
- SainSmart Board (A-49)
- Apple iPhone 1 (A-50)
- Through Mold Via (TMV) PoP (A-51)
- MCeP (A-52)
- Apple iPhone 4–6 (A-53)
- EIT Package-Interposer-Package (PIP) Test Vehicle (A-54)

A person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine the teachings of these references with the charted references because they arise from the same field of semiconductor packaging design and address closely related structural and functional problems. Each reference discloses improvements to known semiconductor

packaging interconnect structures—such as modifications to interconnect types and arrangements—aimed at improving connection pitch, reliability, or performance. Combining these teachings would have involved no more than the predictable use of known elements according to their established functions, resulting in a semiconductor package stack that operates in the same expected manner as its constituent parts. Thus, a POSITA would have found such combinations of available prior art to be a straightforward integration of already available design choices at the time within a mature and well-developed technical field, yielding expected and predictable results.

C. Knowledge of POSITA

To the extent that TopWire contends that any particular feature or element of the Asserted Claims is a novel aspect of the claimed subject matter, Samsung reserves the right to illustrate that the particular feature was widely known, understood, and implemented by POSITAs at the time of the alleged invention, and that it would have been obvious to combine and/or modify the prior art identified throughout these Invalidity Contentions with the knowledge of a POSITA. Samsung reserves the right to illustrate the knowledge of a POSITA using any of the prior art references identified throughout these Invalidity Contentions, expert testimony, learned treatises, and/or testimony of prior art fact witnesses.

D. No Secondary Considerations

As of the date these Invalidity Contentions were served, TopWire has not identified any secondary considerations of non-obviousness. Samsung reserves all rights to respond to any secondary considerations of non-obviousness raised by TopWire, including by updating, modifying, and/or adding to these Invalidity Contentions.

Samsung contends that there are no secondary considerations of non-obviousness evidencing the validity of any of the Asserted Claims. Secondary considerations of non-obviousness, also referred to as objective indicia of non-obviousness, “can include copying, long

felt but unsolved need, failure of others, commercial success, unexpected results created by the claimed invention, unexpected properties of the claimed invention, licenses showing industry respect for the invention, awards or other industry praise for the invention, and skepticism of skilled artisans before the invention.” *Power Integrations, Inc. v. Fairchild Semiconductor Int’l, Inc.*, 711 F.3d 1348, 1368 (Fed. Cir. 2013). “A nexus between the merits of the claimed invention and evidence of secondary considerations is required in order for the evidence to be given substantial weight in an obviousness decision.” *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 668 (Fed. Cir. 2000). Even when a nexus is found to exist, secondary considerations of non-obviousness “simply cannot overcome [a] strong prima facie showing of obviousness.” *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1368 (Fed. Cir. 2008).

TopWire has not identified or proven any objective indicia or secondary considerations of non-obviousness supporting the validity of any Asserted Claim. TopWire also has not established a nexus between any of the Asserted Claims and any alleged objective indicia or secondary considerations. Samsung reserves the right to supplement these invalidity contentions to respond to any such evidence should TopWire be permitted to raise them in the future. Further, while discovery in this case is ongoing and Samsung’s investigation continues (including via fact and expert discovery), to the extent TopWire alleges that one or more Asserted Claims are not obvious based on secondary considerations, Samsung contends such allegations are without merit.

Samsung also reserves the right to identify any of the art herein as evidence of simultaneous invention, which shows the obviousness of the Asserted Claims.

VII. GROUNDS FOR INVALIDITY UNDER 35 U.S.C. § 112

Samsung alleges that the Asserted Claims are invalid under 35 U.S.C. § 112 for failing to satisfy the written description and enablement requirements (§ 112, ¶ 1). Samsung reserves all rights to amend its Invalidity Contentions under 35 U.S.C. § 112, including after the Asserted

Claims are ultimately construed by the Court, in response to any interpretation of the Asserted Claims embodied in TopWire’s infringement positions, and/or to account for any changes in the law concerning invalidity under 35 U.S.C. § 112. Samsung also reserves the right to provide additional explanation and/or argument for its Invalidity Contentions under § 112, including, for example, based on expert testimony.

These contentions shall not be construed as an admission that any claim construction advanced by Samsung in this case is in any way inconsistent, flawed or erroneous. Nor should these contentions prevent Samsung from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to TopWire’s purported construction of the claim language or of other positions advanced by TopWire during the course of this litigation.

Samsung provides below its preliminary invalidity contentions under § 112.

1. Legal Standard

35 U.S.C. § 112 includes an enablement requirement: “The specification shall contain a written description . . . of the manner and process of making and using [the invention] in such full, clear, concise and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same.” 35 U.S.C. § 112, ¶ 1.

To satisfy the enablement requirement, the disclosure “must teach those skilled in the art how to make and use the full scope of the claimed invention without ‘undue experimentation.’” *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1366 (Fed. Cir. 1997); *MagSil Corp. v. Hitachi Glob. Storage Techs., Inc.*, 687 F.3d 1377, 1381 (Fed. Cir. 2012); *Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 999 (Fed. Cir. 2008). Moreover, “[i]t is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of an invention in order to constitute adequate enablement.” *Genentech, Inc.*, 108 F.3d at 1366. “If, by following the steps set forth in

the specification, one of ordinary skill in the art is not able to replicate the claimed invention without undue experimentation, the claim has not been enabled as required by 112, paragraph 1.” *National Recovery Tech., Inc. v. Magnetic Separation Syst., Inc.*, 166 F.3d 1190, 1196 (Fed. Cir. 1990). Similarly, if a specification teaches away from a substantial portion of the claim, or otherwise does not enable the full scope of the claim, there is no enablement. *AK Steel Corp. v. Sollac*, 344 F.3d 1234 (Fed. Cir. 2003); *see also MagSil Corp.*, 687 F.3d at 1383-84 (Fed. Cir. 2012).

35 U.S.C. § 112 further includes a written description requirement: “The specification shall contain a written description of the invention” 35 U.S.C. § 112, ¶ 1. “To satisfy the written description requirement, a patent applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention.” *ICU Medical, Inc. v. Alaris Medical Systems, Inc.*, 558 F.3d 1368, 1377 (Fed. Cir. 2009) (internal quotation marks and citations omitted); *see also Synthes USA, LLC v. Spinal Kinetics, Inc.*, 734 F.3d 1332, 1340 (Fed. Cir. 2013). “The test [for written description support] requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed.” *Ariad Pharmaceuticals, Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc).

The specification must describe the claimed invention in sufficient detail so that a POSITA can recognize what is claimed. “The appearance of mere indistinct words in a specification or a claim, even an original claim, does not necessarily satisfy that requirement.” *University of Rochester v. G.D. Searle & Co.*, 358 F.3d 916, 923 (Fed. Cir. 2004) (internal quotation marks and citations omitted).

2. Invalidity Argument

The identified grounds noted below both individually and collectively render the Asserted Claims of the '202 patent invalid under the statutory requirements of § 112. By identifying certain claim language below, Samsung does not imply that such language is entitled to any patentable weight when comparing the claim as a whole to the prior art.

a. Lack of Written Description

The Asserted Claims of the '202 patent are invalid for failure to comply with the written description requirement under § 112, ¶ 1. For example, the '202 patent does not contain written description support at least for the following claim terms, either individually or collectively, particularly as TopWire is asserting the claims for purposes of infringement, rendering the Asserted Claims in which they appear (and any claims depending therefrom) invalid for lack of written description:

Claim Terms	Asserted Claims
“end-to-end manner”	6
“top metal pillar”	1, 4, 6, 9
“bottom metal pillar”	1, 4, 6, 9
“top package substrate”	1–4, 6, 9
“bottom package substrate”	1, 3–4, 6, 9
“bottom metal pillars of the top package substrate”	1, 4, 6, 9
“top metal pillars of the bottom package substrate”	1, 4, 6, 9

At least under TopWire’s apparent interpretation and application of the Asserted Claims, the '202 patent does not provide sufficient written description support for the above claim terms. For example, at least under TopWire’s apparent interpretation and application of the Asserted Claims, the specification does not adequately describe a “top metal pillar” or “bottom metal pillar”

to demonstrate the inventor’s possession of the full scope of the claim. Indeed, nothing in the specification supports or suggests that the claimed metal pillars could encompass a solder structure. Similarly, the specification does not adequately describe a “bottom package substrate” or “top package substrate” to demonstrate the inventor’s possession of the full scope of the claim, at least under TopWire’s apparent interpretation, which encompass a printed circuit board assembly.

Accordingly, Asserted Claims 1, 3–4, 6, and 9 are invalid for lack of written description.

b. Lack of Enablement

The Asserted Claims of the ’202 patent are also invalid for failure to comply with the enablement requirement under § 112, ¶ 1. For example, the ’202 patent fails to provide an enabling disclosure with respect to the following claim terms, either individually or collectively, particularly as TopWire is asserting the claims for purposes of infringement, rendering the Asserted Claims in which they appear (and any claims depending therefrom) invalid for lack of enablement:

Claim Terms	Asserted Claims
“metal pillar”	1, 4, 6, 9
“top package substrate”	1–4, 6, 9
“bottom package substrate”	1, 3–4, 6, 9
“bottom metal pillars of the top package substrate”	1, 4, 6, 9
“top metal pillars of the bottom package substrate”	1, 4, 6, 9
“end-to-end manner”	6

At least under TopWire’s apparent interpretation and application of the Asserted Claims, the ’202 patent does not enable the above claim terms. For example, at least under TopWire’s apparent interpretation and application of the Asserted Claims, the specification does not adequately enable a POSITA to construct a “metal pillar,” “top package substrate,” “bottom

package substrate,” “bottom metal pillar of the top package substrate,” or “top metal pillar of the bottom package substrate.” Moreover, the specification does not provide enablement for the full scope of the claims to the extent the scope of the claims is interpreted to cover the accused embodiments, which are not described or enabled in the specification.

Accordingly, all Asserted Claims are invalid for lack of enablement.

VIII. ADDITIONAL INVALIDITY CONTENTIONS

Samsung has identified other invalidity defenses, which are outside the scope of Patent Rule 3-3, and are set forth in Samsung’s initial disclosures. Samsung will identify all bases upon which the Asserted Claims are invalid and/or unenforceable, as discovery proceeds. Samsung reserves the right to amend or supplement these Invalidity Contentions to address any additional invalidity arguments that become apparent in view of any relevant facts and information revealed during the course of discovery. Samsung expressly reserves the right to assert that the Asserted Patent is invalid under 35 U.S.C. § 102(f) in the event Samsung obtains evidence that the named inventor of the Asserted Patent did not invent the subject matter claimed in the Asserted Patent, or alternatively other inventor(s) contributed to the subject matter claimed in the Asserted Patent but were not included as named inventors of the Asserted Patent.

IX. DOCUMENT PRODUCTION AND ACCOMPANYING INVALIDITY CONTENTIONS

Documents required to be produced under the Docket Control Order (Dkt. No. 21) and Patent Local Rule 3-4 are being produced to TopWire under a separate letter or will be made available for inspection. By way of example, Samsung has separately produced documents or produces concurrently with service of these Invalidity Contentions prior art references and materials at SAMS.TopWire.003871–SAMS.TopWire.0005477. Samsung reserves the right to produce and rely on additional documents relating to their products in view of additional discovery.

Dated: May 21, 2026

Respectfully submitted,

/s/ Neil P. Sirota

Neil P. Sirota

neil.sirota@bakerbotts.com

Frank Zhu

frank.zhu@bakerbotts.com

Pilseon Yoo

pilseon.yoo@bakerbotts.com

Coleman Strine

coleman.strine@bakerbotts.com

BAKER BOTTS L.L.P.

30 Rockefeller Plaza, Ste 4340

New York, NY 10112-4498

Phone: 212.408.2500

Fax: 212.408.2501

Melissa R. Smith

Texas State Bar No. 24001351

GILLAM & SMITH, LLP

303 South Washington Avenue

Marshall, Texas 75670

Phone: (903) 934-8450

Fax: (903) 934-9257

melissa@gillamsmithlaw.com

*Counsel for Defendants Samsung Electronics Co., Ltd.
and Samsung Electronics America, Inc.*

CERTIFICATE OF SERVICE

I hereby certify that on May 21, 2026, a true and correct copy of the foregoing document was served on all counsel of record via electronic mail.

Dated: May 21, 2026

Respectfully submitted,

/s/ Neil P. Sirota
Neil P. Sirota

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

U.S. Patent Publication No. 20080155820 (“Arai”) is titled Wiring Substrate, Manufacturing Method Thereof, and Semiconductor Device and lists Tadashi Arai and Toshio Kobayashi as inventors. Arai is assigned to Shinko Electric Industries Co., Ltd. Arai anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Arai is a U.S. patent publication that was filed November 13, 2007 and published July 3, 2008. Arai is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Arai, or otherwise rendered obvious by disclosures and teachings of Arai, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Arai does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Arai with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Arai, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Arai “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

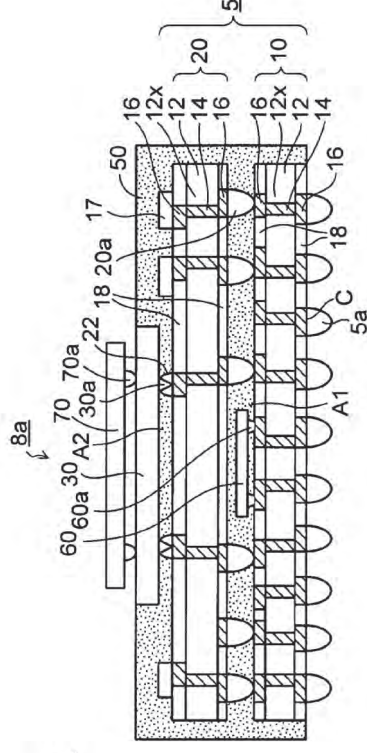
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Arai or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Arai set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Arai discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“The present invention relates to a wiring substrate which includes a base wiring board constructed by stacking a plurality of unit wiring boards each having wiring patterns which enable an electrical connection between upper and lower sides, in a state that the plurality of unit wiring boards are connected to each other via a connection terminal, a silicon interposer which is stacked on the base wiring board, and having wiring patterns which enable an electrical connection between upper and lower sides, and connected to the wiring patterns of the base wiring board via a connection terminal, and a resin portion which is filled in a gap</p>

	<p>between the plurality of unit wiring boards as well as a gap between the base wiring board and the silicon interposer, and which integrates the base wiring board and the silicon interposer.” Arai, [0014].</p> <p>“As shown in FIG. 7, in the interposer built-in wiring substrate 7 according to this embodiment, the second unit wiring board 20 is stacked to be connected to the first unit wiring board 10 in the thickness direction to construct the base wiring board 5. In the first unit wiring board 10, the wiring patterns 16 are formed on both surface sides of the insulating layer 12, and the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12. Furthermore, the solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12. In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed, on both surface sides of the insulating layer 12, to be connected to each other via the through-hole-conductive layers 14. The solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12. In addition, the capacitor components 17 are mounted to be connected to the wiring pattern 16 on the upper surface of the second unit wiring board 20. Furthermore, the connection terminals 20 a are disposed on the connection parts of the wiring patterns 16 on the lower surface side of the insulating layer 12. Subsequently, the connection terminals 20 a of the second unit wiring board 20 are joined to be electrically connected to the connection parts of the wiring patterns 16 of the first unit wiring board 10.” Arai, [0057-0060].</p>
--	---

FIG. 11



Arai, FIG. 11

“Moreover, as in an interposer built-in substrate 7 a shown in FIG. 8, solder balls or the like may be mounted on the connection parts C of the wiring patterns 16 on the lower surface side of the interposer built-in wiring substrate 7 of FIG. 7 to provide external connection terminals 5 a, whereby the interposer built-in substrate 7 may be used as a BGA (Ball Grid Array) type.” Arai, [0072].

“FIG. 9 shows an interposer built-in wiring substrate 7 b according to a modification of this embodiment. In the interposer built-in wiring substrate 7 b according to the modification, bumps 60 of a semiconductor chip 60 (LSI chip) are connected by flip-chip bonding to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10 of the interposer built-in wiring substrate 7 a of FIG. 8. The semiconductor chip 60 is embedded in the resin portion 50. A gap between the first unit wiring board 10 and the semiconductor chip 60 is also filled with the resin portion 50. The semiconductor chip 60 is housed in a space which is formed to have a height corresponding to that of the connection

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>terminal 20 a of the second unit wiring board 20. The semiconductor chip 60 is sealed with the resin portion 50.” Arai, [0073-0074].</p> <p>“FIG. 10 shows a semiconductor device 8 according to this embodiment. The semiconductor device 8 is constructed in a way that bumps 70 a of a semiconductor chip 70 (LSI chip) are mounted to be connected by flip-chip bonding to the connection parts of the wiring patterns 36 (FIG. 4) on the upper surface of the silicon interposer 30 of the interposer built-in wiring substrate 7 a of FIG. 8. The capacitor components 17 mounted on the base wiring board 5 are connected between a power line and a ground line of the semiconductor chip 70, and serves as decoupling capacitors.” Arai, [0075].</p> <p>“FIG. 11 shows a semiconductor device 8 a according to a modification of the embodiment of the present invention. As shown in FIG. 11, the semiconductor device 8 a according to the modification is constructed in such a way that the bumps 70 a of the semiconductor chip 70 are connected by flip-chip bonding to the interposer 30 of the interposer built-in wiring substrate 7 b of FIG. 9.” Arai, [0078-0079].</p>
[1.A] a bottom package substrate;	<p>Arai discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the first unit wiring board 10, through-holes 12 x are formed in an insulating layer 12 which is made of, for example, an epoxy resin (prepreg), or the like, containing glass fabrics. Each through-hole 12 x is filled with a through-hole-conductive layer 14 which is made of copper or the like. Furthermore, on both surface sides of the insulating layer 12, wiring patterns 16 made of copper or the like are formed. The wiring patterns 16 on both surface</p>

	<p>sides are connected to each other via the through-hole-conductive layer 14. In addition, solder resists 18 having openings are formed on both surface sides of the insulating layer 12, and the openings are provided on the connection parts of the wiring patterns 16.” Arai, [0037-0038].</p> <p>FIG. 11</p> <p>Arai, FIG. 11</p> <p>“Subsequently, as shown in FIG. 2, the second unit wiring board 20 is disposed on the first unit wiring board 10 so that the connection terminals 20 a of the second unit wiring board 20 can match the connection parts of the wiring patterns 16 of the upper side of the first unit wiring board 10. In addition, a heat treatment is performed thereto at a temperature of 180° C. to 220° C., so that the connection terminals 20 a of the second unit wiring board 20 are joined to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10.” Arai, [0043].</p>
--	--

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>“Consequently, as shown FIG. 3, the first and second unit wiring boards 10 and 20, each having the wiring patterns 16 of two layers, are stacked and connected in a three dimensional manner in the thickness direction, and thus a base wiring board 5 is constructed. The base wiring board 5 is constructed to have the wiring patterns 16 of four layers, which are connected to each other with the through-hole-conductive layers 14 and the connection terminals 20 a interposed therebetween, and the capacitor components 17 are mounted on the uppermost wiring patterns 16.” Arai, [0044].</p> <p>“As shown in FIG. 7, in the interposer built-in wiring substrate 7 according to this embodiment, the second unit wiring board 20 is stacked to be connected to the first unit wiring board 10 in the thickness direction to construct the base wiring board 5. In the first unit wiring board 10, the wiring patterns 16 are formed on both surface sides of the insulating layer 12, and the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12. Furthermore, the solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12.” Arai, [0057-0058].</p> <p>“FIG. 7 shows an example of an external connection type used as LGA (Land Grid Array) type, and connection parts C of the wiring patterns 16 on the lower surface of the base wiring board 5 are used as lands.” Arai, [0064].</p> <p>“FIG. 9 shows an interposer built-in wiring substrate 7 b according to a modification of this embodiment. In the interposer built-in wiring substrate 7 b according to the modification, bumps 60 of a semiconductor chip 60 (LSI chip) are connected by flip-chip bonding to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10 of the interposer built-in wiring substrate 7 a of FIG. 8. The semiconductor chip 60 is embedded in the resin portion 50.” Arai, [0073].</p>
--	--

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

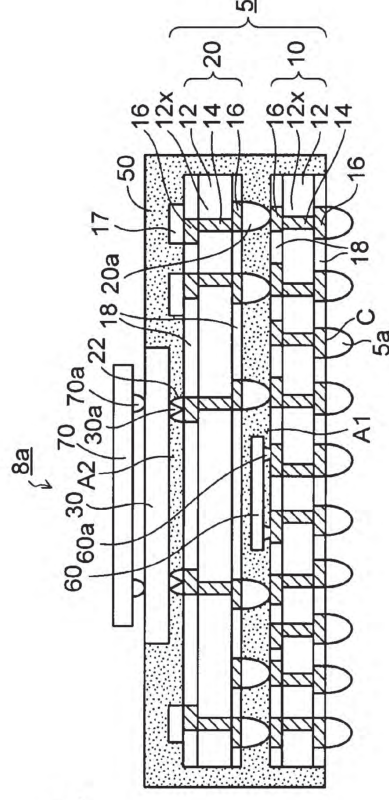
	<p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Arai discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the wiring substrate according to the present invention, connection electrodes with a narrow pitch of the high-performance semiconductor chip is connected to the silicon interposer having fine wirings, and the pitch is converted from the silicon interposer to the base wiring board.” Arai, [0017].</p> <p>“Subsequently, as shown in FIG. 2, the second unit wiring board 20 is disposed on the first unit wiring board 10 so that the connection terminals 20 a of the second unit wiring board 20 can match the connection parts of the wiring patterns 16 of the upper side of the first unit wiring board 10. In addition, a heat treatment is performed thereto at a temperature of 180° C. to 220° C., so that the connection terminals 20 a of the second unit wiring board 20 are joined to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10.” Arai, [0043].</p> <p>“Consequently, as shown FIG. 3, the first and second unit wiring boards 10 and 20, each having the wiring patterns 16 of two layers, are stacked and connected in a three dimensional</p>

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>manner in the thickness direction, and thus a base wiring board 5 is constructed.” Arai, [0044].</p> <p>“Subsequently, the silicon interposer 30 is disposed on the base wiring board 5 so that the connection terminals 30 a of the silicon interposer 30 match the solder materials 22 on the base wiring board 5. Furthermore, a heat treatment is performed at a temperature of 180° C. to 220° C., so that the connection terminals 30 a of the interposer 30 are joined to the solder materials 22 provided on the base wiring board 5, and thereby electrically connected to the wiring patterns 16 of the base wiring board 5. Thus, as shown in FIG. 5, the silicon interposer 30 is stacked to be connected onto the base wiring board 5 in a three dimensional manner, whereby an interposer-attached wiring substrate 6 is obtained.” Arai, [0047-0048].</p> <p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed, on both surface sides of the insulating layer 12, to be connected to each other via the through-hole-conductive layers 14. The solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12. In addition, the capacitor components 17 are mounted to be connected to the wiring pattern 16 on the upper surface of the second unit wiring board 20. Furthermore, the connection terminals 20 a are disposed on the connection parts of the wiring patterns 16 on the lower surface side of the insulating layer 12. Subsequently, the connection terminals 20 a of the second unit wiring board 20 are joined to be electrically connected to the connection parts of the wiring patterns 16 of the first unit wiring board 10.” Arai, [0059-0060].</p> <p>“Furthermore, the silicon interposer 30 is stacked to be connected onto the base wiring board 5 in the thickness direction. In the silicon interposer 30, as described above referring to FIG. 4, the wiring patterns 36 are formed on the on both surface sides of the silicon substrate 32,</p>
--	--

so that the wiring patterns 36 are connected to each other via the through-hole-conductive layer 34." Arai, [0061].

FIG. 11



Arai, FIG. 11

To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein

Arai discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.

See, e.g.:

	<p>“Subsequently, as shown in FIG. 2, the second unit wiring board 20 is disposed on the first unit wiring board 10 so that the connection terminals 20 a of the second unit wiring board 20 can match the connection parts of the wiring patterns 16 of the upper side of the first unit wiring board 10. In addition, a heat treatment is performed thereto at a temperature of 180° C. to 220° C., so that the connection terminals 20 a of the second unit wiring board 20 are joined to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10. When the connection terminals 20 a of the second unit wiring board 20 are formed of gold bumps, gold layers are formed on the connection parts of the wiring patterns 16 of the first unit wiring board 10, and connected thereto by means of ultrasonic bonding. Consequently, as shown FIG. 3, the first and second unit wiring boards 10 and 20, each having the wiring patterns 16 of two layers, are stacked and connected in a three dimensional manner in the thickness direction, and thus a base wiring board 5 is constructed. The base wiring board 5 is constructed to have the wiring patterns 16 of four layers, which are connected to each other with the through-hole-conductive layers 14 and the connection terminals 20 a interposed therebetween, and the capacitor components 17 are mounted on the uppermost wiring patterns 16. Incidentally, instead of providing the connection terminals 20 a on the second unit wiring board 20, the connection terminals may be provided on the wiring patterns 16 on the upper surface of the first unit wiring board 10. Next, as shown in FIG. 4, a silicon interposer 30 having wiring patterns 36 which enable the electrical connection between the upper and lower sides is prepared.” Arai, [0043-0045].</p>
--	---

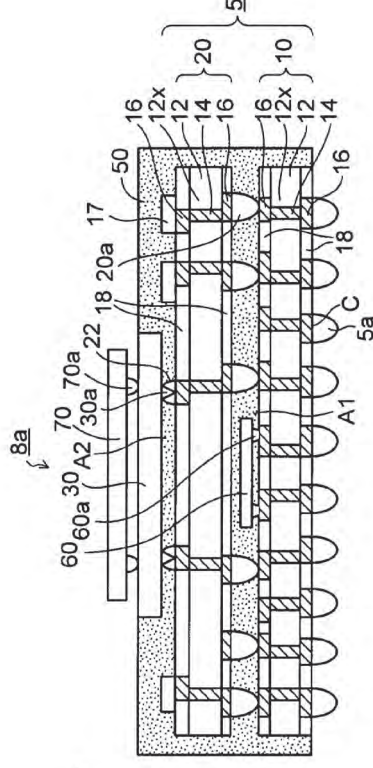


FIG. 11

Arai, FIG. 11

“At this time, between the first unit wiring board 10 and the second unit wiring board 20, as well as between the second unit wiring board 20 and the silicon interposer 30, there exist gaps which correspond to a thickness of the connection terminal 20 a of the second unit wiring board 20, and to a thickness of the connection terminal 30 a of the silicon interposer 30, respectively.” Arai, [0048].

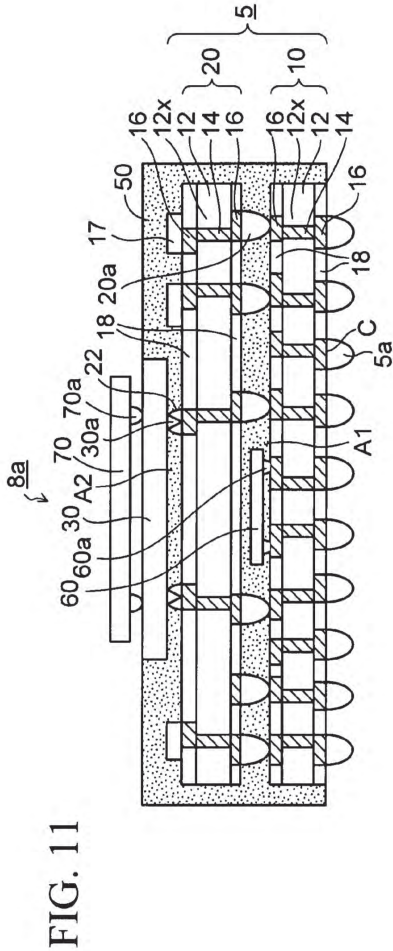
“Next, as also shown in FIG. 6, a molten resin is introduced into the space A constructed by the mold die 40 through the resin-introducing part R. At this time, the resin is introduced in a state where the space A is depressurized (or vacuumized) by exhausting the air. Thus, the resin is introduced into the space A in the mold die 40 through the resin-introducing part R, so that the resin is filled in the gap A 1 between the first unit wiring board 10 and the second unit wiring board 20, the gap A 2 between the second unit wiring board 20 and the silicon interposer 30, and the like.” Arai, [0052-0053].

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>“Still furthermore, the gap A 1 between the first unit wiring board 10 and the second unit wiring board 20 as well as the gap A 2 between the second unit wiring board 20 and the silicon interposer 30 are filled with the resin portion 50. The resin portion 50 is integrally formed to be connected from these gaps A 1, A 2 to the sides of the base wiring board 5 and the silicon interposer 30.” Arai, [0056].</p> <p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed, on both surface sides of the insulating layer 12, to be connected to each other via the through-hole-conductive layers 14. The solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12. In addition, the capacitor components 17 are mounted to be connected to the wiring pattern 16 on the upper surface of the second unit wiring board 20. Furthermore, the connection terminals 20 a are disposed on the connection parts of the wiring patterns 16 on the lower surface side of the insulating layer 12. Subsequently, the connection terminals 20 a of the second unit wiring board 20 are joined to be electrically connected to the connection parts of the wiring patterns 16 of the first unit wiring board 10.” Arai, [0059-0060].</p> <p>“The height of the connection terminal 20 a of the second unit wiring board 20 is adjusted such that semiconductor chip 60 can be housed between the first unit wiring board 10 and the second unit wiring board 20 according to the thickness of the semiconductor chip 60.” Arai, [0074].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Arai discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Firstly, in the method of manufacturing a wiring substrate according to this embodiment, as shown in FIG. 1, a sheet-like first unit wiring board 10 and a sheet-like second unit wiring board 20 which respectively have wiring patterns 16 which enable electrical connection between the upper and lower sides are prepared. In the first unit wiring board 10, through-holes 12 x are formed in an insulating layer 12 which is made of, for example, an epoxy resin (prepreg), or the like, containing glass fabrics. Each through-hole 12 x is filled with a through-hole-conductive layer 14 which is made of copper or the like. Furthermore, on both surface sides of the insulating layer 12, wiring patterns 16 made of copper or the like are formed.” Arai, [0037-0038].</p> <p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed and connected to each other via a through-hole-conductive layer 14 in a through-hole 12 x on both surface sides of an insulating layer 12. In addition, similarly to the first unit wiring board 10, solder resists 18 having openings are formed on both surface sides of the insulating layer 12, and the openings are provided on the connection parts of the wiring patterns 16. Moreover, a capacitor component 17 is mounted to be connected to the wiring pattern 16 on the upper surface side of the second unit wiring board 20. Note that, besides the capacitor 17, a passive component such as a resistance component or an inductor component may be mounted thereon. In addition, in the second unit wiring board 20, a connection terminal 20 a is provided to the connection part of the wiring pattern 16 on the lower surface side of the insulating layer 12.” Arai, [0039-0040].</p>
--	--



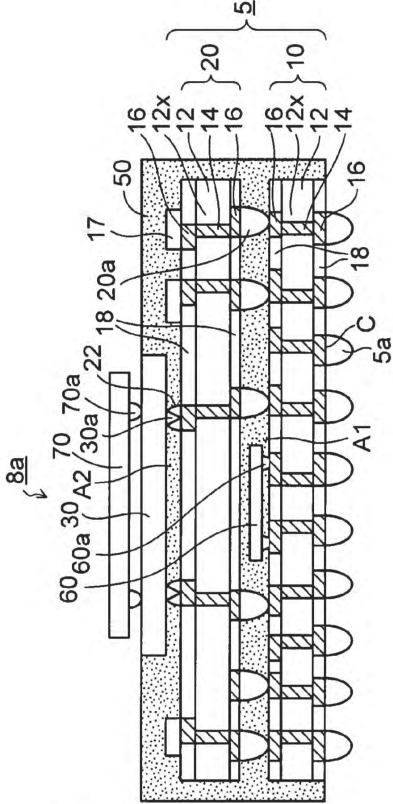
Arai, FIG. 11

“Subsequently, as shown in FIG. 2, the second unit wiring board 20 is disposed on the first unit wiring board 10 so that the connection terminals 20 a of the second unit wiring board 20 can match the connection parts of the wiring patterns 16 of the upper side of the first unit wiring board 10. In addition, a heat treatment is performed thereto at a temperature of 180° C. to 220° C., so that the connection terminals 20 a of the second unit wiring board 20 are joined to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10.” Arai, [0043].

“Consequently, as shown FIG. 3, the first and second unit wiring boards 10 and 20, each having the wiring patterns 16 of two layers, are stacked and connected in a three dimensional manner in the thickness direction, and thus a base wiring board 5 is constructed. The base wiring board 5 is constructed to have the wiring patterns 16 of four layers, which are connected to each other with the through-hole-conductive layers 14 and the connection

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>terminals 20 a interposed therebetween, and the capacitor components 17 are mounted on the uppermost wiring patterns 16.” Arai, [0044].</p> <p>“In the first unit wiring board 10, the wiring patterns 16 are formed on both surface sides of the insulating layer 12, and the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12. Furthermore, the solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12.” Arai, [0058].</p> <p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed, on both surface sides of the insulating layer 12, to be connected to each other via the through-hole-conductive layers 14. The solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12. In addition, the capacitor components 17 are mounted to be connected to the wiring pattern 16 on the upper surface of the second unit wiring board 20. Furthermore, the connection terminals 20 a are disposed on the connection parts of the wiring patterns 16 on the lower surface side of the insulating layer 12.” Arai, [0059].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Arai discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p>

	<p>See, e.g.:</p> <p>“In the first unit wiring board 10, through-holes 12 x are formed in an insulating layer 12 which is made of, for example, an epoxy resin (prepreg), or the like, containing glass fabrics. Each through-hole 12 x is filled with a through-hole-conductive layer 14 which is made of copper or the like.” Arai, [0037].</p> <p>FIG. 11</p>  <p>Arai, FIG. 11</p> <p>“In the silicon interposer 30, through-holes 32 x are provided in a silicon substrate 32, and insulating layers 33 are formed on both surfaces of the silicon substrate 32 as well as on the inner surfaces of the through-holes 32 x. The through-hole 32 x is filled with a through-hole-conductive layer 34 formed of copper or the like.” Arai, [0037].</p>
--	--

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed and connected to each other via a through-hole-conductive layer 14 in a through-hole 12 x on both surface sides of an insulating layer 12.” Arai, [0039].</p> <p>“In the first unit wiring board 10, the wiring patterns 16 are formed on both surface sides of the insulating layer 12, and the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12.” Arai, [0058].</p> <p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed, on both surface sides of the insulating layer 12, to be connected to each other via the through-hole-conductive layers 14.” Arai, [0059].</p> <p>“In the silicon interposer 30, as described above referring to FIG. 4, the wiring patterns 36 are formed on the on both surface sides of the silicon substrate 32, so that the wiring patterns 36 are connected to each other via the through-hole-conductive layer 34.” Arai, [0061].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Arai discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

	<p>“In addition, solder resists 18 having openings are formed on both surface sides of the insulating layer 12, and the openings are provided on the connection parts of the wiring patterns 16. In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed and connected to each other via a through-hole-conductive layer 14 in a through-hole 12 x on both surface sides of an insulating layer 12.” Arai, [0038-0039].</p> <p style="text-align: center;">FIG. 11</p>
--	--

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

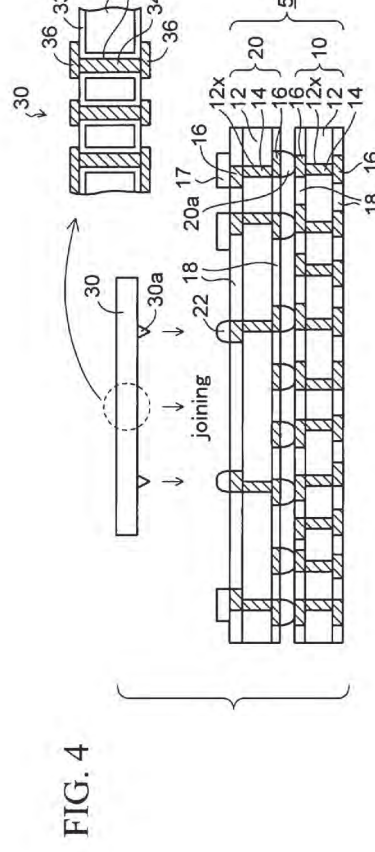
	<p>“In addition, in the second unit wiring board 20, a connection terminal 20 a is provided to the connection part of the wiring pattern 16 on the lower surface side of the insulating layer 12.” Arai, [0039-0040].</p> <p>“In the silicon interposer 30, through-holes 32 x are provided in a silicon substrate 32, and insulating layers 33 are formed on both surfaces of the silicon substrate 32 as well as on the inner surfaces of the through-holes 32 x. The through-hole 32 x is filled with a through-hole-conductive layer 34 formed of copper or the like. Furthermore, on both surface sides of the silicon substrate 32, the wiring patterns 36 made of copper or the like are formed. The wiring patterns 36 are connected to each other via the through-hole-conductive layer 34.” Arai, [0045].</p> <p>“In addition, connection terminals 30 a each made of a gold bump or the like and which has a height of 30 μm to 100 μm are formed onto the wiring pattern 36 of the lower surface of the silicon interposer 30.” Arai, [0046].</p> <p>“Furthermore, the connection terminals 20 a are disposed on the connection parts of the wiring patterns 16 on the lower surface side of the insulating layer 12.” Arai, [0059].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars</p>	<p>Arai discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p>

<p>protrudes downwardly from a bottom surface of the core substrate,</p>	<p>See, <i>e.g.</i>:</p> <p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed and connected to each other via a through-hole-conductive layer 14 in a through-hole 12 x on both surface sides of an insulating layer 12. In addition, similarly to the first unit wiring board 10, solder resists 18 having openings are formed on both surface sides of the insulating layer 12, and the openings are provided on the connection parts of the wiring patterns 16. Moreover, a capacitor component 17 is mounted to be connected to the wiring pattern 16 on the upper surface side of the second unit wiring board 20. Note that, besides the capacitor 17, a passive component such as a resistance component or an inductor component may be mounted thereon.” Arai, [0039].</p> <p style="text-align: center;"> </p> <p style="text-align: center;">FIG. 11</p> <p style="text-align: center;">Arai, FIG. 11</p>
--	--

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>“Each wiring pattern 16 of the first unit wiring board 10 and the second unit wiring board 20 are formed by below method. Firstly, the through-hole 12 x is formed in the insulating layer 12. Subsequently, a metal layer which is connected to both surfaces of the insulating layer 12 from the inside of the through-hole 12 x, is formed by means of a plating method. Thereafter, the metal layer is patterned by photolithography and etching. Alternatively, the wiring pattern may be formed on both surface sides on the bases of processing a copper-clad laminate. Each wiring pattern 16 of the first unit wiring board 10 and the second unit wiring board 20 is set to have a minimum width of, for example, 30 μm to 50 μm.” Arai, [0041].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Arai discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p> <p>“Next, as shown in FIG. 4, a silicon interposer 30 having wiring patterns 36 which enable the electrical connection between the upper and lower sides is prepared. In the silicon interposer 30, through-holes 32 x are provided in a silicon substrate 32, and insulating layers 33 are formed on both surfaces of the silicon substrate 32 as well as on the inner surfaces of the through-holes 32 x. The through-hole 32 x is filled with a through-hole-conductive layer 34 formed of copper or the like. Furthermore, on both surface sides of the silicon substrate 32,</p>

the wiring patterns 36 made of copper or the like are formed. The wiring patterns 36 are connected to each other via the through-hole-conductive layer 34." Arai, [0045].



Arai, FIG. 11

“Since the silicon interposer 30 is manufactured by manufacturing processes of a semiconductor integrated circuit, the silicon interposer 30 is formed at a finer pitch rather than the case of the wiring pattern 16 of the above-described base wiring board 5 and, and the minimum width thereof is formed to be in the range of, for example, 3 μm to 5 μm . In addition, connection terminals 30 a each made of a gold bump or the like and which has a height of 30 μm to 100 μm are formed onto the wiring pattern 36 of the lower surface of the silicon interposer 30. Note that, the wiring patterns 36 of the silicon interposer 30 may be stacked on both surface sides of the silicon substrate 32 in an arbitrary number of layers.” Arai, [0046].

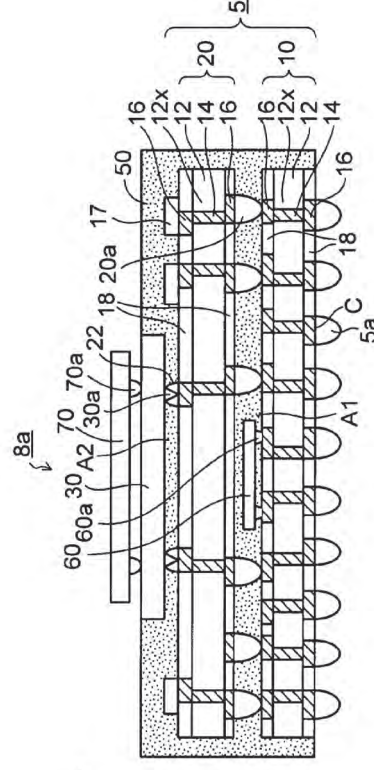
	<p>“As shown also in FIG. 4, solder materials 22 are formed on connection parts for the interposer, which are on the uppermost wiring patterns 16 of the base wiring board 5. The solder materials 22 are formed of a solder ball or a solder paste. Subsequently, the silicon interposer 30 is disposed on the base wiring board 5 so that the connection terminals 30 a of the silicon interposer 30 match the solder materials 22 on the base wiring board 5. Furthermore, a heat treatment is performed at a temperature of 180° C. to 220° C., so that the connection terminals 30 a of the interposer 30 are joined to the solder materials 22 provided on the base wiring board 5, and thereby electrically connected to the wiring patterns 16 of the base wiring board 5.” Arai, [0047].</p> <p>“Furthermore, the silicon interposer 30 is stacked to be connected onto the base wiring board 5 in the thickness direction. In the silicon interposer 30, as described above referring to FIG. 4, the wiring patterns 36 are formed on the on both surface sides of the silicon substrate 32, so that the wiring patterns 36 are connected to each other via the through-hole-conductive layer 34. The connection terminals 30 a formed of the gold bump or the like are provided on the connection parts of the wiring patterns 36 on the lower surface of the silicon substrate 32. The connection terminals 30 a of the silicon interposer 30 are joined to the connection parts of the wiring patterns 16 of the base wiring board 5 by use of the solder materials 22.” Arai, [0061].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Arai discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In addition, in the second unit wiring board 20, a connection terminal 20a is provided to the connection part of the wiring pattern 16 on the lower surface side of the insulating layer 12. The connection terminal 20 a is formed of a silver (Ag) paste, a solder paste, a solder ball, a copper ball covered with solder on the outer surface, a gold bump, or the like, and the height is set to 30 μm to 100 μm.” Arai, [0040].</p> <p>“As shown also in FIG. 4, solder materials 22 are formed on connection parts for the interposer, which are on the uppermost wiring patterns 16 of the base wiring board 5. The solder materials 22 are formed of a solder ball or a solder paste. Subsequently, the silicon interposer 30 is disposed on the base wiring board 5 so that the connection terminals 30 a of the silicon interposer 30 match the solder materials 22 on the base wiring board 5. Furthermore, a heat treatment is performed at a temperature of 180° C. to 220° C., so that the connection terminals 30 a of the interposer 30 are joined to the solder materials 22 provided on the base wiring board 5, and thereby electrically connected to the wiring patterns 16 of the base wiring board 5.” Arai, [0047].</p> <p>“In the first unit wiring board 10, the wiring patterns 16 are formed on both surface sides of the insulating layer 12, and the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12. Furthermore, the solder resists 18 having the openings on the connection parts of the wiring</p>
---	---

patterns 16 are respectively provided on both surface sides of the insulating layer 12." Arai, [0058].

FIG. 11



Arai, FIG. 11

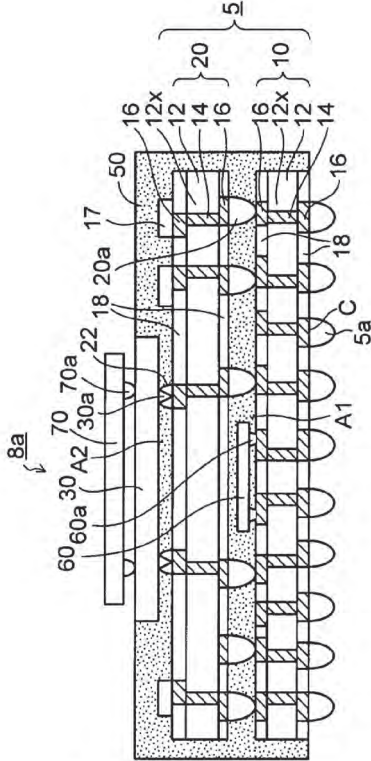
To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Arai discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.

See, e.g.:

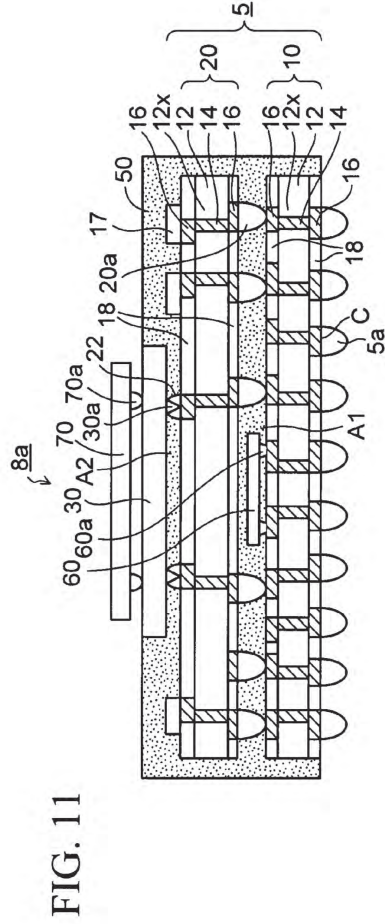
Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

top metal pillars of the bottom package substrate; and	<p>“In addition, in the second unit wiring board 20, a connection terminal 20a is provided to the connection part of the wiring pattern 16 on the lower surface side of the insulating layer 12. The connection terminal 20a is formed of a silver (Ag) paste, a solder paste, a solder ball, a copper ball covered with solder on the outer surface, a gold bump, or the like, and the height is set to 30 μm to 100 μm.” Arai, [0040].</p> <p>“the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12.” Arai, [0045-0046].</p> <p>“As shown also in FIG. 4, solder materials 22 are formed on connection parts for the interposer, which are on the uppermost wiring patterns 16 of the base wiring board 5. The solder materials 22 are formed of a solder ball or a solder paste. Subsequently, the silicon interposer 30 is disposed on the base wiring board 5 so that the connection terminals 30a of the silicon interposer 30 match the solder materials 22 on the base wiring board 5. Furthermore, a heat treatment is performed at a temperature of 180° C. to 220° C., so that the connection terminals 30a of the interposer 30 are joined to the solder materials 22 provided on the base wiring board 5, and thereby electrically connected to the wiring patterns 16 of the base wiring board 5.” Arai, [0047].</p> <p>“the second unit wiring board 20 is stacked to be connected to the first unit wiring board 10 in the thickness direction to construct the base wiring board 5.” Arai, [0057].</p>
--	---

	<p>FIG. 11</p>  <p>Arai, FIG. 11</p> <p>“the wiring patterns 16 are formed, on both surface sides of the insulating layer 12, to be connected to each other via the through-hole-conductive layers 14” Arai, [0059].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Arai discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p> <p>“FIG. 9 shows an interposer built-in wiring substrate 7 b according to a modification of this embodiment. In the interposer built-in wiring substrate 7 b according to the modification,</p>

bumps 60 of a semiconductor chip 60 (LSI chip) are connected by flip-chip bonding to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10 of the interposer built-in wiring substrate 7 a of FIG. 8. The semiconductor chip 60 is embedded in the resin portion 50. A gap between the first unit wiring board 10 and the semiconductor chip 60 is also filled with the resin portion 50.” Arai, [0073].

“The semiconductor chip 60 is housed in a space which is formed to have a height corresponding to that of the connection terminal 20 a of the second unit wiring board 20. The semiconductor chip 60 is sealed with the resin portion 50. The height of the connection terminal 20 a of the second unit wiring board 20 is adjusted such that semiconductor chip 60 can be housed between the first unit wiring board 10 and the second unit wiring board 20 according to the thickness of the semiconductor chip 60. In the interposer built-in wiring substrate 7 b according to the modified example also, the resin portion 50 is filled by the above-described vacuum transfer molding.” Arai, [0074].



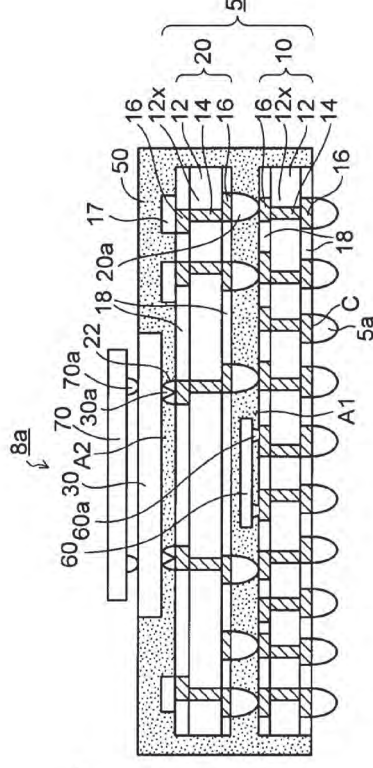
Arai, FIG. 11

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>“FIG. 11 shows a semiconductor device 8 a according to a modification of the embodiment of the present invention. As shown in FIG. 11, the semiconductor device 8 a according to the modification is constructed in such a way that the bumps 70 a of the semiconductor chip 70 are connected by flip-chip bonding to the interposer 30 of the interposer built-in wiring substrate 7 b of FIG. 9.” Arai, [0078-0079].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Arai discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Moreover, in a method filling a gap with a liquid resin by means of capillarity, it is generally extremely difficult to fill a narrow gap with a resin containing a large amount of fillers. In this embodiment, even when the gap A 1 between the first unit wiring board 10 and the second unit wiring board 20 as well as the gap A 2 between the second unit wiring board 20 and the silicon interposer 30 are quite narrow (for example, 30 μm), because the filling with resin is performed by means of vacuum transfer molding, it is possible to fill a narrow gap with a resin containing a large amount of fillers with high reliability.” Arai, [0056-0057].</p> <p>“As shown in FIG. 7, in the interposer built-in wiring substrate 7 according to this embodiment, the second unit wiring board 20 is stacked to be connected to the first unit</p>

	<p>wiring board 10 in the thickness direction to construct the base wiring board 5. In the first unit wiring board 10, the wiring patterns 16 are formed on both surface sides of the insulating layer 12, and the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12.” Arai, [0057-0058].</p> <p>“In the first unit wiring board 10, the wiring patterns 16 are formed on both surface sides of the insulating layer 12, and the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12. Furthermore, the solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12. In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed, on both surface sides of the insulating layer 12, to be connected to each other via the through-hole-conductive layers 14. The solder resists 18 having the openings on the connection parts of the wiring patterns 16 are respectively provided on both surface sides of the insulating layer 12.” Arai, [0058-0059].</p> <p>“The semiconductor chip 60 is housed in a space which is formed to have a height corresponding to that of the connection terminal 20 a of the second unit wiring board 20. The semiconductor chip 60 is sealed with the resin portion 50. The height of the connection terminal 20 a of the second unit wiring board 20 is adjusted such that semiconductor chip 60 can be housed between the first unit wiring board 10 and the second unit wiring board 20 according to the thickness of the semiconductor chip 60.” Arai, [0073-0074].</p>
--	--

FIG. 11



Arai, FIG. 11

“FIG. 10 shows a semiconductor device 8 according to this embodiment. The semiconductor device 8 is constructed in a way that bumps 70 of a semiconductor chip 70 (LSI chip) are mounted to be connected by flip-chip bonding to the connection parts of the wiring patterns 36 (FIG. 4) on the upper surface of the silicon interposer 30 of the interposer built-in wiring substrate 7 of FIG. 8.” Arai, [0075].

“FIG. 11 shows a semiconductor device 8 a according to a modification of the embodiment of the present invention. As shown in FIG. 11, the semiconductor device 8 a according to the modification is constructed in such a way that the bumps 70 a of the semiconductor chip 70 are connected by flip-chip bonding to the interposer 30 of the interposer built-in wiring substrate 7 b of FIG. 9.” Arai, [0078-0079].

To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Arai discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p> <p>“a sheet-like first wiring board 10 and a sheet-like second unit wiring board 20 which respectively have wiring patterns 16 which enable electrical connection between the upper and lower sides are prepared. In the first unit wiring board 10, through-holes 12 x are formed in an insulating layer 12 which is made of, for example, an epoxy resin (prepreg), or the like, containing glass fabrics. Each through-hole 12 x is filled with a through-hole-conductive layer 14 which is made of copper or the like.” Arai, [0044-0045].</p> <p>FIG. 11</p> <p>Arai, FIG. 11</p>

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>“In addition, the capacitor components 17 are mounted to be connected to the wiring pattern 16 on the upper surface of the second unit wiring board 20. Furthermore, the connection terminals 20 a are disposed on the connection parts of the wiring patterns 16 on the lower surface side of the insulating layer 12.” Arai, [0059].</p> <p>“The capacitor components 17 mounted on the base wiring board 5 are connected between a power line and a ground line of the semiconductor chip 70, and serves as decoupling capacitors.” Arai, [0075].</p> <p>“Another embodiment may be constructed as follows. Firstly, two units are prepared, each having a structure in which the silicon interposer 30 is mounted on the base wiring board 5. The units are symmetrically connected to each other with a connection terminal.” Arai, [0078].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

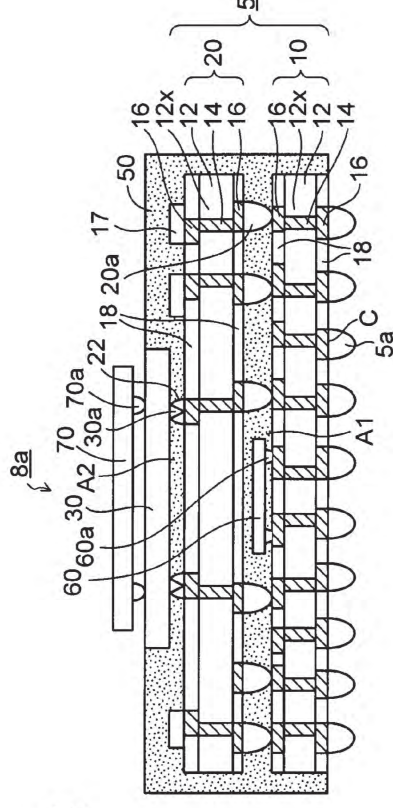
Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced	Arai discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

downwardly from the bottom surface of the top package substrate.	<p><i>See, e.g.:</i></p> <p>“At this time, between the first unit wiring board 10 and the second unit wiring board 20, as well as between the second unit wiring board 20 and the silicon interposer 30, there exist gaps which correspond to a thickness of the connection terminal 20 a of the second unit wiring board 20, and to a thickness of the connection terminal 30 a of the silicon interposer 30, respectively.” Arai, [0048].</p> <p>“The silicon interposer 30 is embedded in the resin portion 50 in a state of exposing the upper surface of the silicon interposer 30, that is a semiconductor-chip-mounting surface. And, the upper surface of the silicon interposer 30 and the upper surface of the resin portion 50 constitute identical surface.” Arai, [0063].</p> <p>“Still furthermore, the gap A 1 between the first unit wiring board 10 and the second unit wiring board 20 as well as the gap A 2 between the second unit wiring board 20 and the silicon interposer 30 are filled with the resin portion 50.” Arai, [0071].</p> <p>“A gap between the first unit wiring board 10 and the semiconductor chip 60 is also filled with the resin portion 50.” Arai, [0073].</p> <p>“The semiconductor chip 60 is housed in a space which is formed to have a height corresponding to that of the connection terminal 20 a of the second unit wiring board 20.” Arai, [0074].</p>
--	---

FIG. 11



Arai, FIG. 11

To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

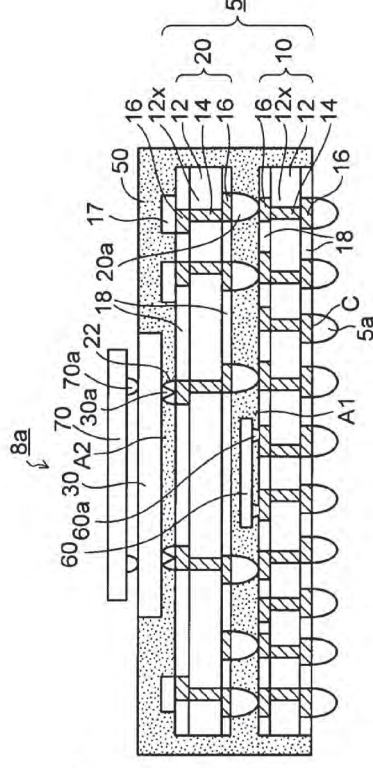
Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

<p>package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p><i>See, e.g.:</i></p> <p>“FIG. 9 shows an interposer built-in wiring substrate 7 b according to a modification of this embodiment. In the interposer built-in wiring substrate 7 b according to the modification, bumps 60 of a semiconductor chip 60 (LSI chip) are connected by flip-chip bonding to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10 of the interposer built-in wiring substrate 7 a of FIG. 8. The semiconductor chip 60 is embedded in the resin portion 50. A gap between the first unit wiring board 10 and the semiconductor chip 60 is also filled with the resin portion 50. The semiconductor chip 60 is housed in a space which is formed to have a height corresponding to that of the connection terminal 20 a of the second unit wiring board 20.” Arai, [0073-0074].</p> <p>“The semiconductor device 8 is constructed in a way that bumps 70 a of a semiconductor chip 70 (LSI chip) are mounted to be connected by flip-chip bonding to the connection parts of the wiring patterns 36 (FIG. 4) on the upper surface of the silicon interposer 30 of the interposer built-in wiring substrate 7 a of FIG. 8. The capacitor components 17 mounted on the base wiring board 5 are connected between a power line and a ground line of the semiconductor chip 70, and serves as decoupling capacitors.” Arai, [0075].</p>
--	--

FIG. 11



Arai, FIG. 11

“FIG. 11 shows a semiconductor device 8 a according to a modification of the embodiment of the present invention. As shown in FIG. 11, the semiconductor device 8 a according to the modification is constructed in such a way that the bumps 70 a of the semiconductor chip 70 are connected by flip-chip bonding to the interposer 30 of the interposer built-in wiring substrate 7 b of FIG. 9.” Arai, [0078-0079].

“In the semiconductor device 8, 8 a of this embodiment, even when a high-performance semiconductor device 70 having connection electrodes with narrow pitch is mounted, the semiconductor chip 70 can be electrically connected to the base wiring board 5 while converting the pitch of the connection electrodes thereof, by mounting the semiconductor chip 70 on the silicon interposer 30 having the wiring pattern corresponding the connection electrode of the semiconductor chip 70.” Arai, [0080].

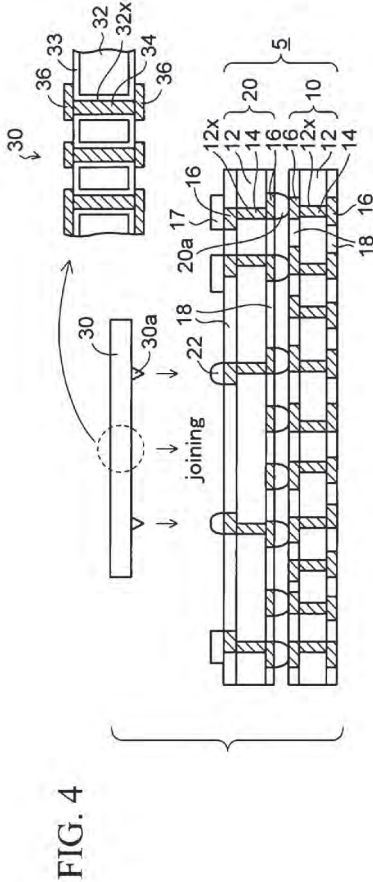
Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Arai discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Subsequently, as shown in FIG. 2, the second unit wiring board 20 is disposed on the first unit wiring board 10 so that the connection terminals 20 a of the second unit wiring board 20 can match the connection parts of the wiring patterns 16 of the upper side of the first unit wiring board 10. In addition, a heat treatment is performed thereto at a temperature of 180° C. to 220° C., so that the connection terminals 20 a of the second unit wiring board 20 are joined to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10.” Arai, [0043].</p> <p>“As shown also in FIG. 4, solder materials 22 are formed on connection parts for the interposer, which are on the uppermost wiring patterns 16 of the base wiring board 5. The</p>

solder materials 22 are formed of a solder ball or a solder paste. Subsequently, the silicon interposer 30 is disposed on the base wiring board 5 so that the connection terminals 30 a of the silicon interposer 30 match the solder materials 22 on the base wiring board 5. Furthermore, a heat treatment is performed at a temperature of 180° C. to 220° C., so that the connection terminals 30 a of the interposer 30 are joined to the solder materials 22 provided on the base wiring board 5, and thereby electrically connected to the wiring patterns 16 of the base wiring board 5.” Arai, [0047].



Arai, FIG. 4

“In the first unit wiring board 10, the wiring patterns 16 are formed on both surface sides of the insulating layer 12, and the wiring patterns 16 are connected to each other via the through-hole-conductive layers 14 filled in the through-holes 12 x of the insulating layer 12.” Arai, [0058].

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed, on both surface sides of the insulating layer 12, to be connected to each other via the through-hole-conductive layers 14.” Arai, [0059].</p> <p>“Subsequently, the connection terminals 20 a of the second unit wiring board 20 are joined to be electrically connected to the connection parts of the wiring patterns 16 of the first unit wiring board 10.” Arai, [0060].</p> <p>“The connection terminals 30 a formed of the gold bump or the like are provided on the connection parts of the wiring patterns 36 on the lower surface of the silicon substrate 32. The connection terminals 30 a of the silicon interposer 30 are joined to the connection parts of the wiring patterns 16 of the base wiring board 5 by use of the solder materials 22.” Arai, [0061].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

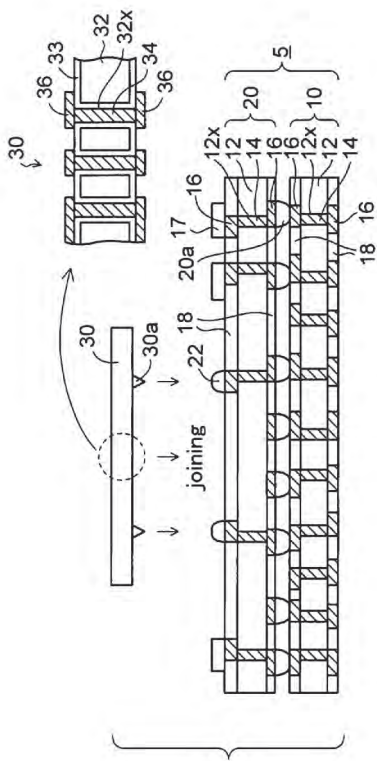
Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the pillars protruding downwardly from the	Arai discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

<p>bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In the first unit wiring board 10, through-holes 12 x are formed in an insulating layer 12 which is made of, for example, an epoxy resin (prepreg), or the like, containing glass fabrics. Each through-hole 12 x is filled with a through-hole-conductive layer 14 which is made of copper or the like. Furthermore, on both surface sides of the insulating layer 12, wiring patterns 16 made of copper or the like are formed. The wiring patterns 16 on both surface sides are connected to each other via the through-hole-conductive layer 14.” Arai, [0037-0038].</p> <p>“Subsequently, as shown in FIG. 2, the second unit wiring board 20 is disposed on the first unit wiring board 10 so that the connection terminals 20 a of the second unit wiring board 20 can match the connection parts of the wiring patterns 16 of the upper side of the first unit wiring board 10. In addition, a heat treatment is performed thereto at a temperature of 180° C. to 220° C., so that the connection terminals 20 a of the second unit wiring board 20 are joined to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10.” Arai, [0043].</p> <p>“Consequently, as shown FIG. 3, the first and second unit wiring boards 10 and 20, each having the wiring patterns 16 of two layers, are stacked and connected in a three dimensional manner in the thickness direction, and thus a base wiring board 5 is constructed. The base wiring board 5 is constructed to have the wiring patterns 16 of four layers, which are connected to each other with the through-hole-conductive layers 14 and the connection</p>
--	---

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>terminals 20 a interposed therebetween, and the capacitor components 17 are mounted on the uppermost wiring patterns 16.” Arai, [0044].</p> <p>“In addition, connection terminals 30 a each made of a gold bump or the like and which has a height of 30 μm to 100 μm are formed onto the wiring pattern 36 of the lower surface of the silicon interposer 30. Note that, the wiring patterns 36 of the silicon interposer 30 may be stacked on both surface sides of the silicon substrate 32 in an arbitrary number of layers. As shown also in FIG. 4, solder materials 22 are formed on connection parts for the interposer, which are on the uppermost wiring patterns 16 of the base wiring board 5. The solder materials 22 are formed of a solder ball or a solder paste. Subsequently, the silicon interposer 30 is disposed on the base wiring board 5 so that the connection terminals 30 a of the silicon interposer 30 match the solder materials 22 on the base wiring board 5. Furthermore, a heat treatment is performed at a temperature of 180° C. to 220° C., so that the connection terminals 30 a of the interposer 30 are joined to the solder materials 22 provided on the base wiring board 5, and thereby electrically connected to the wiring patterns 16 of the base wiring board 5.” Arai, [0046-0047].</p>
--	--



Arai, FIG. 4

“Furthermore, the connection terminals 20 a are disposed on the connection parts of the wiring patterns 16 on the lower surface side of the insulating layer 12. Subsequently, the connection terminals 20 a of the second unit wiring board 20 are joined to be electrically connected to the connection parts of the wiring patterns 16 of the first unit wiring board 10.” Arai, [0059-0060].

“The connection terminals 30 a formed of the gold bump or the like are provided on the connection parts of the wiring patterns 36 on the lower surface of the silicon substrate 32. The connection terminals 30 a of the silicon interposer 30 are joined to the connection parts of the wiring patterns 16 of the base wiring board 5 by use of the solder materials 22.” Arai, [0061].

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom ends of the plurality of metal pillars of the bottom package substrate via the plurality of metal pillars, and bottom ends of the plurality of bottom metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Arai discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In the first unit wiring board 10, through-holes 12 x are formed in an insulating layer 12 which is made of, for example, an epoxy resin (prepreg), or the like, containing glass fabrics. Each through-hole 12 x is filled with a through-hole-conductive layer 14 which is made of copper or the like. Furthermore, on both surface sides of the insulating layer 12, wiring patterns 16 made of copper or the like are formed. The wiring patterns 16 on both surface sides are connected to each other via the through-hole-conductive layer 14. In addition, solder resists 18 having openings are formed on both surface sides of the insulating layer 12, and</p>

	<p>the openings are provided on the connection parts of the wiring patterns 16.” Arai, [0037-0038].</p> <p>“In the second unit wiring board 20, similarly to the first unit wiring board 10, the wiring patterns 16 are formed and connected to each other via a through-hole-conductive layer 14 in a through-hole 12 x on both surface sides of an insulating layer 12. In addition, similarly to the first unit wiring board 10, solder resists 18 having openings are formed on both surface sides of the insulating layer 12, and the openings are provided on the connection parts of the wiring patterns 16. Moreover, a capacitor component 17 is mounted to be connected to the wiring pattern 16 on the upper surface side of the second unit wiring board 20. Note that, besides the capacitor 17, a passive component such as a resistance component or an inductor component may be mounted thereon. In addition, in the second unit wiring board 20, a connection terminal 20 a is provided to the connection part of the wiring pattern 16 on the lower surface side of the insulating layer 12. The connection terminal 20 a is formed of a silver (Ag) paste, a solder paste, a solder ball, a copper ball covered with solder on the outer surface, a gold bump, or the like, and the height is set to 30 μm to 100 μm. Each wiring pattern 16 of the first unit wiring board 10 and the second unit wiring board 20 are formed by below method. Firstly, the through-hole 12 x is formed in the insulating layer 12. Subsequently, a metal layer which is connected to both surfaces of the insulating layer 12 from the inside of the through-hole 12 x, is formed by means of a plating method.” Arai, [0039-0041].</p>
--	--

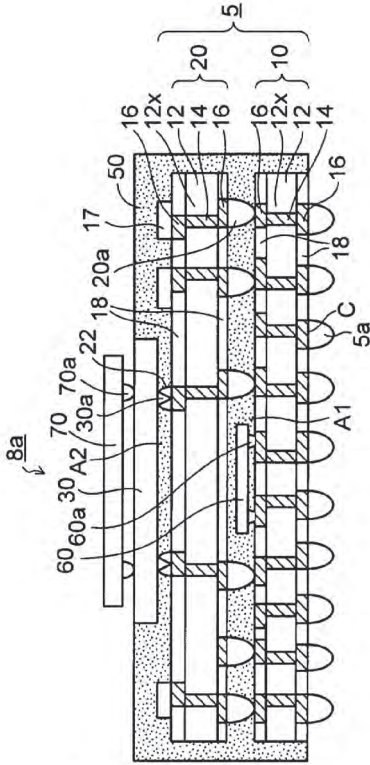


FIG. 11

Arai, FIG. 11

“Subsequently, as shown in FIG. 2, the second unit wiring board 20 is disposed on the first unit wiring board 10 so that the connection terminals 20 a of the second unit wiring board 20 can match the connection parts of the wiring patterns 16 of the upper side of the first unit wiring board 10. In addition, a heat treatment is performed thereto at a temperature of 180° C. to 220° C., so that the connection terminals 20 a of the second unit wiring board 20 are joined to the connection parts of the wiring patterns 16 on the upper surface of the first unit wiring board 10.” Arai, [0043].

“In the silicon interposer 30, through-holes 32 x are provided in a silicon substrate 32, and insulating layers 33 are formed on both surfaces of the silicon substrate 32 as well as on the inner surfaces of the through-holes 32 x. The through-hole 32 x is filled with a through-hole-conductive layer 34 formed of copper or the like. Furthermore, on both surface sides of the silicon substrate 32, the wiring patterns 36 made of copper or the like are formed. The wiring patterns 36 are connected to each other via the through-hole-conductive layer 34. Since the

Appendix A-1 - Invalidity of U.S. Patent No. 9859202 in view of Arai - U.S. Patent Publication No. 20080155820

	<p>silicon interposer 30 is manufactured by manufacturing processes of a semiconductor integrated circuit, the silicon interposer 30 is formed at a finer pitch rather than the case of the wiring pattern 16 of the above-described base wiring board 5 and, and the minimum width thereof is formed to be in the range of, for example, 3 μm to 5 μm. In addition, connection terminals 30 a each made of a gold bump or the like and which has a height of 30 μm to 100 μm are formed onto the wiring pattern 36 of the lower surface of the silicon interposer 30.” Arai, [0045-0046].</p> <p>“Subsequently, the silicon interposer 30 is disposed on the base wiring board 5 so that the connection terminals 30 a of the silicon interposer 30 match the solder materials 22 on the base wiring board 5. Furthermore, a heat treatment is performed at a temperature of 180° C. to 220° C., so that the connection terminals 30 a of the interposer 30 are joined to the solder materials 22 provided on the base wiring board 5, and thereby electrically connected to the wiring patterns 16 of the base wiring board 5.” Arai, [0047].</p> <p>“The connection terminals 30 a formed of the gold bump or the like are provided on the connection parts of the wiring patterns 36 on the lower surface of the silicon substrate 32. The connection terminals 30 a of the silicon interposer 30 are joined to the connection parts of the wiring patterns 16 of the base wiring board 5 by use of the solder materials 22.” Arai, [0061].</p> <p>To the extent Plaintiff contends that Arai fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

U.S. Patent No. 7687899 (“Berry”) is titled Dual Laminate Package Structure with Embedded Elements and lists Christopher J. Berry as the inventor. Berry is assigned to Amkor Technology, Inc. Berry anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Berry is a U.S. patent that was filed August 7, 2007 and issued March 30, 2010. Berry is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Berry, or otherwise rendered obvious by disclosures and teachings of Berry, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Berry does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Berry with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Berry, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

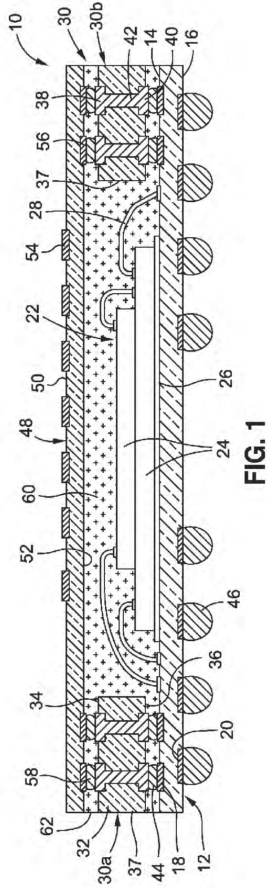
Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

Where the chart below states that Berry “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Berry or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Berry set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Berry discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“Referring now to the drawings wherein the showings are for purposes of illustrating various embodiments of the present invention only, and not for purposes of limiting the same, FIG. 1 depicts a semiconductor package 10 constructed in accordance with a first embodiment of the present invention. The semiconductor package 10 comprises a laminate bottom substrate 12 which has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the bottom substrate 12 defines a generally planar top surface 14 and an opposed, generally planar bottom surface 16.” Berry, [3:15-3:24].</p>



Berry, FIG. 1

“The semiconductor package 10 of the first embodiment further comprises a laminate top substrate 48 which is mechanically and electrically connected to the interposer 30 in a manner which will be described in more detail below. The top substrate 48 also has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the top substrate 48 defines a generally planar top surface 50 and an opposed, generally planar bottom surface 52.” Berry, [4:55-4:62].

“Referring now to FIG. 2, there is depicted a semiconductor package 100 constructed in accordance with a second embodiment of the present invention. The semiconductor package 100 comprises a laminate bottom substrate 112 which has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the bottom substrate 112 defines a generally planar top surface 114 and an opposed, generally planar bottom surface 116.” Berry, [6:20-6:27].

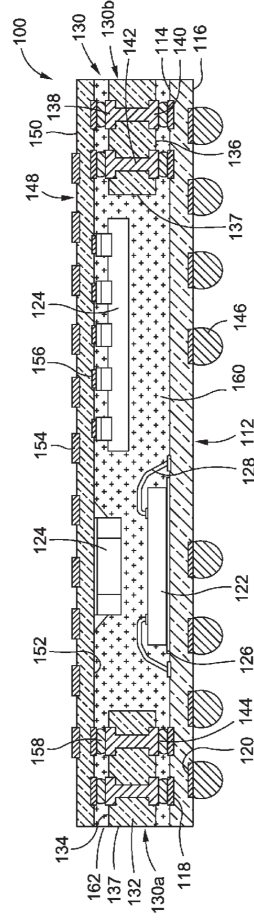


FIG. 2

Berry, FIG. 2

“Referring now to FIG. 3, there is depicted a semiconductor package 200 constructed in accordance with a third embodiment of the present invention. The semiconductor package 200 comprises a laminate bottom substrate 212 which has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the bottom substrate 212 defines a generally planar top surface 214 and an opposed, generally planar bottom surface 216.” Berry, [6:20-6:27].

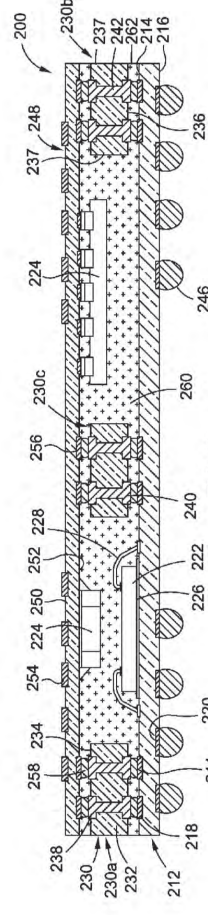


FIG. 3

Berry, FIG. 3

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“The semiconductor package 100 of the first embodiment further comprises a laminate top substrate 148 which is mechanically and electrically connected to the interposer 130 in a manner which will be described in more detail below. The top substrate 148 also has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the top substrate 148 defines a generally planar top surface 150 and an opposed, generally planar bottom surface 152.” Berry, [7:54-7:61].</p> <p>“The semiconductor package 200 of the third embodiment further comprises a laminate top substrate 248 which is mechanically and electrically connected to the interposer 230 in a manner which will be described in more detail below. The top substrate 248 also has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the top substrate 248 defines a generally planar top surface 250 and an opposed, generally planar bottom surface 252.” Berry, [11:3-11:10].</p>
[1.A] a bottom package substrate;	<p>Berry discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The semiconductor package 10 comprises a laminate bottom substrate 12 which has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the bottom substrate 12 defines a generally planar top surface 14 and an opposed, generally planar bottom surface 16. Disposed on the top surface 14 is a plurality of top contacts 18 of the bottom substrate 12. In the bottom substrate 12, the top contacts 18 are segregated into two sets, with the top contacts 18 of each set extending along and in spaced relation to a respective one of an opposed pair of the peripheral edge segments defined by the bottom substrate 12. Formed on the bottom surface 16 of the bottom substrate 12 is a plurality of</p>

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>bottom contacts 20. Though not shown in FIG. 1, the top and bottom contacts 18, 20 are electrically connected to each other in a prescribed pattern or arrangement by conductive vias which extend through the bottom substrate 12.” Berry, [3:20-3:35].</p> <p>“Formed on each of the bottom contacts 20 of the bottom substrate 12 is a solder bump or solder ball 46.” Berry, [4:52-4:54].</p> <p>“The semiconductor package 100 comprises a laminate bottom substrate 112 which has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the bottom substrate 112 defines a generally planar top surface 114 and an opposed, generally planar bottom surface 116. Disposed on the top surface 114 is a plurality of top contacts 118 of the bottom substrate 112. In the bottom substrate 112, the top contacts 118 are segregated into two sets, with the top contacts 118 of each set extending along and in spaced relation to a respective one of an opposed pair of the peripheral edge segments defined by the bottom substrate 112. Formed on the bottom surface 116 of the bottom substrate 112 is a plurality of bottom contacts 120. Though not shown in FIG. 2, the top and bottom contacts 118, 120 are electrically connected to each other in a prescribed pattern or arrangement by conductive vias which extend through the bottom substrate 112.” Berry, [6:22-6:38].</p>
--	--

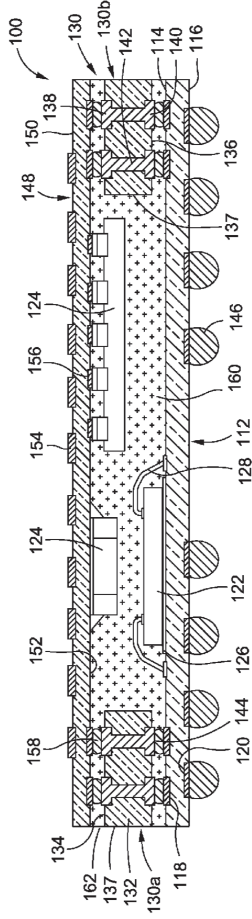


FIG. 2

Berry, FIG. 2

“Formed on each of the bottom contacts 120 of the bottom substrate 112 is a solder bump or solder ball 146.” Berry, [7:51-7:53].

“The semiconductor package 200 comprises a laminate bottom substrate 212 which has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the bottom substrate 212 defines a generally planar top surface 214 and an opposed, generally planar bottom surface 216. Disposed on the top surface 214 is a plurality of top contacts 218 of the bottom substrate 212. In the bottom substrate 212, the top contacts 218 are segregated into at least three sets, with the top contacts 218 of two of these sets extending along and in spaced relation to a respective one of an opposed pair of the peripheral edge segments defined by the bottom substrate 212. The top contacts 218 of the third set extend between and in generally parallel relation to the top contacts 218 of the other two sets thereof. Formed on the bottom surface 216 of the bottom substrate 212 is a plurality of bottom contacts 220. Though not shown in FIG. 3, the top and bottom contacts 218, 220 are electrically connected to each other in a prescribed pattern or arrangement by conductive vias which extend through the bottom substrate 212.” Berry, [9:40-9:59].

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

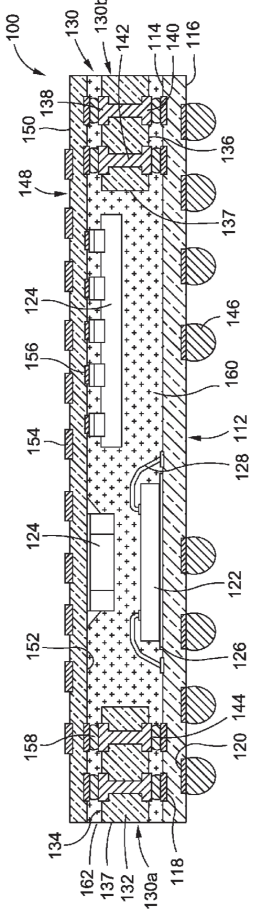
	<p>“In the next step of the fabrication process, a bottom substrate strip 312 is provided, such bottom substrate strip 312 including multiple bottom substrates 112 which are integrally connected to each other. In this respect, disposed on the top surface of the bottom substrate strip 312 is a plurality of the top contacts 118 which are oriented such that each of the bottom substrates 112 included in the bottom substrate strip 312 is provided with an assortment of the top contacts 118 arranged in the same pattern described above in relation to the bottom substrate 112 of the semiconductor package 100 shown in FIG. 2.” Berry, [13:62-14:4].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Berry discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The semiconductor package 10 of the first embodiment further comprises a laminate top substrate 48 which is mechanically and electrically connected to the interposer 30 in a manner which will be described in more detail below. The top substrate 48 also has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the top substrate 48 defines a generally planar top surface 50 and an opposed, generally planar bottom surface 52. Disposed in the approximate center of the top surface 50 of the top substrate 48 is a plurality of top contacts 54 of the top substrate 48. Additionally, formed on the bottom surface 52 of the top substrate 48 is a plurality of bottom contacts 56 thereof. In</p>

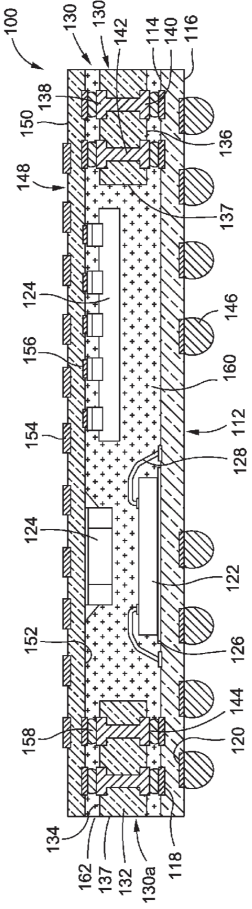
Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>the top substrate 48, the bottom contacts 56 are segregated into two sets, with the bottom contacts 56 of each set extending along and in spaced relation to a respective one of an opposed pair of the peripheral edge segments defined by the top substrate 48. Though not shown, the top and bottom contacts 54, 56 are electrically connected to each other by conductive vias which extend through the top substrate 48. Those of ordinary skill in the art will recognize that each top contact 54 may be electrically connected to one or more bottom contacts 56 in any pattern or arrangement through the use of such conductive vias. The top and bottom contacts 54, 56 are also each preferably identically configured to each other, and fabricated from a suitable conductive material, as is any conductive via extending there between.” Berry, [4:55-5:13].</p> <p>“When the top substrate 48 is electrically and mechanically connected to the interposer 30 in the above-described manner, the die stack 22 as well as the conductive wires 28 are effectively positioned between the bottom and top substrates 12, 48, and more particularly the top surface 14 of the bottom substrate 12 and the bottom surface 52 of the top substrate 48.” Berry, [5:31-5:37].</p> <p>“The semiconductor package 200 of the third embodiment further comprises a laminate top substrate 248 which is mechanically and electrically connected to the interposer 230 in a manner which will be described in more detail below. The top substrate 248 also has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the top substrate 248 defines a generally planar top surface 250 and an opposed, generally planar bottom surface 252. Disposed on the top surface 250 of the top substrate 248 is a plurality of top contacts 254 of the top substrate 248. Additionally, formed on the bottom surface 252 of the top substrate 248 is a plurality of bottom contacts 256 thereof.” Berry, [7:54-7:65].</p>
--	--

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“When the top substrate 148 is electrically and mechanically connected to the interposer 130 in the above-described manner, the electronic components 122, 124 as well as the conductive wires 128 are effectively positioned between the bottom and top substrates 112, 148, and more particularly the top surface 114 of the bottom substrate 112 and the bottom surface 152 of the top substrate 148.” Berry, [8:47-8:53].</p> <p>“The semiconductor package 100 of the first embodiment further comprises a laminate top substrate 148 which is mechanically and electrically connected to the interposer 130 in a manner which will be described in more detail below. The top substrate 148 also has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the top substrate 148 defines a generally planar top surface 150 and an opposed, generally planar bottom surface 152. Disposed in the approximate center of the top surface 150 of the top substrate 148 is a plurality of top contacts 154 of the top substrate 148. Additionally, formed on the bottom surface 152 of the top substrate 148 is a plurality of bottom contacts 156 thereof. In the top substrate 148, some of the bottom contacts 156 are segregated into two sets, with the bottom contacts 156 of each such set extending along and in spaced relation to a respective one of an opposed pair of the peripheral edge segments defined by the top substrate 148. Though not shown, the top and bottom contacts 154, 156 are electrically connected to each other by conductive vias which extend through the top substrate 148. Those of ordinary skill in the art will recognize that each top contact 154 may be electrically connected to one or more bottom contacts 156 in any pattern or arrangement through the use of such conductive vias. The top and bottom contacts 154, 156 are also each preferably identically configured to each other, and fabricated from a suitable conductive material, as is any conductive via extending there between. Attached to a central area of the bottom surface 152 of the top substrate 148 is at least one, and preferably multiple electronic components 124.” Berry, [11:3-11:30].</p>
--	---

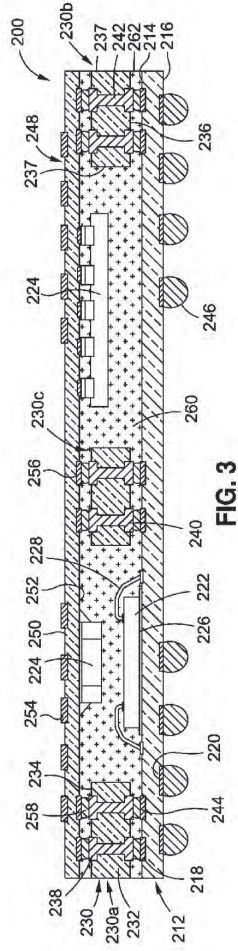
	 <p>FIG. 2</p> <p>Berry, FIG. 2</p> <p>“When the top substrate 248 is electrically and mechanically connected to the interposer 230 in the above-described manner, the electronic components 222, 224 as well as the conductive wires 228 are effectively positioned between the bottom and top substrates 212, 248, and more particularly the top surface 214 of the bottom substrate 212 and the bottom surface 252 of the top substrate 248.” Berry, [11:64-12:3].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom</p>	<p>Berry discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p>

package substrate and the top package substrate, wherein	<p>“In the semiconductor package 100, each bottom pad 140 in each of the first and second segments 130 a, 130 b is electrically connected to a respective one of the top contacts 118 of a corresponding set thereof by a solder ball 144. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 144. As seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the bottom substrate 112. Formed on each of the bottom contacts 120 of the bottom substrate 112 is a solder bump or solder ball 146. The semiconductor package 100 of the first embodiment further comprises a laminate top substrate 148 which is mechanically and electrically connected to the interposer 130 in a manner which will be described in more detail below.” Berry, [7:40-7:57].</p>  <p>FIG. 2</p> <p>Berry, FIG. 2</p> <p>“In the semiconductor package 100, each top pad 138 of each of the first and second segments 130 a, 130 b of the interposer 130 is electrically connected to a respective one of the bottom</p>
--	--

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>contacts 156 of a corresponding set thereof by a solder ball 158. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 158. As is also seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the top substrate 148. Thus, in addition to extending in generally co-planar relation to respective longitudinal side surfaces 137 of the first and second segments 130 a, 130 b, the peripheral edge segments defined by the top substrate 148 also extend in generally co-planar relation to respective ones of the peripheral edge segments defined by the bottom substrate 112. When the top substrate 148 is electrically and mechanically connected to the interposer 130 in the above-described manner, the electronic components 122, 124 as well as the conductive wires 128 are effectively positioned between the bottom and top substrates 112, 148, and more particularly the top surface 114 of the bottom substrate 112 and the bottom surface 152 of the top substrate 148.” Berry, [8:29-8:53].</p> <p>“The semiconductor package 200 further comprises an interposer 230 which is mounted and electrically connected to the top contacts 218 of the bottom substrate 212. It is contemplated that the interposer 230 may comprise separate first, second and third segments 230 a, 230 b, 230 c which are electrically connected to each of the top contacts 218 of respective ones of the three sets thereof. The first, second and third segments 230 a, 230 b, 230 c of the interposer 230 are identically configured to each other and, in the completed semiconductor package 200, extend in spaced, generally parallel relation to each other.” Berry, [10:17-10:27].</p> <p>“In the semiconductor package 200, each top pad 238 of each of the first, second and third segments 230 a, 230 b, 230 c of the interposer 230 is electrically connected to a respective</p>
--	---

one of the bottom contacts 256 of a corresponding set thereof by a solder ball 258. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 258. As is also seen in FIG. 3, such attachment is preferably facilitated such that one of the longitudinal side surfaces 237 of each of the first and second segments 230 a, 230 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the top substrate 248. Thus, in addition to extending in generally co-planar relation to respective longitudinal side surfaces 237 of the first and second segments 230 a, 230 b, the peripheral edge segments defined by the top substrate 248 also extend in generally co-planar relation to respective ones of the peripheral edge segments defined by the bottom substrate 212. When the top substrate 248 is electrically and mechanically connected to the interposer 230 in the above-described manner, the electronic components 222, 224 as well as the conductive wires 228 are effectively positioned between the bottom and top substrates 212, 248, and more particularly the top surface 214 of the bottom substrate 212 and the bottom surface 252 of the top substrate 248.” Berry, [11:46-12:3].



Berry, FIG. 3

“In the next step of the fabrication process shown in FIG. 4C, each of the top substrates 148 shown in FIG. 4A is mated and electrically connected to a respective one of the interposers

130 within the interposer strip 330. The mounting and electrical connection of each top substrate 148 to a respective interposer 130 is accomplished in the same manner described above in relation to the electrical connection of the top substrate 148 to the interposer 130 in the semiconductor package 100 shown in FIG. 2. In this regard, each of the solder balls 158 formed on respective ones of the bottom contacts 156 on each of the top substrates 148 is brought into direct contact with a respective one of the top pads 138 included in each of the interposers 130 of the interposer strip 330. Thereafter, a reflow process is completed as effectively electrically connects each of the top substrates 148 to a corresponding one of the interposers 130 within the interposer strip 330. Subsequent to the mounting and electrical connection of each of the top substrates 148 to respective ones of the interposers 130 within the interposer strip 330, a suitable encapsulant material or mold compound is injected between the top surface of the bottom substrate strip 312 and the bottom surface 152 of each of the top substrates 148 mounted and electrically connected to the interposer strip 330.” Berry, [13:62-14:17].

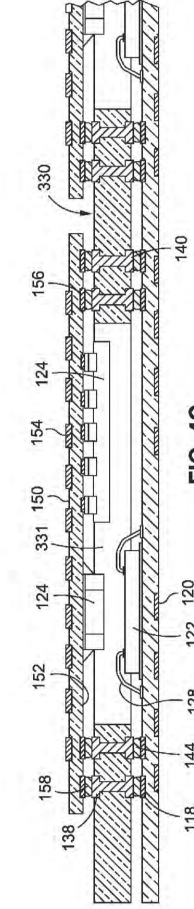


FIG. 4C

Berry, FIG. 4C

To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.D] the spacer connector comprises a core substrate;	<p>Berry discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The semiconductor package 10 further comprises an interposer 30 which is mounted and electrically connected to the top contacts 18 of the bottom substrate 12. It is contemplated that the interposer 30 may comprise a first segment 30 a which is electrically connected to each of the top contacts 18 of one of the sets thereof, and a separate second segment 30 b which is electrically connected to each of the top contacts 18 of the remaining set thereof.” Berry, [4:1-4:9].</p> <p>“Each of the interposer segments 30 a, 30 b of the interposer 30 comprises an interposer body 32 having a top surface 34, a bottom surface 36, an opposed pair of longitudinal side surfaces 37, and an opposed pair of lateral side surfaces.” Berry, [4:15-4:18].</p> <p>“The semiconductor package 100 further comprises an interposer 130 which is mounted and electrically connected to the top contacts 118 of the bottom substrate 112. It is contemplated that the interposer 130 may comprise a first segment 130 a which is electrically connected to each of the top contacts 118 of one of the sets thereof, and a separate second segment 130 b which is electrically connected to each of the top contacts 118 of the remaining set thereof.” Berry, [7:1-7:8].</p> <p>“The semiconductor package 200 further comprises an interposer 230 which is mounted and electrically connected to the top contacts 218 of the bottom substrate 212. It is contemplated</p>

that the interposer 230 may comprise separate first, second and third segments 230 a, 230 b, 230 c which are electrically connected to each of the top contacts 218 of respective ones of the three sets thereof.” Berry, [10:17-10:23].

“Each of the interposer segments 130 a, 130 b of the interposer 130 comprises an interposer body 132 having a top surface 134, a bottom surface 136, an opposed pair of longitudinal side surfaces 137, and an opposed pair of lateral side surfaces.” Berry, [10:28-10:32].

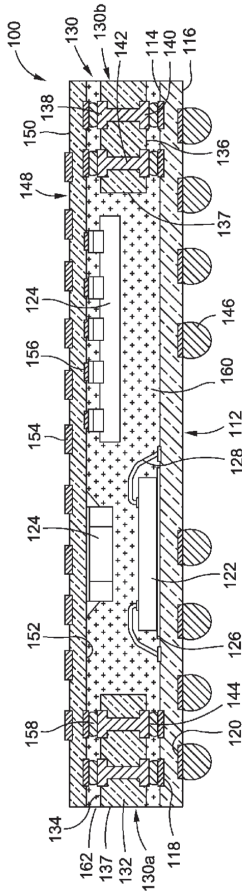


FIG. 2

Berry, FIG. 2

“Each of the interposer segments 230 a, 230 b, 230 c of the interposer 230 comprises an interposer body 232 having a top surface 234, a bottom surface 236, an opposed pair of longitudinal side surfaces 237, and an opposed pair of lateral side surfaces.” Berry, [10:28-10:31].

To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Berry discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Each of the interposer segments 30 a, 30 b of the interposer 30 comprises an interposer body 32 having a top surface 34, a bottom surface 36, an opposed pair of longitudinal side surfaces 37, and an opposed pair of lateral side surfaces. Disposed on the top surface 34 of the interposer body 32 of each of the first and second segments 30 a, 30 b is a plurality of top pads 38. Similarly, disposed on the bottom surface 36 of each of the first and second segments 30 a, 30 b is a plurality of bottom pads 40. The top and bottom pads 38, 40 disposed on the interposer body 32 of each of the first and second segments 30 a, 30 b are segregated into multiple pairs, with the top pad 38 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 40 of the same pair. The top and bottom pads 38, 40 of each pair within each of the first and second segments 30 a, 30 b are electrically connected to each other by one or more conductive vias 42 which extend through the interposer body 32 substantially perpendicularly between the top and bottom pads 38, 40 of the corresponding pair.” Berry, [4:15-4:32].</p>

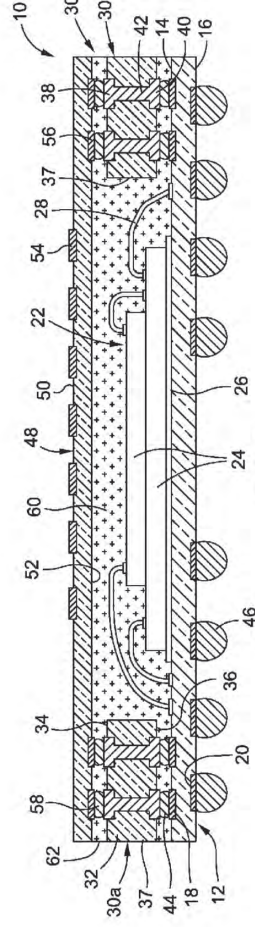


FIG. 1

Berry, FIG. 1

“The top and bottom pads 138, 140 disposed on the interposer body 132 of each of the first and second segments 130 a, 130 b are segregated into multiple pairs, with the top pad 138 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 140 of the same pair. The top and bottom pads 138, 140 of each pair within each of the first and second segments 130 a, 130 b are electrically connected to each other by one or more conductive vias 142 which extend through the interposer body 132 substantially perpendicularly between the top and bottom pads 138, 140 of the corresponding pair. The top and bottom pads 138, 140 of each pair are preferably identically configured to each other, and fabricated from a suitable conductive material, as is the conductive via(s) 142 extending therebetween. Those of ordinary skill in the art will recognize that the top and bottom pads 138, 140 of each pair need not necessarily be in exact vertical alignment, and that some degree of juxtaposition therebetween is contemplated to fall within the scope of the present invention.” Berry, [7:21-7:39].

“Each of the interposer segments 130 a, 130 b of the interposer 130 comprises an interposer body 132 having a top surface 134, a bottom surface 136, an opposed pair of longitudinal

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>side surfaces 137, and an opposed pair of lateral side surfaces. Disposed on the top surface 134 of the interposer body 132 of each of the first and second segments 130 a, 130 b is a plurality of top pads 138. Similarly, disposed on the bottom surface 136 of each of the first and second segments 130 a, 130 b is a plurality of bottom pads 140.” Berry, [10:28-10:36].</p> <p>“Each of the interposer segments 230 a, 230 b, 230 c of the interposer 230 comprises an interposer body 232 having a top surface 234, a bottom surface 236, an opposed pair of longitudinal side surfaces 237, and an opposed pair of lateral side surfaces. Disposed on the top surface 234 of the interposer body 232 of each of the first, second and third segments 230 a, 230 b, 230 c is a plurality of top pads 238. Similarly, disposed on the bottom surface 236 of each of the first, second and third segments 230 a, 230 b, 230 c is a plurality of bottom pads 240.” Berry, [10:28-10:36].</p> <p>“The top and bottom pads 238, 240 disposed on the interposer body 232 of each of the first, second and third segments 230 a, 230 b, 230 c are segregated into multiple pairs, with the top pad 238 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 240 of the same pair. The top and bottom pads 238, 240 of each pair within each of the first and second segments 230 a, 230 b are electrically connected to each other by one or more conductive vias 242 which extend through the interposer body 232 substantially perpendicularly between the top and bottom pads 238, 240 of the corresponding pair.” Berry, [10:37-10:47].</p>
--	---

a, 30 b are electrically connected to each other by one or more conductive vias 42 which extend through the interposer body 32 substantially perpendicularly between the top and bottom pads 38, 40 of the corresponding pair.” Berry, [4:19-4:32].

“Disposed on the top surface 134 of the interposer body 132 of each of the first and second segments 130 a, 130 b is a plurality of top pads 138. Similarly, disposed on the bottom surface 136 of each of the first and second segments 130 a, 130 b is a plurality of bottom pads 140. The top and bottom pads 138, 140 disposed on the interposer body 132 of each of the first and second segments 130 a, 130 b are segregated into multiple pairs, with the top pad 138 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 140 of the same pair. The top and bottom pads 138, 140 of each pair within each of the first and second segments 130 a, 130 b are electrically connected to each other by one or more conductive vias 142 which extend through the interposer body 132 substantially perpendicularly between the top and bottom pads 138, 140 of the corresponding pair.” Berry, [7:17-7:31].

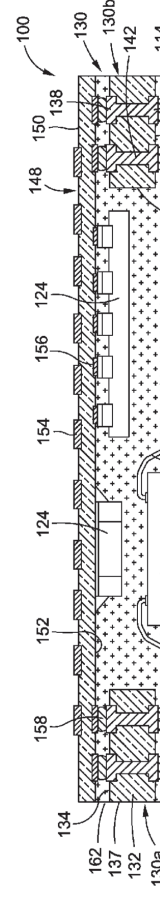


FIG. 2

Berry, FIG. 2

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“Disposed on the top surface 234 of the interposer body 232 of each of the first, second and third segments 230 a, 230 b, 230 c is a plurality of top pads 238. Similarly, disposed on the bottom surface 236 of each of the first, second and third segments 230 a, 230 b, 230 c is a plurality of bottom pads 240. The top and bottom pads 238, 240 disposed on the interposer body 232 of each of the first, second and third segments 230 a, 230 b, 230 c are segregated into multiple pairs, with the top pad 238 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 240 of the same pair. The top and bottom pads 238, 240 of each pair within each of the first and second segments 230 a, 230 b are electrically connected to each other by one or more conductive vias 242 which extend through the interposer body 232 substantially perpendicularly between the top and bottom pads 238, 240 of the corresponding pair.” Berry, [10:32-10:47].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Berry discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the semiconductor package 10, each bottom pad 40 in each of the first and second segments 30 a, 30 b is electrically connected to a respective one of the top contacts 18 of a corresponding set thereof by a solder ball 44.” Berry, [4:41-4:44].</p>

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“Formed on each of the bottom contacts 20 of the bottom substrate 12 is a solder bump or solder ball 46.” Berry, [4:52-4:54].</p> <p>“Each of the interposer segments 130 a, 130 b of the interposer 130 comprises an interposer body 132 having a top surface 134, a bottom surface 136, an opposed pair of longitudinal side surfaces 137, and an opposed pair of lateral side surfaces. Disposed on the top surface 134 of the interposer body 132 of each of the first and second segments 130 a, 130 b is a plurality of top pads 138. Similarly, disposed on the bottom surface 136 of each of the first and second segments 130 a, 130 b is a plurality of bottom pads 140. The top and bottom pads 138, 140 disposed on the interposer body 132 of each of the first and second segments 130 a, 130 b are segregated into multiple pairs, with the top pad 138 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 140 of the same pair. The top and bottom pads 138, 140 of each pair within each of the first and second segments 130 a, 130 b are electrically connected to each other by one or more conductive vias 142 which extend through the interposer body 132 substantially perpendicularly between the top and bottom pads 138, 140 of the corresponding pair. The top and bottom pads 138, 140 of each pair are preferably identically configured to each other, and fabricated from a suitable conductive material, as is the conductive via(s) 142 extending therebetween. Those of ordinary skill in the art will recognize that the top and bottom pads 138, 140 of each pair need not necessarily be in exact vertical alignment, and that some degree of juxtaposition therebetween is contemplated to fall within the scope of the present invention.” Berry, [7:13-7:39].</p>
--	--

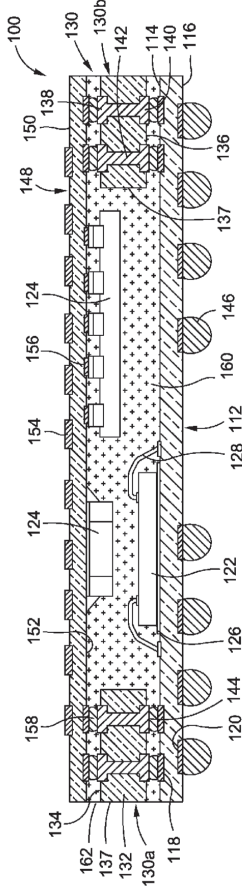


FIG. 2

Berry, FIG. 2

“In the semiconductor package 100, each bottom pad 140 in each of the first and second segments 130 a, 130 b is electrically connected to a respective one of the top contacts 118 of a corresponding set thereof by a solder ball 144.” Berry, [7:40-7:43].

“Formed on each of the bottom contacts 120 of the bottom substrate 112 is a solder bump or solder ball 146.” Berry, [7:51-7:53].

“In the semiconductor package 200, each bottom pad 240 in each of the first, second and third segments 230 a, 230 b, 230 c is electrically connected to a respective one of the top contacts 218 of a corresponding set thereof by a solder ball 244.” Berry, [10:56-10:59].

To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Berry discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In the semiconductor package 10, each top pad 38 of each of the first and second segments 30 a, 30 b of the interposer 30 is electrically connected to a respective one of the bottom contacts 56 of a corresponding set thereof by a solder ball 58. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 58. As is also seen in FIG. 1, such attachment is preferably facilitated such that one of the longitudinal side surfaces 37 of each of the first and second segments 30 a, 30 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the top substrate 48.” Berry, [5:14-5:25].</p> <p>“The top and bottom pads 138, 140 disposed on the interposer body 132 of each of the first and second segments 130 a, 130 b are segregated into multiple pairs, with the top pad 138 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 140 of the same pair. The top and bottom pads 138, 140 of each pair within each of the first and second segments 130 a, 130 b are electrically connected to each other by one or more conductive vias 142 which extend through the interposer body 132 substantially perpendicularly between the top and bottom pads 138, 140 of the corresponding pair.” Berry, [7:21-7:31].</p> <p>“Additionally, formed on the bottom surface 152 of the top substrate 148 is a plurality of bottom contacts 156 thereof. In the top substrate 148, some of the bottom contacts 156 are</p>
--	---

	<p>segregated into two sets, with the bottom contacts 156 of each such set extending along and in spaced relation to a respective one of an opposed pair of the peripheral edge segments defined by the top substrate 148.” Berry, [7:64-8:3].</p> <p>“In the semiconductor package 100, each top pad 138 of each of the first and second segments 130 a, 130 b of the interposer 130 is electrically connected to a respective one of the bottom contacts 156 of a corresponding set thereof by a solder ball 158. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 158. As is also seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally coplanar relation to a respective one of the sides or peripheral edge segments defined by the top substrate 148.” Berry, [8:29-8:41].</p> <div></div> <p style="text-align: center;">FIG. 2</p> <p>Berry, FIG. 2</p> <p>“In the semiconductor package 200, each top pad 238 of each of the first, second and third segments 230 a, 230 b, 230 c of the interposer 230 is electrically connected to a respective</p>
--	---

one of the bottom contacts 256 of a corresponding set thereof by a solder ball 258. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 258. As is also seen in FIG. 3, such attachment is preferably facilitated such that one of the longitudinal side surfaces 237 of each of the first and second segments 230 a, 230 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the top substrate 248.” Berry, [11:46-11:58].

“In the next step of the fabrication process shown in FIG. 4C, each of the top substrates 148 shown in FIG. 4A is mated and electrically connected to a respective one of the interposers 130 within the interposer strip 330. The mounting and electrical connection of each top substrate 148 to a respective interposer 130 is accomplished in the same manner described above in relation to the electrical connection of the top substrate 148 to the interposer 130 in the semiconductor package 100 shown in FIG. 2. In this regard, each of the solder balls 158 formed on respective ones of the bottom contacts 156 on each of the top substrates 148 is brought into direct contact with a respective one of the top pads 138 included in each of the interposers 130 of the interposer strip 330.” Berry, [13:62-14:7].

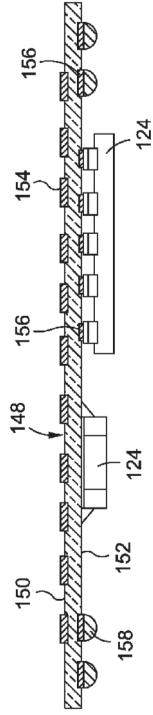


FIG. 4A

Berry, FIG. 4A

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Berry discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“The top and bottom pads 38, 40 of each pair within each of the first and second segments 30 a, 30 b are electrically connected to each other by one or more conductive vias 42 which extend through the interposer body 32 substantially perpendicularly between the top and bottom pads 38, 40 of the corresponding pair.” Berry, [4:28-4:33].</p> <p>“In the semiconductor package 10, each bottom pad 40 in each of the first and second segments 30 a, 30 b is electrically connected to a respective one of the top contacts 18 of a corresponding set thereof by a solder ball 44. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 44. As seen in FIG. 1, such attachment is preferably facilitated such that one of the longitudinal side surfaces 37 of each of the first and second segments 30 a, 30 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the bottom substrate 12.” Berry, [4:41-4:52].</p> <p>“Disposed on the top surface 14 is a plurality of top contacts 18 of the bottom substrate 12. In the bottom substrate 12, the top contacts 18 are segregated into two sets, with the top</p>

contacts 18 of each set extending along and in spaced relation to a respective one of an opposed pair of the peripheral edge segments defined by the bottom substrate 12.” Berry, [6:27-6:33].

“In the semiconductor package 100, each bottom pad 140 in each of the first and second segments 130 a, 130 b is electrically connected to a respective one of the top contacts 118 of a corresponding set thereof by a solder ball 144. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 144. As seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the bottom substrate 112.” Berry, [10:56-11:1].

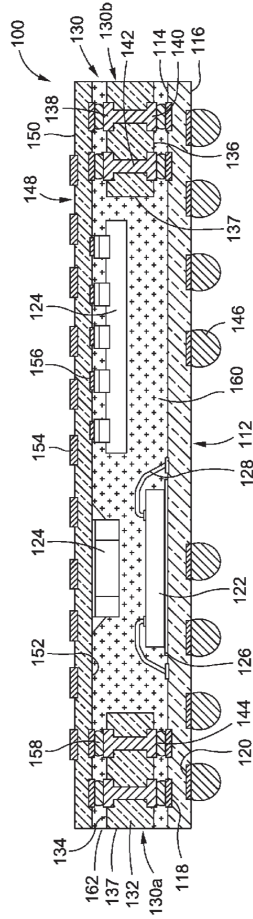


FIG. 2

Berry, FIG. 2

“In the semiconductor package 200, each bottom pad 240 in each of the first, second and third segments 230 a, 230 b, 230 c is electrically connected to a respective one of the top

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>contacts 218 of a corresponding set thereof by a solder ball 244. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 244. As seen in FIG. 3, such attachment is preferably facilitated such that one of the longitudinal side surfaces 237 of each of the first and second segments 230 a, 230 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the bottom substrate 212.” Berry, [10:56-11:1].</p> <p>“The electrical connection of the interposer strip 330 to the top contacts 118 of the bottom substrate strip 312 is preferably accomplished by initially forming solder balls 144 upon respective ones of the top contacts 118, and completing a reflow process subsequent to the abutment of the bottom pads 140 of each of the interposers 130 within the interposer strip 330 against respective ones of the solder balls 144.” Berry, [13:51-13:58].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Berry discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p>

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“In the semiconductor package 10, each bottom pad 40 in each of the first and second segments 30 a, 30 b is electrically connected to a respective one of the top contacts 18 of a corresponding set thereof by a solder ball 44. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 44.” Berry, [4:41-4:47].</p> <p>“Though not shown, the top and bottom contacts 154, 156 are electrically connected to each other by conductive vias which extend through the top substrate 148. Those of ordinary skill in the art will recognize that each top contact 154 may be electrically connected to one or more bottom contacts 156 in any pattern or arrangement through the use of such conductive vias.” Berry, [5:4-5:10].</p> <p>“The top and bottom pads 138, 140 of each pair within each of the first and second segments 130 a, 130 b are electrically connected to each other by one or more conductive vias 142 which extend through the interposer body 132 substantially perpendicularly between the top and bottom pads 138, 140 of the corresponding pair.” Berry, [7:26-7:31].</p> <p>“In the semiconductor package 100, each top pad 138 of each of the first and second segments 130 a, 130 b of the interposer 130 is electrically connected to a respective one of the bottom contacts 156 of a corresponding set thereof by a solder ball 158. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 158. As is also seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the top substrate 148. Thus, in addition to extending in generally co-planar relation to respective longitudinal side surfaces 137 of the first and second segments 130 a, 130 b, the peripheral</p>
--	--

edge segments defined by the top substrate 148 also extend in generally co-planar relation to respective ones of the peripheral edge segments defined by the bottom substrate 112. When the top substrate 148 is electrically and mechanically connected to the interposer 130 in the above-described manner, the electronic components 122, 124 as well as the conductive wires 128 are effectively positioned between the bottom and top substrates 112, 148, and more particularly the top surface 114 of the bottom substrate 112 and the bottom surface 152 of the top substrate 148.” Berry, [8:29-8:53].

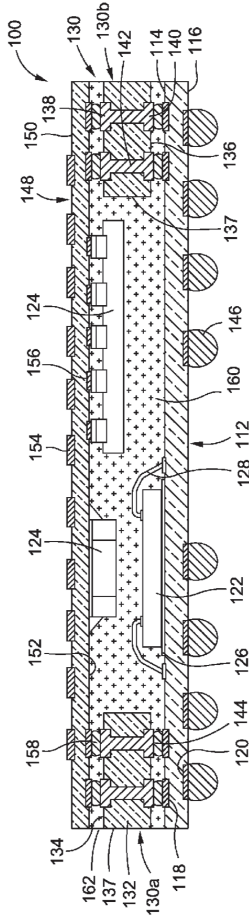


FIG. 2

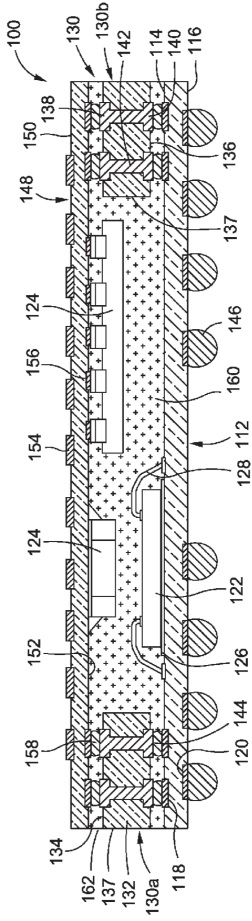
Berry, FIG. 2

“Though not shown in FIG. 2, the top and bottom contacts 118, 120 are electrically connected to each other in a prescribed pattern or arrangement by conductive vias which extend through the bottom substrate 112.” Berry, [9:56-9:59].

“In the semiconductor package 100, each bottom pad 140 in each of the first and second segments 130 a, 130 b is electrically connected to a respective one of the top contacts 118 of a corresponding set thereof by a solder ball 144. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>employed as an alternative to the use of the solder balls 144. As seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the bottom substrate 112.” Berry, [10:56-11:1].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Berry discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Attached to a central area of the top surface 14 of the bottom substrate 12 is at least one electronic component of the semiconductor package 10, and more particularly a die stack 22.” Berry, [3:36-3:39].</p> <p>“When the top substrate 48 is electrically and mechanically connected to the interposer 30 in the above-described manner, the die stack 22 as well as the conductive wires 28 are effectively positioned between the bottom and top substrates 12, 48, and more particularly the top surface 14 of the bottom substrate 12 and the bottom surface 52 of the top substrate 48.” Berry, [5:31-5:37].</p>

	<p>“Attached to a central area of the top surface 114 of the bottom substrate 100, which is preferably a semiconductor component 122 of the semiconductor package 100, which is preferably a semiconductor die.” Berry, [6:43-6:46].</p> <p>“When the top substrate 148 is electrically and mechanically connected to the interposer 130 in the above-described manner, the electronic components 122, 124 as well as the conductive wires 128 are effectively positioned between the bottom and top substrates 112, 148, and more particularly the top surface 114 of the bottom substrate 112 and the bottom surface 152 of the top substrate 148.” Berry, [8:47-8:53].</p> <div></div> <p>FIG. 2</p> <p>Berry, FIG. 2</p> <p>“Attached to a central area of the top surface 214 of the bottom substrate 212 is at least one electronic component 222 of the semiconductor package 200, which is preferably a semiconductor die.” Berry, [9:60-9:63].</p> <p>“When the top substrate 248 is electrically and mechanically connected to the interposer 230 in the above-described manner, the electronic components 222, 224 as well as the conductive</p>
--	---

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>wires 228 are effectively positioned between the bottom and top substrates 212, 248, and more particularly the top surface 214 of the bottom substrate 212 and the bottom surface 252 of the top substrate 248.” Berry, [11:64-12:3].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Berry discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Attached to a central area of the top surface 14 of the bottom substrate 12 is at least one electronic component of the semiconductor package 10, and more particularly a die stack 22. The die stack 22 comprises a plurality of individual semiconductor dies 24 which are arranged in a stacked configuration. In this regard, the uppermost semiconductor die 24 in the die stack 22 is secured to the semiconductor die 24 below it by a layer of suitable adhesive. Similarly, the attachment of the lowermost semiconductor die 24 in the die stack 22 to the top surface 14 of the bottom substrate 12 is facilitated by an adhesive layer 26.” Berry, [3:36-3:46].</p> <p>“In the semiconductor package 10, the die stack 22, wires 28 and portions of the first and second segments 30 a, 30 b of the interposer 30 are encapsulated or covered by an encapsulant material which is injected between the bottom and top substrates 12, 48. Such encapsulant material, upon hardening, forms a package body 60 of the semiconductor package 10. Also</p>

fully covered by the package body 60 are the solder balls 44, 58 used to effectuate the electrical connection between the first and second segments 30 a, 30 b of the interposer 30 and the bottom and top substrates 12, 48.” Berry, [5:38-5:47].

“Attached to a central area of the top surface 114 of the bottom substrate 100, is at least one electronic component 122 of the semiconductor package 100, which is preferably a semiconductor die. The attachment of the electronic component 122 to the top surface 114 of the bottom substrate 112 is facilitated by an adhesive layer 126.” Berry, [6:43-6:48].

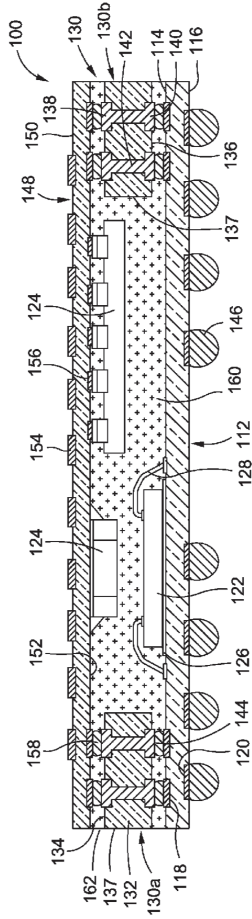
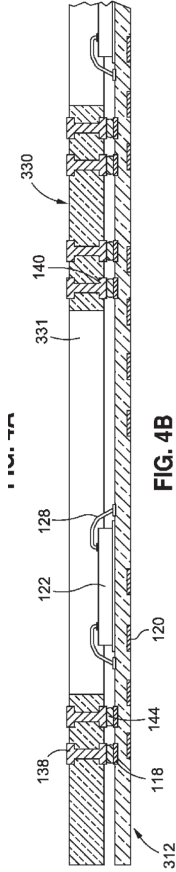


FIG. 2

Berry, FIG. 2

“When the top substrate 148 is electrically and mechanically connected to the interposer 130 in the above-described manner, the electronic components 122, 124 as well as the conductive wires 128 are effectively positioned between the bottom and top substrates 112, 148, and more particularly the top surface 114 of the bottom substrate 112 and the bottom surface 152 of the top substrate 148.” Berry, [8:47-8:53].

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“Attached to a central area of the top surface 214 of the bottom substrate 212 is at least one electronic component 222 of the semiconductor package 200, which is preferably a semiconductor die. The attachment of the electronic component 222 to the top surface 214 of the bottom substrate 212 is facilitated by an adhesive layer 226.” Berry, [9:60-9:65].</p> <p>“As further shown in FIG. 4B, in addition to the interposer strip 330 being electrically connected to the bottom substrate strip 312 in the aforementioned manner, one or more electronic components 122 is/are attached to a prescribed location of the top surface of the bottom substrate strip 312.” Berry, [13:45-13:49].</p>  <p>FIG. 4B</p> <p>Berry, FIG. 4B</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Berry discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“In the bottom substrate 12, the top contacts 18 are segregated into two sets, with the top contacts 18 of each set extending along and in spaced relation to a respective one of an opposed pair of the peripheral edge segments defined by the bottom substrate 12.” Berry, [3:26-3:30].</p> <p>“As indicated above, in the semiconductor package 100, two sets of the top contacts 118 are provided on the bottom substrate 112, with the top contacts 118 of each set extending along a respective one of an opposed pair of side surfaces 162 defined by the package body 160.” Berry, [5:61-5:65].</p> <p>“Attached to a central area of the top surface 114 of the bottom substrate 112 is at least one electronic component 122 of the semiconductor package 100, which is preferably a semiconductor die. The attachment of the electronic component 122 to the top surface 114 of the bottom substrate 112 is facilitated by an adhesive layer 126. Those of ordinary skill in the art will recognize that the electronic component 122 may alternatively comprise the die stack 22 described above in relation to the semiconductor package 10. In the semiconductor package 100, the pads or terminals of the electronic component 122 are electrically connected to at least some of the top contacts 118 through the use of conductive wires 128. More particularly, in the semiconductor package 100, it is contemplated that the conductive wires 128 may extend from the electronic component 122 to conductive traces or the like which are disposed on the top surface 114 and in turn electrically connected to the top contacts 118 in a prescribed pattern or arrangement.” Berry, [6:43-6:59].</p> <p>“The semiconductor package 100 further comprises an interposer 130 which is mounted and electrically connected to the top contacts 118 of the bottom substrate 112. It is contemplated that the interposer 130 may comprise a first segment 130 a which is electrically connected to each of the top contacts 118 of one of the sets thereof, and a separate second segment 130 b</p>
--	---

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>which is electrically connected to each of the top contacts 118 of the remaining set thereof. The first and second segments 130 a, 130 b of the interposer 130 are identically configured to each other and, in the completed semiconductor package 100, extend in spaced, generally parallel relation to each other.” Berry, [7:1-7:12].</p> <p>Claim 2, U.S. Patent No. 9859202</p>
--	--

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced	Berry discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

downwardly from the bottom surface of the top package substrate.	<p><i>See, e.g.:</i></p> <p>“When the top substrate 48 is electrically and mechanically connected to the interposer 30 in the above-described manner, the die stack 22 as well as the conductive wires 28 are effectively positioned between the bottom and top substrates 12, 48, and more particularly the top surface 14 of the bottom substrate 12 and the bottom surface 52 of the top substrate 48.” Berry, [5:31-5:37].</p> <p>“In the semiconductor package 10, the die stack 22, wires 28 and portions of the first and second segments 30 a, 30 b of the interposer 30 are encapsulated or covered by an encapsulant material which is injected between the bottom and top substrates 12, 48.” Berry, [5:38-5:42].</p> <p>“When the top substrate 148 is electrically and mechanically connected to the interposer 130 in the above-described manner, the electronic components 122, 124 as well as the conductive wires 128 are effectively positioned between the bottom and top substrates 112, 148, and more particularly the top surface 114 of the bottom substrate 112 and the bottom surface 152 of the top substrate 148.” Berry, [8:47-8:53].</p>
--	---

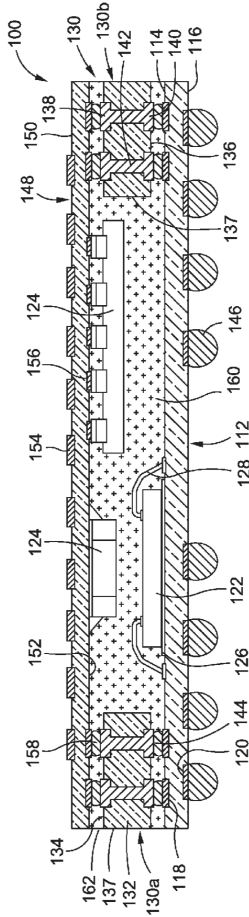


FIG. 2

Berry, FIG. 2

“In the semiconductor package 100, the electronic components 122, 124, wires 128 and portions of the first and second segments 130 a, 130 b of the interposer 130 are encapsulated or covered by an encapsulant material which is injected between the bottom and top substrates 112, 148. Such encapsulant material, upon hardening, forms a package body 160 of the semiconductor package 100.” Berry, [8:54-8:60].

“When the top substrate 248 is electrically and mechanically connected to the interposer 230 in the above-described manner, the electronic components 222, 224 as well as the conductive wires 228 are effectively positioned between the bottom and top substrates 212, 248, and more particularly the top surface 214 of the bottom substrate 212 and the bottom surface 252 of the top substrate 248.” Berry, [11:64-12:3].

“In the semiconductor package 200, the electronic components 222, 224, wires 228, portions of the first and second segments 230 a, 230 b of the interposer 230, and the entirety of the third segment 230 c of the interposer 230 are encapsulated or covered by an encapsulant

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>material which is injected between the bottom and top substrates 212, 248.” Berry, [12:8-12:13].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Berry discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“The semiconductor package 10 of the first embodiment further comprises a laminate top substrate 48 which is mechanically and electrically connected to the interposer 30 in a manner which will be described in more detail below. The top substrate 48 also has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the top substrate 48 defines a generally planar top surface 50 and an opposed, generally planar bottom surface 52. Disposed in the approximate center of the top surface 50 of the top substrate 48 is a plurality of top contacts 54 of the top substrate 48.” Berry, [4:55-4:65].</p>

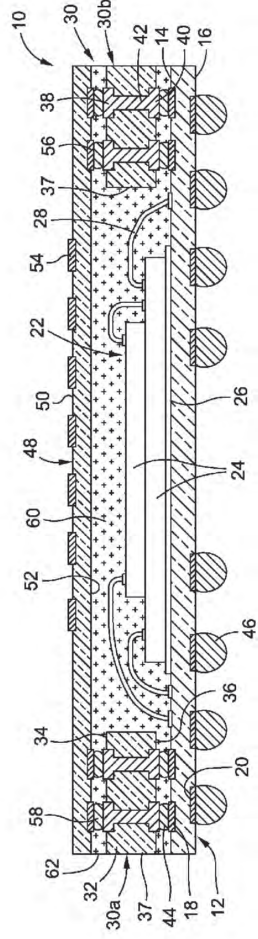


FIG. 1

Berry, FIG. 1

“Those of ordinary skill in the art will recognize that each top contact 54 may be electrically connected to one or more bottom contacts 56 in any pattern or arrangement through the use of such conductive vias.” Berry, [5:7-5:10].

“The top contacts 54 of the top substrate 48 provide top side routing also known as a ‘lands-over-top’ feature in the completed semiconductor package 10.” Berry, [6:17-6:20].

To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Berry discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The top and bottom pads 138, 140 disposed on the interposer body 132 of each of the first and second segments 130 a, 130 b are segregated into multiple pairs, with the top pad 138 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 140 of the same pair. The top and bottom pads 138, 140 of each pair within each of the first and second segments 130 a, 130 b are electrically connected to each other by one or more conductive vias 142 which extend through the interposer body 132 substantially perpendicularly between the top and bottom pads 138, 140 of the corresponding pair.” Berry, [7:21-7:31].</p> <p align="center">FIG. 2</p>

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>Berry, FIG. 2</p> <p>“The top and bottom pads 138, 140 of each pair are preferably identically configured to each other, and fabricated from a suitable conductive material, as is the conductive via(s) 142 extending therebetween. Those of ordinary skill in the art will recognize that the top and bottom pads 138, 140 of each pair need not necessarily be in exact vertical alignment, and that some degree of juxtaposition therebetween is contemplated to fall within the scope of the present invention.” Berry, [7:32-7:39].</p> <p>“As seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the bottom substrate 112.” Berry, [7:47-7:51].</p> <p>“In the semiconductor package 100, each top pad 138 of each of the first and second segments 130 a, 130 b of the interposer 130 is electrically connected to a respective one of the bottom contacts 156 of a corresponding set thereof by a solder ball 158. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 158.” Berry, [8:29-8:36].</p> <p>“As is also seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the top substrate 148. Thus, in addition to extending in generally co-planar relation to respective longitudinal side surfaces 137 of the first and second segments 130 a, 130 b, the peripheral edge segments defined by the top substrate 148 also extend in generally co-planar</p>
--	---

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>relation to respective ones of the peripheral edge segments defined by the bottom substrate 112.” Berry, [8:36-8:47].</p> <p>“In the semiconductor package 100, each bottom pad 140 in each of the first and second segments 130 a, 130 b is electrically connected to a respective one of the top contacts 118 of a corresponding set thereof by a solder ball 144. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 144.” Berry, [10:56-10:63].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Berry discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

<p>ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>“The top and bottom pads 38, 40 of each pair within each of the first and second segments 30 a, 30 b are electrically connected to each other by one or more conductive vias 42 which extend through the interposer body 32 substantially perpendicularly between the top and bottom pads 38, 40 of the corresponding pair.” Berry, [4:28-4:33].</p> <p>“In the semiconductor package 10, each bottom pad 40 in each of the first and second segments 30 a, 30 b is electrically connected to a respective one of the top contacts 18 of a corresponding set thereof by a solder ball 44. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 44. As seen in FIG. 1, such attachment is preferably facilitated such that one of the longitudinal side surfaces 37 of each of the first and second segments 30 a, 30 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the bottom substrate 12.” Berry, [4:41-4:52].</p> <p>“In the semiconductor package 10, each top pad 38 of each of the first and second segments 30 a, 30 b of the interposer 30 is electrically connected to a respective one of the bottom contacts 56 of a corresponding set thereof by a solder ball 58. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 58.” Berry, [5:14-5:21].</p> <p>“The top and bottom pads 138, 140 of each pair within each of the first and second segments 130 a, 130 b are electrically connected to each other by one or more conductive vias 142 which extend through the interposer body 132 substantially perpendicularly between the top and bottom pads 138, 140 of the corresponding pair.” Berry, [7:26-7:31].</p>
---	---

“In the semiconductor package 100, each bottom pad 140 in each of the first and second segments 130 a, 130 b is electrically connected to a respective one of the top contacts 118 of a corresponding set thereof by a solder ball 144. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 144. As seen in FIG. 2, such attachment is preferably facilitated such that one of the longitudinal side surfaces 137 of each of the first and second segments 130 a, 130 b extends in generally co-planar relation to a respective one of the sides or peripheral edge segments defined by the bottom substrate 112. Formed on each of the bottom contacts 120 of the bottom substrate 112 is a solder bump or solder ball 146. The semiconductor package 100 of the first embodiment further comprises a laminate top substrate 148 which is mechanically and electrically connected to the interposer 130 in a manner which will be described in more detail below. The top substrate 148 also has a generally quadrangular configuration defining four (4) peripheral edge segments. In addition, the top substrate 148 defines a generally planar top surface 150 and an opposed, generally planar bottom surface 152.” Berry, [7:40-7:61].

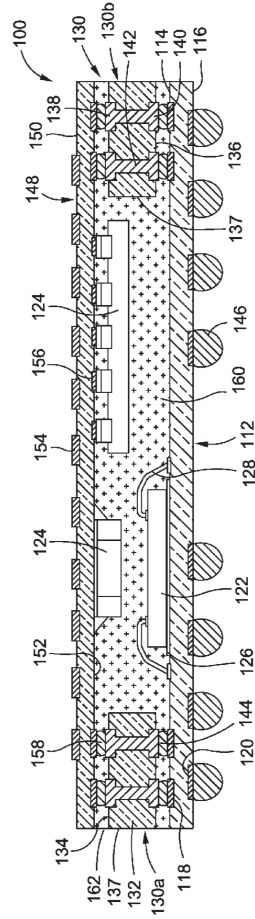


FIG. 2

Berry, FIG. 2

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“In the semiconductor package 100, each top pad 138 of each of the first and second segments 130 a, 130 b of the interposer 130 is electrically connected to a respective one of the bottom contacts 156 of a corresponding set thereof by a solder ball 158. However, those of ordinary skill in the art will recognize that solder paste, conductive adhesive, or other suitable materials may be employed as an alternative to the use of the solder balls 158.” Berry, [8:29-8:36].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the bottom ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Berry discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

“Similarly, disposed on the bottom surface 36 of each of the first and second segments 30 a, 30 b is a plurality of bottom pads 40. The top and bottom pads 38, 40 disposed on the interposer body 32 of each of the first and second segments 30 a, 30 b are segregated into multiple pairs, with the top pad 38 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 40 of the same pair. The top and bottom pads 38, 40 of each pair within each of the first and second segments 30 a, 30 b are electrically connected to each other by one or more conductive vias 42 which extend through the interposer body 32 substantially perpendicularly between the top and bottom pads 38, 40 of the corresponding pair. The top and bottom pads 38, 40 of each pair are preferably identically configured to each other, and fabricated from a suitable conductive material, as is the conductive via(s) 42 extending therebetween. Those of ordinary skill in the art will recognize that the top and bottom pads 38, 40 of each pair need not necessarily be in exact vertical alignment, and that some degree of juxtaposition therebetween is contemplated to fall within the scope of the present invention. In the semiconductor package 10, each bottom pad 40 in each of the first and second segments 30 a, 30 b is electrically connected to a respective one of the top contacts 18 of a corresponding set thereof by a solder ball 44.” Berry, [4:21-4:44].

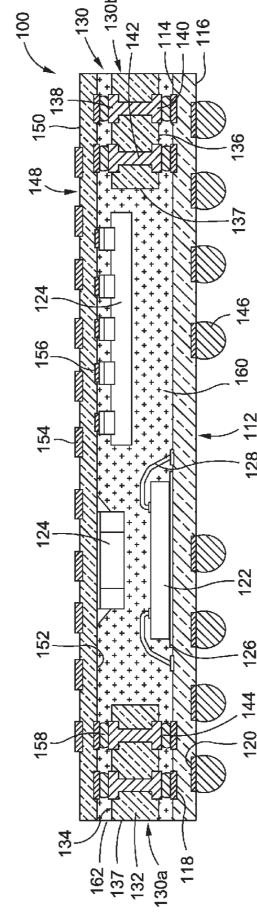


FIG. 2

Berry, FIG. 2

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“In the semiconductor package 10, each top pad 38 of each of the first and second segments 30 a, 30 b of the interposer 30 is electrically connected to a respective one of the bottom contacts 56 of a corresponding set thereof by a solder ball 58.” Berry, [5:14-5:17].</p> <p>“Similarly, disposed on the bottom surface 136 of each of the first and second segments 130 a, 130 b is a plurality of bottom pads 140. The top and bottom pads 138, 140 disposed on the interposer body 132 of each of the first and second segments 130 a, 130 b are segregated into multiple pairs, with the top pad 138 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 140 of the same pair. The top and bottom pads 138, 140 of each pair within each of the first and second segments 130 a, 130 b are electrically connected to each other by one or more conductive vias 142 which extend through the interposer body 132 substantially perpendicularly between the top and bottom pads 138, 140 of the corresponding pair. The top and bottom pads 138, 140 of each pair are preferably identically configured to each other, and fabricated from a suitable conductive material, as is the conductive via(s) 142 extending therebetween. Those of ordinary skill in the art will recognize that the top and bottom pads 138, 140 of each pair need not necessarily be in exact vertical alignment, and that some degree of juxtaposition therebetween is contemplated to fall within the scope of the present invention. In the semiconductor package 100, each bottom pad 140 in each of the first and second segments 130 a, 130 b is electrically connected to a respective one of the top contacts 118 of a corresponding set thereof by a solder ball 144.” Berry, [7:19-7:43].</p> <p>“In the semiconductor package 100, each top pad 138 of each of the first and second segments 130 a, 130 b of the interposer 130 is electrically connected to a respective one of the bottom contacts 156 of a corresponding set thereof by a solder ball 158.” Berry, [8:29-8:33].</p>
--	---

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

	<p>“Similarly, disposed on the bottom surface 236 of each of the first, second and third segments 230 a, 230 b, 230 c is a plurality of bottom pads 240. The top and bottom pads 238, 240 disposed on the interposer body 232 of each of the first, second and third segments 230 a, 230 b, 230 c are segregated into multiple pairs, with the top pad 238 of each pair being disposed in spaced, substantial vertical alignment with the bottom pad 240 of the same pair. The top and bottom pads 238, 240 of each pair within each of the first and second segments 230 a, 230 b are electrically connected to each other by one or more conductive vias 242 which extend through the interposer body 232 substantially perpendicularly between the top and bottom pads 238, 240 of the corresponding pair. The top and bottom pads 238, 240 of each pair are preferably identically configured to each other, and fabricated from a suitable conductive material, as is the conductive via(s) 242 extending therebetween. Those of ordinary skill in the art will recognize that the top and bottom pads 238, 240 of each pair need not necessarily be in exact vertical alignment, and that some degree of juxtaposition therebetween is contemplated to fall within the scope of the present invention. In the semiconductor package 200, each bottom pad 240 in each of the first, second and third segments 230 a, 230 b, 230 c is electrically connected to a respective one of the top contacts 218 of a corresponding set thereof by a solder ball 244.” Berry, [10:34-10:59].</p> <p>“In the semiconductor package 200, each top pad 238 of each of the first, second and third segments 230 a, 230 b, 230 c of the interposer 230 is electrically connected to a respective one of the bottom contacts 256 of a corresponding set thereof by a solder ball 258.” Berry, [11:46-11:50].</p> <p>To the extent Plaintiff contends that Berry fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-2 - Invalidity of U.S. Patent No. 9859202 in view of Berry - U.S. Patent No. 7687899

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

U.S. Patent Publication No. 20130182402 (“Chen '402”) is titled PoP Structures Including Through-Assembly Via Modules and lists Chih-Hua Chen, Chen-Shien Chen, and Ching-Wen Hsiao as inventors. Chen '402 is assigned to Taiwan Semiconductor Manufacturing Company, Ltd. Chen '402 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the '202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff's apparent infringement theory.² Chen '402 is a U.S. patent publication that was filed January 18, 2012 and published July 18, 2013. Chen '402 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Chen '402, or otherwise rendered obvious by disclosures and teachings of Chen '402, including under TopWire's apparent interpretation of the Asserted Claims as Samsung understands them from TopWire's Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Chen '402 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Chen '402 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung's other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung's Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Chen '402, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire's March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court's order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire's apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung's interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Chen '402 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Chen '402 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Chen '402 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Chen '402 discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“A Package-on-Package (PoP) structure and the methods of forming the same are provided in accordance with various exemplary embodiments.” Chen '402, [0008].</p> <p>“FIGS. 1 through 9 are cross-sectional views and a top view of intermediate stages in the manufacturing of a Package-on-Package (PoP) structure in accordance with some exemplary embodiments. FIG. 1 illustrates carrier 20 and release layer 22 on carrier 20. Carrier 20 may</p>

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>be a glass carrier, a ceramic carrier, or the like. Release layer 22 may be formed of an adhesive such as an Ultra-Violet (UV) glue. Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22. The bottom surfaces of package component 24 and TAV modules 28 are in contact with the top surface of release layer 22, and are level with each other. The position of package component 24 and TAV modules 28 are accurately aligned to desirable locations, so that the subsequent formed redistribution lines may electrically couple to metal posts 26 and 30. In some embodiments, package component 24 includes one or a plurality of device dies. For example, package component 24 may include a Central Computing Unit (CPU) die or another type of logic die having logic circuits. In alternative embodiments, package component 24 includes a plurality of memory dies stacked together (please refer to FIG. 11). In the embodiments wherein package component 24 is a device die, package component 24 may include semiconductor substrate 25 and active devices (such as transistors) 27 at a top surface of semiconductor substrate 25. The bottom surface of semiconductor substrate 25 is thus in contact with release layer 22. Semiconductor substrate 25 may be free from through-substrate vias formed therein, although through-substrate vias may also be formed to penetrate through semiconductor substrate 25. Package component 24 may also be a package that includes device die(s), interposer(s), package substrate(s) (not shown), and/or the like. Metal posts 26 (such as copper posts) are formed as a top portion of package component 24.” Chen ’402, [0009].</p>
--	--

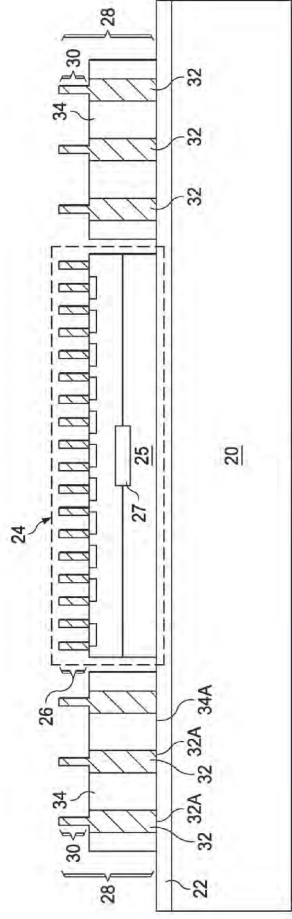


FIG. 1

Chen '402, Fig. 1

“TAV modules 28 are integrated modules that are pre-formed before being placed on release layer 22. TAV modules 28 include substrate 34, which may be a semiconductor substrate such as a silicon substrate. Alternatively, substrate 34 is a dielectric substrate such as a glass substrate. Through-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34. Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like. In some embodiments, bottom ends 32A of through-substrate vias 32 are level with the bottom surface 34A of substrate 34. Accordingly, bottom ends 32A of through-substrate vias 32 may be in contact with release layer 22. TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal post 26 and 30 are substantially level with each other.” Chen '402, [0010].

“FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, TAV modules 28 are disposed on opposite sides of package component 24.

Although two TAV modules 28 are illustrated, there may be one or more than two TAV modules 28. TAV modules 28 may have an identical structure. Alternatively, TAV modules 28 may have different structures with different counts of metal posts 30, different layouts of metal posts 30, different sizes, and/or different materials. The plurality of TAV modules 28 may be laid out on release layer 22 with any layout.” Chen ’402, [0012].

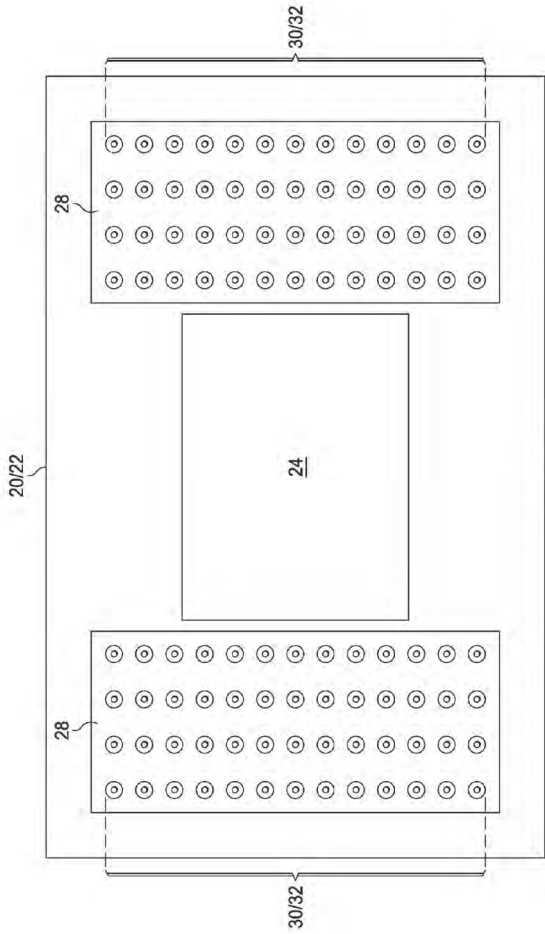


FIG. 2

Chen ’402, Fig. 2

“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also

interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer. In some exemplary embodiments, the formation of connectors 44 includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls. In alternative embodiments, the formation of connectors 44 includes performing a plating step to form solder regions on RDLs 42, and then reflowing the solder regions. Connectors 44 may also include metal pillars, or metal pillars and solder caps, which may also be formed through plating. Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen ’402, [0014].

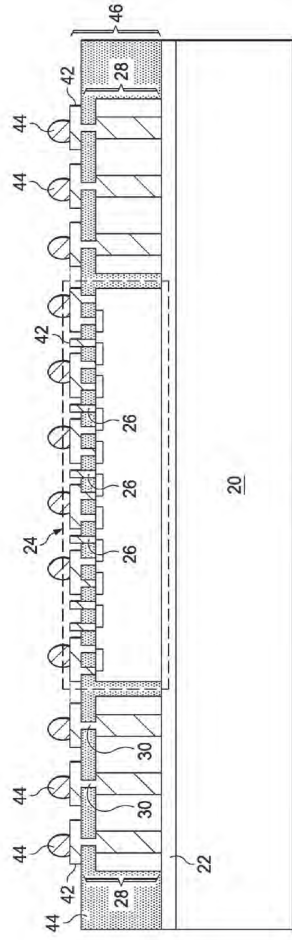


FIG. 4

Chen '402, Fig. 4

“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are

used to electrically couple the circuit devices in package component 62 to package component 56.” Chen ’402, [0019].

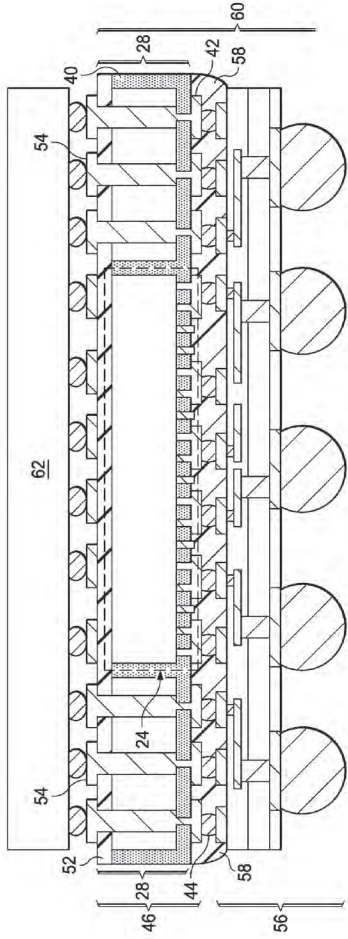
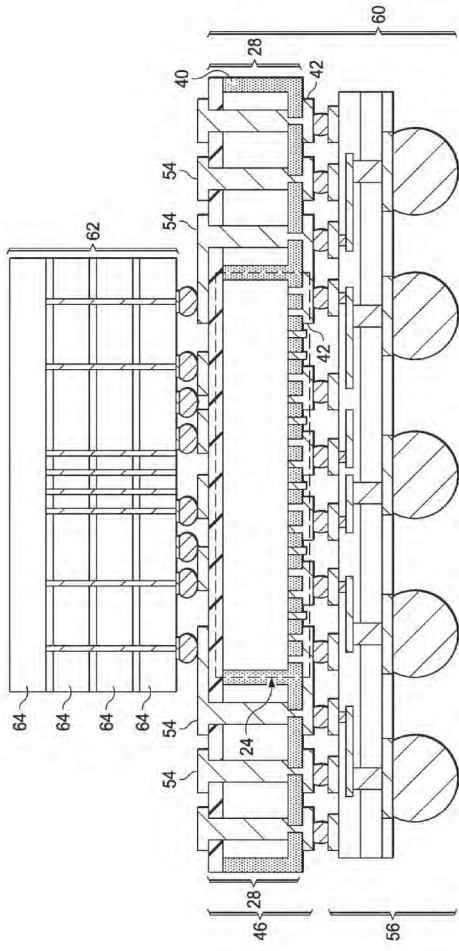


FIG. 9

Chen ’402, Fig. 9

“FIG. 10 illustrates an exemplary embodiment wherein package component 62 includes a plurality of stacked dies 64. In some embodiments, stacked dies 64 are memory dies. Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to package component 24, which are further connected to the RDLs 54 over and aligned to TAV modules 28. In these embodiments, package component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56. FIG. 11 illustrates alternative embodiments, wherein the positions of stacked dies 64 and package component 24 are swapped as compared to FIG. 10.” Chen ’402, [0020].

	 <p>FIG. 10</p> <p>Chen '402, Fig. 10</p>
[1.A] a bottom package substrate;	<p>Chen '402 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 8, package 46 is bonded to package component 56 to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like. Polymer 58 is dispensed between package 46 and package component 56.” Chen '402, [0018].</p>

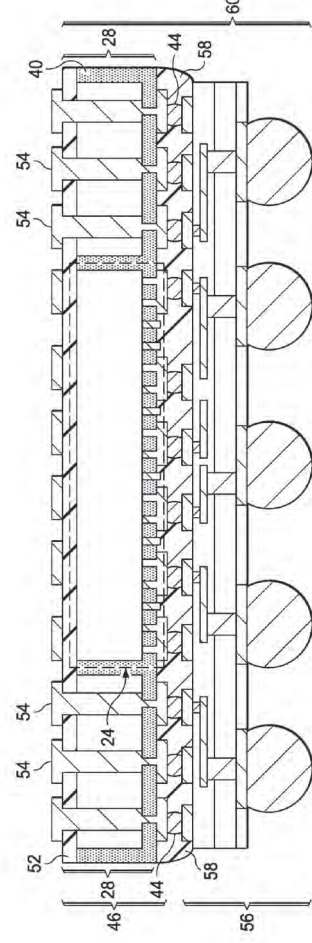


FIG. 8

Chen '402, Fig. 8

“Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like.” Chen '402, [0018].

“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like.” Chen '402, [0019].

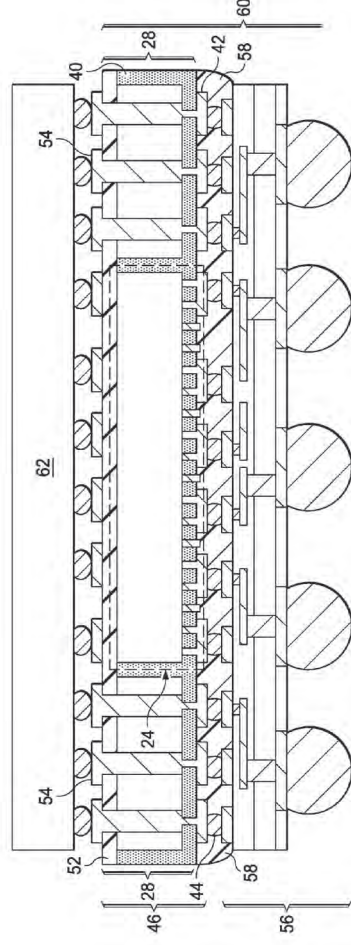
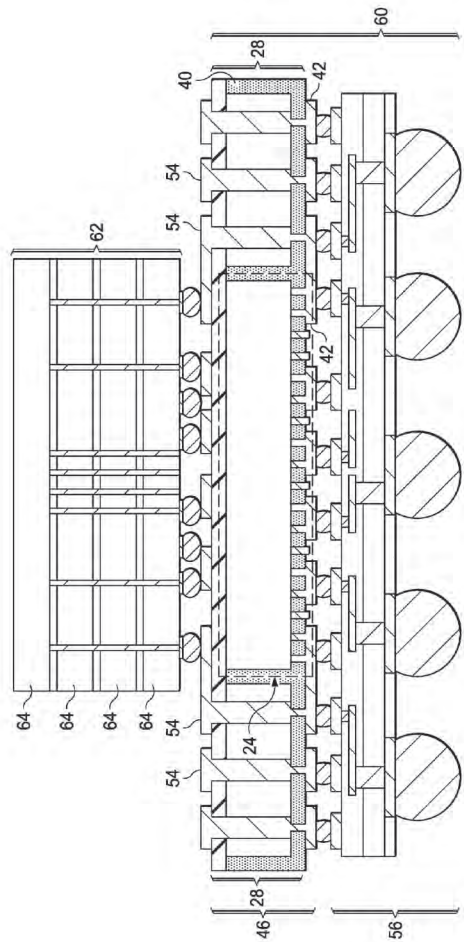


FIG. 9

Chen '402, Fig. 9

“FIG. 10 illustrates an exemplary embodiment wherein package component 62 includes a plurality of stacked dies 64. In some embodiments, stacked dies 64 are memory dies. Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to package component 24, which are further connected to the RDLs 54 over and aligned to TAV modules 28. In these embodiments, package component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56. FIG. 11 illustrates alternative embodiments, wherein the positions of stacked dies 64 and package component 24 are swapped as compared to FIG. 10.” Chen ’402, [0020].



Chen '402, Fig. 10

“In accordance with other embodiments, a device includes a bottom package, and a top package component bonded to the bottom package. The bottom package includes a package substrate, a plurality of connectors over the package substrate, and a package.” Chen '402, [0024].

“A plurality of RDLs is under the molding compound and electrically coupled to the device die and the plurality of through-vias in the TAV module. The plurality of RDLs is bonded to the package substrate through the plurality of connectors.” Chen '402, [0024].

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>“The polymer is ground to expose metal posts of the device die and metal posts of the TAV module. A first plurality of RDLs is formed over the polymer and connected to the metal posts of the device die and the metal posts of the TAV module, wherein the device die, the TAV module, and the first plurality of RDLs form a package. The package is mounted on a second carrier, wherein the first and the second carriers are on opposite sides of the package.” Chen '402, [0025].</p> <p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Chen '402 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 8, package 46 is bonded to package component 56 to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like.” Chen '402, [0018].</p>

	<div></div> <div><p>FIG. 8</p></div> <div><p>Chen '402, Fig. 8</p></div> <div><p>“Alternatively, package 60 may be molded, for example, using compress molding, and RDLs 54 are exposed through the respective molding compound (not shown).” Chen '402, [0018].</p></div> <div><p>“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like.” Chen '402, [0019].</p></div>
--	--

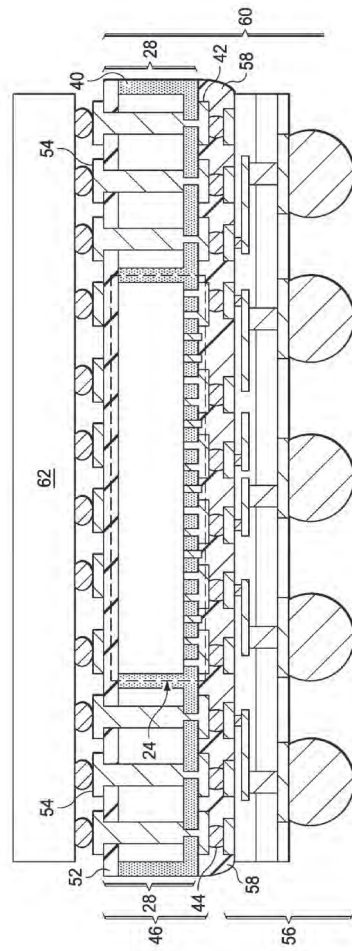
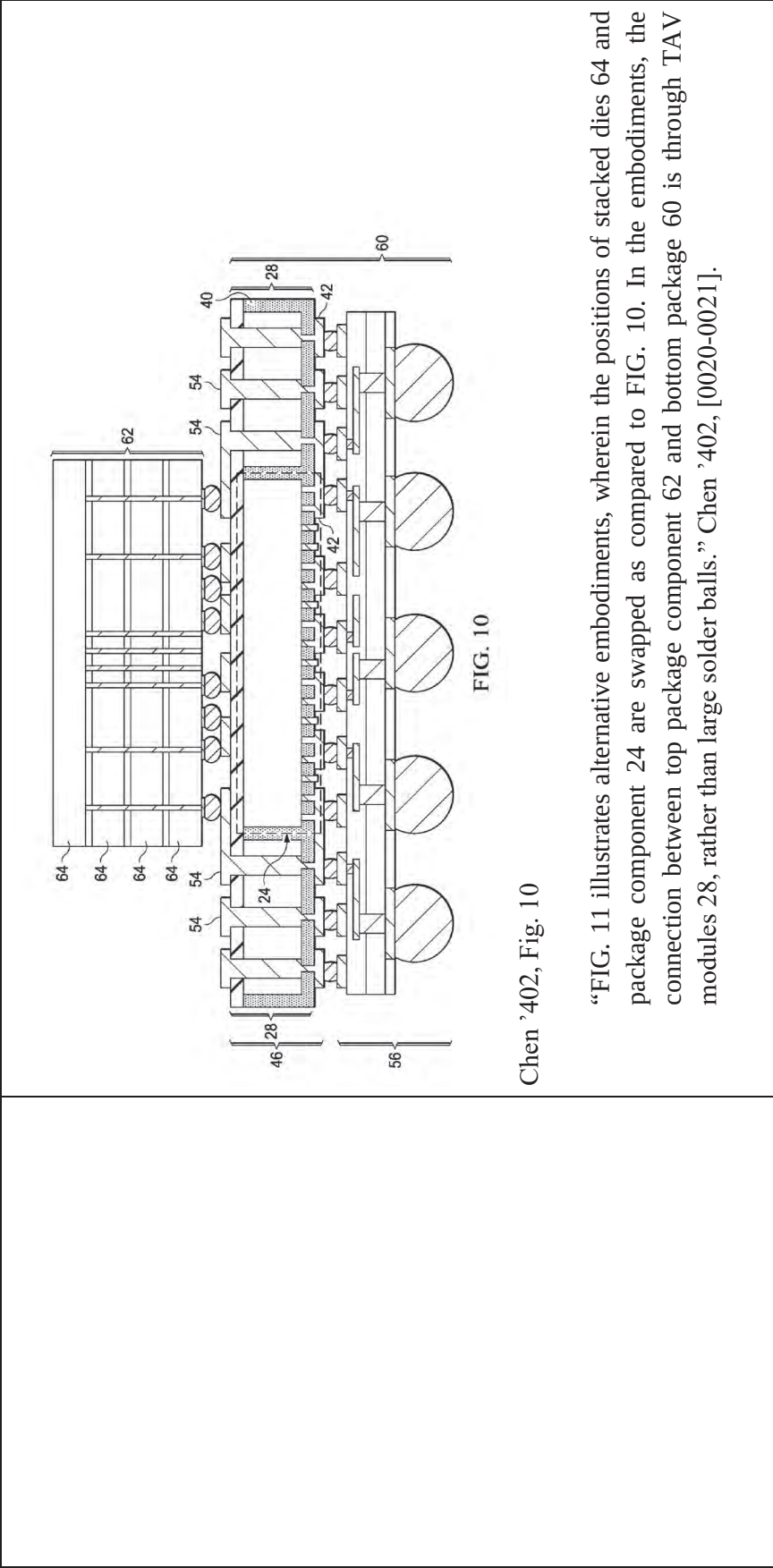


FIG. 9

Chen '402, Fig. 9

“FIG. 10 illustrates an exemplary embodiment wherein package component 62 includes a plurality of stacked dies 64. In some embodiments, stacked dies 64 are memory dies. Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to package component 24, which are further connected to the RDLs 54 over and aligned to TAV modules 28. In these embodiments, package component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56.”
Chen '402, [0020].



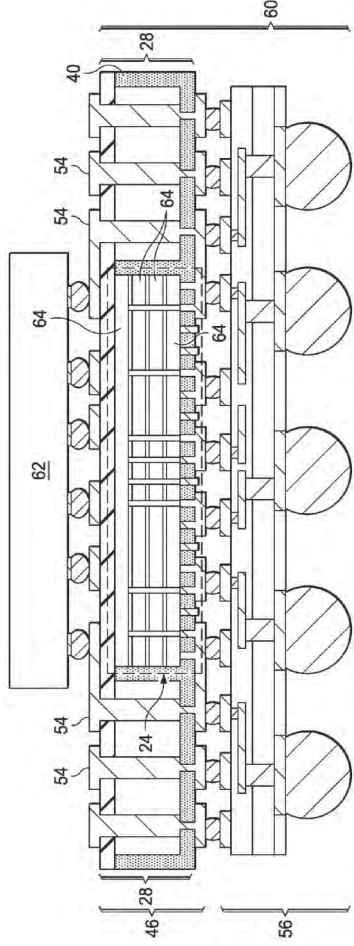


FIG. 11

Chen '402, Fig. 11

“In accordance with other embodiments, a device includes a bottom package, and a top package component bonded to the bottom package. The bottom package includes a package substrate, a plurality of connectors over the package substrate, and a package. The package includes a device die, and a TAV Module substantially level with the device die. The TAV module is free from active devices therein, and includes a substrate and a plurality of through-vias penetrating through the substrate. A molding compound contacts a bottom surface of the device die, a bottom surface of the TAV module, and sidewalls of the device die and the TAV module. A plurality of RDLs is under the molding compound and electrically coupled to the device die and the plurality of through-vias in the TAV module. The plurality of RDLs is bonded to the package substrate through the plurality of connectors.” Chen '402, [0023-0024].

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Chen '402 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates carrier 20 and release layer 22 on carrier 20. Carrier 20 may be a glass carrier, a ceramic carrier, or the like. Release layer 22 may be formed of an adhesive such as an Ultra-Violet (UV) glue. Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22. The bottom surfaces of package component 24 and TAV modules 28 are in contact with the top surface of release layer 22, and are level with each other.” Chen '402, [0009].</p>

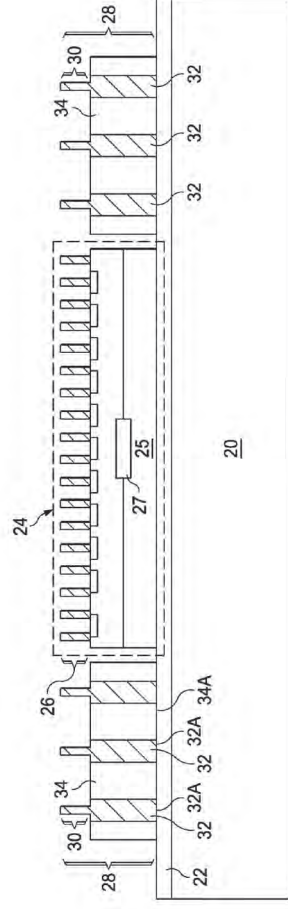


FIG. 1

Chen '402, Fig. 1

“In some embodiments, package component 24 includes one or a plurality of device dies.”
Chen '402, [0009].

Chen '402, [0009].

“TAV modules 28 are integrated modules that are pre-formed before being placed on release layer 22. TAV modules 28 include substrate 34, which may be a semiconductor substrate such as a silicon substrate. Alternatively, substrate 34 is a dielectric substrate such as a glass substrate. Through-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34. Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like. In some embodiments, bottom ends 32A of through-substrate vias 32 are level with the bottom surface 34A of substrate 34. Accordingly, bottom ends 32A of through-substrate vias 32 may be in contact with release layer 22. TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal posts 26 and 30 are substantially level with each other.” Chen ’402, [0010].

“FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, TAV modules 28 are disposed on opposite sides of package component 24. Although two TAV modules 28 are illustrated, there may be one or more than two TAV modules 28. TAV modules 28 may have an identical structure. Alternatively, TAV modules 28 may have different structures with different counts of metal posts 30, different layouts of metal posts 30, different sizes, and/or different materials. The plurality of TAV modules 28 may be laid out on release layer 22 with any layout.” Chen '402, [0012].

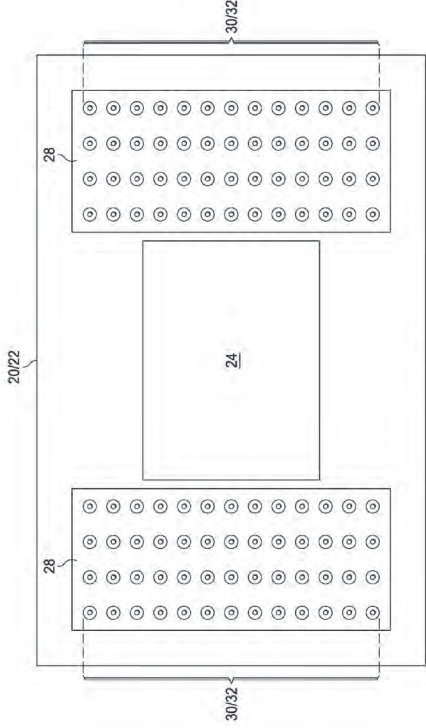


FIG. 2

Chen '402, Fig. 2

“Referring to FIG. 3, polymer 40 is molded on package component 24 and TAV modules 28. Polymer 40 fills the gaps between package component 24 and TAV modules 28, and may be in contact with release layer 22. Furthermore, polymer 40 is filled into the gaps between

metal posts 26, and into the gaps between metal posts 30. Polymer 40 may include a molding compound, a molding underfill, or a kind of epoxy. The top surface of polymer 40 may be level with or higher than the top surfaces of metal posts 26 and 30.” Chen ’402, [0013].

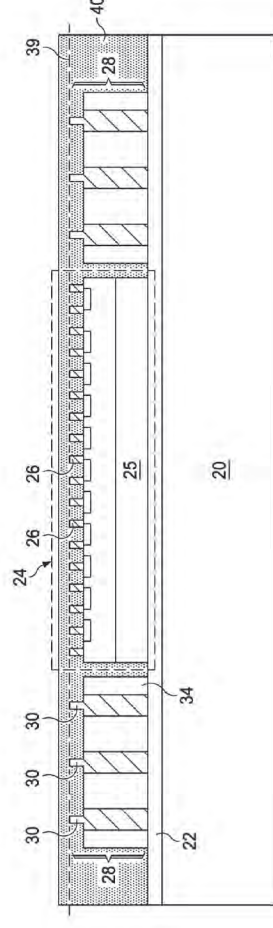
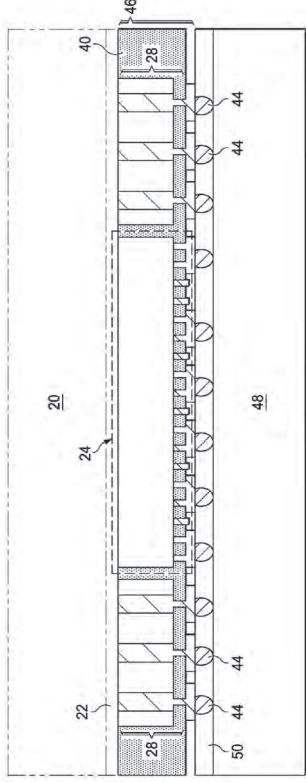


FIG. 3

Chen '402, Fig. 3

“Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46. Referring to FIG. 5, a carrier switch is performed. In the carrier switch process, carrier 48 is first attached to package 46, wherein carriers 20 and 48 are on the opposite sides of package 46.” Chen ’402, [0014-0015].



Chen '402, Fig. 5

“Referring to FIG. 8, package 46 is bonded to package component 56 to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like. Polymer 58 is dispensed between package 46 and package component 56. Polymer 58 may be an underfill or a molding underfill. Alternatively, package 60 may be molded, for example, using compress molding, and RDLs 54 are exposed through the respective molding compound (not shown). FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” Chen '402, [0018-0019].

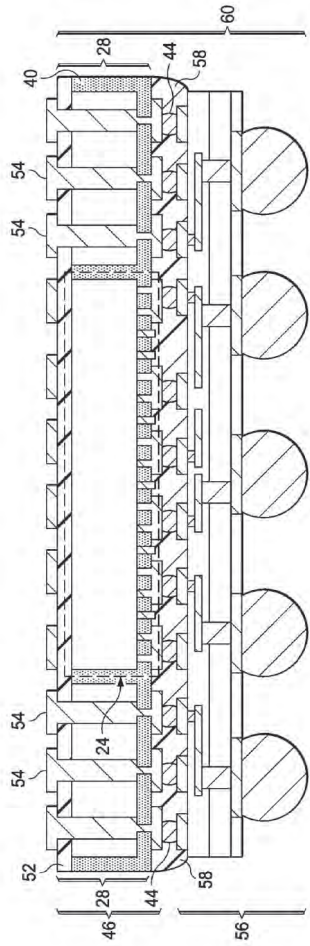


FIG. 8

Chen '402, Fig. 8

“FIG. 10 illustrates an exemplary embodiment wherein package component 62 includes a plurality of stacked dies 64. In some embodiments, stacked dies 64 are memory dies. Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to package component 24, which are further connected to the RDLs 54 over and aligned to TAV modules 28. In these embodiments, package component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56.”
Chen '402, [0020].

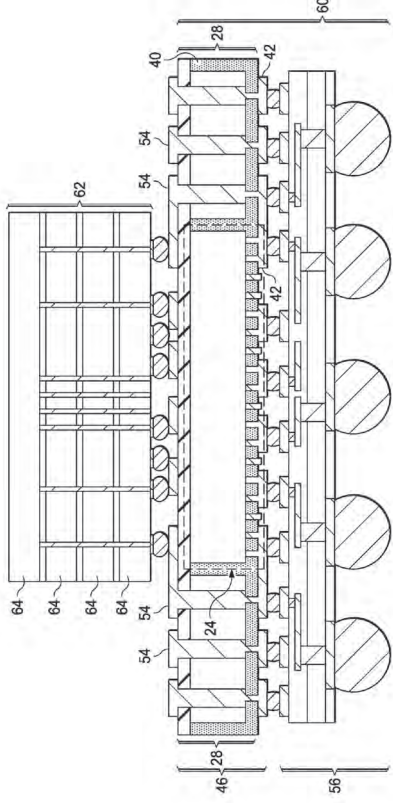
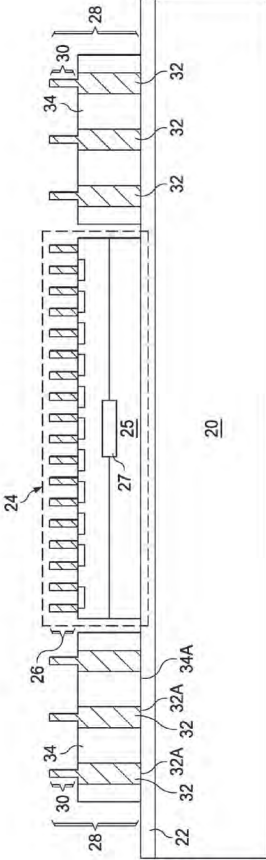


FIG. 10

Chen '402, Fig. 10

“In the embodiments, the connection between top package component 62 and bottom package 60 is through TAV modules 28, rather than large solder balls. Since TAV modules 28 may be formed using lithography processes and/or other processes that are used on silicon substrates, the pitches and the sizes of through-substrate vias 32 may be very small. Accordingly, the number of connections between top package component 62 and bottom package 60 is increased. The throughput of the packaging process is also high.” Chen '402, [0021].

To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Chen '402 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, e.g.:</p> <p>“FIG. 1 illustrates carrier 20 and release layer 22 on carrier 20. Carrier 20 may be a glass carrier, a ceramic carrier, or the like. Release layer 22 may be formed of an adhesive such as an Ultra-Violet (UV) glue. Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22.” Chen '402, [0009].</p>  <p>FIG. 1</p> <p>Chen '402, Fig. 1</p> <p>“TAV modules 28 are integrated modules that are pre-formed before being placed on release layer 22. TAV modules 28 include substrate 34, which may be a semiconductor substrate such as a silicon substrate. Alternatively, substrate 34 is a dielectric substrate such as a glass substrate.” Chen '402, [0010].</p>
---	---

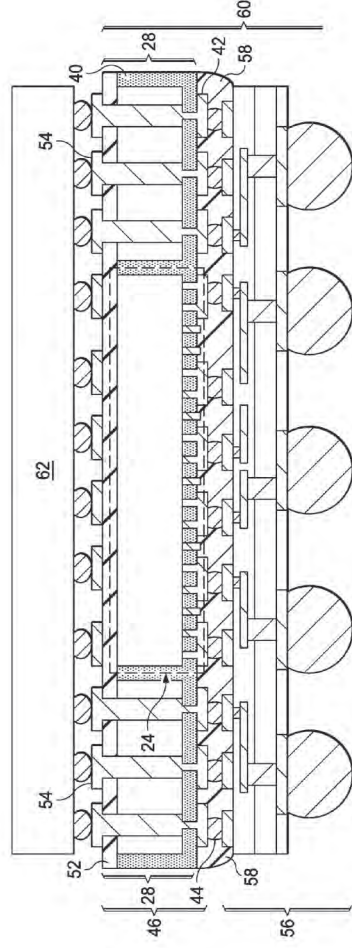


FIG. 9

Chen '402, Fig. 9

“Through-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34. Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like.” Chen et al., 2002, [0010].

“TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal post 26 and 30 are substantially level with each other. No active devices such as transistors are formed in TAV modules 28.” Chen, 402, [0010-0011].

“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also

interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer. In some exemplary embodiments, the formation of connectors 44 includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls. In alternative embodiments, the formation of connectors 44 includes performing a plating step to form solder regions on RDLs 42, and then reflowing the solder regions. Connectors 44 may also include metal pillars, or metal pillars and solder caps, which may also be formed through plating. Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen '402, [0014].

“Referring to FIG. 6, after the carrier switch, the back surface of TAV modules 28 is exposed, and through-substrate vias 32 in TAV modules 28 are exposed. In some embodiments, a grinding is performed to lightly grind the back surface of package component 24 and TAV modules 28, so that through-substrate vias 32 protrude above the back surface of substrate 34.” Chen '402, [0016].

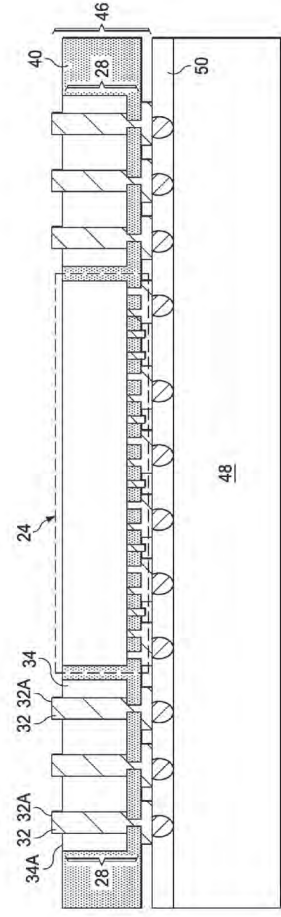


FIG. 6

Chen '402, Fig. 6

“As shown in FIG. 7, dielectric layer 52 is formed on the illustrated top surface of package 46. In some embodiments, dielectric layer 52 includes a polymer, which may be polyimide, benzocyclobutene (BCB), or the like. Dielectric layer 52 may also be formed of a light-sensitive material, which may be exposed in a lithography step, and then patterned. Alternatively, dielectric layer 52 may be formed of other materials such as oxides, nitrides, combination thereof, and multilayers thereof. RDLs 54 are then formed on dielectric layer 52 and connected to RDLs 54. RDLs 54 may extend to over and aligned to package component 24. Accordingly, RDLs 54 have a fan-in structure. The RDLs 54 that are over and aligned to package component 24 may be connected to the RDLs over and aligned to TAV modules 28. The dashed portions of RDLs 54 illustrate the connecting portions of RDLs 54. Next, carrier 48 (FIG. 6) is demounted from package 46. The formation of package 46 is thus finished.” Chen '402, [0017].

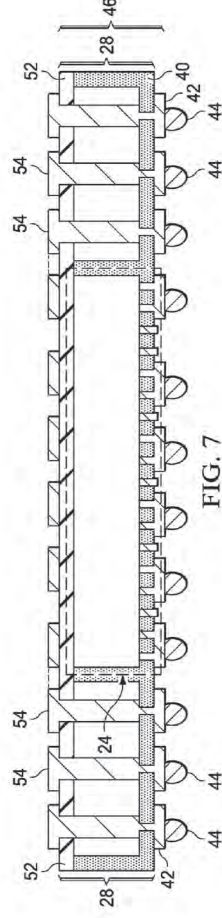


FIG. 7

Chen '402, Fig. 7

“In the embodiments, the connection between top package component 62 and bottom package 60 is through TAV modules 28, rather than large solder balls. Since TAV modules 28 may be formed using lithography processes and/or other processes that are used on silicon

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>substrates, the pitches and the sizes of through-substrate vias 32 may be very small. Accordingly, the number of connections between top package component 62 and bottom package 60 is increased. The throughput of the packaging process is also high.” Chen ’402, [0021].</p> <p>“In accordance with embodiments, a device includes a TAV Module, which includes a substrate, a plurality of through-vias penetrating through the substrate, and a second plurality of metal posts at a bottom surface of the TAV module and electrically coupled to the plurality of through-vias.” Chen ’402, [0023].</p> <p>To the extent Plaintiff contends that Chen ’402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Chen ’402 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Through-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34. Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like.” Chen ’402, [0010].</p>

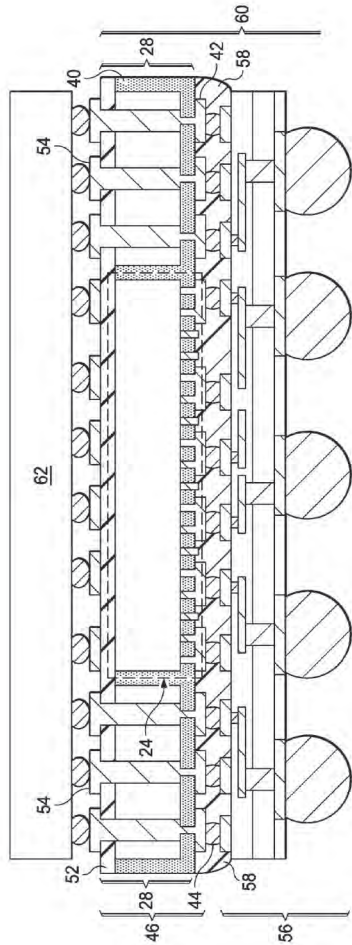


FIG. 9

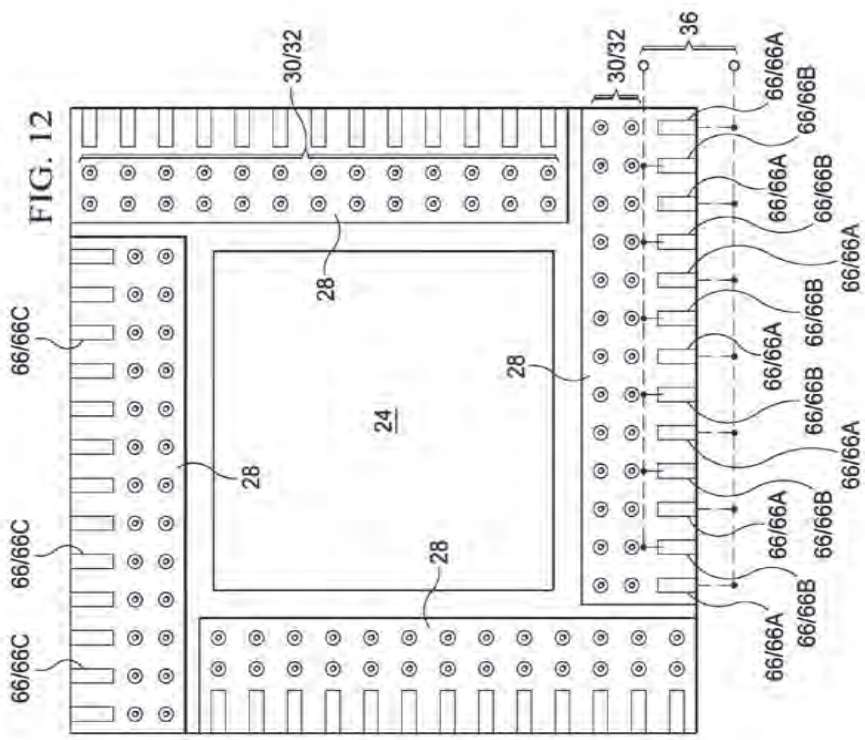
Chen '402, Fig. 9

“TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal post 26 and 30 are substantially level with each other.” Chen '402, [0010].

“No active devices such as transistors are formed in TAV modules 28. In accordance with some embodiments, TAV modules 28 do not include passive devices such as capacitors, inductors, resistors, and/or the like. In alternative embodiments, TAV modules 28 may include the passive devices therein. Exemplary capacitor 36 is illustrated in FIG. 12, which capacitor 36 includes two or more parallel metal strips 66 that penetrate through substrate 34 to form the capacitor plates of capacitor 36. TAV modules 28 may include redistribution layer(s) that include redistribution lines and metal pads on the top sides of TAV modules 28. Alternatively, no redistribution layer is formed on either side of one or each of TAV modules

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	28, and metal posts 30 are connected to, and are aligned to, through-substrate vias 32, with no redistribution lines between metal posts and through-substrate vias 32.” Chen ’402, [0011].
--	---



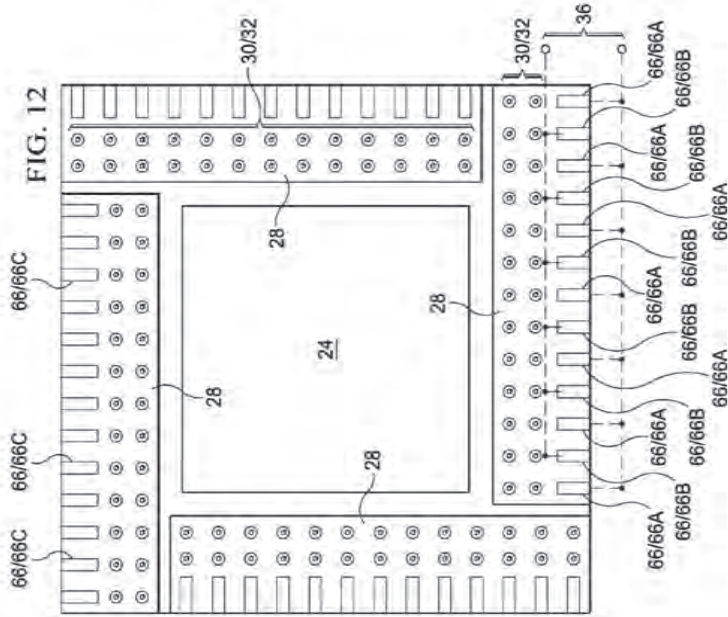
Chen '402, Fig. 12

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>“FIG. 12 illustrates a top view of the structure in FIG. 1 in accordance with alternative embodiments. In TAV modules 28, besides through-substrate vias 32, which are used for electrically connecting the features on opposite sides of TAV modules 28, strip-shaped vias 66 may also be formed. In accordance with some embodiments, strip-shaped vias 66 are used for dissipating the heat generated in package component 24 as in FIGS. 9 through 11. Accordingly, strip-shaped vias 66 (such as 66C) may be electrically floating when TAV modules 28 are used in the package structure in FIGS. 9 through 11. In these embodiments, since strip-shaped vias 66C are formed of metals that have good thermal conductivity, the heat dissipating ability is improved over that of molding compound. In alternative embodiments, strip-shaped vias 66 may be interconnected to form a capacitor. For example, in FIG. 12, strip-shaped vias 66 include strip-shaped vias 66A that are interconnected to form one of the capacitor plates, and strip-shaped vias 66B that are interconnected to form the other capacitor plate. Strip-shaped vias 66A and strip-shaped vias 66B are laid out in an alternating pattern to increase the capacitance.” Chen '402, [0022].</p> <p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Chen '402 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p>See, e.g.:</p> <p>“Metal posts 26 (such as copper posts) are formed as a top portion of package component 24.” Chen '402, [0009].</p>

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>“Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22. The bottom surfaces of package component 24 and TAV modules 28 are in contact with the top surface of release layer 22, and are level with each other. The position of package component 24 and TAV modules 28 are accurately aligned to desirable locations, so that the subsequent formed redistribution lines may electrically couple to metal posts 26 and 30.” Chen '402, [0009].</p> <p>“TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal post 26 and 30 are substantially level with each other.” Chen '402, [0010].</p> <p>“No active devices such as transistors are formed in TAV modules 28. In accordance with some embodiments, TAV modules 28 do not include passive devices such as capacitors, inductors, resistors, and/or the like. In alternative embodiments, TAV modules 28 may include the passive devices therein. Exemplary capacitor 36 is illustrated in FIG. 12, which capacitor 36 includes two or more parallel metal strips 66 that penetrate through substrate 34 to form the capacitor plates of capacitor 36. TAV modules 28 may include redistribution layer(s) that include redistribution lines and metal pads on the top sides of TAV modules 28. Alternatively, no redistribution layer is formed on either side of one or each of TAV modules 28, and metal posts 30 are connected to, and are aligned to, through-substrate vias 32, with no redistribution lines between metal posts and through-substrate vias 32.” Chen '402, [0011].</p>
--	---



Chen '402, Fig. 12

“Furthermore, polymer 40 is filled into the gaps between metal posts 26, and into the gaps between metal posts 30. Polymer 40 may include a molding compound, a molding underfill, or a kind of epoxy. The top surface of polymer 40 may be level with or higher than the top surfaces of metal posts 26 and 30. A grinding step may be performed to grind polymer 40, until metal posts 26 and 30 are exposed.” Chen '402, [0013].

	<p>“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30.” Chen ’402, [0014].</p> <p>“As indicated by dashed lines, RDLs 42 may also interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer. In some exemplary embodiments, the formation of connectors 44 includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls. In alternative embodiments, the formation of connectors 44 includes performing a plating step to form solder regions on RDLs 42, and then reflowing the solder regions. Connectors 44 may also include metal pillars, or metal pillars and solder caps, which may also be formed through plating. Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen ’402, [0014].</p> <p>“RDLs 54 are then formed on dielectric layer 52 and connected to RDLs 54. RDLs 54 may extend to over and aligned to package component 24. Accordingly, RDLs 54 have a fan-in structure. The RDLs 54 that are over and aligned to package component 24 may be connected to the RDLs over and aligned to TAV modules 28.” Chen ’402, [0017].</p>
--	--

	<p>FIG. 9</p>
	<p>Chen '402, Fig. 9</p> <p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Chen '402 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, <i>e.g.</i>:</p> <p>“FIGS. 1 through 9 are cross-sectional views and a top view of intermediate stages in the manufacturing of a Package-on-Package (PoP) structure in accordance with some exemplary</p>

	<p>embodiments. FIG. 1 illustrates carrier 20 and release layer 22 on carrier 20. Carrier 20 may be a glass carrier, a ceramic carrier, or the like. Release layer 22 may be formed of an adhesive such as an Ultra-Violet (UV) glue. Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22. The bottom surfaces of package component 24 and TAV modules 28 are in contact with the top surface of release layer 22, and are level with each other. The position of package component 24 and TAV modules 28 are accurately aligned to desirable locations, so that the subsequent formed redistribution lines may electrically couple to metal posts 26 and 30. In some embodiments, package component 24 includes one or a plurality of device dies. For example, package component 24 may include a Central Computing Unit (CPU) die or another type of logic die having logic circuits. In alternative embodiments, package component 24 includes a plurality of memory dies stacked together (please refer to FIG. 11). In the embodiments wherein package component 24 is a device die, package component 24 may include semiconductor substrate 25 and active devices (such as transistors) 27 at a top surface of semiconductor substrate 25. The bottom surface of semiconductor substrate 25 is thus in contact with release layer 22. Semiconductor substrate 25 may be free from through-substrate vias formed therein, although through-substrate vias may also be formed to penetrate through semiconductor substrate 25. Package component 24 may also be a package that includes device die(s), interposer(s), package substrate(s) (not shown), and/or the like. Metal posts 26 (such as copper posts) are formed as a top portion of package component 24.” Chen ’402, [0009].</p>
--	--

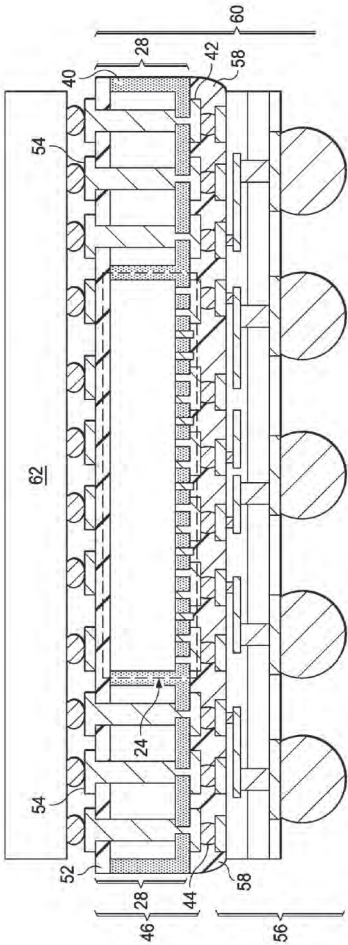


FIG. 9

Chen '402, Fig. 9

“TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal post 26 and 30 are substantially level with each other.” Chen '402, [0010].

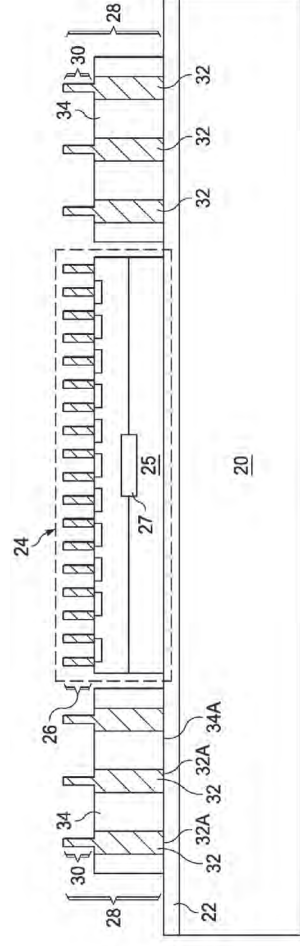


FIG. 1

Chen '402, Fig. 1

“metal posts 30 are connected to, and are aligned to, through-substrate vias 32, with no redistribution lines between metal posts and through-substrate vias 32.” Chen ’402, [0011].

“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer.” Chen '402, [0014].

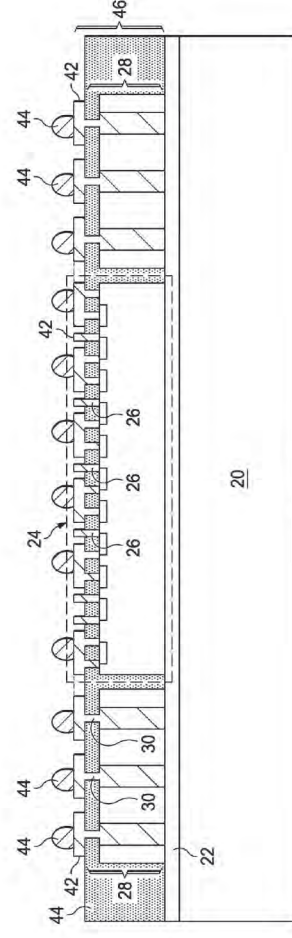


FIG. 4

Chen '402, Fig. 4

“Referring to FIG. 6, after the carrier switch, the back surface of TAV modules 28 is exposed, and through-substrate vias 32 in TAV modules 28 are exposed. In some embodiments, a grinding is performed to lightly grind the back surface of package component 24 and TAV modules 28, so that through-substrate vias 32 protrude above the back surface of substrate 34. Alternatively, the grinding step is skipped. When no grinding is performed, surfaces 32A of through-substrate vias 32 are level with back surface 34A of substrate 34.” Chen ‘402, [0016].

	<p>FIG. 6</p> <p>Chen '402, Fig. 6</p> <p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Chen '402 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p> <p>“In an existing PoP process, the bottom package is formed first, which includes a device die bonded to a package substrate. A molding compound is then molded on the package substrate, wherein the device die is molded in the molding compound. The package substrate further includes solder balls formed thereon, wherein the solder balls and the device die are on a</p>

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>same side of the package substrate. The solder balls are used for connecting the top package to the bottom package. Accordingly, the heights of the solder balls need to be greater than the thickness of the device die, so that the top portions of the solder balls may protrude above the top surface of the device die, and above the top surface of the molding compound. Accordingly, the lateral sizes of the solder balls are also large, and the amount of the solder balls that can be used in a PoP structure is limited.” Chen ’402, [0002].</p> <p>“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer. In some exemplary embodiments, the formation of connectors 44 includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls. In alternative embodiments, the formation of connectors 44 includes performing a plating step to form solder regions on RDLs 42, and then reflowing the solder regions. Connectors 44 may also include metal pillars, or metal pillars and solder caps, which may also be formed through plating. Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen ’402, [0014].</p>
--	---

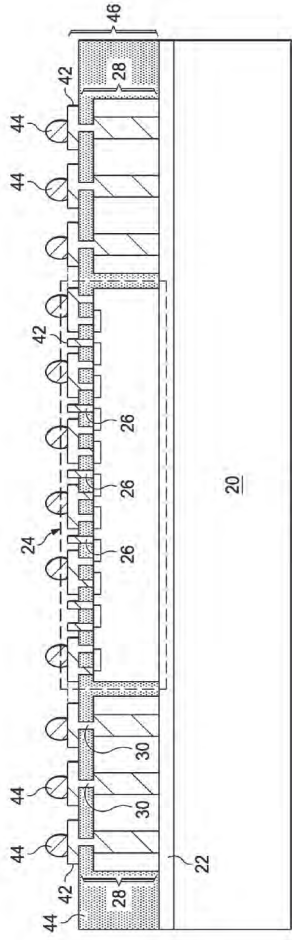


FIG. 4

Chen '402, Fig. 4

“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” Chen '402, [0019].

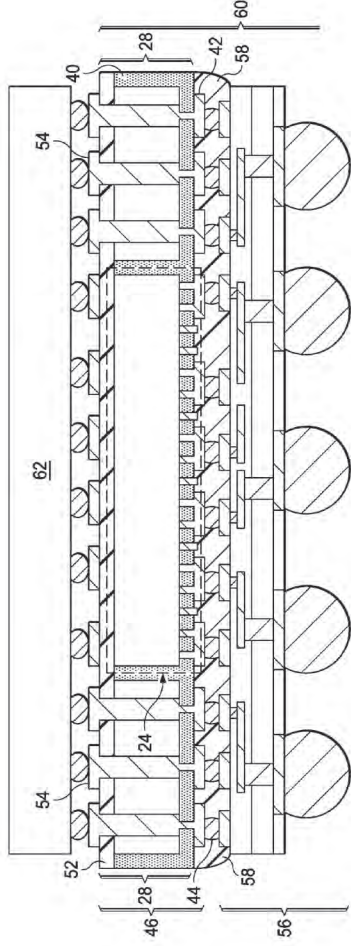


FIG. 9

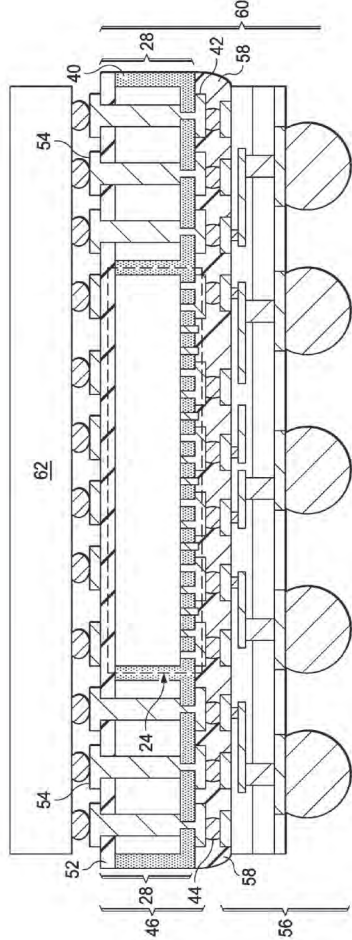
Chen '402, Fig. 9

“In the embodiments, the connection between top package component 62 and bottom package 60 is through TAV modules 28, rather than large solder balls. Since TAV modules 28 may be formed using lithography processes and/or other processes that are used on silicon substrates, the pitches and the sizes of through-substrate vias 32 may be very small. Accordingly, the number of connections between top package component 62 and bottom package 60 is increased. The throughput of the packaging process is also high.” Chen '402, [0021].

To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Chen '402 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer. In some exemplary embodiments, the formation of connectors 44 includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls. In alternative embodiments, the formation of connectors 44 includes performing a plating step to form solder regions on RDLs 42, and then reflowing the solder regions. Connectors 44 may also include metal pillars, or metal pillars and solder caps, which may also be formed through plating. Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen '402, [0014].</p>
---	--



Chen '402, Fig. 9

“Referring to FIG. 6, after the carrier switch, the back surface of TAV modules 28 is exposed, and through-substrate vias 32 in TAV modules 28 are exposed. In some embodiments, a grinding is performed to lightly grind the back surface of package component 24 and TAV modules 28, so that through-substrate vias 32 protrude above the back surface of substrate 34. Alternatively, the grinding step is skipped. When no grinding is performed, surfaces 32 A of through-substrate vias 32 are level with back surface 34 A of substrate 34. As shown in FIG. 7, dielectric layer 52 is formed on the illustrated top surface of package 46. In some embodiments, dielectric layer 52 includes a polymer, which may be polyimide, benzocyclobutene (BCB), or the like. Dielectric layer 52 may also be formed of a light-sensitive material, which may be exposed in a lithography step, and then patterned. Alternatively, dielectric layer 52 may be formed of other materials such as oxides, nitrides, combination thereof, and multilayers thereof. RDLs 54 are then formed on dielectric layer

52 and connected to RDLs 54. RDLs 54 may extend to over and aligned to package component 24. Accordingly, RDLs 54 have a fan-in structure. The RDLs 54 that are over and aligned to package component 24 may be connected to the RDLs over and aligned to TAV modules 28.” Chen ’402, [0016-0017].

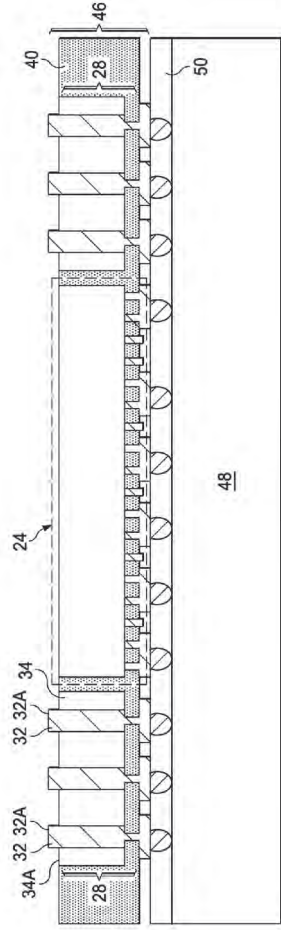


FIG. 6

Chen ’402, Fig. 6

“Referring to FIG. 8, package 46 is bonded to package component 56 to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like. Polymer 58 is dispensed between package 46 and package component 56. Polymer 58 may be an underfill or a molding underfill.” Chen ’402, [0018].

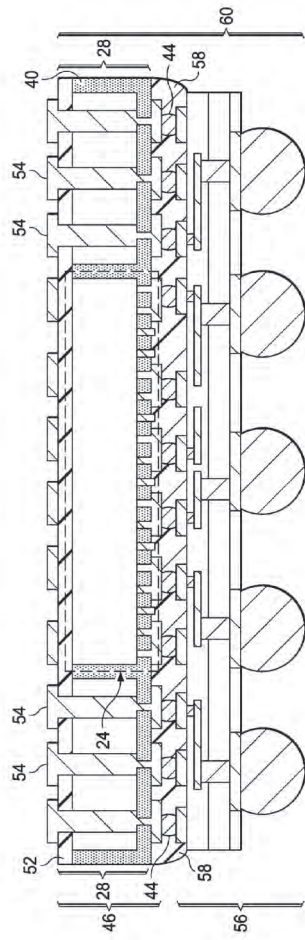


FIG. 8

Chen '402, Fig. 8

“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” Chen '402, [0019].

“A first plurality of RDLs is underlying a bottom surface of the second and the third portions of the polymer. A second plurality of RDLs is over the first package component and the TAV module. The first plurality of RDLs is electrically coupled to the second plurality of RDLs through the plurality of through-vias in the TAV module.” Chen '402, [0023].

“The package includes a device die, and a TAV Module substantially level with the device die. The TAV module is free from active devices therein, and includes a substrate and a

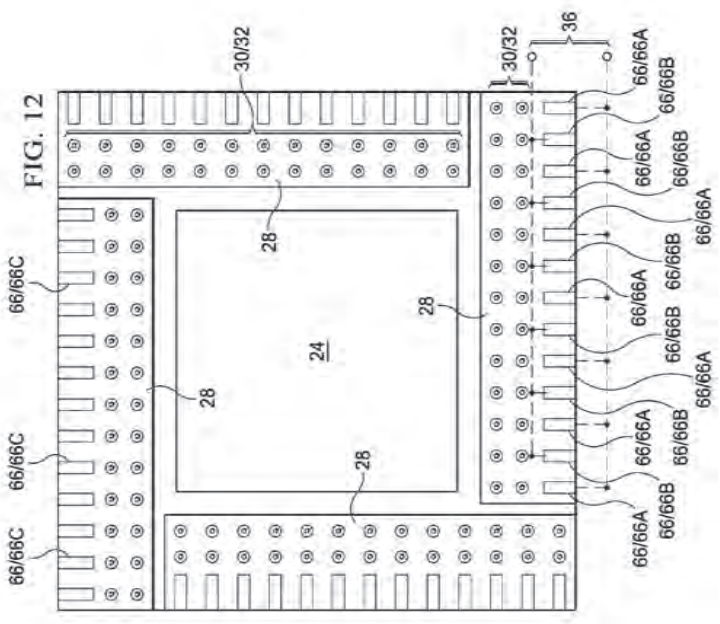
Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>plurality of through-vias penetrating through the substrate. A molding compound contacts a bottom surface of the device die, a bottom surface of the TAV module, and sidewalls of the device die and the TAV module. A plurality of RDLs is under the molding compound and electrically coupled to the device die and the plurality of through-vias in the TAV module. The plurality of RDLs is bonded to the package substrate through the plurality of connectors.” Chen '402, [0024].</p> <p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Chen '402 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“No active devices such as transistors are formed in TAV modules 28. In accordance with some embodiments, TAV modules 28 do not include passive devices such as capacitors, inductors, resistors, and/or the like. In alternative embodiments, TAV modules 28 may include the passive devices therein. Exemplary capacitor 36 is illustrated in FIG. 12, which capacitor 36 includes two or more parallel metal strips 66 that penetrate through substrate 34 to form the capacitor plates of capacitor 36. TAV modules 28 may include redistribution layer(s) that include redistribution lines and metal pads on the top sides of TAV modules 28. Alternatively, no redistribution layer is formed on either side of one or each of TAV modules</p>

	<p>28, and metal posts 30 are connected to, and are aligned to, through-substrate vias 32, with no redistribution lines between metal posts and through-substrate vias 32.” Chen ’402, [0011].</p> <p>“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also interconnect metal posts 26 and 30.” Chen ’402, [0014].</p> <div></div> <p>FIG. 4</p> <p>Chen ’402, Fig. 4</p> <p>“RDLs 54 are then formed on dielectric layer 52 and connected to RDLs 42. RDLs 54 may extend to over and aligned to package component 24. Accordingly, RDLs 54 have a fan-in structure. The RDLs 54 that are over and aligned to package component 24 may be connected to the RDLs over and aligned to TAV modules 28.” Chen ’402, [0017].</p>
--	---

	<p>“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” Chen '402, [0019].</p> <div></div> <p>FIG. 9</p> <p>Chen '402, Fig. 9</p> <p>“In these embodiments, package component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56.” Chen '402, [0020].</p> <p>“In the embodiments, the connection between top package component 62 and bottom package 60 is through TAV modules 28, rather than large solder balls. Since TAV modules</p>
--	--

	<p>28 may be formed using lithography processes and/or other processes that are used on silicon substrates, the pitches and the sizes of through-substrate vias 32 may be very small. Accordingly, the number of connections between top package component 62 and bottom package 60 is increased.” Chen ’402, [0021].</p> <p>“FIG. 12 illustrates a top view of the structure in FIG. 1 in accordance with alternative embodiments. In TAV modules 28, besides through-substrate vias 32, which are used for electrically connecting the features on opposite sides of TAV modules 28, strip-shaped vias 66 may also be formed. In accordance with some embodiments, strip-shaped vias 66 are used for dissipating the heat generated in package component 24 as in FIGS. 9 through 11. Accordingly, strip-shaped vias 66 (such as 66C) may be electrically floating when TAV modules 28 are used in the package structure in FIGS. 9 through 11. In these embodiments, since strip-shaped vias 66C are formed of metals that have good thermal conductivity, the heat dissipating ability is improved over that of molding compound. In alternative embodiments, strip-shaped vias 66 may be interconnected to form a capacitor. For example, in FIG. 12, strip-shaped vias 66 include strip-shaped vias 66A that are interconnected to form one of the capacitor plates, and strip-shaped vias 66B that are interconnected to form the other capacitor plate. Strip-shaped vias 66A and strip-shaped vias 66B are laid out in an alternating pattern to increase the capacitance.” Chen ’402, [0022].</p>
--	---



Chen '402, Fig. 12

“A plurality of RDLs is under the molding compound and electrically coupled to the device die and the plurality of through-vias in the TAV module. The plurality of RDLs is bonded to the package substrate through the plurality of connectors.” Chen '402, [0024].

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Chen '402 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22. The bottom surfaces of package component 24 and TAV modules 28 are in contact with the top surface of release layer 22, and are level with each other. The position of package component 24 and TAV modules 28 are accurately aligned to desirable locations, so that the subsequent formed redistribution lines may electrically couple to metal posts 26 and 30. In some embodiments, package component 24 includes one or a plurality of device dies. For example, package component 24 may include a Central Computing Unit (CPU) die or another type of logic die having logic circuits. In alternative embodiments, package component 24 includes a plurality of memory dies stacked together (please refer to FIG. 11)”</p> <p>Chen '402, [0009].</p>

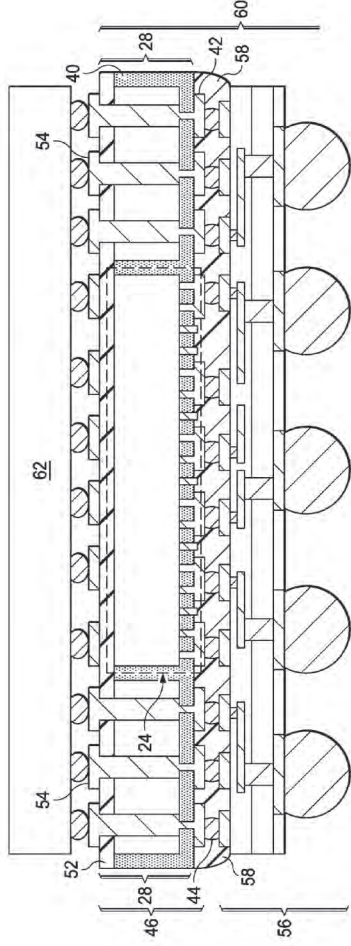


FIG. 9

Chen '402, Fig. 9

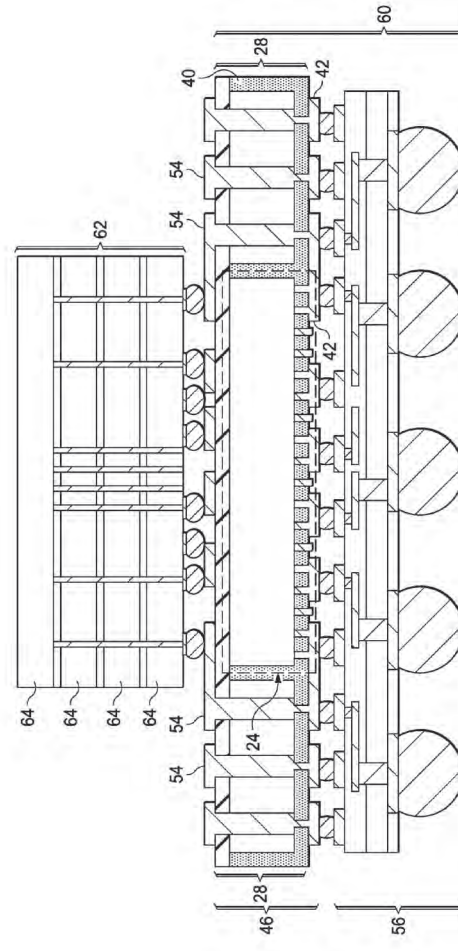
“In some embodiments, package component 24 includes one or a plurality of device dies. For example, package component 24 may include a Central Computing Unit (CPU) die or another type of logic die having logic circuits.” Chen '402, [0009].

“In the embodiments wherein package component 24 is a device die, package component 24 may include semiconductor substrate 25 and active devices (such as transistors) 27 at a top surface of semiconductor substrate 25. The bottom surface of semiconductor substrate 25 is thus in contact with release layer 22.” Chen '402, [0009].

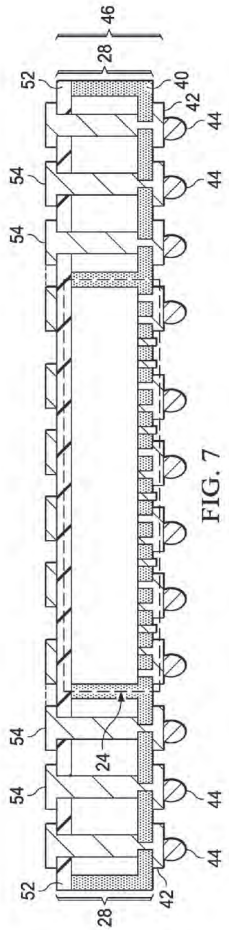
“Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen '402, [0014].

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>“FIG. 8, package 46 is bonded to package component 56 to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like. Polymer 58 is dispensed between package 46 and package component 56.” Chen '402, [0018].</p> <p>“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” Chen '402, [0019].</p> <p>“FIG. 10 illustrates an exemplary embodiment wherein package component 62 includes a plurality of stacked dies 64. In some embodiments, stacked dies 64 are memory dies. Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to package component 24, which are further connected to the RDLs 54 over and aligned to TAV modules 28. In these embodiments, package component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56. FIG. 11 illustrates alternative embodiments, wherein the positions of stacked dies 64 and package component 24 are swapped as compared to FIG. 10.” Chen '402, [0020].</p>
--	--

	 <p>FIG. 10</p> <p>Chen '402, Fig. 10</p> <p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Chen '402 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<p>“FIG. 1 illustrates carrier 20 and release layer 22 on carrier 20. Carrier 20 may be a glass carrier, a ceramic carrier, or the like. Release layer 22 may be formed of an adhesive such as an Ultra-Violet (UV) glue. Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22. The bottom surfaces of package component 24 and TAV modules 28 are in contact with the top surface of release layer 22, and are level with each other.” Chen '402, [0009].</p> <div><p>FIG. 1</p></div> <p>Chen '402, Fig. 1</p> <p>“As shown in FIG. 7, dielectric layer 52 is formed on the illustrated top surface of package 46. In some embodiments, dielectric layer 52 includes a polymer, which may be polyimide, benzocyclobutene (BCB), or the like. Dielectric layer 52 may also be formed of a light-sensitive material, which may be exposed in a lithography step, and then patterned. Alternatively, dielectric layer 52 may be formed of other materials such as oxides, nitrides, combination thereof, and multilayers thereof. RDLs 54 are then formed on dielectric layer</p>
--	---

	<p>52 and connected to RDLs 54. RDLs 54 may extend to over and aligned to package component 24.” Chen '402, [0017].</p>  <p>FIG. 7</p> <p>Chen '402, Fig. 7</p> <p>“Referring to FIG. 8, package 46 is bonded to package component 56 to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like. Polymer 58 is dispensed between package 46 and package component 56.” Chen '402, [0018].</p>
--	---

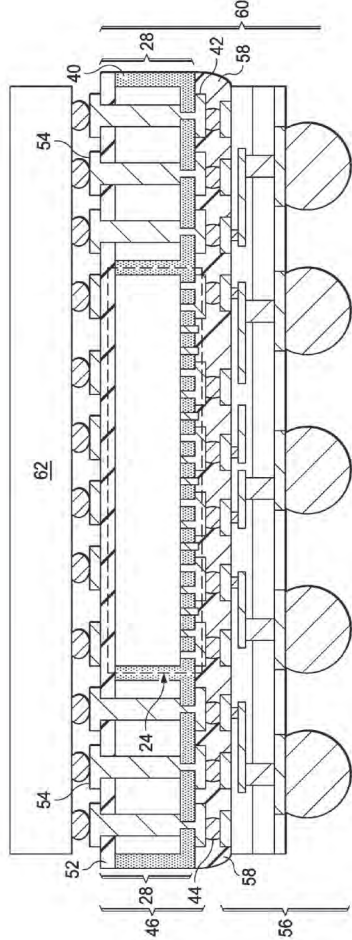


FIG. 9

Chen '402, Fig. 9

“Referring to FIG. 8, package 46 is bonded to package component 56 to form bottom package 60.” Chen '402, [0018].

“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like.” Chen '402, [0019].

“The first plurality of RDLs is electrically coupled to the second plurality of RDLs through the plurality of through-vias in the TAV module. In accordance with other embodiments, a device includes a bottom package, and a top package component bonded to the bottom package. The bottom package includes a package substrate, a plurality of connectors over the

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>package substrate, and a package. The package includes a device die, and a TAV Module substantially level with the device die.” Chen ’402, [0023-0024].</p> <p>To the extent Plaintiff contends that Chen ’402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Chen ’402 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates carrier 20 and release layer 22 on carrier 20. Carrier 20 may be a glass carrier, a ceramic carrier, or the like. Release layer 22 may be formed of an adhesive such as an Ultra-Violet (UV) glue. Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22. The bottom surfaces of package component 24 and TAV modules 28 are in contact with the top surface of release layer 22, and are level with each other.” Chen ’402, [0009].</p> <p>“FIG. 2 illustrates a top view of the structure in FIG. 1. In accordance with some embodiments, TAV modules 28 are disposed on opposite sides of package component 24. Although two TAV modules 28 are illustrated, there may be one or more than two TAV modules 28.” Chen ’402, [0012].</p>

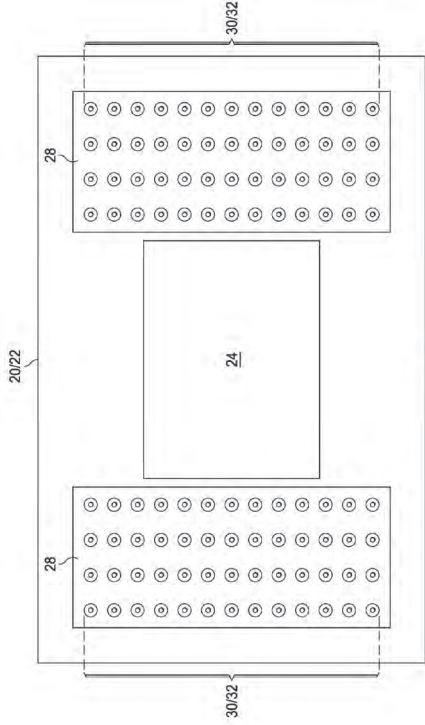


FIG. 2

Chen '402, Fig. 2

“TAV modules 28 may have an identical structure. Alternatively, TAV modules 28 may have different structures with different counts of metal posts 30, different layouts of metal posts 30, different sizes, and/or different materials. The plurality of TAV modules 28 may be laid out on release layer 22 with any layout.” Chen '402, [0012].

“Referring to FIG. 3, polymer 40 is molded on package component 24 and TAV modules 28. Polymer 40 fills the gaps between package component 24 and TAV modules 28, and may be in contact with release layer 22.” Chen '402, [0013].

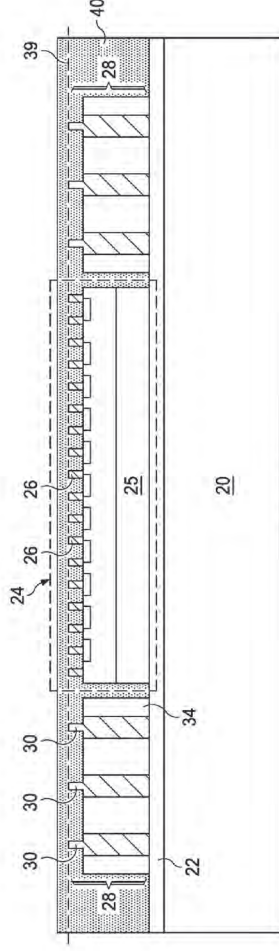


FIG. 3

Chen '402, Fig. 3

“Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen '402, [0014].

“In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” Chen '402, [0019].

“FIG. 12 illustrates a top view of the structure in FIG. 1 in accordance with alternative embodiments. In TAV modules 28, besides through-substrate vias 32, which are used for electrically connecting the features on opposite sides of TAV modules 28, strip-shaped vias 66 may also be formed. In accordance with some embodiments, strip-shaped vias 66 are used for dissipating the heat generated in package component 24 as in FIGS. 9 through 11. Accordingly, strip-shaped vias 66 (such as 66C) may be electrically floating when TAV modules 28 are used in the package structure in FIGS. 9 through 11. In these embodiments, since strip-shaped vias 66C are formed of metals that have good thermal conductivity, the

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>heat dissipating ability is improved over that of molding compound. In alternative embodiments, strip-shaped vias 66 may be interconnected to form a capacitor. For example, in FIG. 12, strip-shaped vias 66 include strip-shaped vias 66A that are interconnected to form one of the capacitor plates, and strip-shaped vias 66B that are interconnected to form the other capacitor plate. Strip-shaped vias 66A and strip-shaped vias 66B are laid out in an alternating pattern to increase the capacitance.” Chen ’402, [0022].</p> <p>To the extent Plaintiff contends that Chen ’402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Chen ’402 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“RDLs 54 are then formed on dielectric layer 52 and connected to RDLs 54. RDLs 54 may extend to over and aligned to package component 24. Accordingly, RDLs 54 have a fan-in structure. The RDLs 54 that are over and aligned to package component 24 may be connected to the RDLs over and aligned to TAV modules 28.” Chen ’402, [0017].</p>

“Referring to FIG. 8, package 46 is bonded to package component 56 to form bottom package 60. Package component 56 may be a package substrate, an interposer, a device die, a Printed Circuit Board (PCB), or the like. Polymer 58 is dispensed between package 46 and package component 56. Polymer 58 may be an underfill or a molding underfill. Alternatively, package 60 may be molded, for example, using compress molding, and RDLs 54 are exposed through the respective molding compound (not shown). FIG. 9 illustrates the bonding of top package component 62 to bottom package 60.” Chen '402, [0018-0019].

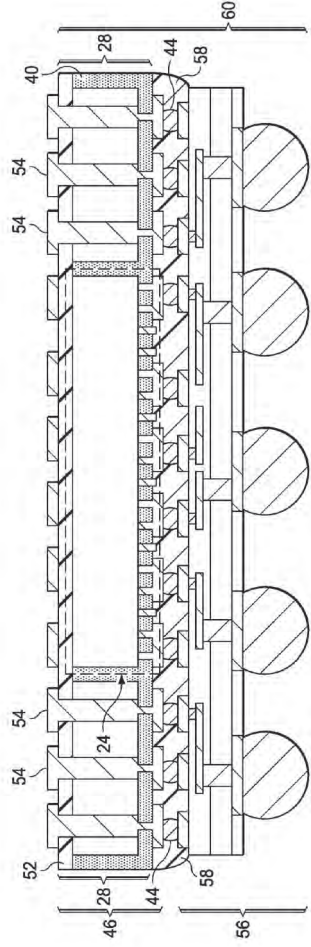


FIG. 8

Chen '402, Fig. 8

“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are

used to electrically couple the circuit devices in package component 62 to package component 56.” Chen ’402, [0019].

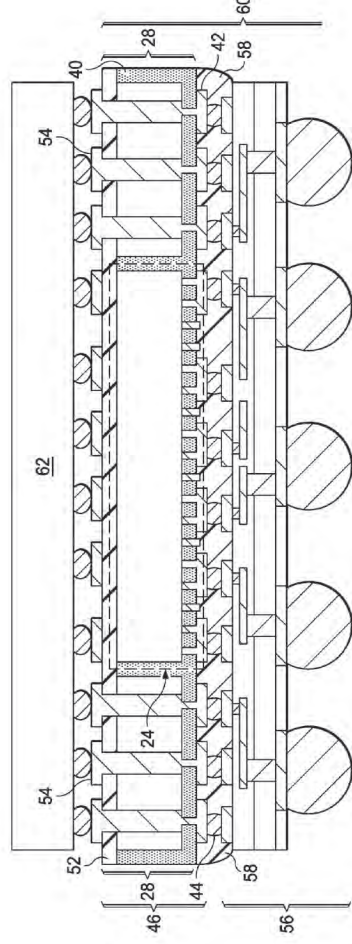


FIG. 9

Chen '402, Fig. 9

“FIG. 10 illustrates an exemplary embodiment wherein package component 62 includes a plurality of stacked dies 64. In some embodiments, stacked dies 64 are memory dies. Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to package component 24, which are further connected to the RDLs 54 over and aligned to TAV modules 28. In these embodiments, package component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56.”
Chen '402, [0020].

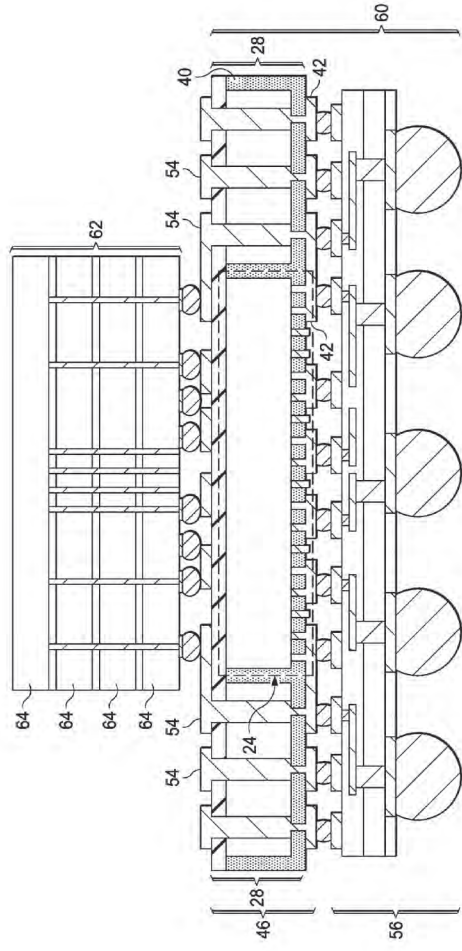


FIG. 10

Chen '402, Fig. 10

“In accordance with other embodiments, a device includes a bottom package, and a top package component bonded to the bottom package. The bottom package includes a package substrate, a plurality of connectors over the package substrate, and a package. The package includes a device die, and a TAV Module substantially level with the device die. The TAV module is free from active devices therein, and includes a substrate and a plurality of through-vias penetrating through the substrate. A molding compound contacts a bottom surface of the device die, a bottom surface of the TAV module, and sidewalls of the device die and the TAV module. A plurality of RDLs is under the molding compound and electrically coupled to the device die and the plurality of through-vias in the TAV module. The plurality of RDLs is

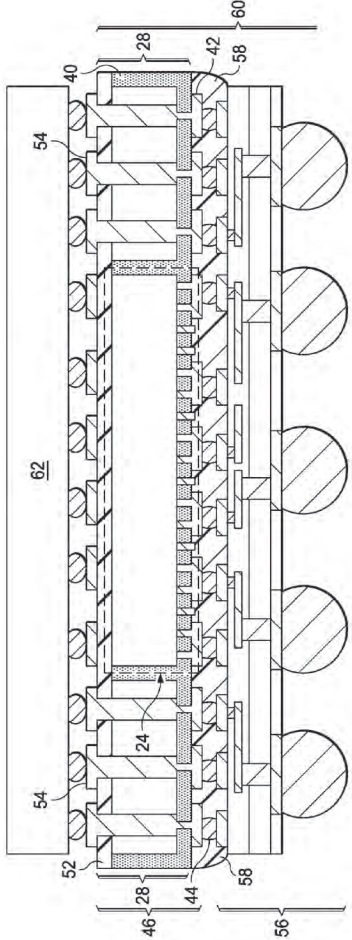
Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>bonded to the package substrate through the plurality of connectors.” Chen ’402, [0023-0024].</p> <p>To the extent Plaintiff contends that Chen ’402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

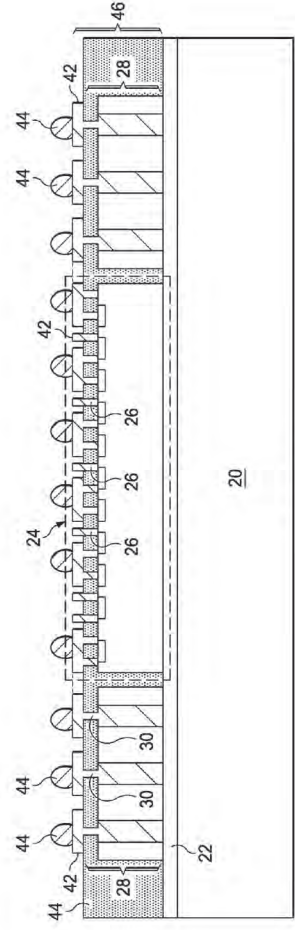
Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Chen ’402 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“FIGS. 1 through 9 are cross-sectional views and a top view of intermediate stages in the manufacturing of a Package-on-Package (PoP) structure in accordance with some exemplary embodiments. FIG. 1 illustrates carrier 20 and release layer 22 on carrier 20. Carrier 20 may be a glass carrier, a ceramic carrier, or the like. Release layer 22 may be formed of an adhesive such as an Ultra-Violet (UV) glue. Package component 24 and Through-Assembly Via (TAV) modules 28 are then placed on release layer 22. The bottom surfaces of package component 24 and TAV modules 28 are in contact with the top surface of release layer 22,</p>

	<p>and are level with each other. The position of package component 24 and TAV modules 28 are accurately aligned to desirable locations, so that the subsequent formed redistribution lines may electrically couple to metal posts 26 and 30. In some embodiments, package component 24 includes one or a plurality of device dies. For example, package component 24 may include a Central Computing Unit (CPU) die or another type of logic die having logic circuits. In alternative embodiments, package component 24 includes a plurality of memory dies stacked together (please refer to FIG. 11). In the embodiments wherein package component 24 is a device die, package component 24 may include semiconductor substrate 25 and active devices (such as transistors) 27 at a top surface of semiconductor substrate 25. The bottom surface of semiconductor substrate 25 is thus in contact with release layer 22. Semiconductor substrate 25 may be free from through-substrate vias formed therein, although through-substrate vias may also be formed to penetrate through semiconductor substrate 25. Package component 24 may also be a package that includes device die(s), interposer(s), package substrate(s) (not shown), and/or the like. Metal posts 26 (such as copper posts) are formed as a top portion of package component 24.” Chen ’402, [0009].</p> <p>“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” Chen ’402, [0019].</p> <p>“FIG. 10 illustrates an exemplary embodiment wherein package component 62 includes a plurality of stacked dies 64. In some embodiments, stacked dies 64 are memory dies. Stacked dies 64 may be bonded to RDLs 54 that are over and aligned to package component 24, which are further connected to the RDLs 54 over and aligned to TAV modules 28. In these</p>
--	--

	<p>embodiments, package component 24 may be electrically coupled to stacked dies 64, for example, through RDLs 54, TAV modules 28, RDLs 42, and/or package component 56.” Chen '402, [0020].</p>  <p>Chen '402, Fig. 9</p> <p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p>	<p>Chen '402 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“No active devices such as transistors are formed in TAV modules 28. In accordance with some embodiments, TAV modules 28 do not include passive devices such as capacitors, inductors, resistors, and/or the like. In alternative embodiments, TAV modules 28 may include the passive devices therein. Exemplary capacitor 36 is illustrated in FIG. 12, which capacitor 36 includes two or more parallel metal strips 66 that penetrate through substrate 34 to form the capacitor plates of capacitor 36. TAV modules 28 may include redistribution layer(s) that include redistribution lines and metal pads on the top sides of TAV modules 28. Alternatively, no redistribution layer is formed on either side of one or each of TAV modules 28, and metal posts 30 are connected to, and are aligned to, through-substrate vias 32, with no redistribution lines between metal posts and through-substrate vias 32.” Chen '402, [0011].</p> <p>“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer. In some exemplary embodiments, the formation of connectors 44 includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls. In alternative embodiments, the formation of connectors 44 includes performing</p>

	<p>a plating step to form solder regions on RDLs 42, and then reflowing the solder regions. Connectors 44 may also include metal pillars, or metal pillars and solder caps, which may also be formed through plating. Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen ’402, [0014].</p> <div></div> <p>FIG. 4</p> <p>Chen ’402, Fig. 4</p> <p>“FIG. 9 illustrates the bonding of top package component 62 to bottom package 60. In some embodiments, top package component 62 is a device die. Alternatively, package component 62 is a package that includes a device die (not shown) bonded to a package substrate (not shown), an interposer (not shown), or the like. In the resulting package, TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 5” Chen ’402, [0019].</p>
--	---

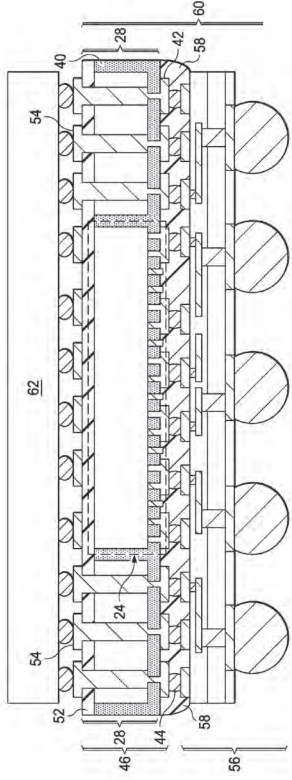


FIG. 9

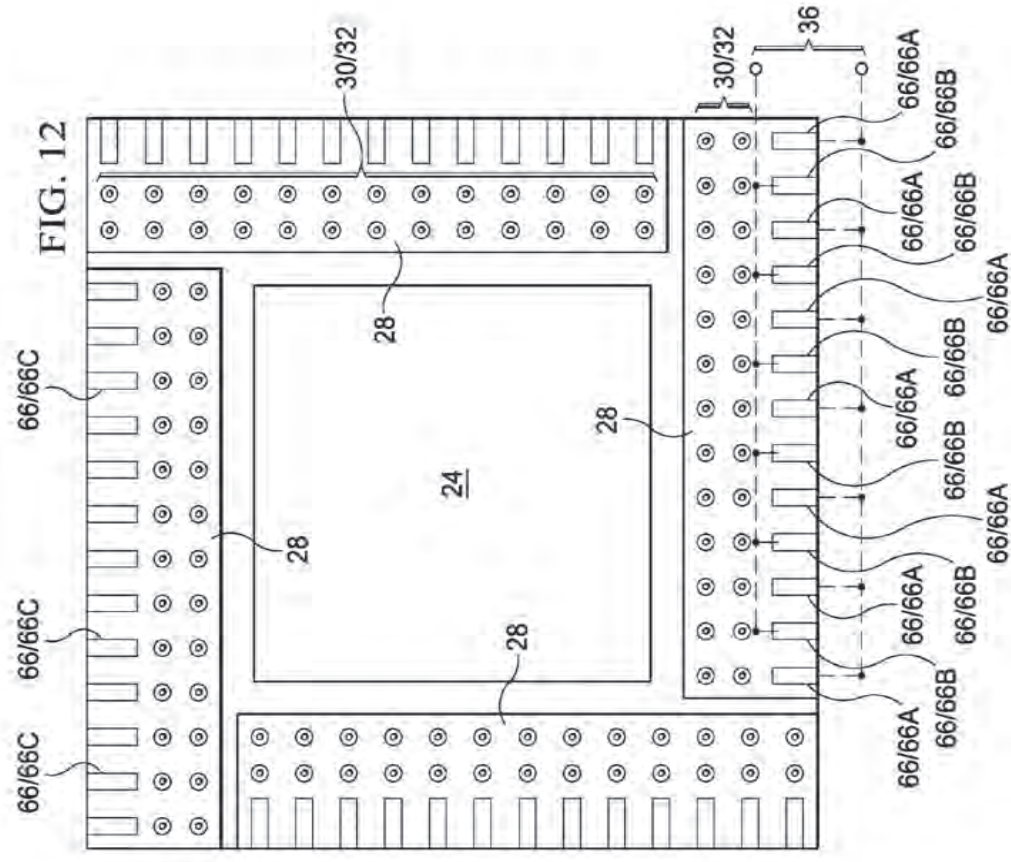
Chen '402, Fig. 9

“In the embodiments, the connection between top package component 62 and bottom package 60 is through TAV modules 28, rather than large solder balls” Chen '402, [0021].

“FIG. 12 illustrates a top view of the structure in FIG. 1 in accordance with alternative embodiments. In TAV modules 28, besides through-substrate vias 32, which are used for electrically connecting the features on opposite sides of TAV modules 28, strip-shaped vias 66 may also be formed. In accordance with some embodiments, strip-shaped vias 66 are used for dissipating the heat generated in package component 24 as in FIGS. 9 through 11. Accordingly, strip-shaped vias 66 (such as 66C) may be electrically floating when TAV modules 28 are used in the package structure in FIGS. 9 through 11. In these embodiments, since strip-shaped vias 66C are formed of metals that have good thermal conductivity, the heat dissipating ability is improved over that of molding compound. In alternative embodiments, strip-shaped vias 66 may be interconnected to form a capacitor. For example, in FIG. 12, strip-shaped vias 66 include strip-shaped vias 66A that are interconnected to form

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	one of the capacitor plates, and strip-shaped vias 66B that are interconnected to form the other capacitor plate. Strip-shaped vias 66A and strip-shaped vias 66B are laid out in an alternating pattern to increase the capacitance.” Chen ’402, [0022].
--	---



Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>Chen '402, Fig. 12</p> <p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

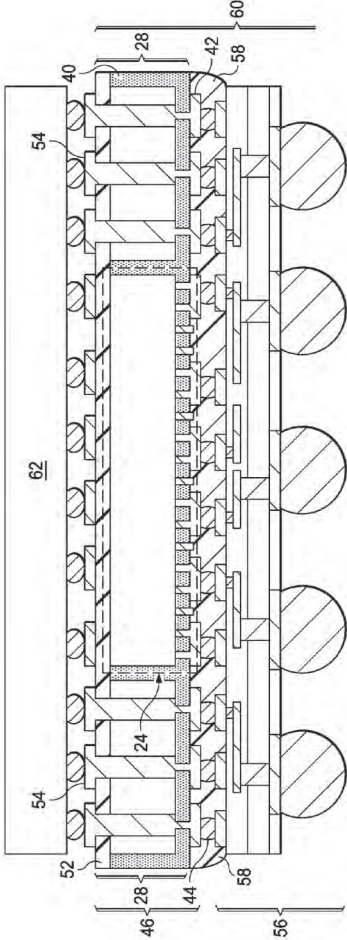
Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Chen '402 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Metal posts 26 (such as copper posts) are formed as a top portion of package component 24. TAV modules 28 are integrated modules that are pre-formed before being placed on release layer 22. TAV modules 28 include substrate 34, which may be a semiconductor substrate such as a silicon substrate. Alternatively, substrate 34 is a dielectric substrate such as a glass substrate. Through-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34.” Chen '402, [0009-0010].</p>

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>“In some embodiments, bottom ends 32 A of through-substrate vias 32 are level with the bottom surface 34 A of substrate 34. Accordingly, bottom ends 32 A of through-substrate vias 32 may be in contact with release layer 22. TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal post 26 and 30 are substantially level with each other.” Chen ’402, [0010].</p> <p>“TAV modules 28 may include redistribution layer(s) that include redistribution lines and metal pads on the top sides of TAV modules 28. Alternatively, no redistribution layer is formed on either side of one or each of TAV modules 28, and metal posts 30 are connected to, and are aligned to, through-substrate vias 32, with no redistribution lines between metal posts and through-substrate vias 32.” Chen ’402, [0011].</p> <p>“A grinding step may be performed to grind polymer 40, until metal posts 26 and 30 are exposed. Line 39 marks an exemplary position of the top surface of polymer 40 after the grinding. Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30.” Chen ’402, [0013-0014].</p> <p>“Next, referring to FIG. 4, Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer.” Chen ’402, [0014].</p> <p>“Referring to FIG. 6, after the carrier switch, the back surface of TAV modules 28 is exposed, and through-substrate vias 32 in TAV modules 28 are exposed. In some embodiments, a grinding is performed to lightly grind the back surface of package component 24 and TAV modules 28, so that through-substrate vias 32 protrude above the back surface of substrate</p>
--	---

	<p>34. Alternatively, the grinding step is skipped. When no grinding is performed, surfaces 32 A of through-substrate vias 32 are level with back surface 34 A of substrate 34. As shown in FIG. 7, dielectric layer 52 is formed on the illustrated top surface of package 46. In some embodiments, dielectric layer 52 includes a polymer, which may be polyimide, benzocyclobutene (BCB), or the like. Dielectric layer 52 may also be formed of a light-sensitive material, which may be exposed in a lithography step, and then patterned. Alternatively, dielectric layer 52 may be formed of other materials such as oxides, nitrides, combination thereof, and multilayers thereof. RDLs 54 are then formed on dielectric layer 52 and connected to RDLs 54. RDLs 54 may extend to over and aligned to package component 24. Accordingly, RDLs 54 have a fan-in structure. The RDLs 54 that are over and aligned to package component 24 may be connected to the RDLs over and aligned to TAV modules 28. The dashed portions of RDLs 54 illustrate the connecting portions of RDLs 54. Next, carrier 48 (FIG. 6) is demounted from package 46. The formation of package 46 is thus finished. Referring to FIG. 8, package 46 is bonded to package component 56 to form bottom package 60.” Chen '402, [0016-0018].</p>
--	---

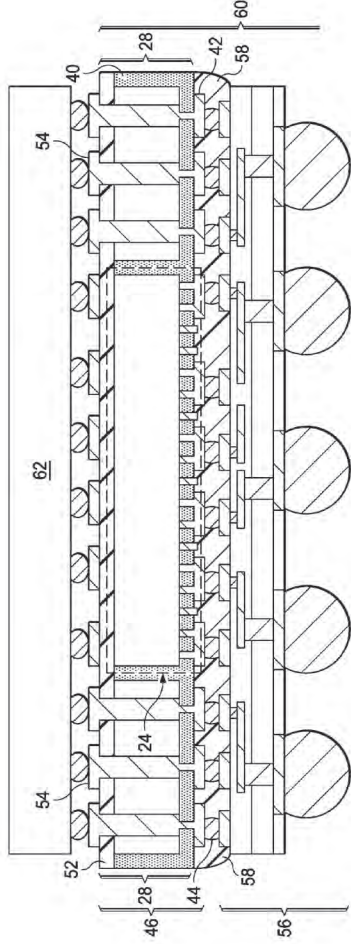
	<div><p style="text-align: center;">FIG. 9</p><p>Chen '402, Fig. 9</p><p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to	Chen '402 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

<p>the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“TAV modules 28 include substrate 34, which may be a semiconductor substrate such as a silicon substrate. Alternatively, substrate 34 is a dielectric substrate such as a glass substrate. Through-substrate vias 32 are formed in substrate 34 for inter-coupling the conductive features on opposite sides of substrate 34. Through-substrate vias 32 are formed of a conductive material, which may include copper, aluminum, tungsten, and/or the like. In some embodiments, bottom ends 32 A of through-substrate vias 32 are level with the bottom surface 34 A of substrate 34. Accordingly, bottom ends 32 A of through-substrate vias 32 may be in contact with release layer 22. TAV modules 28 may also include metal posts 30 (such as copper posts) formed as top portions of TAV modules 28. The top surfaces of metal post 26 and 30 are substantially level with each other. No active devices such as transistors are formed in TAV modules 28. In accordance with some embodiments, TAV modules 28 do not include passive devices such as capacitors, inductors, resistors, and/or the like. In alternative embodiments, TAV modules 28 may include the passive devices therein. Exemplary capacitor 36 is illustrated in FIG. 12, which capacitor 36 includes two or more parallel metal strips 66 that penetrate through substrate 34 to form the capacitor plates of capacitor 36. TAV modules 28 may include redistribution layer(s) that include redistribution lines and metal pads on the top sides of TAV modules 28.” Chen '402, [0010-0011].</p>
--	---



Chen '402, Fig. 9

“Redistribution Lines (RDLs) 42 and connectors 44 are formed to connect to metal posts 26 and 30. As indicated by dashed lines, RDLs 42 may also interconnect metal posts 26 and 30. RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer. In some exemplary embodiments, the formation of connectors 44 includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls. In alternative embodiments, the formation of connectors 44 includes performing a plating step to form solder regions on RDLs 42, and then reflowing the solder regions. Connectors 44 may also include metal pillars, or metal pillars and solder caps, which may also be formed through plating. Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46.” Chen '402, [0014].

Appendix A-3 - Invalidity of U.S. Patent No. 9859202 in view of Chen '402 - U.S. Patent Publication No. 20130182402

	<p>To the extent Plaintiff contends that Chen '402 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Chen '484 - U.S. Patent Publication No. 20150102484

U.S. Patent Publication No. 20150102484 (“Chen ’484”) is titled Package Structure and Fabrication Method Thereof and lists Chia-Cheng Chen, Ming-Chen Sun, Tzu-Chieh Shen, Liang-yi Hung, Wei-chung Hsiao, Yu-cheng Pai, Shih-Chao Chiu, Don-Son Jiang, Yi-Feng Chang, and Lung-Yuan Wang as inventors. Chen ’484 is assigned to Siliconware Precision Industries Co., Ltd. Chen ’484 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Chen ’484 is a U.S. patent publication that was filed December 20, 2013 and published April 16, 2015. Chen ’484 claims priority to TW 102137271 filed on October 16, 2013. Chen ’484 is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Chen ’484, or otherwise rendered obvious by disclosures and teachings of Chen ’484, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Chen ’484 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Chen ’484 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Chen ’484, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

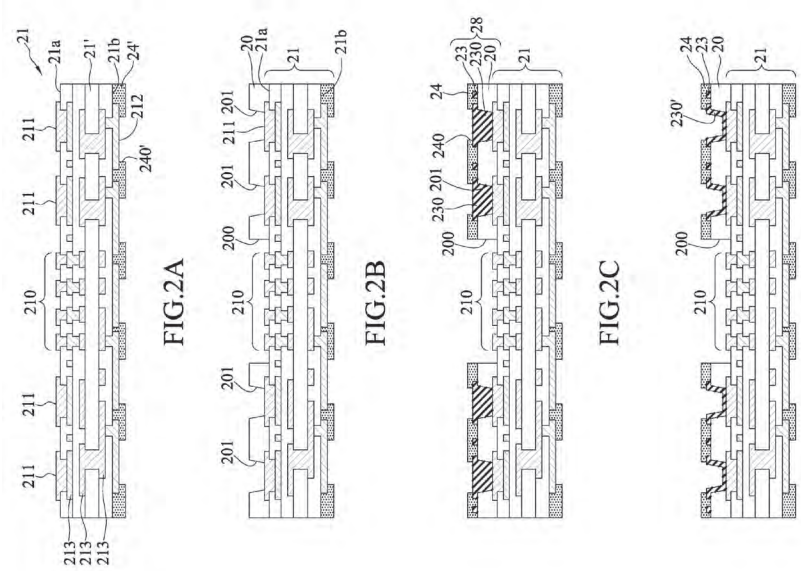
Where the chart below states that Chen '484 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Chen '484 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Chen '484 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Chen '484 discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“In view of the above-described drawbacks, the present invention provides a package structure, which comprises: a first substrate; a build-up layer formed on and electrically connected to the first substrate and having a cavity; at least an electronic element disposed in the cavity and electrically connected to the first substrate; a stack member disposed on the build-up layer so as to be stacked on the first substrate; and an encapsulant formed between the build-up layer and the stack member.” Chen '484, [0011].</p>

“FIGS. 2A to 2F are schematic cross-sectional views showing a method for fabricating a package structure 2 according to the present invention.” Chen ’484, [0031].



Chen ’484, FIGS. 2A, 2B, 2C, 2C’

“FIGS. 3 and 4 are schematic cross-sectional views showing other embodiments of the package structure of the present invention.” Chen ’484, [0032].

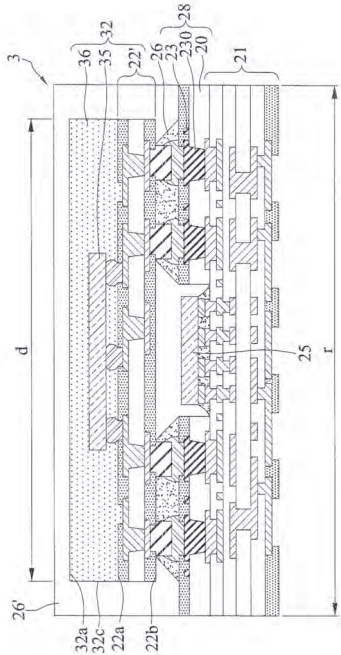


FIG.3

Chen ’484, FIG. 3

“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an electronic element 26, 26’ disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26’ formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32.” Chen ’484, [0052-0054].

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>“Therefore, the present invention forms on the first substrate 21 the build-up layer 28 having the conductive members 230 embedded in the dielectric layer 20 and stacks the stack member 22, 32 on the build-up layer 28, thus achieving a stand-off effect on the conductive members 230 and preventing solder bridging from occurring therebetween.” Chen ’484, [0057].</p> <p>“In the present embodiment, the build-up layer 28, 48 has: at least a dielectric layer 20 formed on the first substrate 21, a circuit layer 23 formed on the dielectric layer 20, and a plurality of conductive members 230 formed in and exposed from the dielectric layer 20.” Chen ’484, [0062].</p>
[1.A] a bottom package substrate;	<p>Chen ’484 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the above-described package structure and method, the first substrate can be a circuit board.” Chen ’484, [0021].</p> <p>“Referring to FIG. 2A, a first substrate 21 having a first surface 21 a and a second surface 21 b opposite to the first surface 21 a is provided. In the present embodiment, the first substrate 21 is a circuit board having a core layer 21 ’ and a plurality of circuits 213 formed on upper and lower sides of the core layer 21 ’. Further, the first surface 21 a of the first substrate 21 has a plurality of first bonding pads 210 and a plurality of second bonding pads 211, and the second surface 21 b of the first substrate 21 has a plurality of third bonding pads 212.” Chen ’484, [0036-0037].</p>

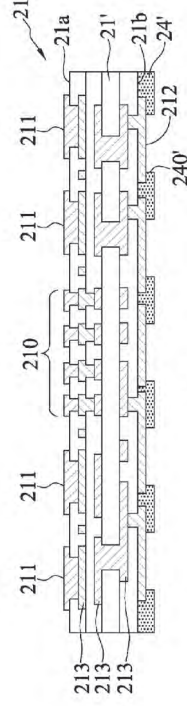


FIG. 2A

Chen '484, FIG. 2A

“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27.” Chen ’484, [0050-0051].

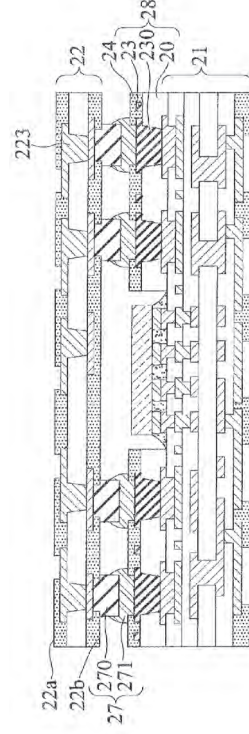


FIG.2E

Chen '484, FIG. 2E

“Referring to FIG. 2F, an encapsulant 26 is formed between the first surface 21 a of the first substrate 21 and the stack member 22. In the present embodiment, the encapsulant 26 is formed between the dielectric layer 20 (or the insulating layer 24) and the stack member 22, but is not formed in the cavity 200.” Chen ’484, [0053-0054].

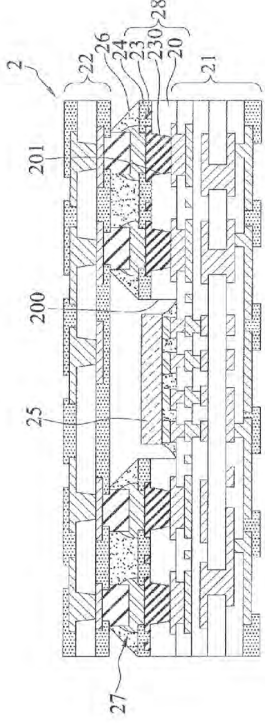


FIG.2F

Chen ’484, FIG. 2F

“In another embodiment, referring to FIG. 3, the width d of the stack member 32 is less than the width r of the first substrate 21 so as for the encapsulant 26 ’ to encapsulate both side and upper surfaces 32 c, 32 a of the stack member 32.” Chen ’484, [0055].

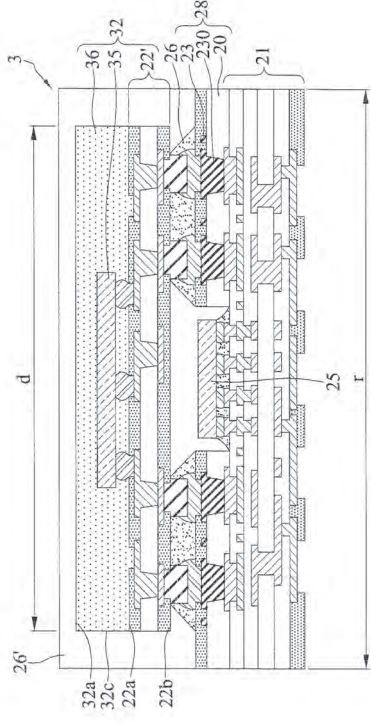


FIG.3

Chen '484, FIG. 3

“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ' formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32. The first substrate 21 is a circuit board, which has opposite first and second surfaces 21 a, 21 b.” Chen '484, [0059-0060].

To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Chen '484 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28.”</p> <p>Chen '484, [0050-0051].</p> <div> </div> <p style="text-align: center;">FIG. 2E</p> <p>Chen '484, FIG. 2E</p>

“Further, referring to FIG. 3, the stack member 32 can be a package, which has: a substrate 22', an electronic element 35 disposed on an upper surface 22 a of the substrate 22', and an encapsulant 36 formed on the upper surface 22 a of the substrate 22' for encapsulating the electronic element 35. The electronic element 35 is electrically connected to the substrate 22' in a flip-chip manner or through wire bonding.” Chen '484, [0052].

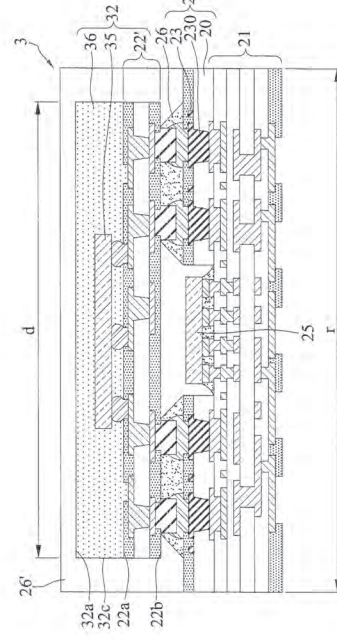


FIG. 3

Chen '484, FIG. 3

“Referring to FIG. 2F, an encapsulant 26 is formed between the first surface 21 a of the first substrate 21 and the stack member 22. In the present embodiment, the encapsulant 26 is formed between the dielectric layer 20 (or the insulating layer 24) and the stack member 22, but is not formed in the cavity 200.” Chen ’484, [0053-0054].

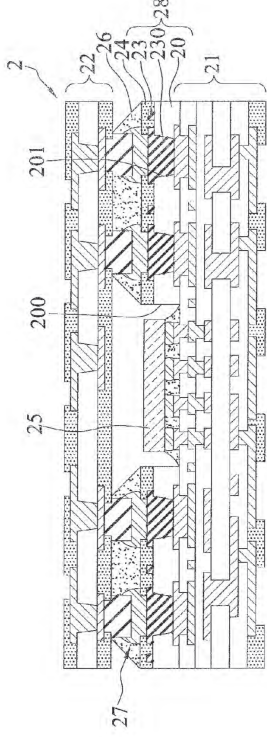


FIG.2F

Chen '484, FIG. 2F

“In another embodiment, referring to FIG. 3, the width d of the stack member 32 is less than the width r of the first substrate 21 so as for the encapsulant 26 to encapsulate both side and upper surfaces 32 c, 32 a of the stack member 32.” Chen '484, [0055].

“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21; an electronic element 25 disposed on and electrically connected to the first substrate 21; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21; and an encapsulant 26, 26' formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32. The first substrate 21 is a circuit board, which has opposite first and second surfaces 21 a, 21 b.” Chen '484, [0059-0060].

“The stack member 22, 32 is disposed on the build-up layer 28, 48. In particular, the stack member 22, 32 is bonded to the conductive members 230, 230' through a plurality of conductive elements 27 so as to be stacked on the first substrate 21.” Chen '484, [0065-0066].

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Chen '484 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Therefore, by forming the build-up layer on the first substrate so as to stack the stack member on the build-up layer, the present invention achieves a stand-off effect and prevents solder bridging. Further, the size of the conductive members can be controlled through the openings of the dielectric layer so as to cause the conductive members to have a uniform height.” Chen '484, [0028-0029].</p> <p>“Referring to FIG. 2B, a dielectric layer 20 is formed on the first surface 21 a of the first substrate 21. The dielectric layer 20 has a cavity 200 for exposing the first bonding pads 210 and a portion of the first surface 21 a around peripheries of the first bonding pads 210, and a plurality of openings 201 for exposing the second bonding pads 211. In the present embodiment, the dielectric layer 20 is laminated on the first surface 21 a of the first substrate 21 first and then the cavity 200 and the openings 201 are formed in the dielectric layer 20 by laser drilling. In other embodiments, the cavity 200 and the openings 201 are formed in the dielectric layer 20 first and then the dielectric layer 20 having the cavity 200 and the openings 201 is laminated on the first surface 21 a of the first substrate 21. The dielectric layer 20 can</p>
---	--

be made of prepreg (PP). Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28. The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21. In the present embodiment, an insulating layer 24, such as a solder mask layer, is formed on the dielectric layer 20 and the circuit layer 23, and a plurality of openings 240 are formed in the insulating layer 24 for exposing the conductive members 230.” Chen ’484, [0040-0044].

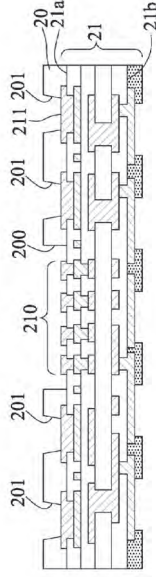


FIG.2B

Chen ’484, FIG. 2B

“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0050-0051].

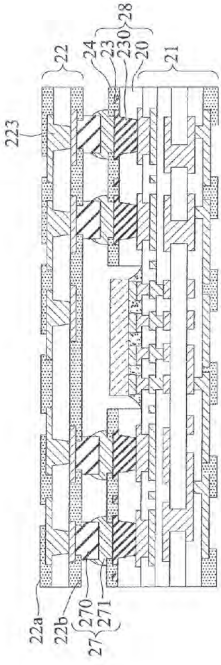


FIG. 2E

Chen '484, FIG. 2E

“Referring to FIG. 2F, an encapsulant 26 is formed between the first surface 21 a of the first substrate 21 and the stack member 22. In the present embodiment, the encapsulant 26 is formed between the dielectric layer 20 (or the insulating layer 24) and the stack member 22, but is not formed in the cavity 200. Therefore, the conductive elements 27 are encapsulated by the encapsulant 26, but the electronic element 25 is not encapsulated by the encapsulant 26.” Chen '484, [0053-0054].

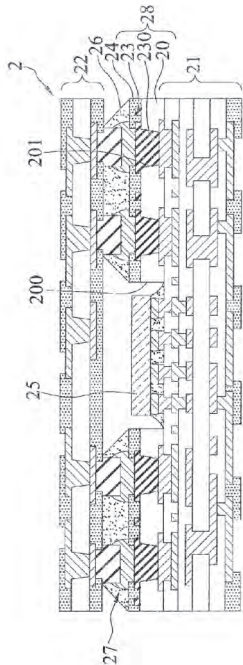


FIG. 2F

Chen '484, FIG. 2F

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>“Therefore, the present invention forms on the first substrate 21 the build-up layer 28 having the conductive members 230 embedded in the dielectric layer 20 and stacks the stack members 22, 32 on the build-up layer 28, thus achieving a stand-off effect on the conductive members 230 and preventing solder bridging from occurring therebetween.” Chen ’484, [0057].</p> <p>“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ’ formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32.” Chen ’484, [0059].</p> <p>To the extent Plaintiff contends that Chen ’484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Chen ’484 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The dielectric layer 20 can be made of prepreg (PP).” Chen ’484, [0016].</p> <p>“In the present embodiment, the first substrate 21 is a circuit board having a core layer 21 ’ and a plurality of circuits 213 formed on upper and lower sides of the core layer 21 ’.” Chen ’484, [0037].</p>

“In the present embodiment, the dielectric layer 20 is laminated on the first surface 21 a of the first substrate 21 first and then the cavity 200 and the openings 201 are formed in the dielectric layer 20 by laser drilling. In other embodiments, the cavity 200 and the openings 201 are formed in the dielectric layer 20 first and then the dielectric layer 20 having the cavity 200 and the openings 201 is laminated on the first surface 21 a of the first substrate 21. The dielectric layer 20 can be made of prepreg (PP). Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28.” Chen ’484, [0041-0043].

“In another embodiment, referring to FIG. 4, the build-up layer 48 of the package structure 4 has a plurality of dielectric layers 20 and a plurality of circuit layers 23.” Chen ‘484, [0056].

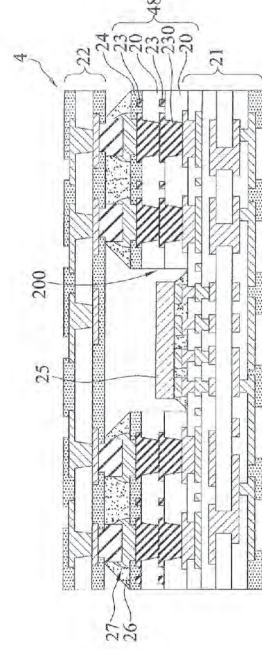


FIG. 4

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>Chen '484, FIG. 4</p> <p>“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ' formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32.” Chen '484, [0059].</p> <p>“In the present embodiment, the build-up layer 28, 48 has: at least a dielectric layer 20 formed on the first substrate 21, a circuit layer 23 formed on the dielectric layer 20, and a plurality of conductive members 230 formed in and exposed from the dielectric layer 20.” Chen '484, [0062].</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Chen '484 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2B, a dielectric layer 20 is formed on the first surface 21 a of the first substrate 21. The dielectric layer 20 has a cavity 200 for exposing the first bonding pads 210 and a portion of the first surface 21 a around peripheries of the first bonding pads 210, and a</p>

plurality of openings 201 for exposing the second bonding pads 211. In the present embodiment, the dielectric layer 20 is laminated on the first surface 21 a of the first substrate 21 first and then the cavity 200 and the openings 201 are formed in the dielectric layer 20 by laser drilling." Chen '484, [0040-0041].

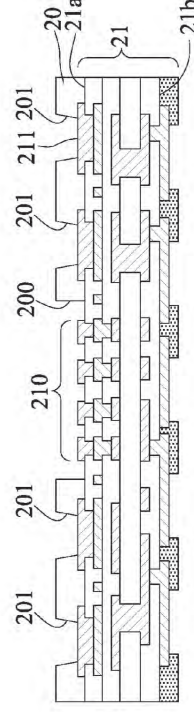
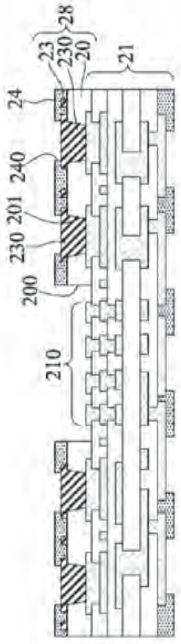
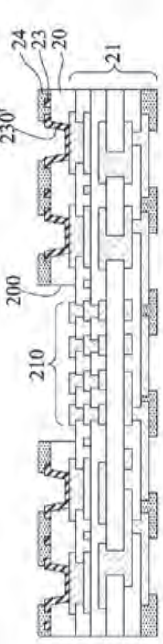


FIG. 2B

Chen '484, FIG. 2B

“Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28. The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21. In the present embodiment, an insulating layer 24, such as a solder mask layer, is formed on the dielectric layer 20 and the circuit layer 23, and a plurality of openings 240 are formed in the insulating layer 24 for exposing the conductive members 230. Further, the conductive members 230 are made of a metal material, such as copper, and the conductive members 230 are of a pillar shape.” Chen ’484, [0043-0045].



Chen '484, FIGS. 2C, 2C'

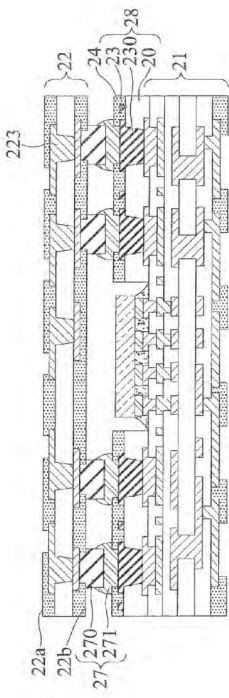
“In another embodiment, referring to FIG. 2 C’, the conductive members 230 ’ can be of a groove shape.” Chen ’484, [0046].

“In the present embodiment, the build-up layer 28, 48 has: at least a dielectric layer 20 formed on the first substrate 21, a circuit layer 23 formed on the dielectric layer 20, and a plurality of conductive members 230 formed in and exposed from the dielectric layer 20. In particular, the cavity 200 penetrates the dielectric layer 20. The dielectric layer 20 further has a plurality of openings 201. The dielectric layer 20 can be made of prepreg. The conductive members 230, 230 ’ are formed in the openings 201 of the dielectric layer 20 for electrically connecting

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>the circuit layer 23 and the first substrate 21. The conductive members 230, 230 ' are made of metal and of a pillar shape or a groove shape." Chen '484, [0062-0063].</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Chen '484 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>"Further, the first surface 21 a of the first substrate 21 has a plurality of first bonding pads 210 and a plurality of second bonding pads 211, and the second surface 21 b of the first substrate 21 has a plurality of third bonding pads 212." Chen '484, [0037].</p> <p>"Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28. The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21. In the present embodiment, an insulating layer 24, such as a solder mask layer, is formed on the dielectric layer 20 and the circuit layer 23, and a plurality of openings 240 are formed in the insulating layer 24 for exposing the conductive members 230." Chen '484, [0043-0044].</p>

	<p>“Referring to FIG. 2D, an electronic element 25 is disposed on the first bonding pads 210 in the cavity 200 through a plurality of solder bumps 250 and an underfill 251 is formed between the first substrate 21 and the electronic element 25 for encapsulating the solder bumps 250.” Chen ’484, [0047].</p> <div></div> <p style="text-align: center;">FIG.2D</p> <p>Chen ’484, FIG. 2D</p> <p>“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28. Alternatively, a plurality of conductive elements 27 each consisting of a metal pillar 270 (such as a copper pillar) and a solder material 271 formed on the metal pillar 270 can be formed between the conductive members 230 and the stack member 22 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0050-0051].</p>
--	---

	 <p>FIG. 2E</p> <p>Chen '484, FIG. 2E</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Chen '484 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

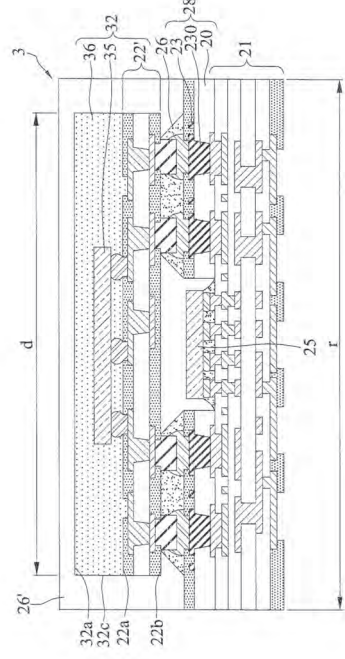


FIG. 3

Chen '484, FIG. 3

To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Chen '484 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.

See, e.g.:

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>“In the above-described package structure and method, the stack member can be bonded to the build-up layer through a plurality of conductive elements.” Chen ’484, [0024].</p> <p>“Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28. The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21. In the present embodiment, an insulating layer 24, such as a solder mask layer, is formed on the dielectric layer 20 and the circuit layer 23, and a plurality of openings 240 are formed in the insulating layer 24 for exposing the conductive members 230. Further, the conductive members 230 are made of a metal material, such as copper, and the conductive members 230 are of a pillar shape.” Chen ’484, [0043-0045].</p> <p>“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28. Alternatively, a plurality of conductive elements 27 each consisting of a metal pillar 270 (such as a copper pillar) and a solder material 271 formed on the metal pillar 270 can be formed between the conductive members 230 and the stack member 22 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0050-0051].</p>
--	--

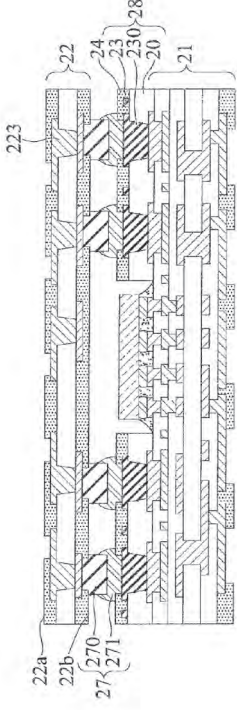


FIG. 2E

Chen '484, FIG. 2E

“Further, referring to FIG. 3, the stack member 32 can be a package, which has: a substrate 22', an electronic element 35 disposed on an upper surface 22 a of the substrate 22', and an encapsulant 36 formed on the upper surface 22 a of the substrate 22' for encapsulating the electronic element 35. The electronic element 35 is electrically connected to the substrate 22' in a flip-chip manner or through wire bonding.” Chen '484, [0052].

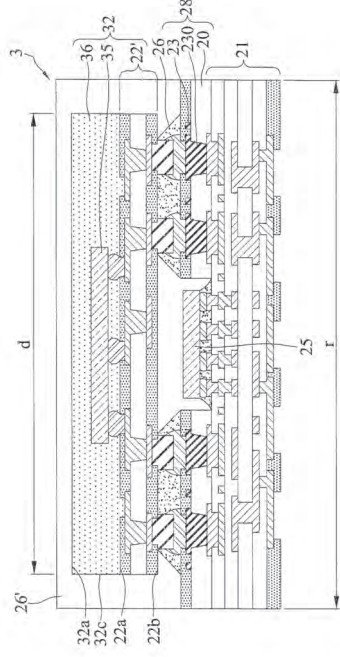


FIG. 3

Chen '484, FIG. 3

“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21; an electronic element 25 disposed on and electrically connected to the first substrate 21; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21; and an encapsulant 26, 26' formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32. The first substrate 21 is a circuit board, which has opposite first and second surfaces 21 a, 21 b. The build-up layer 28, 48 has a cavity 200 exposing a portion of the first surface 21 a of the first substrate 21. In the present embodiment, the build-up layer 28, 48 has: at least a dielectric layer 20 formed on the first substrate 21, a circuit layer 23 formed on the dielectric layer 20, and a plurality of conductive members 230 formed in and exposed from the dielectric layer 20. In particular, the cavity 200 penetrates the dielectric layer 20. The dielectric layer 20 further has a plurality of openings 201. The

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>dielectric layer 20 can be made of prepreg. The conductive members 230, 230 ' are formed in the openings 201 of the dielectric layer 20 for electrically connecting the circuit layer 23 and the first substrate 21. The conductive members 230, 230 ' are made of metal and of a pillar shape or a groove shape. The package structure 2, 3, 4 can further have an insulating layer 24 formed on the build-up layer 28, 48 and exposing the conductive members 230, 230 '. The electronic element 25 is an active component or a passive component. The electronic element 25 is disposed on the first surface 21 a of the first substrate 21 in the cavity 200. The stack member 22, 32 is disposed on the build-up layer 28, 48. In particular, the stack member 22, 32 is bonded to the conductive members 230, 230 ' through a plurality of conductive elements 27 so as to be stacked on the first substrate 21.' Chen '484, [0059-0064].</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Chen '484 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p> <p>“Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28. The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21. In the present</p>

	<p>embodiment, an insulating layer 24, such as a solder mask layer, is formed on the dielectric layer 20 and the circuit layer 23, and a plurality of openings 240 are formed in the insulating layer 24 for exposing the conductive members 230.” Chen ’484, [0043-0044].</p> <p>“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28. Alternatively, a plurality of conductive elements 27 each consisting of a metal pillar 270 (such as a copper pillar) and a solder material 271 formed on the metal pillar 270 can be formed between the conductive members 230 and the stack member 22 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0050-0051].</p> <p>“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ’ formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32. The first substrate 21 is a circuit board, which has opposite first and second surfaces 21 a, 21 b. The build-up layer 28, 48 has a cavity 200 exposing a portion of the first surface 21 a of the first substrate 21. In the present embodiment, the build-up layer 28, 48 has: at least a dielectric layer 20 formed on the first substrate 21, a circuit layer 23 formed on the dielectric layer 20, and a plurality of conductive members 230 formed in and exposed from the dielectric layer 20. In particular, the cavity 200 penetrates</p>
--	---

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>the dielectric layer 20. The dielectric layer 20 further has a plurality of openings 201. The dielectric layer 20 can be made of prepreg. The conductive members 230, 230' are formed in the openings 201 of the dielectric layer 20 for electrically connecting the circuit layer 23 and the first substrate 21. The conductive members 230, 230' are made of metal and of a pillar shape or a groove shape. The package structure 2, 3, 4 can further have an insulating layer 24 formed on the build-up layer 28, 48 and exposing the conductive members 230, 230'." Chen '484, [0059-0063].</p> <p>"In particular, the stack member 22, 32 is bonded to the conductive members 230, 230' through a plurality of conductive elements 27 so as to be stacked on the first substrate 21." Chen '484, [0065].</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Chen '484 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>"The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21." Chen '484, [0043].</p>

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>“As such, the electronic element 25 is disposed on the first surface 21 a of the first substrate 21 to form a package, and the electronic element 25 is electrically connected to the circuits 213 and the first bonding pads 210 of the first substrate 21 in a flip-chip manner.” Chen ’484, [0047].</p> <p>“In other embodiments, the electronic element 25 can be electrically connected to the first substrate 21 through wire bonding. Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28. Alternatively, a plurality of conductive elements 27 each consisting of a metal pillar 270 (such as a copper pillar) and a solder material 271 formed on the metal pillar 270 can be formed between the conductive members 230 and the stack member 22 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0049-0051].</p> <p>“In the present embodiment, the build-up layer 28, 48 has: at least a dielectric layer 20 formed on the first substrate 21, a circuit layer 23 formed on the dielectric layer 20, and a plurality of conductive members 230 formed in and exposed from the dielectric layer 20. In particular, the cavity 200 penetrates the dielectric layer 20. The dielectric layer 20 further has a plurality of openings 201. The dielectric layer 20 can be made of prepreg. The conductive members 230, 230 ’ are formed in the openings 201 of the dielectric layer 20 for electrically connecting the circuit layer 23 and the first substrate 21. The conductive members 230, 230 ’ are made of metal and of a pillar shape or a groove shape. The package structure 2, 3, 4 can further</p>
--	---

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>have an insulating layer 24 formed on the build-up layer 28, 48 and exposing the conductive members 230, 230 '. The electronic element 25 is an active component or a passive component. The electronic element 25 is disposed on the first surface 21 a of the first substrate 21 in the cavity 200. The stack member 22, 32 is disposed on the build-up layer 28, 48. In particular, the stack member 22, 32 is bonded to the conductive members 230, 230 ' through a plurality of conductive elements 27 so as to be stacked on the first substrate 21." Chen '484, [0062-0066].</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Chen '484 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2D, an electronic element 25 is disposed on the first bonding pads 210 in the cavity 200 through a plurality of solder bumps 250 and an underfill 251 is formed between the first substrate 21 and the electronic element 25 for encapsulating the solder bumps 250. As such, the electronic element 25 is disposed on the first surface 21 a of the first substrate 21 to form a package, and the electronic element 25 is electrically connected to the circuits 213 and the first bonding pads 210 of the first substrate 21 in a flip-chip manner.” Chen '484, [0047].</p>

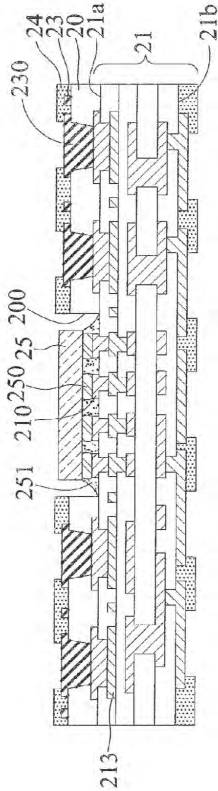


FIG.2D

Chen '484, FIG. 2D

“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25.” Chen '484, [0050].

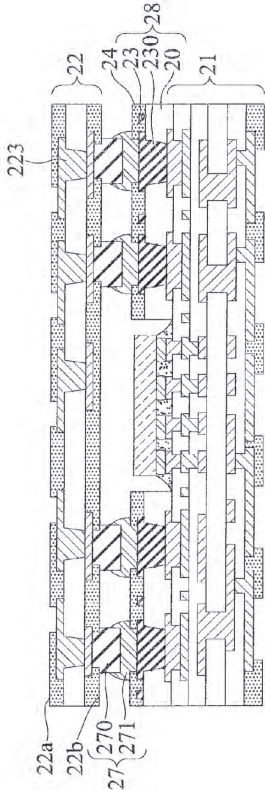


FIG.2E

Chen '484, FIG. 2E

“Referring to FIG. 2F, an encapsulant 26 is formed between the first surface 21 a of the first substrate 21 and the stack member 22. In the present embodiment, the encapsulant 26 is formed between the dielectric layer 20 (or the insulating layer 24) and the stack member 22, but is not formed in the cavity 200. Therefore, the conductive elements 27 are encapsulated by the encapsulant 26, but the electronic element 25 is not encapsulated by the encapsulant 26.” Chen ’484, [0053-0054].

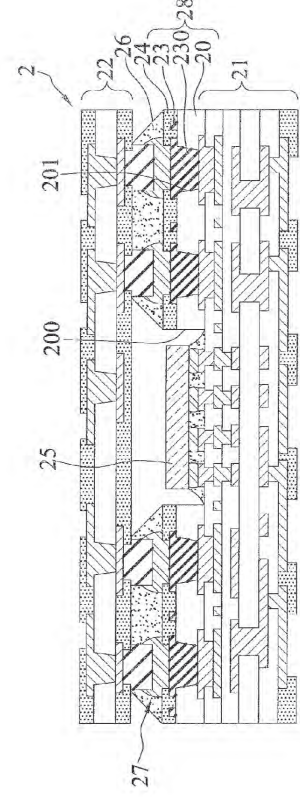


FIG.2F

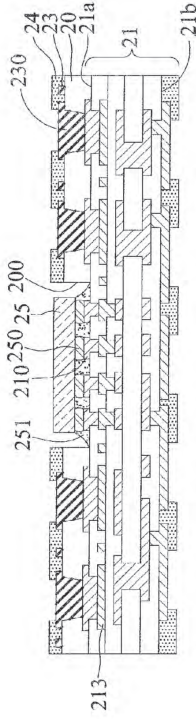
Chen ’484, FIG. 2F

“In other embodiments, the encapsulant 26 can be filled between the first surface 21 a of the first substrate 21 and the stack member 22 so as to encapsulate the conductive elements 27 and the electronic element 25.” Chen ’484, [0054].

“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an

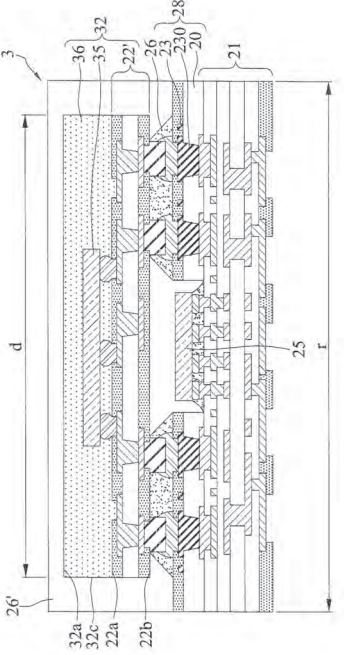
Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ' formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32. The first substrate 21 is a circuit board, which has opposite first and second surfaces 21 a, 21 b. The build-up layer 28, 48 has a cavity 200 exposing a portion of the first surface 21 a of the first substrate 21.” Chen ’484, [0059-0061].</p> <p>“The electronic element 25 is disposed on the first surface 21 a of the first substrate 21 in the cavity 200. The stack member 22, 32 is disposed on the build-up layer 28, 48. In particular, the stack member 22, 32 is bonded to the conductive members 230, 230 ' through a plurality of conductive elements 27 so as to be stacked on the first substrate 21.” Chen ’484, [0064-0065].</p> <p>To the extent Plaintiff contends that Chen ’484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Chen ’484 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In view of the above-described drawbacks, the present invention provides a package structure, which comprises: a first substrate; a build-up layer formed on and electrically connected to the first substrate and having a cavity; at least an electronic element disposed in the cavity and electrically connected to the first substrate; a stack member disposed on the</p>

	<p>build-up layer so as to be stacked on the first substrate; and an encapsulant formed between the build-up layer and the stack member.” Chen ’484, [0011].</p> <p>“Referring to FIG. 2D, an electronic element 25 is disposed on the first bonding pads 210 in the cavity 200 through a plurality of solder bumps 250 and an underfill 251 is formed between the first substrate 21 and the electronic element 25 for encapsulating the solder bumps 250. As such, the electronic element 25 is disposed on the first surface 21 a of the first substrate 21 to form a package, and the electronic element 25 is electrically connected to the circuits 213 and the first bonding pads 210 of the first substrate 21 in a flip-chip manner.” Chen ’484, [0047].</p>  <p style="text-align: center;">FIG.2D</p> <p>Chen ’484, FIG. 2D</p> <p>“As such, the electronic element 25 is disposed on the first surface 21 a of the first substrate 21 to form a package, and the electronic element 25 is electrically connected to the circuits 213 and the first bonding pads 210 of the first substrate 21 in a flip-chip manner.” Chen ’484, [0047].</p>
--	---

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>“Referring to FIG. 2D, an electronic element 25 is disposed on the first bonding pads 210 in the cavity 200 through a plurality of solder bumps 250 and an underfill 251 is formed between the first substrate 21 and the electronic element 25 for encapsulating the solder bumps 250.” Chen ’484, [0047].</p> <p>“The electronic element 25 is disposed on the first surface 21 a of the first substrate 21 in the cavity 200.” Chen ’484, [0047].</p> <p>“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ’ formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32.” Chen ’484, [0059].</p> <p>To the extent Plaintiff contends that Chen ’484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.	<p>Chen ’484 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>

	 <p style="text-align: center;">FIG. 3</p> <p>Chen '484, FIG. 3</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	Chen '484 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

downwardly from the bottom surface of the top package substrate.

See, e.g.:

“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25.” Chen ‘484, [0050].

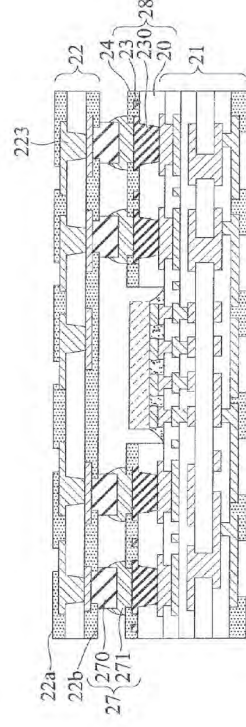


FIG. 2E

Chen '484, FIG. 2E

“Referring to FIG. 2F, an encapsulant 26 is formed between the first surface 21 a of the first substrate 21 and the stack member 22. In the present embodiment, the encapsulant 26 is formed between the dielectric layer 20 (or the insulating layer 24) and the stack member 22, but is not formed in the cavity 200. Therefore, the conductive elements 27 are encapsulated by the encapsulant 26, but the electronic element 25 is not encapsulated by the encapsulant 26.” Chen ’484, [0053-0054].

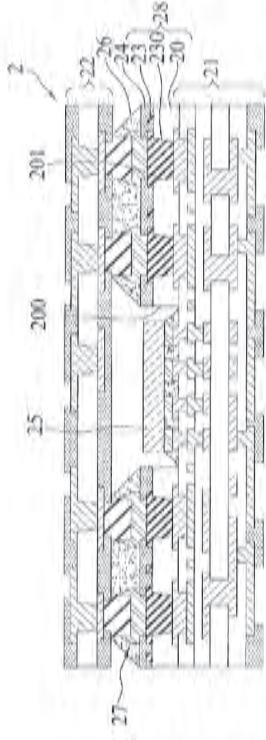


FIG. 2F

Chen '484, FIG. 2F

“In other embodiments, the encapsulant 26 can be filled between the first surface 21 a of the first substrate 21 and the stack member 22 so as to encapsulate the conductive elements 27 and the electronic element 25.” Chen '484, [0054].

“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ' formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32.” Chen '484, [0059].

“The stack member 22, 32 is disposed on the build-up layer 28, 48. In particular, the stack member 22, 32 is bonded to the conductive members 230, 230 ' through a plurality of conductive elements 27 so as to be stacked on the first substrate 21.” Chen '484, [0065-0066].

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>“In an embodiment, the encapsulant 26’ is further formed between the first substrate 21 and the stack member 32.” Chen ’484, [0066].</p> <p>To the extent Plaintiff contends that Chen ’484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Chen ’484 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“As such, the electronic element 25 is disposed on the first surface 21 a of the first substrate 21 to form a package, and the electronic element 25 is electrically connected to the circuits 213 and the first bonding pads 210 of the first substrate 21 in a flip-chip manner. In the present embodiment, the electronic element 25 is an active component, such as a chip, and/or a passive component, such as a resistor, a capacitor or an inductor. In other embodiments, the electronic element 25 can be electrically connected to the first substrate 21 through wire bonding. Referring to FIG. 2E, a stack member 22 is disposed on the conductive members</p>

230 so as to be stacked on the build-up layer 28 and cover the electronic element 25." Chen '484, [0047-0050].

“Further, referring to FIG. 3, the stack member 32 can be a package, which has: a substrate 22', an electronic element 35 disposed on an upper surface 22 a of the substrate 22', and an encapsulant 36 formed on the upper surface 22 a of the substrate 22' for encapsulating the electronic element 35. The electronic element 35 is electrically connected to the substrate 22' in a flip-chip manner or through wire bonding.” Chen '484, [0052].

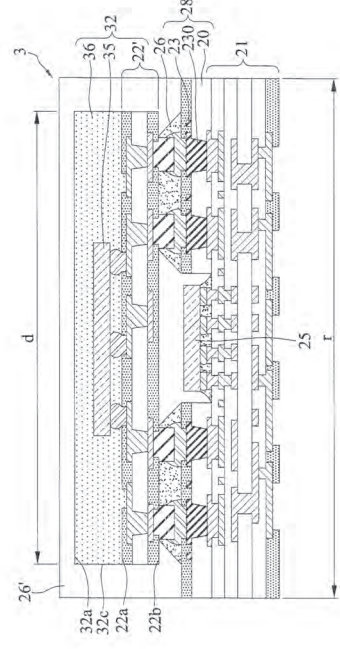


FIG. 3

Chen '484, FIG. 3

“In another embodiment, referring to FIG. 3, the width d of the stack member 32 is less than the width r of the first substrate 21 so as for the encapsulant 26 ' to encapsulate both side and upper surfaces 32 c, 32 a of the stack member 32.” Chen '484, [0055].

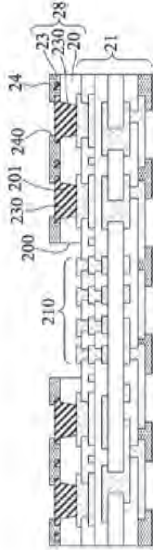
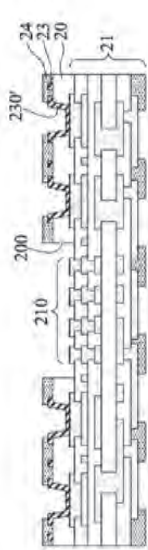
Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21 ; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21 ; an electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ' formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32.” Chen '484, [0059].</p> <p>“In an embodiment, the stack member 22 is a second substrate such as a circuit board. In another embodiment, the stack member 32 is a package. In an embodiment, the width d of the stack member 32 is less than the width r of the first substrate 21 so as for the encapsulant 26 ' to encapsulate the stack member 32.” Chen '484, [0067-0068].</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding bottom metal pillars of the top package substrate is aligned with a corresponding	Chen '484 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

<p>metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>See, e.g.:</p> <p>“Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28. The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21.” Chen ’484, [0043].</p> <div></div> <p>FIG.2C</p> <div></div> <p>FIG.2C'</p> <p>Chen ’484, FIGS. 2C, 2C’</p> <p>“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present</p>
---	---

embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0050-0051].

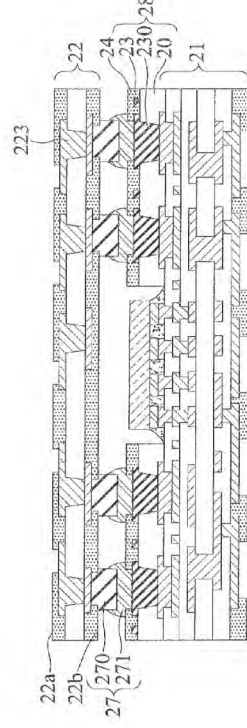


FIG. 2E

Chen '484, FIG. 2E

“In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28. Alternatively, a plurality of conductive elements 27 each consisting of a metal pillar 270 (such as a copper pillar) and a solder material 271 formed on the metal pillar 270

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>can be formed between the conductive members 230 and the stack member 22 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0051].</p> <p>“Further, the size of the conductive members 230 can be controlled through the openings 201 of the dielectric layer 20 so as to cause the conductive members 230 to have a uniform height. Therefore, the present invention overcomes the conventional drawback of joint deviation and prevents poor contacts or short circuits from occurring between the conductive elements 27 and the conductive members 230, thereby improving the product yield.” Chen ’484, [0058].</p> <p>“The conductive members 230, 230 ’ are formed in the openings 201 of the dielectric layer 20 for electrically connecting the circuit layer 23 and the first substrate 21. The conductive members 230, 230 ’ are made of metal and of a pillar shape or a groove shape.” Chen ’484, [0063].</p> <p>“In particular, the stack member 22, 32 is bonded to the conductive members 230, 230 ’ through a plurality of conductive elements 27 so as to be stacked on the first substrate 21.” Chen ’484, [0065].</p> <p>To the extent Plaintiff contends that Chen ’484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Chen '484 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28. The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21. In the present embodiment, an insulating layer 24, such as a solder mask layer, is formed on the dielectric layer 20 and the circuit layer 23, and a plurality of openings 240 are formed in the insulating layer 24 for exposing the conductive members 230.” Chen '484, [0043-0044].</p>
--	--

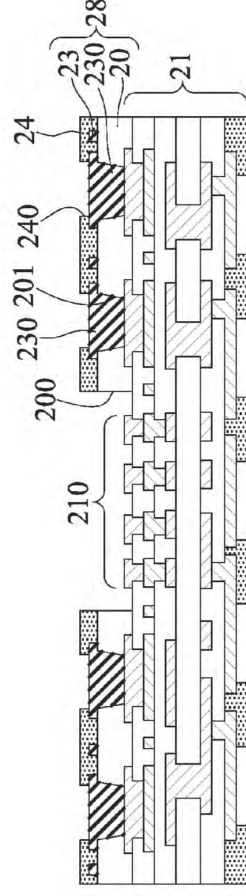


FIG. 2C

Chen '484, FIG. 2C

“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28. Alternatively, a plurality of conductive elements 27 each consisting of a metal pillar 270 (such as a copper pillar) and a solder material 271 formed on the metal pillar 270 can be formed between the conductive members 230 and the stack member 22 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0050-0051].

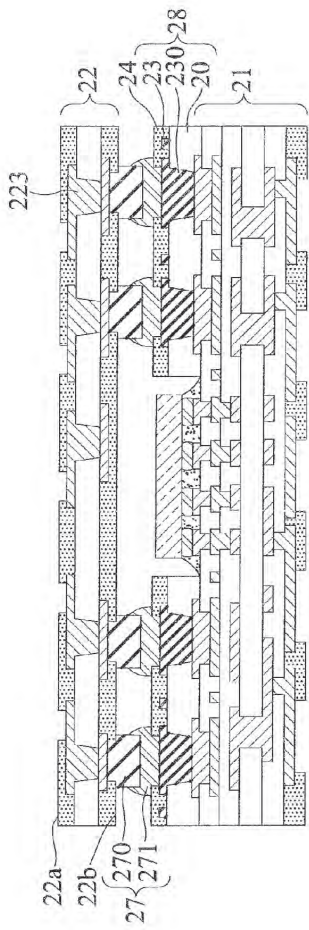


FIG. 2E

Chen '484, FIG. 2E

“In the present embodiment, the build-up layer 28, 48 has: at least a dielectric layer 20 formed on the first substrate 21, a circuit layer 23 formed on the dielectric layer 20, and a plurality of conductive members 230 formed in and exposed from the dielectric layer 20. In particular, the cavity 200 penetrates the dielectric layer 20. The dielectric layer 20 further has a plurality of openings 201. The dielectric layer 20 can be made of prepreg. The conductive members 230, 230' are formed in the openings 201 of the dielectric layer 20 for electrically connecting the circuit layer 23 and the first substrate 21.” Chen '484, [0062-0063].

“The conductive members 230, 230' are formed in the openings 201 of the dielectric layer 20 for electrically connecting the circuit layer 23 and the first substrate 21. The conductive members 230, 230' are made of metal and of a pillar shape or a groove shape. The package

Appendix A-4 - Invalidity of U.S. Patent No. 9859202 in view of Chen 2 - U.S. Patent Publication No. 20150102484

	<p>structure 2, 3, 4 can further have an insulating layer 24 formed on the build-up layer 28, 48 and exposing the conductive members 230, 230 '." Chen '484, [0063-0064].</p> <p>"The stack member 22, 32 is disposed on the build-up layer 28, 48. In particular, the stack member 22, 32 is bonded to the conductive members 230, 230 ' through a plurality of conductive elements 27 so as to be stacked on the first substrate 21." Chen '484, [0065-0066].</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the corresponding bottom metal pads of the bottom package substrate via the corresponding top metal pads of the spacer connector.	<p>Chen '484 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

“In the above-described method, forming the build-up layer can comprise: forming at least a dielectric layer on the first substrate and forming the cavity and a plurality of openings in the dielectric layer; and forming in the openings of the dielectric layer a plurality of conductive members electrically connected to the first substrate.” Chen ’484, [0015].

“In the above-described package structure and method, the stack member can be bonded to the build-up layer through a plurality of conductive elements. In the above-described package structure and method, the stack member can be a second substrate or a package. The second substrate can be a circuit board.” Chen ’484, [0024-0025].

“Referring to FIG. 2B, a dielectric layer 20 is formed on the first surface 21 a of the first substrate 21. The dielectric layer 20 has a cavity 200 for exposing the first bonding pads 210 and a portion of the first surface 21 a around peripheries of the first bonding pads 210, and a plurality of openings 201 for exposing the second bonding pads 211.” Chen ’484, [0040].

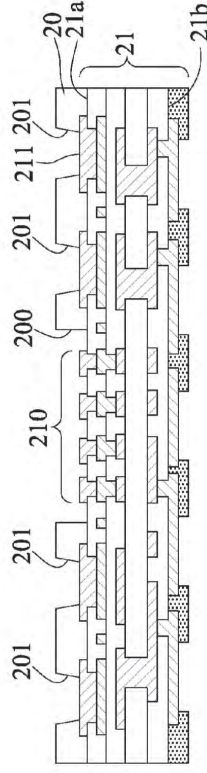


FIG.2B

Chen ’484, FIG. 2B

	<p>“Referring to FIG. 2C, a circuit layer 23 is formed on the dielectric layer 20 and a plurality of conductive members 230 are formed in the openings 201 of the dielectric layer 20. As such, the dielectric layer 20, the circuit layer 23 and the conductive members 230 together form a build-up layer 28. The conductive members 230 electrically connect the circuit layer 23 to the second bonding pads 211 and the circuits 213 of the first substrate 21. In the present embodiment, an insulating layer 24, such as a solder mask layer, is formed on the dielectric layer 20 and the circuit layer 23, and a plurality of openings 240 are formed in the insulating layer 24 for exposing the conductive members 230. Further, the conductive members 230 are made of a metal material, such as copper, and the conductive members 230 are of a pillar shape.” Chen ’484, [0043-0045].</p> <div></div> <p style="text-align: center;">FIG.2C</p> <p>Chen ’484, FIG. 2C</p> <p>“Referring to FIG. 2E, a stack member 22 is disposed on the conductive members 230 so as to be stacked on the build-up layer 28 and cover the electronic element 25. In the present</p>
--	--

embodiment, the stack member 22 is a second substrate, such as a circuit board. The stack member 22 is bonded to the conductive members 230 through a plurality of conductive elements 27. For example, a plurality of conductive elements 27 made of such as a solder material are formed on a lower surface 22 b of the stack member 22 and electrically connected to the conductive members 230 so as to stack the stack member 22 on the build-up layer 28. Alternatively, a plurality of conductive elements 27 each consisting of a metal pillar 270 (such as a copper pillar) and a solder material 271 formed on the metal pillar 270 can be formed between the conductive members 230 and the stack member 22 so as to stack the stack member 22 on the build-up layer 28.” Chen ’484, [0050-0051].

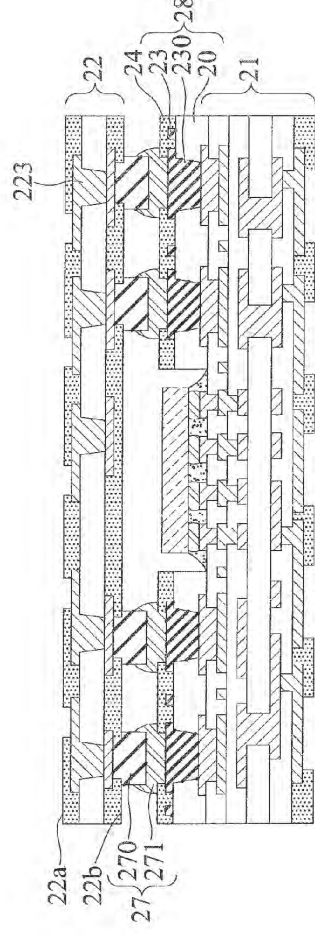


FIG. 2E

Chen '484, FIG. 2E

“The present invention further provides a package structure 2, 3, 4, which has: a first substrate 21; a build-up layer 28, 48 formed on and electrically connected to the first substrate 21; an

	<p>electronic element 25 disposed on and electrically connected to the first substrate 21 ; a stack member 22, 32 stacked on the build-up layer 28, 48 so as to be stacked on the first substrate 21 ; and an encapsulant 26, 26 ' formed between the build-up layer 28, 48 (or the insulating layer 24) and the stack member 22, 32. The first substrate 21 is a circuit board, which has opposite first and second surfaces 21 a, 21 b. The build-up layer 28, 48 has a cavity 200 exposing a portion of the first surface 21 a of the first substrate 21. In the present embodiment, the build-up layer 28, 48 has: at least a dielectric layer 20 formed on the first substrate 21, a circuit layer 23 formed on the dielectric layer 20, and a plurality of conductive members 230 formed in and exposed from the dielectric layer 20. In particular, the cavity 200 penetrates the dielectric layer 20. The dielectric layer 20 further has a plurality of openings 201. The dielectric layer 20 can be made of prepreg. The conductive members 230, 230 ' are formed in the openings 201 of the dielectric layer 20 for electrically connecting the circuit layer 23 and the first substrate 21. The conductive members 230, 230 ' are made of metal and of a pillar shape or a groove shape. The package structure 2, 3, 4 can further have an insulating layer 24 formed on the build-up layer 28, 48 and exposing the conductive members 230, 230 '. The electronic element 25 is an active component or a passive component. The electronic element 25 is disposed on the first surface 21 a of the first substrate 21 in the cavity 200. The stack member 22, 32 is disposed on the build-up layer 28, 48. In particular, the stack member 22, 32 is bonded to the conductive members 230, 230 ' through a plurality of conductive elements 27 so as to be stacked on the first substrate 21." Chen '484, [0059-0064].</p> <p>To the extent Plaintiff contends that Chen '484 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

U.S. Patent No.9401320 (“Daizo”) is titled Combined Substrate and lists Tomoya Daizo, Takema Adachi, Takeshi Furusawa, Wataru Nakamura, Yuki Ito, Yuki Yoshikawa, and Tomoyoshi Hirabayashi as inventors. Daizo is assigned to Ilden Co., Ltd. Daizo anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Daizo is a U.S. patent that was filed March 4, 2015 and published September 10, 2015. Daizo claims priority to JP 2014-044520 filed on March 7, 2014. Daizo is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(2).

The chart below provides representative examples of where each element of each Asserted Claim is found within Daizo, or otherwise rendered obvious by disclosures and teachings of Daizo, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Daizo does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Daizo with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Daizo, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

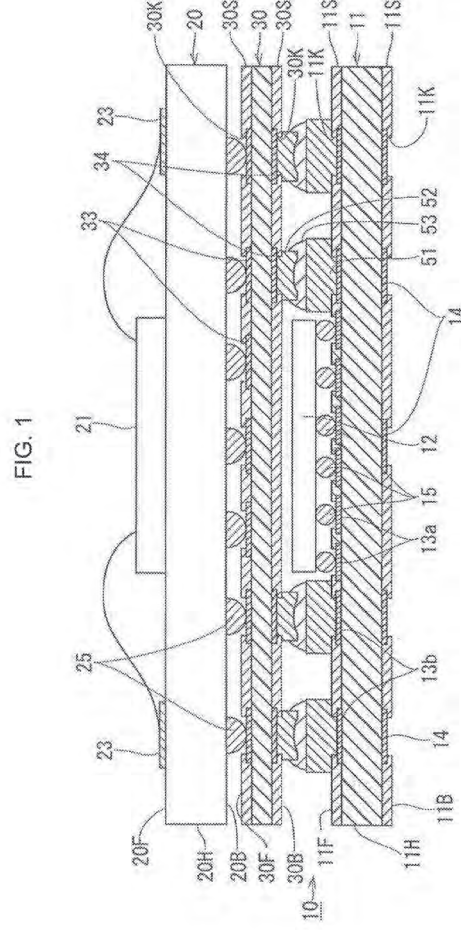
makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Daizo “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Daizo or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Daizo set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Daizo discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“According to one aspect of the present invention, a combined substrate includes a first substrate having multiple first metal posts, a second substrate having multiple second metal posts such that the second metal posts are positioned to oppose the first metal posts, respectively, and multiple solder structures interposed between the first metal posts and the second metal posts, respectively.” Daizo, [1:26-1:32].</p>



Daizo, FIG. 1

“A combined substrate 10 of the present embodiment is formed by superposing a second substrate 30 on a first substrate 11. A so-called PoP structure (package-on-package structure) in which a third substrate 20 is superposed on the combined substrate 10 is illustrated in FIG. 2. Daizo, [2:3-2:8].

“The first substrate 11 is, for example, a CPU substrate in which a CPU 12 is mounted on a substrate body (11 H). The substrate body (11 H) forms a multilayer structure with a built-in circuit (not illustrated in the drawings).” Daizo, [2:11-2:14].

“The third substrate 20 is, for example, a memory substrate in which a memory chip 21 is mounted on a substrate body (20 H). The substrate body (20 H), for example, has a planar

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>shape that is substantially the same as the substrate body (11 H) of the first substrate 11.” Daizo, [2:44-2:48].</p> <p>“The second substrate 30, for example, has a planar shape that is substantially the same as the substrate bodies (11 H, 20 H) of the first substrate 11 and the third substrate 20. Similar to the above-described substrate bodies (11 H, 20 H), the second substrate 30 also forms a multilayer structure with a built-in circuit (not illustrated in the drawings).” Daizo, [2:59-2:64].</p> <p>“In a combined substrate which has metal posts protruding from one substrate and soldered to solder bumps of another substrate, there is a conceivable problem that an internal stress occurs between the metal posts and the solder bumps due to thermal deformation of the substrates and thus reliability of electrical connection between the substrates decreases.” Daizo, [5:64-6:2].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.A] a bottom package substrate;	<p>Daizo discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“A combined substrate 10 of the present embodiment is formed by superposing a second substrate 30 on a first substrate 11. A so-called PoP structure (package-on-package structure) in which a third substrate 20 is superposed on the combined substrate 10 is illustrated in FIG.</p>

	<p>1. In the PoP structure, the second substrate 30 becomes an interposer for connecting the third substrate 20 to the first substrate 11.” Daizo, [2:3-2:10].</p> <p>“The first substrate 11 is, for example, a CPU substrate in which a CPU 12 is mounted on a substrate body (11 H). The substrate body (11 H) forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (11 F), which is a mounting surface, and a B surface (11 B), which is a back surface of the substrate body (11 H), are covered by solder resist layers (11 S, 11 S). Further, for example, multiple circular pad openings (11 K) are formed in the front and back solder resist layers (11 S, 11 S).” Daizo, [2:11-2:19].</p> <p style="text-align: center;">FIG. 1</p> <p style="text-align: right;">Daizo, FIG. 1</p>
--	--

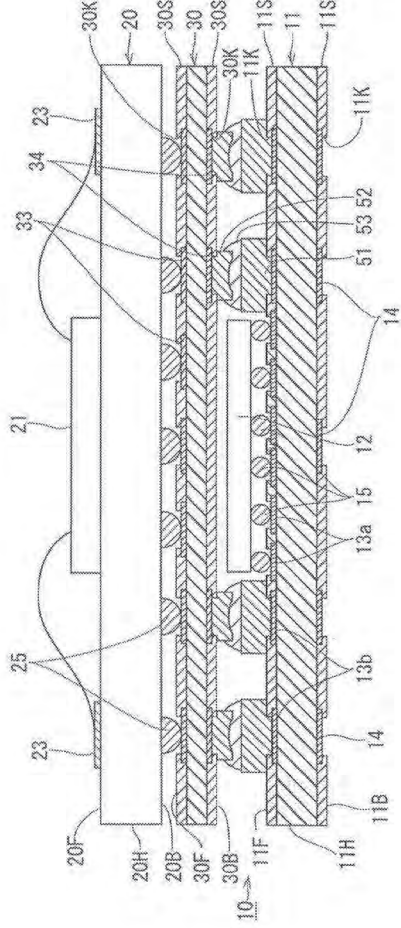
Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>“Further, the group of the pads 14 of the B surface (11 B) of the substrate body (11 H) is bump-connected to another substrate (not illustrated in the drawings).” Daizo, [2:40-2:42].</p> <p>“In order to manufacture the combined substrate 10, the third substrate 20 is prepared in advance in which the memory chip 21 is mounted on the F surface (20 F) of the substrate body (20 H) that is provided with the solder bumps 25. Further, the first substrate 11 is manufactured in which the CPU 12 is mounted on the F surface (11 F) of the substrate body (11 H).” Daizo, [4:17-4:23].</p> <p>“Next, the first substrate 11 and the second substrate 30 are heated at a temperature lower than the melting point of the solder balls 15 of the CPU 12 to reflow the solders 53 and to crush the solders 53 between the front-end surfaces (51 B, 52 B) of the first and second metal posts (51, 52). Then, the solders 53 are solidified to formed a combined body in which the second substrate 30 is fixed on the first substrate 11.” Daizo, [4:29-4:36].</p> <p>“In addition, as described above, the first substrate 11 is thicker than the second substrate 30 and thus is unlikely to thermally deform. In the present embodiment, as described above, the first metal post 51 of the first substrate 11 that is unlikely to thermally deform is formed longer.” Daizo, [5:3-5:8].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Daizo discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p>

See, e.g.:

“A combined substrate 10 of the present embodiment is formed by superposing a second substrate 30 on a first substrate 11. A so-called PoP structure (package-on-package structure) in which a third substrate 20 is superposed on the combined substrate 10 is illustrated in FIG. 1. In the PoP structure, the second substrate 30 becomes an interposer for connecting the third substrate 20 to the first substrate 11.” Daizo, [2:3-2:11].

FIG. 1

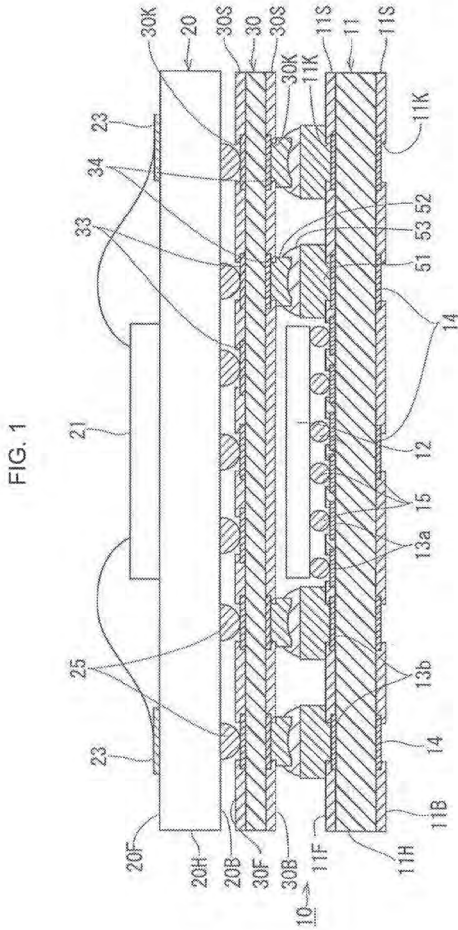


Daizo, FIG. 1

“The solder bumps 25 of the third substrate 20 are soldered to the group of the pads 33 of the F surface (30 F) of the second substrate 30.” Daizo, [3:10-3:12].

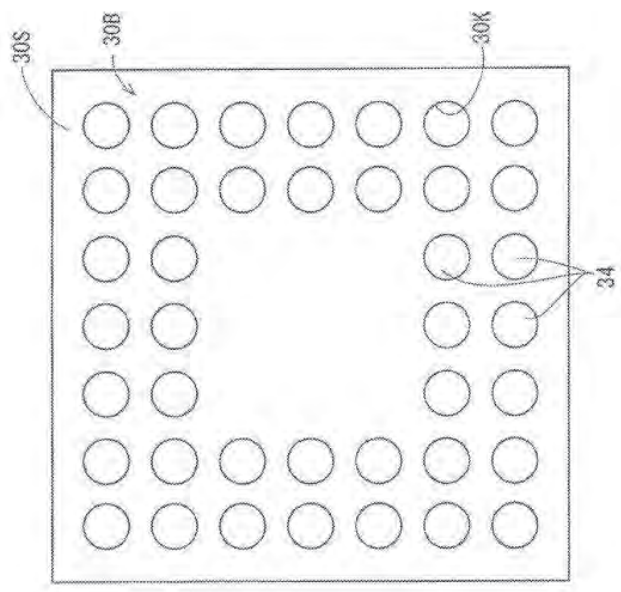
Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>“Then, the second substrate 30 is mounted on the first substrate 11.” Daizo, [4:23-4:24].</p> <p>“Next, the first substrate 11 and the second substrate 30 are heated at a temperature lower than the melting point of the solder balls 15 of the CPU 12 to reflow the solders 53 and to crush the solders 53 between the front-end surfaces (51 B, 52 B) of the first and second metal posts (51, 52). Then, the solders 53 are solidified to formed a combined body in which the second substrate 30 is fixed on the first substrate 11.” Daizo, [4:29-4:36].</p> <p>“Thereafter, the third substrate 20 is superposed on the second substrate 30 of the combined body and is heated at a temperature lower than the melting point of the solders 53 to reflow the solder bumps 25 of the third substrate 20 and thereby solder the third substrate 20 to the second substrate 30.” Daizo, [4:36-4:41].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Daizo discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In the PoP structure, the second substrate 30 becomes an interposer for connecting the third substrate 20 to the first substrate 11.” Daizo, [2:8-2:10].</p>



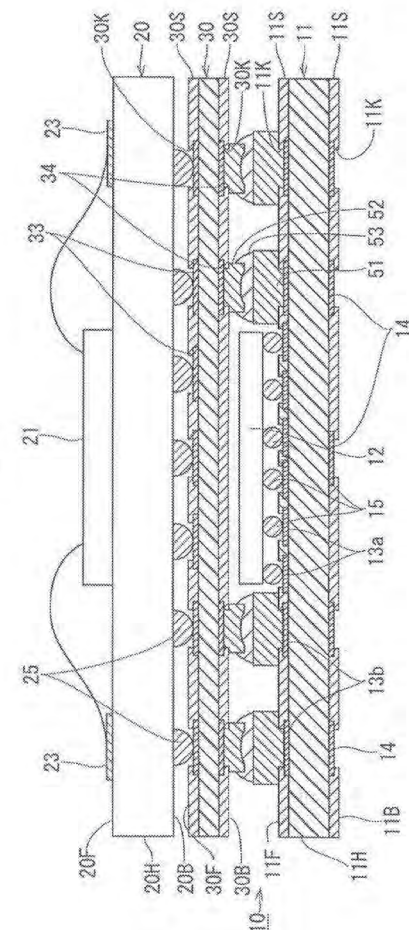
Daizo, FIG. 1

“The second substrate 30, for example, has a planar shape that is substantially the same as the substrate bodies (11 H, 20 H) of the first substrate 11 and the third substrate 20. Similar to the above-described substrate bodies (11 H, 20 H), the second substrate 30 also forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (30 F) and a B surface (30 B) are covered by solder resist layers (30 S, 30 S).” Daizo, [2:59-2:66].

	<div><p>30</p></div> <div><p>FIG. 3</p></div> <div></div> <div><p>Daizo, FIG. 3</p></div> <div><p>“Further, as compared to the substrate bodies (11 H, 20 H) in which the CPU 12 or the memory chip 21 is mounted, in the second substrate 30, strength required is low and a circuit structure is also simple. Therefore, the second substrate 30 is thinner than the first substrate 11 and the third substrate 20.” Daizo, [3:5-3:9].</p></div>
--	---

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>“The solder bumps 25 of the third substrate 20 are soldered to the group of the pads 33 of the F surface (30 F) of the second substrate 30. On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group of the pads 34 of the B surface (30 B) of the second substrate 30.” Daizo, [3:10-3:15].</p> <p>“Thereafter, the third substrate 20 is superposed on the second substrate 30 of the combined body and is heated at a temperature lower than the melting point of the solders 53 to reflow the solder bumps 25 of the third substrate 20 and thereby solder the third substrate 20 to the second substrate 30.” Daizo, [4:36-4:41].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Daizo discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the following, a first embodiment of the present invention is described based on FIG. 1-5. A combined substrate 10 of the present embodiment is formed by superposing a second substrate 30 on a first substrate 11. A so-called PoP structure (package-on-package structure) in which a third substrate 20 is superposed on the combined substrate 10 is illustrated in FIG. 1.” Daizo, [2:2-2:8].</p> <p>“The second substrate 30, for example, has a planar shape that is substantially the same as the substrate bodies (11 H, 20 H) of the first substrate 11 and the third substrate 20. Similar</p>

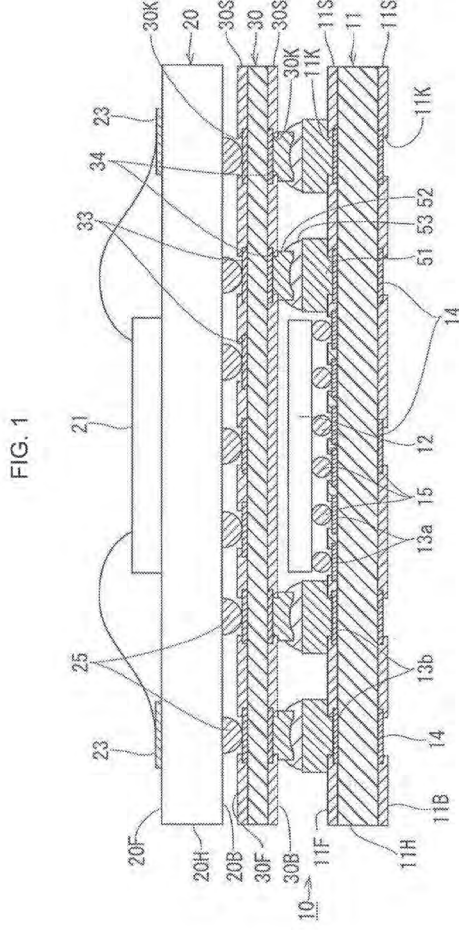
	<p>to the above-described substrate bodies (11 H, 20 H), the second substrate 30 also forms a multilayer structure with a built-in circuit (not illustrated in the drawings).” Daizo, [2:59-2:64].</p> <p style="text-align: center;">FIG. 1</p>  <p style="text-align: center;">Daizo, FIG. 1</p> <p>“Further, as compared to the substrate bodies (11 H, 20 H) in which the CPU 12 or the memory chip 21 is mounted, in the second substrate 30, strength required is low and a circuit structure is also simple. Therefore, the second substrate 30 is thinner than the first substrate 11 and the third substrate 20.” Daizo, [3:5-3:9].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	--

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>plan view of the B surface (30B) of the second substrate 30 is illustrated in FIG. 3. The group of the pads 34 is arranged opposing the group of the pads (13 b) arranged on the F surface (11F) of the first substrate 11 illustrated in FIG. 2.” Daizo, [2:62-3:5].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Daizo discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p>See, e.g.:</p> <div style="text-align: center;"> <p>FIG. 1</p> </div>

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>Daizo, FIG. 1</p> <p>“Similar to the above-described substrate bodies (11H, 20H), the second substrate 30 also forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (30F) and a B surface (30B) are covered by solder resist layers (30S, 30S). Pads 33, 34 are provided on deep sides of pad openings (30K) of the solder resist layers (30S, 30S). A plan view of the B surface (30B) of the second substrate 30 is illustrated in FIG. 3. The group of the pads 34 is arranged opposing the group of the pads (13 b) arranged on the F surface (11F) of the first substrate 11 illustrated in FIG. 2.” Daizo, [2:62-3:5].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,	<p>Daizo discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

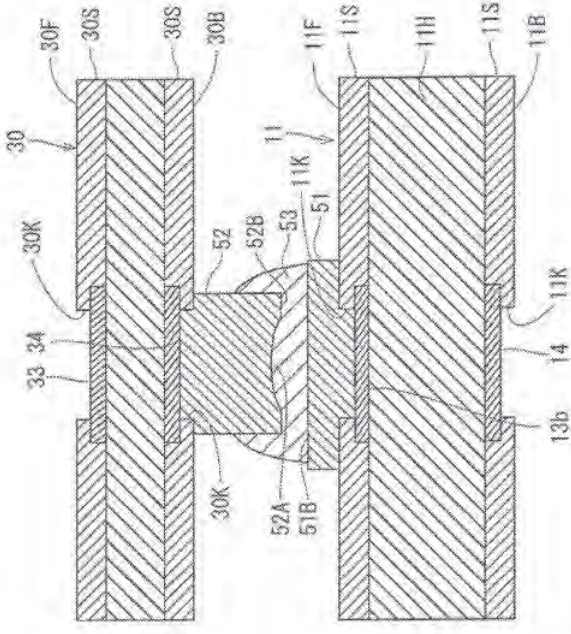


Daizo, FIG. 1

“Similar to the above-described substrate bodies (11H, 20H), the second substrate 30 also forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (30F) and a B surface (30B) are covered by solder resist layers (30S, 30S). Pads 33, 34 are provided on deep sides of pad openings (30K) of the solder resist layers (30S, 30S). A plan view of the B surface (30B) of the second substrate 30 is illustrated in FIG. 3. The group of the pads 34 is arranged opposing the group of the pads (13 b) arranged on the F surface (11F) of the first substrate 11 illustrated in FIG. 2.” Daizo, [2:62-3:5].

“The solder bumps 25 of the third substrate 20 are soldered to the group of the pads 33 of the F surface (30F) of the second substrate 30. On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

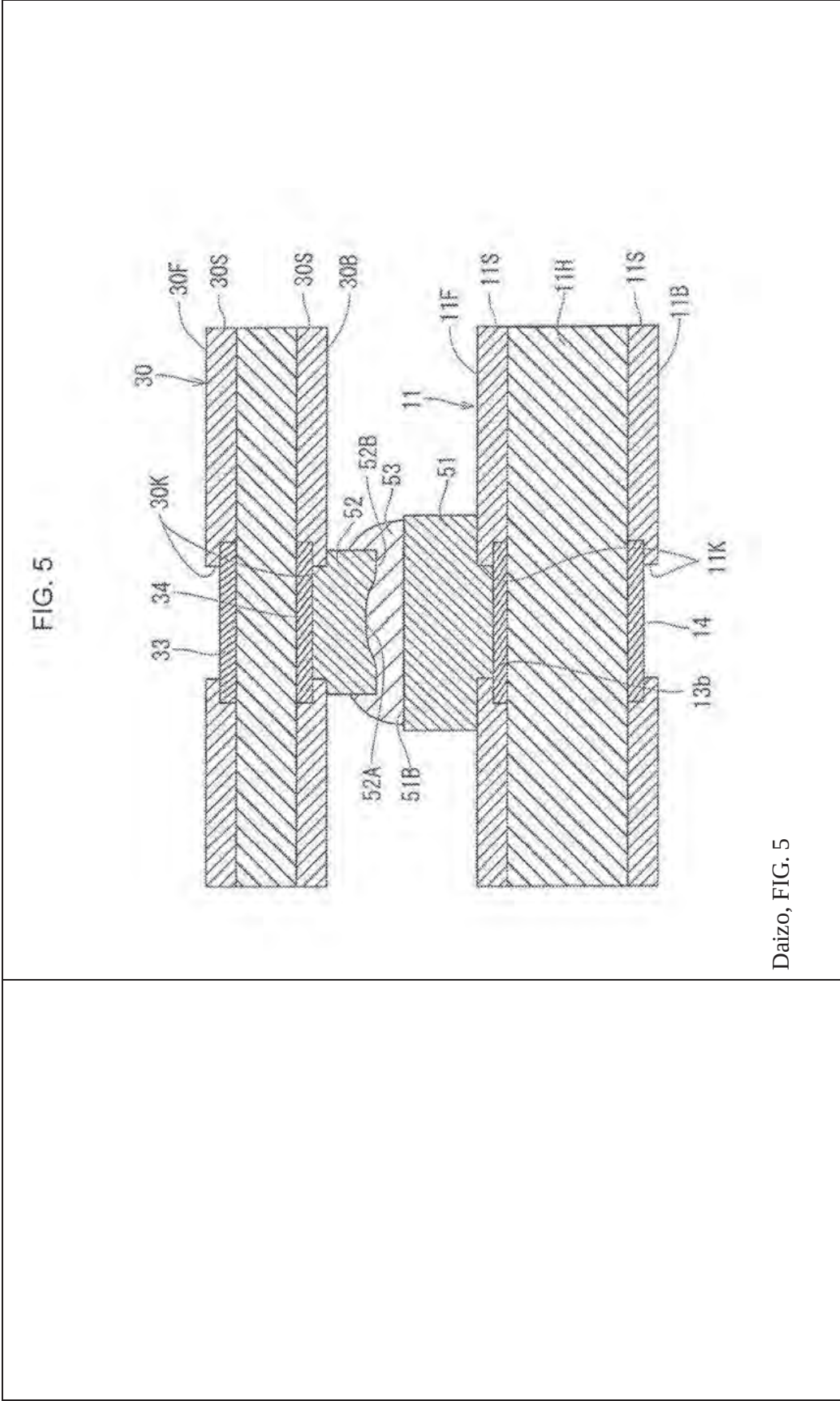
	<p>of the pads 34 of the B surface (30B) of the second substrate 30. The group of the second metal posts 52 and the group of the first metal posts 51 are fixed by solders 53 in a state in which the second metal posts 52 and the first metal posts 51 respectively butt against each other.” Daizo, [3:10-3:19].</p> <p style="text-align: center;">FIG. 6</p>  <p style="text-align: right;">Daizo, FIG. 6</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	---

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Daizo discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <div> </div> <p>FIG. 1</p> <p>Daizo, FIG. 1</p> <p>“On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group of the pads 34 of the B surface (30B) of the</p>

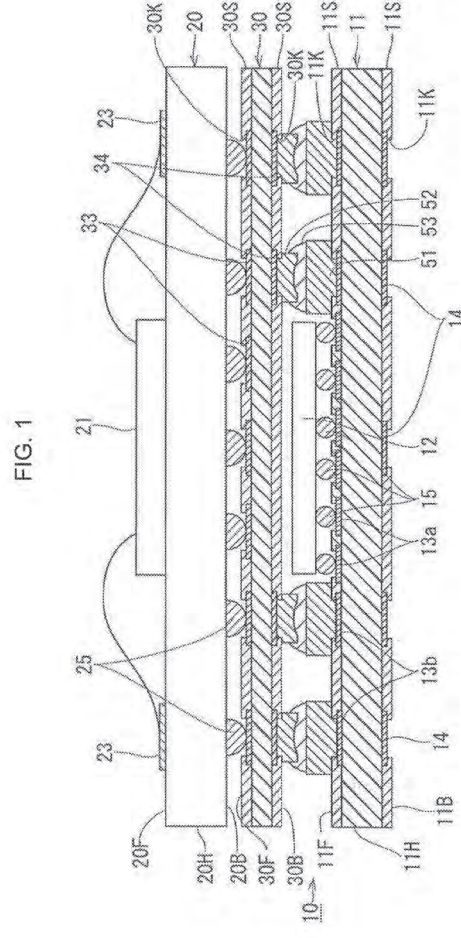
Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	second substrate 30. The group of the second metal posts 52 and the group of the first metal posts 51 are fixed by solders 53 in a state in which the second metal posts 52 and the first metal posts 51 respectively butt against each other.” Daizo, [3:12-3:19].
--	---



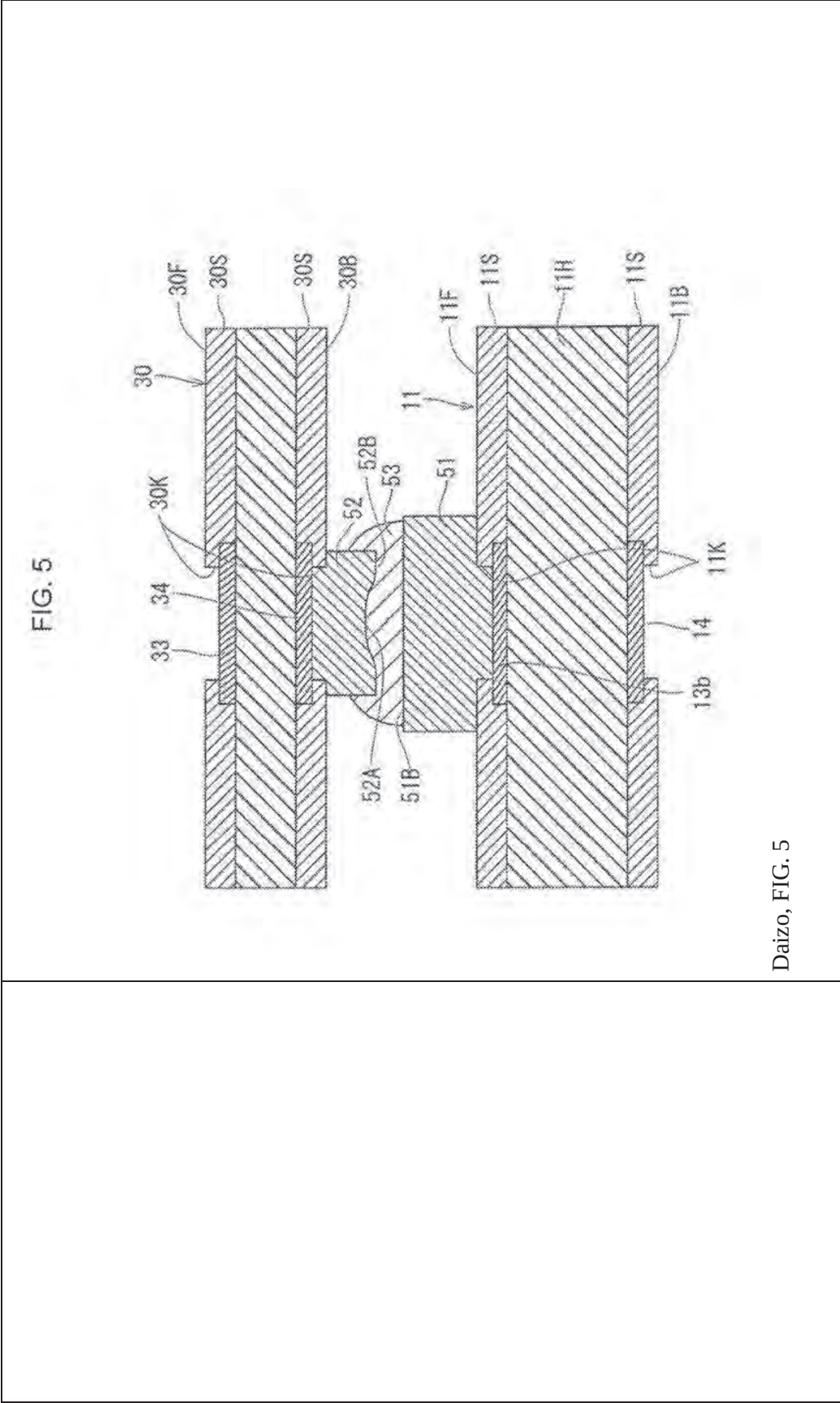
Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>“The first and second metal posts (51, 52) are formed, for example, by subjecting the substrate body (11H) of the first substrate 11 and the second substrate 30 to copper plating processing. Specifically, the substrate body (11H) is covered by an insulating film (not illustrated in the drawings). A circular hole is formed in a part of the insulating film to expose the pad (13 b) of the substrate body (11H). In this state, the substrate body (11H) is subjected to copper plating processing and thereby the first metal post 51 is formed. As illustrated in FIG. 5, for example, the first metal post 51 forms a columnar shape having an outer diameter larger than that of the circular opening (11K) for the pad (13 b) in the solder resist layer (11S), and is in close contact with an opening edge and an inner surface of the pad opening (11K) and the pad (13 b) in the pad opening (11K). The second metal post 52 is also similarly formed by plating processing, forms a columnar shape having an outer diameter larger than that of the pad opening (30K) of the solder resist layer (30S), and is in close contact with an opening edge and an inner surface of the pad opening (30K) and the pad 34.” Daizo, [3:20-3:39].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Daizo discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p>



Daizo, FIG. 1

“On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group of the pads 34 of the B surface (30B) of the second substrate 30. The group of the second metal posts 52 and the group of the first metal posts 51 are fixed by solders 53 in a state in which the second metal posts 52 and the first metal posts 51 respectively butt against each other.” Daizo, [3:12-3:19].



Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

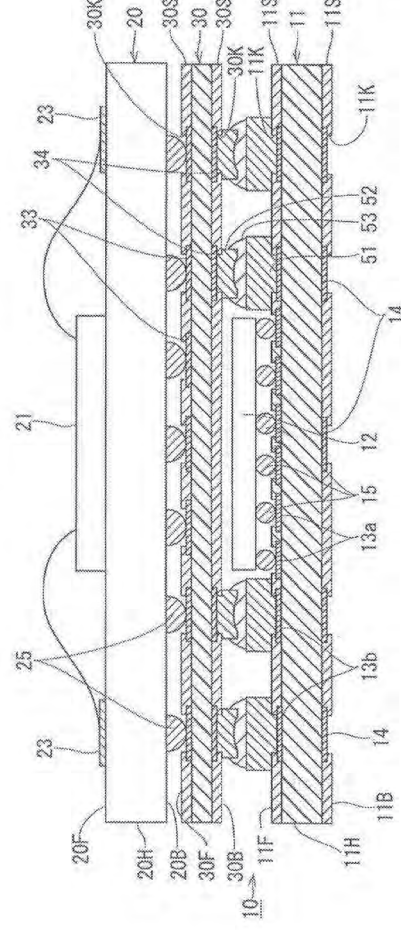
	<p>“The first and second metal posts (51, 52) are formed, for example, by subjecting the substrate body (11H) of the first substrate 11 and the second substrate 30 to copper plating processing. Specifically, the substrate body (11H) is covered by an insulating film (not illustrated in the drawings). A circular hole is formed in a part of the insulating film to expose the pad (13 b) of the substrate body (11H). In this state, the substrate body (11H) is subjected to copper plating processing and thereby the first metal post 51 is formed. As illustrated in FIG. 5, for example, the first metal post 51 forms a columnar shape having an outer diameter larger than that of the circular opening (11K) for the pad (13 b) in the solder resist layer (11S), and is in close contact with an opening edge and an inner surface of the pad opening (11K) and the pad (13 b) in the pad opening (11K). The second metal post 52 is also similarly formed by plating processing, forms a columnar shape having an outer diameter larger than that of the pad opening (30K) of the solder resist layer (30S), and is in close contact with an opening edge and an inner surface of the pad opening (30K) and the pad 34.” Daizo, [3:20-3:39].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p>	<p>Daizo discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p>

top metal pillars of the bottom package substrate; and	
[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein	<p>Daizo, FIG. 1</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Daizo discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p>

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>“A combined substrate 10 of the present embodiment is formed by superposing a second substrate 30 on a first substrate 11. A so-called PoP structure (package-on-package structure) in which a third substrate 20 is superposed on the combined substrate 10 is illustrated in FIG. 1. In the PoP structure, the second substrate 30 becomes an interposer for connecting the third substrate 20 to the first substrate 11. The first substrate 11 is, for example, a CPU substrate in which a CPU 12 is mounted on a substrate body (11 H).” Daizo, [2:3-2:12].</p> <p>“The above-described CPU 12 is bump-connected (this is also referred to as a “flip-chip connection”) to the group of the pads (13 a) by solder balls 15, and first metal posts 51 (to be described in detail later) protrude from the group of the pads (13 b). The substrate body (11 H) may be a multilayer substrate having a core substrate, for example, as described in Japanese Patent Laid-Open Publication No. 2007-227512, or may be a so-called coreless substrate that does not have a core substrate as described in Japanese Patent Laid-Open Publication No. 2005-236244. The entire contents of Japanese Patent Laid-Open Publication No. 2007-227512 are incorporated herein by reference. Further, the group of the pads 14 of the B surface (11 B) of the substrate body (11 H) is bump-connected to another substrate (not illustrated in the drawings). The third substrate 20 is, for example, a memory substrate in which a memory chip 21 is mounted on a substrate body (20 H). The substrate body (20 H), for example, has a planar shape that is substantially the same as the substrate body (11 H) of the first substrate 11.” Daizo, [2:29-2:49].</p>
--	---

FIG. 1



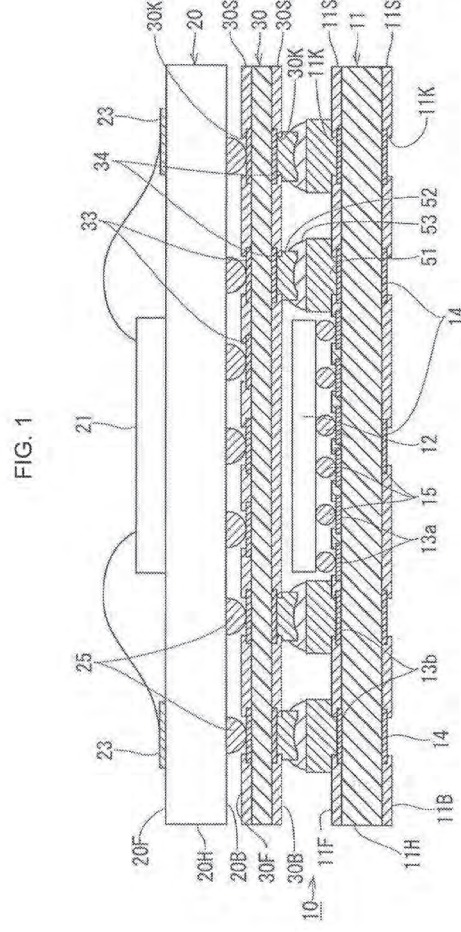
Daizo, FIG. 1

“The above-described memory chip 21 is fixed at a center of the F surface (20 F) and is wire-bonded to a group of pads 23 surrounding the memory chip 21. Further, solder bumps 25 connected to a group of pads (not illustrated in the drawings) are provided on substantially the entire B surface (20 B) of the substrate body (20 H). The second substrate 30, for example, has a planar shape that is substantially the same as the substrate bodies (11 H, 20 H) of the first substrate 11 and the third substrate 20.” Daizo, [2:53-2:61].

“The solder bumps 25 of the third substrate 20 are soldered to the group of the pads 33 of the F surface (30 F) of the second substrate 30. On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group of the pads 34 of the B surface (30 B) of the second substrate 30. The group of the second

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>metal posts 52 and the group of the first metal posts 51 are fixed by solders 53 in a state in which the second metal posts 52 and the first metal posts 51 respectively butt against each other.” Daizo, [3:10-3:19].</p> <p>“It is also possible that, after the first substrate 11 and the second substrate 30 are connected, the third substrate 20 is mounted after mold resin is poured in to fix the CPU 12 and the substrate.” Daizo, [4:42-4:45].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Daizo discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The first substrate 11 is, for example, a CPU substrate in which a CPU 12 is mounted on a substrate body (11 H). The substrate body (11 H) forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (11 F), which is a mounting surface, and a B surface (11 B), which is a back surface of the substrate body (11 H), are covered by solder resist layers (11 S, 11 S).” Daizo, [2:11-2:17].</p>



Daizo, FIG. 1

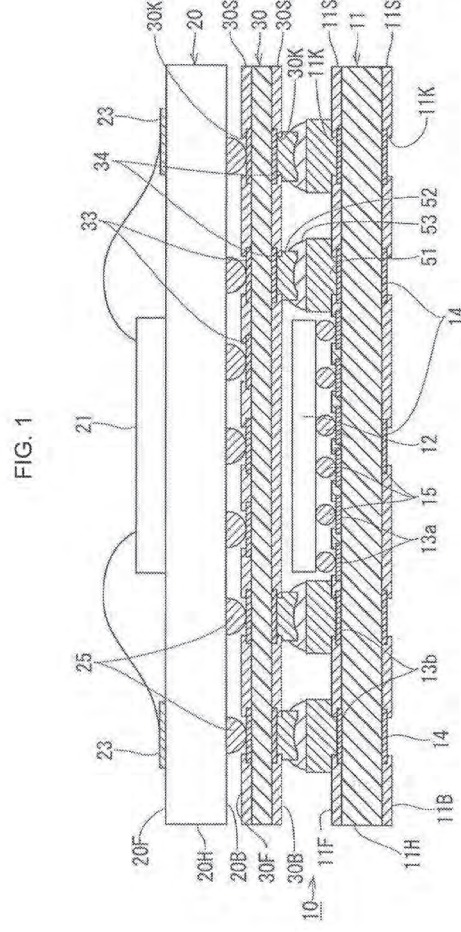
“A plan view of the F surface (11 F) of the first substrate 11 is illustrated in FIG. 2. A group of the pads (13 a) for connecting to the above-described CPU 12 is arranged in a matrix shape in a central portion of the F surface (11 F).” Daizo, [2:22-2:26].

“The above-described CPU 12 is bump-connected (this is also referred to as a “flip-chip connection”) to the group of the pads (13 a) by solder balls 15, and first metal posts 51 (to be described in detail later) protrude from the group of the pads (13 b).” Daizo, [2:29-2:33].

“The third substrate 20 is, for example, a memory substrate in which a memory chip 21 is mounted on a substrate body (20 H). The substrate body (20 H), for example, has a planar

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>shape that is substantially the same as the substrate body (11 H) of the first substrate 11.” Daizo, [2:44-2:48].</p> <p>“The above-described memory chip 21 is fixed at a center of the F surface (20 F) and is wire-bonded to a group of pads 23 surrounding the memory chip 21.” Daizo, [2:53-2:56].</p> <p>“In order to manufacture the combined substrate 10, the third substrate 20 is prepared in advance in which the memory chip 21 is mounted on the F surface (20 F) of the substrate body (20 H) that is provided with the solder bumps 25. Further, the first substrate 11 is manufactured in which the CPU 12 is mounted on the F surface (11 F) of the substrate body (11 H).” Daizo, [4:17-4:23].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Daizo discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“In the PoP structure, the second substrate 30 becomes an interposer for connecting the third substrate 20 to the first substrate 11.” Daizo, [2:8-2:10].</p>



Daizo, FIG. 1

“The second substrate 30, for example, has a planar shape that is substantially the same as the substrate bodies (11H, 20H) of the first substrate 11 and the third substrate 20. Similar to the above-described substrate bodies (11H, 20H), the second substrate 30 also forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (30F) and a B surface (30B) are covered by solder resist layers (30S, 30S). Pads 33, 34 are provided on deep sides of pad openings (30K) of the solder resist layers (30S, 30S). A plan view of the B surface (30B) of the second substrate 30 is illustrated in FIG. 3. The group of the pads 34 is arranged opposing the group of the pads (13 b) arranged on the F surface (11F) of the first substrate 11 illustrated in FIG. 2. Further, as compared to the substrate bodies (11H, 20H) in which the CPU 12 or the memory chip 21 is mounted, in the second substrate 30, strength required is low and a circuit structure is also simple. Therefore, the second substrate

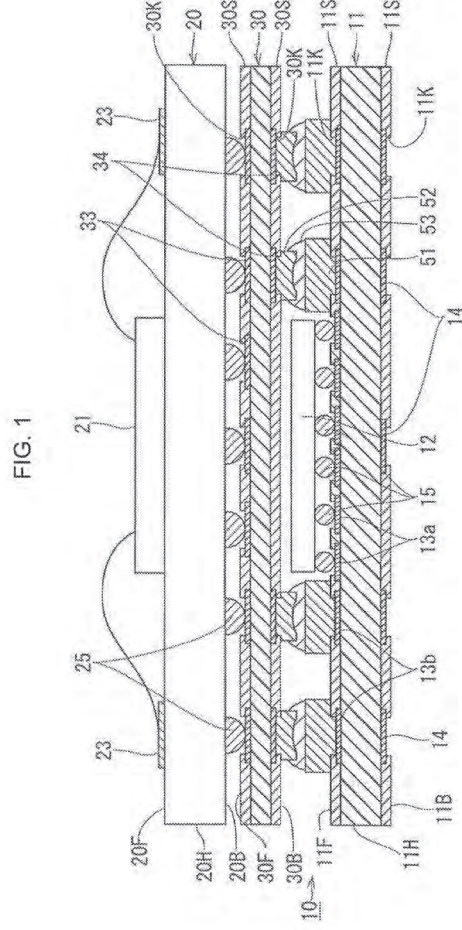
Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>30 is thinner than the first substrate 11 and the third substrate 20. The solder bumps 25 of the third substrate 20 are soldered to the group of the pads 33 of the F surface (30F) of the second substrate 30. On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group of the pads 34 of the B surface (30B) of the second substrate 30.” Daizo, [2:59-3:15].</p> <p>“Thereafter, the third substrate 20 is superposed on the second substrate 30 of the combined body and is heated at a temperature lower than the melting point of the solders 53 to reflow the solder bumps 25 of the third substrate 20 and thereby solder the third substrate 20 to the second substrate 30.” Daizo, [4:36-4:41].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Daizo discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>

“The first substrate 11 is, for example, a CPU substrate in which a CPU 12 is mounted on a substrate body (11 H). The substrate body (11 H) forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (11 F), which is a mounting surface, and a B surface (11 B), which is a back surface of the substrate body (11 H), are covered by solder resist layers (11 S, 11 S).” Daizo, [2:11-2:17].



Daizo, FIG. 1

“The above-described CPU 12 is bump-connected (this is also referred to as a “flip-chip connection”) to the group of the pads (13 a) by solder balls 15, and first metal posts 51 (to be described in detail later) protrude from the group of the pads (13 b).” Daizo, [2:29-2:33].

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

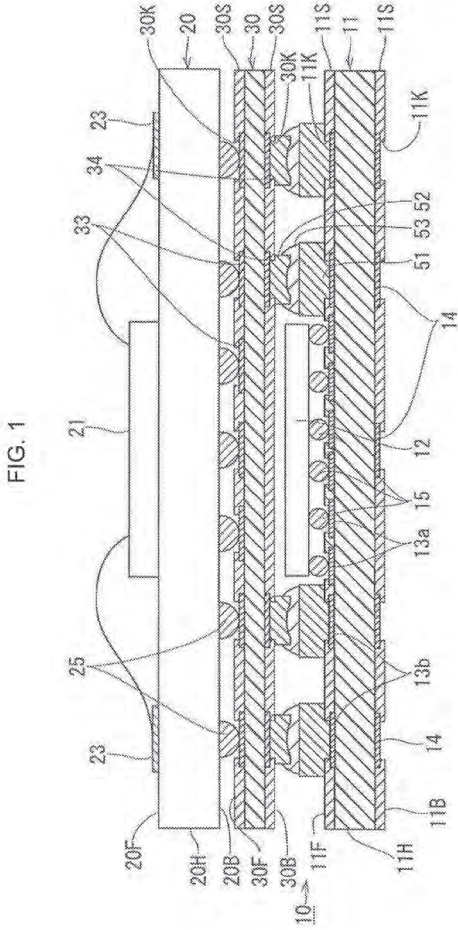
	<p>“The group of the second metal posts 52 and the group of the first metal posts 51 are fixed by solders 53 in a state in which the second metal posts 52 and the first metal posts 51 respectively butt against each other.” Daizo, [3:15-3:19].</p> <p>“The first metal post 51 is thinner and longer than the second metal post 52. Specifically, the first metal post 51 has an outer diameter of 70-170 μm and a total length of 30-160 μm, and the second metal post 52 has an outer diameter of 70-140 μm and a total length of 15-90 μm.” Daizo, [3:40-3:44].</p> <p>“The total length of a metal post means a height from a surface of an uppermost layer (the solder resist layers (11 S, 30 S)) of the substrate to a highest part of the metal post.” Daizo, [3:52-3:55].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Daizo discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

<p>package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p><i>See, e.g.:</i></p> <p>“A so-called PoP structure (package-on-package structure) in which a third substrate 20 is superposed on the combined substrate 10 is illustrated in FIG. 1. In the PoP structure, the second substrate 30 becomes an interposer for connecting the third substrate 20 to the first substrate 11. The first substrate 11 is, for example, a CPU substrate in which a CPU 12 is mounted on a substrate body (11 H).” Daizo, [2:5-2:12].</p> <p>“A plan view of the F surface (11 F) of the first substrate 11 is illustrated in FIG. 2. A group of the pads (13 a) for connecting to the above-described CPU 12 is arranged in a matrix shape in a central portion of the F surface (11 F). A group of the pads (32 b), which are larger than the pads (13 a), is arranged in a matrix shape in a frame-shaped region surrounding the pads (13 a).” Daizo, [2:22-2:29].</p> <p>“Further, the group of the pads 14 of the B surface (11 B) of the substrate body (11 H) is bump-connected to another substrate (not illustrated in the drawings). The third substrate 20 is, for example, a memory substrate in which a memory chip 21 is mounted on a substrate body (20 H). The substrate body (20 H), for example, has a planar shape that is substantially the same as the substrate body (11 H) of the first substrate 11. Further, although not illustrated in the drawings, the substrate body (20 H) also forms a multilayer structure with a built-in circuit, similar to the substrate body (11 H) of the first substrate 11. Multiple pads that are connected to the internal circuit are provided on an F surface (20 F) and a B surface (20 B).” Daizo, [2:40-2:53].</p>
--	---



Daizo, FIG. 1

“The above-described memory chip 21 is fixed at a center of the F surface (20 F) and is wire-bonded to a group of pads 23 surrounding the memory chip 21. Further, solder bumps 25 connected to a group of pads (not illustrated in the drawings) are provided on substantially the entire B surface (20 B) of the substrate body (20 H).” Daizo, [2:53-2:58].

“A plan view of the B surface (30 B) of the second substrate 30 is illustrated in FIG. 3. The group of the pads 34 is arranged opposing the group of the pads (13 b) arranged on the F surface (11 F) of the first substrate 11 illustrated in FIG. 2.” Daizo, [3:1-3:5].

“Therefore, the second substrate 30 is thinner than the first substrate 11 and the third substrate 20. The solder bumps 25 of the third substrate 20 are soldered to the group of the pads 33 of

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

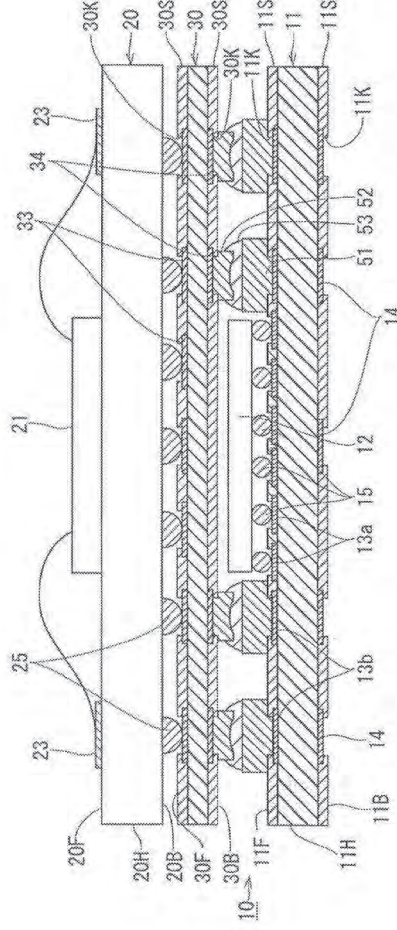
	<p>the F surface (30 F) of the second substrate 30. On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group of the pads 34 of the B surface (30 B) of the second substrate 30.” Daizo, [3:8-3:15].</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>Daizo discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The group of the pads 34 is arranged opposing the group of the pads (13 b) arranged on the F surface (11 F) of the first substrate 11 illustrated in FIG. 2.” Daizo, [3:2-3:5].</p> <p>“On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group of the pads 34 of the B surface (30 B) of the second substrate 30.” Daizo, [3:12-3:15].</p>

“The group of the second metal posts 52 and the group of the first metal posts 51 are fixed by solders 53 in a state in which the second metal posts 52 and the first metal posts 51 respectively butt against each other.” Daizo, [3:15-3:19].

FIG. 1



Daizo, FIG. 1

“Specifically, the second substrate 30 is superposed on the F surface (11 F) of the first substrate 11, and the solders 53 of the group of the second metal posts 52 and the front-end surfaces (51 B) of the group of the first metal posts 51 are put in a state of being in contact with each other.” Daizo, [4:25-4:29].

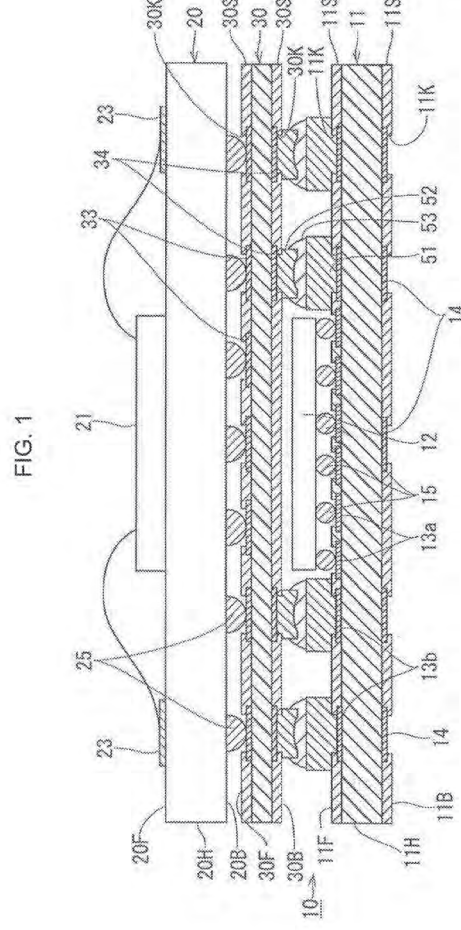
Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>“Next, the first substrate 11 and the second substrate 30 are heated at a temperature lower than the melting point of the solder balls 15 of the CPU 12 to reflow the solders 53 and to crush the solders 53 between the front-end surfaces (51 B, 52 B) of the first and second metal posts (51, 52).” Daizo, [4:29-4:34].</p> <p>“Further, the outer diameter of the first metal post 51 is larger than the outer diameter of the second metal post 52. Therefore, positional displacement of the front-end surface (52 B) of the second metal post 52 can be allowed within the front-end surface (51 B) of the first metal post 51.” Daizo, [4:64-5:1].</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Daizo discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

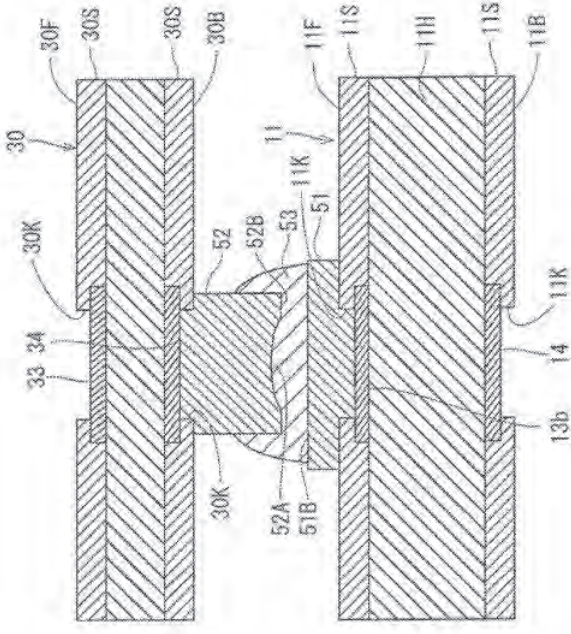
spacer connector via the corresponding top metal pads of the spacer connector.



Daizo, FIG. 1

“Similar to the above-described substrate bodies (11H, 20H), the second substrate 30 also forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (30F) and a B surface (30B) are covered by solder resist layers (30S, 30S). Pads 33, 34 are provided on deep sides of pad openings (30K) of the solder resist layers (30S, 30S). A plan view of the B surface (30B) of the second substrate 30 is illustrated in FIG. 3. The group of the pads 34 is arranged opposing the group of the pads (13 b) arranged on the F surface (11F) of the first substrate 11 illustrated in FIG. 2.” Daizo, [2:62-3:5].

“The solder bumps 25 of the third substrate 20 are soldered to the group of the pads 33 of the F surface (30F) of the second substrate 30. On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group

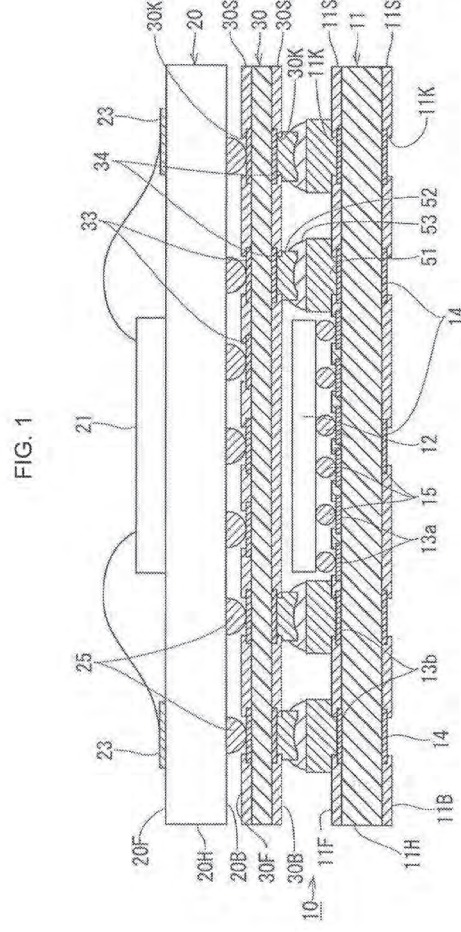
	<p>of the pads 34 of the B surface (30B) of the second substrate 30. The group of the second metal posts 52 and the group of the first metal posts 51 are fixed by solders 53 in a state in which the second metal posts 52 and the first metal posts 51 respectively butt against each other.” Daizo, [3:10-3:19].</p> <p style="text-align: center;">FIG. 6</p>  <p style="text-align: right;">Daizo, FIG. 6</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	---

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the plurality of bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	Daizo discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector. <i>See, e.g.:</i>

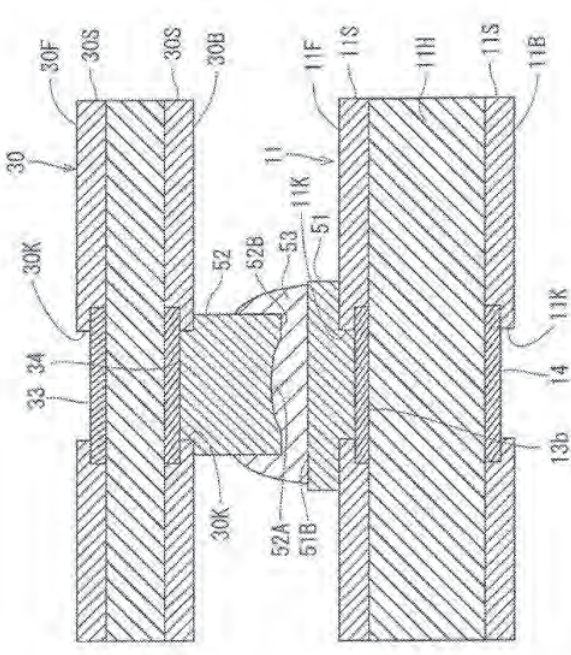


Daizo, FIG. 1

“Similar to the above-described substrate bodies (11H, 20H), the second substrate 30 also forms a multilayer structure with a built-in circuit (not illustrated in the drawings). An F surface (30F) and a B surface (30B) are covered by solder resist layers (30S, 30S). Pads 33, 34 are provided on deep sides of pad openings (30K) of the solder resist layers (30S, 30S). A plan view of the B surface (30B) of the second substrate 30 is illustrated in FIG. 3. The group of the pads 34 is arranged opposing the group of the pads (13 b) arranged on the F surface (11F) of the first substrate 11 illustrated in FIG. 2.” Daizo, [2:62-3:5].

“The solder bumps 25 of the third substrate 20 are soldered to the group of the pads 33 of the F surface (30F) of the second substrate 30. On the other hand, multiple second metal posts 52 corresponding to the first metal posts 51 of the first substrate 11 protrude from the group

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	<p>of the pads 34 of the B surface (30B) of the second substrate 30. The group of the second metal posts 52 and the group of the first metal posts 51 are fixed by solders 53 in a state in which the second metal posts 52 and the first metal posts 51 respectively butt against each other.” Daizo, [3:10-3:19].</p> <p style="text-align: center;">FIG. 6</p>  <p style="text-align: right;">Daizo, FIG. 6</p> <p>To the extent Plaintiff contends that Daizo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	---

Appendix A-5 - Invalidity of U.S. Patent No. 9859202 in view of Daizo - U.S. Patent No. 9401320

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

U.S. Patent No. 8436475 (“Dunne”) is titled IC Device Having Low Resistance TSV Comprising Ground Connection and lists Rajiv Dunne, Gary P. Morrison, Satyendra S. Chauham, Masood Murtuza, Thomas D. Bonifield as inventors. Dunne is assigned to Texas Instruments Incorporated. Dunne anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Dunne is a U.S. patent that was filed April 11, 2012 and published August 2, 2012. Dunne claims priority to a provisional application filed on May 12, 2008. Dunne is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Dunne, or otherwise rendered obvious by disclosures and teachings of Dunne, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Dunne does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Dunne with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Dunne, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Dunne “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Dunne or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Dunne set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Dunne discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 1A, a cross sectional depiction of an IC die 100 is shown comprising a substrate 105 including a top semiconductor comprising surface 106 and a bottom surface 107 on an opposite side of the IC die 100. Although described as an IC die 100, the substrate 105 can comprise a wafer having a plurality of IC die 100. The TSV 110 comprises a first electrically conductive filler material 124 (e.g., Cu or a Cu alloy) having an optional liner 125. TSV 110 includes a protruding integral tip 104 comprising sidewalls 103 that comprises the first electrically conductive filler material 124.” Dunne, [4:12-4:21].</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

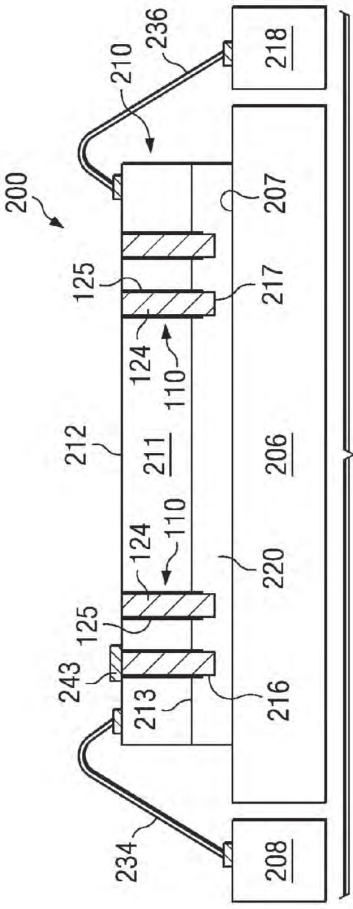
	<p>“Referring again to FIG. 1A, a metal comprising layer 112 is shown on both the bottom surface 107 of the IC die 100 and the sidewalls 103 and the distal end 111 of the tip 104 including over the liner 125. Metal layer 112 is shown comprising a continuous (i.e. blanket) metal layer that extends over an entire area of the bottom surface 107 of the IC die 100. The metal layer 112 comprises a second electrically conductive metal comprising composition that is different from the first electrically conductive filler material 124. In one embodiment, the metal layer 112 can comprise a solder or solder alloy. Generally, a barrier layer (not shown), then a seed layer (not shown) are under the metal layer 112.” Dunne, [6:47-6:58].</p> <p>“Now referring to FIG. 1B, an IC die 150 is shown that further comprises an electrically conductive adhesive layer 163 comprising a third electrically conductive composition on the metal layer 112. Electrically conductive adhesive layer 163 performs a ground enhancement function, by lowering the resistance from TSV 110 to a ground connection proximate to the bottom surface 107 of the IC die 150, such as the die pad of a lead frame (not shown). The third electrically conductive composition is compositionally different from the first electrically conductive filler material 124 and the second electrically conductive composition of the metal layer 112.” Dunne, [7:3-7:14].</p> <p>“Referring now to FIG. 2, a cross sectional depiction of semiconductor device 200 comprising first IC die 210 comprising of substrate (e.g., wafer or die) 211 including active top semiconductor surface 212 and a bottom surface 213, according to an embodiment of the invention, is shown. Device 200 comprises a package substrate with leadframe 205 comprising a die paddle 206, wherein the die paddle 206 has a top metal comprising surface 207. Packaging material, such as plastic encapsulant, is not shown. Bond wires 234 and 236 are shown providing a connection between an I/O or power supply node for integrated circuitry formed on active semiconductor surface 212 to lead fingers 208 and 218. First IC</p>
--	---

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>die 210 is shown mounted face up on the top metal comprising surface 207. A plurality of TSVs 110 comprising a first electrically conductive filler material 124 extends from the top semiconductor comprising surface 212 to protruding integral tips 216 and 217 that extend beyond the bottom surface 213 and provide an electrical contact between die paddle 206 and a ground pad (i.e. connected to ground pins of the IC 210) 243 on the top semiconductor surface 212.” Dunne, [7:46-7:65].</p> <p>“FIG. 3 shows a cross sectional depiction of a semiconductor device 300 that comprises IC die 260 joined to die pad 206 of lead-frame 205, according to another embodiment of the invention. The IC die 260 includes a thin metal layer 221 and an electrically conductive die attach adhesive layer 222 comprising a third electrically conductive composition, such as a solder filled polymer, wherein the solder can be arranged in an electrically interconnected network, positioned between the metal layer 221 and the die pad 206 of the package substrate 205. As shown in FIG. 3, the metal layer 221 capped protruding integral tips 216, 217 extend into the electrically conductive die attach adhesive layer 222 which functions as a ground connection enhancement region.” Dunne, [8:41-8:53].</p> <p>“FIG. 4 shows a cross sectional depiction of a stacked die comprising semiconductor device 400 according to another embodiment of the invention. Stacked die comprising semiconductor device 400 comprises a second IC die 410 flip chip joined to the semiconductor device 300 shown in FIG. 3. Pads 411 of second IC die 410 are bonded to the tops of TSVs 110 by bond pads 243 which can comprise materials such as solder, Au or other suitable bond pad materials. Low resistance ground connections are thus provided to IC 410 via TSVs 110 to die paddle 206 via protruding integral tips 216, 217, backside finish layer 221 and ground connection enhancement region 222. Although not shown, second IC die 410 can also comprise TSVs and thus be stacked face-up on IC die 260, and can include additional TSV comprising die (not shown) stacked thereon.” Dunne, [9:18-9:32].</p>
--	--

<p>[1.A] a bottom package substrate;</p>	<p>Dunne discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The package substrate can comprise a printed circuit board (PCB), BT substrate, lead frame, or tape. The lead frame can be part of generally any wire-bond (WB) package type, such as QFN or QFP, for example.” Dunne, [3:1-3:4].</p> <p>“Referring now to FIG. 2, a cross sectional depiction of semiconductor device 200 comprising first IC die 210 comprising of substrate (e.g., wafer or die) 211 including active</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>top semiconductor surface 212 and a bottom surface 213, according to an embodiment of the invention, is shown. Device 200 comprises a package substrate with leadframe 205 comprising a die paddle 206, wherein the die paddle 206 has a top metal comprising surface 207. Packaging material, such as plastic encapsulant, is not shown. Bond wires 234 and 236 are shown providing a connection between an I/O or power supply node for integrated circuitry formed on active semiconductor surface 212 to lead fingers 208 and 218. First IC die 210 is shown mounted face up on the top metal comprising surface 207.” Dunne, [7:45-7:58].</p>  <p style="text-align: center;">FIG. 2</p> <p>Dunne, FIG. 2</p> <p>“Referring now to FIG. 2, a cross sectional depiction of semiconductor device 200 comprising first IC die 210 comprising of substrate (e.g., wafer or die) 211 including active top semiconductor surface 212 and a bottom surface 213, according to an embodiment of the</p>
--	--

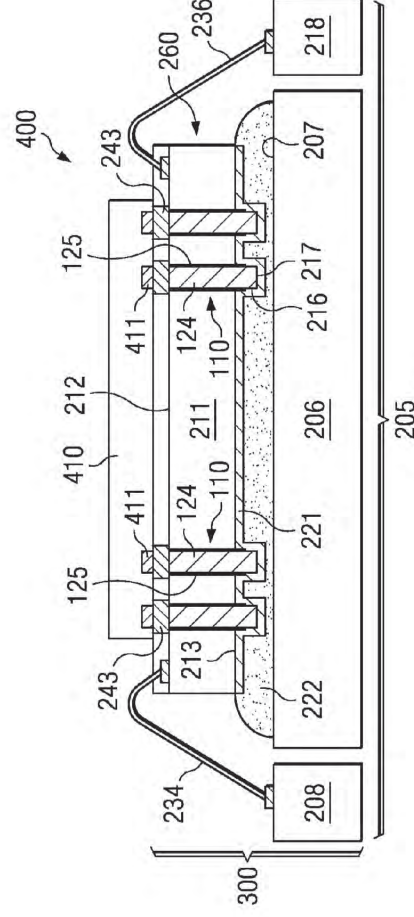
Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>invention, is shown. Device 200 comprises a package substrate with leadframe 205 comprising a die paddle 206, wherein the die paddle 206 has a top metal comprising surface 207.” Dunne, [7:46-7:53].</p> <p>“Device 200 comprises a package substrate with leadframe 205 comprising a die paddle 206, wherein the die paddle 206 has a top metal comprising surface 207. Packaging material, such as plastic encapsulant, is not shown.” Dunne, [7:51-7:54].</p> <p>“FIG. 3 shows a cross sectional depiction of a semiconductor device 300 that comprises IC die 260 joined to die pad 206 of lead-frame 205, according to another embodiment of the invention.” Dunne, [8:41-8:44].</p> <p>“Stacked die comprising semiconductor device 400 comprises a second IC die 410 flip chip joined to the semiconductor device 300 shown in FIG. 3. Pads 411 of second IC die 410 are bonded to the tops of TSVs 110 by bond pads 243 which can comprise materials such as solder, Au or other suitable bond pad materials. Low resistance ground connections are thus provided to IC 410 via TSVs 110 to die paddle 206 via protruding integral tips 216, 217, backside finish layer 221 and ground connection enhancement region 222.” Dunne, [9:21-9:30].</p> <p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	Dunne discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.

See, e.g.:

“Embodiments of the present invention describe IC die comprising a substrate having a semiconductor surface (and wafers having a plurality of such IC die) having at least one, and generally a plurality of TSVs.” Dunne, [2:38-2:41].

“FIG. 4 shows a cross sectional depiction of a stacked die comprising semiconductor device 400 according to another embodiment of the invention. Stacked die comprising semiconductor device 400 comprises a second IC die 410 flip chip joined to the semiconductor device 300 shown in FIG. 3. Pads 411 of second IC die 410 are bonded to the tops of TSVs 110 by bond pads 243 which can comprise materials such as solder, Au or other suitable bond pad materials.” Dunne, [9:18-9:25].

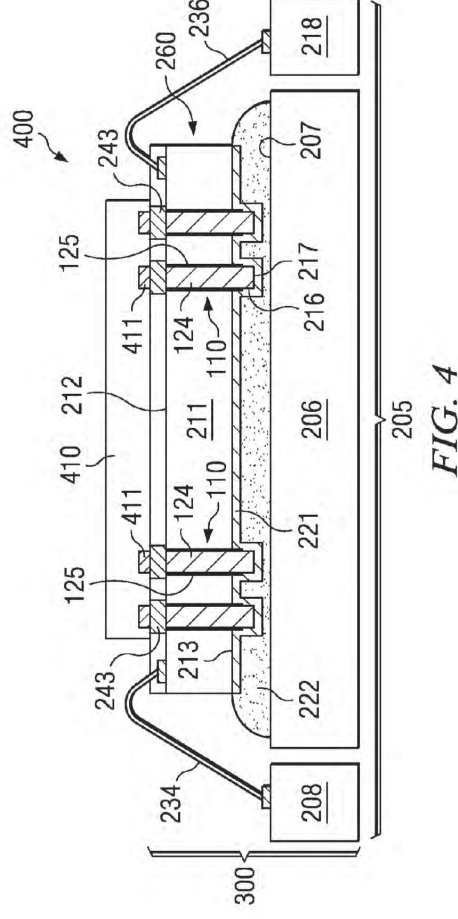


Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>Dunne, FIG. 4</p> <p>“Although not shown, second IC die 410 can also comprise TSVs and thus be stacked face-up on IC die 260, and can include additional TSV comprising die (not shown) stacked thereon.” Dunne, [9:30-9:34].</p> <p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Dunne discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p> <p>“Referring now to FIG. 2, a cross sectional depiction of semiconductor device 200 comprising first IC die 210 comprising of substrate (e.g., wafer or die) 211 including active top semiconductor surface 212 and a bottom surface 213, according to an embodiment of the invention, is shown. Device 200 comprises a package substrate with leadframe 205 comprising a die paddle 206, wherein the die paddle 206 has a top metal comprising surface 207. Packaging material, such as plastic encapsulant, is not shown. Bond wires 234 and 236 are shown providing a connection between an I/O or power supply node for integrated circuitry formed on active semiconductor surface 212 to lead fingers 208 and 218. First IC die 210 is shown mounted face up on the top metal comprising surface 207. A plurality of TSVs 110 comprising a first electrically conductive filler material 124 extends from the top</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>semiconductor comprising surface 212 to protruding integral tips 216 and 217 that extend beyond the bottom surface 213 and provide an electrical contact between die paddle 206 and a ground pad (i.e. connected to ground pins of the IC 210) 243 on the top semiconductor surface 212.” Dunne, [7:46-7:65].</p> <p>“FIG. 3 shows a cross sectional depiction of a semiconductor device 300 that comprises IC die 260 joined to die pad 206 of lead-frame 205, according to another embodiment of the invention. The IC die 260 includes a thin metal layer 221 and an electrically conductive die attach adhesive layer 222 comprising a third electrically conductive composition, such as a solder filled polymer, wherein the solder can be arranged in an electrically interconnected network, positioned between the metal layer 221 and the die pad 206 of the package substrate 205. As shown in FIG. 3, the metal layer 221 capped protruding integral tips 216, 217 extend into the electrically conductive die attach adhesive layer 222 which functions as a ground connection enhancement region.” Dunne, [8:41-8:53].</p> <p>“FIG. 4 shows a cross sectional depiction of a stacked die comprising semiconductor device 400 according to another embodiment of the invention. Stacked die comprising semiconductor device 400 comprises a second IC die 410 flip chip joined to the semiconductor device 300 shown in FIG. 3. Pads 411 of second IC die 410 are bonded to the tops of TSVs 110 by bond pads 243 which can comprise materials such as solder, Au or other suitable bond pad materials. Low resistance ground connections are thus provided to IC 410 via TSVs 110 to die paddle 206 via protruding integral tips 216, 217, backside finish layer 221 and ground connection enhancement region 222. Although not shown, second IC die 410 can also comprise TSVs and thus be stacked face-up on IC die 260, and can include additional TSV comprising die (not shown) stacked thereon.” Dunne, [9:18-9:32].</p>
--	--



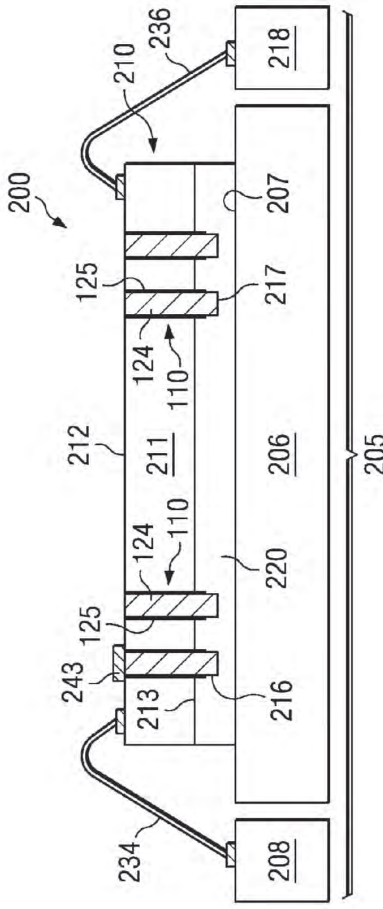
Dunne, FIG. 4

To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Dunne discloses, either expressly or inherently, the spacer connector comprises a core substrate.

See, e.g.:

“Referring now to FIG. 2, a cross sectional depiction of semiconductor device 200 comprising first IC die 210 comprising of substrate (e.g., wafer or die) 211 including active top semiconductor surface 212 and a bottom surface 213, according to an embodiment of the

	<p>invention, is shown. Device 200 comprises a package substrate with leadframe 205 comprising a die paddle 206, wherein the die paddle 206 has a top metal comprising surface 207. Packaging material, such as plastic encapsulant, is not shown. Bond wires 234 and 236 are shown providing a connection between an I/O or power supply node for integrated circuitry formed on active semiconductor surface 212 to lead fingers 208 and 218. First IC die 210 is shown mounted face up on the top metal comprising surface 207. A plurality of TSVs 110 comprising a first electrically conductive filler material 124 extends from the top semiconductor comprising surface 212 to protruding integral tips 216 and 217 that extend beyond the bottom surface 213 and provide an electrical contact between die paddle 206 and a ground pad (i.e. connected to ground pins of the IC 210) 243 on the top semiconductor surface 212. Although not shown, TSVs 110 generally include a barrier layer and seed layer in the case of conventional Cu TSVs.” Dunne, [7:46-7:67].</p>  <p style="text-align: center;">FIG. 2</p> <p>Dunne, FIG. 2</p>
--	---

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>“FIG. 4 shows a cross sectional depiction of a stacked die comprising semiconductor device 400 according to another embodiment of the invention. Stacked die comprising semiconductor device 400 comprises a second IC die 410 flip chip joined to the semiconductor device 300 shown in FIG. 3. Pads 411 of second IC die 410 are bonded to the tops of TSVs 110 by bond pads 243 which can comprise materials such as solder, Au or other suitable bond pad materials. Low resistance ground connections are thus provided to IC 410 via TSVs 110 to die paddle 206 via protruding integral tips 216, 217, backside finish layer 221 and ground connection enhancement region 222. Although not shown, second IC die 410 can also comprise TSVs and thus be stacked face-up on IC die 260, and can include additional TSV comprising die (not shown) stacked thereon.” Dunne, [9:19-9:34].</p> <p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Dunne discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“As known in the art, TSVs which are also referred to as through-wafer vias (TWVs), are vertical electrical connections that pass from the frontside surface of a wafer or IC die (e.g., contact level or one of the metal levels) completely through to the backside surface.” Dunne, [1:23-1:27].</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>“The TSV 110 comprises a first electrically conductive filler material 124 (e.g., Cu or a Cu alloy) having an optional liner 125. TSV 110 includes a protruding integral tip 104 comprising sidewalls 103 that comprises the first electrically conductive filler material 124.” Dunne, [4:17-4:21].</p> <p>“Liner 125 is shown extending from the top semiconductor surface 106 to the bottom surface 107 and include a tip liner portion that extends past the bottom surface 107 a distance equal to at least 1% of tip height.” Dunne, [4:24-4:27].</p> <p>“Embedded via-first TSVs are conventionally formed by topside via etching (e.g., by RIE) to a depth less than the thickness of the substrate/wafer, framing the via by forming a dielectric liner in the via, followed by filling the via with an electrically conductive filler material.” Dunne, [4:49-4:53].</p> <p>“A plurality of TSVs 110 comprising a first electrically conductive filler material 124 extends from the top semiconductor comprising surface 212 to protruding integral tips 216 and 217 that extend beyond the bottom surface 213 and provide an electrical contact between die paddle 206 and a ground pad (i.e. connected to ground pins of the IC 210) 243 on the top semiconductor surface 212. Although not shown, TSVs 110 generally include a barrier layer and seed layer in the case of conventional Cu TSVs. As shown in FIG. 2, the protruding integral tips 216, 217 protrude from the bottom surface 213 of the substrate 211 a tip height that is generally 1 to 50 μm, and is typically between 2 and 20 μm. A metal layer 220 is on both the bottom surface 213 of the substrate 211 and on the protruding integral tips 216, 217. The metal layer 220 comprises a second electrically conductive metal comprising composition that is different from the first electrically conductive filler material 124 of the TSV 110, and the top metal comprising surface 207 of the die paddle 206.” Dunne, [7:58-8:10].</p>
--	--

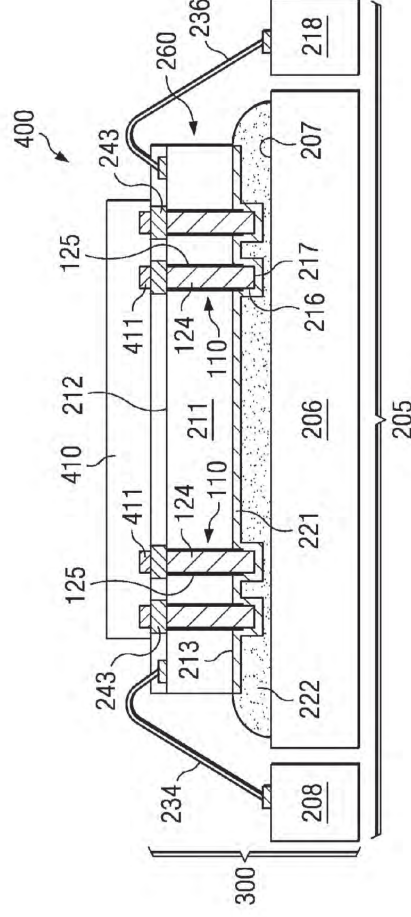


FIG. 4

Dunne, FIG. 4

“The IC die 260 includes a thin metal layer 221 and an electrically conductive die attach adhesive layer 222 comprising a third electrically conductive composition, such as a solder filled polymer, wherein the solder can be arranged in an electrically interconnected network, positioned between the metal layer 221 and the die pad 206 of the package substrate 205. As shown in FIG. 3, the metal layer 221 capped protruding integral tips 216, 217 extend into the electrically conductive die attach adhesive layer 222 which functions as a ground connection enhancement region.” Dunne, [8:44-8:53].

To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;	<p>Dunne discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“The TSV 110 comprises a first electrically conductive filler material 124 (e.g., Cu or a Cu alloy) having an optional liner 125. TSV 110 includes a protruding integral tip 104 comprising sidewalls 103 that comprises the first electrically conductive filler material 124.” Dunne, [4:17-4:21].</p> <p>“A plurality of TSVs 110 comprising a first electrically conductive filler material 124 extends from the top semiconductor comprising surface 212 to protruding integral tips 216 and 217 that extend beyond the bottom surface 213 and provide an electrical contact between die paddle 206 and a ground pad (i.e. connected to ground pins of the IC 210) 243 on the top semiconductor surface 212.” Dunne, [7:58-7:64].</p>

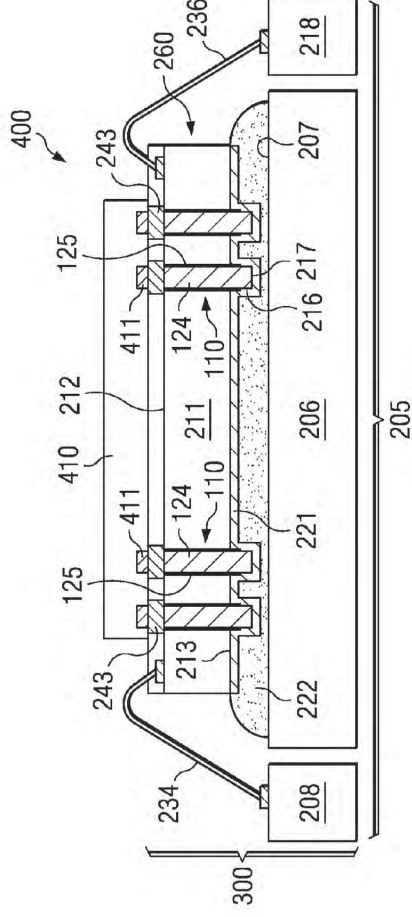


FIG. 4

Dunne, FIG. 4

“A plurality of TSVs 110 comprising a first electrically conductive filler material 124 extends from the top semiconductor surface 212 to protruding integral tips 216 and 217 that extend beyond the bottom surface 213 and provide an electrical contact between die paddle 206 and a ground pad (i.e. connected to ground pins of the IC 210) 243 on the top semiconductor surface 212. Although not shown, TSVs 110 generally include a barrier layer and seed layer in the case of conventional Cu TSVs.” Dunne, [7:59-7:67].

“As shown in FIG. 2, the protruding integral tips 216, 217 protrude from the bottom surface 213 of the substrate 211 a tip height that is generally 1 to 50 μm , and is typically between 2 and 20 μm . A metal layer 220 is on both the bottom surface 213 of the substrate 211 and on the protruding integral tips 216, 217.” Dunne, [8:1-8:6].

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>“Thin metal backside finish layer 221 can comprise an electrolessly plated metal finish in a thickness range from about 0.5 to 3 μm. Exemplary materials for thin metal backside finish layer 221 can include Al(Cu), electroless NiPd or NiAu or NiPdAu, Cu/electroless NiPd or NiAu or NiPdAu, and Cu/electrolytic NiPd. Although not shown, protruding integral tips 216, 217 can further comprise tip surface finish layers that are only on the protruding integral tips 216, 217.” Dunne, [8:61-9:1].</p> <p>“Pads 411 of second IC die 410 are bonded to the tops of TSVs 110 by bond pads 243 which can comprise materials such as solder, Au or other suitable bond pad materials.” Dunne, [9:23-9:26].</p> <p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Dunne discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The TSVs comprise a first electrically conductive composition and include a protruding integral tip having sidewalls comprising the first electrically conductive composition that protrudes from a bottom surface of the substrate to a tip having a distal end that has a tip height that is generally between 1 and 50 μm. A metal layer is on the bottom surface of the IC die, and the sidewalls and the distal end of the protruding integral tip, wherein the metal</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

layer comprises a second electrically conductive metal comprising composition that is different from the first electrically conductive composition.” Dunne, [2:41-2:51].

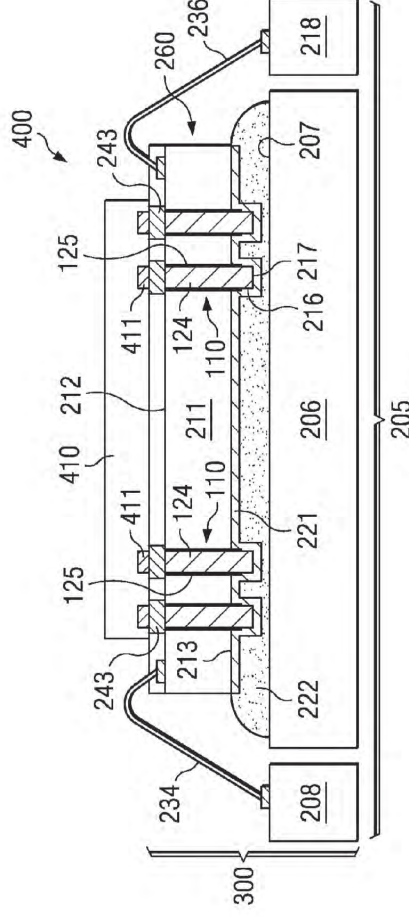


FIG. 4

Dunne, FIG. 4

“The TSV 110 comprises a first electrically conductive filler material 124 (e.g., Cu or a Cu alloy) having an optional liner 125. TSV 110 includes a protruding integral tip 104 comprising sidewalls 103 that comprises the first electrically conductive filler material 124.” Dunne, [4:17-4:21].

“FIG. 1A shows the liner 125 extending out from the bottom surface 107 of substrate 105 a distance that is at least about 50% of the tip height.” Dunne, [4:35-4:37].

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>“A plurality of TSVs 110 comprising a first electrically conductive filler material 124 extends from the top semiconductor comprising surface 212 to protruding integral tips 216 and 217 that extend beyond the bottom surface 213 and provide an electrical contact between die paddle 206 and a ground pad (i.e. connected to ground pins of the IC 210) 243 on the top semiconductor surface 212.” Dunne, [7:59-7:65].</p> <p>“As shown in FIG. 2, the protruding integral tips 216, 217 protrude from the bottom surface 213 of the substrate 211 a tip height that is generally 1 to 50 μm, and is typically between 2 and 20 μm.” Dunne, [8:1-8:4].</p> <p>“As shown in FIG. 3, the metal layer 221 capped protruding integral tips 216, 217 extend into the electrically conductive die attach adhesive layer 222 which functions as a ground connection enhancement region.” Dunne, [8:50-8:53].</p> <p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Dunne discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

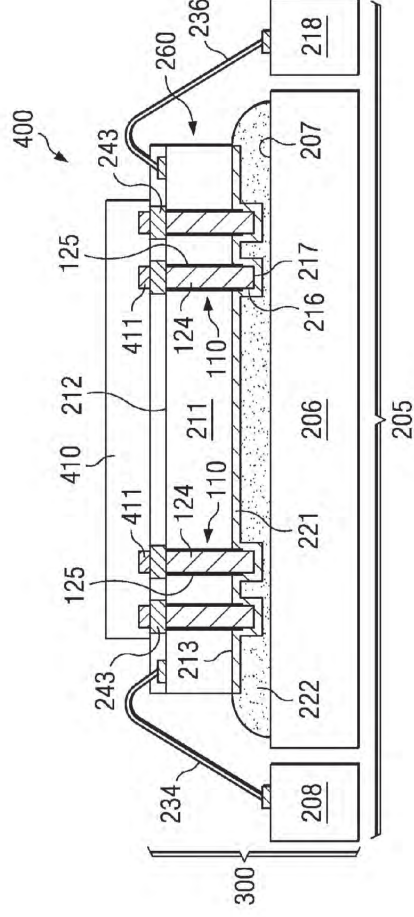


FIG. 4

Dunne, FIG. 4

To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.1] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and

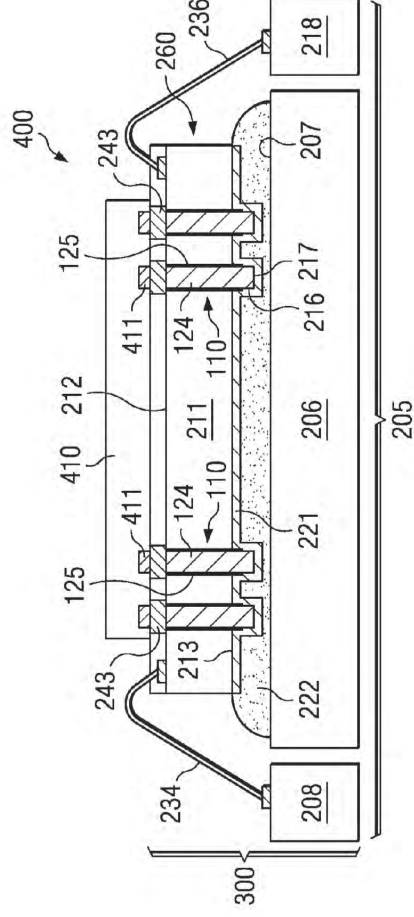
Dunne discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.

See, e.g.:

	<p style="text-align: center;">FIG. 4</p>
	<p>Dunne, FIG. 4</p> <p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p>	<p>Dunne discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

<p>top metal pillars of the bottom package substrate; and</p>	<p style="text-align: center;">FIG. 4</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Dunne, FIG. 4</p> <p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Dunne discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>



Dunne, FIG. 4

To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and

See, e.g.:

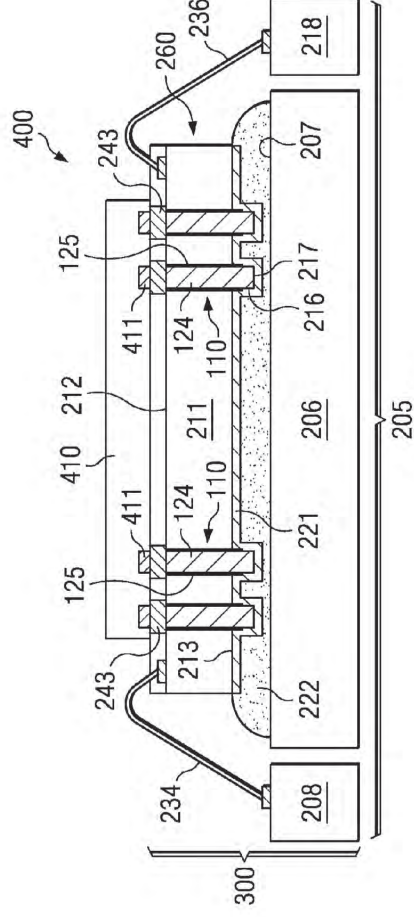


FIG. 4

Dunne, FIG. 4

To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

See, e.g.:

“FIG. 4 shows a cross sectional depiction of a stacked die comprising semiconductor device 400 according to another embodiment of the invention. Stacked die comprising

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

semiconductor device 400 comprises a second IC die 410 flip chip joined to the semiconductor device 300 shown in FIG. 3. Pads 411 of second IC die 410 are bonded to the tops of TSVs 110 by bond pads 243 which can comprise materials such as solder, Au or other suitable bond pad materials. Low resistance ground connections are thus provided to IC 410 via TSVs 110 to die paddle 206 via protruding integral tips 216, 217, backside finish layer 221 and ground connection enhancement region 222. Although not shown, second IC die 410 can also comprise TSVs and thus be stacked face-up on IC die 260, and can include additional TSV comprising die (not shown) stacked thereon." Dunne, [9:19-9:34].

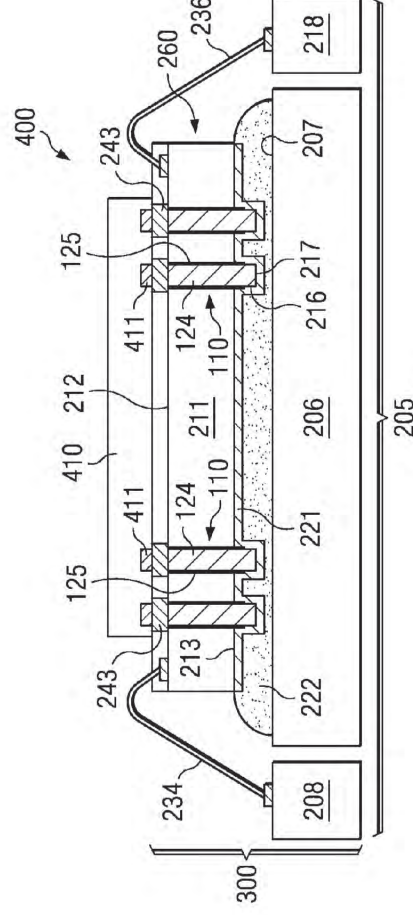


FIG. 4

Dunne, FIG. 4

To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
Claim 2, U.S. Patent No. 9859202	
Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Dunne discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p>See, e.g.:</p> <p>Dunne, FIG. 4</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Dunne discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Referring now to FIG. 2, a cross sectional depiction of semiconductor device 200 comprising first IC die 210 comprising of substrate (e.g., wafer or die) 211 including active top semiconductor surface 212 and a bottom surface 213, according to an embodiment of the invention, is shown. Device 200 comprises a package substrate with leadframe 205 comprising a die paddle 206, wherein the die paddle 206 has a top metal comprising surface 207. Packaging material, such as plastic encapsulant, is not shown. Bond wires 234 and 236 are shown providing a connection between an I/O or power supply node for integrated circuitry formed on active semiconductor surface 212 to lead fingers 208 and 218. First IC die 210 is shown mounted face up on the top metal comprising surface 207.” Dunne, [7:46-7:59].</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>“FIG. 3 shows a cross sectional depiction of a semiconductor device 300 that comprises IC die 260 joined to die pad 206 of lead-frame 205, according to another embodiment of the invention. The IC die 260 includes a thin metal layer 221 and an electrically conductive die attach adhesive layer 222 comprising a third electrically conductive composition, such as a solder filled polymer, wherein the solder can be arranged in an electrically interconnected network, positioned between the metal layer 221 and the die pad 206 of the package substrate 205.” Dunne, [8:41-8:50].</p> <p>“FIG. 4 shows a cross sectional depiction of a stacked die comprising semiconductor device 400 according to another embodiment of the invention. Stacked die comprising semiconductor device 400 comprises a second IC die 410 flip chip joined to the semiconductor device 300 shown in FIG. 3. Pads 411 of second IC die 410 are bonded to the tops of TSVs 110 by bond pads 243 which can comprise materials such as solder, Au or other suitable bond pad materials. Low resistance ground connections are thus provided to IC 410 via TSVs 110 to die paddle 206 via protruding integral tips 216, 217, backside finish layer 221 and ground connection enhancement region 222. Although not shown, second IC die 410 can also comprise TSVs and thus be stacked face-up on IC die 260, and can include additional TSV comprising die (not shown) stacked thereon.” Dunne, [9:19-9:34].</p>
--	--

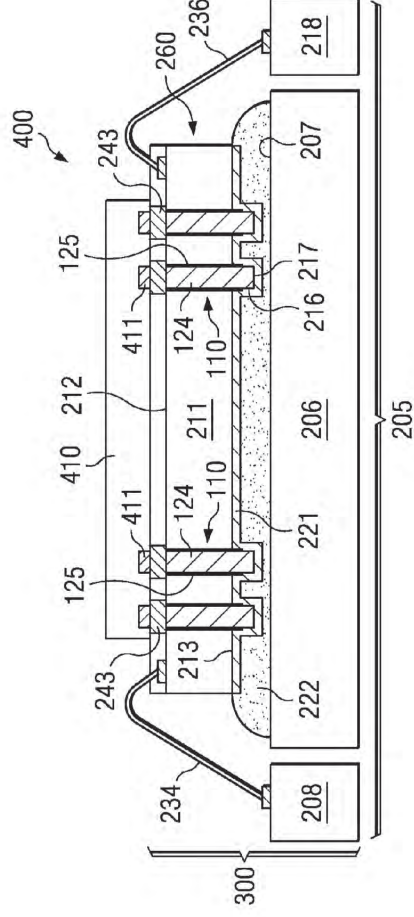


FIG. 4

Dunne, FIG. 4

“Although not shown, second IC die 410 can also comprise TSVs and thus be stacked face-up on IC die 260, and can include additional TSV comprising die (not shown) stacked thereon.” Dunne, [9:30-9:34].

To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Dunne discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <div> </div> <p align="center">FIG. 4</p> <p>Dunne, FIG. 4</p> <p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p>See, e.g.:</p>	<p>Dunne discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p>See, e.g.:</p> <p>FIG. 4</p> <p>Dunne, FIG. 4</p>

Appendix A-6 - Invalidity of U.S. Patent No. 9859202 in view of Dunne - U.S. Patent No. 8436475

	<p>To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the plurality of metal pillars of the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the bottom package substrate via the plurality of metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>	<p>Dunne discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

the corresponding top metal pads of the spacer connector.

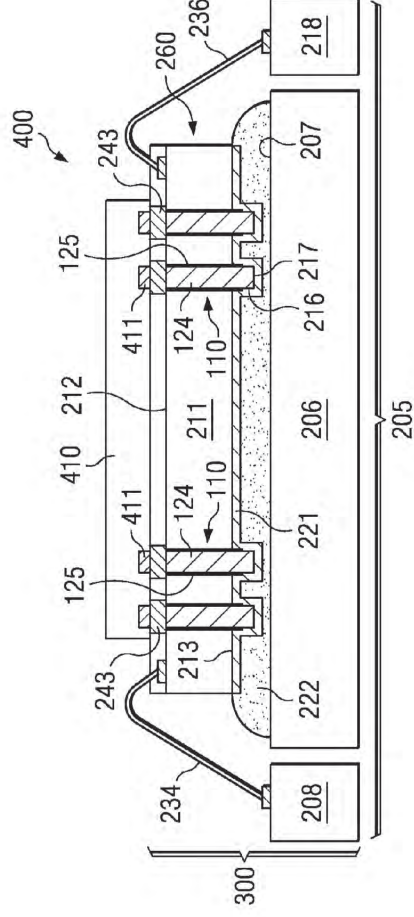


FIG. 4

Dunne, FIG. 4

To the extent Plaintiff contends that Dunne fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

U.S. Patent No. 8618669 (“Furuta '669”) is titled Combination Substrate and lists Toru Furuta as inventor. Furuta '669 is assigned to Ibidon Co., Ltd. Furuta '669 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the '202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff's apparent infringement theory.² Furuta '669 is a U.S. patent that was filed July 16, 2008 and published July 9, 2009. Furuta '669 claims priority to a provisional application filed on January 9, 2008. Furuta '669 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Furuta '669, or otherwise rendered obvious by disclosures and teachings of Furuta '669, including under TopWire's apparent interpretation of the Asserted Claims as Samsung understands them from TopWire's Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Furuta '669 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Furuta '669 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung's other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung's Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Furuta '669, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire's March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court's order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire's apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung's interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Furuta '669 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Furuta '669 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Furuta '669 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Furuta '669 discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 4(A) illustrates a sectional view of a combination substrate 10 in accordance with Example 1. The combination substrate 10 comprises an upper substrate 12 U and a lower substrate 12 L. On the upper substrate 12 U there are disposed a pad group of pads for package substrate connection 42 P on the center portion of the upper substrate 12 U, as illustrated in the plan view of FIG. 6(A) corresponding to the a arrow directional view in FIG. 4(A). On the lower substrate 12 L there is likewise formed a pad group for external connection such as</p>

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>the BGA of pads 42 D for connecting to another printed wiring board. On the upper face of the lower substrate 12 L there is mounted an IC chip 50. As to the lower substrate 12 L, conductor circuits 42 b on the lower face and conductor circuits 42 a on the upper face are connected via vias 44, and the IC chip 50 and the conductor circuits 42 a on the upper face are connected via solder bumps 52. In this case, the IC chip 50 may be mounted by other mounting configurations (wire bonding mounting, for example). A plurality of IC chips may be mounted. In the opening portions 48 a in a solder resist 8 of the conductor circuits 42 a on the upper face side of the lower substrate 12 L there is formed a pad group of pads 42 G for upper substrate connection. In the opening portions 48 a in a solder resist 48 of the conductor circuits 42 on the lower face side there is formed a pad group constituting pads 42 D for printed wiring board connection. Likewise, as to the upper substrate 12 U, the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected via vias 44. In the opening portions 42 a in the solder resist 48 of the conductor circuits 42 a on the lower face side of the upper substrate 12 U there is formed a pad group of pads 42 F for lower substrate connection, and in the opening portions 48 a in the solder resist 48 of the conductor circuits 42 b on the upper face side there is formed a pad group of pads 42 P for package substrate connection. Between the lower substrate 12 L and the IC chip 50 there is filled an insulating resin such as an underfill 60 such as an epoxy resin, and between the upper substrate 12 U and the lower substrate 12 L there is filled an insulating resin being a resin filler agent (underfill) 62. The underfill 60 and the resin filler agent 62 are preferably composed of a thermosetting resin and an inorganic filler. The pads 42 F on the lower face side of the upper substrate 12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected via cylindrical metal posts 46, 46.” Furuta ’669, [2:58-3:34].</p> <p>“FIG. 7 illustrates a combination substrate pertaining to Revised Example 1 of Example 1. With Example 1, an IC chip 50 was mounted on the upper face of the lower substrate 12 L</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>as illustrated in FIG. 5(B). In lieu of this, an IC chip may also be mounted on the lower face of the upper substrate 12 U, as illustrated in FIG. 7." Furuta '669, [6:66-7:4].</p> <p>"FIG. 12(A) illustrates a sectional view of the combination substrate 10 in accordance with Example 2. The combination substrate 10 comprises an upper substrate 12 U, an interposer 12 M being an intermediate material, and a lower substrate 12 L. On the upper substrate 12 U, a pad group of pads 42 P for package substrate connection is disposed in the center region of the upper substrate 12 U, as illustrated in the plan view of FIG. 14(A) corresponding to the arrow directional view in FIG. 12(A). On the lower substrate 12 L there is likewise formed a pad group of pads 42 D to connect to a printed wiring board. On the upper face of the lower substrate 12 L there is mounted an IC chip 50. As to the lower substrate 12 L conductor circuits 42 b on the lower face side and conductor circuits 42 a on the upper face side are connected vias 44, and the IC chip 50 and the conductor circuits 42 b on the upper face side are connected via solder bumps 52. In openings 48 a in a solder resist 48 on the conductor circuits 42 a on the upper face side of the lower substrate 12 L there are formed pads 42 G for the upper substrate connection, and in openings 48 a in a solder resist 48 on conductor circuits 42 b on the lower face side there are formed a pad group of pads 42 D for printed wiring substrate connection. Likewise, as to the lower substrate 12 L the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected vias 44. In openings 48 a in the solder resist 48 on the conductor circuits 42 a on the lower face side of the upper substrate 12 U there are formed pads 42 F for the lower substrate connection, and in openings 48 a in the solder resist 48 on the conductor circuits 42 b on the upper face side there are formed pads 42 P for package substrate connection. Between the lower substrate 12 L and the IC chip 50 there is filled underfill 60 being an insulating resin, and between the upper substrate 12 U and the lower substrate 12 L there is filled a resin filler (underfill) 62. The pads 42 F on the lower face side of the upper substrate</p>
--	---

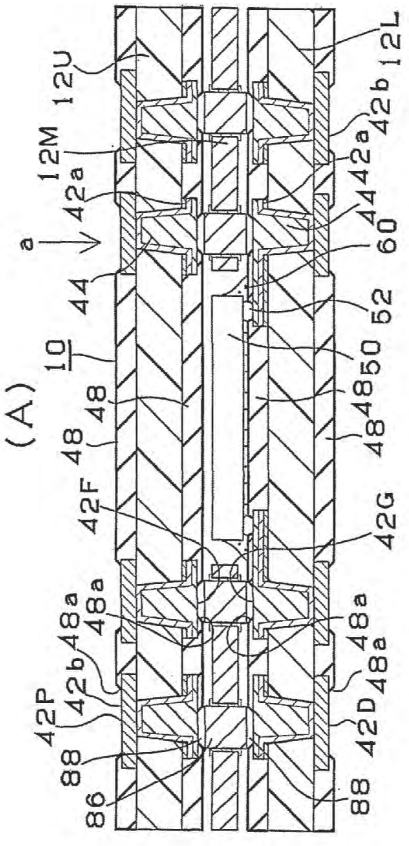
	<p>12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected with cylindrical metal posts 86 of the interposer 12 M.” Furuta ’669, [7:16-7:56].</p> <p>FIG. 12</p> <p>Furuta, FIG. 12</p> <p>“FIG. 15 illustrates a combination substrate pertaining to Revised Example 1 of Example 2. With Example 2, an IC chip 50 was mounted on the upper face of the lower substrate 12 L as illustrated in FIG. 13(A). In lieu of this, an IC chip may also be mounted on the lower face of the upper substrate 12 U, as illustrated in FIG. 15.” Furuta ’669, [10:14-10:19].</p> <p>“According to the foregoing embodiments, a combination substrate includes a lower substrate having the first main face and the second main face opposite the previously-described first main face; connection pads formed on the first face of the previously-described lower</p>
--	--

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>substrate; mounting pads formed on the second main face of the previously-described lower substrate and for connecting with a printed wiring board; an upper substrate having the first main face and the second main face opposite the previously-described first main face; mounting pads formed on the first main face of the previously-described upper substrate and for loading a package substrate; component loading pads formed on the second main face of the previously-described upper substrate or on the first main face of the previously-described lower substrate and for loading an electronic component; and connection pads formed on the second main face of the previously-described upper substrate and for electrically connecting with the connection pads of the previously-described lower substrate. The first main face of the previously-described lower substrate and the second main face of the previously-described upper substrate mutually face and a resin is filled between the previously-described lower substrate and the previously-described upper substrate.” Furuta ’669, [10:27-10:49].</p>
[1.A] a bottom package substrate;	<p>Furuta ’669 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 4(A) illustrates a sectional view of a combination substrate 10 in accordance with Example 1. The combination substrate 10 comprises an upper substrate 12 U and a lower substrate 12 L. On the upper substrate 12 U there are disposed a pad group of pads for package substrate connection 42 P on the center portion of the upper substrate 12 U, as illustrated in the plan view of FIG. 6(A) corresponding to the a arrow directional view in FIG. 4(A). On the lower substrate 12 L there is likewise formed a pad group for external connection such as the BGA of pads 42 D for connecting to another printed wiring board. On the upper face of the lower substrate 12 L there is mounted an IC chip 50. As to the lower substrate 12 L, conductor circuits 42 b on the lower face and conductor circuits 42 a on the upper face are</p>

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

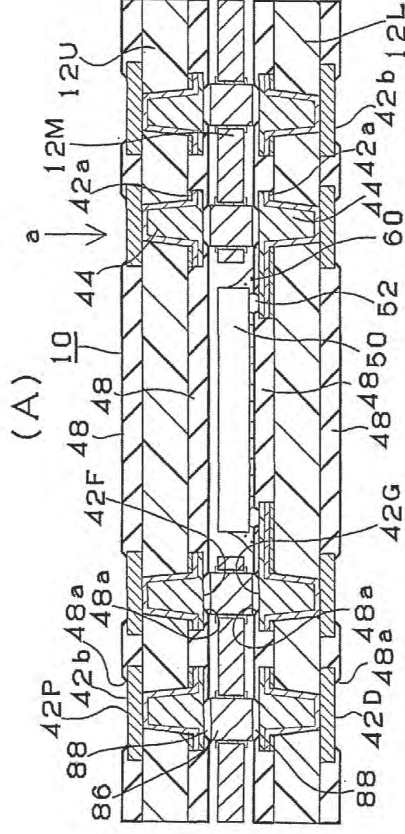
	<p>connected via vias 44, and the IC chip 50 and the conductor circuits 42 a on the upper face are connected via solder bumps 52.” Furuta ’669, [2:58-3:6].</p> <p>“In the opening portions 48 a in a solder resist 8 of the conductor circuits 42 a on the upper face side of the lower substrate 12 L there is formed a pad group of pads 42 G for upper substrate connection. In the opening portions 48 a in a solder resist 48 of the conductor circuits 42 on the lower face side there is formed a pad group constituting pads 42 D for printed wiring board connection.” Furuta ’669, [3:9-3:15].</p> <p>“On the pads 42 D on the lower face side of the combination substrate 10 there are provided external connection terminals 64 L such as BGA and solder bumps, and by their being connected to pads 76 of another printed wiring board 74 as illustrated in FIG. 5(B) said combination substrate 10 is loaded onto the printed wiring board 74.” Furuta ’669, [3:35-3:40].</p> <p>“FIG. 12(A) illustrates a sectional view of the combination substrate 10 in accordance with Example 2. The combination substrate 10 comprises an upper substrate 12 U, an interposer 12 M being an intermediate material, and a lower substrate 12 L. On the upper substrate 12 U, a pad group of pads 42 P for package substrate connection is disposed in the center region of the upper substrate 12 U, as illustrated in the plan view of FIG. 14(A) corresponding to the arrow directional view in FIG. 12(A). On the lower substrate 12 L there is likewise formed a pad group of pads 42 D to connect to a printed wiring board. On the upper face of the lower substrate 12 L there is mounted an IC chip 50. As to the lower substrate 12 L conductor circuits 42 b on the lower face side and conductor circuits 42 a on the upper face side are connected vias 44, and the IC chip 50 and the conductor circuits 42 b on the upper face side are connected via solder bumps 52. In openings 48 a in a solder resist 48 on the conductor circuits 42 a on the upper face side of the lower substrate 12 L there are formed pads 42 G</p>
--	---

	<p>for the upper substrate connection, and in openings 48 a in a solder resist 48 on conductor circuits 42 b on the lower face side there are formed a pad group of pads 42 D for printed wiring substrate connection.” Furuta ’669, [7:16-7:38].</p> <p>FIG. 12</p>  <p>Furuta, FIG. 12</p> <p>“Steps 1 through 4 under Example 1 apply likewise (FIG. 10(A)). Then, with the mounting step for the IC chip 50 having been performed, the lower substrate 12 L with the IC chip 50 mounted can be obtained (FIG. 10(B), FIG. 10(C)).” Furuta ’669, [8:15-8:18].</p> <p>“According to the foregoing embodiments, a combination substrate includes a lower substrate having the first main face and the second main face opposite the previously-described first main face; connection pads formed on the first face of the previously-described lower</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>substrate; mounting pads formed on the second main face of the previously-described lower substrate and for connecting with a printed wiring board; an upper substrate having the first main face and the second main face opposite the previously-described first main face; mounting pads formed on the first main face of the previously-described upper substrate and for loading a package substrate; component loading pads formed on the second main face of the previously-described upper substrate or on the first main face of the previously-described lower substrate and for loading an electronic component; and connection pads formed on the second main face of the previously-described upper substrate and for electrically connecting with the connection pads of the previously-described lower substrate.” Furuta ’669, [10:27-10:44].</p> <p>To the extent Plaintiff contends that Furuta ’669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Furuta ’669 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The combination substrate 10 comprises an upper substrate 12 U and a lower substrate 12 L. On the upper substrate 12 U there are disposed a pad group of pads for package substrate connection 42 P on the center portion of the upper substrate 12 U, as illustrated in the plan view of FIG. 6(A) corresponding to the a arrow directional view in FIG. 4(A). On the lower substrate 12 L there is likewise formed a pad group for external connection such as the BGA of pads 42 D for connecting to another printed wiring board.” Furuta ’669, [2:59-3:1].</p>

FIG. 12



Furuta, FIG. 12

“The pads 42 F on the lower face side of the upper substrate 12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected via cylindrical metal posts 46, 46. On the pads 42 D on the lower face side of the combination substrate 10 there are provided external connection terminals 64 L such as BGA and solder bumps, and by their being connected to pads 76 of another printed wiring board 74 as illustrated in FIG. 5(B) said combination substrate 10 is loaded onto the printed wiring board 74. In the combination substrate 10 in Example 1, on account of the underfill 62 having been filled between the upper substrate 12 U and the lower substrate 12 L, it now becomes possible to control the warpage and separation of the upper substrate 12 U and the lower substrate 12 L and to ease stresses on account of the underfill 62 even when the upper substrate 12 U and the lower

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>substrate 12 L are heated such that stresses are generated toward warpage and separation being generated.” Furuta ’669, [3:31-3:48].</p> <p>“The circuits (pads) 42 G of the lower substrate 12 L and the circuits (pads) 42 F of the upper substrate 12 U are aligned. At that time, the joining is done such that the posts 46 of the upper substrate 12 U are pressed onto the posts 46 of the lower substrate 12 L, on which solder 49 is formed (FIG. 3(E)). Then, the conductor circuits (pads) 42 G of the lower substrate 12 L and the conductor circuits (pads) 42 F of the upper substrate 12 U are connected via the posts 46, 46 by reflow.” Furuta ’669, [5:51-5:58].</p> <p>“The combination substrate 10 comprises an upper substrate 12 U, an interposer 12 M being an intermediate material, and a lower substrate 12 L. On the upper substrate 12 U, a pad group of pads 42 P for package substrate connection is disposed in the center region of the upper substrate 12 U, as illustrated in the plan view of FIG. 14(A) corresponding to the arrow directional view in FIG. 12(A). On the lower substrate 12 L there is likewise formed a pad group of pads 42 D to connect to a printed wiring board.” Furuta ’669, [7:18-7:27].</p> <p>“The circuits (pads) 42 G of the lower substrate 12 L, posts 86 of the interposer 12 M, and the circuits (pads) 42 F of the upper substrate 12 U are aligned (FIG. 12(A)). At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact. That allows the upper substrate 12 U and the lower substrate 12 L to be electrically connected via the interposer 12 M.” Furuta ’669, [9:3-9:13].</p> <p>“According to the foregoing embodiments, a combination substrate includes a lower substrate having the first main face and the second main face opposite the previously-described first</p>
--	--

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>main face; connection pads formed on the first face of the previously-described lower substrate; mounting pads formed on the second main face of the previously-described lower substrate and for connecting with a printed wiring board; an upper substrate having the first main face and the second main face opposite the previously-described first main face; mounting pads formed on the first main face of the previously-described upper substrate and for loading a package substrate; component loading pads formed on the second main face of the previously-described upper substrate or on the first main face of the previously-described lower substrate and for loading an electronic component; and connection pads formed on the second main face of the previously-described upper substrate and for electrically connecting with the connection pads of the previously-described lower substrate. The first main face of the previously-described lower substrate and the second main face of the previously-described upper substrate mutually face and a resin is filled between the previously-described lower substrate and the previously-described upper substrate.” Furuta ’669, [10:27-10:49].</p> <p>To the extent Plaintiff contends that Furuta ’669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Furuta ’669 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p> <p>“Between the lower substrate 12 L and the IC chip 50 there is filled an insulating resin such as an underfill 60 such as an epoxy resin, and between the upper substrate 12 U and the lower</p>

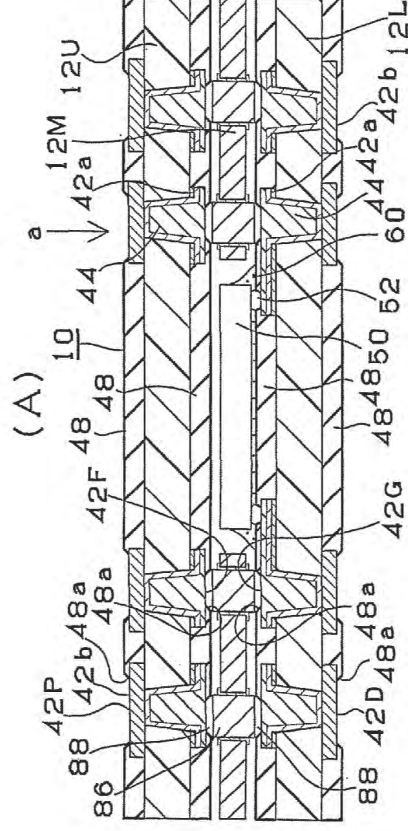
Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

substrate 12 L there is filled an insulating resin being a resin filler agent (underfill) 62.”
Furuta '669, [3:25-3:29].

“Then, the conductor circuits (pads) 42 G of the lower substrate 12 L and the conductor circuits (pads) 42 F of the upper substrate 12 U are connected via the posts 46, 46 by reflow. At that juncture, the end faces of the upper substrate 12 U and of the lower substrate 12 L are in a linear configuration.” Furuta ’669, [5:56-5:60].

“The combination substrate 10 comprises an upper substrate 12 U, an interposer 12 M being an intermediate material, and a lower substrate 12 L.” Furuta ’669, [7:18-7:20].

FIG. 12



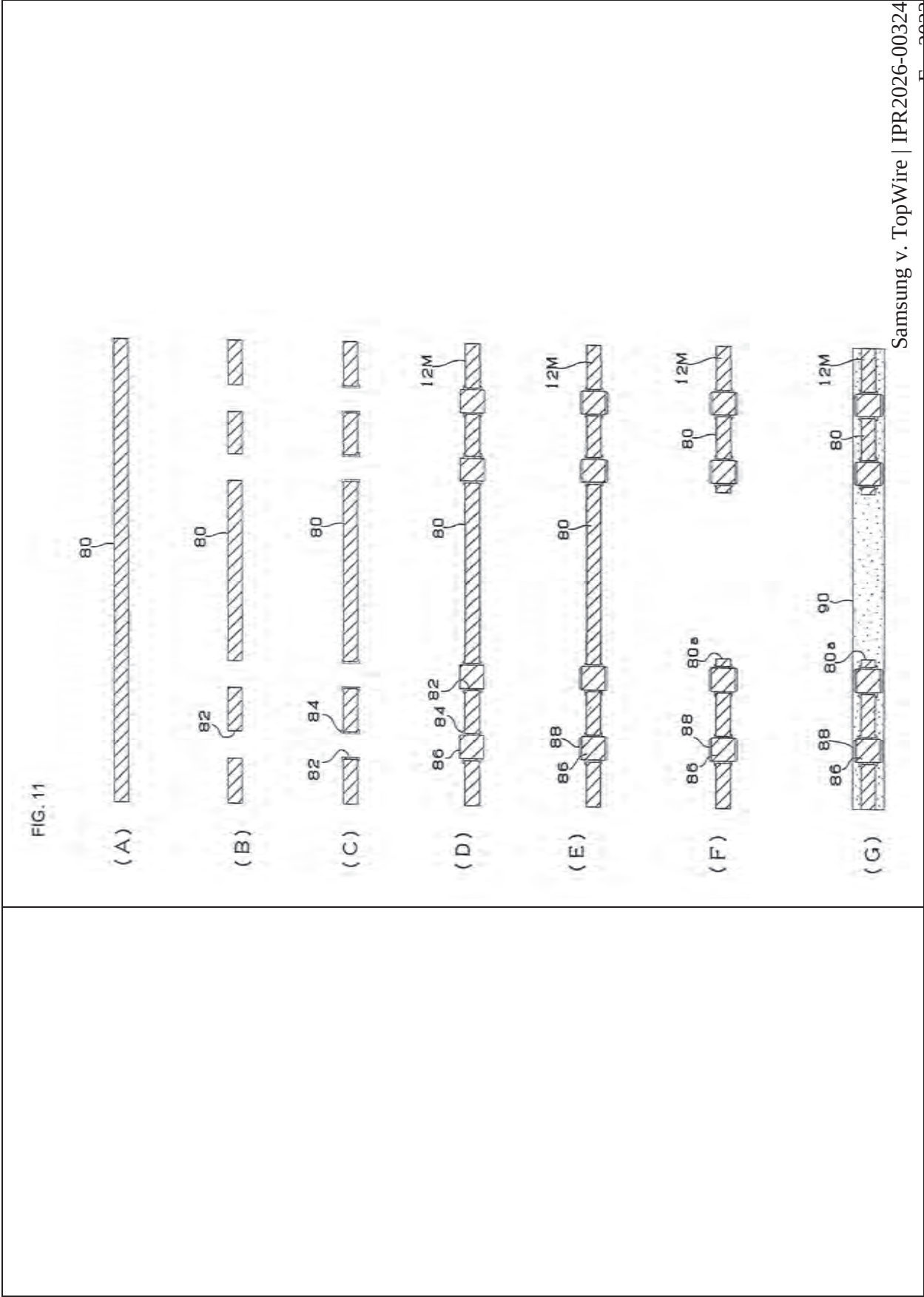
Furuta, FIG. 12

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>“An insulating material 80 is prepared (FIG. 11(A)). Openings 82 penetrating the insulating material 80 are formed (FIG. 11 (B)), and a conductor layer 84 is formed in said openings 82 (FIG. 11(C)). The conductor layer 84 is formed by the through-hole, via, and post such as implant.” Furuta '669, [8:20-8:24].</p> <p>“The circuits (pads) 42 G of the lower substrate 12 L, posts 86 of the interposer 12 M, and the circuits (pads) 42 F of the upper substrate 12 U are aligned (FIG. 12(A)). At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact.” Furuta '669, [9:3-9:10].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Furuta '669 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The combination substrate 10 comprises an upper substrate 12 U, an interposer 12 M being an intermediate material, and a lower substrate 12 L.” Furuta '669, [7:18-7:20].</p> <p>“Formation of an Interposer An insulating material 80 is prepared (FIG. 11(A)). Openings 82 penetrating the insulating material 80 are formed (FIG. 11 (B)), and a conductor layer 84 is formed in said openings 82 (FIG. 11(C)). The conductor layer 84 is formed by the through-</p>

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>hole, via, and post such as implant. For a conductor layer, a metal such as Cu, Ni, and a precious metal may be used. As an example therefor, a method of filling a post with an implant is available. An insulating substrate having on both faces a conductor layer formed with a copper foil, plating, etc., is prepared. Openings for penetration are provided in the insulating substrate with drilling or laser. Then, a resist layer is provided on the entirety of the face of the conductor layer, and a mask with the wiring pattern drawn thereon is placed. Following that, a pattern for the interposer is formed through an etching treatment after having undergone exposure and development. Then, a solder resist layer may be formed or the external shape may be treated (single-piece treatment of interposer), as necessary. This results in the preparation of an insulating substrate having openings for implant.” Furuta ’669, [8:18-8:38].</p>
--	---



Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

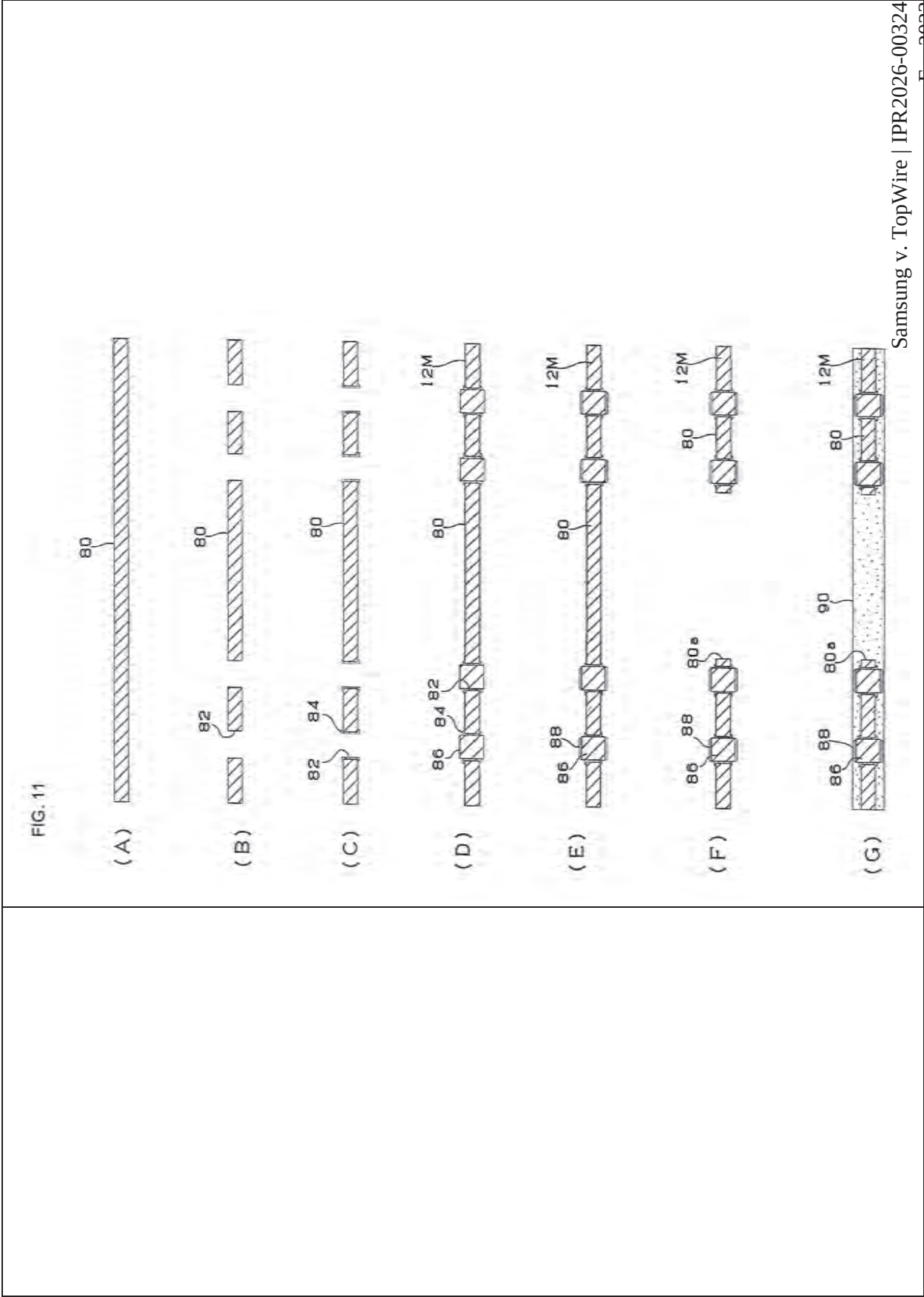
	<p>Furuta, FIG. 11</p> <p>“This allows the preparation of an interposer 12 M to be sandwiched between the upper substrate and the lower substrate.” Furuta '669, [8:65-8:67].</p> <p>“The circuits (pads) 42 G of the lower substrate 12 L, posts 86 of the interposer 12 M, and the circuits (pads) 42 F of the upper substrate 12 U are aligned (FIG. 12(A)). At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact. That allows the upper substrate 12 U and the lower substrate 12 L to be electrically connected via the interposer 12 M.” Furuta '669, [9:3-9:13].</p> <p>“The conductor layers 86 and the conductor layers 42 G, 42 F of each of the substrates may be connected with the use of solder, etc., as a conductive adhesive 88. At that time, when the upper substrate and the lower substrate are viewed with the center portion of the interposer as the axis, the circuit portions of the connection portions are set up set that they are of a mirror surface structure (top and bottom symmetrical structure).” Furuta '669, [9:13-9:20].</p> <p>“In addition, in lieu of resin fill, the both faces of the interposer 12 M could be coated with a resin 90, as illustrated in FIG. 11(G), such that the space between upper substrate 12 U and the lower substrate 12 L is sealed with said resin 90.” Furuta '669, [9:34-9:38].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Furuta '669 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The pads 42 F on the lower face side of the upper substrate 12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected with cylindrical metal posts 86 of the interposer 12 M.” Furuta '669, [7:51-7:55].</p> <p>“An insulating material 80 is prepared (FIG. 11(A)). Openings 82 penetrating the insulating material 80 are formed (FIG. 11 (B)), and a conductor layer 84 is formed in said openings 82 (FIG. 11(C)). The conductor layer 84 is formed by the through-hole, via, and post such as implant. For a conductor layer, a metal such as Cu, Ni, and a precious metal may be used.” Furuta '669, [8:20-8:26].</p> <p>“Implant material to constitute posts for implant is prepared. The thickness (height) thereof is preferably greater than that of the insulating substrate. A lower jig for the implant step is placed in advance underneath the implant material. At that time, an upper jig having a protrusion shape and for punching is placed over the implant material. The upper jig is punched part way down the implant material. The punched-out implant material is inserted and tapped into the openings 82 of the insulating substrate 80 which had been prepared such that the conductor layer (posts) 86 penetrating the insulating substrate is formed (FIG. 11(D)). Then, they are severed from the implant material and the height of a plurality of posts 86 protruding from the insulating substrate 80 is evened out. This allows the insulating substrate 80 being the interposer 12 M to make an electrical connection between the front and the back and to have conductor layer (posts) 86 being nearly the same in height of the protrusions off the insulating substrate 80.” Furuta '669, [8:39-8:56].</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

--	--

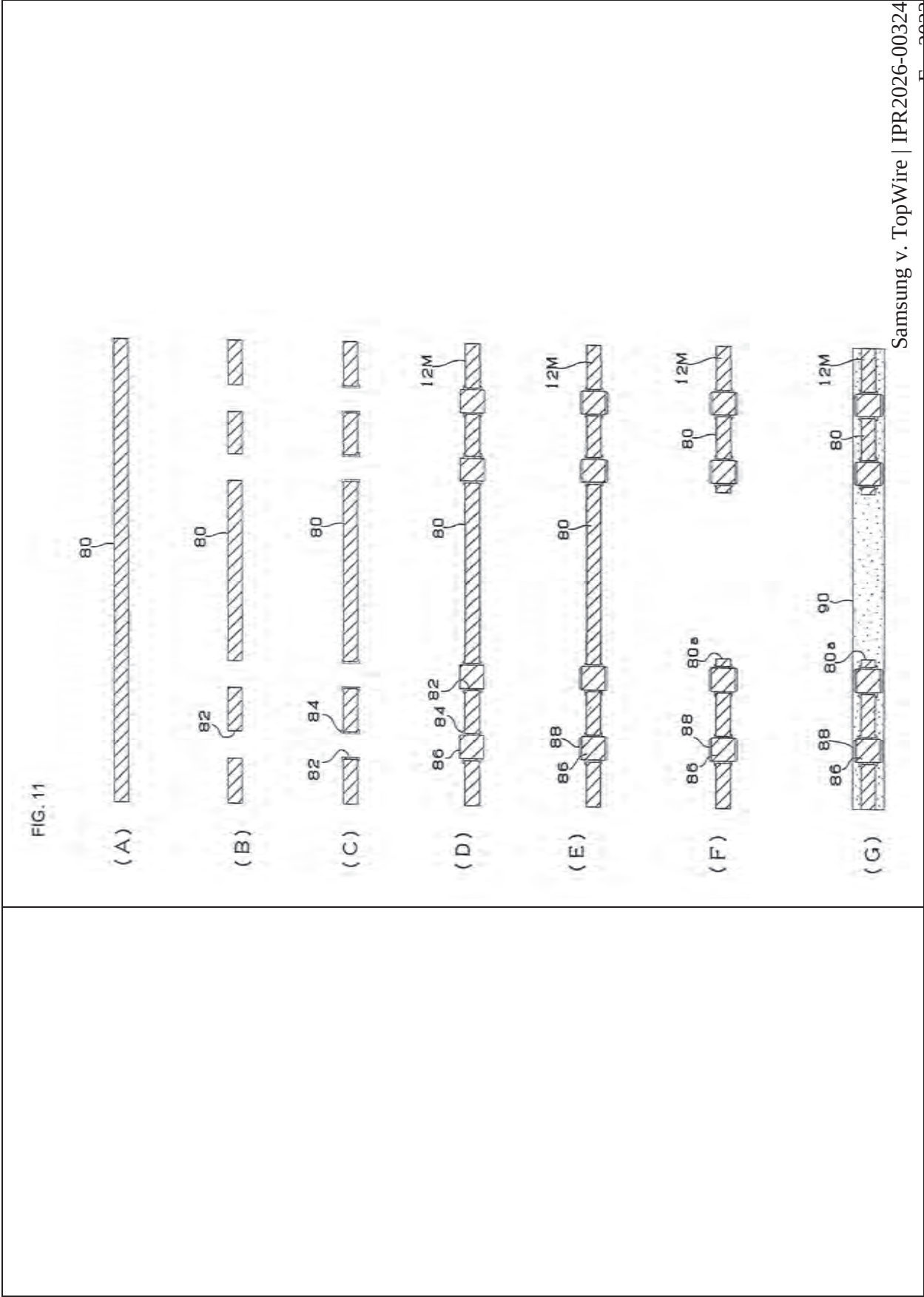


Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>Furuta, FIG. 11</p> <p>“This allows the insulating substrate 80 being the interposer 12 M to make an electrical connection between the front and the back and to have conductor layer (posts) 86 being nearly the same in height of the protrusions off the insulating substrate 80. At that time, an adhesive 88 may be applied, etc., as necessary, to affix the posts 86 being the conductor layer (FIG. 11(E)).” Furuta '669, [8:54-8:60].</p> <p>“The circuits (pads) 42 G of the lower substrate 12 L, posts 86 of the interposer 12 M, and the circuits (pads) 42 F of the upper substrate 12 U are aligned (FIG. 12(A)). At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact. That allows the upper substrate 12 U and the lower substrate 12 L to be electrically connected via the interposer 12 M.” Furuta '669, [9:3-9:13].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Furuta '669 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>“A plurality of IC chips may be mounted. In the opening portions 48 a in a solder resist 8 of the conductor circuits 42 a on the upper face side of the lower substrate 12L, there is formed a pad group of pads 42G for upper substrate connection. In the opening portions 48 a in a solder resist 48 of the conductor circuits 42 on the lower face side there is formed a pad group constituting pads 42D for printed wiring board connection.” Furuta '669, [3:8-3:15].</p> <p>“The punched-out implant material is inserted and tapped into the openings 82 of the insulating substrate 80 which had been prepared such that the conductor layer (posts) 86 penetrating the insulating substrate is formed (FIG. 11(D)). Then, they are severed from the implant material and the height of a plurality of posts 86 protruding from the insulating substrate 80 is evened out. This allows the insulating substrate 80 being the interposer 12M to make an electrical connection between the front and the back and to have conductor layer (posts) 86 being nearly the same in height of the protrusions off the insulating substrate 80. At that time, an adhesive 88 may be applied, etc., as necessary, to affix the posts 86 being the conductor layer (FIG. 11(E)). And, the tip portions of the conductor layer may undergo steps for improving anti-oxidation and the connection of the substrate with the conductor layer (roughened face formation, mirror surface treatment, etc.). Further, a via hole 80 a allowing an interference with the IC chip to be avoided could be formed (FIG. 11(F)). This allows the preparation of an interposer 12M to be sandwiched between the upper substrate and the lower substrate.” Furuta '669, [8:48-8:67].</p>
--	--

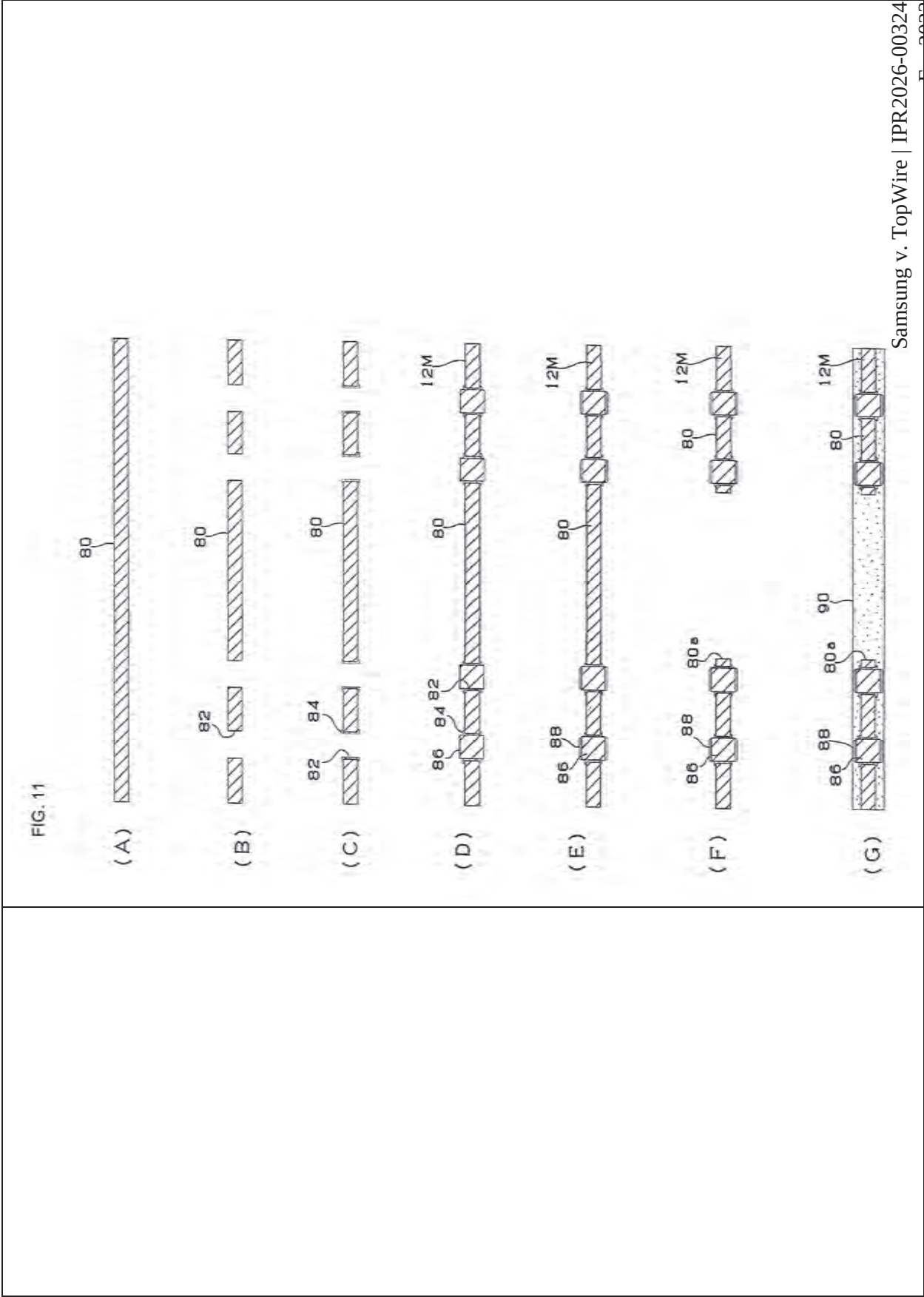


Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>Furuta, FIG. 11</p> <p>“The circuits (pads) 42G of the lower substrate 12L, posts 86 of the interposer 12M, and the circuits (pads) 42F of the upper substrate 12U are aligned (FIG. 12(A)). At that time, the circuit portions 42G of the lower substrate 12L and the conductor layers 86 of the interposer 12M are brought in mutual contact. The circuit portions 42F of the upper substrate 12U and the conductor layers 86 of the interposer 12M are brought in mutual contact. That allows the upper substrate 12U and the lower substrate 12L to be electrically connected via the interposer 12M. The conductor layers 86 and the conductor layers 42G, 42F of each of the substrates may be connected with the use of solder, etc., as a conductive adhesive 88. At that time, when the upper substrate and the lower substrate are viewed with the center portion of the interposer as the axis, the circuit portions of the connection portions are set up set that they are of a mirror surface structure (top and bottom symmetrical structure).” Furuta '669, [9:3-9:20].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Furuta '669 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>“The conductor layer 84 is formed by the through-hole, via, and post such as implant. For a conductor layer, a metal such as Cu, Ni, and a precious metal may be used.” Furuta ’669, [8:23-8:26].</p> <p>“An insulating substrate having on both faces a conductor layer formed with a copper foil, plating, etc., is prepared. Openings for penetration are provided in the insulating substrate with drilling or laser. Then, a resist layer is provided on the entirety of the face of the conductor layer, and a mask with the wiring pattern drawn thereon is placed. Following that, a pattern for the interposer is formed through an etching treatment after having undergone exposure and development. Then, a solder resist layer may be formed or the external shape may be treated (single-piece treatment of interposer), as necessary. This results in the preparation of an insulating substrate having openings for implant.” Furuta ’669, [8:28-8:40].</p> <p>“Implant material to constitute posts for implant is prepared. The thickness (height) thereof is preferably greater than that of the insulating substrate. A lower jig for the implant step is placed in advance underneath the implant material. At that time, an upper jig having a protrusion shape and for punching is placed over the implant material. The upper jig is punched part way down the implant material. The punched-out implant material is inserted and tapped into the openings 82 of the insulating substrate 80 which had been prepared such that the conductor layer (posts) 86 penetrating the insulating substrate is formed (FIG. 11(D)). Then, they are severed from the implant material and the height of a plurality of posts 86 protruding from the insulating substrate 80 is evened out. This allows the insulating substrate 80 being the interposer 12 M to make an electrical connection between the front and the back and to have conductor layer (posts) 86 being nearly the same in height of the protrusions off the insulating substrate 80.” Furuta ’669, [8:39-8:56].</p>
--	---

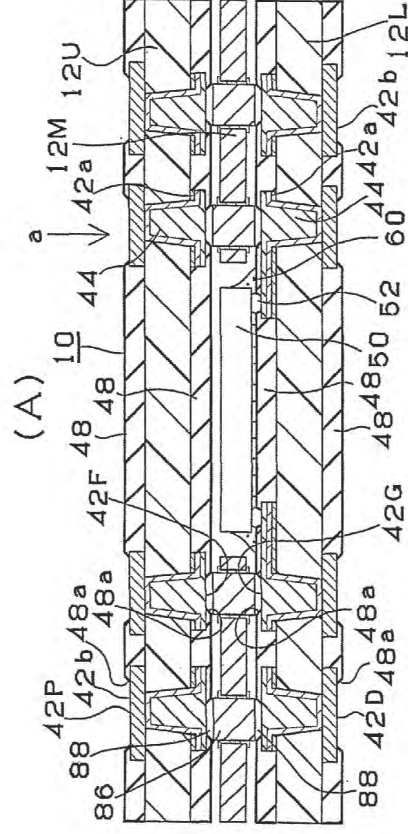


Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>Furuta, FIG. 11</p> <p>“Further, a via hole 80 a allowing an interference with the IC chip to be avoided could be formed (FIG. 11(F)). This allows the preparation of an interposer 12 M to be sandwiched between the upper substrate and the lower substrate.” Furuta '669, [8:64-8:67].</p> <p>“At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact.” Furuta '669, [9:5-9:10].</p> <p>“In addition, in lieu of resin fill, the both faces of the interposer 12 M could be coated with a resin 90, as illustrated in FIG. 11(G), such that the space between upper substrate 12 U and the lower substrate 12 L is sealed with said resin 90.” Furuta '669, [9:34-9:38].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Furuta '669 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

“Likewise, as to the lower substrate 12L the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected vias 44. In openings 48 a in the solder resist 48 on the conductor circuits 42 a on the lower face side of the upper substrate 12U there are formed pads 42F for the lower substrate connection, and in openings 48 a in the solder resist 48 on the conductor circuits 42 b on the upper face side there are formed pads 42P for package substrate connection. Between the lower substrate 12L and the IC chip 50 there is filled underfill 60 being an insulating resin, and between the upper substrate 12U and the lower substrate 12L there is filled a resin filler (underfill) 62. The pads 42F on the lower face side of the upper substrate 12U and the pads 42G on the upper face side of the lower substrate 12L are electrically connected with cylindrical metal posts 86 of the interposer 12M.” Furuta '669, [7:40-7:55].

FIG. 12



Furuta, FIG. 12

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

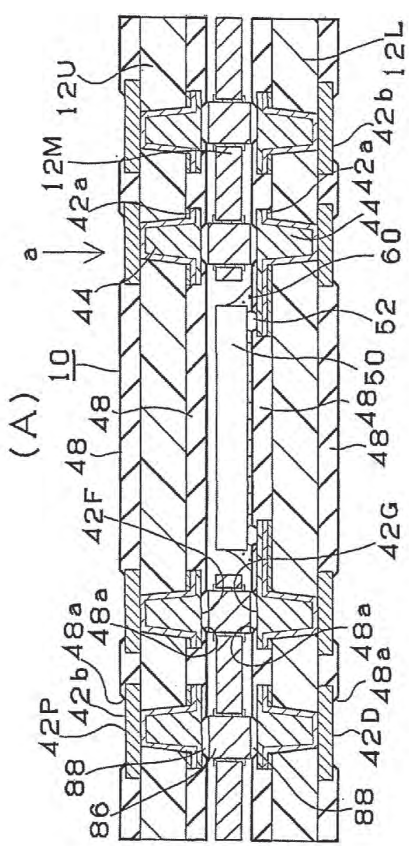
	<p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Furuta '669 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Likewise, as to the lower substrate 12L the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected vias 44. In openings 48 a in the solder resist 48 on the conductor circuits 42 a on the lower face side of the upper substrate 12U there are formed pads 42F for the lower substrate connection, and in openings 48 a in the solder resist 48 on the conductor circuits 42 b on the upper face side there are formed pads 42P for package substrate connection. Between the lower substrate 12L and the IC chip 50 there is filled underfill 60 being an insulating resin, and between the upper substrate 12U and the lower substrate 12L there is filled a resin filler (underfill) 62. The pads 42F on the lower face side of the upper substrate 12U and the pads 42G on the upper face side of the lower substrate 12L are electrically connected with cylindrical metal posts 86 of the interposer 12M.” Furuta '669, [7:40-7:55].</p>

	<p>FIG. 12</p> <p>Furuta, FIG. 12</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of the bottom package substrate.</p> <p>See, e.g.:</p>	<p>Furuta '669 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p>

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

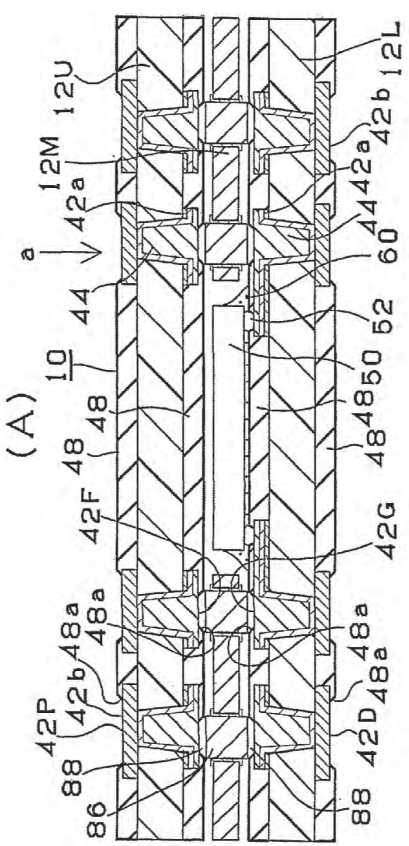
<p>top metal pillars of the bottom package substrate; and</p>	<p>“As to the lower substrate 12 L, conductor circuits 42 b on the lower face and conductor circuits 42 a on the upper face are connected via vias 44, and the IC chip 50 and the conductor circuits 42 a on the upper face are connected via solder bumps 52.” Furuta '669, [3:2-3:6].</p> <p>“Likewise, as to the upper substrate 12 U, the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected via vias 44. In the opening portions 42 a in the solder resist 48 of the conductor circuits 42 a on the lower face side of the upper substrate 12 U there is formed a pad group of pads 42 F for lower substrate connection, and in the opening portions 48 a in the solder resist 48 of the conductor circuits 42 b on the upper face side there is formed a pad group of pads 42 P for package substrate connection.” Furuta '669, [3:16-3:25].</p> <p>“The pads 42 F on the lower face side of the upper substrate 12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected via cylindrical metal posts 46, 46.” Furuta '669, [3:31-3:34].</p> <p>“On the pads 42 E of the lower substrate 12 L for connecting with the IC chip there is formed a solder layer 61 for solder bumps (FIG. 3(B)). The solder layer is preferably formed with printing, etc. With the solder bumps 52 thereof and the metal bumps formed on the IC chip the IC chip 50 is flip-chip mounted through reflow (FIG. 3(C)).” Furuta '669, [5:30-5:35].</p> <p>“Then, the conductor circuits (pads) 42 G of the lower substrate 12 L and the conductor circuits (pads) 42 F of the upper substrate 12 U are connected via the posts 46, 46 by reflow.” Furuta '669, [5:56-5:58].</p>
---	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>“The circuits (pads) 42 G of the lower substrate 12 L, posts 86 of the interposer 12 M, and the circuits (pads) 42 F of the upper substrate 12 U are aligned (FIG. 12(A)). At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact. That allows the upper substrate 12 U and the lower substrate 12 L to be electrically connected via the interposer 12 M.” Furuta '669, [9:3-9:12].</p> <p>FIG. 12</p>  <p>Furuta, FIG. 12</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Furuta '669 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“On the upper face of the lower substrate 12 L there is mounted an IC chip 50. As to the lower substrate 12 L, conductor circuits 42 b on the lower face and conductor circuits 42 a on the upper face are connected via vias 44, and the IC chip 50 and the conductor circuits 42 a on the upper face are connected via solder bumps 52. In this case, the IC chip 50 may be mounted by other mounting configurations (wire bonding mounting, for example). A plurality of IC chips may be mounted. In the opening portions 48 a in a solder resist 8 of the conductor circuits 42 a on the upper face side of the lower substrate 12 L there is formed a pad group of pads 42 G for upper substrate connection. In the opening portions 48 a in a solder resist 48 of the conductor circuits 42 on the lower face side there is formed a pad group constituting pads 42 D for printed wiring board connection. Likewise, as to the upper substrate 12 U, the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected via vias 44. In the opening portions 42 a in the solder resist 48 of the conductor circuits 42 a on the lower face side of the upper substrate 12 U there is formed a pad group of pads 42 F for lower substrate connection, and in the opening portions 48 a in the solder resist 48 of the conductor circuits 42 b on the upper face side there is formed a pad group of pads 42 P for package substrate connection. Between the lower substrate 12 L and the IC chip 50 there is filled an insulating resin such as an underfill 60 such as an epoxy resin, and between the upper substrate 12 U and the lower substrate 12 L</p>

	<p>there is filled an insulating resin being a resin filler agent (underfill) 62.” Furuta ’669, [3:1-3:29].</p> <p>FIG. 12</p>  <p>Furuta, FIG. 12</p> <p>“Formation of Lower Substrate Steps 1 through 5 for the upper substrate apply likewise. 6. A solder layer 49 is formed on metal posts 46 (FIG. 3(A)). A solder layer 49 may be formed with solder plating, printing, transfer method, etc. For solder, a metal with Sn/Pb, Sn/Ag, Sn/Sb, Sn/Ag/Cu, etc., as a principal component may be used. As an example of the formation of a solder layer, electroless solder plating may be mentioned. After those other than the posts are coated with a resist, etc., such that a solder layer would not be formed, a catalyst such as Pd is added to the posts. Then, it is immersed in a plating solution with Sn/Pb being 9:1 and containing therein a reducer and a complex.” Furuta ’669, [5:8-5:20].</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>“FIG. 7 illustrates a combination substrate pertaining to Revised Example 1. With Example 1, an IC chip 50 was mounted on the upper face of the lower substrate 12 L as illustrated in FIG. 5(B). In lieu of this, an IC chip may also be mounted on the lower face of the upper substrate 12 U, as illustrated in FIG. 7.” Furuta ’669, [6:66-7:4].</p> <p>“Likewise, as to the lower substrate 12 L the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected vias 44. In openings 48 a in the solder resist 48 on the conductor circuits 42 a on the lower face side of the upper substrate 12 U there are formed pads 42 F for the lower substrate connection, and in openings 48 a in the solder resist 48 on the conductor circuits 42 b on the upper face side there are formed pads 42 P for package substrate connection. Between the lower substrate 12 L and the IC chip 50 there is filled underfill 60 being an insulating resin, and between the upper substrate 12 U and the lower substrate 12 L there is filled a resin filler (underfill) 62.” Furuta ’669, [7:40-7:51].</p> <p>“Then, with the mounting step for the IC chip 50 having been performed, the lower substrate 12 L with the IC chip 50 mounted can be obtained (FIG. 10(B), FIG. 10(C)).” Furuta ’669, [8:16-8:18].</p> <p>“FIG. 15 illustrates a combination substrate pertaining to Revised Example 1 of Example 2. With Example 2, an IC chip 50 was mounted on the upper face of the lower substrate 12 L as illustrated in FIG. 13(A). In lieu of this, an IC chip may also be mounted on the lower face of the upper substrate 12 U, as illustrated in FIG. 15.” Furuta ’669, [10:14-10:19].</p> <p>To the extent Plaintiff contends that Furuta ’669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Furuta '669 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“On the upper face of the lower substrate 12 L there is mounted an IC chip 50. As to the lower substrate 12 L, conductor circuits 42 b on the lower face and conductor circuits 42 a on the upper face are connected via vias 44, and the IC chip 50 and the conductor circuits 42 a on the upper face are connected via solder bumps 52.” Furuta '669, [3:1-3:6].</p> <p>FIG. 12</p>

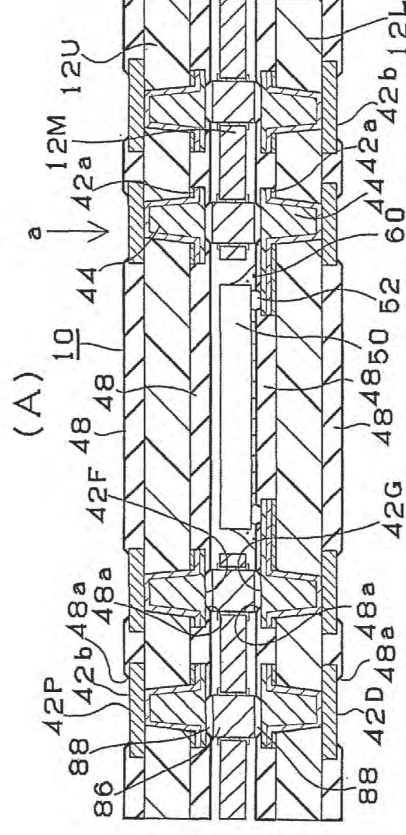
Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>Furuta, FIG. 12</p> <p>“Between the lower substrate 12 L and the IC chip 50 there is filled an insulating resin such as an underfill 60 such as an epoxy resin, and between the upper substrate 12 U and the lower substrate 12 L there is filled an insulating resin being a resin filler agent (underfill) 62.” Furuta '669, [3:25-3:29].</p> <p>“On the pads 42 E of the lower substrate 12 L for connecting with the IC chip there is formed a solder layer 61 for solder bumps (FIG. 3(B)). The solder layer is preferably formed with printing, etc. With the solder bumps 52 thereof and the metal bumps formed on the IC chip the IC chip 50 is flip-chip mounted through reflow (FIG. 3(C)). Then, the underfill 60 is filled in a gap between the IC chip 50 and the lower substrate 12 L (FIG. 3(D)).” Furuta '669, [5:30-5:37].</p> <p>“On the upper face of the lower substrate 12 L there is mounted an IC chip 50. As to the lower substrate 12 L conductor circuits 42 b on the lower face side and conductor circuits 42 a on the upper face side are connected vias 44, and the IC chip 50 and the conductor circuits 42 b on the upper face side are connected via solder bumps 52.” Furuta '669, [7:27-7:32].</p> <p>“Then, with the mounting step for the IC chip 50 having been performed, the lower substrate 12 L with the IC chip 50 mounted can be obtained (FIG. 10(B), FIG. 10(C)).” Furuta '669, [8:16-8:18].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Furuta '669 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 12(A) illustrates a sectional view of the combination substrate 10 in accordance with Example 2. The combination substrate 10 comprises an upper substrate 12U, an interposer 12M being an intermediate material, and a lower substrate 12L. On the upper substrate 12U, a pad group of pads 42P for package substrate connection is disposed in the center region of the upper substrate 12U, as illustrated in the plan view of FIG. 14(A) corresponding to the arrow directional view in FIG. 12(A). On the lower substrate 12L there is likewise formed a pad group of pads 42D to connect to a printed wiring board. On the upper face of the lower substrate 12L there is mounted an IC chip 50. As to the lower substrate 12 L conductor circuits 42 b on the lower face side and conductor circuits 42 a on the upper face side are connected vias 44, and the IC chip 50 and the conductor circuits 42 b on the upper face side are connected via solder bumps 52. In openings 48 a in a solder resist 48 on the conductor circuits 42 a on the upper face side of the lower substrate 12L there are formed pads 42G for the upper substrate connection, and in openings 48 a in a solder resist 48 on conductor circuits 42 b on the lower face side there are formed a pad group of pads 42D for printed wiring substrate connection.” Furuta '669, [7:17-7:39].</p>
--	--

FIG. 12



Furuta, FIG. 12

“An insulating material 80 is prepared (FIG. 11(A)). Openings 82 penetrating the insulating material 80 are formed (FIG. 11(B)), and a conductor layer 84 is formed in said openings 82 (FIG. 11(C)). The conductor layer 84 is formed by the through-hole, via, and post such as implant. For a conductor layer, a metal such as Cu, Ni, and a precious metal may be used.” Furuta ’669, [8:20-8:26].

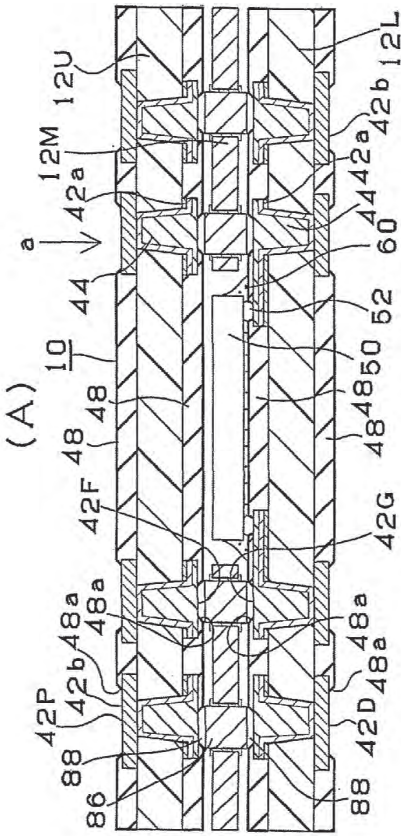
“Further, a via hole 80 allowing an interference with the IC chip to be avoided could be formed (FIG. 11(F)). This allows the preparation of an interposer 12M to be sandwiched between the upper substrate and the lower substrate.” Furuta ’669, [8:64-8:67].

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Furuta '669 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Between the lower substrate 12 L and the IC chip 50 there is filled an insulating resin such as an underfill 60 such as an epoxy resin, and between the upper substrate 12 U and the lower substrate 12 L there is filled an insulating resin being a resin filler agent (underfill) 62.” Furuta '669, [3:25-3:29].</p> <p>“Further, as illustrated in FIG. 6(F), on the upper substrate 12 U there may also be provided pads 43 for electronic component mounting along with pads 42 P. It allows a package substrate on which an IC chip is mounted and a passive component such as a capacitor to be mix-loaded on the upper substrate.” Furuta '669, [6:60-6:65].</p> <p>“FIG. 7 illustrates a combination substrate pertaining to Revised Example 1 of Example 1. With Example 1, an IC chip 50 was mounted on the upper face of the lower substrate 12 L</p>

	<p>as illustrated in FIG. 5(B). In lieu of this, an IC chip may also be mounted on the lower face of the upper substrate 12 U, as illustrated in FIG. 7.” Furuta ’669, [6:66-7:4].</p> <p>“Between the lower substrate 12 L and the IC chip 50 there is filled underfill 60 being an insulating resin, and between the upper substrate 12 U and the lower substrate 12 L there is filled a resin filler (underfill) 62.” Furuta ’669, [7:48-7:51].</p> <p>“Further, a via hole 80 a allowing an interference with the IC chip to be avoided could be formed (FIG. 11(F)). This allows the preparation of an interposer 12 M to be sandwiched between the upper substrate and the lower substrate. C. Formation of Laminate Substrate 1.” Furuta ’669, [8:64-9:2].</p> <p>FIG. 12</p>  <p>Furuta, FIG. 12</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

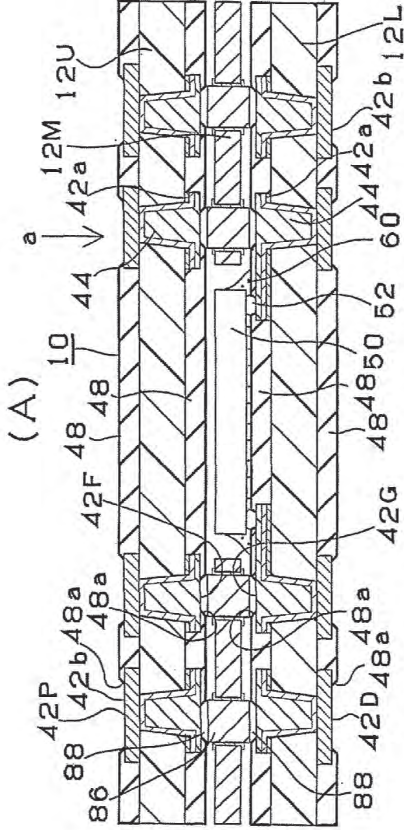
	<p>“FIG. 15 illustrates a combination substrate pertaining to Revised Example 1 of Example 2. With Example 2, an IC chip 50 was mounted on the upper face of the lower substrate 12 L as illustrated in FIG. 13(A). In lieu of this, an IC chip may also be mounted on the lower face of the upper substrate 12 U, as illustrated in FIG. 15.” Furuta '669, [10:14-10:19].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Furuta '669 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“On the upper substrate 12 U there are disposed a pad group of pads for package substrate connection 42 P on the center portion of the upper substrate 12 U, as illustrated in the plan view of FIG. 6(A) corresponding to the a arrow directional view in FIG. 4(A). On the lower substrate 12 L there is likewise formed a pad group for external connection such as the BGA</p>

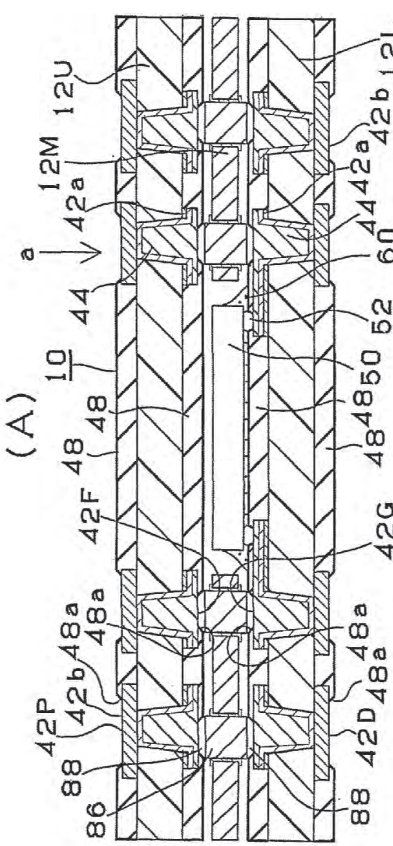
Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>of pads 42 D for connecting to another printed wiring board. On the upper face of the lower substrate 12 L there is mounted an IC chip 50.” Furuta ’669, [2:61-3:2].</p> <p>“On the pad group of the pads 42 P on the upper portion of the upper substrate 12 U, a package substrate 70 with an IC chip 71 embedded therein or mounted thereon may be mounted (FIG. 5 (A)). That provides a laminate package substrate structure having two or more IC chips 50, 71.” Furuta ’669, [6:18-6:23].</p> <p>“And, it can be connected to the pads 72, 76 of the package substrate 70 and the printed wiring board 74 via solder bumps 64 U, 64 L or a BGA formed on the pad group of the pads 42 P, 42 D of the upper substrate 12 U and the lower substrate 12 L, allowing said combination substrate 10 to be connected to the package substrate 70 and the printed wiring substrate 74 (FIG. 5 (B)).” Furuta ’669, [6:25-6:31].</p> <p>“On the upper substrate 12 U, a pad group of pads 42 P for package substrate connection is disposed in the center region of the upper substrate 12 U, as illustrated in the plan view of FIG. 14(A) corresponding to the arrow directional view in FIG. 12(A). On the lower substrate 12 L there is likewise formed a pad group of pads 42 D to connect to a printed wiring board. On the upper face of the lower substrate 12 L there is mounted an IC chip 50.” Furuta ’669, [7:21-7:28].</p> <p>“As necessary, solder bumps 64 L may be formed on the pads 42 D of the lower substrate 12 L (FIG. 12(B)). On the pad group of the pads 42 P on the upper portion of the upper substrate 12 U, a package substrate 70 with an IC chip 71 embedded therein or mounted thereon may be mounted (FIG. 13(A)).” Furuta ’669, [9:39-9:44].</p>
--	--

	<p>“On the pad group of the pads 42 P on the upper portion of the upper substrate 12 U, a package substrate 70 with an IC chip 71 embedded therein or mounted thereon may be mounted (FIG. 13(A)). That provides a laminate package substrate structure having two or more IC chips 50, 71.” Furuta '669, [9:40-9:45].</p> <p>FIG. 12</p>  <p>Furuta, FIG. 12</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p>	<p>Furuta '669 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The pads 42 F on the lower face side of the upper substrate 12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected via cylindrical metal posts 46, 46. On the pads 42 D on the lower face side of the combination substrate 10 there are provided external connection terminals 64 L such as BGA and solder bumps, and by their being connected to pads 76 of another printed wiring board 74 as illustrated in FIG. 5(B) said combination substrate 10 is loaded onto the printed wiring board 74.” Furuta '669, [3:31-3:40].</p> <p>“The circuits (pads) 42 G of the lower substrate 12 L and the circuits (pads) 42 F of the upper substrate 12 U are aligned. At that time, the joining is done such that the posts 46 of the upper substrate 12 U are pressed onto the posts 46 of the lower substrate 12 L, on which solder 49 is formed (FIG. 3(E)). Then, the conductor circuits (pads) 42 G of the lower substrate 12 L and the conductor circuits (pads) 42 F of the upper substrate 12 U are connected via the posts 46, 46 by reflow.” Furuta '669, [5:51-5:58].</p>

	<p>“The pads 42 F on the lower face side of the upper substrate 12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected with cylindrical metal posts 86 of the interposer 12 M.” Furuta '669, [7:51-7:55].</p> <p>“The circuits (pads) 42 G of the lower substrate 12 L, posts 86 of the interposer 12 M, and the circuits (pads) 42 F of the upper substrate 12 U are aligned (FIG. 12(A)). At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact. That allows the upper substrate 12 U and the lower substrate 12 L to be electrically connected via the interposer 12 M.” Furuta '669, [9:3-9:13].</p> <p>FIG. 12</p>  <p>Furuta, FIG. 12</p>
--	---

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>“At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact.” Furuta '669, [9:5-9:10].</p> <p>“The conductor layers 86 and the conductor layers 42 G, 42 F of each of the substrates may be connected with the use of solder, etc., as a conductive adhesive 88.” Furuta '669, [9:13-9:15].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	Furuta '669 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

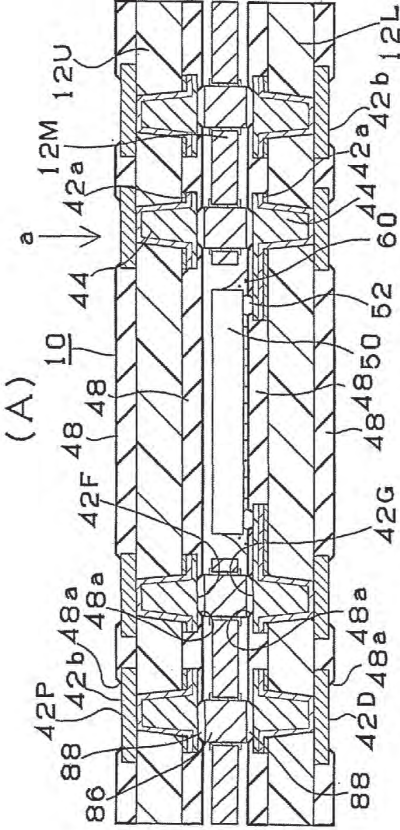
Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

<p>the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p><i>See, e.g.:</i></p> <p>“FIG. 12(A) illustrates a sectional view of the combination substrate 10 in accordance with Example 2. The combination substrate 10 comprises an upper substrate 12 U, an interposer 12 M being an intermediate material, and a lower substrate 12 L. On the upper substrate 12 U, a pad group of pads 42 P for package substrate connection is disposed in the center region of the upper substrate 12 U, as illustrated in the plan view of FIG. 14(A) corresponding to the arrow directional view in FIG. 12(A). On the lower substrate 12 L there is likewise formed a pad group of pads 42 D to connect to a printed wiring board. On the upper face of the lower substrate 12 L there is mounted an IC chip 50. As to the lower substrate 12 L conductor circuits 42 b on the lower face side and conductor circuits 42 a on the upper face side are connected vias 44, and the IC chip 50 and the conductor circuits 42 b on the upper face side are connected via solder bumps 52. In openings 48 a in a solder resist 48 on the conductor circuits 42 a on the upper face side of the lower substrate 12 L there are formed pads 42 G for the upper substrate connection, and in openings 48 a in a solder resist 48 on conductor circuits 42 b on the lower face side there are formed a pad group of pads 42 D for printed wiring substrate connection. Likewise, as to the lower substrate 12 L the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected vias 44. In openings 48 a in the solder resist 48 on the conductor circuits 42 a on the lower face side of the upper substrate 12 U there are formed pads 42 F for the lower substrate connection, and in openings 48 a in the solder resist 48 on the conductor circuits 42 b on the upper face side there are formed pads 42 P for package substrate connection. Between the lower substrate 12 L and the IC chip 50 there is filled underfill 60 being an insulating resin, and between the upper substrate 12 U and the lower substrate 12 L there is filled a resin filler (underfill) 62. The pads 42 F on the lower face side of the upper substrate 12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected with cylindrical metal posts 86 of the interposer 12 M.” Furuta '669, [7:17-7:56].</p>
--	---

“Formation of an Interposer An insulating material 80 is prepared (FIG. 11(A)). Openings 82 penetrating the insulating material 80 are formed (FIG. 11 (B)), and a conductor layer 84 is formed in said openings 82 (FIG. 11(C)). The conductor layer 84 is formed by the through-hole, via, and post such as implant. For a conductor layer, a metal such as Cu, Ni, and a precious metal may be used. As an example therefor, a method of filling a post with an implant is available. An insulating substrate having on both faces a conductor layer formed with a copper foil, plating, etc., is prepared. Openings for penetration are provided in the insulating substrate with drilling or laser. Then, a resist layer is provided on the entirety of the face of the conductor layer, and a mask with the wiring pattern drawn thereon is placed. Following that, a pattern for the interposer is formed through an etching treatment after having undergone exposure and development. Then, a solder resist layer may be formed or the external shape may be treated (single-piece treatment of interposer), as necessary. This results in the preparation of an insulating substrate having openings for implant. Implant material to constitute posts for implant is prepared. The thickness (height) thereof is preferably greater than that of the insulating substrate. A lower jig for the implant step is placed in advance underneath the implant material. At that time, an upper jig having a protrusion shape and for punching is placed over the implant material. The upper jig is punched part way down the implant material. The punched-out implant material is inserted and tapped into the openings 82 of the insulating substrate 80 which had been prepared such that the conductor layer (posts) 86 penetrating the insulating substrate is formed (FIG. 11(D)). Then, they are severed from the implant material and the height of a plurality of posts 86 protruding from the insulating substrate 80 is evened out. This allows the insulating substrate 80 being the interposer 12 M to make an electrical connection between the front and the back and to have conductor layer (posts) 86 being nearly the same in height of the protrusions off the insulating substrate 80.” Furuta ’669, [8:19-8:58].

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>“At that time, an adhesive 88 may be applied, etc., as necessary, to affix the posts 86 being the conductor layer (FIG. 11(E)). And, the tip portions of the conductor layer may undergo steps for improving anti-oxidation and the connection of the substrate with the conductor layer (roughened face formation, mirror surface treatment, etc.)” Furuta ’669, [8:58-8:64].</p> <p>“Formation of Laminate Substrate 1. Alignment of Lower Substrate and Upper Substrate The circuits (pads) 42 G of the lower substrate 12 L, posts 86 of the interposer 12 M, and the circuits (pads) 42 F of the upper substrate 12 U are aligned (FIG. 12(A)). At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact. That allows the upper substrate 12 U and the lower substrate 12 L to be electrically connected via the interposer 12 M. The conductor layers 86 and the conductor layers 42 G, 42 F of each of the substrates may be connected with the use of solder, etc., as a conductive adhesive 88.” Furuta ’669, [9:1-9:15].</p>
--	---

	<p>FIG. 12</p>  <p>Furuta, FIG. 12</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the	Furuta '669 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the

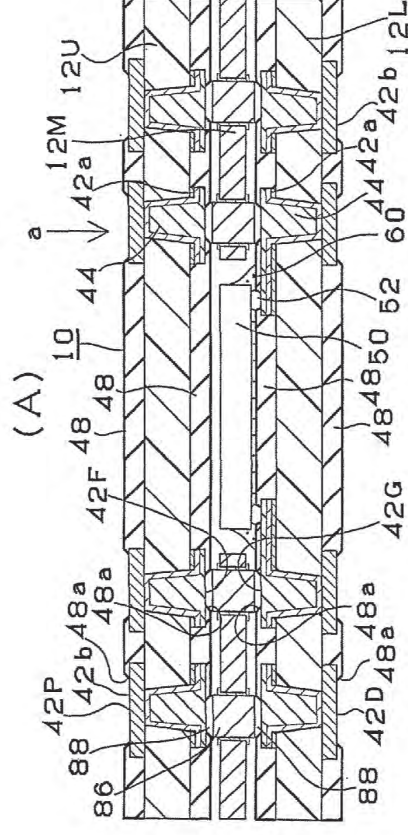
Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

<p>plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In the opening portions 48 a in a solder resist 8 of the conductor circuits 42 a on the upper face side of the lower substrate 12 L there is formed a pad group of pads 42 G for upper substrate connection. In the opening portions 48 a in a solder resist 48 of the conductor circuits 42 on the lower face side there is formed a pad group constituting pads 42 D for printed wiring board connection. Likewise, as to the upper substrate 12 U, the conductor circuits 42 a on the lower face side and the conductor circuits 42 b on the upper face side are connected via vias 44. In the opening portions 42 a in the solder resist 48 of the conductor circuits 42 a on the lower face side of the upper substrate 12 U there is formed a pad group of pads 42 F for lower substrate connection, and in the opening portions 48 a in the solder resist 48 of the conductor circuits 42 b on the upper face side there is formed a pad group of pads 42 P for package substrate connection.” Furuta '669, [3:9-3:25].</p> <p>“The pads 42 F on the lower face side of the upper substrate 12 U and the pads 42 G on the upper face side of the lower substrate 12 L are electrically connected with cylindrical metal posts 86 of the interposer 12 M.” Furuta '669, [7:51-7:55].</p> <p>“C. Formation of an Interposer An insulating material 80 is prepared (FIG. 11(A)). Openings 82 penetrating the insulating material 80 are formed (FIG. 11 (B)), and a conductor layer 84 is formed in said openings 82 (FIG. 11(C)). The conductor layer 84 is formed by the through-</p>
--	--

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>hole, via, and post such as implant. For a conductor layer, a metal such as Cu, Ni, and a precious metal may be used.” Furuta ’669, [8:19-8:26].</p> <p>“Then, a solder resist layer may be formed or the external shape may be treated (single-piece treatment of interposer), as necessary. This results in the preparation of an insulating substrate having openings for implant. Implant material to constitute posts for implant is prepared. The thickness (height) thereof is preferably greater than that of the insulating substrate. A lower jig for the implant step is placed in advance underneath the implant material. At that time, an upper jig having a protrusion shape and for punching is placed over the implant material. The upper jig is punched part way down the implant material. The punched-out implant material is inserted and tapped into the openings 82 of the insulating substrate 80 which had been prepared such that the conductor layer (posts) 86 penetrating the insulating substrate is formed (FIG. 11(D)). Then, they are severed from the implant material and the height of a plurality of posts 86 protruding from the insulating substrate 80 is evened out. This allows the insulating substrate 80 being the interposer 12 M to make an electrical connection between the front and the back and to have conductor layer (posts) 86 being nearly the same in height of the protrusions off the insulating substrate 80. At that time, an adhesive 88 may be applied, etc., as necessary, to affix the posts 86 being the conductor layer (FIG. 11(E)). And, the tip portions of the conductor layer may undergo steps for improving anti-oxidation and the connection of the substrate with the conductor layer (roughened face formation, mirror surface treatment, etc.).” Furuta ’669, [8:37-8:64].</p>
--	---

FIG. 12



Furuta, FIG. 12

“Formation of Laminate Substrate 1. Alignment of Lower Substrate and Upper Substrate The circuits (pads) 42 G of the lower substrate 12 L, posts 86 of the interposer 12 M, and the circuits (pads) 42 F of the upper substrate 12 U are aligned (FIG. 12(A)). At that time, the circuit portions 42 G of the lower substrate 12 L and the conductor layers 86 of the interposer 12 M are brought in mutual contact. The circuit portions 42 F of the upper substrate 12 U and the conductor layers 86 of the interposer 12 M are brought in mutual contact. That allows the upper substrate 12 U and the lower substrate 12 L to be electrically connected via the interposer 12 M. The conductor layers 86 and the conductor layers 42 G, 42 F of each of the substrates may be connected with the use of solder, etc., as a conductive adhesive 88.” Furuta ’669, [9:1-9:15].

Appendix A-7 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '669 - U.S. Patent No. 8618669

	<p>“At that time, when the upper substrate and the lower substrate are viewed with the center portion of the interposer as the axis, the circuit portions of the connection portions are set up set that they are of a mirror surface structure (top and bottom symmetrical structure).” Furuta '669, [9:15-9:20].</p> <p>To the extent Plaintiff contends that Furuta '669 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

U.S. Patent Publication No. 20090140415 (“Furuta '415”) is titled Combination Substrate and lists Toru Furuta as inventor. Furuta '415 is assigned to Iriden Co., Ltd. Furuta '415 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the '202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff's apparent infringement theory.² Furuta '415 is a U.S. patent publication that was filed June 27, 2008 and published June 27, 2008. Furuta '415 claims priority to a provisional application filed on November 29, 2007. Furuta '415 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Furuta '415, or otherwise rendered obvious by disclosures and teachings of Furuta '415, including under TopWire's apparent interpretation of the Asserted Claims as Samsung understands them from TopWire's Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Furuta '415 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Furuta '415 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung's other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung's Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Furuta '415, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire's March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court's order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire's apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung's interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Furuta '415 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Furuta '415 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Furuta '415 set forth in this chart.

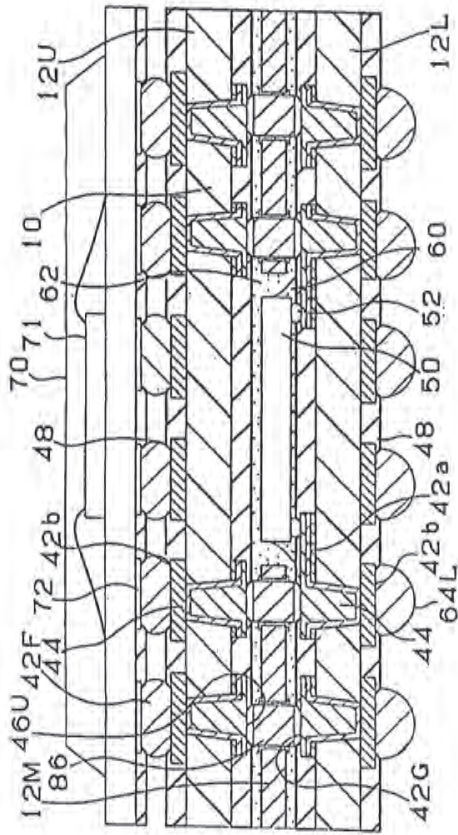
Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Furuta '415 discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 6(A) shows a cross-sectional view of combination substrate 10 according to Example 1. Combination substrate 10 is structured with upper substrate (12 U), interposer (12 M) as an intermediate and lower substrate (12 L). On upper substrate (12 U), as shown in the plan view in FIG. 7(A) equivalent to a fragmentary view taken from the direction (a) in FIG. 6(A), a group of pads (42 P) for connection to a package substrate is arranged in the center portion of upper substrate (12 U). Likewise, on lower substrate (12 L), a group of pads (42 D) for</p>

	<p>connection to a printed wiring board is formed. On the top surface of lower substrate (12 L), IC chip 50 is mounted. At lower substrate (12 L), conductive circuit (42 b) on the bottom surface and conductive circuit (42 a) on the top surface are connected through vias 44, and IC chip 50 and conductive circuit (42 b) on the top surface are connected through solder bumps 52. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the top surface of lower substrate (12 L), pads (42 G) for connection to the upper substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the bottom surface, a group of pads (42 D) for connection to a printed wiring board substrate is formed. In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the bottom surface of upper substrate (12 U), pads (42 F) for connection to the lower substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the top surface, pads (42 P) for connection to a package substrate are formed. Between lower substrate (12 L) and IC chip 50, insulative resin underfill 60 is filled; and between upper substrate (12 U) and lower substrate (12 L), resin filling agent 62 is filled. Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta ’415, [0020-0021].</p>
--	--

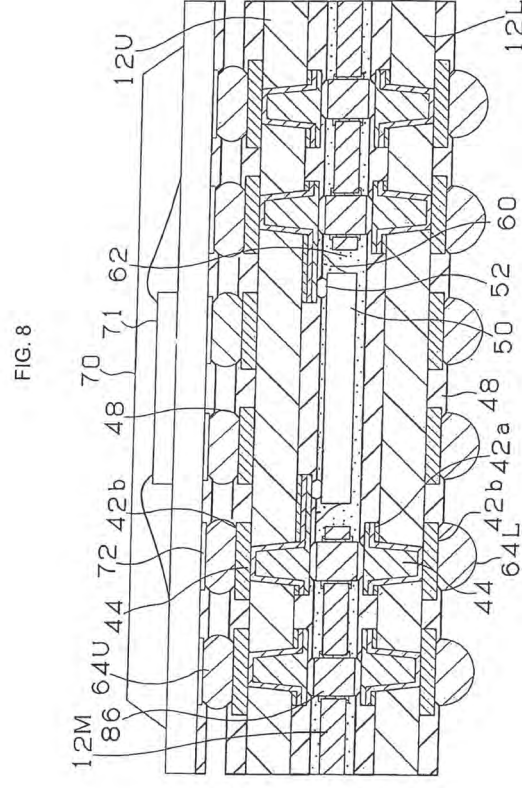
FIG. 6

(A)



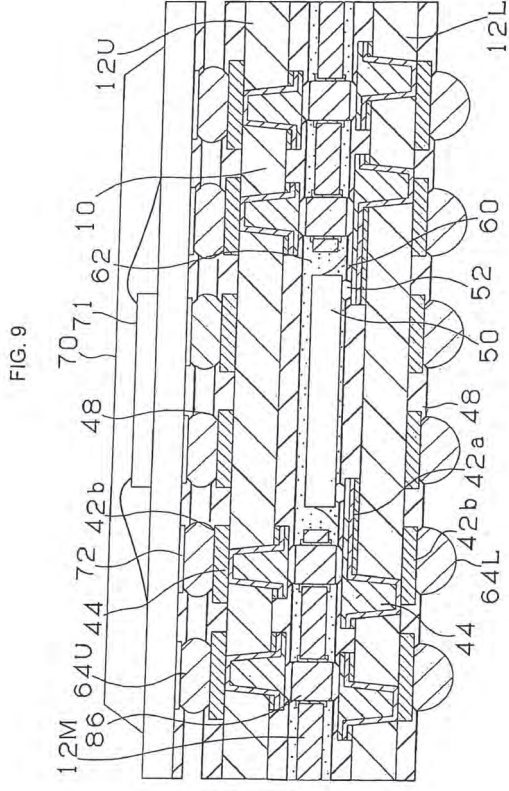
Furuta '415, FIG. 6

“FIG. 8 shows a combination substrate according to Modification 1 to Example 1. In Example 1, as shown in FIG. 6(A), IC chip 50 was mounted on the top surface of lower substrate (12 L). Instead, as shown in FIG. 8, IC chip 50 may also be mounted on the bottom surface of upper substrate (12 U).” Furuta '415, [0047].



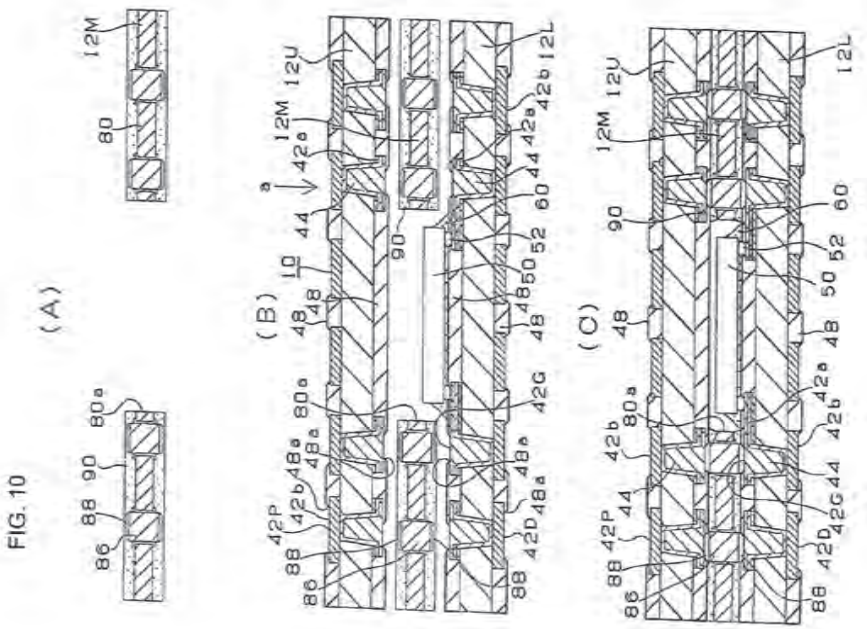
Furuta '415, FIG. 8

“FIG. 9 shows a combination substrate according to Modification 2 to Example 1. In Example 1, upper substrate (12 U) and lower substrate (12 L) are arranged in a mirror image structure. Instead, as shown in FIG. 9, vias 66 and circuit (42 b) of lower substrate (12 L) may be arranged so as to spread toward the periphery (fan out).” Furuta ‘415, [0048].



Furuta '415, FIG. 9

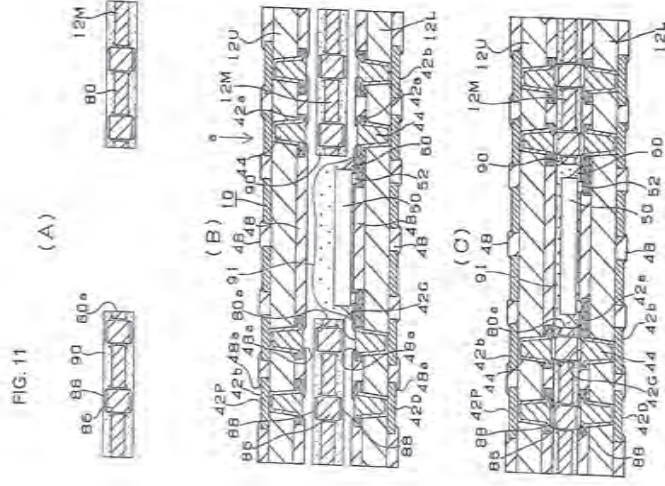
“FIG. 10 show a combination substrate according to Example 2. In Example 1, interiors of open holes (80 a) of interposer (12 M) are filled with underfill 62 or resin 90. In contrast, as shown in FIG. 10(C), Example 2 has a structure so as not to fill the interiors of open holes (80 a) of interposer (12 M) with resin 90. Here, since the interiors of open holes (80 a) of interposer (12 M) are not filled with resin 90, occurrence of cracks at the interface (especially at the corners of the IC chip) between lower substrate (12 L) and mounted IC chip 50 may be suppressed.” Furuta '415, [0049].



Furuta '415, FIG. 10

“FIG. 11 show a combination substrate according to Modification 1 to Example 1 to Example 2. Example 2, as described above with reference to FIG. 10(C), was structured so as not to fill the interiors

of open holes (80 a) of interposer (12 M) with underfill 90. In contrast, according to Modification 1 to Example 2, the interiors of open holes (80 a) are filled with resin 91 which is less elastic than the underfill." Furuta '415, [0051].



Furuta '415, FIG. 11

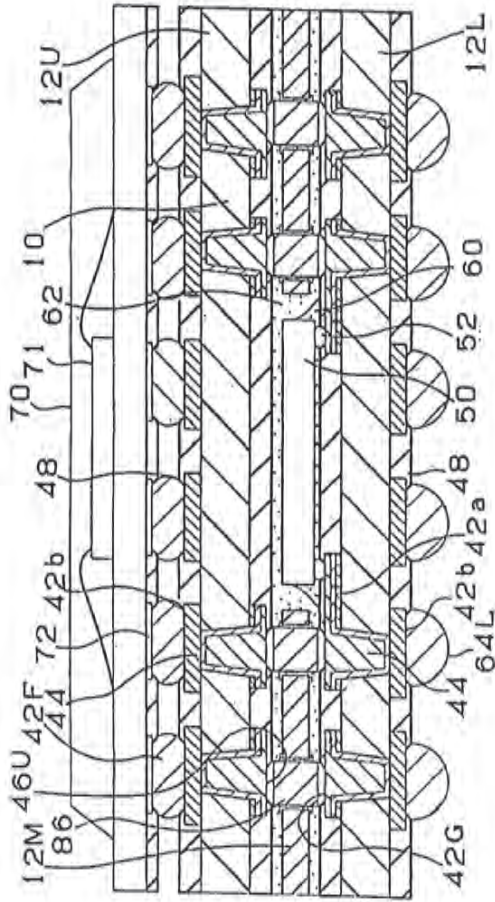
“According to the foregoing embodiments of the present invention, a combination substrate is structured with a lower substrate which is to be installed on a printed wiring board, and an upper substrate which is to be installed on the upper surface of the lower substrate and on

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>which to mount a package substrate; and on the surface of the lower substrate facing the upper substrate, or on the surface of the upper substrate facing the lower substrate, a die is mounted.” Furuta ’415, [0053].</p>
<p>[1.A] a bottom package substrate;</p>	<p>Furuta ’415 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“At lower substrate (12 L), conductive circuit (42 b) on the bottom surface and conductive circuit (42 a) on the top surface are connected through vias 44, and IC chip 50 and conductive circuit (42 b) on the top surface are connected through solder bumps 52. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the top surface of lower substrate (12 L), pads (42 G) for connection to the upper substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the bottom surface, a group of pads (42 D) for connection to a printed wiring board substrate is formed.” Furuta ’415, [0020].</p>

FIG. 6

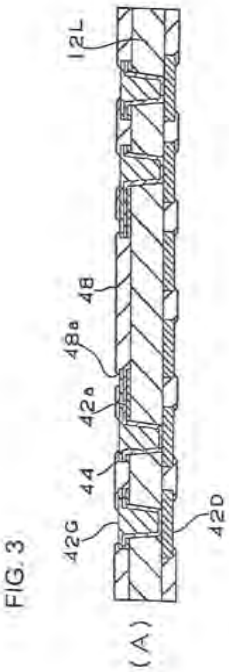
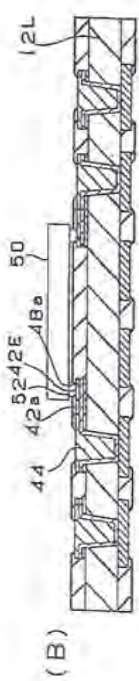
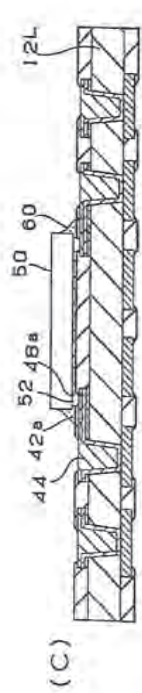
(A)



Furuta '415, FIG. 6

“In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the bottom surface of upper substrate (12 U), pads (42 F) for connection to the lower substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the top surface, pads (42 P) for connection to a package substrate are formed.” Furuta '415, [0021].

	<p>“B. Forming the Lower Substrate Steps 1-5 are the same as in the steps for the upper substrate (FIG. 3(A)). 6. Mounting an IC Chip Solder bumps 52 are formed on IC chip-mounting pads (42 E) of lower substrate (12 L). IC chip 50 is mounted by flip-chip mounting through a reflow process on solder bumps 52 (FIG. 3(C)). Then, in the gap between IC chip 50 and lower substrate (12 L), underfill 60 is filled (FIG. 3(C)). In doing so, a mounting substrate with mounted IC chip 50 (lower substrate (12 L)) is formed.” Furuta ’415, [0031-0033].</p>
--	---



Furuta '415, FIG. 3

“Then, through solder bumps 64 formed on a group of pads (42 L) of lower substrate (12 L) or a BGA, combination substrate 10 is connected to printed wiring board 74 by connecting it to pads 76 of printed wiring board 74 (FIG. 6(B)).” Furuta '415, [0040].

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

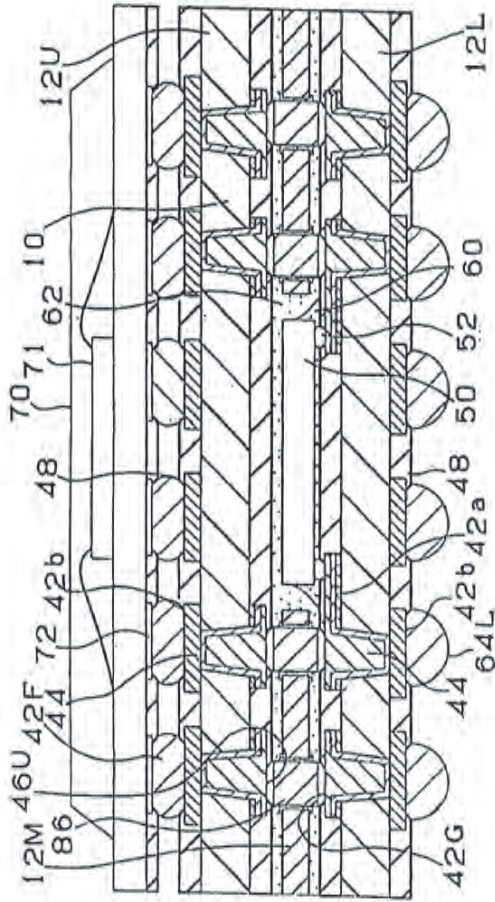
	<p>“According to requirements, solder bumps (64 L) may be formed on pads (42 D) of lower substrate (12 L) (FIG. 5(C)). On a group of pads (42 P) on the top portion of upper substrate (12 U), package substrate 70 with built-in or mounted IC chip 71 may be mounted (FIG. 6(A)). By doing so, a laminated structure of a package substrate having two or more IC chips (50, 71) is obtained.” Furuta '415, [0040].</p> <p>“The lower substrate has connection pads for electrical connection to the upper substrate on the surface facing the upper substrate, and mounting pads for installation on the printed wiring board on the surface opposite the surface facing the upper substrate; the upper substrate has connection pads for electrical connection to the lower substrate on the surface facing the lower substrate, and mounting pads for installation of a package substrate on the surface opposite the surface facing the lower substrate; and a middle substrate positioned between the upper substrate and the lower substrate has conductive members electrically connecting the connection pads on the lower substrate and the connection pads on the upper substrate.” Furuta '415, [0053].</p> <p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Furuta '415 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>“Combination substrate 10 is structured with upper substrate (12 U), interposer (12 M) as an intermediate and lower substrate (12 L).” Furuta ’415, [0020].</p> <p>“In the following, the steps for manufacturing a combination substrate according to Example 1 with reference to FIGS. 6(A) and 6(B) will be described by referring to FIGS. 1-5. A. Forming the Upper Substrate 1.” Furuta ’415, [0026].</p> <p>“Circuit (pads) (42 G) of lower substrate (12 L), posts 86 of interposer (12 M) and circuit (pads) (42 F) of upper substrate (12 U) are aligned (FIG. 5(A)).” Furuta ’415, [0038].</p> <p>“By such, upper substrate (12 U) and lower substrate (12 L) are electrically connected through interposer (12 M).” Furuta ’415, [0038].</p> <p>“On a group of pads (42 P) on the top portion of upper substrate (12 U), package substrate 70 with built-in or mounted IC chip 71 may be mounted (FIG. 6(A)). By doing so, a laminated structure of a package substrate having two or more IC chips (50, 71) is obtained.” Furuta ’415, [0040].</p>
--	---

FIG. 6

(A)



Furuta '415, FIG. 6

“Then, through solder bumps 64 formed on a group of pads (42 L) of lower substrate (12 L) or a BGA, combination substrate 10 is connected to printed wiring board 74 by connecting it to pads 76 of printed wiring board 74 (FIG. 6(B)).” Furuta '415, [0040].

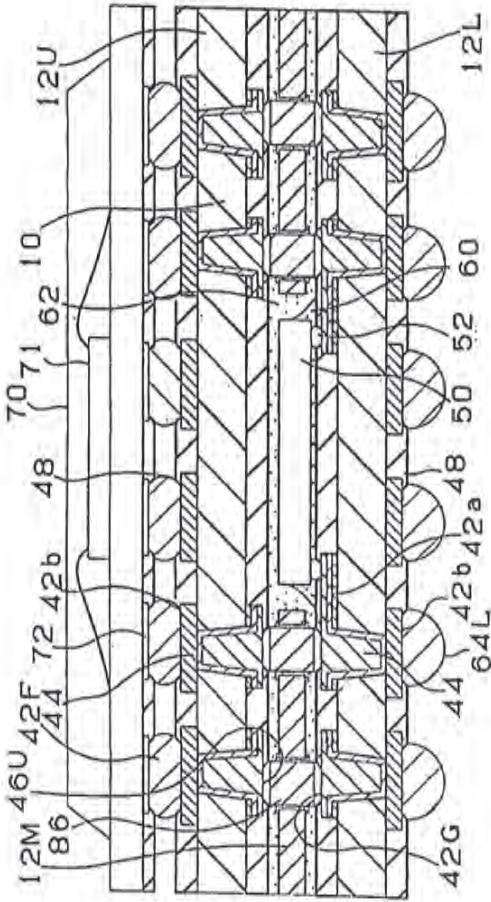
To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Furuta '415 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Between lower substrate (12 L) and IC chip 50, insulative resin underfill 60 is filled; and between upper substrate (12 U) and lower substrate (12 L), resin filling agent 62 is filled. Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M). Metal posts 86 are formed, for example, of copper or copper alloy. As shown in FIG. 6(B), on pads (42 D) on the bottom surface of combination substrate 10, solder bumps (64 L) or a BGA is arranged, then connected to a group of pads 76 on printed wiring board 74 so that combination substrate 10 is loaded onto printed wiring board 74. In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected. Accordingly, it is possible to obtain connection through posts 86 with a smaller diameter than solder bumps, and thus wiring may be arranged with a fine pitch. Also, since uniformly manufactured posts 86 are used, unlike solder bumps of varying sizes, heat is generated uniformly, thus high temperatures in spots may seldom be generated. Moreover, since interposer (12M) lies in between, the height between upper substrate (12U) and lower substrate (12L) may be adjusted, making it easier to secure electrical connectivity and reliability. “ Furuta '415, [0021-0023].</p>

FIG. 6

(A)



Furuta '415, FIG. 6

“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected. Accordingly, it is possible to obtain connection through posts 86 with a smaller diameter than solder bumps, and thus wiring may be arranged with a fine pitch. Also, since uniformly manufactured posts 86 are used, unlike solder bumps of varying sizes, heat is generated

	<p>uniformly, thus high temperatures in spots may seldom be generated. Moreover, since interposer (12 M) lies in between, the height between upper substrate (12 U) and lower substrate (12 L) may be adjusted, making it easier to secure electrical connectivity and reliability.” Furuta ’415, [0023-0024].</p> <p>“C. Forming an Interposer Insulative material 80 is prepared (FIG. 4(A)). Openings 82 penetrating insulative material 80 are formed (FIG. 4(B)) and conductive layers 84 are formed in openings 82 (FIG. 4(C)). Conductive layers 84 are formed by through-holes, vias and post-implants. For the conductive layers, metals such as copper, nickel or noble metals may be used. As an example, there is a method to fill posts with implants. An insulative substrate having conductive layers formed by copper foil, plating or the like on both surfaces is prepared. Openings for through-holes are bored in the insulative substrate using a drill or a laser. Then, resist layers are provided on the entire surfaces of the conductive layers, and masks with a drawn wiring pattern are placed. After that, through exposure to light and development, then through an etching treatment, patterns for an interposer are formed. Then, if necessary, solder-resist layers may be formed or external configuration processing (unit processing for the interposer) may be conducted. By such, an insulative substrate having openings for implants is prepared. Implant material to form implant posts is prepared. The thickness (height) is preferred to be thicker than the insulative substrate. Beneath the implant material, a lower jig for implant processing is placed in advance. Here, on the implant material, an upper jig with projections for piercing is placed. The upper jig pierces to the midway point of the implant material. The pierced implant material is inserted in openings 82 of insulative substrate 80 prepared above, then pounded in. Accordingly, conductive members (metal posts) 86 penetrating the insulative substrate are formed (FIG. 4(D)). Then, the implant material is separated and the height of posts 86 protruding beyond insulative substrate 80 is aligned. In doing so, insulative substrate 80, which is interposer (12 M), obtains conductive members (posts) 86, which enable electrical connection between the top</p>
--	--

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

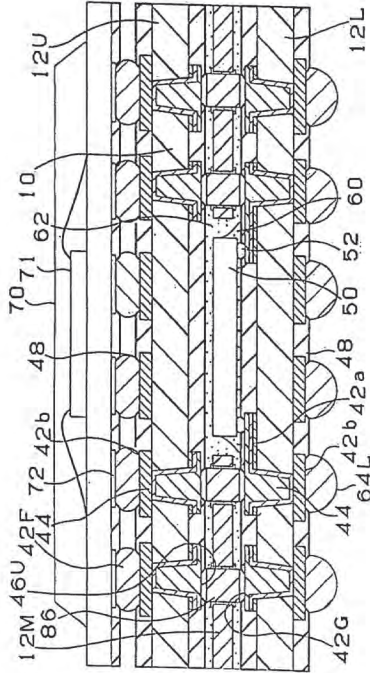
	<p>and bottom, and whose heights protruding beyond insulative substrate 80 are substantially the same.” Furuta ’415, [0033-0037].</p> <p>“C. Forming a Laminated Substrate 1. Aligning the Lower Substrate and the Upper Substrate Circuit (pads) (42 G) of lower substrate (12 L), posts 86 of interposer (12 M) and circuit (pads) (42 F) of upper substrate (12 U) are aligned (FIG. 5(A)). Here, circuit portions (42 G) of lower substrate (12 L) come in contact with posts 86 of interposer (12 M); and circuit portions (42 F) of upper substrate (12 U) come in contact with posts 86 of interposer (12 M). By such, upper substrate (12 U) and lower substrate (12 L) are electrically connected through interposer (12 M). Posts 86 of interposer (12 M) and conductive layers (42 G, 42 F) of each substrate may be connected using solder or the like as conductive adhesive agent 88.” Furuta ’415, [0037-0038].</p> <p>To the extent Plaintiff contends that Furuta ’415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Furuta ’415 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Between lower substrate (12 L) and IC chip 50, insulative resin underfill 60 is filled; and between upper substrate (12 U) and lower substrate (12 L), resin filling agent 62 is filled. Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in</p>

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

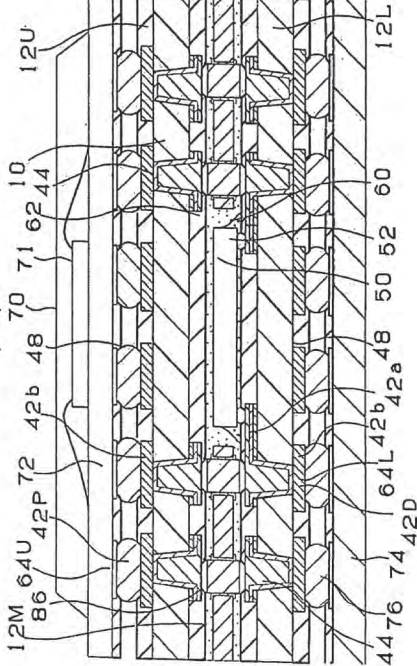
	interposer (12 M). Metal posts 86 are formed, for example, of copper or copper alloy.” Furuta '415, [0021-0022].
--	---

FIG. 6

(A)



(B)

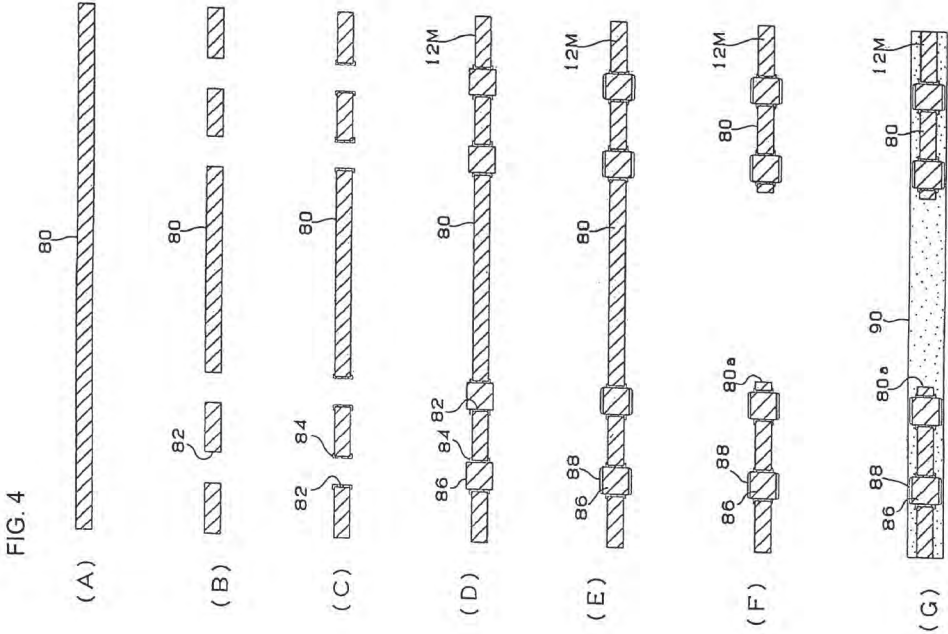


Furuta '415, FIG. 6

	<p>“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected.” Furuta ’415, [0023].</p> <p>“Moreover, since interposer (12 M) lies in between, the height between upper substrate (12 U) and lower substrate (12 L) may be adjusted, making it easier to secure electrical connectivity and reliability.” Furuta ’415, [0023-0024].</p> <p>“Insulative material 80 is prepared (FIG. 4(A)). Openings 82 penetrating insulative material 80 are formed (FIG. 4(B)) and conductive layers 84 are formed in openings 82 (FIG. 4(C)). Conductive layers 84 are formed by through-holes, vias and post-implants. For the conductive layers, metals such as copper, nickel or noble metals may be used. As an example, there is a method to fill posts with implants. An insulative substrate having conductive layers formed by copper foil, plating or the like on both surfaces is prepared. Openings for through-holes are bored in the insulative substrate using a drill or a laser. Then, resist layers are provided on the entire surfaces of the conductive layers, and masks with a drawn wiring pattern are placed. After that, through exposure to light and development, then through an etching treatment, patterns for an interposer are formed. Then, if necessary, solder-resist layers may be formed or external configuration processing (unit processing for the interposer) may be conducted. By such, an insulative substrate having openings for implants is prepared. Implant material to form implant posts is prepared. The thickness (height) is preferred to be thicker than the insulative substrate. Beneath the implant material, a lower jig for implant processing is placed in advance. Here, on the implant material, an upper jig with projections for piercing is placed. The upper jig pierces to the midway point of the implant material. The pierced implant material is inserted in openings 82 of insulative substrate 80 prepared above,</p>
--	--

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>then pounded in. Accordingly, conductive members (metal posts) 86 penetrating the insulative substrate are formed (FIG. 4(D)). Then, the implant material is separated and the height of posts 86 protruding beyond insulative substrate 80 is aligned. In doing so, insulative substrate 80, which is interposer (12 M), obtains conductive members (posts) 86, which enable electrical connection between the top and bottom, and whose heights protruding beyond insulative substrate 80 are substantially the same.” Furuta ’415, [0034-0037].</p>
--	--



Furuta '415, FIG. 4

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

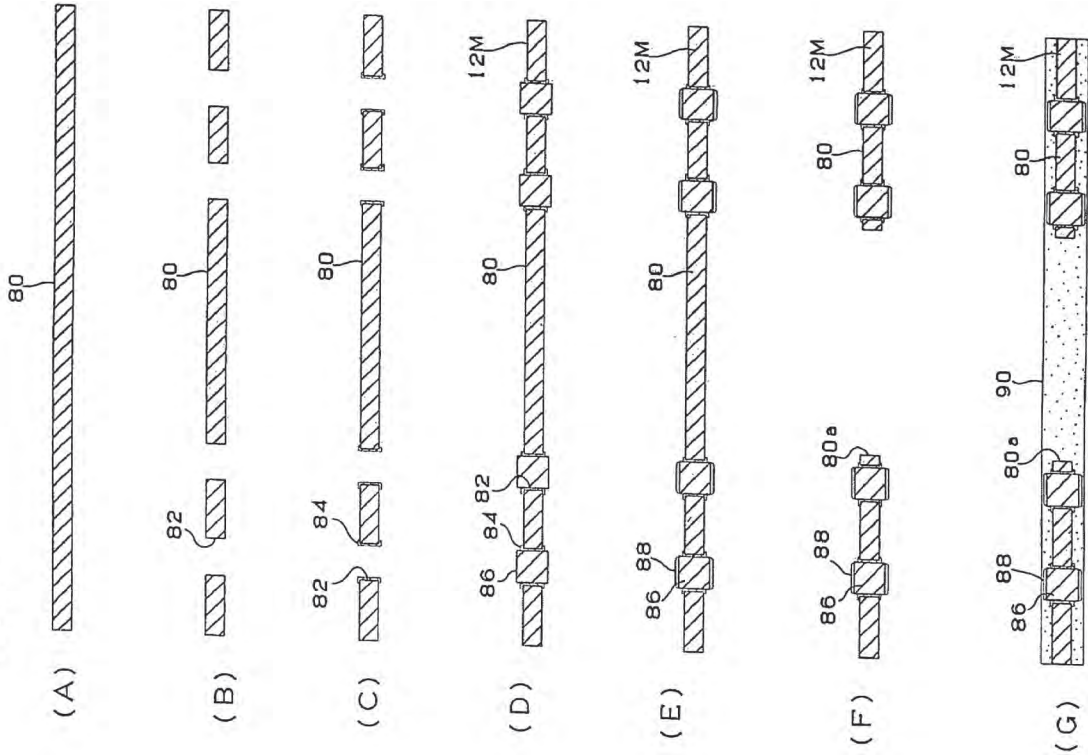
	<p>“In doing so, insulative substrate 80, which is interposer (12 M), obtains conductive members (posts) 86, which enable electrical connection between the top and bottom, and whose heights protruding beyond insulative substrate 80 are substantially the same. Here, if required, adhesive agent 88 may be applied to anchor posts 86, which are conductive layers (FIG. 4(E)). In addition, at the tips of the conductive layers, a process to prevent oxidation or to improve the connection to the conductive layers of the substrate (forming roughened surfaces, mirror surface treatment, etc.) may be conducted. Further, open holes (80 a) may be formed to prevent interference with an IC chip (FIG. 4(F)). In doing so, interposer (12 M) lying between the upper substrate and lower substrate may be prepared.” Furuta '415, [0037].</p> <p>“In Example 1, interiors of open holes (80 a) of interposer (12 M) are filled with underfill 62 or resin 90. In contrast, as shown in FIG. 10(C), Example 2 has a structure so as not to fill the interiors of open holes (80 a) of interposer (12 M) with resin 90.” Furuta '415, [0049].</p> <p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Furuta '415 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p>

	<p>“At lower substrate (12 L), conductive circuit (42 b) on the bottom surface and conductive circuit (42 a) on the top surface are connected through vias 44, and IC chip 50 and conductive circuit (42 b) on the top surface are connected through solder bumps 52.” Furuta '415, [0020].</p> <p>“Between lower substrate (12 L) and IC chip 50, insulative resin underfill 60 is filled; and between upper substrate (12 U) and lower substrate (12 L), resin filling agent 62 is filled. Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta '415, [0021].</p> <p>“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected.” Furuta '415, [0023].</p> <p>“Openings 82 penetrating insulative material 80 are formed (FIG. 4(B)) and conductive layers 84 are formed in openings 82 (FIG. 4(C)). Conductive layers 84 are formed by through-holes, vias and post-implants. For the conductive layers, metals such as copper, nickel or noble metals may be used. As an example, there is a method to fill posts with implants. An insulative substrate having conductive layers formed by copper foil, plating or the like on both surfaces is prepared. Openings for through-holes are bored in the insulative substrate using a drill or a laser. Then, resist layers are provided on the entire surfaces of the conductive layers, and masks with a drawn wiring pattern are placed. After that, through exposure to light and development, then through an etching treatment, patterns for an interposer are formed. Then, if necessary, solder-resist layers may be formed or external configuration processing (unit processing for the interposer) may be conducted. By such, an</p>
--	---

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>insulative substrate having openings for implants is prepared. Implant material to form implant posts is prepared. The thickness (height) is preferred to be thicker than the insulative substrate. Beneath the implant material, a lower jig for implant processing is placed in advance. Here, on the implant material, an upper jig with projections for piercing is placed. The upper jig pierces to the midway point of the implant material. The pierced implant material is inserted in openings 82 of insulative substrate 80 prepared above, then pounded in. Accordingly, conductive members (metal posts) 86 penetrating the insulative substrate are formed (FIG. 4(D)).” Furuta ’415, [0034-0037].</p>
--	--

FIG. 4

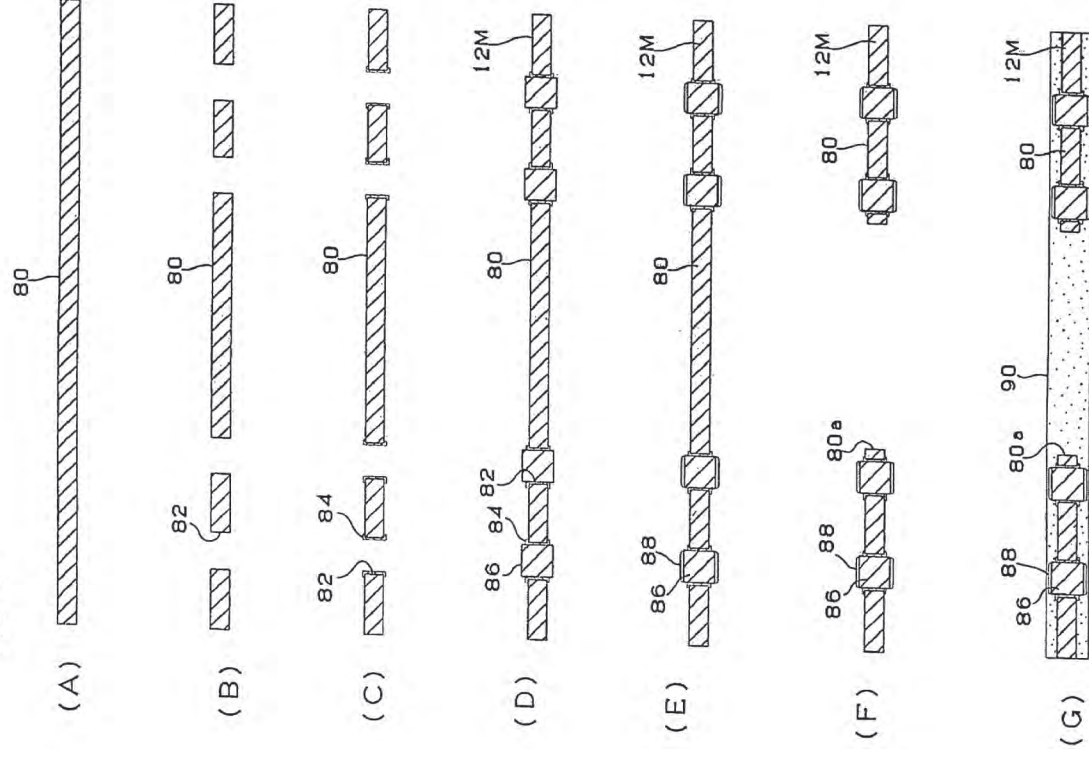


Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>Furuta '415, FIG. 4</p> <p>“Then, the implant material is separated and the height of posts 86 protruding beyond insulative substrate 80 is aligned. In doing so, insulative substrate 80, which is interposer (12 M), obtains conductive members (posts) 86, which enable electrical connection between the top and bottom, and whose heights protruding beyond insulative substrate 80 are substantially the same.” Furuta '415, [0037].</p> <p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Furuta '415 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta '415, [0021].</p> <p>“On upper substrate (12 U), solder-resist layer 48 may be formed to protect conductive circuit 42 if necessary (FIG. 2(C)). Here, at upper substrate (12 U), on the surface facing the lower substrate (the lower portion in the drawing) a group of pads (42 F) for connection to the lower substrate is formed in openings (48 a) of solder-resist layer 48.” Furuta '415, [0031].</p>

	<p>“Accordingly, conductive members (metal posts) 86 penetrating the insulative substrate are formed (FIG. 4(D)). Then, the implant material is separated and the height of posts 86 protruding beyond insulative substrate 80 is aligned. In doing so, insulative substrate 80, which is interposer (12 M), obtains conductive members (posts) 86, which enable electrical connection between the top and bottom, and whose heights protruding beyond insulative substrate 80 are substantially the same.” Furuta '415, [0037].</p> <p>“Circuit (pads) (42G) of lower substrate (12L), posts 86 of interposer (12M) and circuit (pads) (42F) of upper substrate (12U) are aligned (FIG. 5(A)). Here, circuit portions (42G) of lower substrate (12L) come in contact with posts 86 of interposer (12M); and circuit portions (42F) of upper substrate (12U) come in contact with posts 86 of interposer (12M). By such, upper substrate (12U) and lower substrate (12L) are electrically connected through interposer (12M). Posts 86 of interposer (12M) and conductive layers (42G, 42F) of each substrate may be connected using solder or the like as conductive adhesive agent 88. Here, if the upper substrate and the lower substrate are seen from the central portion of the interposer as an axis, the circuit portions at the connection show a mirror structure (a top-bottom symmetrical structure).” Furuta '415, [0038].</p>
--	---

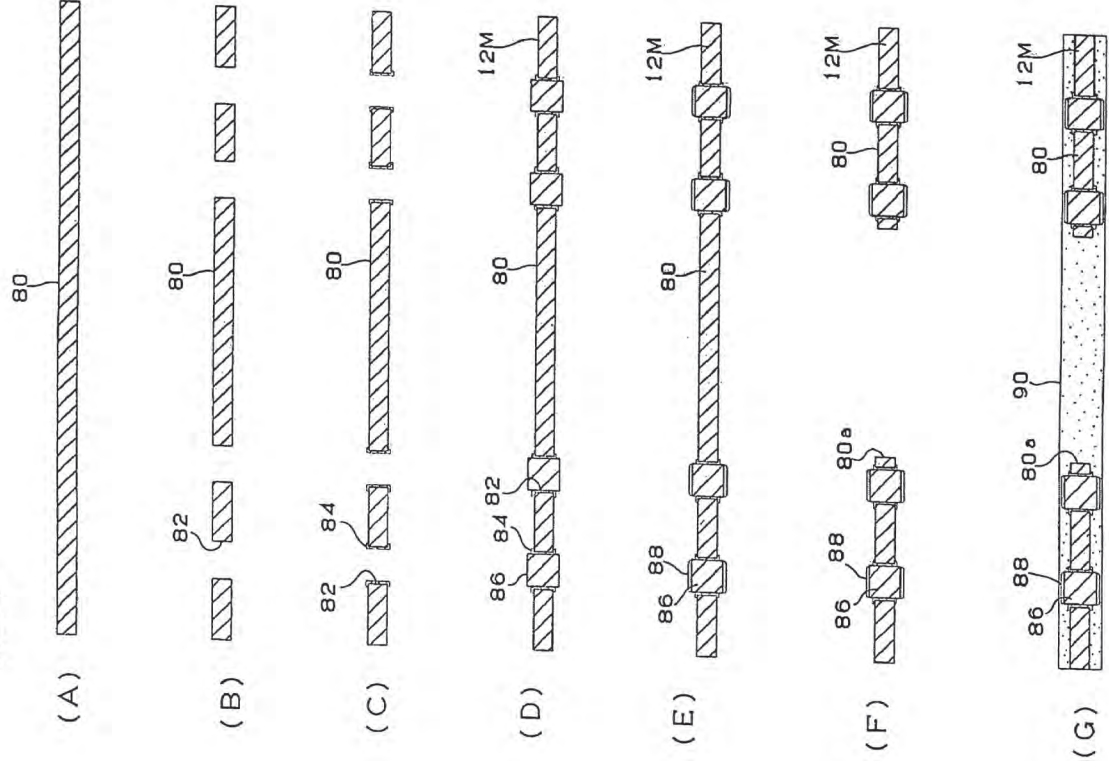
FIG. 4



Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

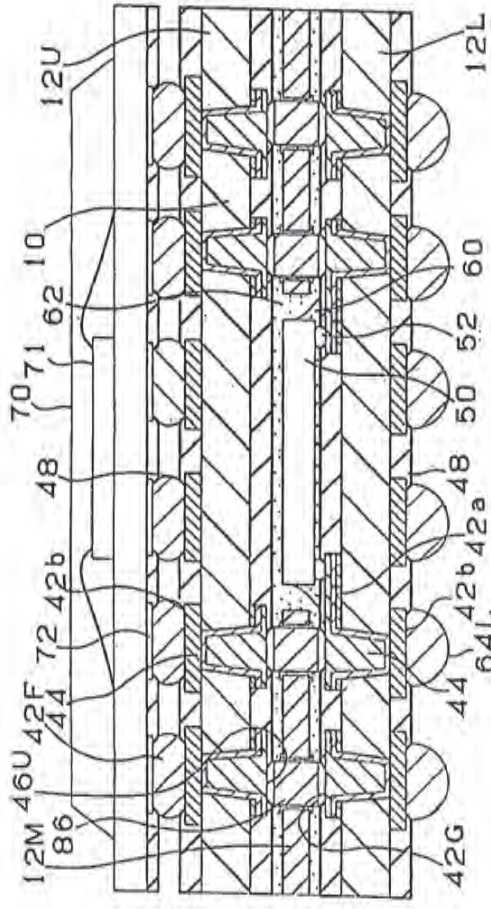
	<p>Furuta '415, FIG. 4</p> <p>“Posts 86 of interposer (12 M) and conductive layers (42 G, 42 F) of each substrate may be connected using solder or the like as conductive adhesive agent 88.” Furuta '415, [0038].</p> <p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Furuta '415 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Then, the implant material is separated and the height of posts 86 protruding beyond insulative substrate 80 is aligned. In doing so, insulative substrate 80, which is interposer (12 M), obtains conductive members (posts) 86, which enable electrical connection between the top and bottom, and whose heights protruding beyond insulative substrate 80 are substantially the same.” Furuta '415, [0037].</p>

FIG. 4



Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>Furuta '415, FIG. 4</p> <p>“Here, if required, adhesive agent 88 may be applied to anchor posts 86, which are conductive layers (FIG. 4(E)). In addition, at the tips of the conductive layers, a process to prevent oxidation or to improve the connection to the conductive layers of the substrate (forming roughened surfaces, mirror surface treatment, etc.) may be conducted. Further, open holes (80 a) may be formed to prevent interference with an IC chip (FIG. 4(F)). In doing so, interposer (12M) lying between the upper substrate and lower substrate may be prepared.” Furuta '415, [0037].</p> <p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Furuta '415 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the bottom surface of upper substrate (12 U), pads (42 F) for connection to the lower substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the top surface, pads (42 P) for connection to a package substrate are formed. Between lower substrate (12 L) and</p>

	<p>IC chip 50, insulative resin underfill 60 is filled; and between upper substrate (12 U) and lower substrate (12 L), resin filling agent 62 is filled.” Furuta ’415, [0021].</p> <p>FIG. 6 (A)</p>  <p>Furuta ’415, FIG. 6</p> <p>“Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta ’415, [0021].</p>
--	--

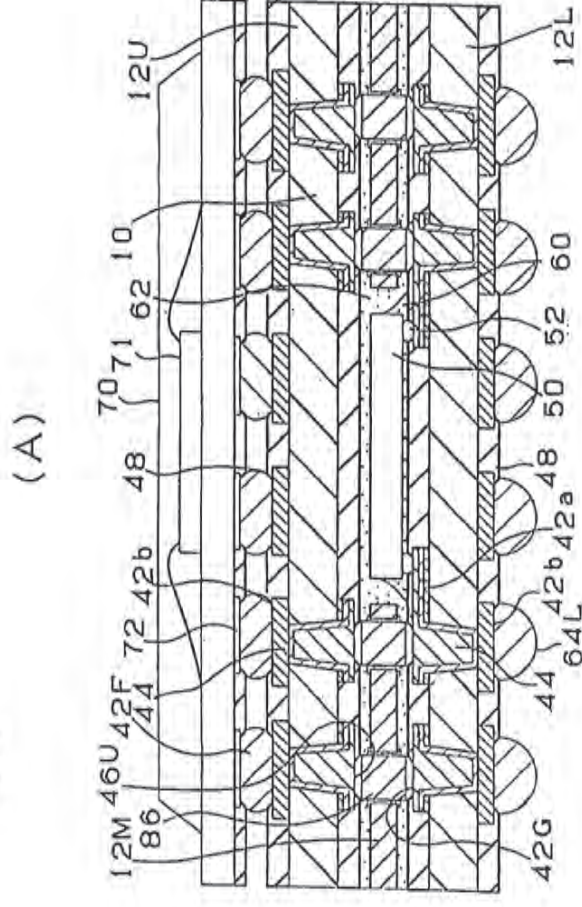
Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected.” Furuta ’415, [0023].</p> <p>“Here, circuit portions (42 G) of lower substrate (12 L) come in contact with posts 86 of interposer (12 M); and circuit portions (42 F) of upper substrate (12 U) come in contact with posts 86 of interposer (12 M). By such, upper substrate (12 U) and lower substrate (12 L) are electrically connected through interposer (12 M).” Furuta ’415, [0038].</p> <p>“Posts 86 of interposer (12 M) and conductive layers (42 G, 42 F) of each substrate may be connected using solder or the like as conductive adhesive agent 88.” Furuta ’415, [0038].</p> <p>“The combination substrate has the following technical features: The lower substrate has connection pads for electrical connection to the upper substrate on the surface facing the upper substrate, and mounting pads for installation on the printed wiring board on the surface opposite the surface facing the upper substrate; the upper substrate has connection pads for electrical connection to the lower substrate on the surface facing the lower substrate, and mounting pads for installation of a package substrate on the surface opposite the surface facing the lower substrate; and a middle substrate positioned between the upper substrate and the lower substrate has conductive members electrically connecting the connection pads on the lower substrate and the connection pads on the upper substrate.” Furuta ’415, [0053].</p> <p>To the extent Plaintiff contends that Furuta ’415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Furuta '415 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“At lower substrate (12 L), conductive circuit (42 b) on the bottom surface and conductive circuit (42 a) on the top surface are connected through vias 44, and IC chip 50 and conductive circuit (42 b) on the top surface are connected through solder bumps 52. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the top surface of lower substrate (12 L), pads (42 G) for connection to the upper substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the bottom surface, a group of pads (42 D) for connection to a printed wiring board substrate is formed. In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the bottom surface of upper substrate (12 U), pads (42 F) for connection to the lower substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the top surface, pads (42 P) for connection to a package substrate are formed.” Furuta '415, [0020-0021].</p>
---	---

FIG. 6



Furuta '415, FIG. 6

“Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta ’415, [0021].

“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>connection pads (42 F) on upper substrate (12 U) are electrically connected.” Furuta ’415, [0023].</p> <p>“Circuit (pads) (42 G) of lower substrate (12 L), posts 86 of interposer (12 M) and circuit (pads) (42 F) of upper substrate (12 U) are aligned (FIG. 5(A)). Here, circuit portions (42 G) of lower substrate (12 L) come in contact with posts 86 of interposer (12 M); and circuit portions (42 F) of upper substrate (12 U) come in contact with posts 86 of interposer (12 M). By such, upper substrate (12 U) and lower substrate (12 L) are electrically connected through interposer (12 M). Posts 86 of interposer (12 M) and conductive layers (42 G, 42 F) of each substrate may be connected using solder or the like as conductive adhesive agent 88.” Furuta ’415, [0038].</p> <p>“The lower substrate has connection pads for electrical connection to the upper substrate on the surface facing the upper substrate, and mounting pads for installation on the printed wiring board on the surface opposite the surface facing the upper substrate; the upper substrate has connection pads for electrical connection to the lower substrate on the surface facing the lower substrate, and mounting pads for installation of a package substrate on the surface opposite the surface facing the lower substrate; and a middle substrate positioned between the upper substrate and the lower substrate has conductive members electrically connecting the connection pads on the lower substrate and the connection pads on the upper substrate.” Furuta ’415, [0053].</p> <p>“Since the post-shaped conductive members electrically connect the connection pads on the lower substrate and the connection pads on the upper substrate, it is possible to obtain connection through conductive members whose diameters are smaller than those of solder bumps.” Furuta ’415, [0055].</p>
--	---

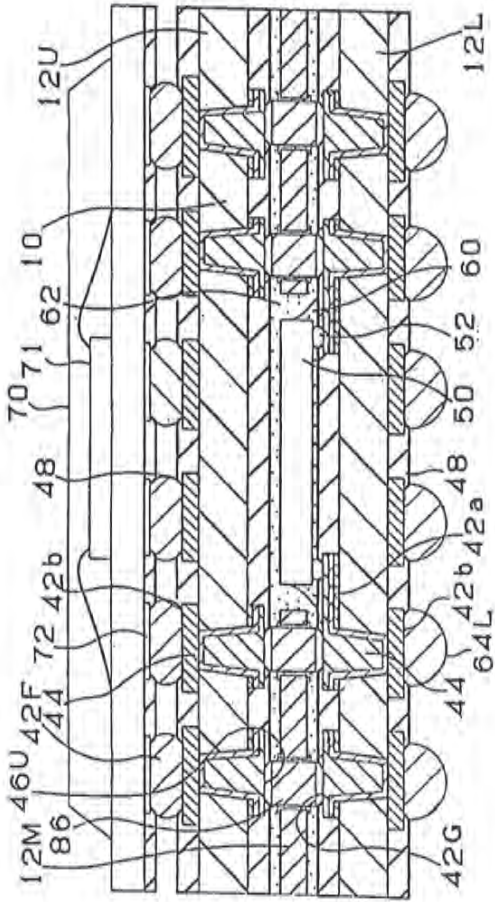
Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Furuta '415 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the bottom surface of upper substrate (12 U), pads (42 F) for connection to the lower substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the top surface, pads (42 P) for connection to a package substrate are formed.” Furuta '415, [0021].</p> <p>“Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta '415, [0021].</p> <p>“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected.” Furuta '415, [0023].</p>

“Here, circuit portions (42 G) of lower substrate (12 L) come in contact with posts 86 of interposer (12 M); and circuit portions (42 F) of upper substrate (12 U) come in contact with posts 86 of interposer (12 M).” Furuta '415, [0038].

FIG. 6

(A)



Furuta '415, FIG. 6

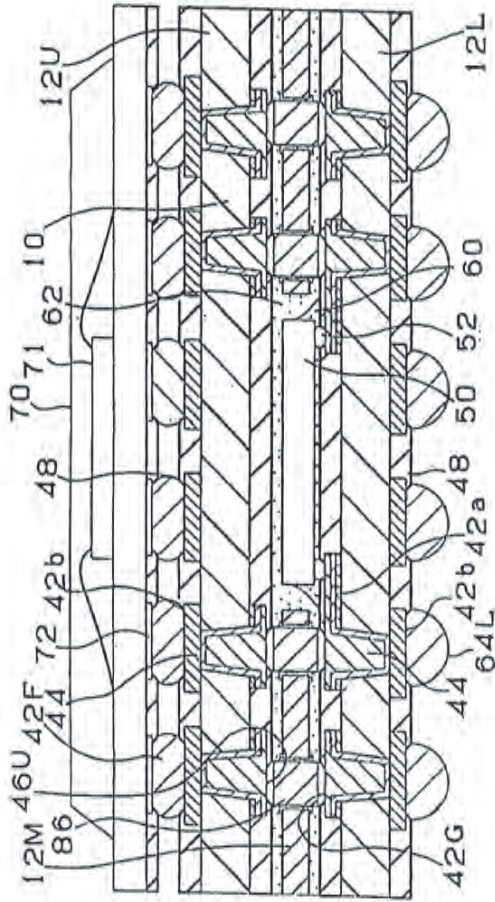
“By such, upper substrate (12 U) and lower substrate (12 L) are electrically connected through interposer (12 M).” Furuta '415, [0038].

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>“Posts 86 of interposer (12 M) and conductive layers (42 G, 42 F) of each substrate may be connected using solder or the like as conductive adhesive agent 88.” Furuta ’415, [0038].</p> <p>To the extent Plaintiff contends that Furuta ’415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Furuta ’415 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the top surface of lower substrate (12 L), pads (42 G) for connection to the upper substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the bottom surface, a group of pads (42 D) for connection to a printed wiring board substrate is formed. In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the bottom surface of upper substrate (12 U), pads (42 F) for connection to the lower substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the top surface, pads (42 P) for connection to a package substrate are formed. Between lower substrate (12 L) and IC chip 50, insulative resin underfill 60 is filled; and between upper substrate (12 U) and lower substrate (12 L), resin filling agent 62 is filled.” Furuta ’415, [0020-0021].</p>

FIG. 6

(A)

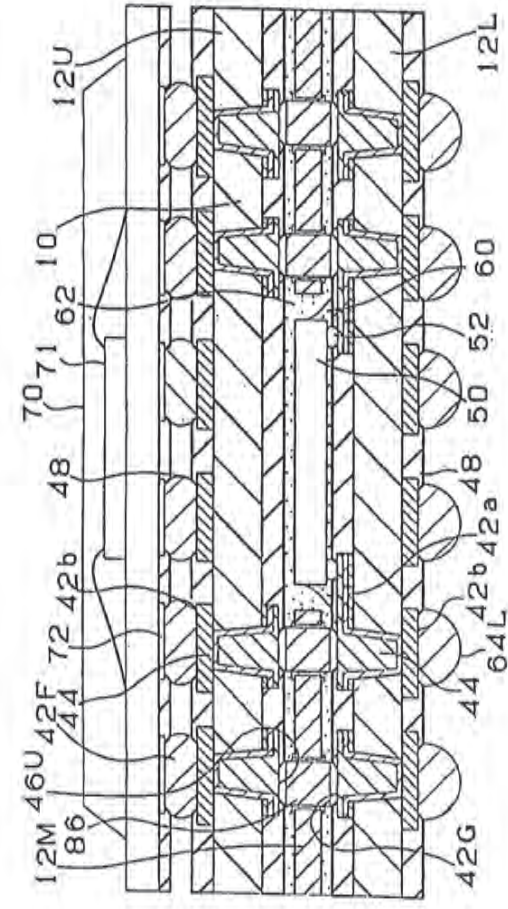


Furuta '415, FIG. 6

“On upper substrate (12 U), as shown in the plan view in FIG. 7(A) equivalent to a fragmentary view taken from the direction (a) in FIG. 6(A), a group of pads (42 P) for connection to a package substrate is arranged in the center portion of upper substrate (12 U). Likewise, on lower substrate (12 L), a group of pads (42 D) for connection to a printed wiring board is formed. On the top surface of lower substrate (12 L), IC chip 50 is mounted.”
Furuta '415, [0020].

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>“Solder bumps 52 are formed on IC chip-mounting pads (42 E) of lower substrate (12 L). IC chip 50 is mounted by flip-chip mounting through a reflow process on solder bumps 52 (FIG. 3(C)). Then, in the gap between IC chip 50 and lower substrate (12 L), underfill 60 is filled (FIG. 3(C)).” Furuta '415, [0033].</p> <p>“FIG. 8 shows a combination substrate according to Modification 1 to Example 1. In Example 1, as shown in FIG. 6(A), IC chip 50 was mounted on the top surface of lower substrate (12 L). Instead, as shown in FIG. 8, IC chip 50 may also be mounted on the bottom surface of upper substrate (12 U).” Furuta '415, [0047].</p> <p>“Here, since the interiors of open holes (80 a) of interposer (12 M) are not filled with resin 90, occurrence of cracks at the interface (especially at the corners of the IC chip) between lower substrate (12 L) and mounted IC chip 50 may be suppressed.” Furuta '415, [0049].</p> <p>“In Example 2, as shown in FIG. 10(A), non-flow type underfill 90 is applied on both surfaces of interposer (12 M) excluding open holes (80 a). As shown in FIG. 10(B), lower substrate (12 L), interposer (12 M) and upper substrate (12 U) are aligned so as to be laminated as shown in FIG. 10(C).” Furuta '415, [0050].</p> <p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Furuta '415 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p>

	<p>See, e.g.:</p> <p>“On the top surface of lower substrate (12 L), IC chip 50 is mounted. At lower substrate (12 L), conductive circuit (42 b) on the bottom surface and conductive circuit (42 a) on the top surface are connected through vias 44, and IC chip 50 and conductive circuit (42 b) on the top surface are connected through solder bumps 52.” Furuta '415, [0020].</p> <p>FIG. 6</p> <p>(A)</p>  <p>Furuta '415, FIG. 6</p>
--	--

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>“Between lower substrate (12 L) and IC chip 50, insulative resin underfill 60 is filled; and between upper substrate (12 U) and lower substrate (12 L), resin filling agent 62 is filled.” Furuta ’415, [0021].</p> <p>“Solder bumps 52 are formed on IC chip-mounting pads (42 E) of lower substrate (12 L). IC chip 50 is mounted by flip-chip mounting through a reflow process on solder bumps 52 (FIG. 3(C)). Then, in the gap between IC chip 50 and lower substrate (12 L), underfill 60 is filled (FIG. 3(C)).” Furuta ’415, [0033].</p> <p>“In doing so, a mounting substrate with mounted IC chip 50 (lower substrate (12 L)) is formed.” Furuta ’415, [0033].</p> <p>“In Example 1, as shown in FIG. 6(A), IC chip 50 was mounted on the top surface of lower substrate (12 L). Instead, as shown in FIG. 8, IC chip 50 may also be mounted on the bottom surface of upper substrate (12 U).” Furuta ’415, [0047].</p> <p>“Here, since the interiors of open holes (80 a) of interposer (12 M) are not filled with resin 90, occurrence of cracks at the interface (especially at the corners of the IC chip) between lower substrate (12 L) and mounted IC chip 50 may be suppressed.” Furuta ’415, [0049].</p> <p>To the extent Plaintiff contends that Furuta ’415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.M] the at least one spacer connector comprises two spacer connectors	<p>Furuta ’415 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

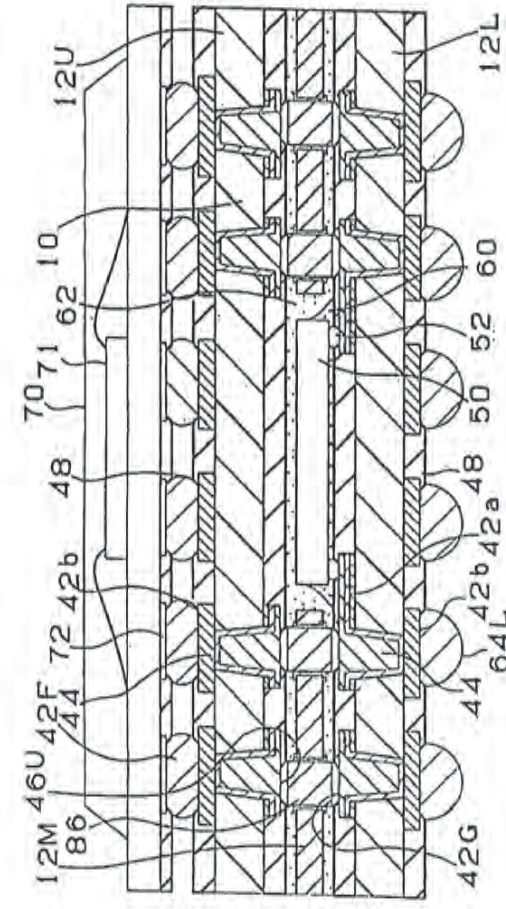
arranged on opposite sides of the bottom chip.	<p><i>See, e.g.:</i></p> <p>“Circuit (pads) (42G) of lower substrate (12L), posts 86 of interposer (12M) and circuit (pads) (42F) of upper substrate (12U) are aligned (FIG. 5(A)). Here, circuit portions (42G) of lower substrate (12L) come in contact with posts 86 of interposer (12M); and circuit portions (42F) of upper substrate (12U) come in contact with posts 86 of interposer (12M). By such, upper substrate (12U) and lower substrate (12L) are electrically connected through interposer (12M). Posts 86 of interposer (12M) and conductive layers (42G, 42F) of each substrate may be connected using solder or the like as conductive adhesive agent 88. Here, if the upper substrate and the lower substrate are seen from the central portion of the interposer as an axis, the circuit portions at the connection show a mirror structure (a top-bottom symmetrical structure).” Furuta '415, [0038].</p>
--	--

	<div><p>FIG. 6</p></div> <div><p>(A)</p></div> <div><p>The diagram shows a cross-section of a semiconductor device with multiple layers. From top to bottom, the layers are labeled: 12M, 46U, 42F, 44, 72, 42b, 48, 70, 71, 62, 10, 12U, 86, 42G, 44, 64L, 42b, 42a, 48, 50, 52, 60, and 12L. The structure includes various patterns, openings, and interfaces between these layers, typical of a semiconductor cross-section.</p></div> <div><p>Furuta '415, FIG. 6</p></div> <div><p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

Claim 2, U.S. Patent No. 9859202

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Furuta '415 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“At lower substrate (12 L), conductive circuit (42 b) on the bottom surface and conductive circuit (42 a) on the top surface are connected through vias 44, and IC chip 50 and conductive circuit (42 b) on the top surface are connected through solder bumps 52. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the top surface of lower substrate (12 L), pads (42 G) for connection to the upper substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the bottom surface, a group of pads (42 D) for connection to a printed wiring board substrate is formed. In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the bottom surface of upper substrate (12 U), pads (42 F) for connection to the lower substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the top surface, pads (42 P) for connection to a package substrate are formed.” Furuta '415, [0020-0021].</p> <p>“Solder bumps 52 are formed on IC chip-mounting pads (42E) of lower substrate (12L). IC chip 50 is mounted by flip-chip mounting through a reflow process on solder bumps 52 (FIG. 3(C)). Then, in the gap between IC chip 50 and lower substrate (12L), underfill 60 is filled (FIG. 3(C)). In doing so, a mounting substrate with mounted IC chip 50 (lower substrate (12L)) is formed. As for underfill 60, either thermosetting resin or photosensitive resin may be used. More specifically, one or more resins such as epoxy resin, polyimide resin, phenolic</p>

	<p>resin or the like may be used. In such a resin, inorganic particles or the like may be contained. Also, instead of mounting by flip-chip, mounting by wire bonding followed by sealing may be employed. In addition, two or more IC chips may be mounted, or passive components such as a capacitor may be loaded together with the IC chip.” Furuta ’415, [0033].</p> <p style="text-align: center;">FIG. 6 (A)</p>  <p style="text-align: right;">Furuta ’415, FIG. 6</p> <p>“In doing so, interposer (12 M) lying between the upper substrate and lower substrate may be prepared. C. Forming a Laminated Substrate 1.” Furuta ’415, [0037].</p>
--	--

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>“Here, since the interiors of open holes (80 a) of interposer (12 M) are not filled with resin 90, occurrence of cracks at the interface (especially at the corners of the IC chip) between lower substrate (12 L) and mounted IC chip 50 may be suppressed.” Furuta ’415, [0049].</p> <p>“In Example 2, as shown in FIG. 10(A), non-flow type underfill 90 is applied on both surfaces of interposer (12 M) excluding open holes (80 a). As shown in FIG. 10(B), lower substrate (12 L), interposer (12 M) and upper substrate (12 U) are aligned so as to be laminated as shown in FIG. 10(C).” Furuta ’415, [0050].</p> <p>“In Example 2, as shown in FIG. 10(A), non-flow type underfill 90 is applied on both surfaces of interposer (12 M) excluding open holes (80 a), and as shown in FIG. 10 (B), on IC chip 50 on lower substrate (12 L), resin 90 with low elasticity is applied. Then, interposer (12 M) and upper substrate (12 U) are aligned so as to be laminated as shown in FIG. 10(C).” Furuta ’415, [0052].</p> <p>To the extent Plaintiff contends that Furuta ’415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

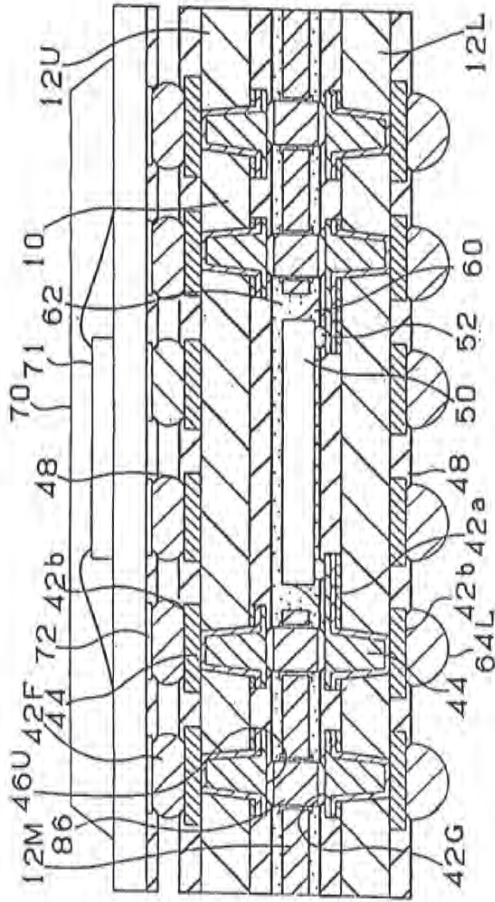
Claim Limitation	Disclosure
------------------	------------

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Furuta '415 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“The contents of the foregoing publication are incorporated herein by reference in their entirety.” Furuta '415, [0005].</p> <p>“FIG. 6(A) shows a cross-sectional view of combination substrate 10 according to Example 1. Combination substrate 10 is structured with upper substrate (12 U), interposer (12 M) as an intermediate and lower substrate (12 L). On upper substrate (12 U), as shown in the plan view in FIG. 7(A) equivalent to a fragmentary view taken from the direction (a) in FIG. 6(A), a group of pads (42 P) for connection to a package substrate is arranged in the center portion of upper substrate (12 U).” Furuta '415, [0020].</p> <p>“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected.” Furuta '415, [0023].</p> <p>“On a group of pads (42 P) on the top portion of upper substrate (12 U), package substrate 70 with built-in or mounted IC chip 71 may be mounted (FIG. 6(A)). By doing so, a laminated structure of a package substrate having two or more IC chips (50, 71) is obtained.” Furuta '415, [0040].</p>
---	--

FIG. 6

(A)



Furuta '415, FIG. 6

“On the upper substrate, a package substrate with a mounted IC chip and a passive component such as a capacitor may be loaded together.” Furuta '415, [0046].

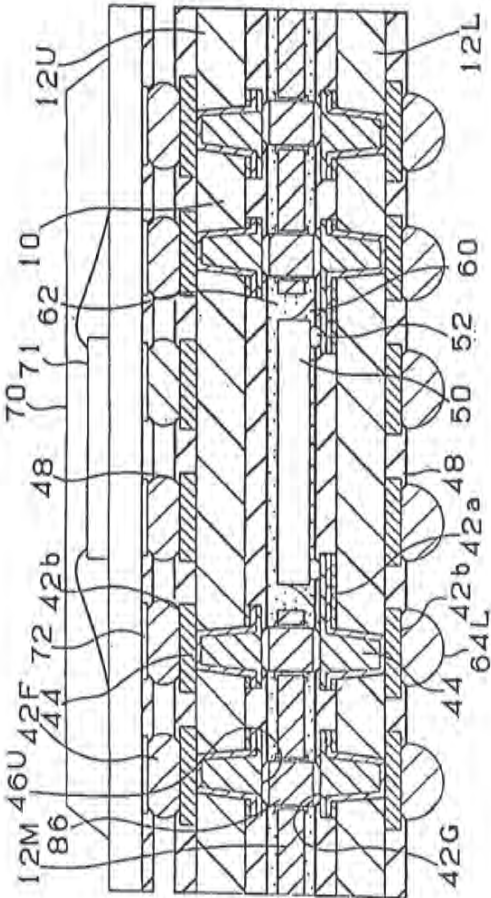
“In Example 1, as shown in FIG. 6(A), IC chip 50 was mounted on the top surface of lower substrate (12 L). Instead, as shown in FIG. 8, IC chip 50 may also be mounted on the bottom surface of upper substrate (12 U).” Furuta '415, [0047].

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Furuta '415 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta '415, [0021].</p> <p>“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected.” Furuta '415, [0023].</p>

	<p>“Forming a Laminated Substrate 1. Aligning the Lower Substrate and the Upper Substrate Circuit (pads) (42 G) of lower substrate (12 L), posts 86 of interposer (12 M) and circuit (pads) (42 F) of upper substrate (12 U) are aligned (FIG. 5(A)). Here, circuit portions (42 G) of lower substrate (12 L) come in contact with posts 86 of interposer (12 M); and circuit portions (42 F) of upper substrate (12 U) come in contact with posts 86 of interposer (12 M). By such, upper substrate (12 U) and lower substrate (12 L) are electrically connected through interposer (12 M).” Furuta '415, [0037-0038].</p> <p>FIG. 6</p> <p>(A)</p>  <p>Furuta '415, FIG. 6</p>
--	---

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>“Here, circuit portions (42 G) of lower substrate (12 L) come in contact with posts 86 of interposer (12 M); and circuit portions (42 F) of upper substrate (12 U) come in contact with posts 86 of interposer (12 M). By such, upper substrate (12 U) and lower substrate (12 L) are electrically connected through interposer (12 M). Posts 86 of interposer (12 M) and conductive layers (42 G, 42 F) of each substrate may be connected using solder or the like as conductive adhesive agent 88.” Furuta ’415, [0038].</p> <p>“Here, if the upper substrate and the lower substrate are seen from the central portion of the interposer as an axis, the circuit portions at the connection show a mirror structure (a top-bottom symmetrical structure).” Furuta ’415, [0038].</p> <p>To the extent Plaintiff contends that Furuta ’415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an	Furuta ’415 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars

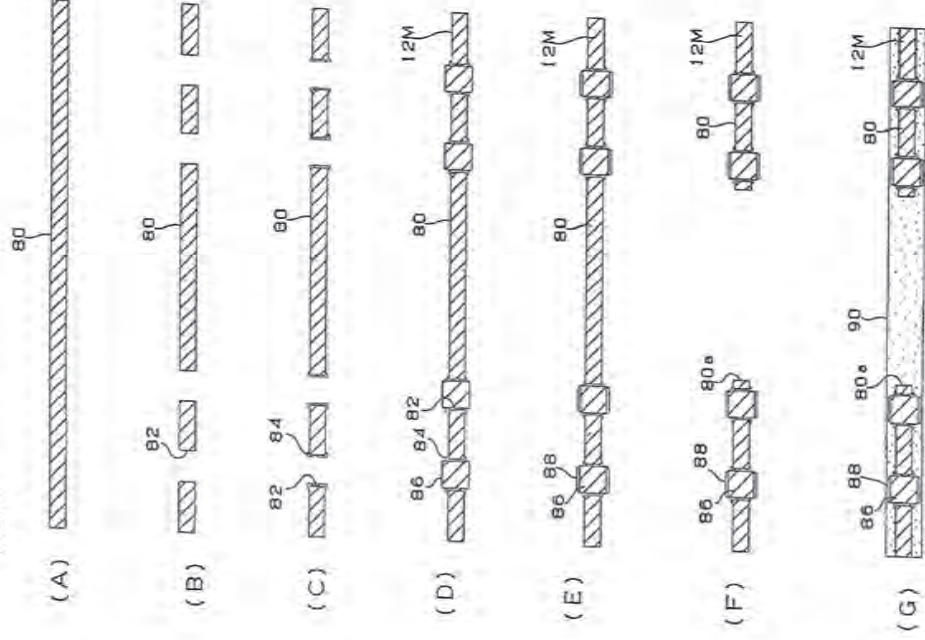
Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

<p>end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“At lower substrate (12 L), conductive circuit (42 b) on the bottom surface and conductive circuit (42 a) on the top surface are connected through vias 44, and IC chip 50 and conductive circuit (42 b) on the top surface are connected through solder bumps 52. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the top surface of lower substrate (12 L), pads (42 G) for connection to the upper substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the bottom surface, a group of pads (42 D) for connection to a printed wiring board substrate is formed. In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44.” Furuta '415, [0020-0021].</p> <p>“Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta '415, [0021].</p> <p>“In combination substrate 10 according to Example 1, through posts 86 fitted into through-holes 82 in interposer (12 M), connection pads (42 G) on lower substrate (12 L) and connection pads (42 F) on upper substrate (12 U) are electrically connected.” Furuta '415, [0023].</p> <p>“Then, if necessary, solder-resist layers may be formed or external configuration processing (unit processing for the interposer) may be conducted. By such, an insulative substrate having</p>
--	--

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>openings for implants is prepared. Implant material to form implant posts is prepared. The thickness (height) is preferred to be thicker than the insulative substrate. Beneath the implant material, a lower jig for implant processing is placed in advance. Here, on the implant material, an upper jig with projections for piercing is placed. The upper jig pierces to the midway point of the implant material. The pierced implant material is inserted in openings 82 of insulative substrate 80 prepared above, then pounded in. Accordingly, conductive members (metal posts) 86 penetrating the insulative substrate are formed (FIG. 4(D)). Then, the implant material is separated and the height of posts 86 protruding beyond insulative substrate 80 is aligned. In doing so, insulative substrate 80, which is interposer (12 M), obtains conductive members (posts) 86, which enable electrical connection between the top and bottom, and whose heights protruding beyond insulative substrate 80 are substantially the same.” Furuta '415, [0035-0037].</p>
--	--

FIG. 4



	<p>Furuta '415, FIG. 4</p> <p>“The upper jig pierces to the midway point of the implant material. The pierced implant material is inserted in openings 82 of insulative substrate 80 prepared above, then pounded in. Accordingly, conductive members (metal posts) 86 penetrating the insulative substrate are formed (FIG. 4(D)). Then, the implant material is separated and the height of posts 86 protruding beyond insulative substrate 80 is aligned. In doing so, insulative substrate 80, which is interposer (12 M), obtains conductive members (posts) 86, which enable electrical connection between the top and bottom, and whose heights protruding beyond insulative substrate 80 are substantially the same.” Furuta '415, [0036-0037].</p> <p>“Circuit (pads) (42G) of lower substrate (12L), posts 86 of interposer (12M) and circuit (pads) (42F) of upper substrate (12U) are aligned (FIG. 5(A)). Here, circuit portions (42G) of lower substrate (12L) come in contact with posts 86 of interposer (12M); and circuit portions (42F) of upper substrate (12U) come in contact with posts 86 of interposer (12M). By such, upper substrate (12U) and lower substrate (12L) are electrically connected through interposer (12M). Posts 86 of interposer (12M) and conductive layers (42G, 42F) of each substrate may be connected using solder or the like as conductive adhesive agent 88. Here, if the upper substrate and the lower substrate are seen from the central portion of the interposer as an axis, the circuit portions at the connection show a mirror structure (a top-bottom symmetrical structure).” Furuta '415, [0038].</p>
--	--

	<div><p>FIG. 6</p></div> <div><p>(A)</p></div> <div><p>The diagram shows a cross-section of a semiconductor device with multiple layers. From top to bottom, the layers are labeled: 12M, 46U, 42F, 44, 72, 42b, 48, 70, 71, 62, 10, 12U, 86, 42G, 44, 64L, 42b, 42a, 48, 50, 52, 60, and 12L. The structure includes various patterns, openings, and interfaces between the layers, typical of a semiconductor cross-section.</p></div> <div><p>Furuta '415, FIG. 6</p></div> <div><p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

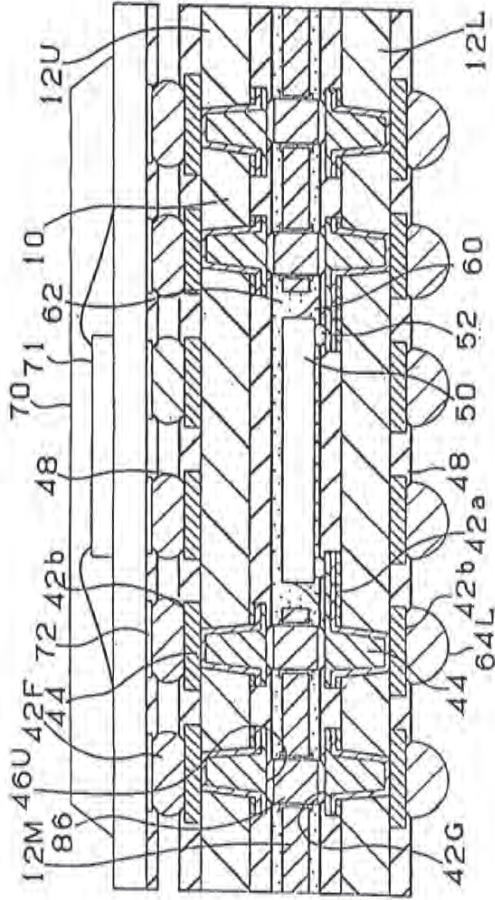
Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Furuta '415 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“At lower substrate (12 L), conductive circuit (42 b) on the bottom surface and conductive circuit (42 a) on the top surface are connected through vias 44, and IC chip 50 and conductive circuit (42 b) on the top surface are connected through solder bumps 52.” Furuta '415, [0020].</p> <p>“In the same manner, at upper substrate (12 U), conductive circuit (42 a) on the bottom surface and conductive circuit (42 b) on the top surface are connected through vias 44. In openings (48 a) of solder resist 48 for conductive circuit (42 a) on the bottom surface of upper substrate (12 U), pads (42 F) for connection to the lower substrate are formed; and in openings (48 a) of solder resist 48 for conductive circuit (42 b) on the top surface, pads (42 P) for connection to a package substrate are formed.” Furuta '415, [0021].</p> <p>“Pads (42 F) on the bottom surface of upper substrate (12 U) and pads (42 G) on the top surface of lower substrate (12 L) are electrically connected by cylindrical metal posts 86 in interposer (12 M).” Furuta '415, [0021].</p>

	<p>“Circuit (pads) (42G) of lower substrate (12L), posts 86 of interposer (12M) and circuit (pads) (42F) of upper substrate (12U) are aligned (FIG. 5(A)). Here, circuit portions (42G) of lower substrate (12L) come in contact with posts 86 of interposer (12M); and circuit portions (42F) of upper substrate (12U) come in contact with posts 86 of interposer (12M). By such, upper substrate (12U) and lower substrate (12L) are electrically connected through interposer (12M). Posts 86 of interposer (12M) and conductive layers (42G, 42F) of each substrate may be connected using solder or the like as conductive adhesive agent 88. Here, if the upper substrate and the lower substrate are seen from the central portion of the interposer as an axis, the circuit portions at the connection show a mirror structure (a top-bottom symmetrical structure).” Furuta '415, [0038].</p>
--	---

FIG. 6

(A)



Furuta '415, FIG. 6

“Posts 86 of interposer (12 M) and conductive layers (42 G, 42 F) of each substrate may be connected using solder or the like as conductive adhesive agent 88.” Furuta '415, [0038].

“Here, circuit portions (42 G) of lower substrate (12 L) come in contact with posts 86 of interposer (12 M); and circuit portions (42 F) of upper substrate (12 U) come in contact with posts 86 of interposer (12 M). By such, upper substrate (12 U) and lower substrate (12 L) are electrically connected through interposer (12 M).” Furuta '415, [0038].

Appendix A-8 - Invalidity of U.S. Patent No. 9859202 in view of Furuta '415 - U.S. Patent Publication No. 20090140415

	<p>To the extent Plaintiff contends that Furuta '415 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

U.S. Patent No.8513792 (“Ganesan”) is titled Package-On-Package Interconnect Stiffener and lists Sanka Ganesan, Yosuke Kanaoka, Ram S. Viswanath, Rajasekaran Swaminathan, Robert M. Nickerson, Leonel R. Arana, John S. Guzek, and Yoshihiro Tomita as inventors. Ganesan is assigned to Intel Corporation. Ganesan anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Ganesan is a U.S. patent that was filed April 10, 2009 and published October 14, 2010. Ganesan is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Ganesan, or otherwise rendered obvious by disclosures and teachings of Ganesan, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Ganesan does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Ganesan with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Ganesan, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Ganesan “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Ganesan or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Ganesan set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Ganesan discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 5 is a perspective view of an assembled PoP assembly having a top device package and a bottom device package attached to an interconnect stiffener according to an embodiment. Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220. FIG. 5 shows an embodiment of assembled PoP with the width and length dimensions of top device</p>

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>package 100 substantially the same with the respective dimensions of stiffener 220.” Ganesan, [2:12-2:26].</p> <p>“Embodiments of the invention include a first semiconductor package having a plurality of inter-package contact pads and a plurality of second level interconnect (SLI) pads; a second semiconductor package having a plurality of SLI pads on the bottom side of the package; and a planar stiffener having a first plurality of planar contact pads on the top side of the stiffener electrically connected to the SLI pads of the second package, and a second plurality of planar contact pads electrically connected to the inter-package contact pads of the first package.” Ganesan, [2:33-2:41].</p> <p>“FIG. 2 is a cross-sectional view of a package-on-package (PoP) assembly having an interconnect stiffener according to an embodiment. The PoP assembly is attachable to a motherboard (not shown) via second level interconnect pads 190 disposed on the bottom side of bottom device package 150. The PoP assembly includes bottom device package 150 interconnected to planar interconnect stiffener 200. Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package 150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170. Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200. Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140. Top device package 100 may be a memory package or cache unit or any other device package suited for connection with the type of device of bottom device package 150. Planar stiffener 200 also includes a plurality of planar contact pads 240 disposed on the bottom side of stiffener 200. In the PoP assembly, planar contact pads 240 are electrically connected to bottom device package 150, for example, by way of micro balls 180.” Ganesan, [2:45-2:66].</p>
--	--

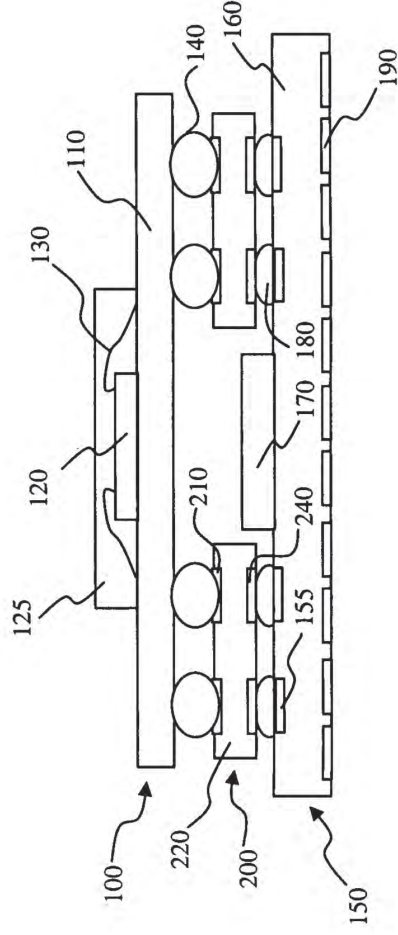


FIG. 2

Ganesan, FIG. 2

“FIG. 3 is an exploded perspective view of a PoP assembly having an interconnect stiffener according to an embodiment. Planar interconnect stiffener 220 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small through openings through which planar contact pads 210 and 240 are formed. Planar contact pads 210 and 240 formed on substrate 220 each includes a solder-wettable surface finish so that during reflow, the solder materials of micro balls 140 and 180 can melt, wet and form permanent conductive connection between stiffener 200 and the top and bottom packages 100, 150.” Ganesan, [3:1-3:12].

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>“FIG. 4 is an exploded perspective view of a top device package and a bottom device package having an interconnect stiffener attached to the top side of the bottom device package according to an embodiment. Stiffener 220 is attached to bottom device package 150 via respective contact pads 155 and 240. Planar contact pads 240 disposed on the bottom side of stiffener 220 are connected to inter-package contact pads 155 of bottom device package 150 by way of conductive micro balls 180. Stiffener 220 may be attached to bottom device package 150 before attaching top device package 100 to the top side of stiffener 220.” Ganesan, [3:17-3:27].</p> <p>“FIG. 6 is a cross-sectional view of a PoP interconnect stiffener according to an embodiment. Stiffener 200 includes substrate 220 to provide structural support and upon which contact pads 210, 240 are fabricated. Stiffener 200 includes solder resist layer 620 disposed on the top surface and bottom surface of core layer 630. For an embodiment, core layer 630 is a cored substrate fabricated from known polymeric materials such as bismaleimide triazine (BT), polyimide, and liquid crystalline (LC) polymer. However, other materials suitable for core layer 630 are not precluded in other embodiments of the invention. Substrate 220 may include a coefficient of thermal expansion (CTE) of approximately between 15 and 25 ppm. Substrate 220 may also include a flexural modulus of approximately between 15 and 30 GPa. The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220. FIG. 6 illustrates a via-in-pad design in which plug material 610 is disposed between core layer 630 and between planar contact pads 210, 240.” Ganesan, [3:46-4:3].</p>
--	--

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

<p>[1.A] a bottom package substrate;</p>	<p>Ganesan discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a cross-sectional view of a known package-on-package (PoP) assembly. Bottom device package 150 may be a core chip such as a microprocessor unit and includes die 170, substrate 160, inter-package contact pads 155 on the top side of bottom package 150, micro balls 180 attached to inter-package contact pads 155, and second level interconnect pads 190 attachable to a motherboard (not shown).” Ganesan, [2:1-2:9].</p> <p>“Embodiments of the invention include a first semiconductor package having a plurality of inter-package contact pads and a plurality of second level interconnect (SLI) pads; a second semiconductor package having a plurality of SLI pads on the bottom side of the package; and a planar stiffener having a first plurality of planar contact pads on the top side of the stiffener electrically connected to the SLI pads of the second package, and a second plurality of planar contact pads electrically connected to the inter-package contact pads of the first package.” Ganesan, [2:33-2:41].</p> <p>“The PoP assembly is attachable to a motherboard (not shown) via second level interconnect pads 190 disposed on the bottom side of bottom device package 150.” Ganesan, [2:47-2:49].</p> <p>“The PoP assembly includes bottom device package 150 interconnected to planar interconnect stiffener 200. Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package 150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170. Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200.” Ganesan, [2:50-2:57].</p>
---	---

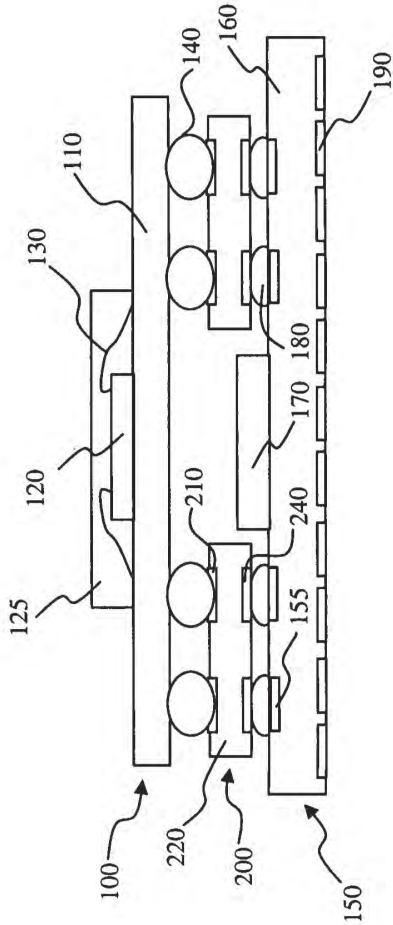


FIG. 2

Ganesan, FIG. 2

“FIG. 4 is an exploded perspective view of a top device package and a bottom device package having an interconnect stiffener attached to the top side of the bottom device package according to an embodiment. Stiffener 220 is attached to bottom device package 150 via respective contact pads 155 and 240. Planar contact pads 240 disposed on the bottom side of stiffener 220 are connected to inter-package contact pads 155 of bottom device package 150 by way of conductive micro balls 180.” Ganesan, [3:17-3:25].

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>“Bottom device package 150 having inter-package contact pads 155 on the top side of the package and second level interconnect (SLI) pads 190 on the bottom side of the package is provided. Bottom device package 150 may be in the form of individual package or multiple packages connected in a panel form.” Ganesan, [4:13-4:18].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Ganesan discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Top device package 100 is stacked onto bottom package 150 to form an electrical connection therebetween. Top device package 100 may be a peripheral chip such as a memory or cache unit, and may include die 120 interconnected to substrate 110 via wire bond 130 and encapsulated by molding 125.” Ganesan, [1:33-1:38].</p>

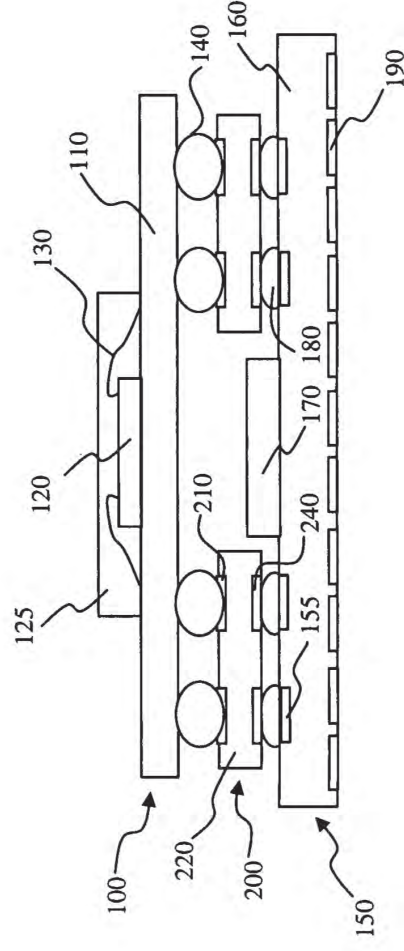


FIG. 2

Ganesan, FIG. 2

“FIG. 5 is a perspective view of an assembled PoP assembly having a top device package and a bottom device package attached to an interconnect stiffener according to an embodiment. Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [2:12-2:19].

“FIG. 2 is a cross-sectional view of a package-on-package (PoP) assembly having an interconnect stiffener according to an embodiment. The PoP assembly is attachable to a motherboard (not shown) via second level interconnect pads 190 disposed on the bottom side

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>of bottom device package 150. The PoP assembly includes bottom device package 150 interconnected to planar interconnect stiffener 200. Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package 150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170. Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200. Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140.” Ganesan, [2:45-2:59].</p> <p>“FIG. 4 is an exploded perspective view of a top device package and a bottom device package having an interconnect stiffener attached to the top side of the bottom device package according to an embodiment. Stiffener 220 is attached to bottom device package 150 via respective contact pads 155 and 240. Planar contact pads 240 disposed on the bottom side of stiffener 220 are connected to inter-package contact pads 155 of bottom device package 150 by way of conductive micro balls 180. Stiffener 220 may be attached to bottom device package 150 before attaching top device package 100 to the top side of stiffener 220.” Ganesan, [3:17-3:27].</p> <p>“Top device package 100 may subsequently be attached to planar contact pads 210 on the top side of stiffener 200 to form a package-on-package assembly.” Ganesan, [4:60-4:62].</p> <p>“Embodiments of the invention provide a device package electrically interconnected with an interconnect stiffener upon which another device package can be mounted and electrically connected to form a package-on-package assembly.” Ganesan, [4:63-4:66].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Ganesan discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small through openings through which planar contact pads 210 and 240 are formed. Planar contact pads 210 and 240 formed on substrate 220 each includes a solder-wettable surface finish so that during reflow, the solder materials of micro balls 140 and 180 can melt, wet and form permanent conductive connection between stiffener 200 and the top and bottom packages 100, 150.” Ganesan, [3:3-3:12].</p>

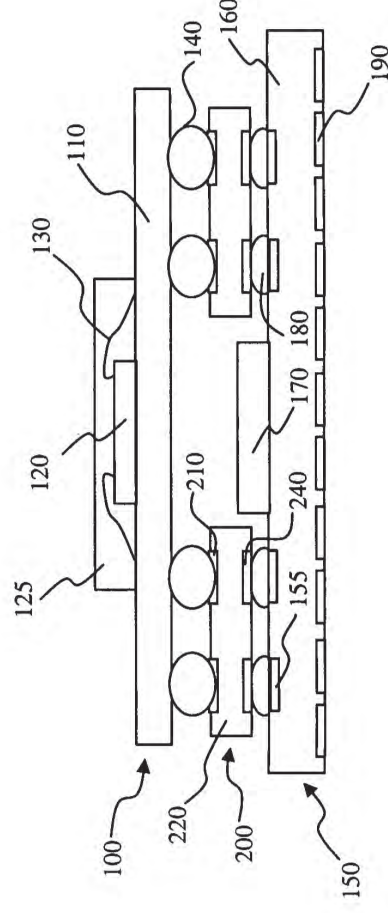
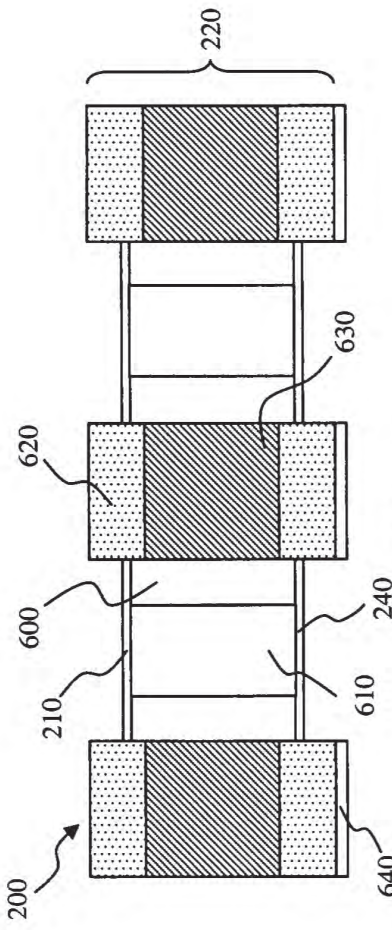


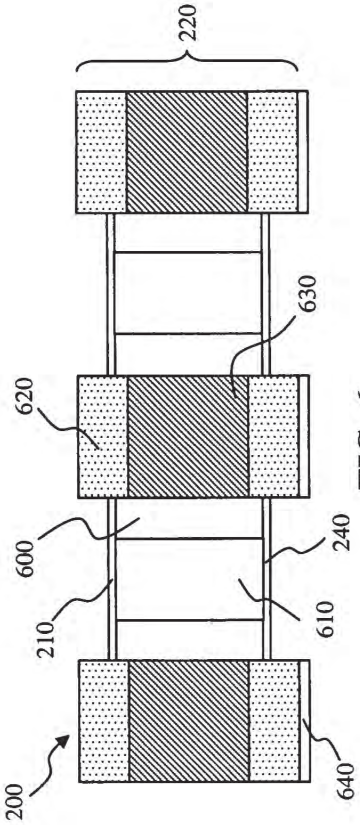
FIG. 2

Ganesan, FIG. 2

“FIG. 6 is a cross-sectional view of a PoP interconnect stiffener according to an embodiment. Stiffener 200 includes substrate 220 to provide structural support and upon which contact pads 210, 240 are fabricated. Stiffener 200 includes solder resist layer 620 disposed on the top surface and bottom surface of core layer 630. For an embodiment, core layer 630 is a cored substrate fabricated from known polymeric materials such as bismaleimide triazine (BT), polyimide, and liquid crystalline (LC) polymer.” Ganesan, [3:46-3:54].

	 <p>Ganesan, FIG. 6</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Ganesan discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small</p>

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>through openings through which planar contact pads 210 and 240 are formed.” Ganesan, [3:3-3:7].</p> <p>“Stiffener 200 includes substrate 220 to provide structural support and upon which contact pads 210, 240 are fabricated. Stiffener 200 includes solder resist layer 620 disposed on the top surface and bottom surface of core layer 630. For an embodiment, core layer 630 is a cored substrate fabricated from known polymeric materials such as bismaleimide triazine (BT), polyimide, and liquid crystalline (LC) polymer.” Ganesan, [3:47-3:54].</p> <div><p style="text-align: center;">FIG. 6</p></div> <p style="text-align: center;">Ganesan, FIG. 6</p> <p>“Substrate 220 may include a coefficient of thermal expansion (CTE) of approximately between 15 and 25 ppm. Substrate 220 may also include a flexural modulus of approximately between 15 and 30 GPa. The properties of stiffener 200 will be designed to provide</p>
--	--

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200.” Ganesan, [3:56-3:64].</p> <p>“The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220.” Ganesan, [3:60-4:1].</p> <p>“FIG. 7 is a cross-sectional view of a PoP interconnect stiffener according to another embodiment. FIG. 7 embodies a via-off-pad design in which core layer 630 extends in planar contact pads 210 and 240 regions, and plug material 610 is disposed between solder resist layers 520 and in substrate 220.” Ganesan, [4:21-4:26].</p> <p>“In operation 710, planar stiffener 200 is fabricated from core layer 630 material. Stiffener 200 may be formed in a panel form from which individual stiffener 200 units may be obtained after singulation. Known process to fabricate package substrate may be used to form stiffener 200 and the key process steps may include: drilling through-holes in core layer 630 ; plating the sidewalls of through-holes; disposing plug material 610 in the through-holes; forming electrically conductive planar contact pads 210 and 240 ; forming a solder-wettable finish on planar contact pads 210 and 240 ; and forming recess 330 in stiffener 200.” Ganesan, [4:38-4:48].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Ganesan discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Stiffener 200 includes substrate 220 to provide structural support and upon which contact pads 210, 240 are fabricated. Stiffener 200 includes solder resist layer 620 disposed on the top surface and bottom surface of core layer 630.” Ganesan, [3:47-3:51].</p> <p>“Substrate 220 may include a coefficient of thermal expansion (CTE) of approximately between 15 and 25 ppm. Substrate 220 may also include a flexural modulus of approximately between 15 and 30 GPa. The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220.” Ganesan, [3:56-4:1].</p> <p>“The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220. FIG. 6 illustrates a via-in-pad design in which plug material 610 is</p>

disposed between core layer 630 and between planar contact pads 210, 240." Ganesan, [3:60-4:3].

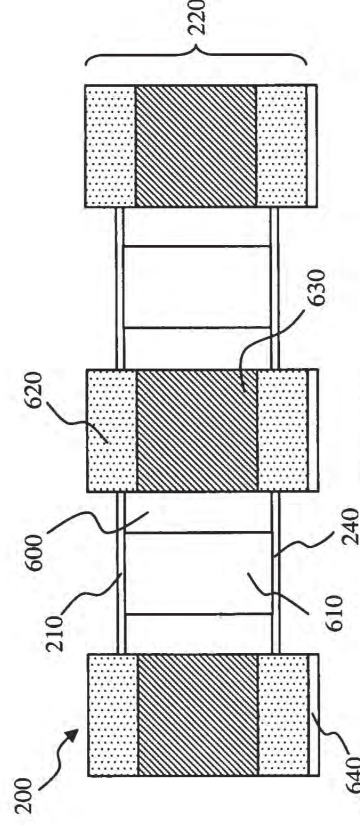


FIG. 6

Ganesan, FIG. 6

“The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220.” Ganesan, [3:60-4:1].

“FIG. 7 is a cross-sectional view of a PoP interconnect stiffener according to another embodiment. FIG. 7 embodies a via-off-pad design in which core layer 630 extends in planar

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>contact pads 210 and 240 regions, and plug material 610 is disposed between solder resist layers 520 and in substrate 220.” Ganesan, [4:21-4:26].</p> <p>“Known process to fabricate package substrate may be used to form stiffener 200 and the key process steps may include: drilling through-holes in core layer 630 ; plating the sidewalls of through-holes; disposing plug material 610 in the through-holes; forming electrically conductive planar contact pads 210 and 240 ; forming a solder-wettable finish on planar contact pads 210 and 240 ; and forming recess 330 in stiffener 200.” Ganesan, [4:41-4:48].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Ganesan discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Planar stiffener 200 also includes a plurality of planar contact pads 240 disposed on the bottom side of stiffener 200. In the PoP assembly, planar contact pads 240 are electrically connected to bottom device package 150, for example, by way of micro balls 180.” Ganesan, [2:62-2:67].</p> <p>“Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small through openings through which planar contact pads 210 and 240 are formed. Planar contact</p>

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>pads 210 and 240 formed on substrate 220 each includes a solder-wettable surface finish so that during reflow, the solder materials of micro balls 140 and 180 can melt, wet and form permanent conductive connection between stiffener 200 and the top and bottom packages 100, 150.” Ganesan, [3:3-3:12].</p> <p>“Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [3:37-3:39].</p> <p>“Stiffener 200 includes substrate 220 to provide structural support and upon which contact pads 210, 240 are fabricated. Stiffener 200 includes solder resist layer 620 disposed on the top surface and bottom surface of core layer 630.” Ganesan, [3:47-3:51].</p> <p>“The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220. FIG. 6 illustrates a via-in-pad design in which plug material 610 is disposed between core layer 630 and between planar contact pads 210, 240.” Ganesan, [3:60-4:3].</p>
--	---

	<div> <p style="text-align: center;">FIG. 6</p> </div> <p>Ganesan, FIG. 6</p> <p>“Known process to fabricate package substrate may be used to form stiffener 200 and the key process steps may include: drilling through-holes in core layer 630 ; plating the sidewalls of through-holes; disposing plug material 610 in the through-holes; forming electrically conductive planar contact pads 210 and 240 ; forming a solder-wettable finish on planar contact pads 210 and 240 ; and forming recess 330 in stiffener 200.” Ganesan, [4:41-4:48].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars</p>	<p>Ganesan discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p>

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

protrudes downwardly from a bottom surface of the core substrate,	<p><i>See, e.g.:</i></p> <p>“Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small through openings through which planar contact pads 210 and 240 are formed.” Ganesan, [3:3-3:7].</p> <p>“Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220. FIG. 6 illustrates a via-in-pad design in which plug material 610 is disposed between core layer 630 and between planar contact pads 210, 240. Plug material 610 forms part of the material for substrate 220 to provide structural rigidity and foundation to contact pads 210 and 240 and is made from known materials such as silica filled epoxy composite or commercially available solder resist materials. Stiffener 220 may also include routing features accommodating various circuitry designs of top device package 100.” Ganesan, [3:25-3:37].</p>
---	--

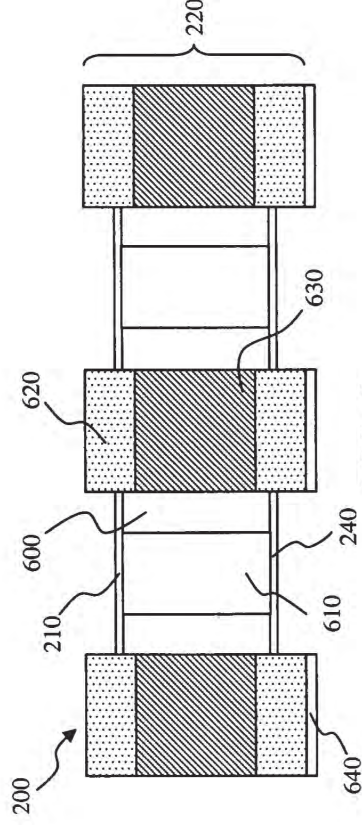


FIG. 6

Ganesan, FIG. 6

“Stiffener 200 includes substrate 220 to provide structural support and upon which contact pads 210, 240 are fabricated. Stiffener 200 includes solder resist layer 620 disposed on the top surface and bottom surface of core layer 630.” Ganesan, [3:47-3:51].

“FIG. 7 is a cross-sectional view of a PoP interconnect stiffener according to another embodiment. FIG. 7 embodies a via-off-pad design in which core layer 630 extends in planar contact pads 210 and 240 regions, and plug material 610 is disposed between solder resist layers 520 and in substrate 220.” Ganesan, [4:21-4:26].

“Known process to fabricate package substrate may be used to form stiffener 200 and the key process steps may include: drilling through-holes in core layer 630 ; plating the sidewalls of through-holes; disposing plug material 610 in the through-holes; forming electrically

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>conductive planar contact pads 210 and 240 ; forming a solder-wettable finish on planar contact pads 210 and 240 ; and forming recess 330 in stiffener 200.” Ganesan, [4:41-4:48].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Ganesan discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The bottom side of top device package 100 includes micro balls 140 reflowed and electrically connected to micro balls 180 on the top side of bottom device package 150.” Ganesan, [1:38-1:41].</p> <p>“Known process to fabricate package substrate may be used to form stiffener 200 and the key process steps may include: drilling through-holes in core layer 630 ; plating the sidewalls of through-holes; disposing plug material 610 in the through-holes; forming electrically conductive planar contact pads 210 and 240 ; forming a solder-wettable finish on planar contact pads 210 and 240 ; and forming recess 330 in stiffener 200. In operation 720 (FIG. 8), planar stiffener 200 is mounted on the top side of bottom device package 150. Planar contact pads 240 on the bottom side of stiffener 200 are aligned and attached to micro balls 180 connected to inter-package contact pads 155 of bottom device package 150.” Ganesan, [2:1-2:16].</p>

“Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200. Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140.” Ganesan, [2:56-2:60].

“Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [3:37-3:39].

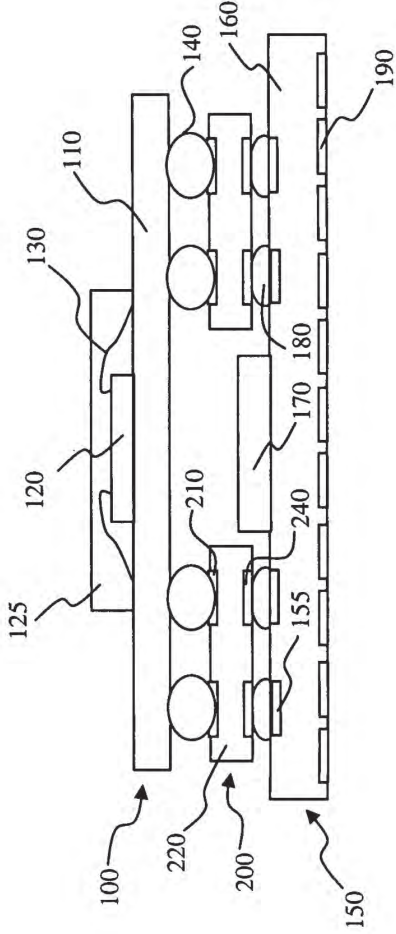


FIG. 2

Ganesan, FIG. 2

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>“The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220.” Ganesan, [3:60-4:1].</p> <p>“Top device package 100 may subsequently be attached to planar contact pads 210 on the top side of stiffener 200 to form a package-on-package assembly.” Ganesan, [4:60-4:62].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Ganesan discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“Bottom device package 150 may be a core chip such as a microprocessor unit and includes die 170, substrate 160, inter-package contact pads 155 on the top side of bottom package 150, micro balls 180 attached to inter-package contact pads 155, and second level interconnect pads 190 attachable to a motherboard (not shown).” Ganesan, [1:28-1:33].</p>

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>“Planar stiffener 200 also includes a plurality of planar contact pads 240 disposed on the bottom side of stiffener 200. In the PoP assembly, planar contact pads 240 are electrically connected to bottom device package 150, for example, by way of micro balls 180.” Ganesan, [2:62-2:67].</p> <p>“Planar contact pads 240 disposed on the bottom side of stiffener 220 are connected to inter-package contact pads 155 of bottom device package 150 by way of conductive micro balls 180. Stiffener 220 may be attached to bottom device package 150 before attaching top device package 100 to the top side of stiffener 220. The layout of planar contact pads 240 on the bottom side of stiffener 220 may match the layout of inter-package contact pads 155 of bottom device package 150.” Ganesan, [3:22-3:30].</p>
--	---

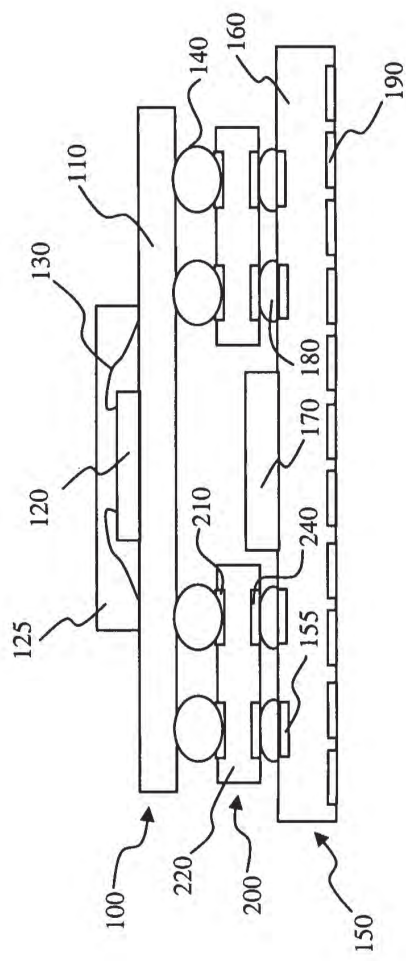


FIG. 2

Ganesan, FIG. 2

“The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220.” Ganesan, [3:60-4:1].

“In operation 700, micro balls 180 are placed on inter-package contact pads 155 of bottom device package 150 and reflowed to form solder interconnection.” Ganesan, [4:35-4:37].

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>“In operation 720 (FIG. 8), planar stiffener 200 is mounted on the top side of bottom device package 150. Planar contact pads 240 on the bottom side of stiffener 200 are aligned and attached to micro balls 180 connected to inter-package contact pads 155 of bottom device package 150. The assembly of stiffener 200 and bottom device package 150 are reflowed to form permanent interconnection.” Ganesan, [4:49-4:55].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Ganesan discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“The bottom side of top device package 100 includes micro balls 140 reflowed and electrically connected to micro balls 180 on the top side of bottom device package 150.” Ganesan, [1:38-1:41].</p> <p>“Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200. Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140. Top device package 100 may be a memory package or cache unit or any other device package suited for connection with</p>

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>the type of device of bottom device package 150. Planar stiffener 200 also includes a plurality of planar contact pads 240 disposed on the bottom side of stiffener 200. In the PoP assembly, planar contact pads 240 are electrically connected to bottom device package 150, for example, by way of micro balls 180.” Ganesan, [2:56-2:67].</p> <p>“Known process to fabricate package substrate may be used to form stiffener 200 and the key process steps may include: drilling through-holes in core layer 630 ; plating the sidewalls of through-holes; disposing plug material 610 in the through-holes; forming electrically conductive planar contact pads 210 and 240 ; forming a solder-wettable finish on planar contact pads 210 and 240 ; and forming recess 330 in stiffener 200. In operation 720 (FIG. 8), planar stiffener 200 is mounted on the top side of bottom device package 150. Planar contact pads 240 on the bottom side of stiffener 200 are aligned and attached to micro balls 180 connected to inter-package contact pads 155 of bottom device package 150. The assembly of stiffener 200 and bottom device package 150 are reflowed to form permanent interconnection. After reflow, die 170 is attached to bottom device package 150 attached to stiffener 200. The assembly of bottom device package 150 and stiffener 200 (in panel form) may then be singulated to yield individual assemblies of bottom device package 150 with stiffener 200 attached thereto.” Ganesan, [3:12-3:31].</p> <p>“Planar contact pads 240 disposed on the bottom side of stiffener 220 are connected to inter-package contact pads 155 of bottom device package 150 by way of conductive micro balls 180.” Ganesan, [3:22-3:25].</p> <p>“Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [3:37-3:39].</p>
--	---

“The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220.” Ganesan, [3:60-4:1].

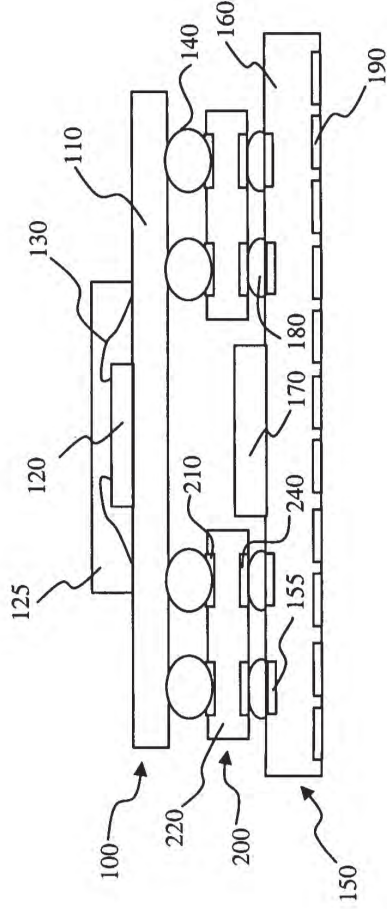


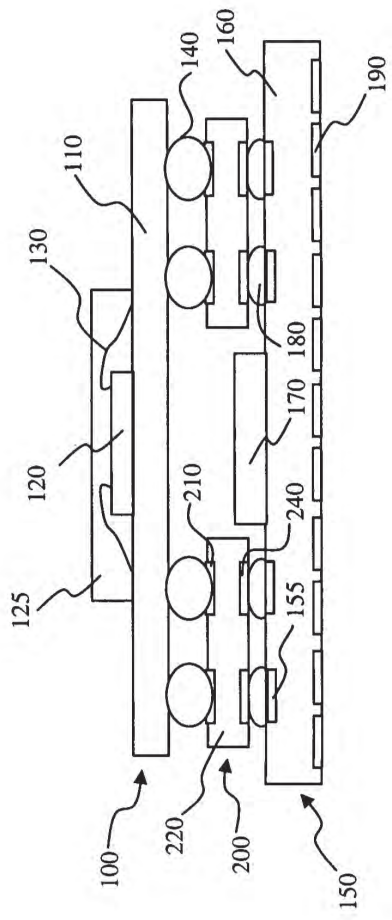
FIG. 2

Ganesan, FIG. 2

To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Ganesan discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Bottom device package 150 may be a core chip such as a microprocessor unit and includes die 170, substrate 160, inter-package contact pads 155 on the top side of bottom package 150, micro balls 180 attached to inter-package contact pads 155, and second level interconnect pads 190 attachable to a motherboard (not shown). Top device package 100 is stacked onto bottom package 150 to form an electrical connection therebetween.” Ganesan, [1:28-1:34].</p> <p>“FIG. 5 is a perspective view of an assembled PoP assembly having a top device package and a bottom device package attached to an interconnect stiffener according to an embodiment. Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [2:12-2:19].</p> <p>“FIG. 2 is a cross-sectional view of a package-on-package (PoP) assembly having an interconnect stiffener according to an embodiment. The PoP assembly is attachable to a motherboard (not shown) via second level interconnect pads 190 disposed on the bottom side of bottom device package 150. The PoP assembly includes bottom device package 150 interconnected to planar interconnect stiffener 200. Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package</p>

	<p>150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170.” Ganesan, [2:45-2:55].</p> <p>“Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150.” Ganesan, [3:3-3:5].</p> <div></div> <p style="text-align: center;">FIG. 2</p> <p>Ganesan, FIG. 2</p> <p>“FIG. 4 is an exploded perspective view of a top device package and a bottom device package having an interconnect stiffener attached to the top side of the bottom device package according to an embodiment. Stiffener 220 is attached to bottom device package 150 via respective contact pads 155 and 240.” Ganesan, [3:17-3:22].</p>
--	---

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>“After reflow, die 170 is attached to bottom device package 150 attached to stiffener 200.” Ganesan, [4:55-4:57].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Ganesan discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Bottom device package 150 may be a core chip such as a microprocessor unit and includes die 170, substrate 160, inter-package contact pads 155 on the top side of bottom package 150, micro balls 180 attached to inter-package contact pads 155, and second level interconnect pads 190 attachable to a motherboard (not shown).” Ganesan, [1:28-1:33].</p> <p>“Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package 150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170.” Ganesan, [2:51-2:55].</p> <p>“Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150.” Ganesan, [3:3-3:5].</p>

“FIG. 4 is an exploded perspective view of a top device package and a bottom device package having an interconnect stiffener attached to the top side of the bottom device package according to an embodiment. Stiffener 220 is attached to bottom device package 150 via respective contact pads 155 and 240.” Ganesan, [3:17-3:22].

“The assembly of stiffener 200 and bottom device package 150 are reflowed to form permanent interconnection. After reflow, die 170 is attached to bottom device package 150 attached to stiffener 200.” Ganesan, [4:53-4:57].

“After reflow, die 170 is attached to bottom device package 150 attached to stiffener 200.” Ganesan, [4:55-4:57].

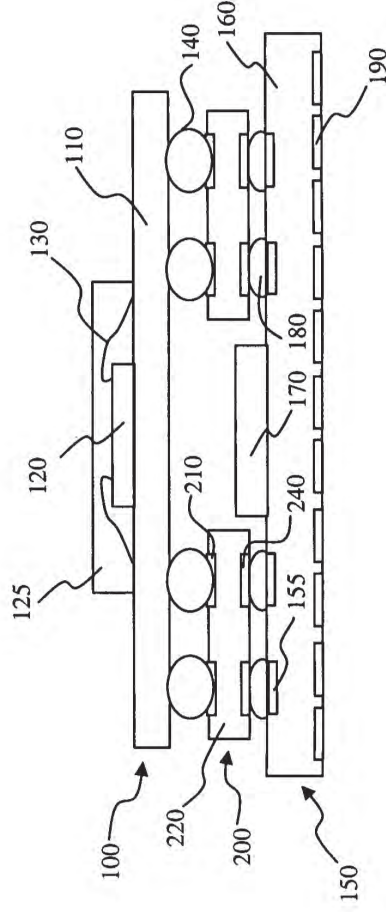


FIG. 2

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>Ganesan, FIG. 2</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Ganesan discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

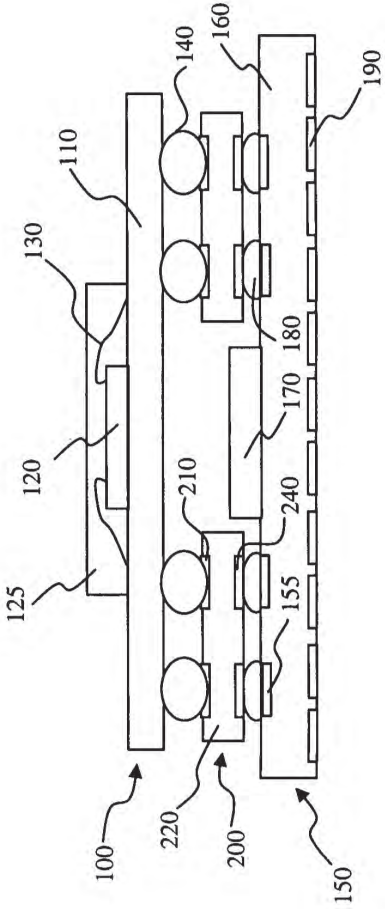
	<div></div> <div><p>FIG. 2</p></div> <div><p>Ganesan, FIG. 2</p></div> <div><p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Ganesan discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Top device package 100 is stacked onto bottom package 150 to form an electrical connection therebetween. Top device package 100 may be a peripheral chip such as a memory or cache unit, and may include die 120 interconnected to substrate 110 via wire bond 130 and encapsulated by molding 125. The bottom side of top device package 100 includes micro balls 140 reflowed and electrically connected to micro balls 180 on the top side of bottom device package 150.” Ganesan, [1:33-1:41].</p> <p>“FIG. 2 is a cross-sectional view of a package-on-package (PoP) assembly having an interconnect stiffener according to an embodiment. The PoP assembly is attachable to a motherboard (not shown) via second level interconnect pads 190 disposed on the bottom side of bottom device package 150. The PoP assembly includes bottom device package 150 interconnected to planar interconnect stiffener 200. Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package 150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170. Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200. Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140.” Ganesan, [2:45-2:59].</p> <p>“Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150.” Ganesan, [3:3-3:5].</p>
---	--

	<p>“After reflow, die 170 is attached to bottom device package 150 attached to stiffener 200.” Ganesan, [4:55-4:57].</p>  <p>FIG. 2</p> <p>Ganesan, FIG. 2</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	<p>Ganesan discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Top device package 100 may be a peripheral chip such as a memory or cache unit, and may include die 120 interconnected to substrate 110 via wire bond 130 and encapsulated by molding 125. The bottom side of top device package 100 includes micro balls 140 reflowed and electrically connected to micro balls 180 on the top side of bottom device package 150.” Ganesan, [1:35-1:41].</p>

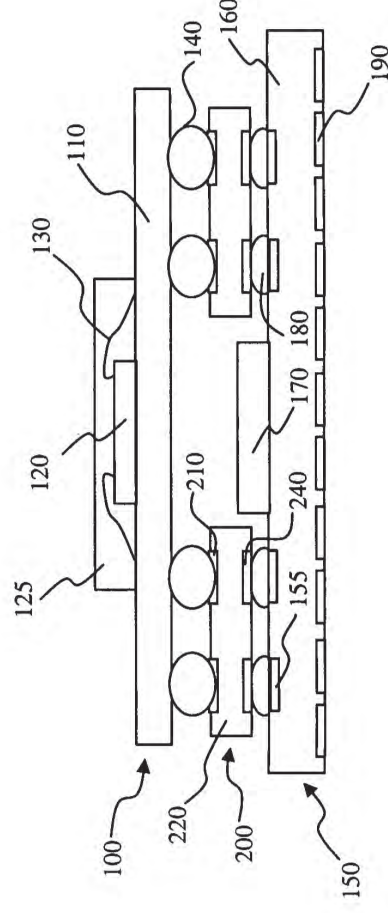


FIG. 2

Ganesan, FIG. 2

“FIG. 5 is a perspective view of an assembled PoP assembly having a top device package and a bottom device package attached to an interconnect stiffener according to an embodiment. Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [2:12-2:19].

“FIG. 2 is a cross-sectional view of a package-on-package (PoP) assembly having an interconnect stiffener according to an embodiment. The PoP assembly is attachable to a motherboard (not shown) via second level interconnect pads 190 disposed on the bottom side of bottom device package 150. The PoP assembly includes bottom device package 150

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>interconnected to planar interconnect stiffener 200. Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package 150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170. Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200. Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140. Top device package 100 may be a memory package or cache unit or any other device package suited for connection with the type of device of bottom device package 150.” Ganesan, [2:45-2:62].</p> <p>“FIG. 3 is an exploded perspective view of a PoP assembly having an interconnect stiffener according to an embodiment. Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small through openings through which planar contact pads 210 and 240 are formed.” Ganesan, [3:1-3:7].</p> <p>“Top device package 100 may subsequently be attached to planar contact pads 210 on the top side of stiffener 200 to form a package-on-package assembly.” Ganesan, [4:60-4:62].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p>	<p>Ganesan discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The bottom side of top device package 100 includes micro balls 140 reflowed and electrically connected to micro balls 180 on the top side of bottom device package 150.” Ganesan, [1:38-1:41].</p> <p>“Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140.” Ganesan, [2:57-2:60].</p> <p>“Planar stiffener 200 also includes a plurality of planar contact pads 240 disposed on the bottom side of stiffener 200. In the PoP assembly, planar contact pads 240 are electrically connected to bottom device package 150, for example, by way of micro balls 180.” Ganesan, [2:62-2:67].</p> <p>“Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [3:37-3:39].</p> <p>“The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the</p>

	<p>interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220.” Ganesan, [3:60-4:1].</p> <p>“Planar contact pads 240 on the bottom side of stiffener 200 are aligned and attached to micro balls 180 connected to inter-package contact pads 155 of bottom device package 150.” Ganesan, [4:50-4:53].</p> <p>FIG. 2</p> <p>Ganesan, FIG. 2</p>
--	--

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Ganesan discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 5 is a perspective view of an assembled PoP assembly having a top device package and a bottom device package attached to an interconnect stiffener according to an embodiment. Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [2:12-2:19].</p> <p>“FIG. 2 is a cross-sectional view of a package-on-package (PoP) assembly having an interconnect stiffener according to an embodiment. The PoP assembly is attachable to a</p>

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>motherboard (not shown) via second level interconnect pads 190 disposed on the bottom side of bottom device package 150. The PoP assembly includes bottom device package 150 interconnected to planar interconnect stiffener 200. Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package 150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170. Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200. Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140. Top device package 100 may be a memory package or cache unit or any other device package suited for connection with the type of device of bottom device package 150.” Ganesan, [2:45-2:62].</p> <p>“Planar stiffener 200 also includes a plurality of planar contact pads 240 disposed on the bottom side of stiffener 200. In the PoP assembly, planar contact pads 240 are electrically connected to bottom device package 150, for example, by way of micro balls 180. FIG. 3 is an exploded perspective view of a PoP assembly having an interconnect stiffener according to an embodiment. Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small through openings through which planar contact pads 210 and 240 are formed. Planar contact pads 210 and 240 formed on substrate 220 each includes a solder-wettable surface finish so that during reflow, the solder materials of micro balls 140 and 180 can melt, wet and form permanent conductive connection between stiffener 200 and the top and bottom packages 100, 150. Various types of solder-wettable surface finish known in the art such as Electroless Nickel/Immersion Gold (ENIG), ENIG+Electroless Gold (ENIG+EG) and Nickel-Palladium-Gold (NiPdAu) are suitable for planar contact pads 210 and 240. FIG. 4 is an exploded perspective view of a top device package and a bottom device package having an interconnect stiffener attached to the top side of the bottom device package according to</p>
--	---

	<p>an embodiment. Stiffener 220 is attached to bottom device package 150 via respective contact pads 155 and 240. Planar contact pads 240 disposed on the bottom side of stiffener 220 are connected to inter-package contact pads 155 of bottom device package 150 by way of conductive micro balls 180.” Ganesan, [2:62-3:25].</p> <p style="text-align: center;">FIG. 2</p> <p>Ganesan, FIG. 2</p> <p>“Known process to fabricate package substrate may be used to form stiffener 200 and the key process steps may include: drilling through-holes in core layer 630 ; plating the sidewalls of through-holes; disposing plug material 610 in the through-holes; forming electrically conductive planar contact pads 210 and 240 ; forming a solder-wettable finish on planar</p>
--	--

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>contact pads 210 and 240 ; and forming recess 330 in stiffener 200. In operation 720 (FIG. 8), planar stiffener 200 is mounted on the top side of bottom device package 150. Planar contact pads 240 on the bottom side of stiffener 200 are aligned and attached to micro balls 180 connected to inter-package contact pads 155 of bottom device package 150. The assembly of stiffener 200 and bottom device package 150 are reflowed to form permanent interconnection. After reflow, die 170 is attached to bottom device package 150 attached to stiffener 200. The assembly of bottom device package 150 and stiffener 200 (in panel form) may then be singulated to yield individual assemblies of bottom device package 150 with stiffener 200 attached thereto.” Ganesan, [3:12-3:31].</p> <p>“FIG. 6 is a cross-sectional view of a PoP interconnect stiffener according to an embodiment. Stiffener 200 includes substrate 220 to provide structural support and upon which contact pads 210, 240 are fabricated. Stiffener 200 includes solder resist layer 620 disposed on the top surface and bottom surface of core layer 630. For an embodiment, core layer 630 is a cored substrate fabricated from known polymeric materials such as bismaleimide triazine (BT), polyimide, and liquid crystalline (LC) polymer. However, other materials suitable for core layer 630 are not precluded in other embodiments of the invention. Substrate 220 may include a coefficient of thermal expansion (CTE) of approximately between 15 and 25 ppm. Substrate 220 may also include a flexural modulus of approximately between 15 and 30 GPa. The properties of stiffener 200 will be designed to provide acceptable end-of-line warpage of the assembly of top device package 100 and stiffener 200 and/or the reliability of the interconnections between top device package 100 and stiffener 200. Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220. FIG. 6 illustrates a via-in-pad design in which plug material 610 is disposed between core layer 630 and between planar contact pads 210, 240. Plug material 610 forms part of the material for substrate 220 to provide structural rigidity and foundation</p>
--	--

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

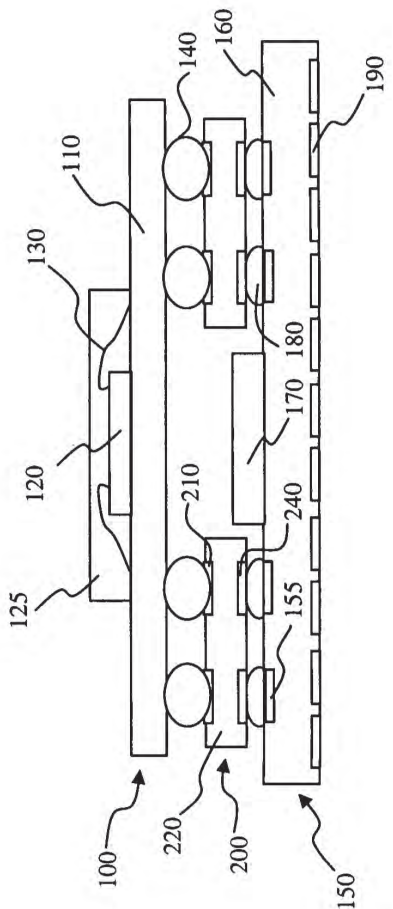
	<p>to contact pads 210 and 240 and is made from known materials such as silica filled epoxy composite or commercially available solder resist materials.” Ganesan, [3:46-4:7].</p> <p>“FIG. 7 is a cross-sectional view of a PoP interconnect stiffener according to another embodiment. FIG. 7 embodies a via-off-pad design in which core layer 630 extends in planar contact pads 210 and 240 regions, and plug material 610 is disposed between solder resist layers 520 and in substrate 220.” Ganesan, [4:21-4:26].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector, and bottom ends of the plurality of bottom metal pads of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Ganesan discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>“FIG. 2 is a cross-sectional view of a package-on-package (PoP) assembly having an interconnect stiffener according to an embodiment. The PoP assembly is attachable to a motherboard (not shown) via second level interconnect pads 190 disposed on the bottom side of bottom device package 150. The PoP assembly includes bottom device package 150 interconnected to planar interconnect stiffener 200. Bottom device package 150 may be any semiconductor package depending on the application. For example, bottom device package 150 may be a semiconductor logic package, an application processor, or a memory package with an integrated circuit in die 170. Planar stiffener 200 includes a plurality of planar contact pads 210 disposed on the top side of stiffener 200. Planar contact pads 210 are configured to be electrically connected to top device package 100, for example, by way of micro balls 140.” Ganesan, [2:45-2:59].</p> <p>“Planar stiffener 200 also includes a plurality of planar contact pads 240 disposed on the bottom side of stiffener 200. In the PoP assembly, planar contact pads 240 are electrically connected to bottom device package 150, for example, by way of micro balls 180. FIG. 3 is an exploded perspective view of a PoP assembly having an interconnect stiffener according to an embodiment. Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small through openings through which planar contact pads 210 and 240 are formed. Planar contact pads 210 and 240 formed on substrate 220 each includes a solder-wettable surface finish so that during reflow, the solder materials of micro balls 140 and 180 can melt, wet and form permanent conductive connection between stiffener 200 and the top and bottom packages 100, 150. Various types of solder-wettable surface finish known in the art such as Electroless Nickel/Immersion Gold (ENIG), ENIG+Electroless Gold (ENIG+EG) and Nickel-Palladium-Gold (NiPdAu) are suitable for planar contact pads 210 and 240. FIG. 4 is an exploded perspective view of a top device package and a bottom device package having</p>
--	---

	<p>an interconnect stiffener attached to the top side of the bottom device package according to an embodiment. Stiffener 220 is attached to bottom device package 150 via respective contact pads 155 and 240. Planar contact pads 240 disposed on the bottom side of stiffener 220 are connected to inter-package contact pads 155 of bottom device package 150 by way of conductive micro balls 180. Stiffener 220 may be attached to bottom device package 150 before attaching top device package 100 to the top side of stiffener 220.” Ganesan, [2:62-3:27].</p>  <p style="text-align: center;">FIG. 2</p> <p>Ganesan, FIG. 2</p> <p>“Planar interconnect stiffener 200 includes substrate 220 defining a through recess 330 adapted to house die 170 of bottom device package 150. Stiffener 200 also includes small</p>
--	--

Appendix A-9 - Invalidity of U.S. Patent No. 9859202 in view of Ganesan - U.S. Patent No. 8513792

	<p>through openings through which planar contact pads 210 and 240 are formed.” Ganesan, [3:3-3:7].</p> <p>“Stiffener 200 also includes conductive traces 600 fabricated in substrate 220 to electrically interconnect planar contact pads 210 on the top side of stiffener 220 with planar contact pads 240 on the bottom side of stiffener 220. FIG. 6 illustrates a via-in-pad design in which plug material 610 is disposed between core layer 630 and between planar contact pads 210, 240. Plug material 610 forms part of the material for substrate 220 to provide structural rigidity and foundation to contact pads 210 and 240 and is made from known materials such as silica filled epoxy composite or commercially available solder resist materials.” Ganesan, [3:25-3:35].</p> <p>“Top device package 100 is connected to stiffener 220 via interconnects such as micro balls 140 disposed on planar contact pads 210 on the top side of stiffener 220.” Ganesan, [3:37-3:39].</p> <p>“In operation 720 (FIG. 8), planar stiffener 200 is mounted on the top side of bottom device package 150. Planar contact pads 240 on the bottom side of stiffener 200 are aligned and attached to micro balls 180 connected to inter-package contact pads 155 of bottom device package 150. The assembly of stiffener 200 and bottom device package 150 are reflowed to form permanent interconnection.” Ganesan, [4:49-4:55].</p> <p>To the extent Plaintiff contends that Ganesan fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

U.S. Patent Publication No. 20150061142 (“Hsu '142”) is titled Ultra Fine Pitch PoP Coreless Package and lists Jun Chung Hsu and Jun Zhai as inventors. Hsu '142 is assigned to Apple Inc. Hsu '142 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the '202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff's apparent infringement theory.² Hsu '142 is a U.S. patent publication that was filed November 25, 2013 and published March 5, 2015. Hsu '142 claims priority to a provisional application filed on August 30, 2013. Hsu '142 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Hsu '142, or otherwise rendered obvious by disclosures and teachings of Hsu '142, including under TopWire's apparent interpretation of the Asserted Claims as Samsung understands them from TopWire's Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Hsu '142 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Hsu '142 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung's other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung's Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Hsu '142, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire's March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court's order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire's apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung's interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

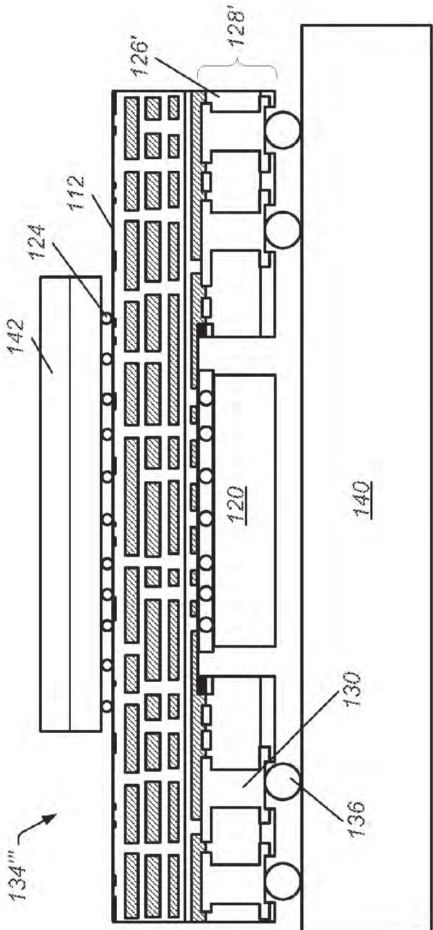
Where the chart below states that Hsu '142 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Hsu '142 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Hsu '142 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

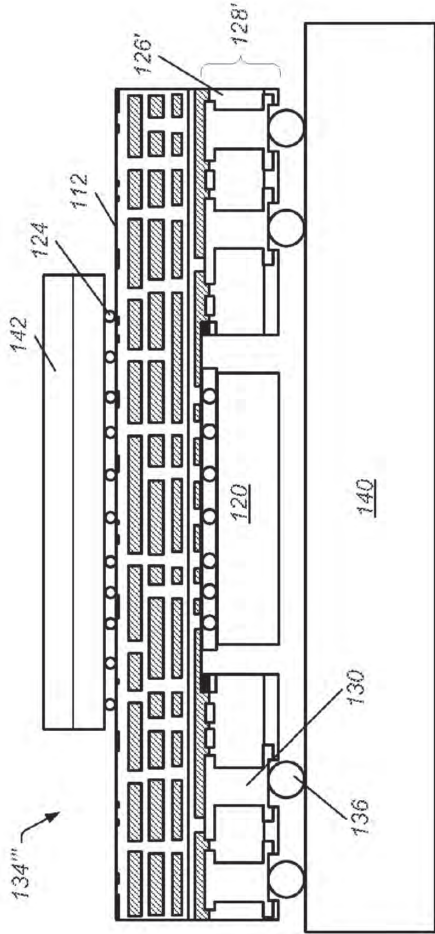
Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Hsu '142 discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIGS. 1A-K depict cross-sectional representations of an embodiment of a process flow for forming a bottom package of a PoP package. FIG. 1A depicts a cross-sectional representation of an embodiment of carrier 100. Carrier 100 may be any carrier suitable for supporting and carrying a coreless substrate or similar thin substrate. Carrier 100 may be, for example, a temporary substrate for a coreless substrate or other thin substrate.” Hsu '142, [0023].</p>

	<p>“FIGS. 2A-K depict cross-sectional representations of an alternative embodiment of a process flow for forming a bottom package of a PoP package. FIG. 2A depicts a cross-sectional representation of an embodiment of core material 102 with metal layer 108 filling vias 106 through the core material. Vias 106 may be formed, for example, by laser drilling in core material 102. Metal layer 108 may be formed, for example, by paste hole (PTH) filling of vias 106. Metal layer 108 may be copper or another suitable conductive metal. Metal layer 108 may also cover portions of the surface of core material 102. In some embodiments, portions of metal layer 108 on the surface of core material 102 is patterned or otherwise defined to provide metal features on the surface of the core material. In certain embodiments, barrier layer 110 is formed on core material 102.” Hsu '142, [0038].</p> <p>“Bottom package 126 may be coupled to a top package (e.g., a memory package) to form a PoP package. FIG. 4 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to top package 132 to form PoP package 134. FIG. 5 depicts an embodiment of bottom package 126' (shown in FIG. 2K) coupled to top package 132 to form PoP package 134'. Top package 132 may include, for example, a memory die or a multilayer printed circuit board (MLB). As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].</p> <p>“FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a</p>
--	---

	<p>memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu ’142, [0048].</p>  <p style="text-align: center;"><i>FIG. 9</i></p> <p>Hsu ’142, FIG. 9</p> <p>“In some embodiments, a bottom package as described herein (e.g., bottom package 126 or bottom package 126’) is flipped over and the reinforcement layer is coupled to a printed circuit board (PCB)(e.g., the top package is a PCB but the entire assembly is flipped over so that the PCB is below the bottom package). A memory die may then be coupled to the opposite side of the bottom package from the printed circuit board. FIG. 8 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to printed circuit board (PCB) 140 and memory die 142.” Hsu ’142, [0048].</p>
--	--

<p>[1.A] a bottom package substrate;</p>	<p>Hsu '142 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 depicts a top view of an embodiment of bottom package 126. Bottom package 126 may be made using either of the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. As shown in FIG. 3, die 120 is located on substrate 112 and substantially surrounded by reinforcement layer 128 and terminals 130 in a fan-out wafer level package (FOWLP) arrangement. While the FOWLP arrangement is shown, it is to be understood that other wafer package arrangements may also be contemplated using the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. Terminals 130 may correspond to locations of metal layer 108 filled vias 106 (shown in FIGS. 1K and 2K).” Hsu '142, [0045].</p> <p>“Bottom package 126 may be coupled to a top package (e.g., a memory package) to form a PoP package. FIG. 4 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to top package 132 to form PoP package 134. FIG. 5 depicts an embodiment of bottom package 126' (shown in FIG. 2K) coupled to top package 132 to form PoP package 134'. Top package 132 may include, for example, a memory die or a multilayer printed circuit board (MLB). As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].</p> <p>“In some embodiments, a bottom package as described herein (e.g., bottom package 126 or bottom package 126') is flipped over and the reinforcement layer is coupled to a printed circuit board (PCB)(e.g., the top package is a PCB but the entire assembly is flipped over so that the PCB is below the bottom package). A memory die may then be coupled to the</p>
--	--

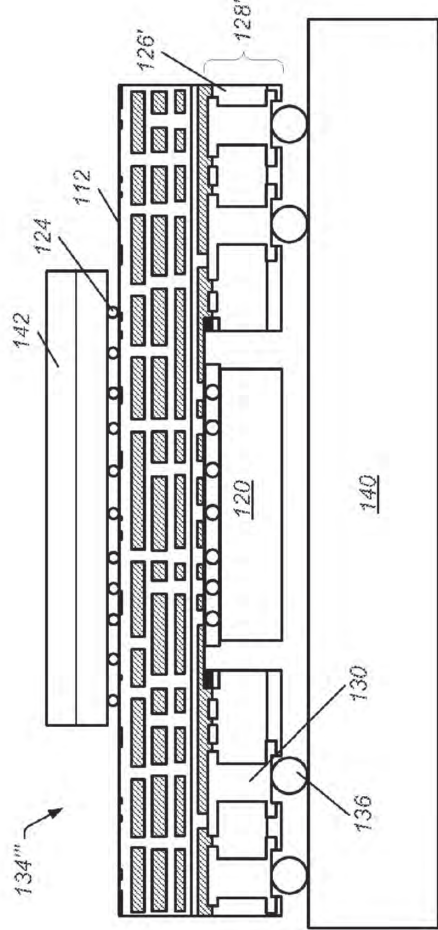
opposite side of the bottom package from the printed circuit board. FIG. 8 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to printed circuit board (PCB) 140 and memory die 142. FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 112 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack." Hsu '142, [0048].



Hsu '142, FIG. 9

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	<p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Hsu '142 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 5 depicts an embodiment of bottom package 126' (shown in FIG. 2K) coupled to top package 132 to form PoP package 134'. Top package 132 may include, for example, a memory die or a multilayer printed circuit board (MLB). As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].</p> <p>“FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu '142, [0048].</p>

	 <p><i>FIG. 9</i></p> <p>Hsu '142, FIG. 9</p> <p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom</p>	<p>Hsu '142 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

package substrate and the top package substrate, wherein	<p>“While the FOWLP arrangement is shown, it is to be understood that other wafer package arrangements may also be contemplated using the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. Terminals 130 may correspond to locations of metal layer 108 filled vias 106 (shown in FIGS. 1K and 2K).” Hsu '142, [0045].</p> <p>“As shown in FIG. 3, die 120 is located on substrate 112 and substantially surrounded by reinforcement layer 128 and terminals 130 in a fan-out wafer level package (FOWLP) arrangement.” Hsu '142, [0045].</p> <p>“top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package.” Hsu '142, [0046].</p>
--	--

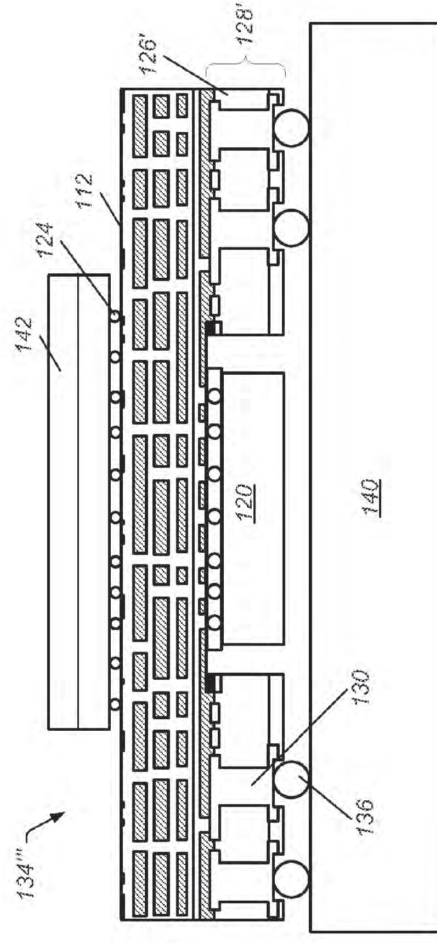


FIG. 9

Hsu '142, FIG. 9

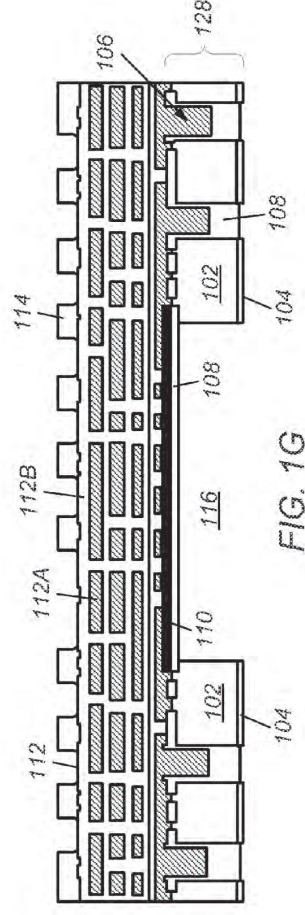
“In some embodiments, a bottom package as described herein (e.g., bottom package 126 or bottom package 126′) is flipped over and the reinforcement layer is coupled to a printed circuit board (PCB)(e.g., the top package is a PCB but the entire assembly is flipped over so that the PCB is below the bottom package). A memory die may then be coupled to the opposite side of the bottom package from the printed circuit board. FIG. 8 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to printed circuit board (PCB) 140 and memory die 142. FIG. 9 depicts another embodiment of bottom package 126′ (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126′) by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	<p>non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu ’142, [0048].</p> <p>To the extent Plaintiff contends that Hsu ’142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Hsu ’142 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Core material 102 may be any suitable material known in the art for use as a core material in integrated circuit packages. For example, core material 102 may be a dielectric material such as, but not limited to, a ceramic or resin material.” Hsu ’142, [0024].</p> <p>“In certain embodiments, after coupling core material 102 to carrier 100, vias 106 (e.g., through holes) are formed in the core material and at least partially filled with metal layer 108, as shown in FIG. 1C. Vias 106 may be formed, for example, by laser drilling in core material 102. After vias 106 are formed, additional metal layer 108 (e.g., copper) may be deposited in the vias. In some embodiments, metal layer 108 only partially fills vias 106. In some embodiments, portions of metal layer 108 on the surface of core material 102 is patterned or otherwise defined to provide metal features on the surface of the core material.” Hsu ’142, [0026].</p>

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	<p>“As shown in FIG. 1D, core material 102, laminate layer 104, and metal layer 108 form reinforcement layer 128. Reinforcement layer 128 provides reinforcement for substrate 112. For example, reinforcement layer 128 may support substrate 112 and stiffen the substrate (e.g., make the substrate more rigid). Stiffening substrate 112 may allow for better handling of the substrate and provide more stiffness to a bottom package made using the substrate.” Hsu '142, [0029].</p> <p>“After carrier 100 is removed, a cavity or opening may be formed to allow connection of a die to substrate 112 through core material 102 (e.g., the cavity or opening is formed to provide a terminal (bump) pad area for a die coupled to the package). FIGS. 1G-1J depict an embodiment of a process for forming the cavity or opening providing the terminal pad area for the die. As shown in FIG. 1G, core material 102 may be removed to form opening 116. Opening 116 may be formed in the area defined by the dotted lines depicted in FIGS. 1C-F. Core material 102 may be removed, for example, by laser ablation of the core material. In certain embodiments, the core material removal process (e.g., the laser ablation process) is stopped by the presence of metal layer 108.” Hsu '142, [0031].</p>
--	---



Hsu '142, FIG. 1G

To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Hsu '142 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.

See, e.g.:

“In certain embodiments, after coupling core material 102 to carrier 100, vias 106 (e.g., through holes) are formed in the core material and at least partially filled with metal layer 108, as shown in FIG. 1C. Vias 106 may be formed, for example, by laser drilling in core material 102. After vias 106 are formed, additional metal layer 108 (e.g., copper) may be deposited in the vias.” Hsu ’142, [0026].

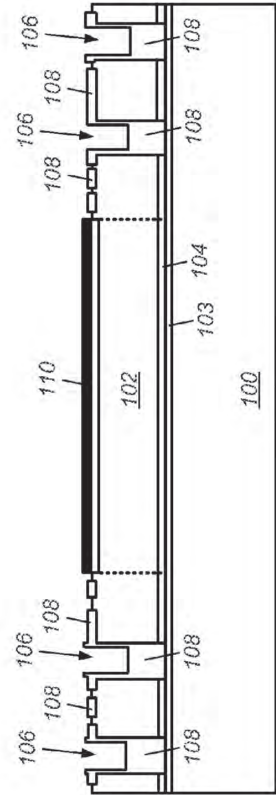


FIG. 1C

Hsu '142, FIG. 1C

“As shown in FIG. 1D, core material 102, laminate layer 104, and metal layer 108 form reinforcement layer 128. Reinforcement layer 128 provides reinforcement for substrate 112.” Hsu '142, [0029].

“FIG. 2A depicts a cross-sectional representation of an embodiment of core material 102 with metal layer 108 filling vias 106 through the core material. Vias 106 may be formed, for example, by laser drilling in core material 102. Metal layer 108 may be formed, for example, by paste hole (PTH) filling of vias 106. Metal layer 108 may be copper or another suitable conductive metal.” Hsu '142, [0038].

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	<p>“Core material 102, laminate layer 104, and metal layer 108 form reinforcement layer 128’. Reinforcement layer 128’, shown in FIG. 2D, is substantially similar to reinforcement layer 128, shown in FIG. 1D, with a difference being the substantially complete filling of vias 106 in core material 102 with metal layer 108 (e.g., the metal layer substantially fills the vias in the core material due to the paste hole filling of the vias).” Hsu ’142, [0040].</p> <p>“Terminals 130 may correspond to locations of metal layer 108 filled vias 106 (shown in FIGS. 1K and 2K).” Hsu ’142, [0045].</p> <p>“In certain embodiments, the pitch between terminals 130 is relatively fine, as shown in FIG. 3. The fine pitch may be possible because of the use of metal layer 108 in vias 106 to define terminals 130 on bottom package 126 or 126’. Using metal layer 108 in vias 106 to define terminals 130 provides the terminals as post-like structures that can have small spacing between the terminals.” Hsu ’142, [0049].</p> <p>To the extent Plaintiff contends that Hsu ’142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;	<p>Hsu ’142 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 depicts a top view of an embodiment of bottom package 126. Bottom package 126 may be made using either of the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K.</p>

As shown in FIG. 3, die 120 is located on substrate 112 and substantially surrounded by reinforcement layer 128 and terminals 130 in a fan-out wafer level package (FOWLP) arrangement. While the FOWLP arrangement is shown, it is to be understood that other wafer package arrangements may also be contemplated using the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. Terminals 130 may correspond to locations of metal layer 108 filled vias 106 (shown in FIGS. 1K and 2K).” Hsu ’142, [0045].

“FIG. 9 depicts another embodiment of bottom package 126’ (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126’) by coupling terminals 136 on the PCB to terminals 130 on the bottom package.” Hsu ’142, [0048].

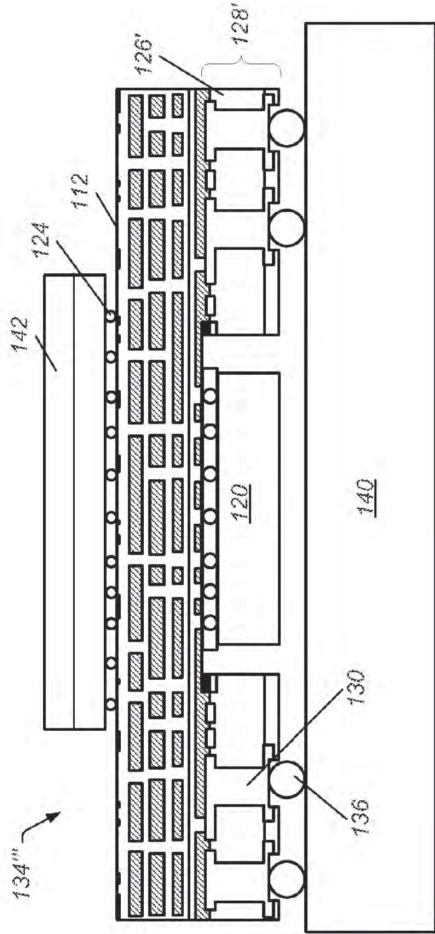


FIG. 9

	<p>Hsu '142, FIG. 9</p> <p>“Using metal layer 108 in vias 106 to define terminals 130 provides the terminals as post-like structures that can have small spacing between the terminals. Thus, terminals 136 on top package 132, shown in FIGS. 4 and 5, may be relatively small solder balls to avoid bridging between adjacent solder balls when the top package is coupled to bottom package 126 or 126’.” Hsu '142, [0049].</p> <p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Hsu '142 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 depicts a top view of an embodiment of bottom package 126. Bottom package 126 may be made using either of the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. As shown in FIG. 3, die 120 is located on substrate 112 and substantially surrounded by reinforcement layer 128 and terminals 130 in a fan-out wafer level package (FOWLP) arrangement. While the FOWLP arrangement is shown, it is to be understood that other wafer package arrangements may also be contemplated using the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. Terminals 130 may correspond to locations of metal layer 108 filled vias 106 (shown in FIGS. 1K and 2K).” Hsu '142, [0045].</p>

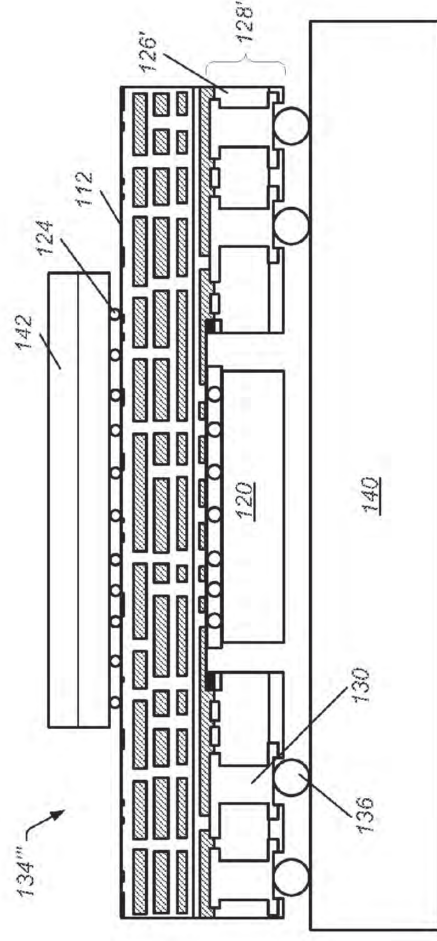


FIG. 9

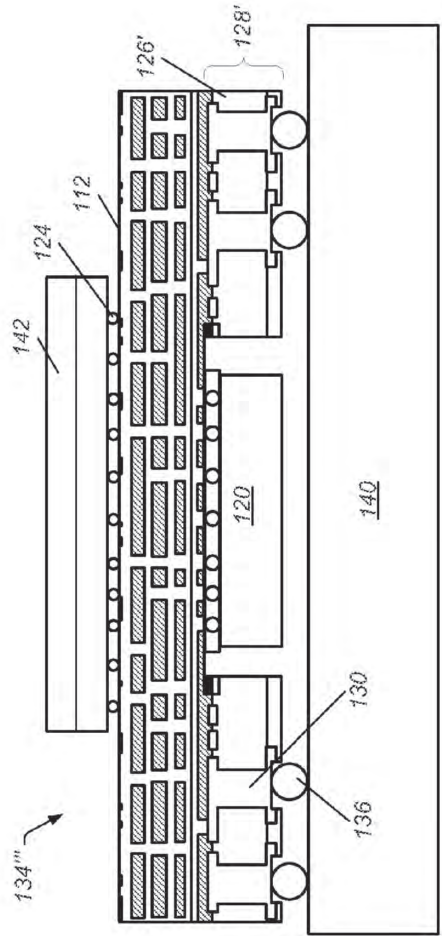
Hsu '142, FIG. 9

“FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package.” Hsu '142, [0048].

“Using metal layer 108 in vias 106 to define terminals 130 provides the terminals as post-like structures that can have small spacing between the terminals. Thus, terminals 136 on top package 132, shown in FIGS. 4 and 5, may be relatively small solder balls to avoid bridging between adjacent solder balls when the top package is coupled to bottom package 126 or 126’.” Hsu ’142, [0049].

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	<p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Hsu '142 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Terminals 124 may be used to couple substrate 112 and package 126 to a motherboard or a system printed circuit board (PCB).” Hsu '142, [0036].</p> <p>“Top package 132 may include, for example, a memory die or a multilayer printed circuit board (MLB). As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package.” Hsu '142, [0046].</p> <p>“In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124.” Hsu '142, [0048].</p>

	<div></div> <div><p>FIG. 9</p></div> <div><p>Hsu '142, FIG. 9</p></div> <div><p>“PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package.” Hsu '142, [0048].</p></div> <div><p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Hsu '142 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package.” Hsu '142, [0046].</p> <p>“Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].</p> <p>“PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package.” Hsu '142, [0048].</p>
---	---

	<div></div> <div><p>FIG. 9</p></div> <div><p>Hsu '142, FIG. 9</p></div> <div><p>“Thus, terminals 136 on top package 132, shown in FIGS. 4 and 5, may be relatively small solder balls to avoid bridging between adjacent solder balls when the top package is coupled to bottom package 126 or 126’.” Hsu '142, [0049].</p></div> <div><p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Hsu '142 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Bottom package 126 may be coupled to a top package (e.g., a memory package) to form a PoP package. FIG. 4 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to top package 132 to form PoP package 134. FIG. 5 depicts an embodiment of bottom package 126' (shown in FIG. 2K) coupled to top package 132 to form PoP package 134'. Top package 132 may include, for example, a memory die or a multilayer printed circuit board (MLB). As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].</p> <p>“FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu '142, [0048].</p>
---	--

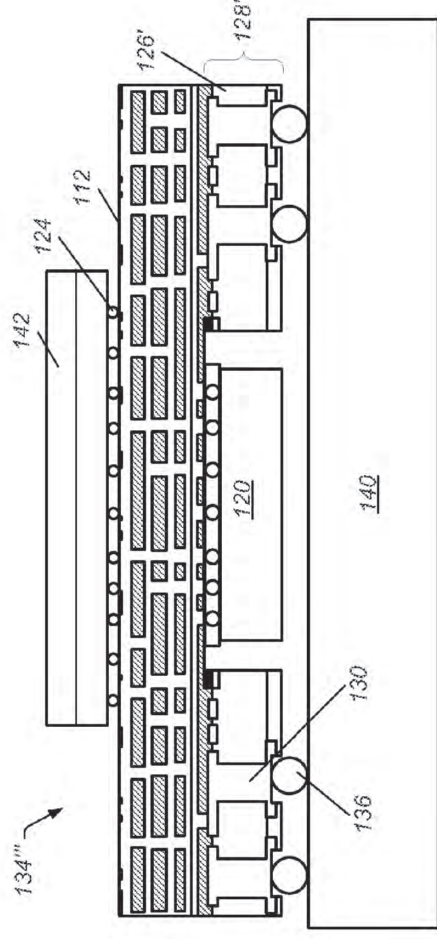


FIG. 9

Hsu '142, FIG. 9

“Using metal layer 108 in vias 106 to define terminals 130 provides the terminals as post-like structures that can have small spacing between the terminals. Thus, terminals 136 on top package 132, shown in FIGS. 4 and 5, may be relatively small solder balls to avoid bridging between adjacent solder balls when the top package is coupled to bottom package 126 or 126’.” Hsu '142, [0049].

To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hsu '142 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“After terminal pad 118 is formed in opening 116, die 120 may be coupled to substrate 112 in the opening, as shown in FIG. 1K. Die 120 may be, for example, a semiconductor chip, an integrated circuit die, a passive component, or a flip chip die. In certain embodiments, die 120 is a system on a chip (“SoC”). Die 120 may be coupled to substrate terminal pad 118 using one or more terminals 122. For example, terminals 122 may be solder balls coupled to solder pads on terminal pad 118. In certain embodiments, as shown in FIG. 1K, the top of die 120 is at a substantially similar height or a lower height than the top of laminate layer 104 on top of core material 102.” Hsu '142, [0035].</p> <p>“As shown in FIG. 3, die 120 is located on substrate 112 and substantially surrounded by reinforcement layer 128 and terminals 130 in a fan-out wafer level package (FOWLP) arrangement. While the FOWLP arrangement is shown, it is to be understood that other wafer package arrangements may also be contemplated using the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. Terminals 130 may correspond to locations of metal layer 108 filled vias 106 (shown in FIGS. 1K and 2K).” Hsu '142, [0045].</p>
---	---

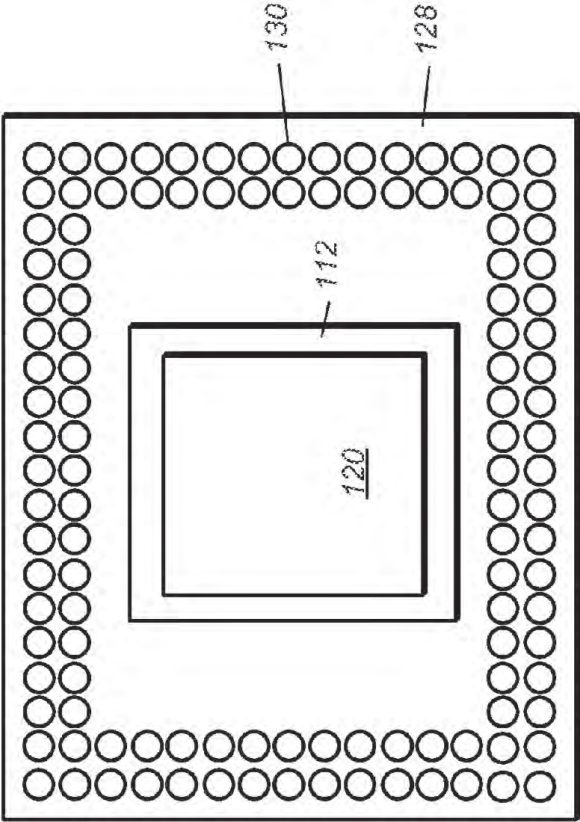


FIG. 3

Hsu '142, FIG. 3

“As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].

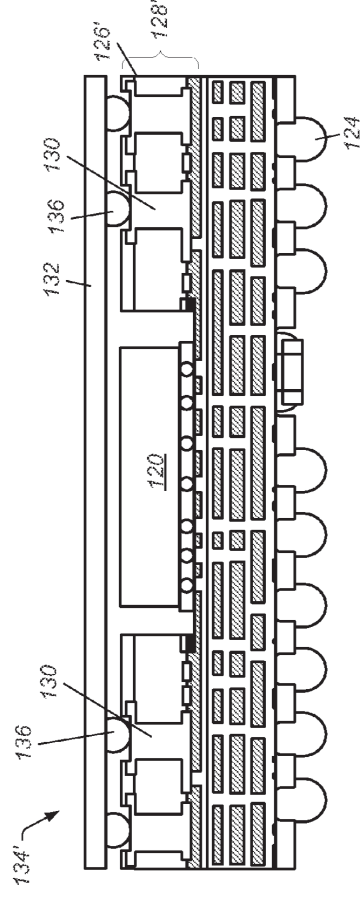
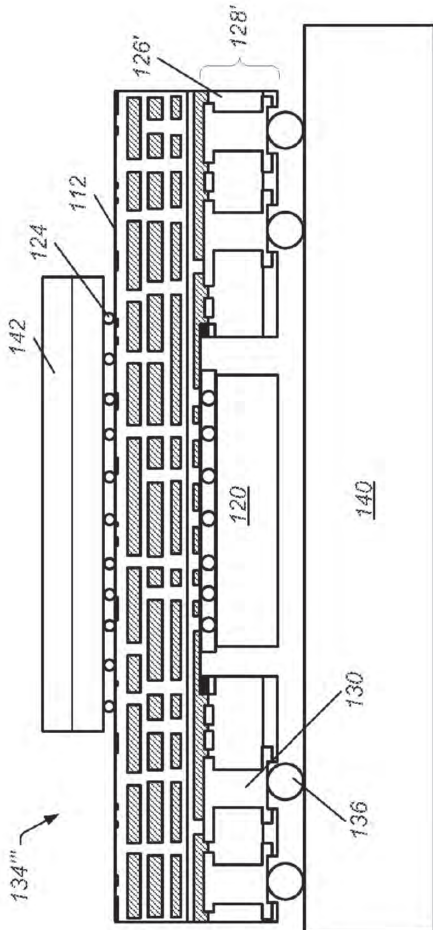


FIG. 5

Hsu '142, FIG. 5

“In some embodiments, a bottom package as described herein (e.g., bottom package 126 or bottom package 126') is flipped over and the reinforcement layer is coupled to a printed circuit board (PCB)(e.g., the top package is a PCB but the entire assembly is flipped over so that the PCB is below the bottom package). A memory die may then be coupled to the opposite side of the bottom package from the printed circuit board. FIG. 8 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to printed circuit board (PCB) 140 and memory die 142. FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu '142, [0048].

	 <p style="text-align: center;">FIG. 9</p> <p>Hsu '142, FIG. 9</p> <p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p> <p>See, e.g.:</p>
--	--

	<p>“After terminal pad 118 is formed in opening 116, die 120 may be coupled to substrate 112 in the opening, as shown in FIG. 1K. Die 120 may be, for example, a semiconductor chip, an integrated circuit die, a passive component, or a flip chip die. In certain embodiments, die 120 is a system on a chip (“SoC”). Die 120 may be coupled to substrate terminal pad 118 using one or more terminals 122. For example, terminals 122 may be solder balls coupled to solder pads on terminal pad 118. In certain embodiments, as shown in FIG. 1K, the top of die 120 is at a substantially similar height or a lower height than the top of laminate layer 104 on top of core material 102.” Hsu '142, [0035].</p> <p>“As shown in FIG. 3, die 120 is located on substrate 112 and substantially surrounded by reinforcement layer 128 and terminals 130 in a fan-out wafer level package (FOWLP) arrangement. While the FOWLP arrangement is shown, it is to be understood that other wafer package arrangements may also be contemplated using the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. Terminals 130 may correspond to locations of metal layer 108 filled vias 106 (shown in FIGS. 1K and 2K).” Hsu '142, [0045].</p>
--	--

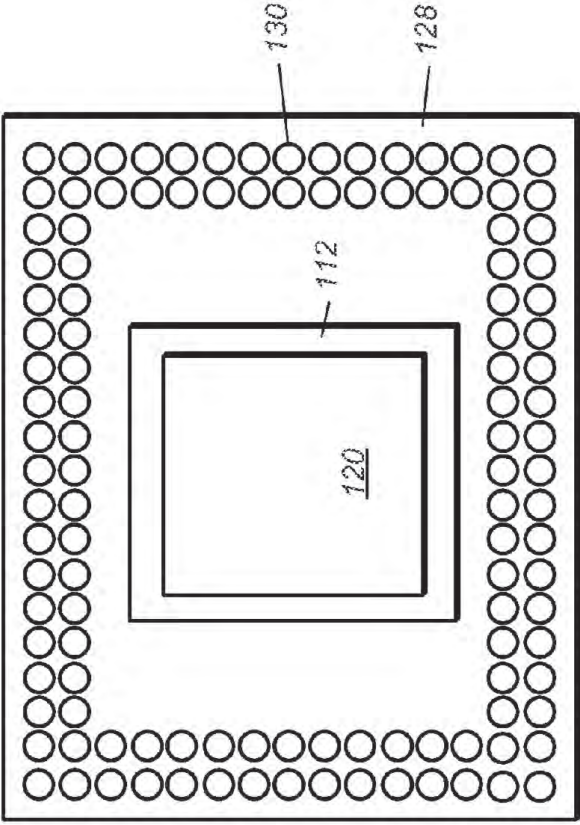


FIG. 3

Hsu '142, FIG. 3

“As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].

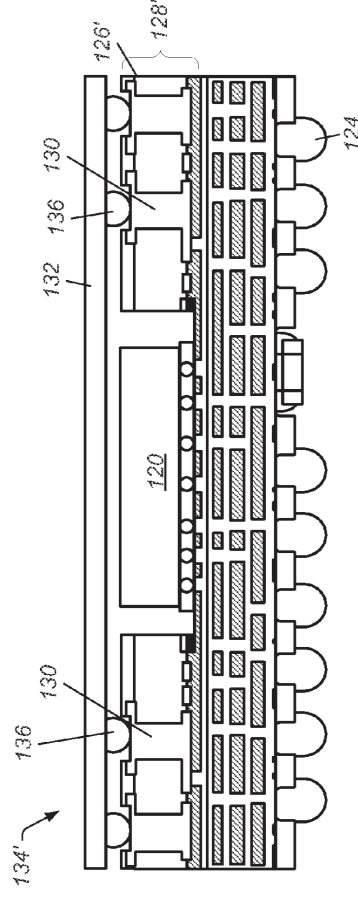
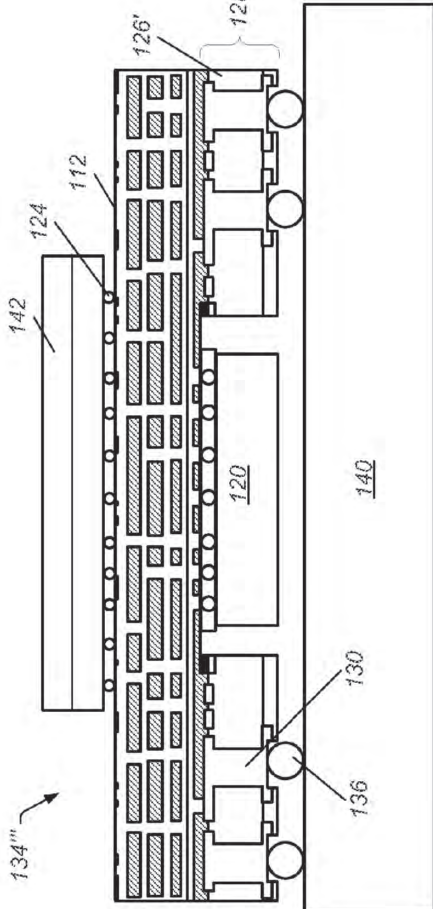


FIG. 5

Hsu '142, FIG. 5

“In some embodiments, a bottom package as described herein (e.g., bottom package 126 or bottom package 126') is flipped over and the reinforcement layer is coupled to a printed circuit board (PCB)(e.g., the top package is a PCB but the entire assembly is flipped over so that the PCB is below the bottom package). A memory die may then be coupled to the opposite side of the bottom package from the printed circuit board. FIG. 8 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to printed circuit board (PCB) 140 and memory die 142. FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu '142, [0048].

	 <p><i>FIG. 9</i></p> <p>Hsu '142, FIG. 9</p> <p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Hsu '142 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>

“As shown in FIG. 3, die 120 is located on substrate 112 and substantially surrounded by reinforcement layer 128 and terminals 130 in a fan-out wafer level package (FOWLP) arrangement.” Hsu '142, [0045].

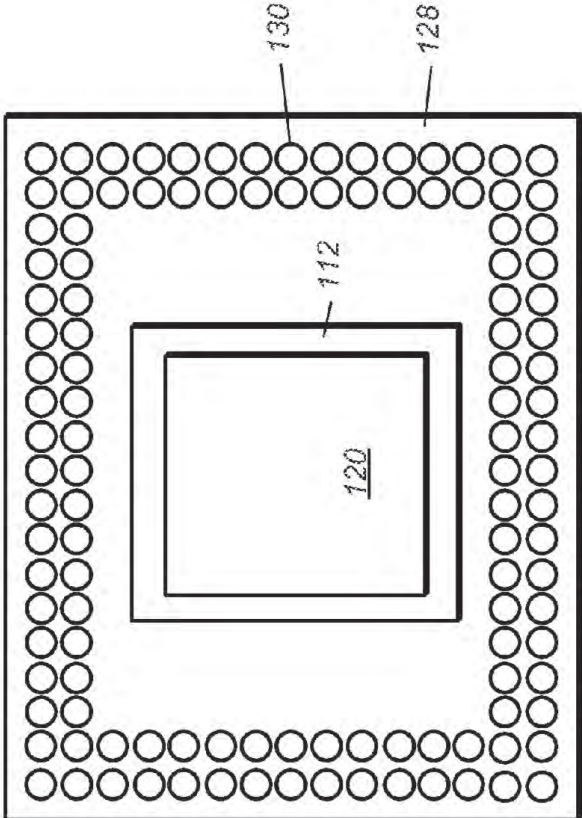
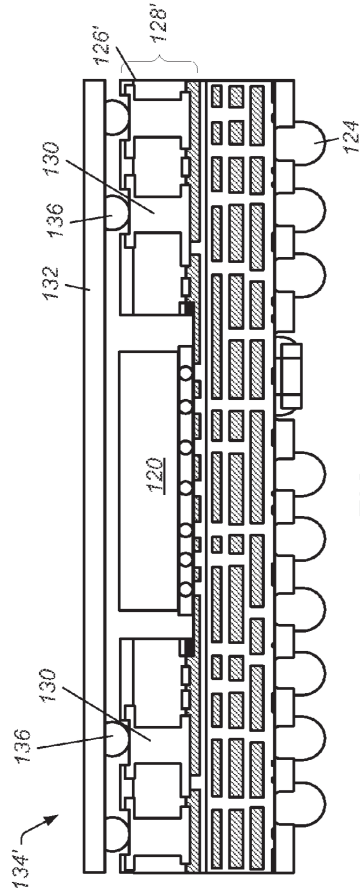


FIG. 3

Hsu '142, FIG. 3

	<p>“FIG. 5 depicts an embodiment of bottom package 126’ (shown in FIG. 2K) coupled to top package 132 to form PoP package 134’. Top package 132 may include, for example, a memory die or a multilayer printed circuit board (MLB). As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128’) in bottom package 126 (or 126’) by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu ’142, [0046].</p>  <p style="text-align: center;">FIG. 5</p> <p>Hsu ’142, FIG. 5</p> <p>“FIG. 9 depicts another embodiment of bottom package 126’ (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126’) by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126’) using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu ’142, [0048].</p>
--	--

	<div></div> <div><p>FIG. 9</p></div> <div><p>Hsu '142, FIG. 9</p></div> <div><p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

Hsu '142 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

See, e.g.:

“In certain embodiments, as shown in FIG. 1K, the top of die 120 is at a substantially similar height or a lower height than the top of laminate layer 104 on top of core material 102.” Hsu ’142, [0035].

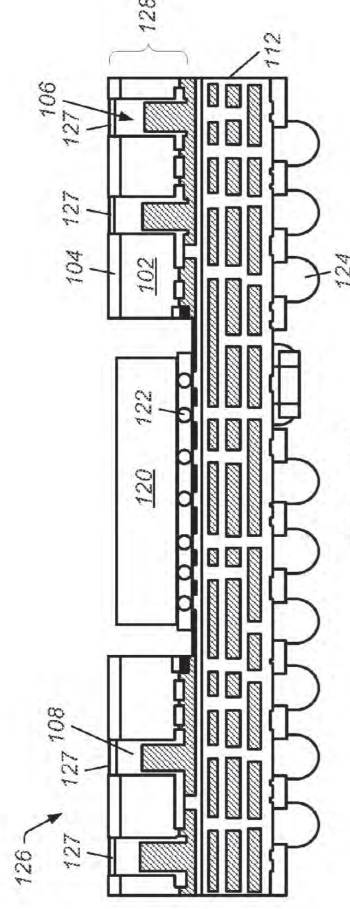
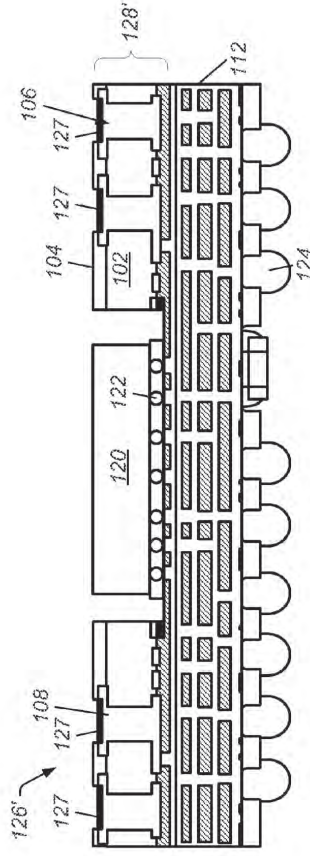


FIG. 1K

Hsu '142, FIG. 1K

	<p>“In addition, the process embodiments depicted in FIGS. 1A-1K and FIGS. 2A-2K process the substrate (substrate 112) before coupling the substrate to a die (die 120).” Hsu '142, [0043].</p> <div><p>FIG. 2K</p></div> <p>Hsu '142, FIG. 2K</p> <p>“As shown in FIG. 3, die 120 is located on substrate 112 and substantially surrounded by reinforcement layer 128 and terminals 130 in a fan-out wafer level package (FOWLP) arrangement. While the FOWLP arrangement is shown, it is to be understood that other wafer package arrangements may also be contemplated using the processes depicted in FIGS. 1A-1K and/or FIGS. 2A-2K. Terminals 130 may correspond to locations of metal layer 108 filled vias 106 (shown in FIGS. 1K and 2K).” Hsu '142, [0045].</p>
--	---

“FIG. 9 depicts another embodiment of bottom package 126’ (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126’) by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 124. Memory die 142 (now top) of bottom package 126 (or 126’) using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu ’142, [0048].

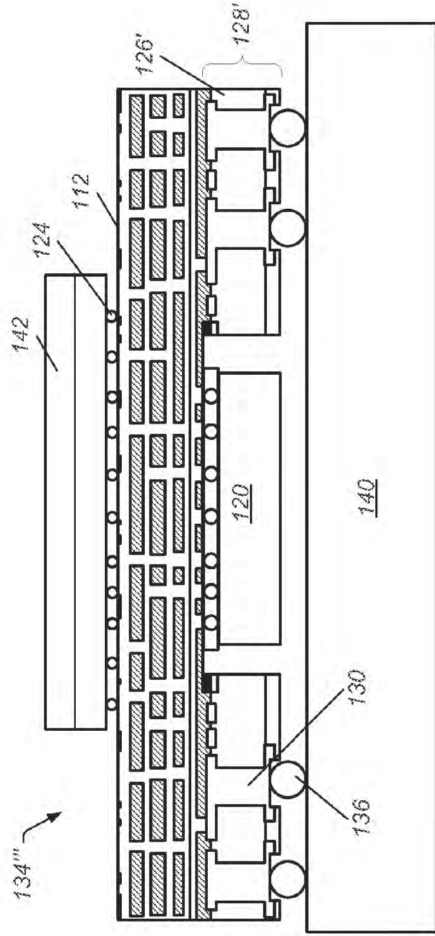


FIG. 9

Hsu '142, FIG. 9

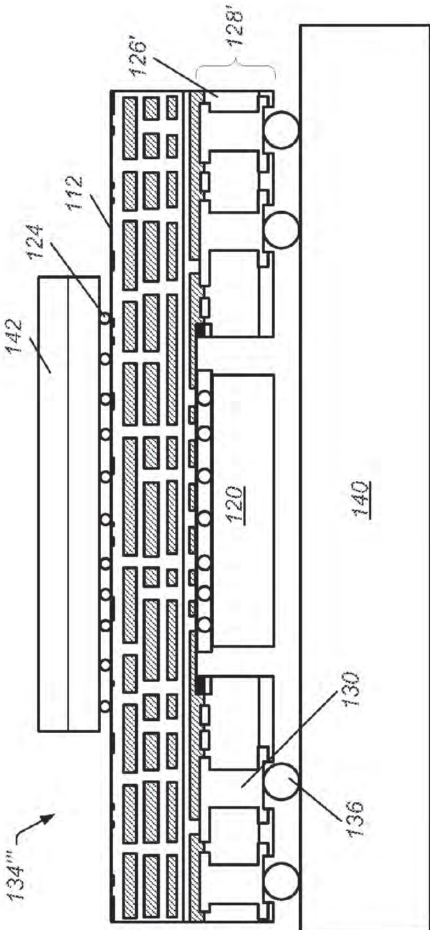
To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	<p>Hsu '142 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 4 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to top package 132 to form PoP package 134. FIG. 5 depicts an embodiment of bottom package 126' (shown in FIG. 2K) coupled to top package 132 to form PoP package 134'. Top package 132 may include, for example, a memory die or a multilayer printed circuit board (MLB). As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128') in bottom package 126 (or 126') by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].</p> <p>“FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain</p>

	<p>embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu ’142, [0048].</p>  <p style="text-align: center;"><i>FIG. 9</i></p> <p>Hsu ’142, FIG. 9</p> <p>“FIG. 8 depicts an embodiment of bottom package 126 (shown in FIG. 1K) coupled to printed circuit board (PCB) 140 and memory die 142.” Hsu ’142, [0048].</p> <p>To the extent Plaintiff contends that Hsu ’142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.	<p>Hsu '142 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“After core material 102 and carrier 100 are coupled using laminate layer 104, bottom package substrate 112 may be formed on core material 102, as shown in FIG. 2D. Core material 102, laminate layer 104, and metal layer 108 form reinforcement layer 128'. Reinforcement layer 128', shown in FIG. 2D, is substantially similar to reinforcement layer 128, shown in FIG. 1D, with a difference being the substantially complete filling of vias 106 in core material 102 with metal layer 108 (e.g., the metal layer substantially fills the vias in the core material due to the paste hole filling of the vias). Subsequent processing of carrier 100, core material 102, laminate layer 104, barrier layer 110, and substrate 112 in FIGS. 2E-2K is also substantially similar to the processing described in FIGS. 1E-1K. Thus, package 126' with reinforcement layer 128', shown in FIG. 2K, has a substantially similar structure to package 126 with reinforcement layer 128, shown in FIG. 1K.” Hsu '142, [0040].</p>

	<p>“In the process embodiments depicted in FIGS. 1A-1K and FIGS. 2A-2K, it should be understood that core material 102 may, in some embodiments, be coupled to both sides of carrier 100 (e.g., the core material is coupled to both the top and bottom of the carrier) and subsequent processing may form identical bottom packages (126 or 126') using core material on both the top and bottom of the carrier. For example, core material 102 on either side of carrier 100 may be detached from the carrier and subsequently processed individually. In addition, more than one bottom package may be formed on either side of carrier 100 from a single layer of core material 102 (e.g., core material 102 may be used as a base layer for multiple packages on either side of the carrier).” Hsu '142, [0044].</p> <p>“FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu '142, [0048].</p>
--	---

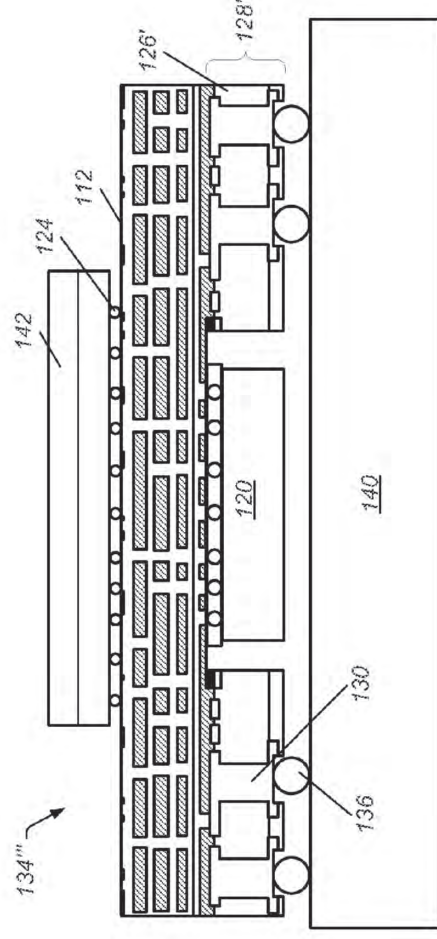


FIG. 9

Hsu '142, FIG. 9

3. The fine pitch may be possible because of the use of metal layer 108 in vias 106 to define terminals 130 on bottom package 126 or 126'. Using metal layer 108 in vias 106 to define terminals 130 provides the terminals as post-like structures that can have small spacing between the terminals. Thus, terminals 136 on top package 132, shown in FIGS. 4 and 5, may be relatively small solder balls to avoid bridging between adjacent solder balls when the top package is coupled to bottom package 126 or 126'." Hsu '142, [0049].

To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Hsu '142 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“After core material 102 and carrier 100 are coupled using laminate layer 104, bottom package substrate 112 may be formed on core material 102, as shown in FIG. 2D. Core material 102, laminate layer 104, and metal layer 108 form reinforcement layer 128'. Reinforcement layer 128', shown in FIG. 2D, is substantially similar to reinforcement layer 128, shown in FIG. 1D, with a difference being the substantially complete filling of vias 106 in core material 102 with metal layer 108 (e.g., the metal layer substantially fills the vias in the core material due to the paste hole filling of the vias). Subsequent processing of carrier 100, core material 102, laminate layer 104, barrier layer 110, and substrate 112 in FIGS. 2E-2K is also substantially similar to the processing described in FIGS. 1E-1K. Thus, package</p>

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	<p>126' with reinforcement layer 128', shown in FIG. 2K, has a substantially similar structure to package 126 with reinforcement layer 128, shown in FIG. 1K." Hsu '142, [0040].</p> <p>"In the process embodiments depicted in FIGS. 1A-1K and FIGS. 2A-2K, it should be understood that core material 102 may, in some embodiments, be coupled to both sides of carrier 100 (e.g., the core material is coupled to both the top and bottom of the carrier) and subsequent processing may form identical bottom packages (126 or 126') using core material on both the top and bottom of the carrier. For example, core material 102 on either side of carrier 100 may be detached from the carrier and subsequently processed individually. In addition, more than one bottom package may be formed on either side of carrier 100 from a single layer of core material 102 (e.g., core material 102 may be used as a base layer for multiple packages on either side of the carrier)." Hsu '142, [0044].</p> <p>"FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack." Hsu '142, [0048].</p>
--	--

	<div></div> <div><p>FIG. 9</p></div> <div><p>Hsu '142, FIG. 9</p></div> <div><p>“In certain embodiments, the pitch between terminals 130 is relatively fine, as shown in FIG. 3. The fine pitch may be possible because of the use of metal layer 108 in vias 106 to define terminals 130 on bottom package 126 or 126'. Using metal layer 108 in vias 106 to define terminals 130 provides the terminals as post-like structures that can have small spacing between the terminals. Thus, terminals 136 on top package 132, shown in FIGS. 4 and 5, may be relatively small solder balls to avoid bridging between adjacent solder balls when the top package is coupled to bottom package 126 or 126'.” Hsu '142, [0049].</p></div> <div><p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p></div>
--	---

Appendix A-10 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '142 - U.S. Patent Publication No. 20150061142

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Hsu '142 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Barrier layer 110 may be formed over core material 102 in an area (defined by the dotted lines in FIG. 1C) that is later used as a terminal (bump) pad area for a die coupled to the package. After core material 102 is patterned and vias 106 are filled with metal layer 108, bottom package substrate 112 may be formed on core material 102, as shown in FIG. 1D.” Hsu '142, [0027-0028].</p> <p>“Die 120 may be coupled to substrate terminal pad 118 using one or more terminals 122. For example, terminals 122 may be solder balls coupled to solder pads on terminal pad 118.” Hsu '142, [0035].</p>

	<p>“In certain embodiments, terminals 127 are formed on or from exposed surfaces of metal layer 108 on top of bottom package 126. Terminals 127 may be used to couple bottom package 126 to a top package in a PoP package.” Hsu '142, [0037].</p> <p>“After core material 102 is patterned and metal layer 108 is formed, core material 102 may be coupled to carrier 100 (shown in FIG. 2B). FIG. 2C depicts core material 102 and carrier 100 coupled using laminate layer 104.” Hsu '142, [0039].</p> <p>“After core material 102 and carrier 100 are coupled using laminate layer 104, bottom package substrate 112 may be formed on core material 102, as shown in FIG. 2D. Core material 102, laminate layer 104, and metal layer 108 form reinforcement layer 128'. Reinforcement layer 128', shown in FIG. 2D, is substantially similar to reinforcement layer 128, shown in FIG. 1D, with a difference being the substantially complete filling of vias 106 in core material 102 with metal layer 108 (e.g., the metal layer substantially fills the vias in the core material due to the paste hole filling of the vias). Subsequent processing of carrier 100, core material 102, laminate layer 104, barrier layer 110, and substrate 112 in FIGS. 2E-2K is also substantially similar to the processing described in FIGS. 1E-1K. Thus, package 126' with reinforcement layer 128', shown in FIG. 2K, has a substantially similar structure to package 126 with reinforcement layer 128, shown in FIG. 1K.” Hsu '142, [0040].</p> <p>“In the process embodiments depicted in FIGS. 1A-1K and FIGS. 2A-2K, it should be understood that core material 102 may, in some embodiments, be coupled to both sides of carrier 100 (e.g., the core material is coupled to both the top and bottom of the carrier) and subsequent processing may form identical bottom packages (126 or 126') using core material on both the top and bottom of the carrier. For example, core material 102 on either side of carrier 100 may be detached from the carrier and subsequently processed individually. In</p>
--	--

addition, more than one bottom package may be formed on either side of carrier 100 from a single layer of core material 102 (e.g., core material 102 may be used as a base layer for multiple packages on either side of the carrier).” Hsu ’142, [0044].

“As shown in FIGS. 4 and 5, top package 132 may be coupled to reinforcement layer 128 (or 128 ') in bottom package 126 (or 126 ') by coupling terminals 136 on the top package to terminals 130 on the bottom package. Terminals 136 may be, for example, solder balls.” Hsu '142, [0046].

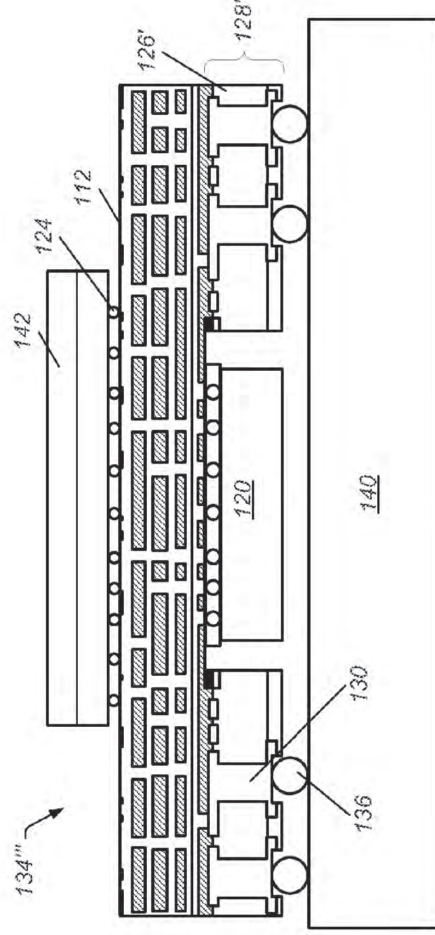


FIG. 9

Hsu '142, FIG. 9

	<p>“PCB 140 may be coupled to bottom package 126 (or 126 ') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126 ') using terminals 124.” Hsu '142, [0048].</p> <p>“FIG. 9 depicts another embodiment of bottom package 126' (shown in FIG. 2K) coupled to PCB 140 and memory die 142. PCB 140 may be coupled to bottom package 126 (or 126') by coupling terminals 136 on the PCB to terminals 130 on the bottom package. In certain embodiments, memory die 142 is coupled to substrate 112 on the non-PCB side (now top) of bottom package 126 (or 126') using terminals 124. Memory die 142 may be, for example, a memory die stack with two memory die stacked on top of each other. In some embodiments, memory die 142 is a fan-out memory die stack.” Hsu '142, [0048].</p> <p>“In certain embodiments, the pitch between terminals 130 is relatively fine, as shown in FIG. 3. The fine pitch may be possible because of the use of metal layer 108 in vias 106 to define terminals 130 on bottom package 126 or 126'. Using metal layer 108 in vias 106 to define terminals 130 provides the terminals as post-like structures that can have small spacing between the terminals. Thus, terminals 136 on top package 132, shown in FIGS. 4 and 5, may be relatively small solder balls to avoid bridging between adjacent solder balls when the top package is coupled to bottom package 126 or 126'.” Hsu '142, [0049].</p> <p>To the extent Plaintiff contends that Hsu '142 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

U.S. Patent No. 8981559 (“Hsu ’559”) is titled Package on Package Devices and Methods of Packaging Semiconductor Dies and lists Chun-Lei Hsu, Chung-Shi Liu, De-Yuan Lu, Ming-Che Ho, and Yu-Feng Chen as inventors. Hsu ’559 is assigned to Taiwan Semiconductor Manufacturing Company, Ltd. Hsu ’559 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Hsu ’559 is a U.S. patent that was filed June 25, 2012 and published December 26, 2013. Hsu ’559 is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Hsu ’559, or otherwise rendered obvious by disclosures and teachings of Hsu ’559, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Hsu ’559 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Hsu ’559 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Hsu ’559, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Hsu '559 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

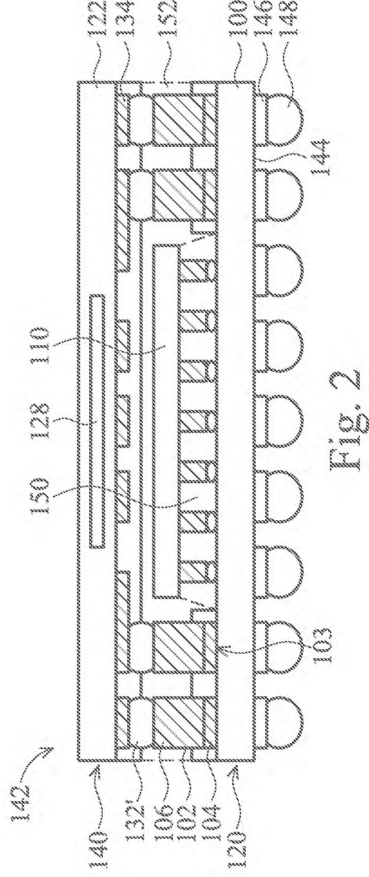
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Hsu '559 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Hsu '559 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Hsu '559 discloses, either expressly or inherently, a structure.</p> <p>See, e.g.:</p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second</p>

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu ’559, [2:50-2:63].</p> <p>“FIG. 2. The molding compound 152 may be formed after the first packaged die and the second packaged die 140 are attached. Alternatively, the molding compound 152 may be applied at least between the metal pillars 102 before the first packaged die 120 and the second packaged die 140 are attached, to be described herein with reference to FIGS. 8, 18, and 19. The molding compound 152 may comprise similar materials described for the underfill material 150, for example. Alternatively, the molding material 152 may comprise other materials. The underfill material 150 may comprise a first molding compound that is formed over sidewalls of the first die 110, and the molding compound 152 may comprise a second molding compound that is formed over the first molding compound 150 and the first die 110, in some embodiments, for example. A plurality of solder balls 148 may optionally be formed on the bottom surface of the first substrate 100, as shown in FIG. 2. The solder balls 148 are attached to the bond pads 146 on the bottom of the first substrate 100, before or after singulating the individual packaged dies 120, for example.” Hsu ’559, [6:6-6:25].</p>
--	--



Hsu '559, Fig. 2.

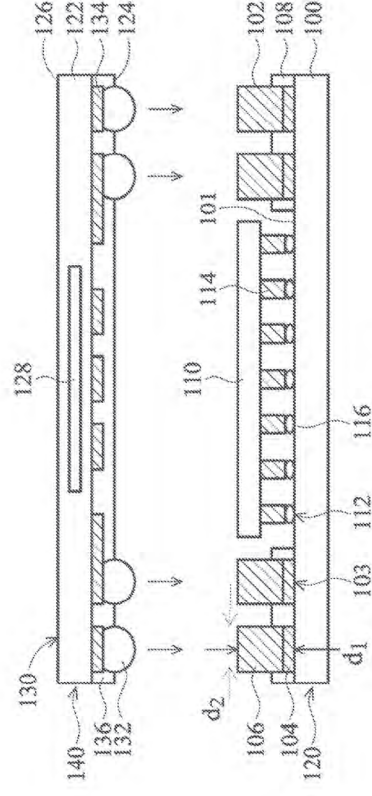
“FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3 ; see solder ball 132 in FIG. 1 and solder joint 132 ' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132 ' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu '559, [6:35-6:46].

“FIG. 4 is a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment, wherein metal pillars 102 a and 102 b are disposed on both the first and second packaged dies 120 and 140, respectively. Metal pillars 102 a are also referred to herein as

	<p>first metal pillars 102 a, and metal pillars 102 b are also referred to herein as second metal pillars 102 b. A solder ball 132 (not shown in FIG. 4; see solder ball 132 in FIG. 1 and solder joint 132 " in FIG. 4 after a reflow process of a solder ball 132) is formed on each of the plurality of first metal pillars 102 a or on each of the plurality of second metal pillars 102 b. A solder ball 132 may alternatively be formed on each of the plurality of first metal pillars 102 a and on each of the plurality of second metal pillars 102 b, for example. Each of the plurality of first metal pillars 102 a is coupled to one of the plurality of second metal pillars 102 b using a solder ball 132 formed on one of the plurality of first metal pillars 102 a and/or a solder ball 132 formed on one of the plurality of second metal pillars 102 b, and a solder reflow process is performed, forming the solder joints 132 " shown in FIG. 4." Hsu '559, [6:48-6:67].</p> <p>"FIG. 5 illustrates a cross-sectional view of a PoP device 142 packaged in accordance with an embodiment wherein the metal pillars 102 comprise a cone or ladder shape. The metal pillars 102 are wider at the bottom than at the top. The sidewalls of the metal pillars 102 may be substantially straight, forming a cone shape, as shown in FIG. 5. Alternatively, the sidewalls of the metal pillars 102 may be stair-stepped and have a ladder shape, as shown in FIG. 6, which is a more detailed view of a metal pillar 102 shown in FIG. 5." Hsu '559, [7:8-7:17].</p> <p>"FIG. 8 is a cross-sectional view of a PoP device packaged in accordance with yet another embodiment, wherein the metal pillars 102 comprise the shape of the letter "I". The I shape of the metal pillars 102 also has a second portion 106 with a narrower top region that facilitates adhering with a solder ball 132. Portions of the solder joint 132 ' form around edges of the narrower top region of the second portion 106 of the metal pillars 102. The solder ball 132 can be printed from a solder film or may comprise a smaller-sized ball than in other embodiments described herein, as examples. If the metal pillar 102 critical dimension (CD)</p>
--	--

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>is substantially the same as the solder ball 132 diameter or solder film width, the metal pillars can form an “I” shape, for example. FIG. 8 also illustrates an optional protective material 154 (see also FIGS. 16 through 18, to be described further herein) that may be formed over top surfaces and sidewalls of the metal pillars 102 before coupling together the first and second packages dies 120 and 140.” Hsu ’559, [7:26-7:43].</p>
[1.A] a bottom package substrate;	<p>Hsu ’559 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1. Referring to FIG. 1, to package the first die 110, the first die 110 is attached to a substrate 100. First, a first substrate 100 is provided. Only one first substrate 100 is shown in the drawings; however, several first substrates 100 are processed on a workpiece comprising a plurality of first substrates 100, and the workpiece is later singulated, after packaging first dies 110 on the first substrates 100. The first substrate 100 comprises an interposer comprised of an insulating material or glass in some embodiments. In other embodiments, the first substrate 100 comprises a semiconductive material such as a semiconductor wafer.” Hsu ’559, [2:50-3:6].</p>



Fi. 50

Hsu '559, Fig. 1.

“The first substrate 100 is then singulated from other first substrates 100 on the workpiece, forming a first packaged die 120. The first packaged die 120 is also referred to herein in some embodiments as a bottom packaged die, for example. In some embodiments, the bottom packaged die 120 includes a plurality of solder balls 148 formed on bond pads 146 on the bottom surface 144 thereof, as shown in FIG. 2. Each of the plurality of metal pillars 102 is bonded to a bond pad and/or trace 103 on the top surface 101 of the bottom packaged die 120.” Hsu ’559, [5:3-5:12].

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

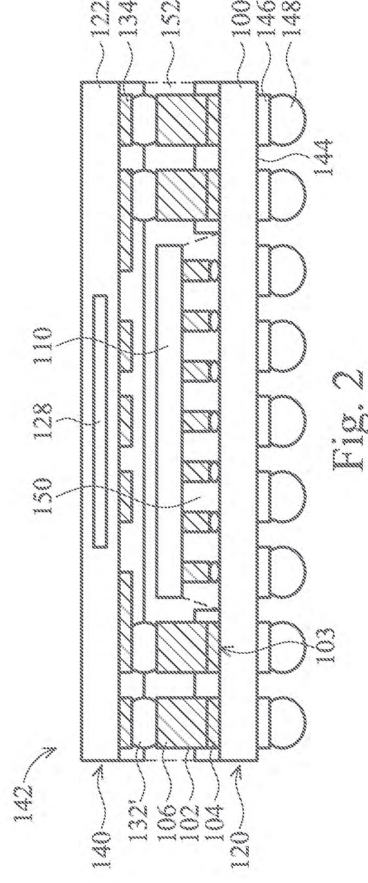
	<p>“Each of the plurality of metal pillars 102 on the top surface 101 of the first substrate 100 (e.g., comprising a bottom substrate) is coupled to a solder ball 132 on the bottom surface 124 of the second substrate 122 (e.g., comprising a top substrate).” Hsu '559, [5:38-5:42].</p> <p>“The solder balls 148 are attached to the bond pads 146 on the bottom of the first substrate 100, before or after singulating the individual packaged dies 120, for example.” Hsu '559, [6:23-6:25].</p> <p>“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die.” Hsu '559, [6:29-6:32].</p> <p>“Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3 ; see solder ball 132 in FIG. 1 and solder joint 132 ' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die.” Hsu '559, [6:33-6:40].</p> <p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Hsu '559 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p>

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>“FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1. Referring to FIG. 1, to package the first die 110, the first die 110 is attached to a substrate 100. First, a first substrate 100 is provided.” Hsu ’559, [2:61-2:66].</p> <p>“The second packaged die 140 is lowered until the solder balls 132 are coupled to the metal pillars 102. Each of the plurality of metal pillars 102 on the top surface 101 of the first substrate 100 (e.g., comprising a bottom substrate) is coupled to a solder ball 132 on the bottom surface 124 of the second substrate 122 (e.g., comprising a top substrate).” Hsu ’559, [5:37-5:42].</p> <p>“The plurality of metal pillars 102 is disposed between the first packaged die 120 and the second packaged die 140, as shown. The solder joints 132 ’ electrically couple together the bond pads and/or traces 103 of the first packaged die 120 and the contacts 134 of the second packaged die 120, and also mechanically couple together the first and second packaged dies 120 and 140.” Hsu ’559, [5:54-5:60].</p> <p>“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die.” Hsu ’559, [6:29-6:32].</p> <p>“FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3 ; see solder ball 132 in FIG. 1 and solder joint 132 ’ in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate)</p>
--	---

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate).” Hsu ’559, [6:35-6:44].</p> <p>To the extent Plaintiff contends that Hsu ’559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hsu ’559 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu ’559, [2:50-2:63].</p>

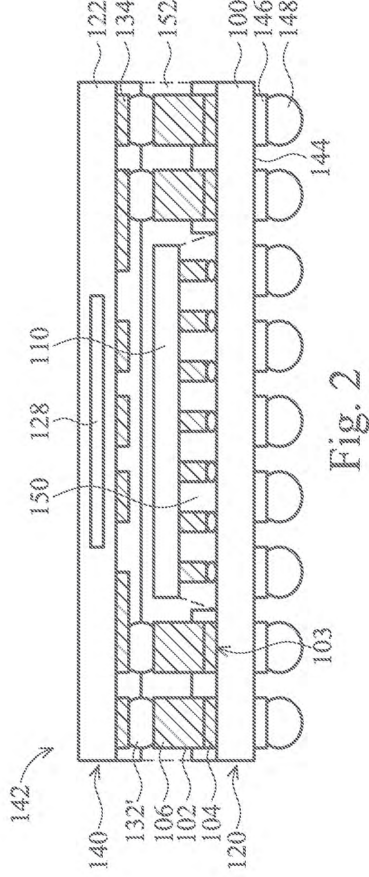


Hsu '559, Fig. 2.

“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu '559, [6:29-6:46].

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Hsu '559 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu '559, [2:50-2:63].</p>



Hsu '559, Fig. 2.

“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu '559, [6:29-6:46].

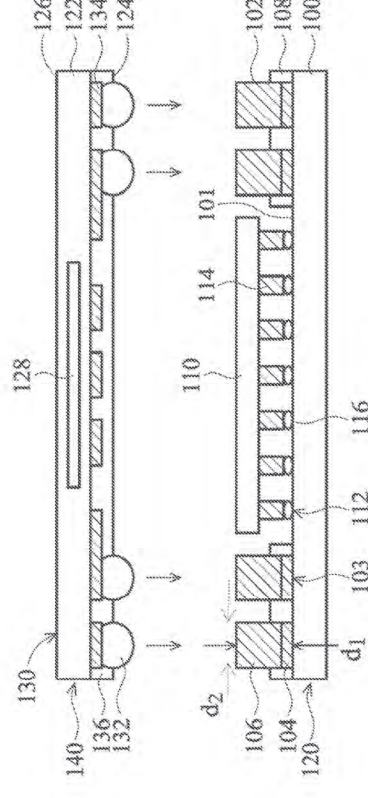
Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>“A molding compound 152 may also optionally be formed between the first packaged die 120 and the second packaged die 140, also shown in phantom in FIG. 2. The molding compound 152 may be formed after the first packaged die and the second packaged die 140 are attached. Alternatively, the molding compound 152 may be applied at least between the metal pillars 102 before the first packaged die 120 and the second packaged die 140 are attached, to be described herein with reference to FIGS. 8, 18, and 19. The molding compound 152 may comprise similar materials described for the underfill material 150, for example. Alternatively, the molding material 152 may comprise other materials. The underfill material 150 may comprise a first molding compound that is formed over sidewalls of the first die 110, and the molding compound 152 may comprise a second molding compound that is formed over the first molding compound 150 and the first die 110, in some embodiments, for example.” Hsu '559, [6:4-6:20].</p> <p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Hsu '559 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is</p>

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu ’559, [2:50-2:63].</p> <p>“The first substrate 100 includes wiring 156 (see FIG. 9) formed within one or more insulating material layers. The wiring 156 provides horizontal electrical connections (e.g., x-axis connections in the view shown in FIG. 1) in some embodiments, for example. The wiring 156 may include fan-out regions that include traces of conductive material for expanding the footprint of the first die 110 to a footprint of the bottom side 144 of the first substrate 100, e.g., of the bond pads 146. The wiring 156 of the first substrate 100 may include one or more redistribution layers (RDLs). The RDLs may comprise one or more insulating layers and wiring layers. The RDLs may include inter-level dielectrics (ILDs) with wiring in metallization layers disposed or formed therein. The wiring 156 may comprise one or more vias and/or conductive lines, for example. The wiring 156 and the TSVs may be formed in the first substrate 100 using one or more subtractive etch processes, single damascene techniques, and/or dual damascene techniques, as examples.” Hsu ’559, [3:40-3:57].</p> <p>“Referring again to FIG. 1, in accordance with embodiments of the present disclosure, a plurality of metal pillars 102 is attached to the bond pads and/or traces 103 on the top surface of the first substrate 100. The plurality of metal pillars 102 is formed using a two-step plating process, to be described further herein. The metal pillars 102 include a first portion 104 and a second portion 106 coupled to the first portion 104. The height of the first portion 104 in a vertical direction is thinner than the height of the second portion 106. The first portion 104</p>
--	---

is disposed directly over the bond pads and/or traces 103. The second portion 106 is coupled to and disposed directly over the first portion 104 of each metal pillar 102.” Hsu ’559, [3:65-4:10].



Fi

Hsu '559, Fig. 1.

“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu ’559, [6:29-6:46].</p> <p>“A plurality of first portions 104 of the plurality of metal pillars 102 is formed in the plurality of first patterns 106 a in the first layer of photoresist 158 using a first plating process 163, as shown in FIG. 10. A plurality of contacts 155 is also optionally simultaneously formed in the plurality of second patterns 106 b in the first layer of photoresist 158 in the first plating process 163, also shown in FIG. 10.” Hsu ’559, [8:55-8:61].</p> <p>“A plurality of second portions 106 of the plurality of metal pillars 102 is formed in the plurality of second patterns 164 in the second layer of photoresist 162 using a second plating process 165, also shown in FIG. 12. The second plating process 165 may comprise an electroplating process or an electro-less plating process. The second plating process 165 may comprise the same type or a different type of plating process than the first plating process 163, for example. The second portions 106 may partially fill the second patterns 164 in the second layer of photoresist 162, or the second portions 106 may substantially completely fill the second patterns 164 in the second layer of photoresist 162, as shown in phantom.” Hsu ’559, [9:7-9:18].</p> <p>“The second substrate 122 may include TSVs 178 and wiring 180 similar to the TSVs and wiring 156 described for the first substrate 100.” Hsu ’559, [13:2-13:4].</p>
--	--

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Hsu '559 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu '559, [2:50-2:63].</p> <p>“Bond pads and/or traces 103 comprising openings in wiring of the first substrate 110 are formed on the top surface of the first substrate 100 in a peripheral region of the first substrate 100 in a top view. Bond pads and/or traces 112 comprising openings in wiring are formed on the top surface of the first substrate 100 in a central region of the first substrate 100 in a top view. Bond pads and/or traces 103 and are shown in a more detailed view in FIG. 9. Bond pads 146 (not shown in FIG. 1 ; see FIG. 2) are formed on the bottom surface 144 of the first substrate 100. The bond pads 146 may be arranged in an array or in rows or columns on the</p>

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>bottom surface 144 of the first substrate 100, not shown. The bond pads 146 may fully populate the bottom surface 144 or may be arranged in various patterns, such as patterns used in ball grid array (BGA) or land grid array (LGA) package devices, as examples. The bond pads and/or traces 103 and 112 and bond pads 146 comprise a conductive material such as Al, Cu, Au, alloys thereof, other materials, or combinations and/or multiple layers thereof, as examples.” Hsu ’559, [3:11-3:29].</p> <p>“Referring again to FIG. 1, in accordance with embodiments of the present disclosure, a plurality of metal pillars 102 is attached to the bond pads and/or traces 103 on the top surface of the first substrate 100. The plurality of metal pillars 102 is formed using a two-step plating process, to be described further herein. The metal pillars 102 include a first portion 104 and a second portion 106 coupled to the first portion 104. The height of the first portion 104 in a vertical direction is thinner than the height of the second portion 106. The first portion 104 is disposed directly over the bond pads and/or traces 103. The second portion 106 is coupled to and disposed directly over the first portion 104 of each metal pillar 102.” Hsu ’559, [3:65-4:10].</p> <p>“The second packaged die 140 includes the second die 128 disposed over the second substrate 122, and a bottom surface 124 including a plurality of bond pads 134 formed thereon. A molding compound 130 may be formed over the second die 128 at a top surface 126 thereof. The bond pads 134 comprise substantially the same footprint or layout as the metal pillars 102 on the first packaged die 120. A plurality of solder balls 132 is formed on the bond pads 134 in the embodiment shown in FIGS. 1 and 2.” Hsu ’559, [5:18-5:26].</p> <p>“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may</p>
--	---

be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together." Hsu '559, [6:29-6:46].

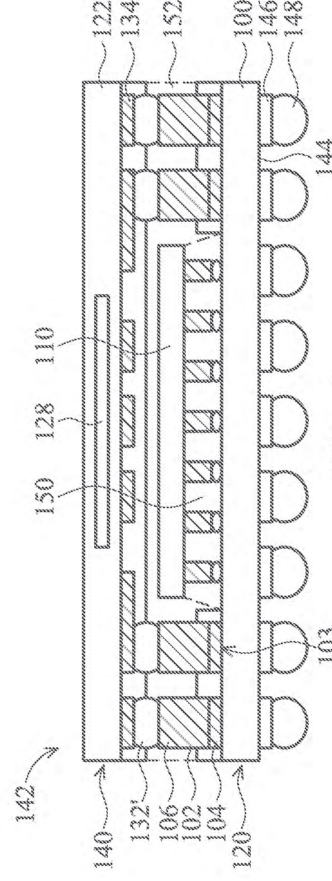


Fig. 2

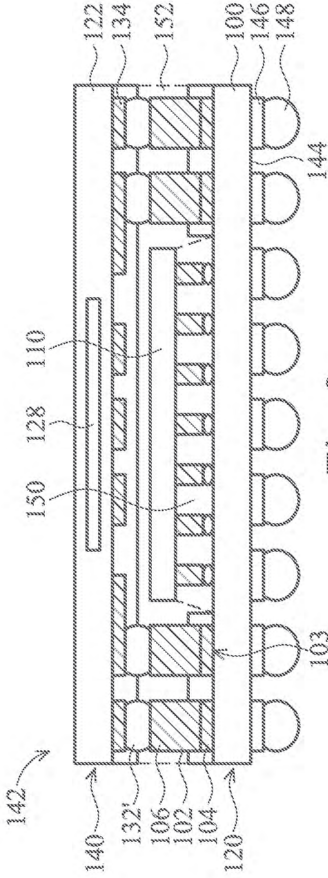
Hsu '559, Fig. 2.

“The optional protection layer 154 comprises a material such as Sn, Au, CuGe, Cu, Ni, Pd, an organic solderability preservative (OSP), or combinations thereof, as examples. The

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>protection layer 154 may be formed in some embodiments using an immersion process, such as an immersion tin (Sn) process or an OSP process. The protection layer 154 may also be formed by an electroless process, such as an electroless nickel immersion gold (ENIG) process or an electroless nickel electroless palladium immersion gold (ENEPIG) process. The protection layer 154 may also be formed using a chemical vapor deposition (CVD) process, e.g., to form CuGe. The protection layer 154 may comprise a thickness of about 10 μm or less, and may comprise about 1 to 2 μm in some embodiments, depending on the materials and formation process. Alternatively, the protection layer 154 may comprise other materials, may be formed using other methods, and may comprise other dimensions. The protection layer 154 may optionally be formed over the metal pillars 102 in the perimeter region of the substrate, and the protection layer 154 may also be simultaneously formed over the contacts 155 in the central region of the substrate for the first die 110, as shown in FIG. 16.” Hsu ’559, [10:29-10:50].</p> <p>“The soldering process for the top surface of the metal pillars 102 in a subsequent processing step used to attach the metal pillars 102 to the solder balls 132 on the second packaged die 140 may likewise result in the protection layer 154 being removed from over the top surfaces of the metal pillars 102 or being absorbed into the solder joints 132 ’ or 132 ” formed during the soldering process. Alternatively, the protection layer 154 may remain on the top surface of the metal pillars 102 after the soldering process, as shown in the embodiment illustrated in FIG. 8.” Hsu ’559, [11:4-11:14].</p> <p>To the extent Plaintiff contends that Hsu ’559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Hsu '559 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, e.g.:</p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged with the first packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu '559, [2:50-2:63].</p>  <p style="text-align: center;">Fig. 2</p>
--	---

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

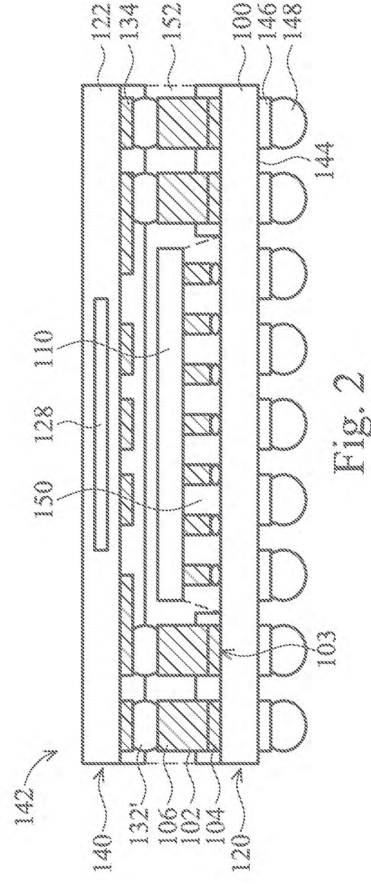
	<p>Hsu '559, Fig. 2.</p> <p>“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu '559, [6:29-6:46].</p> <p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Hsu '559 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

	<p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu '559, [2:50-2:63].</p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu '559, [2:50-2:63].</p> <p>“Referring to FIG. 1, to package the first die 110, the first die 110 is attached to a substrate 100. First, a first substrate 100 is provided. Only one first substrate 100 is shown in the drawings; however, several first substrates 100 are processed on a workpiece comprising a plurality of first substrates 100, and the workpiece is later singulated, after packaging first dies 110 on the first substrates 100. The first substrate 100 comprises an interposer comprised of an insulating material or glass in some embodiments. In other embodiments, the first substrate 100 comprises a semiconductive material such as a semiconductor wafer. The first</p>
--	--

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>substrate 100 may include electronic components and elements formed thereon in some embodiments, or alternatively, the first substrate 100 may be free of electronic components and elements. Bond pads and/or traces 103 comprising openings in wiring of the first substrate 110 are formed on the top surface of the first substrate 100 in a peripheral region of the first substrate 100 in a top view. Bond pads and/or traces 112 comprising openings in wiring are formed on the top surface of the first substrate 100 in a central region of the first substrate 100 in a top view.” Hsu ’559, [2:64-3:17].</p> <p>“A second packaged die 140 is next provided. A cross-sectional view of a second packaged die 140 that includes a second die 128 packaged with a second substrate 122 is shown. Details of the second packaged die 140 are not shown in FIGS. 1 and 2 ; see FIG. 27. The second packaged die 140 includes the second die 128 disposed over the second substrate 122, and a bottom surface 124 including a plurality of bond pads 134 formed thereon. A molding compound 130 may be formed over the second die 128 at a top surface 126 thereof. The bond pads 134 comprise substantially the same footprint or layout as the metal pillars 102 on the first packaged die 120. A plurality of solder balls 132 is formed on the bond pads 134 in the embodiment shown in FIGS. 1 and 2.” Hsu ’559, [5:14-5:26].</p> <p>“The second packaged die 140 is lowered until the solder balls 132 are coupled to the metal pillars 102. Each of the plurality of metal pillars 102 on the top surface 101 of the first substrate 100 (e.g., comprising a bottom substrate) is coupled to a solder ball 132 on the bottom surface 124 of the second substrate 122 (e.g., comprising a top substrate). The solder balls 132 are reflowed, so that a solder joint 132 ’ is formed on each of the metal pillars 102 proximate the second packaged die 140, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with an embodiment.” Hsu ’559, [5:37-5:46].</p>
--	---

“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu '559, [6:29-6:46].



Hsu '559, Fig. 2.

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>“FIG. 5 illustrates a cross-sectional view of a PoP device 142 packaged in accordance with an embodiment wherein the metal pillars 102 comprise a cone or ladder shape. The metal pillars 102 are wider at the bottom than at the top. The sidewalls of the metal pillars 102 may be substantially straight, forming a cone shape, as shown in FIG. 5. Alternatively, the sidewalls of the metal pillars 102 may be stair-stepped and have a ladder shape, as shown in FIG. 6, which is a more detailed view of a metal pillar 102 shown in FIG. 5. FIG. 7 shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment, wherein the metal pillars 102 comprise a socket shape.” Hsu '559, [7:8-7:20].</p> <p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Hsu '559 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second</p>

packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu '559, [2:50-2:63].

“Referring again to FIG. 1, in accordance with embodiments of the present disclosure, a plurality of metal pillars 102 is attached to the bond pads and/or traces 103 on the top surface of the first substrate 100. The plurality of metal pillars 102 is formed using a two-step plating process, to be described further herein. The metal pillars 102 include a first portion 104 and a second portion 106 coupled to the first portion 104. The height of the first portion 104 in a vertical direction is thinner than the height of the second portion 106. The first portion 104 is disposed directly over the bond pads and/or traces 103. The second portion 106 is coupled to and disposed directly over the first portion 104 of each metal pillar 102.” Hsu '559, [3:65-4:9].

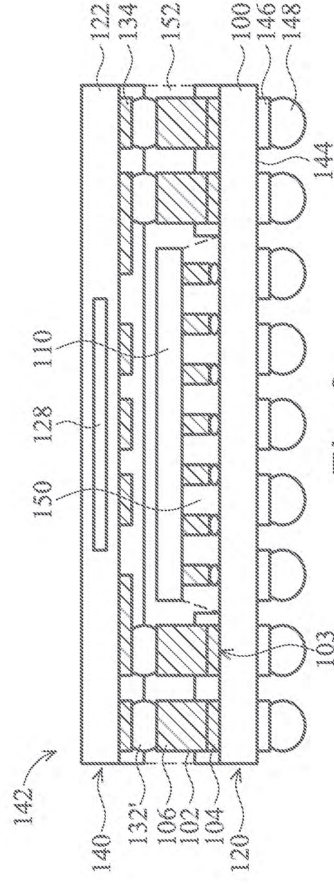


Fig. 2

Hsu '559, Fig. 2.

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

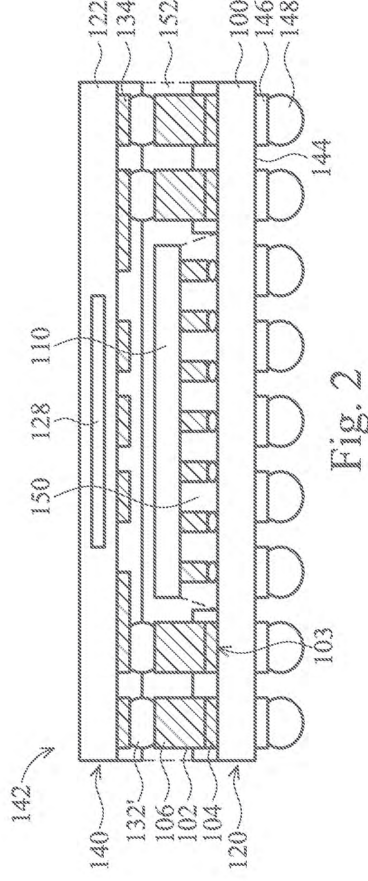
	<p>“The first substrate 100 is then singulated from other first substrates 100 on the workpiece, forming a first packaged die 120. The first packaged die 120 is also referred to herein in some embodiments as a bottom packaged die, for example. In some embodiments, the bottom packaged die 120 includes a plurality of solder balls 148 formed on bond pads 146 on the bottom surface 144 thereof, as shown in FIG. 2. Each of the plurality of metal pillars 102 is bonded to a bond pad and/or trace 103 on the top surface 101 of the bottom packaged die 120.” Hsu ’559, [5:3-5:12].</p> <p>“Each of the plurality of metal pillars 102 on the top surface 101 of the first substrate 100 (e.g., comprising a bottom substrate) is coupled to a solder ball 132 on the bottom surface 124 of the second substrate 122 (e.g., comprising a top substrate).” Hsu ’559, [5:38-5:42].</p> <p>“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132’ in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132’ after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu ’559, [6:29-6:46].</p>
--	---

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>“FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3 ; see solder ball 132 in FIG. 1 and solder joint 132 ' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate).” Hsu '559, [6:35-6:44].</p> <p>“FIG. 4 is a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment, wherein metal pillars 102 a and 102 b are disposed on both the first and second packaged dies 120 and 140, respectively. Metal pillars 102 a are also referred to herein as first metal pillars 102 a, and metal pillars 102 b are also referred to herein as second metal pillars 102 b. A solder ball 132 (not shown in FIG. 4 ; see solder ball 132 in FIG. 1 and solder joint 132 " in FIG. 4 after a reflow process of a solder ball 132) is formed on each of the plurality of first metal pillars 102 a or on each of the plurality of second metal pillars 102 b. A solder ball 132 may alternatively be formed on each of the plurality of first metal pillars 102 a and on each of the plurality of second metal pillars 102 b, for example. Each of the plurality of first metal pillars 102 a is coupled to one of the plurality of second metal pillars 102 b using a solder ball 132 formed on one of the plurality of first metal pillars 102 a and/or a solder ball 132 formed on one of the plurality of second metal pillars 102 b, and a solder reflow process is performed, forming the solder joints 132 " shown in FIG. 4.” Hsu '559, [6:48-6:67].</p> <p>“The molding compound 152 is formed over the first packaged die 120 before coupling together the first and second packages dies 120 and 140. Portions of the molding compound 152 are removed from a top region of the metal pillars 102 (see the embodiment shown in</p>
--	--

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>FIG. 26 and the description thereof) so that electrical and mechanical connections may be made to the solder balls 132 to form the solder joints 132.' Hsu '559, [7:52-7:59].</p> <p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Hsu '559 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1. Referring to FIG. 1, to package the first die 110, the first die 110 is attached to a substrate 100. First, a first substrate 100 is provided.” Hsu '559, [2:50-2:66].</p>



Hsu '559, Fig. 2.

“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu '559, [2:50-2:63].

“The first substrate 100 includes wiring 156 (see FIG. 9) formed within one or more insulating material layers. The wiring 156 provides horizontal electrical connections (e.g., x-axis connections in the view shown in FIG. 1) in some embodiments, for example. The

	<p>wiring 156 may include fan-out regions that include traces of conductive material for expanding the footprint of the first die 110 to a footprint of the bottom side 144 of the first substrate 100, e.g., of the bond pads 146. The wiring 156 of the first substrate 100 may include one or more redistribution layers (RDLs). The RDLs may comprise one or more insulating layers and wiring layers.” Hsu ’559, [3:40-3:50].</p> <p>“Each of the plurality of metal pillars 102 on the top surface 101 of the first substrate 100 (e.g., comprising a bottom substrate) is coupled to a solder ball 132 on the bottom surface 124 of the second substrate 122 (e.g., comprising a top substrate). The solder balls 132 are reflowed, so that a solder joint 132 ’ is formed on each of the metal pillars 102 proximate the second packaged die 140, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with an embodiment.” Hsu ’559, [5:38-5:46].</p> <p>“The solder joints 132 ’ electrically couple together the bond pads and/or traces 103 of the first packaged die 120 and the contacts 134 of the second packaged die 120, and also mechanically couple together the first and second packaged dies 120 and 140.” Hsu ’559, [5:56-5:60].</p> <p>“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132’ in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate)</p>
--	--

	<p>is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu ’559, [6:29-6:46].</p> <p>“In another embodiment, metal pillars may be disposed on both packaged dies 120 and 140. For example, FIG. 4 is a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment, wherein metal pillars 102 a and 102 b are disposed on both the first and second packaged dies 120 and 140, respectively. Metal pillars 102 a are also referred to herein as first metal pillars 102 a, and metal pillars 102 b are also referred to herein as second metal pillars 102 b. A solder ball 132 (not shown in FIG. 4 ; see solder ball 132 in FIG. 1 and solder joint 132 ” in FIG. 4 after a reflow process of a solder ball 132) is formed on each of the plurality of first metal pillars 102 a or on each of the plurality of second metal pillars 102 b. A solder ball 132 may alternatively be formed on each of the plurality of first metal pillars 102 a and on each of the plurality of second metal pillars 102 b, for example. Each of the plurality of first metal pillars 102 a is coupled to one of the plurality of second metal pillars 102 b using a solder ball 132 formed on one of the plurality of first metal pillars 102 a and/or a solder ball 132 formed on one of the plurality of second metal pillars 102 b, and a solder reflow process is performed, forming the solder joints 132 ” shown in FIG. 4.” Hsu ’559, [6:47-6:67].</p> <p>“To package a single second die 18 a or two or more second dies 128 a and 128 b, a second substrate 122 is provided, which may comprise a substrate similar to the first substrate 100 described herein and which may comprise similar materials and components as the first substrate 100. The second substrate 122 may comprise a plurality of second substrates 122 formed on a strip or workpiece (not shown). The second substrate 122 may include TSVs 178 and wiring 180 similar to the TSVs and wiring 156 described for the first substrate 100.</p>
--	---

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>The second substrate 122 includes contact pads 176 on the top surface in a perimeter region and contacts 134 on the bottom surface.” Hsu ’559, [12:62-13:6].</p> <p>To the extent Plaintiff contends that Hsu ’559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hsu ’559 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu ’559, [2:50-2:63].</p>

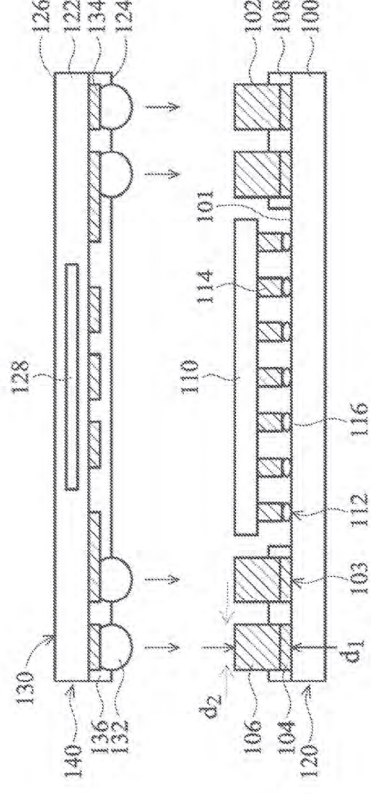


Fig. 1

Hsu '559, Fig. 1.

“Referring to FIG. 1, to package the first die 110, the first die 110 is attached to a substrate 100. First, a first substrate 100 is provided. Only one first substrate 100 is shown in the drawings; however, several first substrates 100 are processed on a workpiece comprising a plurality of first substrates 100, and the workpiece is later singulated, after packaging first dies 110 on the first substrates 100.” Hsu '559, [2:64-3:3].

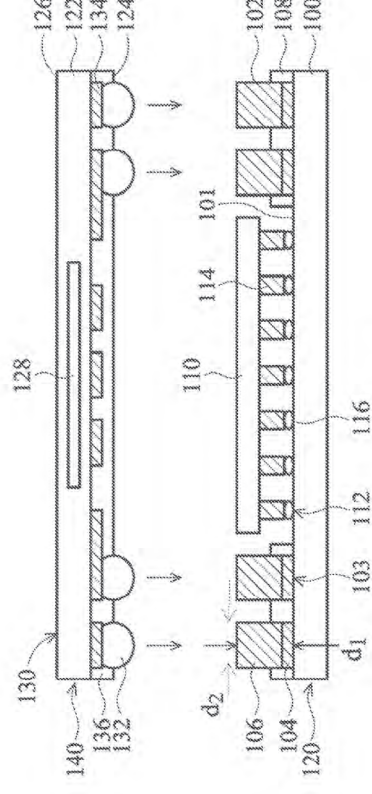
“Referring again to FIG. 1, the first die 110 is attached to the first substrate 100. The first die 110 comprises an integrated circuit or chip that will be packaged with a second die 128 a and optionally also a third die 128 b (not shown in FIG. 1 ; see FIG. 27) in a single PoP device 142.” Hsu '559, [4:35-4:39].

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>“The bumps 114 on the first die 110 are then attached to the bond pads and/or traces 112 on the top surface of the first substrate 100, as shown in FIG. 1. A solder reflow process is used to reflow the solder caps 116 on the solder bumps 114 and attach the first die 110 to the first substrate 100, electrically and mechanically attaching the bumps 114 to the bond pads and/or traces 112 of the first substrate 100, for example.” Hsu '559, [4:56-4:63].</p> <p>“The plurality of metal pillars 102 is disposed between the first packaged die 120 and the second packaged die 140, as shown.” Hsu '559, [5:54-5:56].</p> <p>“A molding compound 152 may also optionally be formed between the first packaged die 120 and the second packaged die 140, also shown in phantom in FIG. 2.” Hsu '559, [6:4-6:6].</p> <p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Hsu '559 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring again to FIG. 1, the first die 110 is attached to the first substrate 100. The first die 110 comprises an integrated circuit or chip that will be packaged with a second die 128 a and optionally also a third die 128 b (not shown in FIG. 1 ; see FIG. 27) in a single PoP device 142. The first die 110 may include a workpiece that includes a semiconductor substrate</p>

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>comprising silicon or other semiconductor materials and may be covered by an insulating layer, for example. The first die 110 may include one or more components and/or circuits formed in and/or over the workpiece, not shown. The first die 110 may include conductive layers and/or semiconductor elements, e.g., transistors, diodes, capacitors, etc., also not shown. The first die 110 may comprise logic circuitry, memory devices, or other types of circuits, as examples. The first die 110 may include a plurality of contacts (not shown) formed on a bottom surface thereof. A plurality of bumps 114 may be formed on the bottom surface of the first die 110, e.g., on the plurality of contacts on the bottom surface of the first die 110. The bumps 114 may comprise microbumps and the bumps 114 may each include a solder cap 116 formed thereon, as examples. The bumps 114 are also referred to herein as conductive bumps. The bumps 114 on the first die 110 are then attached to the bond pads and/or traces 112 on the top surface of the first substrate 100, as shown in FIG. 1.” Hsu ’559, [4:34-4:58].</p>
--	---



150

Hsu '559, Fig. 1.

“The first die 110 comprises an integrated circuit or chip that will be packaged with a second die 128 a and optionally also a third die 128 b (not shown in FIG. 1 ; see FIG. 27) in a single PoP device 142.” Hsu ’559, [4:36-4:39].

“A solder reflow process is used to reflow the solder caps 116 on the solder bumps 114 and attach the first die 110 to the first substrate 100, electrically and mechanically attaching the bumps 114 to the bond pads and/or traces 112 of the first substrate 100, for example.” Hsu ’559, [4:59-4:63].

“In some embodiments, the first die 110 is attached to the first substrate 100 using a flip-chip bond-on-trace (BOT) attachment technique.” Hsu ’559, [4:65-4:67].

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>“FIG. 8 further illustrates a plurality of contacts 155 formed on the first substrate 100 that are formed in a central region of the first substrate 100. The contacts 155 may optionally be formed simultaneously with the formation of first portions 104 of the metal pillars 102 in a first plating process accordance with some embodiments (to be described further herein with reference to FIGS. 9 through 13). The solder caps 116 on the first die 110 are coupled to the contacts 155 of the first substrate 100 in these embodiments, as shown. Each of the plurality of conductive bumps 114 is coupled to one of the plurality of contacts 155 in the central region of the substrate 100 by a solder cap 116.” Hsu '559, [7:60-8:4].</p> <p>“In step 191, a first die 110 is coupled to a first substrate 100.” Hsu '559, [14:20-14:21].</p> <p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Hsu '559 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 1, to package the first die 110, the first die 110 is attached to a substrate 100. First, a first substrate 100 is provided. Only one first substrate 100 is shown in the drawings; however, several first substrates 100 are processed on a workpiece comprising a plurality of first substrates 100, and the workpiece is later singulated, after packaging first dies 110 on the first substrates 100. The first substrate 100 comprises an interposer comprised</p>

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>of an insulating material or glass in some embodiments. In other embodiments, the first substrate 100 comprises a semiconductive material such as a semiconductor wafer. The first substrate 100 may include electronic components and elements formed thereon in some embodiments, or alternatively, the first substrate 100 may be free of electronic components and elements.” Hsu ’559, [2:64-3:10].</p> <p>“The first substrate 100 may optionally include a plurality of through-substrate vias (TSVs) (not shown) formed therein in some embodiments. The TSVs comprise a conductive or semiconductive material that extends completely through the first substrate 100 may optionally be lined with an insulating material. The TSVs provide vertical electrical connections (e.g., y-axis connections in the view shown in FIG. 1) from a bottom surface to a top surface of the first substrate 100.” Hsu ’559, [3:32-3:39].</p> <p>“Referring again to FIG. 1, in accordance with embodiments of the present disclosure, a plurality of metal pillars 102 is attached to the bond pads and/or traces 103 on the top surface of the first substrate 100. The plurality of metal pillars 102 is formed using a two-step plating process, to be described further herein. The metal pillars 102 include a first portion 104 and a second portion 106 coupled to the first portion 104. The height of the first portion 104 in a vertical direction is thinner than the height of the second portion 106. The first portion 104 is disposed directly over the bond pads and/or traces 103. The second portion 106 is coupled to and disposed directly over the first portion 104 of each metal pillar 102. The metal pillars 102 comprise a height comprising dimension d1 of about 200 μm or less in some embodiments. In other embodiments, dimension d1 may comprise about 90 to 190 μm, as another example. The metal pillars 102 comprise a width comprising dimension d2 of about 10 to 250 μm in some embodiments. Alternatively, dimensions d1 and d2 may comprise other values.” Hsu ’559, [3:65-4:17].</p>
--	--

“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu '559, [6:29-6:46].

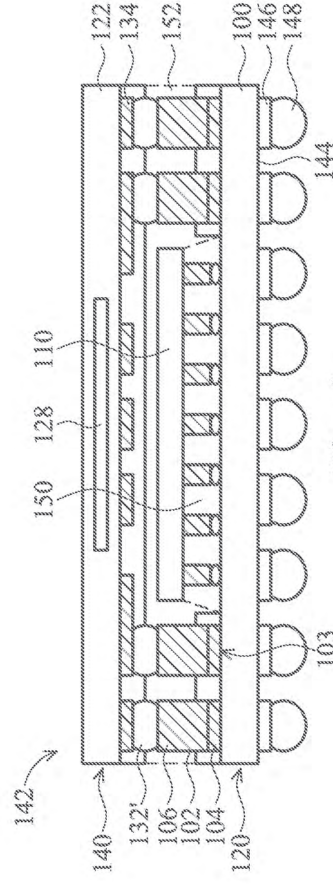


Fig. 2

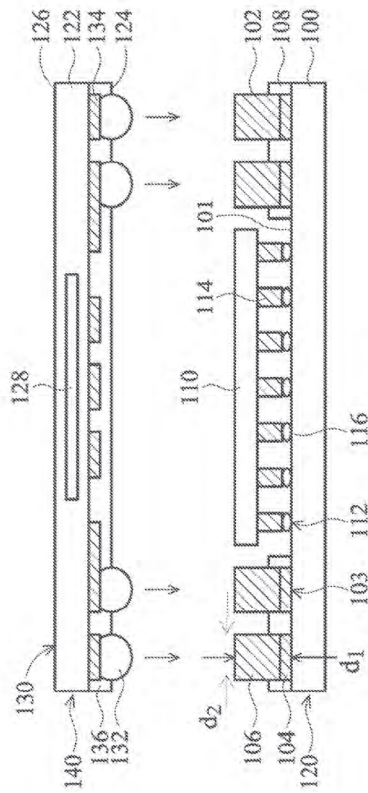
Hsu '559, Fig. 2.

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Hsu '559 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu '559, [2:50-2:63].</p>



Hsu '559, Fig. 1.

“The plurality of metal pillars 102 is disposed between the first packaged die 120 and the second packaged die 140, as shown. The solder joints 132 ' electrically couple together the bond pads and/or traces 103 of the first packaged die 120 and the contacts 134 of the second packaged die 120, and also mechanically couple together the first and second packaged dies 120 and 140.” Hsu '559, [5:54-5:60].

“A molding compound 152 may also optionally be formed between the first packaged die 120 and the second packaged die 140, also shown in phantom in FIG. 2. The molding compound 152 may be formed after the first packaged die and the second packaged die 140 are attached.” Hsu '559, [6:4-6:8].

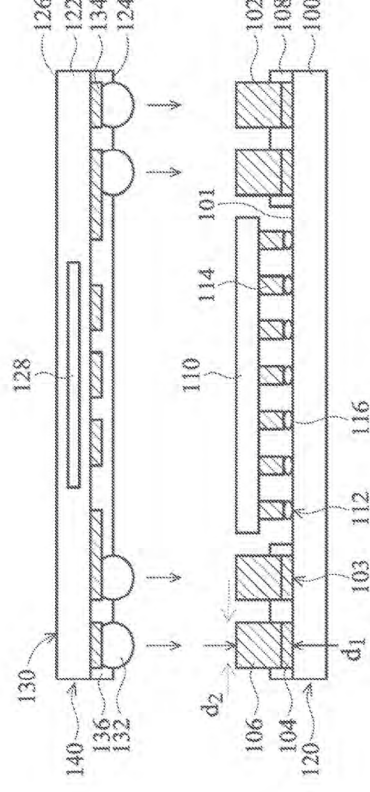
Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>“The CMP process or grinding process can be used to remove a portion of the molding compound 152 and form an air exit space between the first die 110 and the second packaged die 140 in some embodiments, for example.” Hsu ’559, [12:53-12:57].</p> <p>To the extent Plaintiff contends that Hsu ’559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Hsu ’559 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second</p>

packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120, forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1." Hsu '559, [2:50-2:63].



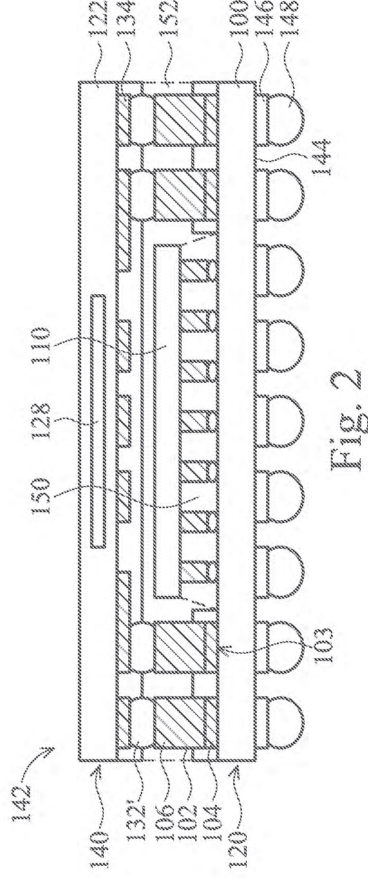
Fi 50

Hsu '559, Fig. 1.

To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p>	<p>Hsu '559 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The first substrate 100 is then singulated from other first substrates 100 on the workpiece, forming a first packaged die 120. The first packaged die 120 is also referred to herein in some embodiments as a bottom packaged die, for example. In some embodiments, the bottom packaged die 120 includes a plurality of solder balls 148 formed on bond pads 146 on the bottom surface 144 thereof, as shown in FIG. 2. Each of the plurality of metal pillars 102 is bonded to a bond pad and/or trace 103 on the top surface 101 of the bottom packaged die 120. Final tests are then performed on the first packaged die 120.” Hsu '559, [5:3-5:13].</p>



Hsu '559, Fig. 2.

“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu '559, [6:29-6:46].

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

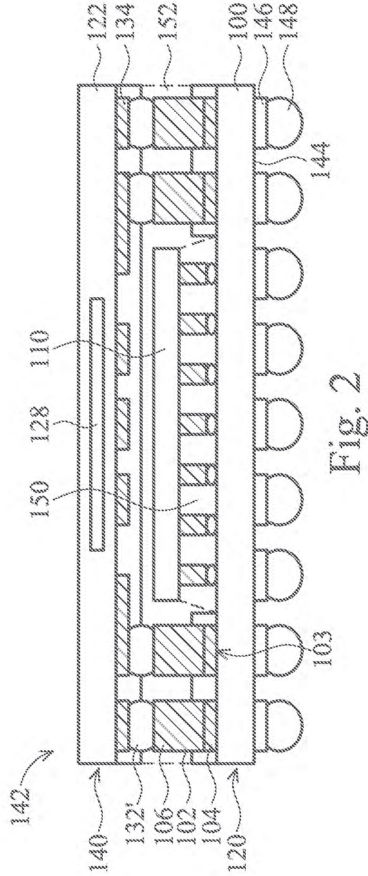
	<p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Hsu '559 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120,</p>

	<p>forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1.” Hsu ’559, [2:50-2:63].</p> <p>“Bond pads and/or traces 103 comprising openings in wiring of the first substrate 110 are formed on the top surface of the first substrate 100 in a peripheral region of the first substrate 100 in a top view. Bond pads and/or traces 112 comprising openings in wiring are formed on the top surface of the first substrate 100 in a central region of the first substrate 100 in a top view. Bond pads and/or traces 103 and are shown in a more detailed view in FIG. 9. Bond pads 146 (not shown in FIG. 1; see FIG. 2) are formed on the bottom surface 144 of the first substrate 100. The bond pads 146 may be arranged in an array or in rows or columns on the bottom surface 144 of the first substrate 100, not shown. The bond pads 146 may fully populate the bottom surface 144 or may be arranged in various patterns, such as patterns used in ball grid array (BGA) or land grid array (LGA) package devices, as examples. The bond pads and/or traces 103 and 112 and bond pads 146 comprise a conductive material such as Al, Cu, Au, alloys thereof, other materials, or combinations and/or multiple layers thereof, as examples. Alternatively, the bond pads and/or traces 103 and 112, and bond pads 146 may comprise other materials.” Hsu ’559, [3:11-3:31].</p> <p>“The first substrate 100 may optionally include a plurality of through-substrate vias (TSVs) (not shown) formed therein in some embodiments. The TSVs comprise a conductive or semiconductive material that extends completely through the first substrate 100 may optionally be lined with an insulating material. The TSVs provide vertical electrical connections (e.g., y-axis connections in the view shown in FIG. 1) from a bottom surface to a top surface of the first substrate 100.” Hsu ’559, [3:32-3:39].</p> <p>“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second</p>
--	--

packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together." Hsu '559, [6:29-6:46].



Hsu '559, Fig. 2.

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom ends of the plurality of metal pillars of the bottom package substrate via the plurality of metal pillars of the bottom package substrate, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Hsu '559 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a cross-sectional view of a method of attaching a second (or top) packaged die 140 to a first (or bottom) packaged die 120 having a plurality of metal pillars 102 disposed thereon in accordance with an embodiment of the present disclosure. A first die 110 is packaged to form the first packaged die 120, and at least one second die 128 is packaged to form a second packaged die 140. The second packaged die 140 is then packaged with the first packaged die 120 by attaching solder balls 132 on the bottom surface 124 of the second packaged die 140 to the metal pillars 102 on the top surface 101 of the first packaged die 120,</p>

	<p>forming a PoP device 142, as shown in FIG. 2, which is a cross-sectional view of a PoP device 142 packaged in accordance with the method shown in FIG. 1. Referring to FIG. 1, to package the first die 110, the first die 110 is attached to a substrate 100. First, a first substrate 100 is provided. Only one first substrate 100 is shown in the drawings; however, several first substrates 100 are processed on a workpiece comprising a plurality of first substrates 100, and the workpiece is later singulated, after packaging first dies 110 on the first substrates 100. The first substrate 100 comprises an interposer comprised of an insulating material or glass in some embodiments. In other embodiments, the first substrate 100 comprises a semiconductive material such as a semiconductor wafer. The first substrate 100 may include electronic components and elements formed thereon in some embodiments, or alternatively, the first substrate 100 may be free of electronic components and elements.” Hsu '559, [2:50-3:10].</p> <p>“Bond pads and/or traces 103 comprising openings in wiring of the first substrate 110 are formed on the top surface of the first substrate 100 in a peripheral region of the first substrate 100 in a top view. Bond pads and/or traces 112 comprising openings in wiring are formed on the top surface of the first substrate 100 in a central region of the first substrate 100 in a top view. Bond pads and/or traces 103 and are shown in a more detailed view in FIG. 9. Bond pads 146 (not shown in FIG. 1; see FIG. 2) are formed on the bottom surface 144 of the first substrate 100. The bond pads 146 may be arranged in an array or in rows or columns on the bottom surface 144 of the first substrate 100, not shown. The bond pads 146 may fully populate the bottom surface 144 or may be arranged in various patterns, such as patterns used in ball grid array (BGA) or land grid array (LGA) package devices, as examples. The bond pads and/or traces 103 and 112 and bond pads 146 comprise a conductive material such as Al, Cu, Au, alloys thereof, other materials, or combinations and/or multiple layers thereof, as examples. Alternatively, the bond pads and/or traces 103 and 112, and bond pads 146 may comprise other materials.” Hsu '559, [3:11-3:31].</p>
--	---

“In the embodiment shown in FIG. 2, the metal pillars 102 are formed on a first packaged die 120 that comprises a bottom packaged die, and solder balls 132 are formed on a second packaged die 140 that comprises a top packaged die. Alternatively, the metal pillars 102 may be formed on a first packaged die 120 that comprises a top packaged die, as shown in FIG. 3, which shows a cross-sectional view of a PoP device 142 packaged in accordance with another embodiment. Solder balls 132 (not shown in FIG. 3; see solder ball 132 in FIG. 1 and solder joint 132' in FIG. 3 after a reflow process of a solder ball 132) are formed on a second packaged die 140 that comprises a bottom packaged die. Each of the plurality of metal pillars 102 on the bottom surface of the first substrate 100 (e.g., comprising a top substrate) is coupled to a solder ball 132 on the top surface of the second substrate 122 (e.g., comprising a bottom substrate). The solder balls 132 become solder joints 132' after a solder reflow process to attach the first and second packaged dies 120 and 140 together.” Hsu '559, [6:29-6:46].

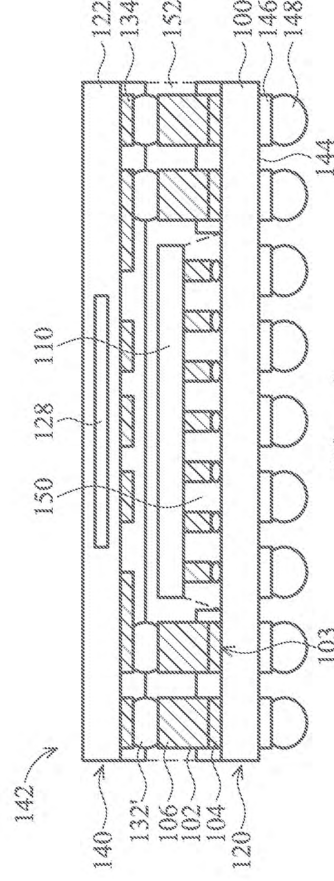


Fig. 2

Appendix A-11 - Invalidity of U.S. Patent No. 9859202 in view of Hsu '559 - U.S. Patent No. 8981559

	<p>Hsu '559, Fig. 2.</p> <p>To the extent Plaintiff contends that Hsu '559 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

U.S. Patent Publication No. 20130175687 (“Hu '687”) is titled Package Stack Device and Fabrication Method Thereof and lists Dyi-Chung Hu as inventor. Hu '687 is assigned to Unimicron Technology Corporation. Hu '687 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the '202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff's apparent infringement theory.² Hu '687 is a U.S. patent publication that was filed June 22, 2012 and published July 11, 2013. Hu '687 claims priority to a TW 101100716 filed on January 6, 2012. Hu '687 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Hu '687, or otherwise rendered obvious by disclosures and teachings of Hu '687, including under TopWire's apparent interpretation of the Asserted Claims as Samsung understands them from TopWire's Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Hu '687 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Hu '687 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung's other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung's Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Hu '687, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire's March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court's order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire's apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung's interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Hu '687 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Hu '687 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Hu '687 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Hu '687 discloses, either expressly or inherently, a structure.</p> <p>See, e.g.:</p> <p>“Accordingly, the present invention provides a package stack device, which comprises: a first package structure, comprising: a first substrate having a first surface with a plurality of first metal posts formed thereon and a second surface opposite to the first surface; and a first electronic element disposed on the first surface of the first substrate and electrically connected to the first substrate; a second package structure, comprising: a second substrate having a third surface and a fourth surface opposite to the third surface, wherein the fourth</p>

surface has a plurality of second metal posts which are connected to the first metal posts, respectively, so as for the second package structure to be stacked on the first package structure, and the height of the second metal posts is greater than, equal to or less than that of the first metal posts; and a second electronic element disposed on the third surface of the second substrate and electrically connected to the second substrate; and an encapsulant formed between the first surface of the first substrate and the fourth surface of the second substrate to encapsulate the first electronic element.” Hu '687, [0012].

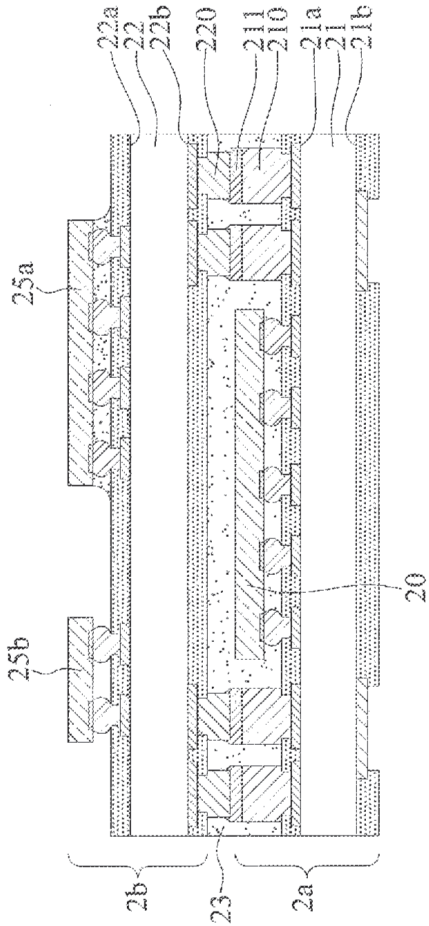


FIG. 2F

Hu '687, FIG. 2F.

“The present invention further provides a fabrication method of a package stack device, which comprises the steps of: providing a first substrate having a first surface with a plurality

	<p>of first metal posts formed thereon and a second surface opposite to the first surface, disposing a first electronic element on the first surface of the first substrate and electrically connecting the first electronic element and the first substrate so as to form a first package structure, providing a second substrate having a third surface and a fourth surface opposite to the third surface, and disposing a second electronic element on the third surface of the second substrate and electrically connecting the second electronic element and the second substrate so as to form a second package structure, wherein the fourth surface of the second substrate has a plurality of second metal posts and the height of the second metal posts is greater than, equal to or less than that of the first metal posts; connecting the second metal posts to the first metal posts, respectively, so as to stack the second package structure on the first package structure; and forming an encapsulant between the first surface of the first substrate and the fourth surface of the second substrate for encapsulating the first electronic element. The present invention further provides a package stack device, which comprises: a first package structure, comprising: a first substrate having a first surface with a plurality of first metal posts formed thereon and a second surface opposite to the first surface; a first electronic element disposed on the first surface of the first substrate and electrically connected to the first substrate in a flip-chip manner; and an underfill formed between the first electronic element and the first surface of the first substrate; a second package structure, comprising: a second substrate having a third surface and a fourth surface opposite to the third surface, wherein the fourth surface has a plurality of second metal posts which are connected to the first metal posts, respectively, so as for the second package structure to be stacked on the first package structure, and the height of the second metal posts is greater than, equal to or less than that of the first metal posts; and a second electronic element disposed on the third surface of the second substrate and electrically connected to the second substrate; and an encapsulant formed between the first surface of the first substrate and the fourth surface of the second substrate to encapsulate the first electronic element and the underfill.” Hu '687, [0013-0014].</p>
--	--

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>“The present invention further provides a package stack device, which has: a first package structure 2 a, a second package structure 2 b stacked on the first package structure 2 a, and an encapsulant 23 disposed between the first and second package structures 2 a, 2 b. The first package structure 2 a has a first substrate 21 having a first surface 21 a and a second surface 21 b opposite to the first surface 21 a, and a first electronic element 20, 20' disposed on the first surface 21 a and electrically connected to the first substrate 21. The first surface 21 a of the first substrate 21 has a plurality of first metal posts 210, 310, 310', 310'', 410, and the second surface 21 b of the first substrate 21 has a plurality of ball pads 212 for mounting solder balls 24.” Hu '687, [0052-0053].</p> <p>“The present invention further provides a package stack device, which has: a first package structure 2 a, a second package structure 2 b stacked on the first package structure 2 a, and an encapsulant 23 disposed between the first and second package structures 2 a, 2 b. The first package structure 2 a has: a first substrate 21 having a first surface 21 a and a second surface 21 b opposite to the first surface 21 a, a first electronic element 20 disposed on the first surface 21 a and electrically connected to the first substrate 21 in a flip-chip manner, and an underfill 550 disposed between the first electronic element 20 and the first surface 21 a of the first substrate 21.” Hu '687, [0063-0064].</p>
[1.A] a bottom package substrate;	<p>Hu '687 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2A, a first substrate 21 having a first surface 21 a and a second surface 21 b opposite to the first surface 21 a is provided. The first surface 21 a of the first substrate 21</p>

has a plurality of bonding pads 211 a and a plurality of contact pads 211 b. The second surface 21 b of the first substrate 21 has a plurality of ball pads 212.” Hu '687, [0031].

“The first package structure 2 a has a first substrate 21 having a first surface 21 a and a second surface 21 b opposite to the first surface 21 a, and a first electronic element 20, 20' disposed on the first surface 21 a and electrically connected to the first substrate 21. The first surface 21 a of the first substrate 21 has a plurality of first metal posts 210, 310, 310', 310'', 410, and the second surface 21 b of the first substrate 21 has a plurality of ball pads 212 for mounting solder balls 24.” Hu '687, [0053].

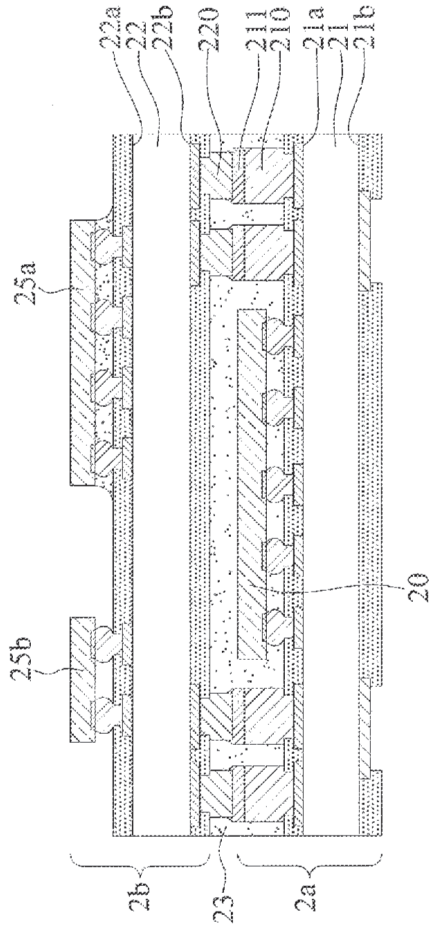


FIG. 2F

Hu '687, FIG. 2F.

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Hu '687 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2A, a first substrate 21 having a first surface 21 a and a second surface 21 b opposite to the first surface 21 a is provided. The first surface 21 a of the first substrate 21 has a plurality of bonding pads 211 a and a plurality of contact pads 211 b. The second surface 21 b of the first substrate 21 has a plurality of ball pads 212.” Hu '687, [0031].</p> <p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu '687, [0038].</p>

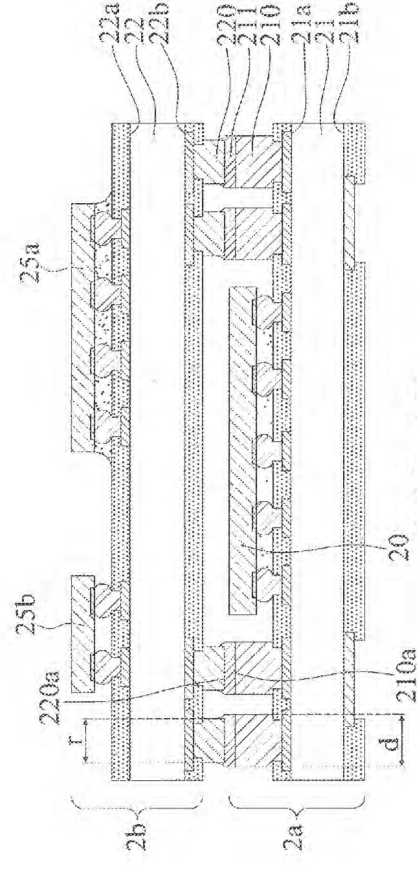


Fig. 2.

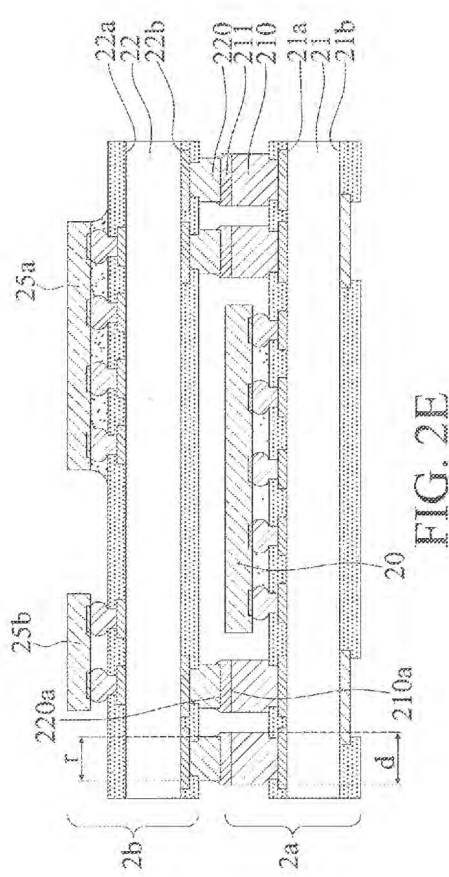
Hu '687, FIG. 2E.

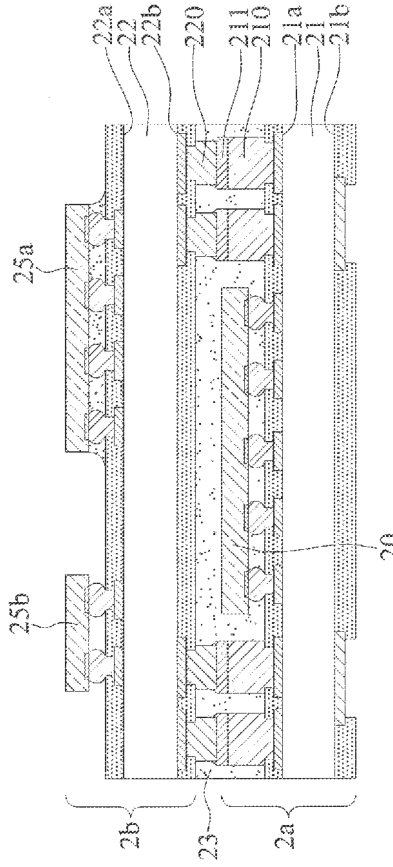
“Referring to FIG. 2F, an encapsulant 23 is formed between the insulating protection layer 213 on the first surface 21 a of the first substrate 21 and the insulating protection layer 223 on the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20.” Hu ’687, [0041].

	<p style="text-align: center;">FIG. 2F</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hu '687, FIG. 2F.</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Hu '687 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p>

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

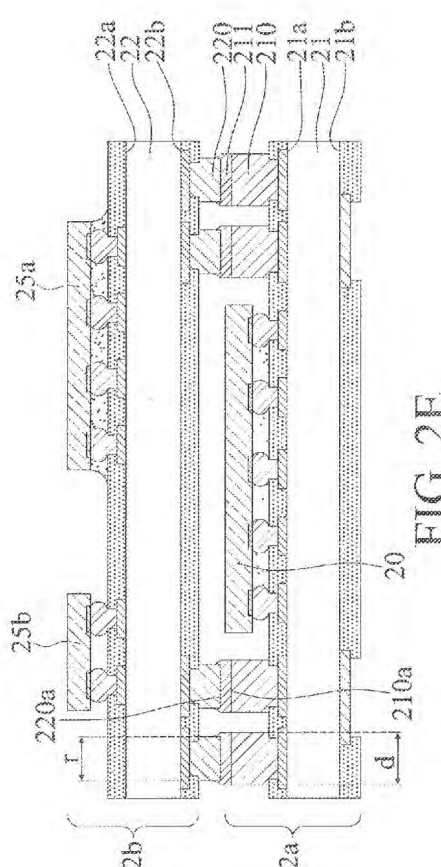
	<p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a. In the present embodiment, the width d (or maximum diameter) of the end surfaces 210 a (surfaces bonding with the second metal posts 220) of the first metal posts 210 is greater than the width r of the end surfaces 220 a of the second metal posts 220. Such a difference in width facilitates alignment of the first and second package structures so as to avoid the risk of joint deviation. Further, increase in the heights of the first and second metal posts 210, 220 will not lead to an increase in the diameters of the first and second metal posts 210, 220. Therefore, a compact-sized and low-profiled device can be achieved. Furthermore, an increased number of the first and second metal posts 210, 220 can be provided in a predetermined region so as to facilitate the alignment of the first and second package structures 2 a, 2 b. Referring to FIG. 2F, an encapsulant 23 is formed between the insulating protection layer 213 on the first surface 21 a of the first substrate 21 and the insulating protection layer 223 on the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20.” Hu '687, [0037-0041].</p>
--	--

	<div><p>FIG. 2E</p></div> <p>Hu '687, FIG. 2E.</p> <p>“Moreover, warpage of the first and second substrates 21, 22 is avoided since the second package structure 2 b is supported on the first package structure 2 a by the first and second metal posts 210, 220 and the gap between the first and second substrates 21, 22 is filled with the encapsulant 23 that is formed by such as molding.” Hu '687, [0051].</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Hu '687 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p>

	<p>See, e.g.:</p> <p>“Referring to FIG. 2F, an encapsulant 23 is formed between the insulating protection layer 213 on the first surface 21 a of the first substrate 21 and the insulating protection layer 223 on the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20.” Hu '687, [0041].</p>  <p>FIG. 2F</p> <p>Hu '687, FIG. 2F.</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Hu '687 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2D, a plurality of second metal posts 220 such as copper posts are formed on the exposed surfaces of the contact pads 221 b of the second substrate 22 by electroplating. The height h of the second metal posts 220 is less than the height t of the first metal posts 210 or less than the sum of the height of the first metal posts 210 and the height of the solder material 211. Further, a plurality of second electronic elements 25 a, 25 b are mounted on the exposed surfaces of the bonding pads 221 a of the second substrate 22 through solder bumps 250 a. As such, a second package structure is obtained. The electrode pads 250 of the second electronic elements 25 a, 25 b are electrically connected to the second substrate 22 in a flip-chip manner.” Hu '687, [0036].</p> <p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu '687, [0038].</p>
--	--

	 <p>FIG. 2E</p> <p>Hu '687, FIG. 2E.</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Hu '687 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p>See, e.g.:</p> <p>“In the present embodiment, the first metal posts 210 are copper posts, and a solder material 211 can be formed on the copper posts for facilitating a subsequent stacking process. The</p>

first electronic element 20 can be an active component such as a chip or a passive component such as a resistor, a capacitor or an inductor. In addition, a plurality of first electronic elements 20 can be provided, which can be active components, passive components or a combination thereof.” Hu '687, [0034].

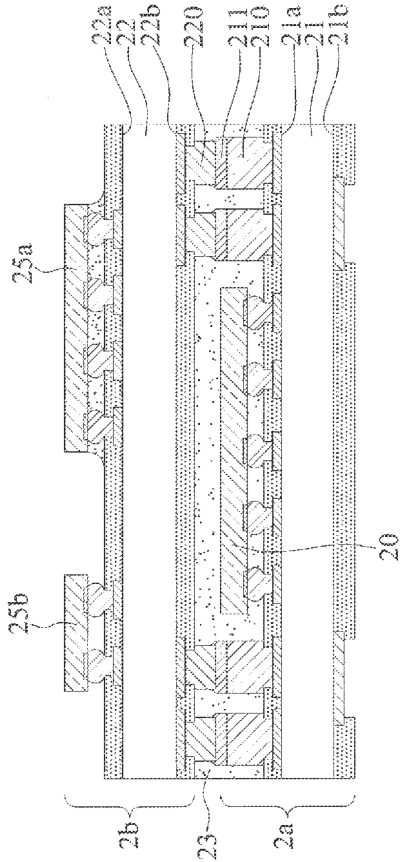


FIG. 2F

Hu '687, FIG. 2F.

“Referring to FIG. 2D, a plurality of second metal posts 220 such as copper posts are formed on the exposed surfaces of the contact pads 221b of the second substrate 22 by electroplating. The height h of the second metal posts 220 is less than the height t of the first metal posts 210 or less than the sum of the height of the first metal posts 210 and the height of the solder material 211. Further, a plurality of second electronic elements 25a, 25b are mounted on the exposed surfaces of the bonding pads 221a of the second substrate 22 through solder bumps 250a. As such, a second package structure is obtained. The electrode pads 250 of the second

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>electronic elements 25 a, 25 b are electrically connected to the second substrate 22 in a flip-chip manner.” Hu ’687, [0036].</p> <p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu ’687, [0038].</p> <p>To the extent Plaintiff contends that Hu ’687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Hu ’687 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the present embodiment, the first metal posts 210 are copper posts, and a solder material 211 can be formed on the copper posts for facilitating a subsequent stacking process. The first electronic element 20 can be an active component such as a chip or a passive component such as a resistor, a capacitor or an inductor. In addition, a plurality of first electronic elements 20 can be provided, which can be active components, passive components or a combination thereof.” Hu ’687, [0034].</p>

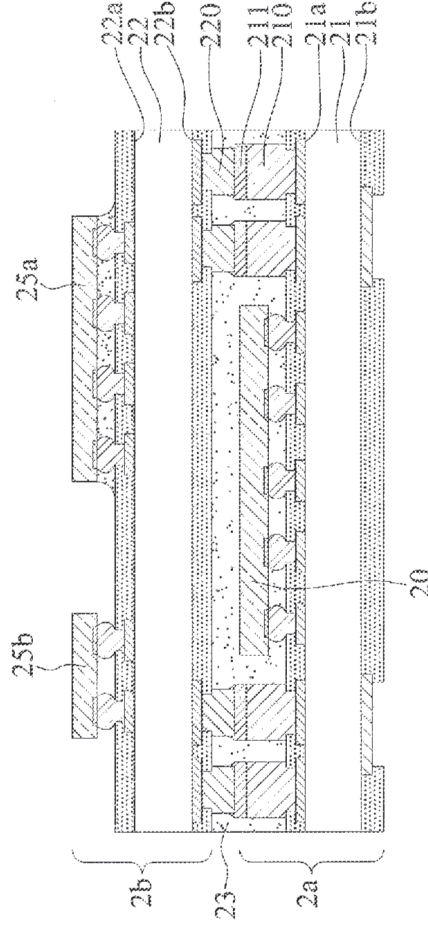


FIG. 2F.

Hu '687, FIG. 2F.

“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu ‘687, [0038].

“Referring to FIG. 2F, an encapsulant 23 is formed between the insulating protection layer 213 on the first surface 21 a of the first substrate 21 and the insulating protection layer 223 on the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20.” Hu ’687, [0041].

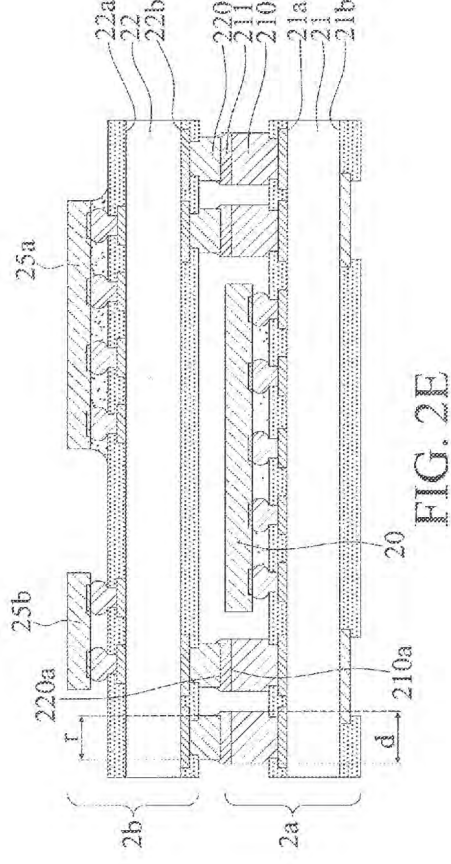
To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Hu '687 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Accordingly, the present invention provides a package stack device, which comprises: a first package structure, comprising: a first substrate having a first surface with a plurality of first metal posts formed thereon and a second surface opposite to the first surface; and a first electronic element disposed on the first surface of the first substrate and electrically connected to the first substrate; a second package structure, comprising: a second substrate having a third surface and a fourth surface opposite to the third surface, wherein the fourth surface has a plurality of second metal posts which are connected to the first metal posts, respectively, so as for the second package structure to be stacked on the first package structure, and the height of the second metal posts is greater than, equal to or less than that of the first metal posts; and a second electronic element disposed on the third surface of the second substrate and electrically connected to the second substrate; and an encapsulant formed between the first surface of the first substrate and the fourth surface of the second substrate to encapsulate the first electronic element.” Hu '687, [0012].</p> <p>“Further, an insulating protection layer 223 such as a solder mask layer is formed on the third and fourth surfaces 22 a, 22 b of the second substrate 22, and a plurality of openings 223 a are formed in the insulating protection layer 223 for exposing the bonding pads 221 a and the contact pads 221 b, respectively. Referring to FIG.” Hu '687, [0035-0036].</p>

“2D, a plurality of second metal posts 220 such as copper posts are formed on the exposed surfaces of the contact pads 221 b of the second substrate 22 by electroplating. The height h of the second metal posts 220 is less than the height t of the first metal posts 210 or less than the sum of the height of the first metal posts 210 and the height of the solder material 211.” Hu '687, [0036].

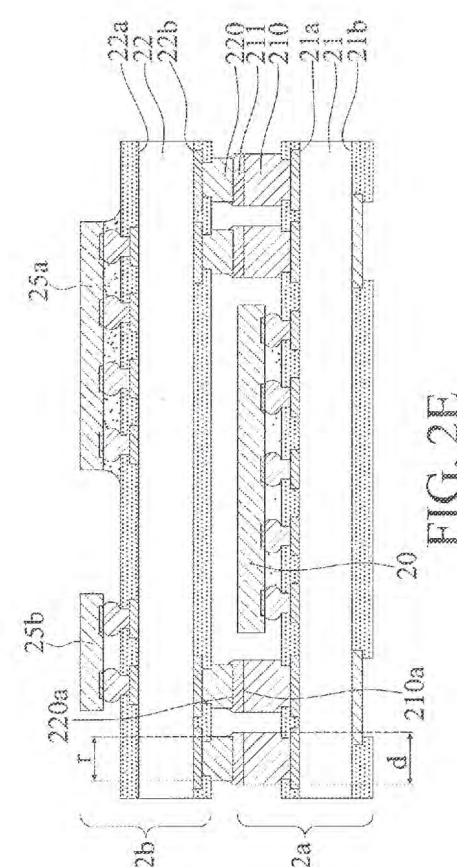
“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu '687, [0038].



Hu '687, FIG. 2E.

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>“Referring to FIG. 2 G', the width d' (such as diameter) of the end surfaces 210 b of the first metal posts 210 ' can be equal to the width r' (such as diameter) of the end surfaces 220 b of the second metal posts 220 '.” Hu '687, [0042-0043].</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Hu '687 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2D, a plurality of second metal posts 220 such as copper posts are formed on the exposed surfaces of the contact pads 221 b of the second substrate 22 by electroplating. The height h of the second metal posts 220 is less than the height t of the first metal posts 210 or less than the sum of the height of the first metal posts 210 and the height of the solder material 211. Further, a plurality of second electronic elements 25 a, 25 b are mounted on the exposed surfaces of the bonding pads 221 a of the second substrate 22 through solder bumps 250 a. As such, a second package structure is obtained. The electrode pads 250 of the second electronic elements 25 a, 25 b are electrically connected to the second substrate 22 in a flip-chip manner.” Hu '687, [0036].</p>

	<p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu ’687, [0038].</p> <div></div> <p>FIG. 2E</p> <p>Hu ’687, FIG. 2E.</p> <p>“Further, increase in the heights of the first and second metal posts 210,220 will not lead to an increase in the diameters of the first and second metal posts 210,220. Therefore, a compact-sized and low-profiled device can be achieved. Furthermore, an increased number of the first and second metal posts 210, 220 can be provided in a predetermined region so as to facilitate the alignment of the first and second package structures 2 a, 2 b.” Hu ’687, [0040].</p>
--	---

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Hu '687 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Accordingly, the present invention provides a package stack device, which comprises: a first package structure, comprising: a first substrate having a first surface with a plurality of first metal posts formed thereon and a second surface opposite to the first surface; and a first electronic element disposed on the first surface of the first substrate and electrically connected to the first substrate; a second package structure, comprising: a second substrate having a third surface and a fourth surface opposite to the third surface, wherein the fourth surface has a plurality of second metal posts which are connected to the first metal posts, respectively, so as for the second package structure to be stacked on the first package structure, and the height of the second metal posts is greater than, equal to or less than that of the first metal posts; and a second electronic element disposed on the third surface of the second substrate and electrically connected to the second substrate; and an encapsulant formed between the first surface of the first substrate and the fourth surface of the second substrate to encapsulate the first electronic element.” Hu '687, [0012].</p>

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>“Referring to FIG. 2B, a plurality of first metal posts 210 are formed on the exposed surfaces of the contact pads 211 b by electroplating, and a first electronic element 20 is mounted on the exposed surfaces of the bonding pads 211 a through a plurality of solder bumps 200 a, i.e., the electrode pads 200 of the first electronic element 20 are electrically connected to the first substrate 21 in a flip-chip manner, thereby forming a first package structure 2 a. In the present embodiment, the first metal posts 210 are copper posts, and a solder material 211 can be formed on the copper posts for facilitating a subsequent stacking process.” Hu '687, [0033-0034].</p> <p>“Referring to FIG. 2D, a plurality of second metal posts 220 such as copper posts are formed on the exposed surfaces of the contact pads 221 b of the second substrate 22 by electroplating.” Hu '687, [0036].</p> <p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu '687, [0038].</p>
--	---

	<div> </div> <div> <p>FIG. 2F</p> </div> <div> <p>Hu '687, FIG. 2F.</p> </div>
--	---

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>320 ', 320 ", 420 which are connected to the first metal posts 210, 310, 310 ', 310 ", 410, respectively, so as for the second package structure 2 b to be stacked on the first package structure 2 a." Hu '687, [0053-0054].</p> <p>"Further, a solder material 211 is disposed between each of the first metal posts 210, 310, 310 ', 310 ", 410 and the corresponding second metal posts 220, 320, 320 ', 320 ", 420." Hu '687, [0057].</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hu '687 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>"Referring to FIG. 2B, a plurality of first metal posts 210 are formed on the exposed surfaces of the contact pads 211 b by electroplating, and a first electronic element 20 is mounted on the exposed surfaces of the bonding pads 211 a through a plurality of solder bumps 200 a, i.e., the electrode pads 200 of the first electronic element 20 are electrically connected to the first substrate 21 in a flip-chip manner, thereby forming a first package structure 2 a." Hu '687, [0033].</p> <p>"In the present embodiment, the first metal posts 210 are copper posts, and a solder material 211 can be formed on the copper posts for facilitating a subsequent stacking process. The</p>

first electronic element 20 can be an active component such as a chip or a passive component such as a resistor, a capacitor or an inductor. In addition, a plurality of first electronic elements 20 can be provided, which can be active components, passive components or a combination thereof." Hu '687, [0034].

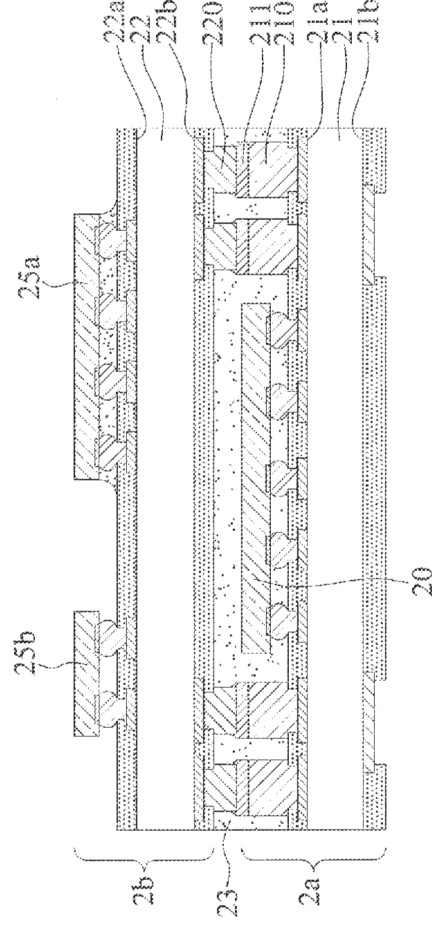
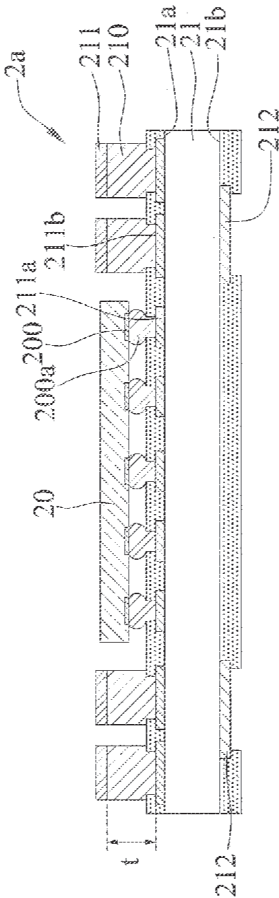


FIG. 2F

Hu '687, FIG. 2F.

“Referring to FIG. 2F, an encapsulant 23 is formed between the insulating protection layer 213 on the first surface 21 a of the first substrate 21 and the insulating protection layer 223 on the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20.” Hu ’687, [0041].

	<p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Hu '687 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2B, a plurality of first metal posts 210 are formed on the exposed surfaces of the contact pads 211 b by electroplating, and a first electronic element 20 is mounted on the exposed surfaces of the bonding pads 211 a through a plurality of solder bumps 200 a, i.e., the electrode pads 200 of the first electronic element 20 are electrically connected to the first substrate 21 in a flip-chip manner, thereby forming a first package structure 2 a.” Hu '687, [0033].</p>  <p>FIG. 2B</p> <p>Hu '687, FIG. 2B.</p>

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>“In the present embodiment, the first metal posts 210 are copper posts, and a solder material 211 can be formed on the copper posts for facilitating a subsequent stacking process. The first electronic element 20 can be an active component such as a chip or a passive component such as a resistor, a capacitor or an inductor. In addition, a plurality of first electronic elements 20 can be provided, which can be active components, passive components or a combination thereof.” Hu '687, [0034].</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Hu '687 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2B, a plurality of first metal posts 210 are formed on the exposed surfaces of the contact pads 211 b by electroplating, and a first electronic element 20 is mounted on the exposed surfaces of the bonding pads 211 a through a plurality of solder bumps 200 a, i.e., the electrode pads 200 of the first electronic element 20 are electrically connected to the first substrate 21 in a flip-chip manner, thereby forming a first package structure 2 a.” Hu '687, [0033].</p>

“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu ‘687, [0038].

“Referring to FIG. 2F, an encapsulant 23 is formed between the insulating protection layer 213 on the first surface 21 a of the first substrate 21 and the insulating protection layer 223 on the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20.” Hu ’687, [0041].

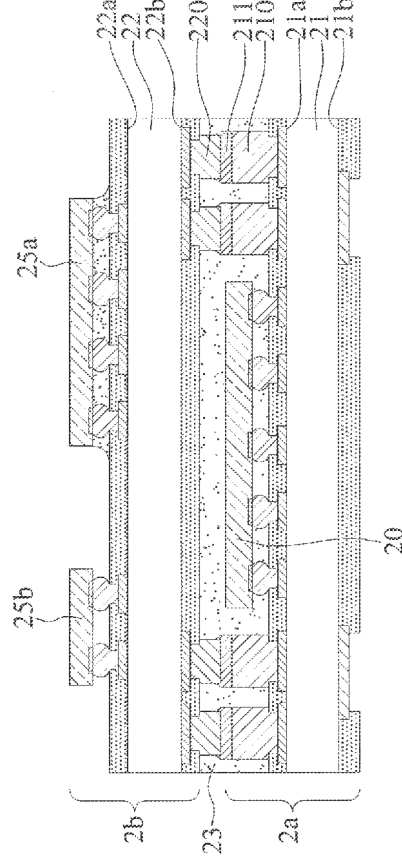


FIG. 2F.

Hu '687, FIG. 2F.

To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Hu '687 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In addition, the present invention avoids warpage of the substrates since the package structures are supported by the metal posts and the gap between the package structures is filled with the encapsulant.” Hu '687, [0024].</p> <p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu '687, [0038].</p> <p>“Referring to FIG. 2F, an encapsulant 23 is formed between the insulating protection layer 213 on the first surface 21 a of the first substrate 21 and the insulating protection layer 223 on the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20.” Hu '687, [0041].</p>

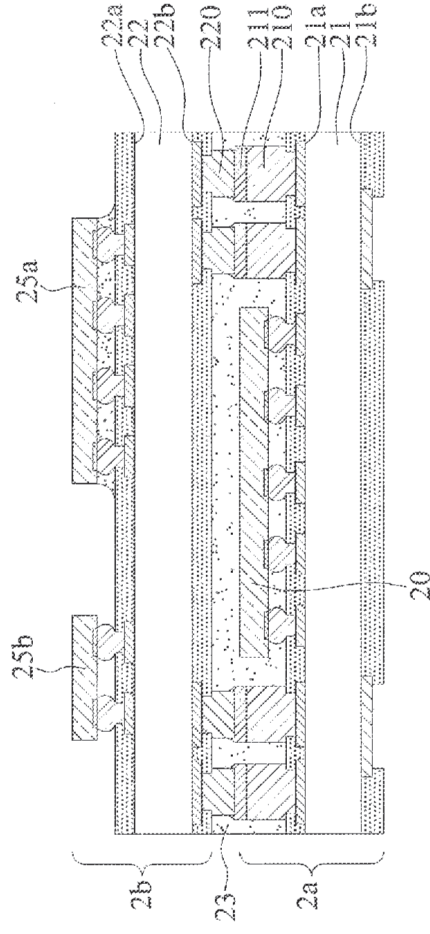


FIG. 2.

Hu '687, FIG. 2F.

“Furthermore, since the first and second metal posts 210, 220 are formed by electroplating, the present invention avoids the risk of bridging when the heights of the first and second metal posts 210, 220 are increased, thereby increasing the product yield.” Hu ’687, [0049-0051].

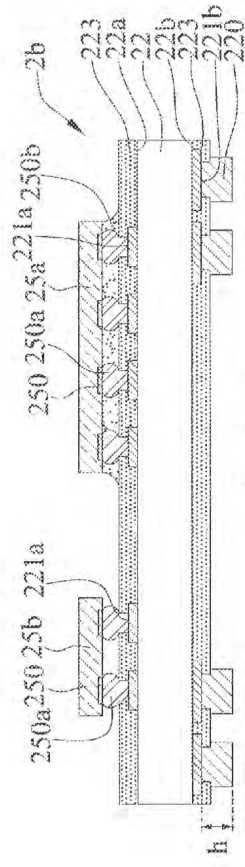
“The encapsulant 23 is disposed between the first surface 21 a of the first substrate 21 and the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20, 20'” Hu '687, [0056].

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>“The encapsulant 23 is disposed between the first surface 21 a of the first substrate 21 and the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20 and the underfill 550.” Hu '687, [0066].</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Hu '687 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2D, a plurality of second metal posts 220 such as copper posts are formed on the exposed surfaces of the contact pads 221 b of the second substrate 22 by electroplating. The height h of the second metal posts 220 is less than the height t of the first metal posts 210 or less than the sum of the height of the first metal posts 210 and the height of the solder material 211. Further, a plurality of second electronic elements 25 a, 25 b are mounted on the exposed surfaces of the bonding pads 221 a of the second substrate 22 through solder bumps</p>

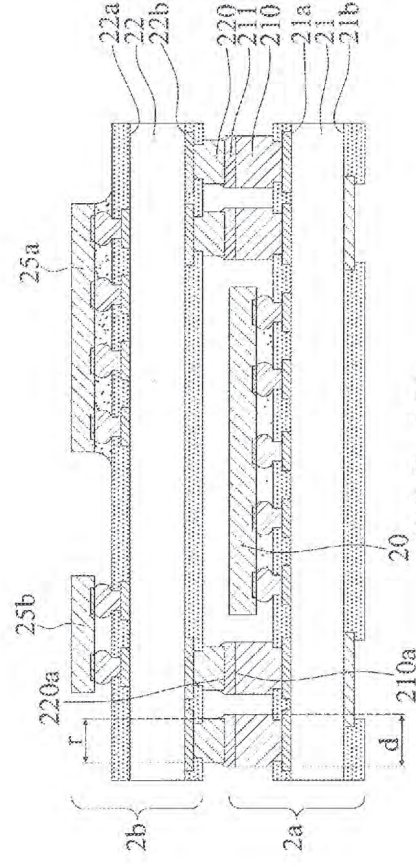
	<p>250 a. As such, a second package structure is obtained. The electrode pads 250 of the second electronic elements 25 a, 25 b are electrically connected to the second substrate 22 in a flip-chip manner.” Hu '687, [0036].</p>  <p style="text-align: center;">FIG. 2D</p> <p>Hu '687, FIG. 2D.</p> <p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a. In the present embodiment, the width d (or maximum diameter) of the end surfaces 210 a (surfaces bonding with the second metal posts 220) of the first metal posts 210 is greater than the width r of the end surfaces 220 a of the second metal posts 220.” Hu '687, [0038-0039].</p> <p>“Referring to FIG. 2F, an encapsulant 23 is formed between the insulating protection layer 213 on the first surface 21 a of the first substrate 21 and the insulating protection layer 223</p>
--	--

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>on the fourth surface 22 b of the second substrate 22 to encapsulate the first electronic element 20.” Hu ’687, [0041].</p> <p>“Referring to FIG. 3, in another embodiment, the height h’ of the second metal posts 320 can be greater than the height t’ of the first metal posts 310, and the width d (such as diameter) of the end surfaces 310 a of the first metal posts 310 can be greater than the width r (such as diameter) of the end surfaces 320 a of the second metal posts 320. In the present embodiment, only one second electronic element 25 a such as an active component is disposed on the second substrate 22.” Hu ’687, [0045].</p> <p>“Referring to FIG. 4, in another embodiment, the height h” of the second metal posts 420 can be equal to the height t” of the first metal posts 410, and the first and second electronic elements 20 ’, 25 a ’ are electrically connected to the first and second substrates 21, 22, respectively, through wire bonding.” Hu ’687, [0047].</p> <p>“The second package structure 2 b has a second substrate 22 having a third surface 22 a and a fourth surface 22 b opposite to the third surface 22 a, and at least a second electronic element 25 a, 25 b, 25 ’ disposed on the third surface 22 a and electrically connected to the second substrate 22. The fourth surface 22 b of the second substrate 22 has a plurality of second metal posts 220, 320, 320 ’, 320 ”, 420 which are connected to the first metal posts 210, 310, 310 ’, 310 ”, 410, respectively, so as for the second package structure 2 b to be stacked on the first package structure 2 a.” Hu ’687, [0054].</p> <p>To the extent Plaintiff contends that Hu ’687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p>	<p>Hu '687 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a. In the present embodiment, the width d (or maximum diameter) of the end surfaces 210 a (surfaces bonding with the second metal posts 220) of the first metal posts 210 is greater than the width r of the end surfaces 220 a of the second metal posts 220. Such a difference in width facilitates alignment of the first and second package structures so as to avoid the risk of joint deviation.” Hu '687, [0038-0039].</p>



25

Hu '687, FIG. 2E.

“Further, increase in the heights of the first and second metal posts 210, 220 will not lead to an increase in the diameters of the first and second metal posts 210, 220.” Hu ’687, [0039-0040].

“Referring to FIG. 2 G', the width d' (such as diameter) of the end surfaces 210 b of the first metal posts 210' can be equal to the width r' (such as diameter) of the end surfaces 220 b of the second metal posts 220'. Although the end surfaces 210 b, 220 b of the metal posts 210', 220' have the same width, since variation in the size of the metal posts are easy to control, the use of the metal posts facilitates vertical stacking of the package structures and helps to reduce the risk of joint deviation as compared with the prior art.” Hu '687, [0042-0043].

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

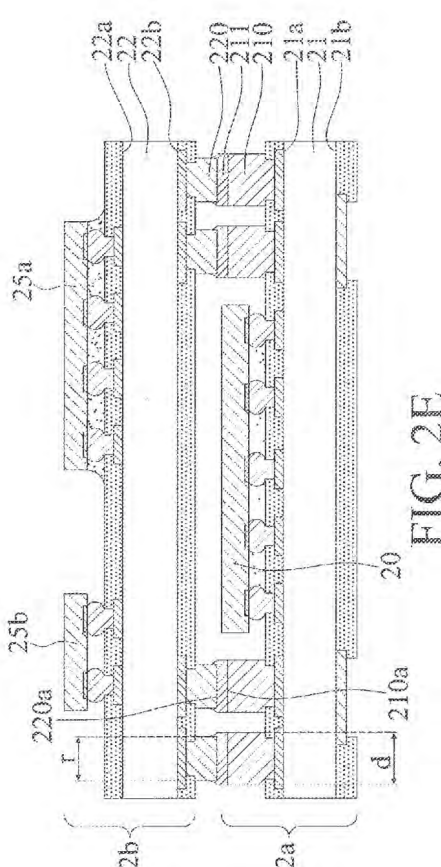
	<p>“Referring to FIG. 3, in another embodiment, the height h’ of the second metal posts 320 can be greater than the height t’ of the first metal posts 310, and the width d (such as diameter) of the end surfaces 310 a of the first metal posts 310 can be greater than the width r (such as diameter) of the end surfaces 320 a of the second metal posts 320.” Hu ’687, [0045].</p> <p>“The second package structure 2 b has a second substrate 22 having a third surface 22 a and a fourth surface 22 b opposite to the third surface 22 a, and at least a second electronic element 25 a, 25 b, 25 ’ disposed on the third surface 22 a and electrically connected to the second substrate 22. The fourth surface 22 b of the second substrate 22 has a plurality of second metal posts 220, 320, 320 ’, 320 ’’, 420 which are connected to the first metal posts 210, 310, 310 ’, 310 ’’, 410, respectively, so as for the second package structure 2 b to be stacked on the first package structure 2 a.” Hu ’687, [0054].</p> <p>“Furthermore, the width d, d’, d’’ of the end surfaces 210 a, 210 b, 210 c, 310 a, 310 b, 310 c of the first metal posts 210, 310, 310 ’, 310 ’’ is greater than, equal to or less than the width r, r’, r’’ of the end surfaces 220 a, 220 b, 220 c, 320 a, 320 b, 320 c of the second metal posts 220, 320, 320 ’, 320 ’’.” Hu ’687, [0058].</p> <p>To the extent Plaintiff contends that Hu ’687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
-------------------------	-------------------

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Hu '687 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2B, a plurality of first metal posts 210 are formed on the exposed surfaces of the contact pads 211 b by electroplating, and a first electronic element 20 is mounted on the exposed surfaces of the bonding pads 211 a through a plurality of solder bumps 200 a, i.e., the electrode pads 200 of the first electronic element 20 are electrically connected to the first substrate 21 in a flip-chip manner, thereby forming a first package structure 2 a. In the present embodiment, the first metal posts 210 are copper posts, and a solder material 211 can be formed on the copper posts for facilitating a subsequent stacking process.” Hu '687, [0033-0034].</p> <p>“Referring to FIG. 2D, a plurality of second metal posts 220 such as copper posts are formed on the exposed surfaces of the contact pads 221 b of the second substrate 22 by electroplating. The height h of the second metal posts 220 is less than the height t of the first metal posts 210 or less than the sum of the height of the first metal posts 210 and the height of the solder material 211.” Hu '687, [0036].</p> <p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a. In the present embodiment,</p>
--	---

	<p>the width d (or maximum diameter) of the end surfaces 210 a (surfaces bonding with the second metal posts 220) of the first metal posts 210 is greater than the width r of the end surfaces 220 a of the second metal posts 220.” Hu '687, [0038-0039].</p>  <p style="text-align: center;">FIG. 2E</p> <p>Hu '687, FIG. 2E.</p> <p>“In the present embodiment, the width d (or maximum diameter) of the end surfaces 210 a (surfaces bonding with the second metal posts 220) of the first metal posts 210 is greater than the width r of the end surfaces 220 a of the second metal posts 220. Such a difference in width facilitates alignment of the first and second package structures so as to avoid the risk of joint deviation.” Hu '687, [0039].</p>
--	---

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>“Further, a solder material 211 is disposed between each of the first metal posts 210, 310, 310', 310", 410 and the corresponding second metal posts 220, 320, 320', 320", 420.” Hu '687, [0057].</p> <p>“Referring to FIG. 5B, a plurality of first metal posts 310 are formed on the exposed surfaces of the contact pads 211 b by electroplating, and a plurality of solder bumps 200 a are formed on the exposed surfaces of the metal bumps 540 so as for the first electronic element 20 to be disposed thereon.” Hu '687, [0061].</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	Hu '687 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

<p>the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>See, e.g.:</p> <p>“Referring to FIG. 2D, a plurality of second metal posts 220 such as copper posts are formed on the exposed surfaces of the contact pads 221 b of the second substrate 22 by electroplating. The height h of the second metal posts 220 is less than the height t of the first metal posts 210 or less than the sum of the height of the first metal posts 210 and the height of the solder material 211. Further, a plurality of second electronic elements 25 a, 25 b are mounted on the exposed surfaces of the bonding pads 221 a of the second substrate 22 through solder bumps 250 a. As such, a second package structure is obtained. The electrode pads 250 of the second electronic elements 25 a, 25 b are electrically connected to the second substrate 22 in a flip-chip manner.” Hu '687, [0036].</p> <div></div> <p>FIG. 2D</p> <p>Hu '687, FIG. 2D.</p>
--	---

Appendix A-12 - Invalidity of U.S. Patent No. 9859202 in view of Hu '687 - U.S. Patent Publication No. 20130175687

	<p>“Referring to FIG. 2E, the second metal posts 220 are connected to the first metal posts 210 (or the solder material 211 on the first metal posts 210), respectively, to thereby stack the second package structure 2 b on the first package structure 2 a.” Hu '687, [0038].</p> <p>To the extent Plaintiff contends that Hu '687 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

U.S. Patent Publication No. 20130249083 (“Hu '083”) is titled Packaging Substrate and lists Dyi-chung Hu, Ying-Chih Chan, and Chun-Ting Lin as inventors. Hu '083 is assigned to Unimicron Technology Corporation. Hu '083 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the '202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff's apparent infringement theory.² Hu '083 is a U.S. patent publication that was filed January 30, 2013 and published January 30, 2013. Hu '083 claims priority to TW 101205295 filed on March 23, 2012. Hu '083 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Hu '083, or otherwise rendered obvious by disclosures and teachings of Hu '083, including under TopWire's apparent interpretation of the Asserted Claims as Samsung understands them from TopWire's Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Hu '083 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Hu '083 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung's other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung's Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Hu '083, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire's March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court's order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire's apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung's interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Hu '083 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

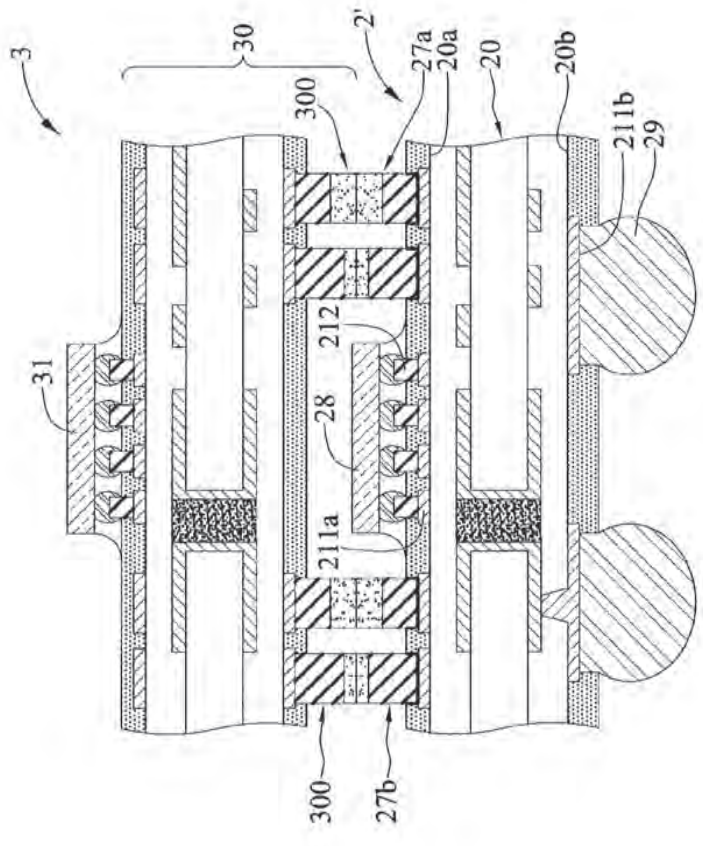
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Hu '083 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Hu '083 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Hu '083 discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 1, a conventional packaging substrate 1 has a substrate body 10 having an upper surface 10 a with a circuit layer 11 a and a lower surface 10 b with a circuit layer 11 b. The circuit layer 11 a has a plurality of bonding pads 111 a, a plurality of first conductive pads 110 a and a plurality of second conductive pads 110 b, and the circuit layer 11 b has a plurality of bonding pads 111 b.” Hu '083, [0005].</p>

	<p>“In view of the above-described drawbacks, the present invention provides a packaging substrate, which comprises: a substrate body having two opposite surfaces respectively provided with a circuit layer, wherein the circuit layer on at least one of the surfaces of the substrate body has a plurality of first conductive pads and a plurality of second conductive pads; an insulating protective layer formed on the substrate body and the circuit layer and having a plurality of openings for exposing the first and second conductive pads; a plurality of first conductive posts respectively formed on the first conductive pads in the openings; a plurality of second conductive posts respectively formed on the second conductive pads in the openings and having a height greater than that of the first conductive posts; a first conductive bonding layer formed on each of the first conductive posts so as for the first conductive posts and the first conductive bonding layer to form first external connection structures; and a second conductive bonding layer formed on each of the second conductive posts so as for the second conductive posts and the second conductive bonding layer to form second external connection structures, wherein the first external connection structures have a height equal to that of the second external connection structures.” Hu ’083, [0010].</p> <p>“Referring to FIG. 2A, a substrate body 20 having an upper surface 20 a and a lower surface 20 b is provided. A circuit layer 21 a is formed on the upper surface 20 a and has a plurality of bonding pads 211 a, a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b. A circuit layer 21 b is formed on the lower surface 20 b and has a plurality of bonding pads 211 b. An insulating protective layer 22 a is formed on the upper surface 20 a, and the circuit layer 21 a and has a plurality of openings 220 a for exposing the bonding pads 211 a and the first and second conductive pads 210 a, 210 b. An insulating protective layer 22 b is formed on the lower surface 20 b and the circuit layer 21 b and has a plurality of openings 220 b for exposing the bonding pads 211 b.” Hu ’083, [0020-0021].</p>
--	---

	<p>“FIG. 3 is a schematic cross-sectional view showing the use of the packaging substrate 2 in subsequent packaging and stacking processes. Referring to FIG. 3, a semiconductor chip 28 is bonded to the bonding pads 211 a through the conductive bumps 212 in a flip-chip manner, and a plurality of solder balls 29 are mounted on the bonding pads 211 b for electrically connecting an electronic device such as a circuit board, so as to form a semiconductor package 2'. Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b.” Hu '083, [0035-0037].</p> <p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b.” Hu '083, [0039].</p>
--	---

	 <p>FIG.3</p>
[1.A] a bottom package substrate;	Hu '083, FIG. 3. Hu '083 discloses, either expressly or inherently, a bottom package substrate.

	<p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2A, a substrate body 20 having an upper surface 20 a and a lower surface 20 b is provided. A circuit layer 21 a is formed on the upper surface 20 a and has a plurality of bonding pads 211 a, a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b. A circuit layer 21 b is formed on the lower surface 20 b and has a plurality of bonding pads 211 b.” Hu ’083, [0020].</p> <p>“In an embodiment, the substrate body 20 further has a core layer 200, a plurality of internal circuits 201 formed on opposite surfaces of the core layer 200, a dielectric layer 202 formed on the core layer 200 and the internal circuits 201, a plurality of conductive vias 203 formed in the dielectric layer 202 for electrically connecting the circuit layers 21 a, 21 b and the internal circuits 201, and a plurality of conductive through holes 204 penetrating the core layer 200 for electrically connecting the internal circuits 201 on the opposite surfaces of the core layer 200. As such, the circuit layers 21 a, 21 b are the outermost circuit layer of the substrate body 20.” Hu ’083, [0022].</p> <p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a</p>
--	---

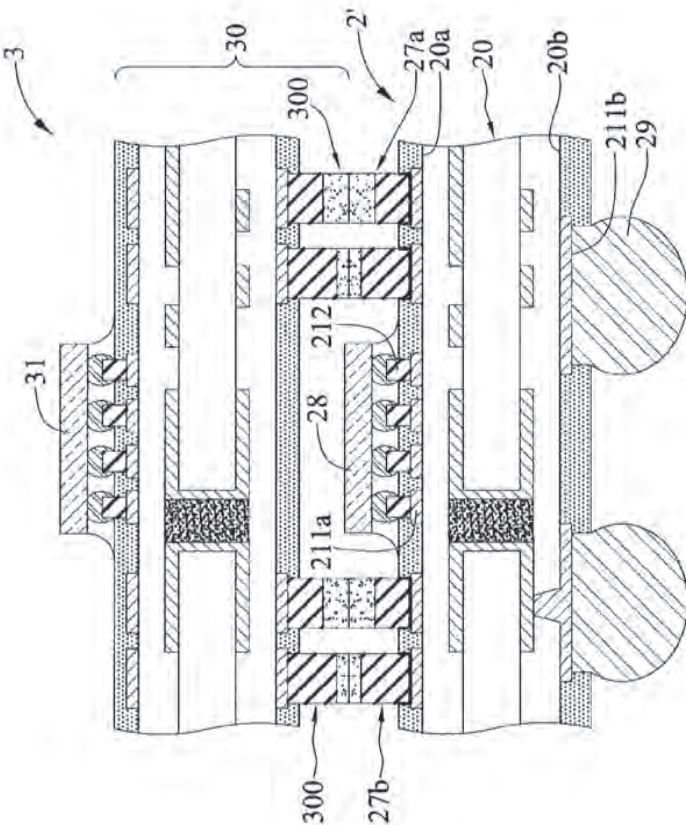
Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b.” Hu ’083, [0039].</p>
--	--

	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p></div>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Hu '083 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2’, thereby forming a package stack structure. In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p>

	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon</p></div>
--	--

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu '083, [0038].</p> <p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hu '083 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In an embodiment, the first and second conductive posts 23 a, 23 b are metal posts such as copper posts.” Hu '083, [0029].</p> <p>“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27 a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second conductive bonding layer 26 b form a plurality of second external connection structures 27 b.” Hu '083, [0030].</p>

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>“Referring to FIG. 3, a semiconductor chip 28 is bonded to the bonding pads 211 a through the conductive bumps 212 in a flip-chip manner, and a plurality of solder balls 29 are mounted on the bonding pads 211 b for electrically connecting an electronic device such as a circuit board, so as to form a semiconductor package 2 ’” Hu ’083, [0036].</p> <p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2 ’, thereby forming a package stack structure.” Hu ’083, [0037].</p>
--	--

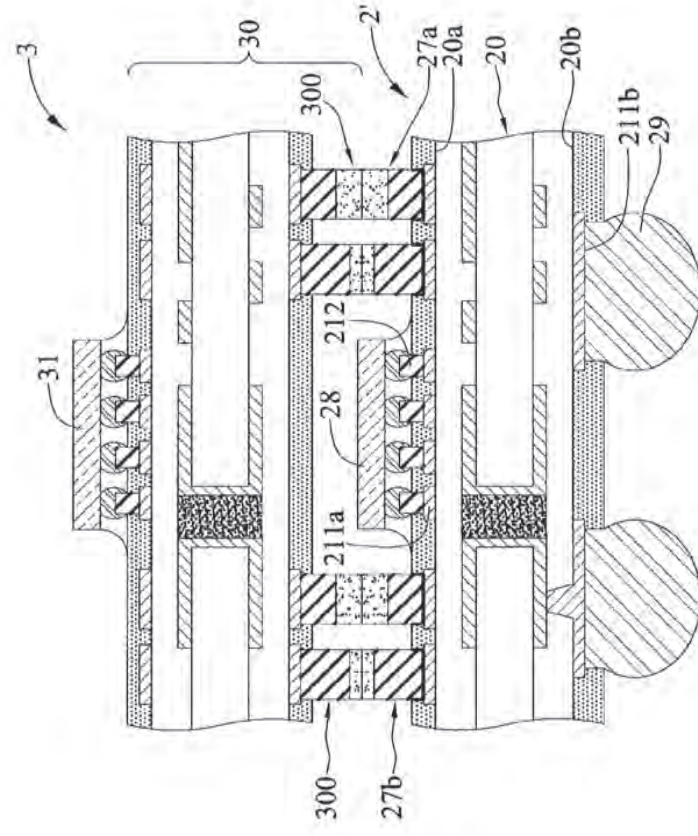
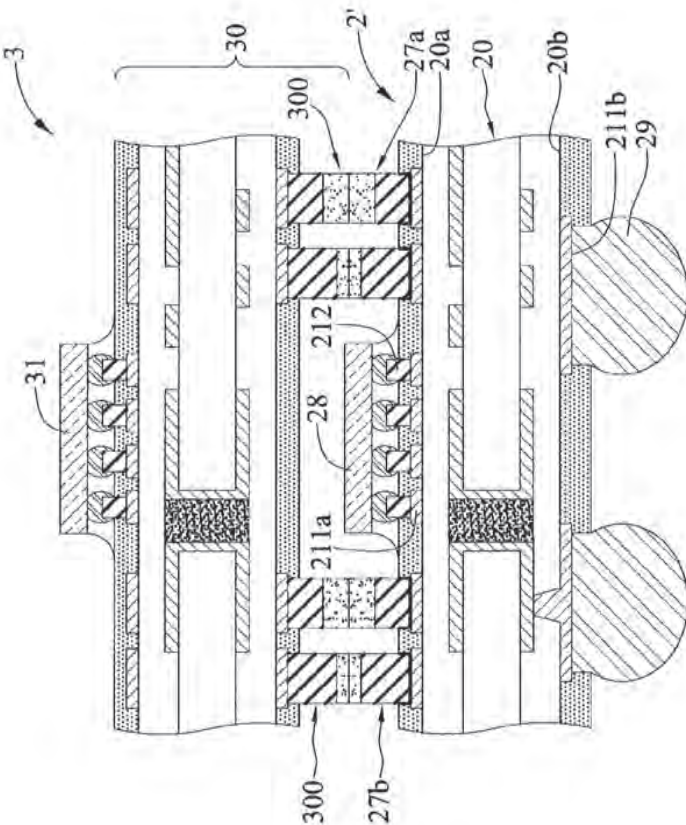


FIG. 3

Hu '083, FIG. 3.

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>“In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p> <p>“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu '083, [0038].</p> <p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Hu '083 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p>

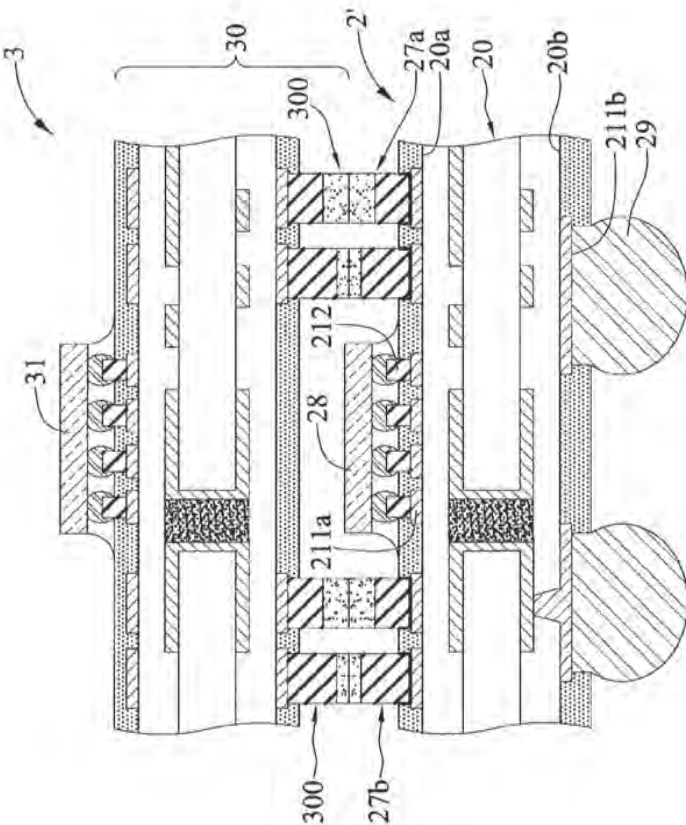
	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p></div>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Hu '083 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“According to the present invention, the conductive posts together with the conductive bonding layer formed thereon form a plurality of external connection structures with the same height so as prevent tilted stack structures and poor coplanarity in a subsequent stacking process, and tHu '083s to improve the product reliability.” Hu '083, [0013].</p> <p>“Referring to FIG. 2C, by using the conductive layer 24 as a current conductive path, an electroplating process is performed such that a plurality of first conductive posts 23 a are respectively formed on the first conductive pads 210 a and a plurality of second conductive posts 23 b are respectively formed on the second conductive pads 210 b. The height h of the second conductive posts 23 b is greater than the height t of the first conductive posts 23 a. In an embodiment, the first and second conductive posts 23 a, 23 b are metal posts such as copper posts.” Hu '083, [0028-0029].</p> <p>“In an embodiment, the first and second conductive posts 23 a, 23 b are metal posts, such as copper posts.” Hu '083, [0029].</p> <p>“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27</p>

	<p>a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second conductive bonding layer 26 b form a plurality of second external connection structures 27 b. The height d of the first external connection structures 27 a is equal to the height d of the second external connection structures 27 b.” Hu ’083, [0030].</p> <p>“In an embodiment, the first and second conductive bonding layers 26 a, 26 b are made of a conductive paste such as a copper paste. Referring to FIG. 2E, the resist layer 25 and the conductive layer 24 under the resist layer 25 are removed. In another embodiment, referring to FIG. 2E’, a plurality of third and fourth external connection structures 27 c, 27 d are further formed on the lower surface 20 b of a substrate body 20’. That is, external connection structures are formed on both the upper and lower surfaces 20 a, 20 b of the substrate body 20’. Since a post made of a copper paste or made of electroplated copper in combination with a copper paste generally has a porous structure, water can easily accumulate in the porous structure during a subsequent wet process, thereby adversely affecting the quality of the structure. Therefore, referring to FIG. 2F, a surface finish layer 270 is formed on each of the first and second external connection structures 27 a, 27 b for facilitating a subsequent solder joint or electrical connection process. In an embodiment, the surface finish layer 270 is made of electroplated nickel/gold, ENIG (Electroless Nickel Immersion Gold) or ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold). In another embodiment, referring to FIG. 2F’, an electroless plated copper layer 270 a is formed on the first and second external connection structures 27 a, 27 b and then an electroplated copper layer 270 b is formed on the electroless plated copper layer 270 such that the electroless plated copper layer 270 a and the electroplated copper layer 270 b constitute a surface finish layer 270’. Preferably, the surface finish layer 270, 270’ has a thickness greater than 3 um. FIG. 3 is a schematic cross-sectional view showing the use of the packaging substrate 2 in subsequent packaging and stacking processes.” Hu ’083, [0031-0035].</p>
--	--

	<p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2', thereby forming a package stack structure. In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p>
--	--

	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon</p></div>
--	--

	<p>constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu ’083, [0038].</p> <p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b.” Hu ’083, [0039].</p> <p>To the extent Plaintiff contends that Hu ’083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Hu '083 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Further, a plurality of first metal posts 13 a are formed on the first conductive pads 110 a, and a plurality of second metal posts 13 b are formed on the second conductive pads 110 b.” Hu '083, [0006].</p> <p>“In view of the above-described drawbacks, the present invention provides a packaging substrate, which comprises: a substrate body having two opposite surfaces respectively provided with a circuit layer, wherein the circuit layer on at least one of the surfaces of the substrate body has a plurality of first conductive pads and a plurality of second conductive pads; an insulating protective layer formed on the substrate body and the circuit layer and having a plurality of openings for exposing the first and second conductive pads; a plurality of first conductive posts respectively formed on the first conductive pads in the openings; a plurality of second conductive posts respectively formed on the second conductive pads in the openings and having a height greater than that of the first conductive posts; a first conductive bonding layer formed on each of the first conductive posts so as for the first conductive posts and the first conductive bonding layer to form first external connection structures; and a second conductive bonding layer formed on each of the second conductive posts so as for the second conductive posts and the second conductive bonding layer to form second external connection structures, wherein the first external connection structures have a height equal to that of the second external connection structures.” Hu '083, [0010].</p>

“In an embodiment, the first and second conductive posts 23 a, 23 b are metal posts such as copper posts.” Hu '083, [0029].

“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27 a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second conductive bonding layer 26 b form a plurality of second external connection structures 27 b.” Hu '083, [0030].

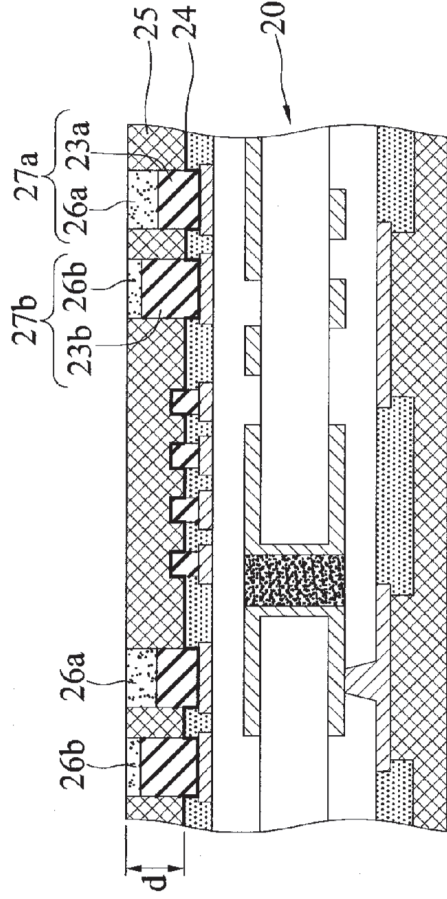
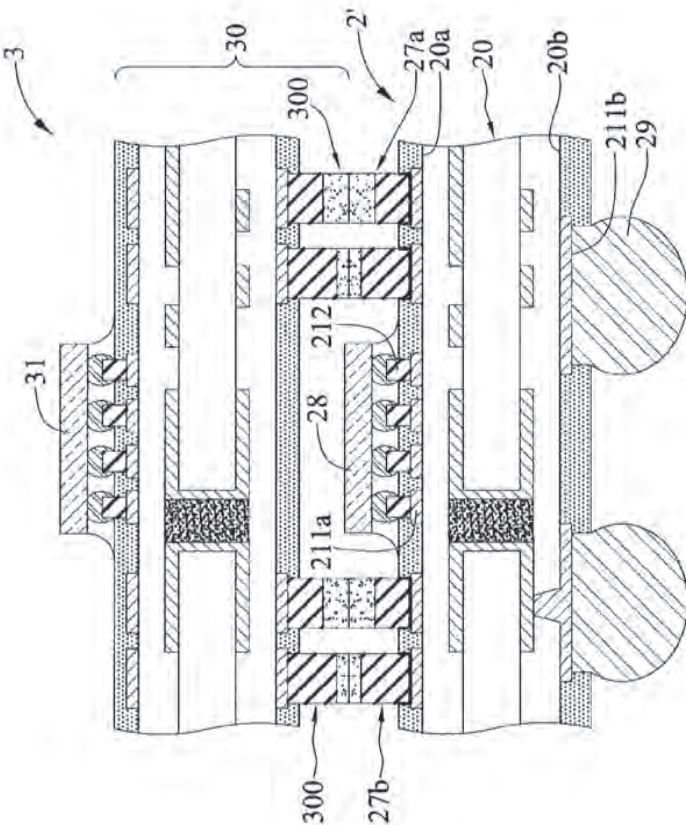


FIG. 2D

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>Hu '083, FIG. 2D.</p> <p>“In an embodiment, the first and second conductive bonding layers 26 a, 26 b are made of a conductive paste such as a copper paste.” Hu '083, [0031].</p> <p>“Therefore, referring to FIG. 2F, a surface finish layer 270 is formed on each of the first and second external connection structures 27 a, 27 b for facilitating a subsequent solder joint or electrical connection process.” Hu '083, [0033].</p> <p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,	<p>Hu '083 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p></div>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Hu '083 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“According to the present invention, the conductive posts together with the conductive bonding layer formed thereon form a plurality of external connection structures with the same height so as prevent tilted stack structures and poor coplanarity in a subsequent stacking process, and tHu '083s to improve the product reliability.” Hu '083, [0013].</p> <p>“Referring to FIG. 2C, by using the conductive layer 24 as a current conductive path, an electroplating process is performed such that a plurality of first conductive posts 23 a are respectively formed on the first conductive pads 210 a and a plurality of second conductive posts 23 b are respectively formed on the second conductive pads 210 b. The height h of the second conductive posts 23 b is greater than the height t of the first conductive posts 23 a. In an embodiment, the first and second conductive posts 23 a, 23 b are metal posts such as copper posts.” Hu '083, [0028-0029].</p> <p>“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27 a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second</p>

	<p>conductive bonding layer 26 b form a plurality of second external connection structures 27 b. The height d of the first external connection structures 27 a is equal to the height d of the second external connection structures 27 b.” Hu ’083, [0030].</p> <p>“In an embodiment, the first and second conductive bonding layers 26 a, 26 b are made of a conductive paste such as a copper paste. Referring to FIG. 2E, the resist layer 25 and the conductive layer 24 under the resist layer 25 are removed. In another embodiment, referring to FIG. 2E’, a plurality of third and fourth external connection structures 27 c, 27 d are further formed on the lower surface 20 b of a substrate body 20’. That is, external connection structures are formed on both the upper and lower surfaces 20 a, 20 b of the substrate body 20’. Since a post made of a copper paste or made of electroplated copper in combination with a copper paste generally has a porous structure, water can easily accumulate in the porous structure during a subsequent wet process, thereby adversely affecting the quality of the structure. Therefore, referring to FIG. 2F, a surface finish layer 270 is formed on each of the first and second external connection structures 27 a, 27 b for facilitating a subsequent solder joint or electrical connection process. In an embodiment, the surface finish layer 270 is made of electroplated nickel/gold, ENIG (Electroless Nickel Immersion Gold) or ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold). In another embodiment, referring to FIG. 2F’, an electroless plated copper layer 270 a is formed on the first and second external connection structures 27 a, 27 b and then an electroplated copper layer 270 b is formed on the electroless plated copper layer 270 such that the electroless plated copper layer 270 a and the electroplated copper layer 270 b constitute a surface finish layer 270’. Preferably, the surface finish layer 270, 270’ has a thickness greater than 3 um. FIG. 3 is a schematic cross-sectional view showing the use of the packaging substrate 2 in subsequent packaging and stacking processes.” Hu ’083, [0031-0035].</p>
--	---

	<p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2', thereby forming a package stack structure. In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p>
--	--

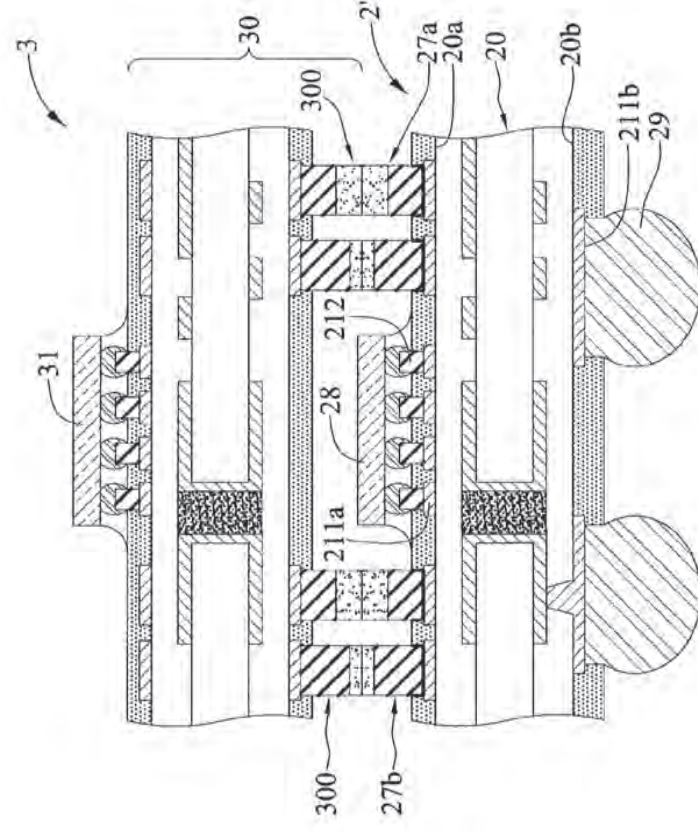


FIG.3

Hu '083, FIG. 3.

“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon

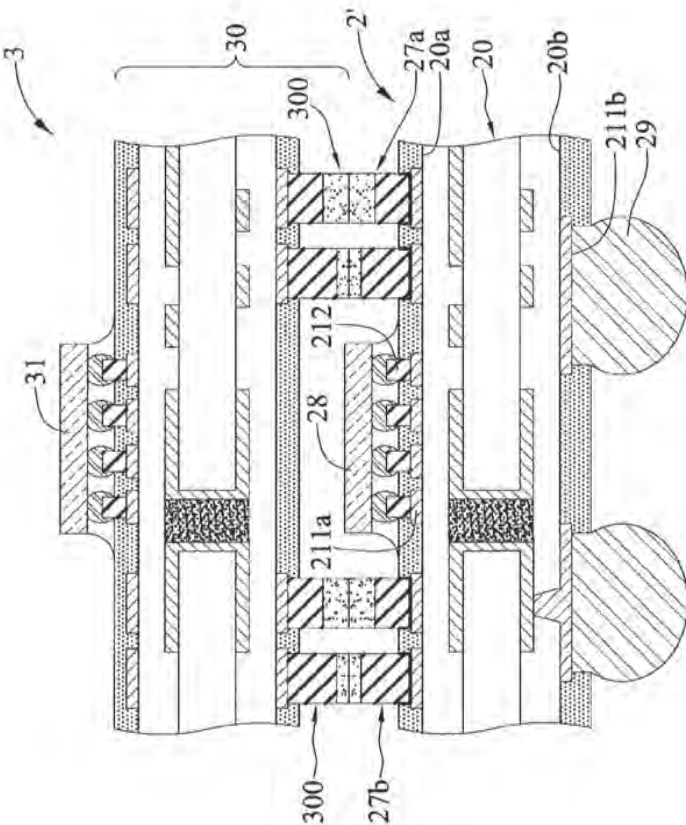
	<p>constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu ’083, [0038].</p> <p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b.” Hu ’083, [0039].</p> <p>To the extent Plaintiff contends that Hu ’083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Hu '083 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“According to the present invention, the conductive posts together with the conductive bonding layer formed thereon form a plurality of external connection structures with the same height so as prevent tilted stack structures and poor coplanarity in a subsequent stacking process, and tHu '083s to improve the product reliability.” Hu '083, [0013].</p> <p>“Referring to FIG. 2C, by using the conductive layer 24 as a current conductive path, an electroplating process is performed such that a plurality of first conductive posts 23 a are respectively formed on the first conductive pads 210 a and a plurality of second conductive posts 23 b are respectively formed on the second conductive pads 210 b. The height h of the second conductive posts 23 b is greater than the height t of the first conductive posts 23 a. In an embodiment, the first and second conductive posts 23 a, 23 b are metal posts such as copper posts.” Hu '083, [0028-0029].</p> <p>“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27 a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second</p>

	<p>conductive bonding layer 26 b form a plurality of second external connection structures 27 b. The height d of the first external connection structures 27 a is equal to the height d of the second external connection structures 27 b.” Hu ’083, [0030].</p> <p>“In an embodiment, the first and second conductive bonding layers 26 a, 26 b are made of a conductive paste such as a copper paste. Referring to FIG. 2E, the resist layer 25 and the conductive layer 24 under the resist layer 25 are removed. In another embodiment, referring to FIG. 2E’, a plurality of third and fourth external connection structures 27 c, 27 d are further formed on the lower surface 20 b of a substrate body 20’. That is, external connection structures are formed on both the upper and lower surfaces 20 a, 20 b of the substrate body 20’. Since a post made of a copper paste or made of electroplated copper in combination with a copper paste generally has a porous structure, water can easily accumulate in the porous structure during a subsequent wet process, thereby adversely affecting the quality of the structure. Therefore, referring to FIG. 2F, a surface finish layer 270 is formed on each of the first and second external connection structures 27 a, 27 b for facilitating a subsequent solder joint or electrical connection process. In an embodiment, the surface finish layer 270 is made of electroplated nickel/gold, ENIG (Electroless Nickel Immersion Gold) or ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold). In another embodiment, referring to FIG. 2F’, an electroless plated copper layer 270 a is formed on the first and second external connection structures 27 a, 27 b and then an electroplated copper layer 270 b is formed on the electroless plated copper layer 270 such that the electroless plated copper layer 270 a and the electroplated copper layer 270 b constitute a surface finish layer 270’. Preferably, the surface finish layer 270, 270’ has a thickness greater than 3 um. FIG. 3 is a schematic cross-sectional view showing the use of the packaging substrate 2 in subsequent packaging and stacking processes.” Hu ’083, [0031-0035].</p>
--	---

	<p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2', thereby forming a package stack structure. In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p>
--	--

	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon</p></div>
--	--

	<p>constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu ’083, [0038].</p> <p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b.” Hu ’083, [0039].</p> <p>To the extent Plaintiff contends that Hu ’083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Hu '083 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In view of the above-described drawbacks, the present invention provides a packaging substrate, which comprises: a substrate body having two opposite surfaces respectively provided with a circuit layer, wherein the circuit layer on at least one of the surfaces of the substrate body has a plurality of first conductive pads and a plurality of second conductive pads; an insulating protective layer formed on the substrate body and the circuit layer and having a plurality of openings for exposing the first and second conductive pads; a plurality of first conductive posts respectively formed on the first conductive pads in the openings; a plurality of second conductive posts respectively formed on the second conductive pads in the openings and having a height greater than that of the first conductive posts; a first conductive bonding layer formed on each of the first conductive posts so as for the first conductive posts and the first conductive bonding layer to form first external connection structures; and a second conductive bonding layer formed on each of the second conductive posts so as for the second conductive posts and the second conductive bonding layer to form second external connection structures, wherein the first external connection structures have a height equal to that of the second external connection structures.” Hu '083, [0010].</p>

	<p>“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27 a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second conductive bonding layer 26 b form a plurality of second external connection structures 27 b.” Hu '083, [0030].</p> <p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2 ', thereby forming a package stack structure.” Hu '083, [0037].</p>
--	---

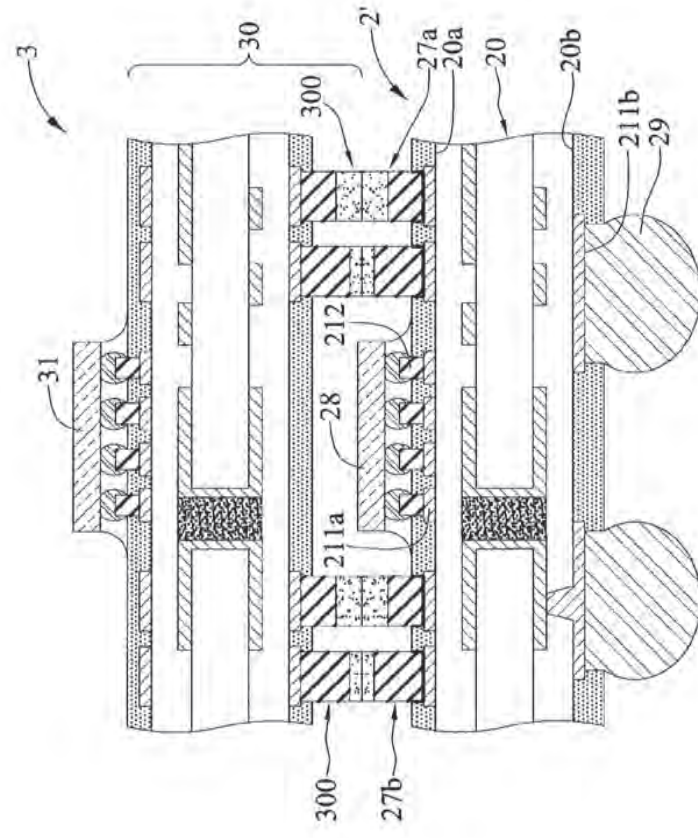


FIG. 3

Hu '083, FIG. 3.

	<p>“In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p> <p>“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu '083, [0038].</p> <p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form</p>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b.” Hu ’083, [0039].</p> <p>To the extent Plaintiff contends that Hu ’083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hu ’083 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2A, a substrate body 20 having an upper surface 20 a and a lower surface 20 b is provided. A circuit layer 21 a is formed on the upper surface 20 a and has a plurality of bonding pads 211 a, a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b.” Hu ’083, [0020].</p> <p>“In an embodiment, the bonding pads 211 a on the upper surface 20 a serve as flip-chip bonding pads for electrically connecting a semiconductor chip, and hence a plurality of conductive bumps 212 are formed on the bonding pads 211 a, respectively.” Hu ’083, [0024].</p> <p>“FIG. 3 is a schematic cross-sectional view showing the use of the packaging substrate 2 in subsequent packaging and stacking processes. Referring to FIG. 3, a semiconductor chip 28 is bonded to the bonding pads 211 a through the conductive bumps 212 in a flip-chip manner, and a plurality of solder balls 29 are mounted on the bonding pads 211 b for electrically</p>

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>connecting an electronic device such as a circuit board, so as to form a semiconductor package 2 '. Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2 ', thereby forming a package stack structure." Hu '083, [0035-0037].</p>
--	--

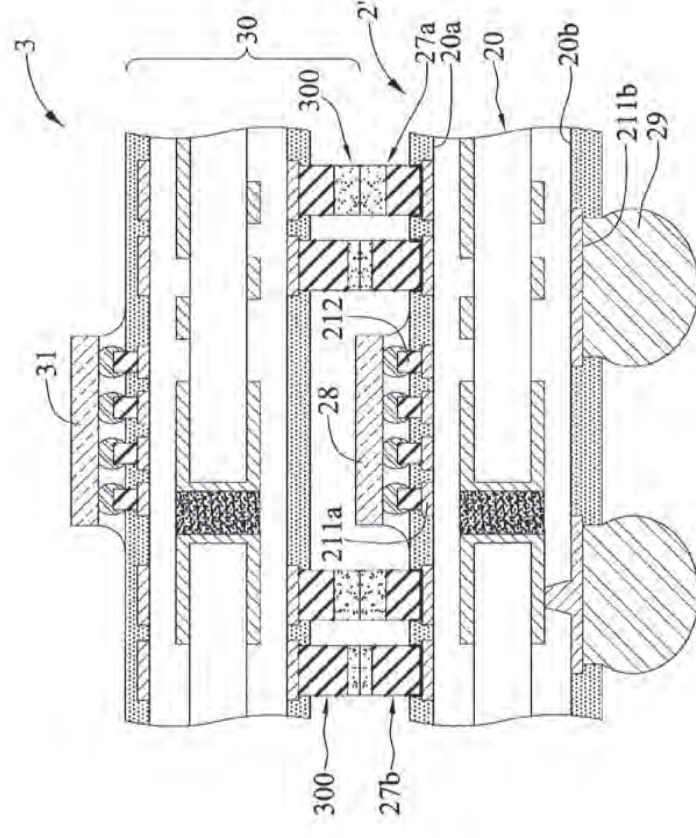


FIG.3

Hu '083, FIG. 3.

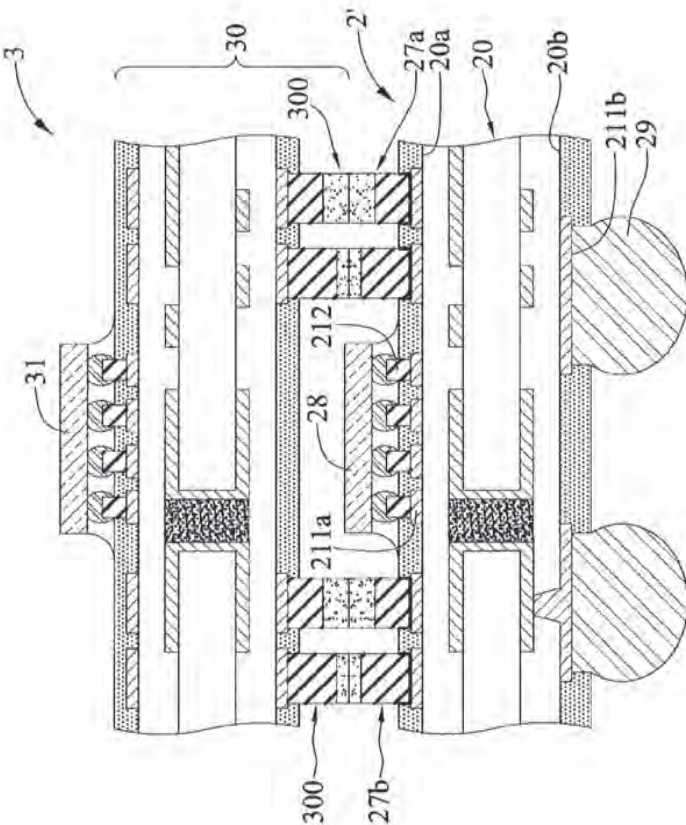
“Referring to FIG. 3, a semiconductor chip 28 is bonded to the bonding pads 211 a through the conductive bumps 212 in a flip-chip manner, and a plurality of solder balls 29 are

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>mounted on the bonding pads 211 b for electrically connecting an electronic device such as a circuit board, so as to form a semiconductor package 2 '." Hu '083, [0036].</p> <p>"Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connections 300 formed on the packaging substrate 30. The external connections 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2 ', thereby forming a package stack structure." Hu '083, [0037].</p> <p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Hu '083 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>"Referring to FIG. 2A, a substrate body 20 having an upper surface 20 a and a lower surface 20 b is provided. A circuit layer 21 a is formed on the upper surface 20 a and has a plurality of bonding pads 211 a, a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b." Hu '083, [0020].</p>

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>“In an embodiment, the bonding pads 211 a on the upper surface 20 a serve as flip-chip bonding pads for electrically connecting a semiconductor chip, and hence a plurality of conductive bumps 212 are formed on the bonding pads 211 a, respectively.” Hu ’083, [0024].</p> <p>“In another embodiment, the bonding pads 211 a on the upper surface 20 a can serve as wire bonding pads (not shown) for electrically connecting a semiconductor chip through bonding wires.” Hu ’083, [0024].</p> <p>“FIG. 3 is a schematic cross-sectional view showing the use of the packaging substrate 2 in subsequent packaging and stacking processes.” Hu ’083, [0035].</p> <p>“Referring to FIG. 3, a semiconductor chip 28 is bonded to the bonding pads 211 a through the conductive bumps 212 in a flip-chip manner, and a plurality of solder balls 29 are mounted on the bonding pads 211 b for electrically connecting an electronic device such as a circuit board, so as to form a semiconductor package 2 ’. Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b.” Hu ’083, [0036-0037].</p>
--	--

	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p></div>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Hu '083 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connections 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2', thereby forming a package stack structure. In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p>

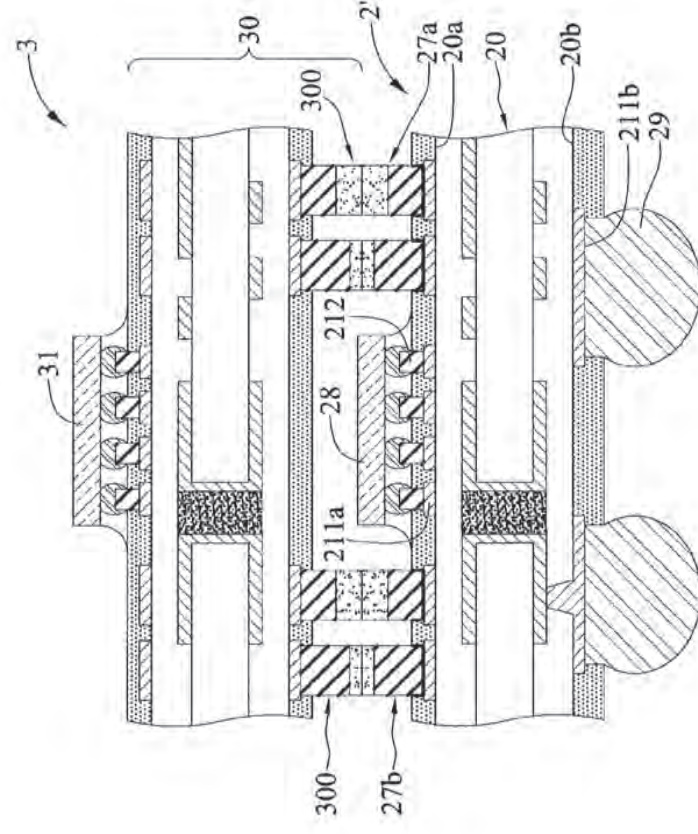


FIG.3

Hu '083, FIG. 3.

“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon

	<p>constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu '083, [0038].</p> <p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b. In an embodiment, the first and second conductive posts 23 a, 23 b are metal posts, such as copper posts.” Hu '083, [0039-0041].</p>
--	--

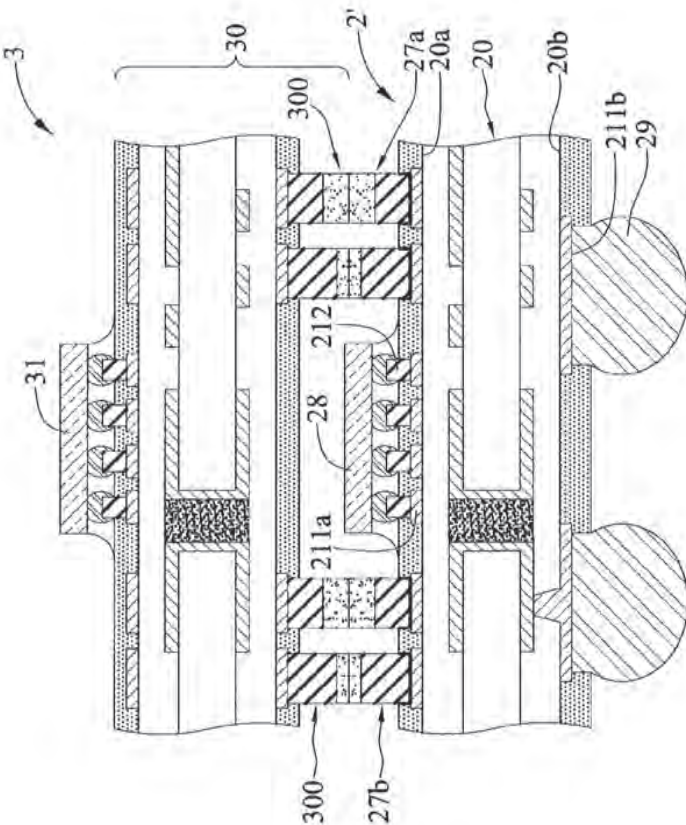
Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Hu '083 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2A, a substrate body 20 having an upper surface 20 a and a lower surface 20 b is provided. A circuit layer 21 a is formed on the upper surface 20 a and has a plurality of bonding pads 211 a, a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b.” Hu '083, [0020].</p> <p>“In an embodiment, the bonding pads 211 a on the upper surface 20 a serve as flip-chip bonding pads for electrically connecting a semiconductor chip, and hence a plurality of conductive bumps 212 are formed on the bonding pads 211 a, respectively.” Hu '083, [0024].</p> <p>“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27</p>

	<p>a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second conductive bonding layer 26 b form a plurality of second external connection structures 27 b. The height d of the first external connection structures 27 a is equal to the height d of the second external connection structures 27 b.” Hu ’083, [0030].</p> <p>“Referring to FIG. 3, a semiconductor chip 28 is bonded to the bonding pads 211 a through the conductive bumps 212 in a flip-chip manner, and a plurality of solder balls 29 are mounted on the bonding pads 211 b for electrically connecting an electronic device such as a circuit board, so as to form a semiconductor package 2 ’. Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2 ’, thereby forming a package stack structure.” Hu ’083, [0036-0037].</p>
--	--

	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon</p></div>
--	--

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

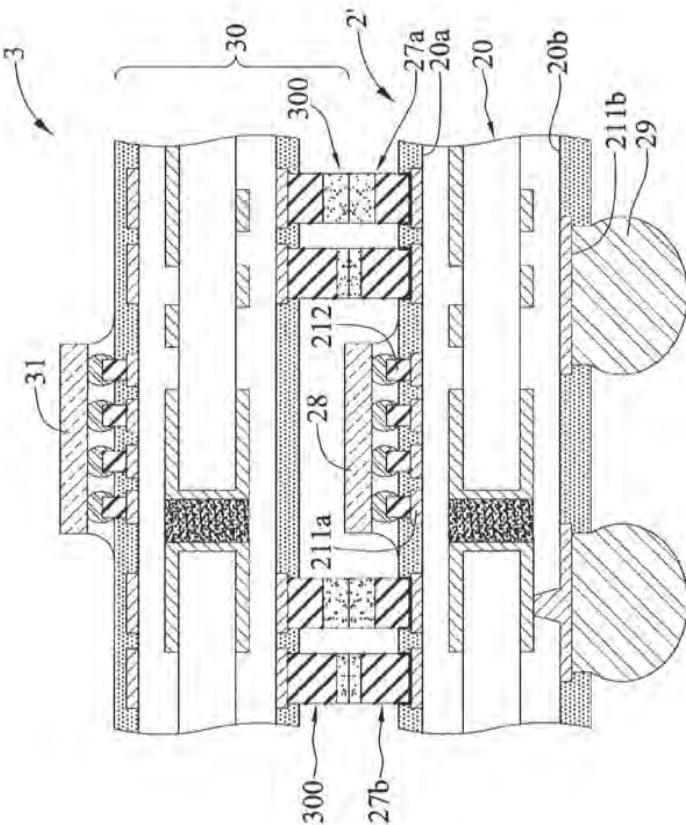
	<p>constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu '083, [0038].</p> <p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Hu '083 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package</p>

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>3 to be stacked on the semiconductor package 2', thereby forming a package stack structure.</p> <p>In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b." Hu '083, [0037].</p>
--	--

	<div></div> <div><p>FIG.3</p></div> <div><p>Hu '083, FIG. 3.</p></div> <div><p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 21 a with a circuit layer 21 a and a lower surface 20 b with a</p></div>
--	--

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b.” Hu ’083, [0039].</p> <p>To the extent Plaintiff contends that Hu ’083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Hu '083 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2C, by using the conductive layer 24 as a current conductive path, an electroplating process is performed such that a plurality of first conductive posts 23 a are respectively formed on the first conductive pads 210 a and a plurality of second conductive posts 23 b are respectively formed on the second conductive pads 210 b.” Hu '083, [0028].</p> <p>“In an embodiment, the first and second conductive posts 23 a, 23 b are metal posts such as copper posts.” Hu '083, [0029].</p> <p>“The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2', thereby forming a package stack structure.” Hu '083, [0037].</p>
--	---

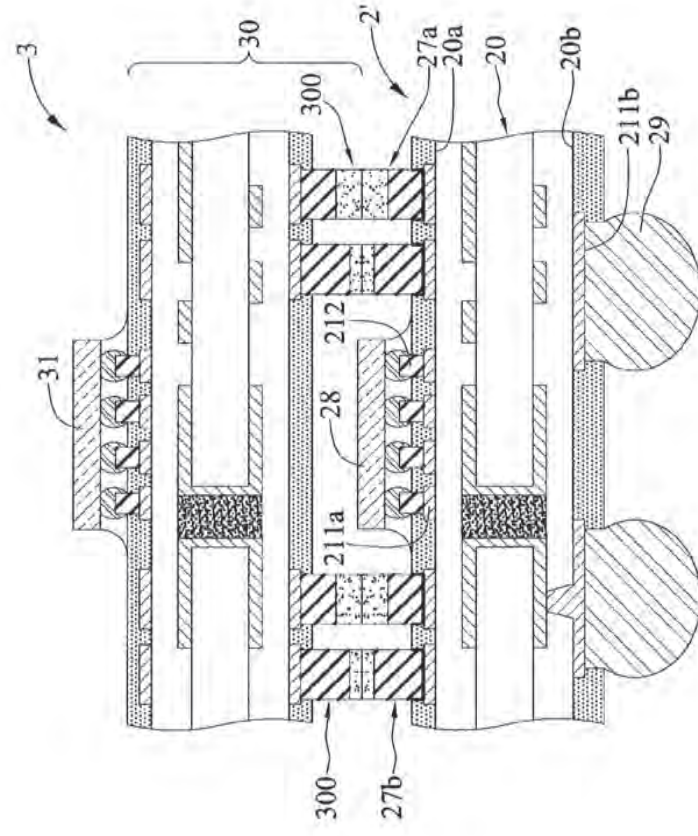


FIG. 3

Hu '083, FIG. 3.

	<p>“The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30.” Hu '083, [0037].</p> <p>“In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p> <p>“The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b.” Hu '083, [0039].</p>
--	---

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

	<p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Hu '083 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27 a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second conductive bonding layer 26 b form a plurality of second external connection structures 27 b.” Hu '083, [0030].</p>

	<p>“Therefore, referring to FIG. 2F, a surface finish layer 270 is formed on each of the first and second external connection structures 27 a, 27 b for facilitating a subsequent solder joint or electrical connection process.” Hu ’083, [0033].</p> <p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connections 300 formed on the packaging substrate 30. The external connections 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package 3 to be stacked on the semiconductor package 2 ’, thereby forming a package stack structure.” Hu ’083, [0037].</p>
--	---

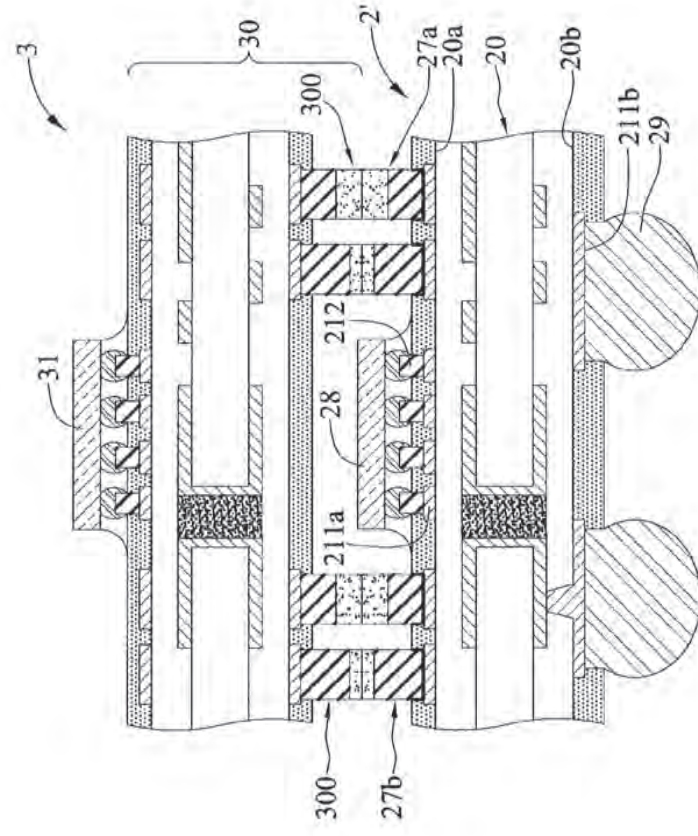


FIG. 3

Hu '083, FIG. 3.

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

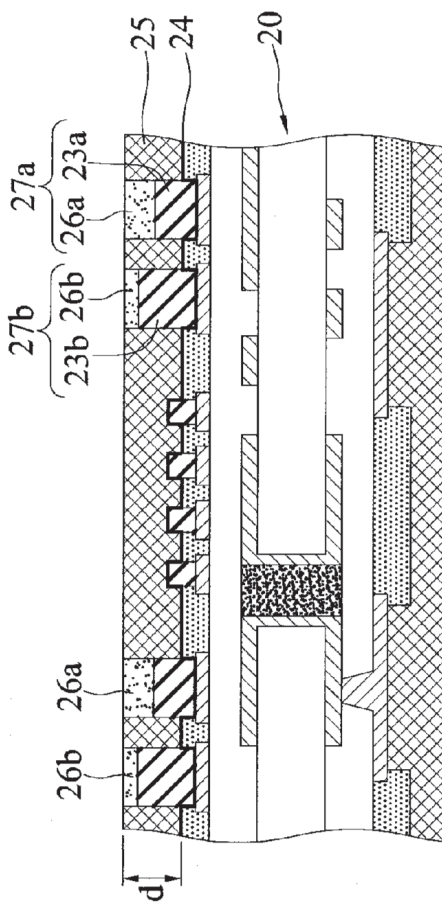
	<p>“In an embodiment, the packaging substrate 30 is similar to the packaging substrate 2, and the external connection structures 30 are similar to the first and second external connection structures 27 a, 27 b.” Hu '083, [0037].</p> <p>“In the packaging substrate 2, the first and second conductive posts 23 a, 23 b together with the first and second conductive bonding layers 26 a, 26 b respectively formed thereon constitute a plurality of first and second external connection structures 27 a, 27 b having the same height d, thereby preventing tilt of the packaging substrate 30 during a subsequent stacking process, improving the coplanarity and consequently effectively improving the product reliability.” Hu '083, [0038].</p> <p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom	Hu '083 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom

Appendix A-13 - Invalidity of U.S. Patent No. 9859202 in view of Hu '083 - U.S. Patent Publication No. 20130249083

<p>pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2C, by using the conductive layer 24 as a current conductive path, an electroplating process is performed such that a plurality of first conductive posts 23 a are respectively formed on the first conductive pads 210 a and a plurality of second conductive posts 23 b are respectively formed on the second conductive pads 210 b.” Hu '083, [0028].</p> <p>“Referring to FIG. 2D, a first conductive bonding layer 26 a is formed on each of the first conductive posts 23 a by printing or coating such that the first conductive posts 23 a and the first conductive bonding layer 26 a form a plurality of first external connection structures 27 a; and a second conductive bonding layer 26 b is formed on each of the second conductive posts 23 b by printing or coating such that the second conductive posts 23 b and the second conductive bonding layer 26 b form a plurality of second external connection structures 27 b. The height d of the first external connection structures 27 a is equal to the height d of the second external connection structures 27 b.” Hu '083, [0030].</p>
---	--

	<div></div> <div><p>FIG.2D</p></div> <div><p>Hu '083, FIG. 2D.</p></div> <div><p>“Therefore, referring to FIG. 2F, a surface finish layer 270 is formed on each of the first and second external connection structures 27 a, 27 b for facilitating a subsequent solder joint or electrical connection process.” Hu '083, [0033].</p></div> <div><p>“Then, a package 3 is bonded to the first and second external connection structures 27 a, 27 b. The package 3 has a packaging substrate 30, a semiconductor chip 31 disposed on the packaging substrate 30 and a plurality of external connection structures 300 formed on the packaging substrate 30. The external connection structures 30 are aligned and bonded to the first and second external connection structures 27 a, 27 b, respectively, so as for the package</p></div>
--	--

	<p>3 to be stacked on the semiconductor package 2', thereby forming a package stack structure." Hu '083, [0037].</p> <p>"The present invention further provides a packaging substrate 2, which has a substrate body 20 having an upper surface 20 a with a circuit layer 21 a and a lower surface 20 b with a circuit layer 21 b, wherein the circuit layers 21 a, 21 b have a plurality of bonding pads 211 a, 211 b, respectively, and the circuit layer 21 a further has a plurality of first conductive pads 210 a and a plurality of second conductive pads 210 b; an insulating protective layer 22 a formed on the upper surface 20 a and the circuit layer 21 a and an insulating protective layer 22 b formed on the lower surface 20 b and the circuit layer 21 b, wherein the insulating protective layer 22 a has a plurality of openings 220 a for exposing the first and second conductive pads 210 a, 210 b, respectively; a plurality of first conductive posts 23 a respectively formed on the first conductive pads 210 a; a plurality of second conductive posts 23 b respectively formed on the second conductive pads 210 b and having a height greater than that of the first conductive posts 23 a; a first conductive bonding layer 26 a formed on each of the first conductive posts 23 a so as for the first conductive posts 23 a and the first conductive bonding layer 26 a to form first external connection structures 27 a; and a second conductive bonding layer 26 b formed on each of the second conductive posts 23 b so as for the second conductive posts 23 b and the second conductive bonding layer 26 b to form second external connection structures 27 b, wherein the first external connection structures 27 a have a height equal to that of the second external connection structures 27 b." Hu '083, [0039].</p> <p>To the extent Plaintiff contends that Hu '083 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

U.S. Patent No. 9357659 (“Hu ’659”) is titled Packaging Substrate Having Embedded Through-Via Interposer and lists Dyi-Chung Hu, and Tzyy-Jang Tseng as inventors. Hu ’659 is assigned to Unimicron Technology Corporation. Hu ’659 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Hu ’659 is a U.S. patent that was filed January 22, 2015 and published May 14, 2015. Hu ’659 claims priority to TW 100139667 filed on October 31, 2011. Hu ’659 is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Hu ’659, or otherwise rendered obvious by disclosures and teachings of Hu ’659, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Hu ’659 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Hu ’659 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Hu ’659, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Hu '659 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Hu '659 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Hu '659 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Hu '659 discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2I, a multi-layer circuit structure may be formed according to practical needs. In an embodiment, the built-up structure 23 has at least a dielectric layer 230, a circuit layer 231 embedded in the dielectric layer 230, and a plurality of conductive vias 232 formed in the dielectric layer 230 and electrically connected with the circuit layer 231. Portions of the conductive vias 232' electrically connect with the second end surfaces 200 b of the conductive through-vias 200.” Hu '659, [6:18-6:26].</p>

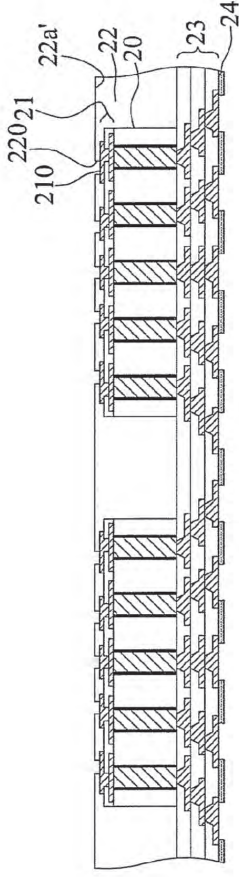


FIG. 2I'

Hu '659, FIG. 2I'.

“Referring to FIGS. 2J, 2J' and 2J'', the structure of FIG. 2I, 2I' or 2I'' is singulated along imaginary scribing lines L of FIG. 2I so as to obtain a plurality of packaging substrates 2, 2' or 2'' having an embedded through-via interposer 20.” Hu '659, [6:44-6:47].

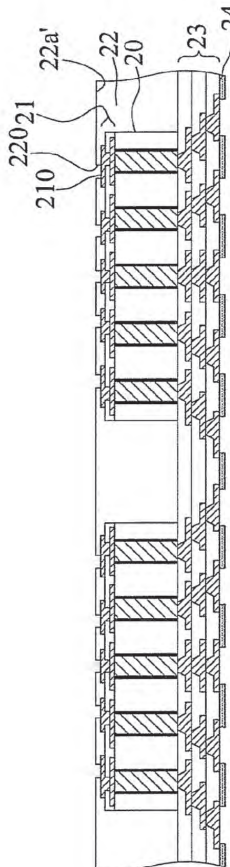
“The present invention further provides a packaging substrate 2, 2', 2'' having an embedded through-via interposer 20. The packaging substrate 2, 2', 2'' comprises an encapsulant layer 22 having a first surface 22 a, 22 a', 22 a'' and an opposite second surface 22 b; a through-via interposer 20 embedded in the encapsulant layer 22, a redistribution layer 21 embedded in the encapsulant layer 22 and formed on the through-via interposer 20, a built-up structure 23 formed on the second surface 22 b of the encapsulant layer 22, and an insulating protective layer 24 formed on the built-up structure 23. The through-via interposer 20 has opposite first surface 20 a and second side 20 b, and a plurality of conductive through-vias 200 in communication with the first side 20 a and the second side 20 b. Each of the conductive through-vias 200 has a first end surface 200 a on the first side 20 a of the through-via

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>interposer 20, and a second end surface 200 b on the second side 20 b of the through-via interposer 20, and an insulating layer 201 is formed on the sidewall of the conductive through-via 200. The second side 20 b of the through-via interposer 20 and the second end surfaces 200 b of the conductive through-vias 200 are flush with the second surface 22 b of the encapsulant layer 22.” Hu '659, [6:56-7:10].</p>
<p>[1.A] a bottom package substrate;</p>	<p>Hu '659 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 2G to 2I, a built-up structure 23 is formed on the second surface 22 b of the encapsulant layer 22, the second sides 20 b of the interposers 20, and the second end surfaces 200 b of the conductive through-vias 200.” Hu '659, [5:52-5:55].</p> <div> </div> <p style="text-align: center;">FIG. 2I'</p> <p>Hu '659, FIG. 2I'.</p>

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>“Referring to FIGS. 2J, 2J’ and 2 J”, the structure of FIG. 2I, 2I’ or 2 I” is singulated along imaginary scribing lines L of FIG. 2I so as to obtain a plurality of packaging substrates 2, 2’ or 2” having an embedded through-via interposer 20. Before or after the singulation process, a plurality of solder balls 25 can be mounted on the conductive pads 233 for other electronic devices such as printed circuit boards or semiconductor packages to be mounted thereon.” Hu ’659, [6:44-6:51].</p> <p>“Before or after the singulation process, a plurality of solder balls 25 can be mounted on the conductive pads 233 for other electronic devices such as printed circuit boards or semiconductor packages to be mounted thereon.” Hu ’659, [6:48-6:51].</p> <p>“Referring to FIGS. 3E, 3E’ and 3 E”, the structures 3 D, 3 D’ and 3 D” are singulated along the imaginary scribing lines L of FIG. 3D so as to obtain a plurality of packaging substrates 3, 3’ and 3” having an embedded through-via interposer 30. Before or after the singulation process, a plurality of solder balls 25 can be mounted on the conductive pads 233 for electrically connecting to other electronic devices such as printed circuit boards or packages.” Hu ’659, [8:40-8:47].</p> <p>To the extent Plaintiff contends that Hu ’659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Hu ’659 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	 <p style="text-align: center;">FIG. 2I'</p> <p>Hu '659, FIG. 2I'.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hu '659 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2I, a multi-layer circuit structure may be formed according to practical needs. In an embodiment, the built-up structure 23 has at least a dielectric layer 230, a circuit layer 231 embedded in the dielectric layer 230, and a plurality of conductive vias 232 formed in the dielectric layer 230 and electrically connected with the circuit layer 231. Portions of</p>

the conductive vias 232' electrically connect with the second end surfaces 200 b of the conductive through-vias 200." Hu '659, [6:18-6:26].

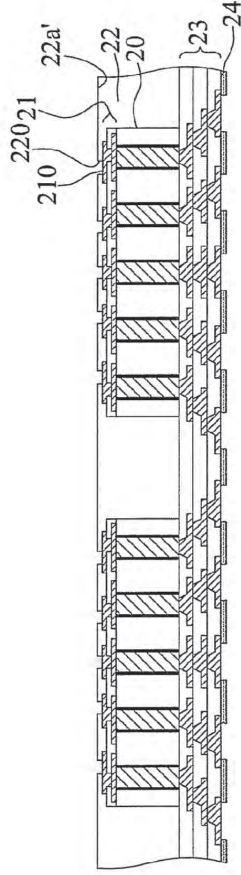


FIG. 2I'

Hu '659, FIG. 2I'.

"The present invention further provides a packaging substrate 2, 2', 2'' having an embedded through-via interposer 20. The packaging substrate 2, 2', 2'' comprises an encapsulant layer 22 having a first surface 22 a, 22 a', 22 a'' and an opposite second surface 22 b; a through-via interposer 20 embedded in the encapsulant layer 22, a redistribution layer 21 embedded in the encapsulant layer 22 and formed on the through-via interposer 20, a built-up structure 23 formed on the second surface 22 b of the encapsulant layer 22, and an insulating protective layer 24 formed on the built-up structure 23. The through-via interposer 20 has opposite first surface 20 a and second side 20 b, and a plurality of conductive through-vias 200 in communication with the first side 20 a and the second side 20 b. Each of the conductive through-vias 200 has a first end surface 200 a on the first side 20 a of the through-via interposer 20, and a second end surface 200 b on the second side 20 b of the through-via

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>interposer 20, and an insulating layer 201 is formed on the sidewall of the conductive through-via 200. The second side 20 b of the through-via interposer 20 and the second end surfaces 200 b of the conductive through-vias 200 are flush with the second surface 22 b of the encapsulant layer 22.” Hu ’659, [6:56-7:10].</p> <p>To the extent Plaintiff contends that Hu ’659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Hu ’659 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 2G to 2I, a built-up structure 23 is formed on the second surface 22 b of the encapsulant layer 22, the second sides 20 b of the interposers 20, and the second end surfaces 200 b of the conductive through-vias 200.” Hu ’659, [5:52-5:55].</p> <p>“Referring to FIG. 2I, a multi-layer circuit structure may be formed according to practical needs. In an embodiment, the built-up structure 23 has at least a dielectric layer 230, a circuit layer 231 embedded in the dielectric layer 230, and a plurality of conductive vias 232 formed in the dielectric layer 230 and electrically connected with the circuit layer 231. Portions of the conductive vias 232’ electrically connect with the second end surfaces 200 b of the conductive through-vias 200.” Hu ’659, [6:18-6:26].</p>

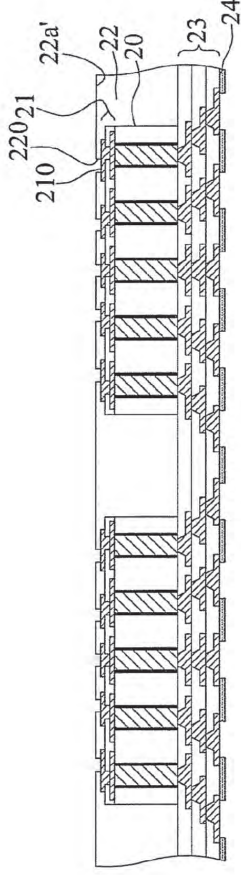


FIG. 2I'

Hu '659, FIG. 2I'.

“The present invention further provides a packaging substrate 2, 2', 2'' having an embedded through-via interposer 20. The packaging substrate 2, 2', 2'' comprises an encapsulant layer 22 having a first surface 22 a, 22 a', 22 a'' and an opposite second surface 22 b; a through-via interposer 20 embedded in the encapsulant layer 22, a redistribution layer 21 embedded in the encapsulant layer 22 and formed on the through-via interposer 20, and an insulating protective layer 24 formed on the built-up structure 23. The through-via interposer 20 has opposite first surface 20 a and second side 20 b, and a plurality of conductive through-vias 200 in communication with the first side 20 a and the second side 20 b. Each of the conductive through-vias 200 has a first end surface 200 a on the first side 20 a of the through-via interposer 20, and a second end surface 200 b on the second side 20 b of the through-via interposer 20, and an insulating layer 201 is formed on the sidewall of the conductive through-via 200. The second side 20 b of the through-via interposer 20 and the second end

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>surfaces 200 b of the conductive through-vias 200 are flush with the second surface 22 b of the encapsulant layer 22.” Hu ’659, [6:56-7:10].</p> <p>To the extent Plaintiff contends that Hu ’659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Hu ’659 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Accordingly, the present invention provides a packaging substrate having an embedded through-via interposer, comprising: an encapsulant layer having opposite first and second surfaces; a through-via interposer embedded in the encapsulant layer and having opposite first and second sides and a plurality of conductive through-vias in communication with the first and second sides, wherein each of the conductive through-vias has a first end surface on the first side of the through-via interposer and a second end surface on the second side of the through-via interposer, and the second side of the through-via interposer is flush with the second end surfaces of the conductive through-vias and the second surface of the encapsulant layer; a redistribution layer embedded in the encapsulant layer and formed on the first side of the through-via interposer and the first end surfaces of the conductive through-vias so as to electrically connect with the first end surfaces of the conductive through-vias, wherein the outermost layer of the redistribution layer has electrode pads; and a built-up structure formed on the second surface of the encapsulant layer, the second side of the through-via interposer and the second end surfaces of the conductive through-vias, and having at least a dielectric</p>

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>layer, a circuit layer embedded in the dielectric layer and a plurality of conductive vias formed in the dielectric layer for electrically connecting with the circuit layer, wherein portions of the conductive vias electrically connect with the second end surfaces of the conductive through-vias, respectively.” Hu ’659, [1:64-2:23].</p> <p>“The present invention further provides a method of fabricating a packaging substrate having an embedded through-via interposer, comprising: providing a through-via interposer having opposite first and second sides and a plurality of conductive through-vias in communication with the first and second sides, wherein each of the conductive through-vias has a first end surface on the first side of the through-via interposer and a second end surface on the second side of the through-via interposer, and the second end surfaces of the conductive through-vias are flush with the second side of the through-via interposer; forming a redistribution layer on the first side of the through-via interposer and the first end surfaces of the conductive through-vias such that the redistribution layer electrically connects with the first end surfaces of the conductive through-vias, wherein the outermost layer of the redistribution layer has electrode pads; forming an encapsulant layer to encapsulate and embed the through-via interposer, wherein the encapsulant layer has opposite first and second surfaces, and the second side of the through-via interposer and the second end surfaces of the conductive through-vias are flush with the second surface of the encapsulant layer, and the encapsulant layer covers the redistribution layer and the electrode pads; and forming a built-up structure on the second surface of the encapsulant layer, the second side of the through-via interposer and the second end surfaces of the conductive through-vias, wherein the built-up structure has at least a dielectric layer, a circuit layer embedded in the dielectric layer and a plurality of conductive vias formed in the dielectric layer for electrically connecting with the circuit layer, wherein portions of the conductive vias electrically connect with the second end surfaces of the conductive through-vias, respectively.” Hu ’659, [2:52-3:15].</p>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>“The present invention further provides another method of fabricating a packaging substrate having an embedded through-via interposer, comprising: providing a through-via interposer having opposite first and second sides and a plurality of conductive through-vias in communication with the first and second sides, wherein each of the conductive through-vias has a first end surface on the first side of the through-via interposer and a second end surface on the second side of the through-via interposer, and the second end surfaces of the conductive through-vias protrude above the second side of the through-via interposer to serve as conductive bumps; forming a redistribution layer on the first side of the through-via interposer and the first end surfaces of the conductive through-vias such that the redistribution layer electrically connects with the first end surfaces of the conductive through-vias, wherein the outermost layer of the redistribution layer has electrode pads; forming an encapsulant layer to encapsulate and embed the through-via interposer, wherein the encapsulant layer has opposite first and second surfaces, the second side of the through-via interposer is exposed from the second surface of the encapsulant layer, the conductive bumps protrude above the second surface of the encapsulant layer, and the encapsulant layer covers the redistribution layer and the electrode pads; and forming a built-up structure on the second surface of the encapsulant layer, the second side of the through-via interposer and the conductive bumps, wherein the built-up structure has at least a dielectric layer, a circuit layer formed on the dielectric layer and a plurality of conductive vias formed in the dielectric layer for electrically connecting with the circuit layer, wherein portions of the conductive vias electrically connect with the conductive bumps, respectively.” Hu '659, [3:17-3:48].</p> <p>“Referring to FIG. 2I, a multi-layer circuit structure may be formed according to practical needs. In an embodiment, the built-up structure 23 has at least a dielectric layer 230, a circuit layer 231 embedded in the dielectric layer 230, and a plurality of conductive vias 232 formed in the dielectric layer 230 and electrically connected with the circuit layer 231. Portions of</p>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>the conductive vias 232' electrically connect with the second end surfaces 200 b of the conductive through-vias 200." Hu '659, [6:18-6:26].</p> <p>"The present invention further provides a packaging substrate 2, 2', 2" having an embedded through-via interposer 20. The packaging substrate 2, 2', 2" comprises an encapsulant layer 22 having a first surface 22 a, 22 a', 22 a" and an opposite second surface 22 b; a through-via interposer 20 embedded in the encapsulant layer 22, a redistribution layer 21 embedded in the encapsulant layer 22 and formed on the through-via interposer 20, a built-up structure 23 formed on the second surface 22 b of the encapsulant layer 22, and an insulating protective layer 24 formed on the built-up structure 23. The through-via interposer 20 has opposite first surface 20 a and second side 20 b, and a plurality of conductive through-vias 200 in communication with the first side 20 a and the second side 20 b. Each of the conductive through-vias 200 has a first end surface 200 a on the first side 20 a of the through-via interposer 20, and a second end surface 200 b on the second side 20 b of the through-via interposer 20, and an insulating layer 201 is formed on the sidewall of the conductive through-via 200. The second side 20 b of the through-via interposer 20 and the second end surfaces 200 b of the conductive through-vias 200 are flush with the second surface 22 b of the encapsulant layer 22." Hu '659, [6:56-7:10].</p> <p>"The through-via interposer 20 has opposite first surface 20 a and second side 20 b, and a plurality of conductive through-vias 200 in communication with the first side 20 a and the second side 20 b. Each of the conductive through-vias 200 has a first end surface 200 a on the first side 20 a of the through-via interposer 20, and a second end surface 200 b on the second side 20 b of the through-via interposer 20, and an insulating layer 201 is formed on the sidewall of the conductive through-via 200." Hu '659, [6:66-7:7].</p>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>“The through-via interposer 30 has opposite first side 30 a and second side 30 b, and a plurality of conductive through-vias 300 in communication with the first side 30 a and the second side 30 b. Each of the conductive through-vias 300 has a first end surface 300 a on the first side 30 a of the through-via interposer 30 and a second end surface 300 b on the second side 30 b of the through-via interposer 30, and an insulating layer 201 is formed on the sidewall of the conductive through-via 300.” Hu '659, [9:31-9:40].</p> <p>“A plurality of through-vias 200 ' are formed at the first side 20 a of the interposer 20 '. In an embodiment, the interposer 20 ' is made of silicon. Referring to FIG. 2B, an insulating layer 201 is formed on sidewalls and bottom portions of the through-vias 200 ', and a copper material is applied to fill the through-vias 200 ' so as to form a plurality of conductive through-vias 200. Each of the conductive through-vias 200 has a first end surface 200 a and a second end surface 200 b corresponding to the first side 20 a and the second side 20 b ' of the interposer 20 ', respectively.” Hu '659, [10:57-11:3].</p>
--	---



FIG. 2A

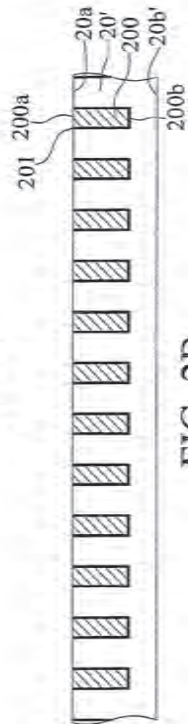


FIG. 2B

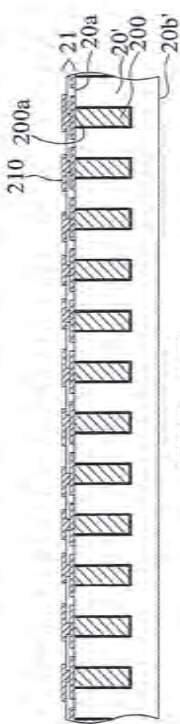


FIG. 2C

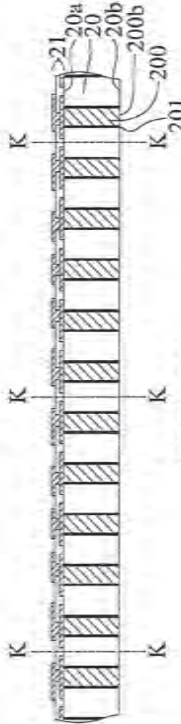


FIG. 2D

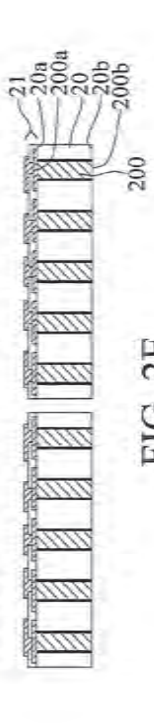


FIG. 2E

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Hu '659 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2C, a redistribution layer (RDL) 21 is formed on the first side 20 a of the interposer 20 ' and the first end surfaces 200 a of the conductive through-vias 200 such that the redistribution layer 21 electrically connects with the first end surfaces 200 a of the conductive through-vias 200. The outermost layer of the redistribution layer 21 has a plurality of electrode pads 210.” Hu '659, [5:4-5:10].</p>



FIG. 2A

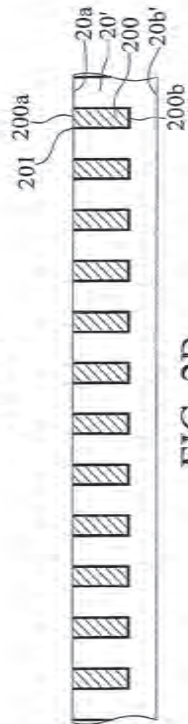


FIG. 2B

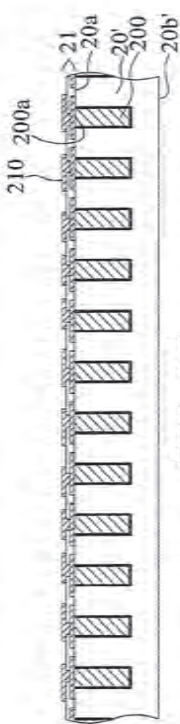


FIG. 2C

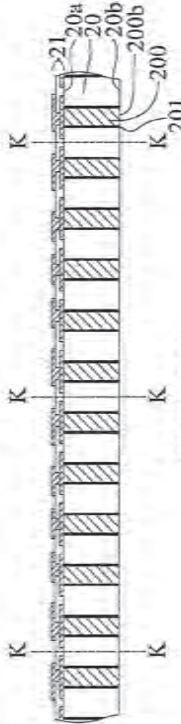


FIG. 2D

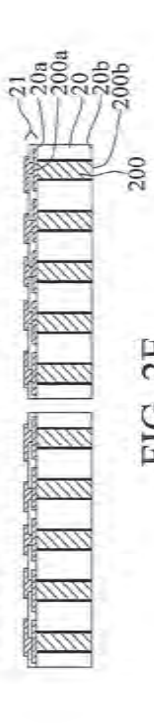


FIG. 2E

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

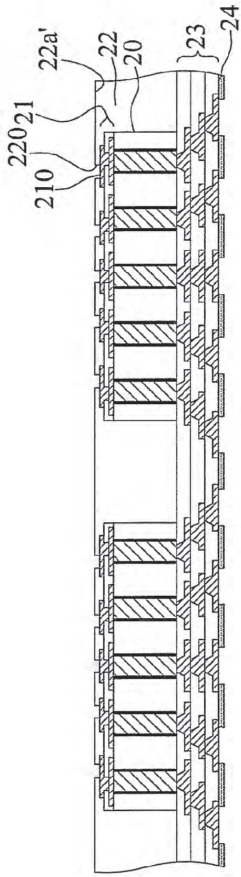
	<p>Hu '659, FIGS. 2A–2E.</p> <p>“Referring to FIG. 2H, a circuit layer 231 and a plurality of conductive vias 232 ' are formed in the circuit intaglios 230 a by an electroplating technique such that the circuit layer 231 is embedded in the dielectric layer 230 and the conductive vias 232 ' electrically connect with the second end surfaces 200 b of the conductive through-vias 200. In an embodiment, a copper material is applied on the dielectric layer 230 and in the circuit intaglios 230 a to serve as a conductive layer (not shown), and a metal material is applied on the dielectric layer 230 and in the circuit intaglios 230 a by an electroplating technique, thereby forming the circuit layer 231 and the conductive vias 232 '.” Hu '659, [5:64-6:8].</p> <p>“Referring to FIG. 2I, a multi-layer circuit structure may be formed according to practical needs. In an embodiment, the built-up structure 23 has at least a dielectric layer 230, a circuit layer 231 embedded in the dielectric layer 230, and a plurality of conductive vias 232 formed in the dielectric layer 230 and electrically connected with the circuit layer 231. Portions of the conductive vias 232 ' electrically connect with the second end surfaces 200 b of the conductive through-vias 200. Further, an insulating protective layer 24 is formed on the built-up structure 23, and a plurality of openings 240 are formed in the insulating protective layer 24 such that portions of the circuit layer 231 are exposed from the openings 240 to serve as conductive pads 233.” Hu '659, [6:18-6:31].</p> <p>“Referring to FIG. 2I, a multi-layer circuit structure may be formed according to practical needs. In an embodiment, the built-up structure 23 has at least a dielectric layer 230, a circuit layer 231 embedded in the dielectric layer 230, and a plurality of conductive vias 232 formed in the dielectric layer 230 and electrically connected with the circuit layer 231. Portions of the conductive vias 232' electrically connect with the second end surfaces 200 b of the conductive through-vias 200.” Hu '659, [6:18-6:26].</p>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>“Before or after the singulation process, a plurality of solder balls 25 can be mounted on the conductive pads 233 for other electronic devices such as printed circuit boards or semiconductor packages to be mounted thereon.” Hu ’659, [6:48-6:51].</p> <p>“The present invention further provides a packaging substrate 2, 2’, 2” having an embedded through-via interposer 20. The packaging substrate 2, 2’, 2” comprises an encapsulant layer 22 having a first surface 22 a, 22 a’, 22 a” and an opposite second surface 22 b; a through-via interposer 20 embedded in the encapsulant layer 22, a redistribution layer 21 embedded in the encapsulant layer 22 and formed on the through-via interposer 20, a built-up structure 23 formed on the second surface 22 b of the encapsulant layer 22, and an insulating protective layer 24 formed on the built-up structure 23. The through-via interposer 20 has opposite first surface 20 a and second side 20 b, and a plurality of conductive through-vias 200 in communication with the first side 20 a and the second side 20 b. Each of the conductive through-vias 200 has a first end surface 200 a on the first side 20 a of the through-via interposer 20, and a second end surface 200 b on the second side 20 b of the through-via interposer 20, and an insulating layer 201 is formed on the sidewall of the conductive through-via 200. The second side 20 b of the through-via interposer 20 and the second end surfaces 200 b of the conductive through-vias 200 are flush with the second surface 22 b of the encapsulant layer 22.” Hu ’659, [6:56-7:10].</p> <p>“The redistribution layer 21 is disposed on the first side 20 a of the through-via interposer 20 and the first end surfaces 200 a of the conductive through-vias 200 and electrically connects with the first end surfaces 200 a of the conductive through-vias 200. The outermost layer of the redistribution layer 21 has a plurality of electrode pads 210.” Hu ’659, [7:11-7:16].</p>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Hu '659 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2B, an insulating layer 201 is formed on sidewalls and bottom portions of the through-vias 200 ', and a copper material is applied to fill the through-vias 200 ' so as to form a plurality of conductive through-vias 200. Each of the conductive through-vias 200 has a first end surface 200 a and a second end surface 200 b corresponding to the first side 20 a and the second side 20 b ' of the interposer 20 ', respectively.” Hu '659, [4:52-4:58].</p> <p>“Referring to FIG. 2D, the first side 20 a of the interposer 20 ' and the redistribution layer 21 are attached to a carrier (not shown), and the second side 20 b of the interposer 20 ' is polished, such that the second end surfaces 200 b of the conductive through-vias 200 are exposed from the second side 20 b of the interposer 20 '.” Hu '659, [5:11-5:16].</p> <p>“Referring to FIG. 2I, a multi-layer circuit structure may be formed according to practical needs. In an embodiment, the built-up structure 23 has at least a dielectric layer 230, a circuit layer 231 embedded in the dielectric layer 230, and a plurality of conductive vias 232 formed in the dielectric layer 230 and electrically connected with the circuit layer 231. Portions of the conductive vias 232' electrically connect with the second end surfaces 200 b of the conductive through-vias 200.” Hu '659, [6:18-6:26].</p>



Hu '659, FIG. 2I'.

“The present invention further provides a packaging substrate 2, 2', 2'' having an embedded through-via interposer 20. The packaging substrate 2, 2', 2'' comprises an encapsulant layer 22 having a first surface 22 a, 22 a', 22 a'' and an opposite second surface 22 b; a through-via interposer 20 embedded in the encapsulant layer 22, a redistribution layer 21 embedded in the encapsulant layer 22 and formed on the through-via interposer 20, a built-up structure 23 formed on the second surface 22 b of the encapsulant layer 22, and an insulating protective layer 24 formed on the built-up structure 23. The through-via interposer 20 has opposite first surface 20 a and second side 20 b, and a plurality of conductive through-vias 200 in communication with the first side 20 a and the second side 20 b. Each of the conductive through-vias 200 has a first end surface 200 a on the first side 20 a of the through-via interposer 20, and a second end surface 200 b on the second side 20 b of the through-via interposer 20, and an insulating layer 201 is formed on the sidewall of the conductive through-via 200. The second side 20 b of the through-via interposer 20 and the second end

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>surfaces 200 b of the conductive through-vias 200 are flush with the second surface 22 b of the encapsulant layer 22.” Hu ’659, [6:56-7:10].</p> <p>“Referring to FIG. 3C, the structure is singulated along imaginary scribing lines K of FIG. 3B to obtain a plurality of through-via interposers 30. Then, an encapsulate layer 22 having opposite first side 22 a and second surface 22 b is formed to encapsulate and embed the through-via interposers 30. The second sides 30 b of the through-via interposers 30 are exposed from the second surface 22 b of the encapsulant layer 22, and the conductive bumps 301 protrude from the second surface 22 b of the encapsulant layer 22.” Hu ’659, [8:5-8:15].</p> <p>“According to the present embodiment, the second end surfaces 300 b of the conductive through-vias 300 protrude above the second sides 30 b of the through-via interposers 30 to serve as conductive bumps 301. When the circuit intaglios 230 a are formed in the built-up structure 23 via a laser technique, high temperature and pressure generated due the application of the laser technique can be absorbed by the conductive bumps 301 made of a hard material, thereby avoiding damage of the through-via interposers 30 made of a brittle material.” Hu ’659, [8:48-8:56].</p> <p>“Each of the conductive through-vias 300 has a first end surface 300 a on the first side 30 a of the through-via interposer 30 and a second end surface 300 b on the second side 30 b of the through-via interposer 30, and an insulating layer 201 is formed on the sidewall of the conductive through-via 300. The second side 30 b of the through-via interposer 30 is exposed from the second surface 22 b of the encapsulant layer 22. The second end surfaces 300 b of the conductive through-vias 300 protrude above the second side 30 b of the through-via interposer 30 and the second surface 22 b of the encapsulant layer 22 so as to serve as conductive bumps 301.” Hu ’659, [9:35-9:45].</p>
--	---

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Hu '659 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>



FIG. 2A

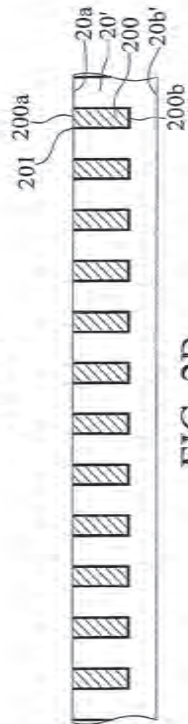


FIG. 2B



FIG. 2C

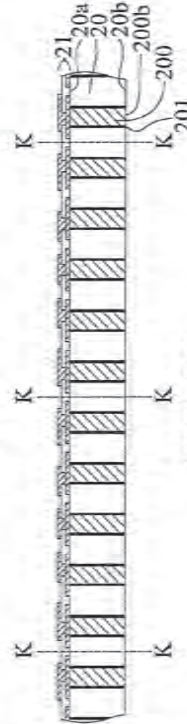


FIG. 2D

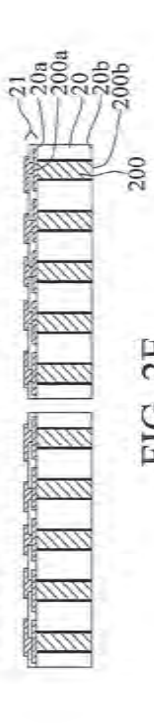


FIG. 2E

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Hu '659 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>



FIG. 2A

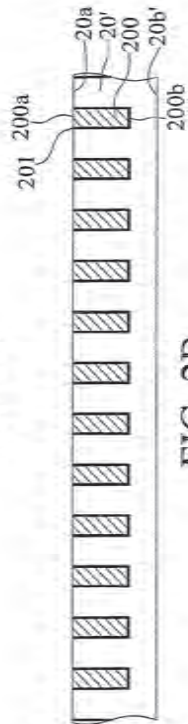


FIG. 2B



FIG. 2C

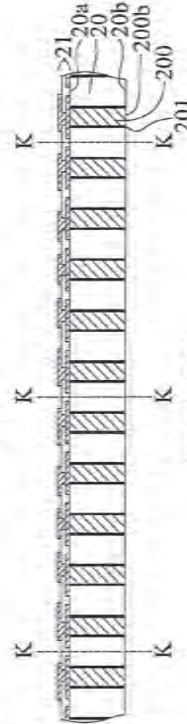


FIG. 2D

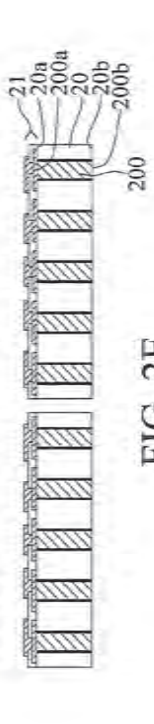


FIG. 2E

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Hu '659 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>



FIG. 2A

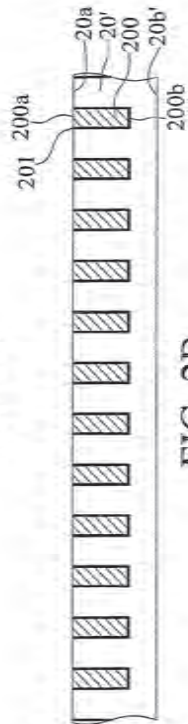


FIG. 2B



FIG. 2C

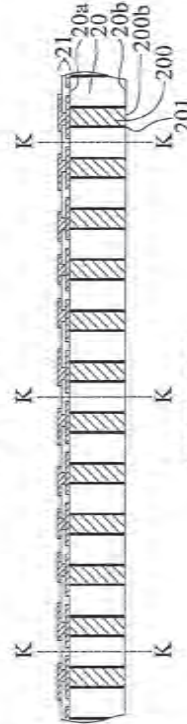


FIG. 2D

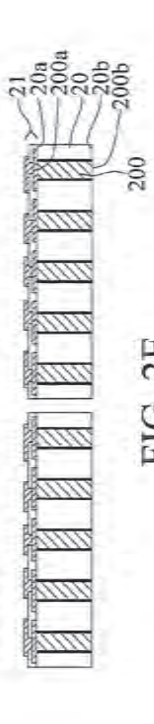


FIG. 2E

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Hu '659 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>



FIG. 2A

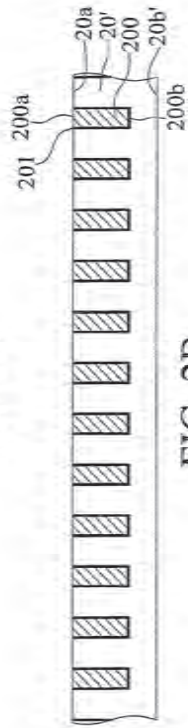


FIG. 2B

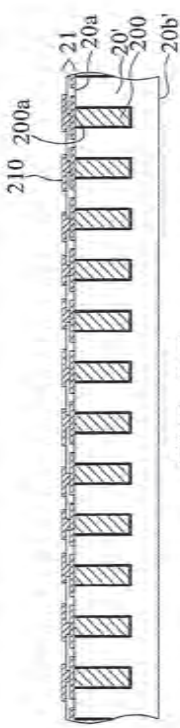


FIG. 2C

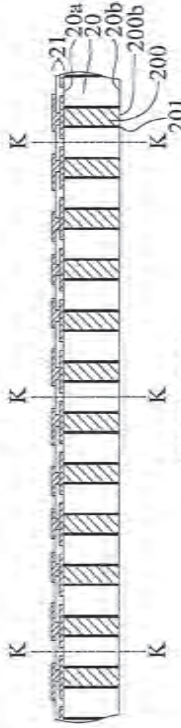


FIG. 2D

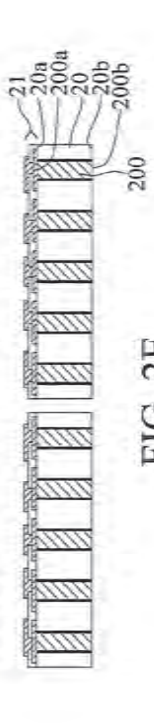


FIG. 2E

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Hu '659 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In other embodiments, the thickness of the encapsulant layer 22 may be decreased from the first surface 22 a thereof so as to expose the electrode pads 210 from the first surface 22 a' 22 a”, thereby allowing a semiconductor chip (not shown) to be mounted thereon. Referring to FIG. 2I', a plurality of openings 220 are formed on the first surface 22 a' of the encapsulant layer 22 for the electrode pads 210 to be exposed from the openings 220. Alternatively, as shown in FIG. 2I", the first surface 22 a" of the encapsulant layer 22 is flush with or lower than the electrode pads 210 so as for the electrode pads 210 to be exposed from the first surface 22 a" of the encapsulant layer 22.” Hu '659, [6:32-6:43].</p>

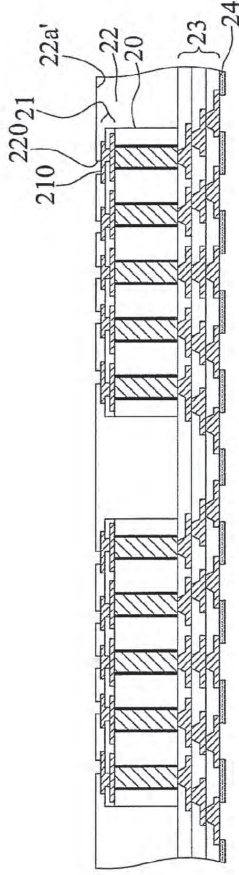


FIG. 2I'

Hu '659, FIG. 2I'.

“According to the present invention, the first end surfaces 200 a of the conductive through-vias 200 electrically connect with the redistribution layer 21 to thereby electrically connect to the electrode pads of a semiconductor chip (not shown) that have smaller pitches, and the other end surfaces 200 b of the conductive through-vias 200 electrically connect with the conductive vias 232' of the built-up structure 23 that have larger pitches, thereby allowing the packaging substrate 2, 2', 2'' to be coupled with the semiconductor chip having high-density circuits. Further, the through-via interposer 20 and the semiconductor chip have CTEs of about 2.6 ppm and are close to each other, cracking of solder bumps between the semiconductor chip and the through-via interposer 20 is prevented, thereby effectively improving the product reliability.” Hu '659, [7:34-7:48].

To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.	<p>Hu '659 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 2J, 2J' and 2J”, the structure of FIG. 2I, 2I' or 2I” is singulated along imaginary scribing lines L of FIG. 2I so as to obtain a plurality of packaging substrates 2, 2' or 2” having an embedded through-via interposer 20.” Hu '659, [6:44-6:47].</p>

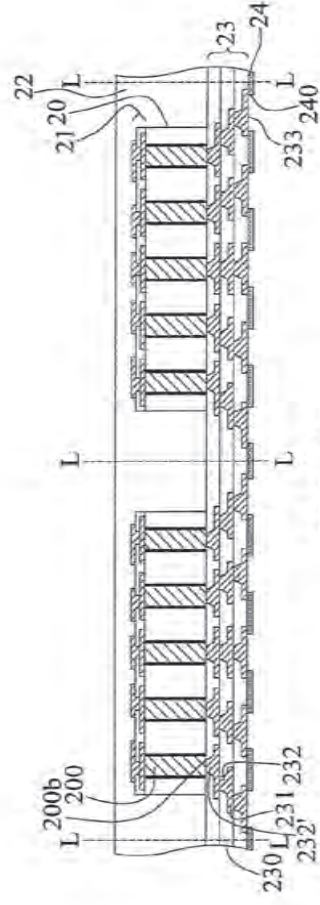


FIG. 2I

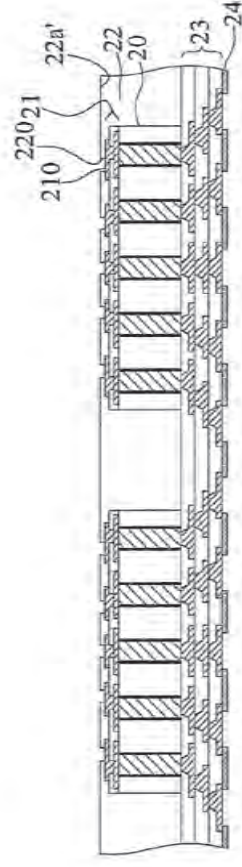


FIG. 2I'

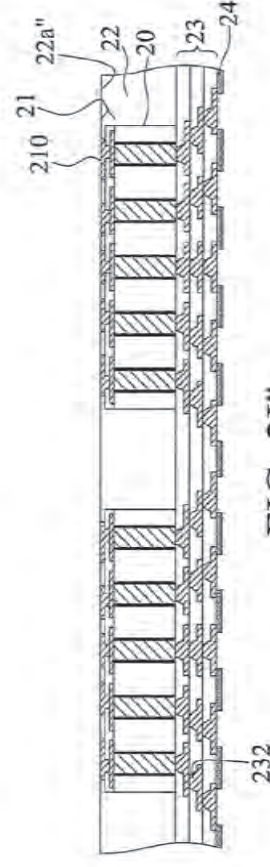


FIG. 2I"

	<p>Hu '659, FIGS. 21-21',</p> <p>“The present invention further provides a packaging substrate 2, 2', 2" having an embedded through-via interposer 20. The packaging substrate 2, 2', 2" comprises an encapsulant layer 22 having a first surface 22 a, 22 a', 22 a" and an opposite second surface 22 b; a through-via interposer 20 embedded in the encapsulant layer 22, a redistribution layer 21 embedded in the encapsulant layer 22 and formed on the through-via interposer 20, a built-up structure 23 formed on the second surface 22 b of the encapsulant layer 22, and an insulating protective layer 24 formed on the built-up structure 23. The through-via interposer 20 has opposite first surface 20 a and second side 20 b, and a plurality of conductive through-vias 200 in communication with the first side 20 a and the second side 20 b. Each of the conductive through-vias 200 has a first end surface 200 a on the first side 20 a of the through-via interposer 20, and a second end surface 200 b on the second side 20 b of the through-via interposer 20, and an insulating layer 201 is formed on the sidewall of the conductive through-via 200. The second side 20 b of the through-via interposer 20 and the second end surfaces 200 b of the conductive through-vias 200 are flush with the second surface 22 b of the encapsulant layer 22.” Hu '659, [6:56-7:10].</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	Hu '659 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate. <i>See, e.g.:</i>

	<div></div> <div><p>FIG. 2A</p></div> <div></div> <div><p>FIG. 2B</p></div> <div></div> <div><p>FIG. 2C</p></div> <div></div> <div><p>FIG. 2D</p></div> <div></div> <div><p>FIG. 2E</p></div>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIG. 2A-2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Hu '659 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p>

	<div></div> <div><p>FIG. 2A</p></div> <div></div> <div><p>FIG. 2B</p></div> <div></div> <div><p>FIG. 2C</p></div> <div></div> <div><p>FIG. 2D</p></div> <div></div> <div><p>FIG. 2E</p></div>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Hu '659 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<div></div> <div><p>FIG. 2A</p></div> <div></div> <div><p>FIG. 2B</p></div> <div></div> <div><p>FIG. 2C</p></div> <div></div> <div><p>FIG. 2D</p></div> <div></div> <div><p>FIG. 2E</p></div>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top metal pads of the spacer connector.</p>	<p>Hu '659 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

	<div></div> <div><p>FIG. 2A</p></div> <div></div> <div><p>FIG. 2B</p></div> <div></div> <div><p>FIG. 2C</p></div> <div></div> <div><p>FIG. 2D</p></div> <div></div> <div><p>FIG. 2E</p></div>
--	--

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the bottom package substrate via the plurality of metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>	<p>Hu '659 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

the corresponding top metal pads of the spacer connector.



FIG. 2A

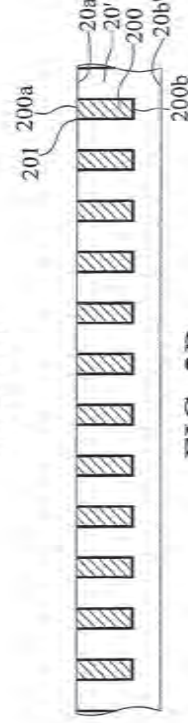


FIG. 2B

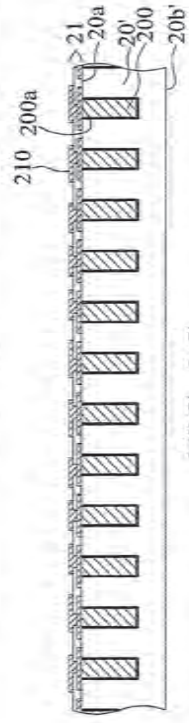


FIG. 2C

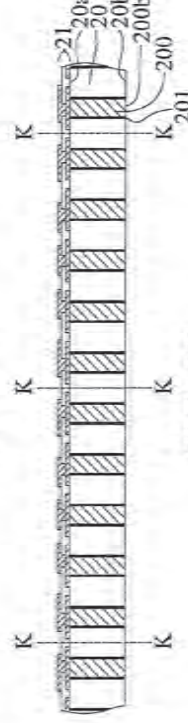


FIG. 2D

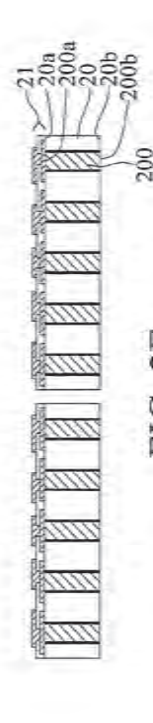


FIG. 2E

Appendix A-14 - Invalidity of U.S. Patent No. 9859202 in view of Hu '659 - U.S. Patent No. 9357659

	<p>Hu '659, FIGS. 2A–2E.</p> <p>To the extent Plaintiff contends that Hu '659 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

U.S. Patent No.8017436 (“Huemoeller”) is titled Thin Substrate Fabrication Method and Structure and lists Ronald Patrick Huemoeller, Sukianto Rusli, Bob Shih-Wei Kuo, Jon Gregory Aday, Lee John Smith, and Robert F. Darveau as inventors. Huemoeller is assigned to Amkor Technology, Inc. Huemoeller anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Huemoeller is a U.S. patent that was filed December 10, 2007. Huemoeller is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Huemoeller, or otherwise rendered obvious by disclosures and teachings of Huemoeller, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Huemoeller does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Huemoeller with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Huemoeller, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Huemoeller “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Huemoeller or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Huemoeller set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Huemoeller discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 28 is a copper pillar flip chip in substrate formation method 2800 in accordance with one embodiment of the present invention. FIG. 29 is a cross-sectional view of a package 2900 during fabrication in accordance with one embodiment. FIGS. 30, 31, 32, 33, 34, 35, 36 are cross-sectional views of package 2900 of FIG. 29 at various stages during fabrication in accordance with various embodiments of the present invention. Referring now to FIGS. 28 and 29 together, in a form circuit pattern on carrier operation 2802, a circuit pattern 2902 is</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>formed on a carrier 2904. Carrier 2904 is similar to top carrier 204 of FIG. 2 and so is not discussed in detail. Further, circuit pattern 2902 is similar to circuit pattern 202 of FIG. 2 and formed in a similar manner and so is not discussed in detail. In accordance with this embodiment, circuit pattern 2902 includes patterned etch stop layer 2906 and patterned conductor layer 2908. Patterned etch stop layer 2906 is formed on carrier 2904. Patterned conductor layer 2908 is formed on patterned etch stop layer 2906. Patterned etch stop layer 2906 and patterned conductor layer 2908 are similar to patterned etch stop layer 206 and patterned conductor layer 208 of FIG. 2 and formed in a similar manner, respectively, and so are not discussed in detail.” Huemoeller, [11:39-11:62].</p> <p>“FIG. 37 is a cross-sectional view of a package 2900 A in accordance with another embodiment. Package 2900 A of FIG. 37 is an example of an exposed chip in substrate (CIS) package. Package 2900 A of FIG. 37 is similar to package 2900 of FIG. 36 and only the significant differences between the packages are discussed below. Referring now to FIG. 37, in accordance with this embodiment, package body 3324 partially encapsulates die 836 such that inactive surface 842 of die 836 is exposed. In this manner, heat transfer from die 836 to the ambient environment is maximized. In another example, a heat sink is attached to exposed inactive surface 842 of die 836.” Huemoeller, [14:18-14:29].</p> <p>“FIG. 38 is a cross-sectional view of a package 2900 B in accordance with another embodiment. Package 2900 B of FIG. 38 is an example of a chip in substrate (CIS) plus shielding package. Package 2900 B of FIG. 38 is similar to package 2900 of FIG. 36 and only the significant differences between the packages are discussed below. Referring now to FIG. 38, in accordance with this embodiment, an electrically conductive shielding layer 3832, e.g., copper or other electrically conductive material, is formed on an upper, e.g., first, surface 3324 U of package body 3324. In accordance with this embodiment, shielding layer 3832 extends around sides 2900 S of package 2900 B. Sides 2900 S are defined by coplanar sides</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>3324 S of package body 3324, sides 3010 S of dielectric material 3010, and sides 3526 S of upper and lower buildup dielectric materials 3526, 3526 A. However, in another embodiment, shielding layer 3832 is formed only on upper surface 3324 U of package body 3324.” Huemoeller, [14:30-14:46].</p> <p>“FIG. 39 is a cross-sectional view of a package 2900 C in accordance with another embodiment. Package 2900 C of FIG. 39 is an example of a chip in substrate (CIS) plus soldered top interposer package. Package 2900 C of FIG. 39 is similar to package 2900 of FIG. 36 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 39 together, from form interconnection balls operation 2824 (or directly from fill artifacts with electrically conductive material operation 2822 if form interconnection balls operation 2824 is not performed), flow moves to a form laser-ablated artifacts operation 2826. In form laser-ablated artifacts operation 2826, package body 3324 and dielectric material 3010 are laser-ablated resulting in the formation of laser-ablated artifacts extending through package body 3324 and dielectric material 3010 and to circuit pattern 2902. More particularly, portions of circuit pattern 2902 are exposed through the laser-ablated artifacts. The laser-ablated artifacts are formed using a laser-ablation process in a manner similar to that described above regarding form artifacts in additional dielectric operation 112 of FIG. 1 and so is only briefly repeated here. During this laser-ablation process, a laser beam is directed at package body 3324 and moved. The laser beam laser-ablates at least partially, and in some places through, package body 3324 and dielectric material 3010. Accordingly, the laser-ablated artifacts are formed at least partially, and in some places through, package body 3324. Further, the laser-ablated artifacts are formed through dielectric material 3010 to expose portions of circuit pattern 2902. The laser-ablated artifacts include laser-ablated channels, laser-ablated land openings, and/or laser-ablated via apertures. The laser-ablated via apertures extend through both package body 3324 and dielectric material 3010 to expose portions of circuit pattern 2902. From form laser-ablated</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

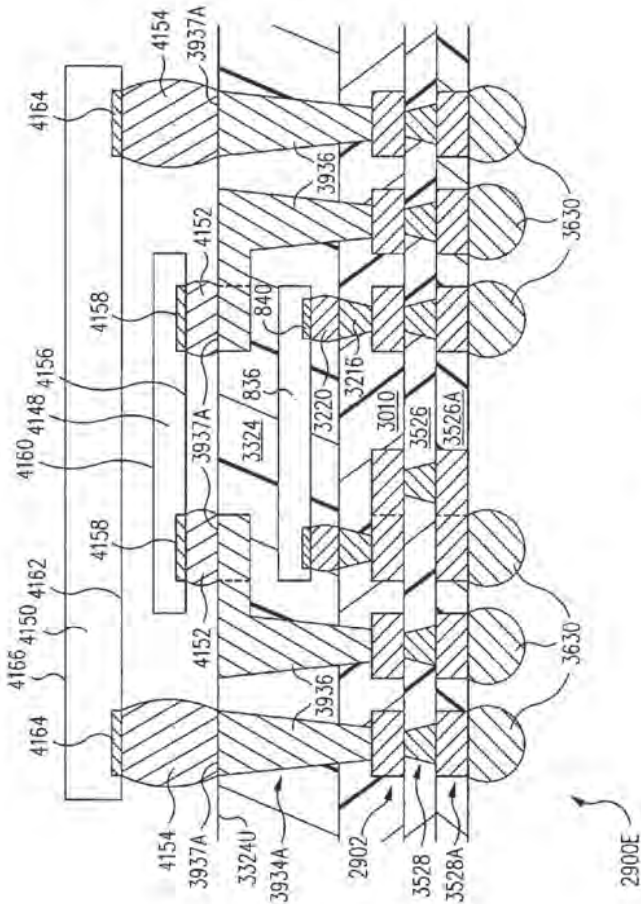
	<p>artifacts 2826, flow moves to a fill laser-ablated artifacts operation 2830. In fill laser-ablated artifacts operation 2830, the laser-ablated artifacts are filled with an electrically conductive filler material, e.g., copper, to form redistribution circuit pattern 3934 as illustrated in FIG. 39. The laser-ablated artifacts are filled with an electrically conductive filler material in a manner similar to that described above regarding fill artifacts with electrically conductive material operation 114 of FIG. 1 and so is only briefly discussed here. As shown in FIG. 39, redistribution circuit pattern 3934 is embedded within package body 3324 and dielectric material 3010. Redistribution circuit pattern 3934 includes electrically conductive traces, lands, and/or vias. In accordance with this embodiment, redistribution circuit pattern 3934 includes electrically conductive vias 3936 electrically connected to circuit pattern 2902. The upper exposed surfaces of vias 3936 form lands 3937 of redistribution circuit pattern 3934. From fill laser-ablated artifacts operation 2830, flow moves to a mount additional structures operation 2832. In mount additional structures operation 2832, additional structures such as an interposer 3938 are mounted to package body 3324 and/or redistribution circuit pattern 3934. Interposer 3938 is electrically connected, e.g., soldered, to redistribution circuit pattern 3934. In one embodiment, interposer 3938 is a structure, e.g., a printed circuit board, to which other structures such as an integrated circuit die are mounted. Interposer 3938 redistributes the pattern of redistribution circuit pattern 3934 to match the footprint of the structure mounted to interposer 3938.” Huemoeller, [14:53-15:51].</p> <p>“FIG. 40 is a cross-sectional view of a package 2900 D in accordance with another embodiment. Package 2900 D of FIG. 40 is an example of a chip in substrate (CIS) plus flip chip (FC) package. In another embodiment, package 2900 D of FIG. 40 is an example of a chip in substrate (CIS) plus full array LOT for system on package. Package 2900 D of FIG. 40 is similar to package 2900 C of FIG. 39 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 40 together, performance of form laser-ablated artifacts operation 2826 and fill laser-ablated artifacts operation 2830</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>forms redistribution circuit pattern 3934 A electrically connected to circuit pattern 2902. In accordance with this embodiment, redistribution circuit pattern 3934 A includes a plurality of lands 3937 A, e.g., distributed as a fully array of lands on upper surface 3324 U of package body 3324. In mount additional structures operation 2832, an electronic structure 4040 is mounted to redistribution circuit pattern 3934 A by electrically conductive bumps 4042. In one embodiment, electronic structure 4040 is die, e.g., an integrated circuit die, having a lower, e.g., first, surface 4044 (e.g., an active surface in this embodiment) with terminals 4046 (e.g., bond pads in this embodiment) formed thereon. Terminals 4046 are physically and electrically flip chip connected to lands 3937 A of redistribution circuit pattern 3934 A by bumps 4042, e.g., flip chip bumps. In another embodiment, electronic structure 4040 is electronic component package, e.g., that includes a die, in a package on package (PoP) configuration. In accordance with this embodiment, terminals 4046 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by bumps 4042, e.g., interconnection balls such as ball grid array solder balls.” Huemoeller, [15:52-16:18].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900 E in accordance with another embodiment. Package 2900 E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900 E of FIG. 41 is similar to package 2900 D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934 A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:18-16:53].</p>
--	--



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

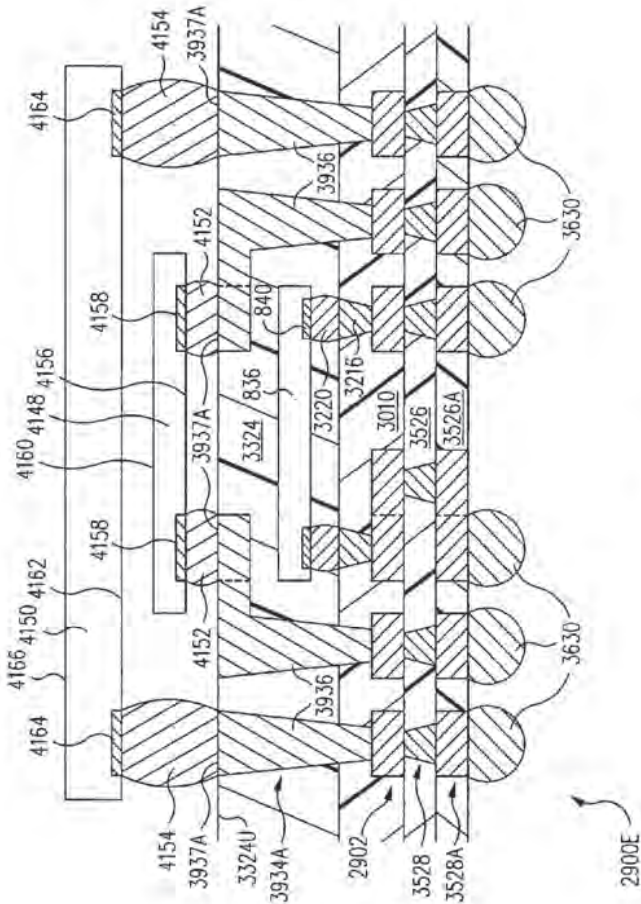
<p>[1.A] a bottom package substrate;</p>	<p>Huemoeller discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“From embed circuit pattern in dielectric operation 106, flow moves to a remove top carrier operation 108. In remove top carrier operation 108, top carrier 204 is removed, e.g., using a selective etch as discussed above, resulting in the structure as illustrated in FIG. 3. From remove top carrier operation 108, flow moves, optionally, to a form blind vias operation 109. In form blind vias operation 109, at least one electrically conductive blind via 314 is formed. Blind vias 314 extend through dielectric material 212 between upper surface 212 U and lower surface 212 L. Blind vias 314 electrically connect circuit pattern 202 to bottom carrier 210 through dielectric material 212.” Huemoeller, [4:1-4:12].</p> <p>“Referring now to FIGS. 1, 4 and 5 together, from fill artifacts with electrically conductive material operation 114, flow moves to a pattern bottom carrier into stiffener operation 116. In pattern bottom carrier into stiffener operation 116, bottom carrier 210 is patterned into a stiffener 502. In one embodiment, bottom carrier 210 is etched to remove a portion of bottom carrier 210, and the remaining portion of bottom carrier 210 forms stiffener 502. Bottom carrier 210 is patterned using a photoimageable dielectric or resist in one embodiment. As stiffener 502 is formed from bottom carrier 210, i.e., is built into package 200, package 200 is formed with stiffener 502 without use of an adhesive to mount stiffener 502.” Huemoeller, [5:49-5:61].</p> <p>“Referring now to FIGS. 15 and 16 together, in a form circuit patterns on top and bottom carriers operation 1502, a top, e.g., first, circuit pattern 1602 is formed on a first, e.g., top,</p>
---	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>carrier 1604 and a bottom, e.g., second, circuit pattern 1602 A is formed on a second, e.g., bottom, carrier 1604 A, sometimes called a removable carrier. Carriers 1604, 1604 A are similar to top carrier 204 and bottom carrier 210 of FIG. 2 and so are not discussed in detail. Bottom carrier 1604 A acts as a stiffener during thin coreless package formation method 1500.” Huemoeller, [8:59-9:1].</p> <p>“Referring now to FIGS. 15, 23 and 24 together, from encapsulate operation 1520 (or directly from wirebond operation 1518 if encapsulate operation 1520 is not performed), flow moves to a remove bottom carrier operation 1522. In remove bottom carrier operation 1522, bottom carrier 1604 A is removed, e.g., using a selective etch process as discussed above. By retaining bottom carrier 1604 A in the operations leading up to remove bottom carrier operation 1522, bottom carrier 1604 A acts a stiffener during the manufacture of package 1600.” Huemoeller, [10:38-10:47].</p> <p>“Referring now to FIGS. 28 and 29 together, in a form circuit pattern on carrier operation 2802, a circuit pattern 2902 is formed on a carrier 2904. Carrier 2904 is similar to top carrier 204 of FIG. 2 and so is not discussed in detail. Further, circuit pattern 2902 is similar to circuit pattern 202 of FIG. 2 and formed in a similar manner and so is not discussed in detail.” Huemoeller, [11:47-11:53].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second,</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	---



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Huemoeller discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring now to FIGS. 15, 16 and 17 together, from form circuit patterns on top and bottom carriers operation 1502, flow moves to an embed circuit patterns in dielectric operation 1504. In embed circuit patterns in dielectric operation 1504, circuit pattern 1602, 1602 A are embedded within a dielectric material 1610 in a manner similar to that discussed above in relation to embed circuit pattern in dielectric operation 106 of FIG. 1 and so is not discussed in detail. More particularly, as shown in FIG. 17, circuit pattern 1602 is embedded into an upper, e.g., first, surface 1610 U of dielectric material 1610. Similarly, circuit pattern 1602 A is embedded into a lower, e.g., second, surface 1610 L of dielectric material 1610. Dielectric material 1610 remains between circuit patterns 1602, 1602 A thereby electrically isolating circuit pattern 1602, 1602 A from each other.” Huemoeller, [9:15-9:29].</p> <p>“Referring now to FIGS. 15 and 20 together, from fill blind via apertures with electrically conductive material operation 1510, flow moves, optionally, to a form resist over bond fingers operation 1512. In form resist over bond fingers operation 1512, photoresist 2016 is selectively formed over bond fingers 2018, sometimes called lands, of top circuit pattern 1602. In one embodiment, the exposed top surface of a blind via 1914 forms a bond fingers 2018. Photoresist 2016 is formed using any one of a number of techniques and the particular</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

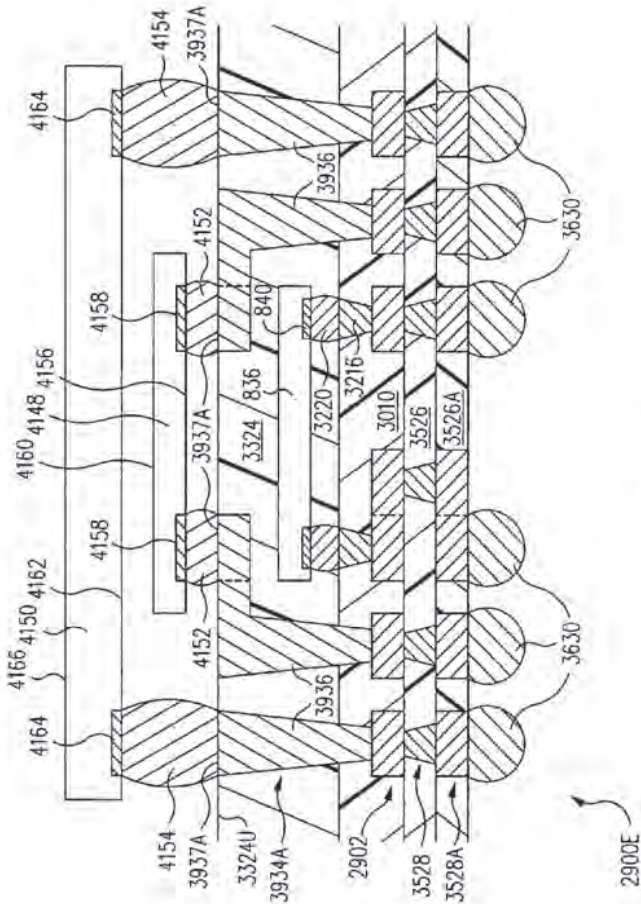
	<p>technique used is not essential to this embodiment. Referring now to FIGS. 15 and 21 together, from form resist over bond fingers operation 1512 (or directly from fill blind via apertures with electrically conductive material operation 1510 if form resist over bond fingers operation 1512 is not performed), flow moves to a die attach operation 1514. In die attach operation 1514, die 836 is die attached to upper surface 1610 U of dielectric material 1610. In the embodiment illustrated in FIG. 21, in addition to being attached to upper surface 1610 U of dielectric material 1610, die 836 is also die attached directly to top circuit pattern 1602 and the exposed top surface of a blind via 1914.” Huemoeller, [9:55-10:8].</p> <p>“Referring now to FIGS. 28 and 35 together, from remove carrier operation 2816, flow moves to a mount additional dielectric operation 2818. In mount additional dielectric operation 2818, an upper, e.g., first, buildup dielectric material 3526 is mounted to dielectric material 3010 and circuit pattern 2902. More particularly, an upper, e.g., first, surface 3526 U of upper buildup dielectric material 3526 is mounted to lower surface 3010 L of dielectric material 3010. Upper buildup dielectric material 3526 further includes a lower, e.g., second, surface 3526 L opposite upper surface 3526 U. From mount additional dielectric operation 2818, flow moves to a form artifacts in additional dielectric operation 2820. In form artifacts in additional dielectric operation 2820, upper buildup dielectric material 3526 is laser-ablated resulting in the formation of laser-ablated artifacts in upper buildup dielectric material 3526.” Huemoeller, [13:6-13:22].</p> <p>“As indicated by the dashed arrow in FIG. 28, operations 2818, 2820, and 2822 can be repeated any one of a number of times to form additional buildup circuit patterns in additional buildup dielectric materials. In accordance with the embodiment illustrated in FIG. 35, operations 2818, 2820, and 2822 are repeated a second time to form a lower, e.g., second, buildup circuit pattern 3528 A in a lower, e.g., second, buildup dielectric material 3526 A.</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>Lower buildup circuit pattern 3528 A redistributes the pattern of upper buildup circuit pattern 3528 to the pattern of lower buildup circuit pattern 3528 A.” Huemoeller, [13:55-13:65].</p> <p>“Referring now to FIGS. 28 and 39 together, from form interconnection balls operation 2824 (or directly from fill artifacts with electrically conductive material operation 2822 if form interconnection balls operation 2824 is not performed), flow moves to a form laser-ablated artifacts operation 2826. In form laser-ablated artifacts operation 2826, package body 3324 and dielectric material 3010 are laser-ablated resulting in the formation of laser-ablated artifacts extending through package body 3324 and dielectric material 3010 and to circuit pattern 2902. More particularly, portions of circuit pattern 2902 are exposed through the laser-ablated artifacts. The laser-ablated artifacts are formed using a laser-ablation process in a manner similar to that described above regarding form artifacts in additional dielectric operation 112 of FIG. 1 and so is only briefly repeated here. During this laser-ablation process, a laser beam is directed at package body 3324 and moved. The laser beam laser-ablates at least partially, and in some places through, package body 3324 and dielectric material 3010. Accordingly, the laser-ablated artifacts are formed at least partially, and in some places through, package body 3324. Further, the laser-ablated artifacts are formed through dielectric material 3010 to expose portions of circuit pattern 2902. The laser-ablated artifacts include laser-ablated channels, laser-ablated land openings, and/or laser-ablated via apertures. The laser-ablated via apertures extend through both package body 3324 and dielectric material 3010 to expose portions of circuit pattern 2902. From form laser-ablated artifacts 2826, flow moves to a fill laser-ablated artifacts operation 2830. In fill laser-ablated artifacts operation 2830, the laser-ablated artifacts are filled with an electrically conductive filler material, e.g., copper, to form redistribution circuit pattern 3934 as illustrated in FIG. 39.” Huemoeller, [14:59-15:26].</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Huemoeller discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--

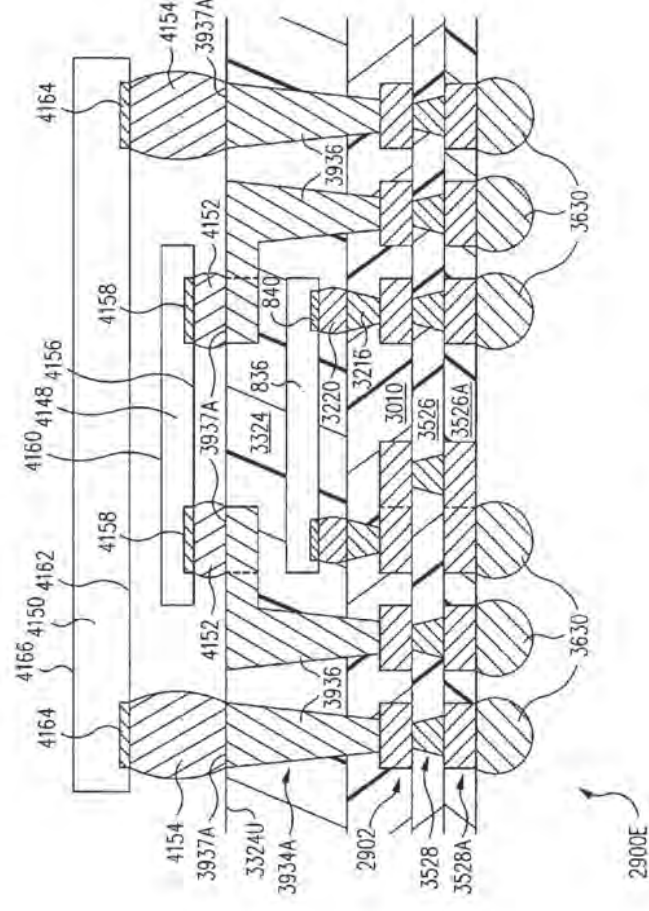


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Huemoeller discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In accordance with one embodiment, a method of forming a package includes forming a circuit pattern on a first carrier and embedding the circuit pattern in a dielectric material on a second carrier. The first carrier is removed and a buildup dielectric material is mounted to the dielectric material and the circuit pattern.” Huemoeller, [1:22-1:27].</p> <p>“Referring now to FIGS. 1, 2 and 3 together, from provide bottom carrier with dielectric operation 104, flow moves to an embed circuit pattern in dielectric operation 106. In embed circuit pattern in dielectric operation 106, circuit pattern 202 is embedded within dielectric layer 212. More particularly, as shown in FIG. 3, circuit pattern 202 is embedded into an upper, e.g., first, surface 212 U of dielectric material 212. A lower, e.g., second, surface 212 L of dielectric material 212 is mounted to bottom carrier 210.” Huemoeller, [3:45-3:53].</p> <p>“In mount additional dielectric operation 110, a buildup dielectric material 416, sometimes called a buildup dielectric layer or a coreless buildup layer, is mounted to dielectric material 212 and circuit pattern 202. Generally, buildup dielectric material 416 is mounted to dielectric material 212 and over circuit pattern 202 and blind vias 314. More particularly, a lower, e.g., first, surface 416 L of buildup dielectric material 416 is mounted to upper surface</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>212 U of dielectric material 212. Buildup dielectric material 416 further includes an upper, e.g., second, surface 416 U opposite lower surface 416 L.” Huemoeller, [4:23-4:35].</p> <p>“Referring now to FIGS. 15, 16 and 17 together, from form circuit patterns on top and bottom carriers operation 1502, flow moves to an embed circuit patterns in dielectric operation 1504. In embed circuit patterns in dielectric operation 1504, circuit pattern 1602, 1602 A are embedded within a dielectric material 1610 in a manner similar to that discussed above in relation to embed circuit pattern in dielectric operation 106 of FIG. 1 and so is not discussed in detail. More particularly, as shown in FIG. 17, circuit pattern 1602 is embedded into an upper, e.g., first, surface 1610 U of dielectric material 1610. Similarly, circuit pattern 1602 A is embedded into a lower, e.g., second, surface 1610 L of dielectric material 1610. Dielectric material 1610 remains between circuit patterns 1602, 1602 A thereby electrically isolating circuit pattern 1602, 1602 A from each other.” Huemoeller, [9:15-9:29].</p> <p>“Referring now to FIGS. 28 and 30 together, from form circuit pattern on carrier operation 2802, flow moves to an attach dielectric operation 2804. In attach dielectric operation 2804, a dielectric material 3010 is attached to circuit pattern 2902 and carrier 2904. More particularly, as shown in FIG. 30, circuit pattern 2902 is embedded into a lower, e.g., first, surface 3010 L of dielectric material 3010. Dielectric material 3010 is attached around circuit pattern 2902 and to carrier 2904.” Huemoeller, [12:4-12:13].</p> <p>“Underfill material 3322 is optional and in one embodiment is not formed. In accordance with this embodiment, package body 3324 fills the space between upper surface 3010U of dielectric material 3010 and active surface 838 of die 836 and around flip chip bumps 3220. Accordingly, although underfill material 3322 is not illustrated except in FIG. 33, in light of this disclosure, those of skill in the art will understand that underfill material 3322 can be formed and would be illustrated in the remaining figures.” Huemoeller, [12:59-12:67].</p>
--	--

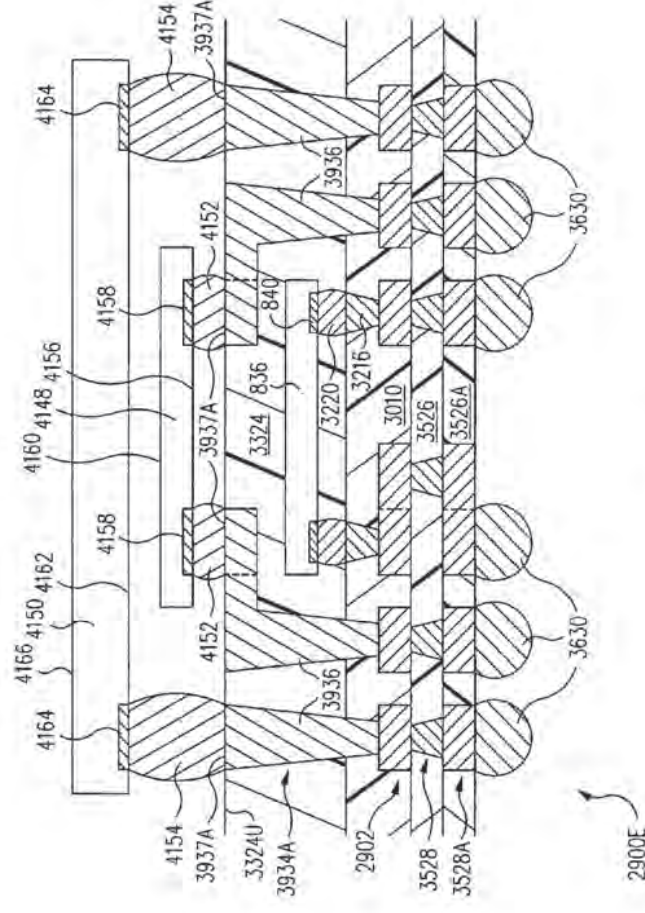


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p> <p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Huemoeller discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“As shown in FIG. 4, buildup circuit pattern 418 is embedded within buildup dielectric material 416. Buildup circuit pattern 418 includes electrically conductive traces, lands, and/or vias. In one embodiment, buildup circuit pattern 418 redistributes the pattern of circuit pattern 202 to the pattern of buildup circuit pattern 418. In one embodiment, a trace extends horizontally and in a direction parallel with upper surface 416 U of buildup dielectric material 416. To illustrate, buildup circuit pattern 418 includes a trace 420. Trace 420 is embedded within upper surface 416 U of buildup dielectric material 416 such that buildup dielectric material 416 remains between trace 420 and lower surface 416 L of buildup dielectric material 416. To further illustrate, buildup circuit pattern 418 includes a land 422, sometimes called a pad. Land 422 is embedded within upper surface 416 U of buildup dielectric material 416 such that buildup dielectric material 416 remains between land 422 and lower surface 416 L of buildup dielectric material 416. To further illustrate, embedded buildup circuit pattern 418 includes vias 424, sometimes called blind vias. Vias 424 extend between upper surface 416 U and lower surface 416 L of buildup dielectric material 416. Vias 424 are electrically connected to circuit pattern 202.” Huemoeller, [5:16-5:39].</p> <p>“In form blind via apertures operation 1508, blind via apertures 1812 are formed. Blind via apertures 1812 extend through dielectric material 1610 between upper surface 1610 U and lower surface 1610 L. In one embodiment, blind via apertures 1812 are formed in dielectric</p>

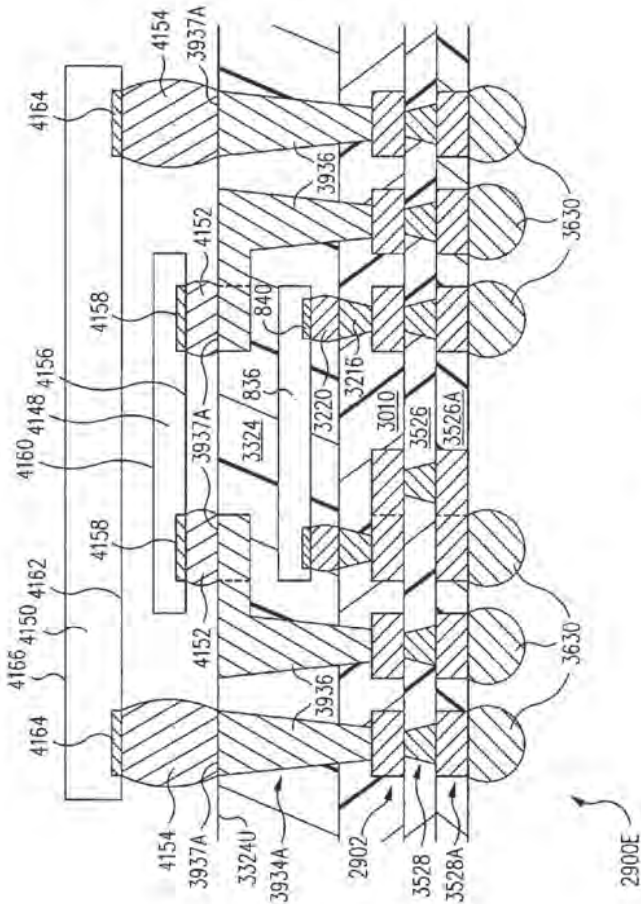
Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>material 1610 using laser-ablation and thus have a taper shape as illustrated. Generally, blind via apertures 1812 are formed between top circuit pattern 1602 and bottom circuit pattern 1602 A. Referring now to FIGS. 15 and 19 together, from form blind via apertures operation 1508, flow moves to a fill blind via apertures with electrically conductive material operation 1510. In fill blind via apertures with electrically conductive material operation 1510, blind via apertures 1812 are filled, e.g., with plated copper or other conductive material, to form electrically conductive blind vias 1914. Blind vias 1914 extend between and electrically connect circuit patterns 1602, 1602 A with one another through dielectric material 1610.” Huemoeller, [9:37-9:54].</p> <p>“In form bump pad openings operation 2806, bump pad openings 3112 are formed within dielectric layer 3010 to expose lands 3114 of circuit pattern 2902. Bump pad openings 3112 extend from upper surface 3010 U of dielectric material 3010, through dielectric material 3010 to expose lands 3114. In one embodiment, bump pad openings 3112 are formed using a laser-ablation process and thus have a taper shaped as illustrated in FIG. 31. Referring now to FIGS. 28, 31 and 32 together, from form bump pad openings operation 2806, flow moves to a fill bump pad openings with electrically conductive material operation 2810. In fill bump pad openings with electrically conductive material operation 2810, bump pad openings 3112 are filled with electrically conductive material, e.g., tin plating, to form electrically conductive vias 3216 within bump pad openings 3112. Vias 3216 extend from upper surface 3010 U of dielectric material 3010, through dielectric material 3010, to contact and be electrically connected to lands 3114.” Huemoeller, [12:22-12:39].</p> <p>“As shown in FIG. 35, upper buildup circuit pattern 3528 is embedded within upper buildup dielectric material 3526. Upper buildup circuit pattern 3528 includes electrically conductive traces, lands, and/or vias. In one embodiment, upper buildup circuit pattern 3528 redistributes the pattern of circuit pattern 2902 to the pattern of upper buildup circuit pattern 3528. As</p>
--	--

	<p>indicated by the dashed arrow in FIG. 28, operations 2818, 2820, and 2822 can be repeated any one of a number of times to form additional buildup circuit patterns in additional buildup dielectric materials. In accordance with the embodiment illustrated in FIG. 35, operations 2818, 2820, and 2822 are repeated a second time to form a lower, e.g., second, buildup circuit pattern 3528 A in a lower, e.g., second, buildup dielectric material 3526 A.” Huemoeller, [13:48-13:62].</p> <p>“The laser-ablated via apertures extend through both package body 3324 and dielectric material 3010 to expose portions of circuit pattern 2902. From form laser-ablated artifacts 2826, flow moves to a fill laser-ablated artifacts operation 2830. In fill laser-ablated artifacts operation 2830, the laser-ablated artifacts are filled with an electrically conductive filler material, e.g., copper, to form redistribution circuit pattern 3934 as illustrated in FIG. 39. The laser-ablated artifacts are filled with an electrically conductive filler material in a manner similar to that described above regarding fill artifacts with electrically conductive material operation 114 of FIG. 1 and so is only briefly discussed here. As shown in FIG. 39, redistribution circuit pattern 3934 is embedded within package body 3324 and dielectric material 3010. Redistribution circuit pattern 3934 includes electrically conductive traces, lands, and/or vias. In accordance with this embodiment, redistribution circuit pattern 3934 includes electrically conductive vias 3936 electrically connected to circuit pattern 2902.” Huemoeller, [15:18-15:38].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	---



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Huemoeller discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“In one embodiment, circuit pattern 202 is a multilayer conductive structure. For example, as indicated by the horizontal dashed line in FIG. 2, circuit pattern 202 includes a patterned etch stop layer 206 formed directly on top carrier 204 and a patterned conductor layer 208 formed directly on patterned etch stop layer 206. The etch stop metal, e.g., nickel, tin, gold, or palladium, of patterned etch stop layer 206 is selectively etchable compared to the conductor metal, e.g., copper, silver, or solder, of patterned conductor layer 208.” Huemoeller, [2:59-2:67].</p> <p>“Further, circuit patterns 1602, 1602 A are similar to circuit pattern 202 and formed in a similar manner and so are not discussed in detail. In accordance with this embodiment, circuit patterns 1602, 1602 A include patterned etch stop layers 1606, 1606 A and patterned conductor layers 1608, 1608 A, respectively. Patterned etch stop layers 1606, 1606 A are formed on carriers 1604, 1604 A, respectively.” Huemoeller, [9:1-9:8].</p> <p>“In accordance with this embodiment, circuit pattern 2902 includes patterned etch stop layer 2906 and patterned conductor layer 2908. Patterned etch stop layer 2906 is formed on carrier</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>2904. Patterned conductor layer 2908 is formed on patterned etch stop layer 2906.” Huemoeller, [11:54-11:58].</p> <p>“In accordance with this embodiment, redistribution circuit pattern 3934 includes electrically conductive vias 3936 electrically connected to circuit pattern 2902. The upper exposed surfaces of vias 3936 form lands 3937 of redistribution circuit pattern 3934.” Huemoeller, [15:35-15:39].</p> <p>“In accordance with this embodiment, redistribution circuit pattern 3934 A includes a plurality of lands 3937 A, e.g., distributed as a fully array of lands on upper surface 3324 U of package body 3324.” Huemoeller, [15:63-15:67].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--

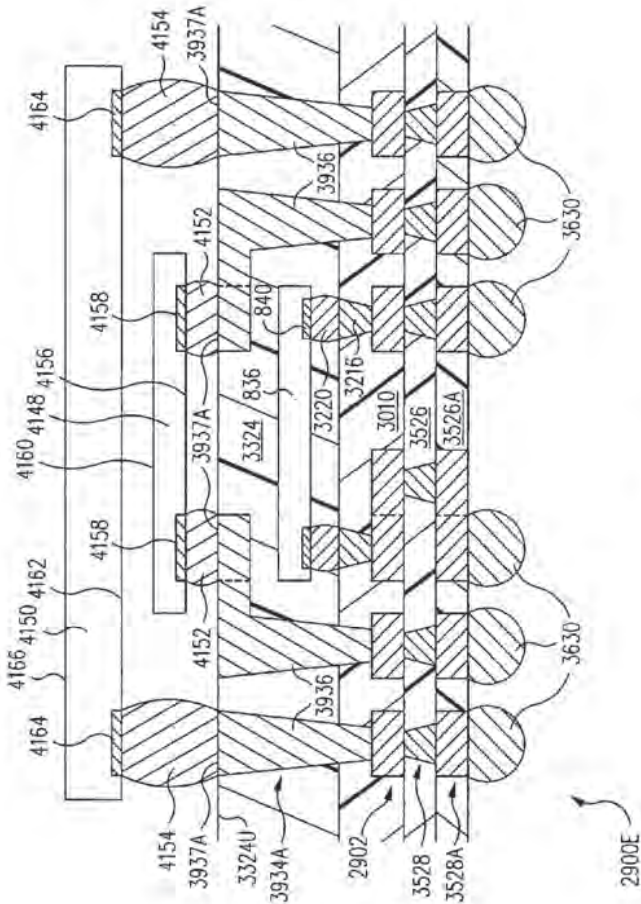


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

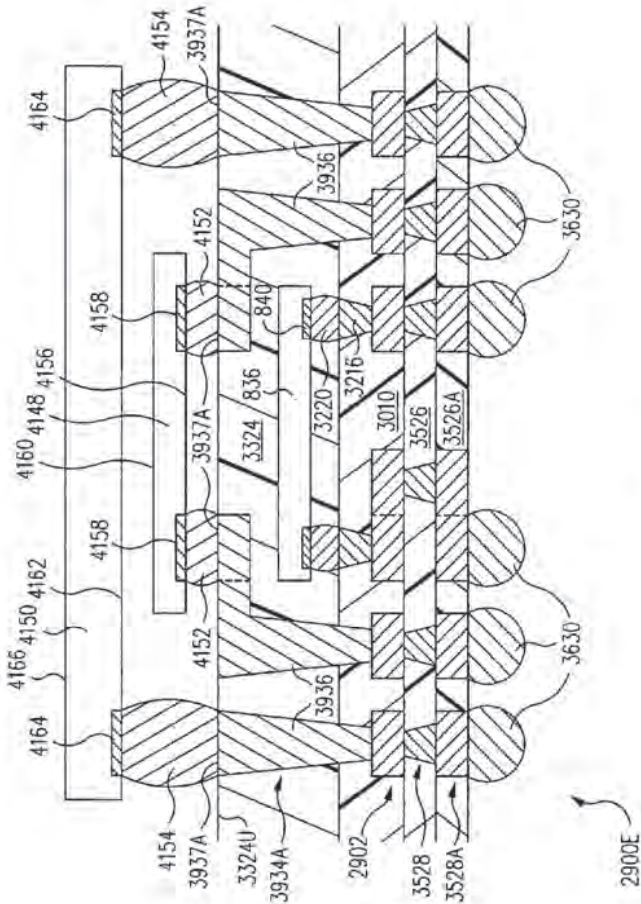
	<p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p> <p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Huemoeller discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Huemoeller discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In form blind vias operation 109, at least one electrically conductive blind via 314 is formed. Blind vias 314 extend through dielectric material 212 between upper surface 212 U and lower surface 212 L. Blind vias 314 electrically connect circuit pattern 202 to bottom carrier 210 through dielectric material 212. In one embodiment, to form blind vias 314, via apertures, sometimes called blind via apertures, are formed in dielectric material 212 using laser-ablation. Generally, the via apertures are formed between circuit pattern 202 and bottom carrier 210. The via apertures are filled, e.g., with copper or other conductive material, to form blind vias 314.” Huemoeller, [4:7-4:18].</p> <p>“In fill bump pad openings with electrically conductive material operation 2810, bump pad openings 3112 are filled with electrically conductive material, e.g., tin plating, to form electrically conductive vias 3216 within bump pad openings 3112. Vias 3216 extend from upper surface 3010 U of dielectric material 3010, through dielectric material 3010, to contact and be electrically connected to lands 3114. Vias 3216 include upper exposed surfaces that define lands 3218, which are coplanar with upper surface 3010 U of dielectric material 3010. From fill bump pad openings with electrically conductive material operation 2810, flow</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>moves to a flip chip die attach operation 2812. In flip chip die attach operation 2812, die 836 is flip chip attached to vias 3216. More particularly, bond pads 840 of die 836 are physically and electrically connected to lands 3218 of vias 3216 by flip chip bumps 3220. Flip chip bumps 3220 are copper pillars or gold stud bumps in various embodiments although solder can be used.” Huemoeller, [12:33-12:50].</p> <p>“From mount additional dielectric operation 2818, flow moves to a form artifacts in additional dielectric operation 2820. In form artifacts in additional dielectric operation 2820, upper buildup dielectric material 3526 is laser-ablated resulting in the formation of laser-ablated artifacts in upper buildup dielectric material 3526. The laser-ablated artifacts are formed using a laser-ablation process in a manner similar to that described above regarding form artifacts in additional dielectric operation 112 of FIG. 1 and so is only briefly repeated here. During this laser-ablation process, a laser beam is directed at upper buildup dielectric material 3526 and moved. The laser beam laser-ablates at least partially, and in some places through, upper buildup dielectric material 3526. Accordingly, the laser-ablated artifacts are formed at least partially, and in some places through, upper buildup dielectric material 3526. The laser-ablated artifacts include laser-ablated channels, laser-ablated land openings, and/or laser-ablated via apertures. From form artifacts in additional dielectric operation 2820, flow moves to a fill artifacts with electrically conductive material operation 2822. In fill artifacts with electrically conductive material operation 2822, the laser-ablated artifacts are filled with an electrically conductive filler material, e.g., copper, to form an upper, e.g., first, buildup circuit pattern 3528 as illustrated in FIG. 35. The laser-ablated artifacts are filled with an electrically conductive filler material in a manner similar to that described above regarding fill artifacts with electrically conductive material operation 114 of FIG. 1 and so is only briefly discussed here. As shown in FIG. 35, upper buildup circuit pattern 3528 is embedded within upper buildup dielectric material 3526. Upper buildup circuit pattern 3528 includes electrically conductive traces, lands, and/or vias. In one embodiment, upper buildup circuit</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>pattern 3528 redistributes the pattern of circuit pattern 2902 to the pattern of upper buildup circuit pattern 3528. As indicated by the dashed arrow in FIG. 28, operations 2818, 2820, and 2822 can be repeated any one of a number of times to form additional buildup circuit patterns in additional buildup dielectric materials. In accordance with the embodiment illustrated in FIG. 35, operations 2818, 2820, and 2822 are repeated a second time to form a lower, e.g., second, buildup circuit pattern 3528 A in a lower, e.g., second, buildup dielectric material 3526 A. Lower buildup circuit pattern 3528 A redistributes the pattern of upper buildup circuit pattern 3528 to the pattern of lower buildup circuit pattern 3528 A.” Huemoeller, [13:17-13:66].</p> <p>“In mount additional structures operation 2832, an electronic structure 4040 is mounted to redistribution circuit pattern 3934 A by electrically conductive bumps 4042. In one embodiment, electronic structure 4040 is die, e.g., an integrated circuit die, having a lower, e.g., first, surface 4044 (e.g., an active surface in this embodiment) with terminals 4046 (e.g., bond pads in this embodiment) formed thereon. Terminals 4046 are physically and electrically flip chip connected to lands 3937 A of redistribution circuit pattern 3934 A by bumps 4042, e.g., flip chip bumps. In another embodiment, electronic structure 4040 is electronic component package, e.g., that includes a die, in a package on package (PoP) configuration. In accordance with this embodiment, terminals 4046 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by bumps 4042, e.g., interconnection balls such as ball grid array solder balls.” Huemoeller, [16:1-16:18].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--

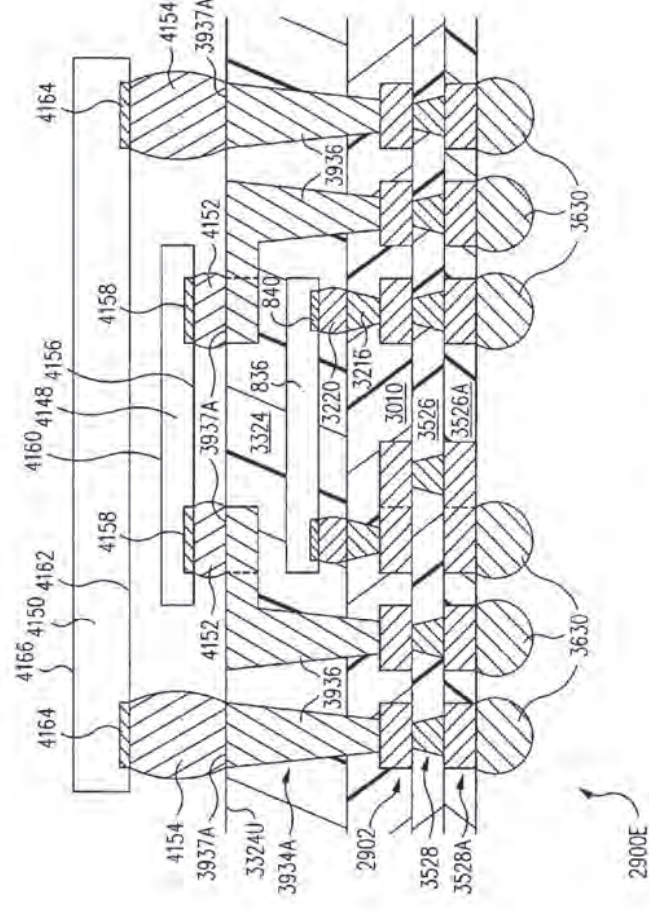


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p> <p>“Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934 A by inner and outer, e.g., first and second, electrically</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

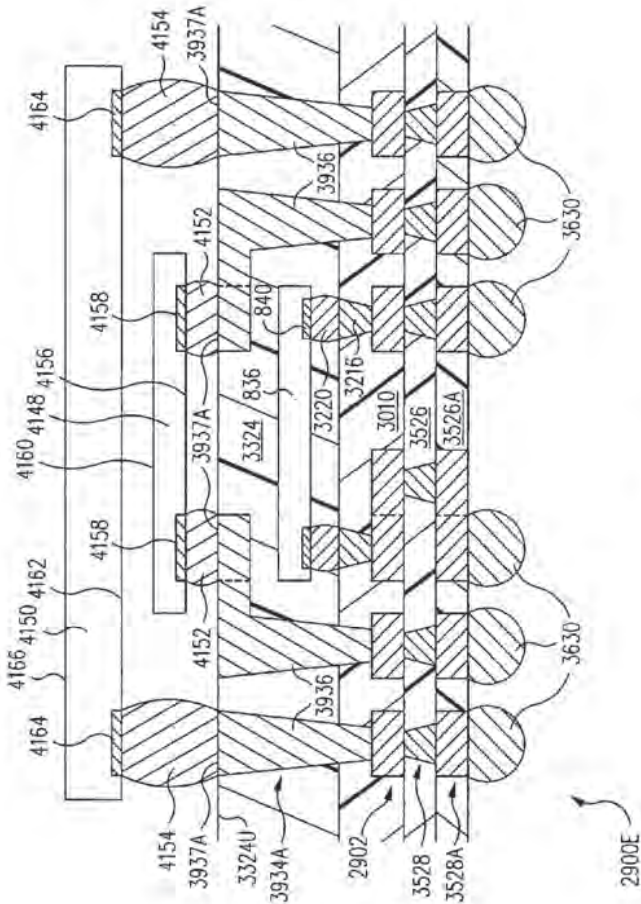
	<p>conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by outer electrically conductive bumps 4154.” Huemoeller, [16:25-16:50].</p> <p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Huemoeller discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“In fill blind via apertures with electrically conductive material operation 1510, blind via apertures 1812 are filled, e.g., with plated copper or other conductive material, to form</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>electrically conductive blind vias 1914. Blind vias 1914 extend between and electrically connect circuit patterns 1602, 1602 A with one another through dielectric material 1610.” Huemoeller, [9:49-9:54].</p> <p>“Referring now to FIGS. 15 and 21 together, from form resist over bond fingers operation 1512 (or directly from fill blind via apertures with electrically conductive material operation 1510 if form resist over bond fingers operation 1512 is not performed), flow moves to a die attach operation 1514. In die attach operation 1514, die 836 is die attached to upper surface 1610 U of dielectric material 1610. In the embodiment illustrated in FIG. 21, in addition to being attached to upper surface 1610 U of dielectric material 1610, die 836 is also die attached directly to top circuit pattern 1602 and the exposed top surface of a blind via 1914.” Huemoeller, [9:65-10:8].</p> <p>“In fill bump pad openings with electrically conductive material operation 2810, bump pad openings 3112 are filled with electrically conductive material, e.g., tin plating, to form electrically conductive vias 3216 within bump pad openings 3112. Vias 3216 extend from upper surface 3010 U of dielectric material 3010, through dielectric material 3010, to contact and be electrically connected to lands 3114. Vias 3216 include upper exposed surfaces that define lands 3218, which are coplanar with upper surface 3010 U of dielectric material 3010.” Huemoeller, [12:33-12:42].</p> <p>“In flip chip die attach operation 2812, die 836 is flip chip attached to vias 3216. More particularly, bond pads 840 of die 836 are physically and electrically connected to lands 3218 of vias 3216 by flip chip bumps 3220. Flip chip bumps 3220 are copper pillars or gold stud bumps in various embodiments although solder can be used.” Huemoeller, [12:45-12:50].</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“Terminals 4158 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by outer electrically conductive bumps 4154.” Huemoeller, [16:38-16:50].</p> <p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Huemoeller discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Vias 424 extends between upper surface 416 U and lower surface 416 L of buildup dielectric material 416. Vias 424 are electrically connected to circuit pattern 202.” Huemoeller, [5:36-5:39].</p> <p>“Blind vias 1914 extend between and electrically connect circuit patterns 1602, 1602 A with one another through dielectric material 1610.” Huemoeller, [9:52-9:54].</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“Vias 3216 extend from upper surface 3010 U of dielectric material 3010, through dielectric material 3010, to contact and be electrically connected to lands 3114.” Huemoeller, [12:37-12:39].</p> <p>“In accordance with this embodiment, redistribution circuit pattern 3934 includes electrically conductive vias 3936 electrically connected to circuit pattern 2902.” Huemoeller, [15:35-15:38].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--

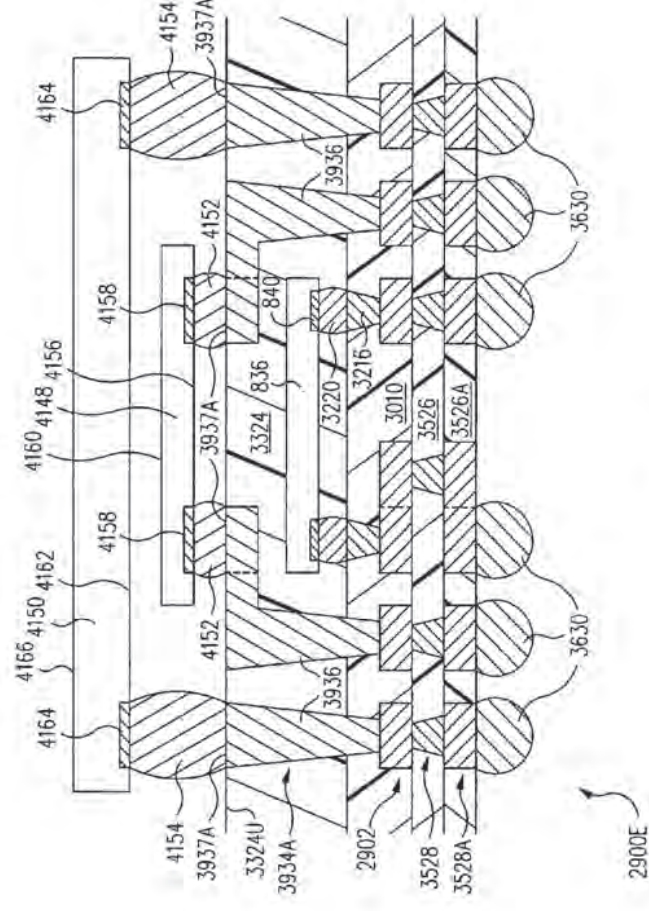
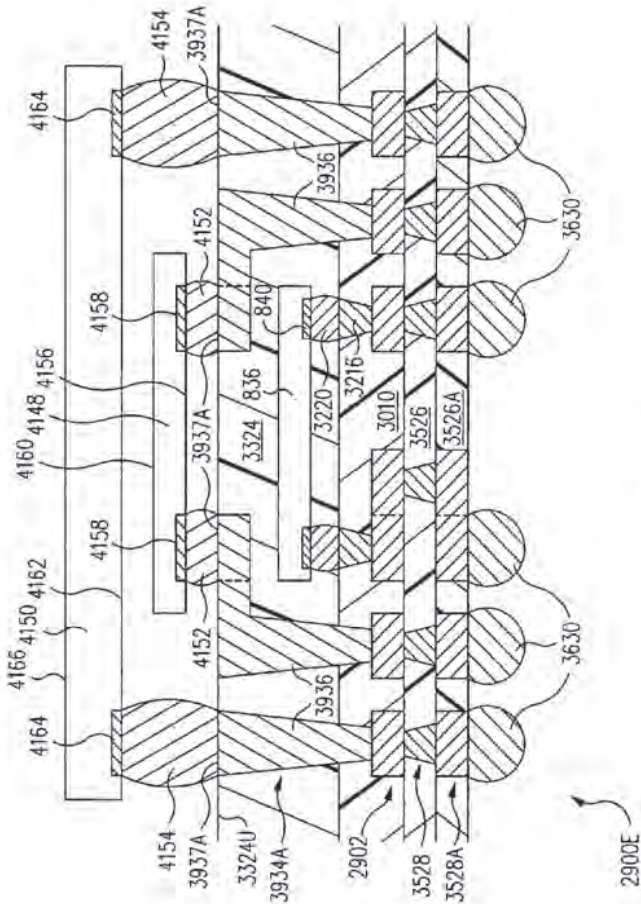


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“Terminals 4158 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by inner electrically conductive bumps 4152.” Huemoeller, [16:38-16:40].</p> <p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Huemoeller discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In die attach operation 118, a die 836 is attached to dielectric material 212. Die 836 is generally an electronic component and in one embodiment is an integrated circuit die. Die 836 includes an active surface 838 having bond pads 840 thereon. Die 836 further includes an inactive surface 842 opposite active surface 838. In die attach operation 118, inactive surface 842 is attached to lower surface 212 L of dielectric material 212 by a die attach adhesive 844. From die attach operation 118, flow moves to a wirebond operation 120. In wirebond operation 120, bond pads 840 of die 836 are wire bonded (electrically connected) to lands 834 of circuit pattern 202 by bond wires 846.” Huemoeller, [6:53-6:67].</p>



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“In die attach operation 1514, die 836 is die attached to upper surface 1610 U of dielectric material 1610. In the embodiment illustrated in FIG. 21, in addition to being attached to upper surface 1610 U of dielectric material 1610, die 836 is also die attached directly to top circuit pattern 1602 and the exposed top surface of a blind via 1914. Die 836 is attached without use of a soldermask over top circuit pattern 1602 and the exposed top surface of blind via 1914. More particularly, inactive surface 842 is attached to upper surface 1610 U of dielectric material 1610, top circuit pattern 1602 and/or the exposed top surface of a blind via 1914 by die attach adhesive 844.” Huemoeller, [10:3-10:14].</p> <p>“Referring now to FIGS. 15 and 27 together, in flip chip die attach operation 1528, die 836 is flip chip attached to bond fingers 2018. More particularly, bond pads 840 of die 836 are physically and electrically connected to bond fingers 2018 by flip chip bumps 2752. From flip chip die attach operation 1528, flow moves, optionally, to encapsulate operation 1520, or directly to remove bottom carrier operation 1522, either of which is performed as discussed above.” Huemoeller, [11:24-11:32].</p> <p>“In flip chip die attach operation 2812, die 836 is flip chip attached to vias 3216. More particularly, bond pads 840 of die 836 are physically and electrically connected to lands 3218 of vias 3216 by flip chip bumps 3220. Flip chip bumps 3220 are copper pillars or gold stud bumps in various embodiments although solder can be used.” Huemoeller, [12:45-12:50].</p> <p>“In one embodiment, an underfill material 3322 is applied between upper surface 3010 U of dielectric material 3010 and active surface 838 of die 836 and around flip chip bumps 3220. A package body 3324 is then applied to encapsulate die 836, underfill 3322, and the exposed portion of upper surface 3010 U of dielectric material 3010.” Huemoeller, [12:53-12:58].</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“Referring now to FIG. 37, in accordance with this embodiment, package body 3324 partially encapsulates die 836 such that inactive surface 842 of die 836 is exposed. In this manner, heat transfer from die 836 to the ambient environment is maximized.” Huemoeller, [14:23-14:27].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p> <p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Huemoeller discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In die attach operation 118, a die 836 is attached to dielectric material 212. Die 836 is generally an electronic component and in one embodiment is an integrated circuit die. Die 836 includes an active surface 838 having bond pads 840 thereon. Die 836 further includes an inactive surface 842 opposite active surface 838. In die attach operation 118, inactive surface 842 is attached to lower surface 212 L of dielectric material 212 by a die attach adhesive 844.” Huemoeller, [6:53-6:63].</p>

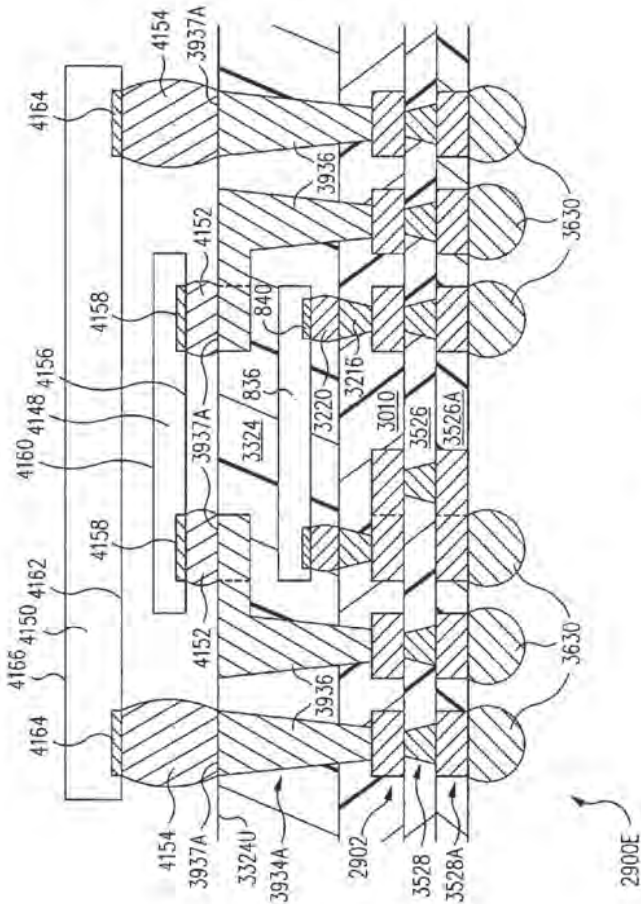


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“From die attach operation 118, flow moves to a wirebond operation 120. In wirebond operation 120, bond pads 840 of die 836 are wire bonded (electrically connected) to lands 834 of circuit pattern 202 by bond wires 846. Optionally, in wirebond operation 120, one or more of bond pads 840 of die 836 are wire bonded (electrically connected) to stiffener 502 by bond wires 846 as indicated by the phantom bond wire 846.” Huemoeller, [6:64-7:3].</p> <p>“In flip chip die attach operation 128, die 836 is flip chip attached to lands 834 of circuit pattern 202. More particularly, an organic solderability protectant (OSP) 1260 is applied within bond finger openings 832 and on lands 834 as illustrated in FIG. 12. Bond pads 840 of die 836 are flip chip attached to lands 834 of circuit pattern 202 with flip chip bumps 1362 as illustrated in FIG. 13.” Huemoeller, [8:30-8:36].</p> <p>“In die attach operation 1514, die 836 is die attached to upper surface 1610 U of dielectric material 1610. In the embodiment illustrated in FIG. 21, in addition to being attached to upper surface 1610 U of dielectric material 1610, die 836 is also die attached directly to top circuit pattern 1602 and the exposed top surface of a blind via 1914. Die 836 is attached without use of a soldermask over top circuit pattern 1602 and the exposed top surface of blind via 1914. More particularly, inactive surface 842 is attached to upper surface 1610 U of dielectric material 1610, top circuit pattern 1602 and/or the exposed top surface of a blind via 1914 by die attach adhesive 844.” Huemoeller, [10:3-10:14].</p> <p>“Referring now to FIGS. 15 and 27 together, in flip chip die attach operation 1528, die 836 is flip chip attached to bond fingers 2018. More particularly, bond pads 840 of die 836 are physically and electrically connected to bond fingers 2018 by flip chip bumps 2752.” Huemoeller, [11:24-11:28].</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

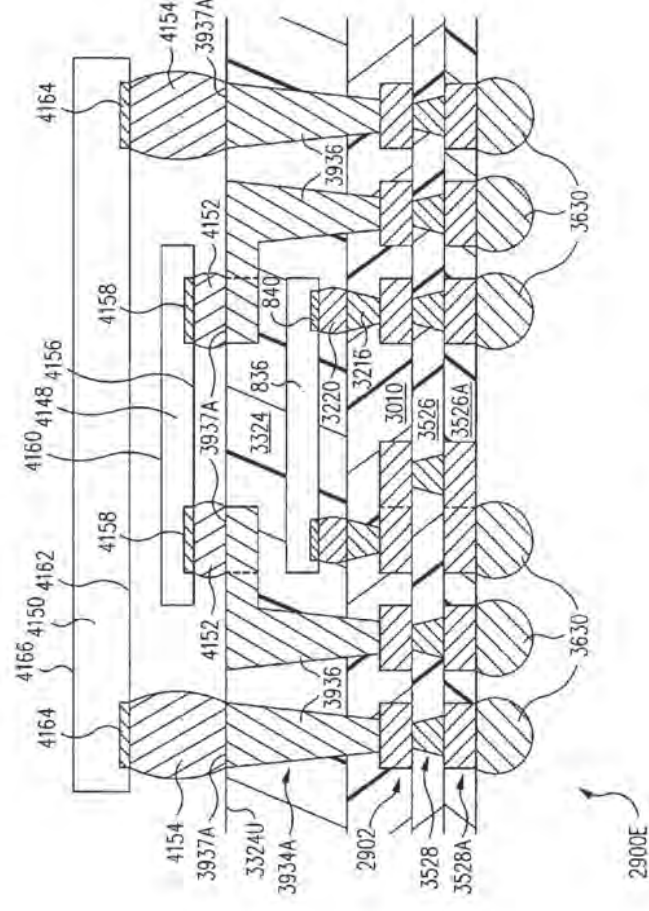
	<p>“In flip chip die attach operation 2812, die 836 is flip chip attached to vias 3216. More particularly, bond pads 840 of die 836 are physically and electrically connected to lands 3218 of vias 3216 by flip chip bumps 3220. Flip chip bumps 3220 are copper pillars or gold stud bumps in various embodiments although solder can be used.” Huemoeller, [12:45-12:50].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p> <p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Huemoeller discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Huemoeller discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In one embodiment, an underfill is applied between upper surface 1610 U of dielectric material 1610 and active surface 838 of die 836 and around flip chip bumps 2752 prior to formation of package body 2348 (formation of package body 2348 is discussed above in reference to FIG. 23).” Huemoeller, [11:32-11:38].</p> <p>“In one embodiment, an underfill material 3322 is applied between upper surface 3010 U of dielectric material 3010 and active surface 838 of die 836 and around flip chip bumps 3220.” Huemoeller, [12:53-12:56].</p> <p>“In accordance with this embodiment, package body 3324 fills the space between upper surface 3010 U of dielectric material 3010 and active surface 838 of die 836 and around flip chip bumps 3220.” Huemoeller, [12:60-12:63].</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>“Terminals 4046 are physically and electrically flip chip connected to lands 3937 A of redistribution circuit pattern 3934 A by bumps 4042, e.g., flip chip bumps.” Huemoeller, [16:8-16:10].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p> <p>“Terminals 4158 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by inner electrically conductive bumps 4152.” Huemoeller, [16:38-16:40].</p> <p>“More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:50-16:55].</p>
--	---

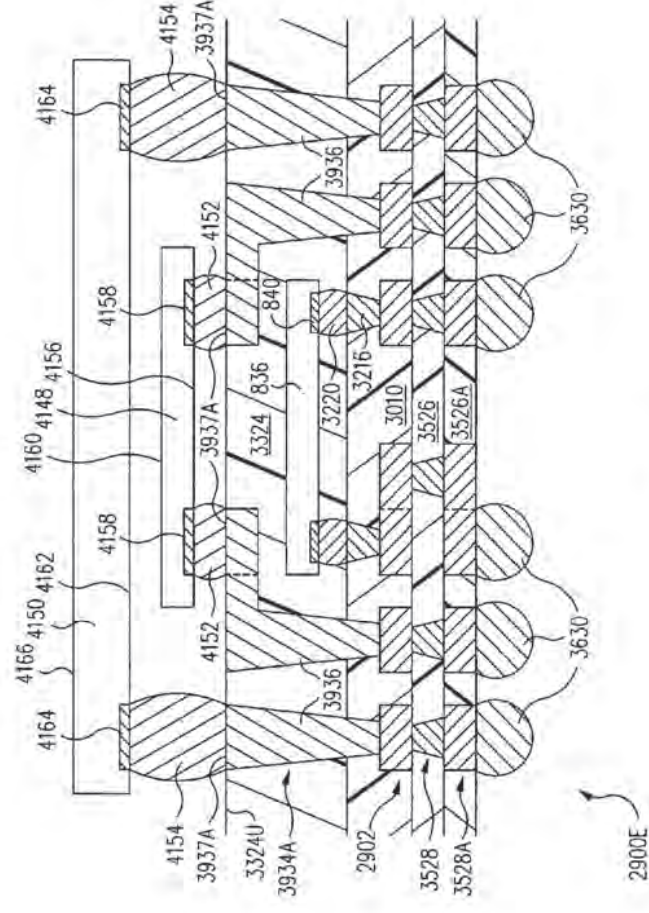


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Huemoeller discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 40 is a cross-sectional view of a package 2900 D in accordance with another embodiment. Package 2900 D of FIG. 40 is an example of a chip in substrate (CIS) plus flip chip (FC) package. In another embodiment, package 2900 D of FIG. 40 is an example of a chip in substrate (CIS) plus full array LOT for system on package. Package 2900 D of FIG. 40 is similar to package 2900 C of FIG. 39 and only the significant differences between the packages are discussed below.” Huemoeller, [15:52-15:59].</p> <p>“Referring now to FIGS. 28 and 40 together, performance of form laser-ablated artifacts operation 2826 and fill laser-ablated artifacts operation 2830 forms redistribution circuit pattern 3934 A electrically connected to circuit pattern 2902. In accordance with this</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>embodiment, redistribution circuit pattern 3934 A includes a plurality of lands 3937 A, e.g., distributed as a fully array of lands on upper surface 3324 U of package body 3324. In mount additional structures operation 2832, an electronic structure 4040 is mounted to redistribution circuit pattern 3934 A by electrically conductive bumps 4042. In one embodiment, electronic structure 4040 is die, e.g., an integrated circuit die, having a lower, e.g., first, surface 4044 (e.g., an active surface in this embodiment) with terminals 4046 (e.g., bond pads in this embodiment) formed thereon. Terminals 4046 are physically and electrically flip chip connected to lands 3937 A of redistribution circuit pattern 3934 A by bumps 4042, e.g., flip chip bumps.” Huemoeller, [15:60-16:10].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900 E in accordance with another embodiment. Package 2900 E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900 E of FIG. 41 is similar to package 2900 D of FIG. 40 and only the significant differences between the packages are discussed below.” Huemoeller, [16:19-16:25].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an</p>
--	--

	<p>upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p> <p>“Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934 A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937 A of redistribution circuit pattern 3934 A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>A of redistribution circuit pattern 3934 A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:25-16:55].</p>
--	--

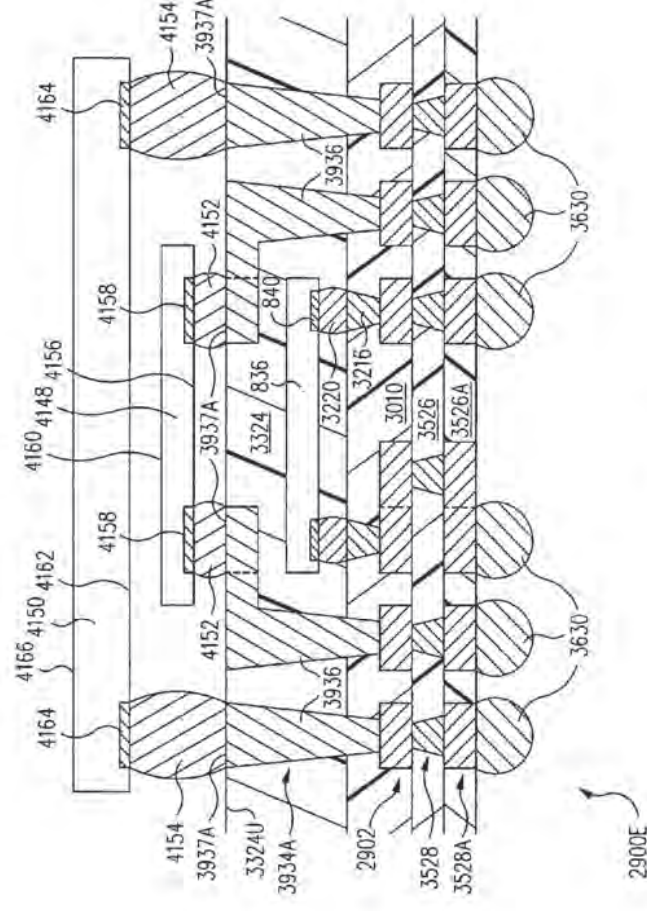


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

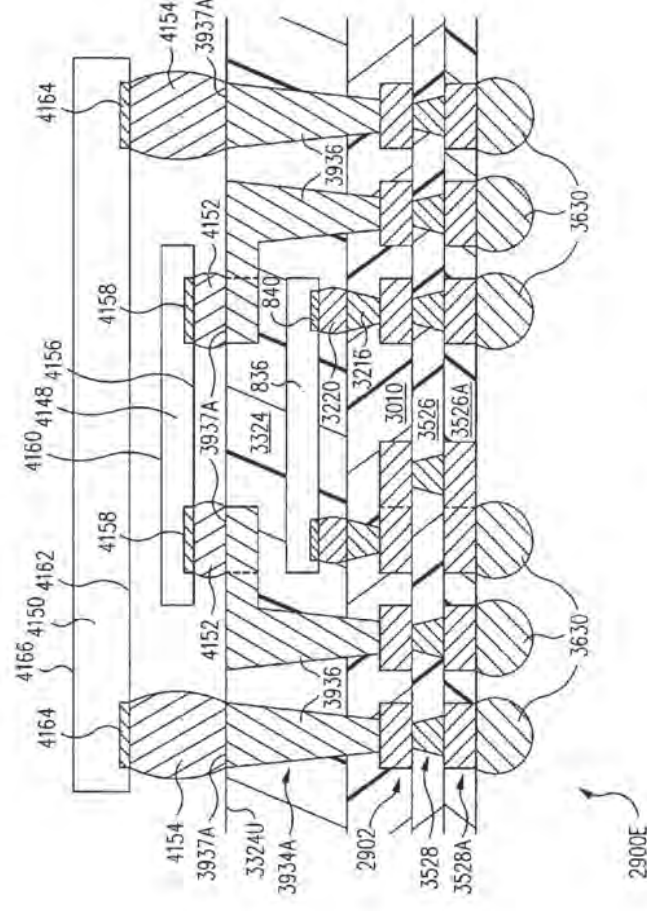
	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Huemoeller discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	---



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Huemoeller discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	---

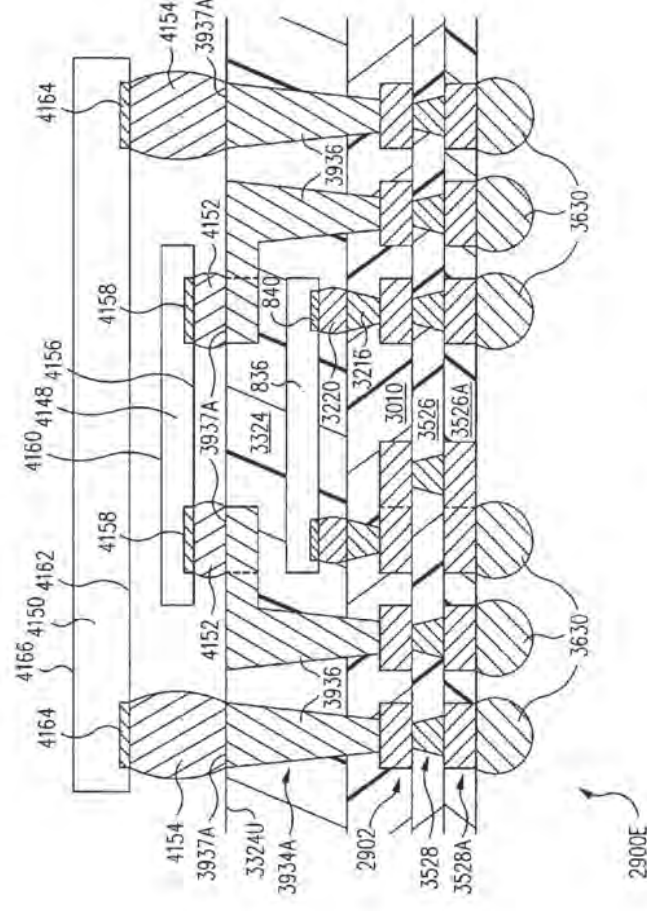


FIG. 41

Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom ends of the plurality of metal pillars of the bottom package substrate via the plurality of metal pillars of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Huemoeller discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring now to FIGS. 1, 2 and 3 together, from provide bottom carrier with dielectric operation 104, flow moves to an embed circuit pattern in dielectric operation 106. In embed circuit pattern in dielectric operation 106, circuit pattern 202 is embedded within dielectric layer 212. More particularly, as shown in FIG. 3, circuit pattern 202 is embedded into an upper, e.g., first, surface 212 U of dielectric material 212. A lower, e.g., second, surface 212 L of dielectric material 212 is mounted to bottom carrier 210. In accordance with one embodiment, circuit pattern 202 is placed on upper surface 212 U of dielectric layer 212. The</p>

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>assembly is heated while circuit pattern 202 is pressed into dielectric material 212, sometimes called a dielectric layer. Due to the heat and pressure, dielectric material 212 is caused to flow around circuit pattern 202 and to top carrier 204. Generally, dielectric material 212 flows to encapsulate circuit pattern 202 within dielectric material 212 such that dielectric material 212 contacts top carrier 204 in the spaces between circuit pattern 202. Dielectric material 212 remains between circuit pattern 202 and bottom carrier 210 thereby electrically isolating circuit pattern 202 and bottom carrier 210 from each other. Stated another way, circuit pattern 202 floats in dielectric material 212. From embed circuit pattern in dielectric operation 106, flow moves to a remove top carrier operation 108. In remove top carrier operation 108, top carrier 204 is removed, e.g., using a selective etch as discussed above, resulting in the structure as illustrated in FIG. 3. From remove top carrier operation 108, flow moves, optionally, to a form blind vias operation 109. In form blind vias operation 109, at least one electrically conductive blind via 314 is formed. Blind vias 314 extend through dielectric material 212 between upper surface 212 U and lower surface 212 L. Blind vias 314 electrically connect circuit pattern 202 to bottom carrier 210 through dielectric material 212. In one embodiment, to form blind vias 314, via apertures, sometimes called blind via apertures, are formed in dielectric material 212 using laser-ablation. Generally, the via apertures are formed between circuit pattern 202 and bottom carrier 210. The via apertures are filled, e.g., with copper or other conductive material, to form blind vias 314.” Huemoeller, [3:45-4:18].</p> <p>“Referring now to FIGS. 1 and 4 together, from form blind vias operation 109 (or directly from remove top carrier operation 108 if form blind vias operation 109 is not performed), flow moves to a mount additional dielectric operation 110. In mount additional dielectric operation 110, a buildup dielectric material 416, sometimes called a buildup dielectric layer or a coreless buildup layer, is mounted to dielectric material 212 and circuit pattern 202. Generally, buildup dielectric material 416 is mounted to dielectric material 212 and over</p>
--	---

	<p>circuit pattern 202 and blind vias 314. More particularly, a lower, e.g., first, surface 416 L of buildup dielectric material 416 is mounted to upper surface 212 U of dielectric material 212. Buildup dielectric material 416 further includes an upper, e.g., second, surface 416 U opposite lower surface 416 L. From mount additional dielectric operation 110, flow moves to a form artifacts in additional dielectric operation 112. In form artifacts in additional dielectric operation 112, buildup dielectric material 416 is laser-ablated resulting in the formation of laser-ablated artifacts in buildup dielectric material 416. The laser-ablated artifacts are formed using a laser-ablation process. During this laser-ablation process, a laser beam is directed at buildup dielectric material 416 and moved. The laser beam laser-ablates at least partially, and in some places through, buildup dielectric material 416. Accordingly, the laser-ablated artifacts are formed at least partially, and in some places through, buildup dielectric material 416. As illustrated in FIG. 4, in one embodiment, the laser-ablated artifacts have a taper profile with the greatest width at upper surface 416 U of buildup dielectric material 416 due to the laser-ablation process. The laser-ablated artifacts include laser-ablated channels, laser-ablated land openings, and/or laser-ablated via apertures. Generally, channels, land openings, and via apertures are particularly shaped laser-ablated voids in buildup dielectric material 416. In one embodiment, a laser-ablated channel, sometimes called a trench, extends horizontally and in a direction parallel with upper surface 416 U of buildup dielectric material 416. In one embodiment, a laser-ablated land opening is an opening, e.g., a circular, rectangular, or other shaped opening, formed using a repeated, e.g., a trepanning, motion of the laser beam. In one embodiment, a laser-ablated via opening, sometimes called a laser-ablated via aperture, is an opening (aperture) extending entirely through buildup dielectric material 416 in a direction perpendicular to upper surface 416 U of buildup dielectric material 416. Although various laser-ablated artifacts are discussed above, in light of this disclosure, those of skill in the art will understand that any one of a number of laser-ablated artifacts can be formed. From form artifacts in additional dielectric operation 112, flow moves to a fill artifacts with electrically conductive material operation</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>114. In fill artifacts with electrically conductive material operation 114, the laser-ablated artifacts are filled with an electrically conductive filler material, e.g., copper, to form a buildup circuit pattern 418 as illustrated in FIG. 4. Optionally, a single layer automatic optical inspection (AOI) is preformed. As shown in FIG. 4, buildup circuit pattern 418 is embedded within buildup dielectric material 416. Buildup circuit pattern 418 includes electrically conductive traces, lands, and/or vias. In one embodiment, buildup circuit pattern 418 redistributes the pattern of circuit pattern 202 to the pattern of buildup circuit pattern 418. In one embodiment, a trace extends horizontally and in a direction parallel with upper surface 416 U of buildup dielectric material 416. To illustrate, buildup circuit pattern 418 includes a trace 420.” Huemoeller, [4:20-5:25].</p> <p>“Referring now to FIGS. 15 and 18 together, from remove top carrier operation 1506, flow moves to a form blind via apertures operation 1508. In form blind via apertures operation 1508, blind via apertures 1812 are formed. Blind via apertures 1812 extend through dielectric material 1610 between upper surface 1610 U and lower surface 1610 L. In one embodiment, blind via apertures 1812 are formed in dielectric material 1610 using laser-ablation and thus have a taper shape as illustrated. Generally, blind via apertures 1812 are formed between top circuit pattern 1602 and bottom circuit pattern 1602 A. Referring now to FIGS. 15 and 19 together, from form blind via apertures operation 1508, flow moves to a fill blind via apertures with electrically conductive material operation 1510. In fill blind via apertures with electrically conductive material operation 1510, blind via apertures 1812 are filled, e.g., with plated copper or other conductive material, to form electrically conductive blind vias 1914. Blind vias 1914 extend between and electrically connect circuit patterns 1602, 1602 A with one another through dielectric material 1610.” Huemoeller, [9:35-9:54].</p> <p>“Referring now to FIGS. 28 and 35 together, from remove carrier operation 2816, flow moves to a mount additional dielectric operation 2818. In mount additional dielectric operation</p>
--	--

	<p>2818, an upper, e.g., first, buildup dielectric material 3526 is mounted to dielectric material 3010 and circuit pattern 2902. More particularly, an upper, e.g., first, surface 3526 U of upper buildup dielectric material 3526 is mounted to lower surface 3010 L of dielectric material 3010. Upper buildup dielectric material 3526 further includes a lower, e.g., second, surface 3526 L opposite upper surface 3526 U. From mount additional dielectric operation 2818, flow moves to a form artifacts in additional dielectric operation 2820. In form artifacts in additional dielectric operation 2820, upper buildup dielectric material 3526 is laser-ablated resulting in the formation of laser-ablated artifacts in upper buildup dielectric material 3526. The laser-ablated artifacts are formed using a laser-ablation process in a manner similar to that described above regarding form artifacts in additional dielectric operation 112 of FIG. 1 and so is only briefly repeated here. During this laser-ablation process, a laser beam is directed at upper buildup dielectric material 3526 and moved. The laser beam laser-ablates at least partially, and in some places through, upper buildup dielectric material 3526. Accordingly, the laser-ablated artifacts are formed at least partially, and in some places through, upper buildup dielectric material 3526. The laser-ablated artifacts include laser-ablated channels, laser-ablated land openings, and/or laser-ablated via apertures. From form artifacts in additional dielectric operation 2820, flow moves to a fill artifacts with electrically conductive material operation 2822. In fill artifacts with electrically conductive material operation 2822, the laser-ablated artifacts are filled with an electrically conductive filler material, e.g., copper, to form an upper, e.g., first, buildup circuit pattern 3528 as illustrated in FIG. 35. The laser-ablated artifacts are filled with an electrically conductive filler material in a manner similar to that described above regarding fill artifacts with electrically conductive material operation 114 of FIG. 1 and so is only briefly discussed here. As shown in FIG. 35, upper buildup circuit pattern 3528 is embedded within upper buildup dielectric material 3526. Upper buildup circuit pattern 3528 includes electrically conductive traces, lands, and/or vias. In one embodiment, upper buildup circuit pattern 3528 redistributes the pattern of circuit pattern 2902 to the pattern of upper buildup circuit pattern 3528. As indicated by the dashed</p>
--	--

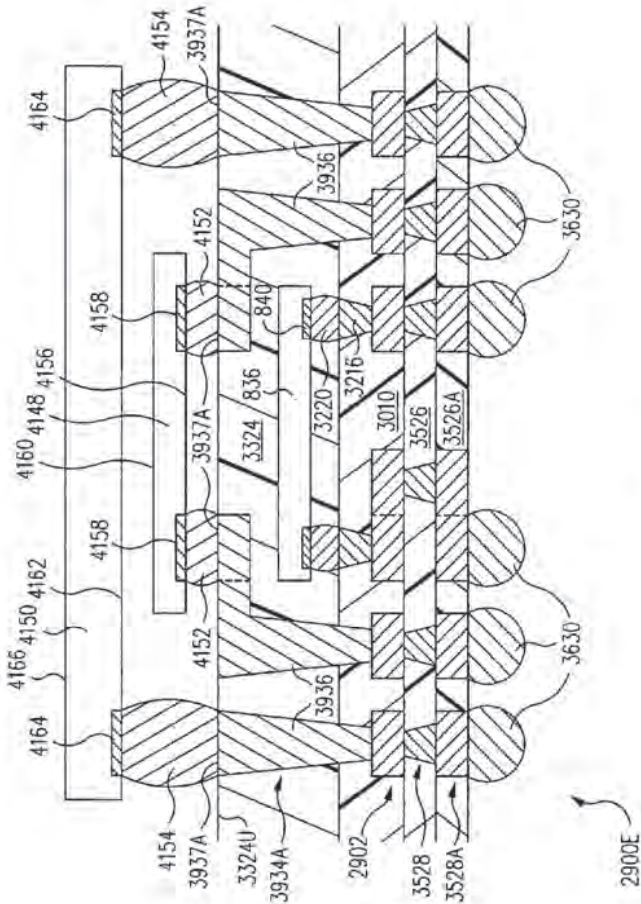
	<p>arrow in FIG. 28, operations 2818, 2820, and 2822 can be repeated any one of a number of times to form additional buildup circuit patterns in additional buildup dielectric materials. In accordance with the embodiment illustrated in FIG. 35, operations 2818, 2820, and 2822 are repeated a second time to form a lower, e.g., second, buildup circuit pattern 3528 A in a lower, e.g., second, buildup dielectric material 3526 A. Lower buildup circuit pattern 3528 A redistributes the pattern of upper buildup circuit pattern 3528 to the pattern of lower buildup circuit pattern 3528 A.” Huemoeller, [13:6-13:66].</p> <p>“Referring now to FIGS. 28 and 39 together, from form interconnection balls operation 2824 (or directly from fill artifacts with electrically conductive material operation 2822 if form interconnection balls operation 2824 is not performed), flow moves to a form laser-ablated artifacts operation 2826. In form laser-ablated artifacts operation 2826, package body 3324 and dielectric material 3010 are laser-ablated resulting in the formation of laser-ablated artifacts extending through package body 3324 and dielectric material 3010 and to circuit pattern 2902. More particularly, portions of circuit pattern 2902 are exposed through the laser-ablated artifacts. The laser-ablated artifacts are formed using a laser-ablation process in a manner similar to that described above regarding form artifacts in additional dielectric operation 112 of FIG. 1 and so is only briefly repeated here. During this laser-ablation process, a laser beam is directed at package body 3324 and moved. The laser beam laser-ablates at least partially, and in some places through, package body 3324 and dielectric material 3010. Accordingly, the laser-ablated artifacts are formed at least partially, and in some places through, package body 3324. Further, the laser-ablated artifacts are formed through dielectric material 3010 to expose portions of circuit pattern 2902. The laser-ablated artifacts include laser-ablated channels, laser-ablated land openings, and/or laser-ablated via apertures. The laser-ablated via apertures extend through both package body 3324 and dielectric material 3010 to expose portions of circuit pattern 2902. From form laser-ablated artifacts 2826, flow moves to a fill laser-ablated artifacts operation 2830. In fill laser-ablated</p>
--	--

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>artifacts operation 2830, the laser-ablated artifacts are filled with an electrically conductive filler material, e.g., copper, to form redistribution circuit pattern 3934 as illustrated in FIG. 39. The laser-ablated artifacts are filled with an electrically conductive filler material in a manner similar to that described above regarding fill artifacts with electrically conductive material operation 114 of FIG. 1 and so is only briefly discussed here. As shown in FIG. 39, redistribution circuit pattern 3934 is embedded within package body 3324 and dielectric material 3010. Redistribution circuit pattern 3934 includes electrically conductive traces, lands, and/or vias. In accordance with this embodiment, redistribution circuit pattern 3934 includes electrically conductive vias 3936 electrically connected to circuit pattern 2902. The upper exposed surfaces of vias 3936 form lands 3937 of redistribution circuit pattern 3934.” Huemoeller, [14:59-15:39].</p> <p>“FIG. 41 is a cross-sectional view of a package 2900E in accordance with another embodiment. Package 2900E of FIG. 41 is an example of a chip in substrate (CIS) plus flip chip (FC) plus package on package (PoP) package. Package 2900E of FIG. 41 is similar to package 2900D of FIG. 40 and only the significant differences between the packages are discussed below. Referring now to FIGS. 28 and 41 together, in mount additional structures operation 2832, inner and outer, e.g., first and second, electronic structures 4148, 4150 are mounted to redistribution circuit pattern 3934A by inner and outer, e.g., first and second, electrically conductive bumps 4152, 4154. In one embodiment, inner electronic structure 4148 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Inner electronic structure 4148 includes a lower, e.g., first, surface 4156 with terminals 4158 formed thereon. Inner electronic structure 4148 further includes an upper, e.g., second, surface 4160 opposite lower surface 4156. Terminals 4158 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by inner electrically conductive bumps 4152. Outer electronic structure 4150 is a die or an electronic component package as discussed above in reference to electronic structure 4040. Outer</p>
--	---

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>electronic structure 4150 includes a lower, e.g., first, surface 4162 with terminals 4164 formed thereon. Outer electronic structure 4150 further includes an upper, e.g., second, surface 4166 opposite lower surface 4162. Terminals 4164 are physically and electrically connected to lands 3937A of redistribution circuit pattern 3934A by outer electrically conductive bumps 4154. More particularly, outer electrically conductive bumps 4154 space outer electronic structure 4150 above inner electronic structure 4148 as illustrated in FIG. 41 such that lower surface 4162 of outer electronic structure 4150 is above upper surface 4160 of inner electronic structure 4148.” Huemoeller, [16:19-16:55].</p>
--	--



Huemoeller, FIG. 41.

Appendix A-15 - Invalidity of U.S. Patent No. 9859202 in view of Huemoeller - U.S. Patent No. 8017436

	<p>To the extent Plaintiff contends that Huemoeller fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

U.S. Patent Publication No. 20150132950 (“Jung”) is titled Semiconductor Packages, Methods of Manufacturing the Same, And Semiconductor Package Structures Including The Same and lists Deok-Young Jung, Pil-Kyu Kang, Byung-Iyul Park, Ji-Soon Park, Seong-Min Son, Jin-Ho An, and Ji-Hwang Kim as inventors. Jung anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Jung is a U.S. patent publication that was filed January 20, 2015 and published May 14, 2015. Jung claims priority to KR 10-2012-0085396 filed on August 3, 2012. Jung is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Jung, or otherwise rendered obvious by disclosures and teachings of Jung, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Jung does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Jung with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Jung, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Jung “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Jung or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Jung set forth in this chart.

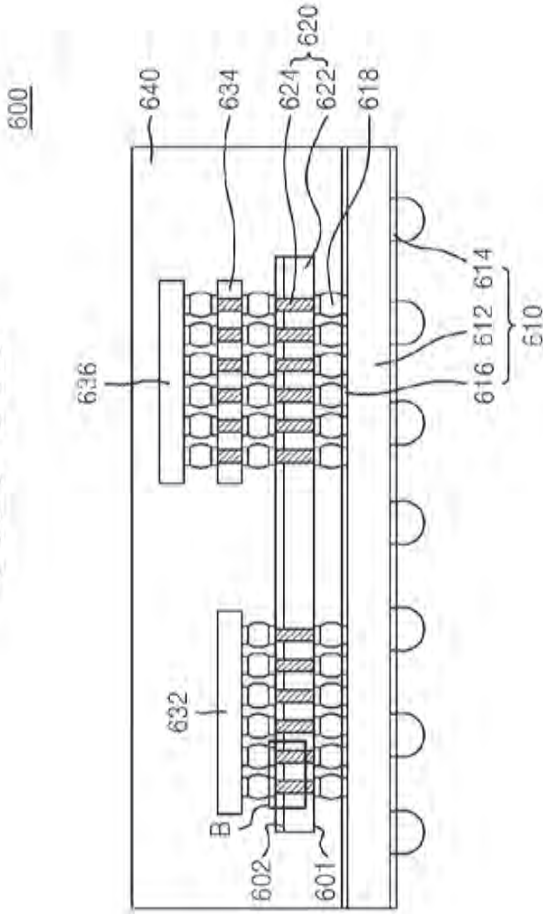
Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Jung discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 20, a semiconductor package 202 according to this example may include a thinned first chip 110 T, a thinned second chip 140 T, and a third chip 170 which are sequentially stacked on the package board 101. The thinned first chip 110 T may include first through-via electrodes 112 and first chip bumps 114 electrically connected to bottom ends of the first through-via electrodes 112, respectively. The thinned second chip 140 T may include second through-via electrodes 143 and second chip bumps 145 electrically connected to bottom ends of the second through-via electrodes 143, respectively.” Jung, [0147-0148].</p>

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>“FIG. 44B is a cross-sectional side view of a semiconductor package 600 according to another example embodiment. FIG. 44C is a partial enlarged cross-sectional view of a portion denoted as B in FIG. 44B. Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636. The package substrate 610 may include a base material 612 and connection pads 614 and 616, as also described above in detail with reference to FIG. 44A and thus, additional descriptions thereof are omitted here.” Jung, [0265-0267].</p>
--	--

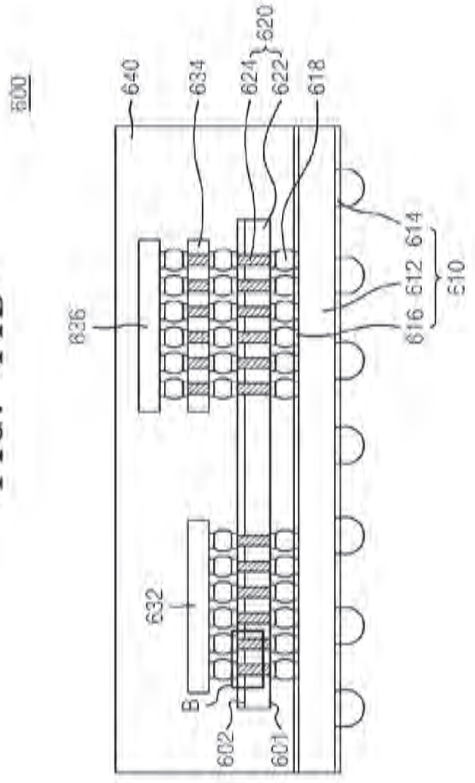
FIG. 44B

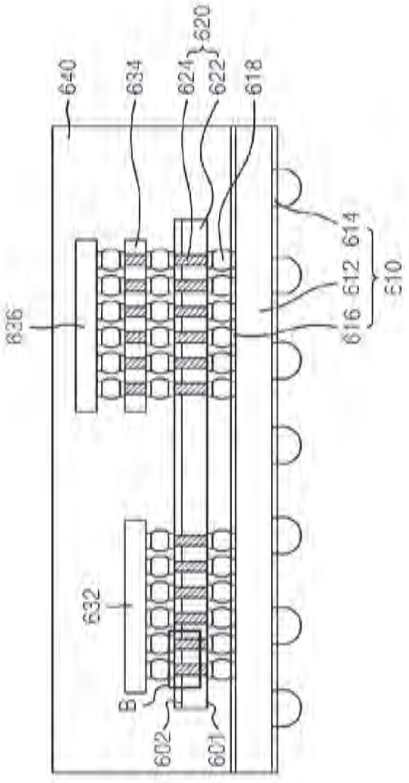


Jung, FIG. 44B

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>“FIG. 44E is a cross-sectional side view of an example of a hybrid memory cube (HMC)-type semiconductor package 703 according to still another example embodiment. Referring to FIG. 44E, a central processing unit (CPU) 722 and a ionic device 720, such as a memory controller, may be disposed on a substrate 710. Also, a plurality of memory devices 730 may be vertically stacked directly on the logic device 720.” Jung, [0283-0284].</p>
<p>[1.A] a bottom package substrate;</p>	<p>Jung discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636. The package substrate 610 may include a base material 612 and connection pads 614 and 616, as also described above in detail with reference to FIG. 44A and thus, additional descriptions thereof are omitted here.” Jung, [0266-0267].</p>

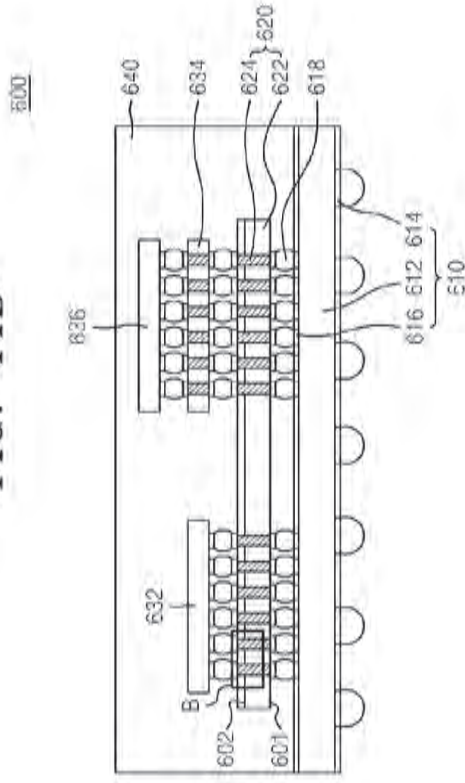
	<p style="text-align: center;">FIG. 44B</p>  <p style="text-align: center;">Jung, FIG. 44B</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p> <p>See, <i>e.g.</i>:</p>
--	---

	<p>“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636.” Jung, [0266].</p> <p style="text-align: center;">FIG. 44B</p>  <p style="text-align: center;">Jung, FIG. 44B</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Jung discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“A first underfiller 118 may fill a space between the thinned first chip 110 T and the package board 101. The first chip bumps 114 may be surrounded by the first underfiller 118. A first mold layer may be disposed on the package board 101 and surround a sidewall of the thinned first chip 110 T.” Jung, [0136-0137].</p> <p>“A second underfiller 147 may fill a space between the thinned first chip 110 T and the second chip 140. A second mold layer 150 may be disposed on the first mold layer 120 a. The second mold layer 150 may surround at least a sidewall of the second chip 140.” Jung, [0140-0141].</p> <p>“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636. The package substrate 610 may include a base material 612 and connection pads 614 and 616, as also described above in detail with reference to FIG. 44A and thus, additional descriptions thereof are omitted here.” Jung, [0266-0267].</p>
---	---

FIG. 44B



Jung, FIG. 44B

“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636. The package substrate 610 may include a base material 612 and connection pads 614 and 616, as also described above in detail with reference to FIG. 44A and thus, additional descriptions thereof are omitted here.” Jung, [0266-0267].

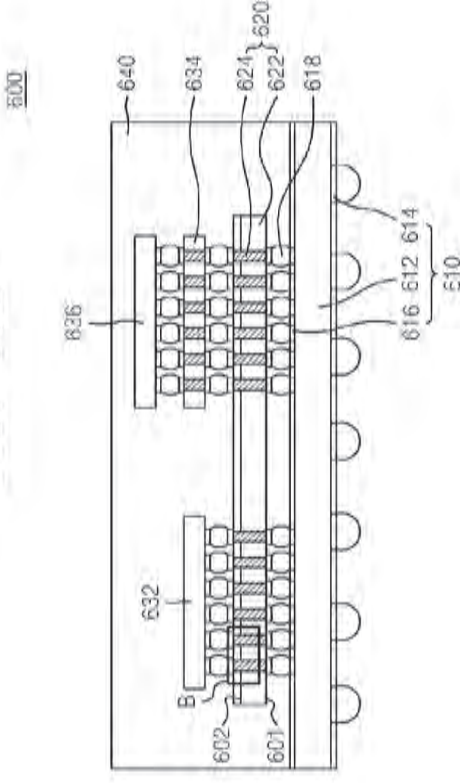
“The interposer 620 may be interposed between the package substrate 610 and the semiconductor substrates 632 and 634. The interposer 620 may include an interposer

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620.” Jung, [0269-0270].</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Jung discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer 620 may be interposed between the package substrate 610 and the semiconductor substrates 632 and 634. The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That</p>

is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such electrical connection may be achieved by conductive interconnections formed in the interposer 620. Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal.” Jung, [0270-0271].

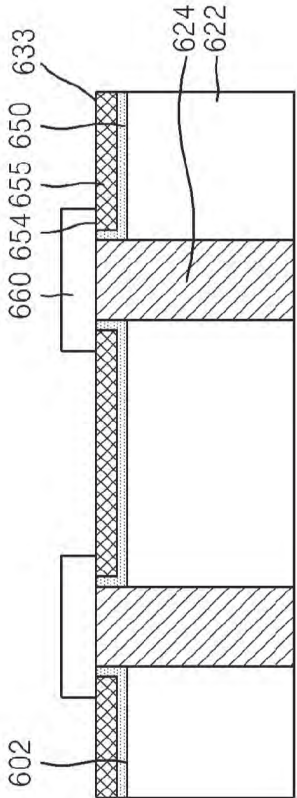
FIG. 44B



Jung, FIG. 44B

“It will be understood by one of ordinary skill in the art that the silicon oxide layer 650 and the silicon nitride layer 655 shown in FIG. 44C are configured similar to those of FIG. 41. Also, it will be understood by one of ordinary skill in the art that the structure shown in FIG. 42 or Fill. 43 may be applied on the second surface 602 of the interposer 620.” Jung, [0276].

FIG. 44C



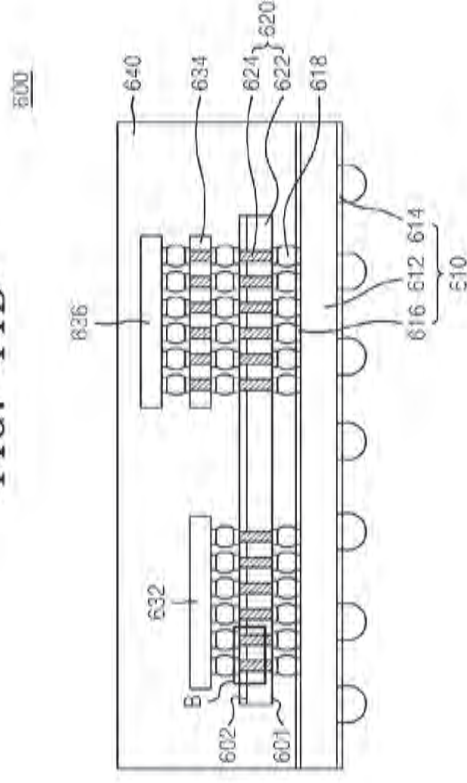
Jung, FIG. 44C

To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Jung discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such electrical connection may be achieved by conductive interconnections formed in the interposer 620.” Jung, [0270-0271].</p>
--	--

FIG. 44B

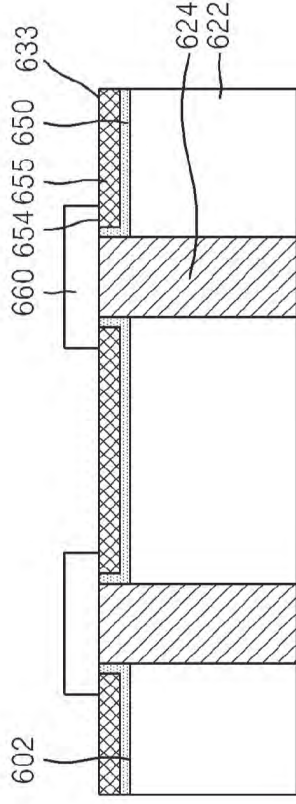


Jung, FIG. 44B

“Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal. A through-via electrode pad 660 may be provided on the second surface 602 and electrically connected to the through-via electrode 624. The through-via electrode pad 660 has been described in detail with reference to FIG. 41, and a method of forming the through-via electrode pad 660 will be described in detail later.” Jung, [0271-0272].

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

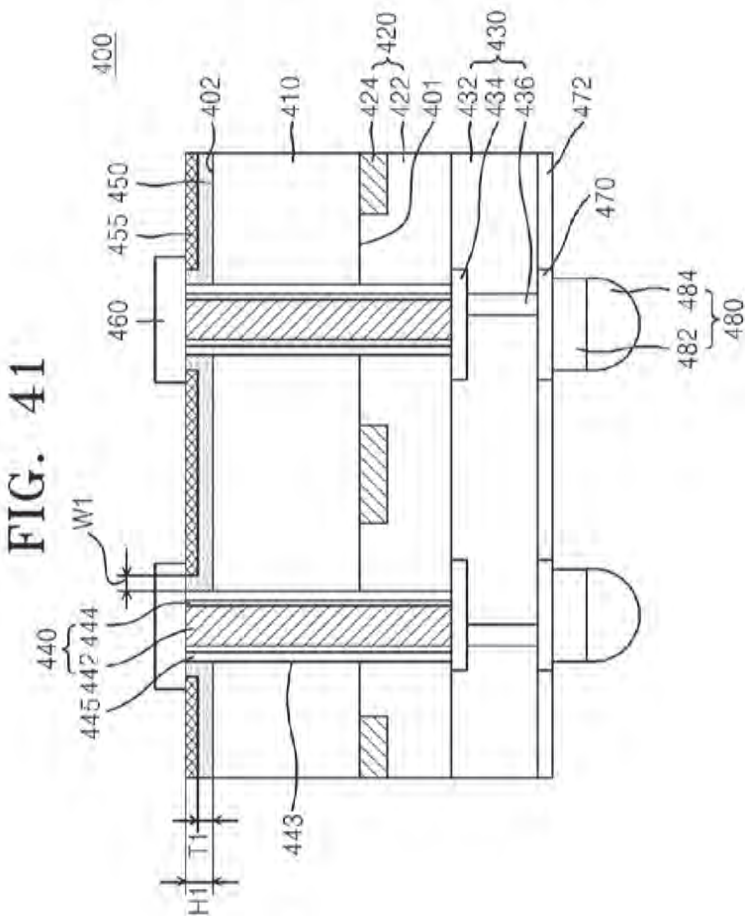
	<p>“The silicon oxide layer 650 may extend along the second surface 602 in a horizontal direction, and extend to the through-via electrode 624. The silicon oxide layer 650 may be in direct contact with the second surface 602. In some embodiments, a vertical portion of the silicon oxide layer 650 may be conformally formed on sidewalls 621 of the through-via electrode 624 and may extend from the second surface 602 to the bottom surface 654 of the through-via electrode pad 660.” Jung, [0274].</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Jung discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal. A through-via electrode pad 660 may be provided on the second surface 602 and electrically connected to the through-via electrode 624. The through-via electrode pad 660 has been described in detail with reference</p>

	<p>to FIG. 41, and a method of forming the through-via electrode pad 660 will be described in detail later.” Jung, [0271-0272].</p> <p style="text-align: center;">FIG. 44C</p>  <p>Jung, FIG. 44C</p> <p>“An oxide layer such as a silicon oxide layer 650 may be provided on the second surface 602 and extend along the second surface 602. A silicon nitride layer 655 may be disposed on the silicon oxide layer 650. The silicon nitride layer 655 may be in contact with at least a portion of a bottom surface 654 of the through-via electrode pad 660. The interposer 622 may be, for example, a silicon substrate, but it is not limited thereto.” Jung, [0273].</p> <p>“The silicon oxide layer 650 may extend along the second surface 602 in a horizontal direction, and extend to the through-via electrode 624. The silicon oxide layer 650 may be in</p>
--	--

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>direct contact with the second surface 602. In some embodiments, a vertical portion of the silicon oxide layer 650 may be conformally formed on sidewalls 621 of the through-via electrode 624 and may extend from the second surface 602 to the bottom surface 654 of the through-via electrode pad 660. The silicon nitride layer 655 may be in direct, contact with the silicon oxide layer 650 and extend in a direction substantially parallel to the second surface 602. Also, the silicon nitride layer 655 may extend under the through-via electrode pad 660. In particular, the silicon nitride layer 655 may be in contact with at least a portion of the bottom surface 654 of the through-via electrode pad 660. In this case, a top surface 633 of the silicon nitride layer 655 may be substantially coplanar with the bottom surface 654 of the through-via electrode pad 660.” Jung, [0274-0275].</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Jung discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The embodiment shown in FIG. 41 illustrates an example in which the through-via electrode 440 has a via-middle structure. That is, after the semiconductor device unit 424 and the interlayer insulating layer 422 are formed and before the interconnection layer 430 is formed, the through-via electrode 440 may be formed. However, the present inventive concept is not limited thereto and may be applied to a via-first structure or a via-last structure. The via-first structure and the via-last structure are known to one of ordinary skill in the art and thus,</p>

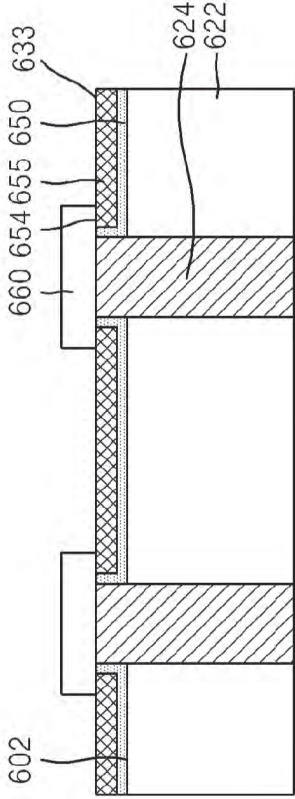
detailed descriptions thereof are omitted. Such examples may be disclosed in U.S. Pat. Nos. 8,653,676 and 8,648,429, the disclosures of which are incorporated herein by reference.”
Jung, [0217].



Jung, FIG. 41

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

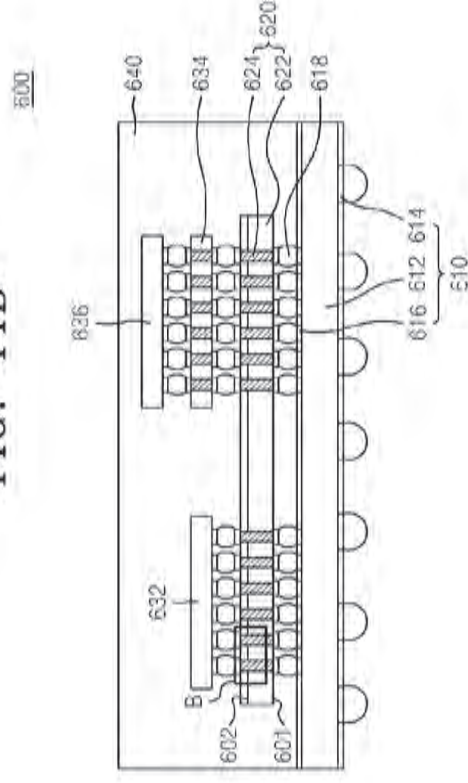
	<p>“As shown in FIG. 44A, an underfill 529 may be injected under the first semiconductor device 520 and the second semiconductor device 530. A top surface of the package substrate 510 and the first and second semiconductor devices 520 and 530 may be encapsulated by an encapsulant 540. The encapsulant 540 may be formed of, for example, a polymer material such as an epoxy molding compound (EMC), but is not limited thereto.” Jung, [0263-0264].</p> <p>“Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal. A through-via electrode pad 660 may be provided on the second surface 602 and electrically connected to the through-via electrode 624. The through-via electrode pad 660 has been described in detail with reference to FIG. 41, and a method of forming the through-via electrode pad 660 will be described in detail later.” Jung, [0271-0272].</p>
--	--

	<p style="text-align: center;">FIG. 44C</p>  <p style="text-align: center;">Jung, FIG. 44C</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Jung discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>“A conductive bump, e.g., a solder bump 501 for connecting the semiconductor chip with an external device may be disposed on the connection pad 514. The solder bump 501 may be a tin (Sn)-based solder bump. In more detail, the solder bump 501 may include Sn as a main component, and include Ag and/or Cu. However, the present inventive concept is not limited thereto.” Jung, [0259].</p> <p>“The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such electrical connection may be achieved by conductive interconnections formed in the interposer 620.” Jung, [0270-0271].</p>
--	--

FIG. 44B



Jung, FIG. 44B

To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the

See, e.g.:

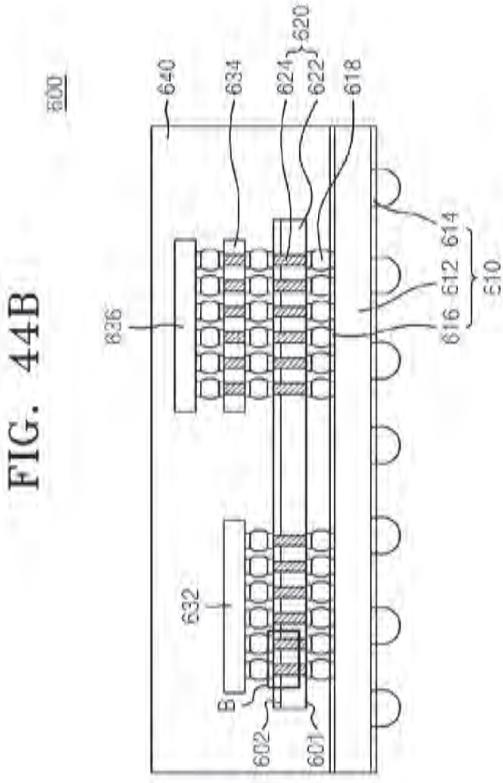
Jung discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

<p>plurality of metal pillars of the spacer connector, and</p>	<p>“Referring to FIG. 1 again, the first chip 110 may be mounted on the package board part 101 by a flip-chip bonding method. Thus, the first chip bump 114 of the first chip 110 may be connected to the internal connection pad 107 of the package board part 101. For example, the first chip 110 may be electrically connected to the package board part 101 through the first chip bump 114. For example, mounting the first chip 110 on the package board part 101 may include loading the first chip 110 on the package board part 101 such that the first chip bump 114 is connected to the internal connection pad 107, and filling a space between the first chip and the package board part 101 with a first underfiller 118.” Jung, [0099].</p> <p>“Referring to FIG. 7, an inter-chip pad 130 may be formed on each of the exposed through-via electrodes 112. The inter-chips pads 130 respectively connected to the through-via electrodes 112 may be spaced apart from each other. The inter-chip pad 130 may include a metal. For example, the inter-chip pad 130 may include copper or solder. The inter-chip pad 130 may be formed by various processes, e.g., a plating process, an inkjet process, and/or a patterning process.” Jung, [0111].</p> <p>“Referring to FIG. 8, a second chip 140 may be mounted on each of the thinned first chips 110 T. The second chip 140 may include at least one second chip bump 145. For example, the second chip 140 may be loaded on the thinned first chip 1107 to connect the second chip bump 145 to the inter-chip pad 130, and then a space between the thinned first chip 110 T and the second chip 140 may be filled with a second underfiller 147. Thus, the second chip 140 may be mounted on the thinned first chip 110 T.” Jung, [0112-0113].</p> <p>“Referring to FIG. 18, a semiconductor package 200 according to an example embodiment may include a thinned first chip 110 T mounted on a package board 101 and a second chip 140 mounted on the thinned first chip 110 T. The package board 101 may include external</p>
--	---

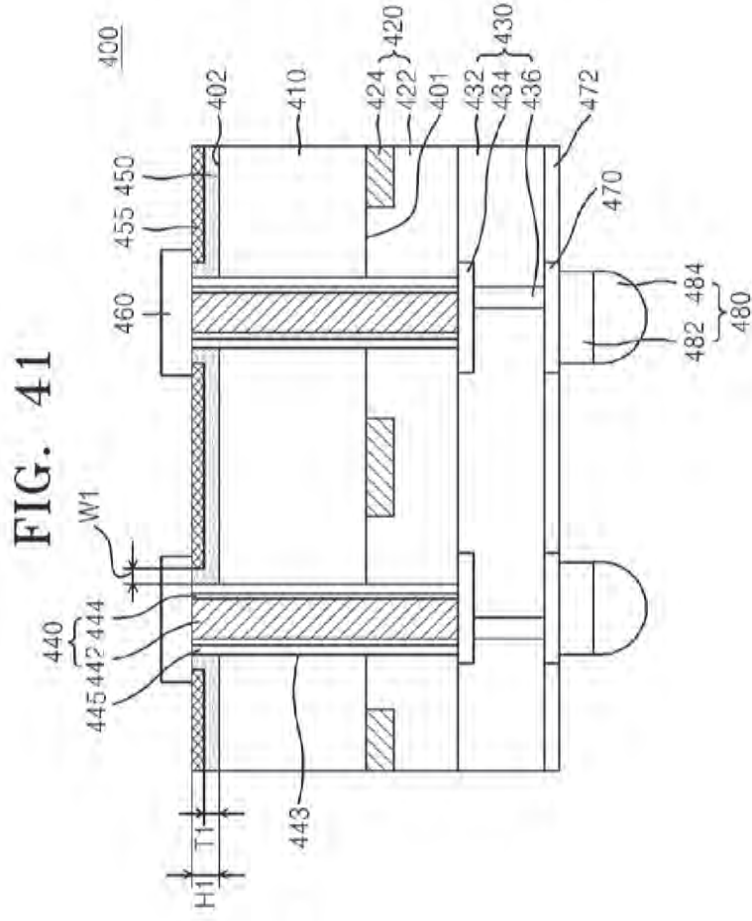
	<p>connection pads 105 disposed on a bottom surface of the package board 101 and internal connection pads 107 disposed on a top surface of the package board 101. The thinned first chip 110 T may have a first surface and a second surface opposite to each other. The first surface of the thinned first chip 110 T may be adjacent to the package board 101. The thinned first chip 110 T may include through-via electrodes 112 penetrating the thinned first chip 110 T. The thinned first chip 110 T may have first chip bumps 114 disposed on the first surface thereof. The first chip bumps 114 may be electrically connected to bottom ends of the through-via electrodes 112, respectively. The first chip bumps 114 of the thinned first chip 110 T may be connected to the internal connection pads 107 of the package board 101, respectively.” Jung, [0135-0136].</p> <p>“The connection member 480 may include a conductive pillar 482 and a micro-bump 484. The conductive pillar 482 may be formed using an electroplating process and have a cylindrical shape. In the present embodiment, the conductive pillar 482 may be a copper (Cu) pillar. However, a material for the metal pillar 482 is not limited to copper. For example, the metal pillar 482 may be formed of aluminum (Al), nickel (Ni), gold (Au), or an alloy thereof. On the other hand, the conductive pillar 482 may be formed not only in a cylindrical shape but also in various shapes, such as a rectangular pillar and an elliptical pillar.” Jung, [0231].</p> <p>“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636. The package substrate 610 may include a base material 612 and connection pads 614 and 616, as also described above in detail with reference to FIG. 44A and thus, additional descriptions thereof are omitted here. Various semiconductor devices may be provided on the active surface of each of the semiconductor substrates 632, 634, and 636. For example,</p>
--	--

	<p>the semiconductor devices may include a memory device, a core circuit device, a peripheral circuit device, a logic circuit device, or a control circuit device, as described in detail with reference to FIG. 44A and thus, additional descriptions are omitted here. The interposer 620 may be interposed between the package substrate 610 and the semiconductor substrates 632 and 634. The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such electrical connection may be achieved by conductive interconnections formed in the interposer 620. Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal. A through-via electrode pad 660 may be provided on the second surface 602 and electrically connected to the through-via electrode 624.” Jung, [0266-0272].</p>
--	--



Jung, FIG. 44B

“The embodiment shown in FIG. 41 illustrates an example in which the through-via electrode 440 has a via-middle structure. That is, after the semiconductor device unit 424 and the interlayer insulating layer 422 are formed and before the interconnection layer 430 is formed, the through-via electrode 440 may be formed. However, the present inventive concept is not limited thereto and may be applied to a via-first structure or a via-last structure. The via-first structure and the via-last structure are known to one of ordinary skill in the art and thus, detailed descriptions thereof are omitted. Such examples may be disclosed in U.S. Pat. Nos. 8,653,676 and 8,648,429, the disclosures of which are incorporated herein by reference.”
Jung, [0217].



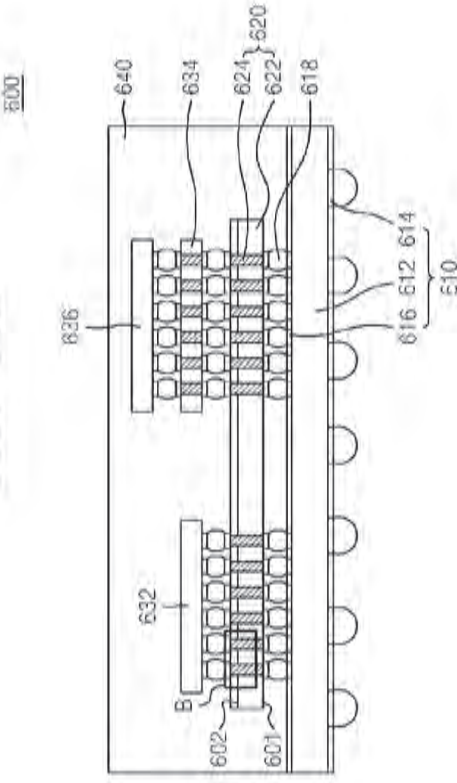
Jung, FIG. 41

To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

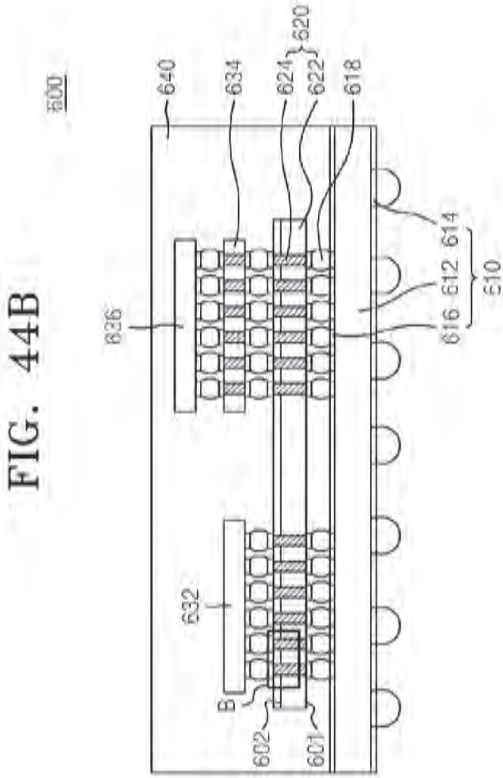
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Jung discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such electrical connection may be achieved by conductive interconnections formed in the interposer 620. Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal.” Jung, [0270-0272].</p>
--	--

	<p style="text-align: center;">FIG. 44B</p> <p>Jung, FIG. 44B</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Jung discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p>

	<p>“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636.” Jung, [0266].</p> <p style="text-align: center;">FIG. 44B</p>  <p style="text-align: right;">Jung, FIG. 44B</p> <p>“Various semiconductor devices may be provided on the active surface of each of the semiconductor substrates 632, 634, and 636. For example, the semiconductor devices may include a memory device, a core circuit device, a peripheral circuit device, a logic circuit</p>
--	---

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>device, or a control circuit device, as described in detail with reference to FIG. 44A and thus, additional descriptions are omitted here.” Jung, [0268].</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Jung discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636.” Jung, [0266].</p>



Jung, FIG. 44B

“Various semiconductor devices may be provided on the active surface of each of the semiconductor substrates 632, 634, and 636. For example, the semiconductor devices may include a memory device, a core circuit device, a peripheral circuit device, a logic circuit device, or a control circuit device, as described in detail with reference to FIG. 44A and thus, additional descriptions are omitted here.” Jung, [0268].

To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

Jung discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

See, e.g.:

“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636.” Jung, [0266].

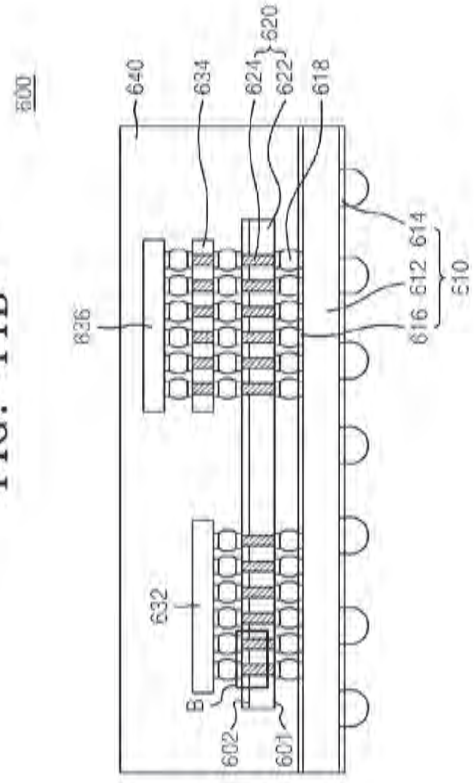
FIG. 44B

Jung, FIG. 44B

	<p>“The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such electrical connection may be achieved by conductive interconnections formed in the interposer 620.” Jung, [0270-0271].</p> <p>“Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal.” Jung, [0271].</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Jung discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636.” Jung, [0266].</p> <p>“The interposer 620 may be interposed between the package substrate 610 and the semiconductor substrates 632 and 634.” Jung, [0269].</p> <p>“The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such</p>

	<p>electrical connection may be achieved by conductive interconnections formed in the interposer 620.” Jung, [0270-0271].</p> <p style="text-align: center;">FIG. 44B</p>  <p style="text-align: center;">Jung, FIG. 44B</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

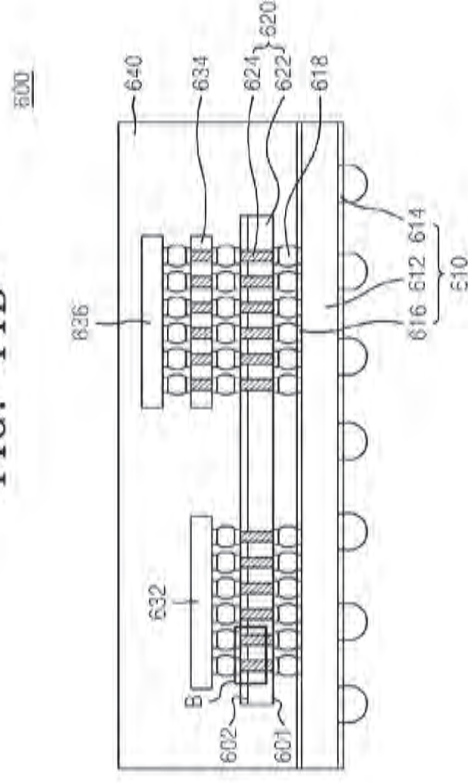
Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Jung discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Various semiconductor devices may be provided on the active surface of each of the semiconductor substrates 632, 634, and 636. For example, the semiconductor devices may include a memory device, a core circuit device, a peripheral circuit device, a logic circuit device, or a control circuit device, as described in detail with reference to FIG. 44A and thus, additional descriptions are omitted here.” Jung, [0268].</p> <p>“The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such electrical connection may be achieved by conductive interconnections formed in the interposer 620.” Jung, [0270-0271].</p>

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Jung discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 44B is a cross-sectional side view of a semiconductor package 600 according to another example embodiment. FIG. 44C is a partial enlarged cross-sectional view of a portion denoted as B in FIG. 44B. Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636.” Jung, [0265-0266].</p>
--	---

FIG. 44B



Jung, FIG. 44B

“The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>electrical connection may be achieved by conductive interconnections formed in the interposer 620.” Jung, [0270-0271].</p> <p>“Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal.” Jung, [0271].</p> <p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

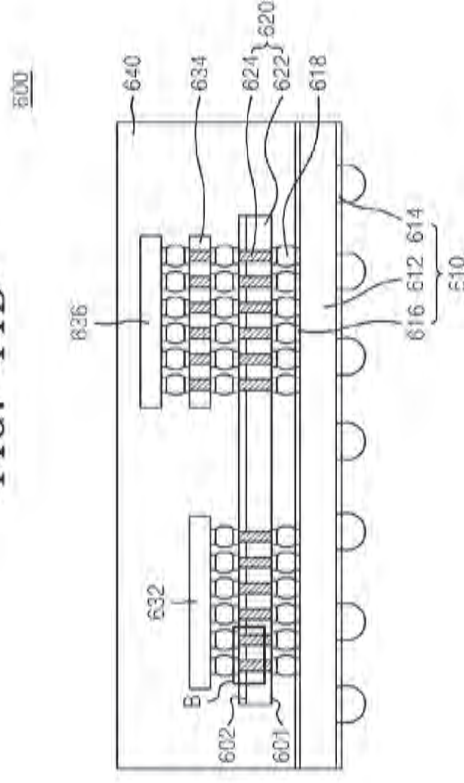
Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	Jung discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

<p>the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p><i>See, e.g.:</i></p> <p>“Referring to FIG. 44C, which is a detailed view of the portion of the interposer 620, which is denoted as B in FIG. 44B, the through-via electrode 624 extending through the interposer substrate 622 may be provided. Although not specifically shown in FIG. 44C, a spacer insulating layer may be further provided along the circumference of the through-via electrode 624 to provide electrical insulation. Also, the through-via electrode 624 may include a barrier metal layer depending on the properties of a conductive metal. A through-via electrode pad 660 may be provided on the second surface 602 and electrically connected to the through-via electrode 624. The through-via electrode pad 660 has been described in detail with reference to FIG. 41, and a method of forming the through-via electrode pad 660 will be described in detail later. An oxide layer such as a silicon oxide layer 650 may be provided on the second surface 602 and extend along the second surface 602. A silicon nitride layer 655 may be disposed on the silicon oxide layer 650. The silicon nitride layer 655 may be in contact with at least a portion of a bottom surface 654 of the through-via electrode pad 660. The interposer 622 may be, for example, a silicon substrate, but it is not limited thereto. The silicon oxide layer 650 may extend along the second surface 602 in a horizontal direction, and extend to the through-via electrode 624. The silicon oxide layer 650 may be in direct contact with the second surface 602. In some embodiments, a vertical portion of the silicon oxide layer 650 may be conformally formed on sidewalls 621 of the through-via electrode 624 and may extend from the second surface 602 to the bottom surface 654 of the through-via electrode pad 660. The silicon nitride layer 655 may be in direct, contact with the silicon oxide layer 650 and extend in a direction substantially parallel to the second surface 602. Also, the silicon nitride layer 655 may extend under the through-via electrode pad 660. In particular, the silicon nitride layer 655 may be in contact with at least a portion of the bottom surface 654 of the through-via electrode pad 660. In this case, a top surface 633 of the silicon nitride layer</p>
--	---

655 may be substantially coplanar with the bottom surface 654 of the through-via electrode pad 660.” Jung, [0271-0275].

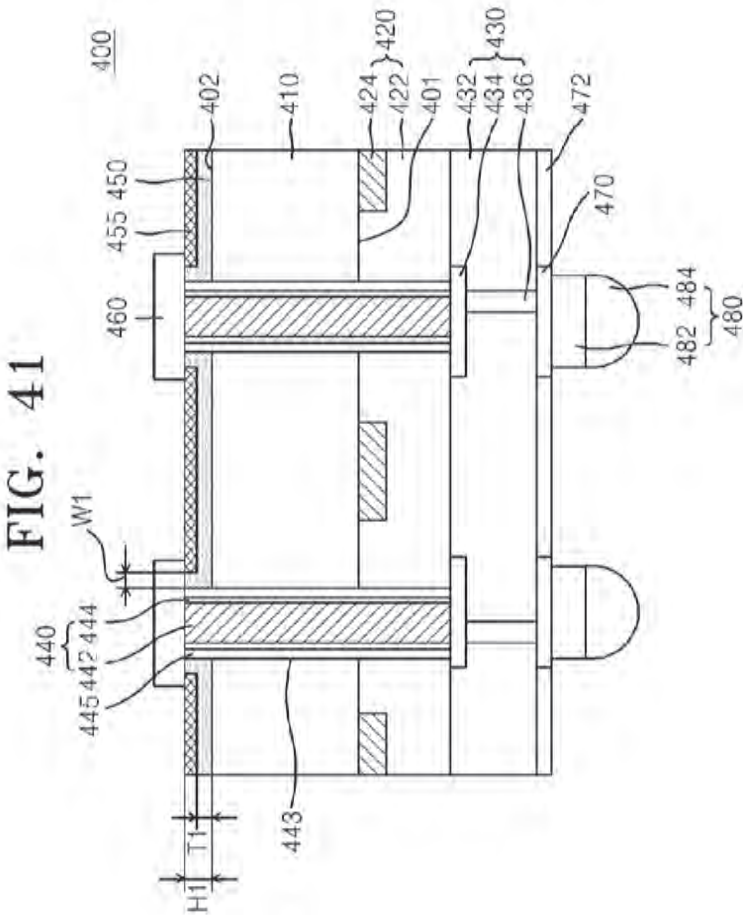
FIG. 44B



Jung, FIG. 44B

“The embodiment shown in FIG. 41 illustrates an example in which the through-via electrode 440 has a via-middle structure. That is, after the semiconductor device unit 424 and the interlayer insulating layer 422 are formed and before the interconnection layer 430 is formed, the through-via electrode 440 may be formed. However, the present inventive concept is not limited thereto and may be applied to a via-first structure or a via-last structure. The via-first structure and the via-last structure are known to one of ordinary skill in the art and thus, detailed descriptions thereof are omitted. Such examples may be disclosed in U.S. Pat. Nos.

8,653,676 and 8,648,429, the disclosures of which are incorporated herein by reference.”
Jung, [0217].



Jung, FIG. 41

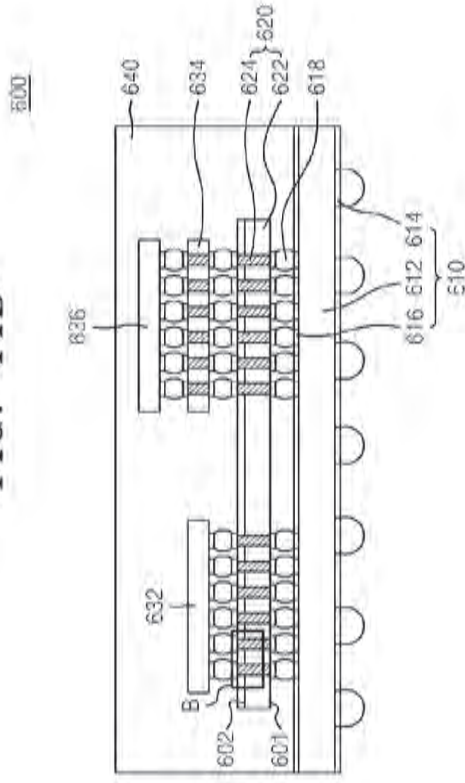
Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom ends of the plurality of metal pillars of the bottom package substrate via the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Jung discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 44B and 44C, semiconductor substrates 632, 634, and 636 disposed on a package substrate 610 may be provided. Semiconductor devices may be formed on active surfaces of the semiconductor substrates 632, 634, and 636. Also, an interposer 620 may be disposed between the package substrate 610 and the semiconductor substrates 632, 634, and 636.” Jung, [0266].</p>

FIG. 44B

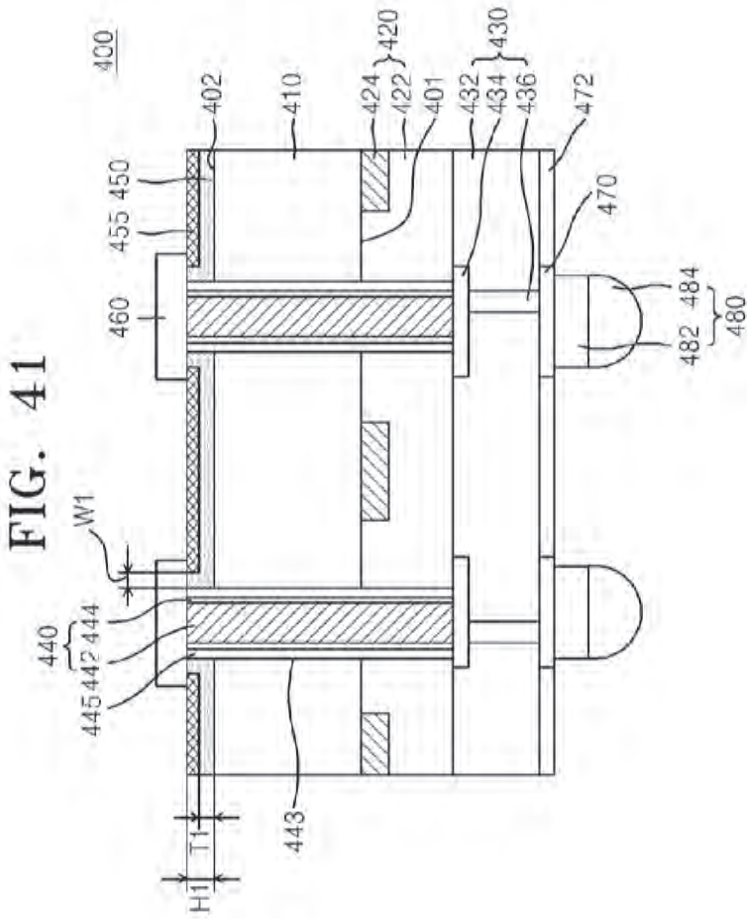


Jung, FIG. 44B

“The interposer 620 may include an interposer substrate 622 having a first surface 601 and a second surface 602 and a through-via electrode 624 extending from the first surface 601 to the second surface 602. Although not illustrated in detail in FIG. 44B, a portion of the through-via electrode 624 may protrude above the second surface 602. The interposer 620 may not only serve as a medium for electrically connecting the semiconductor substrates 632, 634, and 636 with the package substrate 610, but also serve as a medium for electrically connecting the semiconductor substrate 632 and the semiconductor substrate 634, which are arranged horizontally on the interposer 620. That is, at least two semiconductor substrates may be stacked directly on the interposer 620, and electrical connection between the at least two semiconductor substrates may be enabled by the interposer 620. More specifically, such

Appendix A-16 - Invalidity of U.S. Patent No. 9859202 in view of Jung - U.S. Patent Publication No. 20150132950

	<p>electrical connection may be achieved by conductive interconnections formed in the interposer 620.” Jung, [0270-0271].</p> <p>“A through-via electrode pad 660 may be provided on the second surface 602 and electrically connected to the through-via electrode 624. The through-via electrode pad 660 has been described in detail with reference to FIG. 41, and a method of forming the through-via electrode pad 660 will be described in detail later.” Jung, [0272].</p> <p>“The embodiment shown in FIG. 41 illustrates an example in which the through-via electrode 440 has a via-middle structure. That is, after the semiconductor device unit 424 and the interlayer insulating layer 422 are formed and before the interconnection layer 430 is formed, the through-via electrode 440 may be formed. However, the present inventive concept is not limited thereto and may be applied to a via-first structure or a via-last structure. The via-first structure and the via-last structure are known to one of ordinary skill in the art and thus, detailed descriptions thereof are omitted. Such examples may be disclosed in U.S. Pat. Nos. 8,653,676 and 8,648,429, the disclosures of which are incorporated herein by reference.” Jung, [0217].</p>
--	--



Jung, FIG. 41

To the extent Plaintiff contends that Jung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

U.S. Patent Publication No. 20150061093 (“Kim”) is titled Interposer and Semiconductor Package Using the Same, and Method of Manufacturing Interposer and lists Ki Hwan Kim, Jung Hyun Park, Yong Yoon Cho, Sung Won Jeong, Da Hee Kim, And Gi Ho Han as inventors. Kim anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Kim is a U.S. patent publication that was filed August 28, 2014 and published March 5, 2015. Kim claims priority to KR 10-2013-0104142 filed on August 30, 2013. Kim is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Kim, or otherwise rendered obvious by disclosures and teachings of Kim, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Kim does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Kim with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Kim, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

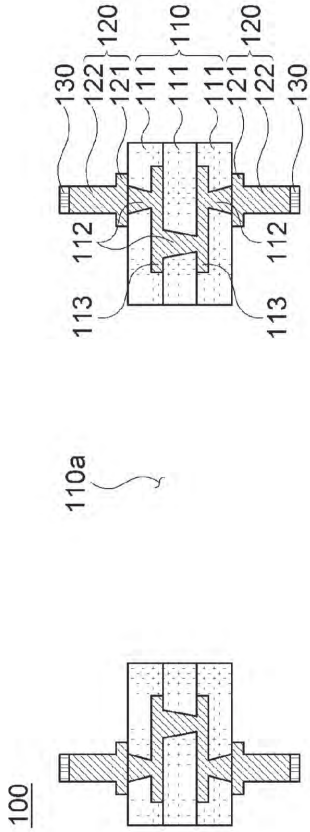
makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

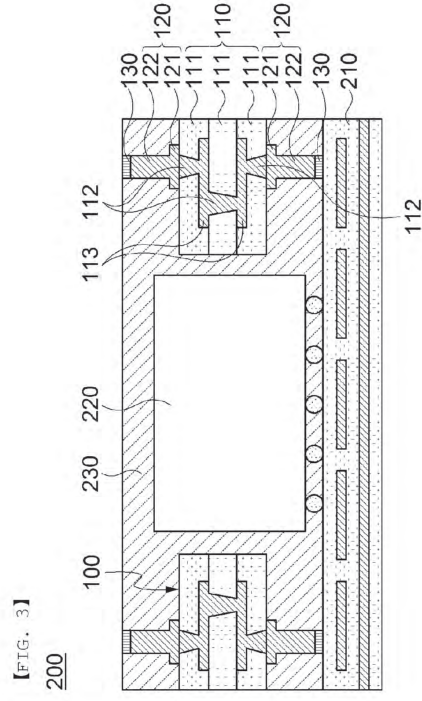
Where the chart below states that Kim “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Kim or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Kim set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Kim discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 1 to 3, an interposer 100 according to an exemplary embodiment of the present invention has as a basic structure an interposer substrate 110 having an upper surface and a lower surface facing the upper surface and a connection electrode 120 disposed on at least any one of an upper surface and a lower surface of the interposer substrate 110.” Kim, [0032].</p>

	<div><p>【FIG. 1】</p></div> <div></div> <div><p>Kim, FIG. 1</p></div> <div><p>“The interposer substrate 110 may be configured of an insulating layer 111 which is made of a rigid dielectric material, such as fiber reinforced bismaleimide triazine (BT), FR-4, glass, and ceramic, or a flexible dielectric material, such as epoxy resin, phenol resin, urethane resin, silicon resin, and polyimide resin, as a base material.” Kim, [0033].</p><p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p></div>
--	--



Kim, FIG. 3

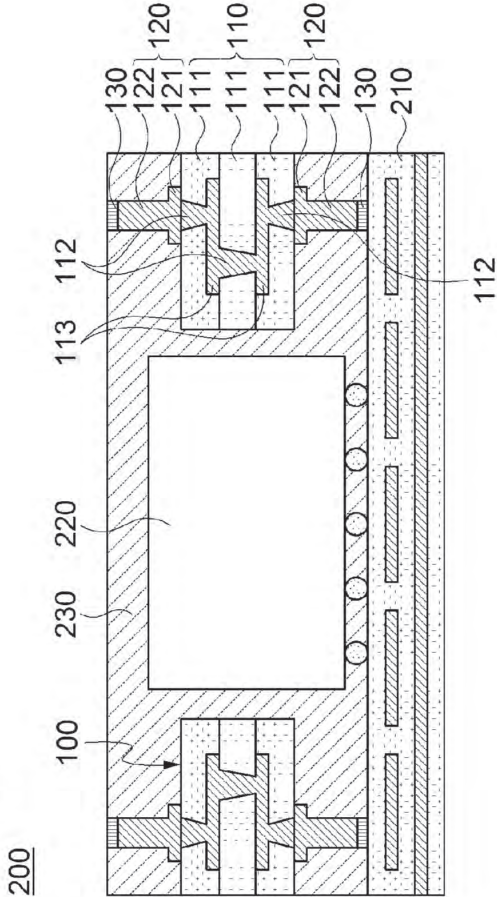
“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p>
[1.A] a bottom package substrate;	<p>Kim discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>

【FIG. 3】



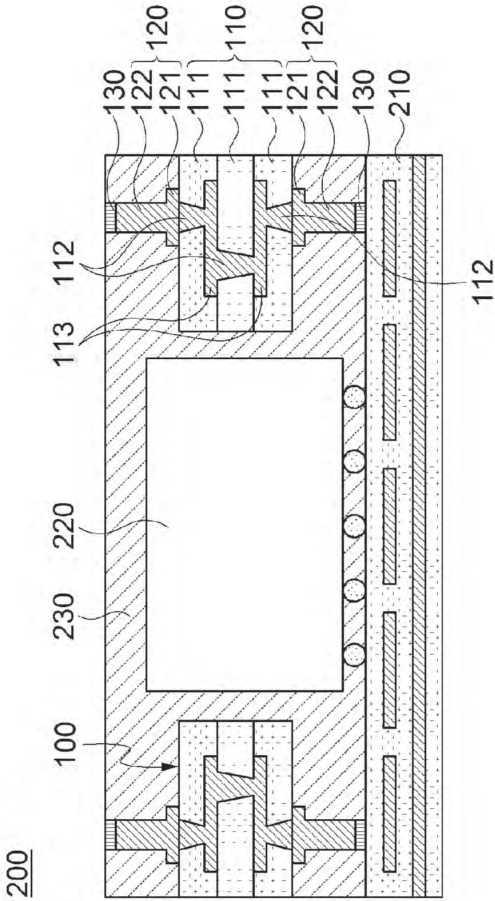
Kim, FIG. 3

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Kim discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>

【FIG. 3】

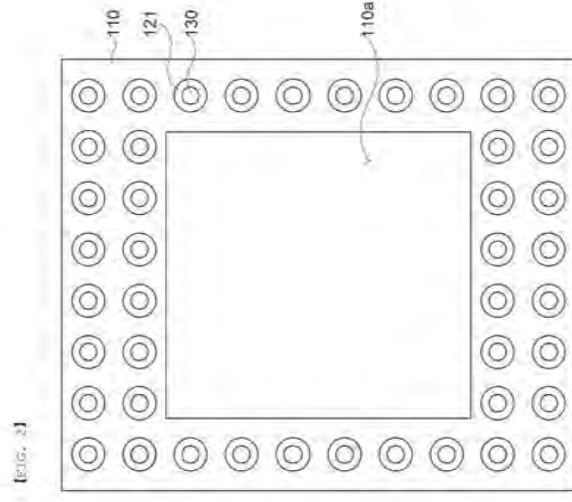


Kim, FIG. 3

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

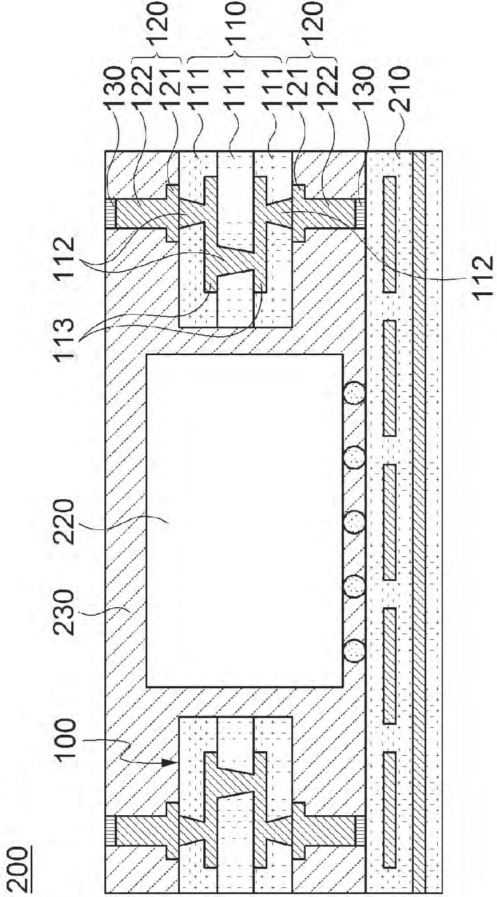
	<p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Kim discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 1 to 3, an interposer 100 according to an exemplary embodiment of the present invention has as a basic structure an interposer substrate 110 having an upper surface and a lower surface facing the upper surface and a connection electrode 120 disposed on at least any one of an upper surface and a lower surface of the interposer substrate 110.” Kim, [0032].</p>



Kim, FIG. 2

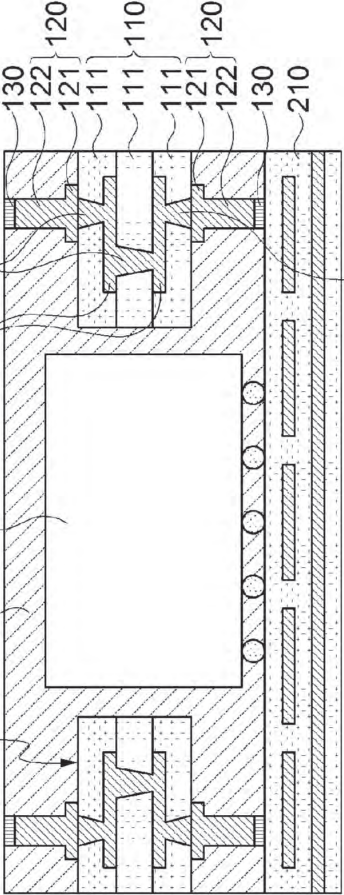
“The interposer substrate 110 may be configured of an insulating layer 111 which is made of a rigid dielectric material, such as fiber reinforced bismaleimide triazine (BT), FR-4, glass, and ceramic, or a flexible dielectric material, such as epoxy resin, phenol resin, urethane resin, silicon resin, and polyimide resin, as a base material.” Kim, [0033].

“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the

	<p>vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p> <p>【FIG. 3】</p>  <p>Kim, FIG. 3</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Kim discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 may be configured of an insulating layer 111 which is made of a rigid dielectric material, such as fiber reinforced bismaleimide triazine (BT), FR-4, glass, and ceramic, or a flexible dielectric material, such as epoxy resin, phenol resin, urethane resin, silicon resin, and polyimide resin, as a base material.” Kim, [0033].</p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>
--	--

	<p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p> <div><p>【FIG. 3】</p><p><u>200</u></p><p>Kim, FIG. 3</p></div> <p>“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings</p>
--	--

	<p>illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].</p> <p>“The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110. The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110.” Kim, [0037-0038].</p> <p>“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].</p> <p>“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the</p>
--	---

	<p>interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200.” Kim, [0039].</p>
--	---

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>“As a result, the wasted material may be reduced due to the stacking of a multi-layer insulating layer, thereby saving the manufacturing cost and the number of processes of stacking the insulating layer is reduced, thereby shortening the manufacturing time and greatly increasing the production efficiency.” Kim, [0040].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Kim discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

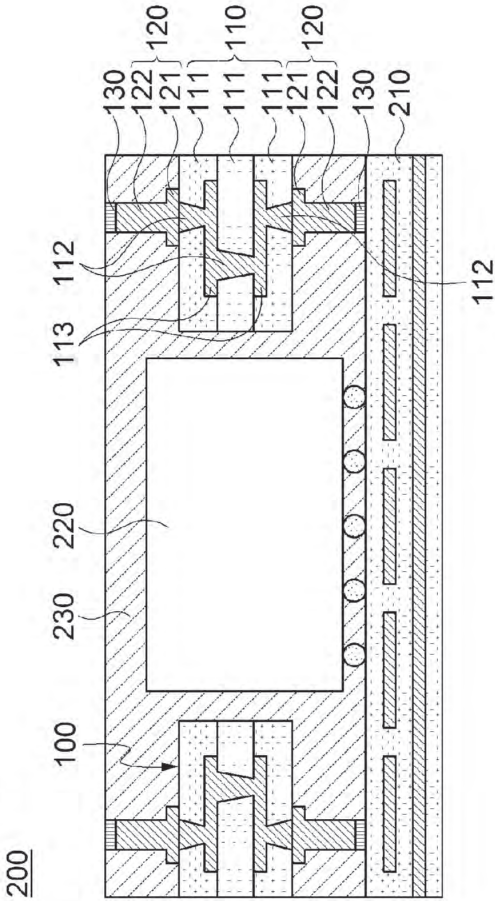
	<p>FIG. 3</p> <p>Kim, FIG. 3</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Kim discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, e.g.:</p>

	<p>FIG. 3</p> <p>Kim, FIG. 3</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the</p>	<p>Kim discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

plurality of metal pillars of the spacer connector,	<p>“Referring to FIGS. 1 to 3, an interposer 100 according to an exemplary embodiment of the present invention has as a basic structure an interposer substrate 110 having an upper surface and a lower surface facing the upper surface and a connection electrode 120 disposed on at least any one of an upper surface and a lower surface of the interposer substrate 110.” Kim, [0032].</p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>
---	---

【FIG. 3】



Kim, FIG. 3

“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ag, Pd, Au, Ti, Cr, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the</p>	<p>Kim discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

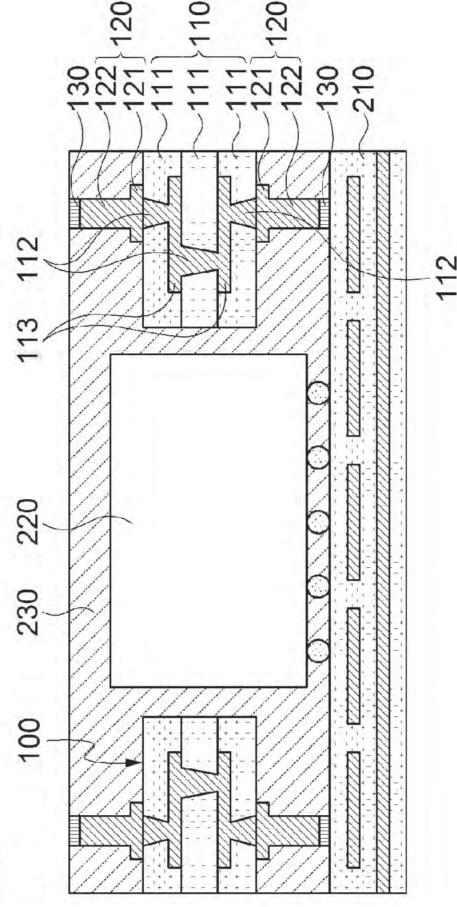
plurality of metal pillars of the spacer connector, and

See, e.g.:

“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].

【FIG. 3】

200

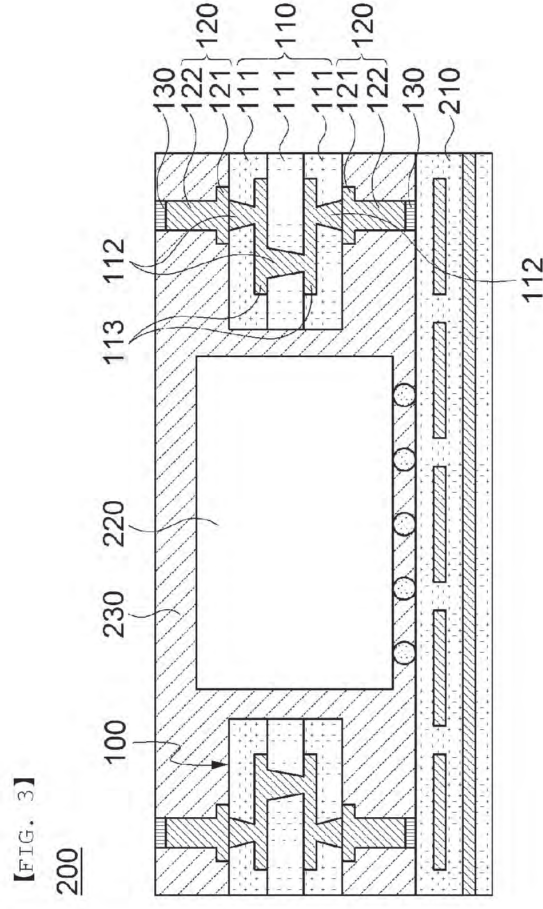


Kim, FIG. 3

	<p>“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].</p> <p>“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p>
--	---

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Kim discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIGS. 1 to 3, an interposer 100 according to an exemplary embodiment of the present invention has as a basic structure an interposer substrate 110 having an upper surface and a lower surface facing the upper surface and a connection electrode 120 disposed on at least any one of an upper surface and a lower surface of the interposer substrate 110.” Kim, [0032].</p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>



Kim, FIG. 3

“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the

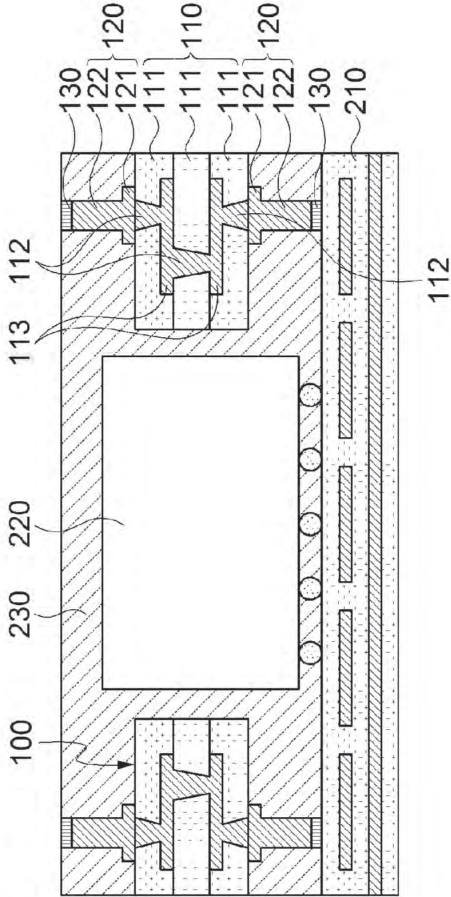
Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Kim discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>

“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].

【FIG. 3】

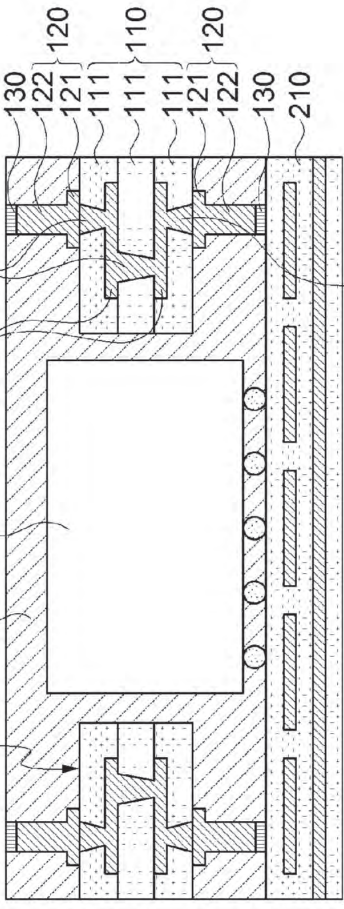
200



Kim, FIG. 3

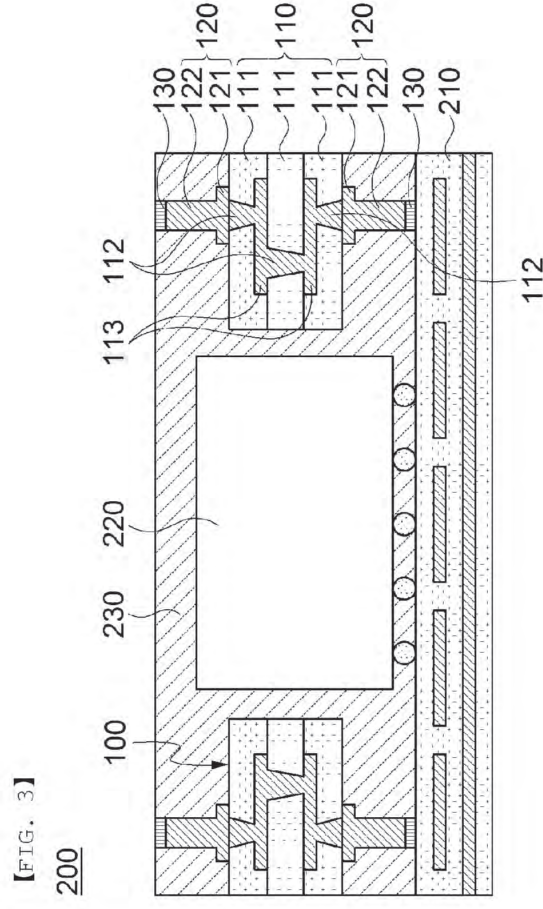
Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Kim discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at</p>

	<p>different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p> <div><p>【FIG. 3】</p><p>200</p><p>Kim, FIG. 3</p></div> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer</p>
--	---

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Kim discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>



Kim, FIG. 3

“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

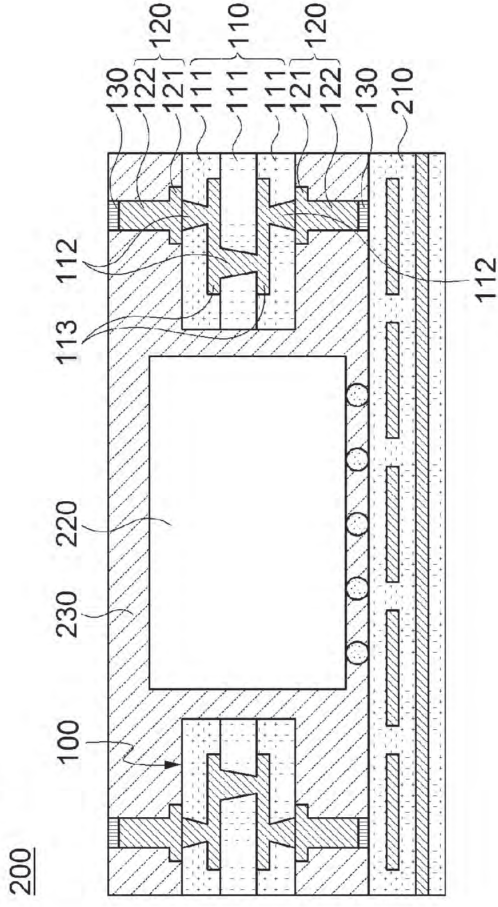
Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Kim discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>
---	--

【FIG. 3】



Kim, FIG. 3

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110.” Kim, [0038].

“In more detail, the semiconductor device 220 is mounted at a side at which the interposer substrate 110 is disposed and thus may be disposed to be inserted into the cavity 110a of the interposer substrate 110. Therefore, the thickness of the interposer 100 including the

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

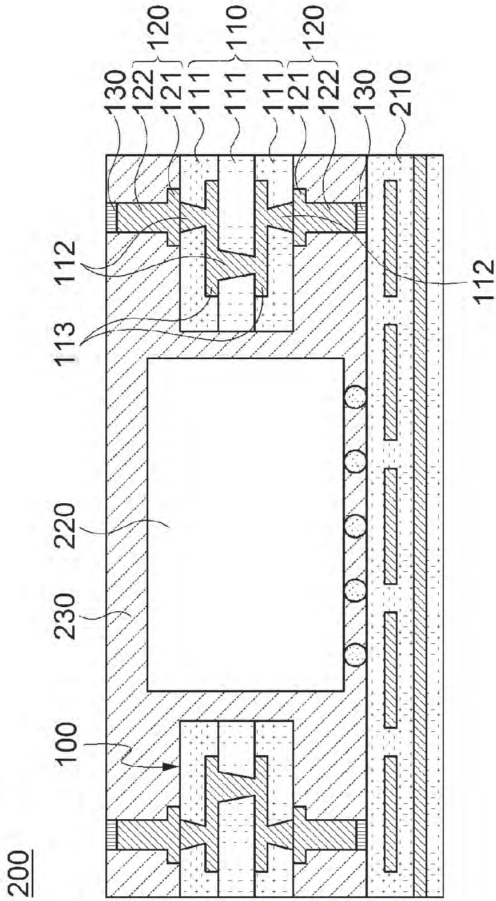
	<p>connection electrode 120 is formed to be larger than that of the mounted semiconductor device 220.” Kim, [0060].</p> <p>“another package substrate on which the semiconductor device is mounted may be connected on the semiconductor package 200 (in detail, on the interposer substrate 110 at an opposite side to the package substrate 210) having the above-mentioned structure by the connection electrode 120, such that the semiconductor package 200 according to the exemplary embodiment of the present invention may also be manufactured to have a package-on-package (PoP) structure.” Kim, [0062].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	Kim discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors. <i>See, e.g.:</i>

overlaps the bottom chip and each of the two spacer connectors.

【FIG. 3】



Kim, FIG. 3

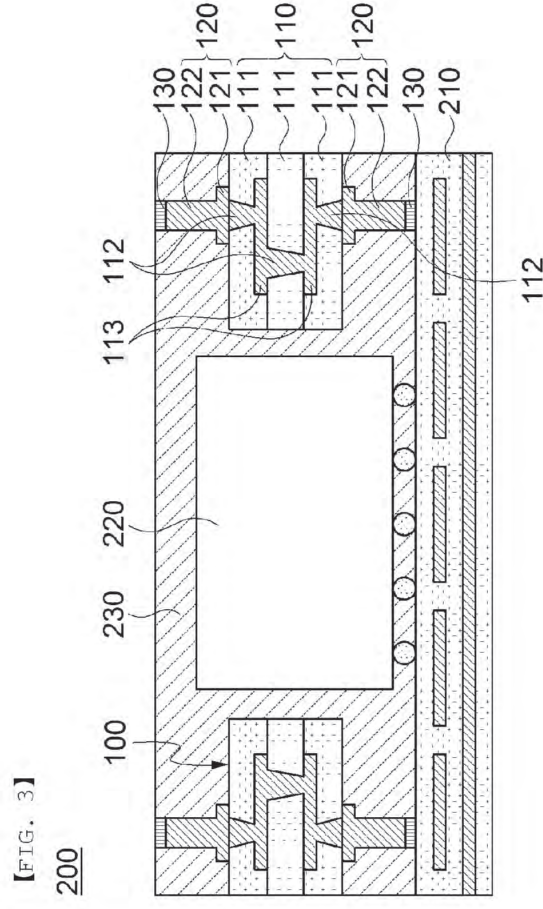
To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Kim discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 may be configured of an insulating layer 111 which is made of a rigid dielectric material, such as fiber reinforced bismaleimide triazine (BT), FR-4, glass, and ceramic, or a flexible dielectric material, such as epoxy resin, phenol resin, urethane resin, silicon resin, and polyimide resin, as a base material.” Kim, [0033].</p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>
--	--



Kim, FIG. 3

“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].

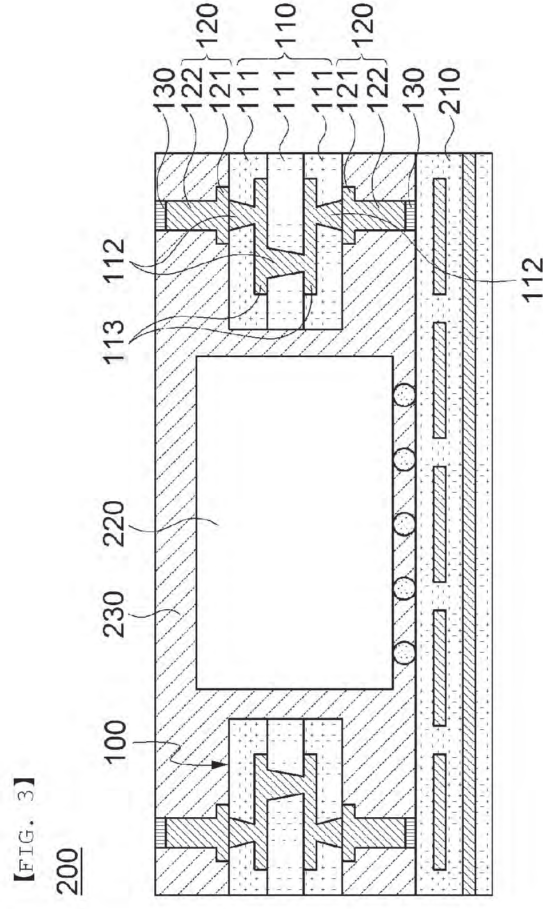
To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>	<p>Kim discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>



Kim, FIG. 3

“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

	<p>connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

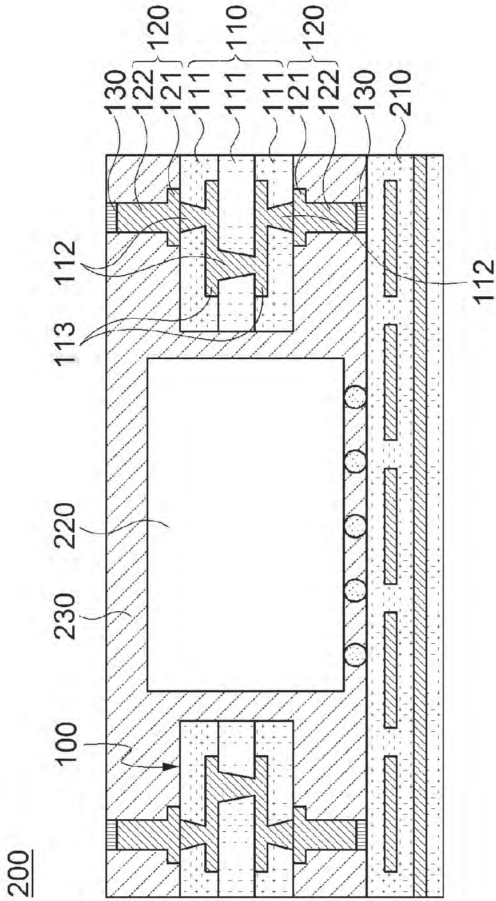
Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-17 - Invalidity of U.S. Patent No. 9859202 in view of Kim - U.S. Patent Publication No. 20150061093

<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Kim discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The interposer substrate 110 is interlayer connected through the vias 112 through which the insulating layers 111 of each layer penetrate, such that one point on an upper portion of the interposer substrate 110 may be internally conducted to one point on a lower portion thereof. In this configuration, the vias 112 of each layer may have a stack via structure in which the vias are straightly connected to each other. Alternatively, the vias 112 may be formed at different positions for each layer and may also be connected to each other through metal wirings 113 formed on each insulating layer 111.” Kim, [0035].</p>
--	---

【FIG. 3】



Kim, FIG. 3

“As described above, the remaining portion of the interposer substrate 110 on which the cavity 110 a is formed may be provided with the connection electrode 120. The drawings illustrate the connection electrodes 120 are disposed on both of the upper and lower surfaces of the interposer substrate 110, but unlike the drawings, the connection electrode 120 may be disposed on any one of the upper and lower surfaces of the interposer substrate 110.” Kim, [0037].

“The connection electrode 120 may receive or transmit electrical signals from the outside, such that at the time of the configuration of the semiconductor package 200 using the interposer 100 according to the exemplary embodiment of the present invention, the

	<p>connection electrode 120 may serve to electrically connect between the interposer substrate 110 and package substrates 210 which are disposed on the upper and lower portions of the interposer substrate 110. Therefore, the connection electrode 120 may be made of any one metal material of Ni, Al, Fe, Cu, Ti, Cr, Au, Ag, Pd, and Pt having excellent electrical conductivity and the number of connection electrodes 120 may be configured in plural, depending on the number of input/output terminals (I/O).” Kim, [0038].</p> <p>“The connection electrode 120 may be configured to include a post part 122 having a pillar shape and a pad part 121 which is disposed between the post part 122 and the interposer substrate 110 to strengthen connection reliability between the vias 112, in which a height of the post part 122 may be controlled corresponding to the thickness of the semiconductor device 220 included in the cavity 110 a at the time of the configuration of the semiconductor package 200. That is, the related art controls the thickness of the interposer depending on the number of layers of the insulating layer forming the interposer substrate, but the interposer 100 according to the exemplary embodiment of the present invention may be set to the required thickness by controlling a height of the connection electrode 120, in detail, the height of the post part 122 which is a component of the connection electrode 120.” Kim, [0039].</p> <p>To the extent Plaintiff contends that Kim fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

U.S. Patent Publication No. 20140054773 (“Kurashima”) is titled ELECTRONIC COMPONENT BUILT-IN SUBSTRATE AND METHOD OF MANUFACTURING THE SAME and lists Nobuyuki Kurashima, Tetsuya Koyama, Hajime Hzuka, And Koichi Tanaka as inventors. Kurashima anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Kurashima is a U.S. patent publication that was filed July 17, 2013 and published February 27, 2014. Kurashima claims priority to a JP 2012-186065 filed on August 27, 2012. Kurashima is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Kurashima, or otherwise rendered obvious by disclosures and teachings of Kurashima, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Kurashima does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Kurashima with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Kurashima, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Kurashima “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Kurashima or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Kurashima set forth in this chart.

Claim 1, U.S. Patent No. 9859202

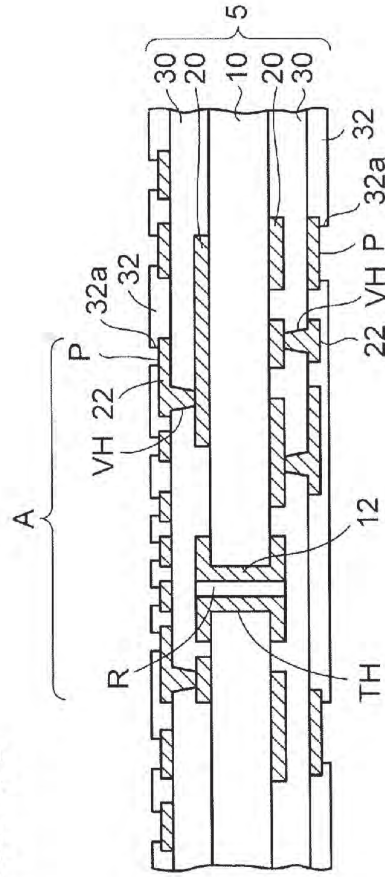
Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Kurashima discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 4A to FIG. 10 are views for explaining a method of manufacturing an electronic component built-in substrate according to an embodiment, and FIG. 11 is a view depicting an electronic component built-in substrate according to an embodiment. In a method of manufacturing an electronic component built-in substrate according to an embodiment, as depicted in FIG. 4A, a lower wiring substrate 5 is prepared. In the lower wiring substrate 5, a core substrate 10 is arranged in the center part in the thickness direction. The core substrate</p>

	<p>10 is formed of insulating material such as a glass epoxy resin, or the like, for example.” Kurashima, [0039-0040].</p> <p style="text-align: center;">FIG. 7B</p> <p style="text-align: center;">Kurashima, FIG. 7B</p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually. In this way, the upper</p>
--	--

	<p>wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6. With the above, a stacked wiring substrate in which the upper wiring substrate 7 is stacked on the lower wiring substrate 5 via the intermediate wiring substrate 6 is obtained. As described above, the first and second connection pads P1, P2 on both surface sides of the intermediate wiring substrate 6 are arranged in the displaced positions mutually. Therefore, the first and second solder balls 28, 29 arranged on the lower and upper sides of the intermediate wiring substrate 6 are also arranged in the displaced positions mutually to correspond to the above displaced positions. Moreover, in the present embodiment, the first and second solder balls 28, 29 arranged on the lower and upper sides of the intermediate wiring substrate 6 are arranged to be displaced in the positions that are not mutually overlapped when viewed from the top, to correspond to the first and second connection pads P1, P2 in FIG. 5B.” Kurashima, [0074-0078].</p> <p>“In the present embodiment, the intermediate wiring substrate 6 is interposed between the lower wiring substrate 5 and the upper wiring substrate 7. Therefore, it is unnecessary to set diameters of the first and second solder balls 28, 29 larger than heights of the semiconductor chip 40 and the chip capacitor 50.” Kurashima, [0079].</p>
[1.A] a bottom package substrate;	<p>Kurashima discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In a method of manufacturing an electronic component built-in substrate according to an embodiment, as depicted in FIG. 4A, a lower wiring substrate 5 is prepared. In the lower wiring substrate 5, a core substrate 10 is arranged in the center part in the thickness direction.</p>

	<p>The core substrate 10 is formed of insulating material such as a glass epoxy resin, or the like, for example. A first wiring layer 20 made of copper, or the like is formed on both surface sides of the core substrate 10 respectively. Through holes TH each penetrating through in the thickness direction are provided in the core substrate 10. The first wiring layer 20 on both surface sides is mutually connected via a through-hole plating layer 12 which is formed on an inner wall of the through hole TH. A resin R is filled in a remaining hole of the through hole TH. Alternatively, the penetrating electrode may be formed by filling the through hole TH of the core substrate 10 with a metal, thereby the first wiring layers 20 on both surface sides may be mutually connected via the penetrating electrode. An interlayer insulating layer 30 covering the first wiring layer 20 is formed on both surface sides of the core substrate 10 respectively. The interlayer insulating layer 30 is formed of an epoxy resin, a polyimide resin, or the like. Via holes VH each reaching the connection part of the first wiring layer 20 are formed in the interlayer insulating layer 30 on both surface sides respectively. Further, second wiring layers 22 each connected to the first wiring layer 20 via a via conductor which is filled in the via hole VH, are formed on the interlayer insulating layer 30 on both surface sides respectively. Also, a solder resist 32 in which opening portions 32 a are provided on connection pads P of the second wiring layers 22 is formed on the interlayer insulating layer 30 and the second wiring layers 22 on both surface sides of the core substrate 10 respectively.” Kurashima, [0040-0045].</p>
--	---

FIG. 4A



Kurashima, FIG. 4A

“In the case that the large size lower wiring substrate 5 for the purpose of multiple production is used, a plurality of product areas are demarcated on the substrate. In FIG. 4A, one product area of the lower wiring substrate 5 is depicted, and a component mounting area A is demarcated in its center part.” Kurashima, [0046].

“Then, as depicted in FIG. 4B, a semiconductor chip 40 which has bump electrodes 42 on the element forming face side is prepared. Then, the bump electrodes 42 of the semiconductor chip 40 are flip-chip connected to the connection pads P of the second wiring layers 22 in the

	<p>component mounting area A of the lower wiring substrate 5. After this, an underfill resin 44 is filled into a clearance located under the semiconductor chip 40. Further, similarly as depicted in FIG. 4B, a chip capacitor 50 is prepared. Then, the chip capacitor 50 is adhered onto the solder resist 32, which is located to the lateral direction of the semiconductor chip 40, on the upper surface side of the lower wiring substrate 5. The chip capacitor 50 has a connection terminal 52 on both end sides of the lateral direction. The connection terminals 52 located to both end sides are arranged in the parallel direction with the surface of the lower wiring substrate 5. Further, the connection terminal 52 on both end sides of the chip capacitor 50 is electrically connected to the connection pads P of the second wiring layers 22 by a solder layer 54 respectively. In this manner, the semiconductor chip 40 and the chip capacitor 50 are mounted side by side in the component mounting area A on the upper surface side of the lower wiring substrate 5.” Kurashima, [0048-0051].</p> <p>“Then, as depicted in FIG. 6B, the first solder balls 28 on the lower surface side of the intermediate wiring substrate 6 in FIG. 6A are arranged on the connection pads P on the upper surface side of the above lower wiring substrate 5 in FIG. 4B, and then the reflow heating is applied. By this matter, the first solder balls 28 of the intermediate wiring substrate 6 are joined to the connection pads P of the lower wiring substrate 5, and thus both members are electrically connected mutually.” Kurashima, [0065].</p> <p>“Further, an external connection terminal 14 is provided onto the connection pads P on the lower surface side of the lower wiring substrate 5 respectively by mounting the solder ball, or the like.” Kurashima, [0106].</p> <p>“As depicted in FIG. 11, in the electronic component built-in substrate 1 according to the embodiment, the bump electrodes 42 of the semiconductor chip 40 are flip-chip connected to the connection pads P in the component mounting area A of the lower wiring substrate 5</p>
--	---

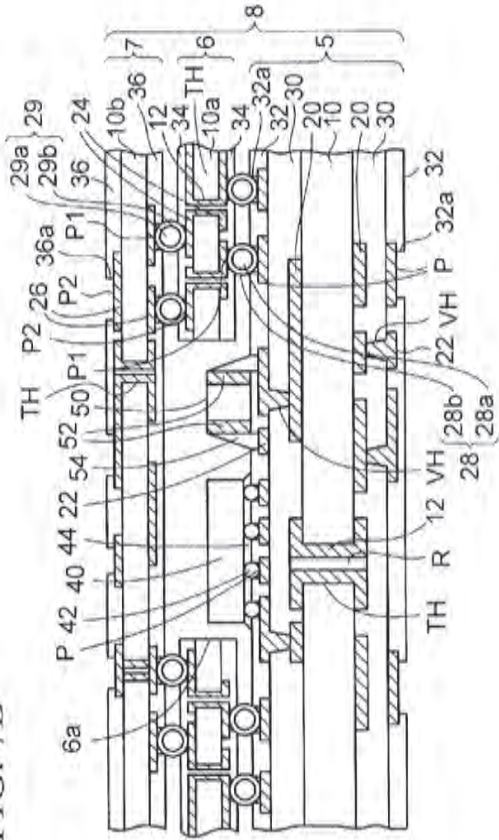
Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>explained in FIG. 4A. The underfill resin 44 is filled into a clearance under the semiconductor chip 40. The chip capacitor 50 having the connection terminal 52 on both end sides is adhered onto the solder resist 32 of the lower wiring substrate 5 in the lateral direction of the semiconductor chip 40. The connection terminals 52 on both end sides of the chip capacitor 50 are connected to the connection pads P of the lower wiring substrate 5 via the solder layer 54. The intermediate wiring substrate 6 shaped like a frame and explained in FIGS. 5A to 5C is arranged in the periphery of the semiconductor chip and the chip capacitor 50. The intermediate wiring substrate 6 has the opening portion 6 a, which penetrates from the upper surface to the lower surface, in the center part, and the semiconductor chip 40 and the chip capacitor 50 are mounted in this opening portion 6 a. The first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 are electrically connected to the connection pads P of the lower wiring substrate 5 via the first solder ball 28.” Kurashima, [0108-0112].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Kurashima discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In a method of manufacturing an electronic component built-in substrate according to the preliminary matter, as depicted in FIG. 1, first, bump electrodes 220 of a semiconductor chip 200 are flip-chip connected to connection pads (not shown) of a lower wiring substrate 100.</p>

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>Then, an underfill resin 240 is filled into a clearance located to the lower side of the semiconductor chip 200. Then, an upper wiring substrate 300 is electrically connected to the lower wiring substrate 100 via solder balls 320.” Kurashima, [0025-0026].</p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P 2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P 2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually.” Kurashima, [0073-0075].</p> <p>“In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6. With the above, a stacked wiring substrate in which the upper wiring substrate 7 is stacked on the lower wiring substrate 5 via the intermediate wiring substrate 6 is obtained.” Kurashima, [0075-0076].</p>
--	---

FIG. 7B



Kurashima, FIG. 7B

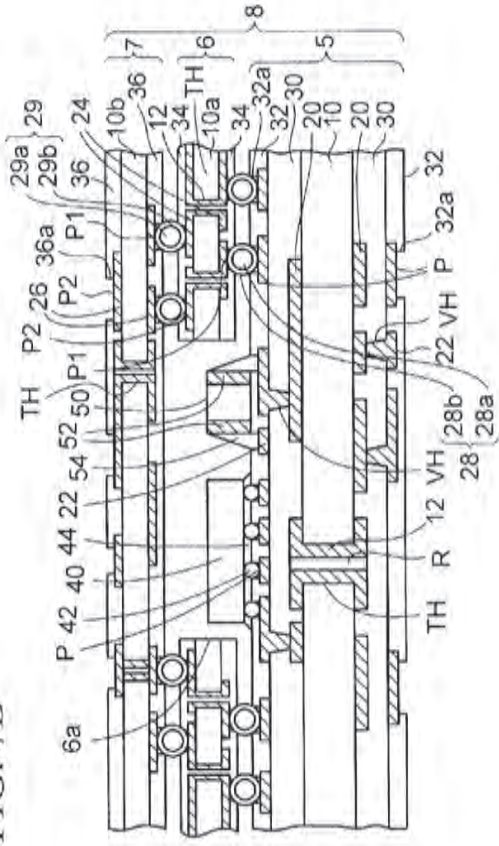
“Then, as depicted in FIG. 8, a molding resin 38 is filled into respective areas between the lower wiring substrate 5, the intermediate wiring substrate 6, and the upper wiring substrate 7 of the stacked wiring substrate 8 in FIG. 7B.” Kurashima, [0090].

“Also, the upper wiring substrate 7 is arranged over the semiconductor chip 40, the chip capacitor 50, and the intermediate wiring substrate 6. The second connection pads P 2 on the upper surface side of the intermediate wiring substrate 6 are electrically connected to the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 via the second solder balls 29. Further, the molding resin 38 sealing the semiconductor chip 40 and the chip

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>capacitor 50 is filled into respective areas between the lower wiring substrate 5, the intermediate wiring substrate 6, and the upper wiring substrate 7.” Kurashima, [0100-0101].</p> <p>“In the electronic component built-in substrate 1 of the present embodiment, by interposing the intermediate wiring substrate 6 between the lower wiring substrate 5 and the upper wiring substrate 7, the respective diameters of the first and second solder balls 28, 29 can be made small.” Kurashima, [0116].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Kurashima discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“The intermediate wiring substrate 6 has a frame-like structure in which an opening portion 6a penetrating from the upper surface to the lower surface is provided in the center part. The opening portion 6a of the intermediate wiring substrate 6 corresponds to the above component mounting area A of the lower wiring substrate 5, and the area of this opening portion 6a is set one size larger than the area of the component mounting area A.” Kurashima, [0053].</p>

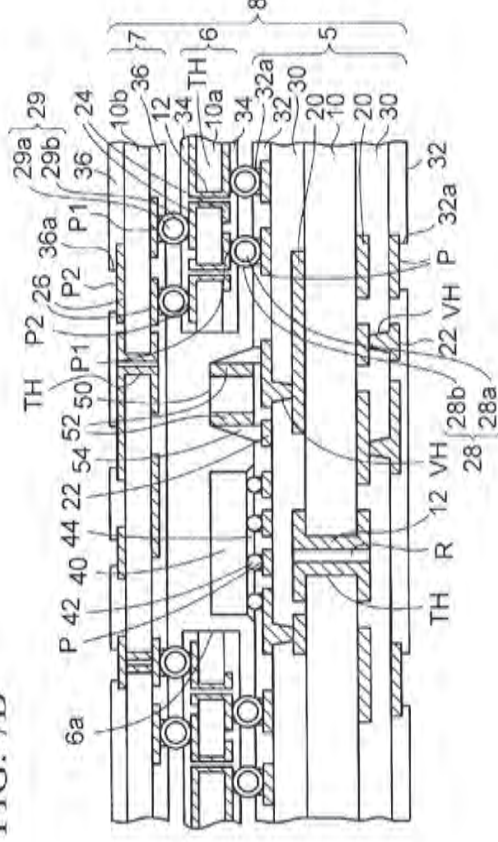
	<p>“Then, as depicted in FIG. 6B, the first solder balls 28 on the lower surface side of the intermediate wiring substrate 6 in FIG. 6A are arranged on the connection pads P on the upper surface side of the above lower wiring substrate 5 in FIG. 4B, and then the reflow heating is applied. By this matter, the first solder balls 28 of the intermediate wiring substrate 6 are joined to the connection pads P of the lower wiring substrate 5, and thus both members are electrically connected mutually. Consequently, it is in a state that the semiconductor chip 40 and the chip capacitor 50 are mounted in the opening portion 6 a of the intermediate wiring substrate 6.” Kurashima, [0065-0066].</p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P 2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P 2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually. In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6. With the above, a stacked wiring substrate in which the upper wiring substrate 7 is stacked on the lower wiring substrate 5 via the intermediate wiring substrate 6 is obtained.” Kurashima, [0073-0076].</p> <p>“In the present embodiment, the intermediate wiring substrate 6 is interposed between the lower wiring substrate 5 and the upper wiring substrate 7. Therefore, it is unnecessary to set diameters of the first and second solder balls 28, 29 larger than heights of the semiconductor chip 40 and the chip capacitor 50. For example, in the case that respective heights of the semiconductor chip 40 including the bump electrodes 42 and the chip capacitor 50 are 300</p>
--	---

	<p>μm, a thickness of the intermediate wiring substrate 6 is set to about 150 μm and diameters of the first and second solder balls 28, 29 arranged on the lower and upper sides of this intermediate wiring substrate 6 can be set to about 100 μm.” Kurashima, [0079-0080].</p> <p>FIG. 7B</p>  <p>Kurashima, FIG. 7B</p> <p>“As depicted in FIG. 11, in the electronic component built-in substrate 1 according to the embodiment, the bump electrodes 42 of the semiconductor chip 40 are flip-chip connected to the connection pads P in the component mounting area A of the lower wiring substrate 5</p>
--	---

	<p>explained in FIG. 4A. The underfill resin 44 is filled into a clearance under the semiconductor chip 40. The chip capacitor 50 having the connection terminal 52 on both end sides is adhered onto the solder resist 32 of the lower wiring substrate 5 in the lateral direction of the semiconductor chip 40. The connection terminals 52 on both end sides of the chip capacitor 50 are connected to the connection pads P of the lower wiring substrate 5 via the solder layer 54. The intermediate wiring substrate 6 shaped like a frame and explained in FIGS. 5A to 5C is arranged in the periphery of the semiconductor chip and the chip capacitor 50. The intermediate wiring substrate 6 has the opening portion 6 a, which penetrates from the upper surface to the lower surface, in the center part, and the semiconductor chip 40 and the chip capacitor 50 are mounted in this opening portion 6 a.” Kurashima, [0109-0111].</p> <p>“Further, the molding resin 38 sealing the semiconductor chip 40 and the chip capacitor 50 is filled into respective areas between the lower wiring substrate 5, the intermediate wiring substrate 6, and the upper wiring substrate 7.” Kurashima, [0114].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Kurashima discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the lower wiring substrate 5, a core substrate 10 is arranged in the center part in the thickness direction. The core substrate 10 is formed of insulating material such as a glass epoxy resin, or the like, for example. A first wiring layer 20 made of copper, or the like is</p>

	<p>formed on both surface sides of the core substrate 10 respectively. Through holes TH each penetrating through in the thickness direction are provided in the core substrate 10. The first wiring layer 20 on both surface sides is mutually connected via a through-hole plating layer 12 which is formed on an inner wall of the through hole TH.” Kurashima, [0040-0042].</p> <p>“The intermediate wiring substrate 6 has a frame-like structure in which an opening portion 6 a penetrating from the upper surface to the lower surface is provided in the center part. The opening portion 6 a of the intermediate wiring substrate 6 corresponds to the above component mounting area A of the lower wiring substrate 5, and the area of this opening portion 6 a is set one size larger than the area of the component mounting area A. In the intermediate wiring substrate 6, a wiring layer 24 is formed on both surface sides of a core substrate 10 a.” Kurashima, [0053-0054].</p> <p>“Similarly to the above-mentioned lower wiring substrate 5, the wiring layers 24 on both surface sides of the core substrate 10 a may be mutually connected via the penetrating electrode formed in the through hole TH.” Kurashima, [0055].</p> <p>“Alternatively, the intermediate wiring substrate 6 may be formed as a coreless substrate that uses a polyimide tape, or the like as a base material and has flexibility.” Kurashima, [0057].</p> <p>“In the intermediate wiring substrate 6, a wiring layer 24 is formed on both surface sides of a core substrate 10 a. The core substrate 10 a is formed of insulating material such as a glass epoxy resin, or the like, for example. The through holes TH penetrating in the thickness direction are provided in the core substrate 10 a. The wiring layers 24 on both surface sides are mutually connected via the through-hole plating layer 12 formed on the inner wall of the through hole TH. The resin R is filled in remaining holes of the through holes TH.” Kurashima, [0068-0069].</p>
--	---

FIG. 7B



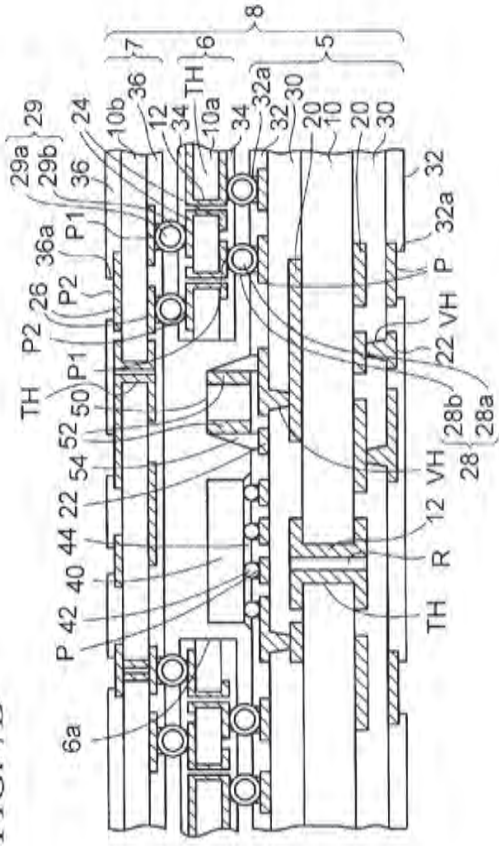
Kurashima, FIG. 7B

“In the upper wiring substrate 7, wiring layers 26 are formed on both surface sides of a core substrate 10 b respectively. The core substrate 10 b is formed of insulating material such as a glass epoxy resin, or the like, for example. The through holes TH penetrating in the thickness direction are provided in the core substrate 10 b. The wiring layers 26 on both surface sides are mutually connected via the through-hole plating layer 12 which is formed on the inner wall of the through hole TH. The resin R is filled in the remaining hole of the through hole TH.” Kurashima, [0068-0069].

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Kurashima discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“A first wiring layer 20 made of copper, or the like is formed on both surface sides of the core substrate 10 respectively. Through holes TH each penetrating through in the thickness direction are provided in the core substrate 10. The first wiring layer 20 on both surface sides is mutually connected via a through-hole plating layer 12 which is formed on an inner wall of the through hole TH.” Kurashima, [0041-0042].</p>

FIG. 7B



Kurashima, FIG. 7B

“Alternatively, the penetrating electrode may be formed by filling the through hole TH of the core substrate 10 with a metal, thereby the first wiring layers 20 on both surface sides may be mutually connected via the penetrating electrode.” Kurashima, [0042].

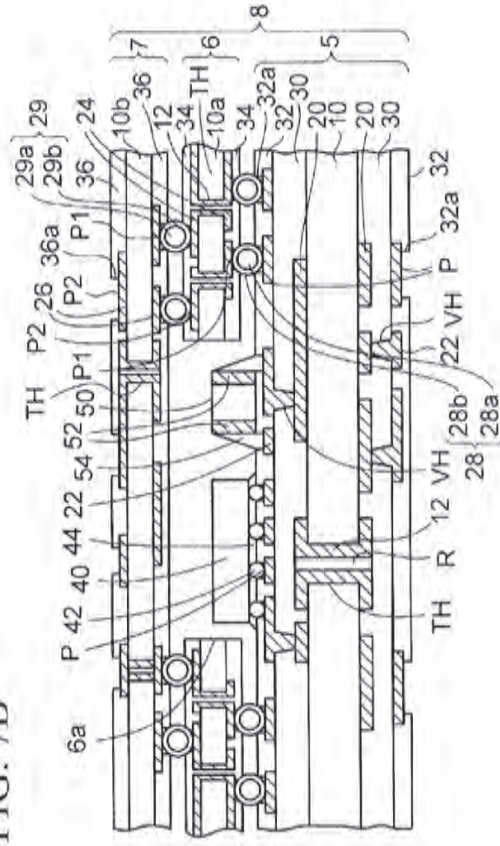
“The wiring layers 24 on both surface sides are mutually connected via the through-hole plating layer 12 formed on the inner wall of the through hole TH.” Kurashima, [0054].

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>“Similarly to the above-mentioned lower wiring substrate 5, the wiring layers 24 on both surface sides of the core substrate 10 a may be mutually connected via the penetrating electrode formed in the through hole TH.” Kurashima, [0055].</p> <p>“The wiring layers 26 on both surface sides are mutually connected via the through-hole plating layer 12 which is formed on the inner wall of the through hole TH.” Kurashima, [0069].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Kurashima discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“The wiring layers 24 on both surface sides are mutually connected via the through-hole plating layer 12 formed on the inner wall of the through hole TH.” Kurashima, [0054].</p> <p>“Then, as depicted in FIG. 6A, a first solder ball 28 is mounted on the first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 respectively. Then, the first solder balls 28 are joined to the first connection pads P 1 by applying the reflow heating.” Kurashima, [0061-0062].</p>

	<p>“The wiring layers 26 on both surface sides are mutually connected via the through-hole plating layer 12 which is formed on the inner wall of the through hole TH.” Kurashima, [0069].</p> <p>“A solder resist 36 in which opening portions 36 a are provided on the first connection pads P 1 of the wiring layers 26 is formed on the lower surface side of the core substrate 10 b. Similarly, the solder resist 36 in which the opening portions 36 a are provided on the second connection pads P 2 of the wiring layers 26 is formed on the upper surface side of the core substrate 10 b.” Kurashima, [0070-0072].</p> <p>“A solder resist 34 in which opening portions 34 a are provided on first connection pads P 1 of the wiring layer 24 is formed on the lower surface side of the core substrate 10 a. Similarly, the solder resist 34 in which the opening portions 34 a are provided on second connection pads P 2 of the wiring layer 24 is formed on the upper surface side of the core substrate 10 a.” Kurashima, [0071].</p>
--	--

FIG. 7B



Kurashima, FIG. 7B

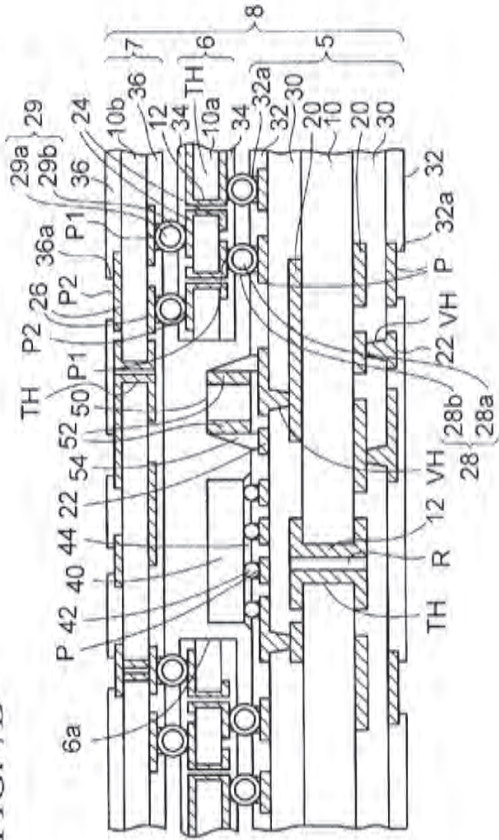
“Then, a second solder ball 29 is mounted on the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 respectively, and then the second solder balls 29 are joined to the first connection pads P 1 by applying the reflow heating.” Kurashima, [0072-0073].

To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Kurashima discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The first wiring layer 20 on both surface sides is mutually connected via a through-hole plating layer 12 which is formed on an inner wall of the through hole TH. A resin R is filled in a remaining hole of the through hole TH.” Kurashima, [0042].</p> <p>“Further, second wiring layers 22 each connected to the first wiring layer 20 via a via conductor which is filled in the via hole VH, are formed on the interlayer insulating layer 30 on both surface sides respectively.” Kurashima, [0044].</p> <p>“The through holes TH penetrating in the thickness direction are provided in the core substrate 10 a. The wiring layers 24 on both surface sides are mutually connected via the through-hole plating layer 12 formed on the inner wall of the through hole TH. The resin R is filled in remaining holes of the through holes TH.” Kurashima, [0054-0055].</p>
--	---

FIG. 7B



Kurashima, FIG. 7B

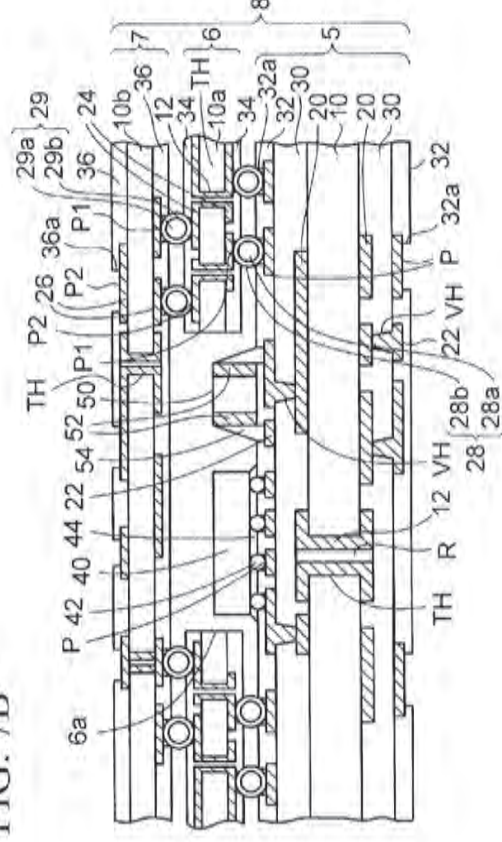
“The wiring layers 26 on both surface sides are mutually connected via the through-hole plating layer 12 which is formed on the inner wall of the through hole TH. The resin R is filled in the remaining hole of the through hole TH.” Kurashima, [0069].

“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P 2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied.” Kurashima, [0074].

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>“Then, as depicted in FIG. 6A, a first solder ball 28 is mounted on the first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 respectively.” Kurashima, [0085-0086].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Kurashima discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P 2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P 2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually. In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6.” Kurashima, [0064-0067].</p>

FIG. 7B



Kurashima, FIG. 7B

“A solder resist 34 in which opening portions 34 a are provided on first connection pads P 1 of the wiring layer 24 is formed on the lower surface side of the core substrate 10 a. Similarly, the solder resist 34 in which the opening portions 34 a are provided on second connection pads P 2 of the wiring layer 24 is formed on the upper surface side of the core substrate 10 a.” Kurashima, [0071].

“Then, a second solder ball 29 is mounted on the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 respectively, and then the second solder balls 29 are joined to the first connection pads P 1 by applying the reflow heating. Similarly to the

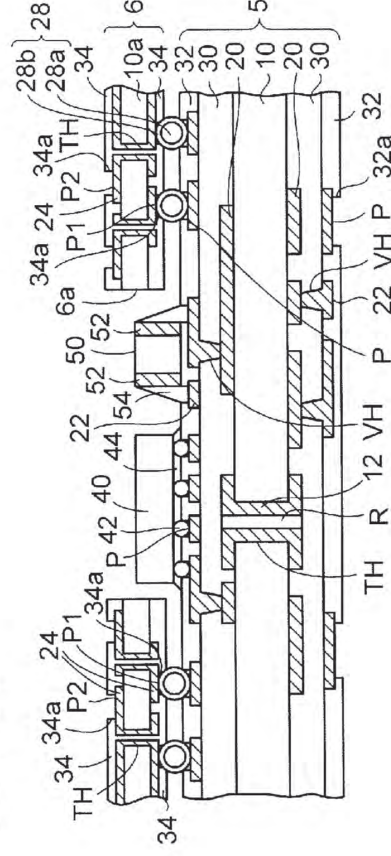
Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>above-mentioned first solder balls 28, preferably the second solder ball is formed by coating a solder layer 29 b on an outer face of a copper core ball 29 a.” Kurashima, [0072-0073].</p> <p>“The first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 are electrically connected to the connection pads P of the lower wiring substrate 5 via the first solder ball 28. Also, the upper wiring substrate 7 is arranged over the semiconductor chip 40, the chip capacitor 50, and the intermediate wiring substrate 6. The second connection pads P 2 on the upper surface side of the intermediate wiring substrate 6 are electrically connected to the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 via the second solder balls 29.” Kurashima, [0111-0114].</p> <p>“Also, the upper wiring substrate 7 is arranged over the semiconductor chip 40, the chip capacitor 50, and the intermediate wiring substrate 6. The second connection pads P 2 on the upper surface side of the intermediate wiring substrate 6 are electrically connected to the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 via the second solder balls 29.” Kurashima, [0112-0114].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the</p>	<p>Kurashima discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

plurality of metal pillars of the spacer connector, and	<p>“Then, as depicted in FIG. 6A, a first solder ball 28 is mounted on the first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 respectively. Then, the first solder balls 28 are joined to the first connection pads P 1 by applying the reflow heating. The first solder ball 28 is one example of the conductive balls. In FIG. 6A, as the preferred example, the first solder ball 28 is formed by coating a solder layer 28 b on an outer face of a copper core ball 28 a. Alternatively, as the solder ball, the ball which is formed by coating a solder layer on an outer face of a resin core ball may be used. Otherwise, in the case that no harm is caused even when an interval between the stacked substrates is slightly varied, a solder ball formed of the solder over the whole may be used as the solder ball. In this manner, as the example of the conductive ball, the solder ball at least an outer face of which is formed of the solder layer can be used. Then, as depicted in FIG. 6B, the first solder balls 28 on the lower surface side of the intermediate wiring substrate 6 in FIG. 6A are arranged on the connection pads P on the upper surface side of the above lower wiring substrate 5 in FIG. 4B, and then the reflow heating is applied. By this matter, the first solder balls 28 of the intermediate wiring substrate 6 are joined to the connection pads P of the lower wiring substrate 5, and thus both members are electrically connected mutually.” Kurashima, [0061-0065].</p>
---	---

FIG. 6B



Kurashima, FIG. 6B

“Also, in the example in FIG. 5B, the first connection pads P 1 and the second connection pads P 2 on the lower and upper surface sides are arranged in two lines respectively. But the number of arrangement can be set arbitrarily. Then, as depicted in FIG. 6A, a first solder ball 28 is mounted on the first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 respectively. Then, the first solder balls 28 are joined to the first connection pads P 1 by applying the reflow heating.” Kurashima, [0071-0073].

“In the present embodiment, by adjusting the thickness of the intermediate wiring substrate 6 with regard to the heights of the semiconductor chip and the chip capacitor 50, the first and

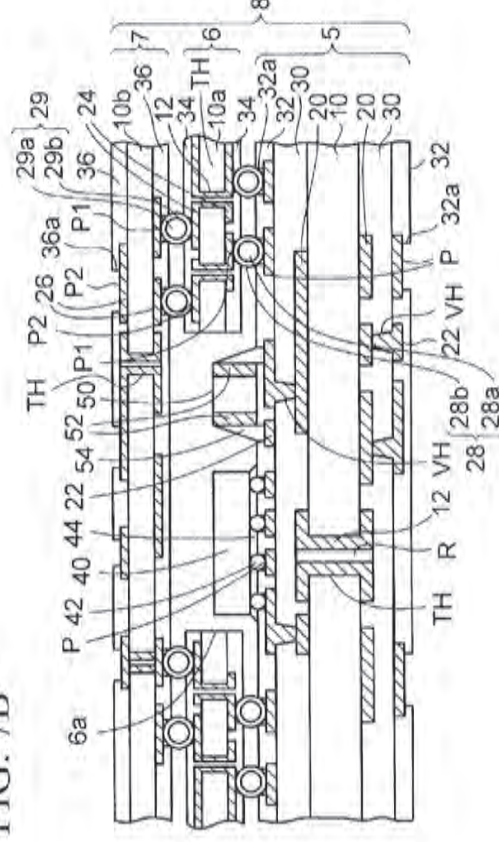
	<p>second solder balls 28, 29 whose diameters are fairly smaller than a height of the semiconductor chip 40 can be employed.” Kurashima, [0082].</p> <p>“Also, in the above steps in FIGS. 6A and 6B, the first solder balls 28 may be joined to the connection pads P on the upper surface side of the lower wiring substrate 5, and then the first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 may joined thereto.” Kurashima, [0087-0088].</p> <p>“The first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 are electrically connected to the connection pads P of the lower wiring substrate 5 via the first solder ball 28.” Kurashima, [0111-0112].</p> <p>“Further, the clauses are disclosed about the above embodiment hereinafter. (Clause 1) A method of manufacturing an electronic component built-in substrate, comprising: mounting an electronic component on a lower wiring substrate; obtaining a stacked wiring substrate having a structure that an intermediate wiring substrate in which an opening portion housing the electronic component is provided, is connected to the lower wiring substrate via a first conductive ball, and that an upper wiring substrate is connected to the intermediate wiring substrate via a second conductive ball; sealing the electronic component by filling a resin into respective areas between the lower wiring substrate, the intermediate wiring substrate, and the upper wiring substrate; and wherein the first conductive ball and the second conductive ball are arranged in displaced positions mutually. (Clause 2) A method of manufacturing an electronic component built-in substrate, according to clause 1, wherein the obtaining the stacked wiring substrate includes, connecting the intermediate wiring substrate to the lower wiring substrate via the first conductive ball, and connecting the upper wiring substrate to the intermediate wiring substrate via the second conductive ball. (Clause 3) A method of manufacturing an electronic component built-in substrate, according to clause 1,</p>
--	---

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>wherein the first conductive ball and second conductive ball are arranged in positions that are not overlapped mutually, when viewed from a top.(Clause 4) A method of manufacturing an electronic component built-in substrate, according to clause 1, wherein each diameter of the first conductive ball and the second conductive ball is set smaller than a height of the electronic component.(Clause 5) A method of manufacturing an electronic component built-in substrate, according to clause” Kurashima, [0121-0129].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Kurashima discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The wiring layers 24 on both surface sides are mutually connected via the through-hole plating layer 12 formed on the inner wall of the through hole TH.” Kurashima, [0054].</p> <p>“By this matter, the first solder balls 28 of the intermediate wiring substrate 6 are joined to the connection pads P of the lower wiring substrate 5, and thus both members are electrically connected mutually. Consequently, it is in a state that the semiconductor chip 40 and the chip capacitor 50 are mounted in the opening portion 6 a of the intermediate wiring substrate 6.” Kurashima, [0065-0066].</p>

	<p>“The through holes TH penetrating in the thickness direction are provided in the core substrate 10 a. The wiring layers 24 on both surface sides are mutually connected via the through-hole plating layer 12 formed on the inner wall of the through hole TH.” Kurashima, [0068-0069].</p> <p>“By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P 2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually.” Kurashima, [0074].</p> <p>“In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6.” Kurashima, [0075].</p>
--	--

FIG. 7B



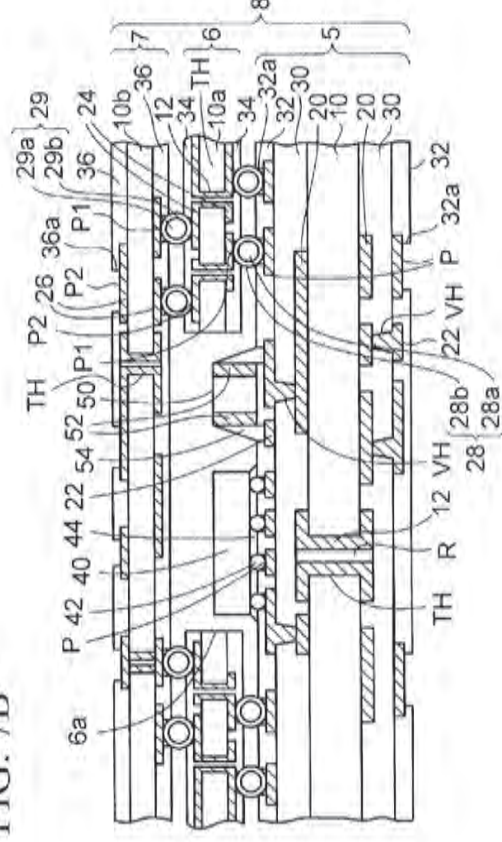
Kurashima, FIG. 7B

“The first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 are electrically connected to the connection pads P of the lower wiring substrate 5 via the first solder ball 28. Also, the upper wiring substrate 7 is arranged over the semiconductor chip 40, the chip capacitor 50, and the intermediate wiring substrate 6. The second connection pads P 2 on the upper surface side of the intermediate wiring substrate 6 are electrically connected to the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 via the second solder balls 29.” Kurashima, [0111-0114].

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Kurashima discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“By this matter, it is in a state that the semiconductor chip 200 is housed in an area between the lower wiring substrate 100 and the upper wiring substrate 300.” Kurashima, [0026].</p> <p>“Consequently, it is in a state that the semiconductor chip 40 and the chip capacitor 50 are mounted in the opening portion 6 a of the intermediate wiring substrate 6. Here, the intermediate wiring substrate 6 linked like a frame is illustrated. In this case, the intermediate wiring substrate 6 may be arranged around the semiconductor chip 40 and the chip capacitor 50 in a state that the intermediate wiring substrate 6 is divided into plural parts.” Kurashima, [0066-0067].</p>

FIG. 7B



Kurashima, FIG. 7B

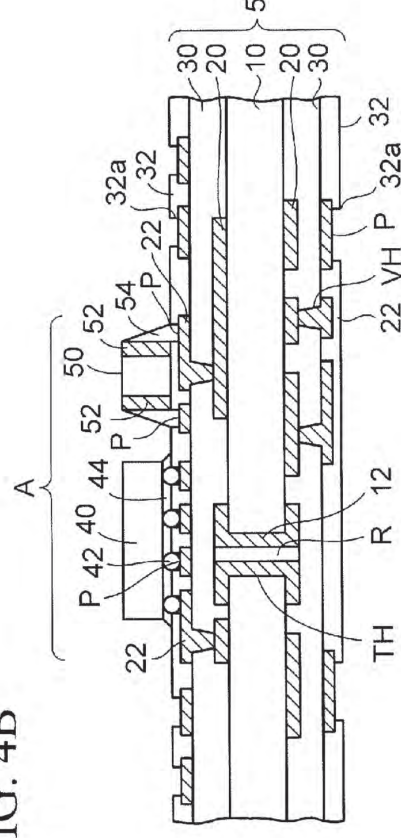
“In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6. With the above, a stacked wiring substrate in which the upper wiring substrate 7 is stacked on the lower wiring substrate 5 via the intermediate wiring substrate 6 is obtained.” Kurashima, [0075-0076].

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>“Then, as depicted in FIG. 8, a molding resin 38 is filled into respective areas between the lower wiring substrate 5, the intermediate wiring substrate 6, and the upper wiring substrate 7 of the stacked wiring substrate 8 in FIG. 7B.” Kurashima, [0090].</p> <p>“The intermediate wiring substrate 6 shaped like a frame and explained in FIGS. 5A to 5C is arranged in the periphery of the semiconductor chip and the chip capacitor 50. The intermediate wiring substrate 6 has the opening portion 6 a, which penetrates from the upper surface to the lower surface, in the center part, and the semiconductor chip 40 and the chip capacitor 50 are mounted in this opening portion 6 a. The first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 are electrically connected to the connection pads P of the lower wiring substrate 5 via the first solder ball 28. Also, the upper wiring substrate 7 is arranged over the semiconductor chip 40, the chip capacitor 50, and the intermediate wiring substrate 6.” Kurashima, [0110-0113].</p> <p>“Further, the molding resin 38 sealing the semiconductor chip 40 and the chip capacitor 50 is filled into respective areas between the lower wiring substrate 5, the intermediate wiring substrate 6, and the upper wiring substrate 7.” Kurashima, [0114].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and	<p>Kurashima discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<p>“In a method of manufacturing an electronic component built-in substrate according to an embodiment, as depicted in FIG. 4A, a lower wiring substrate 5 is prepared. In the lower wiring substrate 5, a core substrate 10 is arranged in the center part in the thickness direction. The core substrate 10 is formed of insulating material such as a glass epoxy resin, or the like, for example. A first wiring layer 20 made of copper, or the like is formed on both surface sides of the core substrate 10 respectively.” Kurashima, [0040-0041].</p> <p>“Then, as depicted in FIG. 4B, a semiconductor chip 40 which has bump electrodes 42 on the element forming face side is prepared. Then, the bump electrodes 42 of the semiconductor chip 40 are flip-chip connected to the connection pads P of the second wiring layers 22 in the component mounting area A of the lower wiring substrate 5.” Kurashima, [0048].</p>
--	--

FIG. 4B



Kurashima, FIG. 4B

“Further, similarly as depicted in FIG. 4B, a chip capacitor 50 is prepared. Then, the chip capacitor 50 is adhered onto the solder resist 32, which is located to the lateral direction of the semiconductor chip 40, on the upper surface side of the lower wiring substrate 5. The chip capacitor 50 has a connection terminal 52 on both end sides of the lateral direction. The connection terminals 52 located to both end sides are arranged in the parallel direction with the surface of the lower wiring substrate 5. Further, the connection terminal 52 on both end sides of the chip capacitor 50 is electrically connected to the connection pads P of the second wiring layers 22 by a solder layer 54 respectively. In this manner, the semiconductor chip 40

	<p>and the chip capacitor 50 are mounted side by side in the component mounting area A on the upper surface side of the lower wiring substrate 5.” Kurashima, [0049-0051].</p> <p>“Then, as depicted in FIG. 6B, the first solder balls 28 on the lower surface side of the intermediate wiring substrate 6 in FIG. 6A are arranged on the connection pads P on the upper surface side of the above lower wiring substrate 5 in FIG. 4B, and then the reflow heating is applied. By this matter, the first solder balls 28 of the intermediate wiring substrate 6 are joined to the connection pads P of the lower wiring substrate 5, and thus both members are electrically connected mutually. Consequently, it is in a state that the semiconductor chip 40 and the chip capacitor 50 are mounted in the opening portion 6 a of the intermediate wiring substrate 6.” Kurashima, [0065-0066].</p> <p>“As depicted in FIG. 11, in the electronic component built-in substrate 1 according to the embodiment, the bump electrodes 42 of the semiconductor chip 40 are flip-chip connected to the connection pads P in the component mounting area A of the lower wiring substrate 5 explained in FIG. 4A. The underfill resin 44 is filled into a clearance under the semiconductor chip 40. The chip capacitor 50 having the connection terminal 52 on both end sides is adhered onto the solder resist 32 of the lower wiring substrate 5 in the lateral direction of the semiconductor chip 40.” Kurashima, [0109-0110].</p> <p>“The intermediate wiring substrate 6 has the opening portion 6 a, which penetrates from the upper surface to the lower surface, in the center part, and the semiconductor chip 40 and the chip capacitor 50 are mounted in this opening portion 6 a. The first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 are electrically connected to the connection pads P of the lower wiring substrate 5 via the first solder ball 28.” Kurashima, [0111-0113].</p>
--	---

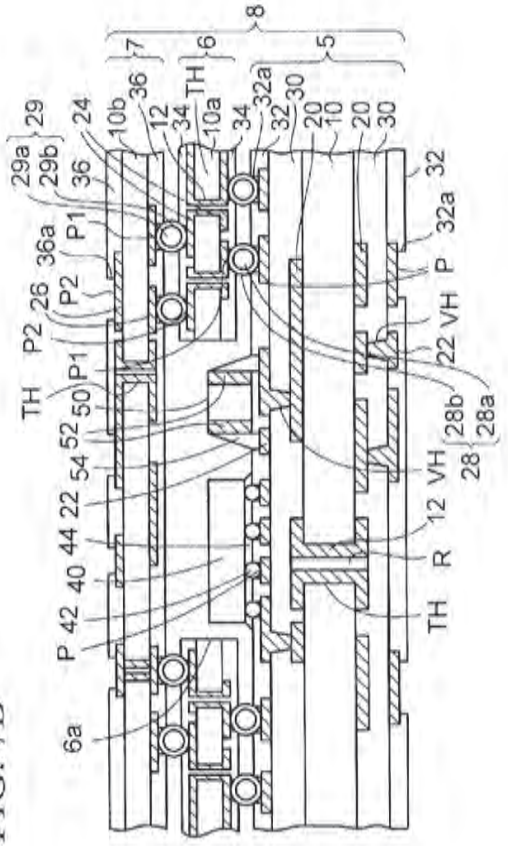
Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Kurashima discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“In this case, the intermediate wiring substrate 6 may be arranged around the semiconductor chip 40 and the chip capacitor 50 in a state that the intermediate wiring substrate 6 is divided into plural parts.” Kurashima, [0067].</p> <p>“Here, the intermediate wiring substrate 6 linked like a frame is illustrated. In this case, the intermediate wiring substrate 6 may be arranged around the semiconductor chip 40 and the chip capacitor 50 in a state that the intermediate wiring substrate 6 is divided into plural parts.” Kurashima, [0067].</p> <p>“Here, in the step of obtaining the above stacked wiring substrate 8, at first, in FIGS. 6A and 6B, the first solder balls 28 on the lower surface side of the intermediate wiring substrate 6 are connected to the connection pads P of the lower wiring substrate 5. After this, in FIGS. 7A and 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 are connected to the second connection pads P 2 of the intermediate wiring substrate 6. Besides this mode, at first, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are connected to the second connection pads P 2 of the intermediate wiring substrate 6 in FIG. 6A, and thus a stacked wiring member is obtained.</p>

	<p>After this, the first solder balls 28 on the lower surface side of the intermediate wiring substrate 6 of this stacked wiring member may be connected to the connection pads P of the lower wiring substrate 5. By employing this method, also the stacked wiring substrate 8 having the same structure as that in FIG. 7B can be obtained.” Kurashima, [0083-0086].</p> <p style="text-align: center;">FIG. 7B</p> <p style="text-align: center;">Kurashima, FIG. 7B</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Kurashima discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Consequently, it is in a state that the semiconductor chip 40 and the chip capacitor 50 are mounted in the opening portion 6 a of the intermediate wiring substrate 6. Here, the intermediate wiring substrate 6 linked like a frame is illustrated. In this case, the intermediate wiring substrate 6 may be arranged around the semiconductor chip 40 and the chip capacitor 50 in a state that the intermediate wiring substrate 6 is divided into plural parts.” Kurashima, [0066-0067].</p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P 2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P 2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually. In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6. With the above, a stacked wiring substrate in which the upper wiring substrate 7 is stacked on the</p>

	<p>lower wiring substrate 5 via the intermediate wiring substrate 6 is obtained.” Kurashima, [0073-0076].</p> <p>FIG. 7B</p>  <p>Kurashima, FIG. 7B</p> <p>“In the present embodiment, the intermediate wiring substrate 6 is interposed between the lower wiring substrate 5 and the upper wiring substrate 7. Therefore, it is unnecessary to set diameters of the first and second solder balls 28, 29 larger than heights of the semiconductor chip 40 and the chip capacitor 50. For example, in the case that respective heights of the semiconductor chip 40 including the bump electrodes 42 and the chip capacitor 50 are 300 μm, a thickness of the intermediate wiring substrate 6 is set to about 150 μm and diameters</p>
--	---

	<p>of the first and second solder balls 28, 29 arranged on the lower and upper sides of this intermediate wiring substrate 6 can be set to about 100 μm.” Kurashima, [0079-0080].</p> <p>“Then, as depicted in FIG. 8, a molding resin 38 is filled into respective areas between the lower wiring substrate 5, the intermediate wiring substrate 6, and the upper wiring substrate 7 of the stacked wiring substrate 8 in FIG. 7B.” Kurashima, [0090].</p> <p>“As depicted in FIG. 11, in the electronic component built-in substrate 1 according to the embodiment, the bump electrodes 42 of the semiconductor chip 40 are flip-chip connected to the connection pads P in the component mounting area A of the lower wiring substrate 5 explained in FIG. 4A. The underfill resin 44 is filled into a clearance under the semiconductor chip 40. The chip capacitor 50 having the connection terminal 52 on both end sides is adhered onto the solder resist 32 of the lower wiring substrate 5 in the lateral direction of the semiconductor chip 40. The connection terminals 52 on both end sides of the chip capacitor 50 are connected to the connection pads P of the lower wiring substrate 5 via the solder layer 54. The intermediate wiring substrate 6 shaped like a frame and explained in FIGS. 5A to 5C is arranged in the periphery of the semiconductor chip and the chip capacitor 50. The intermediate wiring substrate 6 has the opening portion 6 a, which penetrates from the upper surface to the lower surface, in the center part, and the semiconductor chip 40 and the chip capacitor 50 are mounted in this opening portion 6 a.” Kurashima, [0109-0111].</p> <p>“Also, the upper wiring substrate 7 is arranged over the semiconductor chip 40, the chip capacitor 50, and the intermediate wiring substrate 6. The second connection pads P 2 on the upper surface side of the intermediate wiring substrate 6 are electrically connected to the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 via the second solder balls 29.” Kurashima, [0112-0114].</p>
--	--

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

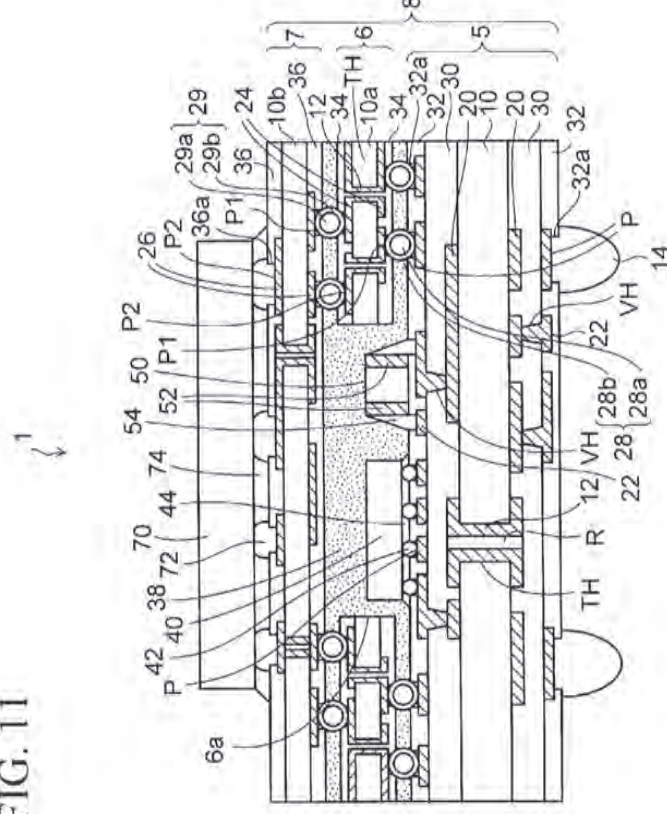
	<p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Kurashima discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P 2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P 2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually. In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6.” Kurashima, [0064-0067].</p>

	<p>“As depicted in FIG. 11, in the electronic component built-in substrate 1 according to the embodiment, the bump electrodes 42 of the semiconductor chip 40 are flip-chip connected to the connection pads P in the component mounting area A of the lower wiring substrate 5 explained in FIG. 4A. The underfill resin 44 is filled into a clearance under the semiconductor chip 40. The chip capacitor 50 having the connection terminal 52 on both end sides is adhered onto the solder resist 32 of the lower wiring substrate 5 in the lateral direction of the semiconductor chip 40. The connection terminals 52 on both end sides of the chip capacitor 50 are connected to the connection pads P of the lower wiring substrate 5 via the solder layer 54. The intermediate wiring substrate 6 shaped like a frame and explained in FIGS. 5A to 5C is arranged in the periphery of the semiconductor chip and the chip capacitor 50. The intermediate wiring substrate 6 has the opening portion 6 a, which penetrates from the upper surface to the lower surface, in the center part, and the semiconductor chip 40 and the chip capacitor 50 are mounted in this opening portion 6 a. The first connection pads P 1 on the lower surface side of the intermediate wiring substrate 6 are electrically connected to the connection pads P of the lower wiring substrate 5 via the first solder ball 28. Also, the upper wiring substrate 7 is arranged over the semiconductor chip 40, the chip capacitor 50, and the intermediate wiring substrate 6. The second connection pads P 2 on the upper surface side of the intermediate wiring substrate 6 are electrically connected to the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 via the second solder balls 29. Further, the molding resin 38 sealing the semiconductor chip 40 and the chip capacitor 50 is filled into respective areas between the lower wiring substrate 5, the intermediate wiring substrate 6, and the upper wiring substrate 7. Also, the solder bumps 72 of the semiconductor device 70 are connected to the second connection pads P 2 on the upper surface side of the upper wiring substrate 7. The underfill resin 74 is filled into a clearance under the semiconductor device 70.” Kurashima, [0108-0115].</p>
--	--

FIG. 11



Kurashima, FIG. 11

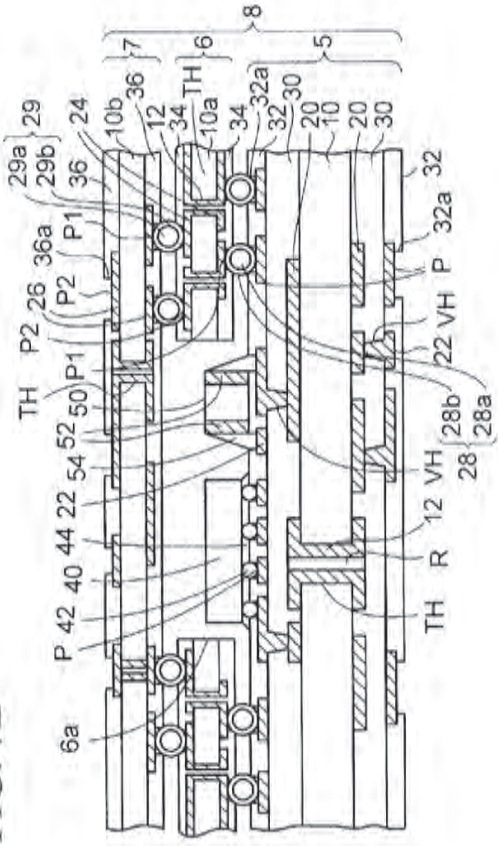
To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.	<p>Kurashima discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the intermediate wiring substrate 6, a wiring layer 24 is formed on both surface sides of a core substrate 10 a. The core substrate 10 a is formed of insulating material such as a glass epoxy resin, or the like, for example. The through holes TH penetrating in the thickness direction are provided in the core substrate 10 a. The wiring layers 24 on both surface sides are mutually connected via the through-hole plating layer 12 formed on the inner wall of the through hole TH.” Kurashima, [0054].</p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P 2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P 2 of the intermediate wiring</p>

	<p>substrate 6, and thus both members are electrically connected mutually. In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6.” Kurashima, [0064-0067].</p> <p>FIG. 7B</p>  <p>Kurashima, FIG. 7B</p> <p>“Then, as depicted in FIG. 6B, the first solder balls 28 on the lower surface side of the intermediate wiring substrate 6 in FIG. 6A are arranged on the connection pads P on the upper surface side of the above lower wiring substrate 5 in FIG. 4B, and then the reflow</p>
--	--

	<p>heating is applied. By this matter, the first solder balls 28 of the intermediate wiring substrate 6 are joined to the connection pads P of the lower wiring substrate 5, and thus both members are electrically connected mutually.” Kurashima, [0065].</p> <p>“In the upper wiring substrate 7, wiring layers 26 are formed on both surface sides of a core substrate 10 b respectively. The core substrate 10 b is formed of insulating material such as a glass epoxy resin, or the like, for example. The through holes TH penetrating in the thickness direction are provided in the core substrate 10 b. The wiring layers 26 on both surface sides are mutually connected via the through-hole plating layer 12 which is formed on the inner wall of the through hole TH.” Kurashima, [0068-0069].</p> <p>“In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6. With the above, a stacked wiring substrate in which the upper wiring substrate 7 is stacked on the lower wiring substrate 5 via the intermediate wiring substrate 6 is obtained.” Kurashima, [0075-0076].</p> <p>“Also, the upper wiring substrate 7 is arranged over the semiconductor chip 40, the chip capacitor 50, and the intermediate wiring substrate 6. The second connection pads P 2 on the upper surface side of the intermediate wiring substrate 6 are electrically connected to the first connection pads P 1 on the lower surface side of the upper wiring substrate 7 via the second solder balls 29. Further, the molding resin 38 sealing the semiconductor chip 40 and the chip capacitor 50 is filled into respective areas between the lower wiring substrate 5, the intermediate wiring substrate 6, and the upper wiring substrate 7.” Kurashima, [0100-0101].</p>
--	---

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Kurashima discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually. In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate</p>

	<p>6, and the first solder balls 28 located under this intermediate wiring substrate 6.” Kurashima, [0074-0075].</p> <p>FIG. 7B</p> <p>Kurashima, FIG. 7B</p> <p>“With the above, a stacked wiring substrate in which the upper wiring substrate 7 is stacked on the lower wiring substrate 5 via the intermediate wiring substrate 6 is obtained. As described above, the first and second connection pads P1, P2 on both surface sides of the intermediate wiring substrate 6 are arranged in the displaced positions mutually. Therefore, the first and second solder balls 28, 29 arranged on the lower and upper sides of the</p>
--	--

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>intermediate wiring substrate 6 are also arranged in the displaced positions mutually to correspond to the above displaced positions.” Kurashima, [0076-0077].</p> <p>“In the present embodiment, the intermediate wiring substrate 6 is interposed between the lower wiring substrate 5 and the upper wiring substrate 7. Therefore, it is unnecessary to set diameters of the first and second solder balls 28, 29 larger than heights of the semiconductor chip 40 and the chip capacitor 50.” Kurashima, [0079].</p> <p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

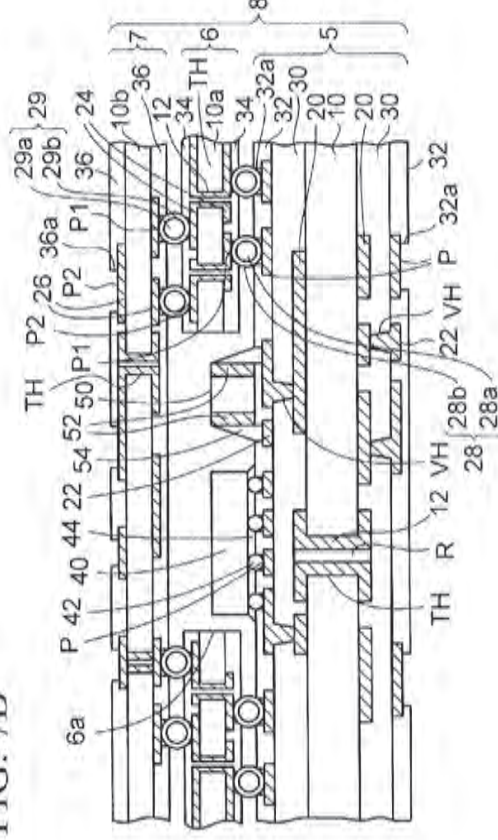
Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom ends of the plurality of metal pillars of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Kurashima discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

“A solder resist 34 in which opening portions 34 a are provided on first connection pads P1 of the wiring layer 24 is formed on the lower surface side of the core substrate 10 a. Similarly, the solder resist 34 in which the opening portions 34 a are provided on second connection pads P2 of the wiring layer 24 is formed on the upper surface side of the core substrate 10 a.” Kurashima, [0056].

FIG. 7B



Kurashima, FIG. 7B

“By reference to a plan view of FIG. 5B together with FIG. 5A, the first connection pads P1 on the lower surface side of the intermediate wiring substrate 6 and the second connection

	<p>pads P2 on the upper surface side thereof are arranged in mutually displaced positions. In FIGS. 5A and 5B, as the preferred example, when viewed from the top, the first connection pads P1 and the second connection pads P2 are arranged in the positions that are not mutually overlapped and are arranged like a staggered arrangement. Any pad arrangements are available if the first connection pads P1 and the second connection pads P2 are arranged in the mutually displaced positions. Besides the example in FIG. 5B, the first connection pads P1 and the second connection pads P2 may be arranged to be displaced in such a state that these connection pads are partially overlapped with each other.” Kurashima, [0059-0060].</p> <p>“Also, in the example in FIG. 5B, the first connection pads P1 and the second connection pads P2 on the lower and upper surface sides are arranged in two lines respectively. But the number of arrangement can be set arbitrarily.” Kurashima, [0061].</p> <p>“Then, as depicted in FIG. 7B, the second solder balls 29 on the lower surface side of the upper wiring substrate 7 in FIG. 7A are arranged on the second connection pads P2 on the upper surface side of the above-mentioned intermediate wiring substrate 6 in FIG. 6B, and then the reflow heating is applied. By this matter, the second solder balls 29 of the upper wiring substrate 7 are joined to the second connection pads P2 of the intermediate wiring substrate 6, and thus both members are electrically connected mutually. In this way, the upper wiring substrate 7 is electrically connected to the lower wiring substrate 5 via the second solder balls 29 located under this upper wiring substrate 7, the intermediate wiring substrate 6, and the first solder balls 28 located under this intermediate wiring substrate 6. With the above, a stacked wiring substrate in which the upper wiring substrate 7 is stacked on the lower wiring substrate 5 via the intermediate wiring substrate 6 is obtained. As described above, the first and second connection pads P1, P2 on both surface sides of the intermediate wiring substrate 6 are arranged in the displaced positions mutually.” Kurashima, [0074-0076].</p>
--	---

Appendix A-18 - Invalidity of U.S. Patent No. 9859202 in view of Kurashima - U.S. Patent Publication No. 20140054773

	<p>To the extent Plaintiff contends that Kurashima fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

U.S. Patent No. 9368566 (“Lee”) is titled Package on Package (POP) Integrated Device Comprising a Capacitor in a Substrate and lists Jong-Hoon Lee, Young Kyu Song, Daeik Daniel Kim, Jung Ho Yoon, Uei-Ming Jow, Mario Francisco Velez, Jonghae Kim, Xiaonan Zhang, and Ryan David Lane as inventors. Lee is assigned to QUALCOMM Incorporated. Lee anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Lee is a U.S. patent that was filed July 17, 2014 and published January 21, 2016. Lee is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(2).

The chart below provides representative examples of where each element of each Asserted Claim is found within Lee, or otherwise rendered obvious by disclosures and teachings of Lee, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Lee does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Lee with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Lee, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Lee “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Lee or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Lee set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Lee discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“A first example provides an integrated device that includes a substrate, a first die, a first encapsulation layer, a first redistribution portion, a second die, a second encapsulation layer, and a second redistribution portion. The substrate includes a first surface and a second surface. The substrate includes a capacitor. The first die is coupled to the first surface of the substrate. The first encapsulation layer encapsulates the first die. The first redistribution portion is coupled to the first encapsulation layer. The second die is coupled to the second</p>

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>surface of the substrate. The second encapsulation layer encapsulates the second die. The second redistribution portion is coupled to the second encapsulation layer.” Lee, [1:64-2:8].</p> <p>“Some features pertain to an integrated device (e.g., integrated package device, package-on-package (PoP) device) that includes a substrate, a first die, a first encapsulation layer, a first redistribution portion, a second die, a second encapsulation layer, and a second redistribution portion. The substrate includes a first surface and a second surface. The substrate includes a capacitor. The first die is coupled to the first surface of the substrate. The first encapsulation layer encapsulates the first die. The first redistribution portion is coupled to the first encapsulation. The second die is coupled to the second surface of the substrate. The second encapsulation layer encapsulates the second die. The second redistribution portion is coupled to the second encapsulation layer.” Lee, [4:30-4:43].</p> <p>“FIG. 2 illustrates an exemplary package on package (PoP) integrated device 200 that includes a capacitor in a substrate. As shown in FIG. 2, the integrated device 200 (e.g., integrated package device) includes a first die 202, a second die 206, a substrate 210, a first encapsulation layer 220, a second encapsulation layer 230, a first redistribution portion 240, and a second redistribution portion 250. The substrate 210 includes a dielectric layer 212, a via 214, a pad 216, a first capacitor 217 and a second capacitor 219. In some implementations, the substrate 210 is a laminate substrate. The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface).” Lee, [5:3-5:14].</p>
--	--

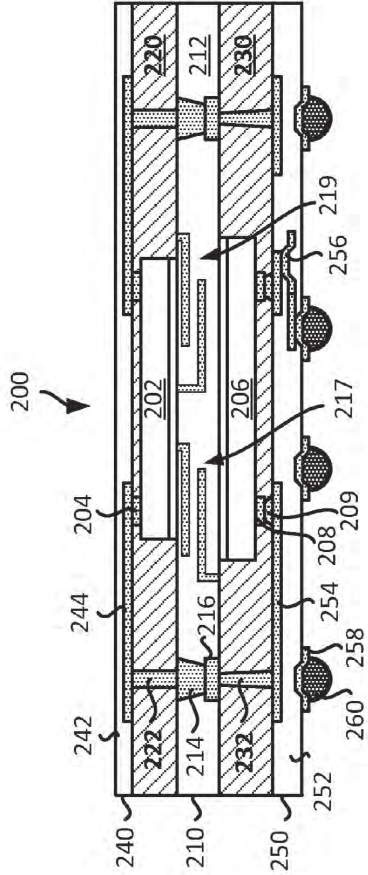


FIG. 2

Lee, FIG. 2

“FIG. 4 illustrates an exemplary package on package (PoP) integrated device 400 that includes a capacitor in a hybrid substrate. As shown in FIG. 4, the integrated device 400 (e.g., integrated package device) includes a first die 402, a second die 406, a substrate 410, a first encapsulation layer 420, a second encapsulation layer 430, a first redistribution portion 440, and a second redistribution portion 450. The substrate 410 includes a first dielectric layer 412, a second dielectric layer 413, a third dielectric layer 415, a via 414, a pad 416, a first capacitor 417 and a second capacitor 419. In some implementations, the substrate 410 is a hybrid laminate substrate.” Lee, [7:64-8:8].

“FIG. 6 illustrates an exemplary package on package (PoP) integrated device 600 that includes a capacitor in a substrate. As shown in FIG. 6, the integrated device 600 (e.g.,

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>integrated package device) includes a first die 602, a second die 606, a substrate 610, a first encapsulation layer 620, a second encapsulation layer 630, a first redistribution portion 640, and a second redistribution portion 650. The substrate 610 includes a dielectric layer 612, a via 614, a pad 616, a capacitor 618. In some implementations, the substrate 610 is a laminate substrate.” Lee, [11:4-11:13].</p> <p>“Stage 1 of FIG. 10A, illustrates a state after a substrate 1000 that includes a capacitor is provided. In some implementations, the substrate 1000 is similar to the substrate 210 of FIG. 2, the substrate 410 of FIG. 4, or the substrate 610 of FIG. 6, described above. In some implementations, the substrate 1000 is provided by a supplier. In some implementations, the substrate 1000 is fabricated (e.g., formed). The substrate 1000 includes a via 1001 and a pad 1003. The via 1001 is coupled to the pad 1003.” Lee, [16:64-17:5].</p>
[1.A] a bottom package substrate;	<p>Lee discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“As shown in FIG. 1, the integrated device 100 includes a first package 102 and a second package 104. The first package 102 includes a first substrate 106, a first die (e.g., chip) 108, a first set of solder balls 116, a first set of interconnects 118, and a capacitor 120. The first substrate 106 may include traces and/or vias (both of which are not shown).” Lee, [1:12-1:17].</p> <p>“FIG. 2 illustrates an exemplary package on package (PoP) integrated device 200 that includes a capacitor in a substrate. As shown in FIG. 2, the integrated device 200 (e.g., integrated package device) includes a first die 202, a second die 206, a substrate 210, a first</p>

encapsulation layer 220, a second encapsulation layer 230, a first redistribution portion 240, and a second redistribution portion 250.” Lee, [5:3-5:9].

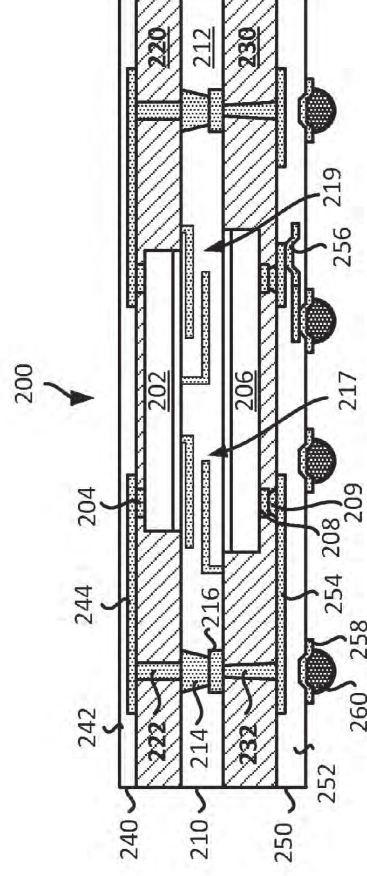


FIG. 2

Lee, FIG. 2

“The substrate 410 includes a first dielectric layer 412, a second dielectric layer 413, a third dielectric layer 415, a via 414, a pad 416, a first capacitor 417 and a second capacitor 419. In some implementations, the substrate 410 is a hybrid laminate substrate. In some implementations, the third dielectric layer 415 has a high k value, relative to the k value of the first dielectric layer 412 and/or the second dielectric layer 413. For example, the third dielectric layer 415 may have a k value that is about at least 2 times greater than the k value of the first dielectric layer 412 and/or the second dielectric layer 413. In some implementations, the substrate 410 may include more than three dielectric layers. The

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>substrate 410 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). The via 414 is coupled to the pad 416. In some implementations, the combination of the via 414 and the pad 416 traverses from the first surface of the substrate 410 to the second surface of the substrate 410. In some implementations, the via 414 and/or the pad 416 is a form of an interconnect that traverses the substrate 410.” Lee, [8:4-8:23].</p> <p>“The substrate 610 includes a dielectric layer 612, a via 614, a pad 616, a capacitor 618. In some implementations, the substrate 610 is a laminate substrate. The substrate 610 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 612 may include several dielectric layers. In some implementations, the dielectric layers may be the same material. The via 614 is coupled to the pad 616. In some implementations, the combination of the via 614 and the pad 616 traverse from the first surface of the substrate 610 to the second surface of the substrate 610. In some implementations, the via 614 and/or the pad 616 is a form of an interconnect that traverse the substrate 610.” Lee, [11:11-11:23].</p> <p>“Stage 1 of FIG. 10A, illustrates a state after a substrate 1000 that includes a capacitor is provided. In some implementations, the substrate 1000 is similar to the substrate 210 of FIG. 2, the substrate 410 of FIG. 4, or the substrate 610 of FIG. 6, described above. In some implementations, the substrate 1000 is provided by a supplier. In some implementations, the substrate 1000 is fabricated (e.g., formed). The substrate 1000 includes a via 1001 and a pad 1003. The via 1001 is coupled to the pad 1003.” Lee, [16:64-17:5].</p> <p>“Stage 7 of FIG. 10B, illustrates a state after a second die 1012 is provided and coupled to a second surface (e.g., bottom surface) of the substrate 1000. The second die 1012 may include a back side and a front side (e.g., active side). In some implementations, the back side of the second die 1012 is coupled to the second surface of the substrate 1002 using a bonding agent</p>
--	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>(e.g., glue). In some implementations, the substrate 1002 may be flipped upside down before the second die 1012 is coupled to the second surface of the substrate 1000.” Lee, [17:33-17:42].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Lee discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates a conventional package on package (PoP) integrated device. As shown in FIG. 1, the integrated device 100 includes a first package 102 and a second package 104. The first package 102 includes a first substrate 106, a first die (e.g., chip) 108, a first set of solder balls 116, a first set of interconnects 118, and a capacitor 120. The first substrate 106 may include traces and/or vias (both of which are not shown). The second package 104 includes a second substrate 105, a second die 107, a third die 109, a second set of solder balls 115, a first set of wire bonding 117, and a second set of wire bonding 119. The second substrate 105 may include traces and/or vias (both of which are not shown). The second package 104 is positioned above the first package 102.” Lee, [1:11-1:23].</p> <p>“A first example provides an integrated device that includes a substrate, a first die, a first encapsulation layer, a first redistribution portion, a second die, a second encapsulation layer, and a second redistribution portion. The substrate includes a first surface and a second</p>

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>The substrate includes a capacitor. The first die is coupled to the first surface of the substrate. The first encapsulation layer encapsulates the first die. The first redistribution portion is coupled to the first encapsulation layer. The second die is coupled to the second surface of the substrate. The second encapsulation layer encapsulates the second die. The second redistribution portion is coupled to the second encapsulation layer.” Lee, [1:64-2:8].</p> <p>“FIG. 2 illustrates an exemplary package on package (PoP) integrated device 200 that includes a capacitor in a substrate. As shown in FIG. 2, the integrated device 200 (e.g., integrated package device) includes a first die 202, a second die 206, a substrate 210, a first encapsulation layer 220, a second encapsulation layer 230, a first redistribution portion 240, and a second redistribution portion 250. The substrate 210 includes a dielectric layer 212, a via 214, a pad 216, a first capacitor 217 and a second capacitor 219. In some implementations, the substrate 210 is a laminate substrate. The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface).” Lee, [5:3-5:14].</p>
--	---

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>integrated package device) includes a first die 602, a second die 606, a substrate 610, a first encapsulation layer 620, a second encapsulation layer 630, a first redistribution portion 640, and a second redistribution portion 650. The substrate 610 includes a dielectric layer 612, a via 614, a pad 616, a capacitor 618. In some implementations, the substrate 610 is a laminate substrate. The substrate 610 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface).” Lee, [11:4-11:15].</p> <p>“Stage 1 of FIG. 10A, illustrates a state after a substrate 1000 that includes a capacitor is provided. In some implementations, the substrate 1000 is similar to the substrate 210 of FIG. 2, the substrate 410 of FIG. 4, or the substrate 610 of FIG. 6, described above. In some implementations, the substrate 1000 is provided by a supplier. In some implementations, the substrate 1000 is fabricated (e.g., formed). The substrate 1000 includes a via 1001 and a pad 1003. The via 1001 is coupled to the pad 1003. Stage 2 illustrates a state after an interconnect 1005 is provided (e.g., formed) on the substrate 1000. Specifically, the interconnect 1005 is provided over the via 1001. In some implementations, the interconnect 1005 is a via (e.g., through encapsulation via, through mold via). The interconnect 1005 may be formed on the substrate through one or more plating processes. Stage 3 illustrates a state after a first die 1002 is provided and coupled to a first surface (e.g., top surface) of the substrate 1000.” Lee, [16:64-17:15].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Lee discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“The substrate 210 includes a dielectric layer 212, a via 214, a pad 216, a first capacitor 217 and a second capacitor 219. In some implementations, the substrate 210 is a laminate substrate. The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 212 may include several dielectric layers. In some implementations, the dielectric layers may be the same material. The via 214 is coupled to the pad 216. In some implementations, the combination of the via 214 and the pad 216 traverses from the first surface of the substrate 210 to the second surface of the substrate 210.” Lee, [5:10-5:21].</p> <p>“The first redistribution portion 240 is coupled to the first surface of the first encapsulation layer 220. The first redistribution portion 240 includes a second dielectric layer 242 and a first set of redistribution interconnects 244. In some implementations, the first redistribution portion 240 may include more than one set of redistribution interconnects. The first set of redistribution interconnects 244 is coupled to the set of die interconnects 204 and the set of interconnects 222.” Lee, [5:58-5:65].</p> <p>“The first die 202 includes a back side and a front side (e.g., active side). The front side is coupled to a set of die interconnects 204. The set of die interconnects 204 may be one of at least pads and/or pillars in some implementations. The back side of the first die 202 is coupled to the first surface of the substrate 210. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the first die 202 to the first surface of the substrate 210. As</p>
---	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>shown in FIG. 2, the back side of the first die 202 is facing the substrate 210 while the front side (e.g., active side) of the first die 202 is facing away from the substrate 210. The first encapsulation layer 220 encapsulates the first die 202 and the set of die interconnects 204. In some implementations, the first encapsulation layer 220 is one of at least a mold, a polymer, and/or a photo-etchable material. In some implementations, a photo-etchable material is a material that may be etched through a photo etching process. The first encapsulation layer 220 includes a set of interconnects 222. In some implementations, the set of interconnects 222 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some implementations, the set of interconnects 222 traverses from a first surface (e.g., top surface) of the first encapsulation layer 220 to a second surface (e.g., bottom surface) of the first encapsulation layer 220. FIG. 2 illustrates that a portion of the set of interconnects 222 in the first encapsulation layer 220 is coupled to the via 214 in the substrate 210.” Lee, [6:1-6:27].</p>
--	---

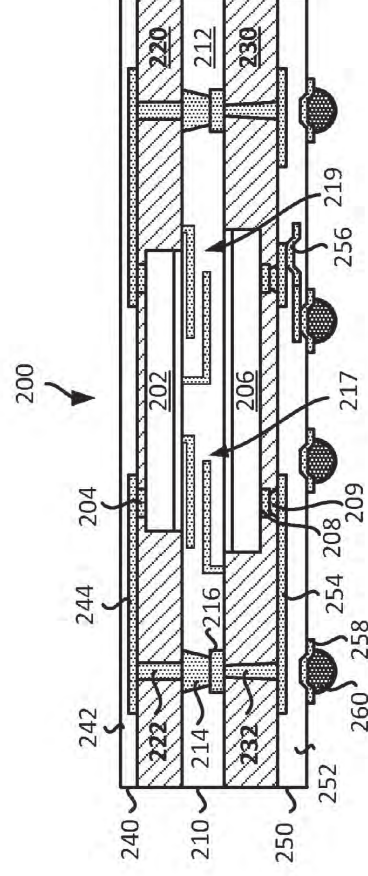


FIG. 2

Lee, FIG. 2

“The second die 206 includes a back side and a front side (e.g., active side). The front side is coupled to a set of interconnects 208. The set of interconnects 208 may be one of at least pads and/or pillars in some implementations. The back side of the second die 206 is coupled to the second surface of the substrate 210. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the second die 206 to the second surface of the substrate 210. As shown in FIG. 2, the back side of the second die 206 is facing the substrate 210 while the front side (e.g., active side) of the second die 206 is facing away from the substrate 210. The second encapsulation layer 230 encapsulates the second die 206 and the set of interconnects 208.” Lee, [6:1-6:13].

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>“FIG. 2 illustrates that a portion of the set of interconnects 232 in the second encapsulation layer 230 is coupled to the pad 216 in the substrate 210. In some implementations, the set of interconnects 209 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). The set of interconnects 209 is coupled to the set of interconnects 208.” Lee, [6:25-6:31].</p> <p>“The second redistribution portion 250 is coupled to the first surface of the second encapsulation layer 230. The second redistribution portion 250 includes a third dielectric layer 252, a second set of redistribution interconnects 254, a third set of redistribution interconnects 256, and a set of under bump metallization (UBM) layers 258. In some implementations, the second redistribution portion 250 may include one, two, or more than two sets of redistribution interconnects. The first set of redistribution interconnects 254 is coupled to the set of interconnects 209 and the set of interconnects 232.” Lee, [6:32-6:41].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Lee discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The substrate 410 includes a first dielectric layer 412, a second dielectric layer 413, a third dielectric layer 415, a via 414, a pad 416, a first capacitor 417 and a second capacitor 419. In some implementations, the substrate 410 is a hybrid laminate substrate. In some implementations, the third dielectric layer 415 has a high k value, relative to the k value of</p>

	<p>the first dielectric layer 412 and/or the second dielectric layer 413. For example, the third dielectric layer 415 may have a k value that is about 2 times greater than the k value of the first dielectric layer 412 and/or the second dielectric layer 413. In some implementations, the substrate 410 may include more than three dielectric layers. The substrate 410 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). The via 414 is coupled to the pad 416. In some implementations, the combination of the via 414 and the pad 416 traverses from the first surface of the substrate 410 to the second surface of the substrate 410. In some implementations, the via 414 and/or the pad 416 is a form of an interconnect that traverses the substrate 410.” Lee, [8:4-8:23].</p> <p>“As shown in FIG. 5, the substrate 410 includes the first dielectric layer 412, the second dielectric layer 413, the third dielectric layer 415, the via 414, the pad 416, the first capacitor 417 and the second capacitor 419. In some implementations, the substrate 410 is a laminate substrate. The substrate 410 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). The via 414 is coupled to the pad 416. In some implementations, the combination of the via 414 and the pad 416 traverses from the first surface of the substrate 410 to the second surface of the substrate 410. In some implementations, the via 414 and/or the pad 416 is a form of an interconnect that traverses the substrate 410.” Lee, [9:63-10:8].</p> <p>“The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 212 may include several dielectric layers. In some implementations, the dielectric layers may be the same material. The via 214 is coupled to the pad 216. In some implementations, the combination of the via 214 and the pad 216 traverses from the first surface of the substrate 210 to the second surface of the substrate 210. In some implementations, the via 214 and/or the pad 216 is a form of an interconnect that traverses the substrate 210.” Lee, [9:65-10:8].</p>
--	---

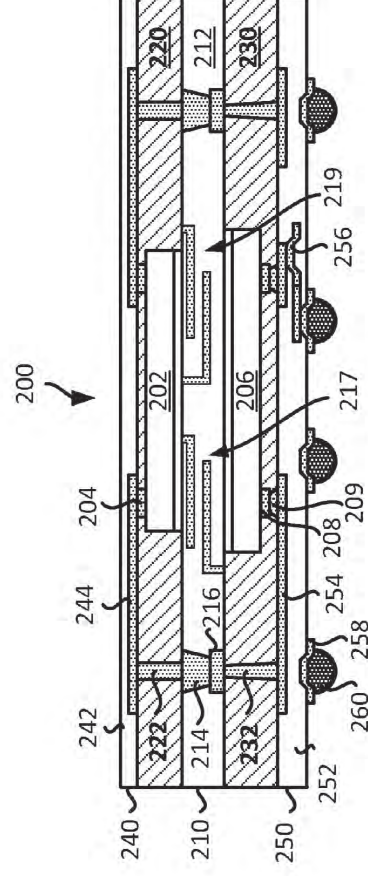


FIG. 2

Lee, FIG. 2

“The substrate 610 includes a dielectric layer 612, a via 614, a pad 616, a capacitor 618. In some implementations, the substrate 610 is a laminate substrate. The substrate 610 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 612 may include several dielectric layers. In some implementations, the dielectric layers may be the same material. The via 614 is coupled to the pad 616. In some implementations, the combination of the via 614 and the pad 616 traverse from the first surface of the substrate 610 to the second surface of the substrate 610. In some implementations, the via 614 and/or the pad 616 is a form of an interconnect that traverse the substrate 610.” Lee, [11:11-11:23].

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>“As shown in FIG. 7, the substrate 610 includes the dielectric layer 612, the via 614, the pad 616, the capacitor 618, a dielectric layer 702, a first via 704, a first interconnect 706, a second via 714, and a second interconnect 716. In some implementations, the substrate 610 is a laminate substrate. The substrate 610 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 612 may include several dielectric layers. The via 614 is coupled to the pad 616. In some implementations, the combination of the via 614 and the pad 616 traverses from the first surface of the substrate 610 to the second surface of the substrate 610. In some implementations, the via 614 and/or the pad 616 is a form of an interconnect that traverses the substrate 610.” Lee, [12:58-13:4].</p> <p>“Stage 1 of FIG. 10A, illustrates a state after a substrate 1000 that includes a capacitor is provided. In some implementations, the substrate 1000 is similar to the substrate 210 of FIG. 2, the substrate 410 of FIG. 4, or the substrate 610 of FIG. 6, described above. In some implementations, the substrate 1000 is provided by a supplier. In some implementations, the substrate 1000 is fabricated (e.g., formed). The substrate 1000 includes a via 1001 and a pad 1003. The via 1001 is coupled to the pad 1003.” Lee, [16:64-17:5].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Lee discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p>See, e.g.:</p>

“The first encapsulation layer 220 includes a set of interconnects 222. In some implementations, the set of interconnects 222 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some implementations, the set of interconnects 222 traverses from a first surface (e.g., top surface) of the first encapsulation layer 220 to a second surface (e.g., bottom surface) of the first encapsulation layer 220. FIG. 2 illustrates that a portion of the set of interconnects 222 in the first encapsulation layer 220 is coupled to the via 214 in the substrate 210.” Lee, [5:47-5:57].

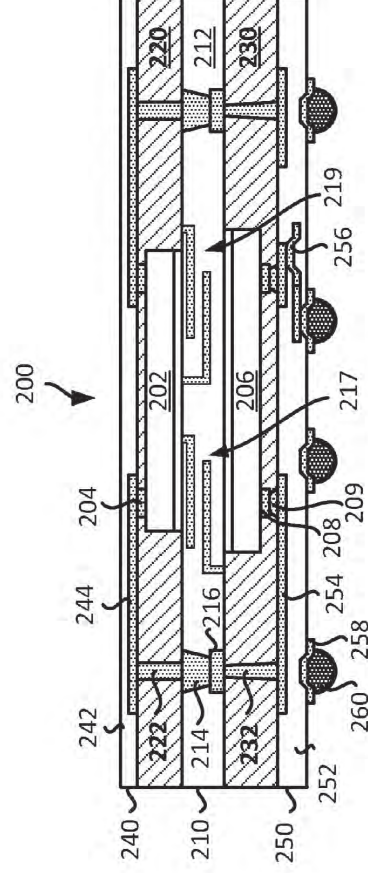


FIG. 2

Lee, FIG. 2

“The second encapsulation layer 230 includes a set of interconnects 232 and a set of interconnects 209. In some implementations, the set of interconnects 232 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>implementations, the set of interconnects 232 traverses from a first surface (e.g., top surface) of the second encapsulation layer 230 to a second surface (e.g., bottom surface) of the second encapsulation layer 230. FIG. 2 illustrates that a portion of the set of interconnects 232 in the second encapsulation layer 230 is coupled to the pad 216 in the substrate 210.” Lee, [6:17-6:28].</p> <p>“Stage 12 illustrates a state after at least one cavity 921 is formed in at least one of the dielectric layers. As shown at stage 12, the cavity 921 is formed over a pad 922 (which is part of the first metal layer 902). The cavity traverses, the first, second, fourth, and fifth dielectric layers 904, 908, 916, and 920. In some implementations, the dielectric layer 923 may represent the first, second, fourth, and fifth dielectric layers 904, 908, 916, and 920. In some implementations, the cavity 921 is formed using a laser etching process (e.g., laser ablation). Stage 13 illustrates a state after the cavity 921 is filled with a metal material to define an interconnect 924. In some implementations, the interconnect 924 is a via that is coupled to the pad 922. Different implementations may use different processes to fill the cavity 921. In some implementations, a plating process is used.” Lee, [16:24-16:39].</p> <p>“Stage 2 illustrates a state after an interconnect 1005 is provided (e.g., formed) on the substrate 1000. Specifically, the interconnect 1005 is provided over the via 1001. In some implementations, the interconnect 1005 is a via (e.g., through encapsulation via, through mold via). The interconnect 1005 may be formed on the substrate through one or more plating processes.” Lee, [17:6-17:12].</p> <p>“Stage 9 illustrates a state after a first cavity 1015 and a second cavity 1017 are formed in the second encapsulation layer 1014. Different implementations may use different processes for forming the cavities. In some implementations, a laser etching process (e.g., laser ablation) is used to form the cavities. In some implementations, a photo-etching process is</p>
--	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>used to form the cavities. As shown at stage 9, the cavity 1015 is formed on the pad 1003, and the cavity 1017 is formed on an interconnect (e.g., pad, pillar) of the second die 1012. Stage 10 illustrates a state after the first cavity 1015 and the second cavity 1017 are filled with an electrically conductive material to form an interconnect 1016, and an interconnect 1018, respectively. In some implementations, the interconnect 1016 is a via (e.g., through encapsulation via, through mold via). In some implementations, the interconnect 1018 is a via (e.g., through encapsulation via, through mold via).” Lee, [17:48-17:63].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Lee discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 2 illustrates that a portion of the set of interconnects 222 in the first encapsulation layer 220 is coupled to the via 214 in the substrate 210.” Lee, [5:54-5:57].</p> <p>“The second redistribution portion 250 includes a third dielectric layer 252, a second set of redistribution interconnects 254, a third set of redistribution interconnects 256, and a set of under bump metallization (UBM) layers 258. In some implementations, the second redistribution portion 250 may include one, two, or more than two sets of redistribution interconnects. The first set of redistribution interconnects 254 is coupled to the set of interconnects 209 and the set of interconnects 232.” Lee, [6:33-6:41].</p>

“FIG. 3 illustrates a close-up view of a portion of the substrate 210 of FIG. 2. As shown in FIG. 3, the substrate 210 includes the dielectric layer 212, the via 214, the pad 216, the first capacitor 217 and the second capacitor 219. In some implementations, the substrate 210 is a laminate substrate. The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 212 may include several dielectric layers. The via 214 is coupled to the pad 216. In some implementations, the combination of the via 214 and the pad 216 traverses from the first surface of the substrate 210 to the second surface of the substrate 210. In some implementations, the via 214 and/or the pad 216 is a form of an interconnect that traverses the substrate 210. It should be noted that the substrate 210 may include additional interconnects (e.g., traces, vias), which are not shown for the purpose of clarity. These un-shown (or not visible) interconnects may couple the capacitors 217 and/or 219 to the via 214 and/or pad 216 in some implementations. In some implementations, at least one of the capacitors 217 and/or 219 may be electrically coupled to at least the first die 202 and/or the second die 206. For example, the capacitor 217 may be electrically coupled to the first die 202 through the via 214, the interconnect 222, the interconnect 244, and/or the interconnect 204. Similarly, the capacitor 217 may be electrically coupled to the second die 206 through the via 214, the pad 216, the interconnect 232, the interconnect 254, the interconnect 208, and/or the interconnect 209.” Lee, [6:48-7:8].

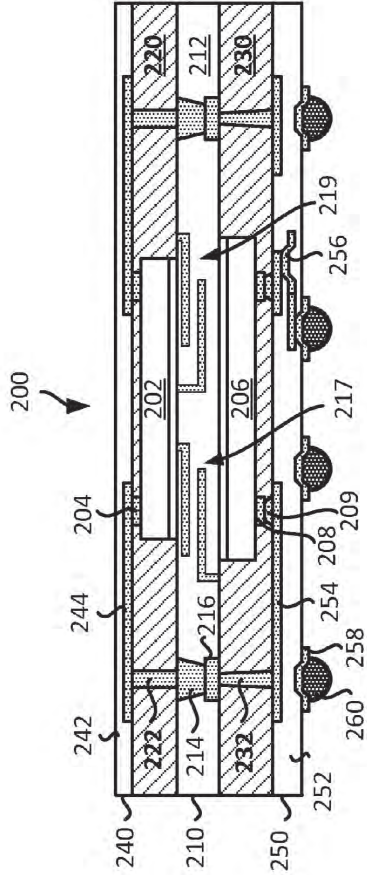


FIG. 2

Lee, FIG. 2

“Stage 2 illustrates a state after a first metal layer 802 is provided (e.g., formed) on the carrier 800. Specifically, stage 2 illustrates a state after the first metal layer 802 is formed over a first surface of the carrier 800. In some implementations, providing the first metal layer 802 may include forming the first metal layer 802 and selectively etching portions of the first metal layer 802 to define one or more interconnects (e.g., form one or more pads, vias, traces).” Lee, [13:45-13:52].

“Stage 4 illustrates a state after a second metal layer 806 is provided (e.g., formed) on the first dielectric layer 804. Specifically, stage 4 illustrates a state after the second metal layer 806 is formed over a first surface of the first dielectric layer 804. In some implementations, providing the second metal layer 806 may include forming the second metal layer 806 and

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>selectively etching portions of the second metal layer 806 to define one or more interconnects (e.g., form one or more pads, vias, traces). In some implementations, the second metal layer 806 is plated on the first dielectric layer 804 using a plating process. In some implementations, some portions of the second metal layer 806 may be coupled to some portions of the first metal layer 802.” Lee, [13:58-14:3].</p> <p>“Stage 10 illustrates a state after a fifth metal layer 818 is provided (e.g., formed) on the fourth dielectric layer 816. Specifically, stage 10 illustrates a state after the fifth metal layer 818 is formed over a first surface of the fourth dielectric layer 816. In some implementations, providing the fifth metal layer 818 may include forming the fifth metal layer 818 and selectively etching portions of the fifth metal layer 818 to define one or more interconnects (e.g., form one or more pads, vias, traces). In some implementations, the fifth metal layer 818 is plated on the fourth dielectric layer 816 using a plating process. In some implementations, some portions of the fifth metal layer 818 may be coupled to some portions of the fourth metal layer 814.” Lee, [14:43-14:55].</p> <p>“Stage 13 illustrates a state after the cavity 821 is filled with a metal material to define an interconnect 824. In some implementations, the interconnect 824 is a via that is coupled to the pad 822. Different implementations may use different processes to fill the cavity 821. In some implementations, a plating process is used.” Lee, [14:65-15:3].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,

Lee discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.

See, e.g.:

“FIG. 2 illustrates an exemplary package on package (PoP) integrated device 200 that includes a capacitor in a substrate. As shown in FIG. 2, the integrated device 200 (e.g., integrated package device) includes a first die 202, a second die 206, a substrate 210, a first encapsulation layer 220, a second encapsulation layer 230, a first redistribution portion 240, and a second redistribution portion 250.” Lee, [5:3-5:9].

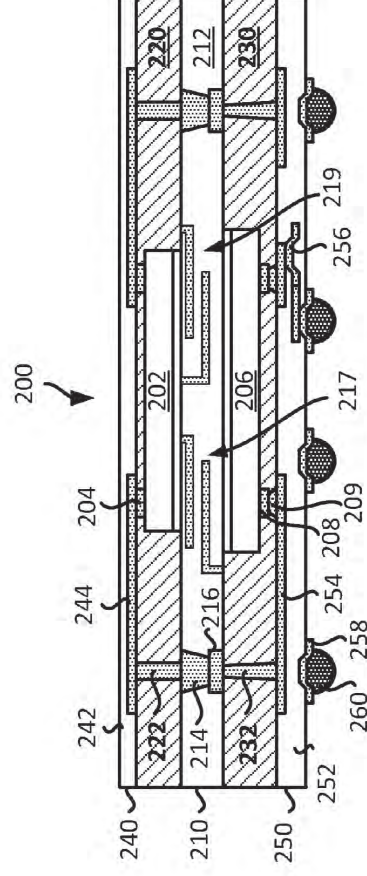


FIG. 2

Lee, FIG. 2

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>“The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 212 may include several dielectric layers. In some implementations, the dielectric layers may be the same material. The via 214 is coupled to the pad 216. In some implementations, the combination of the via 214 and the pad 216 traverses from the first surface of the substrate 210 to the second surface of the substrate 210.” Lee, [5:14-5:21].</p> <p>“FIG. 2 illustrates that a portion of the set of interconnects 222 in the first encapsulation layer 220 is coupled to the via 214 in the substrate 210. The first redistribution portion 240 is coupled to the first surface of the first encapsulation layer 220. The first redistribution portion 240 includes a second dielectric layer 242 and a first set of redistribution interconnects 244. In some implementations, the first redistribution portion 240 may include more than one set of redistribution interconnects. The first set of redistribution interconnects 244 is coupled to the set of die interconnects 204 and the set of interconnects 222.” Lee, [5:54-5:65].</p> <p>“Stage 2 illustrates a state after a first metal layer 802 is provided (e.g., formed) on the carrier 800. Specifically, stage 2 illustrates a state after the first metal layer 802 is formed over a first surface of the carrier 800. In some implementations, providing the first metal layer 802 may include forming the first metal layer 802 and selectively etching portions of the first metal layer 802 to define one or more interconnects (e.g., form one or more pads, vias, traces). In some implementations, the first metal layer 802 is plated on the carrier 800 using a plating process.” Lee, [13:45-13:54].</p> <p>“Stage 12 illustrates a state after at least one cavity 821 is formed in at least one of the dielectric layers. As shown at stage 12, the cavity 821 is formed over a pad 822 (which is part of the first metal layer 802). The cavity traverses, the first, second, third, fourth and fifth</p>
--	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>dielectric layers 804, 808, 812, 816, and 820. In some implementations, the cavity 821 is formed using a laser etching process (e.g., laser ablation).” Lee, [14:58-14:64].</p> <p>“Stage 2 illustrates a state after an interconnect 1005 is provided (e.g., formed) on the substrate 1000. Specifically, the interconnect 1005 is provided over the via 1001. In some implementations, the interconnect 1005 is a via (e.g., through encapsulation via, through mold via). The interconnect 1005 may be formed on the substrate through one or more plating processes.” Lee, [17:6-17:12].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Lee discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p> <p>“The second die 206 includes a back side and a front side (e.g., active side). The front side is coupled to a set of interconnects 208. The set of interconnects 208 may be one of at least pads and/or pillars in some implementations. The back side of the second die 206 is coupled to the second surface of the substrate 210. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the second die 206 to the second surface of the substrate 210. As shown in FIG. 2, the back side of the second die 206 is facing the substrate 210 while the front side (e.g., active side) of the second die 206 is facing away from the</p>

	<p>substrate 210. The second encapsulation layer 230 encapsulates the second die 206 and the set of interconnects 208. In some implementations, the second encapsulation layer 230 is one of at least a mold, a polymer, and/or a photo-etchable material. In some implementations, a photo-etchable material is a material that may be etched through a photo etching process. The second encapsulation layer 230 includes a set of interconnects 232 and a set of interconnects 209. In some implementations, the set of interconnects 232 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some implementations, the set of interconnects 232 traverses from a first surface (e.g., top surface) of the second encapsulation layer 230 to a second surface (e.g., bottom surface) of the second encapsulation layer 230. FIG. 2 illustrates that a portion of the set of interconnects 232 in the second encapsulation layer 230 is coupled to the pad 216 in the substrate 210. In some implementations, the set of interconnects 209 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). The set of interconnects 209 is coupled to the set of interconnects 208.” Lee, [6:1-6:31].</p> <p>“The second redistribution portion 250 is coupled to the first surface of the second encapsulation layer 230. The second redistribution portion 250 includes a third dielectric layer 252, a second set of redistribution interconnects 254, a third set of redistribution interconnects 256, and a set of under bump metallization (UBM) layers 258. In some implementations, the second redistribution portion 250 may include one, two, or more than two sets of redistribution interconnects. The first set of redistribution interconnects 254 is coupled to the set of interconnects 209 and the set of interconnects 232. In some implementations, the third dielectric layer 252 includes one or more dielectric layers.” Lee, [6:32-6:43].</p> <p>“The first redistribution portion 440 is coupled to the first surface of the first encapsulation layer 420. The first redistribution portion 440 includes a fourth dielectric layer 442 and a first</p>
--	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>set of redistribution interconnects 444. In some implementations, the first redistribution portion 440 may include more than one set of redistribution interconnects. The first set of redistribution interconnects 444 is coupled to the set of die interconnects 404 and the set of interconnects 422. In some implementations, the fourth dielectric layer 442 includes one or more dielectric layers.” Lee, [9:5-9:14].</p> <p>“The first redistribution portion 240 is coupled to the first surface of the first encapsulation layer 220. The first redistribution portion 240 includes a second dielectric layer 242 and a first set of redistribution interconnects 244. In some implementations, the first redistribution portion 240 may include more than one set of redistribution interconnects. The first set of redistribution interconnects 244 is coupled to the set of die interconnects 204 and the set of interconnects 222. In some implementations, the second dielectric layer 242 includes one or more dielectric layers.” Lee, [9:46-9:55].</p>
--	--

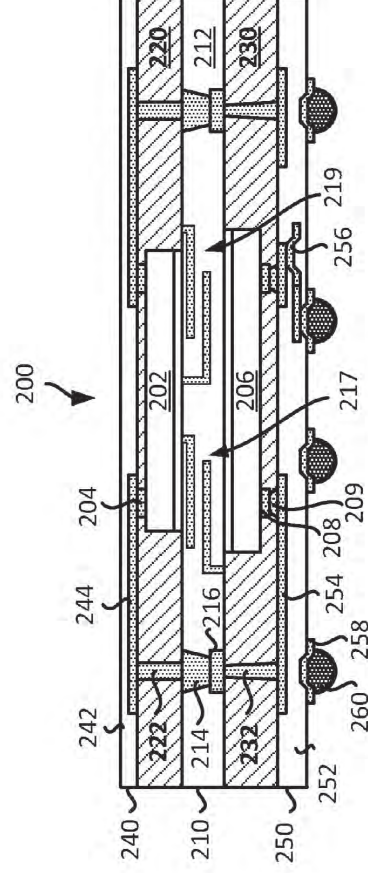


FIG. 2

Lee, FIG. 2

“The first redistribution portion 640 is coupled to the first surface of the first encapsulation layer 620. The first redistribution portion 640 includes a second dielectric layer 642 and a first set of redistribution interconnects 644. In some implementations, the first redistribution portion 640 may include more than one set of redistribution interconnects. The first set of redistribution interconnects 644 is coupled to the set of die interconnects 604 and the set of interconnects 622. In some implementations, the second dielectric layer 642 includes one or more dielectric layers.” Lee, [11:54-11:63].

“Stage 11 illustrates a state after a second redistribution interconnect 1020 is provided (e.g., formed) on the second encapsulation layer 1014. In some implementations, the second redistribution interconnect 1020 is formed by forming one or more metal layers and

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>selectively etching portions of the one or more metal layers. The second redistribution interconnect 1020 may be coupled to the interconnect 1005 and the second die 1012.” Lee, [17:64-18:4].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Lee discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p> <p>“The second encapsulation layer 230 encapsulates the second die 206 and the set of interconnects 208. In some implementations, the second encapsulation layer 230 is one of at least a mold, a polymer, and/or a photo-etchable material. In some implementations, a photo-etchable material is a material that may be etched through a photo etching process. The second encapsulation layer 230 includes a set of interconnects 232 and a set of interconnects 209. In some implementations, the set of interconnects 232 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some implementations, the set of interconnects 232 traverses from a first surface (e.g., top surface) of the second encapsulation layer 230 to a second surface (e.g., bottom surface) of the second encapsulation layer 230. FIG. 2 illustrates that a portion of the set of interconnects 232 in the second encapsulation layer 230 is coupled to the pad 216 in the substrate 210. In some implementations, the set of interconnects 209 is one of at least a through encapsulation via</p>

(TEV) and/or a through mold via (TMV). The set of interconnects 209 is coupled to the set of interconnects 208.” Lee, [6:12-6:31].

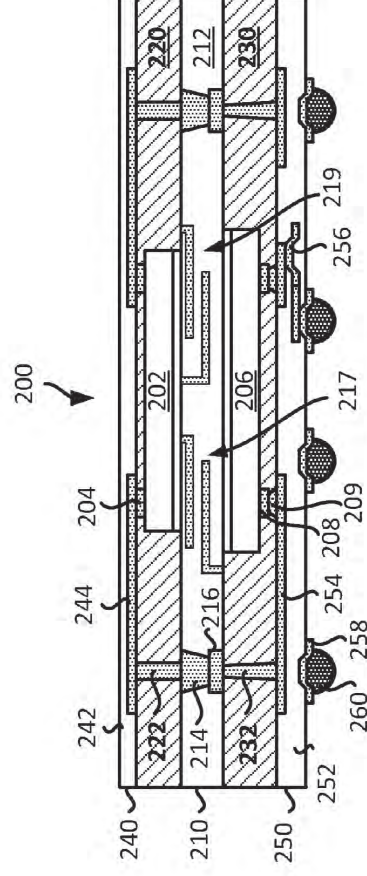


FIG. 2

Lee, FIG. 2

“The first set of redistribution interconnects 254 is coupled to the set of interconnects 209 and the set of interconnects 232. In some implementations, the third dielectric layer 252 includes one or more dielectric layers.” Lee, [6:40-6:43].

“It should be noted that the substrate 210 may include additional interconnects (e.g., traces, vias), which are not shown for the purpose of clarity. These un-shown (or not visible) interconnects may couple the capacitors 217 and/or 219 to the via 214 and/or pad 216 in some implementations. In some implementations, at least one of the capacitors 217 and/or 219 may

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>be electrically coupled to at least the first die 202 and/or the second die 206. For example, the capacitor 217 may be electrically coupled to the first die 202 through the via 214, the interconnect 222, the interconnect 244, and/or the interconnect 204. Similarly, the capacitor 217 may be electrically coupled to the second die 206 through the via 214, the pad 216, the interconnect 232, the interconnect 254, the interconnect 208, and/or the interconnect 209.” Lee, [6:62-7:8].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Lee discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p> <p>“FIG. 2 illustrates that a portion of the set of interconnects 232 in the second encapsulation layer 230 is coupled to the pad 216 in the substrate 210. In some implementations, the set of interconnects 209 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). The set of interconnects 209 is coupled to the set of interconnects 208. The second redistribution portion 250 is coupled to the first surface of the second encapsulation layer 230. The second redistribution portion 250 includes a third dielectric layer 252, a second set of redistribution interconnects 254, a third set of redistribution interconnects 256, and a set of under bump metallization (UBM) layers 258. In some implementations, the second</p>

redistribution portion 250 may include one, two, or more than two sets of redistribution interconnects. The first set of redistribution interconnects 254 is coupled to the set of interconnects 209 and the set of interconnects 232. In some implementations, the third dielectric layer 252 includes one or more dielectric layers. A set of solder balls 260 is coupled to the set of UBM layers 258. In some implementations, the UBM layers 258 are optional. In such instances, the set of solder balls 260 may be directly coupled to one of the redistribution interconnects." Lee, [5:53-6:9].

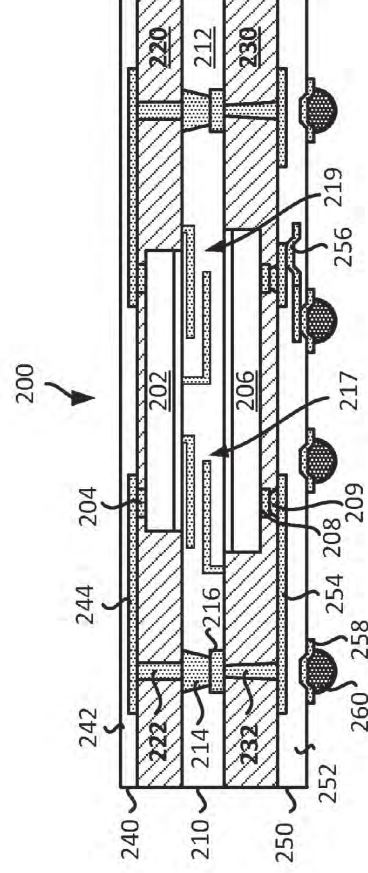


FIG. 2

Lee, FIG. 2

“In some implementations, at least one of the capacitors 217 and/or 219 may be electrically coupled to at least the first die 202 and/or the second die 206. For example, the capacitor 217 may be electrically coupled to the first die 202 through the via 214, the interconnect 222, the

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>interconnect 244, and/or the interconnect 204. Similarly, the capacitor 217 may be electrically coupled to the second die 206 through the via 214, the pad 216, the interconnect 232, the interconnect 254, the interconnect 208, and/or the interconnect 209.” Lee, [6:66-7:8].</p> <p>“In some implementations, at least one of the capacitors 417 and/or 419 may be electrically coupled to at least the first die 402 and/or the second die 406. For example, the capacitor 417 may be electrically coupled to the first die 402 through the via 414, the interconnect 422, the interconnect 444, and/or the interconnect 404. Similarly, the capacitor 417 may be electrically coupled to the second die 406 through the via 414, the pad 416, the interconnect 432, the interconnect 454, the interconnect 408, and/or the interconnect 409.” Lee, [8:28-8:37].</p> <p>“FIG. 4 illustrates that a portion of the set of interconnects 432 in the second encapsulation layer 430 is coupled to the pad 416 in the substrate 410. In some implementations, the set of interconnects 409 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). The set of interconnects 409 is coupled to the set of interconnects 408. The second redistribution portion 450 is coupled to the first surface of the second encapsulation layer 430. The second redistribution portion 450 includes a fifth dielectric layer 452, a second set of redistribution interconnects 454, a third set of redistribution interconnects 456, and a set of under bump metallization (UBM) layers 458. In some implementations, the second redistribution portion 450 may include one, two, or more than two sets of redistribution interconnects. The first set of redistribution interconnects 454 is coupled to the set of interconnects 409 and the set of interconnects 432. In some implementations, the fifth dielectric layer 452 includes one or more dielectric layers. A set of solder balls 460 is coupled to the set of UBM layers 458. In some implementations, the UBM layers 458 is optional. In</p>
--	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>such instances, the set of solder balls 460 may be directly coupled to one of the redistribution interconnects.” Lee, [9:39-9:61].</p> <p>“FIG. 6 illustrates that a portion of the set of interconnects 632 in the second encapsulation layer 630 is coupled to the pad 616 in the substrate 610. In some implementations, the set of interconnects 609 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). The set of interconnects 609 is coupled to the set of interconnects 608. The second redistribution portion 650 is coupled to the first surface of the second encapsulation layer 630. The second redistribution portion 650 includes a third dielectric layer 652, a second set of redistribution interconnects 654, a third set of redistribution interconnects 656, and a set of under bump metallization (UBM) layers 658. In some implementations, the second redistribution portion 650 may include one, two, or more than two sets of redistribution interconnects. The first set of redistribution interconnects 654 is coupled to the set of interconnects 609 and the set of interconnects 632. In some implementations, the third dielectric layer 652 includes one or more dielectric layers.” Lee, [12:21-12:39].</p> <p>“In some implementations, the capacitor 618 may be electrically coupled to at least the first die 602 and/or the second die 606. For example, the capacitor 618 may be electrically coupled to the first die 602 through the via 614, the interconnect 622, the interconnect 644, and/or the interconnect 604. Similarly, the capacitor 618 may be electrically coupled to the second die 606 through the via 614, the pad 616, the interconnect 632, the interconnect 654, the interconnect 608, and/or the interconnect 609.” Lee, [12:44-12:52].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Lee discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“The second die 206 includes a back side and a front side (e.g., active side). The front side is coupled to a set of interconnects 208. The set of interconnects 208 may be one of at least pads and/or pillars in some implementations. The back side of the second die 206 is coupled to the second surface of the substrate 210. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the second die 206 to the second surface of the substrate 210. As shown in FIG. 2, the back side of the second die 206 is facing the substrate 210 while the front side (e.g., active side) of the second die 206 is facing away from the substrate 210. The second encapsulation layer 230 encapsulates the second die 206 and the set of interconnects 208.” Lee, [6:1-6:13].</p>
---	---

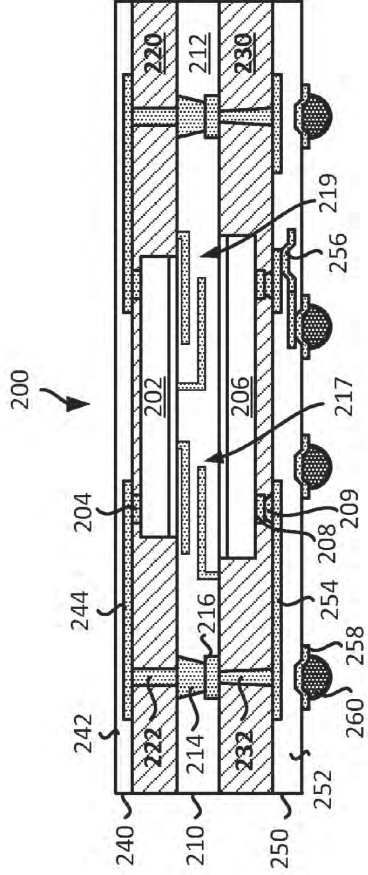


FIG. 2

Lee, FIG. 2

“It should be noted that the substrate 210 may include additional interconnects (e.g., traces, vias), which are not shown for the purpose of clarity. These un-shown (or not visible) interconnects may couple the capacitors 217 and/or 219 to the via 214 and/or pad 216 in some implementations. In some implementations, at least one of the capacitors 217 and/or 219 may be electrically coupled to at least the first die 202 and/or the second die 206. For example, the capacitor 217 may be electrically coupled to the first die 202 through the via 214, the interconnect 222, the interconnect 244, and/or the interconnect 204. Similarly, the capacitor 219 may be electrically coupled to the second die 206 through the via 214, the pad 216, the interconnect 232, the interconnect 254, the interconnect 208, and/or the interconnect 209.”
Lee, [6:62-7:8].

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Lee discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The second die 206 includes a back side and a front side (e.g., active side). The front side is coupled to a set of interconnects 208. The set of interconnects 208 may be one of at least pads and/or pillars in some implementations. The back side of the second die 206 is coupled to the second surface of the substrate 210. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the second die 206 to the second surface of the substrate 210. As shown in FIG. 2, the back side of the second die 206 is facing the substrate 210 while the front side (e.g., active side) of the second die 206 is facing away from the substrate 210. The second encapsulation layer 230 encapsulates the second die 206 and the set of interconnects 208” Lee, [6:1-6:13].</p>

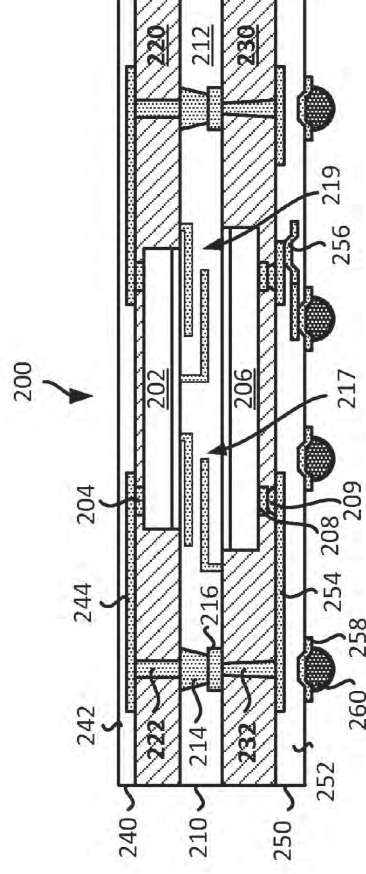


FIG. 2

Lee, FIG. 2

To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

Lee discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

See, e.g.:

“FIG. 2 illustrates an exemplary package on package (PoP) integrated device 200 that includes a capacitor in a substrate. As shown in FIG. 2, the integrated device 200 (e.g.,

integrated package device) includes a first die 202, a second die 206, a substrate 210, a first encapsulation layer 220, a second encapsulation layer 230, a first redistribution portion 240, and a second redistribution portion 250. The substrate 210 includes a dielectric layer 212, a via 214, a pad 216, a first capacitor 217 and a second capacitor 219. In some implementations, the substrate 210 is a laminate substrate. The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 212 may include several dielectric layers. In some implementations, the dielectric layers may be the same material. The via 214 is coupled to the pad 216. In some implementations, the combination of the via 214 and the pad 216 traverses from the first surface of the substrate 210 to the second surface of the substrate 210. In some implementations, the via 214 and/or the pad 216 is a form of an interconnect that traverses the substrate 210.” Lee, [5:3-5:23].

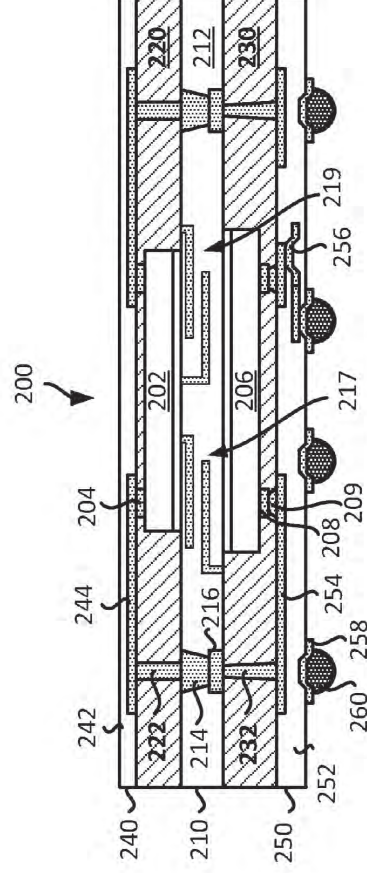


FIG. 2

Lee, FIG. 2

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Lee discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“As shown in FIG. 2, the back side of the first die 202 is facing the substrate 210 while the front side (e.g., active side) of the first die 202 is facing away from the substrate 210. The first encapsulation layer 220 encapsulates the first die 202 and the set of die interconnects 204. In some implementations, the first encapsulation layer 220 is one of at least a mold, a polymer, and/or a photo-etchable material. In some implementations, a photo-etchable material is a material that may be etched through a photo etching process. The first encapsulation layer 220 includes a set of interconnects 222. In some implementations, the set of interconnects 222 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some implementations, the set of interconnects 222 traverses from a first surface (e.g., top surface) of the first encapsulation layer 220 to a second surface (e.g., bottom surface) of the first encapsulation layer 220. FIG. 2 illustrates that a portion of the set of</p>

interconnects 222 in the first encapsulation layer 220 is coupled to the via 214 in the substrate 210.” Lee, [5:38-5:57].

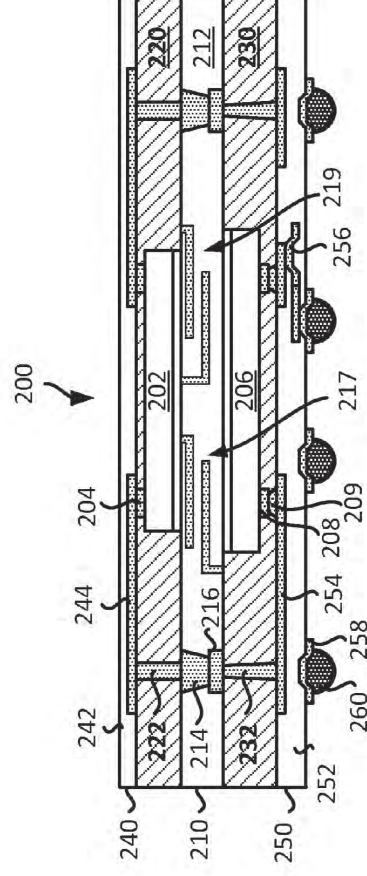


FIG. 2

Lee, FIG. 2

“The back side of the first die 402 is coupled to the first surface of the substrate 410. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the first die 402 to the first surface of the substrate 410. As shown in FIG. 4, the back side of the first die 402 is facing the substrate 410 while the front side (e.g., active side) of the first die 402 is facing away from the substrate 410. The first encapsulation layer 420 encapsulates the first die 402 and the set of die interconnects 404. In some implementations, the first encapsulation layer 420 is one of at least a mold, a polymer, and/or a photo-etchable material. In some implementations, a photo-etchable material is a material that may be etched through a photo

	<p>etching process. The first encapsulation layer 420 includes a set of interconnects 422. In some implementations, the set of interconnects 422 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some implementations, the set of interconnects 422 traverses from a first surface (e.g., top surface) of the first encapsulation layer 420 to a second surface (e.g., bottom surface) of the first encapsulation layer 420. FIG. 4 illustrates that a portion of the set of interconnects 422 in the first encapsulation layer 420 is coupled to the via 414 in the substrate 410. The first redistribution portion 440 is coupled to the first surface of the first encapsulation layer 420.” Lee, [8:48-9:6].</p> <p>“The capacitor 618 is further described in detail below in FIG. 7. The first die 602 includes a back side and a front side (e.g., active side). The front side is coupled to a set of die interconnects 604. The set of die interconnects 604 may be one of at least pads and/or pillars in some implementations. The back side of the first die 602 is coupled to the first surface of the substrate 610. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the first die 602 to the first surface of the substrate 610. As shown in FIG. 6, the back side of the first die 602 is facing the substrate 610 while the front side (e.g., active side) of the first die 602 is facing away from the substrate 610. The first encapsulation layer 620 encapsulates the first die 602 and the set of die interconnects 604. In some implementations, the first encapsulation layer 620 is one of at least a mold, a polymer, and/or a photo-etchable material. In some implementations, a photo-etchable material is a material that may be etched through a photo etching process. The first encapsulation layer 620 includes a set of interconnects 622. In some implementations, the set of interconnects 622 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some implementations, the set of interconnects 622 traverses from a first surface (e.g., top surface) of the first encapsulation layer 620 to a second surface (e.g., bottom surface) of the first encapsulation layer 620.” Lee, [11:25-11:50].</p>
--	---

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>“Stage 3 illustrates a state after a first die 1002 is provided and coupled to a first surface (e.g., top surface) of the substrate 1000. The first die 1002 may include a back side and a front side (e.g., active side). In some implementations, the back side of the first die 1002 is coupled to the first surface of the substrate 1000 using a bonding agent (e.g., glue). Stage 4 illustrates a state after a first encapsulation layer 1004 is provided (e.g., formed) on the first surface of the substrate 1000. The first encapsulation layer 1004 covers the first die 1002 and at least some of the interconnect 1005. Stage 5 illustrates a state after a first redistribution interconnect 1006 is provided (e.g., formed) on the first encapsulation layer 1004. In some implementations, the first redistribution interconnect 1006 is formed by forming one or more metal layers and selectively etching portions of the one or more metal layers. The first redistribution interconnect 1006 is coupled to the via 1001 and the first die 1002. Stage 6 illustrates a state after a first dielectric layer 1008 is provided (e.g., formed) on the first encapsulation layer 1004 and the first redistribution interconnect 1006.” Lee, [17:13-17:32].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate,	Lee discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	<p>stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, e.g.:</p> <p>“FIG. 2 illustrates an exemplary package on package (PoP) integrated device 200 that includes a capacitor in a substrate. As shown in FIG. 2, the integrated device 200 (e.g., integrated package device) includes a first die 202, a second die 206, a substrate 210, a first encapsulation layer 220, a second encapsulation layer 230, a first redistribution portion 240, and a second redistribution portion 250. The substrate 210 includes a dielectric layer 212, a via 214, a pad 216, a first capacitor 217 and a second capacitor 219. In some implementations, the substrate 210 is a laminate substrate. The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface).” Lee, [5:3-5:15].</p> <p>“The first die 202 includes a back side and a front side (e.g., active side). The front side is coupled to a set of die interconnects 204. The set of die interconnects 204 may be one of at least pads and/or pillars in some implementations. The back side of the first die 202 is coupled to the first surface of the substrate 210. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the first die 202 to the first surface of the substrate 210. As shown in FIG. 2, the back side of the first die 202 is facing the substrate 210 while the front side (e.g., active side) of the first die 202 is facing away from the substrate 210. The first encapsulation layer 220 encapsulates the first die 202 and the set of die interconnects 204.” Lee, [5:31-5:43].</p>
---	--

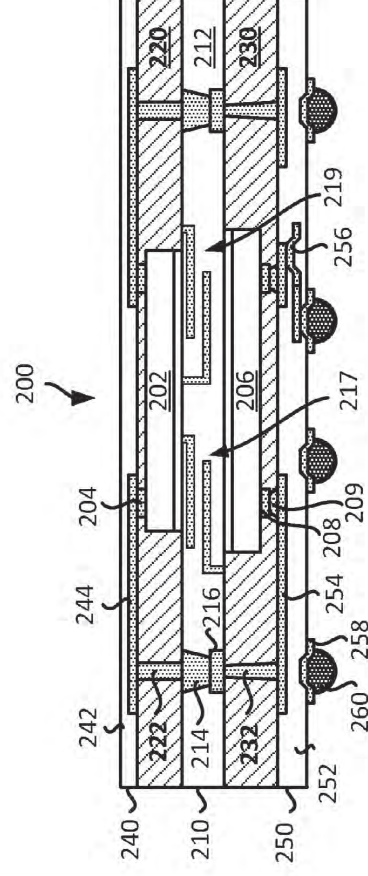


FIG. 2

Lee, FIG. 2

“The second die 206 includes a back side and a front side (e.g., active side). The front side is coupled to a set of interconnects 208. The set of interconnects 208 may be one of at least pads and/or pillars in some implementations. The back side of the second die 206 is coupled to the second surface of the substrate 210. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the second die 206 to the second surface of the substrate 210. As shown in FIG. 2, the back side of the second die 206 is facing the substrate 210 while the front side (e.g., active side) of the second die 206 is facing away from the substrate 210. The second encapsulation layer 230 encapsulates the second die 206 and the set of interconnects 208.” Lee, [6:1-6:13].

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>“The first die 402 includes a back side and a front side (e.g., active side). The front side is coupled to a set of die interconnects 404. The set of die interconnects 404 may be one of at least pads and/or pillars in some implementations. The back side of the first die 402 is coupled to the first surface of the substrate 410. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the first die 402 to the first surface of the substrate 410. As shown in FIG. 4, the back side of the first die 402 is facing the substrate 410 while the front side (e.g., active side) of the first die 402 is facing away from the substrate 410. The first encapsulation layer 420 encapsulates the first die 402 and the set of die interconnects 404.” Lee, [8:45-8:57].</p> <p>“The second die 406 includes a back side and a front side (e.g., active side). The front side is coupled to a set of interconnects 408. The set of interconnects 408 may be one of at least pads and/or pillars in some implementations. The back side of the second die 406 is coupled to the second surface of the substrate 410. In some implementations, a bonding agent (e.g., glue) is used to couple the back side of the second die 406 to the second surface of the substrate 410. As shown in FIG. 4, the back side of the second die 406 is facing the substrate 410 while the front side (e.g., active side) of the second die 406 is facing away from the substrate 410. The second encapsulation layer 430 encapsulates the second die 406 and the set of interconnects 408.” Lee, [9:15-9:27].</p> <p>“Stage 3 illustrates a state after a first die 1002 is provided and coupled to a first surface (e.g., top surface) of the substrate 1000. The first die 1002 may include a back side and a front side (e.g., active side). In some implementations, the back side of the first die 1002 is coupled to the first surface of the substrate 1000 using a bonding agent (e.g., glue). Stage 4 illustrates a state after a first encapsulation layer 1004 is provided (e.g., formed) on the first surface of the substrate 1000. The first encapsulation layer 1004 covers the first die 1002 and at least some of the interconnect 1005.” Lee, [17:13-17:22].</p>
--	---

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Lee discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 2 illustrates that a portion of the set of interconnects 222 in the first encapsulation layer 220 is coupled to the via 214 in the substrate 210. The first redistribution portion 240 is coupled to the first surface of the first encapsulation layer 220. The first redistribution portion 240 includes a second dielectric layer 242 and a first set of redistribution interconnects 244. In some implementations, the first redistribution portion 240 may include more than one set of redistribution interconnects. The first set of redistribution interconnects 244 is coupled to the set of die interconnects 204 and the set of interconnects 222.” Lee, [5:54-5:65].</p>

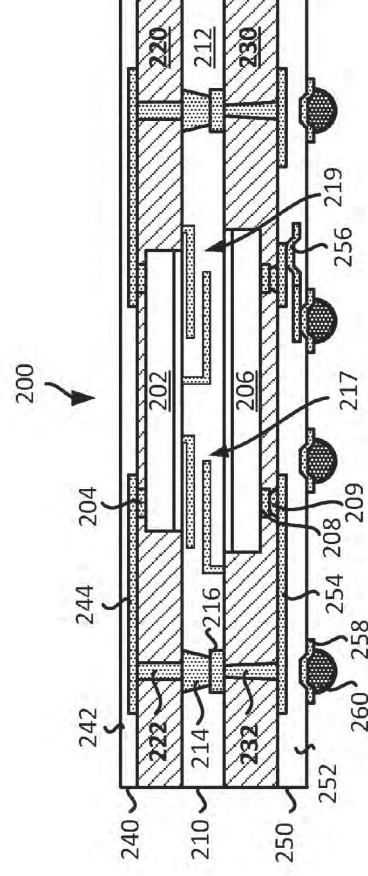


FIG. 2

Lee, FIG. 2

“FIG. 4 illustrates that a portion of the set of interconnects 422 in the first encapsulation layer 420 is coupled to the via 414 in the substrate 410. The first redistribution portion 440 is coupled to the first surface of the first encapsulation layer 420. The first redistribution portion 440 includes a fourth dielectric layer 442 and a first set of redistribution interconnects 444. In some implementations, the first redistribution portion 440 may include more than one set of redistribution interconnects. The first set of redistribution interconnects 444 is coupled to the set of die interconnects 404 and the set of interconnects 422.” Lee, [9:1-9:12].

“FIG. 4 illustrates that a portion of the set of interconnects 432 in the second encapsulation layer 430 is coupled to the pad 416 in the substrate 410. In some implementations, the set of interconnects 409 is one of at least a through encapsulation via (TEV) and/or a through mold

	<p>via (TMV). The set of interconnects 409 is coupled to the set of interconnects 408. The second redistribution portion 450 is coupled to the first surface of the second encapsulation layer 430.” Lee, [9:39-9:47].</p> <p>“FIG. 6 illustrates that a portion of the set of interconnects 622 in the first encapsulation layer 620 is coupled to the via 614 in the substrate 610. The first redistribution portion 640 is coupled to the first surface of the first encapsulation layer 620. The first redistribution portion 640 includes a second dielectric layer 642 and a first set of redistribution interconnects 644. In some implementations, the first redistribution portion 640 may include more than one set of redistribution interconnects. The first set of redistribution interconnects 644 is coupled to the set of die interconnects 604 and the set of interconnects 622.” Lee, [11:50-11:61].</p> <p>“FIG. 6 illustrates that a portion of the set of interconnects 632 in the second encapsulation layer 630 is coupled to the pad 616 in the substrate 610. In some implementations, the set of interconnects 609 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). The set of interconnects 609 is coupled to the set of interconnects 608.” Lee, [12:21-12:27].</p> <p>“Stage 10 illustrates a state after the first cavity 1015 and the second cavity 1017 are filled with an electrically conductive material to form an interconnect 1016, and an interconnect 1018, respectively. In some implementations, the interconnect 1016 is a via (e.g., through encapsulation via, through mold via). In some implementations, the interconnect 1018 is a via (e.g., through encapsulation via, through mold via). Stage 11 illustrates a state after a second redistribution interconnect 1020 is provided (e.g., formed) on the second encapsulation layer 1014. In some implementations, the second redistribution interconnect 1020 is formed by forming one or more metal layers and selectively etching portions of the</p>
--	---

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>one or more metal layers. The second redistribution interconnect 1020 may be coupled to the interconnect 1005 and the second die 1012.” Lee, [17:57-18:4].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Lee discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 2 illustrates an exemplary package on package (PoP) integrated device 200 that includes a capacitor in a substrate. As shown in FIG. 2, the integrated device 200 (e.g., integrated package device) includes a first die 202, a second die 206, a substrate 210, a first encapsulation layer 220, a second encapsulation layer 230, a first redistribution portion 240, and a second redistribution portion 250. The substrate 210 includes a dielectric layer 212, a</p>

	<p>via 214, a pad 216, a first capacitor 217 and a second capacitor 219. In some implementations, the substrate 210 is a laminate substrate. The substrate 210 includes a first surface (e.g., top surface) and a second surface (e.g., bottom surface). In some implementations, the dielectric layer 212 may include several dielectric layers. In some implementations, the dielectric layers may be the same material. The via 214 is coupled to the pad 216. In some implementations, the combination of the via 214 and the pad 216 traverses from the first surface of the substrate 210 to the second surface of the substrate 210. In some implementations, the via 214 and/or the pad 216 is a form of an interconnect that traverses the substrate 210.” Lee, [5:3-5:23].</p> <div></div> <p style="text-align: center;">FIG. 2</p> <p>Lee, FIG. 2</p> <p>“FIG. 2 illustrates that a portion of the set of interconnects 222 in the first encapsulation layer 220 is coupled to the via 214 in the substrate 210.” Lee, [5:54-5:57].</p>
--	--

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>“The first set of redistribution interconnects 244 is coupled to the set of die interconnects 204 and the set of interconnects 222. In some implementations, the second dielectric layer 242 includes one or more dielectric layers.” Lee, [5:63-5:67].</p> <p>“The first set of redistribution interconnects 254 is coupled to the set of interconnects 209 and the set of interconnects 232.” Lee, [6:40-6:41].</p> <p>“Stage 10 illustrates a state after the first cavity 1015 and the second cavity 1017 are filled with an electrically conductive material to form an interconnect 1016, and an interconnect 1018, respectively. In some implementations, the interconnect 1016 is a via (e.g., through encapsulation via, through mold via). In some implementations, the interconnect 1018 is a via (e.g., through encapsulation via, through mold via).” Lee, [17:57-17:63].</p> <p>“Stage 11 illustrates a state after a second redistribution interconnect 1020 is provided (e.g., formed) on the second encapsulation layer 1014. In some implementations, the second redistribution interconnect 1020 is formed by forming one or more metal layers and selectively etching portions of the one or more metal layers. The second redistribution interconnect 1020 may be coupled to the interconnect 1005 and the second die 1012.” Lee, [17:64-18:4].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the plurality of top metal pillars of the bottom package substrate via the plurality of metal pillars of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Lee discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The via 214 is coupled to the pad 216. In some implementations, the combination of the via 214 and the pad 216 traverses from the first surface of the substrate 210 to the second surface of the substrate 210. In some implementations, the via 214 and/or the pad 216 is a form of an interconnect that traverses the substrate 210.” Lee, [5:18-5:23].</p> <p>“FIG. 2, the back side of the first die 202 is facing the substrate 210 while the front side (e.g., active side) of the first die 202 is facing away from the substrate 210. The first encapsulation layer 220 encapsulates the first die 202 and the set of die interconnects 204. In some implementations, the first encapsulation layer 220 is one of at least a mold, a polymer, and/or a photo-etchable material. In some implementations, a photo-etchable material is a material that may be etched through a photo etching process. The first encapsulation layer 220 includes a set of interconnects 222. In some implementations, the set of interconnects 222 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). In some</p>

implementations, the set of interconnects 222 traverses from a first surface (e.g., top surface) of the first encapsulation layer 220 to a second surface (e.g., bottom surface) of the first encapsulation layer 220. FIG. 2 illustrates that a portion of the set of interconnects 222 in the first encapsulation layer 220 is coupled to the via 214 in the substrate 210. The first redistribution portion 240 is coupled to the first surface of the first encapsulation layer 220.” Lee, [5:38-5:59].

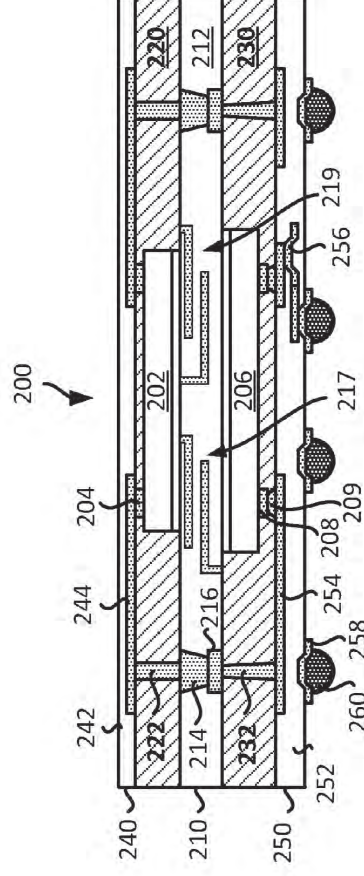


FIG. 2

Lee, FIG. 2

“FIG. 2 illustrates that a portion of the set of interconnects 232 in the second encapsulation layer 230 is coupled to the pad 216 in the substrate 210. In some implementations, the set of interconnects 209 is one of at least a through encapsulation via (TEV) and/or a through mold via (TMV). The set of interconnects 209 is coupled to the set of interconnects 208. The

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>second redistribution portion 250 is coupled to the first surface of the second encapsulation layer 230. The second redistribution portion 250 includes a third dielectric layer 252, a second set of redistribution interconnects 254, a third set of redistribution interconnects 256, and a set of under bump metallization (UBM) layers 258. In some implementations, the second redistribution portion 250 may include one, two, or more than two sets of redistribution interconnects. The first set of redistribution interconnects 254 is coupled to the set of interconnects 209 and the set of interconnects 232.” Lee, [6:25-6:41].</p> <p>“Stage 13 illustrates a state after the cavity 821 is filled with a metal material to define an interconnect 824. In some implementations, the interconnect 824 is a via that is coupled to the pad 822. Different implementations may use different processes to fill the cavity 821. In some implementations, a plating process is used. In some implementations, the cavity 821 is filled with a conducting paste.” Lee, [14:65-15:4].</p> <p>“Stage 2 illustrates a state after an interconnect 1005 is provided (e.g., formed) on the substrate 1000. Specifically, the interconnect 1005 is provided over the via 1001. In some implementations, the interconnect 1005 is a via (e.g., through encapsulation via, through mold via). The interconnect 1005 may be formed on the substrate through one or more plating processes.” Lee, [17:6-17:12].</p> <p>“Stage 10 illustrates a state after the first cavity 1015 and the second cavity 1017 are filled with an electrically conductive material to form an interconnect 1016, and an interconnect 1018, respectively. In some implementations, the interconnect 1016 is a via (e.g., through encapsulation via, through mold via). In some implementations, the interconnect 1018 is a via (e.g., through encapsulation via, through mold via). Stage 11 illustrates a state after a second redistribution interconnect 1020 is provided (e.g., formed) on the second encapsulation layer 1014. In some implementations, the second redistribution interconnect</p>
--	---

Appendix A-19 - Invalidity of U.S. Patent No. 9859202 in view of Lee - U.S. Patent No. 9368566

	<p>1020 is formed by forming one or more metal layers and selectively etching portions of the one or more metal layers. The second redistribution interconnect 1020 may be coupled to the interconnect 1005 and the second die 1012.” Lee, [17:57-18:4].</p> <p>To the extent Plaintiff contends that Lee fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

U.S. Patent No. 7514774 (“Leung”) is titled Stacked Multi-Chip Package with EMI Shielding and lists Lap Wai Leung, Yu-Chih Chen, Man-Lung Sham, and Chang-Hwa Chung, as inventors. Leung is assigned to Hong Kong Applied Science Technology Research Institute Company Limited. Leung anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Leung is a U.S. patent that was filed September 15, 2006 and published March 20, 2008. Leung is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Leung, or otherwise rendered obvious by disclosures and teachings of Leung, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Leung does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Leung with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Leung, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Leung “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Leung or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Leung set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Leung discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“In view of the forgoing, there is disclosed herein a stacked multi-chip package with an EMI shielded space comprising a first substrate having a first ground plane laminated between dielectric layers of the first substrate, an electronic component mounted of a first side of the first substrate layer and a second substrate having a second ground plane laminated between dielectric layers of the second substrate, wherein the first substrate is mounted to the second substrate by a grid array of metallic connecting nodes with the electronic component positioned between the substrates, and at least a group of the metallic connecting nodes</p>

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>surround the electronic component and are electrically connected to both the first ground plane and the second ground plane.” Leung, [1:57-2:2].</p> <p>“More generally, there is disclosed herein a stacked electronic component package comprising a first substrate, a second substrate mounted to the first substrate, an electronic component positioned between the substrates, a first conductive plane associated with the first substrate, a second conductive plane associated with the second substrate, and a plurality of conductive nodes surrounding the electronic component and interconnected with both the first and second conductive planes.” Leung, [2:14-2:22].</p> <p>“Generally the invention is a stacked multi-chip package with first and second substrates mounted together by a grid array of metallic connecting nodes, such as a solder Ball Grid Array. Each substrate has a ground plane laminated between dielectric layers of the substrate. A sensitive or EMI generating component is mounted between the first and second substrates and is surrounded by a group of the metallic connecting nodes that are also electrically connected to the ground planes of both substrates to form a conductive Faraday cage about the component.” Leung, [2:52-2:60].</p>
--	---

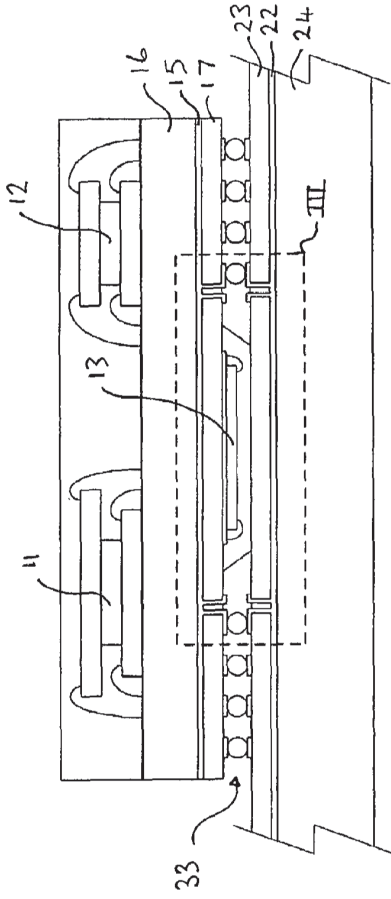


Figure 2

Leung, FIG. 2

“In the drawings there is depicted an exemplary embodiment of the invention as practiced in a multi-chip integrated package having both radio frequency (RF) and digital integrated circuit (IC) chips packaged together in a stacked substrate arrangement. This type of arrangement is often termed a stacked multi-chip module (MCM).” Leung, [2:62-2:67].

“Referring to the drawings generally, in the exemplary embodiment a MCM 1 is mounted to a main system board, or motherboard 2, and interconnected thereto by a Ball Grid Array (BGA) 3. The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side.” Leung, [3:21-3:26].

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern.” Leung, [3:47-3:51].</p>
<p>[1.A] a bottom package substrate;</p>	<p>Leung discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to the drawings generally, in the exemplary embodiment a MCM 1 is mounted to a main system board, or motherboard 2, and interconnected thereto by a Ball Grid Array (BGA) 3. The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side. The digital IC chips 11, 12 are a memory chip and a logic chip for controlling the RF module 1. The RF chip 13 must be thin enough to mount in the BGA 3 stand-off space 33 between the RF module 1 and the main board 2. A typical RF chip is 15-25 mils thick: too thick for a robust BGA stand-off distance. However, chips can be thinned to between 5-7 mils. Thinning of chips is conventional in the art of IC technology and manufacture. The RF module supporting substrate 10 has printed circuits on one or more of its surfaces and bonding pads for mounted the chips 11, 12, 13 to the supporting substrate 10 in known manner using interconnect wires 14.” Leung, [3:21-3:37].</p>

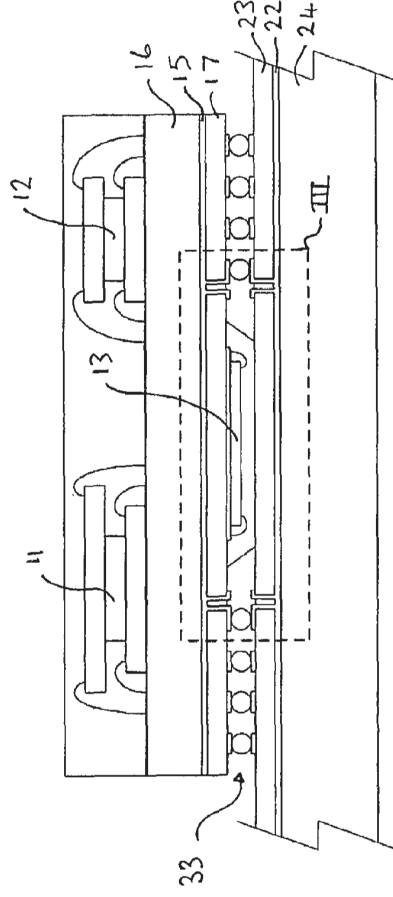


Figure 2

Leung, FIG. 2

“The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1. At the center of the bonding pad 21, 37 grid pattern is a corresponding RF chip space.” Leung, [3:62-3:67].

“The system substrate 20 is also of a type having one or more conductive ground planes 22 laminated between dielectric layers 23, 24. The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22.” Leung, [3:67-4:9].

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip. The Faraday cage comprises upper and lower ground planes 15, 22 of the RF module substrate 10 and the system substrate 20 interconnected around a shielded chip space 32 by a plurality of ground plane vias 34, 36 and the inner perimeter of BGA solder balls 31.” Leung, [4:9-4:17].</p> <p>“Referring to FIG. 7, a large conductive plane or pad 25 may be formed on the surface of one of the substrates, for example the system substrate 20, for receiving the inner perimeter solder balls 31 and forming one side of the shielding cage.” Leung, [5:5-5:10].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Leung discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Further, the exemplary embodiment is a single stack package having a single interconnecting support substrate bonded to a system substrate or motherboard.” Leung, [3:7-3:9].</p>

“Referring to the drawings generally, in the exemplary embodiment a MCM 1 is mounted to a main system board, or motherboard 2, and interconnected thereto by a Ball Grid Array (BGA) 3. The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side.” Leung, [3:21-3:26].

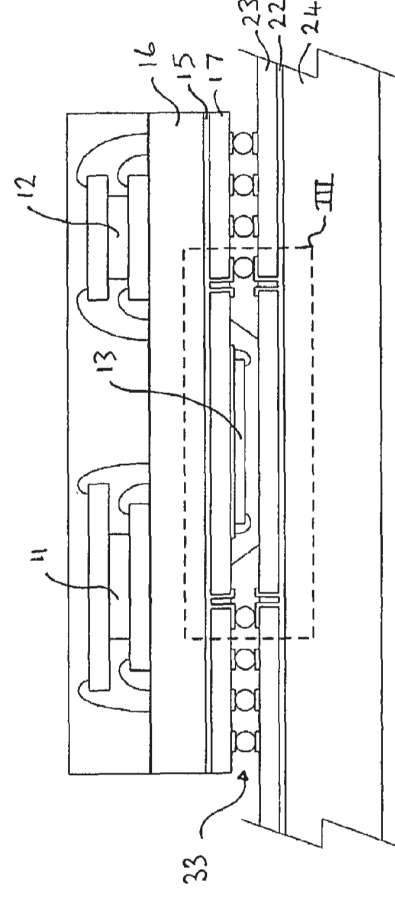


Figure 2

Leung, FIG. 2

“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern.” Leung, [3:47-3:51].

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip.” Leung, [4:9-4:12].</p> <p>“In the current invention, however, the RF chip 13, or other component, being shielded is located in the BGA stand-off space 33 between the substrates 10, 20. The thickness of the epoxy mold 40 encapsulating the RF chip 13 is therefore controlled and trimmed to act as a spacer for the BGA stand-off 33. The epoxy mold 40 of the RF chip 13 is in contact with the system substrate 20 to help support the module substrate 10 which prevents the BGA solder balls 30, 31 from collapsing during the reflow heating process.” Leung, [4:43-4:52].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Leung discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Generally the invention is a stacked multi-chip package with first and second substrates mounted together by a grid array of metallic connecting nodes, such as a solder Ball Grid Array. Each substrate has a ground plane laminated between dielectric layers of the substrate. A sensitive or EMI generating component is mounted between the first and second substrates and is surrounded by a group of the metallic connecting nodes that are also electrically</p>

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>connected to the ground planes of both substrates to form a conductive Faraday cage about the component.” Leung, [2:52-2:61].</p> <p>“The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side. The digital IC chips 11, 12 are a memory chip and a logic chip for controlling the RF module 1. The RF chip 13 must be thin enough to mount in the BGA 3 stand-off space 33 between the RF module 1 and the main board 2.” Leung, [3:24-3:30].</p> <p>“The RF module supporting substrate 10 is of a type having one or more conductive ground planes 15 laminated between dielectric layers 16, 17 of epoxy or other suitable non-conductive material. Substrates of this type are conventional in the art of printed circuit board technology and manufacture. The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3.” Leung, [3:42-3:48].</p> <p>“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern.” Leung, [3:47-3:51].</p> <p>“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip.” Leung, [4:9-4:12].</p> <p>“Typically, the gaps between solder balls 31 will be just a few hundreds micrometers, much less than the wavelength of the EMI waves, which will therefore generally not pass through the gaps between solder balls 31. To make the design more robust to vibration in use the</p>
--	---

chips and interconnect wires are overmolded in epoxy casings 40, 41. This is conventional in circuit board and MCM assembly and methods are known in the art. In the current invention, however, the RF chip 13, or other component, being shielded is located in the BGA stand-off space 33 between the substrates 10, 20. The thickness of the epoxy mold 40 encapsulating the RF chip 13 is therefore controlled and trimmed to act as a spacer for the BGA stand-off 33. The epoxy mold 40 of the RF chip 13 is in contact with the system substrate 20 to help support the module substrate 10 which prevents the BGA solder balls 30, 31 from collapsing during the reflow heating process. During the solder printing process, the volume of solder paste on each molding pad may be increased to enhance the tolerance to variations in solder ball height and substrate warpage." Leung, [4:36-4:54].

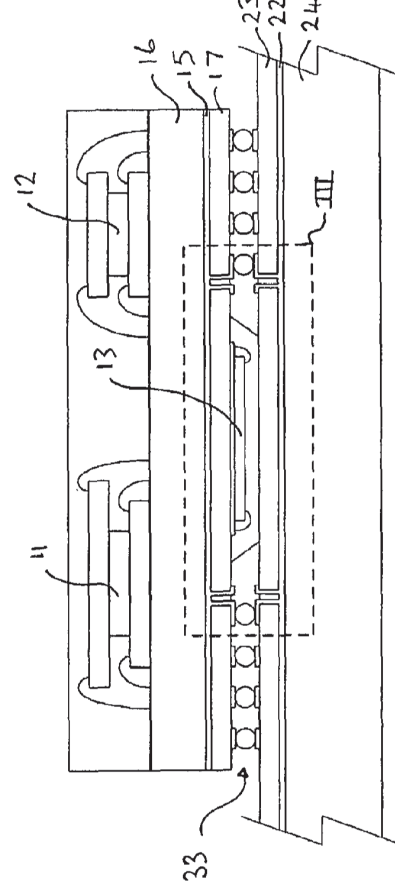


Figure 2

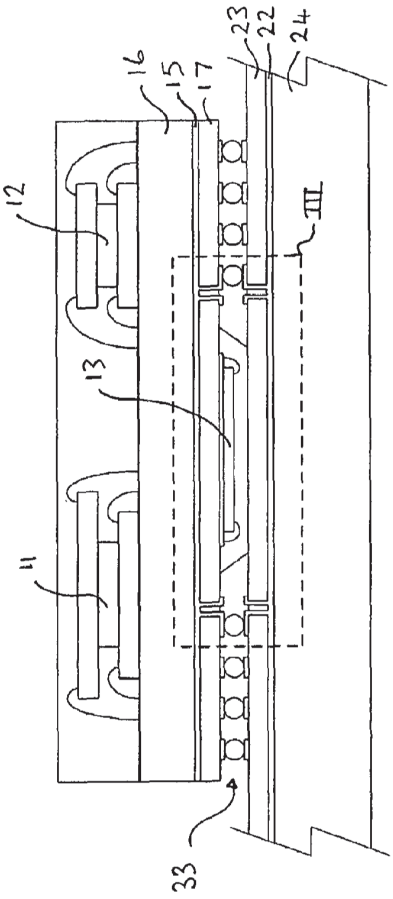
Leung, FIG. 2

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

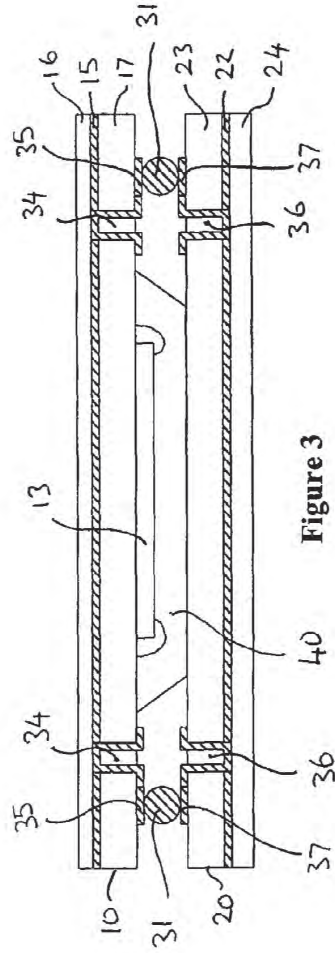
	<p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Leung discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Generally the invention is a stacked multi-chip package with first and second substrates mounted together by a grid array of metallic connecting nodes, such as a solder Ball Grid Array. Each substrate has a ground plane laminated between dielectric layers of the substrate. A sensitive or EMI generating component is mounted between the first and second substrates and is surrounded by a group of the metallic connecting nodes that are also electrically connected to the ground planes of both substrates to form a conductive Faraday cage about the component.” Leung, [2:52-2:61].</p> <p>“The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side. The digital IC chips 11, 12 are a memory chip and a logic chip for controlling the RF module 1. The RF chip 13 must be thin enough to mount in the BGA 3 stand-off space 33 between the RF module 1 and the main board 2.” Leung, [3:24-3:30].</p> <p>“The RF module supporting substrate 10 is of a type having one or more conductive ground planes 15 laminated between dielectric layers 16, 17 of epoxy or other suitable non-conductive material. Substrates of this type are conventional in the art of printed circuit board</p>

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>technology and manufacture. The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3.” Leung, [3:42-3:48].</p> <p>“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern.” Leung, [3:47-3:51].</p> <p>“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip.” Leung, [4:9-4:12].</p> <p>“Typically, the gaps between solder balls 31 will be just a few hundreds micrometers, much less than the wavelength of the EMI waves, which will therefore generally not pass through the gaps between solder balls 31. To make the design more robust to vibration in use the chips and interconnect wires are overmolded in epoxy casings 40, 41. This is conventional in circuit board and MCM assembly and methods are known in the art. In the current invention, however, the RF chip 13, or other component, being shielded is located in the BGA stand-off space 33 between the substrates 10, 20. The thickness of the epoxy mold 40 encapsulating the RF chip 13 is therefore controlled and trimmed to act as a spacer for the BGA stand-off 33. The epoxy mold 40 of the RF chip 13 is in contact with the system substrate 20 to help support the module substrate 10 which prevents the BGA solder balls 30, 31 from collapsing during the reflow heating process. During the solder printing process, the volume of solder paste on each molding pad may be increased to enhance the tolerance to variations in solder ball height and substrate warpage.” Leung, [4:36-4:54].</p>
--	--

	 <p style="text-align: center;">Figure 2</p> <p>Leung, FIG. 2</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Leung discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p>See, e.g.:</p> <p>“The RF module supporting substrate 10 is of a type having one or more conductive ground planes 15 laminated between dielectric layers 16, 17 of epoxy or other suitable non-</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	

conductive material. Substrates of this type are conventional in the art of printed circuit board technology and manufacture. The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern. A typical BGA grid pattern is shown in FIG. 5. Referring to FIG. 6, in a BGA 3 according to the invention the inner most solder balls 31 (shown in solid lines in FIG. 6) that form the perimeter of the RF chip space 32 are electrically connected to the ground plane 15 within the module substrate 10. This electrical connection is provided by ground plane vias 34 between the second surface of the substrate 10 and the ground plane 15. The ground plane vias 34 are connected with via bonding pads 35 or under bump metallization (UBM) solder on the second side of the module substrate 10 to which the inner perimeter of solder balls 31 are attached." Leung, [3:42-3:61].



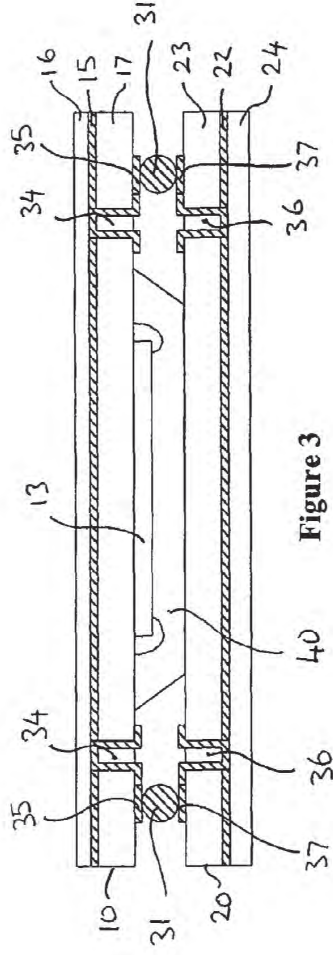
Leung, FIG. 3

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1. At the center of the bonding pad 21, 37 grid pattern is a corresponding RF chip space. The system substrate 20 is also of a type having one or more conductive ground planes 22 laminated between dielectric layers 23, 24. The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22. Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip. The Faraday cage comprises upper and lower ground planes 15, 22 of the RF module substrate 10 and the system substrate 20 interconnected around a shielded chip space 32 by a plurality of ground plane vias 34, 36 and the inner perimeter of BGA solder balls 31. The remaining solder balls 30 (shown in dashed lines in FIG. 6) of the BGA 3 provide electrical interconnection between the RF module 1 and the system 2 in known manner. This electrical interconnection between the RF module 1 and the system 2 is electrically isolated from the ground planes 15, 22 of the module and system substrates 10, 20.” Leung, [3:62-4:23].</p> <p>“To make the design more robust to vibration in use the chips and interconnect wires are overmolded in epoxy casings 40, 41. This is conventional in circuit board and MCM assembly and methods are known in the art. In the current invention, however, the RF chip 13, or other component, being shielded is located in the BGA stand-off space 33 between the substrates 10, 20. The thickness of the epoxy mold 40 encapsulating the RF chip 13 is therefore controlled and trimmed to act as a spacer for the BGA stand-off 33. The epoxy mold 40 of the RF chip 13 is in contact with the system substrate 20 to help support the</p>
--	---

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>module substrate 10 which prevents the BGA solder balls 30, 31 from collapsing during the reflow heating process. During the solder printing process, the volume of solder paste on each molding pad may be increased to enhance the tolerance to variations in solder ball height and substrate warpage.” Leung, [4:40-4:55].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Leung discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“This electrical connection is provided by ground plane vias 34 between the second surface of the substrate 10 and the ground plane 15. The ground plane vias 34 are connected with via bonding pads 35 or under bump metallization (UBM) solder on the second side of the module substrate 10 to which the inner perimeter of solder balls 31 are attached.” Leung, [3:56-3:61].</p>



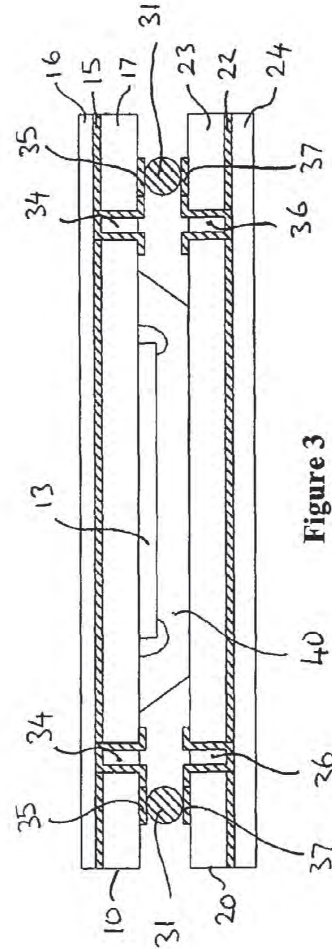
Leung, FIG. 3

“The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22.” Leung, [4:3-4:9].

“Additionally, referring to FIG. 9, a similar conductive plane or pad 26 may be formed on an opposite side of the substrate mounting the shielded electronic component and connected to the solder balls 31 by plated through-holes” Leung, [5:12-5:17].

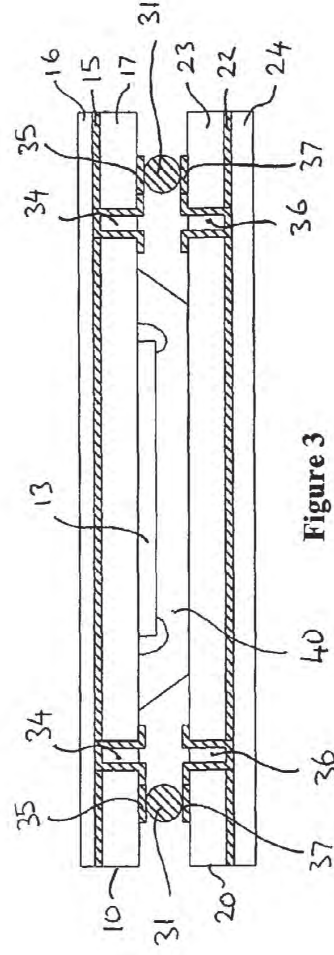
To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	
	<p>Leung discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, e.g.:  Figure 3</p> <p>Leung, FIG. 3</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>	<p>Leung discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

plurality of metal pillars of the spacer connector,

“This electrical connection is provided by ground plane vias 34 between the second surface of the substrate 10 and the ground plane 15. The ground plane vias 34 are connected with via bonding pads 35 or under bump metallization (UBM) solder on the second side of the module substrate 10 to which the inner perimeter of solder balls 31 are attached.” Leung, [3:56-3:61].

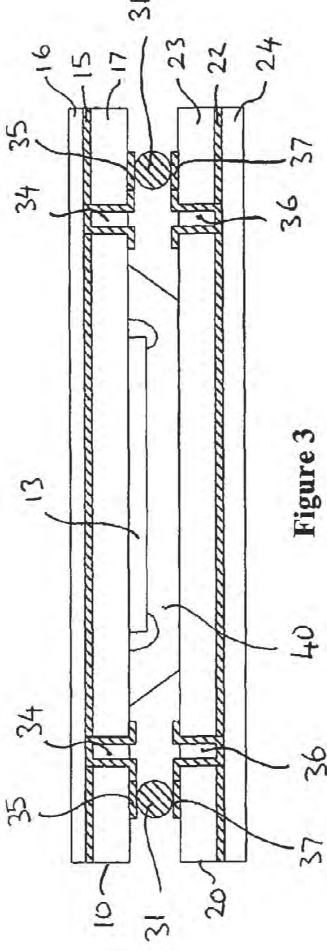


Leung, FIG. 3

“The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22.” Leung, [4:3-4:9].

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“Additionally, referring to FIG. 9, a similar conductive plane or pad 26 may be formed on an opposite side of the substrate mounting the shielded electronic component and connected to the solder balls 31 by plated through-holes” Leung, [5:12-5:17].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Leung discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1. At the center of the bonding pad 21, 37 grid pattern is a corresponding RF chip space. The system substrate 20 is also of a type having one or more conductive ground planes 22 laminated between dielectric layers 23, 24. The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22. Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip. The Faraday cage comprises</p>

	<p>upper and lower ground planes 15, 22 of the RF module substrate 10 and the system substrate 20 interconnected around a shielded chip space 32 by a plurality of ground plane vias 34, 36 and the inner perimeter of BGA solder balls 31. The remaining solder balls 30 (shown in dashed lines in FIG. 6) of the BGA 3 provide electrical interconnection between the RF module 1 and the system 2 in known manner. This electrical interconnection between the RF module 1 and the system 2 is electrically isolated from the ground planes 15, 22 of the module and system substrates 10, 20.” Leung, [3:62-4:23].</p> <div></div> <p>Leung, FIG. 3</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Leung discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern.” Leung, [3:47-3:51].</p> <p>“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3.” Leung, [3:47-3:48].</p> <p>“The ground plane vias 34 are connected with via bonding pads 35 or under bump metallization (UBM) solder on the second side of the module substrate 10 to which the inner perimeter of solder balls 31 are attached.” Leung, [3:58-3:61].</p> <p>“The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1.” Leung, [3:62-3:66].</p> <p>“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip.” Leung, [4:9-4:12].</p>
---	---

“The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22. Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip. The Faraday cage comprises upper and lower ground planes 15, 22 of the RF module substrate 10 and the system substrate 20 interconnected around a shielded chip space 32 by a plurality of ground plane vias 34, 36 and the inner perimeter of BGA solder balls 31. The remaining solder balls 30 (shown in dashed lines in FIG. 6) of the BGA 3 provide electrical interconnection between the RF module 1 and the system 2 in known manner.” Leung, [5:33-6:15].

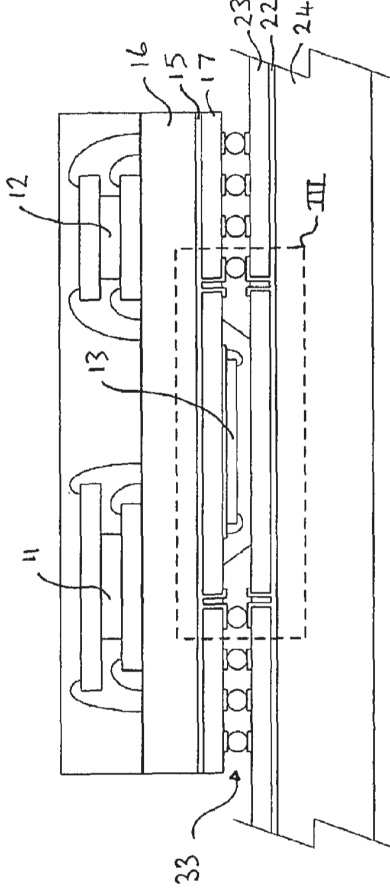


Figure 2

Leung, FIG. 2

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Leung discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Referring to the drawings generally, in the exemplary embodiment a MCM 1 is mounted to a main system board, or motherboard 2, and interconnected thereto by a Ball Grid Array (BGA) 3. The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side. The digital IC chips 11, 12 are a memory chip and a logic chip for controlling the RF module 1. The RF chip 13 must be thin enough to mount in the BGA 3 stand-off space 33 between the RF module 1 and the main board 2.” Leung, [3:21-3:30].</p> <p>“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern.” Leung, [3:47-3:51].</p> <p>“The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1. At the center of the bonding</p>

pad 21, 37 grid pattern is a corresponding RF chip space. The system substrate 20 is also of a type having one or more conductive ground planes 22 laminated between dielectric layers 23, 24. The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22. Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip. The Faraday cage comprises upper and lower ground planes 15, 22 of the RF module substrate 10 and the system substrate 20 interconnected around a shielded chip space 32 by a plurality of ground plane vias 34, 36 and the inner perimeter of BGA solder balls 31.” Leung, [3:62-4:17].

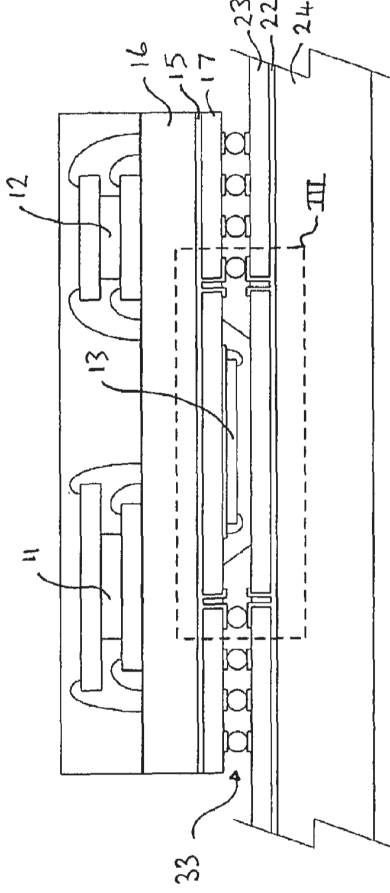


Figure 2

Leung, FIG. 2

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“To make the design more robust to vibration in use the chips and interconnect wires are overmolded in epoxy casings 40, 41. This is conventional in circuit board and MCM assembly and methods are known in the art. In the current invention, however, the RF chip 13, or other component, being shielded is located in the BGA stand-off space 33 between the substrates 10, 20. The thickness of the epoxy mold 40 encapsulating the RF chip 13 is therefore controlled and trimmed to act as a spacer for the BGA stand-off 33. The epoxy mold 40 of the RF chip 13 is in contact with the system substrate 20 to help support the module substrate 10 which prevents the BGA solder balls 30, 31 from collapsing during the reflow heating process.” Leung, [4:40-4:52].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Leung discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In the drawings there is depicted an exemplary embodiment of the invention as practiced in a multi-chip integrated package having both radio frequency (RF) and digital integrated circuit (IC) chips packaged together in a stacked substrate arrangement. This type of arrangement is often termed a stacked multi-chip module (MCM). This exemplary example is not however intended to limit the scope of use or functionality of the present invention. Those skilled in the art will appreciate that aspects of the invention may be practiced with</p>

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>other types of stacked substrate arrangements where it is desirable to isolated one or more component from noise interference in, or from introducing noise interference into, other parts of the package. Further, the exemplary embodiment is a single stack package having a single interconnecting support substrate bonded to a system substrate or motherboard. The skilled artisan will appreciate that the invention applies equally to multi-stack substrates and could be used between two or more interconnected substrates separately from the system substrate. A particular IC chip configuration is also described to illustrate the invention, and this is also not intended to limit the scope of use or functionality of the invention. Other chip types, components and/or their combinations may be used with the invention. The invention applies generally to any sensitive electronic or EMI generating component that must be isolated within a layered substrate package. Referring to the drawings generally, in the exemplary embodiment a MCM 1 is mounted to a main system board, or motherboard 2, and interconnected thereto by a Ball Grid Array (BGA) 3. The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side.” Leung, [1:29-1:63].</p>
--	--

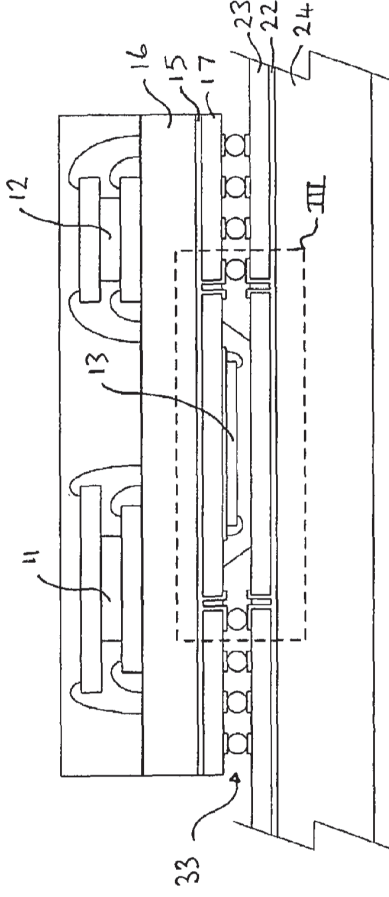


Figure 2

Leung, FIG. 2

“The RF module supporting substrate 10 is of a type having one or more conductive ground planes 15 laminated between dielectric layers 16, 17 of epoxy or other suitable non-conductive material. Substrates of this type are conventional in the art of printed circuit board technology and manufacture. The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern.” Leung, [3:42-3:51].

“The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1. At the center of the bonding pad 21, 37 grid pattern is a corresponding RF chip space.” Leung, [3:62-3:67].

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip.” Leung, [4:9-4:12].</p> <p>“To make the design more robust to vibration in use the chips and interconnect wires are overmolded in epoxy casings 40, 41. This is conventional in circuit board and MCM assembly and methods are known in the art. In the current invention, however, the RF chip 13, or other component, being shielded is located in the BGA stand-off space 33 between the substrates 10, 20. The thickness of the epoxy mold 40 encapsulating the RF chip 13 is therefore controlled and trimmed to act as a spacer for the BGA stand-off 33. The epoxy mold 40 of the RF chip 13 is in contact with the system substrate 20 to help support the module substrate 10 which prevents the BGA solder balls 30, 31 from collapsing during the reflow heating process.” Leung, [4:40-4:52].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Leung discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“Generally the invention is a stacked multi-chip package with first and second substrates mounted together by a grid array of metallic connecting nodes, such as a solder Ball Grid</p>

Array. Each substrate has a ground plane laminated between dielectric layers of the substrate. A sensitive or EMI generating component is mounted between the first and second substrates and is surrounded by a group of the metallic connecting nodes that are also electrically connected to the ground planes of both substrates to form a conductive Faraday cage about the component.” Leung, [2:52-2:61].

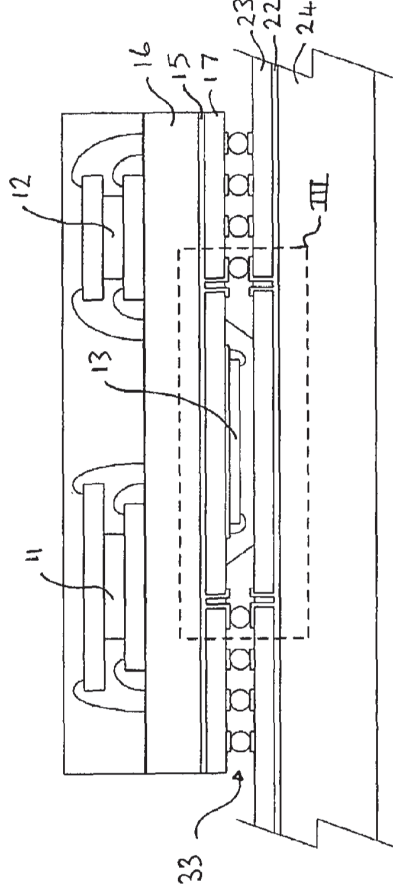


Figure 2

Leung, FIG. 2

“In the drawings there is depicted an exemplary embodiment of the invention as practiced in a multi-chip integrated package having both radio frequency (RF) and digital integrated circuit (IC) chips packaged together in a stacked substrate arrangement. This type of arrangement is often termed a stacked multi-chip module (MCM). This exemplary example is not however intended to limit the scope of use or functionality of the present invention. Those skilled in the art will appreciate that aspects of the invention may be practiced with

	<p>other types of stacked substrate arrangements where it is desirable to isolated one or more component from noise interference in, or from introducing noise interference into, other parts of the package. Further, the exemplary embodiment is a single stack package having a single interconnecting support substrate bonded to a system substrate or motherboard. The skilled artisan will appreciate that the invention applies equally to multi-stack substrates and could be used between two or more interconnected substrates separately from the system substrate. A particular IC chip configuration is also described to illustrate the invention, and this is also not intended to limit the scope of use or functionality of the invention. Other chip types, components and/or their combinations may be used with the invention. The invention applies generally to any sensitive electronic or EMI generating component that must be isolated within a layered substrate package.” Leung, [2:62-3:19].</p> <p>“Referring to the drawings generally, in the exemplary embodiment a MCM 1 is mounted to a main system board, or motherboard 2, and interconnected thereto by a Ball Grid Array (BGA) 3. The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side. The digital IC chips 11, 12 are a memory chip and a logic chip for controlling the RF module 1. The RF chip 13 must be thin enough to mount in the BGA 3 stand-off space 33 between the RF module 1 and the main board 2. A typical RF chip is 15-25 mils thick; too thick for a robust BGA stand-off distance. However, chips can be thinned to between 5-7 mils. Thinning of chips is conventional in the art of IC technology and manufacture. The RF module supporting substrate 10 has printed circuits on one or more of its surfaces and bonding pads for mounted the chips 11, 12, 13 to the supporting substrate 10 in known manner using interconnect wires 14. The digital IC and RF chips 11, 12, 13 are interconnected by plated through-holes (vias) in the substrate. The printed circuits and chip interconnect vias are not critical to the current invention and so are not shown for clarity.” Leung, [3:21-3:41].</p>
--	--

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“The RF module supporting substrate 10 is of a type having one or more conductive ground planes 15 laminated between dielectric layers 16, 17 of epoxy or other suitable non-conductive material. Substrates of this type are conventional in the art of printed circuit board technology and manufacture. The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern. A typical BGA grid pattern is shown in FIG. 5. Referring to FIG. 6, in a BGA 3 according to the invention the inner most solder balls 31 (shown in solid lines in FIG. 6) that form the perimeter of the RF chip space 32 are electrically connected to the ground plane 15 within the module substrate 10. This electrical connection is provided by ground plane vias 34 between the second surface of the substrate 10 and the ground plane 15. The ground plane vias 34 are connected with via bonding pads 35 or under bump metallization (UBM) solder on the second side of the module substrate 10 to which the inner perimeter of solder balls 31 are attached.” Leung, [3:42-3:61].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced	Leung discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

downwardly from the bottom surface of the top package substrate.	<p><i>See, e.g.:</i></p> <p>“In view of the forgoing, there is disclosed herein a stacked multi-chip package with an EMI shielded space comprising a first substrate having a first ground plane laminated between dielectric layers of the first substrate, an electronic component mounted of a first side of the first substrate layer and a second substrate having a second ground plane laminated between dielectric layers of the second substrate, wherein the first substrate is mounted to the second substrate by a grid array of metallic connecting nodes with the electronic component positioned between the substrates, and at least a group of the metallic connecting nodes surround the electronic component and are electrically connected to both the first ground plane and the second ground plane.” Leung, [1:57-2:2].</p> <p>“Preferably, the electronic component is an integrated circuit chip, and the chip has been thinned to a thickness of between 5 and 7 mils.” Leung, [2:6-2:8].</p> <p>“The RF chip 13 must be thin enough to mount in the BGA 3 stand-off space 33 between the RF module 1 and the main board 2.” Leung, [3:28-3:30].</p>
--	--

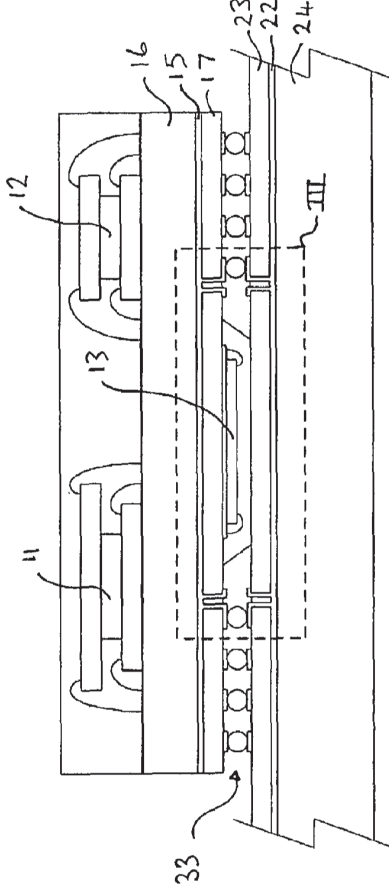


Figure 2

Leung, FIG. 2

“A typical RF chip is 15-25 mils thick: too thick for a robust BGA stand-off distance. However, chips can be thinned to between 5-7 mils.” Leung, [3:30-3:32].

“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip.” Leung, [4:9-4:12].

“In the current invention, however, the RF chip 13, or other component, being shielded is located in the BGA stand-off space 33 between the substrates 10, 20. The thickness of the epoxy mold 40 encapsulating the RF chip 13 is therefore controlled and trimmed to act as a spacer for the BGA stand-off 33. The epoxy mold 40 of the RF chip 13 is in contact with the

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>system substrate 20 to help support the module substrate 10 which prevents the BGA solder balls 30, 31 from collapsing during the reflow heating process.” Leung, [4:43-4:52].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Leung discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Generally the invention is a stacked multi-chip package with first and second substrates mounted together by a grid array of metallic connecting nodes, such as a solder Ball Grid Array. Each substrate has a ground plane laminated between dielectric layers of the substrate. A sensitive or EMI generating component is mounted between the first and second substrates and is surrounded by a group of the metallic connecting nodes that are also electrically connected to the ground planes of both substrates to form a conductive Faraday cage about the component.” Leung, [2:52-2:61].</p>

“Referring to the drawings generally, in the exemplary embodiment a MCM 1 is mounted to a main system board, or motherboard 2, and interconnected thereto by a Ball Grid Array (BGA) 3. The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side.” Leung, [3:21-3:26].

“The MCM 1 comprises a supporting substrate 10 having two digital IC chips 11, 12 mounted on its first side and an RF chip 13 mounted on its second side. The digital IC chips 11, 12 are a memory chip and a logic chip for controlling the RF module 1.” Leung, [3:24-3:28].

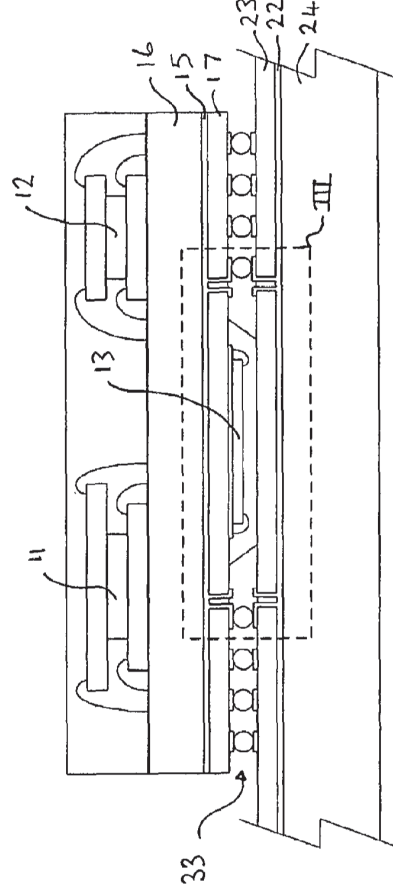


Figure 2

Leung, FIG. 2

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“The RF chip 13 must be thin enough to mount in the BGA 3 stand-off space 33 between the RF module 1 and the main board 2. A typical RF chip is 15-25 mils thick; too thick for a robust BGA stand-off distance. However, chips can be thinned to between 5-7 mils.” Leung, [3:28-3:32].</p> <p>“The RF module supporting substrate 10 is of a type having one or more conductive ground planes 15 laminated between dielectric layers 16, 17 of epoxy or other suitable non-conductive material. Substrates of this type are conventional in the art of printed circuit board technology and manufacture. The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3.” Leung, [3:42-3:48].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>Leung discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3. On the second side of the RF module substrate 10 surrounding the RF chip 13 is a plurality of balls of solder 30, 31 arranged in a grid pattern.” Leung, [3:47-3:51].</p> <p>“The module substrate 10 is mounted and interconnected to the system substrate 20 by the Ball Grid Array (BGA) 3.” Leung, [3:47-3:48].</p> <p>“The ground plane vias 34 are connected with via bonding pads 35 or under bump metallization (UBM) solder on the second side of the module substrate 10 to which the inner perimeter of solder balls 31 are attached.” Leung, [3:58-3:61].</p> <p>“The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1.” Leung, [3:62-3:66].</p> <p>“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip.” Leung, [4:9-4:12].</p> <p>“The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22. Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided</p>
--	---

about the RF chip 13 for EMI Shielding of the chip. The Faraday cage comprises upper and lower ground planes 15, 22 of the RF module substrate 10 and the system substrate 20 interconnected around a shielded chip space 32 by a plurality of ground plane vias 34, 36 and the inner perimeter of BGA solder balls 31. The remaining solder balls 30 (shown in dashed lines in FIG. 6) of the BGA 3 provide electrical interconnection between the RF module 1 and the system 2 in known manner.” Leung, [5:33-6:15].

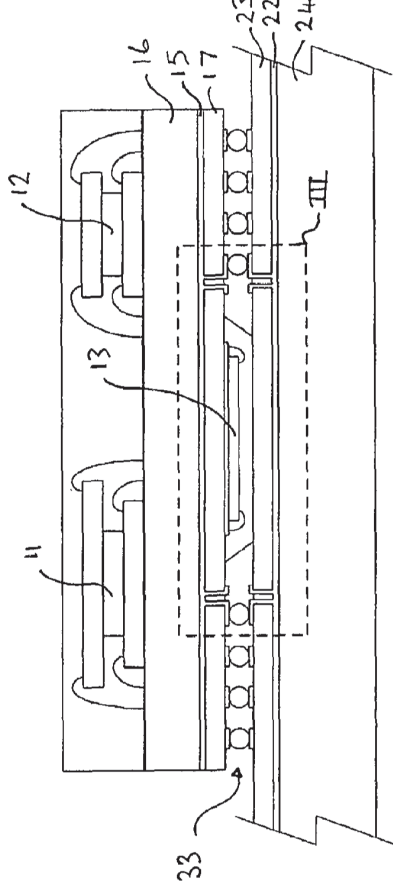


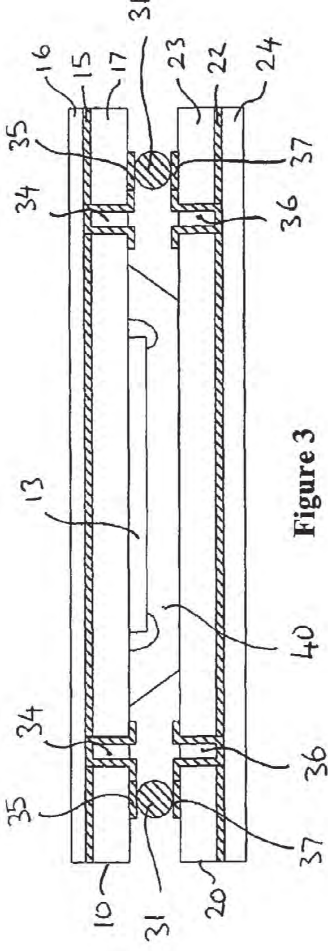
Figure 2

Leung, FIG. 2

To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Leung discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p>See, e.g.:</p>  <p>Leung, FIG. 3</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>to which the inner perimeter of solder balls 31 are attached. The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1.” Leung, [3:48-3:66].</p> <p>“The ground plane vias 34 are connected with via bonding pads 35 or under bump metallization (UBM) solder on the second side of the module substrate 10 to which the inner perimeter of solder balls 31 are attached. The surface of the system substrate 20 to receive the RF module 1 is provided with electrical bonding pads 21, 37 or UBM points arranged in a corresponding grid pattern to receive the solder balls 30, 31 of the Ball Grid Array 3 of the RF module 1. At the center of the bonding pad 21, 37 grid pattern is a corresponding RF chip space. The system substrate 20 is also of a type having one or more conductive ground planes 22 laminated between dielectric layers 23, 24. The inner most line of bonding pads 35 that form the perimeter of the system substrate RF chip space is electrically connected to the system substrate ground plane 22 in the same way as the inner perimeter of solder balls 31 on the module support substrate 10. That is, ground plane vias 36 are formed between the inner perimeter bonding pads 37 of the system substrate and its ground plane 22.” Leung, [3:58-4:9].</p> <p>“Accordingly, when the RF module 1 is mounted to the system substrate 2, in known manner, via the Ball Grid Array 3 a type of Faraday cage is provided about the RF chip 13 for EMI Shielding of the chip. The Faraday cage comprises upper and lower ground planes 15, 22 of the RF module substrate 10 and the system substrate 20 interconnected around a shielded chip space 32 by a plurality of ground plane vias 34, 36 and the inner perimeter of BGA solder balls 31. The remaining solder balls 30 (shown in dashed lines in FIG. 6) of the BGA 3 provide electrical interconnection between the RF module 1 and the system 2 in known manner.” Leung, [4:9-4:20].</p>
--	--

Appendix A-20 - Invalidity of U.S. Patent No. 9859202 in view of Leung - U.S. Patent No. 7514774

	<p>“Referring to FIG. 7, a large conductive plane or pad 25 may be formed on the surface of one of the substrates, for example the system substrate 20, for receiving the inner perimeter solder balls 31 and forming one side of the shielding cage. Additionally, referring to FIG. 9, a similar conductive plane or pad 26 may be formed on an opposite side of the substrate mounting the shielded electronic component and connected to the solder balls 31 by plated through-holes 27.” Leung, [5:5-5:17].</p> <p>To the extent Plaintiff contends that Leung fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

U.S. Patent No.10418298 (“Lin”) is titled Semiconductor Device and Method of Forming Dual Fan-Out Semiconductor Package and lists Yaojin Lin as inventor. Lin is assigned to STATS ChipPAC Pte. Ltd. Lin anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory². Lin is a U.S. patent that was filed September 24, 2013 and published March 26, 2015. Lin is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Lin, or otherwise rendered obvious by disclosures and teachings of Lin, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Lin does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Lin with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Lin, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

Where the chart below states that Lin “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Lin or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Lin set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Lin discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 6 shows dual Fo-WLCSP 230 after singulation. Semiconductor die 124 is electrically connected through build-up interconnect structure 180 and build-up interconnect structure 222 to bumps 220 for connection to external devices.” Lin, [17:40-17:43].</p>

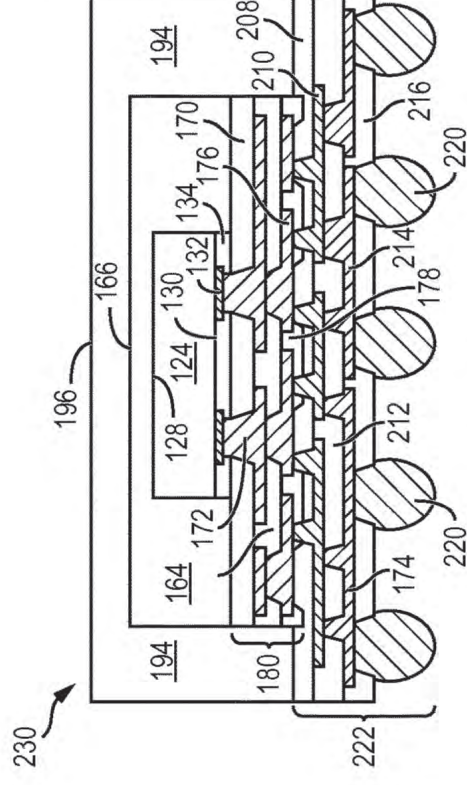


FIG. 6

Lin, FIG. 6

“FIG. 8 shows dual Fo-WLCSP 336 after singulation. Semiconductor die 274 are electrically connected through build-up interconnect structure 270 and build-up interconnect structure 328 to bumps 326 for connection to external devices.” Lin, [24:50-24:54].

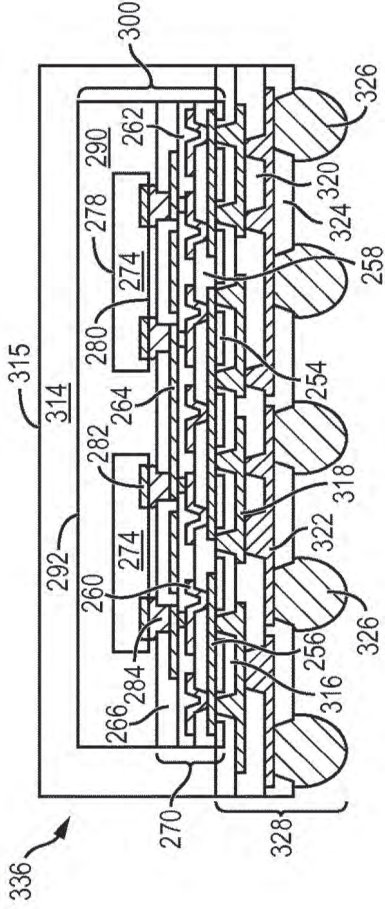


FIG. 8

Lin, FIG. 8

“FIG. 10 shows dual Fo-WLCSP 440 after singulation. Semiconductor die 354 is electrically connected through build-up interconnect structure 390 and build-up interconnect structure 432 to bumps 430 for connection to external devices.” Lin, [31:53-31:57].

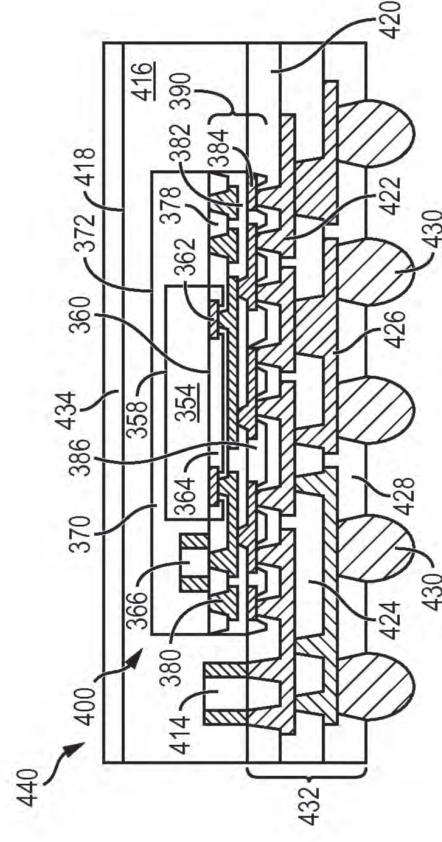
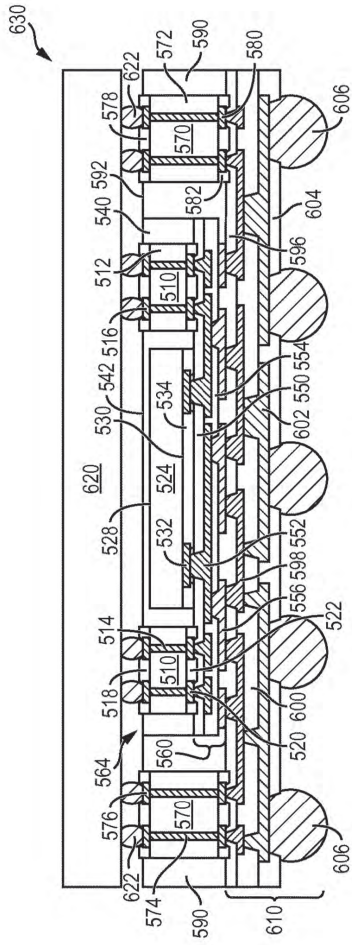


FIG. 10

Lin, FIG. 10

“FIG. 12 shows dual Fo-PoP 630 after singulation. Semiconductor die 524 is electrically connected through build-up interconnect structure 560 and build-up interconnect structure 610 to bumps 606 for connection to external devices.” Lin, [41:23-41:26].

	<div><p>A detailed cross-sectional diagram of a dual Fo-PoP 760 after singulation. The diagram shows two semiconductor dies, 654 and 654', stacked vertically. Die 654 is connected to a build-up interconnect structure 690. The structure includes various layers and bumps, labeled with reference numerals: 510, 512, 514, 516, 518, 520, 522, 524, 528, 530, 532, 534, 536, 538, 540, 542, 544, 546, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 568, 570, 572, 574, 576, 578, 580, 582, 584, 586, 588, 590, 592, 594, 596, 598, 600, 602, 604, 606, 610, 612, 614, 616, 618, 620, 622, 624, 626, 628, 630. The diagram illustrates the electrical connection between the dies and the external devices through the build-up interconnect structure.</p></div> <div><p>FIG. 12</p></div> <div><p>Lin, FIG. 12</p></div> <div><p>“FIG. 13 shows dual Fo-PoP 760 after singulation. Semiconductor die 654 is electrically connected through build-up interconnect structure 690 and build-up interconnect structure 746 to bumps 744 for connection to external devices.” Lin, [49:47-49:50].</p></div>
--	--

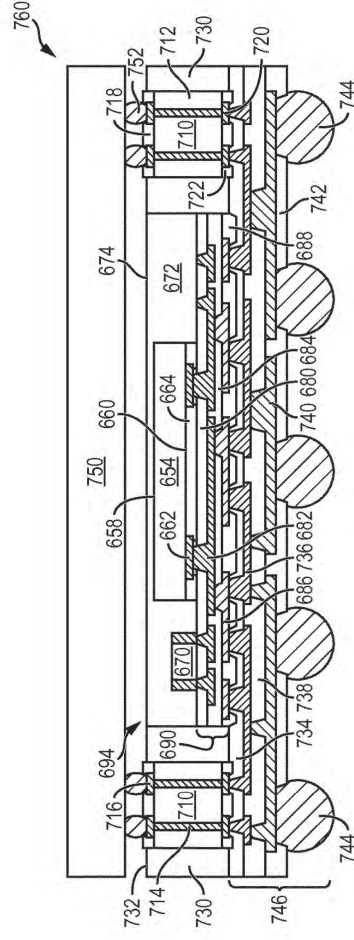
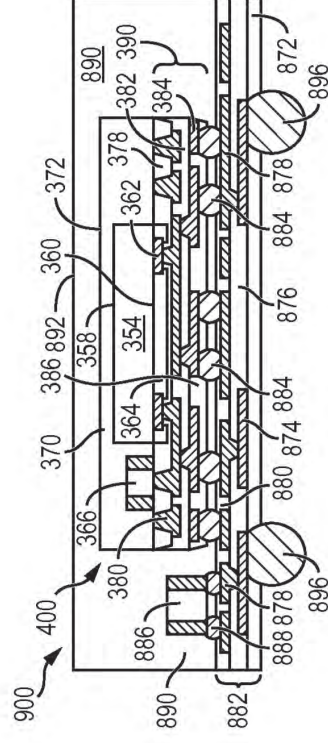


FIG. 13

Lin, FIG. 13

“FIG. 16 shows dual Fo-WLCSP 900 after singulation. Semiconductor die 354 is electrically connected through build-up interconnect structure 390 and build-up interconnect structure 882 to bumps 896 for connection to external devices.” Lin, [62:50-62:54].



Lin, FIG. 16

[1.A] a bottom package substrate;

Lin discloses, either expressly or inherently, a bottom package substrate.

See, e.g.:

“FIG. 5a shows a cross-sectional view of a portion of a carrier or temporary substrate 160 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 162 is formed over carrier 160 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. Carrier 160 can be a round or rectangular panel (greater than 300 mm) with capacity for multiple semiconductor die 124. Carrier 160 may have a larger surface area than the surface area of semiconductor wafer 120. A larger carrier reduces the manufacturing cost of the semiconductor package as more semiconductor die can be processed on the larger

	<p>carrier thereby reducing the cost per unit. Semiconductor packaging and processing equipment are designed and configured for the size of the wafer or carrier being processed. To further reduce manufacturing costs, the size of carrier 160 is selected independent of the size of semiconductor die 124 or size of semiconductor wafer 120. That is, carrier 160 has a fixed or standardized size, which can accommodate various size semiconductor die 124 singulated from one or more semiconductor wafers 120. In one embodiment, carrier 160 is circular with a diameter of 330 mm. In another embodiment, carrier 160 is rectangular with a width of 560 mm and length of 600 mm. Semiconductor die 124 may have dimensions of 10 mm by 10 mm, which are placed on the standardized carrier 160.” Lin, [11:16-11:43].</p> <div> </div> <p>Lin, FIG. 5a</p> <p>FIG. 5a</p> <p>“FIG. 7a shows a cross-sectional view of a portion of a carrier or temporary substrate 250 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An insulating or passivation layer 254 is applied over carrier 250. Insulating layer 254 can be formed using PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation. Insulating layer 254 includes one or more layers of Si₃N₄, SiO₂, SiON, SiO₂/Si₃N₄, Ta₂O₅, Al₂O₃, polymer dielectric, or</p>
--	---

	<p>other material having similar insulating and structural properties. In one embodiment, insulating layer 254 includes a laminated dielectric film. In alternate embodiments, insulating layer 254 can be replaced by a conductive layer, such as Cu. Insulating layer 254 is chosen to have good selectivity as a silicon etchant and can act as an etch stop during later removal of the dummy substrate. An electrically conductive layer or RDL 256 is formed over insulating layer 254 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 256 includes a conductive material, such as Al, Cu, Sn, Ni, Au, Ag, or other electrically conductive material.” Lin, [18:66-19:21].</p> <div> <p>FIG. 7a</p> </div> <p>Lin, FIG. 7a</p> <p>“FIG. 5k, the reconstituted wafer is singulated through build-up interconnect structure 180 and encapsulant 164 using a saw blade or laser cutting tool 182 into individual Fo-WLCSP 186 containing semiconductor die 124. In FIG. 5l Fo-WLCSP 186 from FIG. 5k are mounted to a carrier or temporary substrate 190 with conductive layer 176 of Fo-WLCSP 186 oriented toward the carrier. Carrier or temporary substrate 190 contains sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-stop tape 192 is formed over carrier 190 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. Carrier 190 can be a round or rectangular panel (greater than 300 mm) with capacity for multiple Fo-WLCSP 186. Carrier 190 may have a larger surface area than the surface area of the reconstituted</p>
--	--

wafer containing semiconductor die 124 and build-up interconnect structure 180. A larger carrier reduces the manufacturing cost of the semiconductor package as more semiconductor packages can be processed on the larger carrier thereby reducing the cost per unit. Semiconductor packaging and processing equipment are designed and configured for the size of the wafer or carrier being processed. To further reduce manufacturing costs, the size of carrier 190 is selected independent of the size of Fo-WLCSP 186 or the size of the reconstituted wafer containing semiconductor die 124 and build-up interconnect structure 180. That is, carrier 190 has a fixed or standardized size, which can accommodate various size semiconductor packages 186 singulated from one or more reconstituted wafers. In one embodiment, carrier 190 is circular with a diameter of 330 mm. In another embodiment, carrier 190 is rectangular with a width of 560 mm and length of 600 mm. Standardized carrier 190 can handle any size Fo-WLCSP 186, which allows subsequent semiconductor processing equipment to be standardized to a common carrier, i.e., independent of die size or incoming wafer size. Semiconductor packaging equipment can be designed and configured for a standard carrier using a common set of processing tools, equipment, and bill of materials to process any semiconductor die size from any incoming wafer size." Lin, [21:59-22:34].

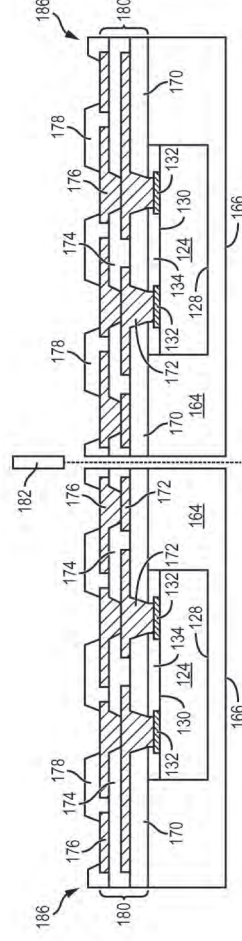
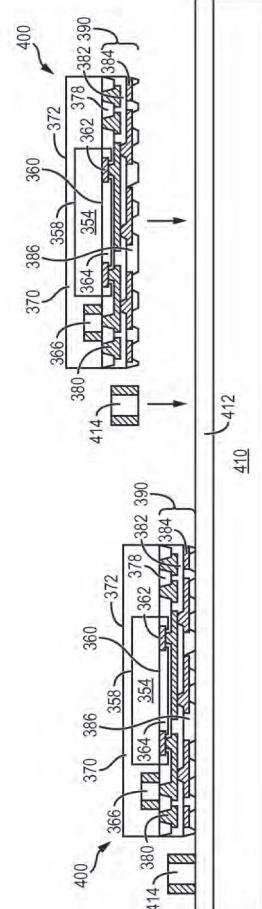


FIG. 5k

Lin, FIG. 5k

	<p>“FIG. 9f, Fo-WLCSP 400 from FIG. 9e and additional semiconductor components or passive devices 414 are aligned with and mounted to substrate or carrier 410 with insulating layer 386 of Fo-WLCSP 400 oriented toward carrier 410. Carrier or temporary substrate 410 contains a sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 412 is formed over carrier 410 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer.” Lin, [28:51-28:60].</p>  <p style="text-align: center;">FIG. 9f</p> <p>Lin, FIG. 9f</p> <p>“FIG. 11e, Fo-WLCSP 564 from FIG. 11d, and 3D interconnect structures or interposers 570 are aligned with and mounted to temporary substrate or carrier 566 with conductive layer 556 of Fo-WLCSP 564 and insulating layer 582 and conductive layer 580 of interposer 570 oriented toward carrier 566. 3D interconnect structure or interposer 570 is prefabricated, i.e., interposer 570 is formed prior to mounting interposer 570 to carrier 566. Interposer 570 includes a core substrate 572. Substrate 572 includes one or more laminated layers of polytetrafluoroethylene prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of</p>
--	---

	<p>phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Alternatively, core substrate 572 includes one or more insulating or dielectric layers.” Lin, [36:57-37:5].</p> <div></div> <p style="text-align: center;"><i>FIG. 11e</i></p> <p>Lin, FIG. 11e</p> <p>“FIG. 15a shows a cross-sectional view of a portion of a carrier or temporary substrate 870 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An insulating or passivation layer 872 is applied over carrier 870. Insulating layer 872 can be formed using PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation. Insulating layer 872 includes one or more layers of Si₃N₄, SiO₂, SiON, SiO₂/Si₃N₄, Ta₂O₅, Al₂O₃, or other material having similar insulating and structural properties. In one embodiment, insulating layer 872 includes a laminated dielectric film. In alternate embodiments, insulating layer 872 can be replaced by a conductive layer, such as Cu. Insulating layer 872 is chosen to have good selectivity as a silicon etchant and can act as an etch stop during later removal of the carrier. In FIG. 15b, an</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>electrically conductive layer or RDL 874 is formed over insulating layer 872 and carrier 870 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating.” Lin, [59:45-59:65].</p>  <p>FIG. 15a</p> <p>Lin, FIG. 15a</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Lin discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In FIG. 5I Fo-WLCSP 186 from FIG. 5k are mounted to a carrier or temporary substrate 190 with conductive layer 176 of Fo-WLCSP 186 oriented toward the carrier. Carrier or temporary substrate 190 contains sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 192 is formed over carrier 190 as a temporary adhesive bonding film,</p>

etch-stop layer, or thermal release layer. Carrier 190 can be a round or rectangular panel (greater than 300 mm) with capacity for multiple Fo-WLCSP 186.” Lin, [11:14-11:24].

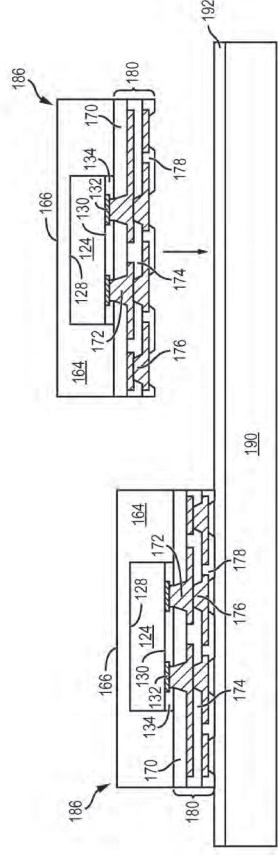


FIG. 51

Lin, FIG. 51

“In FIG. 7i, Fo-WLCSPs 300 from FIG. 7h are aligned with and mounted to a carrier 310 with insulating layer 254 of Fo-WLCSP 300 oriented toward carrier 310. Carrier or temporary substrate 310 contains sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 312 is formed over carrier 310 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer.” Lin, [21:63-22:4].

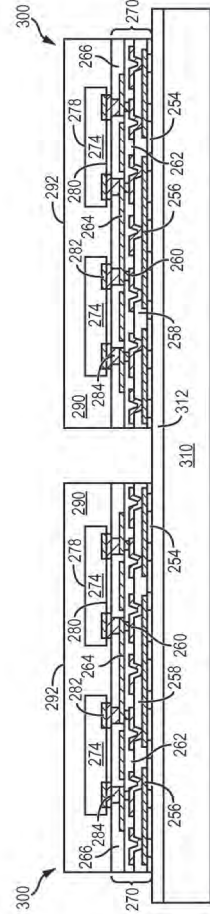


FIG. 7i

Lin, FIG. 7i

“In FIG. 9f, Fo-WLCSP 400 from FIG. 9e and additional semiconductor components or passive devices 414 are aligned with and mounted to substrate 410 with insulating layer 386 of Fo-WLCSP 400 oriented toward carrier 410. Carrier or temporary substrate 410 contains a sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support.” Lin, [28:51-28:58].

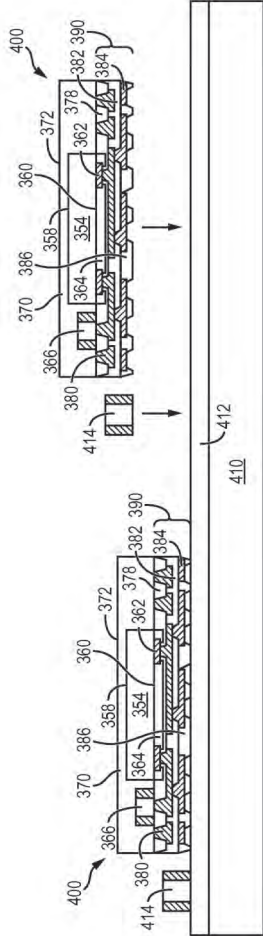
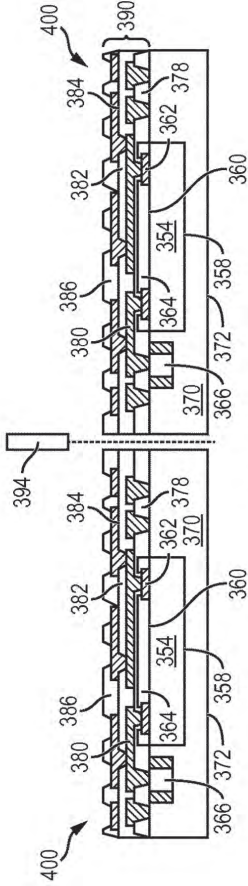


FIG. 9f

	<p>Lin, FIG. 9f</p> <div></div> <p><i>FIG. 9e</i></p> <p>Lin, FIG. 9e</p> <p>“In FIG. 11e, Fo-WLCSP 564 from FIG. 11d, and 3D interconnect structures or interposers 570 are aligned with and mounted to temporary substrate or carrier 566 with conductive layer 556 of Fo-WLCSP 564 and insulating layer 582 and conductive layer 580 of interposer 570 oriented toward carrier 566.” Lin, [36:57-36:62].</p>
--	--

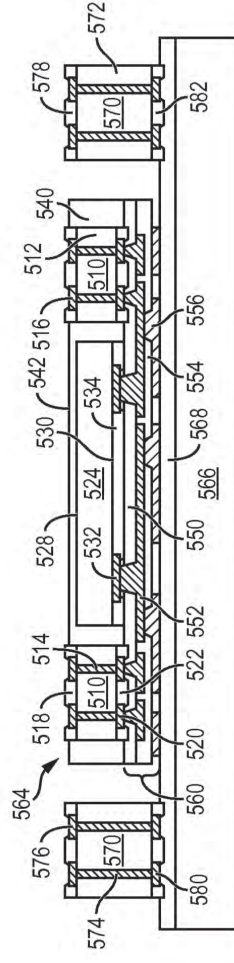


FIG. 11e

Lin, FIG. 11e

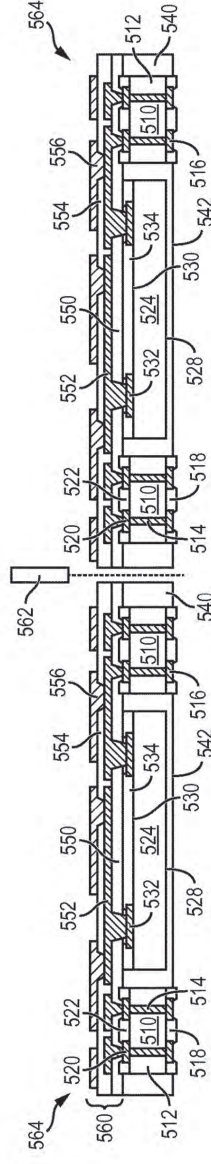


FIG. 11d

Lin, FIG. 11d

“Fo-WLCSP 694 is similar to Fo-WLCSP 400 in FIG. 9 e. Fo-WLCSP 694 and 3D interconnect structures or interposers 710, similar to interposer 570 in FIG. 11e, are aligned with and mounted to a temporary substrate or carrier, similar to carrier 566 in FIG. 11e, with

	<p>conductive layer 586 and insulating layer 588 of Fo-WLCSP 694 and insulating layer 722 and conductive layer 720 of interposer 710 oriented toward the carrier.” Lin, [45:11-45:19].</p> <div></div> <p>Lin, FIG. 9e</p> <p>FIG. 9e</p> <p>“In FIG. 15d, Fo-WLCSP 400, including semiconductor die 354, passive device 366, and build-up interconnect structure 390, from FIG. 9e and a plurality of semiconductor components or passive devices 886 are disposed over build-up interconnect structure 882 and carrier 870.” Lin, [61:14-61:18].</p>
--	---

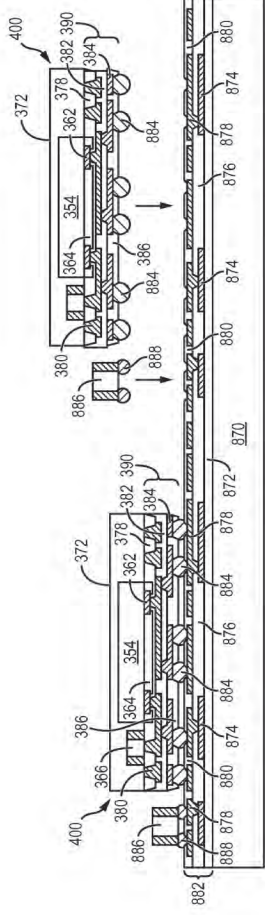


FIG. 15d

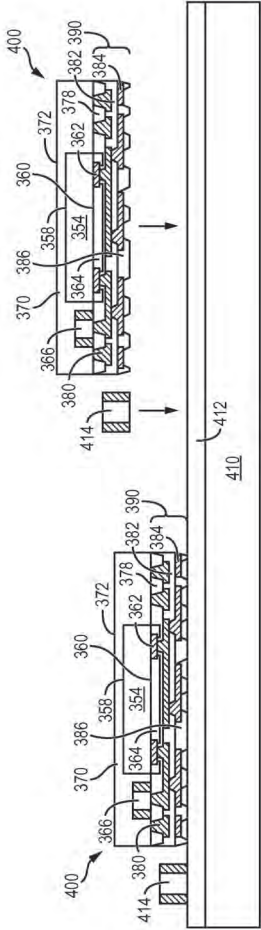
Lin, FIG. 15d

To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Lin discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.

See, e.g.:

“In FIG. 9f, Fo-WLCSP 400 from FIG. 9e and additional semiconductor components or passive devices 414 are aligned with and mounted to substrate or carrier 410 with insulating layer 386 of Fo-WLCSP 400 oriented toward carrier 410. Carrier or temporary substrate 410 contains a sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape

	<p>412 is formed over carrier 410 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. In FIG. 9g, an encapsulant or molding compound 416 is deposited over and around Fo-WLCSP 400 and passive device 414 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator.” Lin, [28:51-28:65].</p> <div></div> <p>Lin, FIG. 9f</p> <p>FIG. 9f</p> <p>“In FIG. 11e, Fo-WLCSP 564 from FIG. 11d, and 3D interconnect structures or interposers 570 are aligned with and mounted to temporary substrate or carrier 566 with conductive layer 556 of Fo-WLCSP 564 and insulating layer 582 and conductive layer 580 of interposer 570 oriented toward carrier 566. 3D interconnect structure or interposer 570 is prefabricated, i.e., interposer 570 is formed prior to mounting interposer 570 to carrier 566. Interposer 570 includes a core substrate 572. Substrate 572 includes one or more laminated layers of polytetrafluoroethylene prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>reinforcement fibers or fabrics. Alternatively, core substrate 572 includes one or more insulating or dielectric layers. A plurality of through vias is formed through core substrate 572 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 574. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers. An electrically conductive layer or RDL 576 is formed over a surface of core substrate 572 and conductive vias 574 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 576 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 576 is electrically connected to conductive vias 574. Conductive layer 576 operates as contact pads electrically connected to conductive vias 574. An insulating or passivation layer 578 is formed over the surface of core substrate 572 and conductive layer 576 using PVD, CVD, printing, spin coating, spray coating, slit coating, rolling coating, lamination, sintering, or thermal oxidation. Insulating layer 578 includes one or more layers of SiO₂, Si₃N₄, SiON, Ta₂O₅, Al₂O₃, HfO₂, BCB, PI, PBO, polymer dielectric resist with or without fillers or fibers, or other material having similar structural and dielectric properties. A portion of insulating layer 578 is removed by LDA, etching, or other suitable process to expose portions of conductive layer 576. In one embodiment, insulating layer 578 is a masking layer. An electrically conductive layer or RDL 580 is formed over a surface of core substrate 572 opposite the conductive layer 576 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 580 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 580 is electrically connected to conductive vias 574 and conductive layer 576. Alternatively, conductive vias 574 are formed through core substrate</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>572 after forming conductive layer 576 and/or conductive layer 580. An insulating or passivation layer 582 is formed over conductive layer 580 using PVD, CVD, printing, spin coating, spray coating, slit coating, rolling coating, lamination, sintering, or thermal oxidation. The insulating layer 582 includes one or more layers of SiO₂, Si₃N₄, SiON, Ta₂O₅, Al₂O₃, HfO₂, BCB, PI, PBO, polymer dielectric resist with or without fillers or fibers, or other material having similar structural and dielectric properties. A portion of insulating layer 582 is removed by an exposure and development process, LDA, etching, or other suitable process to expose portions of conductive layer 580. In one embodiment, insulating layer 582 is a masking layer. Substrate 572 is then singulated into individual 3D interconnect units or interposers 570. Interposer 570 provides electrical interconnect vertically across the substrate through conductive vias 574 according to the electrical function of semiconductor die 524 and later mounted semiconductor die or devices. Interposer 570 is known good having been inspected and tested by open/short probe or auto-scope inspection at an interim stage, i.e., prior to mounting Fo-WLCSP 564. In FIG. 11f, an encapsulant or molding compound 590 is deposited over Fo-WLCSP 564 and around interposer 570 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator.” Lin, [36:57-38:6].</p>
--	--

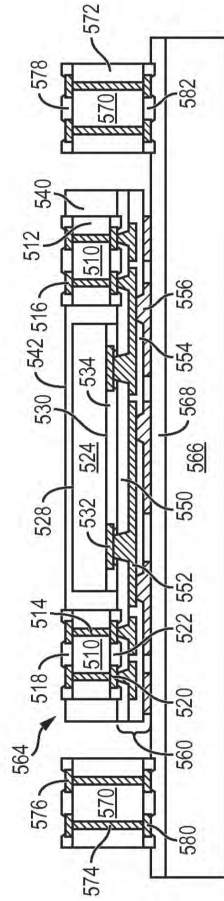
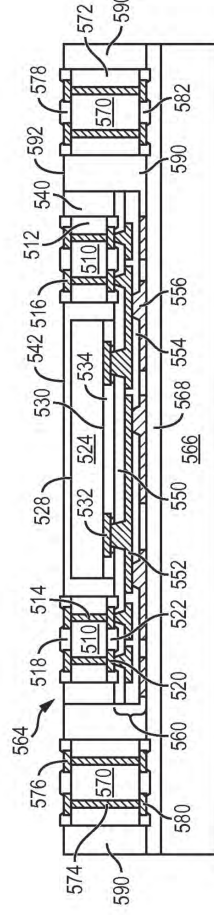


FIG. 11e

Lin, FIG. 11e

“Interposer 570 provides electrical interconnect vertically across the substrate through conductive vias 574 according to the electrical function of semiconductor die 524 and later mounted semiconductor die or devices. Interposer 570 is known good having been inspected and tested by open/short probe or auto-scope inspection at an interim stage, i.e., prior to mounting Fo-WLCSP 564. In FIG. 11f, an encapsulant or molding compound 590 is deposited over Fo-WLCSP 564 and around interposer 570 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator.” Lin, [37:63-38:7].



Lin, FIG. 11f

“Interposer 710 provides electrical interconnect vertically through dual Fo-PoP 760 according to the design and function of semiconductor die 654 and semiconductor device 750. Interposer 710 can be made with low cost manufacturing technology, such as substrate manufacturing, and provide a cost effective process for forming vertical interconnection in dual Fo-PoP 760. Interposer 710 allows integration of additional packages or devices, e.g., device 750, within dual Fo-PoP 760. Incorporating additional devices in a stacked or “package-on-package” orientation increases the electrical performance and functionality of dual Fo-PoP 760 without increasing the package footprint.” Lin, [49:25-49:37].

“Fo-WLCSP 694, interposer 710, semiconductor device 750, and build-up interconnect structure 746 represent a dual Fo-PoP in reconstituted wafer form. The reconstituted wafer is singulated through build-up interconnect structure 746, semiconductor device 750, and encapsulant 730 using a saw blade or laser cutting tool into individual dual Fo-PoP 760 containing semiconductor die 654, passive device 670, interposer 710, and semiconductor device 750. Alternatively, semiconductor device 750 is mounted after singulation. FIG. 13

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>shows dual Fo-PoP 760 after singulation. Semiconductor die 654 is electrically connected through build-up interconnect structure 690 and build-up interconnect structure 746 to bumps 744 for connection to external devices.” Lin, [49:38-49:50].</p> <p>“Interposer 810 provides electrical interconnect vertically through dual Fo-PoP 860 according to the design and function of semiconductor die 764 and semiconductor device 850. Interposer 810 can be made with low cost manufacturing technology, such as substrate manufacturing, and provide a cost effective process for forming vertical interconnection in dual Fo-PoP 860. Interposer 810 allows integration of additional packages or devices, e.g., device 850, within dual Fo-PoP 860. Incorporating additional devices in a stacked or “package-on-package” orientation increases the electrical performance and functionality of dual Fo-PoP 860 without increasing the package footprint.” Lin, [57:63-58:7].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Lin discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Interposer 510 includes a core substrate 512. Substrate 512 includes one or more laminated layers of polytetrafluoroethylene pre-impregnated (prepreg), FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Alternatively, core substrate 512 includes one or more insulating or passivation layers.” Lin, [33:31-33:38].</p>

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>“Interposer 570 includes a core substrate 572. Substrate 572 includes one or more laminated layers of polytetrafluoroethylene prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Alternatively, core substrate 572 includes one or more insulating or dielectric layers.” Lin, [36:65-37:5].</p> <p>“Interposer 710 includes a core substrate 712. Substrate 712 includes one or more laminated layers of polytetrafluoroethylene prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Alternatively, core substrate 712 includes one or more insulating or dielectric layers.” Lin, [45:28-45:35].</p> <p>“Interposer 810 includes a core substrate 812. Substrate 812 includes one or more laminated layers of polytetrafluoroethylene prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Alternatively, core substrate 812 includes one or more insulating or dielectric layers.” Lin, [53:46-53:52].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Lin discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p>

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p><i>See, e.g.:</i></p> <p>“A plurality of through vias is formed through core substrate 572 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 574. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers.” Lin, [30:20-30:30].</p> <p>“A plurality of through vias is formed through core substrate 712 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 714. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers.” Lin, [45:36-45:45].</p> <p>“A plurality of through vias is formed through core substrate 812 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 814. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers.” Lin, [55:8-55:17].</p>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

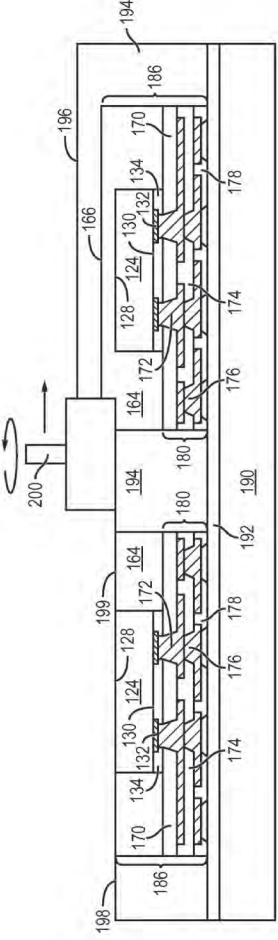
	<p>“A plurality of through vias is formed through encapsulant 830 over component 800 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 834. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers.” Lin, [55:8-55:17].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Lin discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“An electrically conductive layer or RDL 516 is formed over the surface of core substrate 512 and conductive vias 514 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 516 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 516 is electrically connected to conductive vias 514. Conductive layer 516 operates as contact pads electrically connected to conductive vias 514.” Lin, [33:50-33:59].</p>

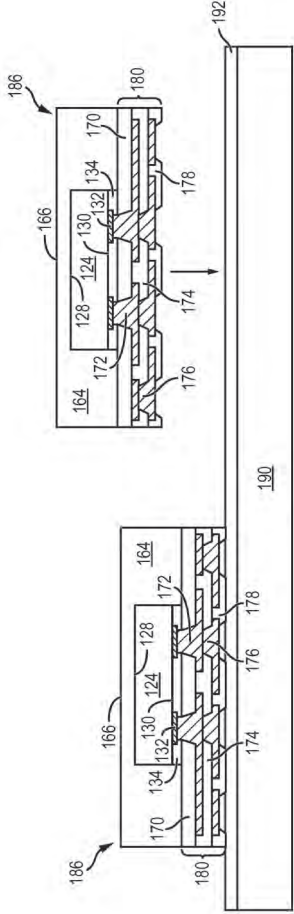
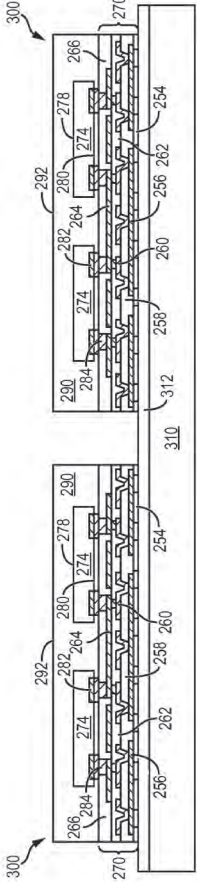
Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

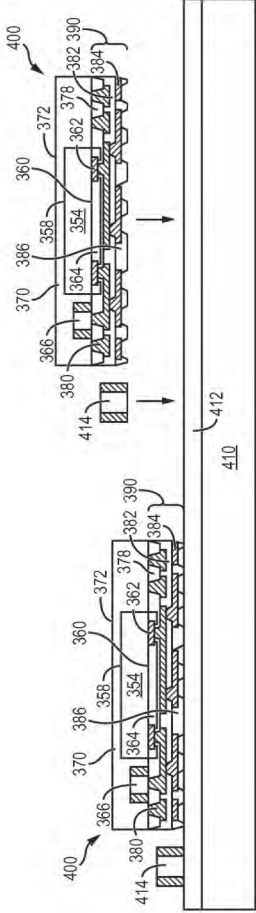
	<p>“An electrically conductive layer or RDL 520 is formed over a surface of core substrate 512 opposite conductive layer 516 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 520 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 520 is electrically connected to conductive vias 514 and conductive layer 516. Conductive layer 520 operates as contact pads electrically connected to conductive vias 514.” Lin, [34:6-34:15].</p> <p>“An electrically conductive layer or RDL 576 is formed over a surface of core substrate 572 and conductive vias 574 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 576 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 576 is electrically connected to conductive vias 574. Conductive layer 576 operates as contact pads electrically connected to conductive vias 574.” Lin, [37:17-37:26].</p> <p>“An electrically conductive layer or RDL 580 is formed over a surface of core substrate 572 opposite the conductive layer 576 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 580 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 580 is electrically connected to conductive vias 574 and conductive layer 576.” Lin, [37:39-37:47].</p> <p>“An electrically conductive layer or RDL 716 is formed over a surface of core substrate 712 and conductive vias 714 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 716 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>material. Conductive layer 716 is electrically connected to conductive vias 714. Conductive layer 716 operates as contact pads electrically connected to conductive vias 714.” Lin, [45:46-45:55].</p> <p>“An electrically conductive layer or RDL 816 is formed over a surface of core substrate 812 and conductive vias 814 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 816 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 816 is electrically connected to conductive vias 814. Conductive layer 816 operates as contact pads electrically connected to conductive vias 814.” Lin, [53:63-54:5].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Lin discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In FIG. 5n, a portion of back surface 196 of encapsulant 194 and a portion of back surface 166 of encapsulant 164 are removed by grinder 200 in an optional backgrinding operation. The backgrinding operation reduces a thickness of encapsulants 194 and 164 and may expose back surface 128 of semiconductor die 124. In FIG. 5n, surface 198 of encapsulant 194 and</p>

	<p>surface 199 of encapsulant 164 are co-planar with surface 128 of semiconductor die 124 after the backgrinding operation.” Lin, [15:11-15:19].</p>  <p>Lin, FIG. 5n</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Lin discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

	<p>“In FIG. 5l Fo-WLCSP 186 from FIG. 5k are mounted to a carrier or temporary substrate 190 with conductive layer 176 of Fo-WLCSP 186 oriented toward the carrier.” Lin, [14:13-14:15].</p> <div></div> <p>FIG. 5l</p> <p>Lin, FIG. 5l</p> <p>“In FIG. 7i, Fo-WLCSPs 300 from FIG. 7h are aligned with and mounted to a carrier 310 with insulating layer 254 of Fo-WLCSP 300 oriented toward carrier 310.” Lin, [21:63-21:65].</p> <div></div> <p>FIG. 7i</p>
--	---

	<div><p>Lin, FIG. 7i</p></div> <div><p>“In FIG. 9f, Fo-WLCSP 400 from FIG. 9e and additional semiconductor components or passive devices 414 are aligned with and mounted to substrate or carrier 410 with insulating layer 386 of Fo-WLCSP 400 oriented toward carrier 410.” Lin, [28:51-28:55].</p></div> <div></div> <div><p>FIG. 9f</p></div> <div><p>Lin, FIG. 9f</p></div> <div><p>“In FIG. 11e, Fo-WLCSP 564 from FIG. 11d, and 3D interconnect structures or interposers 570 are aligned with and mounted to temporary substrate or carrier 566 with conductive layer 556 of Fo-WLCSP 564 and insulating layer 582 and conductive layer 580 of interposer 570 oriented toward carrier 566. 3D interconnect structure or interposer 570 is prefabricated, i.e., interposer 570 is formed prior to mounting interposer 570 to carrier 566. Interposer 570 includes a core substrate 572. Substrate 572 includes one or more laminated layers of polytetrafluoroethylene prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other</p></div>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>reinforcement fibers or fabrics. Alternatively, core substrate 572 includes one or more insulating or dielectric layers. A plurality of through vias is formed through core substrate 572 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 574. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers. An electrically conductive layer or RDL 576 is formed over a surface of core substrate 572 and conductive vias 574 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 576 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 576 is electrically connected to conductive vias 574. Conductive layer 576 operates as contact pads electrically connected to conductive vias 574. An insulating or passivation layer 578 is formed over the surface of core substrate 572 and conductive layer 576 using PVD, CVD, printing, spin coating, spray coating, slit coating, rolling coating, lamination, sintering, or thermal oxidation. Insulating layer 578 includes one or more layers of SiO₂, Si₃N₄, SiON, Ta₂O₅, Al₂O₃, HfO₂, BCB, PI, PBO, polymer dielectric resist with or without fillers or fibers, or other material having similar structural and dielectric properties. A portion of insulating layer 578 is removed by LDA, etching, or other suitable process to expose portions of conductive layer 576. In one embodiment, insulating layer 578 is a masking layer. An electrically conductive layer or RDL 580 is formed over a surface of core substrate 572 opposite the conductive layer 576 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 580 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 580 is electrically connected to conductive vias 574 and conductive layer 576.” Lin, [36:57-37:45].</p>
--	--

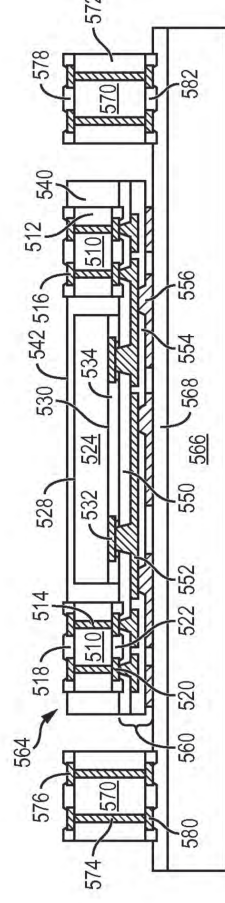


FIG. 11e

Lin, FIG. 11e

“Fo-WLCSP 694 is similar to Fo-WLCSP 400 in FIG. 9 e. Fo-WLCSP 694 and 3D interconnect structures or interposers 710, similar to interposer 570 in FIG. 11e, are aligned with and mounted to a temporary substrate or carrier, similar to carrier 566 in FIG. 11e, with conductive layer 586 and insulating layer 588 of Fo-WLCSP 694 and insulating layer 722 and conductive layer 720 of interposer 710 oriented toward the carrier.” Lin, [45:11-45:19].

“Fo-WLCSP 794, a 3D interconnect structures or interposer 810, and a semiconductor device or component 800 are aligned with and mounted to a temporary substrate or carrier, similar to carrier 566 in FIG. 11e, with conductive layer 782 and insulating layer 784 of Fo-WLCSP 794 and insulating layer 822 and conductive layer 820 of interposer 810 oriented toward the carrier.” Lin, [53:31-53:37].

To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and	<p>Lin discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In FIG. 11e, Fo-WLCSP 564 from FIG. 11d, and 3D interconnect structures or interposers 570 are aligned with and mounted to temporary substrate or carrier 566 with conductive layer 556 of Fo-WLCSP 564 and insulating layer 582 and conductive layer 580 of interposer 570 oriented toward carrier 566. 3D interconnect structure or interposer 570 is prefabricated, i.e., interposer 570 is formed prior to mounting interposer 570 to carrier 566. Interposer 570 includes a core substrate 572. Substrate 572 includes one or more laminated layers of polytetrafluoroethylene prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Alternatively, core substrate 572 includes one or more insulating or dielectric layers. A plurality of through vias is formed through core substrate 572 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 574. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers. An electrically conductive layer or RDL 576 is formed over a surface of core substrate 572 and conductive vias 574 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and</p>

electroless plating. Conductive layer 576 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 576 is electrically connected to conductive vias 574." Lin, [36:57-37:23].

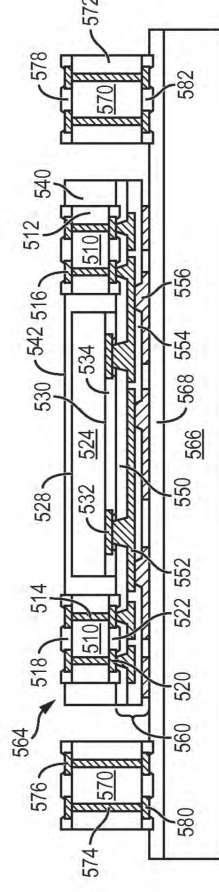


FIG. 11e

Lin, FIG. 11e

“An electrically conductive layer or RDL 598 is formed over insulating layer 596. Conductive layer 598 can be one or more layers of Al, Ti, TiW, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer 598 is electrically connected to conductive layer 556 of Fo-WLCSP 564. One portion of conductive layer 598 is electrically connected to conductive layer 580 of interposer 570. Other portions of conductive layer 598 can be electrically common or electrically isolated depending on the design and function of semiconductor die 524.” Lin, [38:60-39:2].

“In one embodiment, a portion of build-up interconnect structure 610 includes a ground plane. A semiconductor device or component 620 is mounted to conductive layer 576 of interposer

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>570 and conductive layer 516 of interposer 510 with bumps 622 at the wafer level, i.e., before singulation. Semiconductor device 620 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 622 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 622 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 622 represent one type of interconnect structure that can be formed between semiconductor device 620 and conductive layers 576 and 516. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 620 is mounted using pick and place or other suitable operation.” Lin, [40:45-40:63].</p> <p>“A semiconductor device or component 620 is mounted to conductive layer 576 of interposer 570 and conductive layer 516 of interposer 510 with bumps 622 at the wafer level, i.e., before singulation. Semiconductor device 620 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 622 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 622 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 622 represent one type of interconnect structure that can be formed between semiconductor device 620 and conductive layers 576 and 516. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 620 is mounted using pick and place or other suitable operation. Semiconductor device 620 is electrically connected to build-up interconnect structure 560 through conductive vias 514. Semiconductor device 620 is electrically connected to build-up interconnect structure 610 through conductive vias 574.” Lin, [40:48-40:67].</p>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>“Semiconductor device or component 850 is mounted to conductive layer 816 of interposer 810 and conductive vias 834 at the wafer level, i.e., before singulation. Semiconductor device 850 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 852 electrically connect semiconductor device 850 to conductive vias 814 and 834. Bumps 852 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 852 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 852 represent one type of interconnect structure that can be formed between semiconductor devices 850 and conductive vias 814 and 834. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 850 is mounted using pick and place or other suitable operation. Semiconductor device 850 is electrically connected to build-up interconnect structure 848 through conductive vias 814 and electrically connected to component 800 through conductive vias 834.” Lin, [57:43-57:63].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of</p>	<p>Lin discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

top metal pillars of the bottom package substrate; and	<p>“A semiconductor device or component 620 is mounted to conductive layer 576 of interposer 570 and conductive layer 516 of interposer 510 with bumps 622 at the wafer level, i.e., before singulation. Semiconductor device 620 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 622 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 622 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 622 represent one type of interconnect structure that can be formed between semiconductor device 620 and conductive layers 576 and 516. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 620 is mounted using pick and place or other suitable operation. Semiconductor device 620 is electrically connected to build-up interconnect structure 560 through conductive vias 514. Semiconductor device 620 is electrically connected to build-up interconnect structure 610 through conductive vias 574.” Lin, [40:47-40:66].</p> <p>“Interposers 510 and 570 provide electrical interconnect vertically through dual Fo-PoP 630 according to the design and function of semiconductor die 524 and semiconductor device 620. Interposers 510 and 570 can be made with low cost manufacturing technology, such as substrate manufacturing, and provide a cost effective process for forming vertical interconnection in dual Fo-PoP 630. Interposers 510 and 570 allow integration of additional packages or devices, e.g., device 620, within dual Fo-PoP 630.” Lin, [41:10-41:19].</p> <p>“A semiconductor device or component 750 is mounted to conductive layer 716 of interposer 710 with bumps 752 at the wafer level, i.e., before singulation. Semiconductor device 750 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 752 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations</p>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>thereof. Bumps 752 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 752 represent one type of interconnect structure that can be formed between semiconductor devices 750 and conductive layer 716. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 750 is mounted using pick and place or other suitable operation. Semiconductor device 750 is electrically connected to build-up interconnect structure 746 through conductive vias 714.” Lin, [49:8-49:25].</p> <p>“Interposer 710 provides electrical interconnect vertically through dual Fo-PoP 760 according to the design and function of semiconductor die 654 and semiconductor device 750. Interposer 710 can be made with low cost manufacturing technology, such as substrate manufacturing, and provide a cost effective process for forming vertical interconnection in dual Fo-PoP 760. Interposer 710 allows integration of additional packages or devices, e.g., device 750, within dual Fo-PoP 760.” Lin, [49:25-49:33].</p> <p>“Semiconductor device or component 850 is mounted to conductive layer 816 of interposer 810 and conductive vias 834 at the wafer level, i.e., before singulation. Semiconductor device 850 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 852 electrically connect semiconductor device 850 to conductive vias 814 and 834. Bumps 852 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 852 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 852 represent one type of interconnect structure that can be formed between semiconductor devices 850 and conductive vias 814 and 834. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 850 is mounted using pick and place or other suitable operation. Semiconductor device 850 is electrically connected to build-up interconnect</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>structure 848 through conductive vias 814 and electrically connected to component 800 through conductive vias 834.” Lin, [57:43-57:63].</p> <p>“Interposer 810 provides electrical interconnect vertically through dual Fo-PoP 860 according to the design and function of semiconductor die 764 and semiconductor device 850. Interposer 810 can be made with low cost manufacturing technology, such as substrate manufacturing, and provide a cost effective process for forming vertical interconnection in dual Fo-PoP 860. Interposer 810 allows integration of additional packages or devices, e.g., device 850, within dual Fo-PoP 860.” Lin, [57:63-58:4].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Lin discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In FIG. 5I Fo-WLCSP 186 from FIG. 5k are mounted to a carrier or temporary substrate 190 with conductive layer 176 of Fo-WLCSP 186 oriented toward the carrier. Carrier or temporary substrate 190 contains sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 192 is formed over carrier 190 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. Carrier 190 can be a round or rectangular panel (greater than 300 mm) with capacity for multiple Fo-WLCSP 186. Carrier 190 may have a</p>

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>larger surface area than the surface area of the reconstituted wafer containing semiconductor die 124 and build-up interconnect structure 180. A larger carrier reduces the manufacturing cost of the semiconductor package as more semiconductor packages can be processed on the larger carrier thereby reducing the cost per unit. Semiconductor packaging and processing equipment are designed and configured for the size of the wafer or carrier being processed. To further reduce manufacturing costs, the size of carrier 190 is selected independent of the size of Fo-WLCSP 186 or the size of the reconstituted wafer containing semiconductor die 124 and build-up interconnect structure 180. That is, carrier 190 has a fixed or standardized size, which can accommodate various size semiconductor packages 186 singulated from one or more reconstituted wafers. In one embodiment, carrier 190 is circular with a diameter of 330 mm. In another embodiment, carrier 190 is rectangular with a width of 560 mm and length of 600 mm. Standardized carrier 190 can handle any size Fo-WLCSP 186, which allows subsequent semiconductor processing equipment to be standardized to a common carrier, i.e., independent of die size or incoming wafer size. Semiconductor packaging equipment can be designed and configured for a standard carrier using a common set of processing tools, equipment, and bill of materials to process any semiconductor die size from any incoming wafer size. The common or standardized carrier 190 lowers manufacturing costs and capital risk by reducing or eliminating the need for specialized semiconductor processing lines based on die size or incoming wafer size. By selecting a predetermined carrier size to use for any size semiconductor package from all semiconductor wafer, a flexible manufacturing line can be implemented. In FIG. 5m, an encapsulant or molding compound 194 is deposited over and around Fo-WLCSP 186 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator.” Lin, [11:14-11:61].</p> <p>“In FIG. 7i, Fo-WLCSPs 300 from FIG. 7h are aligned with and mounted to a carrier 310 with insulating layer 254 of Fo-WLCSP 300 oriented toward carrier 310. Carrier or temporary</p>
--	---

	<p>substrate 310 contains sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 312 is formed over carrier 310 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. In FIG. 7j, an encapsulant or molding compound 314 is deposited over and around Fo-WLCSP 300 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 314 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 314 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.” Lin, [21:63-22:13].</p> <p>“In FIG. 9f, Fo-WLCSP 400 from FIG. 9e and additional semiconductor components or passive devices 414 are aligned with and mounted to substrate or carrier 410 with insulating layer 386 of Fo-WLCSP 400 oriented toward carrier 410. Carrier or temporary substrate 410 contains a sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 412 is formed over carrier 410 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. In FIG. 9g, an encapsulant or molding compound 416 is deposited over and around Fo-WLCSP 400 and passive device 414 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator.” Lin, [28:51-28:65].</p> <p>“Fo-WLCSP 694 is similar to Fo-WLCSP 400 in FIG. 9 e. Fo-WLCSP 694 and 3D interconnect structures or interposers 710, similar to interposer 570 in FIG. 11e, are aligned with and mounted to a temporary substrate or carrier, similar to carrier 566 in FIG. 11e, with conductive layer 586 and insulating layer 588 of Fo-WLCSP 694 and insulating layer 722 and conductive layer 720 of interposer 710 oriented toward the carrier. The carrier contains a</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape, similar to interface layer 568 in FIG. 11e, is formed over the carrier as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. 3D interconnect structure or interposer 710 is prefabricated, i.e., interposer 710 is formed prior to mounting interposer 710 to the carrier.” Lin, [45:11-45:28].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Lin discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In FIG. 7e, semiconductor die 274, similar to semiconductor die 144 in FIG. 4c, are disposed over build-up interconnect structure 270. Semiconductor die 274 include contact pads 282 formed on active surfaces 280. Conductive bumps 284 are formed on contact pads 282. Semiconductor die 274 are mounted to build-up interconnect structure 270 using a pick-and-place operation.” Lin, [20:64-21:3].</p>

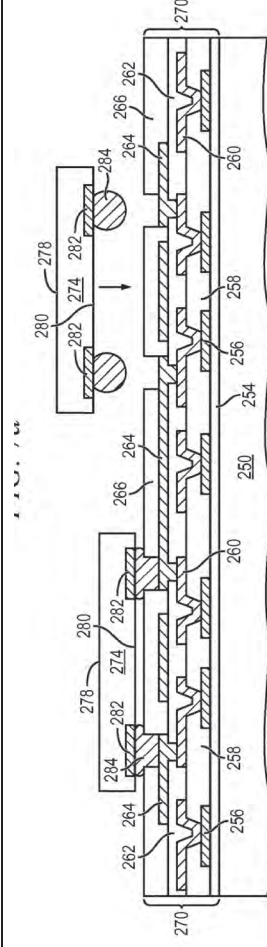


FIG. 7e

Lin, FIG. 7e

“In FIG. 5I Fo-WLCSP 186 from FIG. 5k are mounted to a carrier or temporary substrate 190 with conductive layer 176 of Fo-WLCSP 186 oriented toward the carrier. Carrier or temporary substrate 190 contains sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support.” Lin, [21:63-22:1].

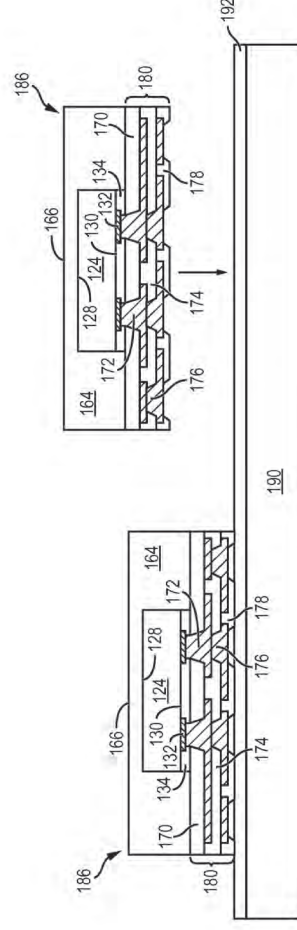


FIG. 51

FIG. 9a, with active surface 660 of semiconductor die 654 oriented toward the carrier. The carrier includes a sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape, similar to interface layer 352 in FIG. 9a, is formed over the carrier as a temporary adhesive bonding film, etch-stop layer, or thermal release layer." Lin, [42:48-42:62].

FIG. 9a

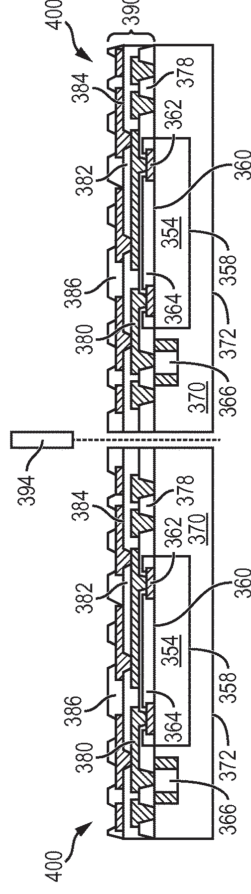


FIG. 9e

Lin, FIG. 9e

“In FIG. 15d, Fo-WLCSP 400, including semiconductor die 354, passive device 366, and build-up interconnect structure 390, from FIG. 9e and a plurality of semiconductor components or passive devices 886 are disposed over build-up interconnect structure 882 and carrier 870.” Lin, [61:14-61:18].

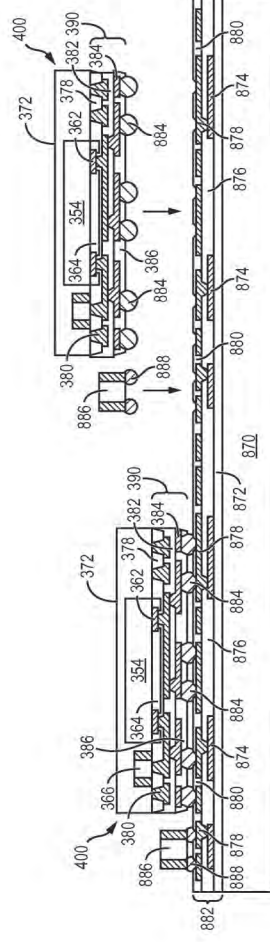


FIG. 15d

Lin, FIG. 15d

To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Lin discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

See, e.g.:

“FIG. 9a shows a cross-sectional view of a portion of a carrier or temporary substrate 350 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 352 is formed over carrier 350 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. Semiconductor die 354 similar to semiconductor die 124 from FIG.

3c, are mounted to carrier 350 and interface layer 352 using, for example, a pick and place operation with active surface 360 oriented toward the carrier. A plurality of other semiconductor components or passive devices 366 are mounted to carrier 350 adjacent to semiconductor die 354." Lin, [26:22-26:35].

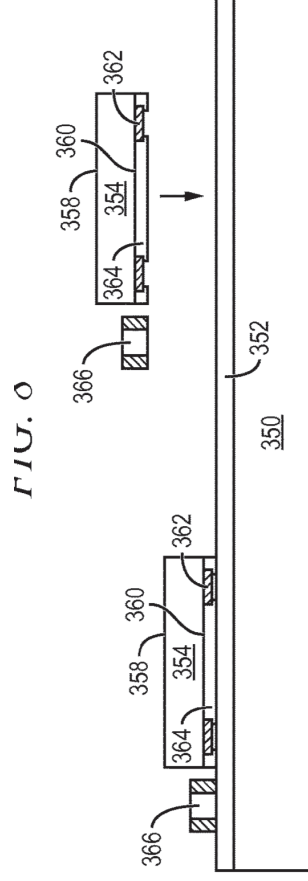


FIG. 9a

Lin, FIG. 9a

“In FIG. 9f, Fo-WLCSP 400 from FIG. 9e and additional semiconductor components or passive devices 414 are aligned with and mounted to substrate or carrier 410 with insulating layer 386 of Fo-WLCSP 400 oriented toward carrier 410.” Lin, [28:51-28:55].

“FIGS. 11a-11h illustrate, in relation to FIGS. 1 and 2 a - 2 c, a process of forming a dual fan-out semiconductor device including embedded 3D interconnect structures. FIG. 11a shows a cross-sectional view of a portion of a carrier or temporary substrate 500 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 502 is formed over

	<p>carrier 500 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. Semiconductor die 524, similar to semiconductor die 124 from FIG. 3c, are mounted to carrier 500 and interface layer 502 using, for example, a pick and place operation with active surface 530 oriented toward the carrier.” Lin, [33:13-33:26].</p> <p>Lin, FIG. 11a</p> <p><i>FIG. 11a</i></p> <p>“In FIG. 11e, Fo-WLCSP 564 from FIG. 11d, and 3D interconnect structures or interposers 570 are aligned with and mounted to temporary substrate or carrier 566 with conductive layer 556 of Fo-WLCSP 564 and insulating layer 582 and conductive layer 580 of interposer 570 oriented toward carrier 566.” Lin, [36:57-36:62].</p> <p>“FIG. 13 illustrates an embodiment of dual Fo-PoP 760 including a Fo-WLCSP 694, an interposer 710, and a build-up interconnect structure 746. Fo-WLCSP 694 is similar to Fo-WLCSP 400 in FIG. 9e ; interposer 710 is similar to interposer 570 in FIG. 11e ; build-up interconnect structure 746 is similar to build-up interconnect structure 610 in FIG. 11 h.” Lin, [42:46-42:52].</p>
--	--

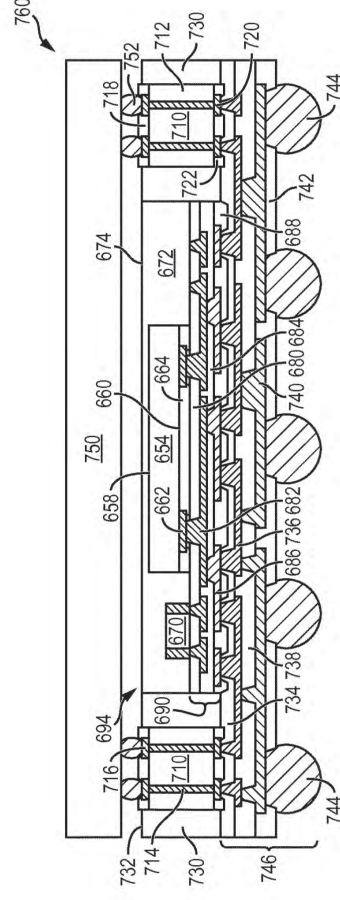


FIG. 13

Lin, FIG. 13

“In dual Fo-WLCSP 920, semiconductor die 274 are electrically connected through build-up interconnect structure 270 and build-up interconnect structure 882 to bumps 896 for connection to external devices.” Lin, [65:1-65:4].

To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
-------------------------	-------------------

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Lin discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In FIG. 5m, an encapsulant or molding compound 194 is deposited over and around Fo-WLCSP 186 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 194 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 194 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. Encapsulant 194 also protects semiconductor die 124 from degradation due to exposure to light. The filler and CTE of encapsulant 194 are selected to aid with gap filling, warpage control, and reliability. Prior to forming encapsulant 194, a backgrinding operation and/or an RF etching, plasma clean, solvent strip, or wet clean process is performed on Fo-WLCSP 186 to roughen the surfaces of encapsulant 164 and build-up interconnect structure 180 and improve adhesion of encapsulant 194. In one embodiment, encapsulant 164 and/or encapsulant 194 include a controlled stress-releasing agent to improve adhesion of encapsulant 194. In FIG. 5n, a portion of back surface 196 of encapsulant 194 and a portion of back surface 166 of encapsulant 164 are removed by grinder 200 in an optional backgrinding operation. The backgrinding operation reduces a thickness of encapsulants 194 and 164 and may expose back surface 128 of semiconductor die 124. In FIG. 5n, surface 198 of encapsulant 194 and surface 199 of encapsulant 164 are co-planar with surface 128 of semiconductor die 124 after the backgrinding operation.” Lin, [14:57-15:20].</p>
---	--

	<div></div> <div><p>FIG. 5m</p></div> <div><p>Lin, FIG. 5m</p></div> <div><p>“In FIG. 9g, an encapsulant or molding compound 416 is deposited over and around Fo-WLCSP 400 and passive device 414 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 416 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 416 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. Encapsulant 416 also protects semiconductor die 354 from degradation due to exposure to light. The filler and CTE of encapsulant 416 are selected to aid with gap filling, warpage control, and reliability. Prior to forming encapsulant 416, a backgrinding operation and/or an RF etching, plasma clean, solvent strip, or wet clean process is performed on Fo-WLCSP 400 to roughen the surfaces of encapsulant 370 and build-up interconnect structure 390 and improve adhesion of encapsulant 416. Encapsulant 416 and/or encapsulant 370 include a controlled stress-releasing agent to improve adhesion of encapsulant 416. In one embodiment, a portion of back surface 418 of encapsulant 416 and a portion of back surface 372 of encapsulant 370 are removed in a backgrinding operation. The backgrinding</p></div>
--	---

operation planarizes encapsulant 416 and encapsulant 370, and exposes back surface 358 of semiconductor die 354. The backgrinding operation reduces an overall thickness of the semiconductor package." Lin, [28:61-29:20].

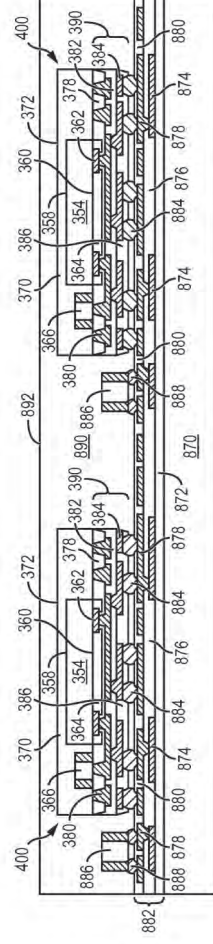
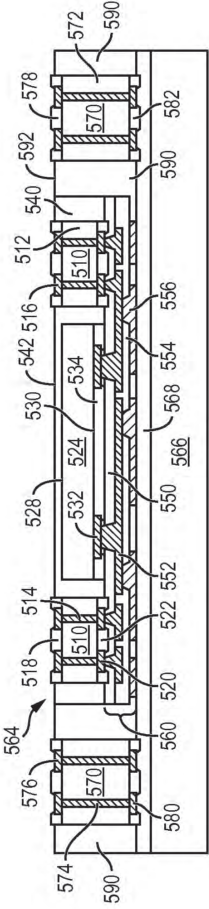


FIG. 15e

Lin, FIG. 15e

“In FIG. 11f, an encapsulant or molding compound 590 is deposited over Fo-WLCSP 564 and around interposer 570 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 590 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 590 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. Encapsulant 590 also protects semiconductor die 524 from degradation due to exposure to light. The filler and CTE of encapsulant 590 are selected to aid with gap filling, warpage control, and reliability. Prior to forming encapsulant 590, a backgrinding operation and/or an RF etching, plasma clean, solvent strip, or wet clean process is performed on Fo-WLCSP 564 to roughen the surfaces of encapsulant 540 and build-up interconnect structure

	<p>560 and improve adhesion of encapsulant 590. Encapsulant 590 and/or encapsulant 540 include a controlled stress-releasing agent to improve adhesion of encapsulant 590. In one embodiment, a backgrinding operation is performed to remove a portion of encapsulants 590 and 540 and expose conductive layer 576 of interposer 570, conductive layer 516 of interposer 510, and surface 528 of semiconductor die 524.” Lin, [38:3-38:27].</p> <div></div> <p style="text-align: center;"><i>FIG. 11f</i></p> <p>Lin, FIG. 11f</p> <p>“FIG. 13 illustrates an embodiment of dual Fo-PoP 760 including a Fo-WLCSP 694, an interposer 710, and a build-up interconnect structure 746. Fo-WLCSP 694 is similar to Fo-WLCSP 400 in FIG. 9e ; interposer 710 is similar to interposer 570 in FIG. 11e ; build-up interconnect structure 746 is similar to build-up interconnect structure 610 in FIG. 11 h. A semiconductor die 654, similar to semiconductor die 124 in FIG. 3c, is disposed over a temporary substrate or carrier, similar to carrier 350 in FIG. 9a, with active surface 660 of semiconductor die 654 oriented toward the carrier. The carrier includes a sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape, similar to interface</p>
--	---

layer 352 in FIG. 9a, is formed over the carrier as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. A semiconductor component or passive device 670, similar to passive device 366 in FIG. 9a, is mounted to the carrier adjacent to semiconductor die 654. An encapsulant 672 is deposited over semiconductor die 654 and passive device 670 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 672 can be a polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 672 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. Encapsulant 672 also protects semiconductor die 654 from degradation due to exposure to light. The filler and CTE of encapsulant 672 are selected to aid with gap filling, warpage control, and reliability. In one embodiment, a portion of back surface 674 of encapsulant 672 is removed in a backgrinding operation. The backgrinding operation planarizes encapsulant 672 and exposes back surface 658 of semiconductor die 654." Lin, [42:46-43:14].

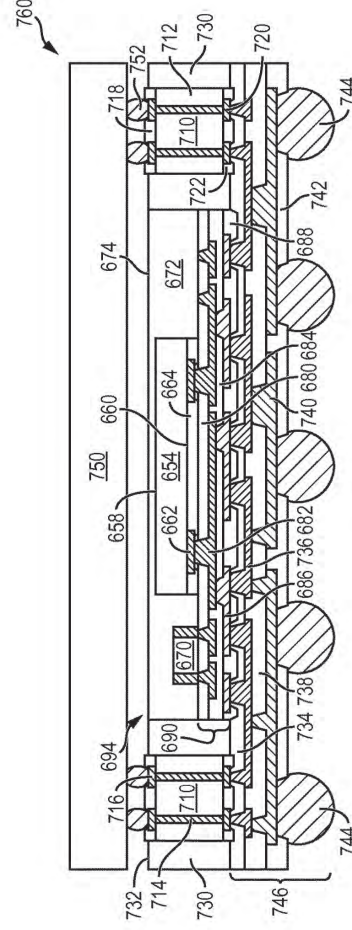


FIG. 13

	<p>Lin, FIG. 13</p> <p>“Encapsulant 730 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 730 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. Encapsulant 730 also protects semiconductor die 654 from degradation due to exposure to light. The filler and CTE of encapsulant 730 are selected to aid with gap filling, warpage control, and reliability. Prior to forming encapsulant 730, a backgrinding operation and/or an RF etching, plasma clean, solvent strip, or wet clean process is performed on Fo-WLCSP 694 to roughen the surfaces of encapsulant 672 and build-up interconnect structure 690 and improve adhesion of encapsulant 730. Encapsulant 730 and/or encapsulant 672 include a controlled stress-releasing agent to improve adhesion of encapsulant 730. In one embodiment, a portion of surface 732 of encapsulant 730 and surface 674 of encapsulant 672 is removed in a backgrinding operation to planarize encapsulants 730 and 672 and expose conductive layer 716 of interposer 710 and back surface 658 of semiconductor die 654.” Lin, [46:36-46:56].</p> <p>“In FIG. 15e, an encapsulant or molding compound 890 is deposited over Fo-WLCSP 400, passive devices 886, and build-up interconnect structure 882 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 890 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 890 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. Encapsulant 890 also protects semiconductor die 354 from degradation due to exposure to light. The filler and CTE of encapsulant 890 are selected to aid with gap filling, warpage control, and reliability. Prior to</p>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>forming encapsulant 890, a backgrinding operation and/or an RF etching, plasma clean, solvent strip, or wet clean process is performed on Fo-WLCSP 400 to roughen the surfaces of encapsulant 370 and build-up interconnect structure 390 and improve adhesion of encapsulant 890. Encapsulant 890 and/or encapsulant 370 include a controlled stress-releasing agent to improve adhesion of encapsulant 890. In one embodiment, a portion of back surface 892 of encapsulant 890 and back surface 372 of encapsulant 370 are removed in a backgrinding operation. The backgrinding operation planarizes the surface of encapsulant 890 and encapsulant 370, and may expose back surface 358 of semiconductor die 354. The backgrinding operation reduces an overall thickness of the semiconductor package.” Lin, [61:57-62:17].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	<p>Lin discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p>

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

<p>overlaps the bottom chip and each of the two spacer connectors.</p>	<p>“A semiconductor device or component 620 is mounted to conductive layer 576 of interposer 570 and conductive layer 516 of interposer 510 with bumps 622 at the wafer level, i.e., before singulation. Semiconductor device 620 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 622 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 622 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 622 represent one type of interconnect structure that can be formed between semiconductor device 620 and conductive layers 576 and 516. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 620 is mounted using pick and place or other suitable operation. Semiconductor device 620 is electrically connected to build-up interconnect structure 560 through conductive vias 514. Semiconductor device 620 is electrically connected to build-up interconnect structure 610 through conductive vias 574.” Lin, [40:48-40:67].</p> <p>“FIG. 12 shows dual Fo-PoP 630 after singulation. Semiconductor die 524 is electrically connected through build-up interconnect structure 560 and build-up interconnect structure 610 to bumps 606 for connection to external devices.” Lin, [41:23-41:26].</p>
--	--

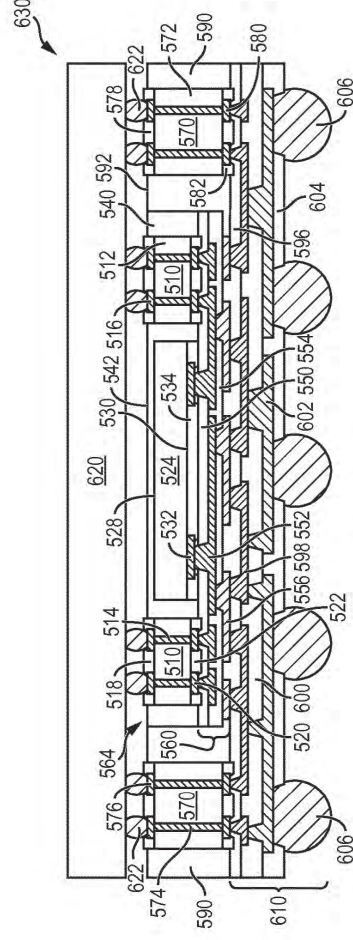


FIG. 12

Lin, FIG. 12

“FIG. 13 illustrates an embodiment of dual Fo-PoP 760 including a Fo-WLCSP 694, an interposer 710, and a build-up interconnect structure 746. Fo-WLCSP 694 is similar to Fo-WLCSP 400 in FIG. 9e ; interposer 710 is similar to interposer 570 in FIG. 11e ; build-up interconnect structure 746 is similar to build-up interconnect structure 610 in FIG. 11h.” Lin, [42:46-42:52].

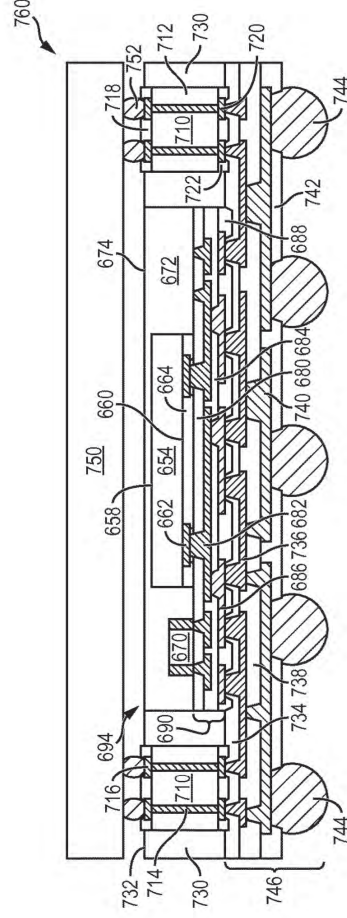
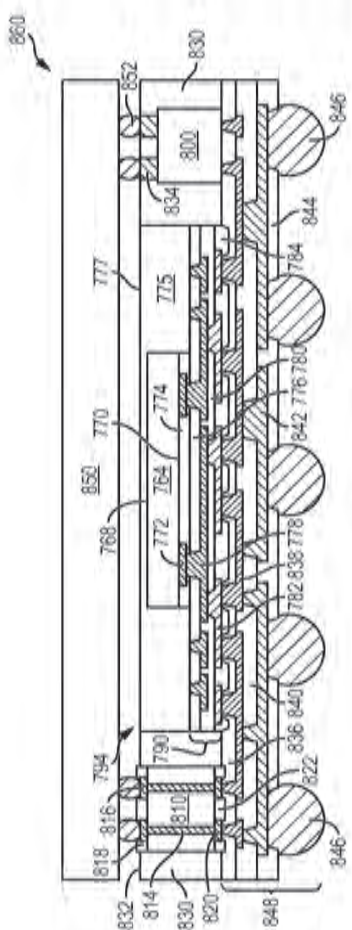


FIG. 13

Lin, FIG. 13

“A semiconductor device or component 750 is mounted to conductive layer 716 of interposer 710 with bumps 752 at the wafer level, i.e., before singulation. Semiconductor device 750 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 752 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 752 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 752 represent one type of interconnect structure that can be formed between semiconductor devices 750 and conductive layer 716. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 750 is mounted using pick and place or other suitable operation. Semiconductor device 750 is electrically connected to build-up interconnect structure 746 through conductive vias 714.” Lin, [49:8-49:25].

	<p>“Semiconductor device or component 850 is mounted to conductive layer 816 of interposer 810 and conductive vias 834 at the wafer level, i.e., before singulation. Semiconductor device 850 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 852 electrically connect semiconductor device 850 to conductive vias 814 and 834. Bumps 852 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 852 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 852 represent one type of interconnect structure that can be formed between semiconductor devices 850 and conductive vias 814 and 834. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 850 is mounted using pick and place or other suitable operation. Semiconductor device 850 is electrically connected to build-up interconnect structure 848 through conductive vias 814 and electrically connected to component 800 through conductive vias 834.” Lin, [57:43-57:63].</p> <p>“FIG. 14 shows dual Fo-PoP 860 after singulation. Semiconductor die 764 is electrically connected through build-up interconnect structure 790 and build-up interconnect structure 848 to bumps 846 for connection to external devices.” Lin, [58:18-58:21].</p>
--	--

	<div></div> <p>Lin, FIG. 14</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Lin discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“An electrically conductive layer or RDL 516 is formed over the surface of core substrate 512 and conductive vias 514 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 516 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 516 is electrically connected to conductive vias 514. Conductive layer 516 operates as contact pads electrically connected to conductive vias 514.” Lin, [33:50-33:59].</p> <p>“An electrically conductive layer or RDL 520 is formed over a surface of core substrate 512 opposite conductive layer 516 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 520 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 520 is electrically connected to conductive vias 514 and conductive layer 516. Conductive layer 520 operates as contact pads electrically connected to conductive vias 514.” Lin, [34:6-34:15].</p> <p>“A semiconductor device or component 620 is mounted to conductive layer 576 of interposer 570 and conductive layer 516 of interposer 510 with bumps 622 at the wafer level, i.e., before singulation. Semiconductor device 620 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>containing semiconductor die or other electronic devices or circuitry. Bumps 622 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 622 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 622 represent one type of interconnect structure that can be formed between semiconductor device 620 and conductive layers 576 and 516. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 620 is mounted using pick and place or other suitable operation. Semiconductor device 620 is electrically connected to build-up interconnect structure 560 through conductive vias 514. Semiconductor device 620 is electrically connected to build-up interconnect structure 610 through conductive vias 574.” Lin, [40:48-40:67].</p> <p>“An electrically conductive layer or RDL 716 is formed over a surface of core substrate 712 and conductive vias 714 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 716 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 716 is electrically connected to conductive vias 714. Conductive layer 716 operates as contact pads electrically connected to conductive vias 714.” Lin, [45:46-45:55].</p> <p>“A semiconductor device or component 750 is mounted to conductive layer 716 of interposer 710 with bumps 752 at the wafer level, i.e., before singulation. Semiconductor device 750 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 752 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 752 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 752 represent one type of interconnect structure that can be formed between semiconductor devices 750 and conductive layer 716. The interconnect structure can also use bond wires,</p>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 750 is mounted using pick and place or other suitable operation. Semiconductor device 750 is electrically connected to build-up interconnect structure 746 through conductive vias 714.” Lin, [49:8-49:25].</p> <p>“Semiconductor device or component 850 is mounted to conductive layer 816 of interposer 810 and conductive vias 834 at the wafer level, i.e., before singulation. Semiconductor device 850 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 852 electrically connect semiconductor device 850 to conductive vias 814 and 834. Bumps 852 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 852 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 852 represent one type of interconnect structure that can be formed between semiconductor devices 850 and conductive vias 814 and 834. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 850 is mounted using pick and place or other suitable operation. Semiconductor device 850 is electrically connected to build-up interconnect structure 848 through conductive vias 814 and electrically connected to component 800 through conductive vias 834.” Lin, [57:43-57:63].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Lin discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Semiconductor die 274 are mounted to build-up interconnect structure 270 using a pick-and-place operation. Bumps 284 are reflowed to metallurgically and electrically connect bumps 284 to conductive layer 264. Semiconductor die 274 are KGD having been tested prior to mounting semiconductor die 274 to build-up interconnect structure 270. In some applications, bumps 284 are reflowed a second time to improve electrical contact to conductive layer 264. Bumps 284 can also be compression bonded or thermocompression bonded to conductive layer 264.” Lin, [21:1-21:11].</p> <p>“A plurality of through vias is formed through core substrate 512 using laser drilling, mechanical drilling, or deep reactive ion etching (DRIE). The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 514. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers. An electrically conductive layer or RDL 516 is formed over the surface of core substrate 512 and conductive vias 514 using a patterning</p>

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 516 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 516 is electrically connected to conductive vias 514. Conductive layer 516 operates as contact pads electrically connected to conductive vias 514.” Lin, [33:39-33:59].</p> <p>“An electrically conductive layer or RDL 520 is formed over a surface of core substrate 512 opposite conductive layer 516 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 520 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 520 is electrically connected to conductive vias 514 and conductive layer 516. Conductive layer 520 operates as contact pads electrically connected to conductive vias 514.” Lin, [34:6-34:15].</p> <p>“A plurality of through vias is formed through core substrate 572 using laser drilling, mechanical drilling, or DRIE. The vias are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable deposition process to form z-direction vertical interconnect conductive vias 574. In one embodiment, Cu is deposited over the sidewall of the through vias by electroless plating and electroplating. The through vias are filled with conductive paste or plugging resin with fillers. An electrically conductive layer or RDL 576 is formed over a surface of core substrate 572 and conductive vias 574 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 576 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 576 is electrically connected to conductive vias 574. Conductive layer 576 operates as contact pads electrically connected to conductive vias 574.” Lin, [37:6-37:26].</p>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>“An electrically conductive layer or RDL 580 is formed over a surface of core substrate 572 opposite the conductive layer 576 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 580 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 580 is electrically connected to conductive vias 574 and conductive layer 576.” Lin, [37:39-37:47].</p> <p>“A semiconductor device or component 620 is mounted to conductive layer 576 of interposer 570 and conductive layer 516 of interposer 510 with bumps 622 at the wafer level, i.e., before singulation. Semiconductor device 620 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 622 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 622 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 622 represent one type of interconnect structure that can be formed between semiconductor device 620 and conductive layers 576 and 516. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 620 is mounted using pick and place or other suitable operation. Semiconductor device 620 is electrically connected to build-up interconnect structure 560 through conductive vias 514. Semiconductor device 620 is electrically connected to build-up interconnect structure 610 through conductive vias 574.” Lin, [40:48-40:67].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the corresponding top metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Lin discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“An electrically conductive layer or RDL 520 is formed over a surface of core substrate 512 opposite conductive layer 516 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 520 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 520 is electrically connected to conductive vias 514 and conductive layer 516. Conductive layer 520 operates as contact pads electrically connected to conductive vias 514.” Lin, [34:6-34:15].</p> <p>“An electrically conductive layer or RDL 576 is formed over a surface of core substrate 572 and conductive vias 574 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 576 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically</p>

	<p>conductive material. Conductive layer 576 is electrically connected to conductive vias 574. Conductive layer 576 operates as contact pads electrically connected to conductive vias 574. An insulating or passivation layer 578 is formed over the surface of core substrate 572 and conductive layer 576 using PVD, CVD, printing, spin coating, spray coating, slit coating, rolling coating, lamination, sintering, or thermal oxidation. Insulating layer 578 includes one or more layers of SiO₂, Si₃N₄, SiON, Ta₂O₅, Al₂O₃, HfO₂, BCB, PI, PBO, polymer dielectric resist with or without fillers or fibers, or other material having similar structural and dielectric properties. A portion of insulating layer 578 is removed by LDA, etching, or other suitable process to expose portions of conductive layer 576. In one embodiment, insulating layer 578 is a masking layer. An electrically conductive layer or RDL 580 is formed over a surface of core substrate 572 opposite the conductive layer 576 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 580 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 580 is electrically connected to conductive vias 574 and conductive layer 576.” Lin, [37:17-37:47].</p> <p>“A semiconductor device or component 620 is mounted to conductive layer 576 of interposer 570 and conductive layer 516 of interposer 510 with bumps 622 at the wafer level, i.e., before singulation. Semiconductor device 620 may include filter, memory and other IC chips, processors, microcontrollers, known-good packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 622 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 622 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 622 represent one type of interconnect structure that can be formed between semiconductor device 620 and conductive layers 576 and 516. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 620 is mounted using pick and place or other suitable operation. Semiconductor device 620 is electrically connected to</p>
--	--

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>build-up interconnect structure 560 through conductive vias 514. Semiconductor device 620 is electrically connected to build-up interconnect structure 610 through conductive vias 574.” Lin, [40:48-40:67].</p> <p>“An electrically conductive layer or RDL 716 is formed over a surface of core substrate 712 and conductive vias 714 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 716 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 716 is electrically connected to conductive vias 714. Conductive layer 716 operates as contact pads electrically connected to conductive vias 714. An insulating or passivation layer 718 is formed over the surface of core substrate 712 and conductive layer 716 using PVD, CVD, printing, spin coating, spray coating, slit coating, rolling coating, lamination, sintering, or thermal oxidation. Insulating layer 718 includes one or more layers of SiO₂, Si₃N₄, SiON, Ta₂O₅, Al₂O₃, HfO₂, BCB, PI, PBO, polymer dielectric resist with or without fillers or fibers, or other material having similar structural and dielectric properties. A portion of insulating layer 718 is removed by LDA, etching, or other suitable process to expose portions of conductive layer 716. In one embodiment, insulating layer 718 is a masking layer. An electrically conductive layer or RDL 720 is formed over a surface of core substrate 712 opposite the conductive layer 716 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 720 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 720 is electrically connected to conductive vias 714 and conductive layer 716.” Lin, [45:46-46:9].</p> <p>“A semiconductor device or component 750 is mounted to conductive layer 716 of interposer 710 with bumps 752 at the wafer level, i.e., before singulation. Semiconductor device 750 may include filter, memory and other IC chips, processors, microcontrollers, known-good</p>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>packages, or any other packaged device containing semiconductor die or other electronic devices or circuitry. Bumps 752 are Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof. Bumps 752 can be eutectic Sn/Pb, high-lead solder, or lead-free solder. Bumps 752 represent one type of interconnect structure that can be formed between semiconductor devices 750 and conductive layer 716. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Semiconductor device 750 is mounted using pick and place or other suitable operation. Semiconductor device 750 is electrically connected to build-up interconnect structure 746 through conductive vias 714.” Lin, [49:8-49:25].</p> <p>“An electrically conductive layer or RDL 816 is formed over a surface of core substrate 812 and conductive vias 814 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 816 includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 816 is electrically connected to conductive vias 814. Conductive layer 816 operates as contact pads electrically connected to conductive vias 814. An insulating or passivation layer 818 is formed over the surface of core substrate 812 and conductive layer 816 using PVD, CVD, printing, spin coating, spray coating, slit coating, rolling coating, lamination, sintering, or thermal oxidation. Insulating layer 818 includes one or more layers of SiO₂, Si₃N₄, SiON, Ta₂O₅, Al₂O₃, HfO₂, BCB, PI, PBO, polymer dielectric resist with or without fillers or fibers, or other material having similar structural and dielectric properties. A portion of insulating layer 818 is removed by LDA, etching, or other suitable process to expose portions of conductive layer 816. In one embodiment, insulating layer 818 is a masking layer. An electrically conductive layer or RDL 820 is formed over a surface of core substrate 812 opposite the conductive layer 816 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 820 includes one or more layers of Al, Cu,</p>
--	---

Appendix A-21 - Invalidity of U.S. Patent No. 9859202 in view of Lin - U.S. Patent No. 10418298

	<p>Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 820 is electrically connected to conductive vias 814 and conductive layer 816.” Lin, [53:63-54:26].</p> <p>To the extent Plaintiff contends that Lin fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

U.S. Patent Publication No. 20140252561 (“Lisk”) is titled VIA-Enabled Package-on-Package and lists Durodami Joscelyn Lisk, Vidhya Ramachandran, and Jae Sik Lee as inventors. Lisk is assigned to Qualcomm Incorporated. Lisk anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Lisk is a U.S. patent publication that was filed March 8, 2013 and published September 11, 2014. Lisk is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Lisk, or otherwise rendered obvious by disclosures and teachings of Lisk, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Lisk does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Lisk with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Lisk, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

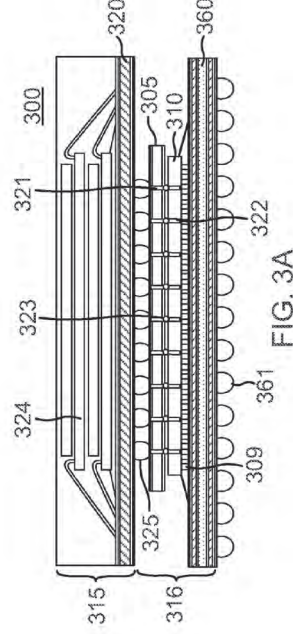
Where the chart below states that Lisk “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Lisk or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Lisk set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Lisk discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3A illustrates an example TSS-enabled PoP (TEP) 300. A second package 315 includes a second package substrate 320 as is conventional in the PoP arts. A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts. First package substrate 360 and second package substrate 320 may each comprise an organic substrate, a semiconductor substrate such as silicon, glass, ceramic, or other suitable materials. Regardless of what materials are used to construct the</p>

package substrates, no interconnects 120 as discussed with regard to MEP 100 are necessary to accommodate the input/output (I/O) signaling for a plurality of second package dies 324 in second package 315. Instead, through silicon vias 322 in first package die 310 accommodate all the I/O signaling for second package dies 324. As used herein, “input/output signaling” includes all the electrical signals received by the second package die(s), including power and ground. Similarly, “input/output signaling” includes all output signals from the second package die(s). Alternative embodiments for TEP 300 may include just a single second package die 324 instead of a plurality of such dies. The terms “first package” and “second package” are used herein simply to denote the different packages as is known in the PoP arts.” Lisk, [0023-0024].



Lisk, FIG. 3A

“Because virtually the entire area of first package die 310 may be used for through silicon vias 322, the interconnect restrictions in PoP technology with regard to the second package die I/O are avoided. In contrast, prior art PoP architectures require the interconnects between the top package substrate and the bottom package substrate to avoid the substrate area on the

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

	<p>bottom package substrate occupied by the bottom package die such as discussed above with regard to MEP 100. Prior-art PoP architectures thus have limited signal density as compared to the improved PoPs disclosed herein because the package-to-package interconnects are not limited to a placement on the peripheral of the bottom package substrate. TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such as micro-bumps 323. Interposer 305 may comprise a semiconductor substrate such as silicon, glass, or other suitable materials.” Lisk, [0025-0026].</p> <p>“FIG. 3B illustrates an alternative embodiment in which a TEP 350 does not include an interposer. Bumps 325 on pads on a lower surface of second package substrate 320 thus couple directly through first package die pads (not illustrated) to first package die through silicon vias 322 (or are coupled to through silicon vias 322 through a backside redistribution layer). As compared to TEP 300, TEP 350 requires fewer manufacturing steps. However, interposer 305 enables additional redistribution of the I/O signaling to second package dies 324. Bumps 325 may comprise interconnects such as copper pillars (micro-bumps), direct metal-to-metal bonds, or collapsed collapse chip connection (C4) bumps or solder balls. Regardless of whether an interposer is included or not, bumps 325 are not restricted to an annular region outside of the area occupied by first package die 310 in direct contrast to conventional PoPs such as MEP 100.” Lisk, [0030-0031].</p>
--	---

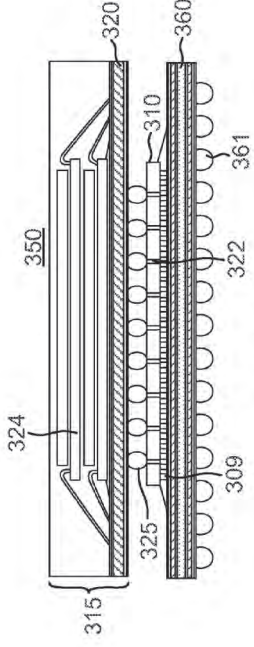
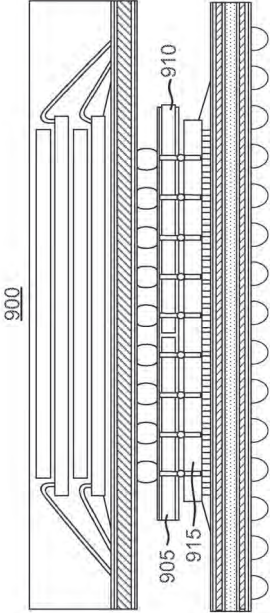


FIG. 3B

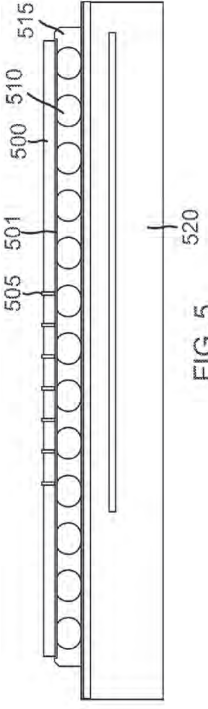
Lisk, FIG. 3B

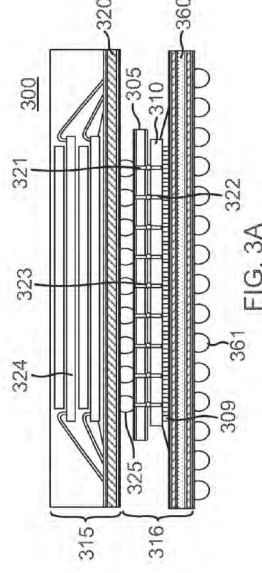
“As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520. However, it will be appreciated that in alternative embodiments, the active surface orientation of first package die 500 may be reversed. In other words, the advantageous TSS-enabled PoP concepts disclosed herein may be applied to any active surface orientation. An underfill 515 such as an epoxy or other polymeric material may then be applied using capillary action. Alternatively, underfill 515 may be pre-applied at the same time bumps 510 are applied. A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown. Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0032-0033].

	<div> <p>FIG. 5</p> </div> <div> <p>Lisk, FIG. 5</p> </div> <div> <p>“Mold compound 715 may then be applied to complete a TEP first package 700 as shown in FIG. 7. An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p> </div> <div> <p>FIG. 7</p> </div> <div> <p>Lisk, FIG. 7</p> </div> <div> <p>“As discussed above, for TEP embodiments that include an interposer, the interposer may be passive or contain active elements. In that regard, an active interposer comprises another die comparable to the first package die discussed above. Several such TSV-containing dies could</p> </div>
--	--

	<p>be stacked within the first package. Moreover, multiple interposers may be used in parallel as shown for TEP 900 of FIG. 9. In particular, an interposer 905 and an interposer 910 both face a back surface of first package die 915. In that regard, interposers 905 and interposer 910 are arranged in parallel in a single layer as opposed to being stacked.” Lisk, [0035].</p>  <p style="text-align: center;">FIG. 9</p> <p>Lisk, FIG. 9</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.A] a bottom package substrate;	<p>Lisk discloses, either expressly or inherently, a bottom package substrate.</p> <p>See, e.g.:</p> <p>“Moreover, the mold through vias or other techniques used to form conventional package-to-package interconnects are unnecessary for the improved PoPs disclosed. The following</p>

	<p>discussion will assume without loss of generality that the first package die is a silicon die such that the through substrate vias it contains are through silicon vias.” Lisk, [0021-0022].</p> <p>“A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts. First package substrate 360 and second package substrate 320 may each comprise an organic substrate, a semiconductor substrate such as silicon, glass, ceramic, or other suitable materials.” Lisk, [0023].</p> <p>“Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325. More generally, second package substrate 320 may be considered to have a first surface and an opposing second surface.” Lisk, [0027].</p> <p>“Such external device I/O would be carried between interposer 305 and the external devices through silicon vias 322 in first package die 310, bumps 309, first package substrate 360 and balls 361 on a lower surface of first package substrate 360.” Lisk, [0028].</p> <p>“In contrast, MEP 100 would need larger substrate sizes in that it must place its interconnects 120 outside of bottom die 115. In this fashion, the TEPs disclosed herein advantageously will have less warpage as compared to analogous MEPs in that warpage depends upon (among other things), the size of the substrates for the top and bottom packages.” Lisk, [0031].</p> <p>“As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520.” Lisk, [0032].</p>
--	---

	 <p>FIG. 5</p> <p>Lisk, FIG. 5</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Lisk discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p> <p>“FIG. 3A illustrates an example TSS-enabled PoP (TEP) 300. A second package 315 includes a second package substrate 320 as is conventional in the PoP arts. A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts. First package substrate 360 and second package substrate 320 may each comprise an organic substrate, a semiconductor substrate such as silicon, glass, ceramic, or other suitable materials.” Lisk, [0023].</p>



“The terms “first package” and “second package” are used herein simply to denote the different packages as is known in the PoP arts. In that regard, first package 316 of FIG. 3A corresponds to a ‘bottom package’ as that term is used in the PoP arts. Similarly second package 315 corresponds to a “top package” as that term is used in the PoP arts.” Lisk, [0024].

“In TEP 300, second package dies 324 are wire-bonded to second package substrate 320 although other mounting technologies may be used such as surface mounting. The wire bonds carry the I/O signaling between second package dies 324 and second package substrate 320. In turn, the I/O signaling for second package dies 324 is carried between second package substrate 320 and interposer 305 through bumps 325. Finally, the I/O signaling for second package dies 324 is carried between interposer 305 and first package die 310 through interposer through silicon vias 321 and first package die's through silicon vias 322. Some I/O signaling for second package dies 324 may originate from or be transmitted to external devices. Such external device I/O would be carried between interposer 305 and the external devices through through silicon vias 322 in first package die 310, bumps 309, first package substrate 360 and balls 361 on a lower surface of first package substrate 360.” Lisk, [0028].

“FIG. 3B illustrates an alternative embodiment in which a TEP 350 does not include an interposer. Bumps 325 on pads on a lower surface of second package substrate 320 thus couple directly through first package die pads (not illustrated) to first package die through silicon vias 322 (or are coupled to through silicon vias 322 through a backside redistribution layer).” Lisk, [0030].

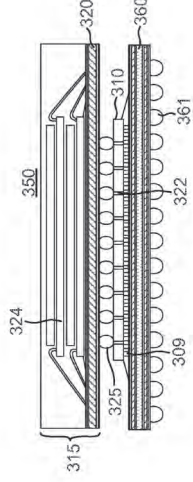


FIG. 3B

Lisk, FIG. 3B

“FIG. 4 illustrates a plan view of a lower surface of second package substrate 320 to show how bumps 325 may use the entire area 400 that faces either first package die 310 (for an interposer-less embodiment such as TEP 350) or interposer 305 (in an interposer-containing embodiment such as TEP 300). In this fashion, substantially more I/O signals can be accommodated as compared to a conventional PoP embodiment. Moreover, because second package substrate 320 can receive bumps 325 across the entire surface area 400 facing first package die 310 (or interposer 305), the size of second package substrate 320 and first package substrate 360 may be reduced accordingly.” Lisk, [0031].

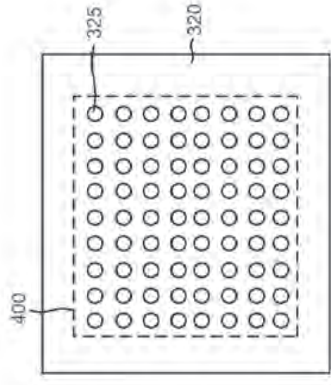


FIG. 4

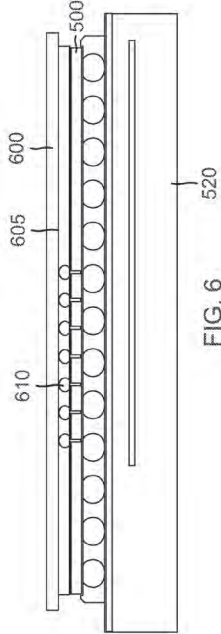
Lisk, FIG. 4

“An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].

To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

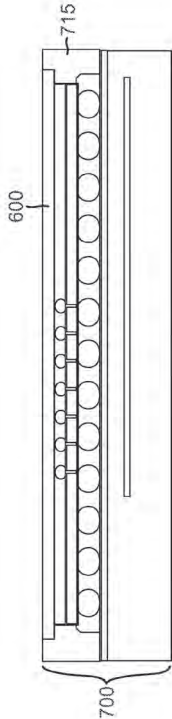
Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Lisk discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such as micro-bumps 323. Interposer 305 may comprise a semiconductor substrate such as silicon, glass, or other suitable materials. Should interposer 305 comprise a silicon substrate, TSVs 321 are through silicon vias. On the other hand, should interposer 305 comprise glass, TSVs 322 are through glass vias (TGVs). The following discussion will assume without loss of generality that TSVs 321 are through silicon vias. Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die's through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325.” Lisk, [0026-0027].</p> <p>“A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown. Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0033].</p>
---	---

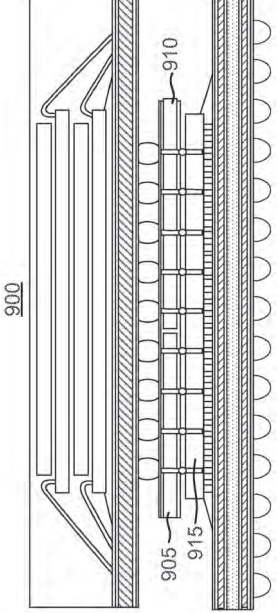


Lisk, FIG. 6

“Mold compound 715 may then be applied to complete a TEP first package 700 as shown in FIG. 7. An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].



Lisk, FIG. 7

	<p>“Moreover, multiple interposers may be used in parallel as shown for TEP 900 of FIG. 9. In particular, an interposer 905 and an interposer 910 both face a back surface of first package die 915. In that regard, interposers 905 and interposer 910 are arranged in parallel in a single layer as opposed to being stacked.” Lisk, [0035].</p>  <p style="text-align: center;">FIG. 9</p> <p>Lisk, FIG. 9</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Lisk discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, e.g.:</p> <p>“TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such</p>

	<p>as micro-bumps 323. Interposer 305 may comprise a semiconductor substrate such as silicon, glass, or other suitable materials.” Lisk, [0026].</p> <p>“Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die’s through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310.” Lisk, [0026-0027].</p> <p>“A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown.” Lisk, [0033].</p> <p>“In particular, an interposer 905 and an interposer 910 both face a back surface of first package die 915. In that regard, interposers 905 and interposer 910 are arranged in parallel in a single layer as opposed to being stacked.” Lisk, [0035].</p> <div> </div> <p style="text-align: center;">FIG. 9</p> <p>Lisk, FIG. 9</p>
--	--

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

	<p>“Moreover, multiple interposers may be used in parallel as shown for TEP 900 of FIG. 9.” Lisk, [0035].</p> <p>“Referring again to first package die 310, first package die 310 may be considered to include a means for carrying the input/output signaling for at least one second package die. In one embodiment, such a means comprises TSVs 322. In an alternative embodiment, the means may comprise deep diffusion regions that couple between pads on a back surface of first package die 310 and active circuitry on an active front surface for first package die 310.” Lisk, [0036].</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate;</p>	<p>Lisk discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Because virtually the entire area of first package die 310 may be used for through silicon vias 322, the interconnect restrictions in PoP technology with regard to the second package die I/O are avoided.” Lisk, [0025].</p>

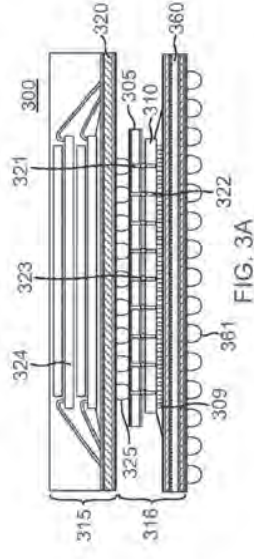
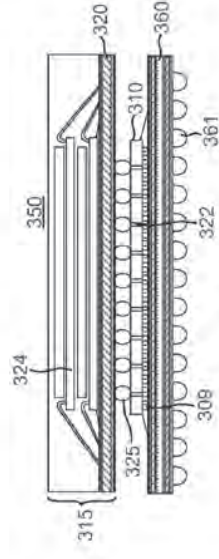


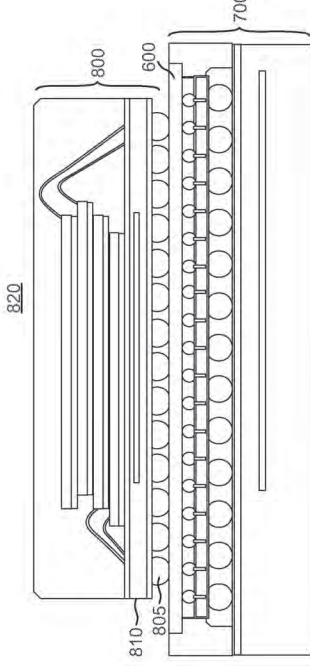
FIG. 3B

Lisk, FIGS. 3A, 3B

“TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such as micro-bumps 323. Interposer 305 may comprise a semiconductor substrate such as silicon, glass, or other suitable materials. Should interposer 305 comprise a silicon substrate, TSVs 321 are through silicon vias.” Lisk, [0026].

“Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die's through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second

	<p>package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325.” Lisk, [0026-0027].</p> <p>“In turn, the I/O signaling for second package dies 324 is carried between second package substrate 320 and interposer 305 through bumps 325. Finally, the I/O signaling for second package dies 324 is carried between interposer 305 and first package die 310 through interposer through silicon vias 321 and first package die’s through silicon vias 322.” Lisk, [0028].</p> <p>“A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown.” Lisk, [0033].</p> <div> <p>FIG. 6</p> </div> <p>Lisk, FIG. 6</p> <p>“An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate</p>
--	--

	<p>810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p>  <p style="text-align: center;">FIG. 8</p> <p>Lisk, FIG. 8</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Lisk discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p>See, <i>e.g.</i>:</p>

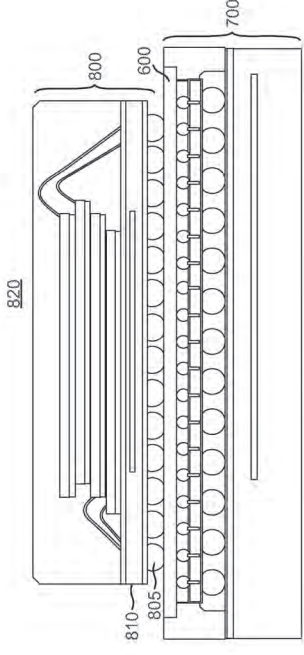
	<p>“A via-enabled package-on-package (PoP) circuit includes a first package die having a plurality of through substrate vias (TSVs). The TSVs are configured to carry the input/output signaling for at least one second package die in an adjoining second package.” Lisk, [0005].</p> <p>“Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die's through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325. More generally, second package substrate 320 may be considered to have a first surface and an opposing second surface.” Lisk, [0027].</p> <p>“Interposer 305 may include active devices and/or passive components in some embodiments. As used herein, “bump” is used to denote a structure such as a solder ball or bump. In addition, this term will be understood to also include structures such as copper pillars. In that regard, bumps 325 refer generically to the interconnecting structures that couple from pads on a bottom surface of second package substrate 320 to through silicon vias 321 on interposer 305. Directly-Coupled TSS-Enabled PoP (No Interposer) FIG. 3B illustrates an alternative embodiment in which a TEP 350 does not include an interposer.” Lisk, [0028-0030].</p> <p>“Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0033].</p> <p>“A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown. Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0033].</p>
--	--

	<div> </div> <p>Lisk, FIG. 6</p> <p>“An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Lisk discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

	<div> </div> <p>FIG. 9</p> <p>Lisk, FIG. 9</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Lisk discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325.” Lisk, [0027].</p> <p>“More generally, second package substrate 320 may be considered to have a first surface and an opposing second surface. Second package dies 324 are mounted on the first surface of</p>

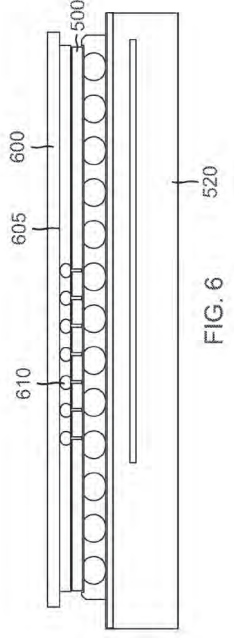
Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

	<p>second package substrate 320 whereas bumps 325 connect to the opposing second surface of second package substrate 320.” Lisk, [0027].</p> <p>“In turn, the I/O signaling for second package dies 324 is carried between second package substrate 320 and interposer 305 through bumps 325.” Lisk, [0028].</p> <p>“Bumps 325 on pads on a lower surface of second package substrate 320 thus couple directly through first package die pads (not illustrated) to first package die through silicon vias 322 (or are coupled to through silicon vias 322 through a backside redistribution layer).” Lisk, [0030].</p> <p>“Bumps 325 may comprise interconnects such as copper pillars (micro-bumps), direct metal-to-metal bonds, or collapsed collapse chip connection (C4) bumps or solder balls.” Lisk, [0030].</p> <p>“In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p>
--	--

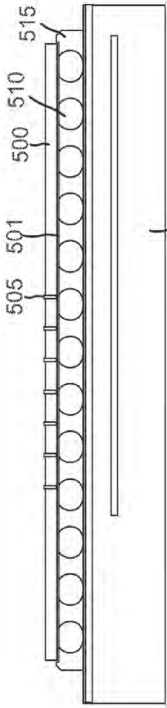
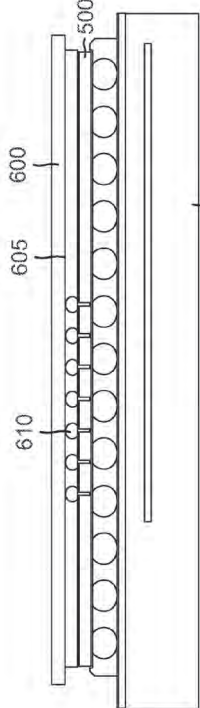
	 <p style="text-align: center;">FIG. 8</p> <p>Lisk, FIG. 8</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Lisk discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts.” Lisk, [0023].</p>

	<p>“Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die’s through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325.” Lisk, [0026-0027].</p> <p>“In addition, this term will be understood to also include structures such as copper pillars. In that regard, bumps 325 refer generically to the interconnecting structures that couple from pads on a bottom surface of second package substrate 320 to through silicon vias 321 on interposer 305.” Lisk, [0029].</p> <p>“As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520.” Lisk, [0032].</p> <div> <p>FIG. 5</p> </div> <p>Lisk, FIG. 5</p> <p>“Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0033].</p>
--	--

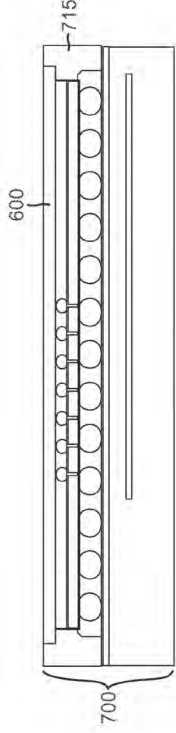
Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

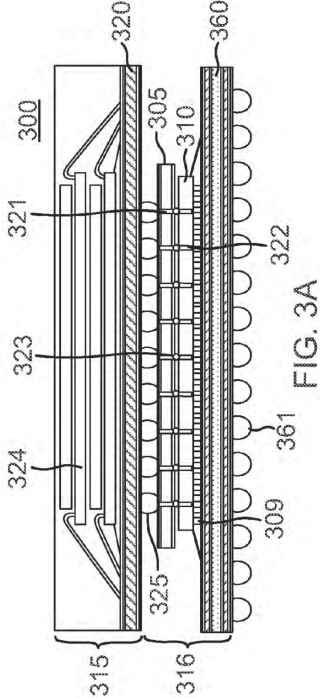
	<p>“A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown. Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0033].</p>  <p>FIG. 6</p> <p>Lisk, FIG. 6</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Lisk discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“Instead, through silicon vias 322 in first package die 310 accommodate all the I/O signaling for second package dies 324. As used herein, “input/output signaling” includes all the</p>

	<p>electrical signals received by the second package die(s), including power and ground. Similarly, “input/output signaling” includes all output signals from the second package die(s).” Lisk, [0023].</p> <p>“Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die’s through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325.” Lisk, [0026-0027].</p> <p>“In turn, the I/O signaling for second package dies 324 is carried between second package substrate 320 and interposer 305 through bumps 325. Finally, the I/O signaling for second package dies 324 is carried between interposer 305 and first package die 310 through interposer through silicon vias 321 and first package die’s through silicon vias 322. Some I/O signaling for second package dies 324 may originate from or be transmitted to external devices. Such external device I/O would be carried between interposer 305 and the external devices through through silicon vias 322 in first package die 310, bumps 309, first package substrate 360 and balls 361 on a lower surface of first package substrate 360.” Lisk, [0028].</p> <p>“As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520.” Lisk, [0032].</p>
--	--

	<div><p>FIG. 5</p></div> <div><p>Lisk, FIG. 5</p></div> <div><p>“A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown. Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0033].</p></div> <div><p>FIG. 6</p></div> <div><p>Lisk, FIG. 6</p></div> <div><p>“Mold compound 715 may then be applied to complete a TEP first package 700 as shown in FIG. 7. An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through</p></div>
--	---

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

	<p>interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p>  <p style="text-align: center;">FIG. 7</p> <p>Lisk, FIG. 7</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Lisk discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“A via-enabled package-on-package (PoP) circuit includes a first package die having a plurality of through substrate vias (TSVs). The TSVs are configured to carry the input/output signaling for at least one second package die in an adjoining second package.” Lisk, [0005].</p>

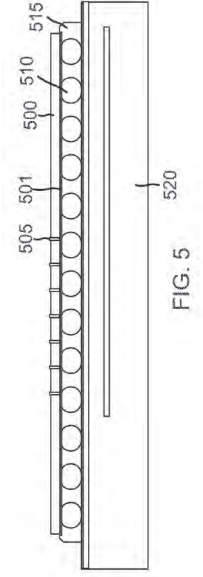
	<p>“FIG. 3A illustrates an example TSS-enabled PoP (TEP) 300. A second package 315 includes a second package substrate 320 as is conventional in the PoP arts. A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts.” Lisk, [0023].</p>  <p>Lisk, FIG. 3A</p> <p>“Prior-art PoP architectures thus have limited signal density as compared to the improved PoPs disclosed herein because the package-to-package interconnects are not limited to a placement on the peripheral of the bottom package substrate. TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such as micro-bumps 323. Interposer 305 may comprise a semiconductor substrate such as silicon, glass, or other suitable materials. Should interposer 305 comprise a silicon substrate, TSVs 321 are through silicon vias. On the other hand, should interposer 305 comprise glass, TSVs 332 are through glass vias (TGVs). The following discussion will assume without loss of generality that TSVs 321</p>
--	---

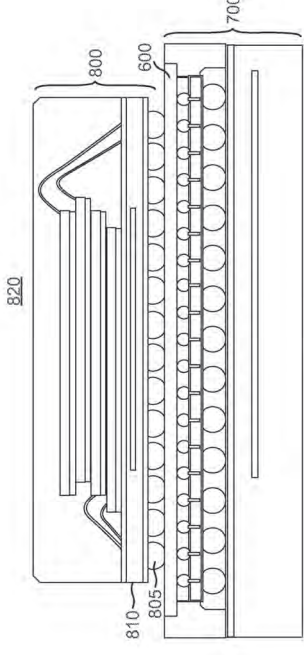
	<p>are through silicon vias. Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die's through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325.” Lisk, [0025-0027].</p> <p>“In TEP 300, second package dies 324 are wire-bonded to second package substrate 320 although other mounting technologies may be used such as surface mounting. The wire bonds carry the I/O signaling between second package dies 324 and second package substrate 320. In turn, the I/O signaling for second package dies 324 is carried between second package substrate 320 and interposer 305 through bumps 325. Finally, the I/O signaling for second package dies 324 is carried between interposer 305 and first package die 310 through interposer through silicon vias 321 and first package die's through silicon vias 322. Some I/O signaling for second package dies 324 may originate from or be transmitted to external devices. Such external device I/O would be carried between interposer 305 and the external devices through through silicon vias 322 in first package die 310, bumps 309, first package substrate 360 and balls 361 on a lower surface of first package substrate 360. Interposer 305 may include active devices and/or passive components in some embodiments.” Lisk, [0028].</p> <p>“As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520. However, it will be appreciated that in alternative embodiments, the active surface orientation of first package die 500 may be reversed.” Lisk, [0032].</p>
--	--

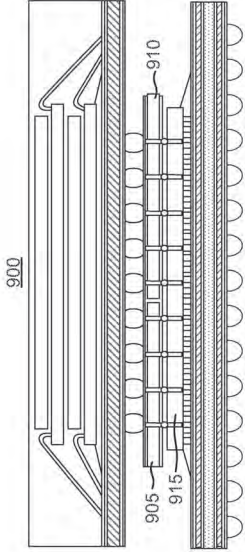
	<div> </div> <div> <p>Lisk, FIG. 5</p> </div> <div> <p>“Mold compound 715 may then be applied to complete a TEP first package 700 as shown in FIG. 7. An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p> </div> <div> </div> <div> <p>Lisk, FIG. 7</p> </div> <div> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p> </div>
--	--

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and substrate, and	<p>Lisk discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts.” Lisk, [0023].</p> <p>“Regardless of what materials are used to construct the package substrates, no interconnects 120 as discussed with regard to MEP 100 are necessary to accommodate the input/output (I/O) signaling for a plurality of second package dies 324 in second package 315. Instead, through silicon vias 322 in first package die 310 accommodate all the I/O signaling for second package dies 324.” Lisk, [0023].</p> <p>“In that regard, first package 316 of FIG. 3A corresponds to a ‘bottom package’ as that term is used in the PoP arts. Similarly second package 315 corresponds to a “top package” as that term is used in the PoP arts. But such references to “top” or “bottom” are not tied to any particular reference system. In other words, a bottom package does not become a top package simply because a PoP is flipped over. Because virtually the entire area of first package die 310 may be used for through silicon vias 322, the interconnect restrictions in PoP technology with regard to the second package die I/O are avoided.” Lisk, [0024-0025].</p>

	<p>“In TEP 300, second package dies 324 are wire-bonded to second package substrate 320 although other mounting technologies may be used such as surface mounting.” Lisk, [0028].</p> <p>“As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520.” Lisk, [0032].</p> <div></div> <p>Lisk, FIG. 5</p> <p>“The manufacture of a first package for an interposer-containing TEP embodiment will now be discussed with regard to FIGS. 5 through 8. The manufacturing process uses a first package die 500 that incorporates through silicon vias 505 to accommodate not only the I/O signaling between first package die 500 and the second package dies but also for external I/O signaling to the second package die (or dies). For example, through silicon vias 505 may accommodate ground and power needs for the second package dies. As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520.” Lisk, [0032].</p>
--	--

	 <p style="text-align: center;">FIG. 8</p> <p>Lisk, FIG. 8</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Lisk discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, <i>e.g.</i>:</p> <p>“FIG. 9 is a cross-sectional view of a TEP including a plurality of interposers.” Lisk, [0017].</p> <p>“Several such TSV-containing dies could be stacked within the first package. Moreover, multiple interposers may be used in parallel as shown for TEP 900 of FIG. 9. In particular, an interposer 905 and an interposer 910 both face a back surface of first package die 915. In</p>

	<p>that regard, interposers 905 and interposer 910 are arranged in parallel in a single layer as opposed to being stacked.” Lisk, [0035].</p> <div></div> <p>FIG. 9</p> <p>Lisk, FIG. 9</p> <p>“As discussed above, for TEP embodiments that include an interposer, the interposer may be passive or contain active elements. In that regard, an active interposer comprises another die comparable to the first package die discussed above. Several such TSV-containing dies could be stacked within the first package. Moreover, multiple interposers may be used in parallel as shown for TEP 900 of FIG. 9.” Lisk, [0035].</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Lisk discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“A second package 315 includes a second package substrate 320 as is conventional in the PoP arts. A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts. First package substrate 360 and second package substrate 320 may each comprise an organic substrate, a semiconductor substrate such as silicon, glass, ceramic, or other suitable materials. Regardless of what materials are used to construct the package substrates, no interconnects 120 as discussed with regard to MEP 100 are necessary to accommodate the input/output (I/O) signaling for a plurality of second package dies 324 in second package 315. Instead, through silicon vias 322 in first package die 310 accommodate all the I/O signaling for second package dies 324.” Lisk, [0023].</p> <p>“FIG. 3A illustrates an example TSS-enabled PoP (TEP) 300. A second package 315 includes a second package substrate 320 as is conventional in the PoP arts. A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts. First package substrate 360 and second package substrate 320 may each comprise an organic substrate, a semiconductor substrate such as silicon, glass, ceramic, or other suitable materials. Regardless of what materials are used to construct the package substrates, no interconnects 120 as discussed with regard to MEP 100 are necessary</p>

	<p>to accommodate the input/output (I/O) signaling for a plurality of second package dies 324 in second package 315. Instead, through silicon vias 322 in first package die 310 accommodate all the I/O signaling for second package dies 324. As used herein, “input/output signaling” includes all the electrical signals received by the second package die(s), including power and ground. Similarly, “input/output signaling” includes all output signals from the second package die(s). Alternative embodiments for TEP 300 may include just a single second package die 324 instead of a plurality of such dies. The terms “first package” and “second package” are used herein simply to denote the different packages as is known in the PoP arts. In that regard, first package 316 of FIG. 3A corresponds to a ‘bottom package’ as that term is used in the PoP arts. Similarly second package 315 corresponds to a “top package” as that term is used in the PoP arts. But such references to “top” or “bottom” are not tied to any particular reference system. In other words, a bottom package does not become a top package simply because a PoP is flipped over. Because virtually the entire area of first package die 310 may be used for through silicon vias 322, the interconnect restrictions in PoP technology with regard to the second package die I/O are avoided. In contrast, prior art PoP architectures require the interconnects between the top package substrate and the bottom package substrate to avoid the substrate area on the bottom package substrate occupied by the bottom package die such as discussed above with regard to MEP 100. Prior-art PoP architectures thus have limited signal density as compared to the improved PoPs disclosed herein because the package-to-package interconnects are not limited to a placement on the peripheral of the bottom package substrate. TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such as micro-bumps 323. Interposer 305 may comprise a semiconductor substrate such as silicon, glass, or other suitable materials. Should interposer 305 comprise a silicon substrate, TSVs 321 are through silicon vias. On the other hand, should interposer 305 comprise glass, TSVs 332 are through glass vias (TGVs). The following discussion will assume without loss of generality that TSVs 321 are through silicon</p>
--	--

vias. Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die's through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325." Lisk, [0023-0027].

“FIG. 3B illustrates an alternative embodiment in which a TEP 350 does not include an interposer. Bumps 325 on pads on a lower surface of second package substrate 320 thus couple directly through first package die pads (not illustrated) to first package die through silicon vias 322 (or are coupled to through silicon vias 322 through a backside redistribution layer). As compared to TEP 300, TEP 350 requires fewer manufacturing steps. However, interposer 305 enables additional redistribution of the I/O signaling to second package dies 324. Bumps 325 may comprise interconnects such as copper pillars (micro-bumps), direct metal-to-metal bonds, or collapsed collapse chip connection (C4) bumps or solder balls. Regardless of whether an interposer is included or not, bumps 325 are not restricted to an annular region outside of the area occupied by first package die 310 in direct contrast to conventional PoPs such as MEP 100.” Lisk, [0030-0031].

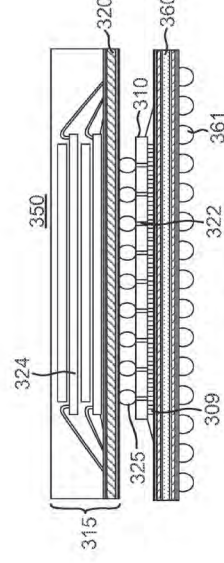
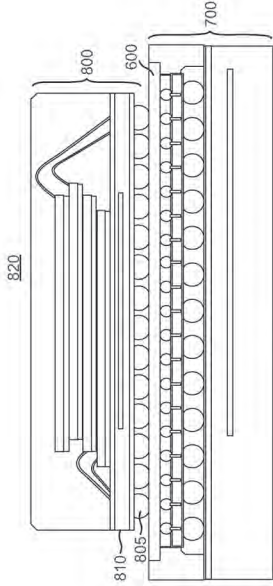


FIG. 3B

	<p>Lisk, FIG. 3B</p> <p>“An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p> <div></div> <p>FIG. 8</p> <p>Lisk, FIG. 8</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Lisk discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“A second package 315 includes a second package substrate 320 as is conventional in the PoP arts. A first package 316 includes a first package substrate 360 on which a first package die 310 is mounted using interconnects such as controlled collapse chip connection (C4) flip-chip bumps 309 as is also conventional in the PoP arts. First package substrate 360 and second package substrate 320 may each comprise an organic substrate, a semiconductor substrate such as silicon, glass, ceramic, or other suitable materials. Regardless of what materials are used to construct the package substrates, no interconnects 120 as discussed with regard to MEP 100 are necessary to accommodate the input/output (I/O) signaling for a plurality of second package dies 324 in second package 315. Instead, through silicon vias 322 in first package die 310 accommodate all the I/O signaling for second package dies 324.” Lisk, [0023].</p> <p>“Because virtually the entire area of first package die 310 may be used for through silicon vias 322, the interconnect restrictions in PoP technology with regard to the second package die I/O are avoided. In contrast, prior art PoP architectures require the interconnects between the top package substrate and the bottom package substrate to avoid the substrate area on the bottom package substrate occupied by the bottom package die such as discussed above with regard to MEP 100. Prior-art PoP architectures thus have limited signal density as compared</p>

	<p>to the improved PoPs disclosed herein because the package-to-package interconnects are not limited to a placement on the peripheral of the bottom package substrate.” Lisk, [0025].</p> <p>“TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such as micro-bumps 323. Interposer 305 may comprise a semiconductor substrate such as silicon, glass, or other suitable materials. Should interposer 305 comprise a silicon substrate, TSVs 321 are through silicon vias. On the other hand, should interposer 305 comprise glass, TSVs 322 are through glass vias (TGVs). The following discussion will assume without loss of generality that TSVs 321 are through silicon vias. Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die's through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325. More generally, second package substrate 320 may be considered to have a first surface and an opposing second surface. Second package dies 324 are mounted on the first surface of second package substrate 320 whereas bumps 325 connect to the opposing second surface of second package substrate 320.” Lisk, [0026-0027].</p> <p>“In TEP 300, second package dies 324 are wire-bonded to second package substrate 320 although other mounting technologies may be used such as surface mounting. The wire bonds carry the I/O signaling between second package dies 324 and second package substrate 320. In turn, the I/O signaling for second package dies 324 is carried between second package substrate 320 and interposer 305 through bumps 325. Finally, the I/O signaling for second package dies 324 is carried between interposer 305 and first package die 310 through</p>
--	--

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

	<p>interposer through silicon vias 321 and first package die's through silicon vias 322.” Lisk, [0028].</p> <p>“FIG. 3B illustrates an alternative embodiment in which a TEP 350 does not include an interposer. Bumps 325 on pads on a lower surface of second package substrate 320 thus couple directly through first package die pads (not illustrated) to first package die through silicon vias 322 (or are coupled to through silicon vias 322 through a backside redistribution layer). As compared to TEP 300, TEP 350 requires fewer manufacturing steps. However, interposer 305 enables additional redistribution of the I/O signaling to second package dies 324.” Lisk, [0030].</p> <p>“Regardless of whether an interposer is included or not, bumps 325 are not restricted to an annular region outside of the area occupied by first package die 310 in direct contrast to conventional PoPs such as MEP 100. FIG. 4 illustrates a plan view of a lower surface of second package substrate 320 to show how bumps 325 may use the entire area 400 that faces either first package die 310 (for an interposer-less embodiment such as TEP 350) or interposer 305 (in an interposer-containing embodiment such as TEP 300). In this fashion, substantially more I/O signals can be accommodated as compared to a conventional PoP embodiment.” Lisk, [0031].</p>
--	---

	<div></div> <p>FIG. 4</p> <p>Lisk, FIG. 4</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the	Lisk discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate. <i>See, e.g.:</i>

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

<p>plurality of top metal pillars of the bottom package substrate.</p>	<p>“Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon vias 321 in interposer 305 may couple to the first package die’s through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325.” Lisk, [0026-0027].</p> <p>“Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325. More generally, second package substrate 320 may be considered to have a first surface and an opposing second surface.” Lisk, [0027].</p> <p>“In turn, the I/O signaling for second package dies 324 is carried between second package substrate 320 and interposer 305 through bumps 325. Finally, the I/O signaling for second package dies 324 is carried between interposer 305 and first package die 310 through interposer through silicon vias 321 and first package die’s through silicon vias 322.” Lisk, [0028].</p> <p>“Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0033].</p> <p>“In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p>
--	--

Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

	<p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

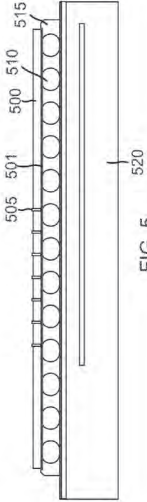
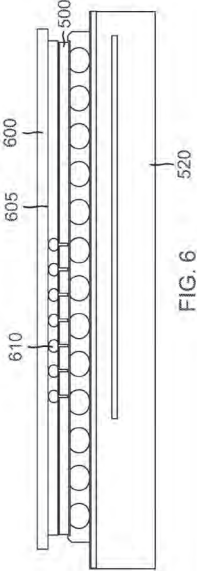
Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Lisk discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such as micro-bumps 323. Interposer 305 may comprise a semiconductor substrate such as silicon, glass, or other suitable materials. Should interposer 305 comprise a silicon substrate, TSVs 321 are through silicon vias. On the other hand, should interposer 305 comprise glass, TSVs 332 are through glass vias (TGVs). The following discussion will assume without loss of generality that TSVs 321 are through silicon vias. Interposer 305 allows for additional redistribution of the I/O signaling to second package dies 324. Alternatively, through silicon</p>

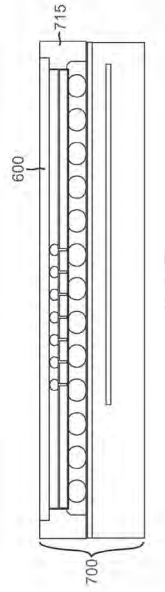
Appendix A-22 - Invalidity of U.S. Patent No. 9859202 in view of Lisk - U.S. Patent Publication No. 20140252561

	<p>vias 321 in interposer 305 may couple to the first package die's through silicon vias 322 through a backside redistribution layer (not illustrated) on the backside of first package die 310. Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325." Lisk, [0026-0027].</p> <p>"As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520." Lisk, [0032].</p> <p>"A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown. Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression." Lisk, [0033].</p> <p>"Mold compound 715 may then be applied to complete a TEP first package 700 as shown in FIG. 7. An upper surface of interposer 600 is exposed in mold compound 715 such that mold compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820." Lisk, [0034].</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the plurality of metal pads of the bottom package substrate, and bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the corresponding top metal pads of the spacer connector.</p>	<p>Lisk discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“TEP 300 includes an interposer 305 having through substrate vias (TSVs) 321 that couple to through silicon vias 322 in first package die 310 through corresponding interconnects such as micro-bumps 323.” Lisk, [0026].</p> <p>“Pads (not illustrated) on a lower surface of second package substrate 320 couple to the interposer through silicon vias 321 through interconnects such as bumps 325.” Lisk, [0027].</p> <p>“Bumps 325 may comprise interconnects such as copper pillars (micro-bumps), direct metal-to-metal bonds, or collapsed collapse chip connection (C4) bumps or solder balls.” Lisk, [0030].</p>

	<p>“As shown in FIG. 5, pads (not illustrated) on an active surface 501 for first package die 500 are mounted through flip-chip bumps 510 to corresponding pads (also not shown for illustration clarity) on a first package substrate 520.” Lisk, [0032].</p>  <p>FIG. 5</p> <p>Lisk, FIG. 5</p> <p>“A through-silicon-via-fabricated interposer 600 may then be bonded to a back surface 605 of first package die 500 as shown in FIG. 6. For illustration clarity, the through silicon vias in interposer 600 are not shown. Bumps 610 couple pads on first package die 500 to corresponding pads on interposer 600 in response to thermo-compression.” Lisk, [0033].</p>  <p>FIG. 6</p> <p>Lisk, FIG. 6</p> <p>“Mold compound 715 may then be applied to complete a TEP first package 700 as shown in FIG. 7. An upper surface of interposer 600 is exposed in mold compound 715 such that mold</p>
--	--

	<p>compound 715 only partially encases interposer 600. In this fashion, pads (not illustrated) on the exposed surface of interposer 600 may then be bonded as shown in FIG. 8 through interconnects 805 to corresponding pads on a lower surface of a second package substrate 810 for a second package 800 to complete the manufacture of an interposer-containing TEP 820.” Lisk, [0034].</p> <div></div> <p>FIG. 7</p> <p>Lisk, FIG. 7</p> <p>To the extent Plaintiff contends that Lisk fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Liu - Taiwan Patent Publication No. 200601516

Taiwan Patent Application Publication No. 200601516 (“Liu”) is titled Stacked Multi-Package Module and lists Sheng-Tsung Liu as inventor. Liu anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Liu is a patent publication that was published January 1, 2006. Liu is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Liu, or otherwise rendered obvious by disclosures and teachings of Liu, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Liu does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Liu with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Liu, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

Where the chart below states that Liu “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Liu or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Liu set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Liu discloses, either expressly or inherently, a structure.</p> <p>See, e.g.:</p> <p>“The present invention relates to a stacked multi-package structure, and more particularly to a stacking structure that uses a transfer plate (spacer) to connect a plurality of semiconductor packages.” Liu, [1]³.</p> <p>“Because the interposer substrate must undergo a ball-planting step and two reflow steps, the process is not only time-consuming and costly, but the interposer substrate is also prone to deformation. (3) Summary of the Invention The primary object of the present invention is to</p>

³ All citations to passages from Liu are in reference to the page numbers of a machine-translated English version of the reference.

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>provide a stacked multi-package structure comprising a first semiconductor package, a transfer plate (spacer), and a second semiconductor package. The transfer plate includes a plurality of upper connecting pads, a plurality of lower connecting pads, a plurality of electrical vias with a metal layer, and a plurality of solder materials. The solder materials are formed within the electrical vias and protrude from the upper” Liu, [2].</p> <p>“According to a specific embodiment of the present invention, referring to Figure 1, a stacked multi-package structure 100 comprises a first semiconductor package 110, a transfer plate (spacer) 120, and a second semiconductor package 130.” Liu, [3].</p> <p>“Claim 1. A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p>
--	--

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>“Chinese Abstract (Title: 多封装件堆疊構造) A stacked multi-package structure comprising a first semiconductor package, a transfer plate (spacer), and a second semiconductor package. The transfer plate includes a plurality of upper connecting pads, a plurality of lower connecting pads, and a plurality of electrical vias with a metal layer. The electrical vias connect the upper connecting pads and lower connecting pads. A plurality of solder materials are formed within the electrical vias and protrude from the upper and lower connecting pads of the transfer plate. The solder materials connect the first semiconductor package and the second semiconductor package.” Liu, [6].</p> <p>“Claim 11. A transfer plate suitable for a stacked multi-package structure, having an upper surface and a lower surface, the transfer plate comprising: a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate.” Liu, [7].</p>
--	---

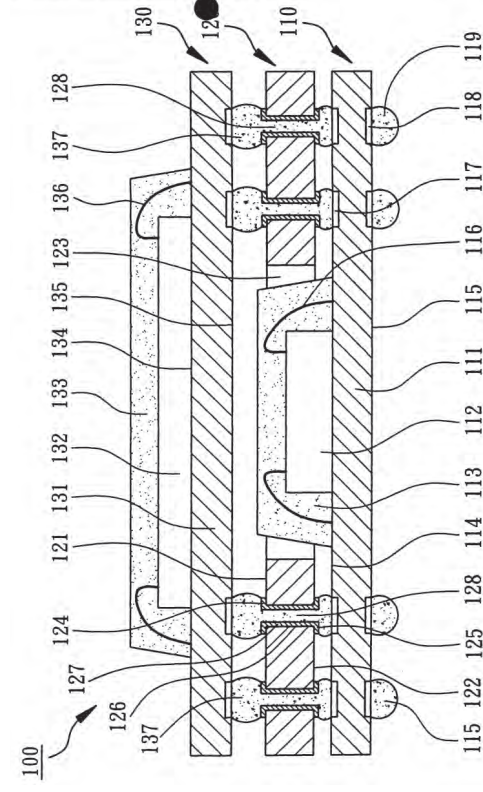


圖 1 第

Liu, FIG. 1.

[1.A] a bottom package substrate;

Liu discloses, either expressly or inherently, a bottom package substrate.

See, e.g.:

“The first semiconductor package 110 may be a ball grid array (BGA) package, which comprises a substrate 111, a chip 112, and an encapsulant 113. The substrate 111 has a first surface 114 and a second surface 115. Referring to Figures 1 and 2, the first surface 114 of the substrate 111 includes a packaging area 114a and a connecting area 114b. In this embodiment, the packaging area 114a is located at the center of the first surface 114 of the substrate. The chip 112 is disposed on the packaging area 114a and is electrically connected to the first surface 114 of the substrate 111 via a plurality of bonding wires 116. The

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>encapsulant 113 is formed on the packaging area 114a to seal the chip 112 and the bonding wires 116. The connecting area 114b is located at the periphery of the first surface 114 of the substrate 111 and surrounds the packaging area 114a. A plurality of bonding pads 117 are formed in the connecting area 114b. A plurality of ball pads 118 are formed on the second surface 115 of the substrate 111, and a plurality of solder balls 119 are planted on the ball pads 118.” Liu, [3].</p> <p>“According to a specific embodiment of the present invention, referring to Figure 1, a stacked multi-package structure 100 comprises a first semiconductor package 110, a transfer plate (spacer) 120, and a second semiconductor package 130.” Liu, [3].</p> <p>“The second semiconductor package 130 may be a ball grid array package, for example a Plastic Ball Grid Array package (PBGA) or a chip-scale package. In this embodiment, a plastic ball grid array package is used. The second semiconductor package 130 comprises a substrate 131, a chip 132, and an encapsulant 133. The substrate 131 has a carrier surface 134 and a bonding surface 135. The chip 132 is disposed on the carrier surface 134 and is electrically connected to the carrier surface 134 of the substrate 131 via a plurality of bonding wires 136. The encapsulant 133 is formed on the carrier surface 134 to seal the chip 132 and the bonding wires 136. A plurality of external terminals 137 are formed on the bonding surface 135 of the substrate 131.” Liu, [4].</p> <p>“Claim 1. A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area,” Liu, [6].</p>
--	---

“Claim 5. The stacked multi-package structure as described in Claim 1, wherein the first semiconductor package is a ball grid array package.” Liu, [6].

“Claim 9. The stacked multi-package structure as described in Claim 1, wherein the second surface of the substrate has a plurality of ball pads formed thereon.” Liu, [7].

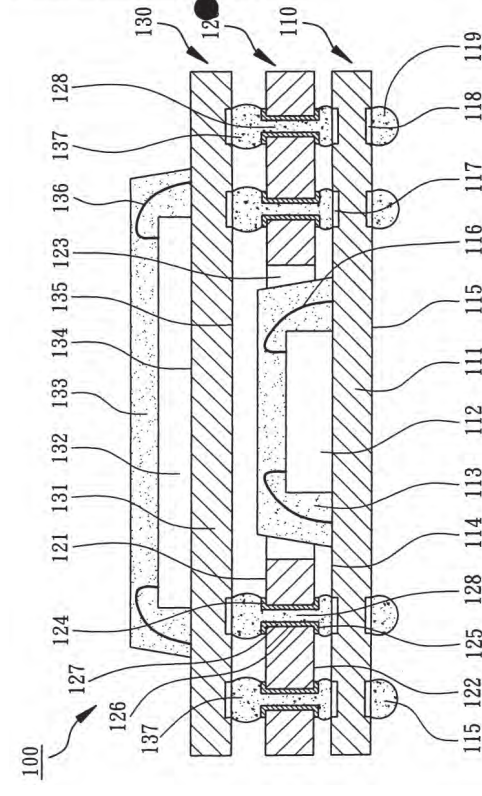


圖 1 第

Liu, FIG. 1.

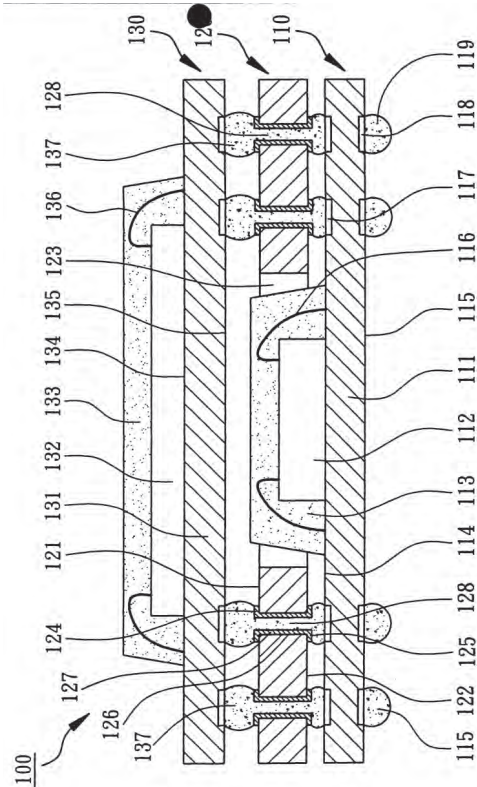
To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Liu discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The present invention relates to a stacked multi-package structure, and more particularly to a stacking structure that uses a transfer plate (spacer) to connect a plurality of semiconductor packages.” Liu, [1].</p> <p>“According to a specific embodiment of the present invention, referring to Figure 1, a stacked multi-package structure 100 comprises a first semiconductor package 110, a transfer plate (spacer) 120, and a second semiconductor package 130.” Liu, [3].</p> <p>“The second semiconductor package 130 comprises a substrate 131, a chip 132, and an encapsulant 133. The substrate 131 has a carrier surface 134 and a bonding surface 135. The chip 132 is disposed on the carrier surface 134 and is electrically connected to the carrier surface 134 of the substrate 131 via a plurality of bonding wires 136. The encapsulant 133 is formed on the carrier surface 134 to seal the chip 132 and the bonding wires 136. A plurality of external terminals 137 are formed on the bonding surface 135 of the substrate 131. The external terminals 137 are selected from solder balls and bumps. The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p> <p>“Therefore, the present invention uses the solder materials 128 of the transfer plate 120 to pass through the electrical vias 126 and bond the bonding pads 117 of the first semiconductor package 110 with the external terminals 137 of the second semiconductor package 130, thereby achieving the effect of multi-package stacking.” Liu, [4].</p>
---	--

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>“Claim 1. A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p> <p>“Chinese Abstract (Title: *4*4#6) A stacked multi-package structure comprising a first semiconductor package, a transfer plate (spacer), and a second semiconductor package. The transfer plate includes a plurality of upper connecting pads, a plurality of lower connecting pads, and a plurality of electrical vias with a metal layer. The electrical vias connect the upper connecting pads and lower connecting pads. A plurality of solder materials are formed within the electrical vias and protrude from the upper and lower connecting pads of the transfer plate. The solder materials connect the first semiconductor package and the second semiconductor package.” Liu, [6].</p>
--	--

	<div><p>The diagram shows a cross-section of a multi-layered assembly. At the top, there is a layer labeled 100. Below it, a series of layers and components are shown. On the left side, labels 127, 126, 137, 124, 121, 131, 132, 133, 134, 135, 123, 136, 137, and 128 point to various layers and features. In the center, there are two large, U-shaped or channel-like structures labeled 115 and 122. To the right of these, there are several vertical, pillar-like structures labeled 114, 113, 112, 111, 115, 116, 117, 118, and 119. At the bottom, there are more layers and components labeled 130, 120, 110, and 119. The diagram illustrates a complex, multi-layered structure with various components and layers.</p></div> <div><p>第 1 圖</p></div> <div><p>Liu, FIG. 1.</p></div>	<p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Liu discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p>	

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>“Because the interposer substrate must undergo a ball-planting step and two reflow steps, the process is not only time-consuming and costly, but the interposer substrate is also prone to deformation. (3) Summary of the Invention The primary object of the present invention is to provide a stacked multi-package structure comprising a first semiconductor package, a transfer plate (spacer), and a second semiconductor package. The transfer plate includes a plurality of upper connecting pads, a plurality of lower connecting pads, a plurality of electrical vias with a metal layer, and a plurality of solder materials. The solder materials are formed within the electrical vias and protrude from the upper” Liu, [2].</p> <p>“A plurality of ball pads 118 are formed on the second surface 115 of the substrate 111, and a plurality of solder balls 119 are planted on the ball pads 118. Referring to Figures 1 and 3, the transfer plate 120 has an upper surface 121, a lower surface 122, and an opening 123. The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110. The transfer plate 120 includes a plurality of upper connecting pads 124, a plurality of lower connecting pads 125, and a plurality of electrical vias 126. The upper connecting pads 124 are formed on the upper surface 121 of the transfer plate 120. The lower connecting pads 125 correspond to the upper connecting pads 124 and are formed on the lower surface 122 of the transfer plate 120. In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123. The diameter of the electrical vias 126 is no less than 1.5 mm. Each electrical via 126 penetrates through the vertically corresponding upper connecting pad 124 and lower connecting pad 125 and has a metal layer 127 formed therein. The metal layer 127 is formed on the sidewall of the corresponding electrical via 126 and connects the corresponding upper connecting pads 124 and” Liu, [3].</p>
--	--

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

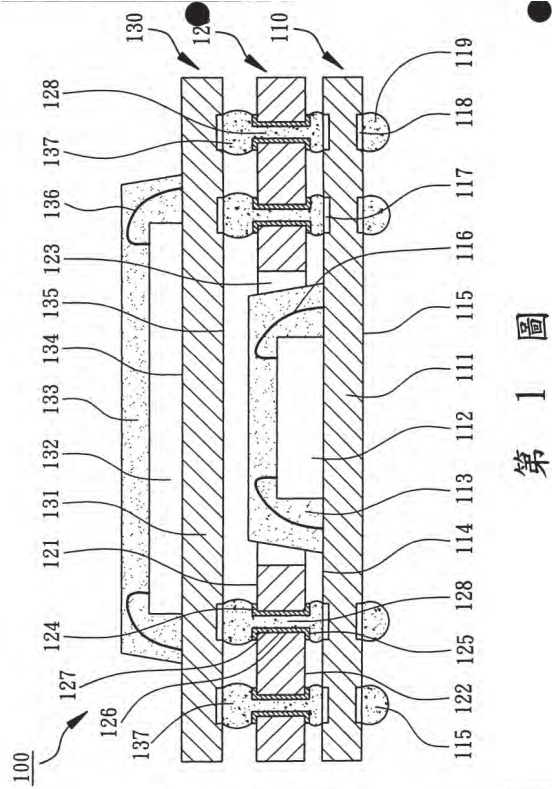
	<p>“According to a specific embodiment of the present invention, referring to Figure 1, a stacked multi-package structure 100 comprises a first semiconductor package 110, a transfer plate (spacer) 120, and a second semiconductor package 130.” Liu, [3].</p> <p>“Therefore, the present invention uses the solder materials 128 of the transfer plate 120 to pass through the electrical vias 126 and bond the bonding pads 117 of the first semiconductor package 110 with the external terminals 137 of the second semiconductor package 130, thereby achieving the effect of multi-package stacking.” Liu, [4].</p> <p>“A stacked multi-package structure comprising a first semiconductor package, a transfer plate (spacer), and a second semiconductor package. The transfer plate includes a plurality of upper connecting pads, a plurality of lower connecting pads, and a plurality of electrical vias with a metal layer. The electrical vias connect the upper connecting pads and lower connecting pads. A plurality of solder materials are formed within the electrical vias and protrude from the upper and lower connecting pads of the transfer plate. The solder materials connect the first semiconductor package and the second semiconductor package.” Liu, [6].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder</p>
--	--

	<p>materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p>
--	---

	<div> </div> <div> <p>第 3 圖</p> </div> <div> <p>Liu, FIG. 3.</p> </div> <div> <p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> </div>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Liu discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, e.g.:</p> <p>“Referring to Figures 1 and 3, the transfer plate 120 has an upper surface 121, a lower surface 122, and an opening 123. The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110. The transfer plate 120 includes a plurality of upper connecting pads 124, a plurality of lower connecting pads 125, and a plurality of electrical vias 126.” Liu, [3].</p>

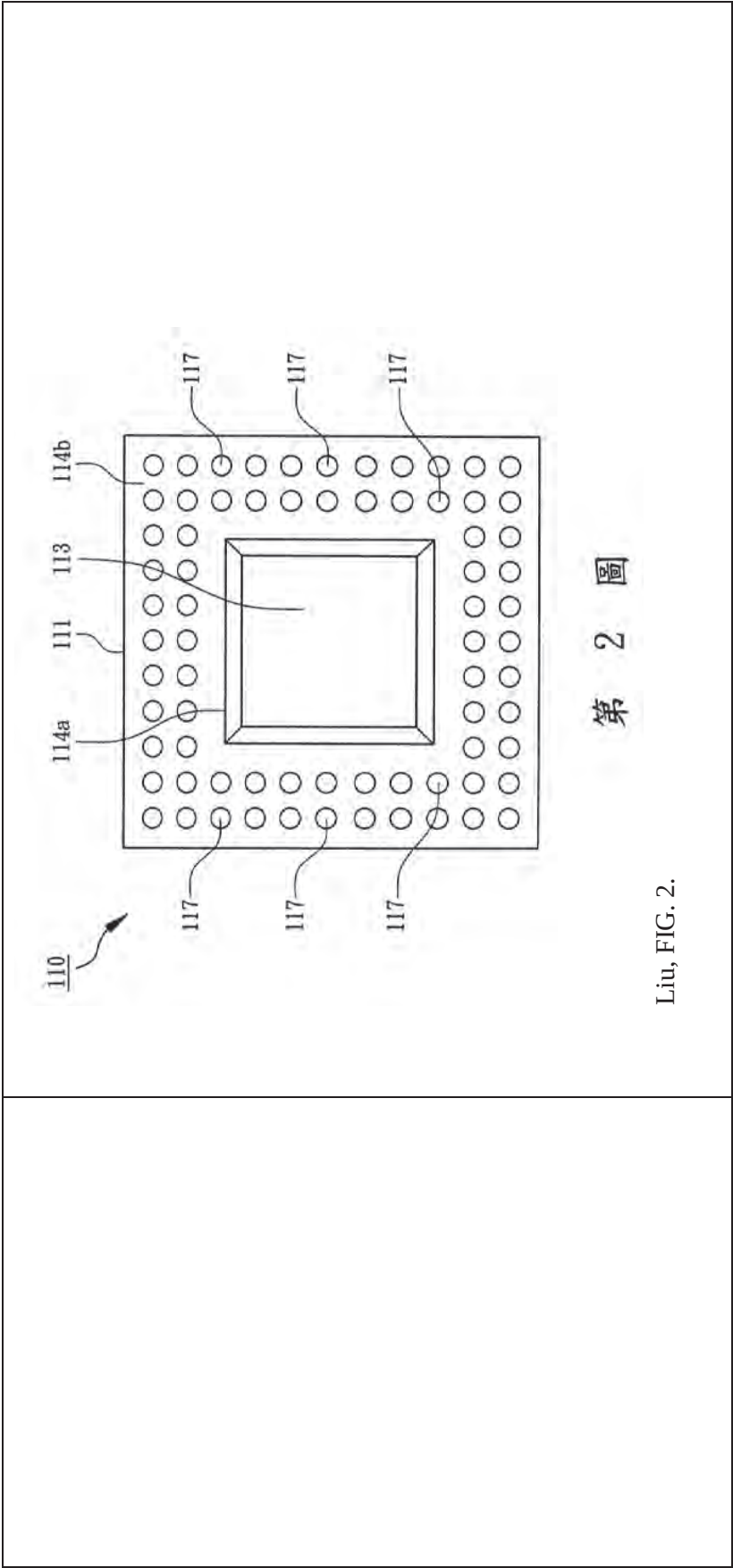
Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

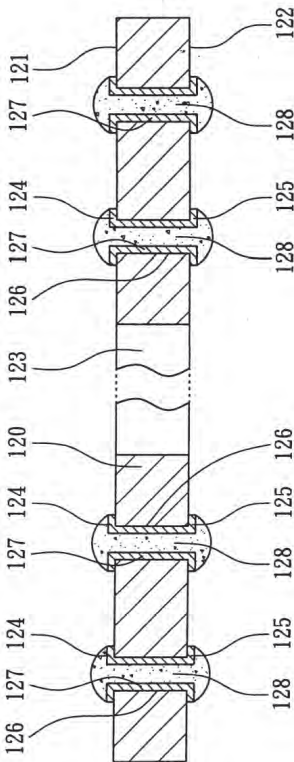
	<p>“The transfer plate 120 includes a plurality of upper connecting pads 124, a plurality of lower connecting pads 125, and a plurality of electrical vias 126. The upper connecting pads 124 are formed on the upper surface 121 of the transfer plate 120. The lower connecting pads 125 correspond to the upper connecting pads 124 and are formed on the lower surface 122 of the transfer plate 120.” Liu, [3].</p> <p>“In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123. The diameter of the electrical vias 126 is no less than 1.5 mm. Each electrical via 126 penetrates through the vertically corresponding upper connecting pad 124 and lower connecting pad 125 and has a metal layer 127 formed therein.” Liu, [3].</p> <p>“Claim 11. A transfer plate suitable for a stacked multi-package structure, having an upper surface and a lower surface, the transfer plate comprising: ● a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate;” Liu, [7].</p> <p>“Claim 15. A transfer plate suitable for a stacked multi-package structure, having a first surface and a second surface, the transfer plate comprising: •• an opening penetrating through the first surface and the second surface; a plurality of electrical vias penetrating through the first surface and the second surface and having a sidewall metal layer formed therein; and” Liu, [7].</p> <p>“Claim 14. The transfer plate as described in Claim 11, suitable for a stacked multi-package structure, wherein the transfer plate has an opening formed at the center of the transfer plate.” Liu, [7].</p>
--	---



第 1 圖

Liu, FIG. 1.



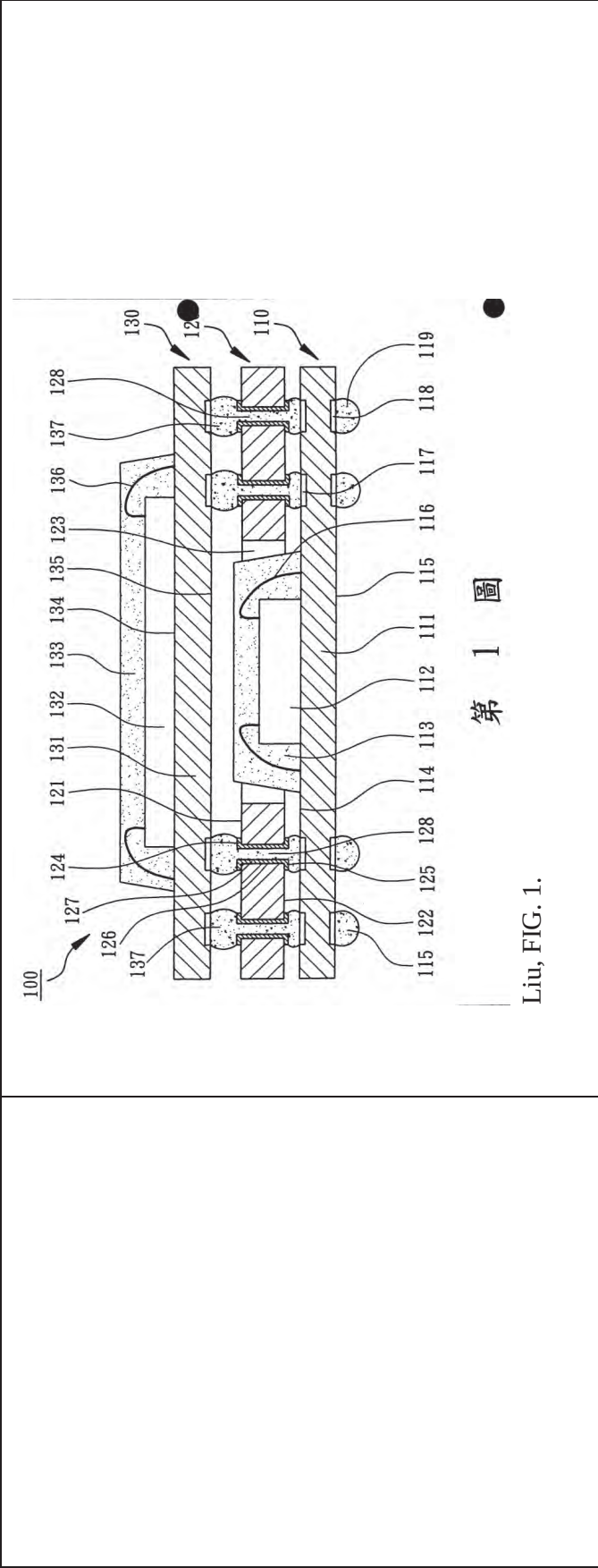
	 <p>The diagram shows a cross-section of a core substrate 120. It contains a plurality of metal pillars 124, each passing through the substrate. Electrical vias 126 are formed in the substrate, each having a metal layer 127 on its sidewall. The vias are arranged around the pillars. Labels 121, 122, 123, 124, 125, 126, 127, and 128 point to various components: 121 points to a top layer, 122 to a bottom layer, 123 to the substrate, 124 to a metal pillar, 125 to a metal layer on a pillar, 126 to an electrical via, 127 to the metal layer on the via sidewall, and 128 to the substrate.</p> <p style="text-align: center;">第 3 圖</p> <p style="text-align: center;">Liu, FIG. 3.</p> <p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Liu discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123. The diameter of the electrical vias 126 is no less than 1.5 mm. Each electrical via 126 penetrates through the vertically corresponding upper connecting pad 124 and lower connecting pad 125 and has a metal layer 127 formed therein. The metal layer 127 is formed on the sidewall of the corresponding electrical via 126 and connects the corresponding upper</p>

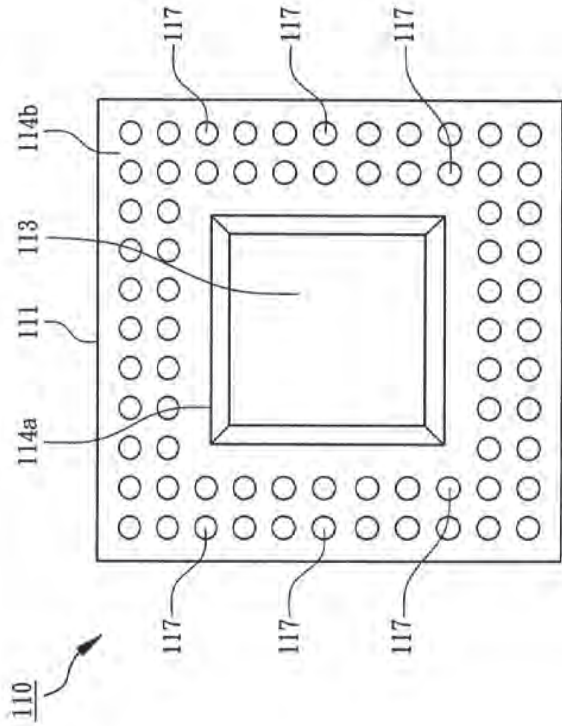
Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>connecting pads 124 and lower connecting pads 125, so that the corresponding upper connecting pads 124 and lower connecting pads 125 are electrically conductive.” Liu, [3].</p> <p>“The transfer plate 120 includes a plurality of upper connecting pads 124, a plurality of lower connecting pads 125, and a plurality of electrical vias 126. The upper connecting pads 124 are formed on the upper surface 121 of the transfer plate 120. The lower connecting pads 125 correspond to the upper connecting pads 124 and are formed on the lower surface 122 of the transfer plate 120.” Liu, [3].</p> <p>“Preferably, the metal layer 127 is integrally formed with the upper connecting pads 124 and the lower connecting pads 125. Alternatively, the metal layer 127 may directly extend to cover the peripheral edges of the electrical vias 126 at both the first surface 121 and the second surface 122, to facilitate the protruding formation of the solder materials 128.” Liu, [3-4].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and” Liu, [6].</p>
--	---

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

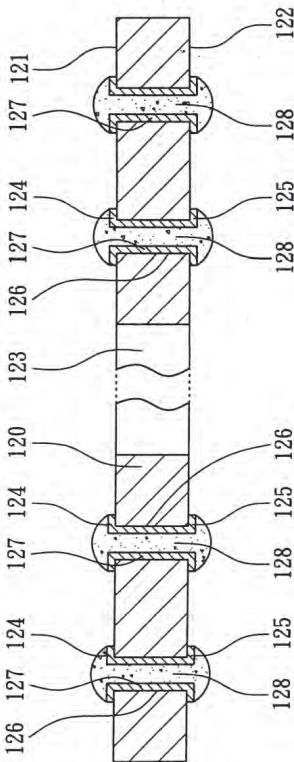
	<p>“Claim 11. A transfer plate suitable for a stacked multi-package structure, having an upper surface and a lower surface, the transfer plate comprising: • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; • • a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and” Liu, [7].</p> <p>“Claim 15. A transfer plate suitable for a stacked multi-package structure, having a first surface and a second surface, the transfer plate comprising: • • an opening penetrating through the first surface and the second surface; a plurality of electrical vias penetrating through the first surface and the second surface and having a sidewall metal layer formed therein; and” Liu, [7].</p>
--	--





第 2 圖

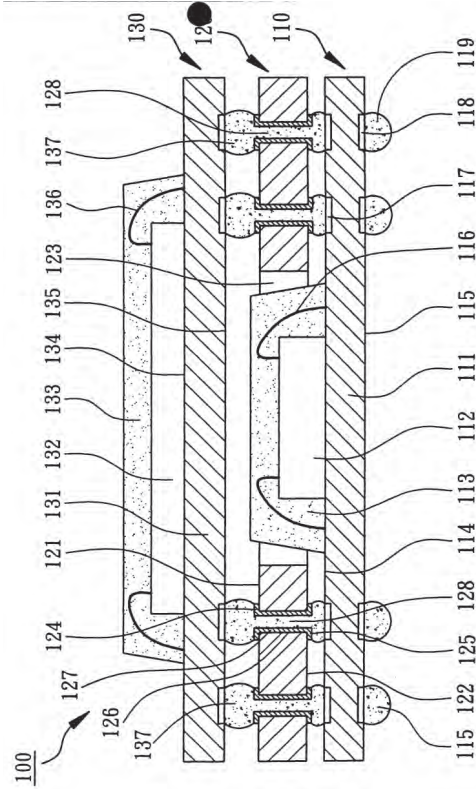
Liu, FIG. 2.

	 <p style="text-align: center;">第 3 圖</p> <p style="text-align: center;">Liu, FIG. 3.</p> <p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Liu discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“The upper connecting pads 124 are formed on the upper surface 121 of the transfer plate 120. The lower connecting pads 125 correspond to the upper connecting pads 124 and are formed on the lower surface 122 of the transfer plate 120. In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123. The diameter of the electrical vias 126 is no less than 1.5 mm. Each electrical via 126 penetrates through the vertically</p>

	<p>corresponding upper connecting pad 124 and lower connecting pad 125 and has a metal layer 127 formed therein. The metal layer 127 is formed on the sidewall of the corresponding electrical via 126 and connects the corresponding upper connecting pads 124 and lower connecting pads 125, so that the corresponding upper connecting pads 124 and lower connecting pads 125 are electrically conductive. Preferably, the metal layer 127 is integrally formed with the upper connecting pads 124 and the lower connecting pads 125. Alternatively, the metal layer 127 may directly extend to cover the peripheral edges of the electrical vias 126 at both the first surface 121 and the second surface 122, to facilitate the protruding formation of the solder materials 128. A plurality of solder materials 128 are formed within the electrical vias 126 and protrude from the upper connecting pads 124 and the lower connecting pads 125 of the transfer plate 120.” Liu, [3-4].</p> <p>“Claim 1. A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and” Liu, [6].</p> <p>“Claim 11. A transfer plate suitable for a stacked multi-package structure, having an upper surface and a lower surface, the transfer plate comprising: • a plurality of upper connecting</p>
--	--

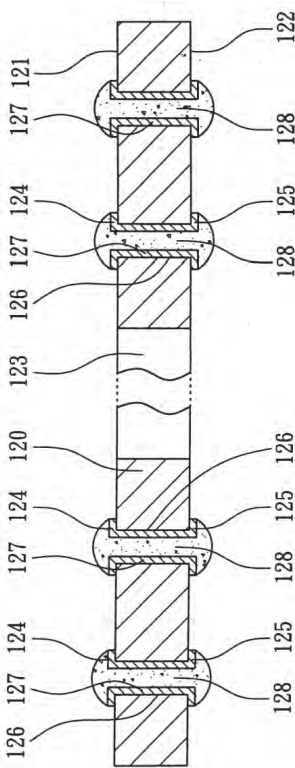
Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; • • a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate.” Liu, [7].</p> <p>“Claim 15. A transfer plate suitable for a stacked multi-package structure, having a first surface and a second surface, the transfer plate comprising: • • an opening penetrating through the first surface and the second surface; a plurality of electrical vias penetrating through the first surface and the second surface and having a sidewall metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the first surface and the second surface of the transfer plate.” Liu, [7].</p> <p>“Claim 16. The transfer plate as described in Claim 15, suitable for a stacked multi-package structure, wherein the sidewall metal layer extends to cover the peripheral edges of the corresponding electrical vias at both the first surface and the second surface, to facilitate the protruding formation of the solder materials.” Liu, [7].</p>
--	---



第 1 圖

Liu, FIG. 1.



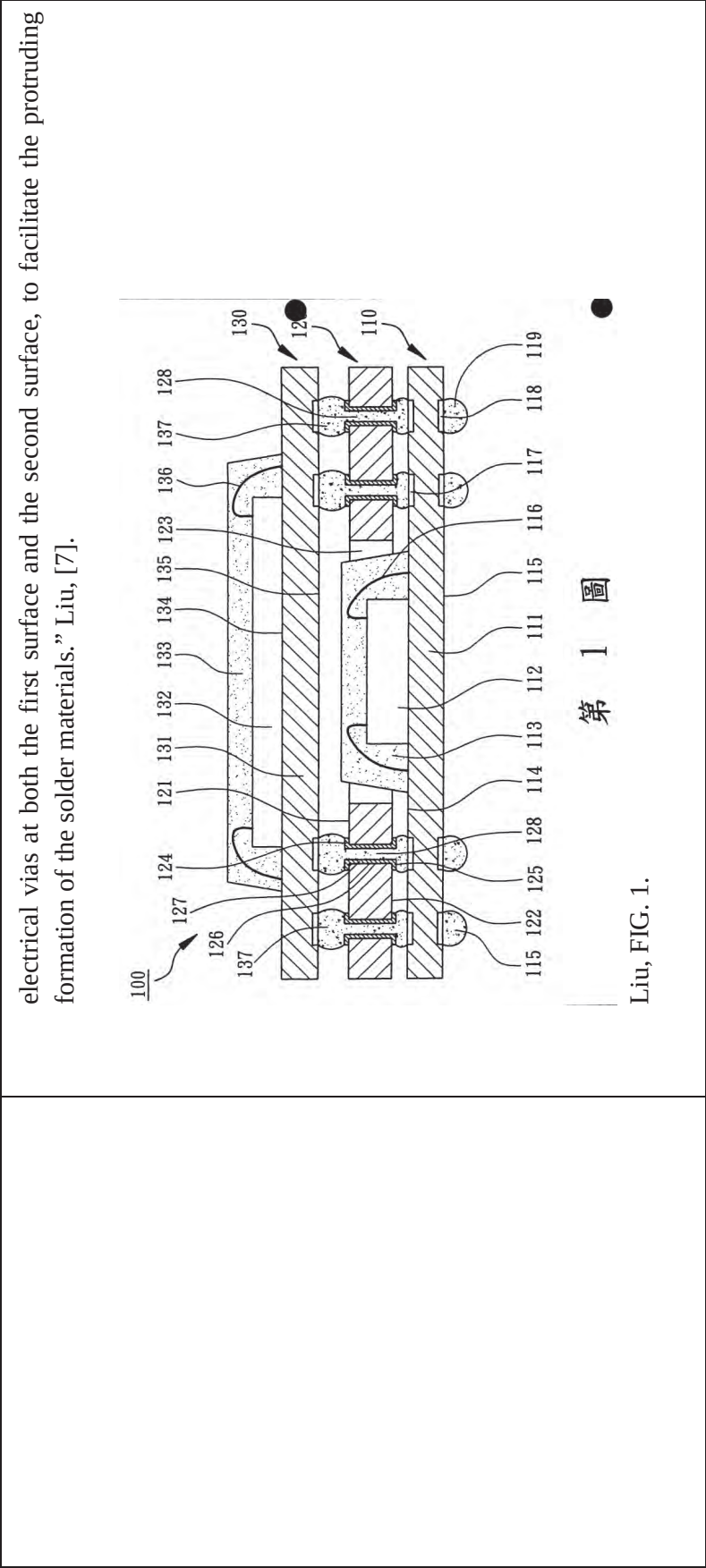
第 3 圖

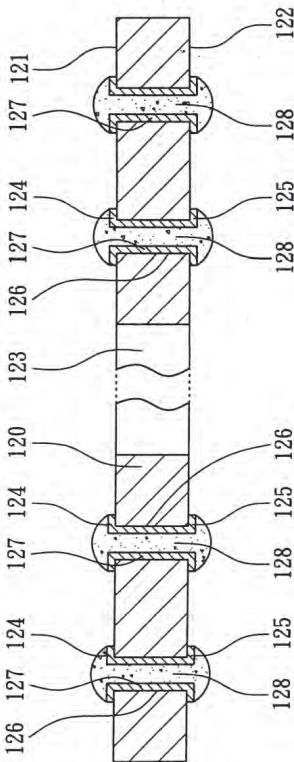
Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>Liu, FIG. 3.</p> <p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Liu discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“A plurality of solder materials 128 are formed within the electrical vias 126 and protrude from the upper connecting pads 124 and the lower connecting pads 125 of the transfer plate 120. Preferably, the height of the solder materials 128 protruding from the lower connecting pads 125 of the transfer plate 120 is no less than the height protruding from the upper connecting pads 124 of the transfer plate 120.” Liu, [4].</p> <p>“Furthermore, because the solder materials 128 are formed within the electrical vias 126 of the transfer plate 120 and protrude from the upper connecting pads 124 and the lower connecting pads 125, only a single reflow step is required to form the solder materials 128 into bump configurations for bonding with the bonding pads 117 of the first semiconductor package 110 and the external terminals 137 of the second semiconductor package 130.” Liu, [4].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the</p>

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and” Liu, [6].</p> <p>“The transfer plate includes a plurality of upper connecting pads, a plurality of lower connecting pads, and a plurality of electrical vias with a metal layer. The electrical vias connect the upper connecting pads and lower connecting pads. A plurality of solder materials are formed within the electrical vias and protrude from the upper and lower connecting pads of the transfer plate.” Liu, [6].</p> <p>“A transfer plate suitable for a stacked multi-package structure, having a first surface and a second surface, the transfer plate comprising: • • an opening penetrating through the first surface and the second surface; a plurality of electrical vias penetrating through the first surface and the second surface and having a sidewall metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the first surface and the second surface of the transfer plate.” Liu, [7].</p> <p>“The transfer plate as described in Claim 15, suitable for a stacked multi-package structure, wherein the sidewall metal layer extends to cover the peripheral edges of the corresponding</p>
--	---

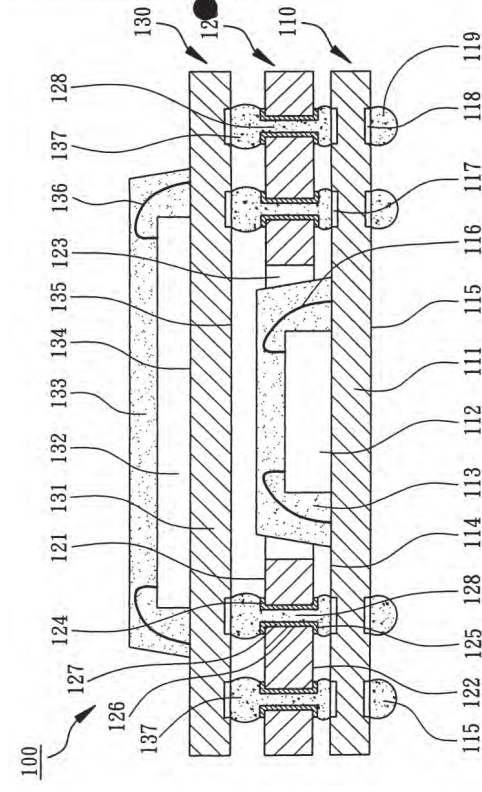


	 <p>The diagram shows a cross-section of a multi-layered substrate assembly. It consists of a top package substrate (121) with a bottom surface (122) having a plurality of metal pillars (123). These pillars are coupled to a corresponding metal pillar (124) in a bottom metal layer (125) of a spacer connector (126). The spacer connector also includes upper connecting pads (127) and lower connecting pads (128). The entire assembly is shown in a cross-sectional view with various layers and components labeled with reference numerals.</p> <p style="text-align: center;">第 3 圖</p> <p style="text-align: center;">Liu, FIG. 3.</p> <p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Liu discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“A secondary object of the present invention is to provide a transfer plate suitable for a stacked multi-package structure that includes a plurality of upper connecting pads, a plurality of lower connecting pads, and a plurality of electrical vias. A plurality of solder materials are</p>

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>formed within the electrical vias and protrude from the upper connecting pads and lower connecting pads of the transfer plate.” Liu, [2].</p> <p>“A plurality of external terminals 137 are formed on the bonding surface 135 of the substrate 131. The external terminals 137 are selected from solder balls and bumps. The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p> <p>“The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p> <p>“The solder materials connect the first semiconductor package and the second semiconductor package. IX.” Liu, [6].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads</p>
--	---

and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].



第 1 圖

Liu, FIG. 1.

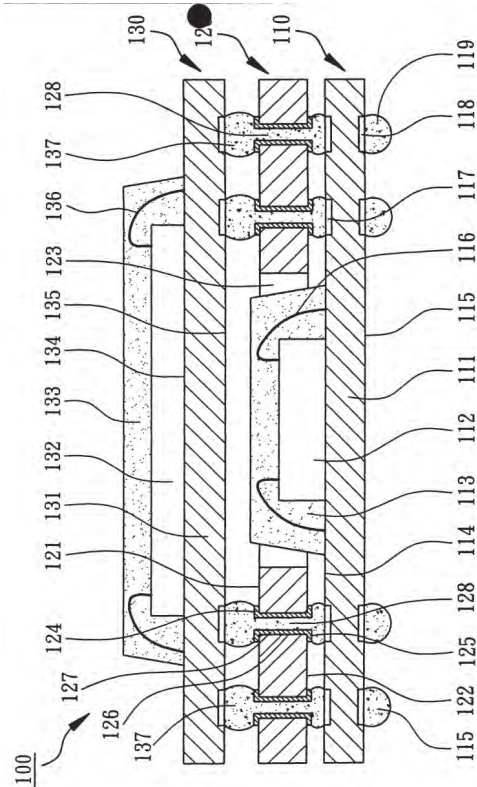
To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Liu discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring to Figures 1 and 2, the first surface 114 of the substrate 111 includes a packaging area 114a and a connecting area 114b. In this embodiment, the packaging area 114a is located at the center of the first surface 114 of the substrate. The chip 112 is disposed on the packaging area 114a and is electrically connected to the first surface 114 of the substrate 111 via a plurality of bonding wires 116. The encapsulant 113 is formed on the packaging area 114a to seal the chip 112 and the bonding wires 116. The connecting area 114b is located at the periphery of the first surface 114 of the substrate 111 and surrounds the packaging area 114a. A plurality of bonding pads 117 are formed in the connecting area 114b.” Liu, [3].</p> <p>“The substrate 111 has a first surface 114 and a second surface 115.” Liu, [3].</p> <p>“A plurality of solder materials 128 are formed within the electrical vias 126 and protrude from the upper connecting pads 124 and the lower connecting pads 125 of the transfer plate 120. Preferably, the height of the solder materials 128 protruding from the lower connecting pads 125 of the transfer plate 120 is no less than the height protruding from the upper connecting pads 124 of the transfer plate 120.” Liu, [4].</p> <p>“The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p>
---	---

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>“Therefore, the present invention uses the solder materials 128 of the transfer plate 120 to pass through the electrical vias 126 and bond the bonding pads 117 of the first semiconductor package 110 with the external terminals 137 of the second semiconductor package 130, thereby achieving the effect of multi-package stacking.” Liu, [4].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p>
--	--

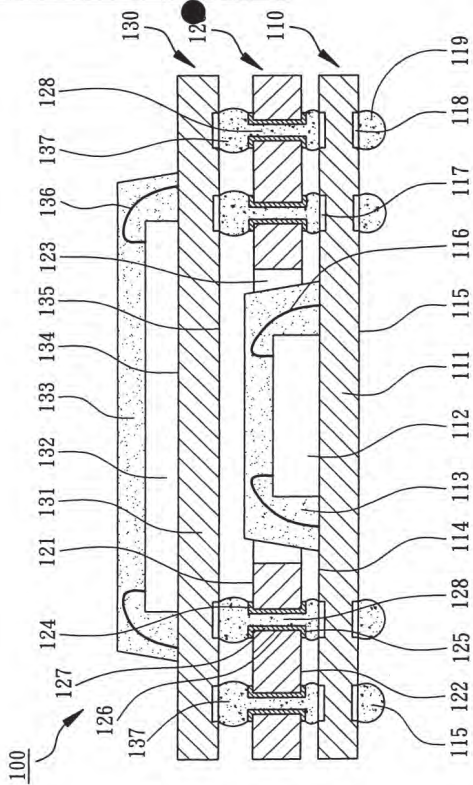
	<div><p>The diagram shows a cross-section of a multi-layered assembly. At the top is a layer labeled 100. Below it are several layers labeled 121, 131, 132, 133, 134, 135, 123, 136, 137, and 128. A central layer is labeled 130. Below this are layers 126, 127, 124, 125, 122, 115, 114, 113, 112, 111, 115, 116, 117, 118, and 119. A central vertical structure is labeled 110. A small circular feature is labeled 120. The bottom layer is labeled 115.</p></div> <div><p>第 1 圖</p></div> <div><p>Liu, FIG. 1.</p></div>	<p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p>	<p>Liu discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p>	

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

top metal pillars of the bottom package substrate; and	<p>“A secondary object of the present invention is to provide a transfer plate suitable for a stacked multi-package structure that includes a plurality of upper connecting pads, a plurality of lower connecting pads, and a plurality of electrical vias. A plurality of solder materials are formed within the electrical vias and protrude from the upper connecting pads and lower connecting pads of the transfer plate.” Liu, [2].</p> <p>“The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126. (5) Advantageous Effects Therefore, the present invention uses the solder materials 128 of the transfer plate 120 to pass through the electrical vias 126 and bond the bonding pads 117 of the first semiconductor package 110 with the external terminals 137 of the second semiconductor package 130, thereby achieving” Liu, [4].</p> <p>“Therefore, the present invention uses the solder materials 128 of the transfer plate 120 to pass through the electrical vias 126 and bond the bonding pads 117 of the first semiconductor package 110 with the external terminals 137 of the second semiconductor package 130, thereby achieving” Liu, [4].</p> <p>“The external terminals 137 are selected from solder balls and bumps. The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein;</p>
--	---

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and” Liu, [6].</p>
--	--

	<div><p>The diagram shows a cross-section of a multi-layered assembly. At the top, there is a layer labeled 100. Below it, a series of layers are labeled 121, 131, 132, 133, 134, 135, 123, 136, 137, and 128. A central vertical structure is labeled 126. To its right, another vertical structure is labeled 130. Below these, there are several horizontal layers labeled 115, 122, 125, 128, 114, 113, 112, 111, 115, 116, 117, 118, and 119. A central vertical structure is labeled 110. To its right, another vertical structure is labeled 120. The diagram is labeled '第 1 圖' (Figure 1) and 'Liu, FIG. 1.'</p></div>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Liu discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p>

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>“However, the conventional interposer substrate requires that solder balls first be planted on the upper and lower connecting pads of the interposer substrate. The upper connecting pads require a first reflow step to form a plurality of solder balls, and then solder paste is printed on the lower connecting pads, followed by a second reflow step to form solder on the lower connecting pads, in order to join the connecting substrate of the second semiconductor package to the base substrate of the first semiconductor package.” Liu, [2].</p> <p>“According to a specific embodiment of the present invention, referring to Figure 1, a stacked multi-package structure 100 comprises a first semiconductor package 110, a transfer plate (spacer) 120, and a second semiconductor package 130. The first semiconductor package 110 may be a ball grid array (BGA) package, which comprises a substrate 111, a chip 112, and an encapsulant 113. The substrate 111 has a first surface 114 and a second surface 115. Referring to Figures 1 and 2, the first surface 114 of the substrate 111 includes a packaging area 114a and a connecting area 114b. In this embodiment, the packaging area 114a is located at the center of the first surface 114 of the substrate. The chip 112 is disposed on the packaging area 114a and is electrically connected to the first surface 114 of the substrate 111 via a plurality of bonding wires 116. The encapsulant 113 is formed on the packaging area 114a to seal the chip 112 and the bonding wires 116. The connecting area 114b is located at the periphery of the first” Liu, [3].</p> <p>“Referring to Figures 1 and 3, the transfer plate 120 has an upper surface 121, a lower surface 122, and an opening 123. The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110.” Liu, [3].</p> <p>“The second semiconductor package 130 may be a ball grid array package, for example a Plastic Ball Grid Array package (PBGA) or a chip-scale package. In this embodiment, a plastic ball grid array package is used. The second semiconductor package 130 comprises a</p>
--	--

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>substrate 131, a chip 132, and an encapsulant 133. The substrate 131 has a carrier surface 134 and a bonding surface 135. The chip 132 is disposed on the carrier surface 134 and is electrically connected to the carrier surface 134 of the substrate 131 via a plurality of bonding wires 136.” Liu, [4].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising.” Liu, [6].</p> <p>“Claim 14. The transfer plate as described in Claim 11, suitable for a stacked multi-package structure, wherein the transfer plate has an opening formed at the center of the transfer plate.” Liu, [7].</p>
--	--

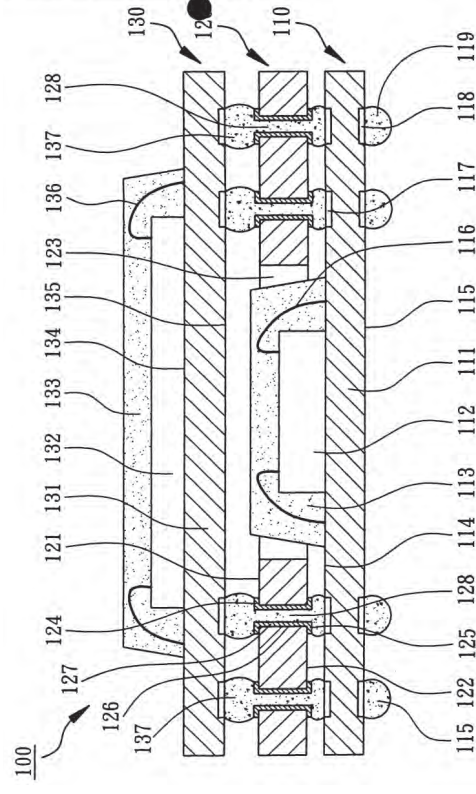


圖 1 第

Liu, FIG. 1.

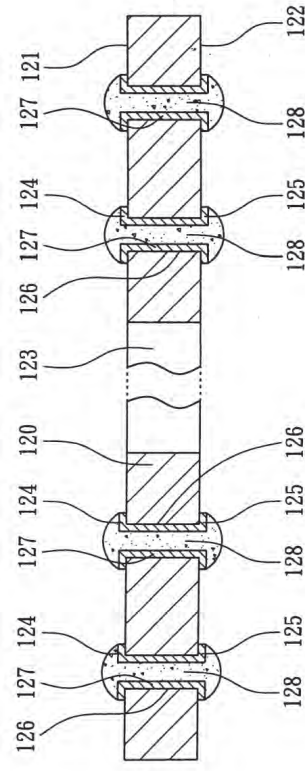


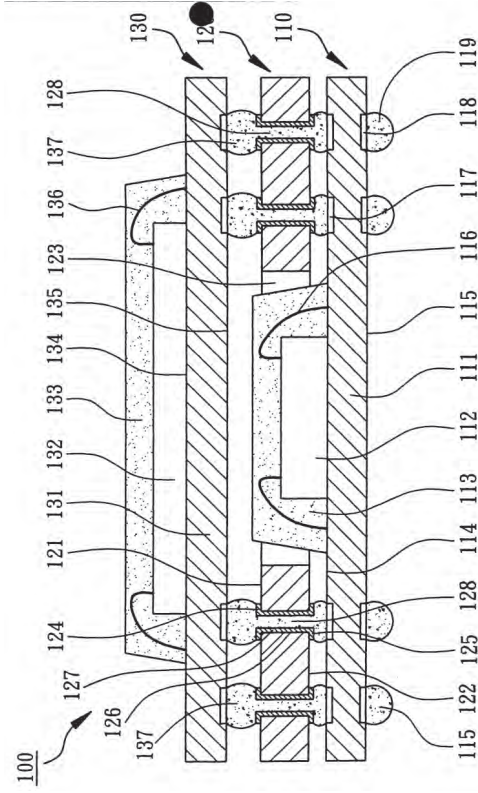
圖
3
第

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>Liu, FIG. 3.</p> <p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Liu discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The chip 112 is disposed on the packaging area 114a and is electrically connected to the first surface 114 of the substrate 111 via a plurality of bonding wires 116.” Liu, [3].</p> <p>“The first semiconductor package 110 may be a ball grid array (BGA) package, which comprises a substrate 111, a chip 112, and an encapsulant 113. The substrate 111 has a first surface 114 and a second surface 115.” Liu, [3].</p> <p>“Referring to Figures 1 and 2, the first surface 114 of the substrate 111 includes a packaging area 114a and a connecting area 114b. In this embodiment, the packaging area 114a is located at the center of the first surface 114 of the substrate. The chip 112 is disposed on the packaging area” Liu, [3].</p> <p>“The encapsulant 113 is formed on the packaging area 114a to seal the chip 112 and the bonding wires 116.” Liu, [3].</p>

“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein,” Liu, [6].

“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of” Liu, [6].

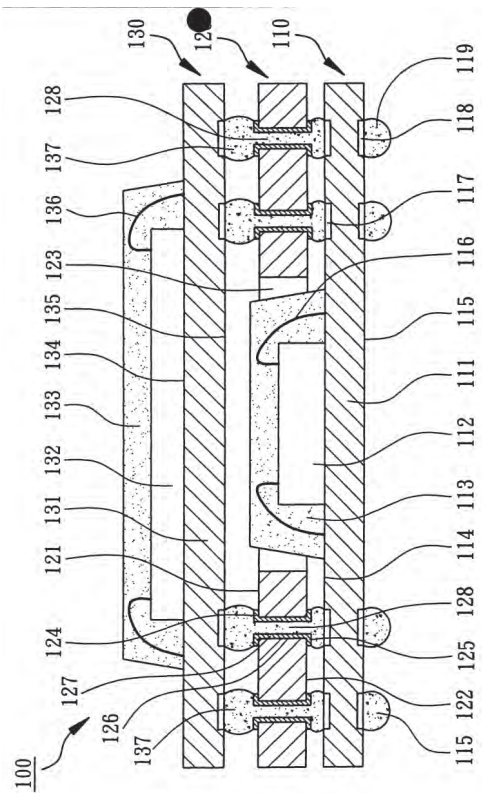


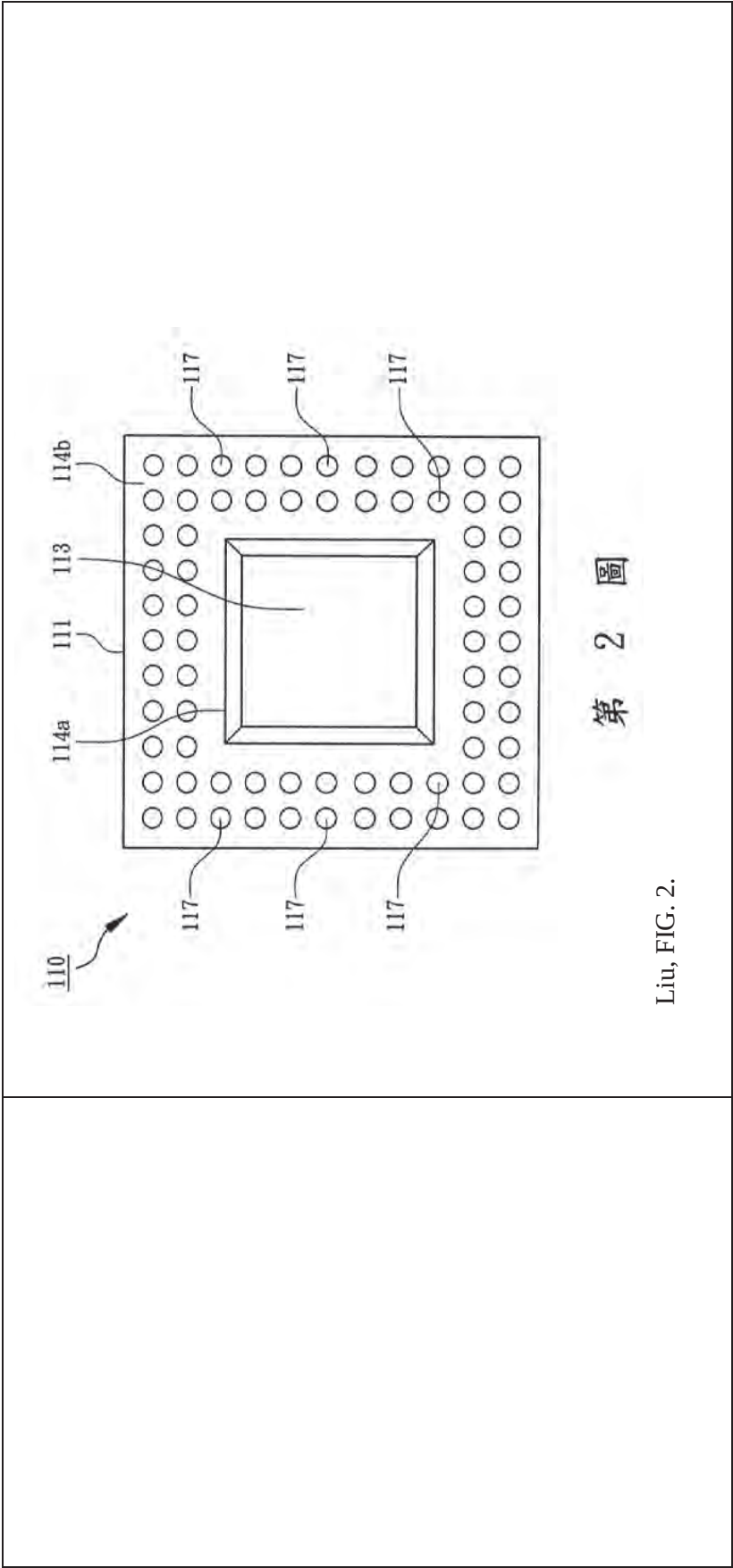
第 1 圖

Liu, FIG. 1.

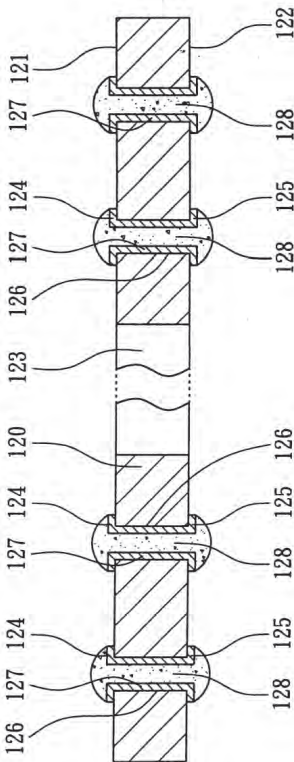
Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Liu discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123.” Liu, [3].</p> <p>“The connecting area 114b is located at the periphery of the first surface 114 of the substrate 111 and surrounds the packaging area 114a.” Liu, [3].</p> <p>“The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110.” Liu, [3].</p> <p>“Claim 8. The stacked multi-package structure as described in Claim 7, wherein the connecting area is at the periphery of the first surface of the substrate.” Liu, [7].</p> <p>“Claim 17. The transfer plate as described in Claim 15, suitable for a stacked multi-package structure, wherein the electrical vias are arranged around the periphery of the opening.” Liu, [7].</p>

	<p>“Claim 14. The transfer plate as described in Claim 11, suitable for a stacked multi-package structure, wherein the transfer plate has an opening formed at the center of the transfer plate.” Liu, [7].</p>  <p>第 1 圖</p> <p>Liu, FIG. 1.</p>
--	---



Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

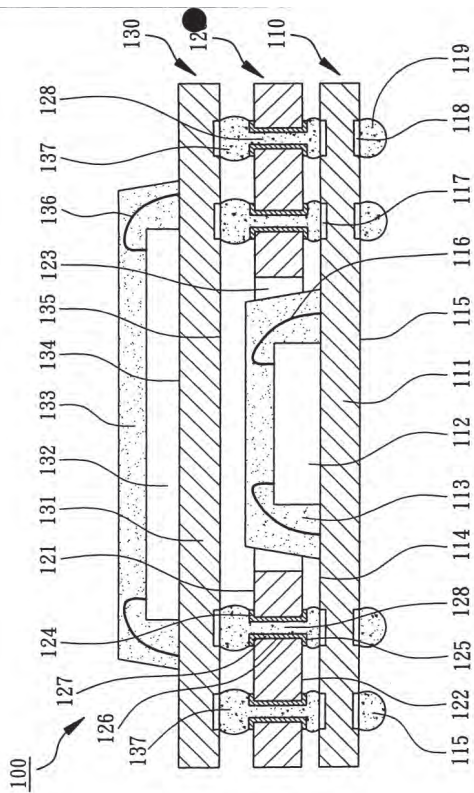
	<div><p style="text-align: center;">第 3 圖</p><p style="text-align: center;">Liu, FIG. 3.</p><p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Liu discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p>See, <i>e.g.</i>:</p>

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>“The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110.” Liu, [3].</p> <p>“Referring to Figures 1 and 3, the transfer plate 120 has an upper surface 121, a lower surface 122, and an opening 123. The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110.” Liu, [3].</p> <p>“In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123.” Liu, [3].</p> <p>“In this embodiment, the packaging area 114a is located at the center of the first surface 114 of the substrate. The chip 112 is disposed on the packaging area 114a and is electrically connected to the first surface 114 of the substrate 111 via a plurality of bonding wires 116. The encapsulant 113 is formed on the packaging area 114a to seal the chip” Liu, [3].</p> <p>“The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p> <p>“Claim 14. The transfer plate as described in Claim 11, suitable for a stacked multi-package structure, wherein the transfer plate has an opening formed at the center of the transfer plate.” Liu, [7].</p>
--	--

	<div><p>The diagram shows a cross-section of a device assembly 100. It consists of multiple layers: a top layer 120, a middle layer 110, and a bottom layer 130. Various components are labeled with reference numerals: 100 (the entire assembly), 120 (top layer), 110 (middle layer), 130 (bottom layer), 121, 122, 123, 124, 125, 126, 127, 128, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200.</p></div> <div><p>第 1 圖</p></div> <div><p>Liu, FIG. 1.</p></div> <div><p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

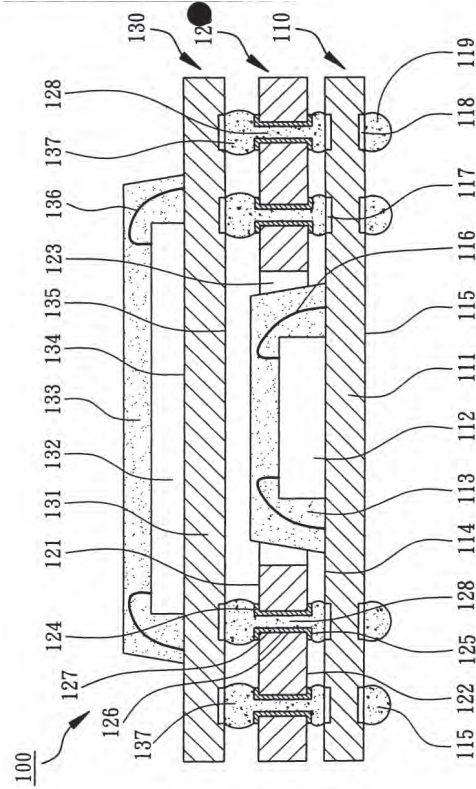
Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Liu discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Referring to Figures 1 and 2, the first surface 114 of the substrate 111 includes a packaging area 114a and a connecting area 114b. In this embodiment, the packaging area 114a is located at the center of the first surface 114 of the substrate. The chip 112 is disposed on the packaging area 114a and is electrically connected to the first surface 114 of the substrate 111 via a plurality of bonding wires 116.” Liu, [3].</p> <p>“Referring to Figures 1 and 3, the transfer plate 120 has an upper surface 121, a lower surface 122, and an opening 123. The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110.” Liu, [3].</p> <p>“In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123.” Liu, [3].</p> <p>“The second semiconductor package 130 comprises a substrate 131, a chip 132, and an encapsulant 133. The substrate 131 has a carrier surface 134 and a bonding surface 135. The chip 132 is disposed on the carrier surface 134 and is electrically connected to the carrier surface 134 of the substrate 131 via a plurality of bonding wires 136.” Liu, [4].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the</p>
---	--

	<p>first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p> <p>“A stacked multi-package structure comprising a first semiconductor package, a transfer plate (spacer), and a second semiconductor package. The transfer plate includes a plurality of upper connecting pads, a plurality of lower connecting pads, and a plurality of electrical vias with a metal layer. The electrical vias connect the upper connecting pads and lower connecting pads. A plurality of solder materials are formed within the electrical vias and protrude from the upper and lower connecting pads of the transfer plate. The solder materials connect the first semiconductor package and the second semiconductor package.” Liu, [6].</p>
--	--



第 1 圖

Liu, FIG. 1.

To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 4, U.S. Patent No. 9859202

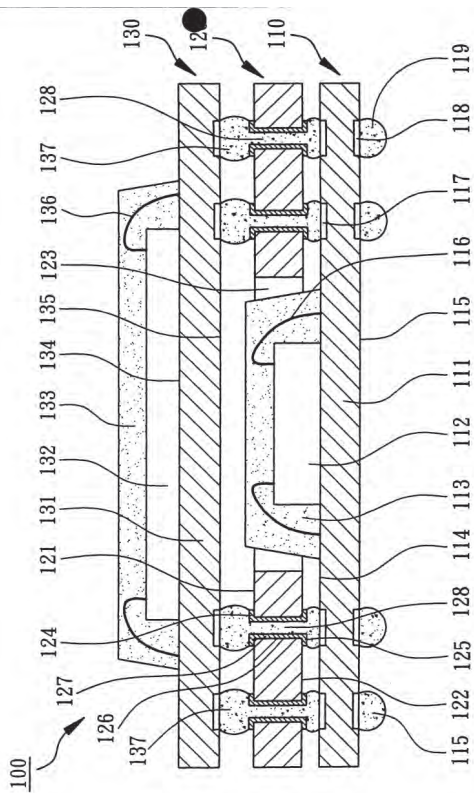
Claim Limitation	Disclosure
------------------	------------

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Liu discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110. The transfer plate 120 includes a plurality of upper connecting pads 124, a plurality of lower connecting pads 125, and a plurality of electrical vias 126. The upper connecting pads 124 are formed on the upper surface 121 of the transfer plate 120. The lower connecting pads 125 correspond to the upper connecting pads 124 and are formed on the lower surface 122 of the transfer plate 120. In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123. The diameter of the electrical vias 126 is no less than 1.5 mm. Each electrical via 126 penetrates through the vertically corresponding upper connecting pad 124 and lower connecting pad 125 and has a metal layer 127 formed therein. The metal layer 127 is formed on the sidewall of the” Liu, [3].</p> <p>“Preferably, the metal layer 127 is integrally formed with the upper connecting pads 124 and the lower connecting pads 125. Alternatively, the metal layer 127 may directly extend to cover the peripheral edges of the electrical vias 126 at both the first surface 121 and the second surface 122, to facilitate the protruding formation of the solder materials 128.” Liu, [3-4].</p>
--	---

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>“The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p> <p>“A plurality of solder materials 128 are formed within the electrical vias 126 and protrude from the upper connecting pads 124 and the lower connecting pads 125 of the transfer plate 120. Preferably, the height of the solder materials 128 protruding from the lower connecting pads 125 of the transfer plate 120 is no less than the height protruding from the upper connecting pads 124 of the transfer plate 120.” Liu, [4].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p>
--	--

	<div><p>The diagram shows a cross-section of a device assembly 100. It consists of multiple layers: a top layer 120, a middle layer 110, and a bottom layer 130. Various components are labeled with reference numerals: 100 (the entire assembly), 120 (top layer), 110 (middle layer), 130 (bottom layer), 121, 122, 123, 124, 125, 126, 127, 128, 129, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200.</p></div> <div><p>第 1 圖</p></div> <div><p>Liu, FIG. 1.</p></div> <div><p>To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Liu discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“A plurality of solder materials 128 are formed within the electrical vias 126 and protrude from the upper connecting pads 124 and the lower connecting pads 125 of the transfer plate 120. Preferably, the height of the solder materials 128 protruding from the lower connecting pads 125 of the transfer plate 120 is no less than the height protruding from the upper connecting pads 124 of the transfer plate 120.” Liu, [4].</p> <p>“Therefore, the present invention uses the solder materials 128 of the transfer plate 120 to pass through the electrical vias 126 and bond the bonding pads 117 of the first semiconductor package 110 with the external terminals 137 of the second semiconductor package 130, thereby achieving the effect of multi-package stacking.” Liu, [4].</p> <p>“The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p> <p>“Furthermore, because the solder materials 128 are formed within the electrical vias 126 of the transfer plate 120 and protrude from the upper connecting pads 124 and the lower connecting pads 125, only a single reflow step is required to form the solder materials 128</p>
--	---

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>into bump configurations for bonding with the bonding pads 117 of the first semiconductor package 110 and the external terminals 137 of the second semiconductor package 130.” Liu, [4].</p> <p>“A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p>
--	--

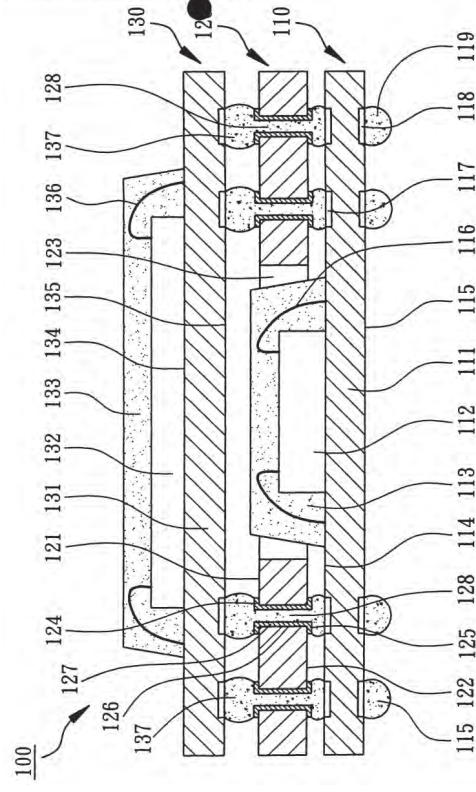


圖 1 第

Liu, FIG. 1.

To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Liu discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Referring to Figures 1 and 3, the transfer plate 120 has an upper surface 121, a lower surface 122, and an opening 123. The opening 123 is formed at the center of the transfer plate 120 to correspond to the chip 112 of the first semiconductor package 110. The transfer plate 120 includes a plurality of upper connecting pads 124, a plurality of lower connecting pads 125, and a plurality of electrical vias 126. The upper connecting pads 124 are formed on the upper surface 121 of the transfer plate 120. The lower connecting pads 125 correspond to the upper connecting pads 124 and are formed on the lower surface 122 of the transfer plate 120. In this embodiment, the electrical vias 126 are arranged around the periphery of the opening 123. The diameter of the electrical vias 126 is no less than 1.5 mm. Each electrical via 126 penetrates through the vertically corresponding upper connecting pad 124 and lower connecting pad 125 and has a metal layer 127 formed therein. The metal layer 127 is formed on the sidewall of the corresponding electrical via 126 and connects the corresponding upper connecting pads 124 and lower connecting pads 125, so that the corresponding upper</p>

Appendix A-23 - Invalidity of U.S. Patent No. 9859202 in view of Liu - Non-Patent Publication

	<p>connecting pads 124 and lower connecting pads 125 are electrically conductive. Preferably, the metal layer 127 is integrally formed with the upper connecting pads 124 and the lower connecting pads 125. Alternatively, the metal layer 127 may directly extend to cover the peripheral edges of the electrical vias 126 at both the first surface 121 and the second surface 122, to facilitate the protruding formation of the solder materials 128. A plurality of solder materials 128 are formed within the electrical vias 126 and protrude from the upper connecting pads 124 and the lower connecting pads 125 of the transfer plate 120.” Liu, [3-4].</p> <p>“The second semiconductor package 130 may be a ball grid array package, for example a Plastic Ball Grid Array package (PBGA) or a chip-scale package. In this embodiment, a plastic ball grid array package is used. The second semiconductor package 130 comprises a substrate 131, a chip 132, and an encapsulant 133. The substrate 131 has a carrier surface 134 and a bonding surface 135. The chip 132 is disposed on the carrier surface 134 and is electrically connected to the carrier surface 134 of the substrate 131 via a plurality of bonding wires 136. The encapsulant 133 is formed on the carrier surface 134 to seal the chip 132 and the bonding wires 136. A plurality of external terminals 137 are formed on the bonding surface 135 of the substrate 131. The external terminals 137 are selected from solder balls and bumps. The external terminals 137 are electrically bonded to the bonding pads 117 of the first semiconductor package 110 through the solder materials 128 passing through the electrical vias 126.” Liu, [4].</p> <p>“Therefore, the present invention uses the solder materials 128 of the transfer plate 120 to pass through the electrical vias 126 and bond the bonding pads 117 of the first semiconductor package 110 with the external terminals 137 of the second semiconductor package 130, thereby achieving the effect of multi-package stacking.” Liu, [4].</p>
--	--

	<p>“Preferably, the height of the solder materials 128 protruding from the lower connecting pads 125 of the transfer plate 120 is no less than the height protruding from the upper connecting pads 124 of the transfer plate 120.” Liu, [4].</p> <p>“Claim 1. A stacked multi-package structure, comprising: a first semiconductor package, comprising at least a substrate and a chip, the substrate having a first surface and a second surface, the first surface including a packaging area and a connecting the chip being disposed in the packaging area, and the connecting area having a plurality of bonding pads formed therein; area, a transfer plate (spacer) having an upper surface, a lower surface, and an opening, the opening corresponding to the chip of the first semiconductor package, the transfer plate comprising: • • • a plurality of upper connecting pads formed on the upper surface of the transfer plate; a plurality of lower connecting pads formed on the lower surface of the transfer plate; a plurality of electrical vias penetrating through the upper connecting pads and the lower connecting pads and having a metal layer formed therein; and a plurality of solder materials formed within the electrical vias and protruding from the upper connecting pads and the lower connecting pads of the transfer plate; and a second semiconductor package having a plurality of external terminals; wherein the solder materials of the transfer plate bond the bonding pads of the first semiconductor package and the external terminals of the second semiconductor package.” Liu, [6].</p> <p>“Claim 16. The transfer plate as described in Claim 15, suitable for a stacked multi-package structure, wherein the sidewall metal layer extends to cover the peripheral edges of the corresponding electrical vias at both the first surface and the second surface, to facilitate the protruding formation of the solder materials.” Liu, [7].</p>
--	---

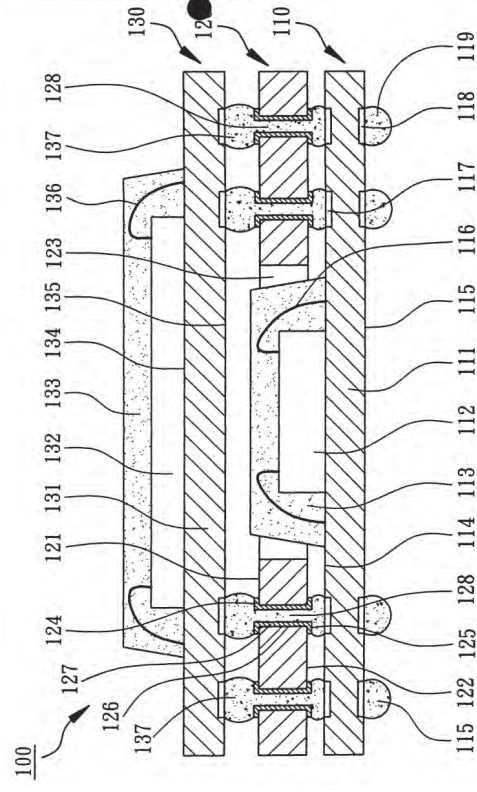


圖 1 第

Liu, FIG. 1.

To the extent Plaintiff contends that Liu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

U.S. Patent Publication No. 5334804 (“Love”) is titled Wire Interconnect Structures for Connecting an Integrated Circuit to a Substrate and lists David G. Love, Larry L. Moresco, William T. Chou, David A. Horine, Connie M. Wong, and Solomon I. Beilin as inventors. Love is assigned to Fujitsu Limited. Love anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Love is a U.S. patent that was filed November 17, 1992. Love is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Love, or otherwise rendered obvious by disclosures and teachings of Love, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Love does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Love with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Love, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Love “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

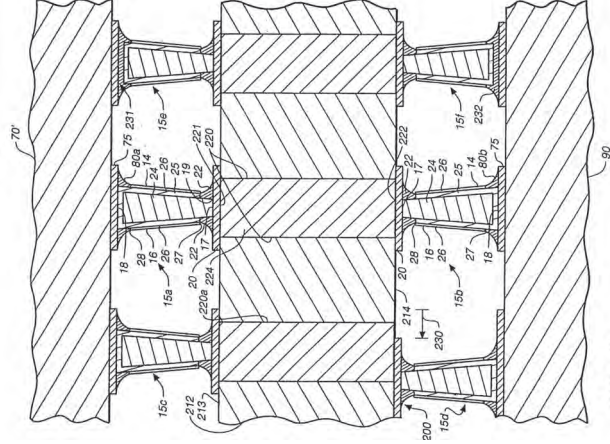
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Love or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Love set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Love discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“The present invention recognizes that these problems experienced in the prior art may be addressed by an interconnect structure having a substrate with a plurality of electrically conductive posts mechanically mounted vertically to the surface of the supporting substrate. The present invention further recognizes that the effects of thermal mechanical stress may be reduced by having a large aspect ratio for each post and by having means disposed at one or both ends of each post for de-concentrating the mechanical stress and strain developed along the body of the post. The present invention further recognizes that the substrate may be the</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>supporting substrate or may be an intermediate substrate which is interposed between the IC chip and a major supporting substrate. In the latter case, electrically conductive posts are disposed on both surfaces of the intermediate interposer substrate. Additionally, the present invention recognizes that such a structure is more reliable than the C4 and UNIAX processes and has the potential of being mass produced at costs lower than those associated with the BIP process.” Love, [4:50-5:3].</p> <p>“FIG. 5 is a cross-sectional view of a second embodiment of the wire interconnect structure according to the present invention, which has been given the general reference designation of 200. The embodiment is referred to as wire interconnect structure 200 and is for electrically coupling a major substrate 90 to integrated circuit chip 70', as shown in FIG. 5. Wire interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70'. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70', and having a first surface 213 and a second surface 214. Interconnect substrate 212 is also referred to as an interposer substrate or an intermediate substrate because it is disposed between substrate 90 and chip 70'. Wire interconnect structure 200 further comprises a first interconnect column 15a on surface 213 constructed according to the first embodiment of the present invention shown in FIGS. 1-3, and a second interconnect column 15b on surface 214, also constructed according to the first embodiment of the present invention.” Love, [12:4-12:25].</p>
--	--



Love, FIG. 5

Love discloses, either expressly or inherently, a bottom package substrate.

See, e.g.:

“FIG. 5 is a cross-sectional view of a second embodiment of the wire interconnect structure according to the present invention, which has been given the general reference designation of 200. The embodiment is referred to as wire interconnect structure 200 and is for electrically coupling a major substrate 90 to integrated circuit chip 70', as shown in FIG. 5. Wire

interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70'. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70', and having a first surface 213 and a second surface 214." Love, [12:4-12:16].

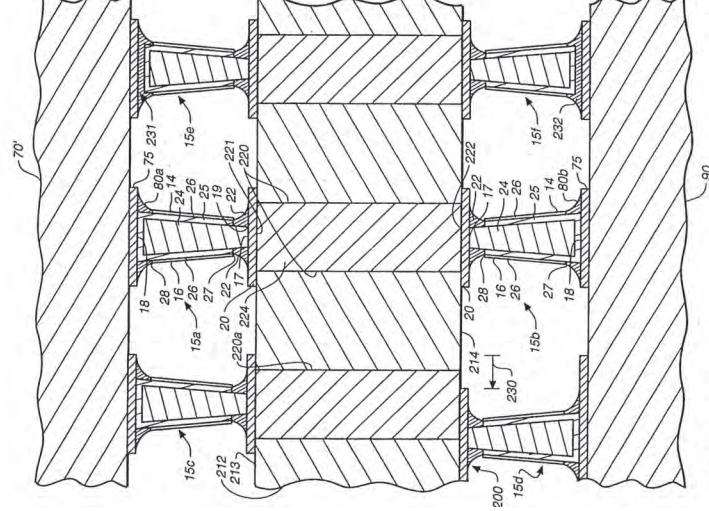


FIG. 5

Love, FIG. 5

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

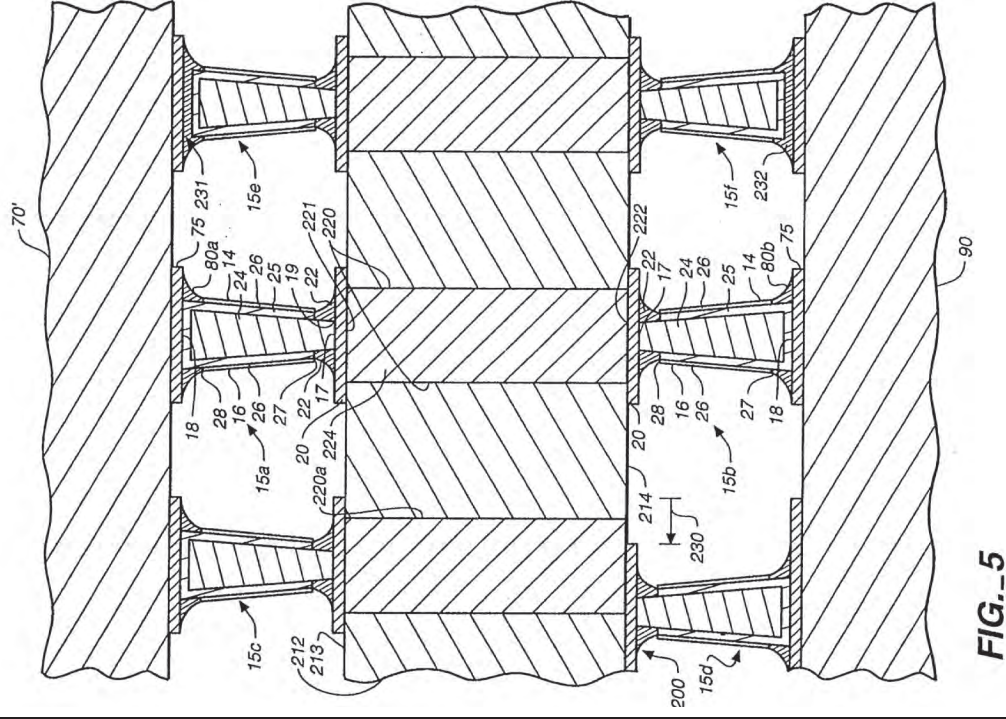
	<p>“First interconnect column 15a is disposed on first surface 213 of substrate 212 such that its bottom end 17 and base pad 20 are mounted to surface 213. First interconnect column 15a is for making contact to IC chip 70'. In a similar manner, second interconnect column 15b is disposed on second surface 214 of substrate 212, such that its bottom end 17 and base pad 20 are mounted to second surface 214. Second interconnect column 15b is for making contact to major substrate 90.” Love, [12:34-12:41].</p> <p>“As indicated above, not all of the interconnect columns 15a and 15b may have the same height, and integrated circuit chip 70' may be warped. Substrate 212 and major substrate 90 may each also be warped, usually each on the order of 2 microns or less, measured from low point to high point. As such, there may be one or more interconnect columns in an array of such columns which does not fully contact either integrated circuit chip 70' or major substrate 90. Such a case in which contact is not made to either of chip 70' and substrate 90 is shown by two interconnect columns 15e and 15f in FIG. 5, as an example. Two gaps 231 and 232 are shown between interconnect column 15e and IC chip 70' and between interconnect column 15f and major substrate 90, respectively. However, as described above with reference to interconnect structure 10, the initial 5 micron height of bump 80 is generally sufficiently high to make electrical contact to an interconnect column which does not physically make contact to its corresponding substrate or IC chip.” Love, [13:41-13:60].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Love discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p><i>See, e.g.:</i></p> <p>“As a practical matter, integrated circuit chip 70' may have a surface which is warped, with a typical maximum deviation of approximately 2 microns from low point to high point. As such, not every interconnect column 15 will make contact to the surface of integrated circuit chip 70'. However, generally at least three of the interconnect structures will contact the surface of integrated circuit chip 70'. Given that the maximum warpage of the surface of chip 70' is approximately 2 microns and that the variation in height of interconnect columns 15 is approximately 2 microns, there is a possibility that one or more of the interconnect columns 15 may be spaced approximately 4 microns away from the surface of chip 70' after the contacting process is completed. However, bump 80 is typically at least 5 microns high and is able to contact its corresponding interconnect structure 10 and form a bond thereto should such a gap exist between the interconnect column and chip 70'. As bump 80 is made from a conductive material, an electrical signal is able to be transmitted between interconnect structure 10 and chip 70' even if interconnect column 15 does not physically touch the surface of chip 70' (e.g., pad 75). It may be appreciated that bumps of solder material can be formed up to a height of 75 microns so that contact can be made if the spacing between chip 70' and an interconnect structure 10 is greater than 5 microns.” Love, [11:4-11:30].</p> <p>“In the embodiments of the present invention in which bumps 80 comprise a metal, such as indium, bismuth, gallium, tin, lead, or their alloys, the surface tension of bump 80, when molten, aids in bringing the array of bumps 80 into alignment with array 100. Under reflow conditions, each of the metal bumps 80 seeks a minimum surface area around the corresponding interconnect column 15 of the wire interconnect array 100 as it flows around the structure, the minimum surface area being achieved when the bump is symmetrically disposed around the top end of its corresponding column 15. The surface tension of each</p>
--	--

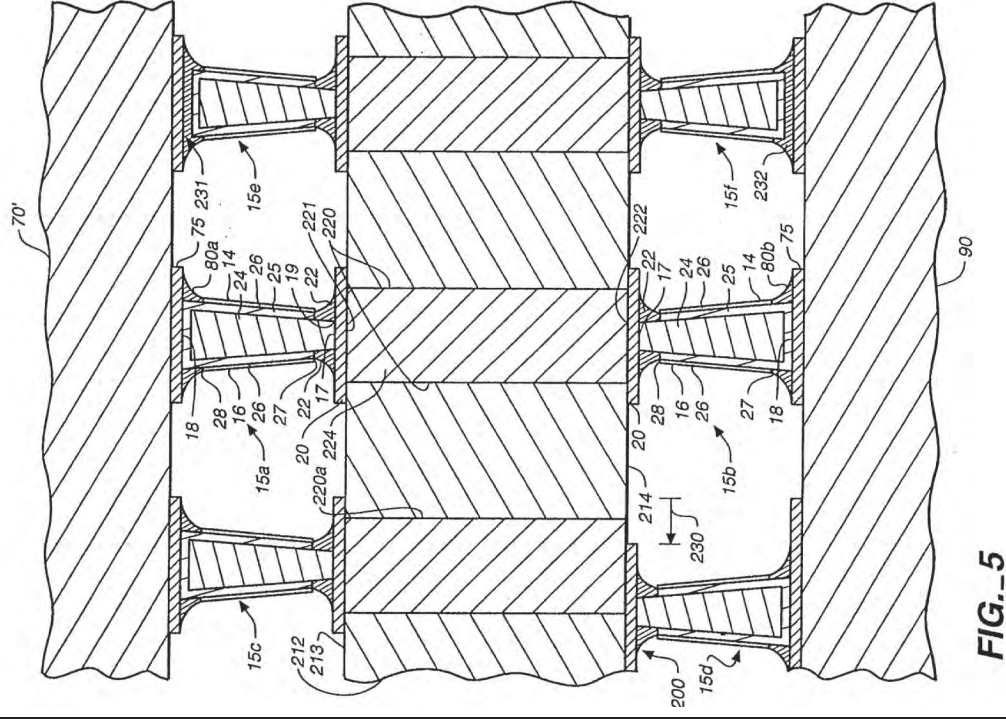
Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>bump surface applies a force between its respective IC chip pad and its corresponding interconnect column 15 in a direction which causes the bump to be symmetrically positioned around its corresponding interconnect column. As such, any misalignment that may occur in positioning IC chip 70' over array 100 before the heat-bonding process will be corrected, or minimized, by the surface tension forces as long as there is an initial contact of a few bumps with their corresponding interconnect structures. Depending upon the material of bump 80 and the size and geometry of the interconnect structure, the surface tension forces can be significant, and may be quite large in comparison to the gravitational force applied to chip 70' during the heat-bonding process.” Love, [11:32-11:56].</p> <p>“FIG. 5 is a cross-sectional view of a second embodiment of the wire interconnect structure according to the present invention, which has been given the general reference designation of 200. The embodiment is referred to as wire interconnect structure 200 and is for electrically coupling a major substrate 90 to integrated circuit chip 70', as shown in FIG. 5. Wire interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70'. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70', and having a first surface 213 and a second surface 214.” Love, [12:4-12:16].</p>
--	--



Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>Love, FIG. 5</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Love discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70’, and having a first surface 213 and a second surface 214. Interconnect substrate 212 is also referred to as an interposer substrate or an intermediate substrate because it is disposed between substrate 90 and chip 70’. Wire interconnect structure 200 further comprises a first interconnect column 15a on surface 213 constructed according to the first embodiment of the present invention shown in FIGS. 1-3, and a second interconnect column 15b on surface 214, also constructed according to the first embodiment of the present invention.” Love, [12:13-12:25].</p>

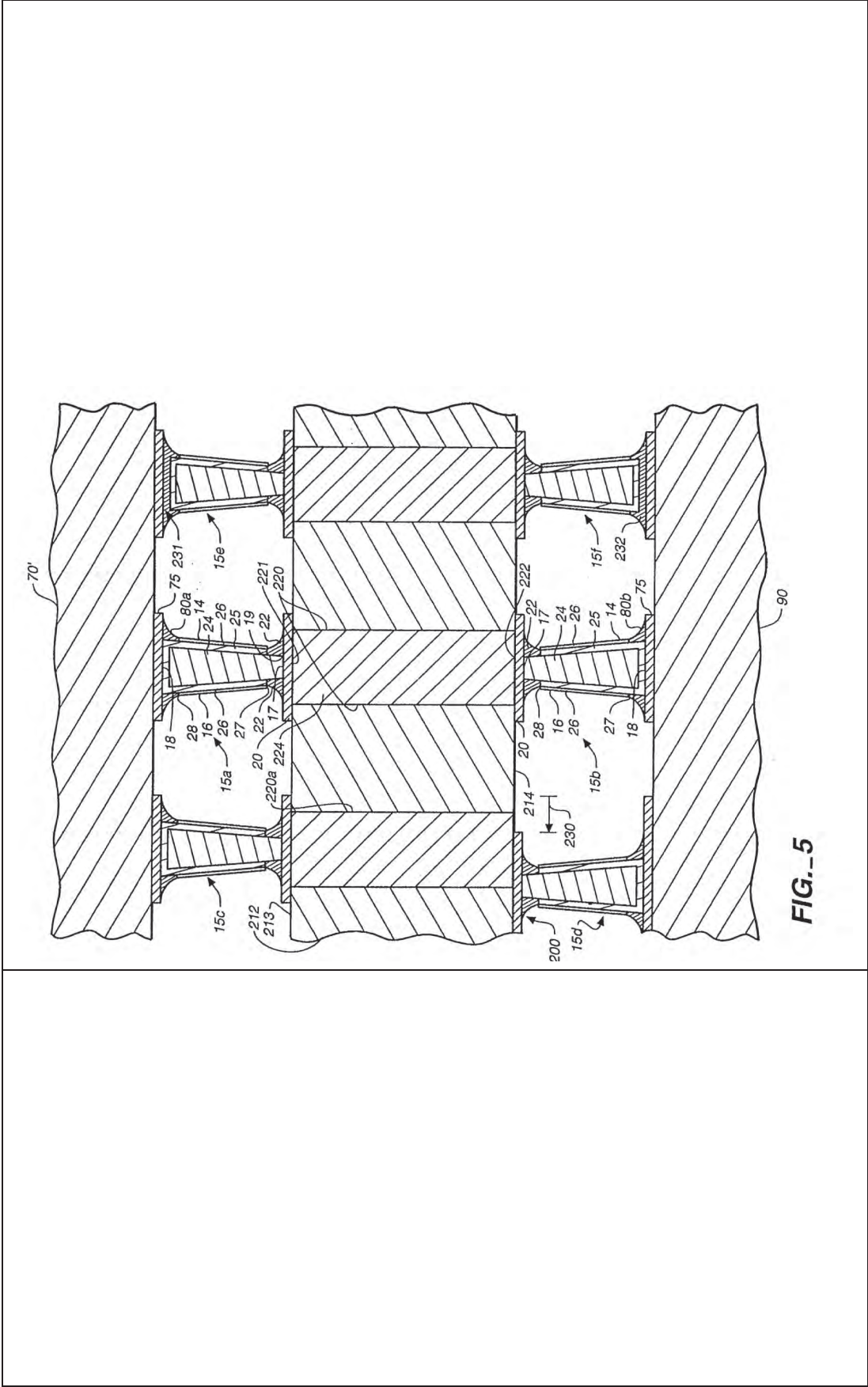


Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>Love, FIG. 5</p> <p>“First interconnect column 15a is disposed on first surface 213 of substrate 212 such that its bottom end 17 and base pad 20 are mounted to surface 213. First interconnect column 15a is for making contact to IC chip 70’. In a similar manner, second interconnect column 15b is disposed on second surface 214 of substrate 212, such that its bottom end 17 and base pad 20 are mounted to second surface 214. Second interconnect column 15b is for making contact to major substrate 90.” Love, [12:34-12:41].</p> <p>“Interconnect structure 200 further comprises a coupling means for electrically coupling first interconnect column 15a to second interconnect column 15b. In a preferred embodiment of the present invention, the coupling means comprises a through hole 220 passing through substrate 212 between first surface 213 and second surface 214, which is filled with a plug of conductive material 224. Through hole 220 includes a first end 221 next to base pad 20 and bottom end 17 of interconnect column 15a, and a second end 222 next to the base pad 20 and bottom end 17 of second interconnect column 15b. Plug 224 preferably comprises a metal, such as copper, or metal alloy which is formed within through hole 220. Plug 224 makes electrical contact to corresponding pads 20 of each of interconnect columns 15a and 15b and forms a conductive path therebetween, thereby electrically coupling columns 15a and 15b to one another.” Love, [12:42-12:59].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

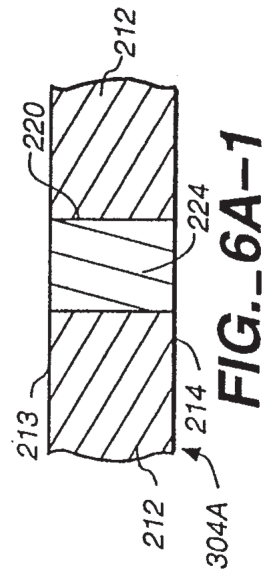
Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Love discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70', and having a first surface 213 and a second surface 214. Interconnect substrate 212 is also referred to as an interposer substrate or an intermediate substrate because it is disposed between substrate 90 and chip 70'. Wire interconnect structure 200 further comprises a first interconnect column 15a on surface 213 constructed according to the first embodiment of the present invention shown in FIGS. 1-3, and a second interconnect column 15b on surface 214, also constructed according to the first embodiment of the present invention.” Love, [12:13-12:25].</p>
--	--



	<p>Love, FIG. 5</p> <p>“Interconnect structure 200 further comprises a coupling means for electrically coupling first interconnect column 15a to second interconnect column 15b. In a preferred embodiment of the present invention, the coupling means comprises a through hole 220 passing through substrate 212 between first surface 213 and second surface 214, which is filled with a plug of conductive material 224. Through hole 220 includes a first end 221 next to base pad 20 and bottom end 17 of interconnect column 15a, and a second end 222 next to the base pad 20 and bottom end 17 of second interconnect column 15b. Plug 224 preferably comprises a metal, such as copper, or metal alloy which is formed within through hole 220. Plug 224 makes electrical contact to corresponding pads 20 of each of interconnect columns 15a and 15b and forms a conductive path therebetween, thereby electrically coupling columns 15a and 15b to one another.” Love, [12:42-12:59].</p> <p>“Interconnect substrate 212 may have a thickness in the range of 100 microns to 2,000 microns, with a value of 250 microns being presently preferred. Additionally, substrate 212 is formed from a non-conductive material and is preferably rigid. For example, substrate 212 may comprise a ceramic material, alumina, a glass material, sapphire, or a composite of polyimide and a rigid material. Through hole 220 is preferably circular in cross-section (as seen from the top plan view of substrate 212), and preferably has a diameter in the range of 12 microns to 50 microns. In one embodiment of interconnect structure 200, through hole 220 has a diameter of approximately 25 microns. Through hole 220 may be formed through substrate 212 by such means as laser drilling, photo etching followed by chemical milling, or by punching techniques. Such techniques are well known to those skilled in the art. The preferred technique used will likely depend on the choice of substrate material.” Love, [12:60-13:11].</p>
--	--

“Flow diagram 300 begins at block 302 with starting substrate 212, which may be made of ceramic. At block 304, through hole 220 is formed through substrate 212 and then plated with conductive material 224. A partial cross-sectional view of substrate 212 showing through hole 220 after the processing of block 304 is shown at 304A in FIG. 6A-1. In order to more clearly show the features of the layers to be subsequently deposited on the surfaces of substrate 212, the horizontal dimension of substrate 212 has been relatively expanded in the drawings shown in the FIGS. 6A-6D and the dimensions of some features have been enlarged so as to make them more readily apparent in these Figures. Through hole 220 may be formed in substrate 212 by a number of methods known in the art as described above. Likewise, conductive material 224 may be formed by a number of methods known in the art. For a single wire interconnect structure 10, the formation of through hole 220 is not a requirement, but may be performed if it provides an advantage in arranging the signal traces on substrate 212 for a particular application.” Love, [14:17-14:37].



Love, FIG. 6A-1

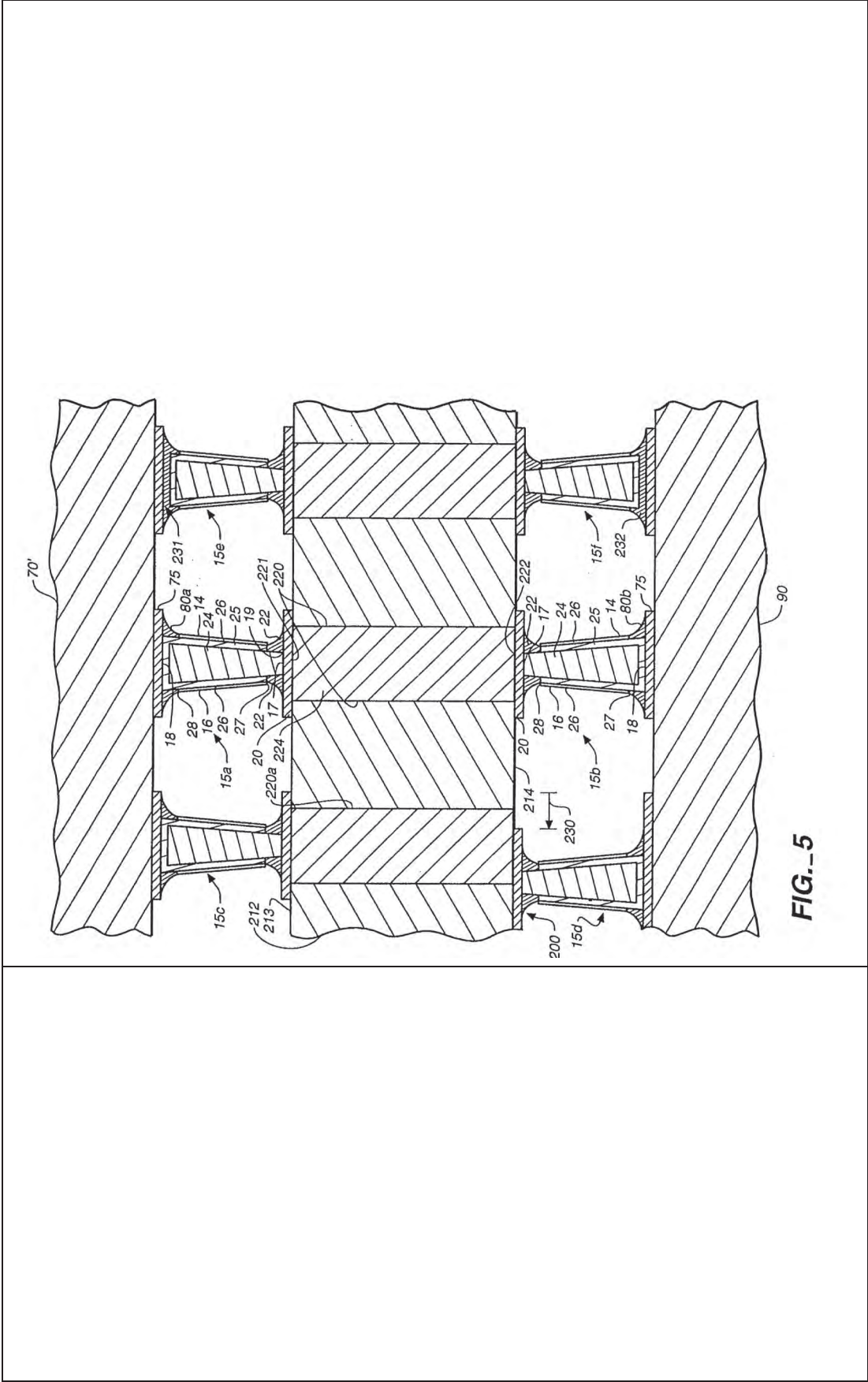
“At block 306, a base pad 20 for each interconnect column 15a and 15b is formed. For each side of substrate 212, the following steps are performed. First, a seed layer of copper is sputtered on each surface of substrate 212. Preferably, the seed layer may comprise an initial

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

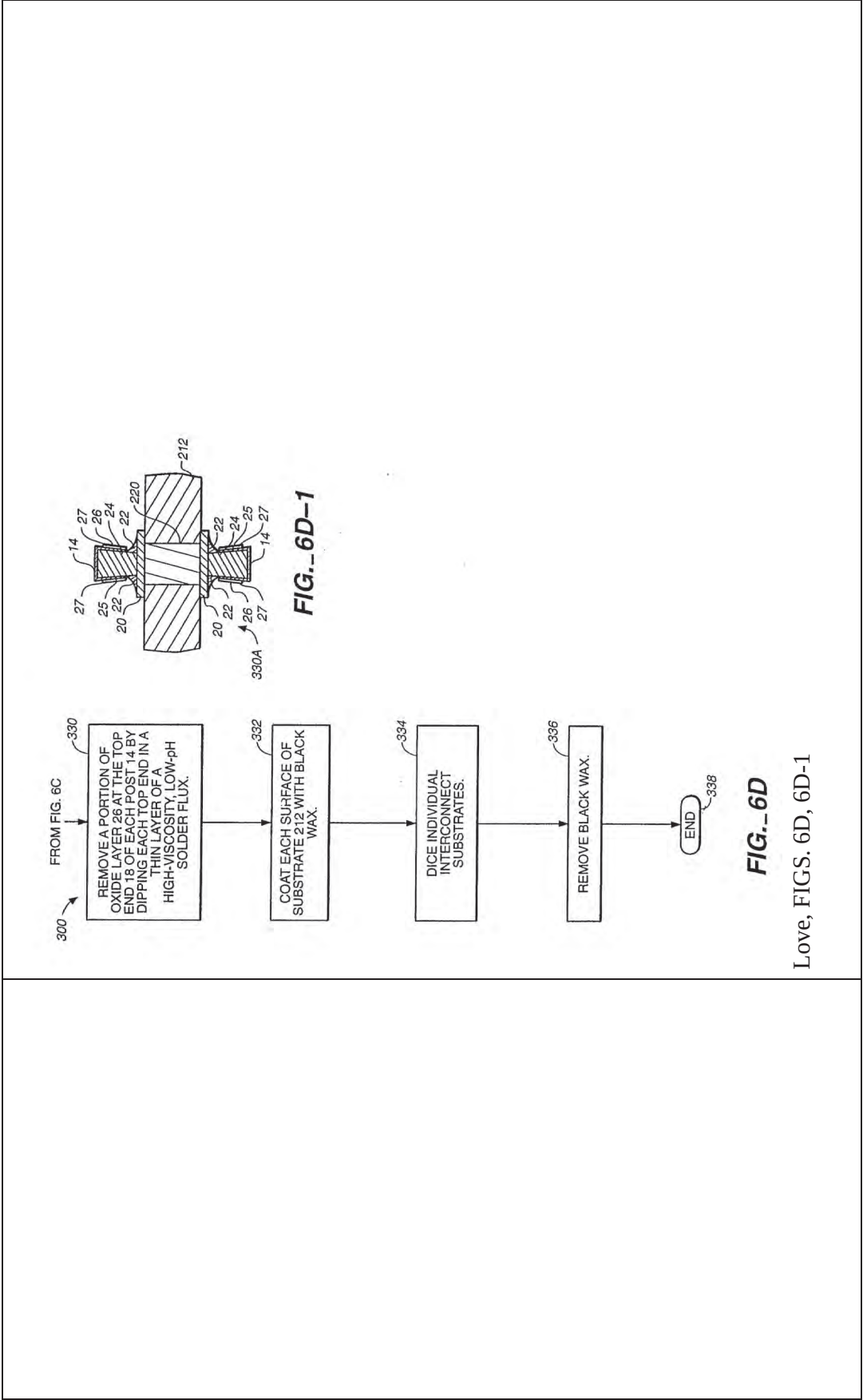
	<p>thin layer of chromium followed by a thin layer of copper (Cr/Cu), may comprise an initial thin layer of titanium followed by a thin layer of copper Ti/Cu), or may comprise a titanium-tungsten alloy layer (50%--50%) followed a layer of copper (Ti--W/Cu). Prior to depositing the seed layer, the surfaces of substrate 212 are cleaned well so as to activate these surfaces for the sputtered seed layer. Second, a photoresist (PR) layer is applied to each substrate side, and portions of the photoresist are removed where pads 20 are to be formed (e.g., exposing the photoresist to UV light through a mask and developing). This exposes the seed layer where pads 20 are to be formed. Third, copper is electroplated onto the exposed areas of the seed layer to a desired thickness, of for example ~1 micron, to form pads 20. The photoresist is then removed. The appearance of substrate 212 and pads 20 at the end of these steps is shown at a partial cross-section 306A of substrate 212 in FIG. 6A-2. A single wire interconnect structure 10 or a one-sided interconnect array 100 may be formed by only processing one side of substrate 212.” Love, [14:56-15:15].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Love discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Interconnect structure 200 further comprises a coupling means for electrically coupling first interconnect column 15a to second interconnect column 15b. In a preferred embodiment of the present invention, the coupling means comprises a through hole 220 passing through</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>substrate 212 between first surface 213 and second surface 214, which is filled with a plug of conductive material 224. Through hole 220 includes a first end 221 next to base pad 20 and bottom end 17 of interconnect column 15a, and a second end 222 next to the base pad 20 and bottom end 17 of second interconnect column 15b. Plug 224 preferably comprises a metal, such as copper, or metal alloy which is formed within through hole 220. Plug 224 makes electrical contact to corresponding pads 20 of each of interconnect columns 15a and 15b and forms a conductive path therebetween, thereby electrically coupling columns 15a and 15b to one another.” Love, [12:42-12:59].</p>
--	--



	<p>Love, FIG. 5</p> <p>“Flow diagram 300 begins at block 302 with starting substrate 212, which may be made of ceramic. At block 304, through hole 220 is formed through substrate 212 and then plated with conductive material 224. A partial cross-sectional view of substrate 212 showing through hole 220 after the processing of block 304 is shown at 304A in FIG. 6A-1. In order to more clearly show the features of the layers to be subsequently deposited on the surfaces of substrate 212, the horizontal dimension of substrate 212 has been relatively expanded in the drawings shown in the FIGS. 6A-6D and the dimensions of some features have been enlarged so as to make them more readily apparent in these Figures. Through hole 220 may be formed in substrate 212 by a number of methods known in the art as described above. Likewise, conductive material 224 may be formed by a number of methods known in the art. For a single wire interconnect structure 10, the formation of through hole 220 is not a requirement, but may be performed if it provides an advantage in arranging the signal traces on substrate 212 for a particular application.” Love, [14:17-14:37].</p>
--	---

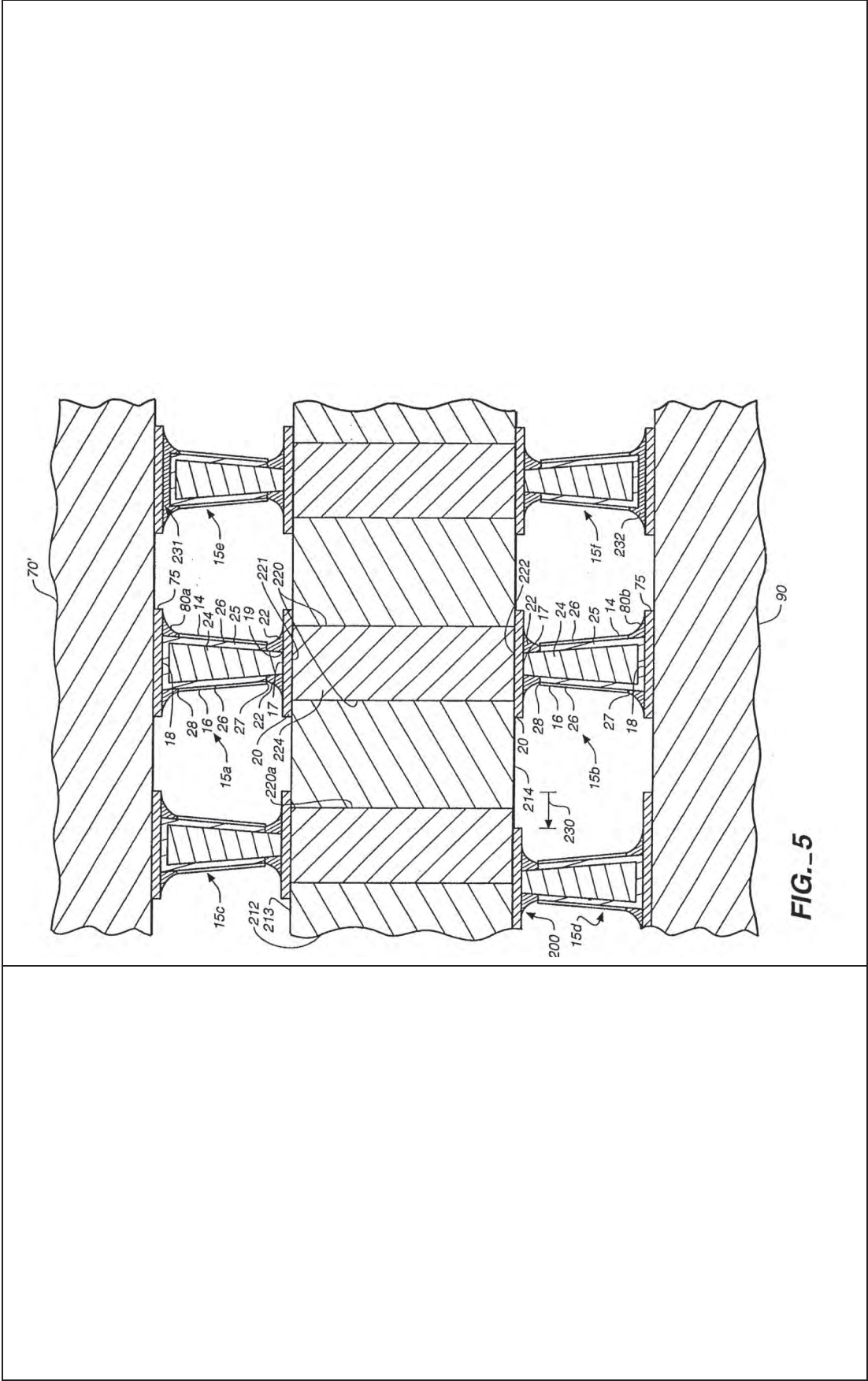


Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>“In one embodiment of the method of the present invention, through hole 220 may be formed and plated with conductive material 224 by the following sequence of steps. First, conductive through holes 220 are formed by either laser drilling or chemical milling from one surface, e.g., the “top” surface. As a second step, a layer of conductive material, such as copper, is sputtered on the other surface, the “back surface” of substrate 212. This sputtered layer will provide a seed layer for a subsequent plating step. As a third step, a conductive material, such as copper, is formed within through holes 220 by electrolytic or electroless plating. As a fourth step, a non-conductive protective layer is deposited on the front surface to protect the through holes 220 from a subsequent etching step. As a fifth step, the metal layer on the back surface is removed by etching. Finally, the protective layer on the front surface is removed and the surfaces of substrate 212 may be mechanically lapped to provide planar surfaces.” Love, [14:38-14:55].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Love discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“In a preferred embodiment of the present invention, interconnect column 15 further comprises a base pad 20 disposed between surface 13 and bottom end 17 of post 14. Base</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	pad 20 is mounted to surface 13, and bottom end 17 of post 14 is mounted to base pad 20.” Love, [7:32-7:36].
--	---



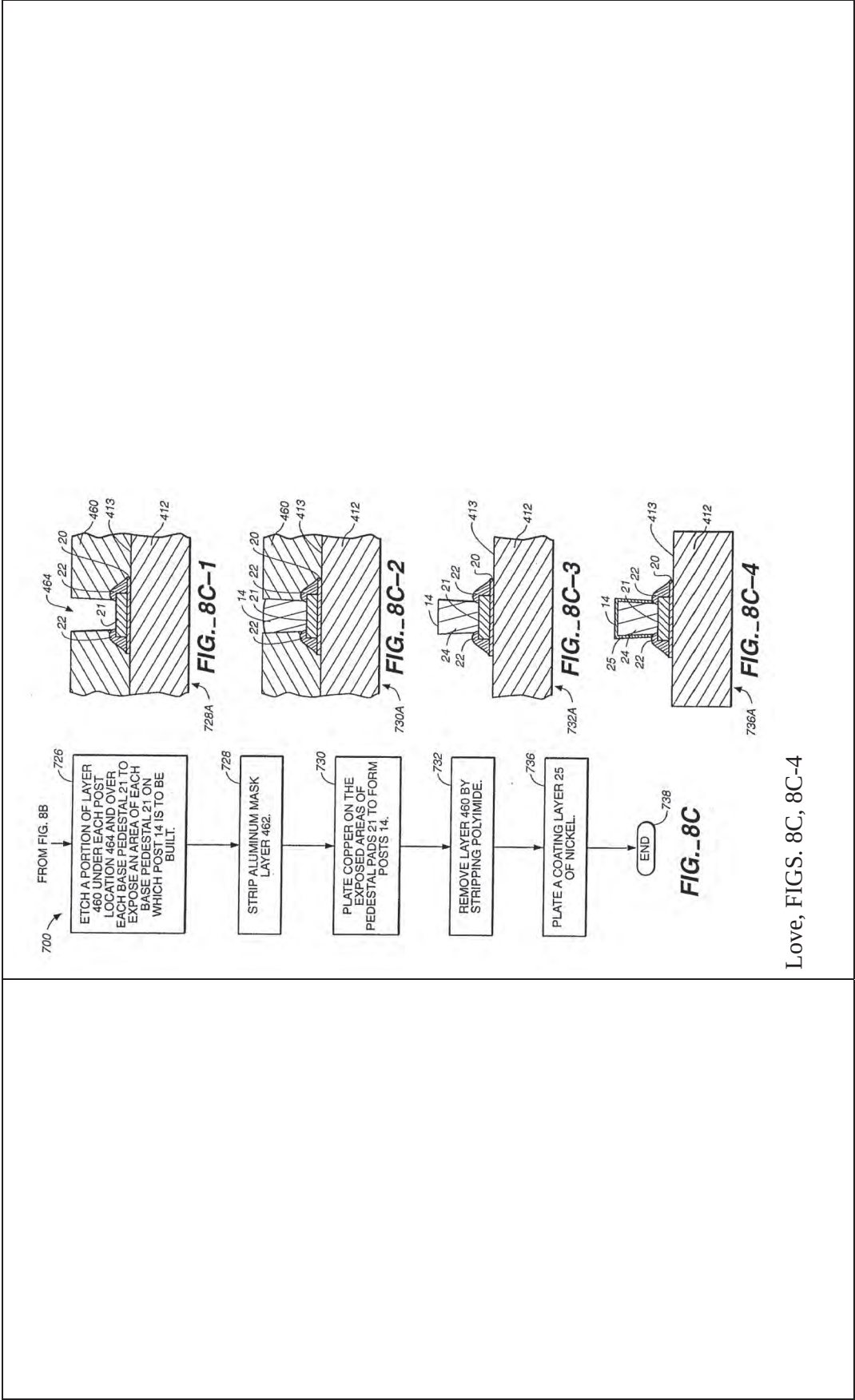
	<p>Love, FIG. 5</p> <p>“Preferably, base pad 20 comprises a metallic material, such as copper, nickel, cobalt, gold, or palladium. As described below in greater detail, base pad 20 facilitates the construction of post 14 by electroless or electrolytic plating, and preferably the top layer of base pad 20 comprises the same material as that of post 14.” Love, [7:36-7:42].</p> <p>“As an option, interconnect structure 10 may include a wire trace 50 on surface 13 for connecting an electronic signal present within substrate 12 to wire interconnect column 15. This signal may, for example, be generated by circuitry within substrate 12 or connected to substrate 12 by another interconnect structure. Trace 50 is electrically coupled to base pad 20 of interconnect column 15 and, in turn, to post 14. As an equivalent, a via in substrate 12 may be used.” Love, [7:43-7:51].</p> <p>“Fillet 22 serves to de-concentrate any of the mechanical stress and strain at the junction of end 17 and base pad 20 that may occur when post 14 is flexed. For example, when a force parallel to surface 13 is applied to the right side of post 14 near top end 18 by chip 70, post 14 will flex such that end 18 is displaced towards the left of its resting point. When flexed in this manner, forces are transmitted to fillet 22 which distribute the forces over a larger area, thereby preventing bottom end 17 from detaching from base pad 20. The transmitted forces include compressive forces applied to fillet 22 at the top of fillet 22 at its left side near point 28 and to the bottom of fillet 22 at its right side near point 29, and tensile forces applied at the right top side and the bottom right side of fillet 22. As the transmitted forces are distributed over a larger area, fillet 22 comprises means for de-concentrating mechanical strain at bottom end 17 of post 14.” Love, [10:5-10:22].</p>
--	---

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>“In one embodiment of the present invention, base pad 20 of each interconnect columns 15a-15d is approximately 40 microns wide and the bottom end 17 is approximately 10 microns in diameter, thereby allowing a 15 micron misalignment error for each of interconnect columns 15a and 15b. Other, more complex structures for interconnecting columns 15a and 15b can be used. It is not intended that the present invention be limited to the use of through holes or opposing interconnect columns.” Love, [13:32-13:39].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Love discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“First interconnect column 15a is disposed on first surface 213 of substrate 212 such that its bottom end 17 and base pad 20 are mounted to surface 213. First interconnect column 15a is for making contact to IC chip 70’. In a similar manner, second interconnect column 15b is disposed on second surface 214 of substrate 212, such that its bottom end 17 and base pad 20 are mounted to second surface 214.” Love, [12:34-12:41].</p> <p>“At block 317, portions of spacer layer 354 underlying post locations 358 are removed. This is may be done by reactive ion etching, other plasma etching processes, or wet etching processes. These portions of layer 354 are removed to expose respective areas of pads 20 upon which respective posts 14 are to be built. An etch process is selected such that relatively</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>little aluminum (layer 356) is removed. Bottom ends 17 of posts 14 are to be mounted at these exposed areas of pads 20.” Love, [16:40-16:48].</p> <p>“At block 320, a conductive material, preferably copper, is deposited on the exposed areas of pads 20. This is preferably done by electroless plating both surfaces of substrate 212. The copper material is only deposited on the exposed surface of each base pad 20 and is not deposited on the top of polyimide layer 354. In this regard, layer 354 also functions as a plating mask. The copper material builds up from each base pad 20 in the corresponding via thereby forming the interior portion 24 of each post 14.” Love, [17:26-17:35].</p> <p>“Interconnect column 415 further comprises a peripheral edge 19 formed around bottom end 17 next to surface 413, and in particular the outer peripheral portions of base pad 20 and base pedestal 21.” Love, [19:61-19:64].</p> <p>“At block 726, portions of spacer layer 460 underlying post locations 464 are removed. This may be done by reactive ion etching, other plasma etching processes, or wet etching processes. These portions of layer 460 are removed to expose respective areas of base pedestals 21 upon which respective posts 14 are to be built. An etch process is selected such that relatively little aluminum (layer 462) is removed. Bottom ends 17 of posts 14 are to be mounted at these exposed areas of base pedestals 21.” Love, [23:55-23:64].</p>
--	--



Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

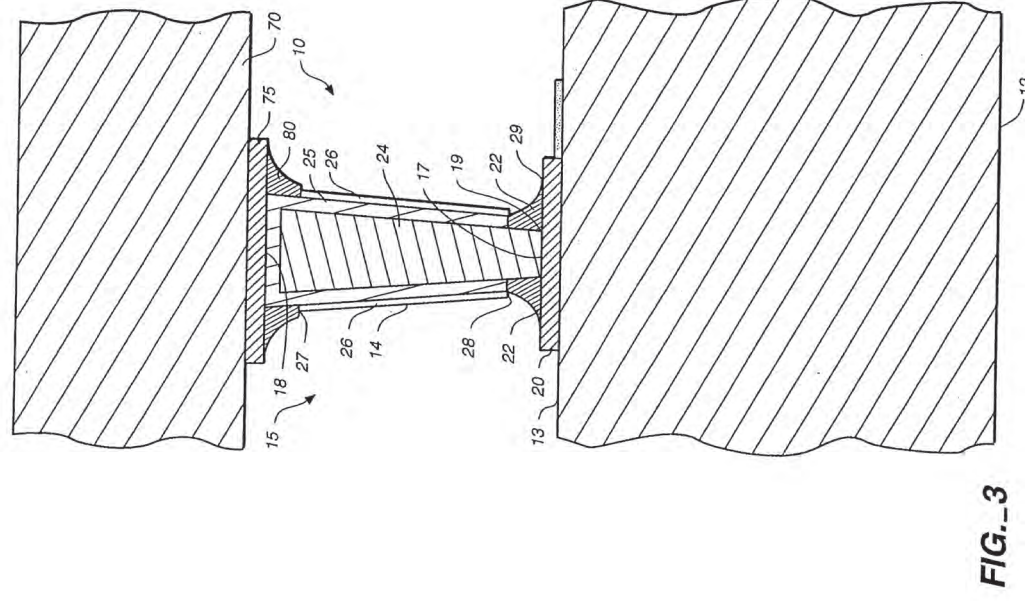
	<p>“At block 730, a conductive material, preferably copper, is deposited on the exposed areas of pedestal 21. This may be done by electroless plating or electrolytic plating of substrate surface 413. The copper material is only deposited on the exposed surface of each base pedestal 21 and is not deposited on the top of spacer layer 460. In this regard, spacer layer 460 also functions as a plating mask. The copper material builds up from each base pedestal 21 in the corresponding via thereby forming the interior portion 24 of each post 14. Each post 14 builds up around its corresponding fillet 22, making contact to the fillet at its peripheral edge 19.” Love, [24:25-24:36].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Love discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“To communicate the signal present on trace 50 to circuitry on integrated circuit chip 70, post 14 is electrically and mechanically connected to integrated circuit 70 via a bump 80 of reflowable and electrically conductive material. (The term “connecting” used herein is intended to have the breadth of the term “coupling” and to mean all means by which elements such as post 14 and chip 70 may be electrically coupled and/or mechanically coupled to one another. For example, electrically connecting is intended to encompass a direct wire</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

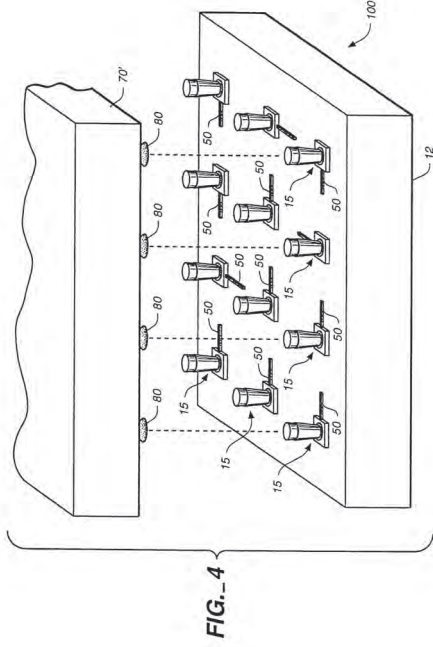
	<p>connection as well as a capacitive coupling between post 14 and IC chip 70, which may be provided by an element electrically and mechanically coupled between the two.) In one preferred embodiment of the present invention, bump 80 comprises a solder material, which is defined as a material which may be reflowed repeatedly and at a relatively low temperature in comparison to the melting temperature of post 14.” Love, [7:52-8:2].</p> <p>“To couple post 14 to bump 80, both post 14 and bump 80 are heated to a temperature which causes the material of bump 80 to become reflowable, in the case of a solder material, or pliable, in the case of a polymer material. Post 14 preferably comprises a material having a higher melting or reflow temperature point than the material of bump 80. During this heating process, chip 70 and substrate 12 are brought in close proximity to one another such that bump 80 makes contact with top end 18 of post 14. Light pressure, on the order of the weight of integrated circuit chip 70 (for example less than 0.5 N/cm.sup.2), is applied between substrate 12 and chip 70 during the contact process. Preferably, the heating process is performed in a forming gas atmosphere, such as 4% to 10% hydrogen in nitrogen, at a temperature exceeding the melting point of the material of bump 80. Once the melting temperature of the material of bump 80 is reached, bump 80 begins to reflow around post 14 near top end 18. Once reflowed, the temperature of substrate 12 and integrated circuit 70 is lowered to cause bump 80 to solidify around post 14, thereby making electrical mechanical coupling thereto.” Love, [8:57-9:11].</p> <p>“As indicated above, when bump 80 is joined to interconnect column 15, bump 80 reflows around post 14, ending substantially at point 27. This is shown in FIG. 3, which shows a cross-section of wire interconnect structure 10, interconnect column 15, substrate 12 and IC chip 70 taken through a vertical plane lying along line 2--2 shown in FIG. 1. Bump 80 also reflows outwardly along the surface of IC chip 70. In one embodiment of the present invention, bump 80 comprises solder disposed on a circular conductive pad 75 of IC chip 70</p>
--	---

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>having a diameter of about 25 microns. Pad 75 is surrounded by material which does not readily wet to solder. A non-wettable ring is thereby formed around pad 75, which forces the solder material to have a certain height (i.e., ball limiting metalization). For a 25 micron circular pad, this height is approximately 5 microns. Bump 80 may be deposited on IC chip 70 using any of the following standard methods of bump deposition well known in the art: lift-off, subtractive, additive, or shadow-mask vapor deposition.” Love, [10:23-10:42].</p>
--	--



	<p>Love, FIG. 3</p> <p>“FIG. 4 is an isometric view of a wire interconnect structure comprising an array of interconnect columns, each interconnect column in the array being the same as interconnect column 15 shown in FIGS. 1 and 2 with the exception that the corresponding electrical trace 50 for each structure is not necessarily oriented in the same direction as that shown in FIGS. 1 and 2. The wire interconnect array has been given the general reference designation of 100 in FIG. 4. Wire interconnect array 100 comprises a plurality of interconnect columns 15 disposed on substrate 12. Using present technology, these interconnect structures may be spaced as close as 30 microns to one another, a distance which may be substantially less than their height. Also shown in FIG. 4 is an integrated circuit chip 70' having a plurality of bumps 80. The plurality of bumps 80 are configured in a “mirrored” array corresponding to array 100 such that each bump is in a generally confronting and corresponding relationship to a respective interconnect column 15. The interconnect columns 15 are bonded to their respective bumps 80 with the above-described heat-reflow process after first being brought into registration by known means.” Love, [10:47-11:2].</p>
--	---



Love, FIG. 4

“FIG. 5 is a cross-sectional view of a second embodiment of the wire interconnect structure according to the present invention, which has been given the general reference designation of 200. The embodiment is referred to as wire interconnect structure 200 and is for electrically coupling a major substrate 90 to integrated circuit chip 70', as shown in FIG. 5. Wire interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70'. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70', and having a first surface 213 and a second surface 214. Interconnect substrate 212 is also referred to as an interposer substrate or an intermediate substrate because it is disposed between substrate 90 and chip 70'. Wire interconnect structure 200 further comprises a first interconnect column 15a on surface 213 constructed according to the first embodiment of the present invention shown in FIGS. 1-3, and a second interconnect column 15b on surface 214, also constructed

according to the first embodiment of the present invention. Each of the interconnect columns 15a and 15b comprises a post 14 with elongated body 16 and ends 17 and 18, a base pad 20, a fillet 22, and a peripheral edge 19, as described above.” Love, [12:4-12:28].

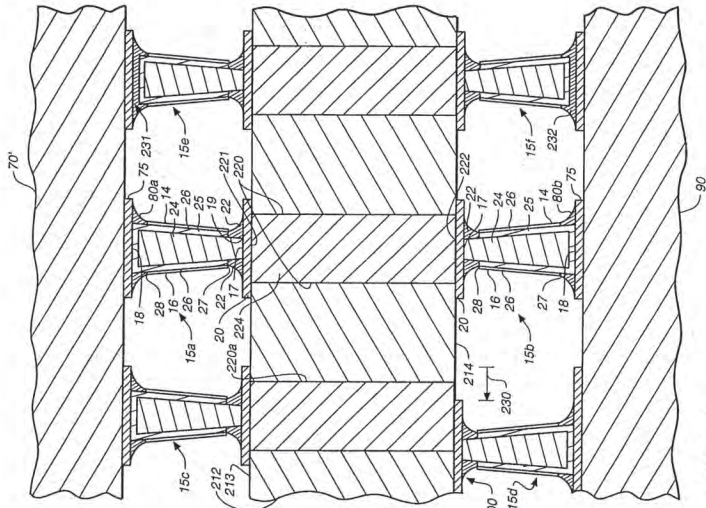


FIG. 5

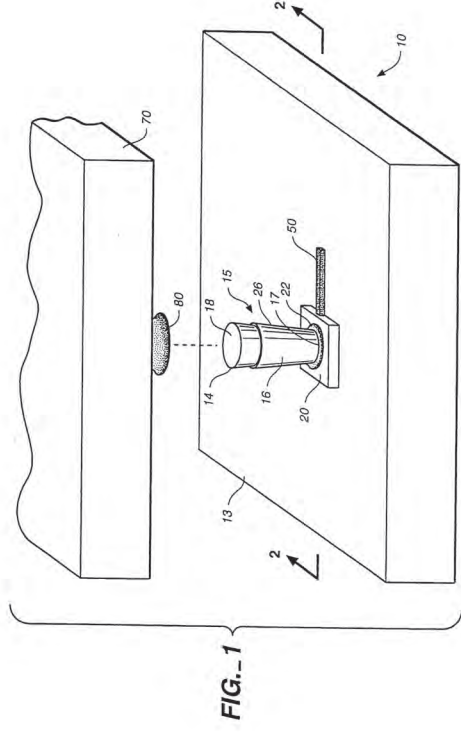
Love, FIG. 5

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>“Interconnect structure 200 further comprises a coupling means for electrically coupling first interconnect column 15a to second interconnect column 15b. In a preferred embodiment of the present invention, the coupling means comprises a through hole 220 passing through substrate 212 between first surface 213 and second surface 214, which is filled with a plug of conductive material 224. Through hole 220 includes a first end 221 next to base pad 20 and bottom end 17 of interconnect column 15a, and a second end 222 next to the base pad 20 and bottom end 17 of second interconnect column 15b. Plug 224 preferably comprises a metal, such as copper, or metal alloy which is formed within through hole 220. Plug 224 makes electrical contact to corresponding pads 20 of each of interconnect columns 15a and 15b and forms a conductive path therebetween, thereby electrically coupling columns 15a and 15b to one another.” Love, [12:42-12:59].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Love discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“FIG. 5 is a cross-sectional view of a second embodiment of the wire interconnect structure according to the present invention, which has been given the general reference designation of 200. The embodiment is referred to as wire interconnect structure 200 and is for electrically coupling a major substrate 90 to integrated circuit chip 70’, as shown in FIG. 5. Wire</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70'. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70', and having a first surface 213 and a second surface 214." Love, [12:4-12:16].</p> <p>"Wire interconnect structure 200 further comprises a first interconnect column 15a on surface 213 constructed according to the first embodiment of the present invention shown in FIGS. 1-3, and a second interconnect column 15b on surface 214, also constructed according to the first embodiment of the present invention. Each of the interconnect columns 15a and 15b comprises a post 14 with elongated body 16 and ends 17 and 18, a base pad 20, a fillet 22, and a peripheral edge 19, as described above. Additionally, post 14 comprises an interior portion 24, a coating layer 25, and an oxide layer 26, all as described above. The reference numerals used in describing interconnect column 15 shown in FIGS. 1-3 have been used for interconnect columns 15a and 15b of FIG. 5. First interconnect column 15a is disposed on first surface 213 of substrate 212 such that its bottom end 17 and base pad 20 are mounted to surface 213. First interconnect column 15a is for making contact to IC chip 70'. In a similar manner, second interconnect column 15b is disposed on second surface 214 of substrate 212, such that its bottom end 17 and base pad 20 are mounted to second surface 214. Second interconnect column 15b is for making contact to major substrate 90. Interconnect structure 200 further comprises a coupling means for electrically coupling first interconnect column 15a to second interconnect column 15b." Love, [12:19-12:44].</p>
--	---



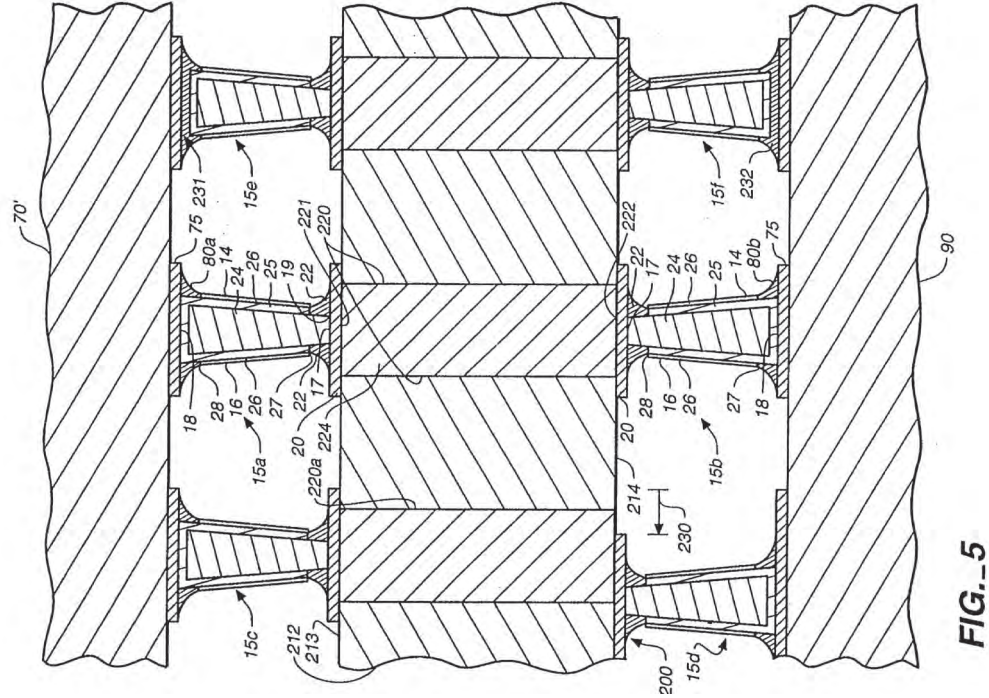
Love, FIG. 1

“In a preferred embodiment of the present invention, the coupling means comprises a through hole 220 passing through substrate 212 between first surface 213 and second surface 214, which is filled with a plug of conductive material 224. Through hole 220 includes a first end 221 next to base pad 20 and bottom end 17 of interconnect column 15a, and a second end 222 next to the base pad 20 and bottom end 17 of second interconnect column 15b. Plug 224 preferably comprises a metal, such as copper, or metal alloy which is formed within through hole 220. Plug 224 makes electrical contact to corresponding pads 20 of each of interconnect columns 15a and 15b and forms a conductive path therebetween, thereby electrically coupling columns 15a and 15b to one another.” Love, [12:44-12:59].

“Also in a preferred embodiment of interconnect structure 200, the posts of interconnect columns 15a and 15b are disposed substantially opposite to one another at respective opposite

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

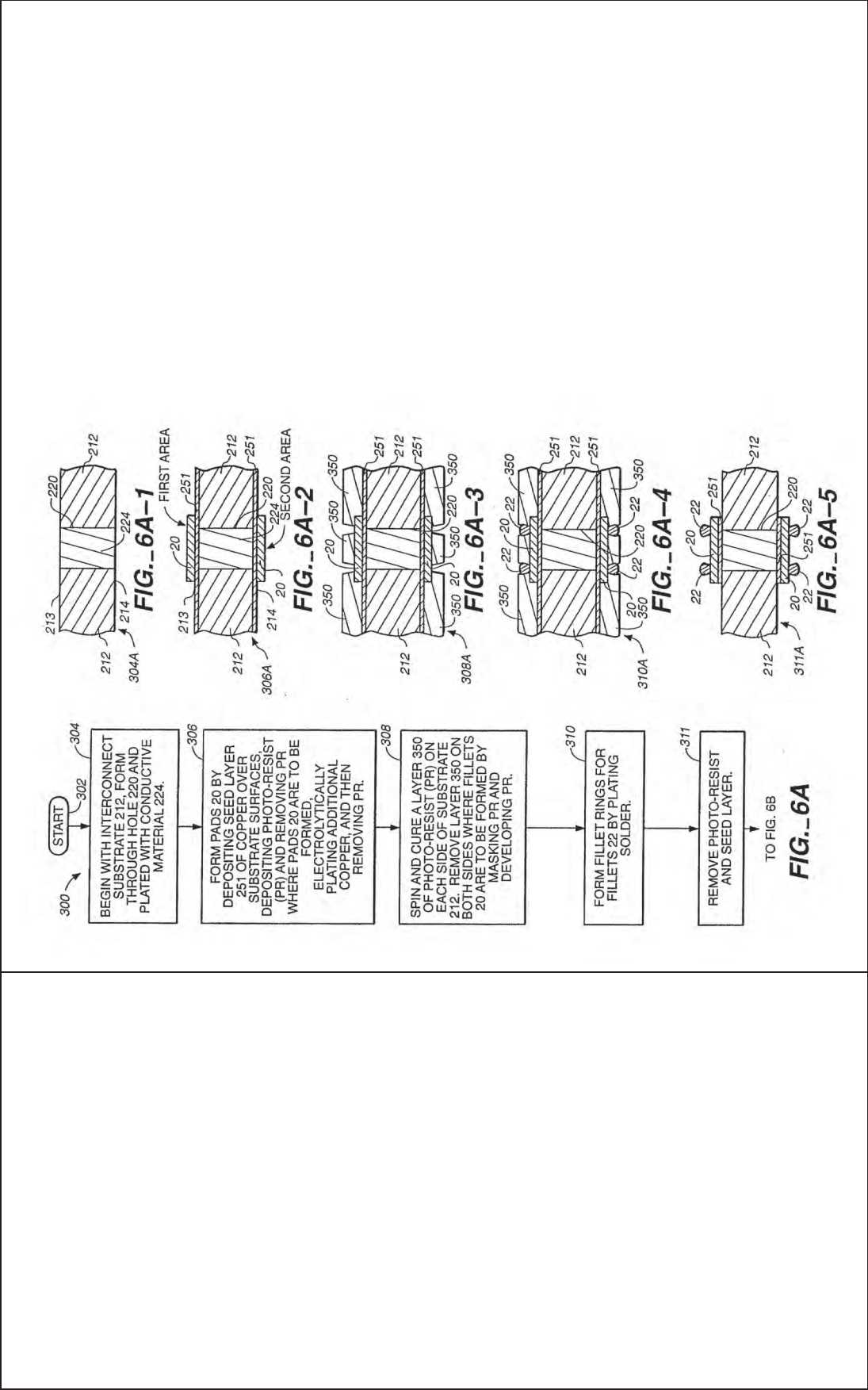
	<p>ends of through hole 220 to facilitate the electrical connection therebetween. However, it may be appreciated that the interconnect columns may be somewhat offset from an exact opposing relationship, as shown, for example, by two interconnect columns 15c and 15d in FIG. 5. Interconnect column 15c is disposed on surface 213 and interconnect column 15d is disposed on surface 214. Interconnect columns 15c and 15d are disposed at opposite ends of a through hole 220a, with an offset 230 in the placement of interconnect column 15d. Such an offset may occur during the construction of interconnect column 15d. As described below in greater detail, photo-lithographic steps applied separately to surfaces 213 and 214 of substrate 212 may be used to form interconnect columns 15c and 15d. The use of separate photo-lithographic steps is susceptible to alignment errors, which may give rise to offset 230. In one embodiment of the present invention, base pad 20 of each interconnect columns 15a-15d is approximately 40 microns wide and the bottom end 17 is approximately 10 microns in diameter, thereby allowing a 15 micron misalignment error for each of interconnect columns 15a and 15b. Other, more complex structures for interconnecting columns 15a and 15b can be used. It is not intended that the present invention be limited to the use of through holes or opposing interconnect columns.” Love, [13:12-13:39].</p>
--	--



	<p>Love, FIG. 5</p> <p>“At block 304, through hole 220 is formed through substrate 212 and then plated with conductive material 224. A partial cross-sectional view of substrate 212 showing through hole 220 after the processing of block 304 is shown at 304A in FIG. 6A-1. In order to more clearly show the features of the layers to be subsequently deposited on the surfaces of substrate 212, the horizontal dimension of substrate 212 has been relatively expanded in the drawings shown in the FIGS. 6A-6D and the dimensions of some features have been enlarged so as to make them more readily apparent in these Figures. Through hole 220 may be formed in substrate 212 by a number of methods known in the art as described above. Likewise, conductive material 224 may be formed by a number of methods known in the art. For a single wire interconnect structure 10, the formation of through hole 220 is not a requirement, but may be performed if it provides an advantage in arranging the signal traces on substrate 212 for a particular application. In one embodiment of the method of the present invention, through hole 220 may be formed and plated with conductive material 224 by the following sequence of steps.” Love, [14:18-14:41].</p> <p>“At block 306, a base pad 20 for each interconnect column 15a and 15b is formed. For each side of substrate 212, the following steps are performed. First, a seed layer of copper is sputtered on each surface of substrate 212. Preferably, the seed layer may comprise an initial thin layer of chromium followed by a thin layer of copper (Cr/Cu), may comprise an initial thin layer of titanium followed by a thin layer of copper Ti/Cu), or may comprise a titanium-tungsten alloy layer (50%--50%) followed a layer of copper (Ti--W/Cu). Prior to depositing the seed layer, the surfaces of substrate 212 are cleaned well so as to activate these surfaces for the sputtered seed layer. Second, a photoresist (PR) layer is applied to each substrate side, and portions of the photoresist are removed where pads 20 are to be formed (e.g., exposing the photoresist to UV light through a mask and developing). This exposes the seed layer</p>
--	---

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>where pads 20 are to be formed. Third, copper is electroplated onto the exposed areas of the seed layer to a desired thickness, of for example, about 1 micron, to form pads 20. The photoresist is then removed. The appearance of substrate 212 and pads 20 at the end of these steps is shown at a partial cross-section 306A of substrate 212 in FIG. 6A-2. A single wire interconnect structure 10 or a one-sided interconnect array 100 may be formed by only processing one side of substrate 212. The copper plug 224 in through hole 220 and pads 20 on the surfaces of substrate 212 collectively comprise an electrical conductive path from a first area (i.e., pad 20) on surface 213 to a second area (i.e., pad 20) on surface 214.” Love, [14:56-15:20].</p>
--	---

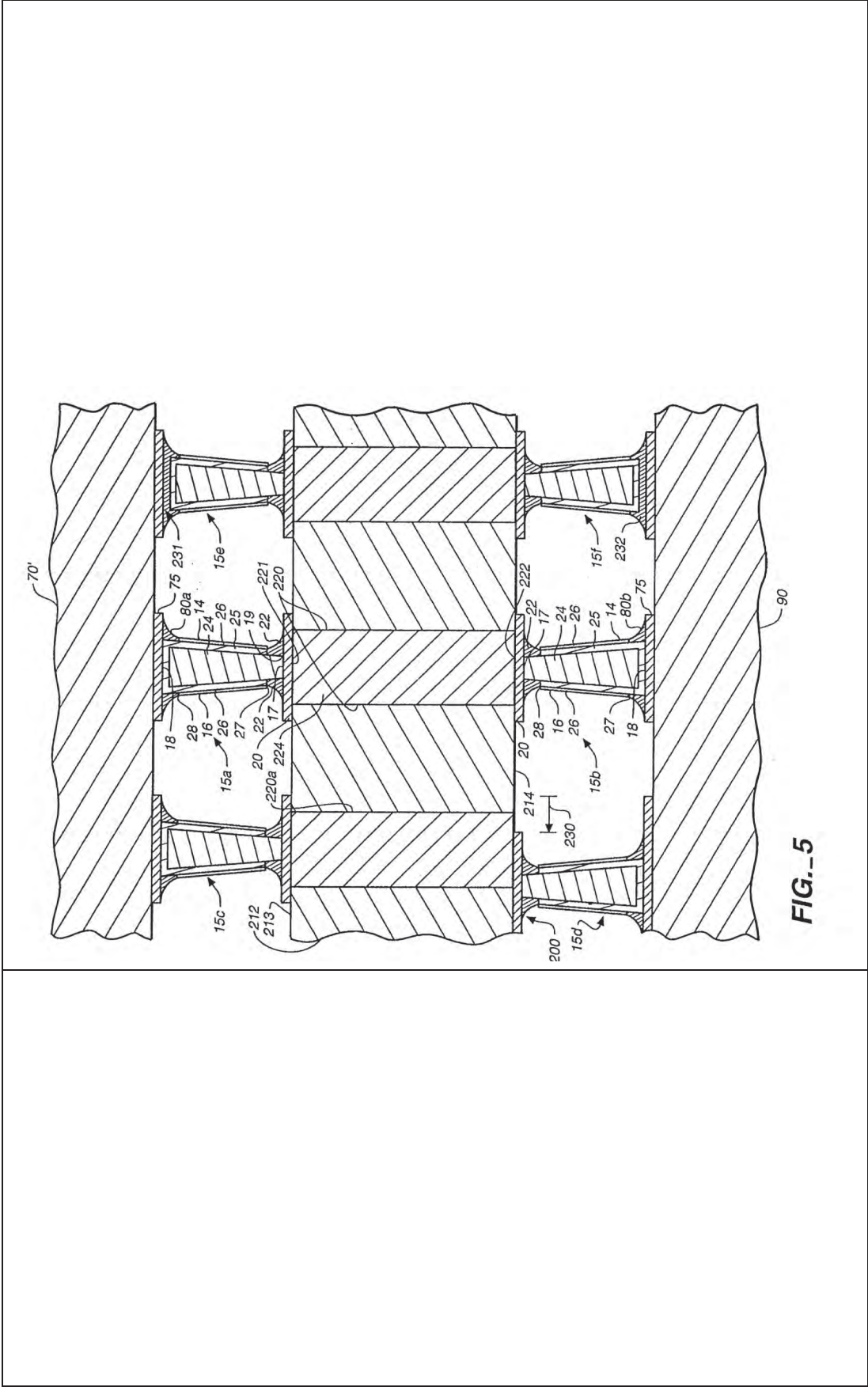


Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>Love, FIGS. 6A, 6A-1–6A-5</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Love discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Wire interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70’. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70’, and having a first surface 213 and a second surface 214. Interconnect substrate 212 is also referred to as an interposer substrate or an intermediate substrate because it is disposed between substrate 90 and chip 70’. Wire interconnect structure 200 further comprises a first interconnect column 15a on surface 213 constructed according to the first embodiment of the present invention shown in FIGS. 1-3, and a second interconnect column 15b on surface 214, also constructed according to the first embodiment of the present invention. Each of the interconnect columns 15a and 15b comprises a post 14 with elongated body 16 and ends 17 and 18, a base pad 20, a fillet 22, and a peripheral edge 19, as described above. Additionally, post 14 comprises an interior portion 24, a coating layer 25, and an oxide layer 26, all as described above. The reference numerals used in describing interconnect column 15 shown</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

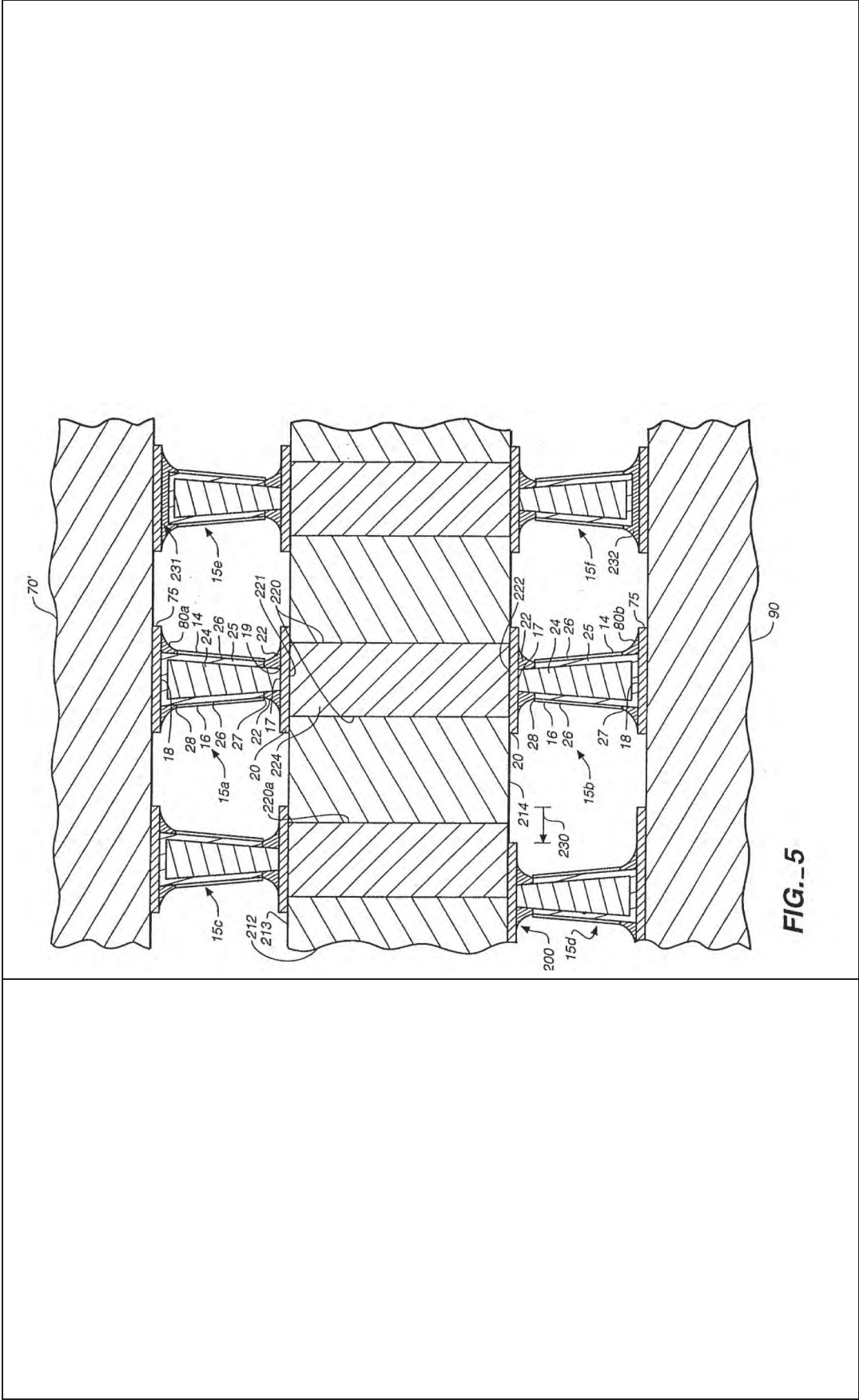
	<p>in FIGS. 1-3 have been used for interconnect columns 15a and 15b of FIG. 5. First interconnect column 15a is disposed on first surface 213 of substrate 212 such that its bottom end 17 and base pad 20 are mounted to surface 213.” Love, [12:10-12:36].</p>
--	--



	<p>Love, FIG. 5</p> <p>“Also in a preferred embodiment of interconnect structure 200, the posts of interconnect columns 15a and 15b are disposed substantially opposite to one another at respective opposite ends of through hole 220 to facilitate the electrical connection therebetween. However, it may be appreciated that the interconnect columns may be somewhat offset from an exact opposing relationship, as shown, for example, by two interconnect columns 15c and 15d in FIG. 5. Interconnect column 15c is disposed on surface 213 and interconnect column 15d is disposed on surface 214. Interconnect columns 15c and 15d are disposed at opposite ends of a through hole 220a, with an offset 230 in the placement of interconnect column 15d. Such an offset may occur during the construction of interconnect column 15d. As described below in greater detail, photo-lithographic steps applied separately to surfaces 213 and 214 of substrate 212 may be used to form interconnect columns 15c and 15d. The use of separate photo-lithographic steps is susceptible to alignment errors, which may give rise to offset 230. In one embodiment of the present invention, base pad 20 of each interconnect columns 15a-15d is approximately 40 microns wide and the bottom end 17 is approximately 10 microns in diameter, thereby allowing a 15 micron misalignment error for each of interconnect columns 15a and 15b. Other, more complex structures for interconnecting columns 15a and 15b can be used. It is not intended that the present invention be limited to the use of through holes or opposing interconnect columns.” Love, [13:12-13:39].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

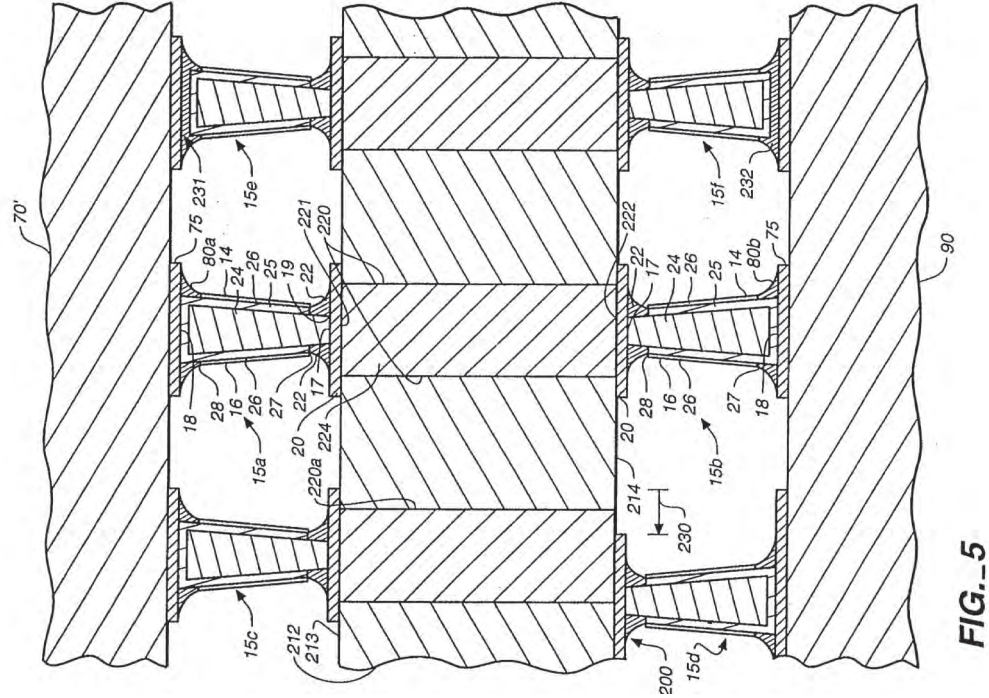
Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Love discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>
---	--



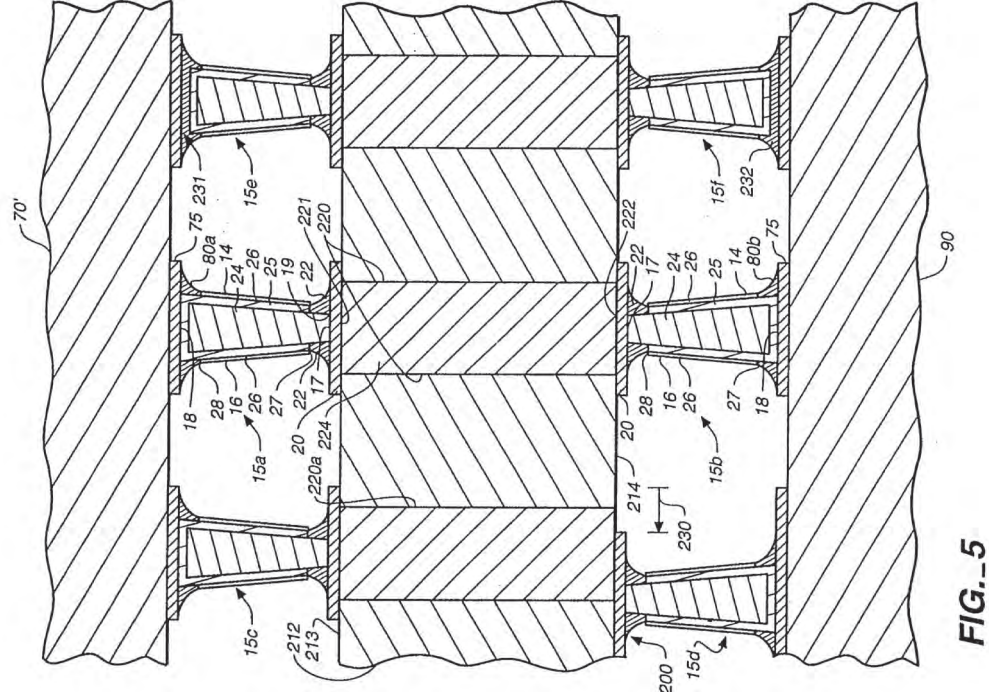
Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>Love, FIG. 5</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Love discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>



Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>Love, FIG. 5</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Love discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>



Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>Love, FIG. 5</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Love discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 5 is a cross-sectional view of a second embodiment of the wire interconnect structure according to the present invention, which has been given the general reference designation of 200. The embodiment is referred to as wire interconnect structure 200 and is for electrically coupling a major substrate 90 to integrated circuit chip 70', as shown in FIG. 5. Wire interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70'. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70', and having a first surface 213 and a second surface 214.” Love, [12:4-12:16].</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

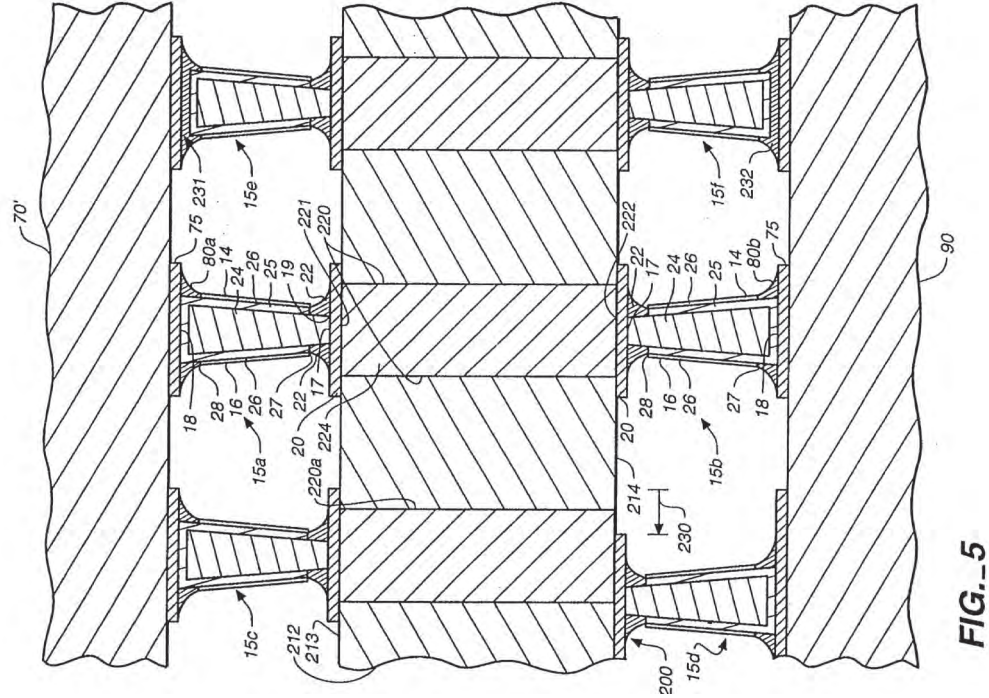
	<p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Love discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“As a practical matter, integrated circuit chip 70' may have a surface which is warped, with a typical maximum deviation of approximately 2 microns from low point to high point. As such, not every interconnect column 15 will make contact to the surface of integrated circuit chip 70'. However, generally at least three of the interconnect structures will contact the surface of integrated circuit chip 70'. Given that the maximum warpage of the surface of chip 70' is approximately 2 microns and that the variation in height of interconnect columns 15 is approximately 2 microns, there is a possibility that one or more of the interconnect columns 15 may be spaced approximately 4 microns away from the surface of chip 70' after the contacting process is completed. However, bump 80 is typically at least 5 microns high and is able to contact its corresponding interconnect structure 10 and form a bond thereto should</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

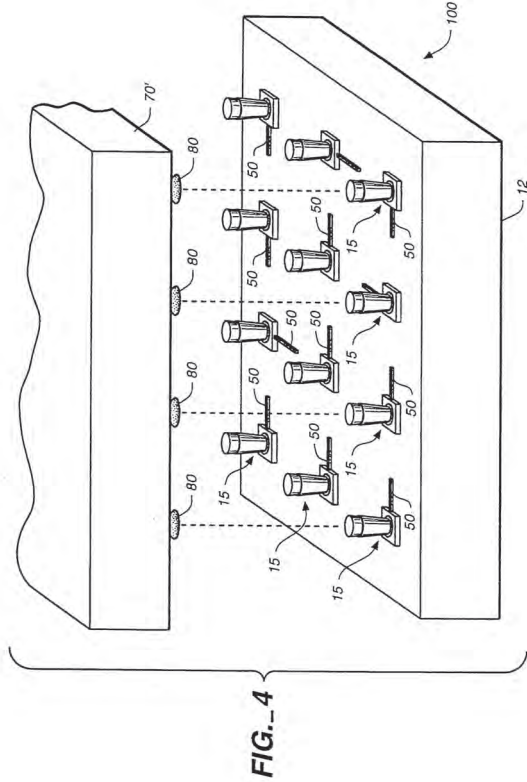
	<p>such a gap exist between the interconnect column and chip 70'. As bump 80 is made from a conductive material, an electrical signal is able to be transmitted between interconnect structure 10 and chip 70' even if interconnect column 15 does not physically touch the surface of chip 70' (e.g., pad 75). It may be appreciated that bumps of solder material can be formed up to a height of 75 microns so that contact can be made if the spacing between chip 70' and an interconnect structure 10 is greater than 5 microns." Love, [11:4-11:30].</p>
--	---



	<p>Love, FIG. 5</p> <p>“In the embodiments of the present invention in which bumps 80 comprise a metal, such as indium, bismuth, gallium, tin, lead, or their alloys, the surface tension of bump 80, when molten, aids in bringing the array of bumps 80 into alignment with array 100. Under reflow conditions, each of the metal bumps 80 seeks a minimum surface area around the corresponding interconnect column 15 of the wire interconnect array 100 as it flows around the structure, the minimum surface area being achieved when the bump is symmetrically disposed around the top end of its corresponding column 15. The surface tension of each bump surface applies a force between its respective IC chip pad and its corresponding interconnect column 15 in a direction which causes the bump to be symmetrically positioned around its corresponding interconnect column. As such, any misalignment that may occur in positioning IC chip 70' over array 100 before the heat-bonding process will be corrected, or minimized, by the surface tension forces as long as there is an initial contact of a few bumps with their corresponding interconnect structures. Depending upon the material of bump 80 and the size and geometry of the interconnect structure, the surface tension forces can be significant, and may be quite large in comparison to the gravitational force applied to chip 70' during the heat-bonding process.” Love, [11:32-11:56].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Love discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 4 is an isometric view of a wire interconnect structure comprising an array of interconnect columns, each interconnect column in the array being the same as interconnect column 15 shown in FIGS. 1 and 2 with the exception that the corresponding electrical trace 50 for each structure is not necessarily oriented in the same direction as that shown in FIGS. 1 and 2. The wire interconnect array has been given the general reference designation of 100 in FIG. 4. Wire interconnect array 100 comprises a plurality of interconnect columns 15 disposed on substrate 12. Using present technology, these interconnect structures may be spaced as close as 30 microns to one another, a distance which may be substantially less than their height. Also shown in FIG. 4 is an integrated circuit chip 70' having a plurality of bumps 80. The plurality of bumps 80 are configured in a “mirrored” array corresponding to array 100 such that each bump is in a generally confronting and corresponding relationship to a respective interconnect column 15.” Love, [10:47-10:66].</p>



Love, FIG. 4

“The interconnect columns 15 are bonded to their respective bumps 80 with the above-described heat-reflow process after first being brought into registration by known means.”
Love, [10:66-11:2].

“In the embodiments of the present invention in which bumps 80 comprise a metal, such as indium, bismuth, gallium, tin, lead, or their alloys, the surface tension of bump 80, when molten, aids in bringing the array of bumps 80 into alignment with array 100. Under reflow conditions, each of the metal bumps 80 seeks a minimum surface area around the corresponding interconnect column 15 of the wire interconnect array 100 as it flows around

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>the structure, the minimum surface area being achieved when the bump is symmetrically disposed around the top end of its corresponding column 15.” Love, [11:32-11:41].</p> <p>“Also in a preferred embodiment of interconnect structure 200, the posts of interconnect columns 15a and 15b are disposed substantially opposite to one another at respective opposite ends of through hole 220 to facilitate the electrical connection therebetween.” Love, [13:12-13:16].</p>
--	---

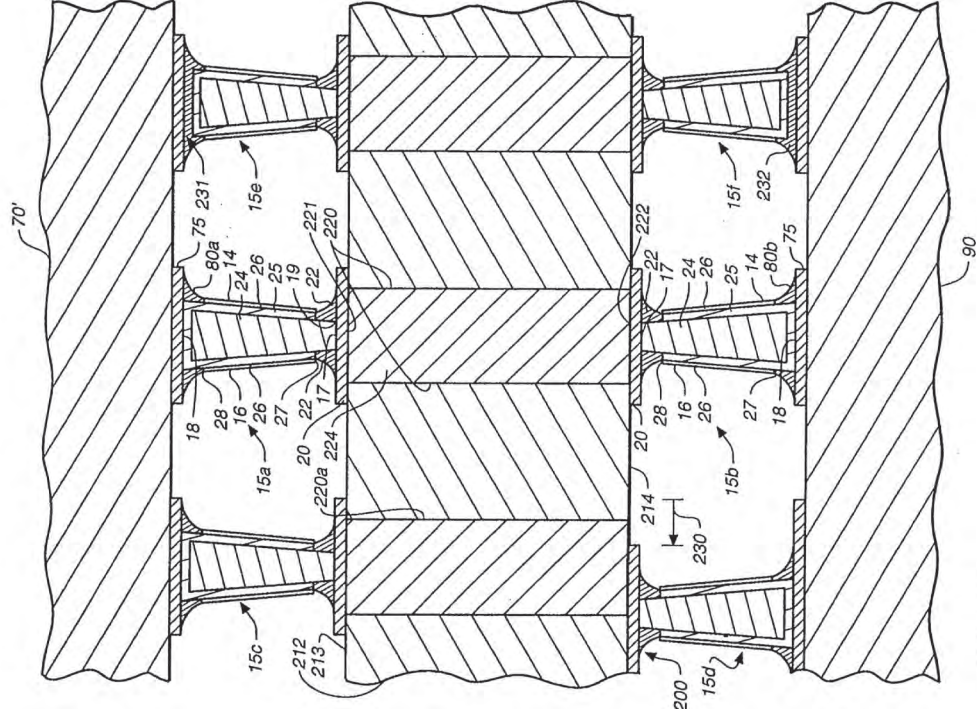


FIG. 5

	<p>Love, FIG. 5</p> <p>“However, it may be appreciated that the interconnect columns may be somewhat offset from an exact opposing relationship, as shown, for example, by two interconnect columns 15c and 15d in FIG. 5. Interconnect column 15c is disposed on surface 213 and interconnect column 15d is disposed on surface 214. Interconnect columns 15c and 15d are disposed at opposite ends of a through hole 220a, with an offset 230 in the placement of interconnect column 15d. Such an offset may occur during the construction of interconnect column 15d. As described below in greater detail, photo-lithographic steps applied separately to surfaces 213 and 214 of substrate 212 may be used to form interconnect columns 15c and 15d. The use of separate photo-lithographic steps is susceptible to alignment errors, which may give rise to offset 230. In one embodiment of the present invention, base pad 20 of each interconnect columns 15a-15d is approximately 40 microns wide and the bottom end 17 is approximately 10 microns in diameter, thereby allowing a 15 micron misalignment error for each of interconnect columns 15a and 15b.” Love, [13:16-13:36].</p> <p>“A single wire interconnect structure 10 or a one-sided interconnect array 100 may be formed by only processing one side of substrate 212. The copper plug 224 in through hole 220 and pads 20 on the surfaces of substrate 212 collectively comprise an electrical conductive path from a first area (i.e., pad 20) on surface 213 to a second area (i.e., pad 20) on surface 214. It may be further appreciated that the above steps for forming through hole 220 and pads 20 collectively comprise a means for forming such an electrically conductive path. At block 308, substrate 212 is prepared for the formation of fillet rings for fillets 22. At block 308, a layer 350 of photoresist is spun on each side (surface) of substrate 212. Next, a portion of layer 350 is removed over each base pad 20 where the fillets 22 are to be formed.” Love, [15:12-15:28].</p>
--	---

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

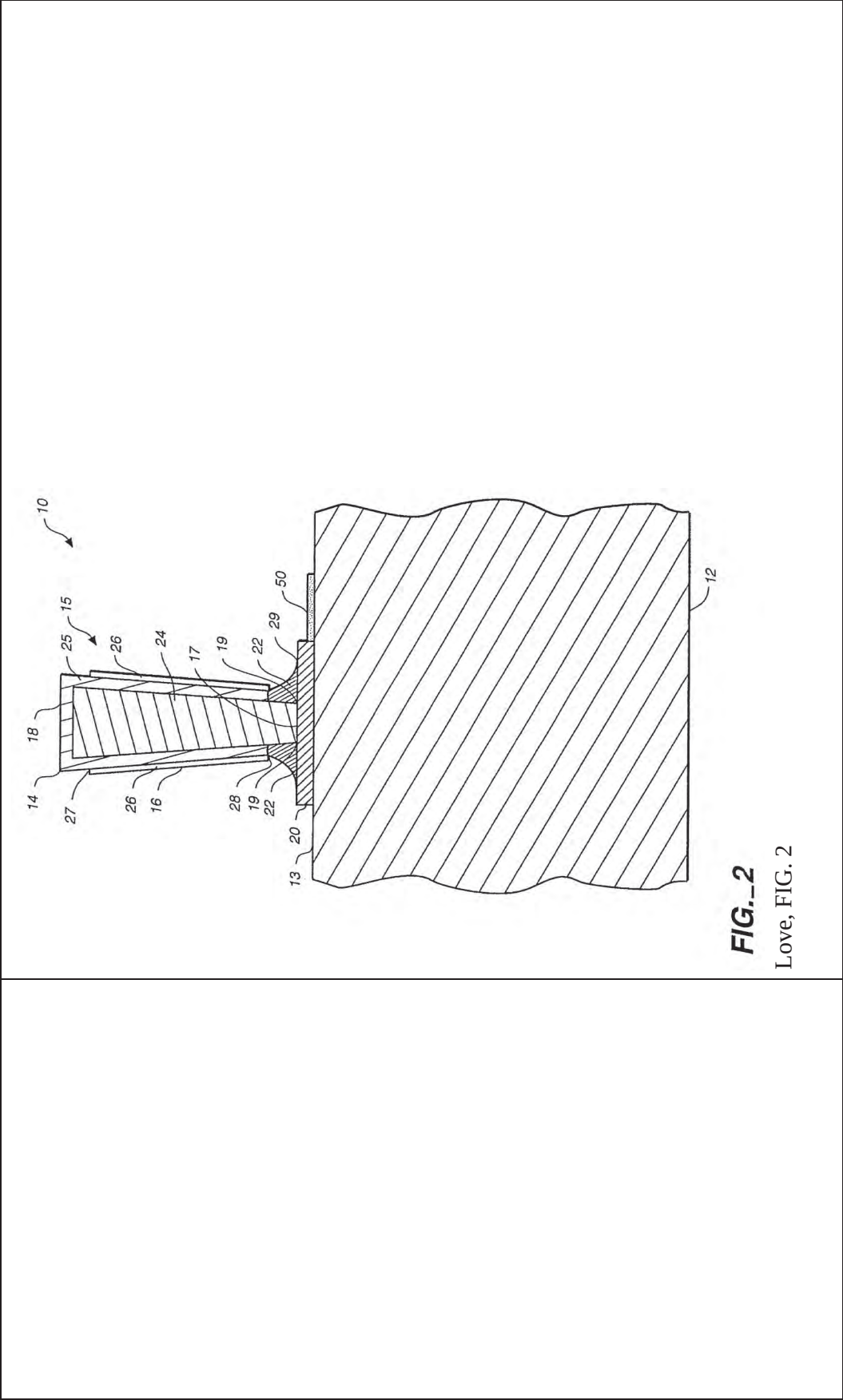
	<p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Love discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In a preferred embodiment of the present invention, the material of post 14 comprises copper. In a preferred embodiment of the present invention, top end 18 has a substantially flat surface which is substantially co-planar with surface 13. Also in a preferred embodiment, the body 16 of each post 14 of structure 10 is substantially circular in a cross-sectional plane co-planar with the surface of its top end 18.” Love, [7:3-7:11].</p> <p>“To couple post 14 to bump 80, both post 14 and bump 80 are heated to a temperature which causes the material of bump 80 to become reflowable, in the case of a solder material, or</p>

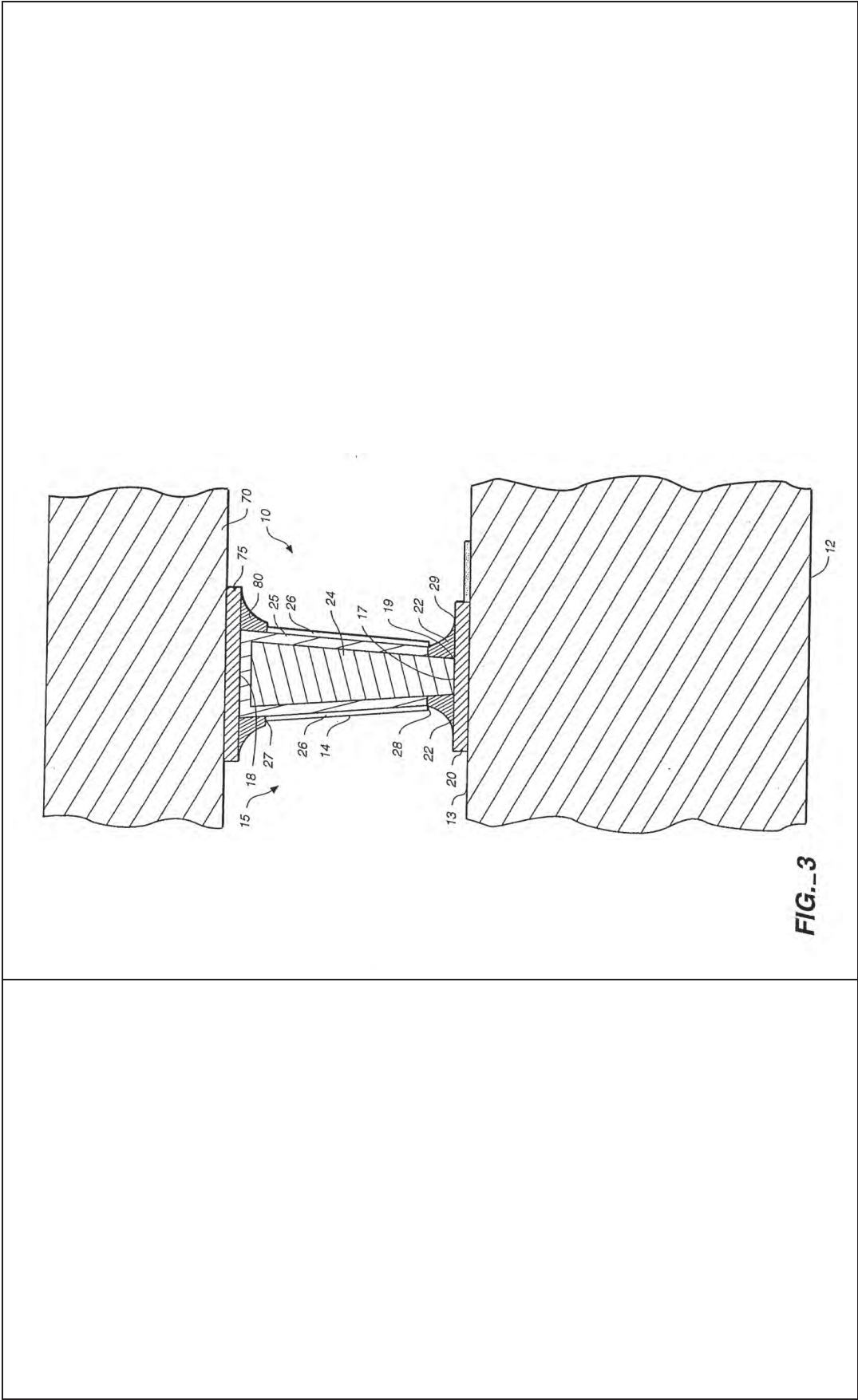
Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>pliable, in the case of a polymer material. Post 14 preferably comprises a material having a higher melting or reflow temperature point than the material of bump 80. During this heating process, chip 70 and substrate 12 are brought in close proximity to one another such that bump 80 makes contact with top end 18 of post 14. Light pressure, on the order of the weight of integrated circuit chip 70 (for example less than 0.5 N/cm.sup.2), is applied between substrate 12 and chip 70 during the contact process. Preferably, the heating process is performed in a forming gas atmosphere, such as 4% to 10% hydrogen in nitrogen, at a temperature exceeding the melting point of the material of bump 80. Once the melting temperature of the material of bump 80 is reached, bump 80 begins to reflow around post 14 near top end 18. Once reflowed, the temperature of substrate 12 and integrated circuit 70 is lowered to cause bump 80 to solidify around post 14, thereby making electrical mechanical coupling thereto." Love, [8:57-9:11].</p> <p>"FIG. 2 is a cross-sectional view of the wire interconnect structure shown in FIG. 1 taken along a vertical plane passing through the line 2--2 shown in FIG. 1. The reference numerals used in FIG. 1 are also used to show the same items in FIG. 2. FIG. 2 shows the features of post 14 in greater detail. In one embodiment of the present invention, post 14 further comprises an interior portion 24 of copper, a coating layer 25 of nickel surrounding interior portion 24, and a nickel oxide layer 26 disposed on nickel layer 25. Layer 25 may typically have a thickness of approximately one micron or less, and oxide layer 26 may have a thickness in the range of 0.1 microns to 0.2 microns. The thicknesses of these layers have been relatively enlarged in the Figures so that these layers may be more clearly shown. Nickel oxide layer 26 extends in the direction of elongation of body 16 from a point 28 near bottom end 17 of post 14 to a point 27 near top end 18 of post 14. As seen in FIG. 1, each of points 27 and 28 is intermediate between bottom end 17 and top end 18 of post 14, with point 28 being intermediate between point 27 and bottom end 17." Love, [9:12-9:32].</p>
--	--



Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

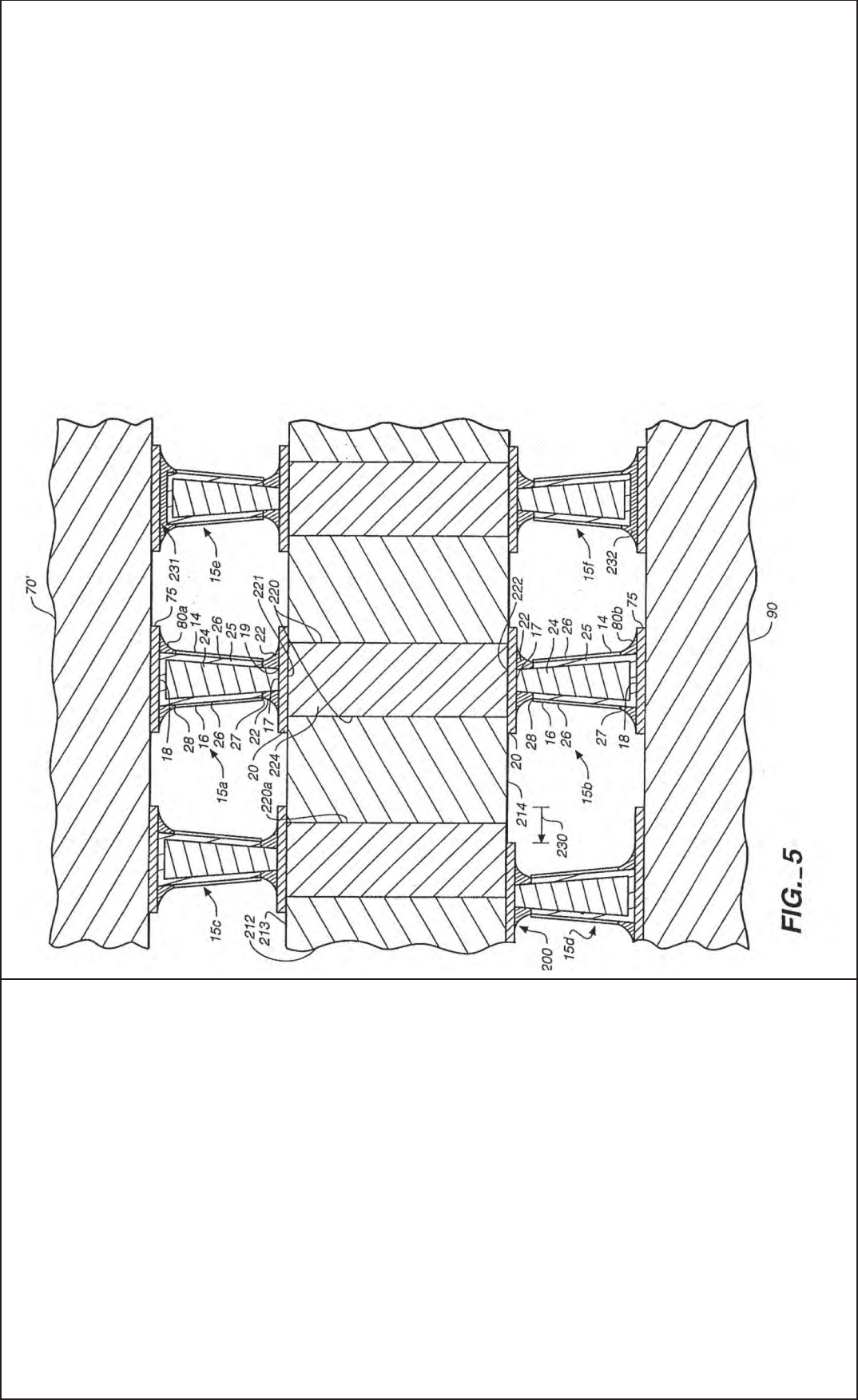
	<p>“FIG. 3, which shows a cross-section of wire interconnect structure 10, interconnect column 15, substrate 12 and IC chip 70 taken through a vertical plane lying along line 2--2 shown in FIG. 1. Bump 80 also reflows outwardly along the surface of IC chip 70. In one embodiment of the present invention, bump 80 comprises solder disposed on a circular conductive pad 75 of IC chip 70 having a diameter of about 25 microns. Pad 75 is surrounded by material which does not readily wet to solder. A non-wettable ring is thereby formed around pad 75, which forces the solder material to have a certain height (i.e., ball limiting metalization). For a 25 micron circular pad, this height is approximately 5 microns. Bump 80 may be deposited on IC chip 70 using any of the following standard methods of bump deposition well known in the art: lift-off, subtractive, additive, or shadow-mask vapor deposition.” Love, [10:25-10:42].</p>
--	--



	<p>Love, FIG. 3</p> <p>“FIG. 5 is a cross-sectional view of a second embodiment of the wire interconnect structure according to the present invention, which has been given the general reference designation of 200. The embodiment is referred to as wire interconnect structure 200 and is for electrically coupling a major substrate 90 to integrated circuit chip 70’, as shown in FIG. 5. Wire interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70’. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70’, and having a first surface 213 and a second surface 214. Interconnect substrate 212 is also referred to as an interposer substrate or an intermediate substrate because it is disposed between substrate 90 and chip 70’. Wire interconnect structure 200 further comprises a first interconnect column 15a on surface 213 constructed according to the first embodiment of the present invention shown in FIGS. 1-3, and a second interconnect column 15b on surface 214, also constructed according to the first embodiment of the present invention. Each of the interconnect columns 15a and 15b comprises a post 14 with elongated body 16 and ends 17 and 18, a base pad 20, a fillet 22, and a peripheral edge 19, as described above. Additionally, post 14 comprises an interior portion 24, a coating layer 25, and an oxide layer 26, all as described above. The reference numerals used in describing interconnect column 15 shown in FIGS. 1-3 have been used for interconnect columns 15a and 15b of FIG. 5. First interconnect column 15a is disposed on first surface 213 of substrate 212 such that its bottom end 17 and base pad 20 are mounted to surface 213. First interconnect column 15a is for making contact to IC chip 70’. In a similar manner, second interconnect column 15b is disposed on second surface 214 of substrate 212, such that its bottom end 17 and base pad 20 are mounted to second surface 214. Second interconnect column 15b is for making contact to major substrate 90. Interconnect structure 200 further comprises a coupling means for electrically coupling first interconnect column 15a to second interconnect column 15b. In a preferred embodiment of</p>
--	---

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>the present invention, the coupling means comprises a through hole 220 passing through substrate 212 between first surface 213 and second surface 214, which is filled with a plug of conductive material 224. Through hole 220 includes a first end 221 next to base pad 20 and bottom end 17 of interconnect column 15a, and a second end 222 next to the base pad 20 and bottom end 17 of second interconnect column 15b. Plug 224 preferably comprises a metal, such as copper, or metal alloy which is formed within through hole 220. Plug 224 makes electrical contact to corresponding pads 20 of each of interconnect columns 15a and 15b and forms a conductive path therebetween, thereby electrically coupling columns 15a and 15b to one another.” Love, [12:4-12:59].</p>
--	--



Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>Love, FIG. 5</p> <p>“Also in a preferred embodiment of interconnect structure 200, the posts of interconnect columns 15a and 15b are disposed substantially opposite to one another at respective opposite ends of through hole 220 to facilitate the electrical connection therebetween. However, it may be appreciated that the interconnect columns may be somewhat offset from an exact opposing relationship, as shown, for example, by two interconnect columns 15c and 15d in FIG. 5. Interconnect column 15c is disposed on surface 213 and interconnect column 15d is disposed on surface 214. Interconnect columns 15c and 15d are disposed at opposite ends of a through hole 220a, with an offset 230 in the placement of interconnect column 15d.” Love, [13:12-13:25].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

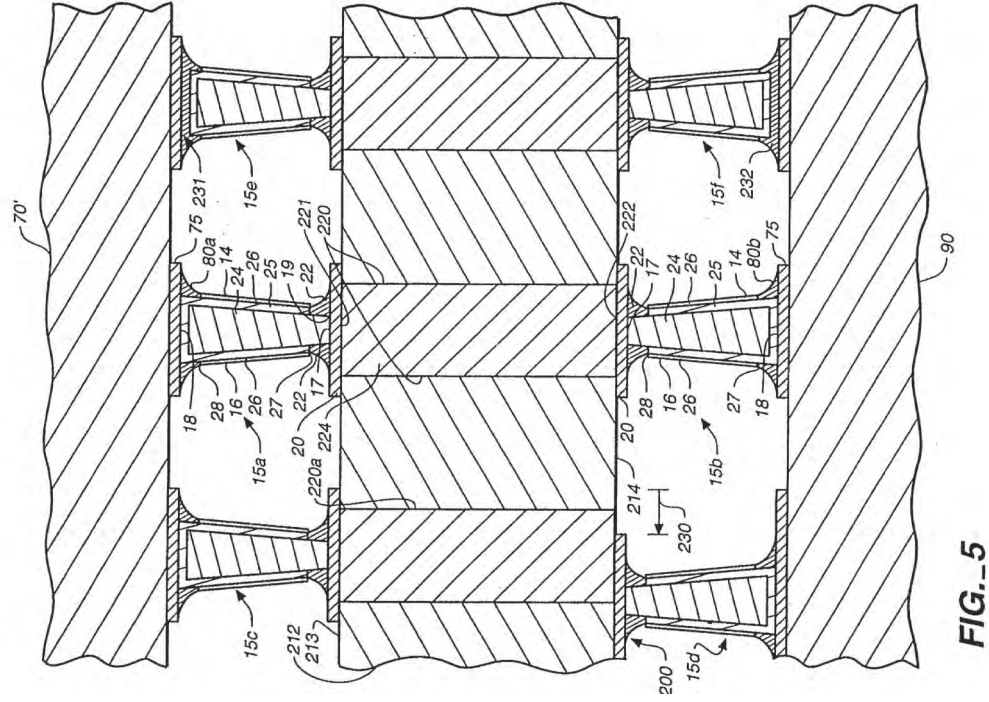
Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom end of a corresponding metal pillar among the plurality of metal pillars,</p>	<p>Love discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom</p>

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

<p>the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In a preferred embodiment of the present invention, interconnect column 15 further comprises a base pad 20 disposed between surface 13 and bottom end 17 of post 14. Base pad 20 is mounted to surface 13, and bottom end 17 of post 14 is mounted to base pad 20. Preferably, base pad 20 comprises a metallic material, such as copper, nickel, cobalt, gold, or palladium. As described below in greater detail, base pad 20 facilitates the construction of post 14 by electroless or electrolytic plating, and preferably the top layer of base pad 20 comprises the same material as that of post 14.” Love, [7:32-7:42].</p> <p>“This aids in the above-described alignment of chip 70' and array 100 by surface tension forces since it provides a large surface area for top end 18 while making it easier for post 14 to be flexed near the bottom of the post by the surface tension forces applied at top end 18. (The tapered shape, along with leverage effects, allows post 14 to flex more near the middle and bottom than the top.) Such flexing helps to bring an interconnect column 15 and its corresponding bump 80 into closer alignment in cases where they initially are not well centered (i.e., aligned). FIG. 5 is a cross-sectional view of a second embodiment of the wire interconnect structure according to the present invention, which has been given the general reference designation of 200. The embodiment is referred to as wire interconnect structure 200 and is for electrically coupling a major substrate 90 to integrated circuit chip 70', as shown in FIG. 5. Wire interconnect structure 200 may be used for coupling electrical signals and power between major substrate 90 and IC chip 70'. Wire interconnect structure 200 comprises an interconnect substrate 212 disposed intermediate between major substrate 90 and IC chip 70', and having a first surface 213 and a second surface 214. Interconnect</p>
---	---

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>substrate 212 is also referred to as an interposer substrate or an intermediate substrate because it is disposed between substrate 90 and chip 70'. Wire interconnect structure 200 further comprises a first interconnect column 15a on surface 213 constructed according to the first embodiment of the present invention shown in FIGS. 1-3, and a second interconnect column 15b on surface 214, also constructed according to the first embodiment of the present invention. Each of the interconnect columns 15a and 15b comprises a post 14 with elongated body 16 and ends 17 and 18, a base pad 20, a fillet 22, and a peripheral edge 19, as described above. Additionally, post 14 comprises an interior portion 24, a coating layer 25, and an oxide layer 26, all as described above. The reference numerals used in describing interconnect column 15 shown in FIGS. 1-3 have been used for interconnect columns 15a and 15b of FIG. 5. First interconnect column 15a is disposed on first surface 213 of substrate 212 such that its bottom end 17 and base pad 20 are mounted to surface 213. First interconnect column 15a is for making contact to IC chip 70'. In a similar manner, second interconnect column 15b is disposed on second surface 214 of substrate 212, such that its bottom end 17 and base pad 20 are mounted to second surface 214." Love, [11:60-12:41].</p>
--	---



	<p>Love, FIG. 5</p> <p>“Interconnect structure 200 further comprises a coupling means for electrically coupling first interconnect column 15a to second interconnect column 15b. In a preferred embodiment of the present invention, the coupling means comprises a through hole 220 passing through substrate 212 between first surface 213 and second surface 214, which is filled with a plug of conductive material 224. Through hole 220 includes a first end 221 next to base pad 20 and bottom end 17 of interconnect column 15a, and a second end 222 next to the base pad 20 and bottom end 17 of second interconnect column 15b. Plug 224 preferably comprises a metal, such as copper, or metal alloy which is formed within through hole 220. Plug 224 makes electrical contact to corresponding pads 20 of each of interconnect columns 15a and 15b and forms a conductive path therebetween, thereby electrically coupling columns 15a and 15b to one another.” Love, [12:42-12:59].</p> <p>“At block 306, a base pad 20 for each interconnect column 15a and 15b is formed. For each side of substrate 212, the following steps are performed. First, a seed layer of copper is sputtered on each surface of substrate 212. Preferably, the seed layer may comprise an initial thin layer of chromium followed by a thin layer of copper (Cr/Cu), may comprise an initial thin layer of titanium followed by a thin layer of copper Ti/Cu), or may comprise a titanium-tungsten alloy layer (50%--50%) followed a layer of copper (Ti--W/Cu). Prior to depositing the seed layer, the surfaces of substrate 212 are cleaned well so as to activate these surfaces for the sputtered seed layer. Second, a photoresist (PR) layer is applied to each substrate side, and portions of the photoresist are removed where pads 20 are to be formed (e.g., exposing the photoresist to UV light through a mask and developing). This exposes the seed layer where pads 20 are to be formed. Third, copper is electroplated onto the exposed areas of the seed layer to a desired thickness, of for example about 1 micron, to form pads 20. The photoresist is then removed. The appearance of substrate 212 and pads 20 at the end of these</p>
--	--

Appendix A-24 - Invalidity of U.S. Patent No. 9859202 in view of Love - U.S. Patent No. 5334804

	<p>steps is shown at a partial cross-section 306A of substrate 212 in FIG. 6A-2.” Love, [14:56-15:12].</p> <p>“In a preferred embodiment of the present invention, interconnect column 415 further comprises a base pad 20 and a base pedestal 21. Base pad 20 is mounted to surface 413 and disposed between surface 413 and base pedestal 21. Base pedestal 21 is mounted to base pad 20 and disposed between base pad 20 and bottom end 17 of post 14. Bottom end 17 of post 14 is mounted to base pedestal 21. Preferably, each of base pad 20 and base pedestal 21 comprises a metallic material, such as copper, nickel, cobalt, gold, or palladium.” Love, [19:24-19:33].</p> <p>“In a preferred embodiment of interconnect column 415, a fillet 22 of rigid material is disposed along peripheral edge 19. Fillet 22 preferably comprises a solder. An exemplary solder for fillet 22 is an alloy of tin and lead, such as 60/40 (tin/lead). Fillet 22 contacts the outer portions of base pad 20, outer portions of base pedestal 21, and portions of post 14 near bottom end 17, as shown in FIG. 7. Fillet 22 has an outside surface extending between post 14 and base pad 20 which may be “S”-shaped. Fillet 22 extends up post 14 from end 17 to substantially point 28. Fillet 22 extends outward from pedestal 21 onto base pad 20 to a point 29. Fillet 22 preferably is disposed in (i.e., fills in) the corner formed between pedestal 21 and base pad 20.” Love, [19:64-20:11].</p> <p>To the extent Plaintiff contends that Love fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

U.S. Patent Publication No. 20130127054 (“Muthukumar”) is titled Stacked-Chip Packages in Package-on-Package Apparatus, Methods of Assembling Same, and Systems Containing Same and lists Sriram Muthukumar and Charles A. Gealer as inventors. Muthukumar anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Muthukumar is a U.S. patent publication that was filed January 14, 2013 and published May 23, 2013. Muthukumar claims priority to US 12/459,226 filed on June 26, 2009. Muthukumar is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Muthukumar, or otherwise rendered obvious by disclosures and teachings of Muthukumar, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Muthukumar does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Muthukumar with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Muthukumar, either alone or in combination with other prior art cited by Samsung and/or with the

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Muthukumar “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Muthukumar or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Muthukumar set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Muthukumar discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 a is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless</p>

communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].

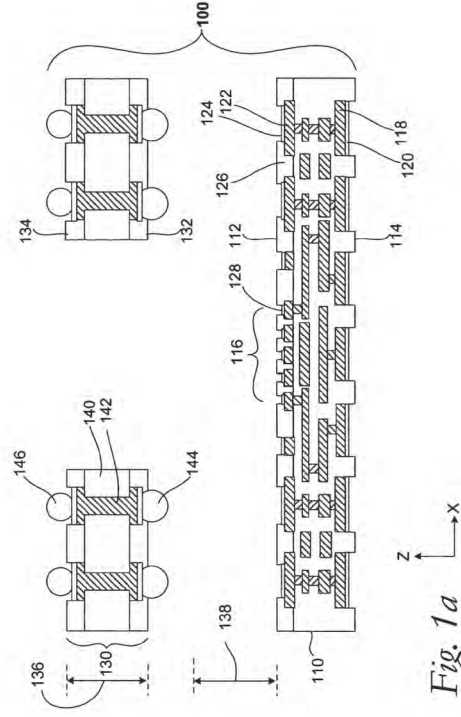


Fig. 1a

Muthukumar, Fig. 1a

“The apparatus 100 is assembled with the interposer 130 that mates to the die-side ball grid array 122. The interposer 130 includes a die side 132 and a top side 134 and has an offset height 136 configured to match an offset height 138 above the package substrate 110 for a multiple die stack (MDS) that will occupy the bottom-chip footprint 116. The interposer 130 may include a core 140 and interconnects 142. In an embodiment, die-side electrical bumps 144 and top-side electrical bumps 146 are coupled to the interconnects 142.” Muthukumar, [0026].

“The apparatus 101 illustrates that the interposer offset height 136 matches the package-substrate offset height 138 (FIG. 1 a). The bottom-chip footprint 116 is surrounded by the interposer 130 and will surround the multiple-die stack that is to be assembled as part of the apparatus 101.” Muthukumar, [0027].

“A bottom chip 150 is placed within the bottom-chip footprint 116 (FIG. 1 b). In an embodiment, the bottom chip 150 is a flip chip 150 that has been flip-chip bonded though a chip ball array, one electrical bump of which is referenced with numeral 152. In an embodiment, an underfill 154 has been flowed to fortify bonding between the bottom chip 150 and the package substrate 110. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the underfill 154. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the fill material 148.” Muthukumar, [0029].

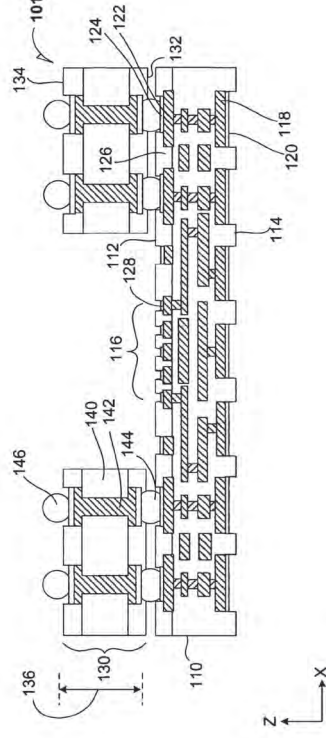


Fig. 1b

	<p>Muthukumar, Fig. 1b</p> <p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>
--	--

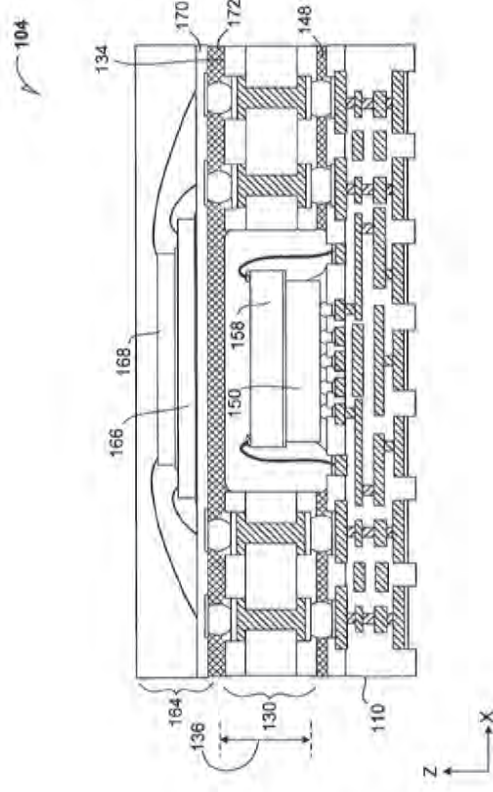


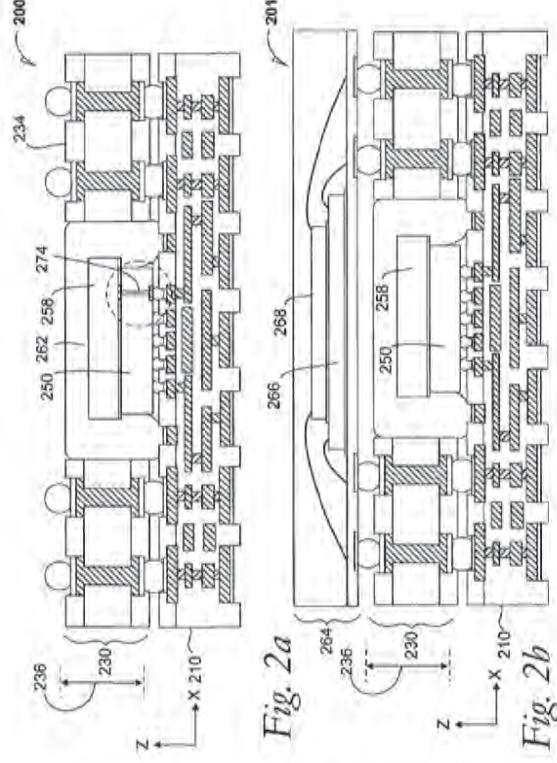
Fig. 1e

Muthukumar, Fig. 1e

“It can be seen that the mixed stack of the bottom chip 150 and top chip 158 have been accommodated by the interposer offset 136 such that the top package 164 does not interfere with the mixed stack. Consequently, the PoP stacked-chip apparatus is assembled with sufficient interposer offset 136 to accommodate an offset height of the chip stack that may vary depending upon a specific application.” Muthukumar, [0037].

“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset

236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].



Muthukumar, Figs. 2a, 2b

“In an embodiment, the bottom chip 150 is a processor and the top chip 158 is a radio-frequency (RF) device.” Muthukumar, [0054].

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

<p>[1.A] a bottom package substrate;</p>	<p>Muthukumar discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“A bottom chip 150 is placed within the bottom-chip footprint 116 (FIG. 1 b). In an embodiment, the bottom chip 150 is a flip chip 150 that has been flip-chip bonded though a chip ball array, one electrical bump of which is referenced with numeral 152. In an embodiment, an underfill 154 has been flowed to fortify bonding between the bottom chip 150 and the package substrate 110. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the underfill 154. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the fill material 148.” Muthukumar, [0029].</p>
---	---

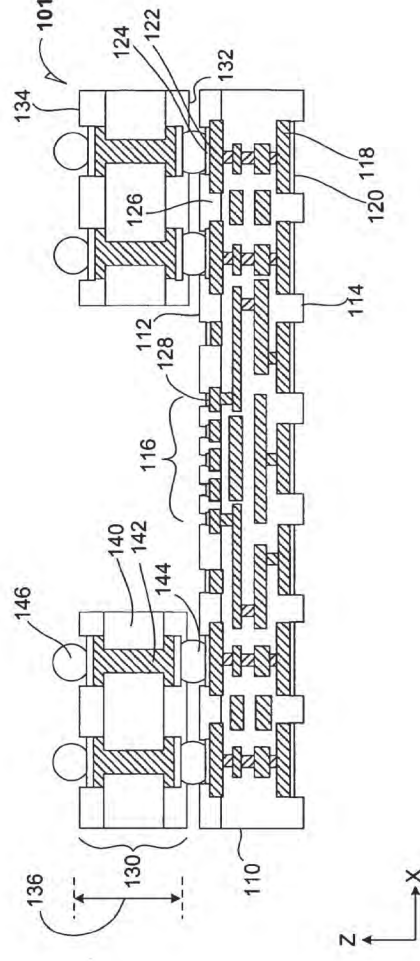
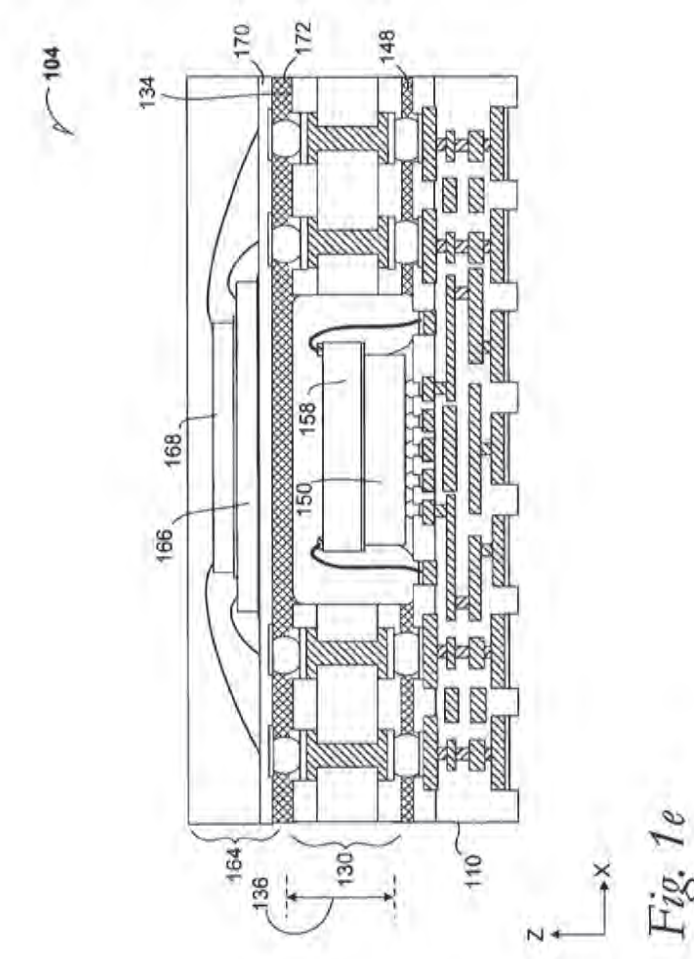


Fig. 16

Muthukumar, Fig. 1b

“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as

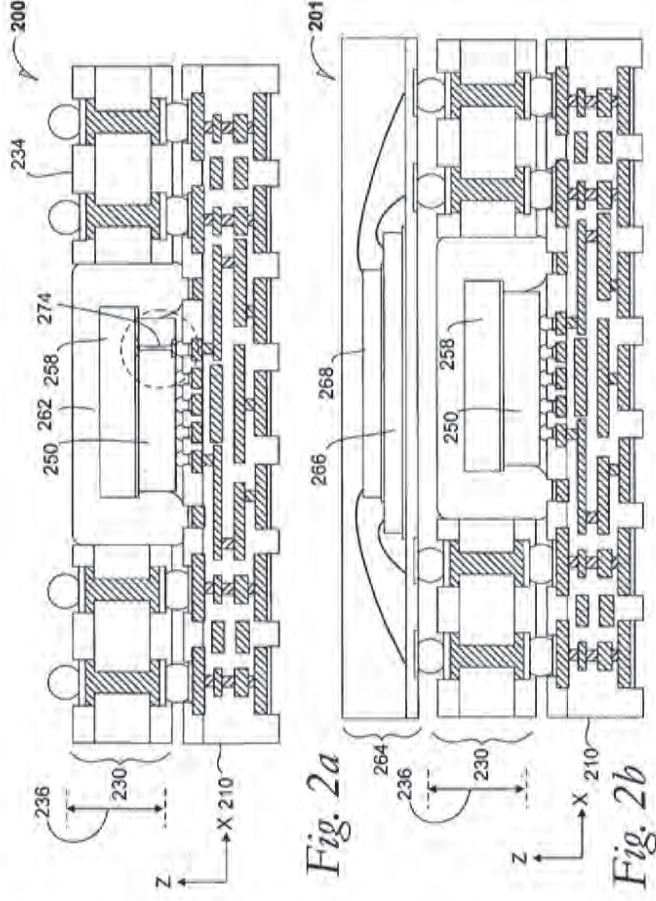
for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].



Muthukumar, Fig. 1e

“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset

236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].



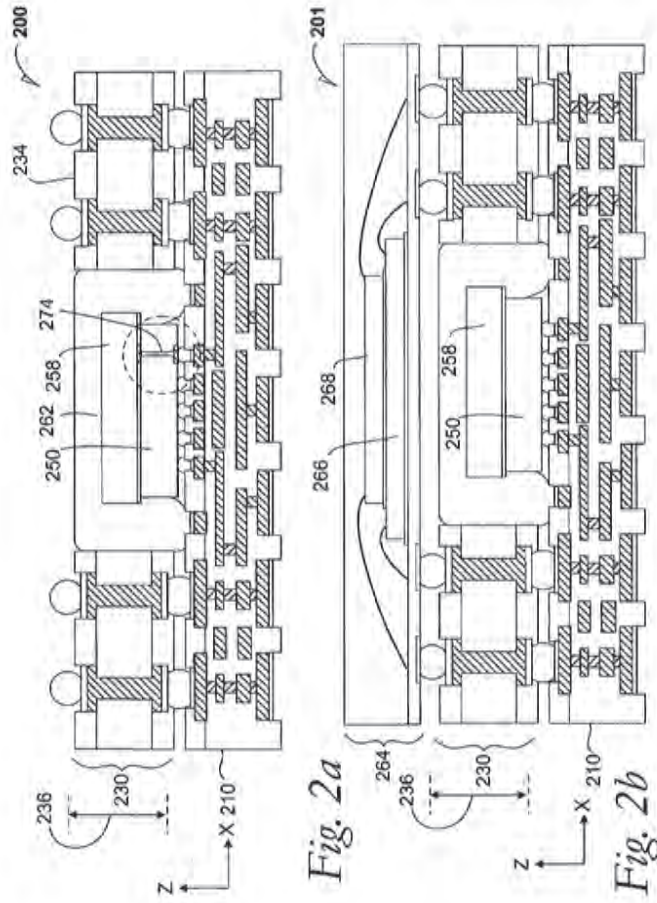
Muthukumar, Figs. 2a, 2b

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Muthukumar discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>

	<div><p>A cross-sectional diagram of a PoP stacked-chip apparatus 201. The diagram shows a top chip 250 and a bottom chip 236 stacked vertically. The bottom chip 236 is mounted on a mounting substrate 270. The top chip 250 is mounted on the bottom chip 236. Various layers and components are labeled with reference numerals: 110, 130, 136, 164, 166, 168, 170, 172, 148, 150, 158. A coordinate system with x and z axes is shown at the bottom left. A bracket labeled 104 is at the top left.</p></div> <div><p><i>Fig. 1e</i></p></div> <div><p>Muthukumar, Fig. 1e</p></div> <div><p>“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250</p></div>
--	---

and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].



Muthukumar, Figs. 2a, 2b

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Muthukumar discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].</p>

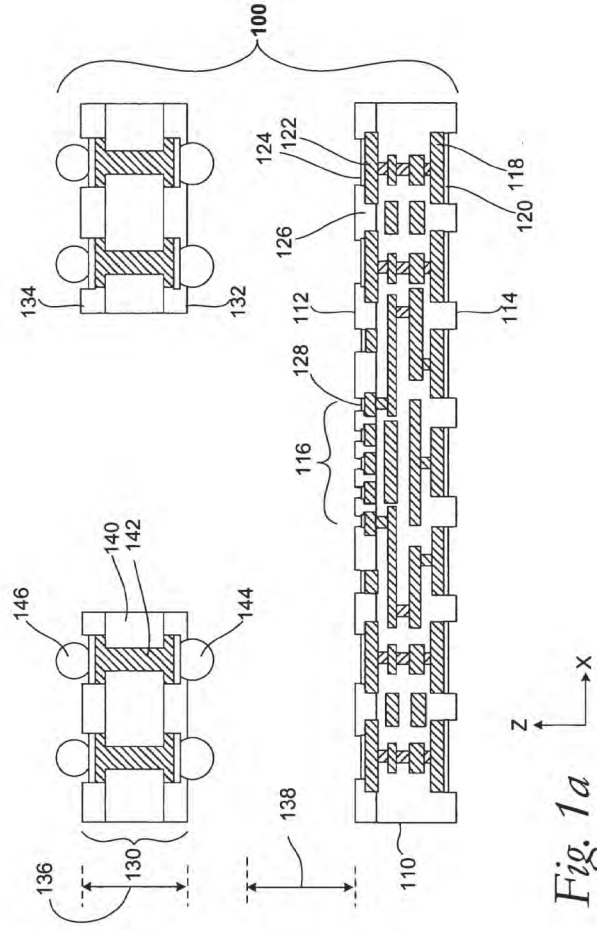


Fig. 1a

Muthukumar, Fig. 1a

“The apparatus 100 is assembled with the interposer 130 that mates to the die-side ball grid array 122. The interposer 130 includes a die side 132 and a top side 134 and has an offset height 136 configured to match an offset height 138 above the package substrate 110 for a multiple die stack (MDS) that will occupy the bottom-chip footprint 116. The interposer 130 may include a core 140 and interconnects 142. In an embodiment, die-side electrical bumps 144 and top-side electrical bumps 146 are coupled to the interconnects 142.” Muthukumar, [00026].

“A bottom chip 150 is placed within the bottom-chip footprint 116 (FIG. 1 b). In an embodiment, the bottom chip 150 is a flip chip 150 that has been flip-chip bonded though a chip ball array, one electrical bump of which is referenced with numeral 152. In an embodiment, an underfill 154 has been flowed to fortify bonding between the bottom chip 150 and the package substrate 110. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the underfill 154. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the fill material 148.” Muthukumar, [0029].

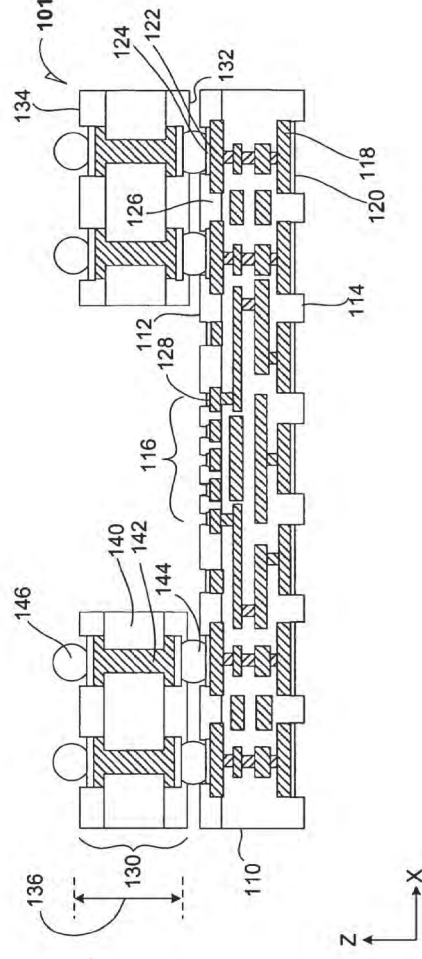
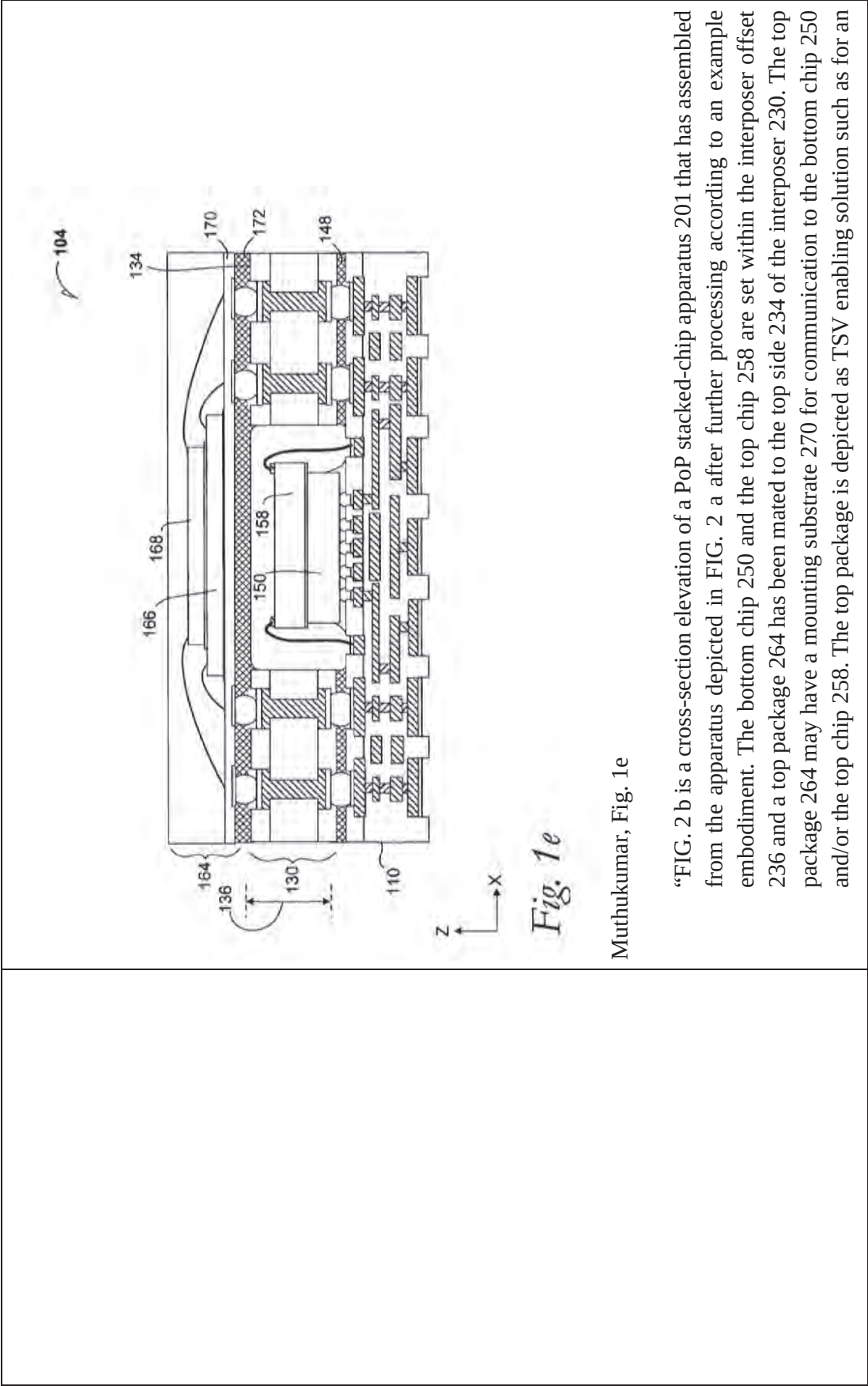
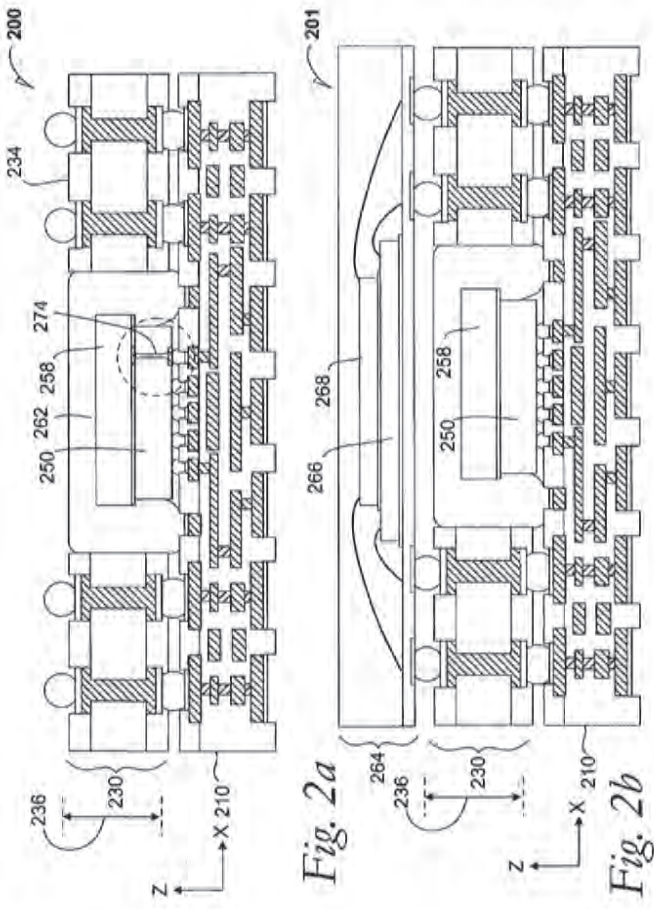


Fig. 1b

Muthukumar, Fig. 1b

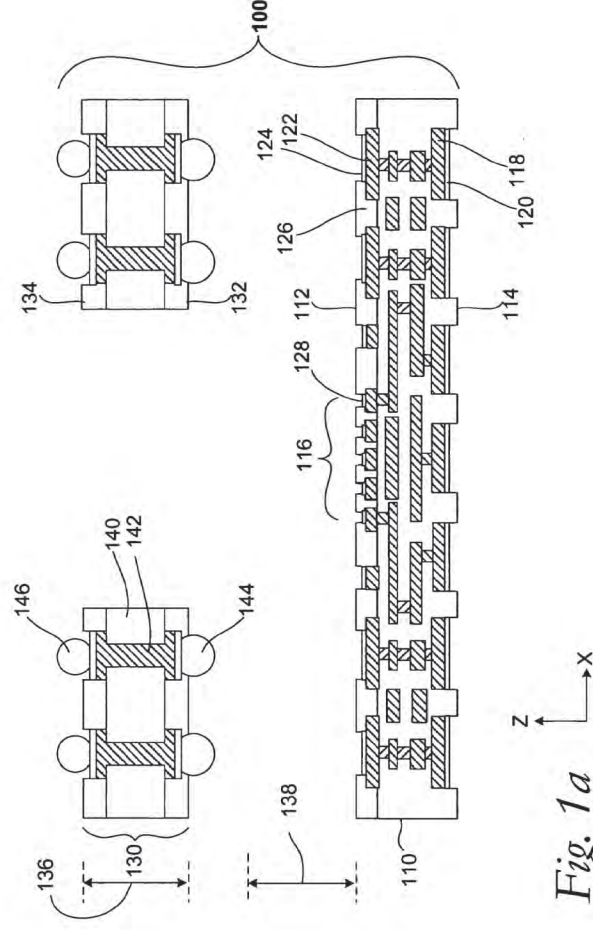
	<p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>
--	---



	<p>original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].</p>  <p>Muthukumar, Figs. 2a, 2b</p> <p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Muthukumar discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 a is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].</p>



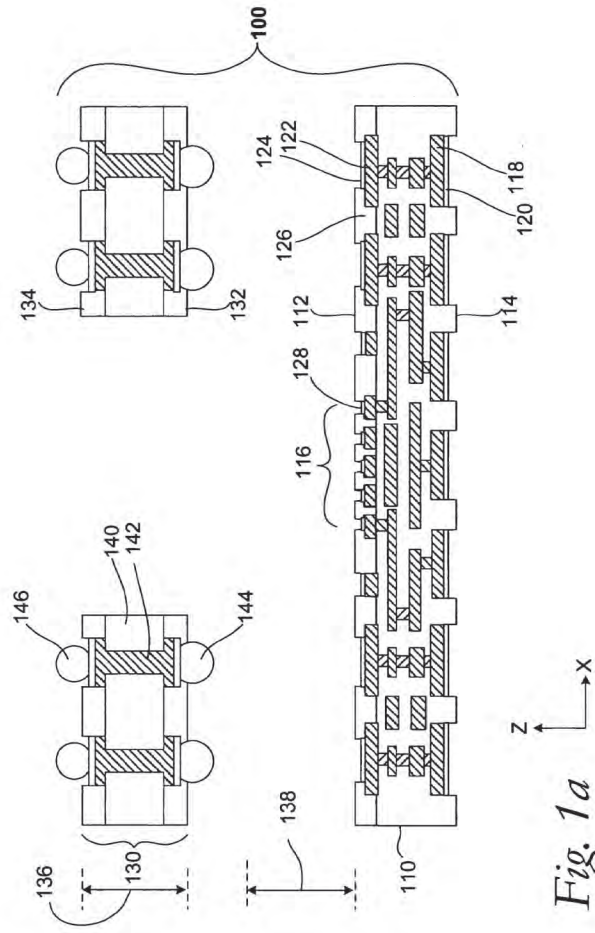
Muthukumar, Fig. 1a

To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.E] a plurality of metal pillars, each passing through the core substrate; and

Muthukumar discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.

	<p><i>See, e.g.:</i></p> <p>“FIG. 1 a is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].</p>
--	---

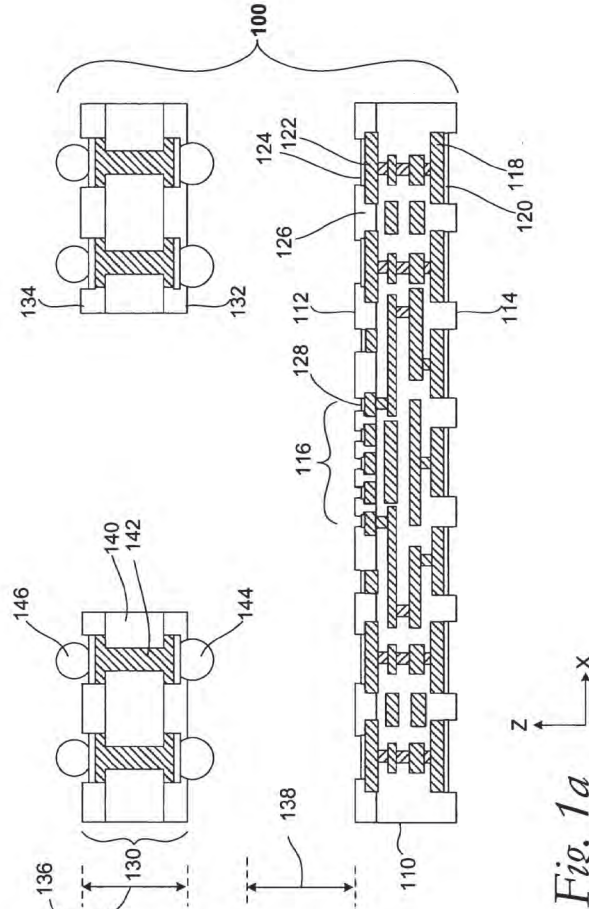


Muthukumar, Fig. 1a

“The apparatus 100 is assembled with the interposer 130 that mates to the die-side ball grid array 122. The interposer 130 includes a die side 132 and a top side 134 and has an offset height 136 configured to match an offset height 138 above the package substrate 110 for a multiple die stack (MDS) that will occupy the bottom-chip footprint 116. The interposer 130 may include a core 140 and interconnects 142. In an embodiment, die-side electrical bumps 144 and top-side electrical bumps 146 are coupled to the interconnects 142.” Muthukumar, [0026].

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Muthukumar discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 a is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].</p>

	 <p><i>Fig. 1a</i></p> <p>Muthukumar, Fig. 1a</p> <p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars</p>	<p>Muthukumar discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p>

protrudes downwardly from a bottom surface of the core substrate,	<p><i>See, e.g.:</i></p> <p>“FIG. 1 a is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].</p>
---	---

Fig. 1a

Muthukumar, Fig. 1a

“The apparatus 100 is assembled with the interposer 130 that mates to the die-side ball grid array 122. The interposer 130 includes a die side 132 and a top side 134 and has an offset height 136 configured to match an offset height 138 above the package substrate 110 for a multiple die stack (MDS) that will occupy the bottom-chip footprint 116. The interposer 130 may include a core 140 and interconnects 142. In an embodiment, die-side electrical bumps 144 and top-side electrical bumps 146 are coupled to the interconnects 142.” Muthukumar, [0026].

	<p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>
--	---

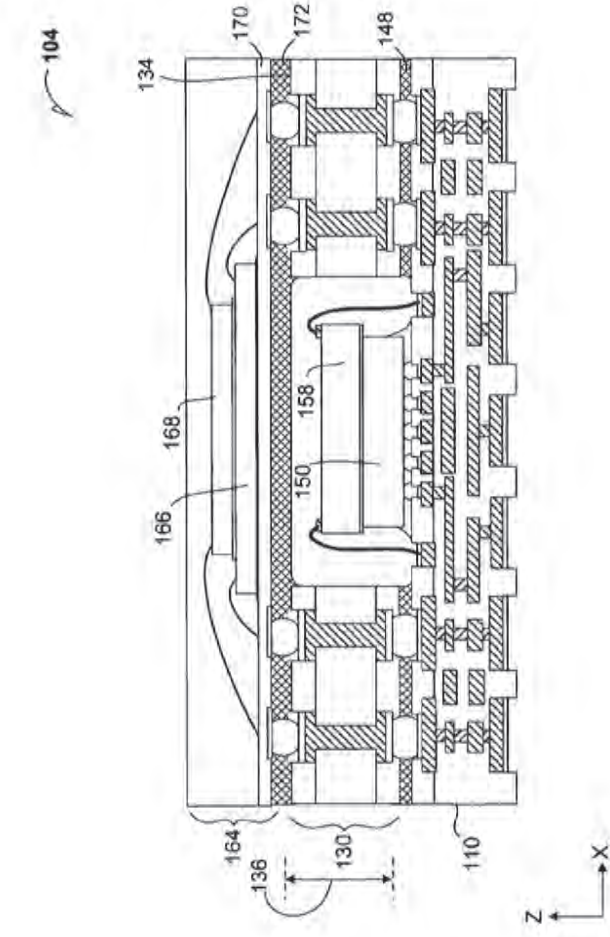
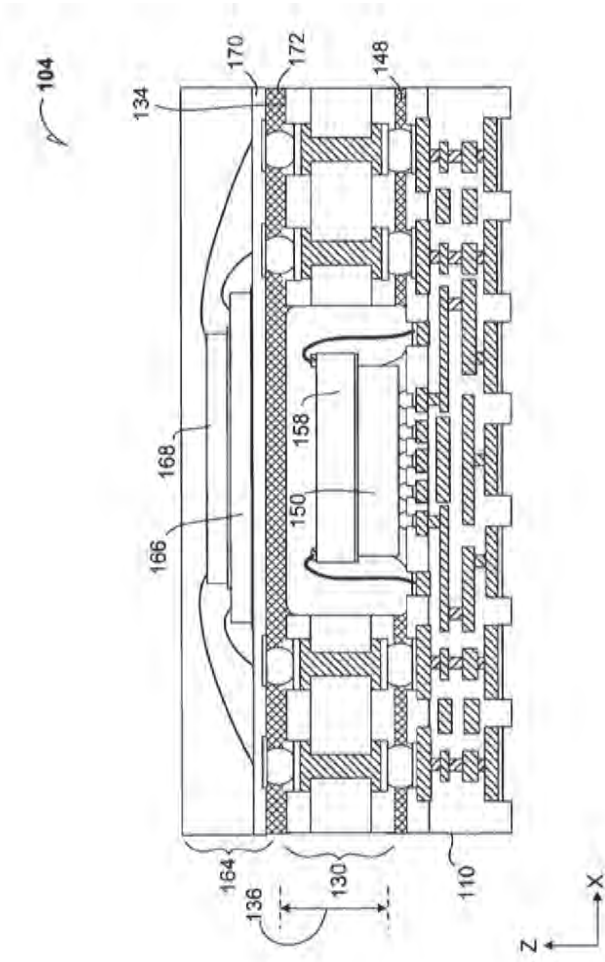


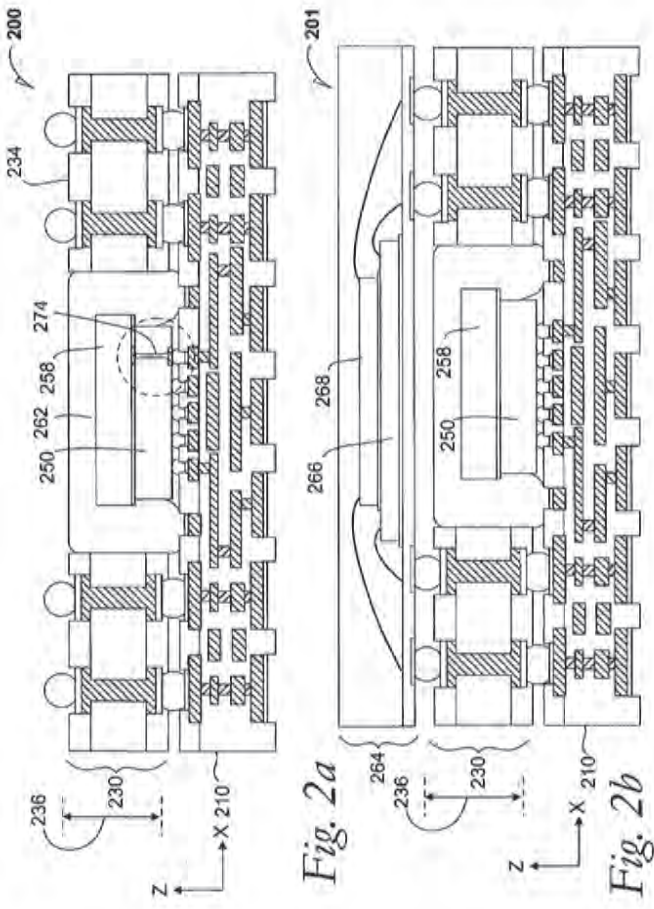
Fig. 1e

Muthukumar, Fig. 1e

To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

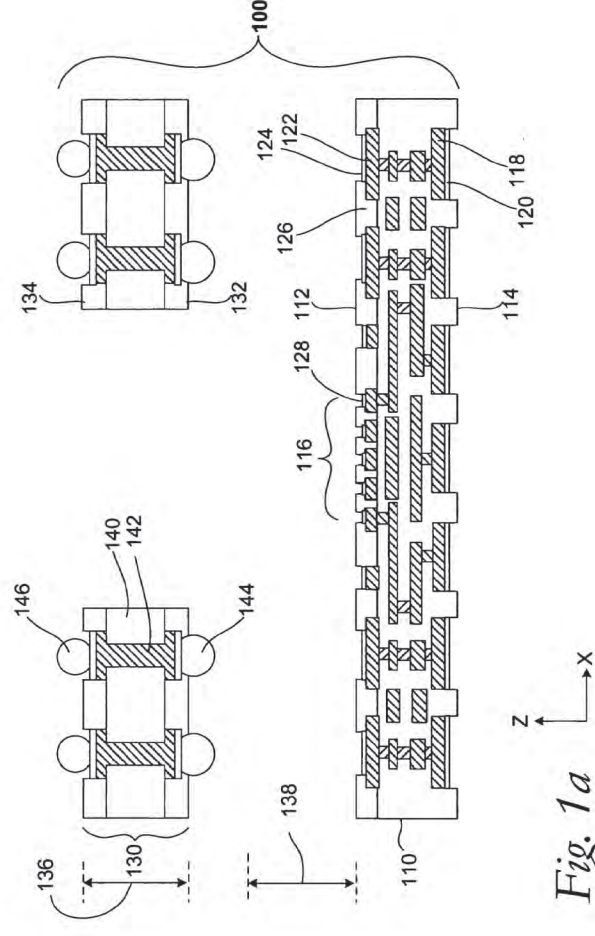
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Muthukumar discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>
--	--

	<div><p>A cross-sectional diagram of a PoP stacked-chip apparatus 201. The diagram shows a top chip 236 and a top package 264 mounted on a mounting substrate 270. The top chip 236 is connected to the top package 264 via a top side 234 of an interposer 230. The top package 264 is connected to the mounting substrate 270 via a bottom chip 250 and the top chip 258. The top chip 258 is set within the interposer 230. The top package 264 has a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an</p></div> <div><p><i>Fig. 1e</i></p></div> <div><p>Muthukumar, Fig. 1e</p></div>
--	---

	<p>original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].</p>  <p>Muthukumar, Figs. 2a, 2b</p> <p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

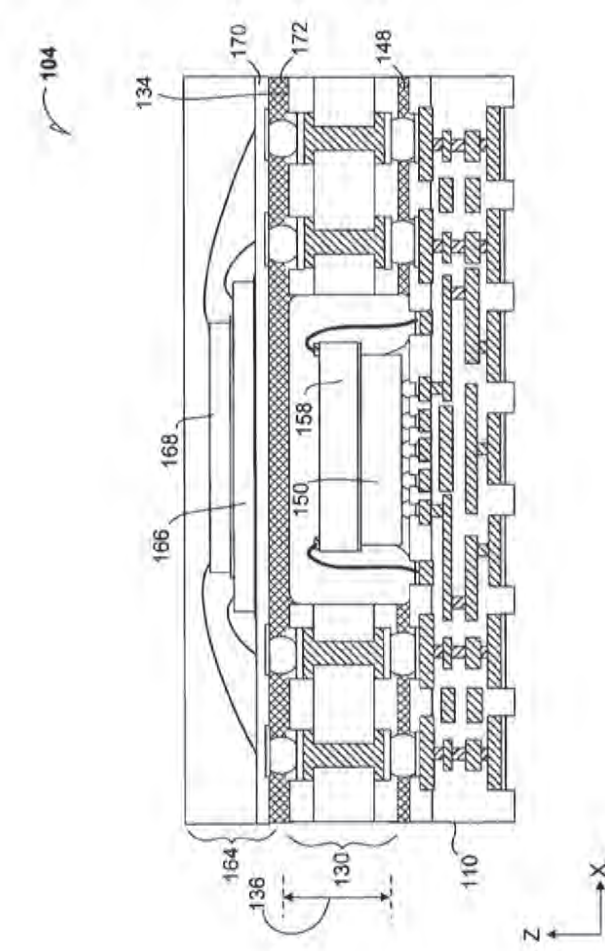
Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Muthukumar discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].</p>

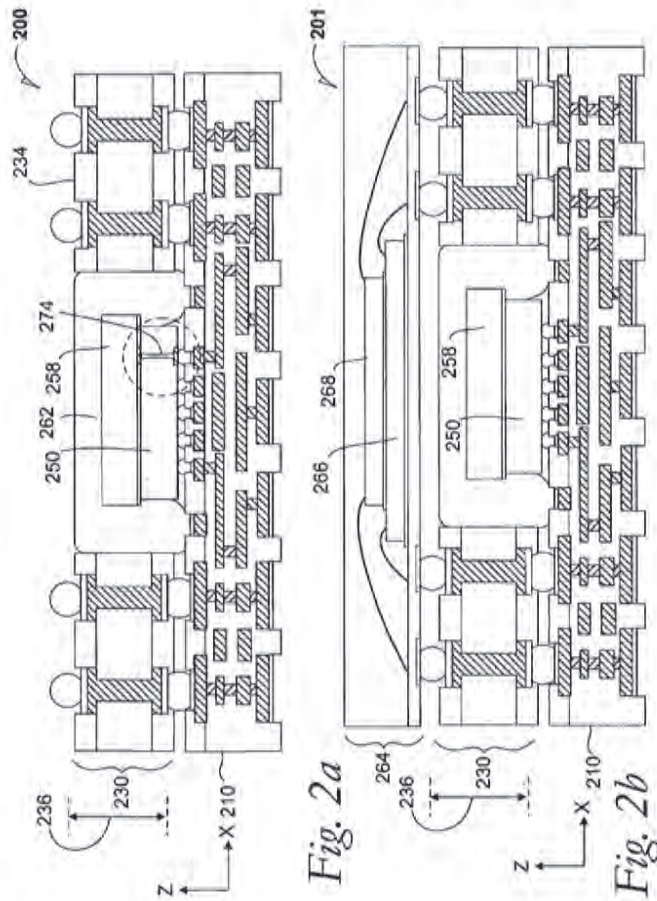


Muthukumar, Fig. 1a

“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package

	<p>164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>  <p><i>Fig. 1e</i></p> <p>Muthukumar, Fig. 1e</p>
--	--

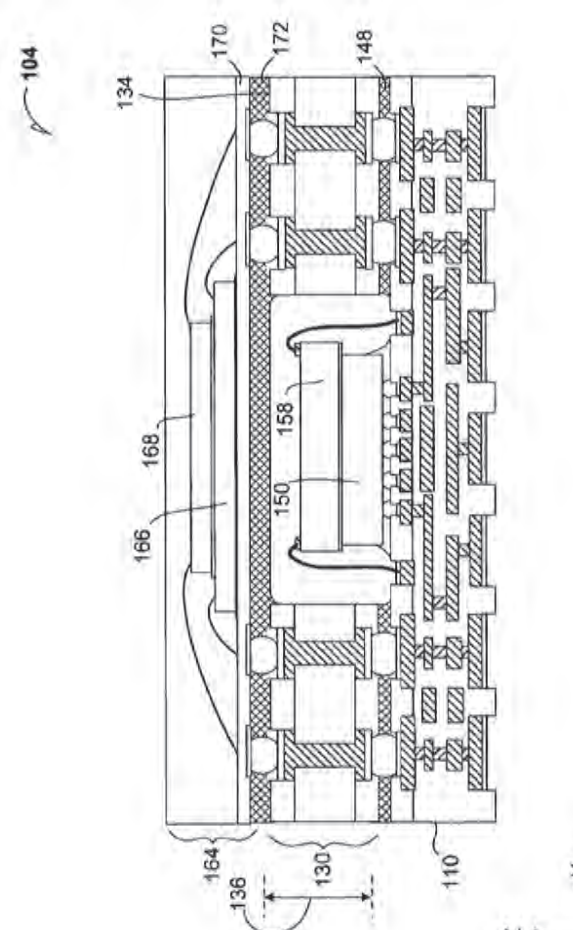
	<p>“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.”</p> <p>Muthukumar, [0044].</p>
--	--

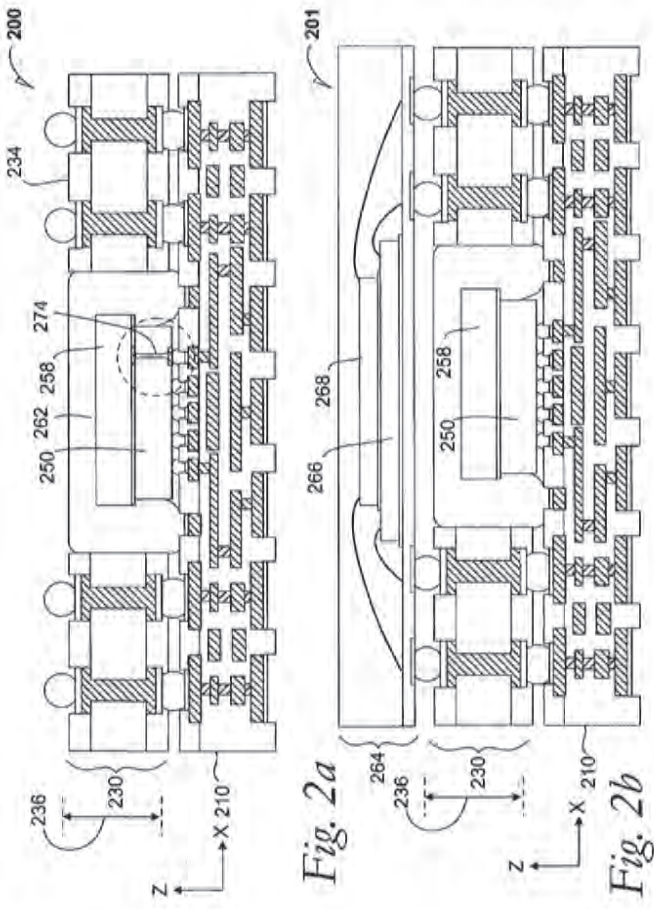


Muthukumar, Figs. 2a, 2b

To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Muthukumar discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>
--	---

	<div><p>A cross-sectional diagram of a PoP stacked-chip apparatus 201. The diagram shows a top chip 236 and a top package 264 mounted on a mounting substrate 270. The top chip 236 is connected to the top package 264 via a top side 234 of an interposer 230. The top package 264 is connected to the mounting substrate 270 via a bottom chip 250 and the top chip 258. The top chip 258 is set within the interposer 230. The top package 264 has a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an</p><p>Fig. 1e</p></div> <p>Muthukumar, Fig. 1e</p>
--	---

	<p>original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].</p>  <p>Muthukumar, Figs. 2a, 2b</p> <p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Muthukumar discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“The apparatus 101 illustrates that the interposer offset height 136 matches the package-substrate offset height 138 (FIG. 1 a). The bottom-chip footprint 116 is surrounded by the interposer 130 and will surround the multiple-die stack that is to be assembled as part of the apparatus 101.” Muthukumar, [0027].</p> <p>“A bottom chip 150 is placed within the bottom-chip footprint 116 (FIG. 1 b). In an embodiment, the bottom chip 150 is a flip chip 150 that has been flip-chip bonded through a chip ball array, one electrical bump of which is referenced with numeral 152. In an embodiment, an underfill 154 has been flowed to fortify bonding between the bottom chip 150 and the package substrate 110. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the underfill 154. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the fill material 148.” Muthukumar, [0029].</p>

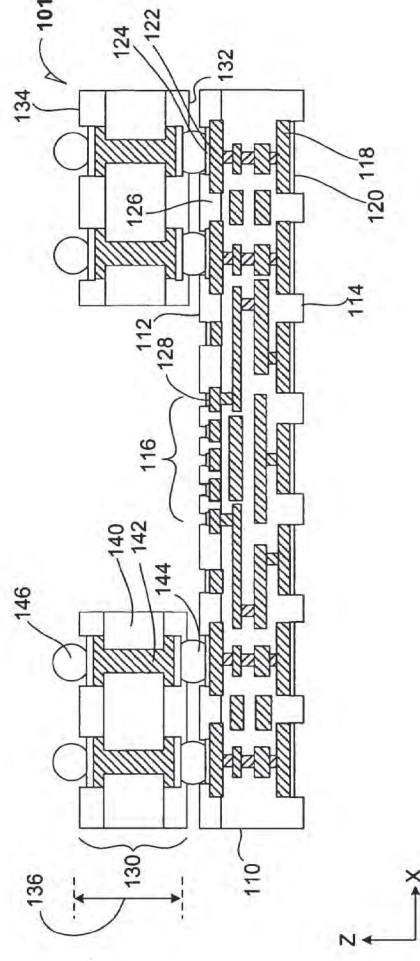
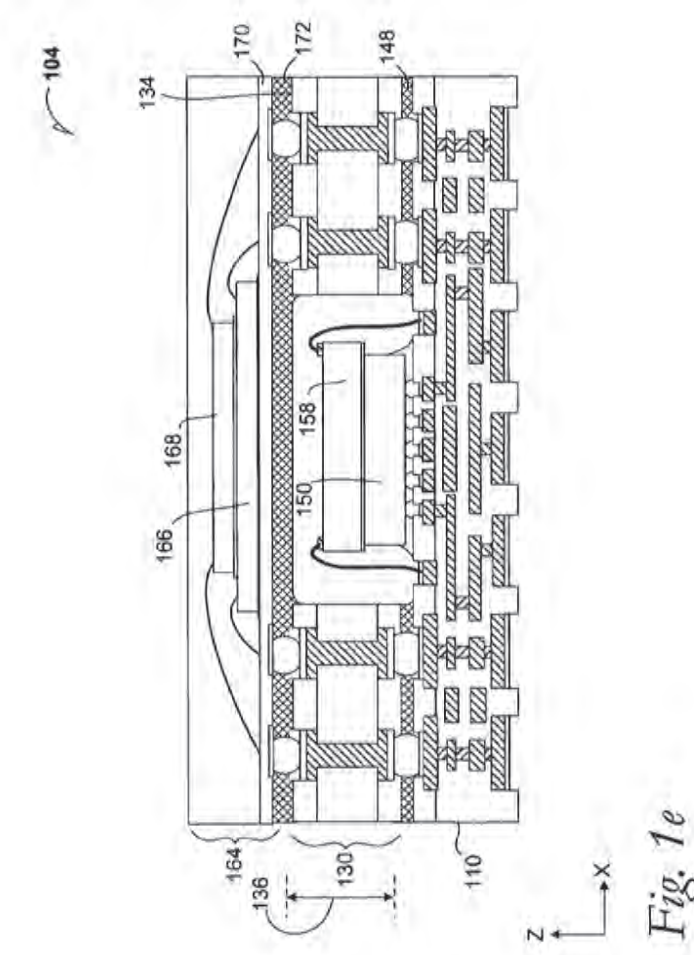


Fig. 16

Muthukumar, Fig. 1b

“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as

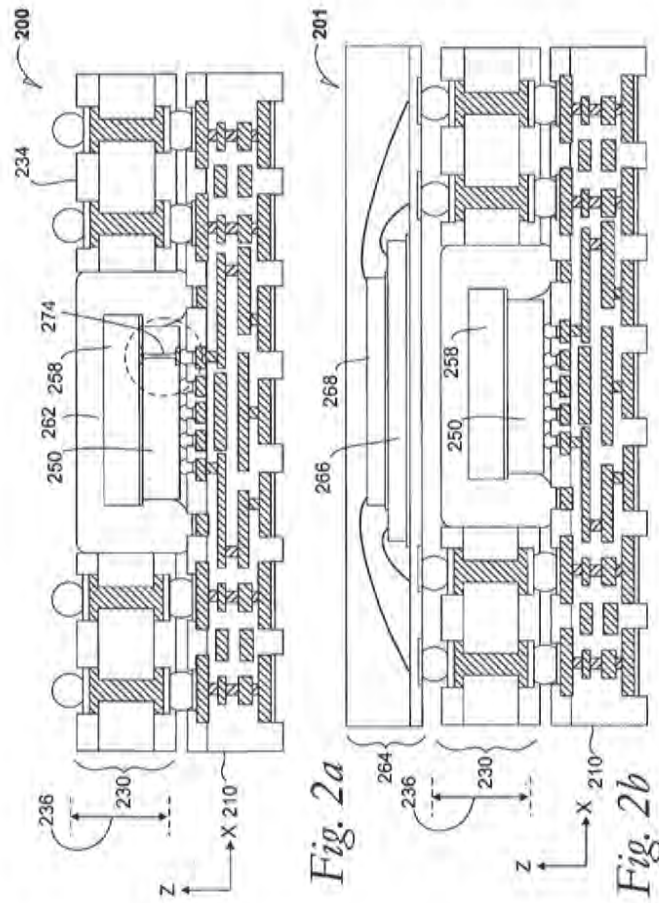
for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].



Muthukumar, Fig. 1e

“It can be seen that the mixed stack of the bottom chip 150 and top chip 158 have been accommodated by the interposer offset 136 such that the top package 164 does not interfere with the mixed stack. Consequently, the PoP stacked-chip apparatus is assembled with

	<p>sufficient interposer offset 136 to accommodate an offset height of the chip stack that may vary depending upon a specific application.” Muthukumar, [0037].</p> <p>“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].</p>
--	---



Muthukumar, Figs. 2a, 2b

“In an embodiment, the bottom chip 150 is a processor and the top chip 158 is a radio-frequency (RF) device.” Muthukumar, [0054].

To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Muthukumar discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>

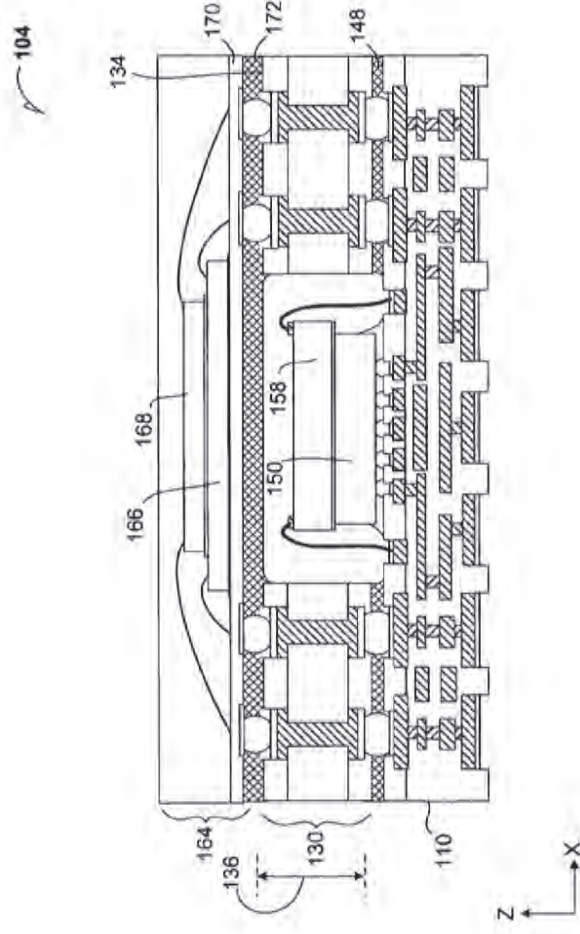
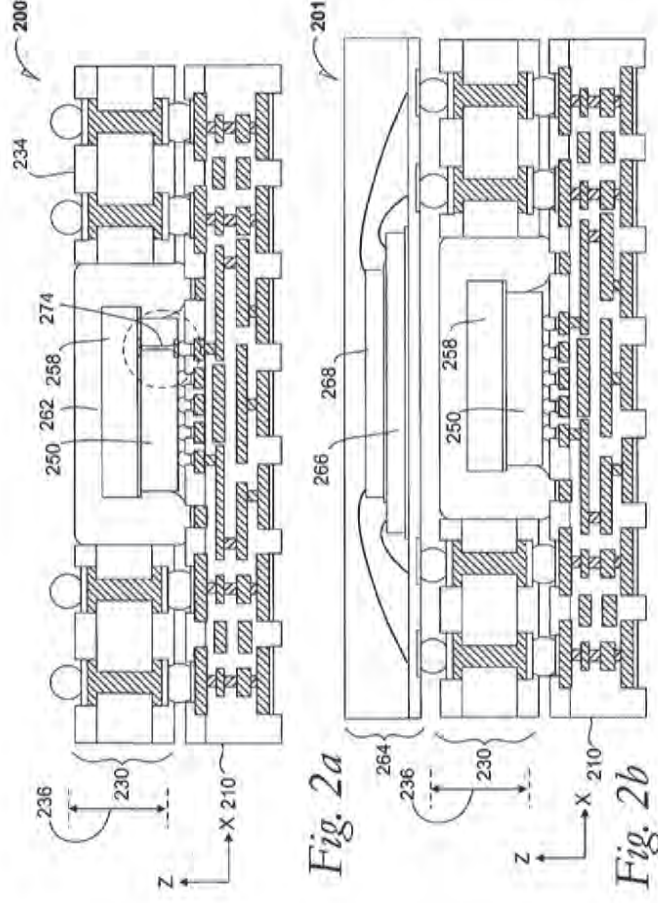


Fig. 1e

Muthukumar, Fig. 1e

“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an

original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.”
Muthukumar, [0044].

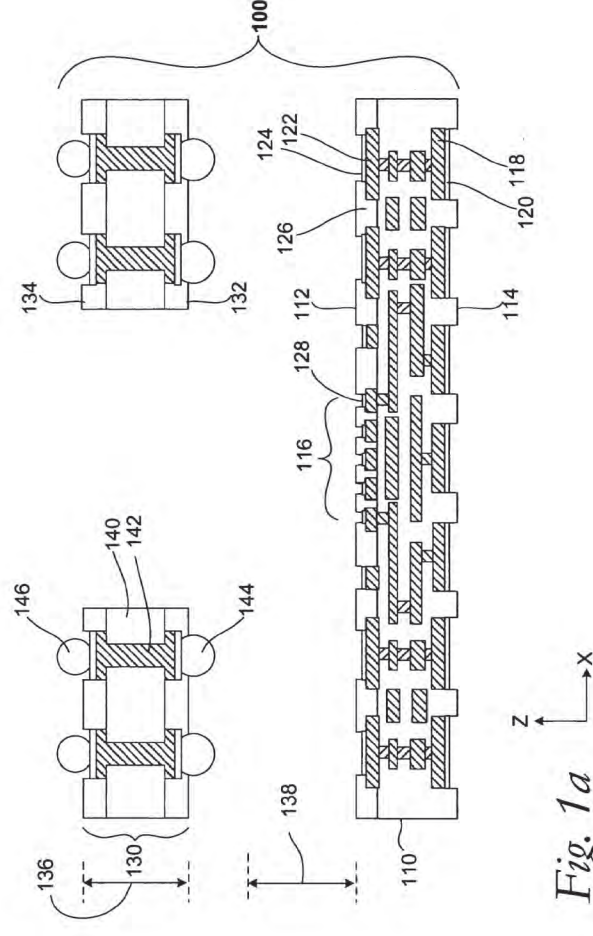


Muthukumar, Figs. 2a, 2b

To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

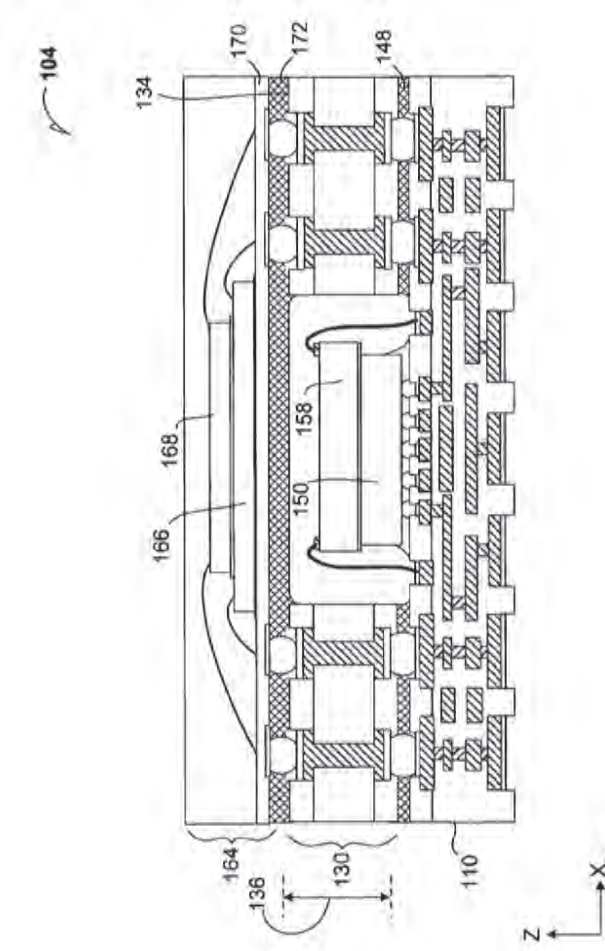
Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Muthukumar discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 a is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].</p>

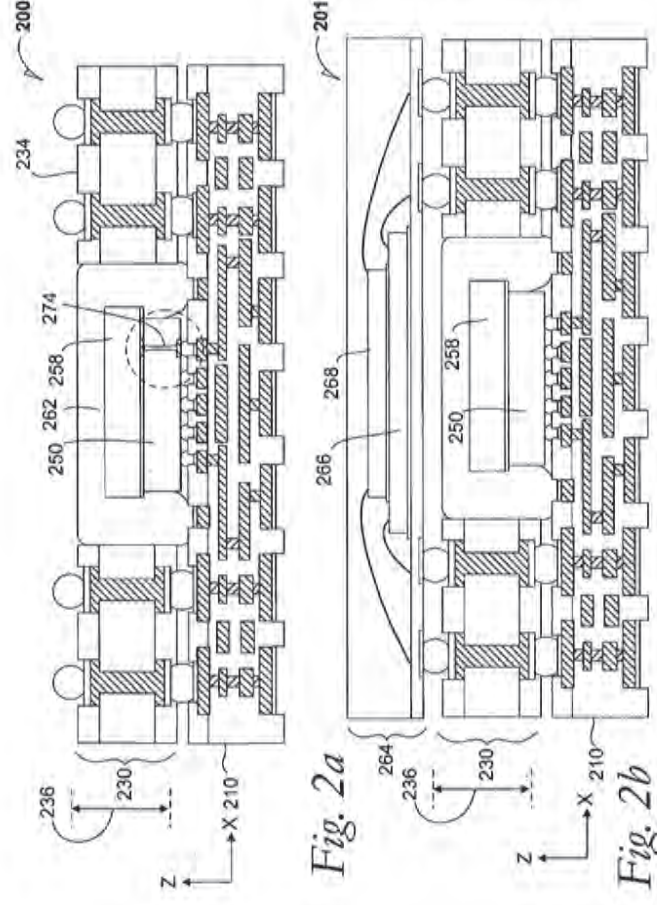


Muthukumar, Fig. 1a

“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package

	<p>164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>  <p><i>Fig. 1e</i></p> <p>Muthukumar, Fig. 1e</p>
--	--

	<p>“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.”</p> <p>Muthukumar, [0044].</p>
--	--



Muthukumar, Fig. 2a, 2b

To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Muthukumar discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“A bottom chip 150 is placed within the bottom-chip footprint 116 (FIG. 1 b). In an embodiment, the bottom chip 150 is a flip chip 150 that has been flip-chip bonded though a chip ball array, one electrical bump of which is referenced with numeral 152. In an embodiment, an underfill 154 has been flowed to fortify bonding between the bottom chip 150 and the package substrate 110. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the underfill 154. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the fill material 148.” Muthukumar, [0029].</p>

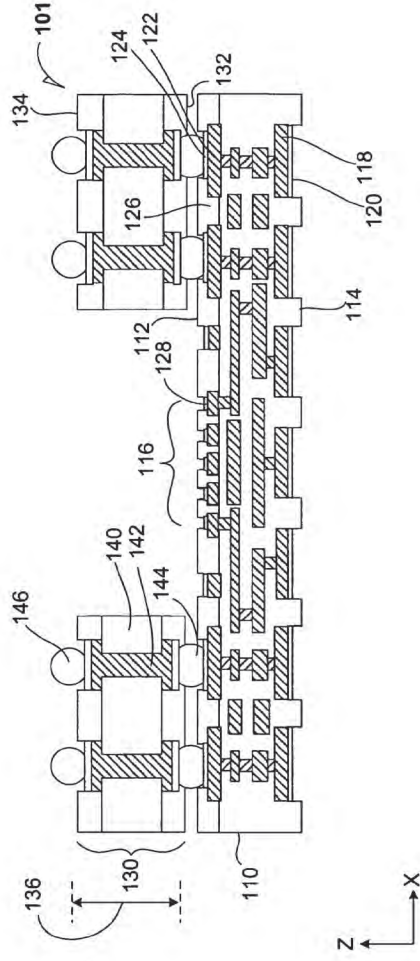
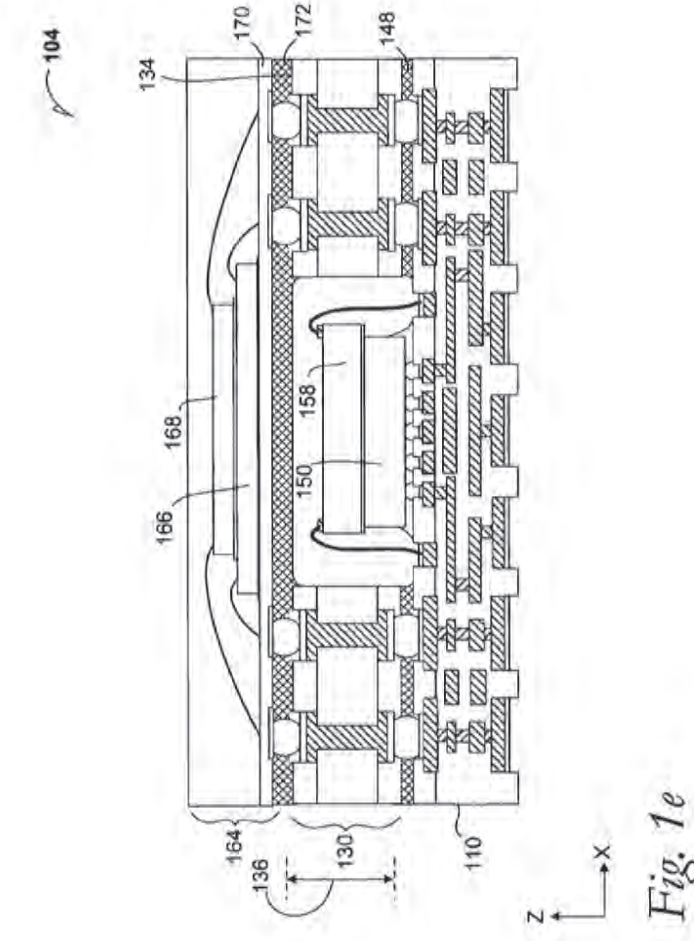


Fig. 1b

Muthukumar, Fig. 1b

“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer 130. The top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as

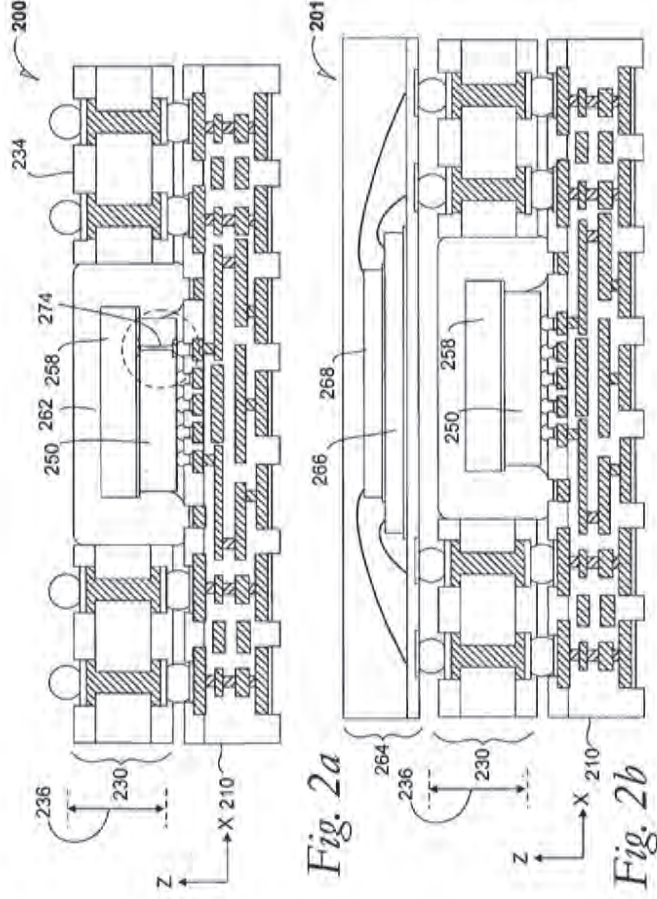
for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].



Muthukumar, Fig. 1e

“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset

236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].



Muthukumar, Figs. 2a, 2b

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	<p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Muthukumar discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack</p>

apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].

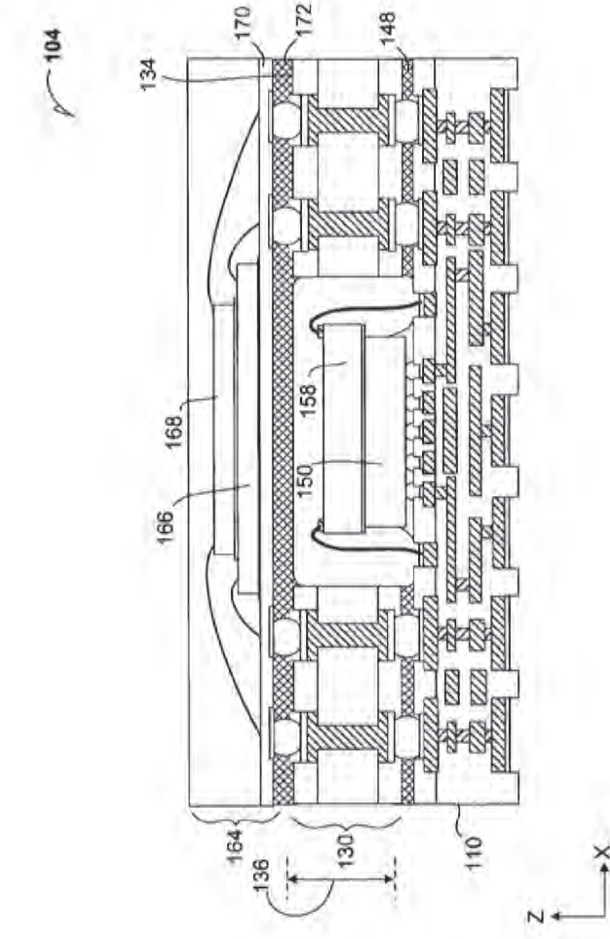
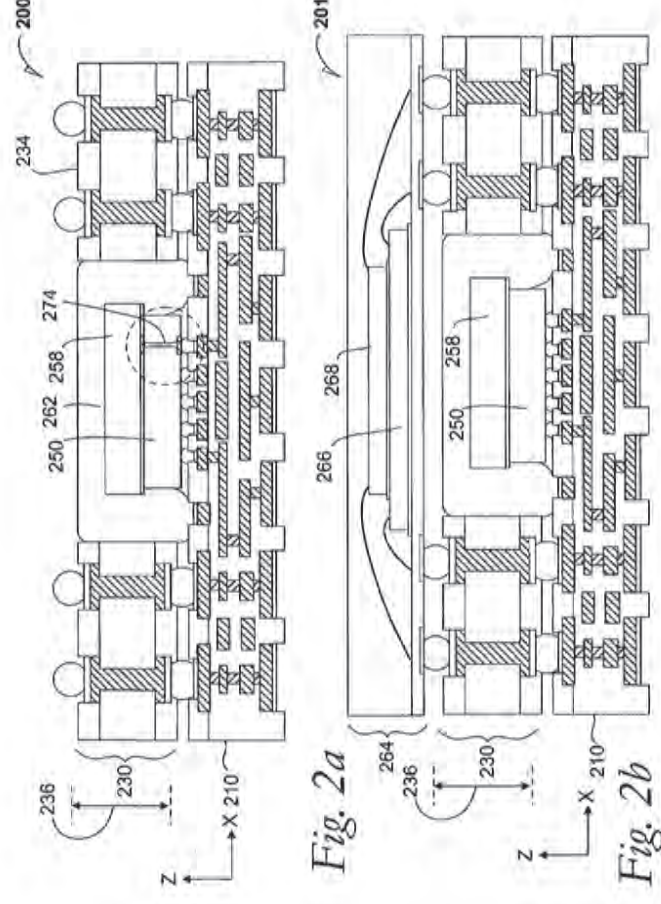


Fig. 1e

Muthukumar, Fig. 1e

“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example

embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].

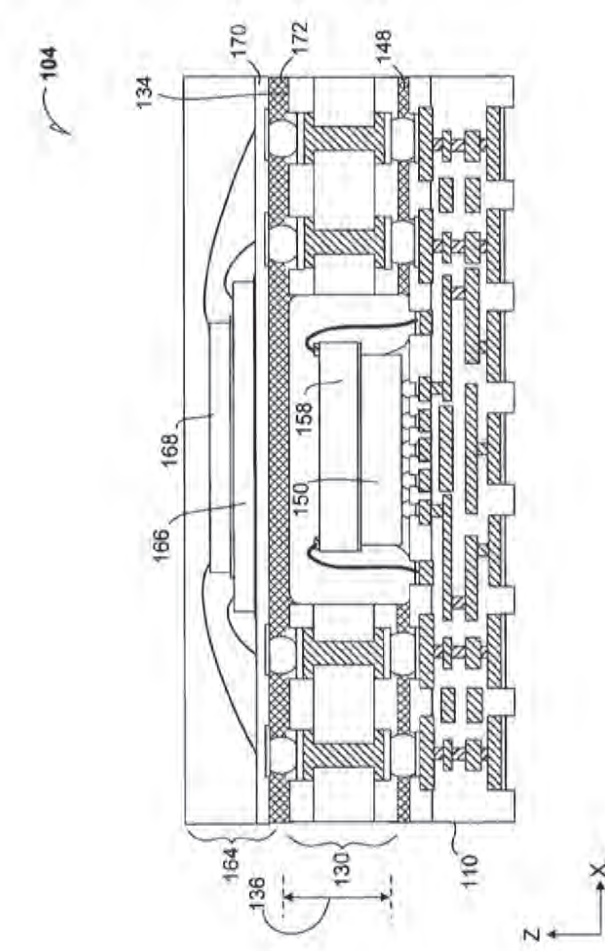


Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

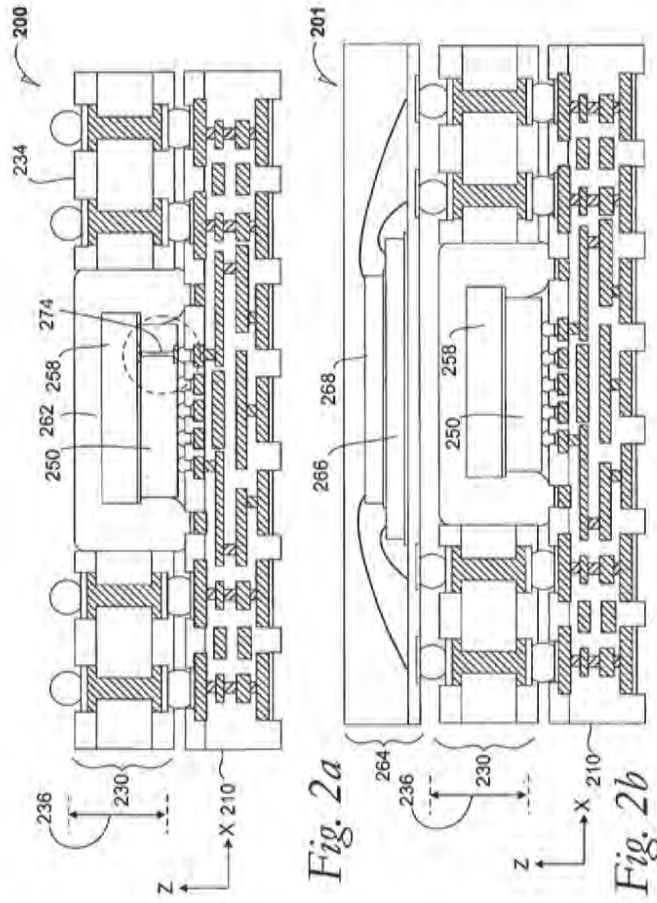
	<p>Muthukumar, Figs. 2a, 2b</p> <p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Muthukumar discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package</p>

	<p>164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>  <p><i>Fig. 1e</i></p> <p>Muthukumar, Fig. 1e</p>
--	--

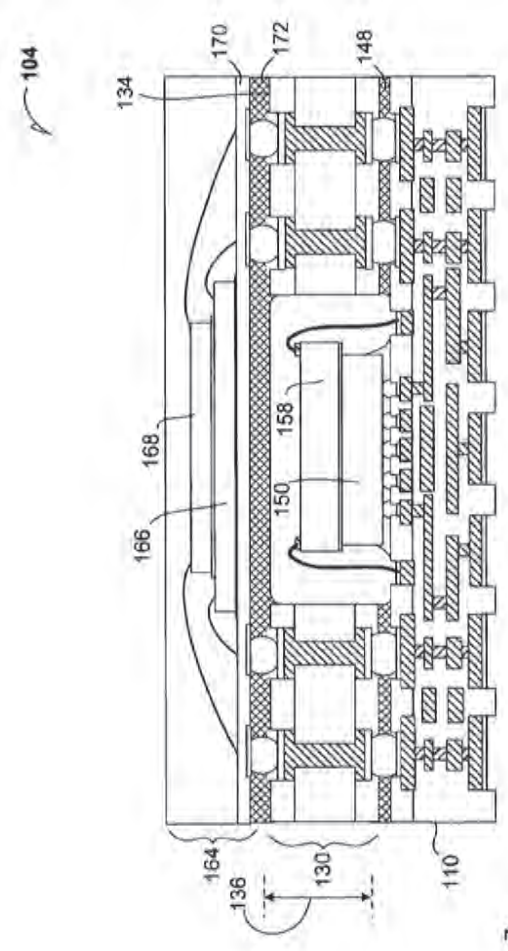
	<p>“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.”</p> <p>Muthukumar, [0044].</p>
--	--

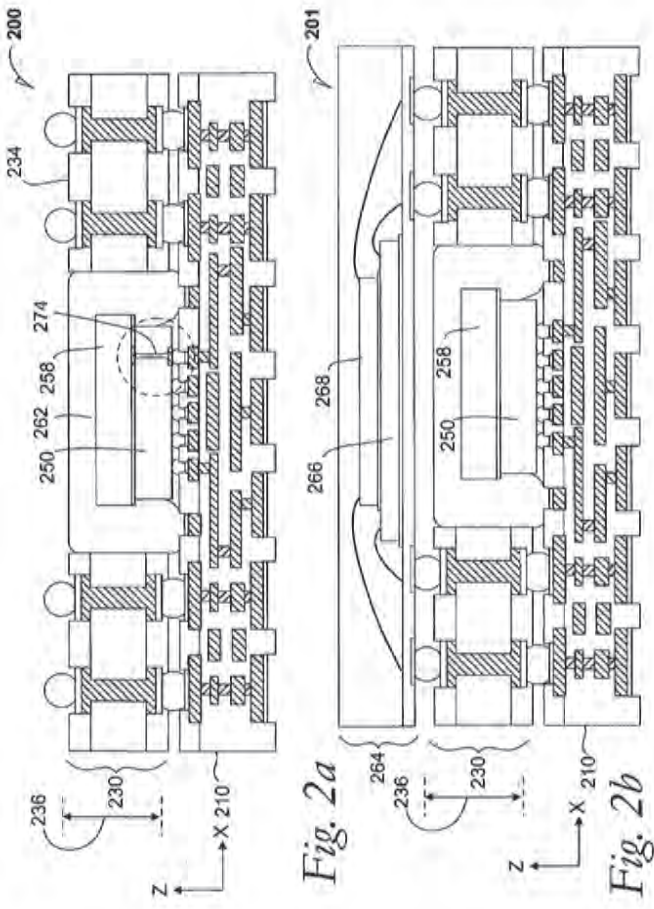


Muthukumar, Figs. 2a, 2b

To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Muthukumar discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].</p>

	<div><p>A cross-sectional diagram of a PoP stacked-chip apparatus 201. The diagram shows a top chip 236 and a top package 264 mounted on a mounting substrate 270. The top chip 236 is connected to the top package 264 via a top side 234 of an interposer 230. The top package 264 is connected to the mounting substrate 270 via a bottom chip 250 and the top chip 258. The top chip 258 is set within the interposer 230. The top package 264 has a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an</p><p>Fig. 1e</p></div> <div><p>Muthukumar, Fig. 1e</p></div>
--	--

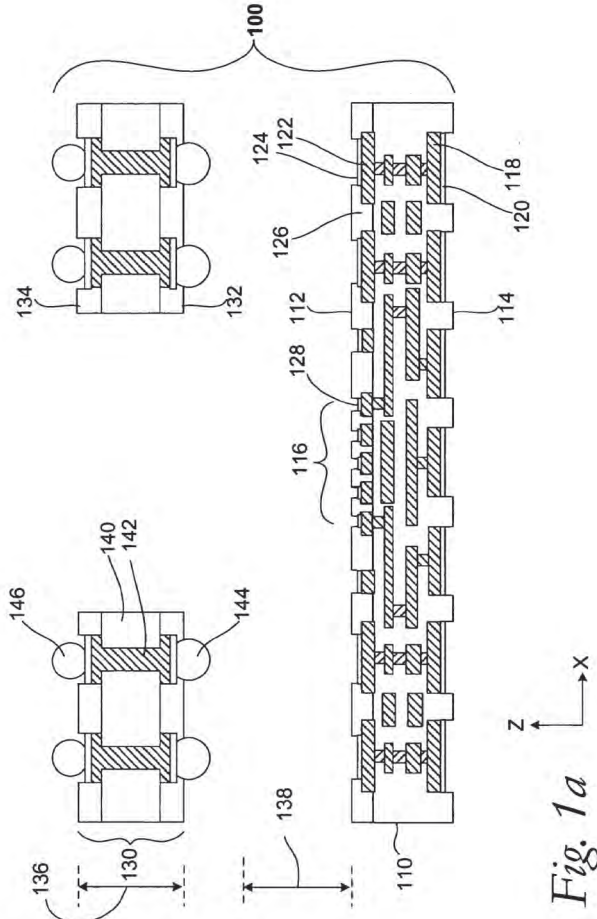
	<p>original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.” Muthukumar, [0044].</p>  <p>Muthukumar, Figs. 2a, 2b</p> <p>To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-25 - Invalidity of U.S. Patent No. 9859202 in view of Muthukumar - U.S. Patent Publication No. 20130127054

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Muthukumar discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a cross-section elevation of a mounting substrate and interposer apparatus 100 for a stacked-chip package according to an example embodiment. The apparatus 100 is depicted vertically (Z-direction) in exploded view including a package substrate 110 and an interposer 130. The package substrate 110 includes a die side 112 to accept a processor, and a land side 114 for coupling to outside communication such as a board. The “board” may be an external- or near-external structure for a hand-held device such as a wireless communicator. The package substrate 110 includes a bottom-chip footprint 116 on the die side 112. The bottom-chip footprint 116 may be ascertained in subsequent drawings disclosed</p>

	<p>herein by projecting illustrated processors on respective die sides of illustrated mounting substrates.” Muthukumar, [0021].</p>  <p><i>Fig. 1a</i></p> <p>Muthukumar, Fig. 1a</p> <p>“A bottom chip 150 is placed within the bottom-chip footprint 116 (FIG. 1 b). In an embodiment, the bottom chip 150 is a flip chip 150 that has been flip-chip bonded though a chip ball array, one electrical bump of which is referenced with numeral 152. In an embodiment, an underfill 154 has been flowed to fortify bonding between the bottom chip 150 and the package substrate 110. In a processing embodiment, reflow of the electrical</p>
--	--

bumps 152 is carried out during simultaneous curing of the underfill 154. In a processing embodiment, reflow of the electrical bumps 152 is carried out during simultaneous curing of the fill material 148.” Muthukumar, [0029].

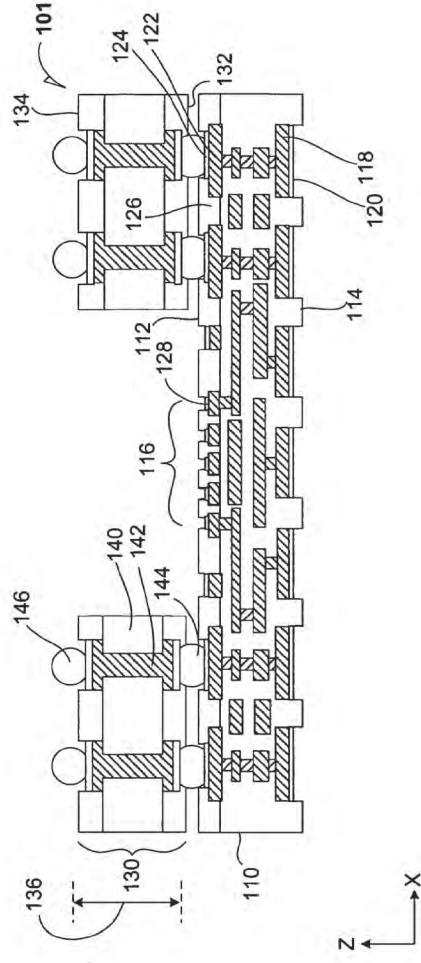


Fig. 1b

Muthukumar, Fig. 1b

“FIG. 1 e is a cross-section elevation of a package-on-package (PoP) stacked chip apparatus 104 that has assembled with the apparatus depicted in FIG. 1 d after further processing according to an example embodiment. The bottom chip 150 and the top chip 158 are set within the interposer offset 136 and a top package 164 has been mated to the top side 134 of the interposer 130. The top package 164 may have a mounting substrate 170 for communication to the bottom chip 150 and/or the top chip 158. The top package 164 is

depicted as a wire-bond enabling solution such as for an original-equipment manufacturer. Two wire-bonded dice are depicted in the top package 164. A die located in the top package 164 may be referred to as a microelectronic device. In an embodiment, the mixed-stack apparatus 103 depicted in FIG. 1 d is provided to accommodate a top package 164 such as for a smart phone, where smart-phone specific microelectronic devices are in the top package 164 and support microelectronic devices are in the chip stack.” Muthukumar, [0035].

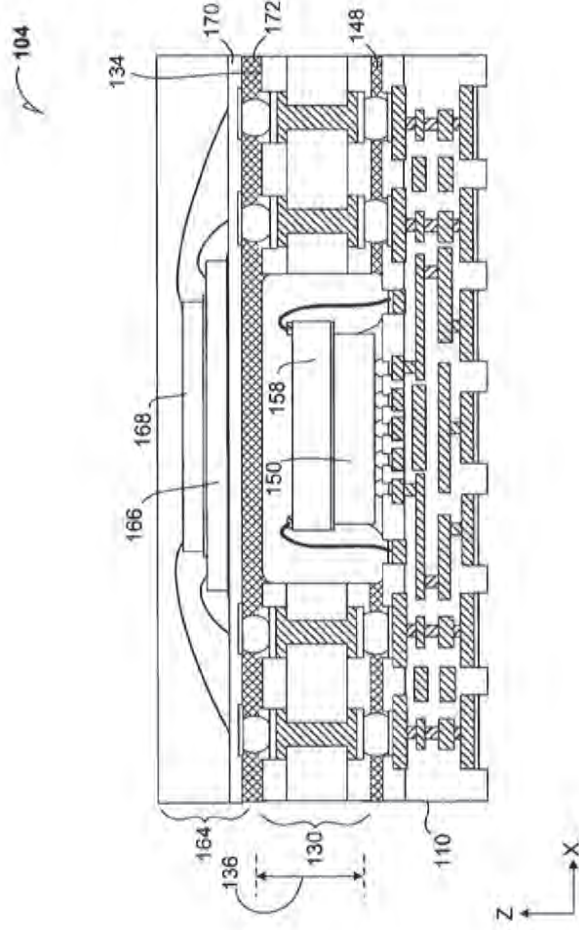
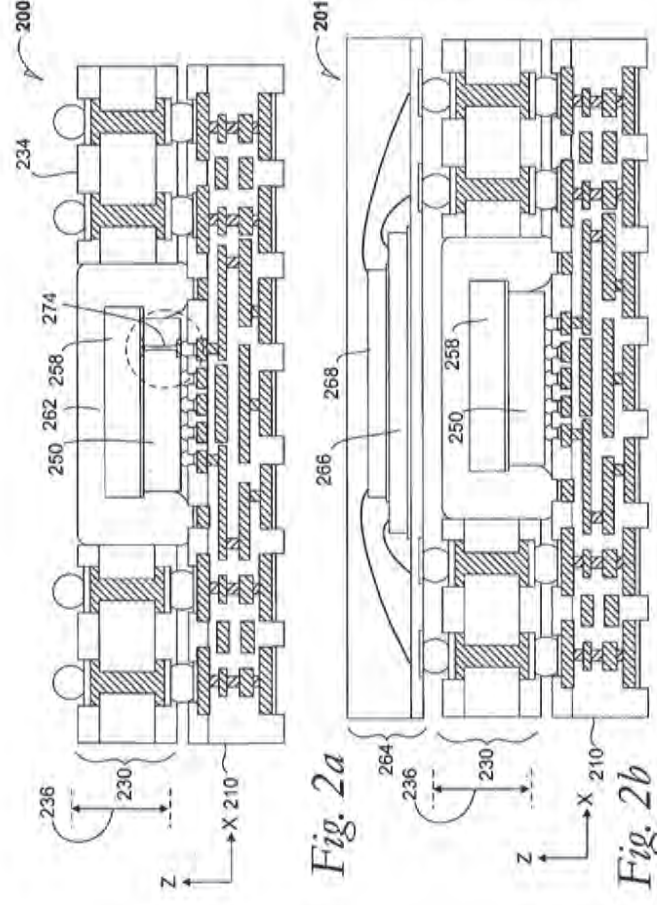


Fig. 1e

Muthukumar, Fig. 1e

	<p>“FIG. 2 b is a cross-section elevation of a PoP stacked-chip apparatus 201 that has assembled from the apparatus depicted in FIG. 2 a after further processing according to an example embodiment. The bottom chip 250 and the top chip 258 are set within the interposer offset 236 and a top package 264 has been mated to the top side 234 of the interposer 230. The top package 264 may have a mounting substrate 270 for communication to the bottom chip 250 and/or the top chip 258. The top package is depicted as TSV enabling solution such as for an original-equipment manufacturer. In an embodiment, the chip stack apparatus 200 depicted in FIG. 2 a is provided to accommodate a top package 264 such as for a smart phone.”</p> <p>Muthukumar, [0044].</p>
--	--



Muthukumar, Figs. 2a, 2b

To the extent Plaintiff contends that Muthukumar fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

U.S. Patent Publication No. 20040227258 (“Nakatani”) is titled Electronic Component Packaging Structure and Method for Producing the Same and lists Seiichi Nakatani as inventor. Nakatani is assigned to Matsushita Electric Industrial Co., Ltd. Nakatani anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ‘202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Nakatani is a U.S. patent publication that was filed May 5, 2004 and published November 18, 2004. Nakatani claims priority to JP 2003-135799 filed on May 14, 2003. Nakatani is therefore prior art to the ‘202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Nakatani, or otherwise rendered obvious by disclosures and teachings of Nakatani, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Nakatani does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Nakatani with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Nakatani, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Nakatani “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Nakatani or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Nakatani set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Nakatani discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a cross-sectional view showing a configuration of a semiconductor package according to this embodiment. In FIG. 1, reference numeral 101 denotes an electrical insulating encapsulation resin made of a mixture in which an inorganic filler and an organic resin are combined. Reference numeral 102 denotes a semiconductor chip that is embedded in the electrical insulating encapsulation resin 101 and is integrated therewith. Reference numeral 103 denotes an inner via that is formed in a thickness direction of the electrical</p>

	<p>insulating encapsulation resin 101, which establishes electric connection between protruding electrodes 105 and 106 that are formed on both surfaces of the electrical insulating encapsulation resin 101. In this example, the protruding electrodes 105 and 106 are formed with solder so that the protrusions are 100 m in length and have a hemispherical shape with a diameter of 200 m. Reference numerals 107 a and 107 b denote electrodes formed at the both surfaces of the electrical insulating encapsulation resin, which are base electrodes for the protruding electrodes 105 and 106.” Nakatani, [0081].</p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105</p>
--	---

and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].

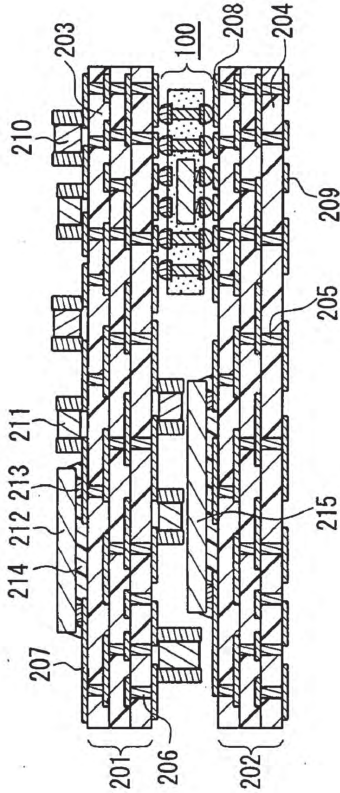


FIG. 3

Nakatani, FIG. 3

“FIG. 4 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards with the same semiconductor package 100 as in Embodiment 1. Reference numeral 301 denotes a circuit board, which includes an insulation material 303, a wiring pattern 304 and an inner via 305. On the circuit board 301, a semiconductor chip 306 and chip components 308, 309 and 310 are mounted. The semiconductor package 100 has the same configuration as shown in FIG. 1, and has protruding electrodes 105 and 106. The semiconductor package 100 connects electrically and mechanically with another circuit board 312 by means of firm securing using solder.” Nakatani, [0095].

	<p>“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively. Available insulation materials of the circuit boards, as in the case of Embodiment 1, are a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric and the like that are impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin and the like. Reference numerals 186 and 209 denote wiring patterns of the circuit boards 180 and 181, and 185 and 184 denote inner vias that connect layers. On the circuit boards 180 and 181, semiconductor chips 190 and 191 and chip components 188 and 189 are mounted. As for the semiconductor chips, a</p>
--	---

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>flip-chip packaging method is available, and the semiconductor chips 190 and 191 are connected with wiring patterns on the circuit boards via bumps. In order to electrically connect the circuit boards 180 and 181 with a narrow pitch, this embodiment shows an example where two semiconductor packages are used. By using the two semiconductor packages 100 and 900 for connecting circuit boards 180 and 181 in the vicinity of both end portions of the circuit boards as in FIG. 13, a package that not only allows the electrical connection with a narrow pitch but also provides an excellent mechanical strength can be obtained.” Nakatani, [0116-0118].</p>
[1.A] a bottom package substrate;	<p>Nakatani discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but</p>

a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].

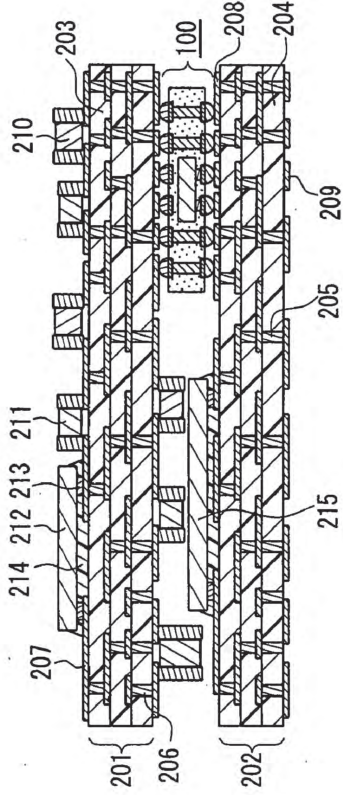


FIG. 3

Nakatani, FIG. 3

“FIG. 4 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards with the same semiconductor package 100 as in Embodiment 1. Reference numeral 301 denotes a circuit board, which includes an insulation material 303, a wiring pattern 304 and an inner via 305. On the circuit board 301, a semiconductor chip 306 and chip components 308, 309 and 310 are mounted. The

	<p>semiconductor package 100 has the same configuration as shown in FIG. 1, and has protruding electrodes 105 and 106. The semiconductor package 100 connects electrically and mechanically with another circuit board 312 by means of firm securing using solder.” Nakatani, [0095].</p> <p>“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively. Available insulation materials of the circuit boards, as in the case of Embodiment 1, are a reinforcing member made of paper, glass woven fabric, glass non-</p>
--	---

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>woven fabric, aramid non-woven fabric and the like that are impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin and the like. Reference numerals 186 and 209 denote wiring patterns of the circuit boards 180 and 181, and 185 and 184 denote inner vias that connect layers.” Nakatani, [0116].</p> <p>“Next, as shown in FIG. 8, the circuit board 301 and the circuit board 312 were electrically connected via the protruding electrodes using the above-stated semiconductor package 600, and at the same time the circuit boards 301 and 312 were firmly bonded and secured to each other using solder. More specifically, as the circuit board 301 having an inner via structure across the entire layers, a four-layered wiring structured aramid epoxy resin board was used. Nickel and gold plating were applied to a wiring pattern of this aramid epoxy resin board in the same manner as above so as to facilitate soldering, and a solder paste was printed using a metal mask on the wiring pattern subjected to the gold plating.” Nakatani, [0147-0148].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Nakatani discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are</p>

	<p>electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].</p>
--	---

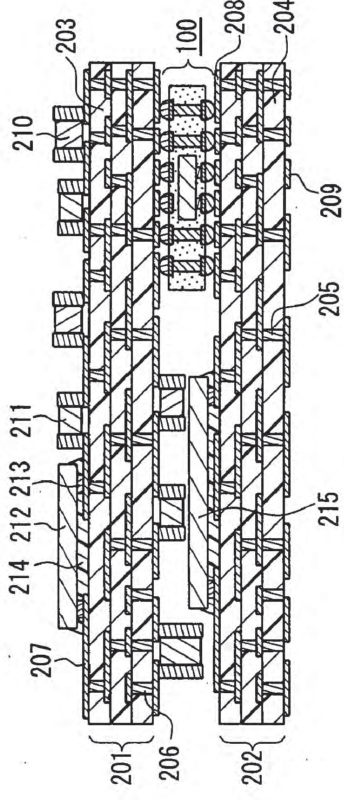


FIG. 3

Nakatani, FIG. 3

“FIG. 4 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards with the same semiconductor package 100 as in Embodiment 1. Reference numeral 301 denotes a circuit board, which includes an insulation material 303, a wiring pattern 304 and an inner via 305. On the circuit board 301, a semiconductor chip 306 and chip components 308, 309 and 310 are mounted. The semiconductor package 100 has the same configuration as shown in FIG. 1, and has protruding electrodes 105 and 106. The semiconductor package 100 connects electrically and mechanically with another circuit board 312 by means of firm securing using solder.” Nakatani, [0095].

“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and

	<p>therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively. Available insulation materials of the circuit boards, as in the case of Embodiment 1, are a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric and the like that are impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin and the like. Reference numerals 186 and 209 denote wiring patterns of the circuit boards 180 and 181, and 185 and 184 denote inner vias that connect layers.” Nakatani, [0116].</p> <p>“Next, as shown in FIG. 8, the circuit board 301 and the circuit board 312 were electrically connected via the protruding electrodes using the above-stated semiconductor package 600,</p>
--	--

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>and at the same time the circuit boards 301 and 312 were firmly bonded and secured to each other using solder.” Nakatani, [0147].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Nakatani discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are</p>

mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].

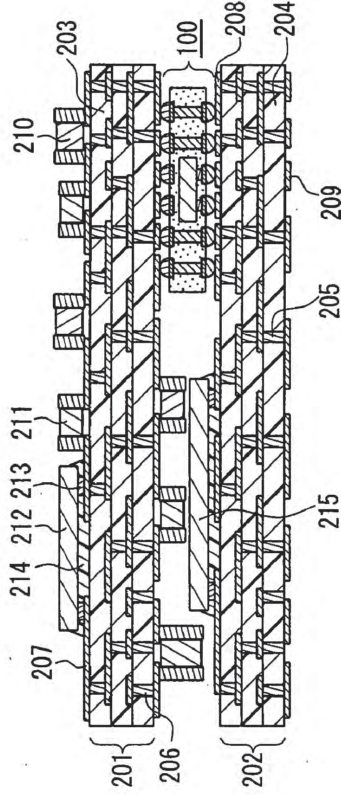


FIG. 3

Nakatani, FIG. 3

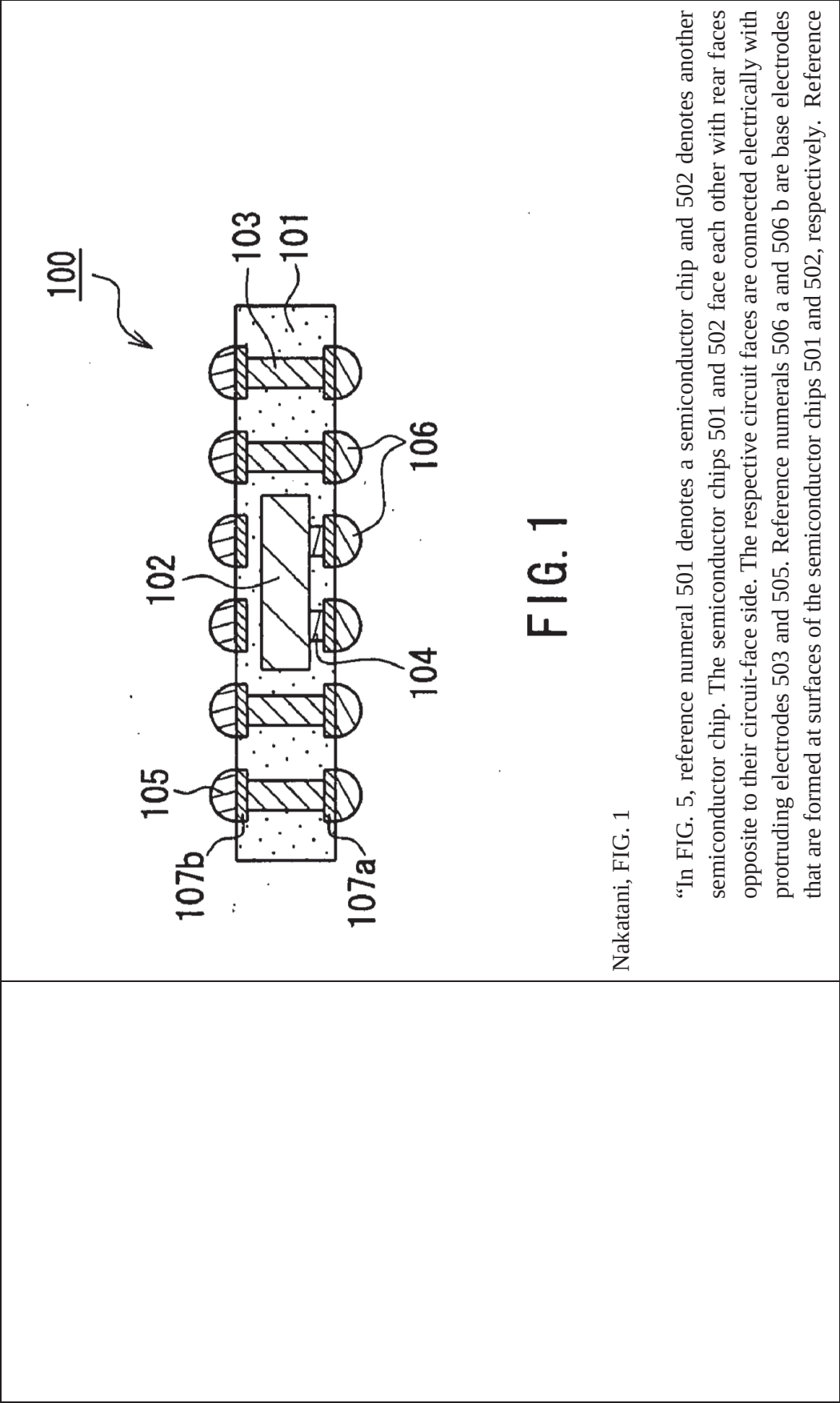
“FIG. 4 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards with the same semiconductor package 100 as in Embodiment 1. Reference numeral 301 denotes a circuit board, which includes an insulation material 303, a wiring pattern 304 and an inner via 305. On the circuit board 301, a

	<p>semiconductor chip 306 and chip components 308, 309 and 310 are mounted. The semiconductor package 100 has the same configuration as shown in FIG. 1, and has protruding electrodes 105 and 106. The semiconductor package 100 connects electrically and mechanically with another circuit board 312 by means of firm securing using solder.” Nakatani, [0095].</p> <p>“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively. Available insulation materials of the circuit boards, as in the case</p>
--	--

	<p>of Embodiment 1, are a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric and the like that are impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin and the like. Reference numerals 186 and 209 denote wiring patterns of the circuit boards 180 and 181, and 185 and 184 denote inner vias that connect layers. On the circuit boards 180 and 181, semiconductor chips 190 and 191 and chip components 188 and 189 are mounted. As for the semiconductor chips, a flip-chip packaging method is available, and the semiconductor chips 190 and 191 are connected with wiring patterns on the circuit boards via bumps. In order to electrically connect the circuit boards 180 and 181 with a narrow pitch, this embodiment shows an example where two semiconductor packages are used. By using the two semiconductor packages 100 and 900 for connecting circuit boards 180 and 181 in the vicinity of both end portions of the circuit boards as in FIG. 13, a package that not only allows the electrical connection with a narrow pitch but also provides an excellent mechanical strength can be obtained.” Nakatani, [0116-0118].</p> <p>“Next, as shown in FIG. 8, the circuit board 301 and the circuit board 312 were electrically connected via the protruding electrodes using the above-stated semiconductor package 600, and at the same time the circuit boards 301 and 312 were firmly bonded and secured to each other using solder. More specifically, as the circuit board 301 having an inner via structure across the entire layers, a four-layered wiring structured aramid epoxy resin board was used. Nickel and gold plating were applied to a wiring pattern of this aramid epoxy resin board in the same manner as above so as to facilitate soldering, and a solder paste was printed using a metal mask on the wiring pattern subjected to the gold plating. The material of the solder used was Pb free solder made of SnAgCu. The above-stated semiconductor package 600 was aligned with the portions where the solder had been printed and was mounted thereon. Thereafter, by using a solder reflow device, soldering was conducted on the aramid epoxy</p>
--	--

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>resin board 301 on which the semiconductor package 600 had been mounted.” Nakatani, [0147-0148].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Nakatani discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In FIG. 1, reference numeral 101 denotes an electrical insulating encapsulation resin made of a mixture in which an inorganic filler and an organic resin are combined. Reference numeral 102 denotes a semiconductor chip that is embedded in the electrical insulating encapsulation resin 101 and is integrated therewith. Reference numeral 103 denotes an inner via that is formed in a thickness direction of the electrical insulating encapsulation resin 101, which establishes electric connection between protruding electrodes 105 and 106 that are formed on both surfaces of the electrical insulating encapsulation resin 101.” Nakatani, [0081].</p>



	<p>numeral 504 denotes an electrical insulating encapsulation resin molded member, which protects the semiconductor chips 501 and 502.” Nakatani, [0098-0099].</p> <p>“The semiconductor chip 601 and the semiconductor chip 602 are die-bonded on a circuit board 603 in a face-up manner so that their circuit faces are directed upwardly. The semiconductor chip 601 mounted directly on the circuit board 603 is electrically connected with a wiring pattern on the circuit board 603 by a wire bonding method. The semiconductor chip 602 is die-bonded on the semiconductor chip 601 in a face-up manner, and a protruding electrode 607 is formed on the semiconductor chip 602 via an electrode 608 b formed therein. Reference numeral 605 denotes an electrical insulating encapsulation resin molded member, which protects the semiconductor chips 601 and 602. The semiconductor chips 601 and 602 are secured with an adhesive and the like, and encapsulation is conducted so as to be coplanar with the surface of the circuit-face using a transfer molding device.” Nakatani, [0103].</p> <p>“In FIG. 9, reference numeral 701 denotes an electrical insulating encapsulation resin molded member with a semiconductor chip 702 embedded therein, and 703 denotes a flexible board (FPC) 703 having wirings patterns 706 a and 706 b. The FPC 703 is bent as shown in FIG. 9, and protruding electrodes 704 and 705 are formed on surfaces of the wirings patterns 706 a and 706 b at the both surfaces, respectively.” Nakatani, [0106].</p> <p>“In FIG. 10, reference numeral 802 denotes a circuit board in which insulation layers and wiring patterns are formed in an arbitrary laminated manner, and these layers are connected with an inner via. On the circuit board 802, a semiconductor chip 801 is mounted, and the semiconductor chip 801 is connected with a wiring pattern on the circuit 802 via a wire 803. Another wiring pattern on the circuit board 802 is connected with a lead frame 804 via a wire 805. The lead frame 804 is bent as shown in FIG. 10 so as to prevent the wire 805 connected therewith by the wire bonding from being exposed to the surface of the semiconductor</p>
--	--

	<p>package. Reference numeral 809 denotes a wiring pattern formed at a surface of the circuit board 802, and a protruding electrode 807 is formed on a surface of this wiring pattern 809. An electrical insulating encapsulation resin molded member 806 encapsulates these circuit board 802, semiconductor chip 801, wires 803 and 805 and lead frame 804 so as to protect and secure the same, and on the surfaces of the circuit board and the electrical insulating encapsulation resin molded member, protruding electrode 807 and 808 are formed, respectively.” Nakatani, [0108-0109].</p> <p>“In FIG. 11, reference numeral 902 denotes a circuit board in which insulation layers and wiring patterns are formed in an arbitrary laminated manner, and these layers are connected with an inner via, as in the case of the previous embodiment. On the circuit board 902, a semiconductor chip 901 is mounted by a flip-chip packaging method, and the semiconductor chip 901 is connected with a wiring pattern on the circuit board 902 via a bump 903. Another wiring pattern on the circuit board 902 is connected with a protruding electrode 907 via a metal ball 904. Reference numeral 908 denotes a wiring pattern formed at a surface of the circuit board 902, and a protruding electrode 906 is formed on this wiring pattern 908. An electrical insulating encapsulation resin molded member 905 encapsulates these circuit board 902, semiconductor chip 901 and metal ball 904 so as to protect and secure the same, and further the protruding electrodes 906 and 907 are formed on a surface of the circuit board and the electrical insulating encapsulation resin molded member, respectively.” Nakatani, [0112-0113].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Nakatani discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“It is preferable that in a part of the protruding electrodes on the both faces of the electrical insulating encapsulation resin molded member, upper and lower protruding electrodes are electrically connected by means of inner vias.” Nakatani, [0036].</p> <p>“Furthermore, the use of the mixture containing at least the inorganic filler and a thermosetting composition as the electrical insulating encapsulation resin molded member can achieve an especially good effect of allowing a thermal expansion coefficient, a thermal conductivity, and a dielectric constant to be controlled freely by selecting the inorganic filler, as compared with the conventional package.” Nakatani, [0078].</p> <p>“Reference numeral 103 denotes an inner via that is formed in a thickness direction of the electrical insulating encapsulation resin 101, which establishes electric connection between protruding electrodes 105 and 106 that are formed on both surfaces of the electrical insulating encapsulation resin 101.” Nakatani, [0081].</p>
--	--

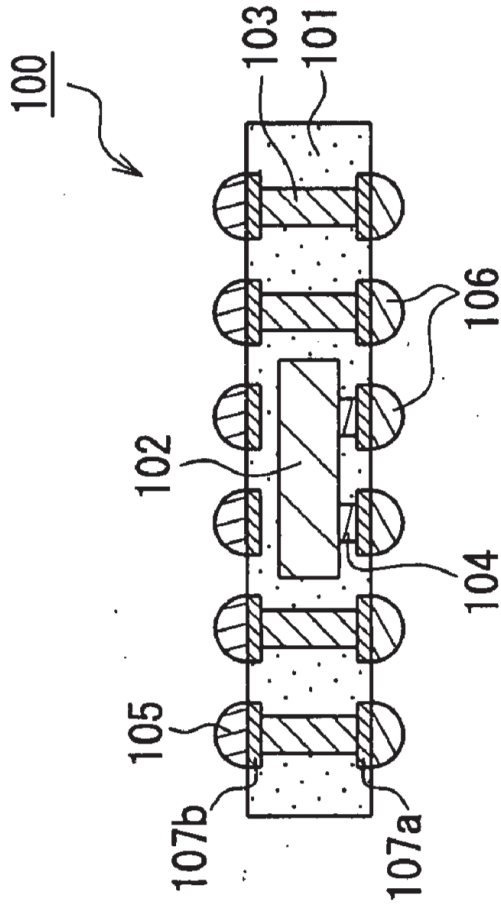


FIG. 1

Nakatani, FIG. 1

“As for the inner via 103, a method for applying copper plating or a conductive paste to a hole processed with a drill or a laser so as to establish electric connection is available.” Nakatani, [0082].

“Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers.” Nakatani, [0092].

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>“As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection.” Nakatani, [0092].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Nakatani discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Reference numerals 107 a and 107 b denote electrodes formed at the both surfaces of the electrical insulating encapsulation resin, which are base electrodes for the protruding electrodes 105 and 106. The base electrodes 107 a and 107 b can be formed concurrently when the semiconductor chip 102 is embedded in the electrical insulating encapsulation resin. The base electrodes can be formed as follows: a semiconductor chip 102 is mounted on a metal substrate, and an electrical insulating encapsulation resin that has been processed into a sheet form is laminated thereon. Then, heat and pressure are applied thereto so that the semiconductor chip 102 is embedded, and thereafter the metal substrate is processed so as to form the base electrodes. A lead frame with a pattern formed therein may be integrated with the electrical insulating encapsulation resin as the base electrodes. As for the inner via 103, a method for applying copper plating or a conductive paste to a hole processed with a drill or a laser so as to establish electric connection is available.” Nakatani, [0081-0082].</p>

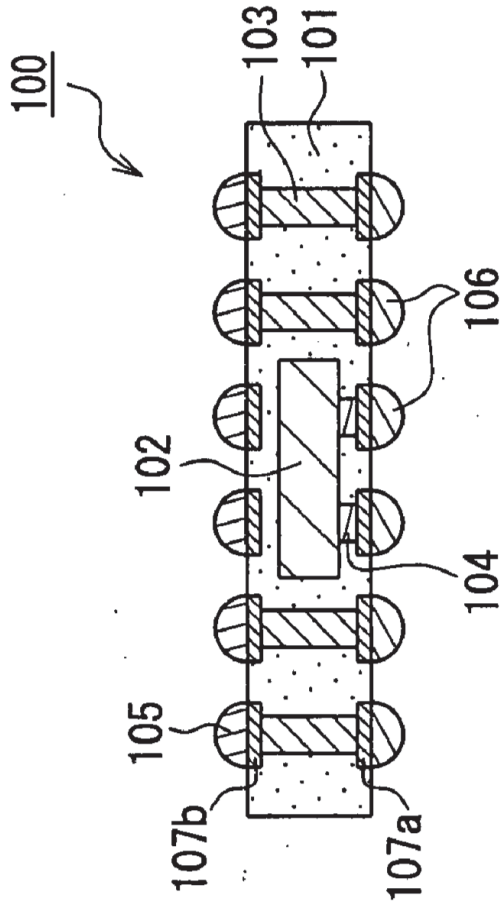


FIG. 1

Nakatani, FIG. 1

“In FIG. 5, reference numeral 501 denotes a semiconductor chip and 502 denotes another semiconductor chip. The semiconductor chips 501 and 502 face each other with rear faces opposite to their circuit-face side. The respective circuit faces are connected electrically with protruding electrodes 503 and 505. Reference numerals 506 a and 506 b are base electrodes that are formed at surfaces of the semiconductor chips 501 and 502, respectively.” Nakatani, [0098].

	<p>“Reference numeral 601 denotes a semiconductor chip and 602 denotes another semiconductor chip. The semiconductor chip 601 and the semiconductor chip 602 are die-bonded on a circuit board 603 in a face-up manner so that their circuit faces are directed upwardly. The semiconductor chip 601 mounted directly on the circuit board 603 is electrically connected with a wiring pattern on the circuit board 603 by a wire bonding method. The semiconductor chip 602 is die-bonded on the semiconductor chip 601 in a face-up manner, and a protruding electrode 607 is formed on the semiconductor chip 602 via an electrode 608 b formed therein.” Nakatani, [0103].</p> <p>“Reference numeral 809 denotes a wiring pattern formed at a surface of the circuit board 802, and a protruding electrode 807 is formed on a surface of this wiring pattern 809” Nakatani, [0108].</p> <p>“Reference numeral 908 denotes a wiring pattern formed at a surface of the circuit board 902, and a protruding electrode 906 is formed on this wiring pattern 908.” Nakatani, [0112].</p> <p>“Reference numeral 170 denotes an electrode formed at a surface of the semiconductor chip 162. Next, as shown in FIG. 14D, encapsulation is conducted with an encapsulation resin 165 up to the circuit face of the semiconductor chip 162. As for the encapsulation resin, the materials shown in Embodiment 1 may be used. Alternatively, the encapsulation may be conducted so as to cover the entire semiconductor chip 162, and thereafter grinding may be conducted so as to reach the electrode at the surface of the semiconductor chip 162. Finally, as shown in FIG. 14E, protruding electrodes 166 and 167 are formed on the wiring pattern 169 a at the surface of the circuit board 163 and on the electrode 170 at the surface of the semiconductor chip 162, so that the semiconductor package can be manufactured.” Nakatani, [0122-0124].</p>
--	--

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Nakatani discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Protruding electrodes are arranged on both faces of the electrical insulating encapsulation resin molded member, and the electronic component is connected electrically with at least a part of the protruding electrodes.” Nakatani, [0017].</p>

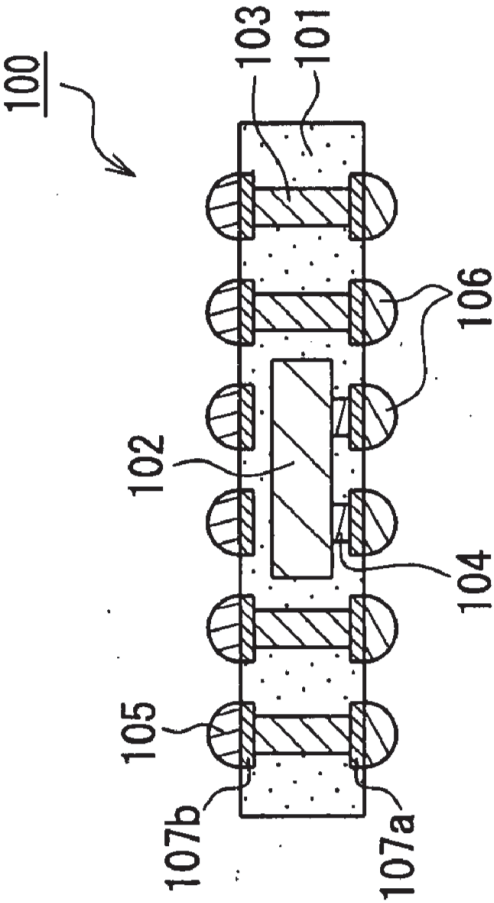


FIG. 1

Nakatani, FIG. 1

“The protruding electrodes preferably have a length of the protrusion of about 10 to 250 m, a diameter of about 50 to 250 m and a pitch (a distance between one protruding electrode and an adjacent protruding electrode, including a space therebetween) of about 100 to 500 m.” Nakatani, [0035].

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the</p>	<p>“In this example, the protruding electrodes 105 and 106 are formed with solder so that the protrusions are 100 m in length and have a hemispherical shape with a diameter of 200 m.” Nakatani, [0081].</p> <p>“Reference numerals 107 a and 107 b denote electrodes formed at the both surfaces of the electrical insulating encapsulation resin, which are base electrodes for the protruding electrodes 105 and 106.” Nakatani, [0081].</p> <p>“The semiconductor chip 602 is die-bonded on the semiconductor chip 601 in a face-up manner, and a protruding electrode 607 is formed on the semiconductor chip 602 via an electrode 608 b formed therein.” Nakatani, [0103].</p> <p>“Finally, as shown in FIG. 14E, protruding electrodes 166 and 167 are formed on the wiring pattern 169 a at the surface of the circuit board 163 and on the electrode 170 at the surface of the semiconductor chip 162, so that the semiconductor package can be manufactured.” Nakatani, [0124].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p></p>	<p>Nakatani discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

plurality of metal pillars of the spacer connector,

“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection.” Nakatani, [0092].

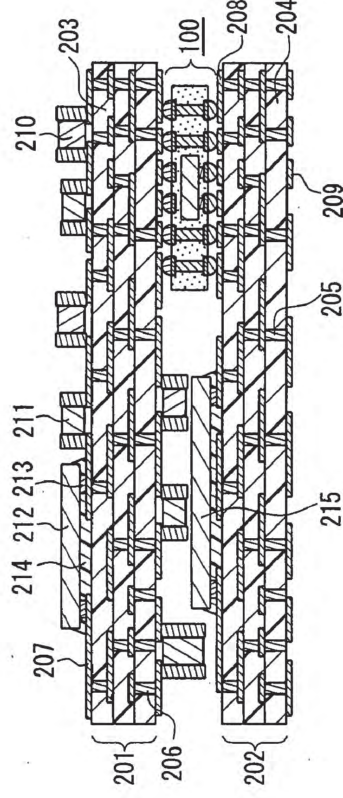


FIG. 3

Nakatani, FIG. 3

	<p>“Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0093].</p> <p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively.” Nakatani, [0116].</p> <p>“In order to electrically connect the circuit boards 180 and 181 with a narrow pitch, this embodiment shows an example where two semiconductor packages are used. By using the two semiconductor packages 100 and 900 for connecting circuit boards 180 and 181 in the vicinity of both end portions of the circuit boards as in FIG. 13, a package that not only allows the electrical connection with a narrow pitch but also provides an excellent mechanical strength can be obtained.” Nakatani, [0118].</p> <p>“More specifically, as the circuit board 301 having an inner via structure across the entire layers, a four-layered wiring structured aramid epoxy resin board was used. Nickel and gold plating were applied to a wiring pattern of this aramid epoxy resin board in the same manner as above so as to facilitate soldering, and a solder paste was printed using a metal mask on the wiring pattern subjected to the gold plating. The material of the solder used was Pb free solder made of SnAgCu. The above-stated semiconductor package 600 was aligned with the portions where the solder had been printed and was mounted thereon.” Nakatani, [0148].</p>
--	---

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Nakatani discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-</p>

chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].

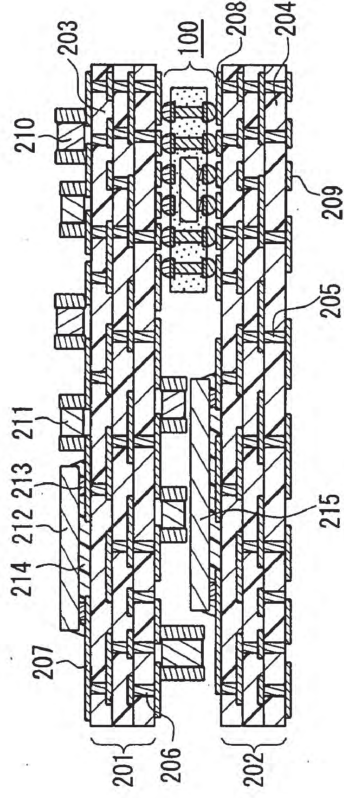


FIG. 3

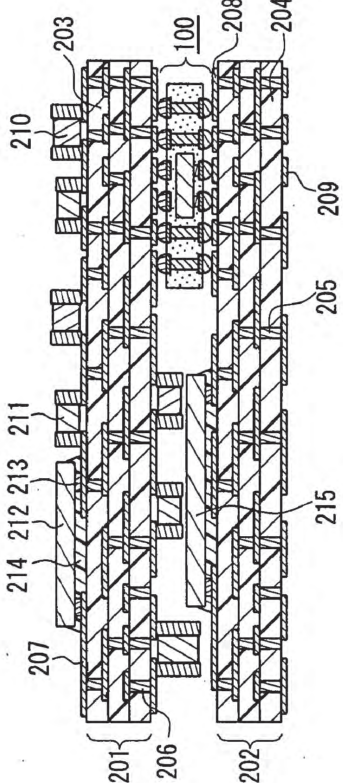
Nakatani, FIG. 3

“FIG. 4 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards with the same semiconductor package 100 as in Embodiment 1. Reference numeral 301 denotes a circuit board, which includes an insulation material 303, a wiring pattern 304 and an inner via 305. On the circuit board 301, a semiconductor chip 306 and chip components 308, 309 and 310 are mounted. The semiconductor package 100 has the same configuration as shown in FIG. 1, and has protruding electrodes 105 and 106. The semiconductor package 100 connects electrically and

	<p>mechanically with another circuit board 312 by means of firm securing using solder.” Nakatani, [0095].</p> <p>“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively. Available insulation materials of the circuit boards, as in the case of Embodiment 1, are a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric and the like that are impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin and the like. Reference numerals 186</p>
--	--

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>and 209 denote wiring patterns of the circuit boards 180 and 181, and 185 and 184 denote inner vias that connect layers.” Nakatani, [0116].</p> <p>“Next, as shown in FIG. 8, the circuit board 301 and the circuit board 312 were electrically connected via the protruding electrodes using the above-stated semiconductor package 600, and at the same time the circuit boards 301 and 312 were firmly bonded and secured to each other using solder. More specifically, as the circuit board 301 having an inner via structure across the entire layers, a four-layered wiring structured aramid epoxy resin board was used. Nickel and gold plating were applied to a wiring pattern of this aramid epoxy resin board in the same manner as above so as to facilitate soldering, and a solder paste was printed using a metal mask on the wiring pattern subjected to the gold plating. The material of the solder used was Pb free solder made of SnAgCu. The above-stated semiconductor package 600 was aligned with the portions where the solder had been printed and was mounted thereon. Thereafter, by using a solder reflow device, soldering was conducted on the aramid epoxy resin board 301 on which the semiconductor package 600 had been mounted.” Nakatani, [0147-0148].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.	<p>Nakatani discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p>

<p>the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>See, e.g.:</p> <p>“As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].</p>  <p style="text-align: center;">FIG. 3</p> <p>Nakatani, FIG. 3</p>
--	--

	<p>“FIG. 4 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards with the same semiconductor package 100 as in Embodiment 1. Reference numeral 301 denotes a circuit board, which includes an insulation material 303, a wiring pattern 304 and an inner via 305. On the circuit board 301, a semiconductor chip 306 and chip components 308, 309 and 310 are mounted. The semiconductor package 100 has the same configuration as shown in FIG. 1, and has protruding electrodes 105 and 106. The semiconductor package 100 connects electrically and mechanically with another circuit board 312 by means of firm securing using solder.” Nakatani, [0095].</p> <p>“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p>
--	---

	<p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively. Available insulation materials of the circuit boards, as in the case of Embodiment 1, are a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric and the like that are impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin and the like. Reference numerals 186 and 209 denote wiring patterns of the circuit boards 180 and 181, and 185 and 184 denote inner vias that connect layers. On the circuit boards 180 and 181, semiconductor chips 190 and 191 and chip components 188 and 189 are mounted. As for the semiconductor chips, a flip-chip packaging method is available, and the semiconductor chips 190 and 191 are connected with wiring patterns on the circuit boards via bumps. In order to electrically connect the circuit boards 180 and 181 with a narrow pitch, this embodiment shows an example where two semiconductor packages are used. By using the two semiconductor packages 100 and 900 for connecting circuit boards 180 and 181 in the vicinity of both end portions of the circuit boards as in FIG. 13, a package that not only allows the electrical connection with a narrow pitch but also provides an excellent mechanical strength can be obtained.” Nakatani, [0116-0118].</p> <p>“More specifically, as the circuit board 301 having an inner via structure across the entire layers, a four-layered wiring structured aramid epoxy resin board was used. Nickel and gold plating were applied to a wiring pattern of this aramid epoxy resin board in the same manner as above so as to facilitate soldering, and a solder paste was printed using a metal mask on the wiring pattern subjected to the gold plating. The material of the solder used was Pb free solder made of SnAgCu. The above-stated semiconductor package 600 was aligned with the portions where the solder had been printed and was mounted thereon. Thereafter, by using a</p>
--	---

	<p>solder reflow device, soldering was conducted on the aramid epoxy resin board 301 on which the semiconductor package 600 had been mounted. The reflow was conducted under the profile of once keeping a temperature at 150 C. and then applying heat so as to reach 250 C., where the state at 250 C. was kept for about 10 seconds. As a result, protruding electrodes on the semiconductor package 600 and the wiring pattern 304 on the aramid epoxy resin board 301 were connected electrically and mechanically using the solder. Next, other protruding electrodes on the semiconductor package 600 and the wiring pattern of the FPC 312 were connected. The FPC 312 included a base film made of polyimide and wiring patterns were connected on both faces of the base film via adhesive layers. Similarly to the above, the solder paste like the above was printed on the wiring pattern 313 of the FPC 312 using a metal mask, and the FPC 312 was aligned with the protruding electrodes on a semiconductor package 600 on a different side from the above, and soldering was conducted by a reflow device while keeping their positions. As a result, the desired wiring patterns of the aramid epoxy resin board 301 and the FPC 312 could be connected electrically and mechanically via the protruding electrodes of the semiconductor package 600.” Nakatani, [0148].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Nakatani discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>

	<p>“FIG. 1 is a cross-sectional view showing a configuration of a semiconductor package according to this embodiment. In FIG. 1, reference numeral 101 denotes an electrical insulating encapsulation resin made of a mixture in which an inorganic filler and an organic resin are combined. Reference numeral 102 denotes a semiconductor chip that is embedded in the electrical insulating encapsulation resin 101 and is integrated therewith. Reference numeral 103 denotes an inner via that is formed in a thickness direction of the electrical insulating encapsulation resin 101, which establishes electric connection between protruding electrodes 105 and 106 that are formed on both surfaces of the electrical insulating encapsulation resin 101. In this example, the protruding electrodes 105 and 106 are formed with solder so that the protrusions are 100 μm in length and have a hemispherical shape with a diameter of 200 μm. Reference numerals 107 a and 107 b denote electrodes formed at the both surfaces of the electrical insulating encapsulation resin, which are base electrodes for the protruding electrodes 105 and 106. The base electrodes 107 a and 107 b can be formed concurrently when the semiconductor chip 102 is embedded in the electrical insulating encapsulation resin. The base electrodes can be formed as follows: a semiconductor chip 102 is mounted on a metal substrate, and an electrical insulating encapsulation resin that has been processed into a sheet form is laminated thereon. Then, heat and pressure are applied thereto so that the semiconductor chip 102 is embedded, and thereafter the metal substrate is processed so as to form the base electrodes. A lead frame with a pattern formed therein may be integrated with the electrical insulating encapsulation resin as the base electrodes.” Nakatani, [0081].</p>
--	--

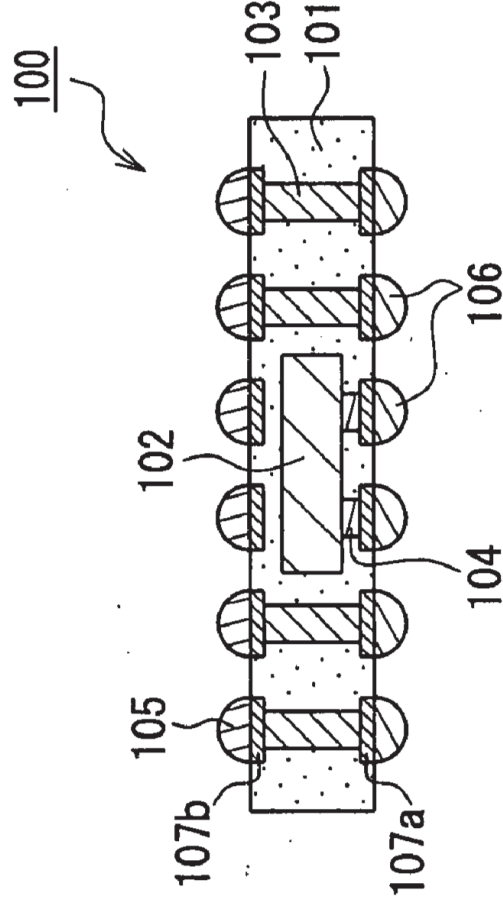


Fig. 1

Nakatani, FIG. 1

“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the

	<p>like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].</p>
--	--

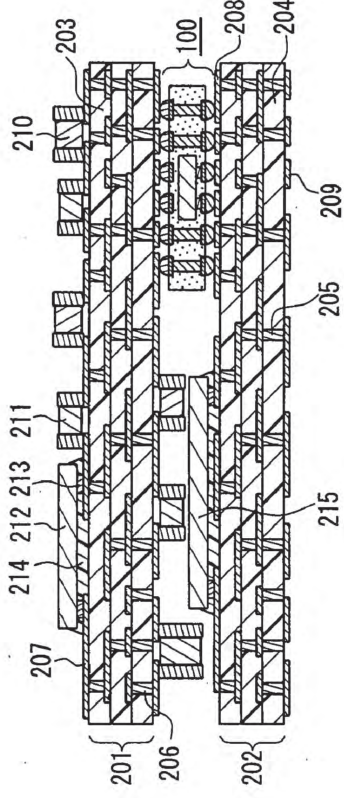


FIG. 3

Nakatani, FIG. 3

“FIG. 4 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards with the same semiconductor package 100 as in Embodiment 1. Reference numeral 301 denotes a circuit board, which includes an insulation material 303, a wiring pattern 304 and an inner via 305. On the circuit board 301, a semiconductor chip 306 and chip components 308, 309 and 310 are mounted. The semiconductor package 100 has the same configuration as shown in FIG. 1, and has protruding electrodes 105 and 106. The semiconductor package 100 connects electrically and mechanically with another circuit board 312 by means of firm securing using solder.” Nakatani, [0095].

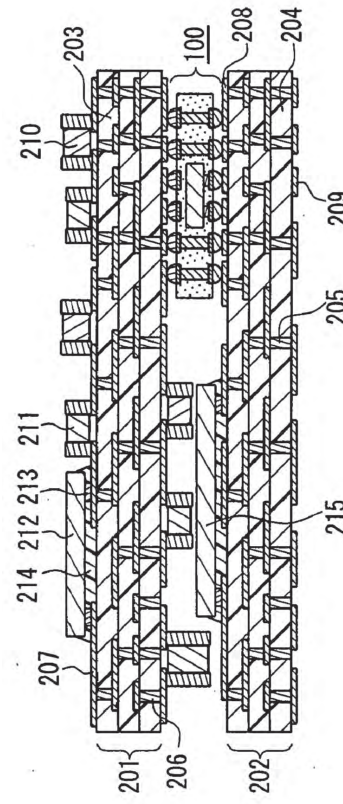
“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and

	<p>therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively. Available insulation materials of the circuit boards, as in the case of Embodiment 1, are a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric and the like that are impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin and the like. Reference numerals 186 and 209 denote wiring patterns of the circuit boards 180 and 181, and 185 and 184 denote inner vias that connect layers. On the circuit boards 180 and 181, semiconductor chips 190 and 191 and chip components 188 and 189 are mounted. As for the semiconductor chips, a flip-chip packaging method is available, and the semiconductor chips 190 and 191 are connected with wiring patterns on the circuit boards via bumps. In order to electrically connect the circuit boards 180 and 181 with a narrow pitch, this embodiment shows an</p>
--	--

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>example where two semiconductor packages are used. By using the two semiconductor packages 100 and 900 for connecting circuit boards 180 and 181 in the vicinity of both end portions of the circuit boards as in FIG. 13, a package that not only allows the electrical connection with a narrow pitch but also provides an excellent mechanical strength can be obtained.” Nakatani, [0116-0118].</p> <p>“Next, as shown in FIG. 8, the circuit board 301 and the circuit board 312 were electrically connected via the protruding electrodes using the above-stated semiconductor package 600, and at the same time the circuit boards 301 and 312 were firmly bonded and secured to each other using solder. More specifically, as the circuit board 301 having an inner via structure across the entire layers, a four-layered wiring structured aramid epoxy resin board was used. Nickel and gold plating were applied to a wiring pattern of this aramid epoxy resin board in the same manner as above so as to facilitate soldering, and a solder paste was printed using a metal mask on the wiring pattern subjected to the gold plating. The material of the solder used was Pb free solder made of SnAgCu. The above-stated semiconductor package 600 was aligned with the portions where the solder had been printed and was mounted thereon.” Nakatani, [0147-0148].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and	<p>Nakatani discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p>See, e.g.:</p>

	<p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder. At this time, by binding the semiconductor package 100 and the wiring patterns 208 of the circuit boards 201 and 202 with an encapsulation resin, still firmer bonding can be carried out. Thereby, the semiconductor package 100 is not used just as an electrical connector between the circuit board 201 and the circuit board 202, but various functions possessed by the semiconductor package 100, such as a processing function, a switching function and a memory holding function, also can be utilized. As a</p>
--	--

	<p>result, a high-performance, precision and compact package can be realized.” Nakatani, [0092-0093].</p>  <p style="text-align: center;">FIG. 3</p> <p>Nakatani, FIG. 3</p> <p>“In FIG. 10, reference numeral 802 denotes a circuit board in which insulation layers and wiring patterns are formed in an arbitrary laminated manner, and these layers are connected with an inner via. On the circuit board 802, a semiconductor chip 801 is mounted, and the semiconductor chip 801 is connected with a wiring pattern on the circuit 802 via a wire 803.” Nakatani, [0108].</p> <p>“In FIG. 11, reference numeral 902 denotes a circuit board in which insulation layers and wiring patterns are formed in an arbitrary laminated manner, and these layers are connected with an inner via, as in the case of the previous embodiment. On the circuit board 902, a semiconductor chip 901 is mounted by a flip-chip packaging method, and the semiconductor</p>
--	--

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>chip 901 is connected with a wiring pattern on the circuit board 902 via a bump 903.” Nakatani, [0112].</p> <p>“Next, as shown in FIG. 14C, the other semiconductor chip 162 is die-bonded in the same manner as stated above. At this time, the semiconductor chip 162 is mounted on a circuit-face of the semiconductor chip 161, and therefore the circuit-face of the semiconductor chip 161 is preferably protected with an insulation film made of polyimide and the like.” Nakatani, [0122].</p> <p>“Next, a conductive paste was applied at portions where semiconductor chips are to be mounted on a surface of the aramid epoxy multilayered board, and subsequently thirty-six semiconductor chips in total (10 mm10 mm, thickness 0.2 mm) were mounted in a matrix form of 66. A heat treatment was conducted to the multilayered board on which the semiconductor chips had been mounted at 150 C. for 30 minutes, so as to cure the conductive adhesive.” Nakatani, [0130].</p> <p>“Furthermore, another semiconductor chip was mounted on each of the semiconductor chips using a conductive adhesive in a similar manner as stated above.” Nakatani, [0130].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.M] the at least one spacer connector comprises two spacer connectors	<p>Nakatani discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>

<p>arranged on opposite sides of the bottom chip.</p>	<p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder. At this time, by binding the semiconductor package 100 and the wiring patterns 208 of the circuit boards 201 and 202 with an encapsulation resin, still firmer bonding can be carried out. Thereby, the semiconductor package 100 is not used just as an electrical connector between the circuit board 201 and the circuit board 202, but various functions possessed by the semiconductor package 100, such as a processing</p>
---	--

function, a switching function and a memory holding function, also can be utilized. As a result, a high-performance, precision and compact package can be realized.” Nakatani, [0092-0093].

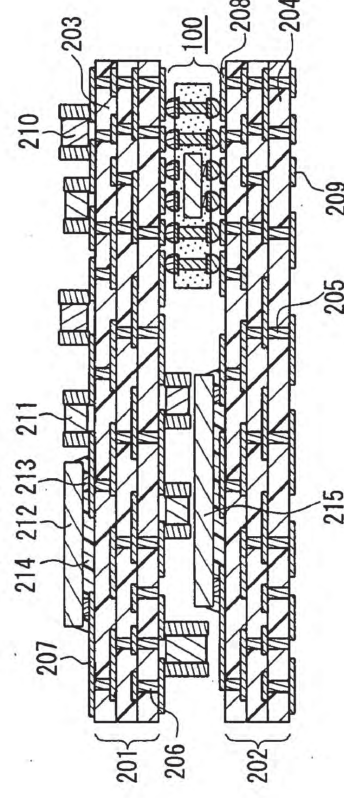
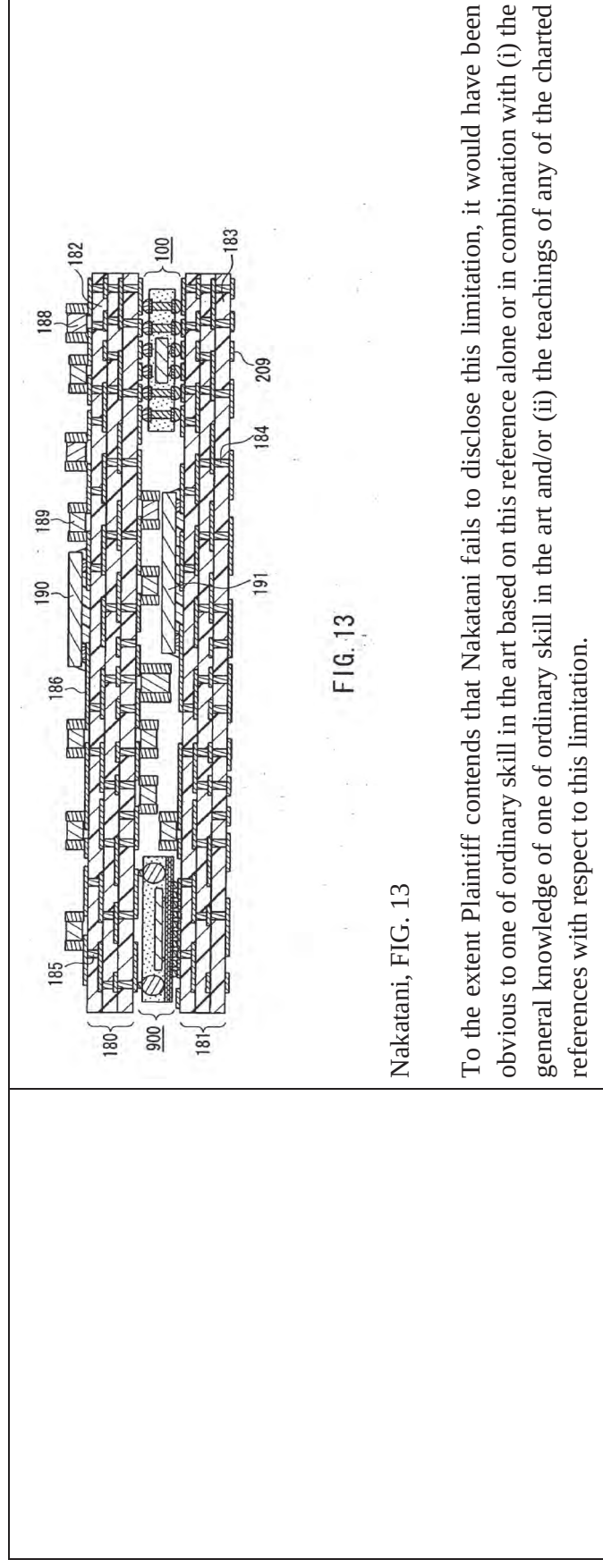


FIG. 3

Nakatani, FIG. 3

“On the circuit boards 180 and 181, semiconductor chips 190 and 191 and chip components 188 and 189 are mounted.” Nakatani, [0093].

“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively.” Nakatani, [0116].



Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	Nakatani discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate. <i>See, e.g.:</i>

	<p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].</p>
--	---

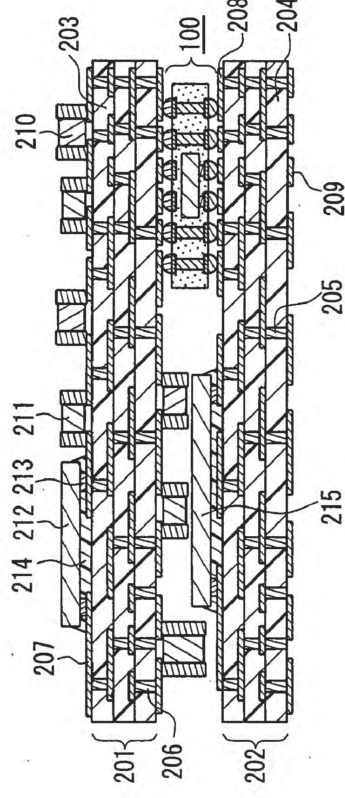


FIG. 3

Nakatani, FIG. 3

“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder. At this time, by binding the semiconductor package 500 and the wiring patterns 208 of the circuit boards 201 and 202 with an encapsulation resin, still firmer bonding can be carried out.” Nakatani, [0101].

“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The

	<p>remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder. At this time, by binding the semiconductor package 600 and the wiring patterns of the circuit boards 301 and 312 with an encapsulation resin, still firmer bonding can be carried out.” Nakatani, [0104].</p> <p>“FIG. 13 is a cross-sectional view showing a configuration in which circuit boards are connected electrically by using the semiconductor package 900 of this embodiment and the semiconductor package 100 of FIG. 1. Reference numerals 180 and 181 denote circuit boards to be electrically-connected, and 182 and 183 denote insulation materials of the circuit boards 180 and 181, respectively. Available insulation materials of the circuit boards, as in the case of Embodiment 1, are a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric and the like that are impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin and the like. Reference numerals 186 and 209 denote wiring patterns of the circuit boards 180 and 181, and 185 and 184 denote inner vias that connect layers. On the circuit boards 180 and 181, semiconductor chips 190 and 191 and chip components 188 and 189 are mounted. As for the semiconductor chips, a flip-chip packaging method is available, and the semiconductor chips 190 and 191 are connected with wiring patterns on the circuit boards via bumps.” Nakatani, [0116-0117].</p> <p>“Next, as shown in FIG. 14C, the other semiconductor chip 162 is die-bonded in the same manner as stated above. At this time, the semiconductor chip 162 is mounted on a circuit-face of the semiconductor chip 161, and therefore the circuit-face of the semiconductor chip 161 is preferably protected with an insulation film made of polyimide and the like. Reference numeral 170 denotes an electrode formed at a surface of the semiconductor chip 162. Next,</p>
--	--

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>as shown in FIG. 14D, encapsulation is conducted with an encapsulation resin 165 up to the circuit face of the semiconductor chip 162. As for the encapsulation resin, the materials shown in Embodiment 1 may be used. Alternatively, the encapsulation may be conducted so as to cover the entire semiconductor chip 162, and thereafter grinding may be conducted so as to reach the electrode at the surface of the semiconductor chip 162.” Nakatani, [0122-0123].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Nakatani discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are</p>

	<p>electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214.” Nakatani, [0092-0093].</p>
--	--

	<div></div> <div><p>FIG. 3</p></div> <div><p>Nakatani, FIG. 3</p></div> <div><p>“FIG. 4 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards with the same semiconductor package 100 as in Embodiment 1. Reference numeral 301 denotes a circuit board, which includes an insulation material 303, a wiring pattern 304 and an inner via 305. On the circuit board 301, a semiconductor chip 306 and chip components 308, 309 and 310 are mounted. The semiconductor package 100 has the same configuration as shown in FIG. 1, and has protruding electrodes 105 and 106. The semiconductor package 100 connects electrically and mechanically with another circuit board 312 by means of firm securing using solder.” Nakatani, [0095].</p></div> <div><p>“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and</p></div>
--	---

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0104].</p> <p>“FIG. 8 is a cross-sectional view of an electronic component packaging structure that electrically connects circuit boards using the above-stated semiconductor package 600. The remaining components and configurations are the same as in those of FIG. 3, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	Nakatani discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>See, e.g.:</p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection.” Nakatani, [0092].</p>
--	--

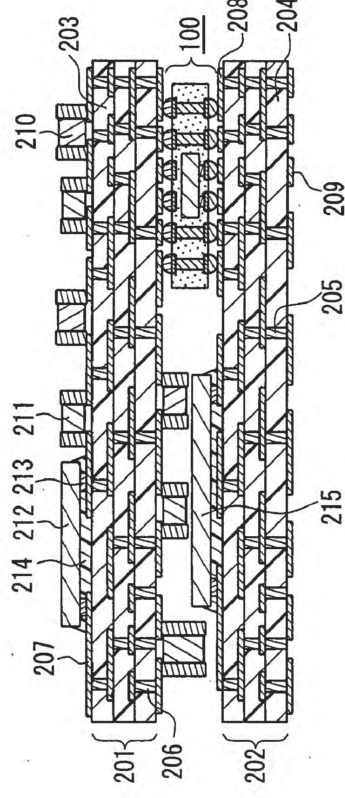


FIG. 3

Nakatani, FIG. 3

“Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0093]

“The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder.” Nakatani, [0101].

“The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>“On the circuit boards 180 and 181, semiconductor chips 190 and 191 and chip components 188 and 189 are mounted. As for the semiconductor chips, a flip-chip packaging method is available, and the semiconductor chips 190 and 191 are connected with wiring patterns on the circuit boards via bumps.” Nakatani, [0117].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the top package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the bottom package substrate are connected to the corresponding top ends of the plurality of metal pillars of the	<p>Nakatani discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are</p>

spacer connector via the corresponding top metal pads of the spacer connector.

electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers.” Nakatani, [0092].

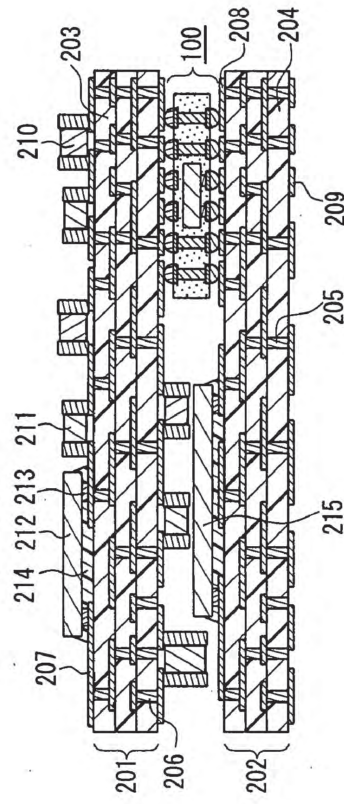


FIG. 3

Nakatani, FIG. 3

“Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105 and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0093].

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

	<p>“The semiconductor package 600 electrically connects a circuit board 301 and a circuit board 312 via protruding electrodes, and at the same time bonds the circuit board 301 and the circuit board 312 firmly using solder.” Nakatani, [0104].</p> <p>“In FIG. 10, reference numeral 802 denotes a circuit board in which insulation layers and wiring patterns are formed in an arbitrary laminated manner, and these layers are connected with an inner via. On the circuit board 802, a semiconductor chip 801 is mounted, and the semiconductor chip 801 is connected with a wiring pattern on the circuit 802 via a wire 803. Another wiring pattern on the circuit board 802 is connected with a lead frame 804 via a wire 805. The lead frame 804 is bent as shown in FIG. 10 so as to prevent the wire 805 connected therewith by the wire bonding from being exposed to the surface of the semiconductor package. Reference numeral 809 denotes a wiring pattern formed at a surface of the circuit board 802, and a protruding electrode 807 is formed on a surface of this wiring pattern 809” Nakatani, [0108].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a	Nakatani discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the

Appendix A-26 - Invalidity of U.S. Patent No. 9859202 in view of Nakatani - U.S. Patent Publication No. 20040227258

<p>plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view of an electronic component packaging structure in which circuit boards are connected electrically with each other using the above-stated semiconductor package 100. Reference numerals 201 and 202 denote circuit boards that are electrically connected, and 203 and 204 denote insulation materials of the circuit boards 201 and 202. Available insulation materials of the circuit boards include a reinforcing member made of paper, glass woven fabric, glass non-woven fabric, aramid non-woven fabric or the like that is impregnated with an organic resin made of epoxy resin, cyanate resin, phenol resin or the like. Reference numerals 207, 208 and 209 denote wiring patterns, and 206 and 205 denote inner vias that connect layers. As the wiring patterns, copper foil can be used, for example, to which chemical etching can be applied so as to form a desired wiring pattern. As for the inner vias 205 and 206, copper plating or a conductive paste is applied to holes processed with a drill or a laser, so as to establish electric connection. On the circuit boards 201 and 202, semiconductor chips 215 and 212 and chip components 211 and 210 are mounted. A method for the mounting is not limited to a mounting method using solder, but a conductive adhesive can be used. As for the semiconductor chips, wire bonding, flip-chip bonding and the like are available, and the semiconductor chips 215 and 212 may be flip-chip mounted via bumps 213 and may be encapsulated with an encapsulation resin 214. Reference numeral 100 denotes the semiconductor package shown in FIG. 1, which connects electrically the circuit board 201 and the circuit board 202 via the protruding electrodes 105</p>
--	--

and 106, and at the same time allows the circuit boards 201 and 202 to be bonded and secured firmly with each other using solder.” Nakatani, [0092-0093].

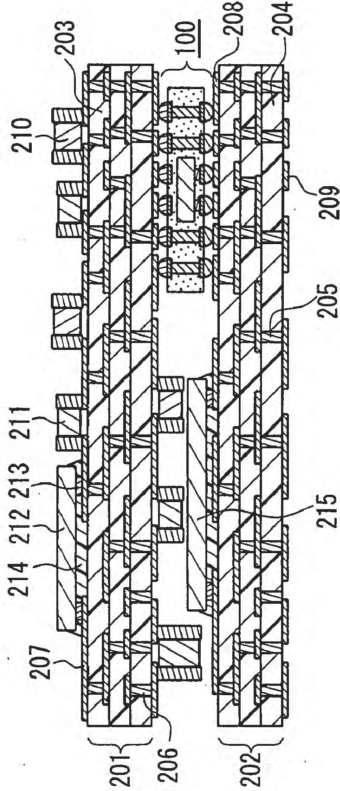


FIG. 3

Nakatani, FIG. 3

“FIG. 5 is a cross-sectional view showing a configuration of a semiconductor package 500 according to this embodiment. In FIG. 5, reference numeral 501 denotes a semiconductor chip and 502 denotes another semiconductor chip. The semiconductor chips 501 and 502 face each other with rear faces opposite to their circuit-face side. The respective circuit faces are connected electrically with protruding electrodes 503 and 505. Reference numerals 506 a and 506 b are base electrodes that are formed at surfaces of the semiconductor chips 501 and 502, respectively. Reference numeral 504 denotes an electrical insulating encapsulation resin molded member, which protects the semiconductor chips 501 and 502. The semiconductor chips 501 and 502 are secured with each other at their rear faces via an adhesive, encapsulation is conducted up to the same height as each of the surfaces of the circuit-faces

	<p>using a transfer molding device, and thereafter the protruding electrodes 503 and 505 are mounted on electrodes on the circuit-faces of the respective semiconductor chips 501 and 502 using a solder ball and the like.” Nakatani, [0098-0099].</p> <p>“FIG. 6 is a cross-sectional view showing an electronic component packaging structure that electrically connects circuit boards by using the above-described semiconductor package 500. The remaining components and configurations are the same as in those of FIG. 2, and therefore the same reference numerals are used and their explanations are omitted. Only essential points are described below. The semiconductor package 500 electrically connects the circuit board 201 and the circuit board 202 via protruding electrodes, and at the same time bonds the circuit board 201 and the circuit board 202 firmly using solder. At this time, by binding the semiconductor package 500 and the wiring patterns 208 of the circuit boards 201 and 202 with an encapsulation resin, still firmer bonding can be carried out.” Nakatani, [0101].</p> <p>“Finally, solder balls with a diameter of 0.4 mm were mounted on the multilayered board and the semiconductor chip electrodes using a solder ball mounter. Thus, the semiconductor package was manufactured by the above-stated method. On the wiring pattern of the semiconductor module of the present invention, a semiconductor chip and an electronic component further can be mounted, and therefore a significantly high-density packaged semiconductor module can be obtained. The thus manufactured semiconductor package not only allows circuit boards to be connected with each other, but also has an especially good effect of allowing a semiconductor chip and a passive component to be mounted on protruding electrodes manufactured on a side of the semiconductor chip as well, thus enabling a still higher-density package.” Nakatani, [0143-0145].</p>
--	--

	<p>“Next, as shown in FIG. 8, the circuit board 301 and the circuit board 312 were electrically connected via the protruding electrodes using the above-stated semiconductor package 600, and at the same time the circuit boards 301 and 312 were firmly bonded and secured to each other using solder. More specifically, as the circuit board 301 having an inner via structure across the entire layers, a four-layered wiring structured aramid epoxy resin board was used. Nickel and gold plating were applied to a wiring pattern of this aramid epoxy resin board in the same manner as above so as to facilitate soldering, and a solder paste was printed using a metal mask on the wiring pattern subjected to the gold plating. The material of the solder used was Pb free solder made of SnAgCu. The above-stated semiconductor package 600 was aligned with the portions where the solder had been printed and was mounted thereon. Thereafter, by using a solder reflow device, soldering was conducted on the aramid epoxy resin board 301 on which the semiconductor package 600 had been mounted. The reflow was conducted under the profile of once keeping a temperature at 150 C. and then applying heat so as to reach 250 C., where the state at 250 C. was kept for about 10 seconds. As a result, protruding electrodes on the semiconductor package 600 and the wiring pattern 304 on the aramid epoxy resin board 301 were connected electrically and mechanically using the solder. Next, other protruding electrodes on the semiconductor package 600 and the wiring pattern of the FPC 312 were connected.” Nakatani, [0147-0148].</p> <p>To the extent Plaintiff contends that Nakatani fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

U.S. Patent No. 6521530 (“Peters”) is titled Composite Interposer and Method for Producing a Composite Interposer and lists Michael G. Peters, Mark Thomas McCormack, and Aris Bernales as inventors. Peters is assigned to Fujitsu Limited. Peters anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Peters is a U.S. patent that was filed May 23, 2001 and published June 20, 2002. Peters claims priority to US 6,081,026 filed on November 13, 1998. Peters is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Peters, or otherwise rendered obvious by disclosures and teachings of Peters, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Peters does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Peters with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Peters, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Peters “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

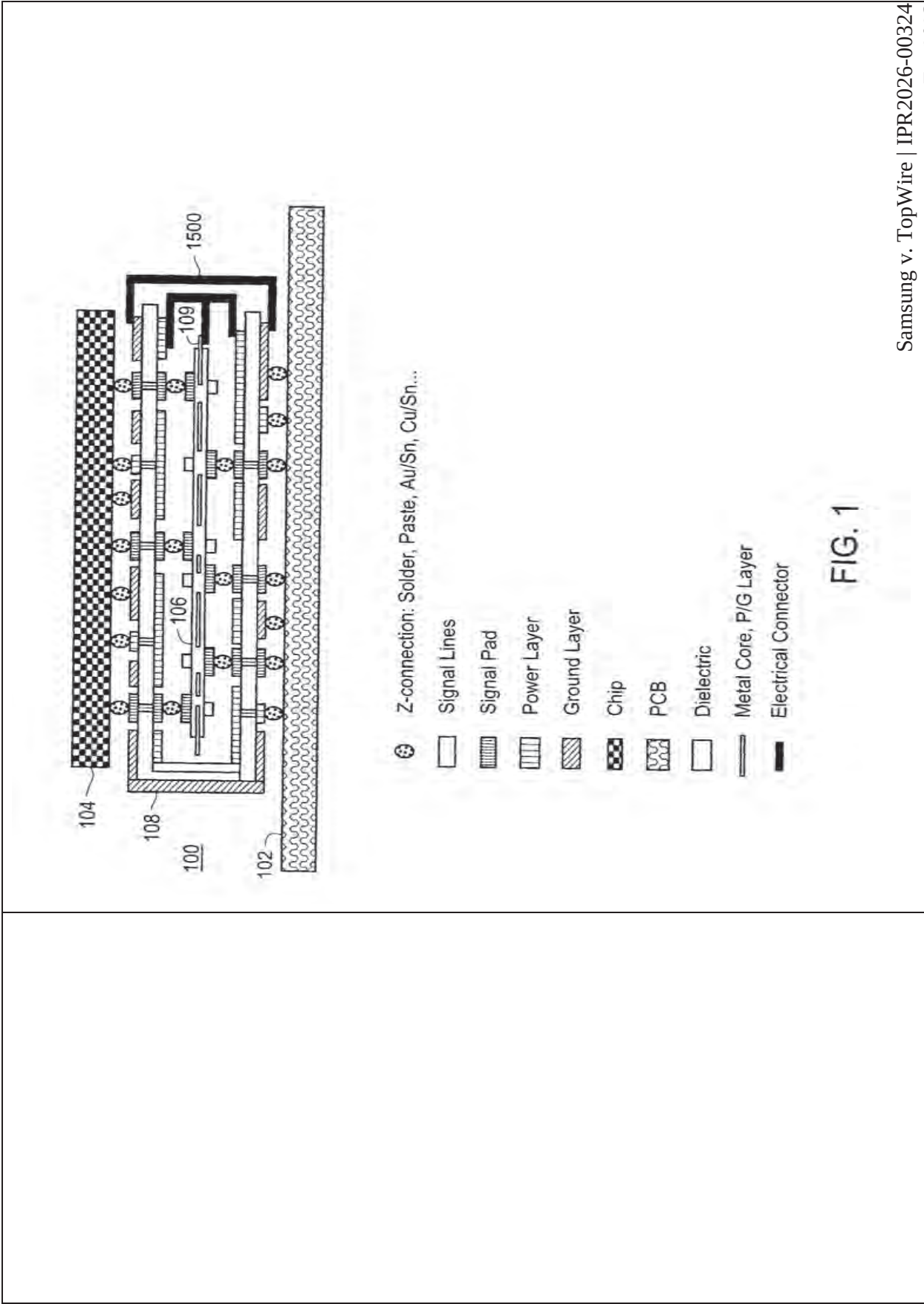
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Peters or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Peters set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Peters discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology,</p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	e.g., solder bumps, anisotropic conducting polymers, or another suitable method.” Peters, [7:36-7:46].
--	--



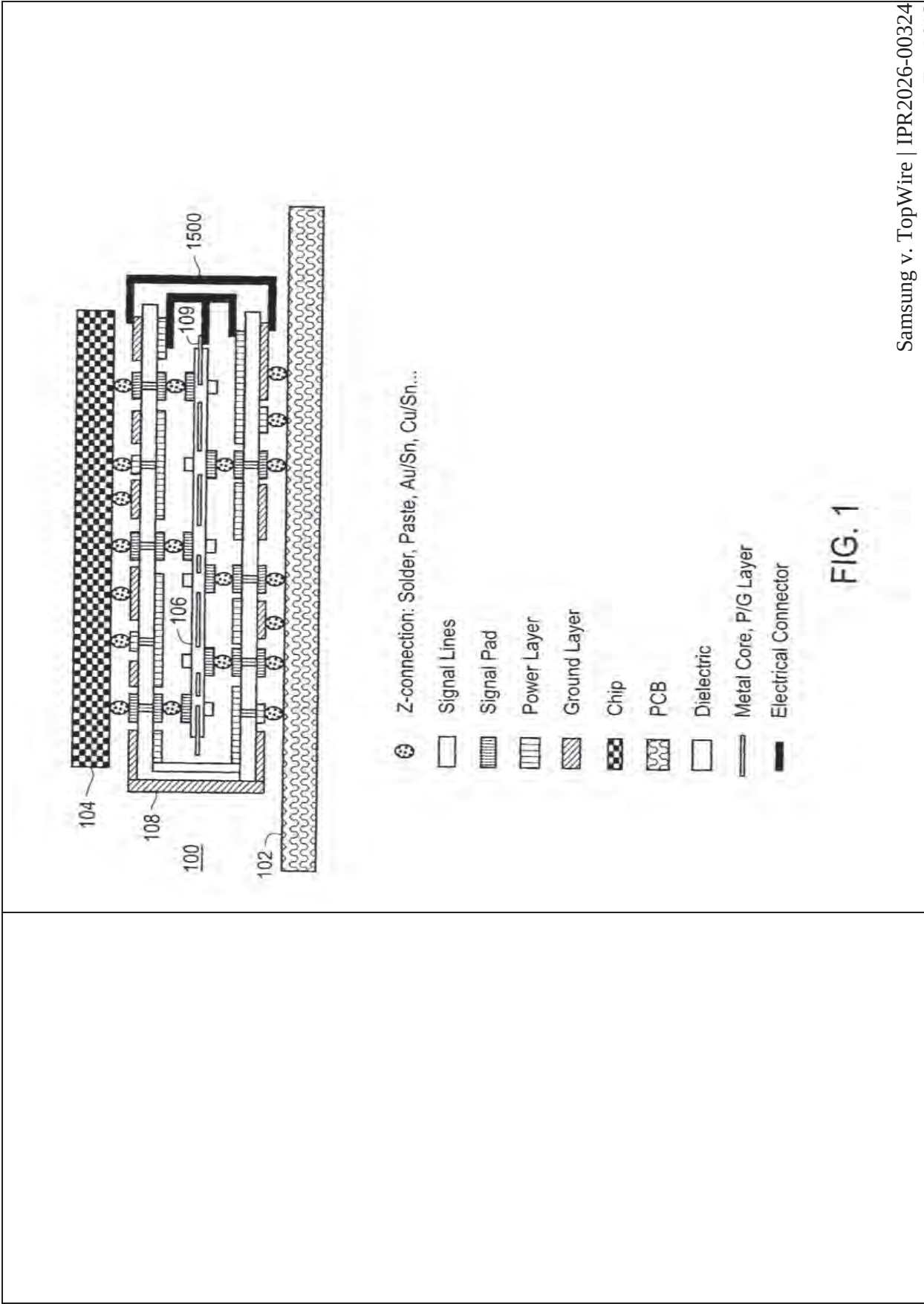
	<p>Peters, FIG. 1</p> <p>“FIG. 3 is a schematic cross-sectional view of one embodiment of the circuit signal core 106 which is part of the interposer of the present invention. Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106. A dielectric film 110 (e.g., Polyimide, BT, etc.) is arranged on both sides of conductive core 111. Signal lines 113 are defined on a patterned metal layer formed on each of the two dielectric film layers. The two patterned metal layers are interconnected as desired by either a through via or a conductive post structure 112, with the through via or conductive post being suitable for interconnecting the signal core to other layers of the interposer structure, or to the mounting substrate or integrated circuit chips.” Peters, [8:18-8:34].</p> <p>“Referring now to FIG. 5, there is seen a schematic cross-sectional view of power ground wrap 108 which is part of embodiments of the interposer of the present invention. Power ground wrap 108 is formed from a dielectric film 120 (e.g. Polyimide, Bt, etc.) on both sides of which is patterned a metal layer. The two metal layers are interconnected as desired by either a through via or conductive post. Substrate 120 is formed into the shape shown in the figure, i.e., a box-shaped structure having a space between an upper and lower substrate.” Peters, [8:51-8:60].</p> <p>“With the signal core of FIG. 4 inserted between the upper and lower substrates of the power/ground wrap, signal connections may be made between the base substrate (element 102 of FIG. 2), the signal core, and the integrated circuit chip(s) in isolation from the power and ground connections between the base substrate and the chip(s). This permits an increase</p>
--	--

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>in signal line density and minimization of signal path lengths while achieving a high degree of electrical isolation between the different types of lines.” Peters, [9:17-9:26].</p> <p>“FIG. 16 discloses a four (4) micro-singulated silicon die 160 surrounding a voltage pad area, generally illustrated as 164. Each micro-singulated silicon die 160 is segmented into four (4) discrete capacitor areas, which are typically necessary to provide high capacitance values with >Ghz resonance frequencies. Each of the segmented discrete capacitor areas on the singulated die 160 may be multilayer parallel capacitors. A top layer 168 (see FIG. 16) of common ground shielding is provided.” Peters, [15:18-15:26].</p>
[1.A] a bottom package substrate;	<p>Peters discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 15 is a schematic cross-sectional view of another embodiment of the composite interposer of the present inventions positioned between a printed circuit board and an integrated circuit chip. FIG. 16 is a top plan view of the composite interposer of FIG.” Peters, [6:21-6:26].</p> <p>“FIG. 2 is a schematic cross-sectional view of another embodiment of the signal interposer 100 positioned between the printed board 102 and the integrated circuit chip 104.” Peters, [8:14-8:17].</p> <p>“With the signal core of FIG. 4 inserted between the upper and lower substrates of the power/ground wrap, signal connections may be made between the base substrate (element 102 of FIG. 2), the signal core, and the integrated circuit chip(s) in isolation from the power and ground connections between the base substrate and the chip(s).” Peters, [9:17-9:23].</p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method.” Peters, [12:65-13:8].</p>
--	---

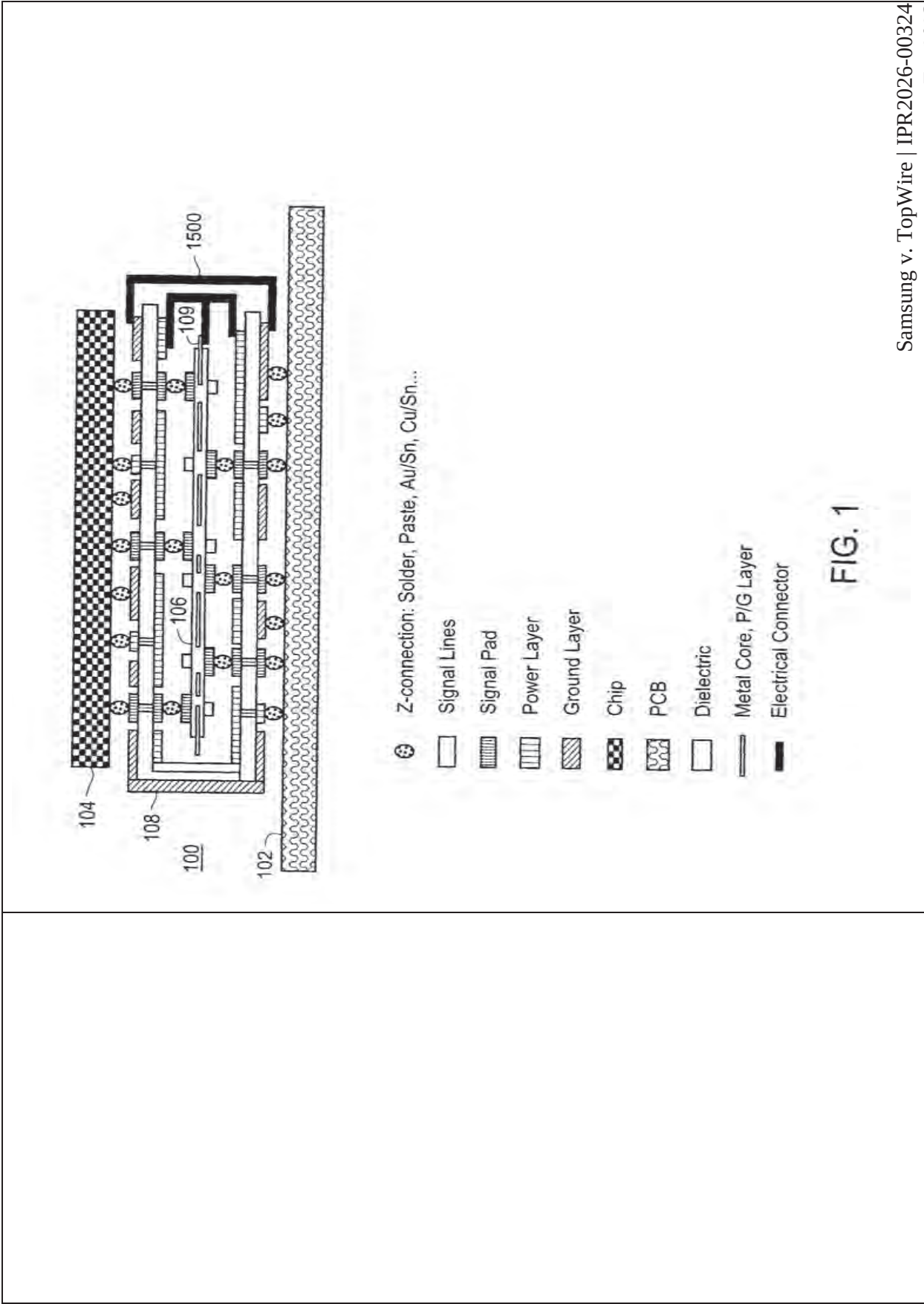


Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>Peters, FIG. 1</p> <p>“FIG. 14 is a schematic cross-sectional view of a different construction of the reduced cross-talk signal interposer of the present invention, and is shown positioned between a printed circuit board and an integrated circuit chip.” Peters, [12:65-13:1].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Peters discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 15 is a schematic cross-sectional view of another embodiment of the composite interposer of the present inventions positioned between a printed circuit board and an integrated circuit chip. FIG. 16 is a top plan view of the composite interposer of FIG.” Peters, [6:21-6:26].</p> <p>“FIG. 2 is a schematic cross-sectional view of another embodiment of the signal interposer 100 positioned between the printed board 102 and the integrated circuit chip 104. FIG.” Peters, [8:14-8:18].</p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104.” Peters, [12:65-13:1].</p>
--	---



Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>Peters, FIG. 1</p> <p>“FIG. 14 is a schematic cross-sectional view of a different construction of the reduced cross-talk signal interposer of the present invention, and is shown positioned between a printed circuit board and an integrated circuit chip.” Peters, [12:65-13:1].</p> <p>“In FIGS. 17-23 there is illustrated a process flow of a method for fabricating one embodiment of the composite interposer 101. In the process step illustrated in FIG. 17, a silicon layer 170 (e.g. a previously processed and tested silicon wafer) having a thickness ranging from about 100 m to about 300 m, such as about 200 m, is adhesively attached to the circuit board 102 (i.e., an organic board).” Peters, [15:33-15:39].</p> <p>“In FIG. 67, two mating (and similarly processed) substrates 380 380 are aligned (one or both of which may be conventional rigid printed circuit board, printed circuit flex, semiconductor, glass or ceramic) such that the solder bumps 396 a 396 a are in contact with mating pads possessing a solder wettable surface (e.g. Au, Au/Ni, Cu, Pd, In, Sn, or solder alloys).” Peters, [25:52-25:58].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom</p>	<p>Peters discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p>

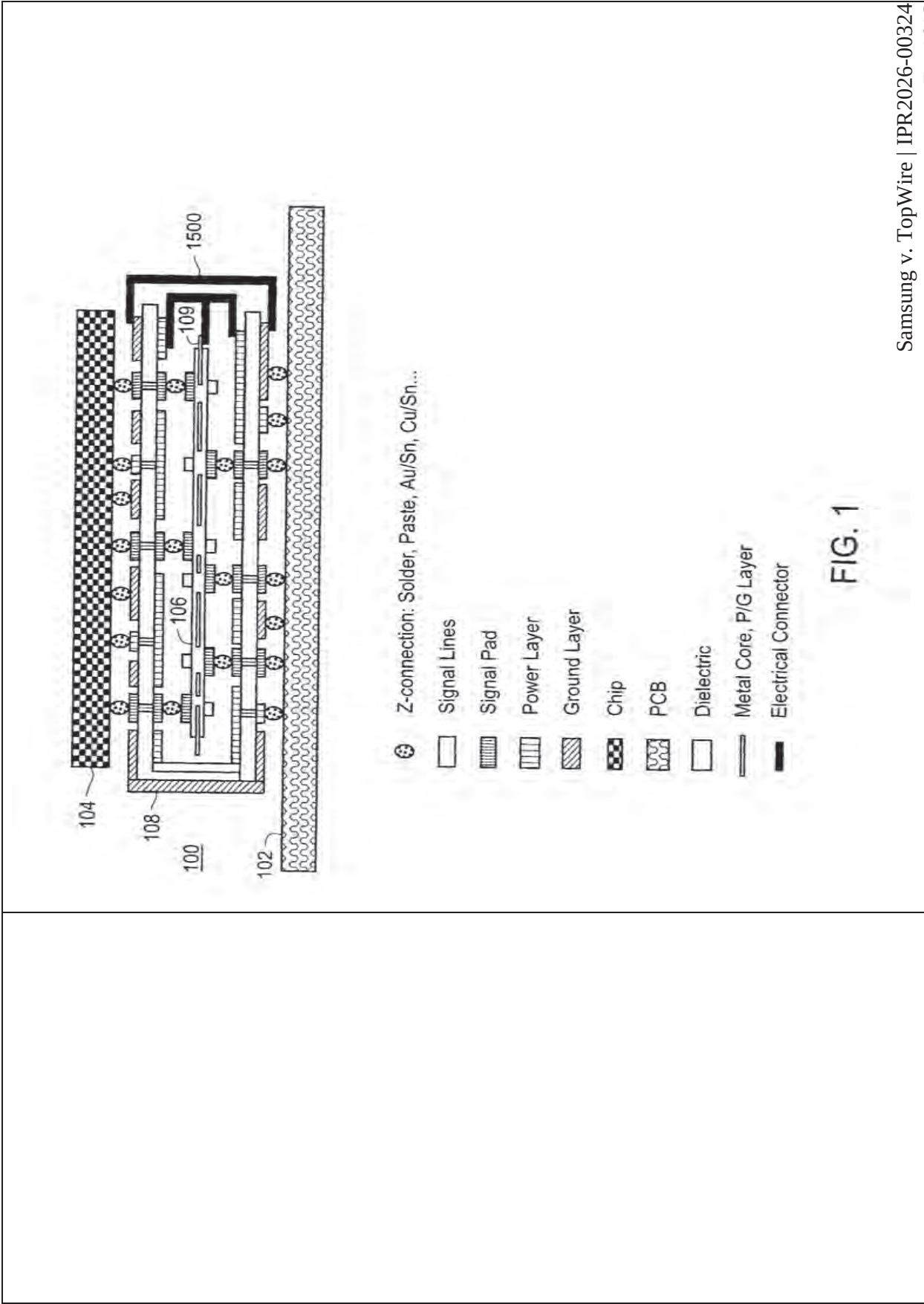
Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

package substrate and the top package substrate, wherein	<p><i>See, e.g.:</i></p> <p>“As shown in FIG. 1, edge connectors 1500 may be used to electrically connect different ground layers (e.g., the lower surface of the lower power/ground substrate to the upper surface of the upper power/ground substrate), different power layers (e.g., the upper surface of the lower power/ground substrate to the lower surface of the upper power/ground substrate), or the power/ground layer of the signal core to other ground or power layers of the interposer. Although a single set of edge connectors 1500 is shown in the figure, note that if the upper and lower power/ground substrates are fabricated separately (rather than formed from a flexible substrate which is bent into a U shape), then a set of connectors 1500 may be used at both ends of the two power/ground substrates.” Peters, [8:1-8:14].</p> <p>“FIG. 2 is a schematic cross-sectional view of another embodiment of the signal interposer 100 positioned between the printed board 102 and the integrated circuit chip 104.” Peters, [8:14-8:17].</p> <p>“FIG. 3 is a schematic cross-sectional view of one embodiment of the circuit signal core 106 which is part of the interposer of the present invention. Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106. A dielectric film 110 (e.g., Polyimide, BT, etc.) is arranged on both sides of conductive core 111. Signal lines 113 are defined on a patterned metal layer formed on each of the two dielectric film layers. The two patterned metal layers are interconnected as desired by either a through via or a conductive post structure 112, with the through via or conductive post being suitable for interconnecting the signal core to other layers of the interposer structure, or to the mounting substrate or integrated circuit chips.” Peters, [8:18-8:34].</p>
--	--

	<p>“Referring now to FIG. 5, there is seen a schematic cross-sectional view of power ground wrap 108 which is part of embodiments of the interposer of the present invention. Power ground wrap 108 is formed from a dielectric film 120 (e.g. Polyimide, Bt, etc.) on both sides of which is patterned a metal layer. The two metal layers are interconnected as desired by either a through via or conductive post. Substrate 120 is formed into the shape shown in the figure, i.e., a box-shaped structure having a space between an upper and lower substrate.” Peters, [8:51-8:60].</p> <p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method. This reduces the cycle time for manufacturing and testing of the structure, and increases the types of processing techniques which may be used to form the different parts of the final structure. As shown in the figure, in accordance with the present invention, power and ground interconnections are routed between the mounting substrate 102 and the chip(s) 104 without passing through the signal core 106. On the other hand, the signal lines are routed between the mounting substrate 102 and the chip(s) 104 by passing only through the signal core. This architecture provides electrical isolation between the power, ground, and signal interconnections (and hence reduces noise and other problems caused by capacitive coupling between lines) while increasing the density of signal lines which can be connected between the substrate and chip(s). Signal core 106 includes a power/ground layer 109 positioned between signal layers which are on either side of that substrate and together form the basis</p>
--	--

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	for the signal core. Power/ground layer 109 acts to reduce cross-talk between signal lines on the same or different signal layers of signal core 106.” Peters, [12:65-13:30].
--	---



Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>Peters, FIG. 1</p> <p>“FIG. 14 is a schematic cross-sectional view of a different construction of the reduced cross-talk signal interposer of the present invention, and is shown positioned between a printed circuit board and an integrated circuit chip. In this situation, the need for precise alignment between the top, bottom, and sides of the wrap and the signal core (which is present in the method described previously with respect to FIG. 13) is lessened. Instead, the top and bottom substrates of the ground/power layers may be fabricated as separate substrates (instead of being formed by bending a single flexible substrate) and assembled to the signal core separately. Edge connectors 1500, 1502 are used to interconnect the power/ground layers between the two power/ground substrates and the power/ground layer of the signal core as needed.” Peters, [12:65-13:12].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Peters discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a schematic cross-sectional view of one embodiment of the circuit signal core 106 which is part of the interposer of the present invention. Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106. A</p>

dielectric film 110 (e.g., Polyimide, BT, etc.) is arranged on both sides of conductive core 111.” Peters, [5:44-5:54].

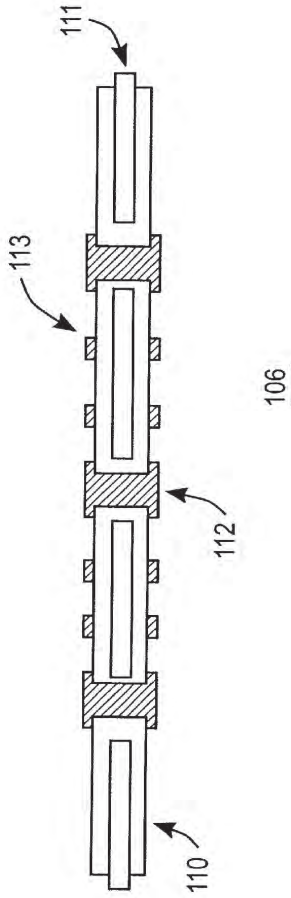


FIG. 3

Peters, FIG. 3

“FIG. 3 is a schematic cross-sectional view of one embodiment of the circuit signal core 106 which is part of the interposer of the present invention. Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106.” Peters, [8:18-8:25].

“Referring now to FIG. 5, there is seen a schematic cross-sectional view of power ground wrap 108 which is part of embodiments of the interposer of the present invention. Power ground wrap 108 is formed from a dielectric film 120 (e.g. Polyimide, Bt, etc.) on both sides

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>of which is patterned a metal layer. The two metal layers are interconnected as desired by either a through via or conductive post. Substrate 120 is formed into the shape shown in the figure, i.e., a box-shaped structure having a space between an upper and lower substrate.” Peters, [8:51-8:60].</p> <p>“FIGS. 6 (a) to 6 (g) show a process flow for one preferred method of fabricating the signal core which is part of the reduced cross-talk interposer of embodiments of the present invention. In the process flow shown in FIG. 6, the metal layers on the two sides of the core substrate are interconnected by a through via. As shown in the figures, the process flow begins with a conductive layer, which may be formed from a suitable metal 202 (FIG. 6 (a))). Holes or apertures are formed in layer 202 at the positions where through vias or conductive posts will later be formed (FIG. 6 (b)). A dielectric layer 204 is then formed on each surface of conductive layer 202.” Peters, [9:33-9:44].</p> <p>“FIGS. 12 (a) to 12 (g) illustrate a process flow for an additional method of fabricating the signal core which is part of the reduced cross-talk interposer of the present invention. In the process flow shown in FIG. 12, a conductive layer 1202 again has holes or apertures formed through it at desired locations (FIGS. 12 (a) and 12 (b)). A dielectric layer 1204 is formed (e.g., laminated) onto one surface of conductive layer 1202.” Peters, [11:35-11:42].</p> <p>“In FIG. 60, a high density print circuit substrate 380 made or comprising a polymer laminate board, ceramic, glass or flexible circuit made from a dielectric film (such as polyimide) with one or two sides of conductive metal circuitry (e.g., pads 382 and 384 in contact with metal filled vias 386) is shown.” Peters, [24:46-24:51].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Peters discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106. A dielectric film 110 (e.g., Polyimide, BT, etc.) is arranged on both sides of conductive core 111. Signal lines 113 are defined on a patterned metal layer formed on each of the two dielectric film layers. The two patterned metal layers are interconnected as desired by either a through via or a conductive post structure 112, with the through via or conductive post being suitable for interconnecting the signal core to other layers of the interposer structure, or to the mounting substrate or integrated circuit chips.” Peters, [8:20-8:34].</p>

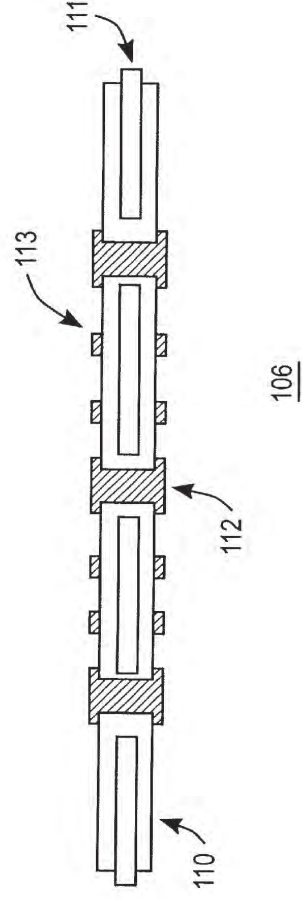


FIG. 3

Peters, FIG. 3

“FIGS. 6 (a) to 6 (g) show a process flow for one preferred method of fabricating the signal core which is part of the reduced cross-talk interposer of embodiments of the present invention. In the process flow shown in FIG. 6, the metal layers on the two sides of the core substrate are interconnected by a through via. As shown in the figures, the process flow begins with a conductive layer, which may be formed from a suitable metal 202 (FIG. 6 (a)). Holes or apertures are formed in layer 202 at the positions where through vias or conductive posts will later be formed (FIG. 6 (b)). A dielectric layer 204 is then formed on each surface of conductive layer 202. Dielectric layers 204 may be laminated onto each surface of layer 202 (FIGS. 6 (c) and 6 (d)). Vias 206 are formed through dielectric layers 204 in the locations corresponding to the predefined apertures in conductive layer 202 (FIG. 6 (e)). Vias 206 may be formed by means of a laser drill or plasma etch process. Vias 206 are then metallized and a seed layer 208 is deposited on the surface of each dielectric layer

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>204 using electroless plating, direct plating, sputtering, or another suitable process (FIG. 6 (f)).” Peters, [9:33-9:52].</p> <p>“FIGS. 12 (a) to 12 (g) illustrate a process flow for an additional method of fabricating the signal core which is part of the reduced cross-talk interposer of the present invention. In the process flow shown in FIG. 12, a conductive layer 1202 again has holes or apertures formed through it at desired locations (FIGS. 12 (a) and 12 (b)). A dielectric layer 1204 is formed (e.g., laminated) onto one surface of conductive layer 1202. A dielectric having a previously formed metallized surface or layer 1205 is then laminated onto the other surface of conductive layer 1202 (FIGS. 12 (c) and 12 (d)). Vias 1206 are formed through dielectric layers 1204 in the locations corresponding to the predefined apertures in conductive layer 1202 (FIG. 12 (e)). Vias 1206 may be formed by means of a laser drill or plasma etch process.” Peters, [11:35-11:48].</p> <p>“Referring now to FIGS. 24-30 for another embodiment of the present invention, instead of dielectric layer 190 being employed to fill openings 184 and 196 and to exposed semiconductor groups 174 and exposed portions of the segmented silicon layers 170 a, 170 b, 170 c and 170 d of FIG. 19, a high-aspect-ratio capable material 201 (see FIG. 27) is employed to fill openings 184 and 196, and to cover the exposed semiconductor groups 174 and exposed portions of the segmented silicon layers 170 a, 170 b, 170 c, and 170 d of FIG. 26. High-aspect-ratio capable material is material which is capable of passing into a high aspect ratio aperture to form high aspect ratio vias. The aspect ratio of an aperture or a corresponding via structure may be defined as the high H of the aperture divided by the smallest cross-sectional width D of the aperture. For example, an aperture with a height H and a width D has as aspect ratio of H/D. The apertures or the formed via structures may have aspect ratios of about 20:1 or more with heights of, e.g., about 450 microns or more, and preferably aspect ratios of about 30:1 or more with heights of, e.g., about 600 microns or</p>
--	---

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>more. Material 201 has an aspect ratio ranging from about 2:1 to about 40:1, preferably from about 4:1 to about 15:1, more preferably from about 6:1 to about 8:1. Material 201 is preferably an epoxy polymer which may be purchased commercially under the trade name SU-8 which was originally developed and patented by IBM-Watson Research Center (Yorktown Height, USA). Current manufacturers of SU-8 are MicroChem Corp. (previously named Microlithography Chemical Corp.), Sotec Microsystems (spin-off from EPFL) in Switzerland, and Mimotec (also spin-off from EPFL). After vias 192 (which are preferably photo-definable through vias, not produced by laser drilling) are formed, layers 201 a, 201 b, 201 c, and 201 d remain from the material 201.” Peters, [16:61-17:27].</p> <p>“Plated vias 264 264 may then be formed respectively between residual silicon layers 230 a, 230 b, and between residual silicon layers 230 b, 230 c, and through dielectric layers 238, 247 and the metal layers, as shown in FIG. 37. Optionally, plated vias 264 264 may be filled with a dielectric material 268 and capped with caps 270 270. Plated vias 264 264 may be formed by any suitable conventional process, such as by laser drilling the necessary vias, and plating (e.g. with copper) by the combination of e-less and electrolytic plating.” Peters, [18:39-18:48].</p> <p>“Circuit board 102 is adhesively connected to the dielectric material 260 b, as also reflected in FIG. 36, and openings 280 280 are subsequently produced between residual silicon layers 230 a, 230 b and residual silicon layers 230 b, 230 c and through dielectric layer 238, dielectric material 260 and circuit board 102, as shown in FIG. 43. Openings 240 are also produced through the dielectric layer 238 to expose operable, non-defective devices or pads 234 a, 234 b, 234 c and 234 d. It is assumed that devices or pads 234 e and 234 f when previously tested, such as previously described with respect to the test performed on the structure of FIG. 39, were discovered to be defective; thus, no openings 240 are to be formed in the dielectric layer 238 to expose devices or pads 234 e and 234 f. Openings 240 over</p>
--	---

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>devices or pads 234 a, 234 b, 234 c and 234 d and openings 280 280 are then filled and plated with a metal, such as copper, in accordance with any suitable conventional plating process, such as e-less and electrolytic plating, to produce plated vias 264 264, as shown in FIG. 44.” Peters, [18:65-19:16].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Peters discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Vias 206 are formed through dielectric layers 204 in the locations corresponding to the predefined apertures in conductive layer 202 (FIG. 6 (e)). Vias 206 may be formed by means of a laser drill or plasma etch process. Vias 206 are then metallized and a seed layer 208 is deposited on the surface of each dielectric layer 204 using electroless plating, direct plating, sputtering, or another suitable process (FIG. 6 (f)). Seed layer 208 is then built up to form a metal layer of desired thickness which is patterned as desired to form signal lines 210 and signal pads 211 (FIG. 6 (g)).” Peters, [9:45-9:55].</p>

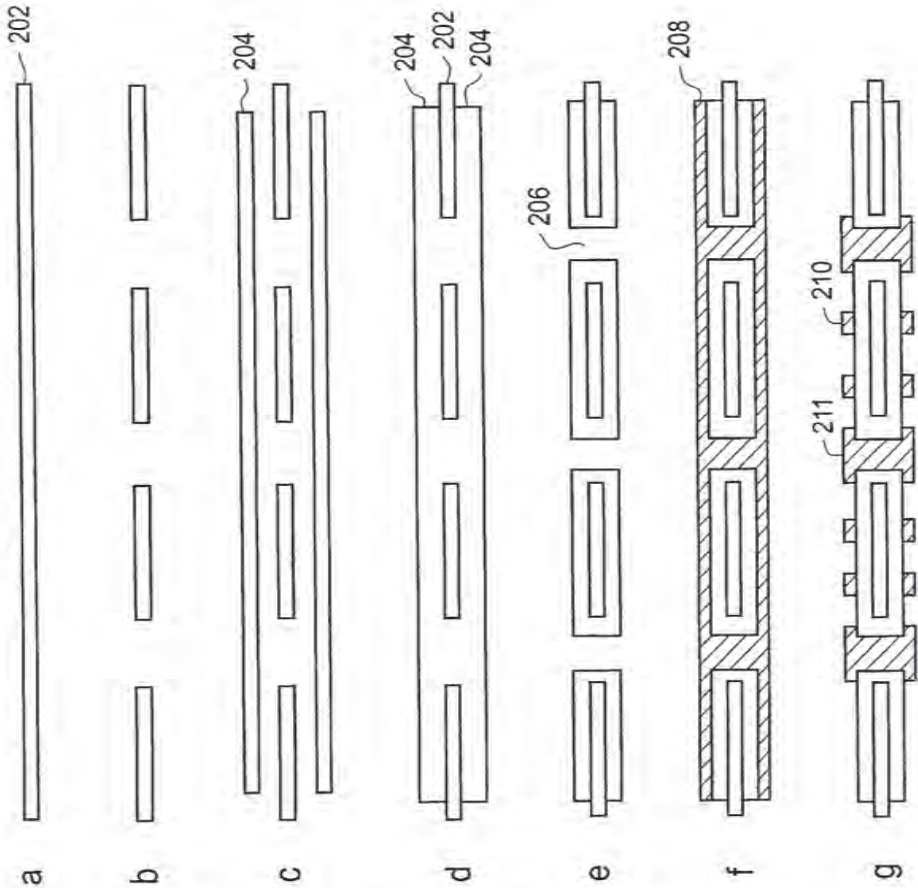


FIG. 6

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>Peters, FIG. 6</p> <p>“A plating or metallization step is then used to fill the vias with a conductive material 710 (FIG. 7 (e)). The initial substrate (as shown in FIG. 7 (a)) is then removed, typically by using an etch process, leaving the signal core 106 (FIG. 7 (f)).” Peters, [10:9-10:12].</p> <p>“The conductive posts 724 are then formed by a suitable electrolytic deposition process. A dielectric layer is then formed over the posts (FIG. 8 (e)). A chemical-mechanical polishing process is then used to planarize the top dielectric layer and level the posts (FIG. 8 (f)). Finally, a metallization step is used to form conductive contacts 726 on the tops of the posts (FIG. 8 (g)).” Peters, [10:32-10:38].</p> <p>“The vias are then filled with a conductive material, and a conductive layer 1004 is formed on the upper and lower surfaces of the substrate (FIG. 10 (c)). The conductive material may be applied by an electroless and/or electrolytic plating process. Metal chemical vapor deposition (MCVD) or another suitable process may also be used. The conductive layers on the upper and lower surfaces of the substrate are then patterned to form the desired power, ground, and signal connections 1006 (FIG. 10 (d)).” Peters, [11:6-11:13].</p> <p>“The vias are then filled with a conductive material, and a conductive layer 1404 is formed on the upper and lower surfaces of the substrate (FIG. 13 (c)). The upper/outer conductive surface 1430 of the power/ground wrap will be patterned to form the ground layer of the power/ground wrap, with electrically isolated pads for signal and power interconnections between the IC chip, interposer, and substrate.” Peters, [12:7-12:14].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	--

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Peters discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a schematic cross-sectional view of one embodiment of the circuit signal core 106 which is part of the interposer of the present invention. Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106. A dielectric film 110 (e.g., Polyimide, BT, etc.) is arranged on both sides of conductive core 111. Signal lines 113 are defined on a patterned metal layer formed on each of the two dielectric film layers. The two patterned metal layers are interconnected as desired by either a through via or a conductive post structure 112, with the through via or conductive post being suitable for interconnecting the signal core to other layers of the interposer structure, or to the mounting substrate or integrated circuit chips.” Peters, [8:18-8:34].</p> <p>“FIGS. 6 (a) to 6 (g) show a process flow for one preferred method of fabricating the signal core which is part of the reduced cross-talk interposer of embodiments of the present invention. In the process flow shown in FIG. 6, the metal layers on the two sides of the core substrate are interconnected by a through via. As shown in the figures, the process flow begins with a conductive layer, which may be formed from a suitable metal 202 (FIG. 6 (a)). Holes or apertures are formed in layer 202 at the positions where through vias or conductive posts will later be formed (FIG. 6 (b)). A dielectric layer 204 is then formed on</p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>each surface of conductive layer 202. Dielectric layers 204 may be laminated onto each surface of layer 202 (FIGS. 6 (c) and 6 (d)). Vias 206 are formed through dielectric layers 204 in the locations corresponding to the predefined apertures in conductive layer 202 (FIG. 6 (e)). Vias 206 may be formed by means of a laser drill or plasma etch process. Vias 206 are then metallized and a seed layer 208 is deposited on the surface of each dielectric layer 204 using electroless plating, direct plating, sputtering, or another suitable process (FIG. 6 (f)). Seed layer 208 is then built up to form a metal layer of desired thickness which is patterned as desired to form signal lines 210 and signal pads 211 (FIG. 6 (g)).” Peters, [9:33-9:55].</p>
--	---

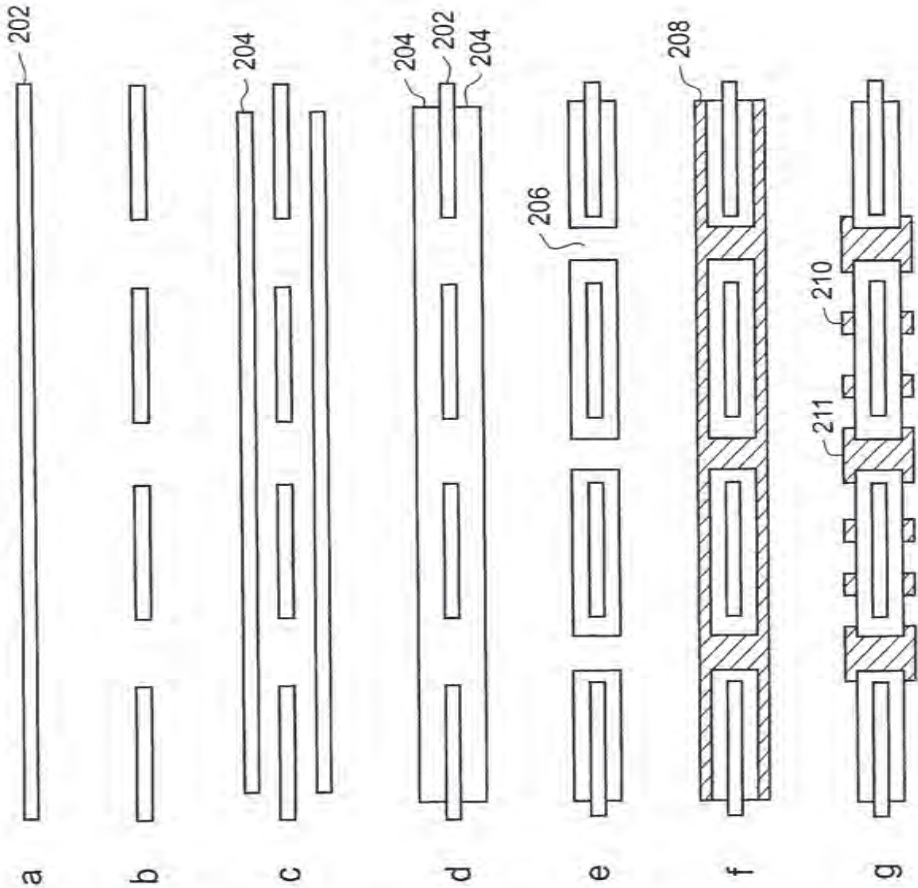


FIG. 6

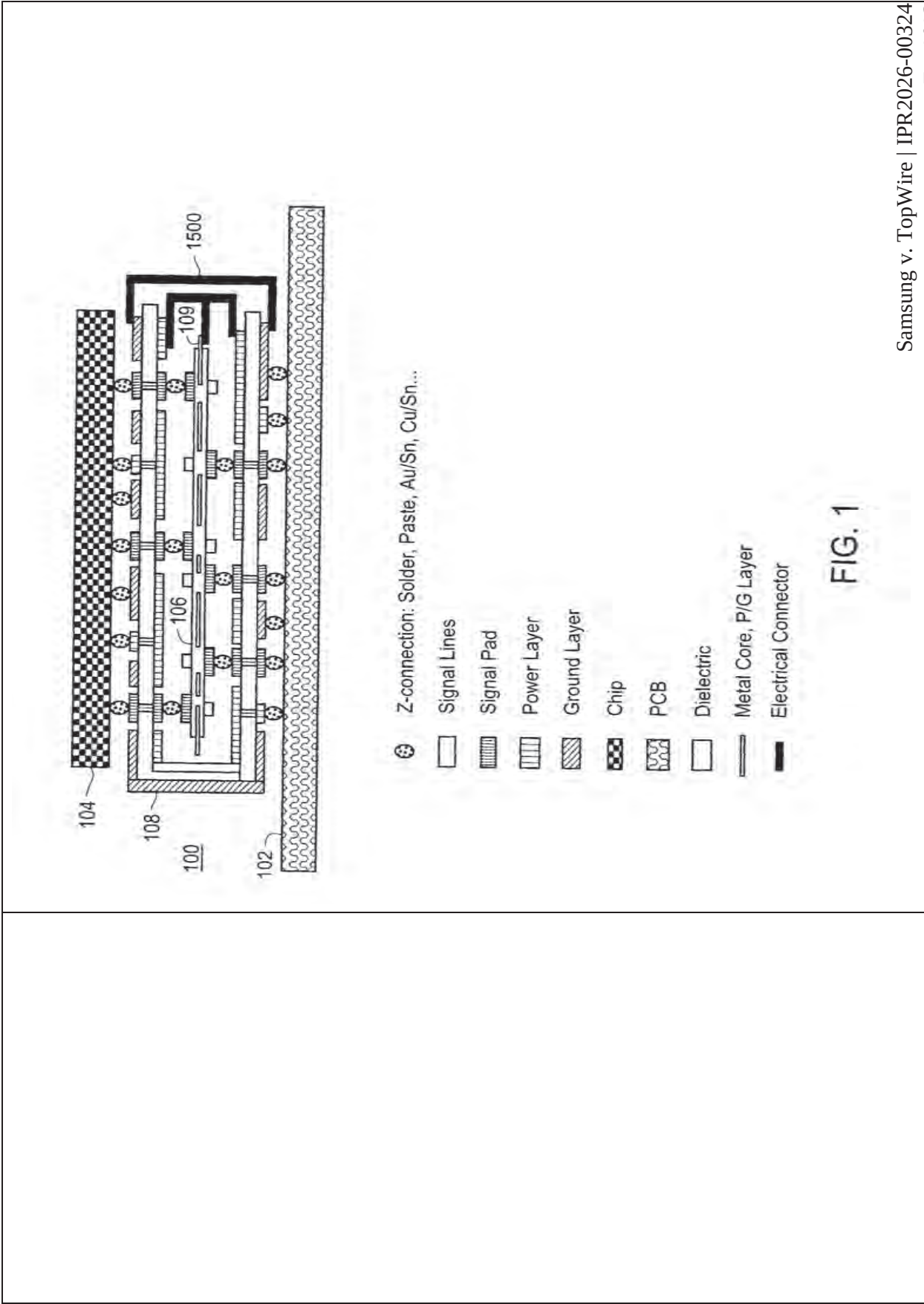
	<p>Peters, FIG. 6</p> <p>“FIGS. 12 (a) to 12 (g) illustrate a process flow for an additional method of fabricating the signal core which is part of the reduced cross-talk interposer of the present invention. In the process flow shown in FIG. 12, a conductive layer 1202 again has holes or apertures formed through it at desired locations (FIGS. 12 (a) and 12 (b)). A dielectric layer 1204 is formed (e.g., laminated) onto one surface of conductive layer 1202. A dielectric having a previously formed metallized surface or layer 1205 is then laminated onto the other surface of conductive layer 1202 (FIGS. 12 (c) and 12 (d)). Vias 1206 are formed through dielectric layers 1204 in the locations corresponding to the predefined apertures in conductive layer 1202 (FIG. 12 (e)). Vias 1206 may be formed by means of a laser drill or plasma etch process.” Peters, [11:35-11:48].</p> <p>“In the process step illustrated in FIG. 17, a silicon layer 170 (e.g. a previously processed and tested silicon wafer) having a thickness ranging from about 100 m to about 300 m, such as about 200 m, is adhesively attached to the circuit board 102 (i.e., an organic board). A plurality of groups or clustered semiconductor devices is disposed on the silicon layer 170. Each semiconductor group is exemplified by the number 174 and includes semiconductor devices 174 a, 174 b and 174 c, such as capacitors. Semiconductor devices 174 a, 174 b and 174 c are preferably capacitors having at least one G via and V via. A dielectric layer is disposed on silicon layer 170 and patterned such that each group of semiconductor devices 174 is encapsulated by a dielectric capsule 178 and separated by openings 180. The dielectric layer for forming dielectric capsules 178 may be composed of any suitable dielectric material, preferably an organic dielectric such as photoresist, photo-definable polyimide, or photo-definable epoxy. Subsequently, the silicon layer 170 is etched through the openings 184 down to the circuit board, 102 as best shown in FIG. 18, to produce a plurality of segmented silicon layers 170 a, 170 b, 170 c and 170 d (see FIG. 18). Then vias 186 may be created in the</p>
--	---

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>circuit board 102 to produce continuous interconnected circuit boards 102 a, 102 b, 102 c and 102 d, supporting segmented silicon layers 170 a, 170 b, 170 c and 170 d (see FIG. 19).” Peters, [15:35-15:60].</p> <p>“Referring now to FIGS. 38-44 for yet another embodiment of the invention, illustrating backside etch without any integrated power or voltage plane (e.g., metal layer 244) or ground plane (e.g. metal layer 249). FIGS. 38 and 39 represent the same interposer structures and methods of FIGS. 31 and 32. FIG. 40 illustrates the silicon layer 230 after thinning (e.g., by CMP), as reflected in FIG. 34. The silicon layer 230 is then segmented into residual silicon layers 230 a, 230 b and 230 c separated by openings 256, as previously indicated for producing the residual silicon layers 230 a, 230 b and 230 c in FIG. 35, which are also separated or spaced by openings 256. The dielectric material 260 fills the openings 256 and covers the bottoms of residual silicon layers 230 a, 230 b, and 230 c, as reflected in FIG. 42. Circuit board 102 is adhesively connected to the dielectric material 260 b, as also reflected in FIG. 36, and openings 280 280 are subsequently produced between residual silicon layers 230 a, 230 b and residual silicon layers 230 b, 230 c and through dielectric layer 238, dielectric material 260 and circuit board 102, as shown in FIG. 43.” Peters, [18:51-19:3].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the</p>	<p>Peters discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

plurality of metal pillars of the spacer connector,	<p><i>See, e.g.:</i></p> <p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method.” Peters, [7:36-7:46].</p>
---	---



	<p>Peters, FIG. 1</p> <p>“As shown in the figure, in accordance with the present invention, power and ground interconnections are routed between the mounting substrate 102 and the chip(s) 104 without passing through the signal core 106. On the other hand, the signal lines are routed between the mounting substrate 102 and the chip(s) 104 by passing only through the signal core. This architecture provides electrical isolation between the power, ground, and signal interconnections (and hence reduces noise and other problems caused by capacitive coupling between lines) while increasing the density of signal lines which can be connected between the substrate and chip(s). Signal core 106 includes a power/ground layer 109 positioned between signal layers which are on either side of that substrate and together form the basis for the signal core. Power/ground layer 109 acts to reduce cross-talk between signal lines on the same or different signal layers of signal core 106.” Peters, [7:51-7:67].</p> <p>“As shown in FIG. 1, edge connectors 1500 may be used to electrically connect different ground layers (e.g., the lower surface of the lower power/ground substrate to the upper surface of the upper power/ground substrate), different power layers (e.g., the upper surface of the lower power/ground substrate to the lower surface of the upper power/ground substrate), or the power/ground layer of the signal core to other ground or power layers of the interposer. Although a single set of edge connectors 1500 is shown in the figure, note that if the upper and lower power/ground substrates are fabricated separately (rather than formed from a flexible substrate which is bent into a “U” shape), then a set of connectors 1500 may be used at both ends of the two power/ground substrates. FIG. 2 is a schematic cross-sectional view of another embodiment of the signal interposer 100 positioned between the printed board 102 and the integrated circuit chip 104.” Peters, [8:1-8:17].</p>
--	--

	<p>“Referring now to FIG. 5, there is seen a schematic cross-sectional view of power ground wrap 108 which is part of embodiments of the interposer of the present invention. Power ground wrap 108 is formed from a dielectric film 120 (e.g. Polyimide, Bt, etc.) on both sides of which is patterned a metal layer. The two metal layers are interconnected as desired by either a through via or conductive post.” Peters, [8:51-8:57].</p> <p>“FIGS. 8 (a) to 8 (g) show a process flow for yet another method of fabricating another embodiment of the signal core which is part of embodiments of the interposer of the present invention. In the process flow shown in FIG. 8, the metal layers on the two sides of the dielectric substrate are interconnected by a conductive post. As shown in the figures, the process flow begins with a substrate 720 (FIG. 8 (a)). A metal layer 704 is then formed over the substrate and patterned (FIG. 8 (b)). A resist layer 720 is then formed over the patterned metal layer (FIG. 8 (c)). The top resist layer is then patterned to form the locations 722 for the posts (FIG. 8 (d)). The conductive posts 724 are then formed by a suitable electrolytic deposition process. A dielectric layer is then formed over the posts (FIG. 8 (e)). A chemical-mechanical polishing process is then used to planarize the top dielectric layer and level the posts (FIG. 8 (f)). Finally, a metallization step is used to form conductive contacts 726 on the tops of the posts FIG. 8 (g)” Peters, [10:21-10:38].</p> <p>“FIGS. 10 (a) to 10 (e) show a process flow for an additional method of fabricating the power/ground wrap 108 which is part of the interposer of the present invention. The fabrication process shown begins with a dielectric substrate 1000 (FIG. 10 (a)). Through vias 1002 are formed in the substrate at the desired locations (FIG. 10 (b)). The vias may be formed by a laser drill, plasma etching, or another suitable method. The vias are then filled with a conductive material, and a conductive layer 1004 is formed on the upper and lower surfaces of the substrate (FIG. 10 (c)). The conductive material may be applied by an electroless and/or electrolytic plating process.” Peters, [10:66-11:10].</p>
--	---

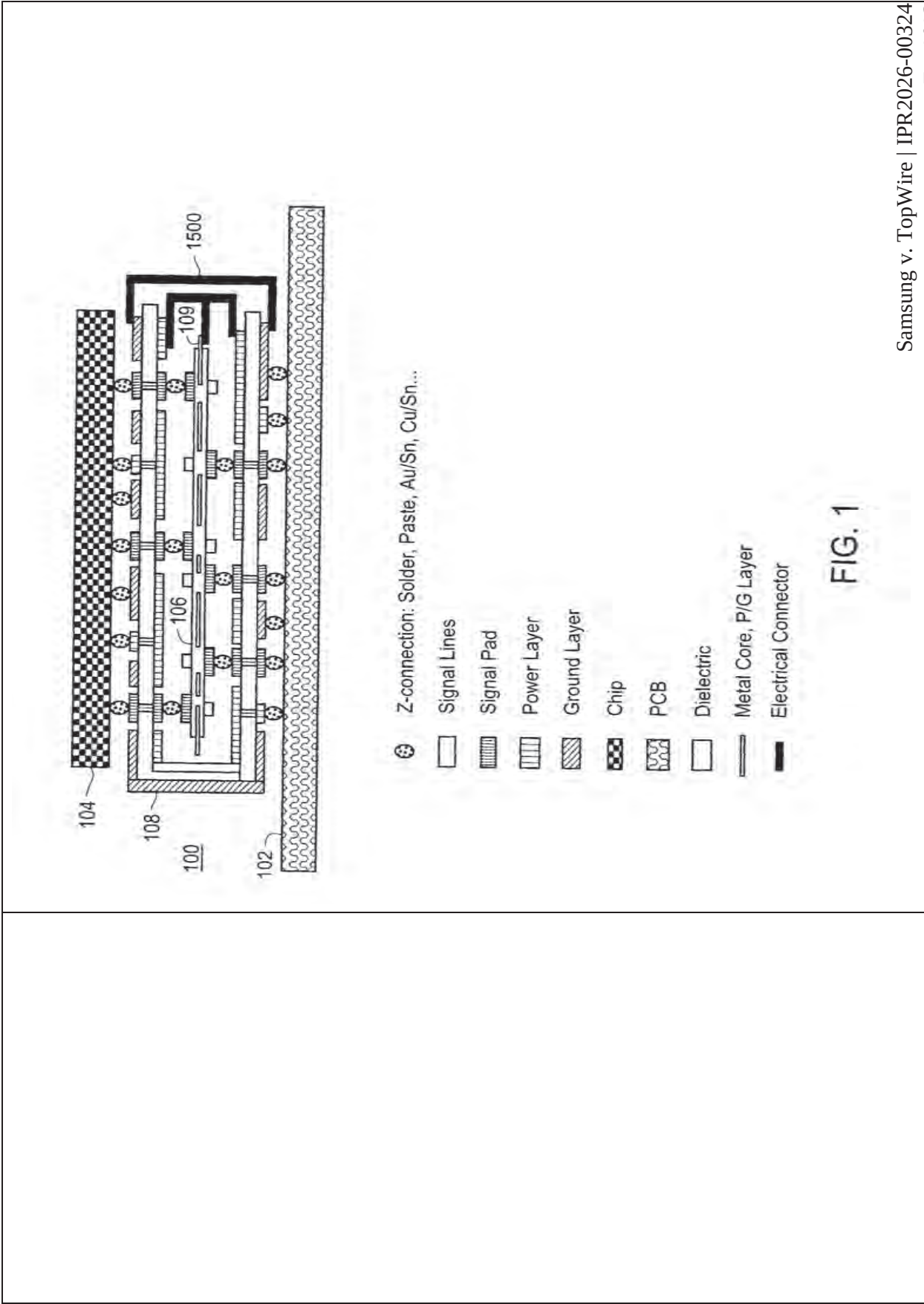
Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>“The integrated circuit chip(s) can be attached to the interposer 108 by flip chip, TAB (tape automated bonding), flip TAB, wire bonding, or another suitable method. For most applications, the preferred interconnection method is a flip chip area array process. The interposer can be connected to the PCB or other substrate by means of a ball grid array (BGA).” Peters, [13:30-13:36].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Peters discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“As shown in FIG. 1, edge connectors 1500 may be used to electrically connect different ground layers (e.g., the lower surface of the lower power/ground substrate to the upper surface of the upper power/ground substrate), different power layers (e.g., the upper surface of the lower power/ground substrate to the lower surface of the upper power/ground substrate), or the power/ground layer of the signal core to other ground or power layers of the interposer. Although a single set of edge connectors 1500 is shown in the figure, note that if the upper and lower power/ground substrates are fabricated separately (rather than formed from a flexible substrate which is bent into a U shape), then a set of connectors 1500 may be used at both ends of the two power/ground substrates.” Peters, [8:1-8:14].</p>

	<p>“FIG. 3 is a schematic cross-sectional view of one embodiment of the circuit signal core 106 which is part of the interposer of the present invention. Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106. A dielectric film 110 (e.g., Polyimide, BT, etc.) is arranged on both sides of conductive core 111. Signal lines 113 are defined on a patterned metal layer formed on each of the two dielectric film layers. The two patterned metal layers are interconnected as desired by either a through via or a conductive post structure 112, with the through via or conductive post being suitable for interconnecting the signal core to other layers of the interposer structure, or to the mounting substrate or integrated circuit chips.” Peters, [8:18-8:34].</p> <p>“Referring now to FIG. 5, there is seen a schematic cross-sectional view of power ground wrap 108 which is part of embodiments of the interposer of the present invention. Power ground wrap 108 is formed from a dielectric film 120 (e.g. Polyimide, Bt, etc.) on both sides of which is patterned a metal layer. The two metal layers are interconnected as desired by either a through via or conductive post.” Peters, [8:51-8:57].</p> <p>“FIGS. 6 (a) to 6 (g) show a process flow for one preferred method of fabricating the signal core which is part of the reduced cross-talk interposer of embodiments of the present invention. In the process flow shown in FIG. 6, the metal layers on the two sides of the core substrate are interconnected by a through via. As shown in the figures, the process flow begins with a conductive layer, which may be formed from a suitable metal 202 (FIG. 6 (a)). Holes or apertures are formed in layer 202 at the positions where through vias or conductive posts will later be formed (FIG. 6 (b)). A dielectric layer 204 is then formed on each surface of conductive layer 202. Dielectric layers 204 may be laminated onto each</p>
--	--

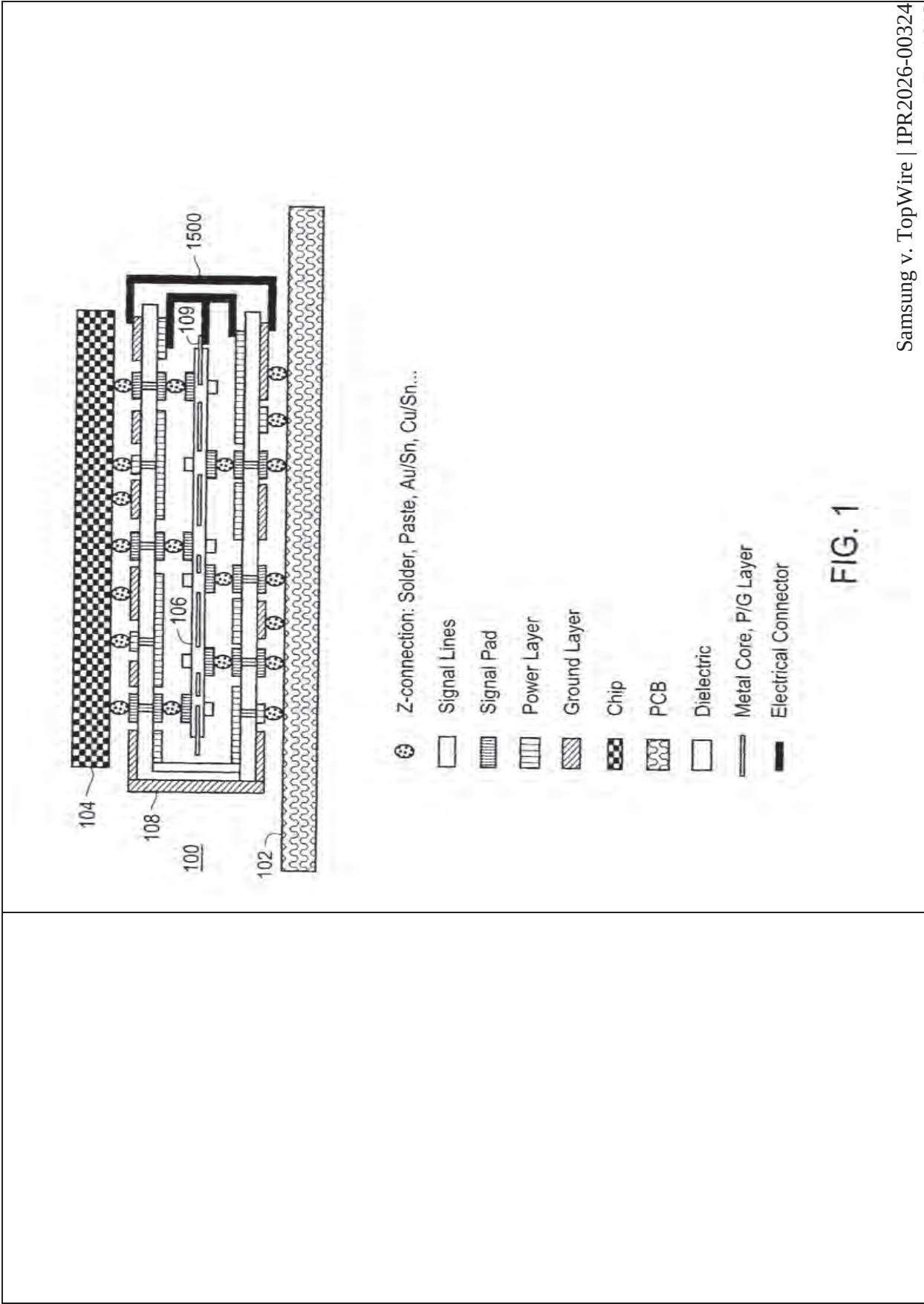
	<p>surface of layer 202 (FIGS. 6 (c) and 6 (d)). Vias 206 are formed through dielectric layers 204 in the locations corresponding to the predefined apertures in conductive layer 202 (FIG. 6 (e)). Vias 206 may be formed by means of a laser drill or plasma etch process. Vias 206 are then metallized and a seed layer 208 is deposited on the surface of each dielectric layer 204 using electroless plating, direct plating, sputtering, or another suitable process (FIG. 6 (f)). Seed layer 208 is then built up to form a metal layer of desired thickness which is patterned as desired to form signal lines 210 and signal pads 211 (FIG. 6 (g)).” Peters, [9:33-9:55].</p> <p>“FIGS. 8 (a) to 8 (g) show a process flow for yet another method of fabricating another embodiment of the signal core which is part of embodiments of the interposer of the present invention. In the process flow shown in FIG. 8, the metal layers on the two sides of the dielectric substrate are interconnected by a conductive post. As shown in the figures, the process flow begins with a substrate 720 (FIG. 8 (a)). A metal layer 704 is then formed over the substrate and patterned (FIG. 8 (b)). A resist layer 720 is then formed over the patterned metal layer (FIG. 8 (c)). The top resist layer is then patterned to form the locations 722 for the posts (FIG. 8 (d)). The conductive posts 724 are then formed by a suitable electrolytic deposition process. A dielectric layer is then formed over the posts (FIG. 8 (e)). A chemical-mechanical polishing process is then used to planarize the top dielectric layer and level the posts (FIG. 8 (f)). Finally, a metallization step is used to form conductive contacts 726 on the tops of the posts FIG. 8 (g)).” Peters, [10:21-10:38].</p> <p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can</p>
--	--

	<p>be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method. This reduces the cycle time for manufacturing and testing of the structure, and increases the types of processing techniques which may be used to form the different parts of the final structure. As shown in the figure, in accordance with the present invention, power and ground interconnections are routed between the mounting substrate 102 and the chip(s) 104 without passing through the signal core 106. On the other hand, the signal lines are routed between the mounting substrate 102 and the chip(s) 104 by passing only through the signal core. This architecture provides electrical isolation between the power, ground, and signal interconnections (and hence reduces noise and other problems caused by capacitive coupling between lines) while increasing the density of signal lines which can be connected between the substrate and chip(s). Signal core 106 includes a power/ground layer 109 positioned between signal layers which are on either side of that substrate and together form the basis for the signal core.” Peters, [12:65-13:27].</p>
--	--



Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>Peters, FIG. 1</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Peters discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method.” Peters, [7:36-7:46].</p>



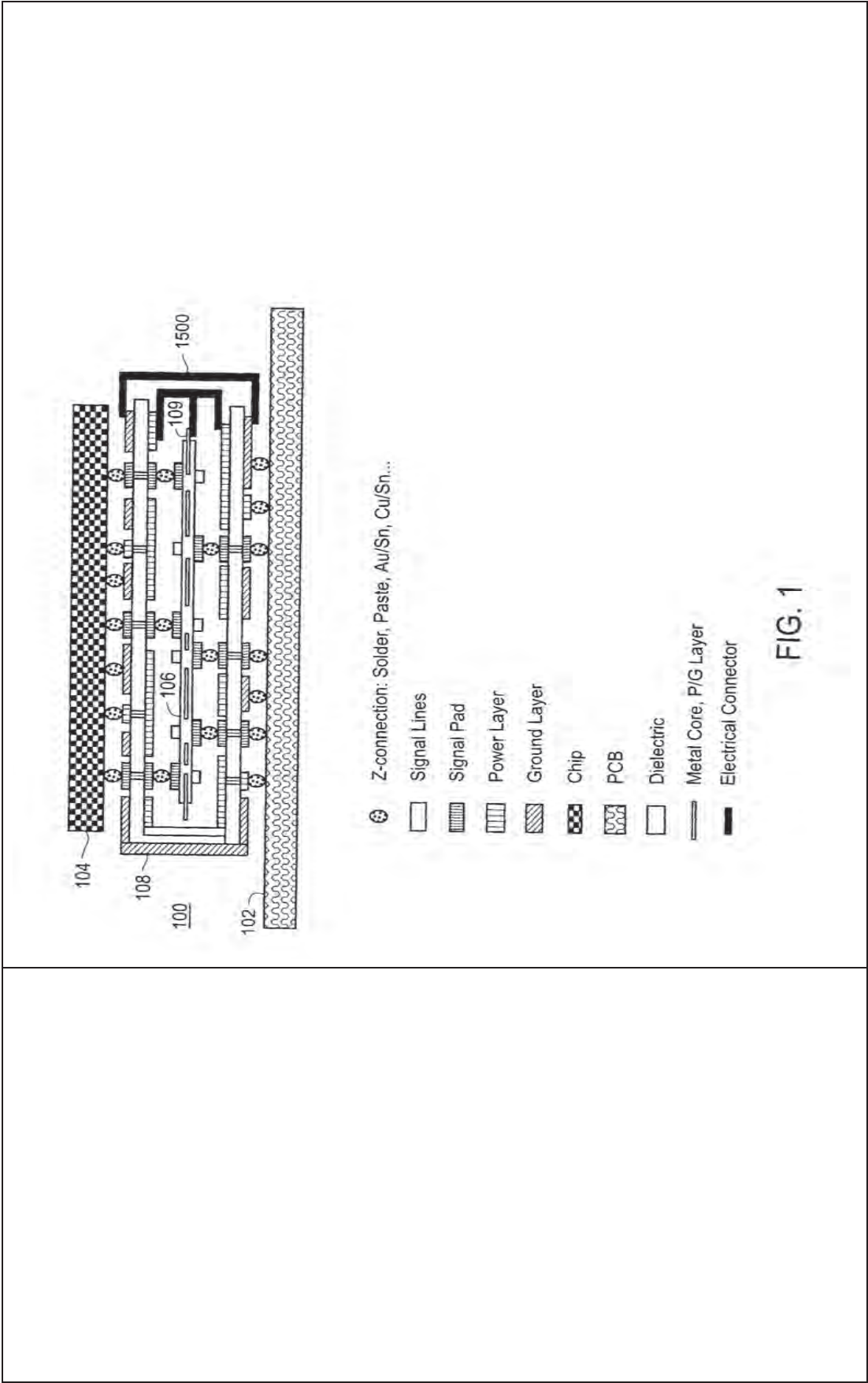
	<p>Peters, FIG. 1</p> <p>“As shown in the figure, in accordance with the present invention, power and ground interconnections are routed between the mounting substrate 102 and the chip(s) 104 without passing through the signal core 106. On the other hand, the signal lines are routed between the mounting substrate 102 and the chip(s) 104 by passing only through the signal core. This architecture provides electrical isolation between the power, ground, and signal interconnections (and hence reduces noise and other problems caused by capacitive coupling between lines) while increasing the density of signal lines which can be connected between the substrate and chip(s)” Peters, [7:51-7:62].</p> <p>“Signal core 106 includes a power/ground layer 109 positioned between signal layers which are on either side of that substrate and together form the basis for the signal core. Power/ground layer 109 acts to reduce cross-talk between signal lines on the same or different signal layers of signal core 106. As shown in FIG. 1, edge connectors 1500 may be used to electrically connect different ground layers (e.g., the lower surface of the lower power/ground substrate to the upper surface of the upper power/ground substrate), different power layers (e.g., the upper surface of the lower power/ground substrate to the lower surface of the upper power/ground substrate), or the power/ground layer of the signal core to other ground or power layers of the interposer.” Peters, [7:62-8:8].</p> <p>“Although a single set of edge connectors 1500 is shown in the figure, note that if the upper and lower power/ground substrates are fabricated separately (rather than formed from a flexible substrate which is bent into a “U” shape), then a set of connectors 1500 may be used at both ends of the two power/ground substrates. FIG. 2 is a schematic cross-sectional view of another embodiment of the signal interposer 100 positioned between the printed board 102 and the integrated circuit chip 104.” Peters, [8:9-8:17].</p>
--	--

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>“Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106. A dielectric film 110 (e.g., Polyimide, BT, etc.) is arranged on both sides of conductive core 111. Signal lines 113 are defined on a patterned metal layer formed on each of the two dielectric film layers. The two patterned metal layers are interconnected as desired by either a through via or a conductive post structure 112, with the through via or conductive post being suitable for interconnecting the signal core to other layers of the interposer structure, or to the mounting substrate or integrated circuit chips.” Peters, [8:20-8:34].</p> <p>“With the signal core of FIG. 3 inserted between the upper and lower substrates of the power/ground wrap, signal connections may be made between the base substrate (element 102 of FIG. 1), the signal core, and the integrated circuit chip(s) in isolation from the power and ground connections between the base substrate and the chip(s). This permits an increase in signal line density and minimization of signal path lengths, while achieving a high degree of electrical isolation between the different types of lines.” Peters, [12:50-12:58].</p> <p>“When fabricating the reduced cross-talk signal interposer structure, the upper power/ground substrate or surface, signal core, and lower power/ground substrate or surface are interconnected as required using a suitable z-connection technology, followed by attachment of the edge connector or connectors to interconnect the power/ground substrates.” Peters, [13:17-13:22].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

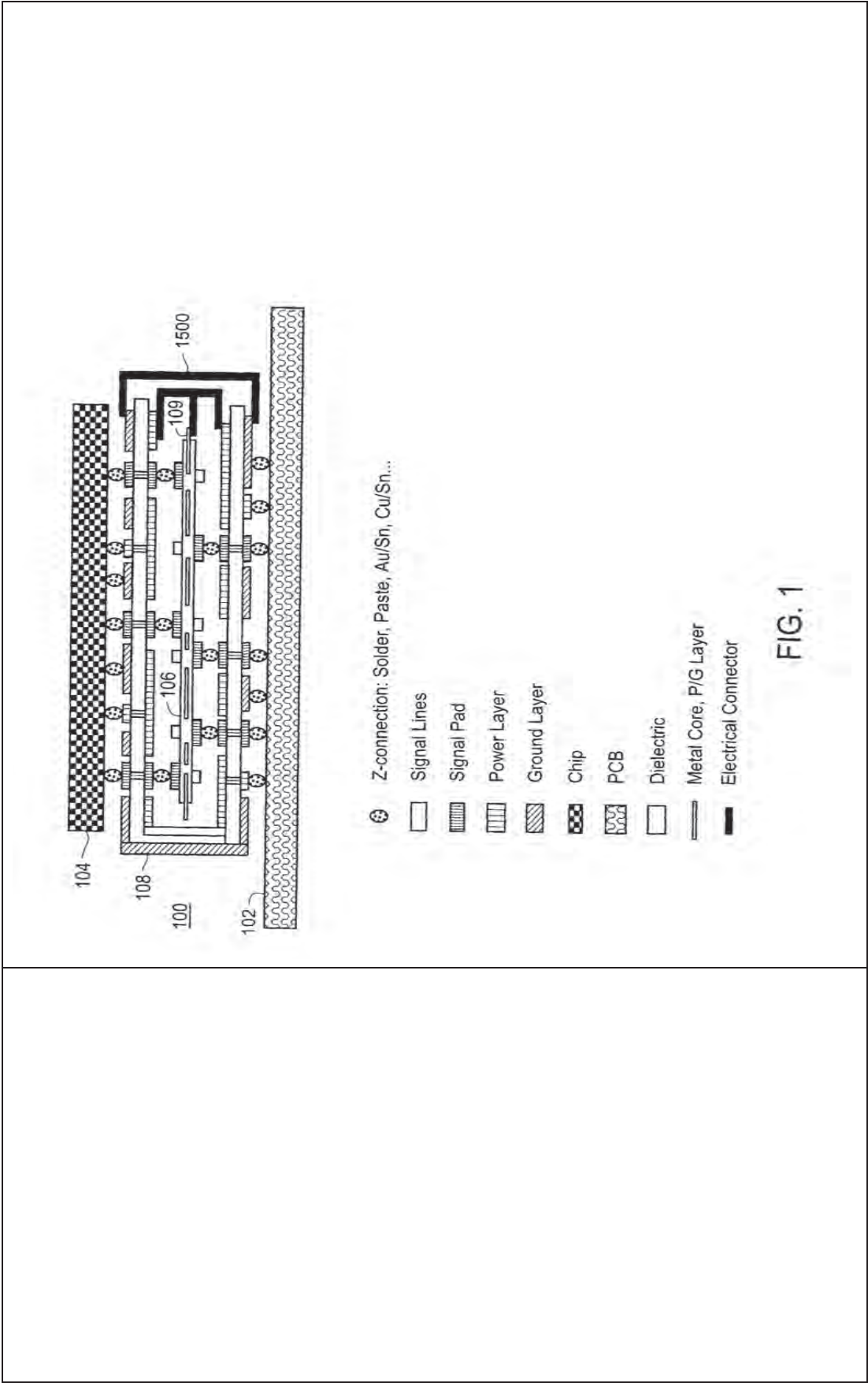
Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein	Peters discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein. <i>See, e.g.:</i>



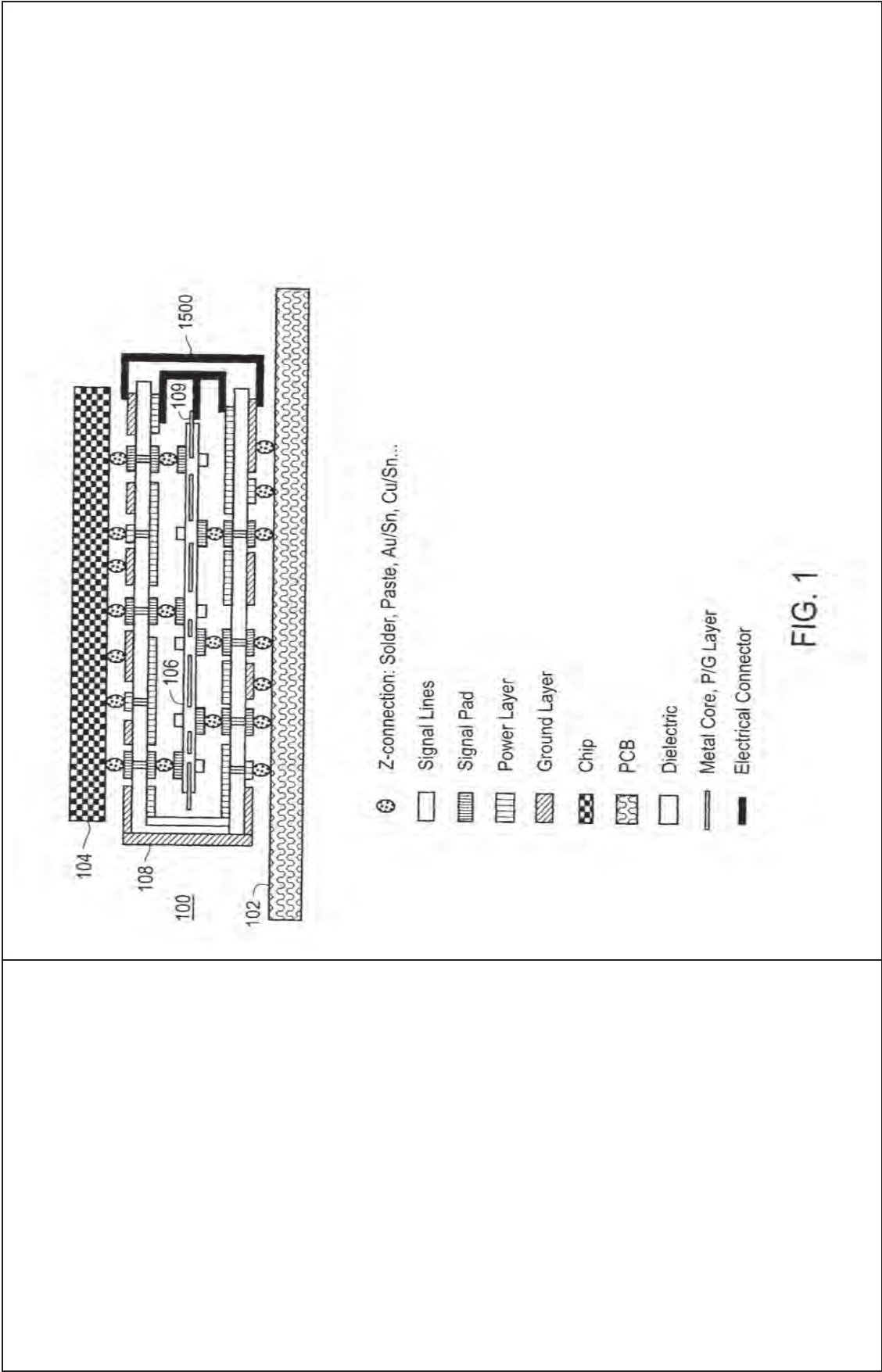
Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>Peters, FIG. 1</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Peters discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>



Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>Peters, FIG. 1</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Peters discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

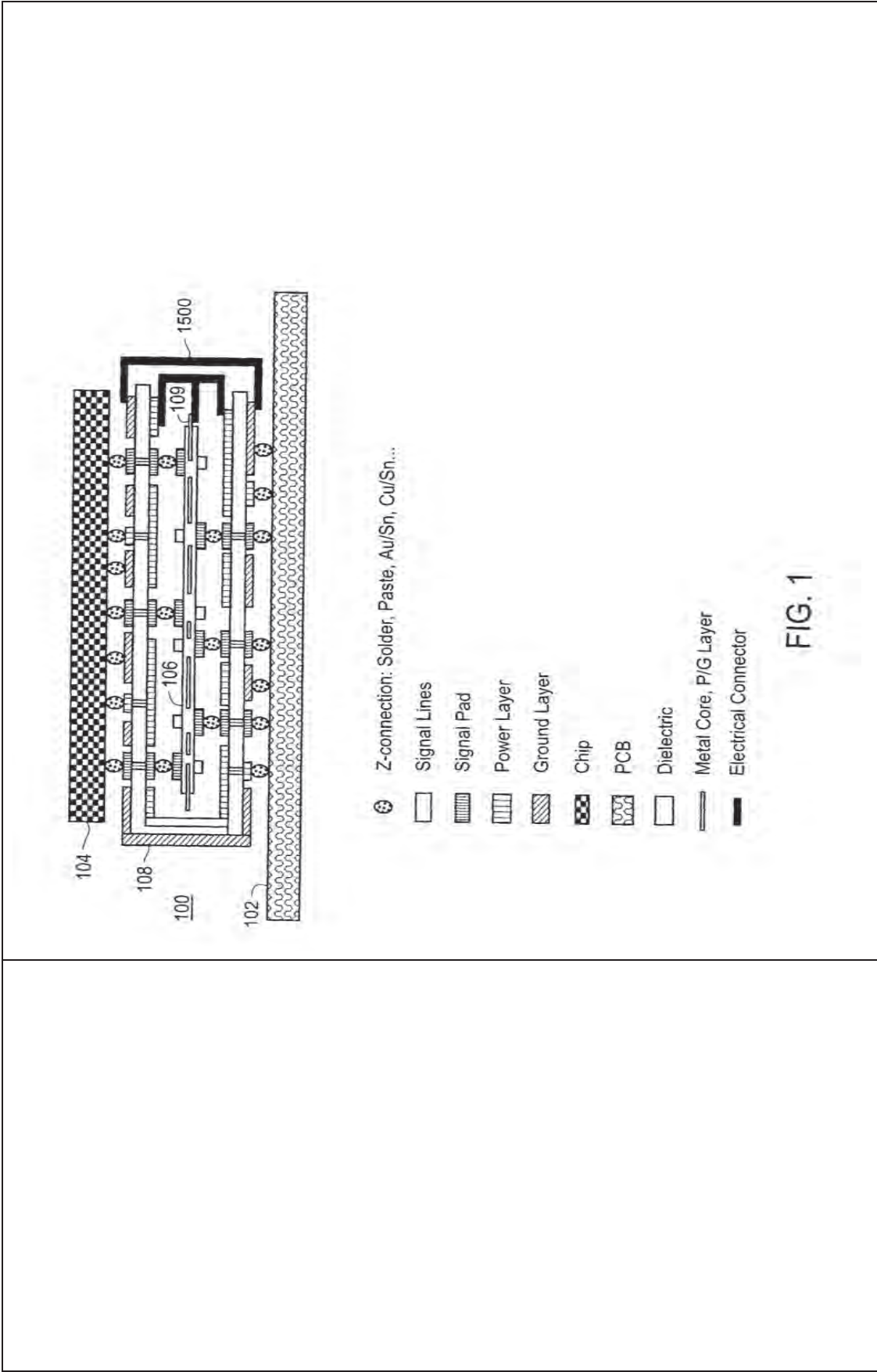


Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>Peters, FIG. 1</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Peters discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>



Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

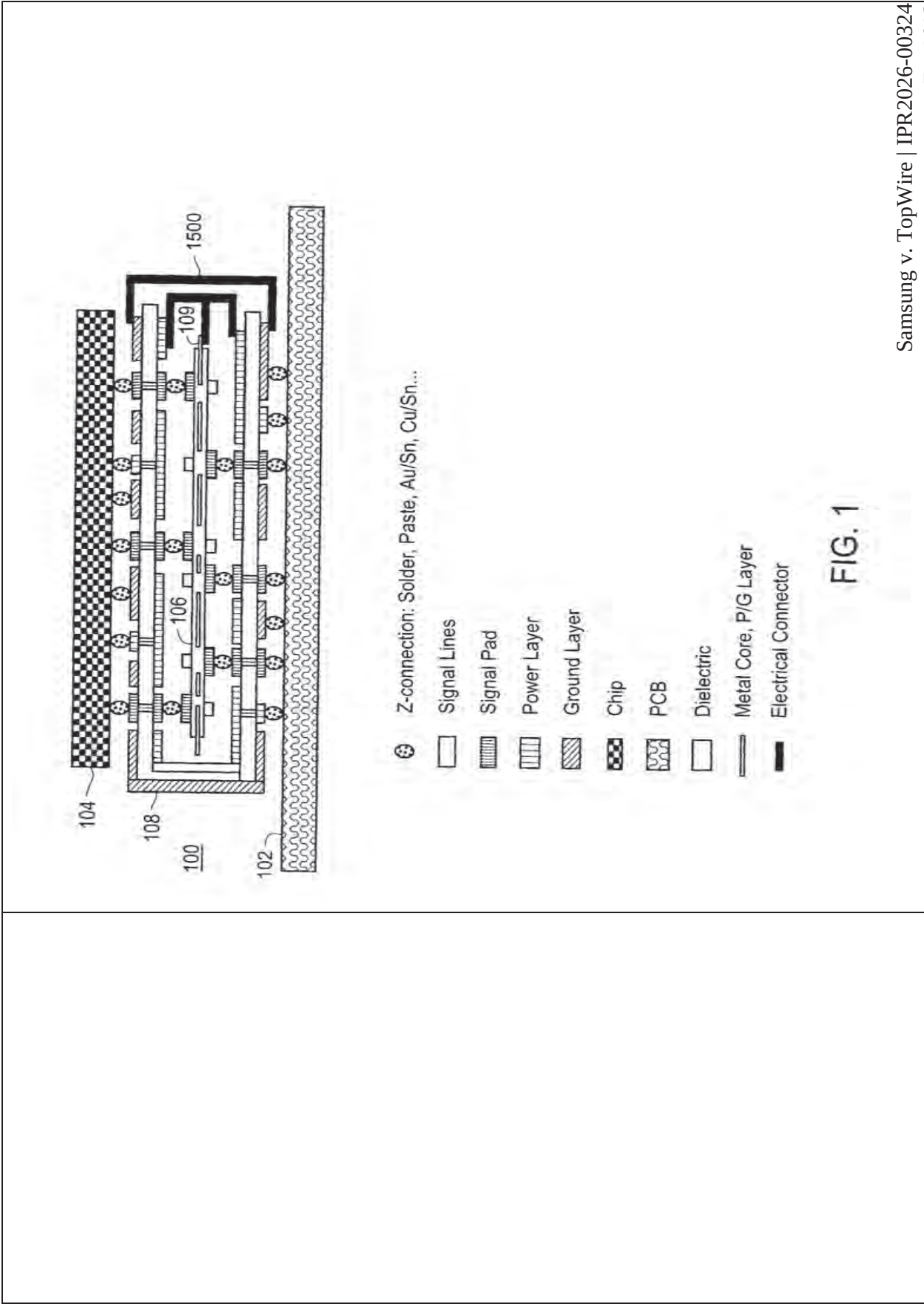
	<p>Peters, FIG. 1</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Peters discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“With an integrated circuit chip or chips connected to the upper layer of the top substrate of the power/ground wrap and a printed circuit board or other mounting substrate connected to the bottom layer of the lower substrate of the wrap, the inventive interposer provides a set of high density and electrically isolated signal, power, and ground interconnections having reduced cross-talk between signal lines.” Peters, [4:12-4:18].</p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>“FIG. 15 is a schematic cross-sectional view of another embodiment of the composite interposer of the present inventions positioned between a printed circuit board and an integrated circuit chip.” Peters, [6:21-6:24].</p> <p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method.” Peters, [7:36-7:46].</p>
--	---



Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

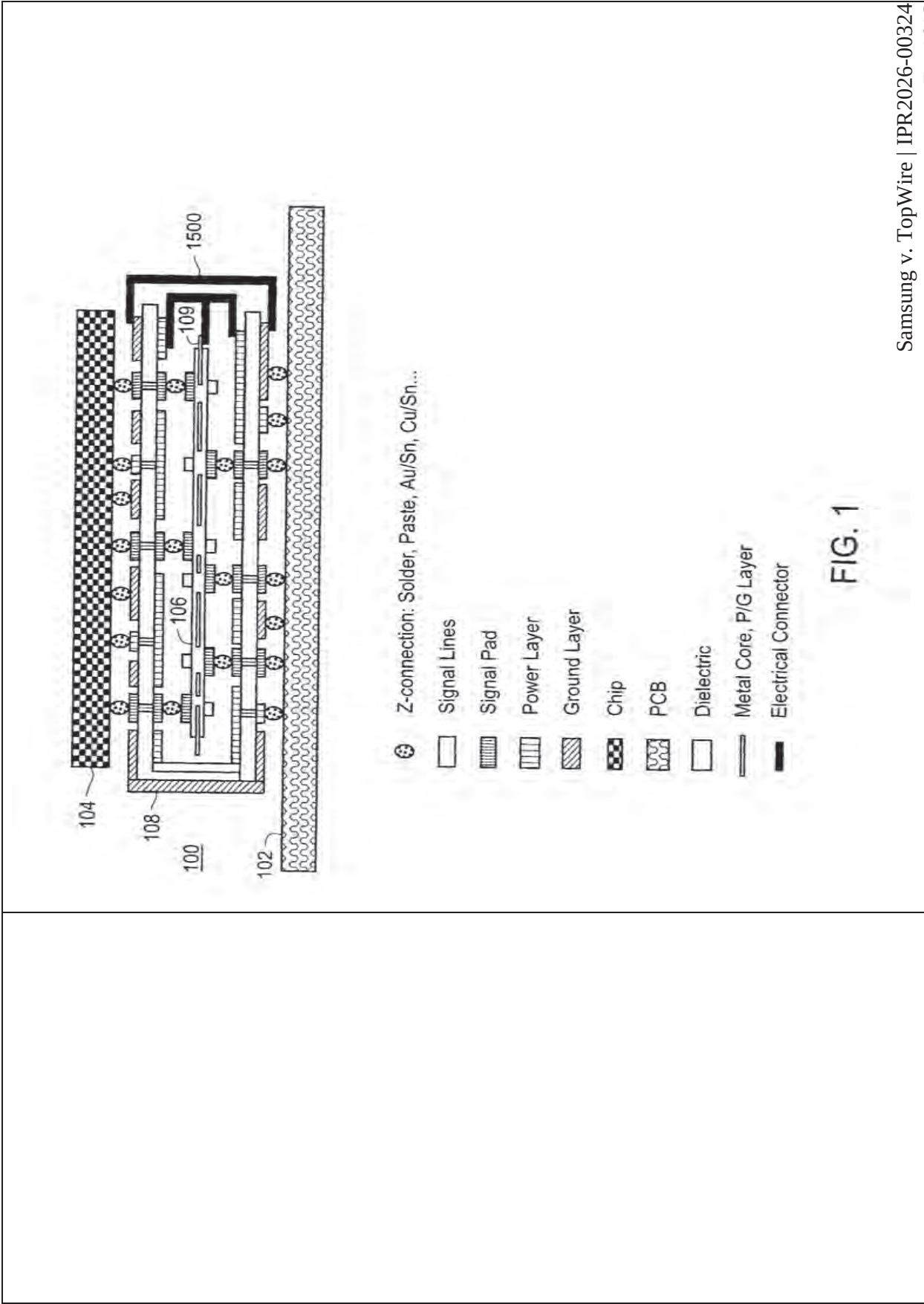
	<p>Peters, FIG. 1</p> <p>“FIG. 2 is a schematic cross-sectional view of another embodiment of the signal interposer 100 positioned between the printed board 102 and the integrated circuit chip 104.” Peters, [8:14-8:17].</p> <p>“FIG. 14 is a schematic cross-sectional view of a different construction of the reduced cross-talk signal interposer of the present invention, and is shown positioned between a printed circuit board and an integrated circuit chip.” Peters, [12:65-13:1].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Peters discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

plurality of top metal pillars of the bottom package substrate.	<p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method.” Peters, [7:36-7:46].</p>
---	--



	<p>Peters, FIG. 1</p> <p>“As shown in FIG. 1, edge connectors 1500 may be used to electrically connect different ground layers (e.g., the lower surface of the lower power/ground substrate to the upper surface of the upper power/ground substrate), different power layers (e.g., the upper surface of the lower power/ground substrate to the lower surface of the upper power/ground substrate), or the power/ground layer of the signal core to other ground or power layers of the interposer.” Peters, [8:1-8:8].</p> <p>“FIG. 3 is a schematic cross-sectional view of one embodiment of the circuit signal core 106 which is part of the interposer of the present invention. Signal core 106 is formed from a conductive core or substrate 111 through which holes or apertures are formed. Conductive core 111 is typically formed from a suitable metal and serves as both a power/ground layer for the interposer and as a reinforcing structure for the signal layers of signal core 106. A dielectric film 110 (e.g., Polyimide, BT, etc.) is arranged on both sides of conductive core 111. Signal lines 113 are defined on a patterned metal layer formed on each of the two dielectric film layers. The two patterned metal layers are interconnected as desired by either a through via or a conductive post structure 112, with the through via or conductive post being suitable for interconnecting the signal core to other layers of the interposer structure, or to the mounting substrate or integrated circuit chips.” Peters, [8:18-8:34].</p> <p>“With the signal core of FIG. 3 inserted between the upper and lower substrates of the power/ground wrap, signal connections may be made between the base substrate (element 102 of FIG. 1), the signal core, and the integrated circuit chip(s) in isolation from the power and ground connections between the base substrate and the chip(s).” Peters, [12:50-12:55].</p>
--	---

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

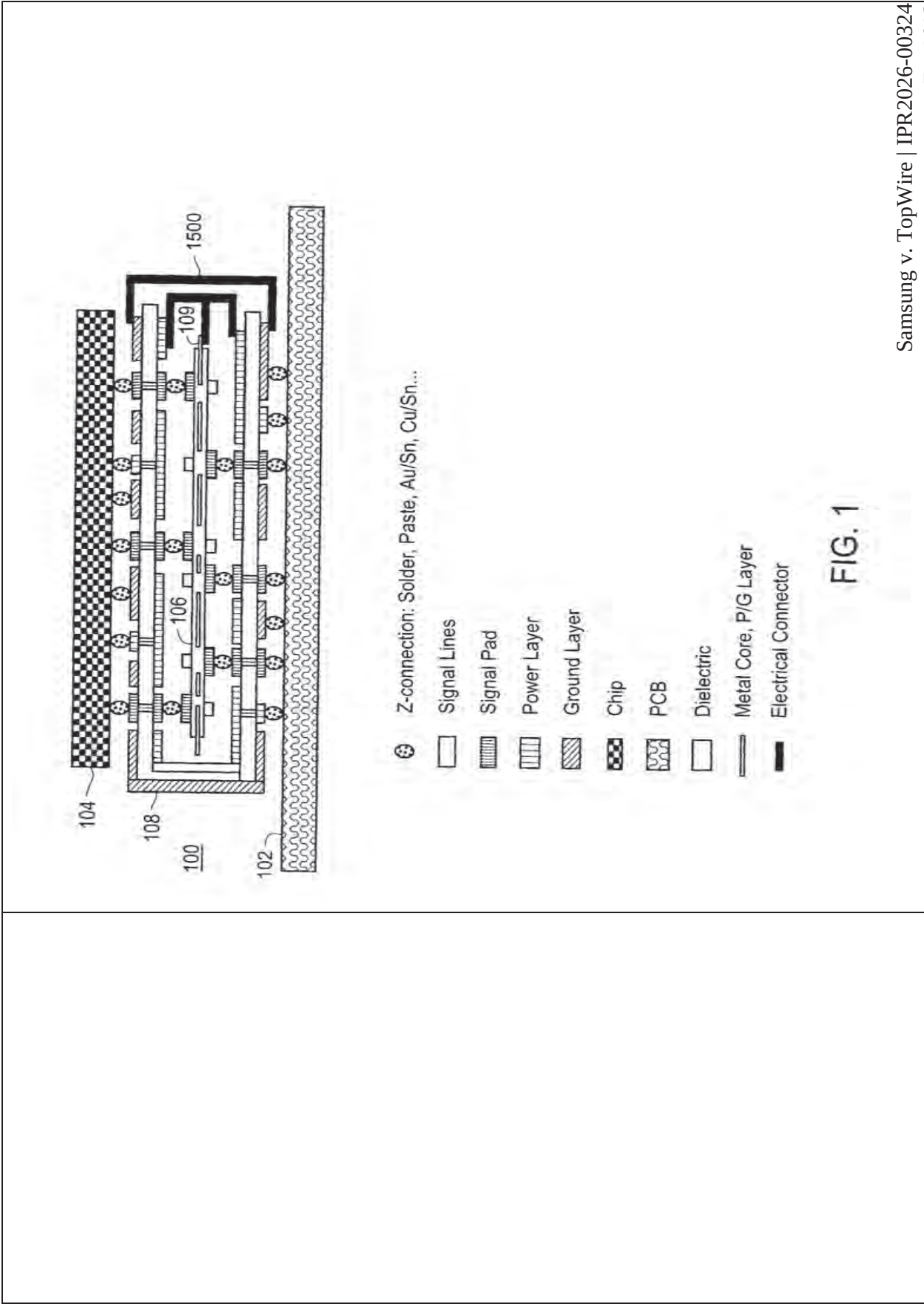
	<p>“FIG. 47 depicts the result after tack lamination. After visual alignment of tack laminated substrate to a matching substrate 310 having metal pads 312, the aligned substrates are laminated to establish the Z-connection between them (as depicted in FIG. 48). Again, vacuum is used to prevent voids from forming at bonding sheet 302 to substrate components interfaces. Lamination is performed under pressure (applied on substrates) and controlled temperature ramping. During temperature ramping the substrates 304 and 310 are heated to allow solder of solder bumps 308 to melt and to form the Z-connection between metal pads 308 and 312 on the matching substrates 304 and 310.” Peters, [20:59-21:5].</p> <p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Peters discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method. This reduces the cycle time for manufacturing and testing of the structure, and increases the types of processing techniques which may be used to form the different parts of the final structure.” Peters, [7:36-7:50].</p>
--	---



	<p>Peters, FIG. 1</p> <p>“As shown in the figure, in accordance with the present invention, power and ground interconnections are routed between the mounting substrate 102 and the chip(s) 104 without passing through the signal core 106. On the other hand, the signal lines are routed between the mounting substrate 102 and the chip(s) 104 by passing only through the signal core. This architecture provides electrical isolation between the power, ground, and signal interconnections (and hence reduces noise and other problems caused by capacitive coupling between lines) while increasing the density of signal lines which can be connected between the substrate and chip(s). Signal core 106 includes a power/ground layer 109 positioned between signal layers which are on either side of that substrate and together form the basis for the signal core. Power/ground layer 109 acts to reduce cross-talk between signal lines on the same or different signal layers of signal core 106.” Peters, [7:51-7:67].</p> <p>“As shown in FIG. 1, edge connectors 1500 may be used to electrically connect different ground layers (e.g., the lower surface of the lower power/ground substrate to the upper surface of the upper power/ground substrate), different power layers (e.g., the upper surface of the lower power/ground substrate to the lower surface of the upper power/ground substrate), or the power/ground layer of the signal core to other ground or power layers of the interposer. Although a single set of edge connectors 1500 is shown in the figure, note that if the upper and lower power/ground substrates are fabricated separately (rather than formed from a flexible substrate which is bent into a “U” shape), then a set of connectors 1500 may be used at both ends of the two power/ground substrates. FIG. 2 is a schematic cross-sectional view of another embodiment of the signal interposer 100 positioned between the printed board 102 and the integrated circuit chip 104.” Peters, [8:1-8:17].</p>
--	--

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

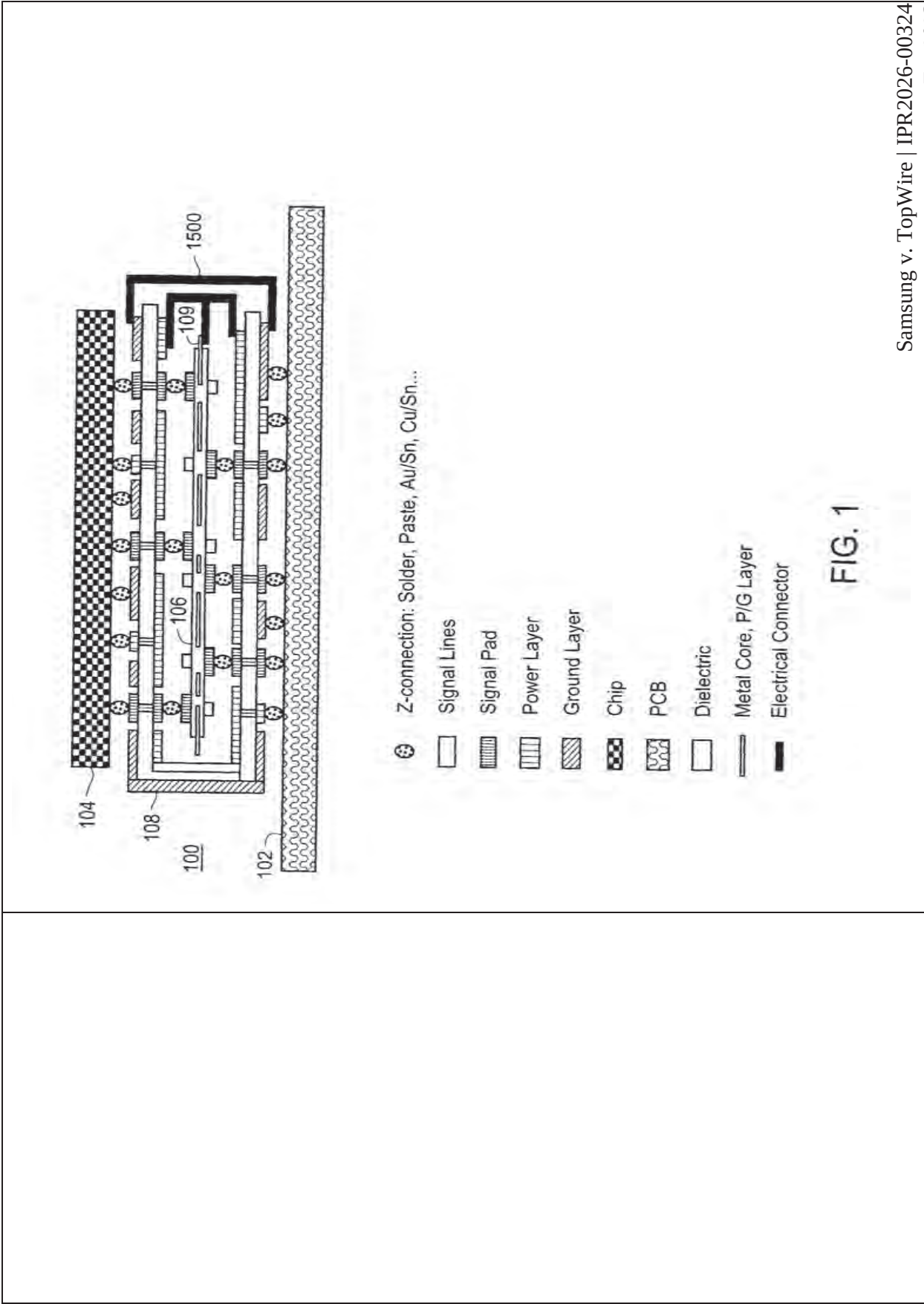
	<p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom ends of the plurality of metal pillars of the bottom package substrate via the plurality of metal pillars of the bottom package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Peters discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a schematic cross-sectional view of one embodiment of the reduced cross-talk signal interposer 100 of the present invention, and is shown positioned between a printed circuit board 102 and an integrated circuit chip 104. The legend for the figure identifies some of the components of the complete structure. As shown in the figure, interposer 100 includes two primary sections; a signal core 106 and a power/ground wrap 108. The two sections can be fabricated and tested separately and then joined together using a z-connection technology, e.g., solder bumps, anisotropic conducting polymers, or another suitable method. This</p>

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	reduces the cycle time for manufacturing and testing of the structure, and increases the types of processing techniques which may be used to form the different parts of the final structure.” Peters, [7:36-7:50].
--	---



	<p>Peters, FIG. 1</p> <p>“As shown in the figure, in accordance with the present invention, power and ground interconnections are routed between the mounting substrate 102 and the chip(s) 104 without passing through the signal core 106. On the other hand, the signal lines are routed between the mounting substrate 102 and the chip(s) 104 by passing only through the signal core. This architecture provides electrical isolation between the power, ground, and signal interconnections (and hence reduces noise and other problems caused by capacitive coupling between lines) while increasing the density of signal lines which can be connected between the substrate and chip(s). Signal core 106 includes a power/ground layer 109 positioned between signal layers which are on either side of that substrate and together form the basis for the signal core. Power/ground layer 109 acts to reduce cross-talk between signal lines on the same or different signal layers of signal core 106.” Peters, [7:51-7:67].</p> <p>“As shown in FIG. 1, edge connectors 1500 may be used to electrically connect different ground layers (e.g., the lower surface of the lower power/ground substrate to the upper surface of the upper power/ground substrate), different power layers (e.g., the upper surface of the lower power/ground substrate to the lower surface of the upper power/ground substrate), or the power/ground layer of the signal core to other ground or power layers of the interposer. Although a single set of edge connectors 1500 is shown in the figure, note that if the upper and lower power/ground substrates are fabricated separately (rather than formed from a flexible substrate which is bent into a “U” shape), then a set of connectors 1500 may be used at both ends of the two power/ground substrates. FIG. 2 is a schematic cross-sectional view of another embodiment of the signal interposer 100 positioned between the printed board 102 and the integrated circuit chip 104.” Peters, [8:1-8:17].</p>
--	--

Appendix A-27 - Invalidity of U.S. Patent No. 9859202 in view of Peters - U.S. Patent No. 6521530

	<p>To the extent Plaintiff contends that Peters fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastious '170 - U.S. Patent No. 7049170

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Savastious '170 - U.S. Patent No. 7049170

U.S. Patent No. 7049170 ("Savastious '170") is titled Integrated Circuits and Packaging Substrates with Cavities, and Attachment Methods Including Insertion of Protruding Contact Pads into Cavities and lists Sergey Savastious, Patrick B. Halahan, and Sam Kao as inventors. Savastious '170 is assigned to Tru-Si Technologies, Inc. Savastious '170 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 ("the '202 Patent") under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff's apparent infringement theory.² Savastious '170 is a U.S. patent that was filed December 17, 2003 and published June 23, 2005. Savastious '170 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Savastious '170, or otherwise rendered obvious by disclosures and teachings of Savastious '170, including under TopWire's apparent interpretation of the Asserted Claims as Samsung understands them from TopWire's Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Savastious '170 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Savastious '170 with: (1) the knowledge of one of ordinary skill in the art ("POSITA") to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung's other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung's Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Savastious '170, either alone or in combination with other prior art cited by Samsung and/or with

¹ As used herein, "Asserted Claims" refers only to those claims charted in TopWire's March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court's order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire's apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung's interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Savastiouk '170 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

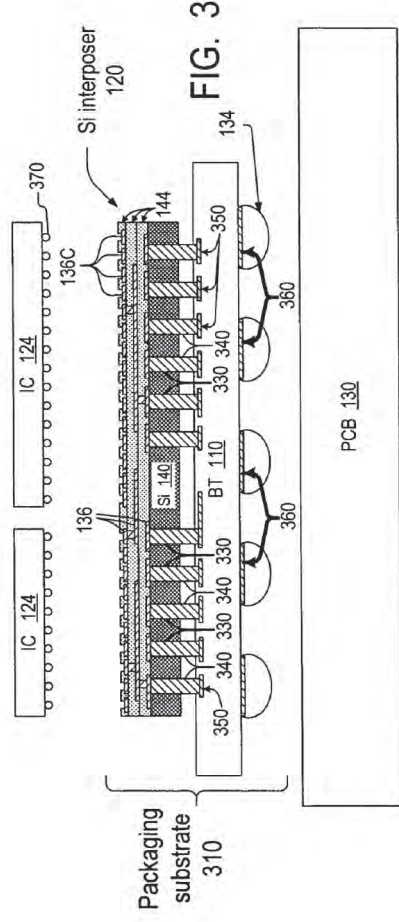
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Savastiouk '170 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Savastiouk '170 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Savastiouk '170 discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>"FIG. 1, die (“IC”) 124 is flip-chip attached, with solder 126, to the intermediate substrate 110 (“BGA substrate”), and BGA substrate 110 is soldered to PCB 130 (with solder 134). BGA substrate 110 provides interconnect lines (not shown) between die 124 and PCB 130." Savastiouk '170, [1:26-1:31].</p>

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>"FIG. 2 illustrates another package with two intermediate substrates 110, 120 between dies (ICs) 124 and PCB 130. Intermediate substrate 110 is a BT substrate, soldered to the underlying PCB 130 with solder balls 134. Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown). Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140 and separated by dielectric layers 144. Dies 124 are attached to interposer 120 with their contact pads facing up." Savastiouk '170, [1:63-2:5].</p> <p>"FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later. Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330." Savastiouk '170, [3:52-4:13].</p>
--	--



Savastiouk '170, FIG. 3

"FIG. 12 is similar to FIG. 11, but solder balls 1210 have been attached to contact pads 136 C. Solder balls 1210 eliminate the need for solder balls 370 (FIG. 3) on dies 124. The packaging substrate manufacturer can provide solder balls 1210 to simplify the die 124 attachment for the substrate buyers." Savastiouk '170, [9:3-9:8].

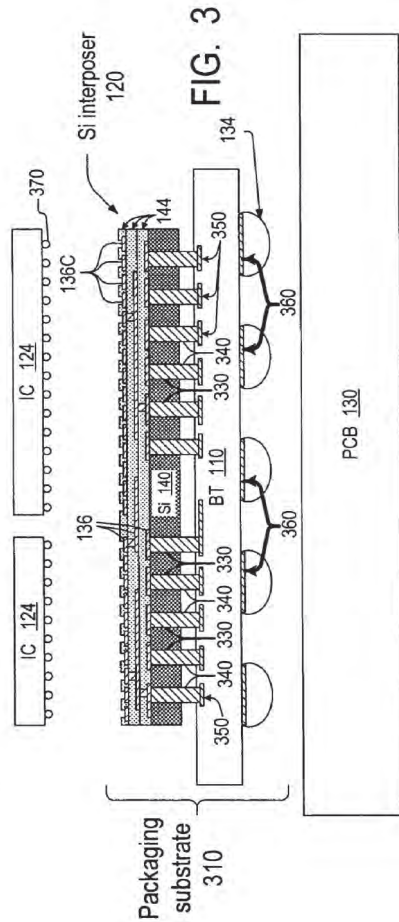
"FIGS. 13–14 illustrate a possible manufacturing sequence with multiple die levels 124. 1, 124. 2, 124. 3 attached to the packaging substrate. The packaging substrate is manufactured as in FIG. 12. The interposer vias are marked 330. 0 (instead of 330 as in FIG. 12), the contact pads at the bottom of the interposer are marked 340. 0, and the solder at the top is marked 1210. 0. Each die 124. 1 has one or more metalized through vias 330. 1 formed in

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>the die's semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1." Savastiouk '170, [9:43-9:56].</p> <p>"FIG. 15. The attachment of dies 124. 1 to interposer 120 is performed by the same techniques as the attachment of the interposer to BT substrate 110. The attachment of dies 124. 2 to dies 124. 1 can also be performed in this way. As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm, below the bottom surface of silicon substrate 140. 1 of die 124. 1. The contact pads are inserted into the cavities in the top surface of the interposer." Savastiouk '170, [11:11-11:23].</p>
[1.A] a bottom package substrate;	<p>Savastiouk '170 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>"FIG. 2 illustrates another package with two intermediate substrates 110, 120 between dies (ICs) 124 and PCB 130. Intermediate substrate 110 is a BT substrate, soldered to the underlying PCB 130 with solder balls 134. Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown)." Savastiouk '170, [1:63-2:1].</p> <p>"FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later. Silicon interposer 120</p>

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330. Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads 350 to contact pads 360 at the bottom surface of substrate 110." Savastiouk '170, [3:52-4:18].</p>
--	---



Savastiouk '170, FIG. 3.

"Interposer 120 (diced or undiced) can be attached to a conventional BT substrate 110 with solder, conductive epoxy, anisotropic adhesive, thermocompression, or possibly by other techniques, known or to be invented. In some embodiments, however, specially processed BT substrates are used to minimize the interposer handling." Savastiouk '170, [6:59-6:64].

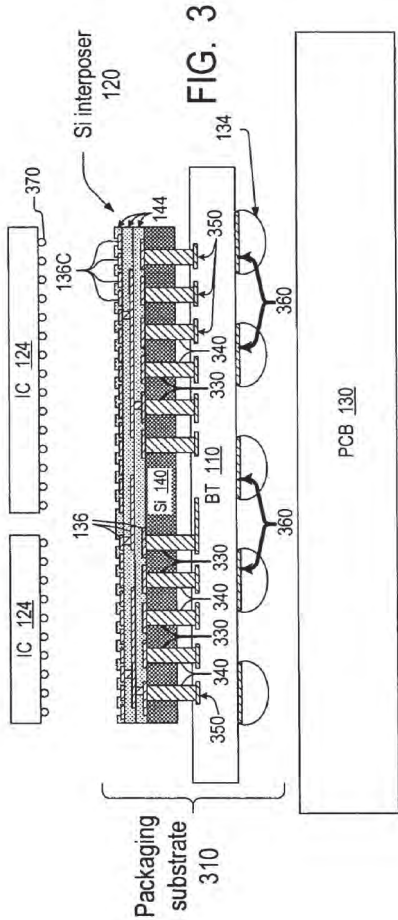
"BT substrate 110 of FIGS. 9 and 10 is formed from one or more BT layers laminated in a conventional manner. Three layers 110. 1, 110. 2, 110. 3 are shown, but any number of layers can be present. Thin film metal layers 910 (e.g. copper) are formed on BT layers 110.i (i=1, 2, 3) and on the bottom side of layer 110. 1 in a conventional manner to provide signal routing paths and ground and power planes. Layers 910 are interconnected through vias in the BT layers 110.i (i.e. 110. 1, 110. 2, 110. 3) using known techniques to provide conductive paths

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastious '170 - U.S. Patent No. 7049170

	<p>between contact pads 350 and contact pads 360. The bottom metal layer 910 provides contact pads 360 (FIG. 3) at the bottom surface of BT substrate 110." Savastious '170, [7:14-7:26].</p> <p>"Silicon interposer contact pads 340 will be inserted into these cavities to form a reliable mechanical and electrical contact. In one embodiment, each cavity 920 has a diameter D_{cav}=150 μm to accommodate a 50 μm to 60 μm diameter D_c of the contact pads 340. D_c can be calculated starting with the diameter D_v (FIG. 4) of via 330, by subtracting double the thickness of the layers 410, 420, 430. 1, 444, 448. The depth H_{cav} of each cavity 920 (about equal to the thickness of layer 110. 3) is 50 μm for a 50 μm height H_d of contact pads 340 (H_{cav} is measured to the top surface of contact pads 350)." Savastious '170, [7:33-7:44].</p> <p>"FIGS. 13–14 illustrate a possible manufacturing sequence with multiple die levels 124. 1, 124. 2, 124. 3 attached to the packaging substrate. The packaging substrate is manufactured as in FIG. 12. The interposer vias are marked 330. 0 (instead of 330 as in FIG. 12), the contact pads at the bottom of the interposer are marked 340. 0, and the solder at the top is marked 1210. 0." Savastious '170, [9:43-9:49].</p> <p>To the extent Plaintiff contends that Savastious '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Savastious '170 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

"FIG. 2 illustrates another package with two intermediate substrates 110, 120 between dies (ICs) 124 and PCB 130. Intermediate substrate 110 is a BT substrate, soldered to the underlying PCB 130 with solder balls 134. Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown)." Savastiouk '170, [1:63-2:1].

"FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later. Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140." Savastiouk '170, [3:52-3:58].



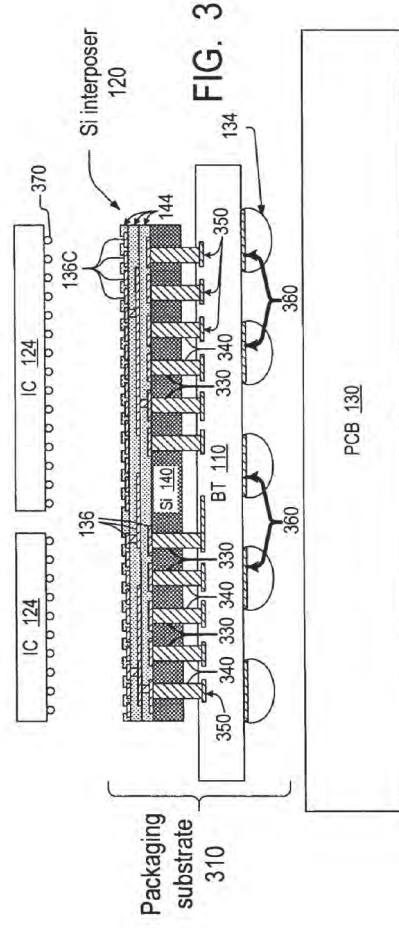
Savastiouk '170, FIG. 3.

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>"Silicon interposer 120 can be manufactured using conventional techniques. See e.g. the aforementioned U.S. Pat. No. 6,322,903. Other techniques are described in U.S. patent application Ser. No. 10/410,929 filed on Apr. 9, 2003 by P. Halahan et al., entitled "Electroplating and electroless plating of conductive materials into openings, and structures obtained thereby", incorporated herein by reference. Still other techniques can possible be used, whether known or to be invented." Savastiouk '170, [4:51-4:59].</p> <p>"Interposer 120 (diced or undiced) can be attached to a conventional BT substrate 110 with solder, conductive epoxy, anisotropic adhesive, thermocompression, or possibly by other techniques, known or to be invented." Savastiouk '170, [6:59-6:62].</p> <p>"Silicon interposer contact pads 340 will be inserted into these cavities to form a reliable mechanical and electrical contact." Savastiouk '170, [7:33-7:35].</p> <p>"Interposer wafer 120 is placed on BT substrate 110 (FIG. 10). Protruding contact pads 340 enter the cavities 920 and contact the solder 930 but do not necessarily reach the metal 910 of contact pads 350. A uniform height of contact pads 340 is not required for a good electrical contact. Underfill 940 spreads out under the interposer." Savastiouk '170, [7:66-8:4].</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Savastiouk '170 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>"Underfill 940 spreads out under the interposer. In the embodiment shown, the bottom surface of silicon 140 does not reach the BT substrate. Underfill 940 helps insulate the silicon from solder 930." Savastiouk '170, [8:4-8:7].</p> <p>"In one embodiment, the final value of the gap G 1 between the silicon 140 and the BT substrate 110 is 25 μm. The gap values of 5 to 10 μm and larger are believed to be appropriate to provide sufficient electrical insulation if no dielectric is formed on the bottom surface of silicon 140." Savastiouk '170, [8:20-8:25].</p>
---	--



Savastiouk '170, FIG. 3.

"As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm , below the bottom surface of silicon substrate 140. 1 of die 124. 1." Savastiouk '170, [11:16-11:22].

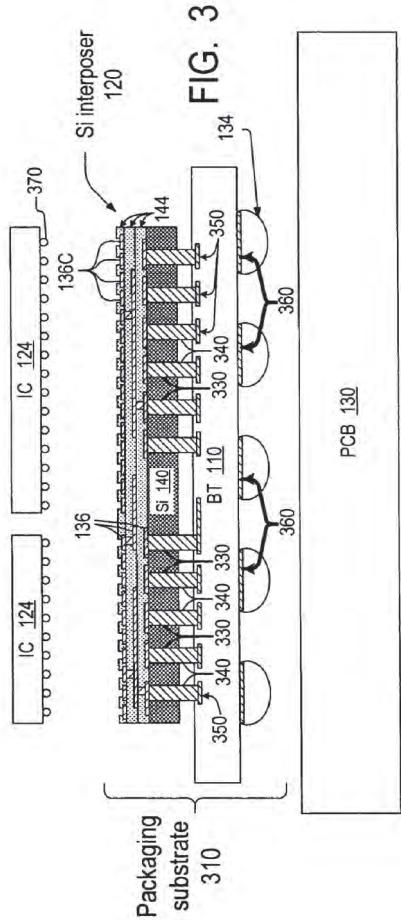
"In some embodiments, the same dimensions are obtained as for the attachment between the BT substrate and the interposer, i.e. the final value of the gap between the silicon 140, 1 and interposer 120 is 25 μm (gap values of 5 to 0 μm and larger are believed to be appropriate to provide sufficient electrical insulation if no dielectric is formed on the bottom surface of

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>silicon 140. 1); the contact 340. 1 portion inside the cavities in top layer 144 is 25 μm high (note dimension C 1 in FIG. 10)." Savastiouk '170, [11:32-11:40].</p> <p>"Underfill (not shown) can be injected between the interposer and the dies 124. 1 using known techniques." Savastiouk '170, [11:42-11:43].</p> <p>"For example, in some embodiments, before the interposer is thinned, solder paste 1210. 0 is placed into the cavities on top of the interposer, then a no-fill underfill is dispensed and a die or dies 124. 1 placed on the interposer, then a heating step is performed." Savastiouk '170, [11:48-11:52].</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Savastiouk '170 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>"Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140" Savastiouk '170, [2:2-2:3].</p>

	<p>FIG. 3</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Savastiouk '170, FIG. 3.</p> <p>"Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140." Savastiouk '170, [4:9-4:11].</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Savastiouk '170 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p>See, e.g.:</p>

"Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330." Savastiouk '170, [4:9-4:13].



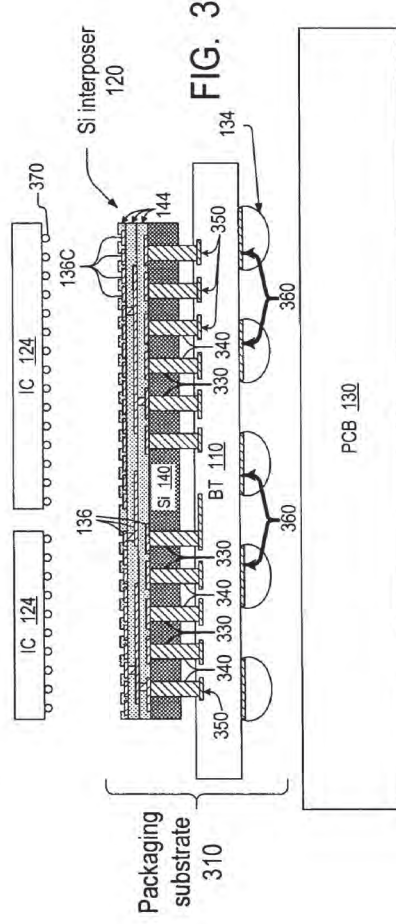
Savastiouk '170, FIG. 3.

"Vias 330 (FIG. 4) are etched in the top surface of silicon substrate 140 (e.g. monocrystalline silicon) by DRIE (deep reactive ion etching) to an exemplary depth $H_v=150\text{ }\mu\text{m}$. (The dimensions, etching processes, and other particulars are exemplary and not limiting.) The via diameter D_v is $25\text{ }\mu\text{m}$ to $100\text{ }\mu\text{m}$." Savastiouk '170, [4:60-4:65].

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>"Copper 430. 2 is electroplated on nickel 448 to fill the vias 330 and possibly protrude out of the vias." Savastiouk '170, [5:17-5:18].</p> <p>"In some embodiments, metal 430. 2 does not fill the through-silicon vias. Metal 430. 2 is a thin film deposited over the via sidewalls, and it can be part of a layer 136." Savastiouk '170, [6:53-6:55].</p> <p>"Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die's semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1." Savastiouk '170, [9:50-9:56].</p> <p>"Dies 124. 2 may be similar to dies 124. 1, but there is no solder on dies 124. 2. Dies 124. 2 include metalized vias 330. 2 in semiconductor substrates 140. 2, and contact pads 340. 2 protruding out of the vias." Savastiouk '170, [10:10-10:13].</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;	<p>Savastiouk '170 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

"Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124." Savastiouk '170, [3:57-4:8].

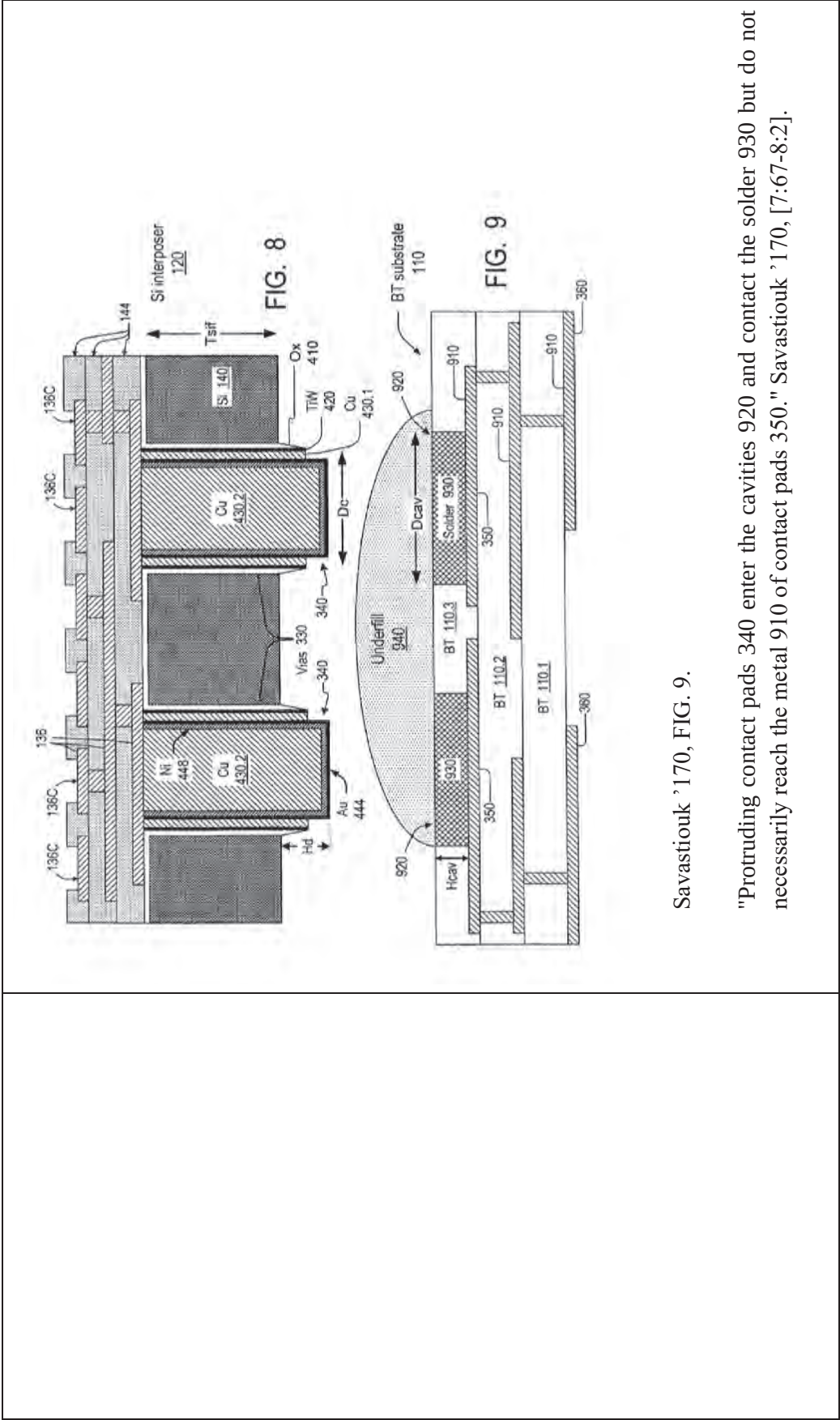


Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>Savastiouk '170, FIG. 3.</p> <p>"Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330." Savastiouk '170, [4:9-4:13].</p> <p>"FIG. 12 is similar to FIG. 11, but solder balls 1210 have been attached to contact pads 136 C. Solder balls 1210 eliminate the need for solder balls 370 (FIG. 3) on dies 124. The packaging substrate manufacturer can provide solder balls 1210 to simplify the die 124 attachment for the substrate buyers. Solder 1210 can be attached to the interposer at any fabrication stage. In one embodiment, solder 1210 is attached to pads 136 C before the interposer wafer is thinned, i.e. before the stage of FIG. 8." Savastiouk '170, [9:3-9:11].</p> <p>"Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die's semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1." Savastiouk '170, [9:50-9:56].</p> <p>"As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3." Savastiouk '170, [11:16-11:19].</p> <p>"Metal layer 1110 (e.g. gold or nickel) can be deposited on the sidewalls and bottom of the vias in top layer 144 to improve the electrical connection and provide a barrier against copper</p>
--	---

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>136 diffusion into solder 1210. 0. Alternatively, metal 1110 can be plated only on the bottom of the openings to provide a copper diffusion barrier." Savastiouk '170, [11:26-11:31].</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Savastiouk '170 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>"To facilitate the interposer handling, the metal contact pads 340 are formed to protrude out of vias 330. The protruding contact pads 340 are inserted into cavities in BT substrate 110, as explained in more detail below." Savastiouk '170, [4:45-4:48].</p> <p>"Metal contact pads 340 are metal protrusions formed by the metal layers 430. 2, 448, 444, 430. 1, 420 below the bottom surface of silicon 140." Savastiouk '170, [6:33-6:35].</p> <p>"The depth H_{cv} of each cavity 920 (about equal to the thickness of layer 110.3) is 50 μm for a 50 μm height H_d of contact pads 340 (H_{cv} is measured to the top surface of contact pads 350)." Savastiouk '170, [7:42-7:45].</p>

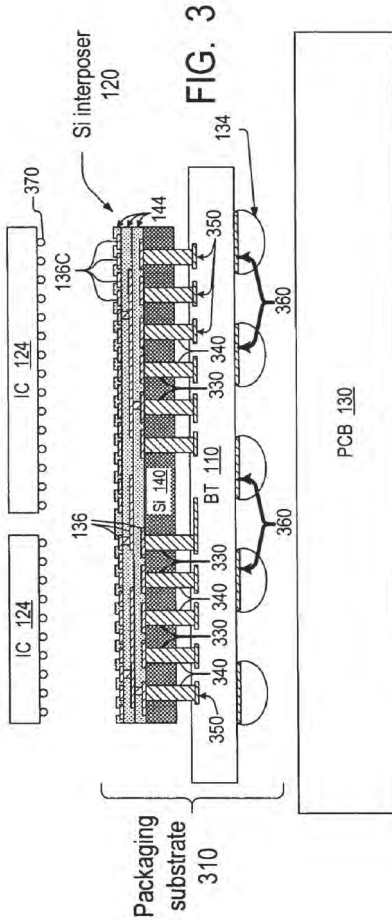


Savastiouk '170, FIG. 9.

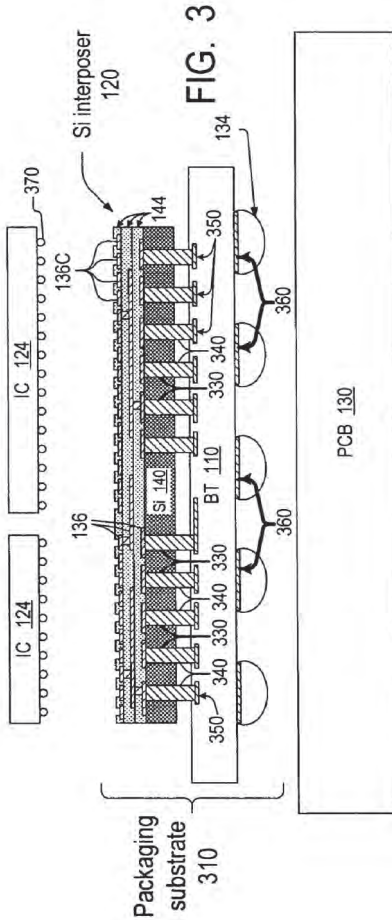
"Protruding contact pads 340 enter the cavities 920 and contact the solder 930 but do not necessarily reach the metal 910 of contact pads 350." Savastiouk '170, [7:67-8:2].

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>"Contact pads 340. 1 protrude out of the respective vias 330. 1. The dies 124. 1 can be manufactured using the same techniques as described above for interposer 120 (involving the wafer thinning to expose the contact pads 340. 1)." Savastiouk '170, [9:56-9:60].</p> <p>"As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm, below the bottom surface of silicon substrate 140. 1 of die 124. 1." Savastiouk '170, [11:16-11:22].</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Savastiouk '170 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

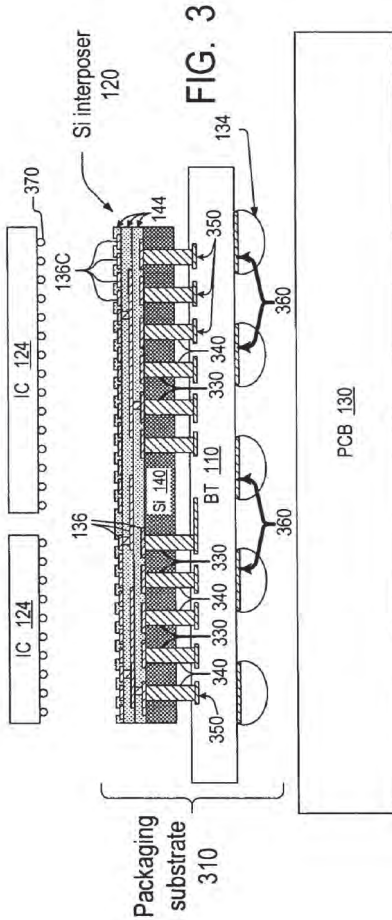
	 <p>FIG. 3</p>
<p>[1.1] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Savastiouk '170, FIG. 3.</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Savastiouk '170 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p>

	<p style="text-align: center;">FIG. 3</p>
	<p>Savastiouk '170, FIG. 3.</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of</p>	<p>Savastiouk '170 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

top metal pillars of the bottom package substrate; and	 <p>FIG. 3</p>
	<p>Savastiouk '170, FIG. 3.</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein	<p>Savastiouk '170 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p>

	<p>FIG. 3</p>
	<p>Savastiouk '170, FIG. 3.</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Savastiouk '170 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p>See, e.g.:</p>

<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Savastiouk '170, FIG. 3.</p>
	<p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Savastiouk '170 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

	<div><p>FIG. 3</p></div> <p>Savastiouk '170, FIG. 3.</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced	Savastiouk '170 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

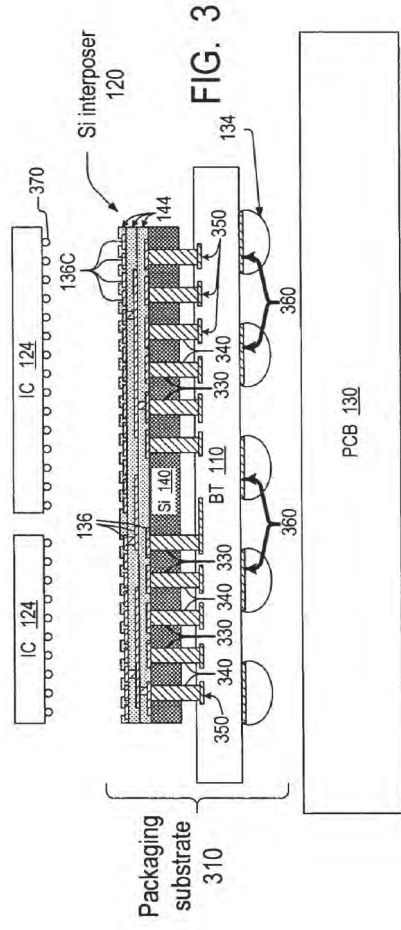
Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

<p>downwardly from the bottom surface of the top package substrate.</p>	<p><i>See, e.g.:</i></p> <p>"Thin interposers are desirable because to reduce the package size and improve the electrical characteristics (by shortening the conductive paths through the interposer). Also, in some embodiments, it is easier to manufacture the through-silicon vias if the interposer is thin." Savastiouk '170, [2:56-2:61].</p> <p>"The semiconductor substrate of the interposer can be quite thin, e.g. 100 μm or thinner." Savastiouk '170, [3:2-3:3].</p> <p>"Substrate 140 has substantially planar top and bottom surfaces, and is quite thin" Savastiouk '170, [3:58-3:59].</p> <p>"FIG. 12. The interposer vias are marked 330. 0 (instead of 330 as in FIG. 12), the contact pads at the bottom of the interposer are marked 340. 0, and the solder at the top is marked 1210. 0. Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die's semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1. Contact pads 340. 1 protrude out of the respective vias 330. 1." Savastiouk '170.,</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
---	--

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Savastiouk '170 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>"FIG. 2 illustrates another package with two intermediate substrates 110, 120 between dies (ICs) 124 and PCB 130. Intermediate substrate 110 is a BT substrate, soldered to the underlying PCB 130 with solder balls 134. Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown). Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140 and separated by dielectric layers 144. Dies 124 are attached to interposer 120 with their contact pads facing up." Savastiouk '170, [1:63-2:5].</p> <p>"FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later." Savastiouk '170, [3:52-3:56].</p>



Savastiouk '170, FIG. 3.

"FIGS. 13–14 illustrate a possible manufacturing sequence with multiple die levels 124. 1, 124. 2, 124. 3 attached to the packaging substrate. The packaging substrate is manufactured as in FIG. 12. The interposer vias are marked 330. 0 (instead of 330 as in FIG. 12), the contact pads at the bottom of the interposer are marked 340. 0, and the solder at the top is marked 1210. 0." Savastiouk '170, [9:43-9:49].

"At step 1430, dies 124. 1 are soldered to interposer 120 with solder 1210. 0, at a temperature of about 218° C. or higher, but below 230° C. not to melt the solder 930. The copper from contact pads 340. 1 dissolves in solder 1210. 0 and increases its melting temperature to about 230° C. Solder 1210. 1 may melt, but its melting temperature does not increase because the solder 1210. 1 is not in contact with copper or other material that could increase the solder

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	<p>melting temperature (the top surface portions of the top contact pads of die 124. 1 are made of suitable materials to ensure that the solder melting temperature does not increase)." Savastiouk '170, [10:34-10:45].</p> <p>"For example, any number of dies can be used at each level. Also, one or more dies 124. 2 can be attached directly to interposer 120, i.e. there may be three levels of dies over one interposer area but only two levels of dies over another interposer area. Any number of die levels can be present in different interposer areas." Savastiouk '170, [10:60-10:65].</p> <p>"In some embodiments, interposer 120 and/or dies 124. 1 are provided with deep cavities 920 at the top surface to increase the mechanical strength of the solder attachment and provide a reliable electrical contact. See FIG. 15. The attachment of dies 124. 1 to interposer 120 is performed by the same techniques as the attachment of the interposer to BT substrate 110." Savastiouk '170, [11:8-11:14].</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

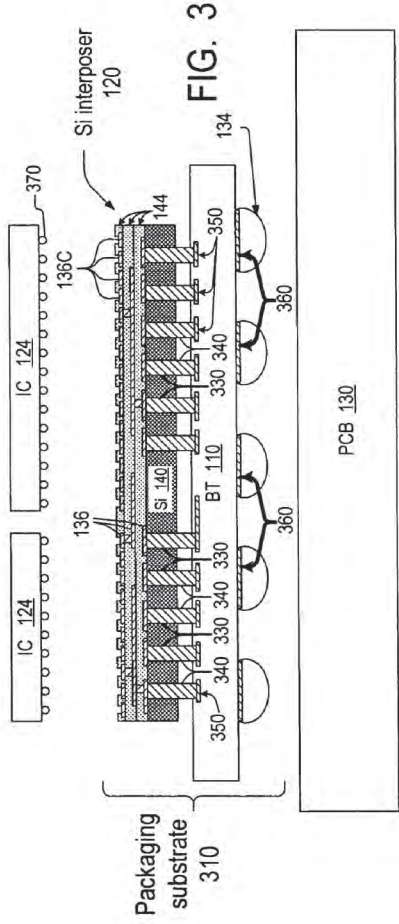
Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of	Savastiouk '170 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding

bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.

metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

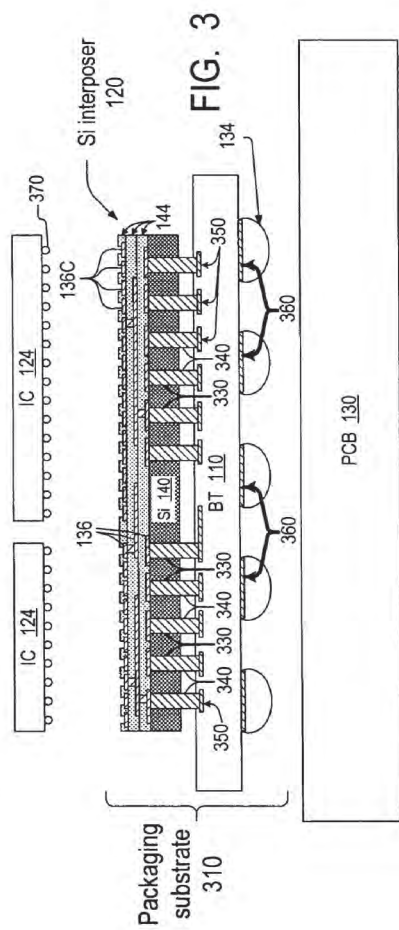
See, e.g.:



Savastiouk '170, FIG. 3.

To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastouk '170 - U.S. Patent No. 7049170

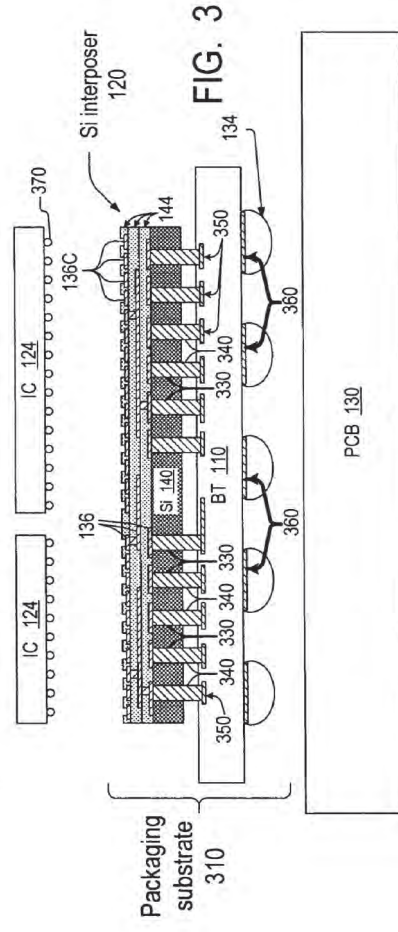
<p>Claim Limitation</p> <p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Disclosure</p> <p>Savastiouk '170 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p>See, e.g.:</p> 
	<p>Savastiouk '170, FIG. 3.</p> <p>To the extent Plaintiff contends that Savastiouk '170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with</p>

Appendix A-28 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '170 - U.S. Patent No. 7049170

	(i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the plurality of bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pads of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Savastiouk '170 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>



Savastiouk '170, FIG. 3.

To the extent Plaintiff contends that Savastiouk ' 170 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

U.S. Patent Publication No. 20050189636 (“Savastiouk '636”) is titled Packaging Substrates for Integrated Circuits and Soldering Methods and lists Sergey Savastiouk, Patrick B. Halahan, and Sam Kao as inventors. Savastiouk '636 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the '202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Savastiouk '636 is a U.S. patent publication that was filed May 5, 2005 and published September 1, 2005. Savastiouk '636 claims priority to US 10/739,707 filed on December 17, 2003. Savastiouk '636 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Savastiouk '636, or otherwise rendered obvious by disclosures and teachings of Savastiouk '636, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Savastiouk '636 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Savastiouk '636 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Savastiouk '636, either alone or in combination with other prior art cited by Samsung and/or with

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Savastiouk '636 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Savastiouk '636 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Savastiouk '636 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, Savastiouk '636 discloses, either expressly or inherently, a structure. <i>See, e.g.:</i> “FIG. 1 illustrates another package with two intermediate substrates 110, 120 between dies (ICs) 124 and PCB 130. Intermediate substrate 110 is a BT substrate, soldered to the underlying PCB 130 with solder balls 134. Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown). Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140 and separated by dielectric

layers 144. Dies 124 are attached to interposer 120 with their contact pads facing up. Savastriouk '636, [0008].

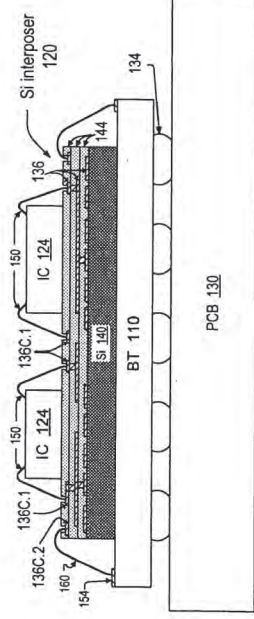
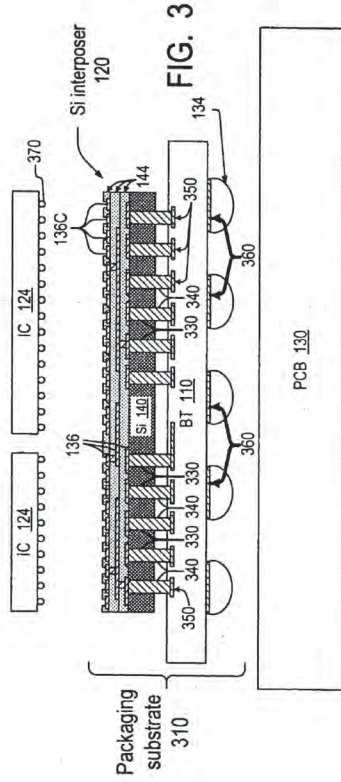


FIG. 1
PRIOR ART

Savastiouk '636, FIG. 1

“FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later. Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on

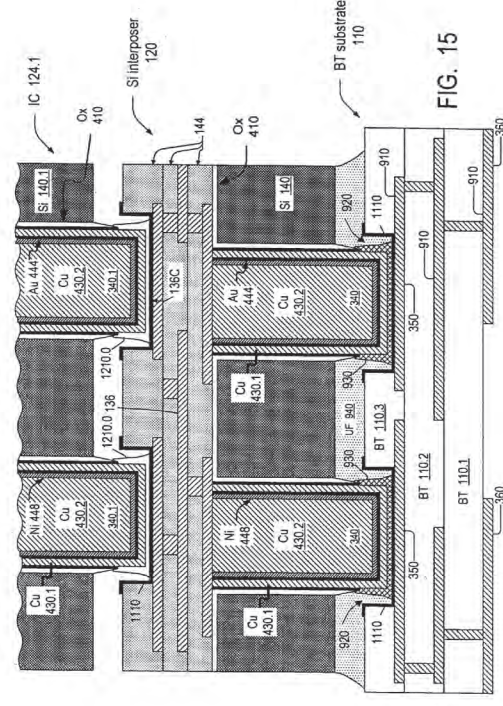
the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330.” Savastiouk '636, [0025-0027].



Savastiouk '636, FIG. 3

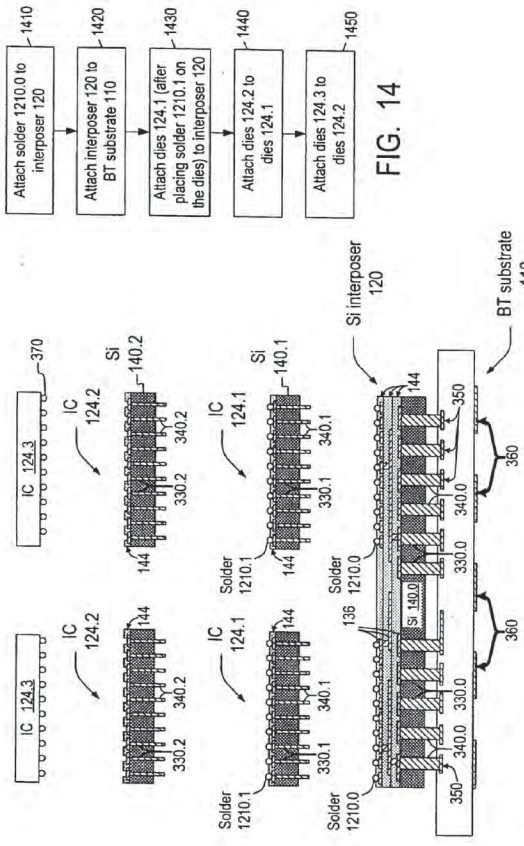
“FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm , below the bottom surface of silicon substrate 140. 1 of die 124. 1. The contact pads are inserted into the cavities in the top surface of the interposer. These cavities

are the openings in top layer 144 that expose the contact pads 136 C." Savastiouk '636, [0048].



Savastiouk '636, FIG. 15

“FIGS. 13-14 illustrate a possible manufacturing sequence with multiple die levels 124. 1, 124. 2, 124. 3 attached to the packaging substrate. The packaging substrate is manufactured as in FIG. 12. The interposer vias are marked 330. 0 (instead of 330 as in FIG. 12), the contact pads at the bottom of the interposer are marked 340. 0, and the solder at the top is marked 1210. 0. Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die's semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from

	<p>contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1. Contact pads 340. 1 protrude out of the respective vias 330. 1.” Savastiouk '636, [0067-0069].</p>  <p>FIG. 13</p> <p>FIG. 14</p> <p>Savastiouk '636, FIG. 13</p>
<p>[1.A] a bottom package substrate;</p>	<p>Savastiouk '636 discloses, either expressly or inherently, a bottom package substrate.</p> <p>See, e.g.:</p>

“FIG. 1 illustrates another package with two intermediate substrates 110, 120 between dies (ICs) 124 and PCB 130. Intermediate substrate 110 is a BT substrate, soldered to the underlying PCB 130 with solder balls 134. Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown).” Savastiouk '636, [0008].

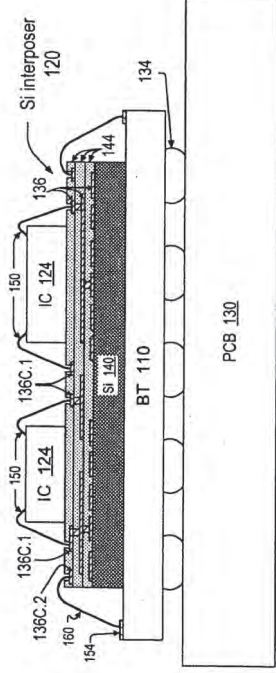


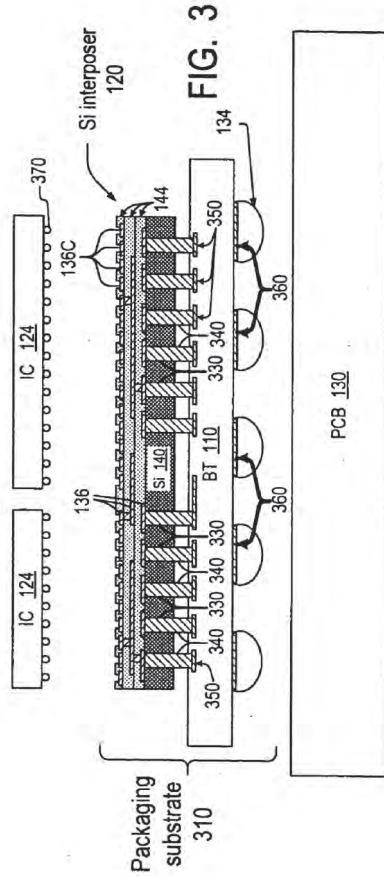
FIG. 1
PRIOR ART

Savastiouk '636, FIG. 1

“For commercial reasons, a manufacturer may sell packaging substrates consisting substantially of a silicon interposer 120 and a BT substrate 110 (FIG. 2). Then the buyers of the packaging substrates attach the dies 124 and the PCBs 130 to the packaging substrates.” Savastiouk '636, [0010].

“In some embodiments of the present invention, a packaging substrate is provided which, like the packaging substrate of FIG. 2, includes a silicon interposer and a BT substrate. However, the silicon interposer has contact pads both on the top and the bottom, and has

	<p>through-silicon vias made in the silicon substrate of the interposer. Conductive paths going through the through-silicon vias connect the contact pads on the top of the interposer to the contact pads on the bottom.” Savastiouk ’636, [0014].</p> <p>“FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later. Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330. Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads 350 to contact pads 360 at the bottom surface of substrate 110.” Savastiouk ’636, [0024-0028].</p>
--	---



Savastiouk '636, FIG. 3

“BT substrate 110 of FIGS. 9 and 10 is formed from one or more BT layers laminated in a conventional manner. Three layers 110. 1, 110. 2, 110. 3 are shown, but any number of layers can be present. Thin film metal layers 910 (e.g. copper) are formed on BT layers 110.i (i=1, 2, 3) and on the bottom side of layer 110. 1 in a conventional manner to provide signal routing paths and ground and power planes. Layers 910 are interconnected through vias in the BT layers 110.i (i.e. 110. 1, 110. 2, 110. 3) using known techniques to provide conductive paths between contact pads 350 and contact pads 360.” Savastiouk '636, [0048-0049].

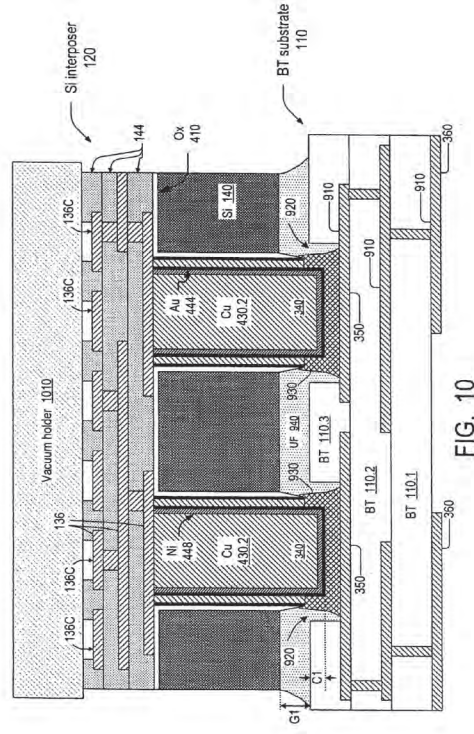
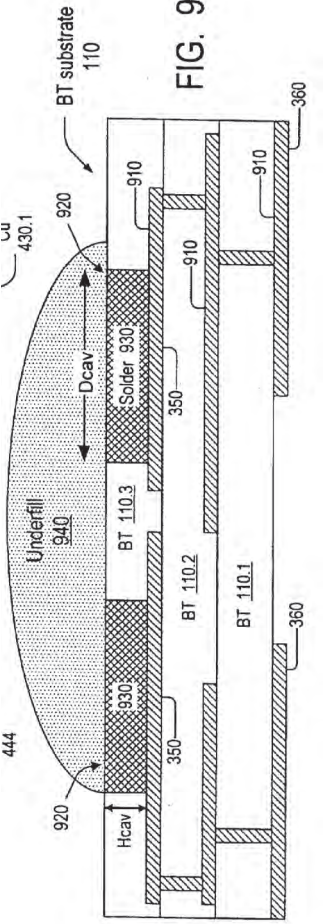


FIG. 10

Savastiouk '636, FIG. 10

“The bottom metal layer 910 provides contact pads 360 (FIG. 3) at the bottom surface of BT substrate 110. The difference between the BT substrate 110 of FIG. 9 and a conventional BT substrate is that the top contact pads 350, and the top metal layer 910, are formed below the top BT layer 110. 3. In FIG. 9, the top contact pads 350 and the top metal 910 are formed on BT layer 110. 2. Layer 110. 3 has vias 920 exposing the contact pads 350. Vias 920 form cavities in the top surface of BT substrate 110. Silicon interposer contact pads 340 will be inserted into these cavities to form a reliable mechanical and electrical contact.” Savastiouk ’636, [0049-0050].

	 <p>FIG. 9</p> <p>Savastiouk '636, FIG. 9</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Savastiouk '636 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“FIG. 1 illustrates another package with two intermediate substrates 110, 120 between dies (ICs) 124 and PCB 130. Intermediate substrate 110 is a BT substrate, soldered to the underlying PCB 130 with solder balls 134. Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown).” Savastiouk '636, [0008].</p>

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>“For commercial reasons, a manufacturer may sell packaging substrates consisting substantially of a silicon interposer 120 and a BT substrate 110 (FIG. 2). Then the buyers of the packaging substrates attach the dies 124 and the PCBs 130 to the packaging substrates.” Savastiouk '636, [0010].</p> <p>“In some embodiments of the present invention, a packaging substrate is provided which, like the packaging substrate of FIG. 2, includes a silicon interposer and a BT substrate. However, the silicon interposer has contact pads both on the top and the bottom, and has through-silicon vias made in the silicon substrate of the interposer.” Savastiouk '636, [0014].</p> <p>“FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later. Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140.” Savastiouk '636, [0025-0026].</p> <p>“Interposer 120 (diced or undiced) can be attached to a conventional BT substrate 110 with solder, conductive epoxy, anisotropic adhesive, thermocompression, or possibly by other techniques, known or to be invented.” Savastiouk '636, [0048].</p> <p>“Multiple interposers can be placed on BT substrate 110, and the solder reflow and underfill curing can be performed in a single heating step for all the interposers.” Savastiouk '636, [0060].</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

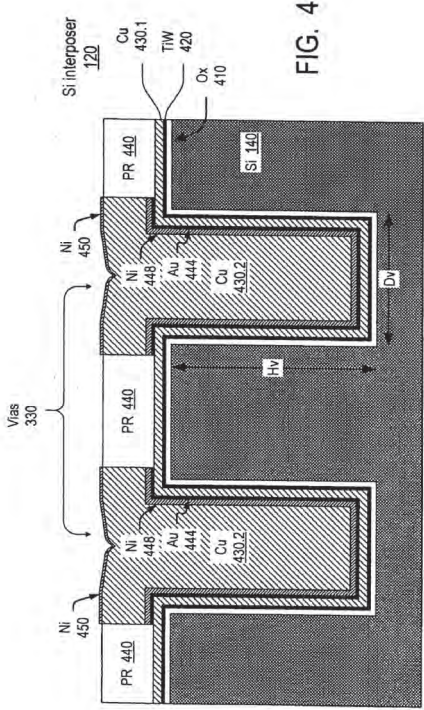
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Savastiouk '636 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330. Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads 350 to contact pads 360 at the bottom surface of substrate 110.” Savastiouk '636, [0027-0028].</p> <p>“Metal contact pads 340 are metal protrusions formed by the metal layers 430. 2, 448, 444, 430. 1, 420 below the bottom surface of silicon 140. In some embodiments, the height Hd of metal contact pads 340 is 50 μm.” Savastiouk '636, [0043-0044].</p> <p>“Interposer wafer 120 is placed on BT substrate 110 (FIG. 10). Protruding contact pads 340 enter the cavities 920 and contact the solder 930 but do not necessarily reach the metal 910 of contact pads 350. A uniform height of contact pads 340 is not required for a good electrical contact. Underfill 940 spreads out under the interposer. In the embodiment shown, the bottom surface of silicon 140 does not reach the BT substrate.” Savastiouk '636, [0055-0056].</p> <p>“In the embodiment shown, the bottom surface of silicon 140 does not reach the BT substrate. Underfill 940 helps insulate the silicon from solder 930. Therefore, it is unnecessary to form a dielectric layer on the bottom silicon surface. The interposer placement can be performed with a placement tool of type SIPLACE F4 available from Siemens corporation of Germany.</p>
---	---

	<p>The placement tool picks up the interposer from the top by a vacuum holder 1010 schematically shown in FIG. 10. The vacuum pick-up flattens the interposer if the interposer is warped.” Savastiouk ’636, [0056-0057].</p> <p>“In one embodiment, the final value of the gap GI between the silicon 140 and the BT substrate 110 is 25 μm. The gap values of 5 to 10 μm and larger are believed to be appropriate to provide sufficient electrical insulation if no dielectric is formed on the bottom surface of silicon 140. The contact 340 portion inside the vias 920 is 25 μm high (C 1 =25 μm in FIG. 10). The value C 1 is in the range from 10 μm to 45 μm in some embodiments.” Savastiouk ’636, [0058-0059].</p> <p>“As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm, below the bottom surface of silicon substrate 140. 1 of die 124. 1. The contact pads are inserted into the cavities in the top surface of the interposer. These cavities are the openings in top layer 144 that expose the contact pads 136 C. Metal layer 1110 (e.g. gold or nickel) can be deposited on the sidewalls and bottom of the vias in top layer 144 to improve the electrical connection and provide a barrier against copper 136 diffusion into solder 1210. 0. Alternatively, metal 1110 can be plated only on the bottom of the openings to provide a copper diffusion barrier. In some embodiments, the same dimensions are obtained as for the attachment between the BT substrate and the interposer, i.e. the final value of the gap between the silicon 140. 1 and interposer 120 is 25 μm (gap values of 5 to 10 μm and larger are believed to be appropriate to provide sufficient electrical insulation if no dielectric is formed on the bottom surface of silicon 140. 1); the contact 340. 1 portion inside the cavities in top layer 144 is 25 μm high (note dimension C 1 in FIG. 10).</p>
--	---

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

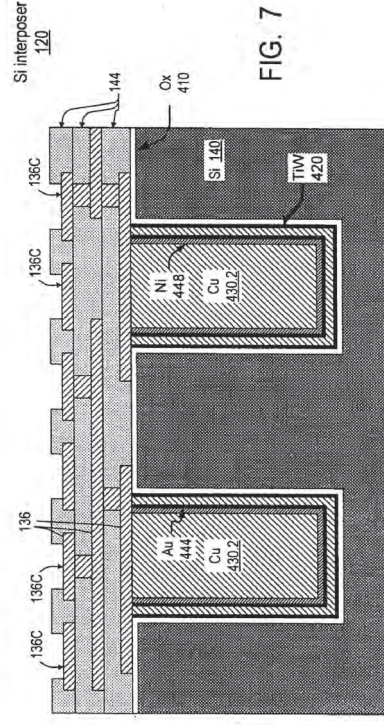
	<p>This value is in the range from 10 μm to 45 μm in some embodiments.” Savastiouk '636, [0080-0083].</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Savastiouk '636 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140 and separated by dielectric layers 144. Dies 124 are attached to interposer 120 with their contact pads facing up. The dies' contact pads are wire bonded to contact pads 136 C. 1 provided by metal layers 136. The wire bonding is done with bond wires 150.” Savastiouk '636, [0008].</p> <p>“In some embodiments, the interposer is thinned before attachment to the BT substrate. The semiconductor substrate of the interposer can be quite thin, e.g. 100 μm or thinner. The semiconductor substrate and the interposer may have substantially planar top and bottom surfaces, as opposed to interposers with cavities large enough to contain a die, with the cavities' sidewalls being thicker than the rest of the interposer to increase the interposer's mechanical strength (see U.S. patent application Ser.” Savastiouk '636, [0015].</p> <p>“Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136</p>

	<p>provide contact pads 136 C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330. Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads 350 to contact pads 360 at the bottom surface of substrate 110.” Savastiouk '636, [0026-0028].</p> <p>“Silicon interposer 120 can be manufactured using conventional techniques. See e.g. the aforementioned U.S. Pat. No. 6,322,903. Other techniques are described in U.S. patent application Ser. No. 10/410,929 filed on Apr. 9, 2003 by P. Halahan et al., entitled “Electroplating and electroless plating of conductive materials into openings, and structures obtained thereby”, incorporated herein by reference. Still other techniques can possible be used, whether known or to be invented. An exemplary manufacturing process is as follows. Vias 330 (FIG. 4) are etched in the top surface of silicon substrate 140 (e.g. monocrystalline silicon) by DRIE (deep reactive ion etching) to an exemplary depth $H_v=150\text{ }\mu\text{m}$.” Savastiouk '636, [0031].</p>
--	---



Savastiouk '636, FIG. 4

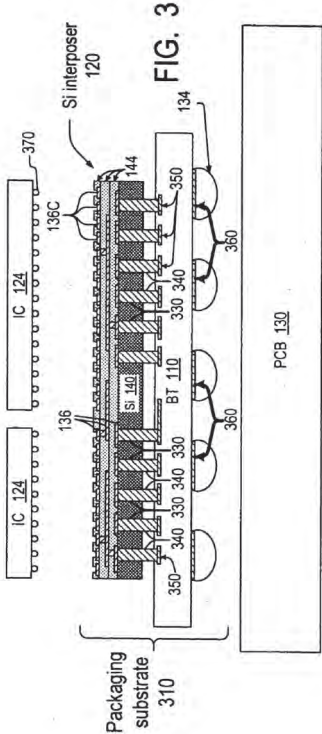
“Metal layers 136 (FIG. 7) and dielectric layers 144 are deposited on the interposer wafer and patterned to provide interconnects and, possibly, other elements as described above. In some embodiments, metal 136 is copper and dielectric 144 is polyimide, but other materials can also be used.” Savastiouk '636, [0038].

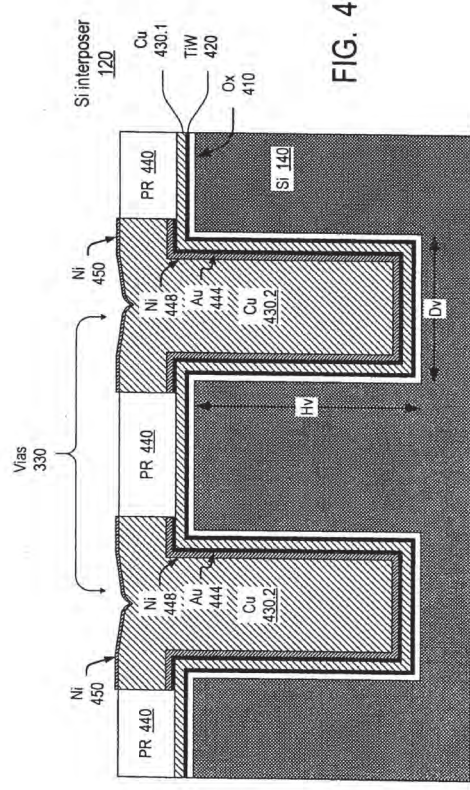


Savastiouk '636, FIG. 7

“Interposer 120 (diced or undiced) can be attached to a conventional BT substrate 110 with solder, conductive epoxy, anisotropic adhesive, thermocompression, or possibly by other techniques, known or to be invented. In some embodiments, however, specially processed BT substrates are used to minimize the interposer handling. The interposer handling should preferably be minimized if the interposer is thin. The interposer’s silicon substrate 140 can be 100 μm or thinner, the interposer can be fragile, and its heat dissipation capability can be low.” Savastiouk ’636, [0048].

To the extent Plaintiff contends that Savastouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Savastiouk '636 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p>See, e.g.:</p> <p>“Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330.” Savastiouk '636, [0027].</p> <div></div> <p>Savastiouk '636, FIG. 3</p> <p>“Vias 330 (FIG. 4) are etched in the top surface of silicon substrate 140 (e.g. monocrystalline silicon) by DRIE (deep reactive ion etching) to an exemplary depth Hv=150 μm. (The dimensions, etching processes, and other particulars are exemplary and not limiting.) The via diameter Dv is 25 μm to 100 μm.” Savastiouk '636, [0031].</p>
---	---



Savastiouk '636, FIG. 4

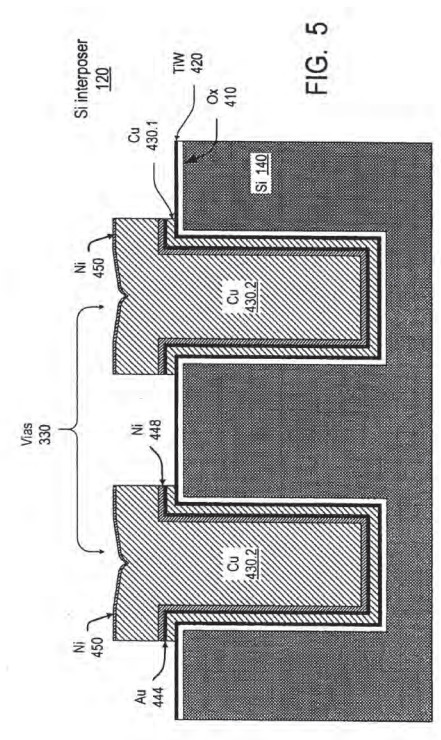
“Copper 430, 2 is electroplated on nickel 448 to fill the vias 330 and possibly protrude out of the vias.” Savastiouk ’636, [0032-0033].

“Metal contact pads 340 are metal protrusions formed by the metal layers 430. 2, 448, 444, 430. 1, 420 below the bottom surface of silicon 140. In some embodiments, the height Hd of metal contact pads 340 is 50 μm .” Savastiouk ’636, [0043-0044].

“Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die’s semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1.” Savastiouk ’636, [0060-0061].</p> <p>“Dies 124. 2 may be similar to dies 124. 1, but there is no solder on dies 124. 2. Dies 124. 2 include metalized vias 330. 2 in semiconductor substrates 140. 2, and contact pads 340. 2 protruding out of the vias.” Savastiouk ’636, [0069-0070].</p> <p>To the extent Plaintiff contends that Savastiouk ’636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Savastiouk ’636 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also</p>

	<p>be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of the interposer.” Savastiouk '636, [0026].</p> <p>“Optionally, nickel (Ni) layer 450 is electroplated on the top surface of copper layer 430. 2 to an exemplary thickness of 0.5 μm. Resist 440 is removed (FIG. 5). A wet copper etch removes the exposed portions of seed copper 430. 1, with nickel 450 acting as a mask. Nickel 450 protects copper 430. 2 in vias 330.” Savastiouk '636, [0033-0035].</p> <div><p>FIG. 5</p></div> <p>Savastiouk '636, FIG. 5</p> <p>“Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die’s semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1.” Savastiouk '636, [0060-0061].</p>
--	---

“FIG. 12 is similar to FIG. 11, but solder balls 1210 have been attached to contact pads 136 C. Solder balls 1210 eliminate the need for solder balls 370 (FIG. 3) on dies 124. The packaging substrate manufacturer can provide solder balls 1210 to simplify the die 124 attachment for the substrate buyers. Solder 1210 can be attached to the interposer at any fabrication stage. In one embodiment, solder 1210 is attached to pads 136 C before the interposer wafer is thinned, i.e. before the stage of FIG. 8.” Savastiouk ’636, [0062-0063].

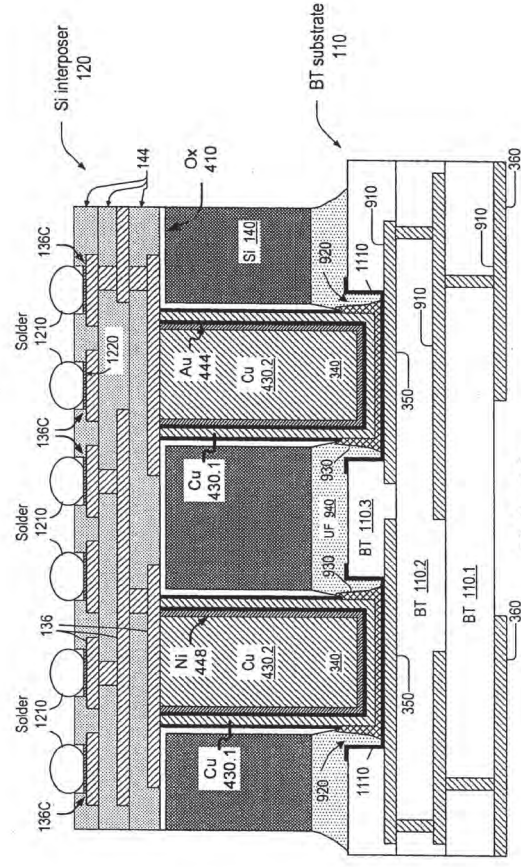


FIG. 12

Savastiouk '636, FIG. 12

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>“Dies 124. 2 may be similar to dies 124. 1, but there is no solder on dies 124. 2. Dies 124. 2 include metalized vias 330. 2 in semiconductor substrates 140. 2, and contact pads 340. 2 protruding out of the vias.” Savastiouk '636, [0069-0070].</p> <p>“Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm, below the bottom surface of silicon substrate 140. 1 of die 124. 1. The contact pads are inserted into the cavities in the top surface of the interposer. These cavities are the openings in top layer 144 that expose the contact pads 136 C.” Savastiouk '636, [0081-0082].</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Savastiouk '636 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In some embodiments of the present invention, a packaging substrate is provided which, like the packaging substrate of FIG. 2, includes a silicon interposer and a BT substrate. However, the silicon interposer has contact pads both on the top and the bottom, and has through-silicon vias made in the silicon substrate of the interposer.” Savastiouk '636, [0014].</p>

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>“Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm, below the bottom surface of silicon substrate 140. 1 of die 124. 1. The contact pads are inserted into the cavities in the top surface of the interposer.” Savastiouk '636, [0027-0028].</p> <p>“The protruding contact pads 340 are inserted into cavities in BT substrate 110, as explained in more detail below.” Savastiouk '636, [0030].</p> <p>“Metal contact pads 340 are metal protrusions formed by the metal layers 430. 2, 448, 444, 430. 1, 420 below the bottom surface of silicon 140.” Savastiouk '636, [0043].</p> <p>“In some embodiments, the height Hd of metal contact pads 340 is 50 μm.” Savastiouk '636, [0043].</p> <p>“Contact pads 340. 1 protrude out of the respective vias 330. 1.” Savastiouk '636, [0069].</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Savastiouk '636 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

	<p>“FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later. Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330.” Savastiouk '636, [0025-0027].</p> <p>“Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads 350 to contact pads 360 at the bottom surface of substrate 110. Solder balls 134 are formed on pads 360 by conventional techniques for attachment to PCB 130.” Savastiouk '636, [0027-0028].</p> <p>“The difference between the BT substrate 110 of FIG. 9 and a conventional BT substrate is that the top contact pads 350, and the top metal layer 910, are formed below the top BT layer</p>
--	---

	<p>110. 3. In FIG. 9, the top contact pads 350 and the top metal 910 are formed on BT layer 110. 2. Layer 110. 3 has vias 920 exposing the contact pads 350. Vias 920 form cavities in the top surface of BT substrate 110. Silicon interposer contact pads 340 will be inserted into these cavities to form a reliable mechanical and electrical contact.” Savastiouk ’636, [0050].</p> <p>“Interposer wafer 120 is placed on BT substrate 110 (FIG. 10). Protruding contact pads 340 enter the cavities 920 and contact the solder 930 but do not necessarily reach the metal 910 of contact pads 350. A uniform height of contact pads 340 is not required for a good electrical contact.” Savastiouk ’636, [0055].</p> <p>“Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die’s semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1. Contact pads 340. 1 protrude out of the respective vias 330. 1.” Savastiouk ’636, [0069].</p> <p>“The attachment of dies 124. 1 to interposer 120 is performed by the same techniques as the attachment of the interposer to BT substrate 110. The attachment of dies 124. 2 to dies 124. 1 can also be performed in this way. As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm, below the bottom surface of silicon substrate 140. 1 of die 124. 1.” Savastiouk ’636, [0080-0081].</p> <p>To the extent Plaintiff contends that Savastiouk ’636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with</p>
--	--

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>(i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Savastiouk '636 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads 350 to contact pads 360 at the bottom surface of substrate 110. Solder balls 134 are formed on pads 360 by conventional techniques for attachment to PCB 130. The size and spacing (pitch) of contact pads 136 C on interposer 120 matches the size and the pitch of the contact pads on dies 124. If dies 124 are silicon integrated circuits, their CTE matches the CTE of the interposer, so the pitch of contact pads 136 C can be small because the low thermal stresses at the interface between the dies and the interposer make it unnecessary to use large solder balls 370. The contact pads 340 on the bottom of the interposer match the top contact pads 350 of BT substrate 110.” Savastiouk '636, [0027-0029].</p> <p>“BT substrate 110 of FIGS. 9 and 10 is formed from one or more BT layers laminated in a conventional manner. Three layers 110. 1, 110. 2, 110. 3 are shown, but any number of layers can be present. Thin film metal layers 910 (e.g. copper) are formed on BT layers 110.i (i=1, 2, 3) and on the bottom side of layer 110. 1 in a conventional manner to provide signal routing paths and ground and power planes. Layers 910 are interconnected through vias in the BT layers 110.i (i.e. 110. 1, 110. 2, 110. 3) using known techniques to provide conductive paths</p>

between contact pads 350 and contact pads 360. The bottom metal layer 910 provides contact pads 360 (FIG. 3) at the bottom surface of BT substrate 110." Savastiouk '636, [0049].

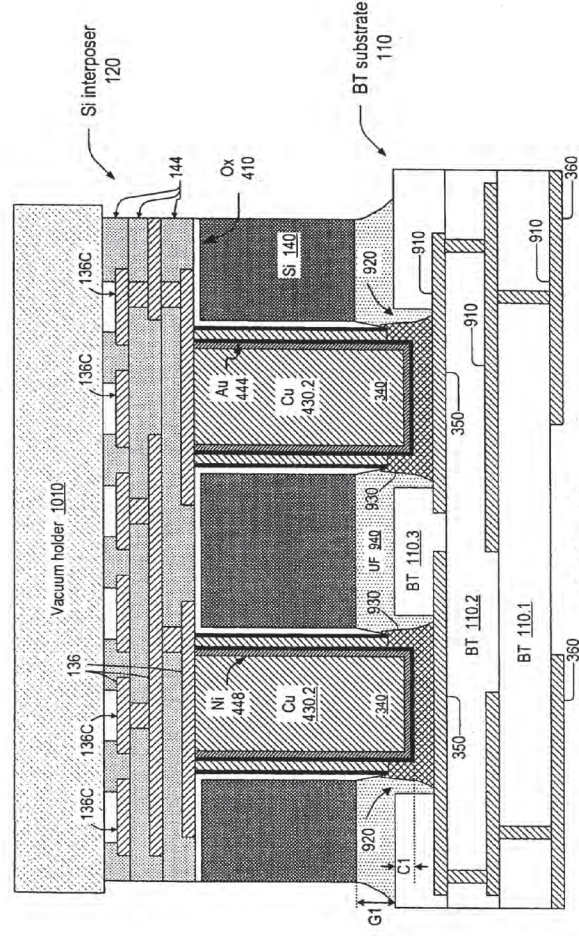
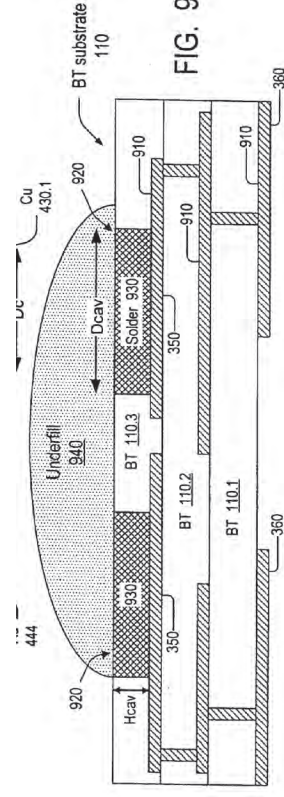


FIG. 10

Savastiouk '636, FIG. 10

“The difference between the BT substrate 110 of FIG. 9 and a conventional BT substrate is that the top contact pads 350, and the top metal layer 910, are formed below the top BT layer 110. 3. In FIG. 9, the top contact pads 350 and the top metal 910 are formed on BT layer 110. 2. Layer 110. 3 has vias 920 exposing the contact pads 350. Vias 920 form cavities in the top surface of BT substrate 110. Silicon interposer contact pads 340 will be inserted into these

cavities to form a reliable mechanical and electrical contact. In one embodiment, each cavity 920 has a diameter $D_{cav}=150\text{ }\mu\text{m}$ to accommodate a $50\text{ }\mu\text{m}$ to $60\text{ }\mu\text{m}$ diameter Dc of the contact pads 340. Dc can be calculated starting with the diameter Dv (FIG. 4) of via 330, by subtracting double the thickness of the layers 410, 420, 430, 1, 444, 448. The depth Hcav of each cavity 920 (about equal to the thickness of layer 110. 3) is $50\text{ }\mu\text{m}$ for a $50\text{ }\mu\text{m}$ height Hd of contact pads 340 (Hcav is measured to the top surface of contact pads 350).” Savastiouk ’636, [0050-0051].



Savastiouk '636, FIG. 9

“FIG. 11 illustrates another embodiment. The BT substrate 110 is similar to the BT substrate of FIGS. 9 and 10, but a metal layer 1110 is formed on the bottom and sidewalls of each cavity 920. Metal 1110 is believed to improve the strength and the electrical conductivity of the solder bond between contact pads 340 and contact pads 350. Metal layer 1110 can be copper deposited on the BT substrate and patterned by lift-off or some other process. In FIG. 11, metal 1110 extends out of cavities 920 to the top surface of the BT layer 110. 3 but does not provide any interconnects or other elements on the top surface of layer 110. 3. Metal 1110 is present only in the immediate vicinity of each cavity 920. Each contact 350 includes the

portions of metal layers 910, 1110 on the bottom and sidewalls of the corresponding cavity 920. In other embodiments, metal 1110 provides an additional level of interconnects and/or a power or ground plane on layer 110. 3." Savastiouk '636, [0061].

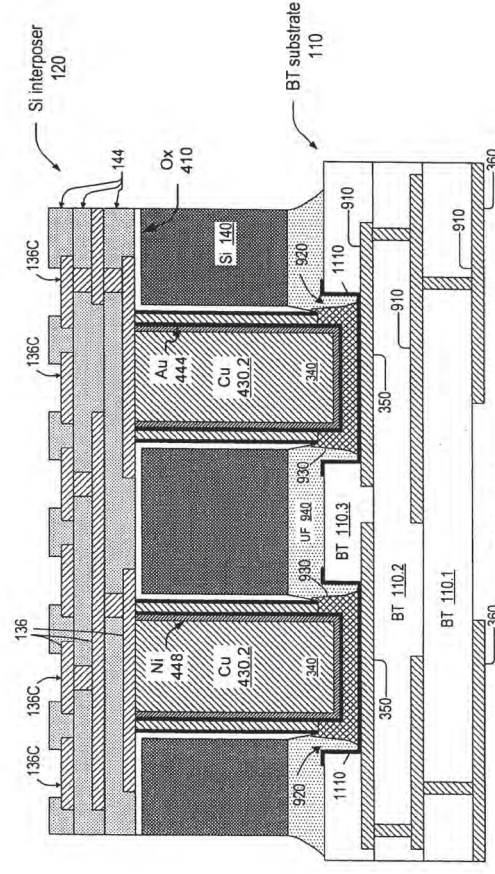


FIG. 11

Savastiouk '636, FIG. 11

“In the BT embodiment described above, the BT layers 110. 1, 110. 2, 110. 3 are laminated on top of each other. Each layer 110. 1, 110. 2 is a solid sheet placed laminated on the structure in a solid form. In some embodiments, the top layer 110. 3 is made from a material different from the material of layers 110. 1, 110. 2. For example, solder dam materials can be used, such as photoimageable polyimide, Dupont VACREL 8100, Dupont Flexible PhotolImageable Coverlay (PIC) 1000 & 2000, Shipley (Dynachem) DynaMASK 5000,

	<p>Shipley ConforMASK 2500, and possibly others. Some of the solder dam materials (e.g. polyimide) can be deposited in a liquid (possibly viscous) form and then cured. FIG. 12 is similar to FIG. 11, but solder balls 1210 have been attached to contact pads 136 C. Solder balls 1210 eliminate the need for solder balls 370 (FIG. 3) on dies 124. The packaging substrate manufacturer can provide solder balls 1210 to simplify the die 124 attachment for the substrate buyers. Solder 1210 can be attached to the interposer at any fabrication stage. In one embodiment, solder 1210 is attached to pads 136 C before the interposer wafer is thinned, i.e. before the stage of FIG. 8. The interposer wafer is mechanically stronger at this stage and its heat dissipating capability is higher, so the interposer handling is easier. Metal 1110 may be omitted (as in FIG. 10). In some embodiments, solder 1210 has a lower melting temperature than solder 930. Therefore, solder 930 is not melted during the attachment of dies 124. In the embodiment of FIG. 12, solder 1210 has the same or higher melting temperature than solder 930, but the melting temperature of solder 930 is increased during the attachment of interposer 120 to BT substrate 110. The melting temperature of solder 930 becomes higher than the melting temperature of solder 1210. The melting temperature of solder 930 is increased because the copper from layer 1110 and/or layer 350 dissolves in solder 930.” Savastiouk ’636, [0062-0066].</p> <p>“Also, in some embodiments, the cavities 920 (FIG. 9) extend through two or more BT layers, for example, through layers 110. 3 and 110. 2. Contact pads 350 can thus be formed from the metal layer 910 located between the BT layers 110. 1, 110. 2. The layer 910 on BT layer 110. 2 can be used for interconnects, power or ground planes, or other elements as discussed above.” Savastiouk ’636, [0087].</p> <p>To the extent Plaintiff contends that Savastiouk ’636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with</p>
--	--

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	(i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Savastiouk '636 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330. Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads</p>

	<p>350 to contact pads 360 at the bottom surface of substrate 110.” Savastiouk ’636, [0025-0028].</p> <p>“Metal contact pads 340 are metal protrusions formed by the metal layers 430. 2, 448, 444, 430. 1, 420 below the bottom surface of silicon 140. In some embodiments, the height Hd of metal contact pads 340 is 50 μm. A dielectric layer (not shown) can optionally be formed on the bottom surface of the interposer to cover the silicon 140 but not the metal contact pads 340. The dielectric can be formed without photolithography. See the aforementioned U.S. Pat. Nos. 6,322,903 and 6,498,381 and U.S. patent application Ser. No. 10/410,929. The interposer wafer can be diced if desired. The dicing can be performed at the same time as the interposer wafer thinning if vias were formed along the dicing lines (scribe lines) simultaneously with vias 330 at the stage of FIG. 4. See U.S. Pat. No. 6,498,074 issued Dec. 24, 2002 to Siniaguine et al., entitled “THINNING AND DICING OF SEMICONDUCTOR WAFERS...”, incorporated herein by reference. In some embodiments, the interposer wafer is not diced. ICs 124 will be attached to the wafer. In some embodiments, metal 430. 2 does not fill the through-silicon vias. Metal 430. 2 is a thin film deposited over the via sidewalls, and it can be part of a layer 136. See the aforementioned U.S. Pat. No. 6,498,381. Also, in some embodiments the contact pads 340 do not protrude out of the bottom surface of the interposer. Interposer 120 (diced or undiced) can be attached to a conventional BT substrate 110 with solder, conductive epoxy, anisotropic adhesive, thermocompression, or possibly by other techniques, known or to be invented.” Savastiouk ’636, [0043-0048].</p> <p>“Interposer wafer 120 is placed on BT substrate 110 (FIG. 10). Protruding contact pads 340 enter the cavities 920 and contact the solder 930 but do not necessarily reach the metal 910 of contact pads 350. A uniform height of contact pads 340 is not required for a good electrical contact. Underfill 940 spreads out under the interposer. In the embodiment shown, the bottom surface of silicon 140 does not reach the BT substrate. Underfill 940 helps insulate the silicon</p>
--	---

from solder 930. Therefore, it is unnecessary to form a dielectric layer on the bottom silicon surface. The interposer placement can be performed with a placement tool of type SIPLACE F4 available from Siemens corporation of Germany. The placement tool picks up the interposer from the top by a vacuum holder 1010 schematically shown in FIG. 10. The vacuum pick-up flattens the interposer if the interposer is warped. Dielectric 144 protects the interposer from being damaged by the holder. Other placement tools, with vacuum and non-vacuum holders, known or to be invented, can also possibly be used. The structure is heated to reflow the solder paste 930 and cure the underfill 940. The solder wets the bottom and side surfaces of copper contact pads 340." Savastiousk '636, [0055-0058].

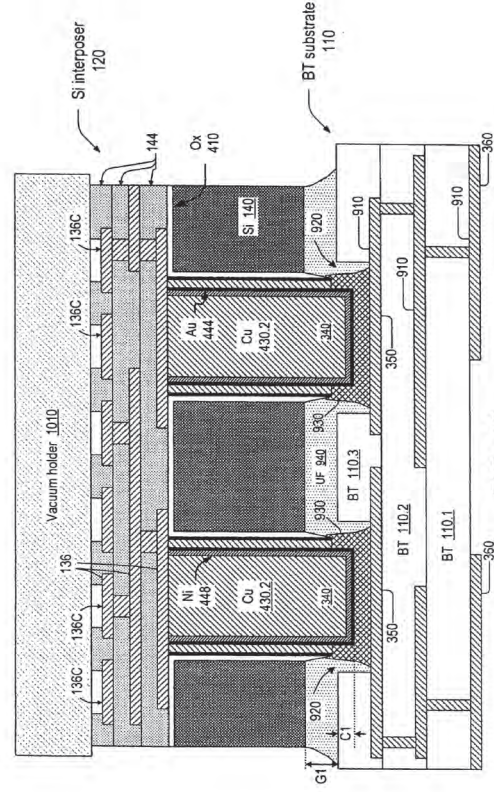


FIG. 10

Savastiouk '636, FIG. 10

	<p>“Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die’s semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1. Contact pads 340. 1 protrude out of the respective vias 330. 1. The dies 124. 1 can be manufactured using the same techniques as described above for interposer 120 (involving the wafer thinning to expose the contact pads 340. 1). Each die may have the same general structure as interposer 120 in FIG. 12. Of course, the circuitry in dies 124. 1 does not have to be identical to the interposer circuitry, and different dies 124. 1 may differ from each other. Also, contact pads 340. 1 may have smaller dimensions, and may be placed closer to each other, as they do not have to meet the BT substrate dimension requirements.” Savastiouk ’636, [0069].</p> <p>“Dies 124. 2 may be similar to dies 124. 1, but there is no solder on dies 124. 2. Dies 124. 2 include metalized vias 330. 2 in semiconductor substrates 140. 2, and contact pads 340. 2 protruding out of the vias. The active surface of dies 124. 2 is the top surface in some embodiments. The third level dies 124. 3 are like dies 124 in FIG. 3. Their active surface is the bottom surface. Solder 370 is attached to the bottom contact pads.” Savastiouk ’636, [0070-0071].</p> <p>“At step 1430, dies 124. 1 are soldered to interposer 120 with solder 1210. 0, at a temperature of about 218° C. or higher, but below 230° C. not to melt the solder 930. The copper from contact pads 340. 1 dissolves in solder 1210. 0 and increases its melting temperature to about 230° C. Solder 1210. 1 may melt, but its melting temperature does not increase because the solder 1210. 1 is not in contact with copper or other material that could increase the solder melting temperature (the top surface portions of the top contact pads of die 124. 1 are made of suitable materials to ensure that the solder melting temperature does not increase). At step</p>
--	--

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>1440, dies 124. 2 are attached to dies 124. 1 with solder 1210. 1. Solders 1210. 0 and 930 do not melt. The melting temperature of solder 1210. 1 is increased to about 230° C. due to the diffusion of copper from contact pads 340. 2.” Savastiouk '636, [0074-0076].</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Savastiouk '636 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 illustrates another package with two intermediate substrates 110, 120 between dies (ICs) 124 and PCB 130. Intermediate substrate 110 is a BT substrate, soldered to the underlying PCB 130 with solder balls 134. Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown). Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140 and separated by dielectric layers 144. Dies 124 are attached to interposer 120 with their contact pads facing up.” Savastiouk '636, [0008].</p>

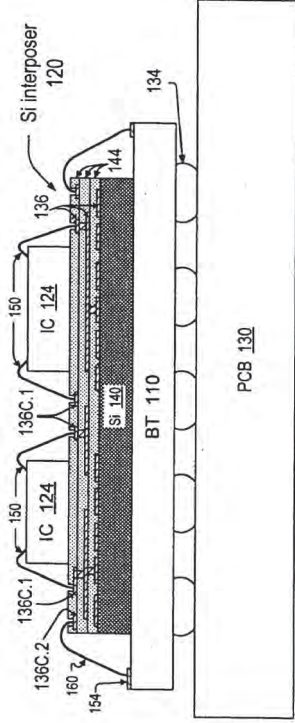
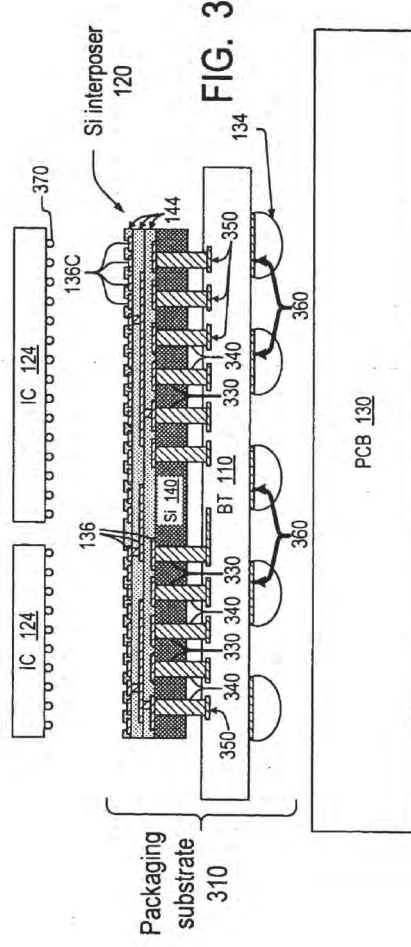


FIG. 1
PRIOR ART

Savastiouk '636, FIG. 1

“The dies’ contact pads are wire bonded to contact pads 136 C. 1 provided by metal layers 136. The wire bonding is done with bond wires 150. Contact pads 136 C. 2 on top of the interposer are wire bonded to contact pads 360 on top of BT substrate 110 using bond wires 160. Interconnect lines made from layers 136 connect the contact pads 136 C. 1 to the contact pads 136 C. 2. Metal layers 136 provide interconnects between the dies 124.” Savastiouk '636, [0008-0009].

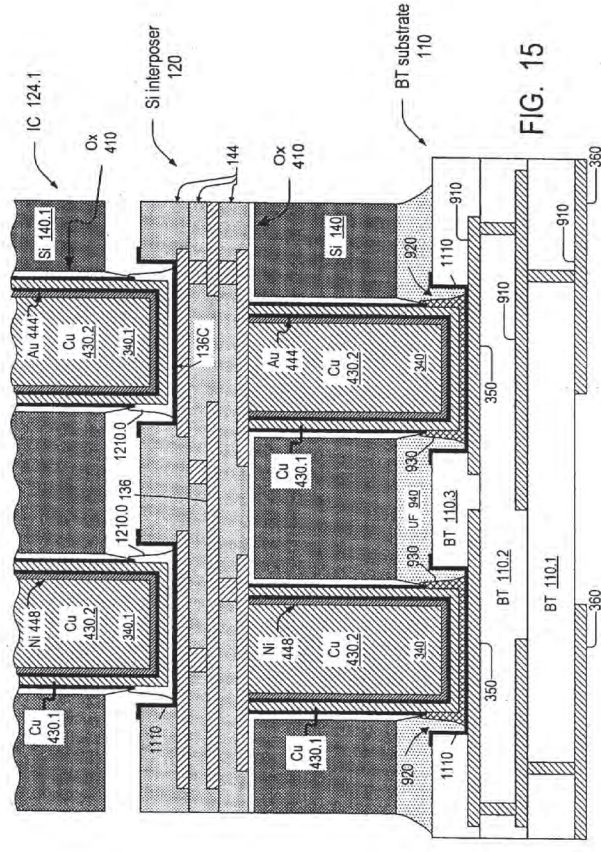
“FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later.” Savastiouk '636, [0025].



Savastiouk '636, FIG. 3

“In one embodiment, the final value of the gap GI between the silicon 140 and the BT substrate 110 is 25 μm . The gap values of 5 to 10 μm and larger are believed to be appropriate to provide sufficient electrical insulation if no dielectric is formed on the bottom surface of silicon 140. The contact 340 portion inside the vias 920 is 25 μm high (C 1 =25 μm in FIG. 10).” Savastiouk ’636, [0058].

“As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm , below the bottom surface of silicon substrate 140. 1 of die 124. 1. The contact pads are inserted into the cavities in the top surface of the interposer.” Savastiouk '636, [0080-0081].



Savastiouk '636, FIG. 15

“In some embodiments, the same dimensions are obtained as for the attachment between the BT substrate and the interposer, i.e. the final value of the gap between the silicon 140, 1 and interposer 120 is 25 μm (gap values of 5 to 10 μm and larger are believed to be appropriate to provide sufficient electrical insulation if no dielectric is formed on the bottom surface of silicon 140, 1); the contact 340, 1 portion inside the cavities in top layer 144 is 25 μm high (note dimension C 1 in FIG. 10).” Savastiouk ’636, [0083].

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Savastiouk '636 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Dies 124 are attached to interposer 120 with their contact pads facing up. The dies’ contact pads are wire bonded to contact pads 136 C. 1 provided by metal layers 136.” Savastiouk '636, [0008].</p> <p>“Intermediate substrate 120 is a silicon interposer attached to the top surface of BT substrate 110 by an adhesive (not shown). Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140 and separated by dielectric layers 144.” Savastiouk '636, [0008].</p> <p>“At step 1430, dies 124. 1 are soldered to interposer 120 with solder 1210. 0, at a temperature of about 218° C. or higher, but below 230° C.” Savastiouk '636, [0008].</p> <p>“Interposer wafer 120 is placed on BT substrate 110 (FIG. 10). Protruding contact pads 340 enter the cavities 920 and contact the solder 930 but do not necessarily reach the metal 910 of contact pads 350.” Savastiouk '636, [0055].</p>

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>“Multiple interposers can be placed on BT substrate 110, and the solder reflow and underfill curing can be performed in a single heating step for all the interposers.” Savastiouk '636, [0060].</p> <p>“In some embodiments, interposer 120 and/or dies 124. 1 are provided with deep cavities 920 at the top surface to increase the mechanical strength of the solder attachment and provide a reliable electrical contact. See FIG. 15. The attachment of dies 124. 1 to interposer 120 is performed by the same techniques as the attachment of the interposer to BT substrate 110.” Savastiouk '636, [0079-0080].</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.	<p>Savastiouk '636 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

	<p>“FIG. 12. The interposer vias are marked 330. 0 (instead of 330 as in FIG. 12), the contact pads at the bottom of the interposer are marked 340. 0, and the solder at the top is marked 1210. 0. Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die’s semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1. Contact pads 340. 1 protrude out of the respective vias 330. 1. The dies 124. 1 can be manufactured using the same techniques as described above for interposer 120 (involving the wafer thinning to expose the contact pads 340. 1). Each die may have the same general structure as interposer 120 in FIG. 12. Of course, the circuitry in dies 124. 1 does not have to be identical to the interposer circuitry, and different dies 124. 1 may differ from each other.” Savastiouk ’636, [0026-0029].</p>
--	---

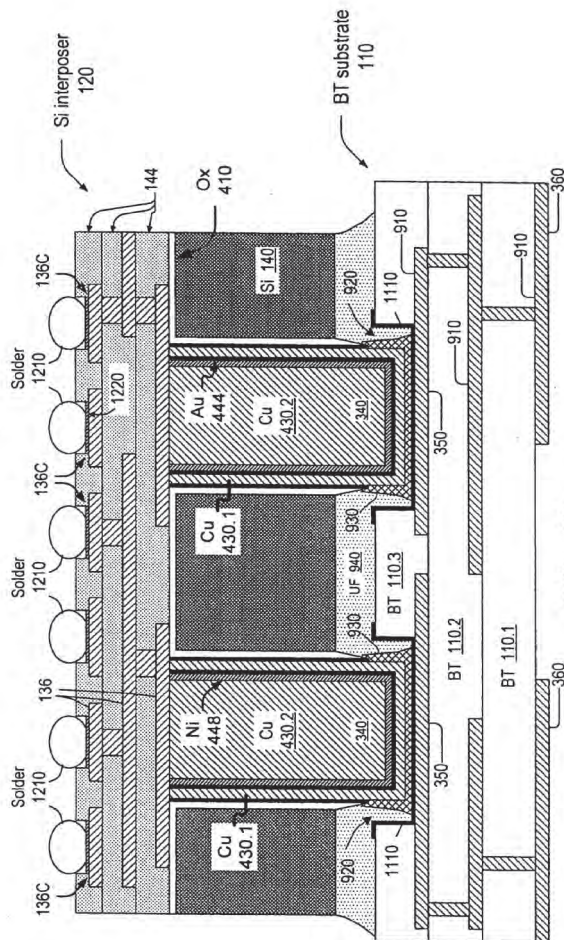


FIG. 12

Savastiouk '636, FIG. 12

“In the embodiment shown, the bottom surface of silicon 140 does not reach the BT substrate. Underfill 940 helps insulate the silicon from solder 930. Therefore, it is unnecessary to form a dielectric layer on the bottom silicon surface. The interposer placement can be performed with a placement tool of type SIPLACE F4 available from Siemens corporation of Germany. The placement tool picks up the interposer from the top by a vacuum holder 1010 schematically shown in FIG. 10. The vacuum pick-up flattens the interposer if the interposer is warped. Dielectric 144 protects the interposer from being damaged by the holder. Other placement tools, with vacuum and non-vacuum holders, known or to be invented, can also possibly be used. The structure is heated to reflow the solder paste 930 and cure the underfill

940. The solder wets the bottom and side surfaces of copper contact pads 340. In one embodiment, the final value of the gap GI between the silicon 140 and the BT substrate 110 is 25 μm .” Savastiouk '636, [0056-0058].

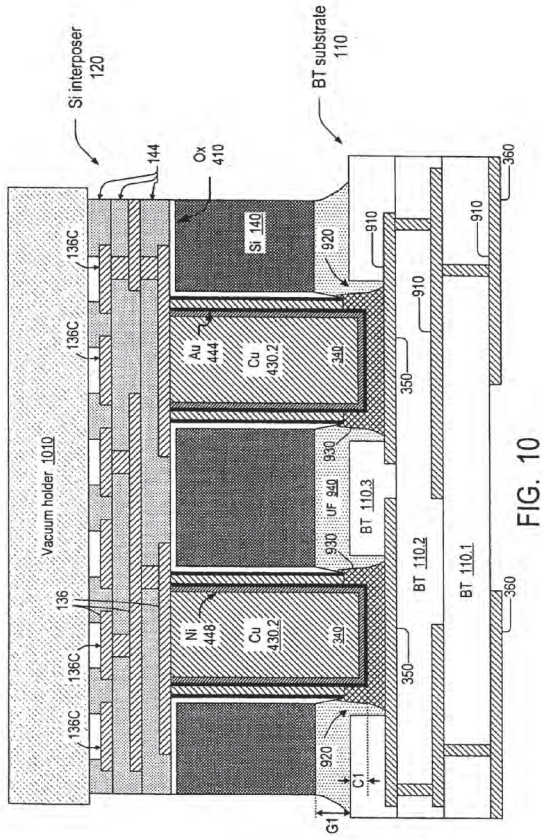


FIG. 10

Savastiouk '636, FIG. 10

“As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm , below the bottom surface of silicon substrate 140. 1 of die 124. 1. The contact pads are inserted into the cavities in the top surface of the

	<p>interposer. These cavities are the openings in top layer 144 that expose the contact pads 136 C. Metal layer 1110 (e.g. gold or nickel) can be deposited on the sidewalls and bottom of the vias in top layer 144 to improve the electrical connection and provide a barrier against copper 136 diffusion into solder 1210. 0. Alternatively, metal 1110 can be plated only on the bottom of the openings to provide a copper diffusion barrier. In some embodiments, the same dimensions are obtained as for the attachment between the BT substrate and the interposer, i.e. the final value of the gap between the silicon 140. 1 and interposer 120 is 25 μm (gap values of 5 to 10 μm and larger are believed to be appropriate to provide sufficient electrical insulation if no dielectric is formed on the bottom surface of silicon 140. 1); the contact 340. 1 portion inside the cavities in top layer 144 is 25 μm high (note dimension C 1 in FIG. 10).” Savastiouk '636, [0081-0083].</p>
--	--

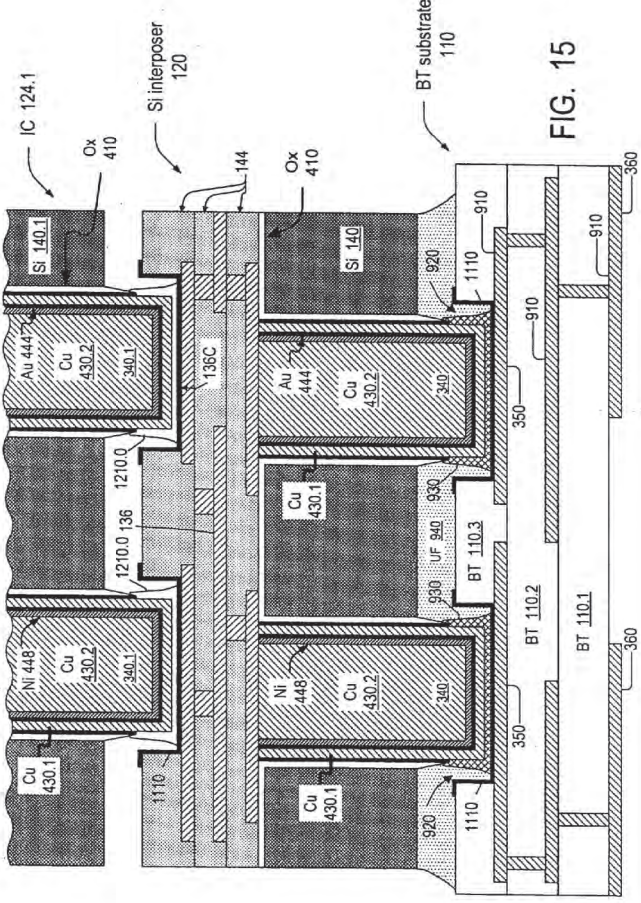


FIG. 15

Savastiouk '636, FIG. 15

To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, e.g.:</p>	<p>Savastiouk '636 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, e.g.:</p> <p>Savastiouk '636, FIG. 3</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>

Claim 4, U.S. Patent No. 9859202

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Savastiouk '636 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330. Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads 350 to contact pads 360 at the bottom surface of substrate 110.” Savastiouk '636, [0026-0028].</p> <p>“Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die’s semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1. Contact pads 340. 1 protrude out of the respective vias 330. 1.” Savastiouk '636, [0026-0027].</p>

Appendix A-29 - Invalidity of U.S. Patent No. 9859202 in view of Savastiouk '636 - U.S. Patent Publication No. 20050189636

	<p>“Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm, below the bottom surface of silicon substrate 140. 1 of die 124. 1. The contact pads are inserted into the cavities in the top surface of the interposer.” Savastiouk '636, [0027-0028].</p> <p>“Protruding contact pads 340 enter the cavities 920 and contact the solder 930 but do not necessarily reach the metal 910 of contact pads 350.” Savastiouk '636, [0055].</p> <p>“At step 1430, dies 124. 1 are soldered to interposer 120 with solder 1210. 0, at a temperature of about 218° C. or higher, but below 230° C. not to melt the solder 930. The copper from contact pads 340. 1 dissolves in solder 1210. 0 and increases its melting temperature to about 230° C.” Savastiouk '636, [0073-0074].</p> <p>“The contact pads are inserted into the cavities in the top surface of the interposer. These cavities are the openings in top layer 144 that expose the contact pads 136 C. Metal layer 1110 (e.g. gold or nickel) can be deposited on the sidewalls and bottom of the vias in top layer 144 to improve the electrical connection and provide a barrier against copper 136 diffusion into solder 1210. 0.” Savastiouk '636, [0081-0082].</p> <p>To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

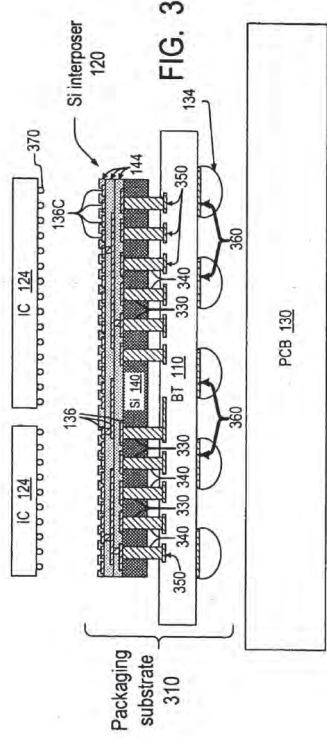
Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
-------------------------	-------------------

[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Savastiouk '636 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

See, e.g.:

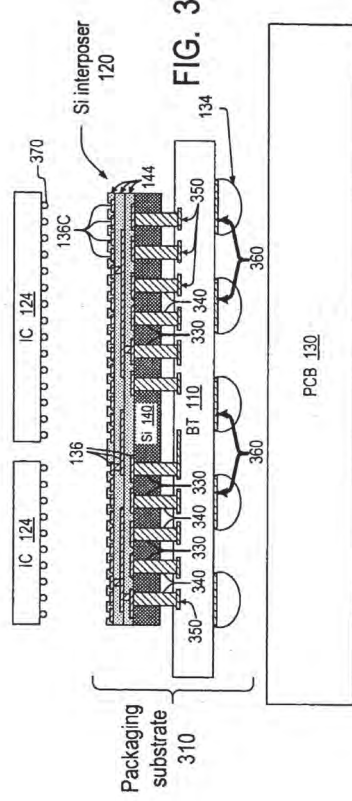


Savastiouk '636, FIG. 3

To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the corresponding top metal pads of the spacer connector.</p>	<p>Savastiouk '636 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p>See, e.g.:</p> <p>“FIG. 3 illustrates an integrated circuit packaging substrate 310 having two intermediate integrated circuit packaging substrates 110, 120. Substrate 120 is a silicon interposer attached to BT substrate 110. Dies 124 and PCB 130 will be attached later. Silicon interposer 120 includes metal layers 136 formed over silicon substrate 140. Substrate 140 has substantially planar top and bottom surfaces, and is quite thin. In some embodiments, the planarity of substrate 140 is suitable for fine geometry photolithography (finer than possible with BT and FR4 substrates). The thickness of substrate 140 can be 100 μm or less (50 μm to 35 μm thickness values believed to be achievable, and smaller values may be possible). Layers 136 provide interconnect lines and may also provide power and ground planes, resistors, inductors, capacitor plates for decoupling capacitors and other capacitor types, and possibly other elements, known or to be invented. Layers 136 can be separated from each other, and from the substrate, by dielectric layers 144. Layers 136 contact each other and the silicon substrate through openings in the dielectric layers. Layers 136 can also be formed directly on the silicon substrate if desired. Layers 136 provide contact pads 136 C at the top surface of</p>

the interposer. The contact pads are available for flip-chip attachment to dies 124. Silicon substrate 140 includes metalized through-silicon vias 330 that pass between the top and bottom surfaces of substrate 140. Conductive paths are provided from contact pads 136 C at the top of the interposer to contact pads 340 at the bottom of the interposer through the vias 330.” Savastiouk '636, [0025-0027].



Savastiouk '636, FIG. 3

“Contact pads 340 are attached to contact pads 350 at the top surface of BT substrate 110. Interconnects (not shown) in BT substrate 110 connect the contact pads 350 to contact pads 360 at the bottom surface of substrate 110. Solder balls 134 are formed on pads 360 by conventional techniques for attachment to PCB 130. The size and spacing (pitch) of contact pads 136 C on interposer 120 matches the size and the pitch of the contact pads on dies 124. If dies 124 are silicon integrated circuits, their CTE matches the CTE of the interposer, so the pitch of contact pads 136 C can be small because the low thermal stresses at the interface

	<p>between the dies and the interposer make it unnecessary to use large solder balls 370. The contact pads 340 on the bottom of the interposer match the top contact pads 350 of BT substrate 110.” Savastiouk ’636, [0027-0029].</p> <p>“To facilitate the interposer handling, the metal contact pads 340 are formed to protrude out of vias 330. The protruding contact pads 340 are inserted into cavities in BT substrate 110, as explained in more detail below. The invention is not limited to the protruding contact pads or the cavities however.” Savastiouk ’636, [0030].</p> <p>“FIG. 12 is similar to FIG. 11, but solder balls 1210 have been attached to contact pads 136 C. Solder balls 1210 eliminate the need for solder balls 370 (FIG. 3) on dies 124. The packaging substrate manufacturer can provide solder balls 1210 to simplify the die 124 attachment for the substrate buyers. Solder 1210 can be attached to the interposer at any fabrication stage. In one embodiment, solder 1210 is attached to pads 136 C before the interposer wafer is thinned, i.e. before the stage of FIG. 8.” Savastiouk ’636, [0062-0063].</p>
--	---

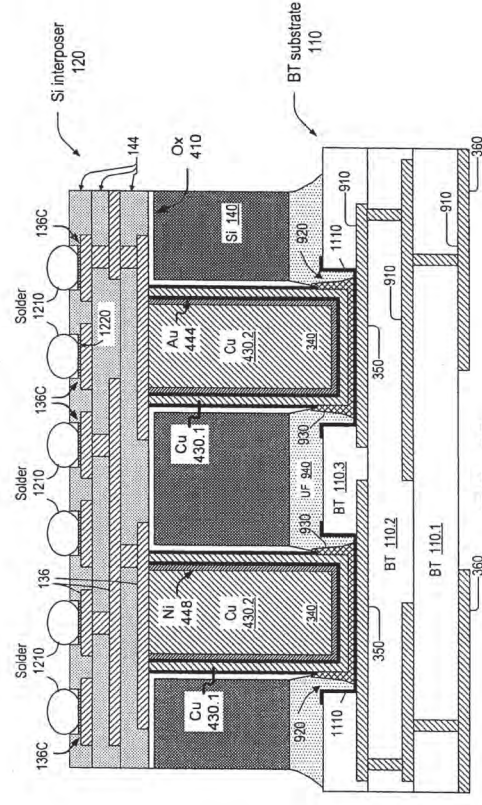


FIG. 12

Savastiouk '636, FIG. 12

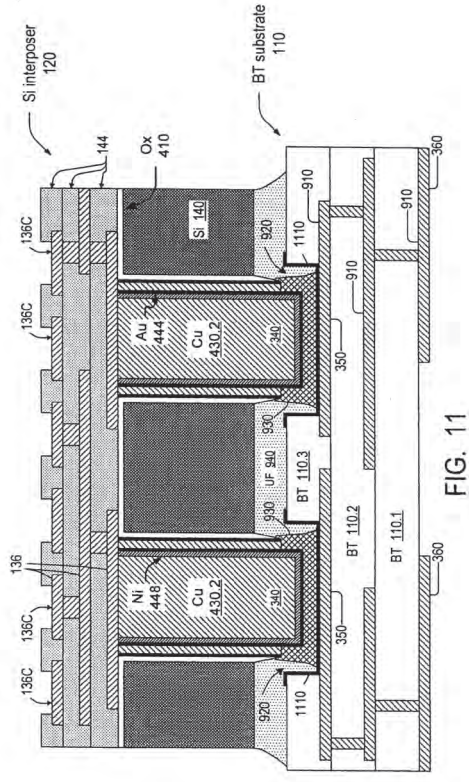


FIG. 11

Savastiouk '636, FIG. 11

“FIGS. 13-14 illustrate a possible manufacturing sequence with multiple die levels 124. 1, 124. 2, 124. 3 attached to the packaging substrate. The packaging substrate is manufactured as in FIG. 12. The interposer vias are marked 330. 0 (instead of 330 as in FIG. 12), the contact pads at the bottom of the interposer are marked 340. 0, and the solder at the top is marked 1210. 0. Each die 124. 1 has one or more metalized through vias 330. 1 formed in the die’s semiconductor substrate 140. 1 (e.g. monocrystalline silicon). Each via 330. 1 passes between the top and bottom surfaces of substrate 140. 1. Conductive paths are provided from contact pads at the top of the die 124. 1 to contact pads 340. 1 at the bottom of the die through the vias 330. 1. Contact pads 340. 1 protrude out of the respective vias 330. 1.” Savastiouk '636, [0067-0069].

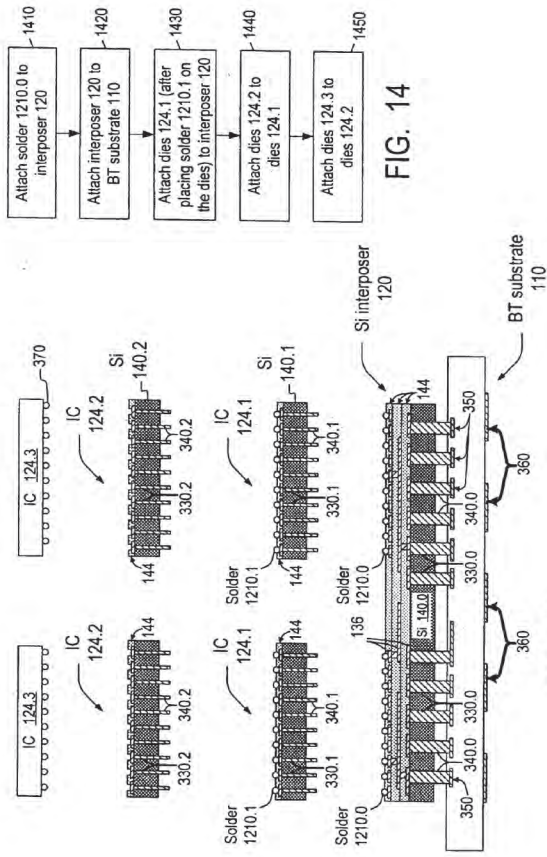
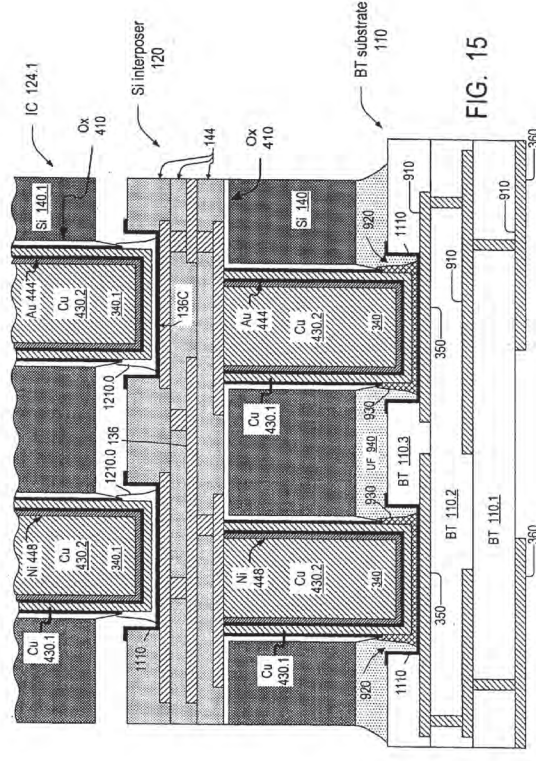


FIG. 13

Savastiouk '636, FIG. 13

“The attachment of dies 124. 1 to interposer 120 is performed by the same techniques as the attachment of the interposer to BT substrate 110. The attachment of dies 124. 2 to dies 124. 1 can also be performed in this way. As shown in FIG. 15, the top dielectric layer 144 in interposer 120 is a thick layer, e.g. 50 μm thick. This can be a photoimageable material such as described above for BT layer 110. 3. Openings in top layer 144 expose contact pads 136 C. Contact pads 340. 1 on die 124. 1 protrude by some distance, e.g. 50 μm, below the bottom surface of silicon substrate 140. 1 of die 124. 1.” Savastiouk '636, [0080-0081].



Savastiouk '636, FIG. 15

To the extent Plaintiff contends that Savastiouk '636 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

U.S. Patent No.9685414 (“Shuto”) is titled Package Assembly for Embedded Die and Associated Techniques and Configurations and lists Takashi Shuto as inventor. Shuto is assigned to Intel Corporation. Shuto anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Shuto is a U.S. patent that was filed June 26, 2013 and published January 1, 2015. Shuto is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Shuto, or otherwise rendered obvious by disclosures and teachings of Shuto, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Shuto does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Shuto with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Shuto, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

Where the chart below states that Shuto “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Shuto or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Shuto set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Shuto discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

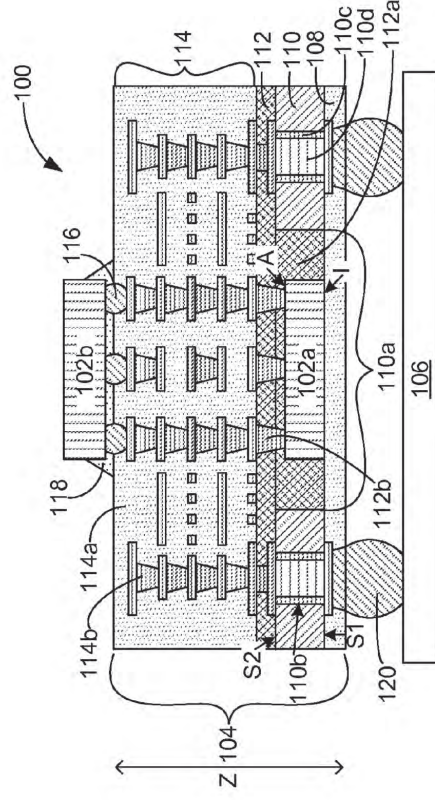


FIG. 1

Shuto, FIG. 1

“FIG. 3 schematically illustrates a cross-section side view of another example IC package assembly (hereinafter “package assembly 300”), in accordance with some embodiments. The package assembly 300 may comport with embodiments described in connection with package assembly 100 or 200, except that the reinforced plate 110 of the package assembly 300 of FIG. 3 includes an electrically conductive core 110 f such as a metal (e.g., aluminum or copper) and an electrically insulative layer 110 g disposed on the core 110 f to provide a barrier between material of the core 110 f and interconnects (e.g., PTHs 110 b) that are disposed in the reinforced plate 110 to prevent shorts and/or leakage.” Shuto, [8:35-8:46].

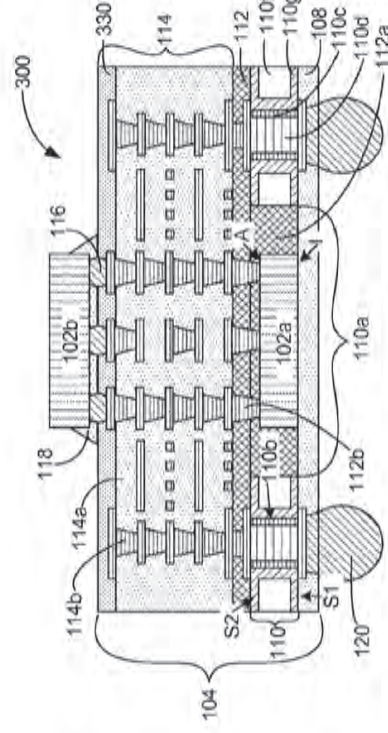


FIG. 3

Shuto, FIG. 3

“FIG. 4 schematically illustrates a cross-section side view of yet another example IC package assembly (hereinafter “package assembly 400”), in accordance with some embodiments. In some embodiments, the die 102 b may be coupled with an inactive side I of the die 102 a, as can be seen. In the depicted embodiment, the die 102 b is coupled with the die 102 a using solderable material 116 (e.g., or other suitable FLIs) that extends through the die attach layer 108.” Shuto, [8:58-8:65].

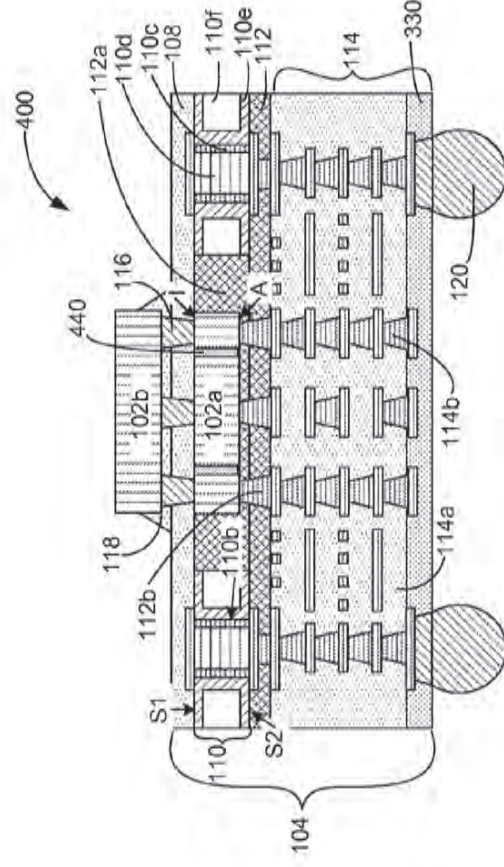
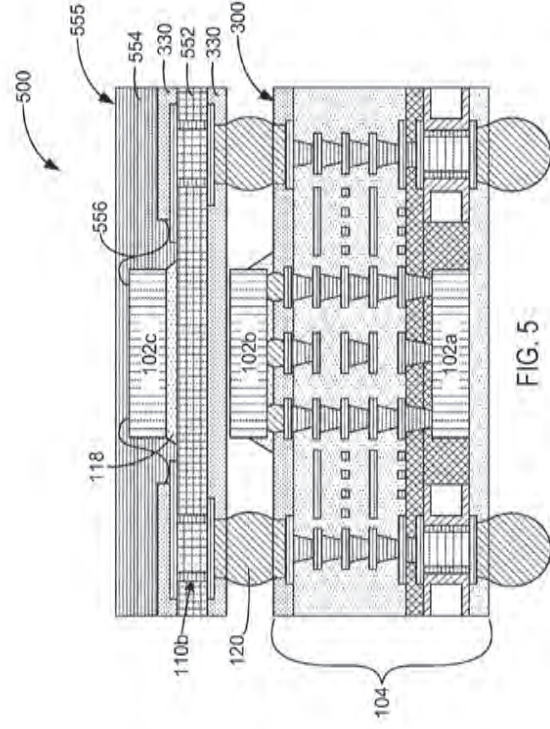


FIG. 4

Shuto, FIG. 4

“FIG. 5 schematically illustrates a cross-section side view of still yet another example IC package assembly (hereinafter “package assembly 500”), in accordance with some embodiments. The package assembly 500 depicts an example PoP configuration. In the package assembly 500, a package substrate 555 including a die 102 c is coupled with the package substrate 104 of package assembly 300 using package-level interconnects such as, for example, solder balls 120.” Shuto, [9:6-9:14].



Shuto, FIG. 5

“FIG. 6 schematically illustrates a cross-section side view of still yet another example IC package assembly (hereinafter “package assembly 600”), in accordance with some embodiments. The package assembly 600 depicts another PoP assembly. In the package assembly 600, a package substrate 555 including a die 102 c is coupled with the package substrate 104 of package assembly 400 using package-level interconnects such as, for example, solder balls 120.” Shuto, [9:45-9:53].

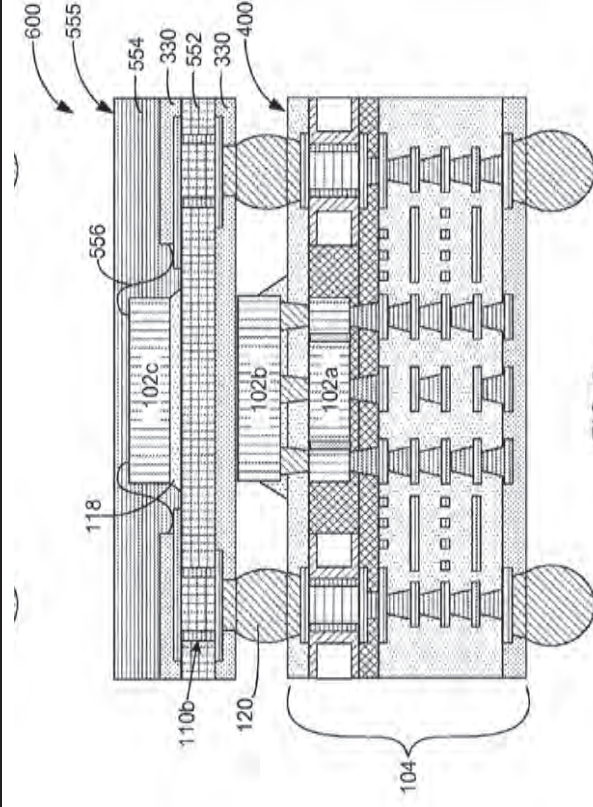


FIG. 6

Shuto, FIG. 6

“According to various embodiments, the present disclosure describes an apparatus (e.g., package assembly) comprising a die attach layer, a die coupled with the die attach layer, the die having an active side including active devices of the die and an inactive side disposed opposite to the active side, a reinforced plate coupled with the die attach layer, the reinforced plate having a first side and a second side disposed opposite to the first side and a cavity disposed in the reinforced plate and one or more build-up layers coupled with the second side of the reinforced plate, the one or more build-up layers including an insulator and conductive features disposed in the insulator, the conductive features being electrically coupled with the die, wherein the inactive side of the die is in direct contact with the die attach layer, the first

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	side of the reinforced plate is in direct contact with the die attach layer and the die is disposed in the cavity.” Shuto, [12:46-12:61].
[1.A] a bottom package substrate;	<p>Shuto discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

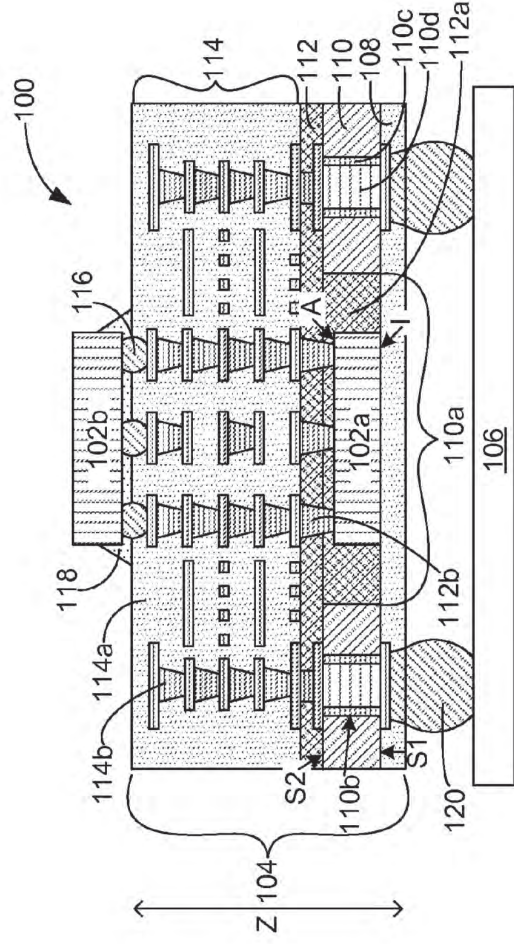


FIG. 1

Shuto, FIG. 1

“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments. In other embodiments, additional build-up layers (not shown) may be formed on the die attach layer 108 to provide additional electrical routing for the package substrate 104 and the package-level interconnects may be coupled with the additional build-up layers.” Shuto, [6:25-6:40].</p> <p>“The package assembly 100 may further include a circuit board 106 coupled with the package substrate 104 through the package-level interconnects (e.g., solder balls 120). Only a small portion of the circuit board 106 may be depicted for the sake of discussion. The package-level interconnects may be coupled with contacts (e.g., pads) of the circuit board 106 to route electrical signals of the dies 102 a, 102 b between the package substrate 104 and the circuit board 106. The circuit board 106 may be a printed circuit board (PCB) composed of an electrically insulative material such as, for example, an epoxy laminate. For example, the circuit board 106 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Electrical routing structures (not shown) such as traces, trenches, vias, and the like may be</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>formed through the electrically insulating layers to route the electrical signals of the dies 102 a, 102 b through the circuit board 106. The circuit board 106 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 106 is a motherboard (e.g., motherboard 802 of FIG. 8).” Shuto, [6:41-6:64].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Shuto discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

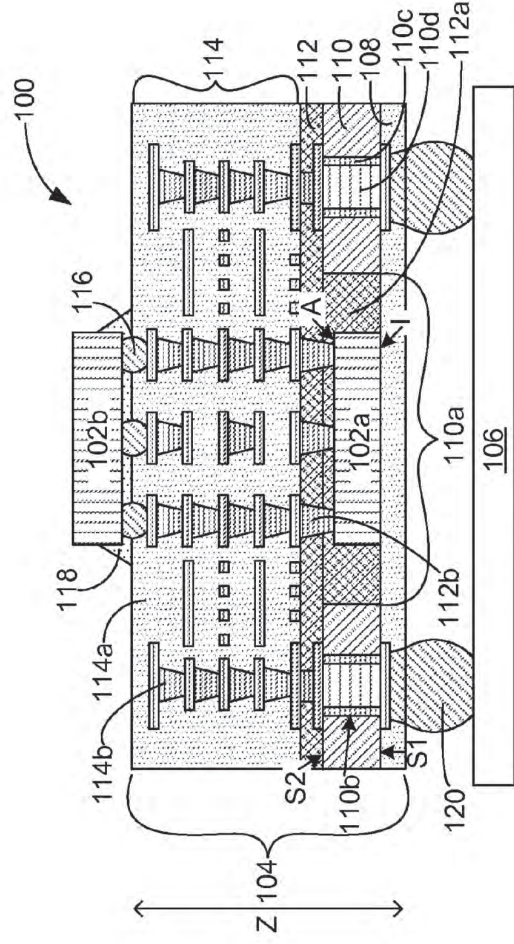


FIG. 1

Shuto, FIG. 1

“The package substrate 104 may include a die attach layer 108, which may be used as a substrate for attachment of the die 102 a. That is, in some embodiments, the die 102 a may be coupled in direct contact with the die attach layer 108. In some embodiments, the die attach layer 108 may be composed of an electrically insulative material such as, for example, an epoxy resin. In some embodiments, the die attach layer 108 may be composed of a same material as an insulator 114 a of the build-up layers 114. The die attach layer 108 may be composed of other suitable materials in other embodiments.” Shuto, [3:26-3:36].

	<p>“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the prepreg material of the laminate layer 112 and die encapsulant material 112 a may include an epoxy resin with glass cloth. The prepreg material may further strengthen and/or reinforce the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114. The material of the laminate layer 112 and die encapsulant material 112 a may include other suitable materials in other embodiments. One or more interconnects may be formed in the laminate layer 112 to electrically couple the die 102 a with conductive features 114 b (e.g., electrical routing features) of the build-up layers 114. For example, in some embodiments, the interconnects may include via structures 112 b that extend through the laminate layer 112 and die encapsulant material 112 a to corresponding contacts such as pads on the die 102 a. The via structures 112 b may be formed using any suitable process including, for example, a laser process to remove material of the laminate layer 112 and die encapsulant material 112 a to</p>
--	--

	<p>provide a laser via joint between the die 102 a and the build-up layers 114. The laser via joint may have a structure consistent with being formed by a laser process. For example, a profile of the laser via joint may taper as can be seen. The interconnects of the laminate layer 112 may include other suitable interconnect structures in other embodiments.” Shuto, [4:63-5:21].</p> <p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Shuto discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can</p>

be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].

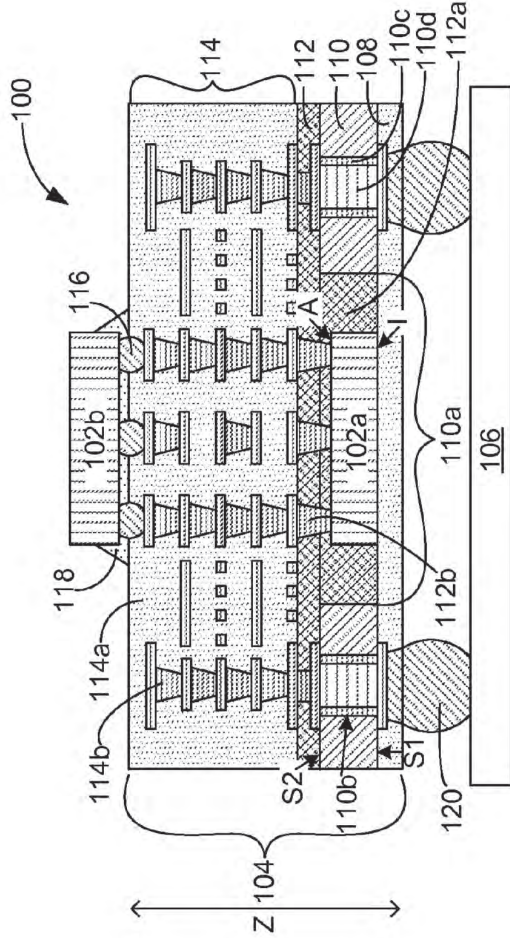


FIG. 1

Shuto, FIG. 1

“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the

	<p>package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].</p> <p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias,</p>
--	---

	<p>traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p>
--	--

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Shuto discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

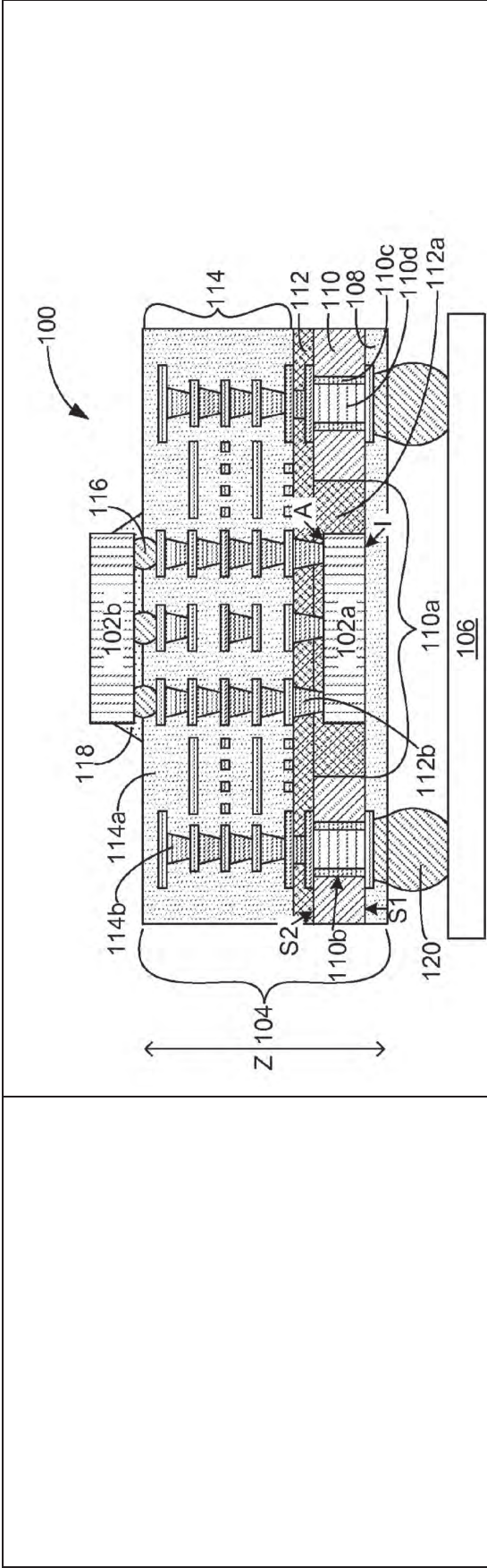


FIG. 1

Shuto, FIG. 1

“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed

	<p>opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].</p> <p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to</p>
--	--

	<p>fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments. In other embodiments, additional build-up layers (not shown) may be formed on the die attach layer 108 to provide additional electrical routing for the package substrate 104 and the package-level interconnects may be coupled with the additional build-up layers.” Shuto, [6:25-6:40].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Shuto discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

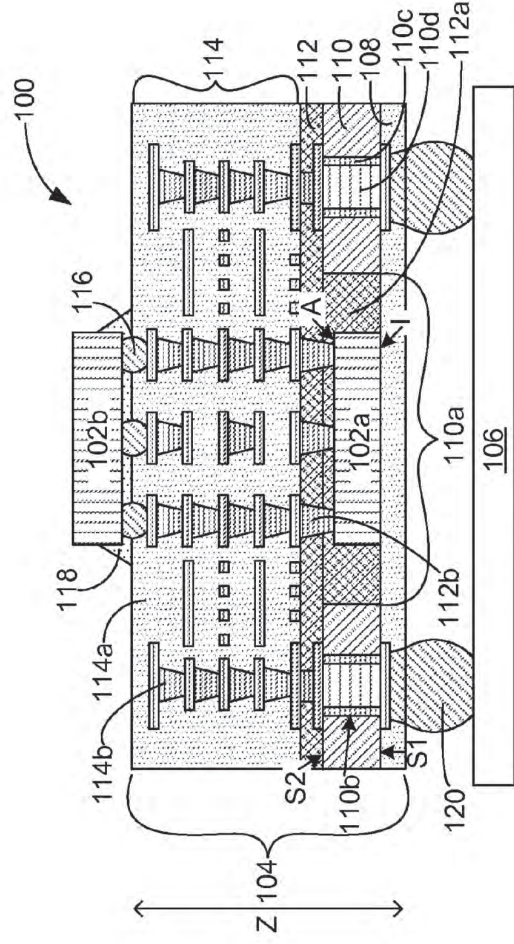


FIG. 1

Shuto, FIG. 1

“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed

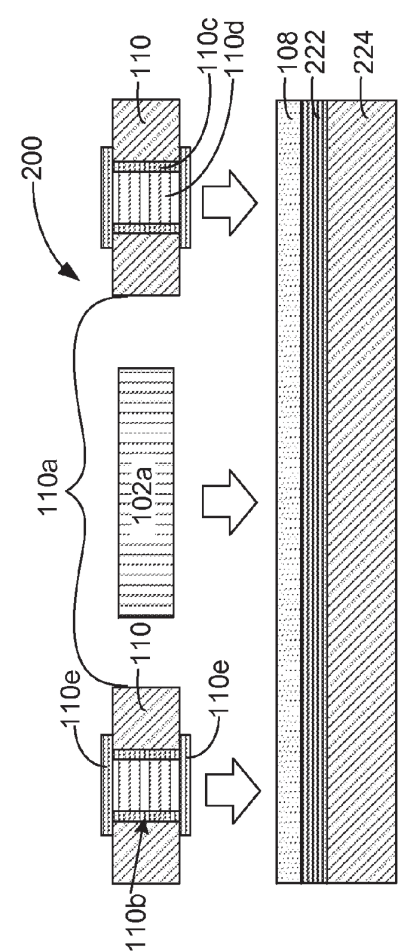
	<p>opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].</p> <p>“In some embodiments, the reinforced plate 110 may include one or more interconnects configured to electrically couple the first side S1 and the second side S2 of the reinforced plate 110 such as, for example, plated through holes (PTHs) 110 b. The PTHs 110 b may be configured to route electrical signals of the die 102 a (and/or possibly other dies such as die 102 b). In some embodiments, the PTHs 110 b may include a plated opening 110 c composed of an electrically conductive material such as a metal (e.g., copper) filled with a plugging material 110 d such as, for example, epoxy resin. The reinforced plate 110 may include other suitable interconnect structures formed through the reinforced plate 110 to route the electrical signals in other embodiments.” Shuto, [4:34-4:47].</p>
--	--

	<p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some</p>
--	---

	<p>embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments. In other embodiments, additional build-up layers (not shown) may be formed on the die attach layer 108 to provide additional electrical routing for the package substrate 104 and the package-level interconnects may be coupled with the additional build-up layers.” Shuto, [6:25-6:40].</p> <p>“A die 102 a and reinforced plate 110 may be placed on the die attach layer 108 as indicated by the downward arrows. Prior to placement on the die attach layer 108, the reinforced plate 110 may be fabricated to include one or more PTHs 110 b having a cavity 110 a and traces 110 e formed on both sides of plated openings 110 c that may be filled with a plugging material 110 d.” Shuto, [7:21-7:27].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Shuto discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin.” Shuto, [5:45-5:49].</p> <p>“In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114.” Shuto, [5:56-5:62].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments.” Shuto, [6:25-6:35].</p>

	<p>“Prior to placement on the die attach layer 108, the reinforced plate 110 may be fabricated to include one or more PTHs 110 b having a cavity 110 a and traces 110 e formed on both sides of plated openings 110 c that may be filled with a plugging material 110 d.” Shuto, [7:23-7:27].</p>  <p>FIG. 2a</p> <p>Shuto, FIG. 2a</p> <p>“FIG. 2f depicts the package assembly 200 subsequent to forming openings 114 c to expose conductive features 114 b of the build-up layers 114 and forming openings 108 a to expose interconnects (e.g., PTHs 110 b) of the reinforced plate 110. The openings 114 c and 108 a may be formed using any suitable technique including, for example, a laser process to drill away material of the insulator 114 a and/or die attach layer 108. A desmesar process may be used to clean surfaces within the openings 114 c and/or 108 a and a surface finish may be</p>
--	---

deposited on electrically conductive surfaces in the openings 114 c and/or 108 a to facilitate formation of joints with the electrically conductive surfaces.” Shuto, [8:9-8:20].

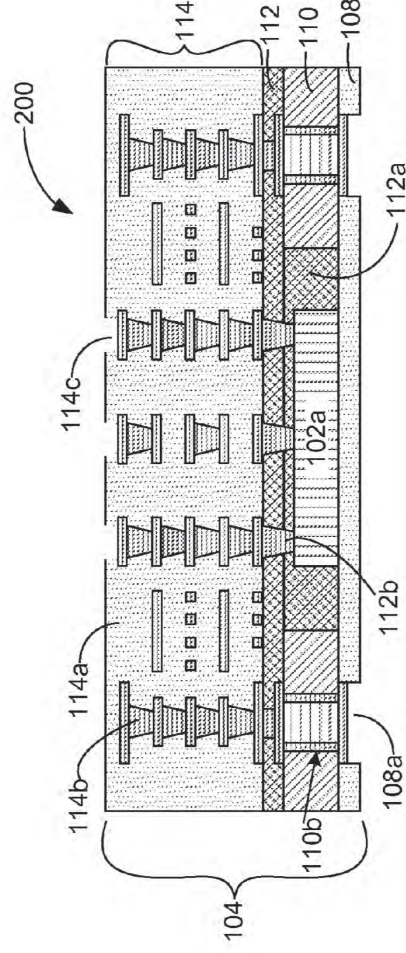
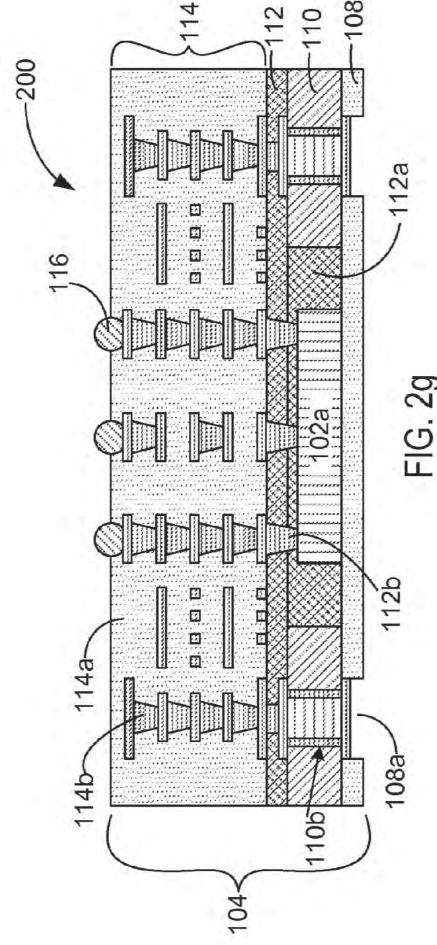


FIG. 2f

Shuto, FIG. 2f

“FIG. 2g depicts the package assembly 200 subsequent to depositing solderable material 116 into the openings 114 c using any suitable technique. The solderable material 116 may include, for example, solder bumps for die attachment.” Shuto, [8:21-8:24]



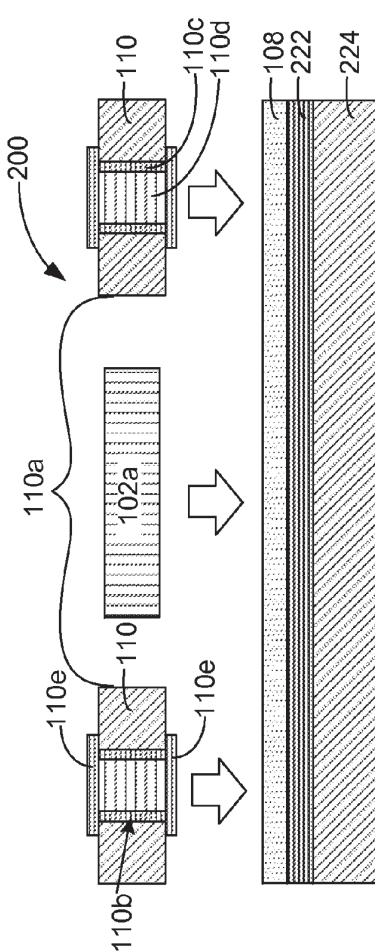
Shuto, FIG. 2g

To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Shuto discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.

See, e.g.:

“Prior to placement on the die attach layer 108, the reinforced plate 110 may be fabricated to include one or more PTHs 110 b having a cavity 110 a and traces 110 e formed on both sides

	<p>of plated openings 110 c that may be filled with a plugging material 110 d.” Shuto, [7:23-7:27].</p>  <p>FIG. 2a</p> <p>Shuto, FIG. 2a</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the</p>	<p>Shuto discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

plurality of metal pillars of the spacer connector,	<p><i>See, e.g.:</i></p> <p>“The package substrate 104 may include a die attach layer 108, which may be used as a substrate for attachment of the die 102 a. That is, in some embodiments, the die 102 a may be coupled in direct contact with the die attach layer 108. In some embodiments, the die attach layer 108 may be composed of an electrically insulative material such as, for example, an epoxy resin. In some embodiments, the die attach layer 108 may be composed of a same material as an insulator 114 a of the build-up layers 114. The die attach layer 108 may be composed of other suitable materials in other embodiments.” Shuto, [3:26-3:36].</p> <p>“The package assembly 100 may include a die 102 a coupled with the die attach layer 108 and embedded in the package substrate 104. The die 102 a may have an active side, A, including active devices such as, for example, one or more transistor devices and an inactive side, I, disposed opposite to the active side A. In some embodiments, the inactive side I of the die 102 a may be in direct contact with the die attach layer 108. The die 102 a may be a discrete unit of an IC product made from a semiconductor material using semiconductor fabrication techniques such as thin film deposition, lithography, etching and the like. In some embodiments, the die may be, include, or be a part of a processor, memory, system on chip (SoC) or ASIC in some embodiments. In one embodiment, the die 102 a is a processor such as, for example, a central processing unit (CPU). The die 102 a may be configured to serve other functions in other embodiments.” Shuto, [3:37-3:53].</p> <p>“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-</p>
---	--

	<p>up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].</p> <p>“In some embodiments, the prepreg material of the laminate layer 112 and die encapsulant material 112 a may include an epoxy resin with glass cloth. The prepreg material may further strengthen and/or reinforce the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114. The material of the laminate layer 112 and die encapsulant material 112 a may include other suitable materials in other embodiments. One or more interconnects may be formed in the laminate layer 112 to electrically couple the die 102 a with conductive features 114 b (e.g., electrical routing</p>
--	---

	<p>features) of the build-up layers 114. For example, in some embodiments, the interconnects may include via structures 112 b that extend through the laminate layer 112 and die encapsulant material 112 a to corresponding contacts such as pads on the die 102 a. The via structures 112 b may be formed using any suitable process including, for example, a laser process to remove material of the laminate layer 112 and die encapsulant material 112 a to provide a laser via joint between the die 102 a and the build-up layers 114. The laser via joint may have a structure consistent with being formed by a laser process. For example, a profile of the laser via joint may taper as can be seen. The interconnects of the laminate layer 112 may include other suitable interconnect structures in other embodiments.” Shuto, [4:63-5:21].</p> <p>“For example, in some embodiments, the interconnects may include via structures 112 b that extend through the laminate layer 112 and die encapsulant material 112 a to corresponding contacts such as pads on the die 102 a. The via structures 112 b may be formed using any suitable process including, for example, a laser process to remove material of the laminate layer 112 and die encapsulant material 112 a to provide a laser via joint between the die 102 a and the build-up layers 114. The laser via joint may have a structure consistent with being formed by a laser process. For example, a profile of the laser via joint may taper as can be seen. The interconnects of the laminate layer 112 may include other suitable interconnect structures in other embodiments.” Shuto, [5:7-5:21].</p>
--	---

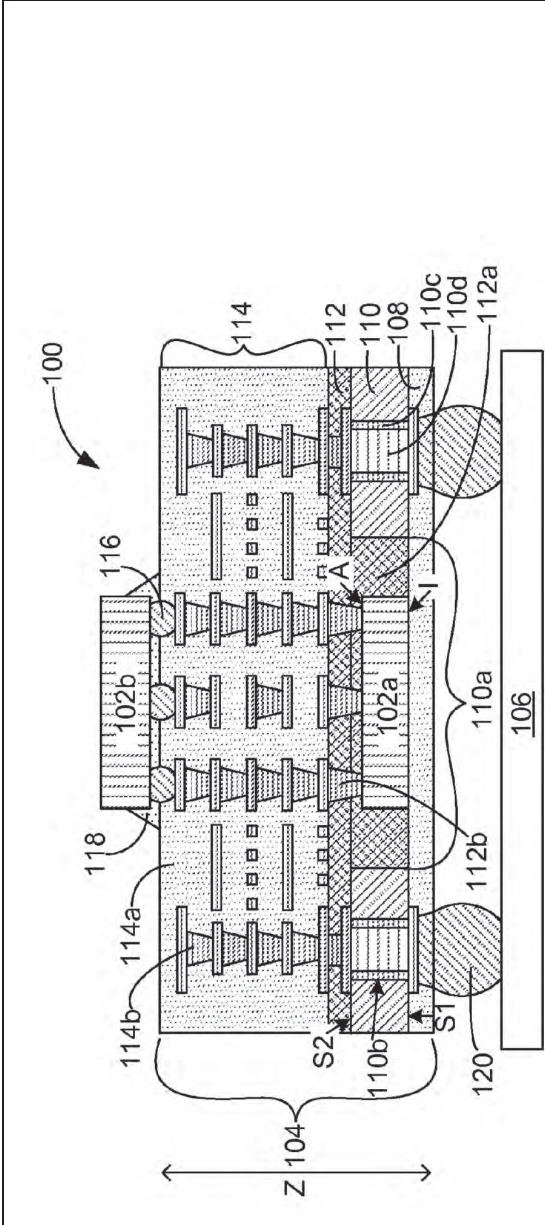


FIG. 1

Shuto, FIG. 1

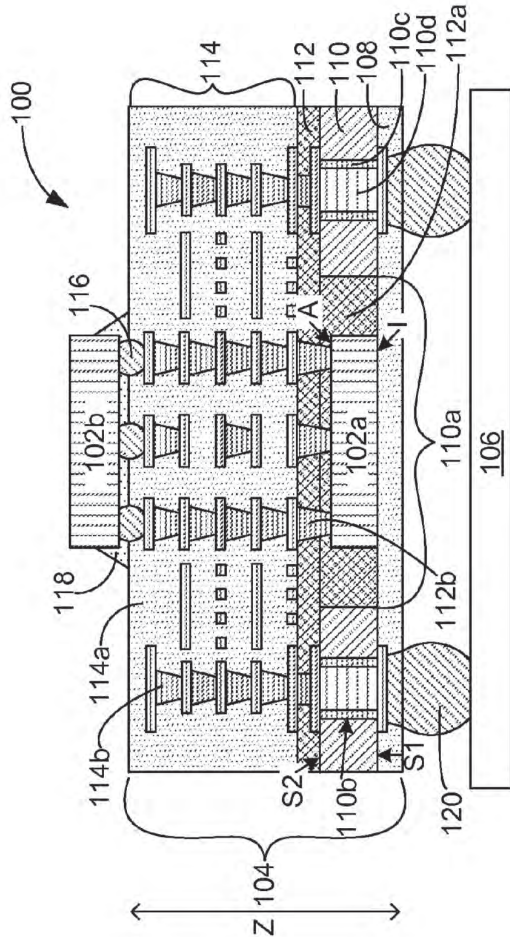
“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable

	<p>materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments.” Shuto, [6:25-6:30].</p> <p>“The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments.” Shuto, [6:33-6:35].</p> <p>“FIG. 2g depicts the package assembly 200 subsequent to depositing solderable material 116 into the openings 114 c using any suitable technique. The solderable material 116 may include, for example, solder bumps for die attachment.” Shuto, [8:21-8:24].</p>
--	--

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>“In the package assembly 600, a package substrate 555 including a die 102 c is coupled with the package substrate 104 of package assembly 400 using package-level interconnects such as, for example, solder balls 120.” Shuto, [9:49-9:53].</p> <p>“At 716, the method 700 may include electrically coupling a second package substrate (e.g., package substrate 555 of FIGS. 5-6) including a third die (e.g., die 102 c of FIGS. 5-6) with the first package substrate (e.g., package substrate 104 of FIGS. 5-6). The second package substrate may be coupled with either one of two opposing sides of the first package substrate as depicted, for example, in connection with FIGS. 5-6 using package-level interconnects such as solder balls 120.” Shuto, [10:41-10:49].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Shuto discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some</p>

embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].



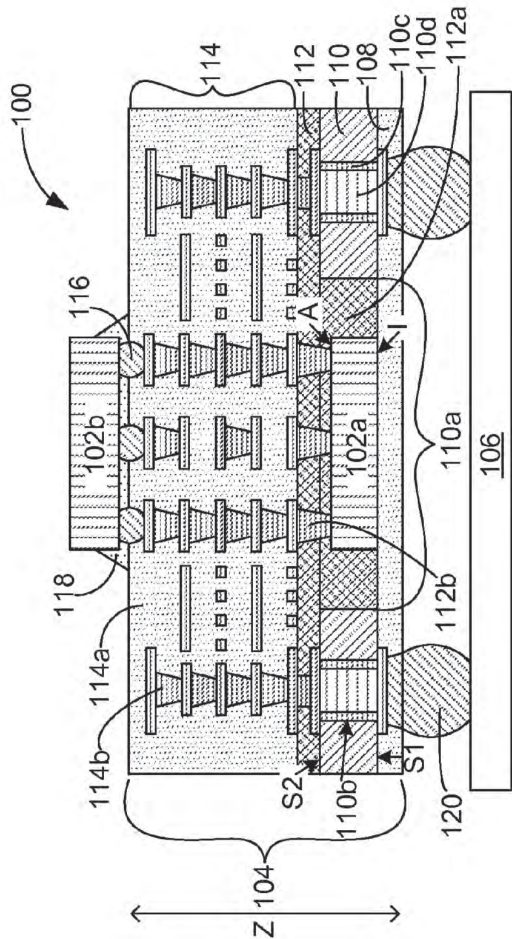
Shuto, FIG. 1

“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals

	<p>to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments. In other embodiments, additional build-up layers (not shown) may be formed on the die attach layer 108 to provide additional electrical routing for the package substrate 104 and the package-level interconnects may be coupled with the additional build-up layers.” Shuto, [6:25-6:40].</p> <p>“The package assembly 100 may further include a circuit board 106 coupled with the package substrate 104 through the package-level interconnects (e.g., solder balls 120). Only a small portion of the circuit board 106 may be depicted for the sake of discussion. The package-level interconnects may be coupled with contacts (e.g., pads) of the circuit board 106 to route electrical signals of the dies 102 a, 102 b between the package substrate 104 and the circuit board 106. The circuit board 106 may be a printed circuit board (PCB) composed of an electrically insulative material such as, for example, an epoxy laminate. For example, the circuit board 106 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Electrical routing structures (not shown) such as traces, trenches, vias, and the like may be formed through the electrically insulating layers to route the electrical signals of the dies 102 a, 102 b through the circuit board 106. The circuit board 106 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 106 is a motherboard (e.g., motherboard 802 of FIG. 8).” Shuto, [6:41-6:64].</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Shuto discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

	<div></div> <div><p>FIG. 1</p></div> <div><p>Shuto, FIG. 1</p></div> <div><p>“The package substrate 104 may include a die attach layer 108, which may be used as a substrate for attachment of the die 102 a. That is, in some embodiments, the die 102 a may be coupled in direct contact with the die attach layer 108. In some embodiments, the die attach layer 108 may be composed of an electrically insulative material such as, for example, an epoxy resin. In some embodiments, the die attach layer 108 may be composed of a same material as an insulator 114 a of the build-up layers 114. The die attach layer 108 may be composed of other suitable materials in other embodiments.” Shuto, [3:26-3:36].</p></div>
--	--

	<p>“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the prepreg material of the laminate layer 112 and die encapsulant material 112 a may include an epoxy resin with glass cloth. The prepreg material may further strengthen and/or reinforce the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114. The material of the laminate layer 112 and die encapsulant material 112 a may include other suitable materials in other embodiments. One or more interconnects may be formed in the laminate layer 112 to electrically couple the die 102 a with conductive features 114 b (e.g., electrical routing features) of the build-up layers 114. For example, in some embodiments, the interconnects may include via structures 112 b that extend through the laminate layer 112 and die encapsulant material 112 a to corresponding contacts such as pads on the die 102 a. The via structures 112 b may be formed using any suitable process including, for example, a laser process to remove material of the laminate layer 112 and die encapsulant material 112 a to</p>
--	--

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>provide a laser via joint between the die 102 a and the build-up layers 114. The laser via joint may have a structure consistent with being formed by a laser process. For example, a profile of the laser via joint may taper as can be seen. The interconnects of the laminate layer 112 may include other suitable interconnect structures in other embodiments.” Shuto, [4:63-5:21].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Shuto discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

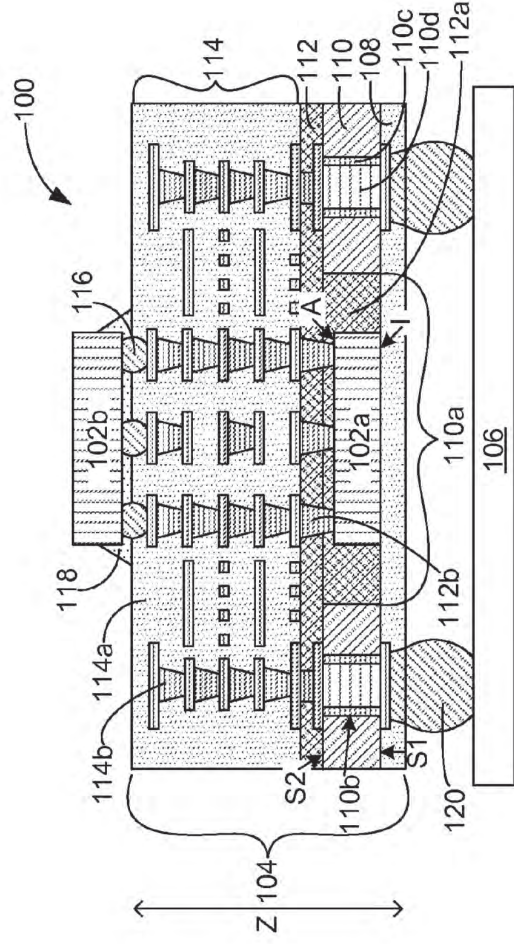


FIG. 1

Shuto, FIG. 1

“The package substrate 104 may include a die attach layer 108, which may be used as a substrate for attachment of the die 102 a. That is, in some embodiments, the die 102 a may be coupled in direct contact with the die attach layer 108. In some embodiments, the die attach layer 108 may be composed of an electrically insulative material such as, for example, an epoxy resin. In some embodiments, the die attach layer 108 may be composed of a same material as an insulator 114 a of the build-up layers 114. The die attach layer 108 may be composed of other suitable materials in other embodiments.” Shuto, [3:26-3:36].

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>“The package assembly 100 may include a die 102 a coupled with the die attach layer 108 and embedded in the package substrate 104. The die 102 a may have an active side, A, including active devices such as, for example, one or more transistor devices and an inactive side, I, disposed opposite to the active side A. In some embodiments, the inactive side I of the die 102 a may be in direct contact with the die attach layer 108. The die 102 a may be a discrete unit of an IC product made from a semiconductor material using semiconductor fabrication techniques such as thin film deposition, lithography, etching and the like. In some embodiments, the die may be, include, or be a part of a processor, memory, system on chip (SoC) or ASIC in some embodiments. In one embodiment, the die 102 a is a processor such as, for example, a central processing unit (CPU). The die 102 a may be configured to serve other functions in other embodiments.” Shuto, [3:37-3:53].</p> <p>“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].</p> <p>“According to various embodiments, the first die 102 a may be a logic die such as, for example, a processor or ASIC and the second die 102 b may be a memory die. The first dies 102 a and/or 102 b may be configured to perform other functions in other embodiments.” Shuto, [6:3-6:7].</p>
--	--

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Shuto discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

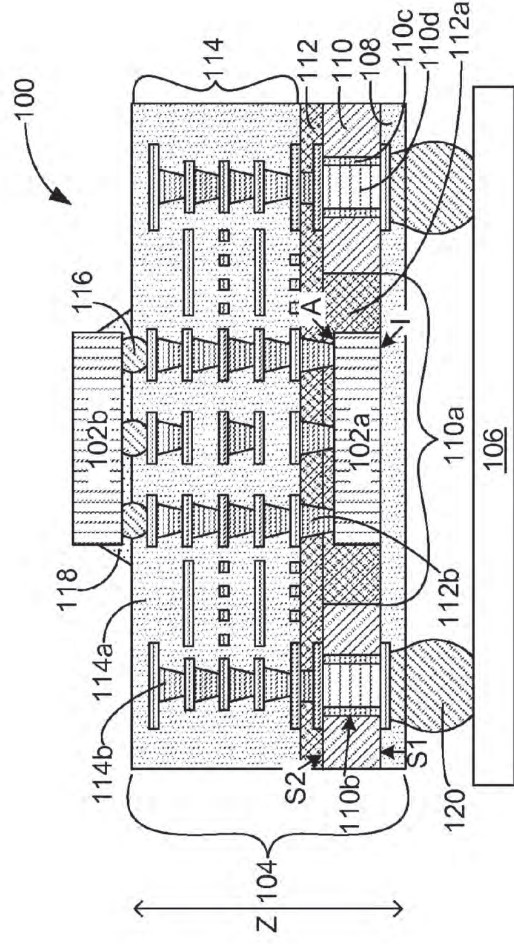


FIG. 1

Shuto, FIG. 1

“The package substrate 104 may include a die attach layer 108, which may be used as a substrate for attachment of the die 102 a. That is, in some embodiments, the die 102 a may be coupled in direct contact with the die attach layer 108. In some embodiments, the die attach layer 108 may be composed of an electrically insulative material such as, for example, an epoxy resin. In some embodiments, the die attach layer 108 may be composed of a same material as an insulator 114 a of the build-up layers 114. The die attach layer 108 may be composed of other suitable materials in other embodiments.” Shuto, [3:26-3:36].

	<p>“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].</p> <p>“According to various embodiments, the first die 102 a may be a logic die such as, for example, a processor or ASIC and the second die 102 b may be a memory die. The first dies</p>
--	--

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>102 a and/or 102 b may be configured to perform other functions in other embodiments.” Shuto, [6:3-6:7].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Shuto discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

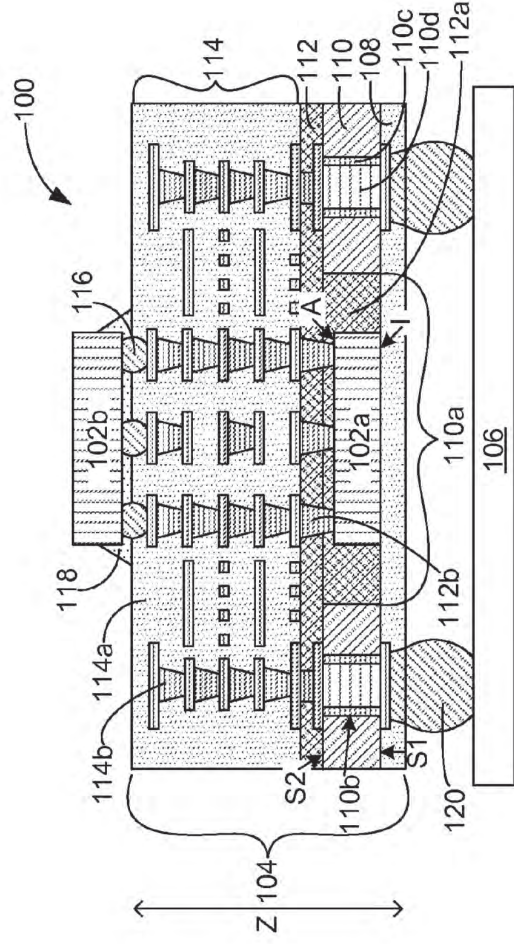


FIG. 1

Shuto, FIG. 1

“The package substrate 104 may include a die attach layer 108, which may be used as a substrate for attachment of the die 102 a. That is, in some embodiments, the die 102 a may be coupled in direct contact with the die attach layer 108. In some embodiments, the die attach layer 108 may be composed of an electrically insulative material such as, for example, an epoxy resin. In some embodiments, the die attach layer 108 may be composed of a same material as an insulator 114 a of the build-up layers 114. The die attach layer 108 may be composed of other suitable materials in other embodiments.” Shuto, [3:26-3:36].

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>“The package assembly 100 may include a die 102 a coupled with the die attach layer 108 and embedded in the package substrate 104. The die 102 a may have an active side, A, including active devices such as, for example, one or more transistor devices and an inactive side, I, disposed opposite to the active side A. In some embodiments, the inactive side I of the die 102 a may be in direct contact with the die attach layer 108. The die 102 a may be a discrete unit of an IC product made from a semiconductor material using semiconductor fabrication techniques such as thin film deposition, lithography, etching and the like. In some embodiments, the die may be, include, or be a part of a processor, memory, system on chip (SoC) or ASIC in some embodiments. In one embodiment, the die 102 a is a processor such as, for example, a central processing unit (CPU). The die 102 a may be configured to serve other functions in other embodiments.” Shuto, [3:37-3:53].</p> <p>“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p>
--	--

	<p>“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].</p> <p>“In some embodiments, the prepreg material of the laminate layer 112 and die encapsulant material 112 a may include an epoxy resin with glass cloth. The prepreg material may further strengthen and/or reinforce the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114. The material of the laminate layer 112 and die encapsulant material 112 a may include other suitable materials in other embodiments. One or more interconnects may be formed in the laminate layer 112 to electrically couple the die 102 a with conductive features 114 b (e.g., electrical routing features) of the build-up layers 114. For example, in some embodiments, the interconnects may include via structures 112 b that extend through the laminate layer 112 and die encapsulant material 112 a to corresponding contacts such as pads on the die 102 a. The via structures 112 b may be formed using any suitable process including, for example, a laser process to remove material of the laminate layer 112 and die encapsulant material 112 a to provide a laser via joint between the die 102 a and the build-up layers 114. The laser via joint may have a structure consistent with being formed by a laser process. For example, a profile of the laser via joint may taper as can be seen. The interconnects of the laminate layer 112 may include other suitable interconnect structures in other embodiments.” Shuto, [4:63-5:21].</p>
--	--

	<p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“According to various embodiments, the first die 102 a may be a logic die such as, for example, a processor or ASIC and the second die 102 b may be a memory die. The first dies 102 a and/or 102 b may be configured to perform other functions in other embodiments.” Shuto, [6:3-6:7].</p>
--	--

	<p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments. In other embodiments, additional build-up layers (not shown) may be formed on the die attach layer 108 to provide additional electrical routing for the package substrate 104 and the package-level interconnects may be coupled with the additional build-up layers.” Shuto, [6:25-6:40].</p> <p>“The package assembly 100 may further include a circuit board 106 coupled with the package substrate 104 through the package-level interconnects (e.g., solder balls 120). Only a small portion of the circuit board 106 may be depicted for the sake of discussion. The package-</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>level interconnects may be coupled with contacts (e.g., pads) of the circuit board 106 to route electrical signals of the dies 102 a, 102 b between the package substrate 104 and the circuit board 106. The circuit board 106 may be a printed circuit board (PCB) composed of an electrically insulative material such as, for example, an epoxy laminate. For example, the circuit board 106 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Electrical routing structures (not shown) such as traces, trenches, vias, and the like may be formed through the electrically insulating layers to route the electrical signals of the dies 102 a, 102 b through the circuit board 106. The circuit board 106 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 106 is a motherboard (e.g., motherboard 802 of FIG. 8).” Shuto, [6:41-6:64].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced</p>	<p>Shuto discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>

downwardly from the bottom surface of the top package substrate.

See, e.g.:

“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 112 and one or more build-up layers (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].

FIG. 1

	<p>Shuto, FIG. 1</p> <p>“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].</p> <p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“According to various embodiments, the first die 102 a may be a logic die such as, for example, a processor or ASIC and the second die 102 b may be a memory die. The first dies 102 a and/or 102 b may be configured to perform other functions in other embodiments.” Shuto, [6:3-6:7].</p> <p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“The package assembly 100 may further include a circuit board 106 coupled with the package substrate 104 through the package-level interconnects (e.g., solder balls 120). Only a small portion of the circuit board 106 may be depicted for the sake of discussion. The package-</p>
--	--

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>level interconnects may be coupled with contacts (e.g., pads) of the circuit board 106 to route electrical signals of the dies 102 a, 102 b between the package substrate 104 and the circuit board 106. The circuit board 106 may be a printed circuit board (PCB) composed of an electrically insulative material such as, for example, an epoxy laminate. For example, the circuit board 106 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Electrical routing structures (not shown) such as traces, trenches, vias, and the like may be formed through the electrically insulating layers to route the electrical signals of the dies 102 a, 102 b through the circuit board 106. The circuit board 106 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 106 is a motherboard (e.g., motherboard 802 of FIG. 8).” Shuto, [6:41-6:64].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate,	Shuto discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	<p>stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>
---	--

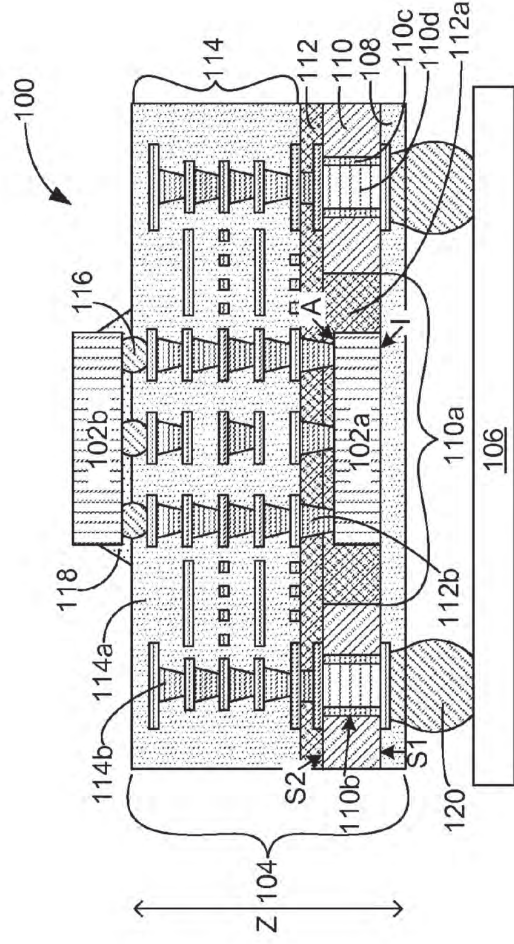


FIG. 1

Shuto, FIG. 1

“In some embodiments, the die 102 a may be disposed in the cavity 110 a. The die may have a thickness that is less than a thickness of the reinforced plate 110 as measured from the first side S1 to the second side S2, as can be seen, in some embodiments. Embedding the die 102 a in the cavity 110 a may reduce a total height (e.g., Z dimension indicated by arrow in FIG. 1) of the package substrate 104 and/or package assembly 100. For example, a separate discrete interposer element may not be needed to couple the package substrate 104 housing the die 102 a with the die 102 b (e.g., no need for micro-solder ball connections between packages housing respective dies 102 a and 102 b), which may allow reduction of the package height.” Shuto, [4:21-4:33].

	<p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“According to various embodiments, the first die 102 a may be a logic die such as, for example, a processor or ASIC and the second die 102 b may be a memory die. The first dies 102 a and/or 102 b may be configured to perform other functions in other embodiments.” Shuto, [6:3-6:7].</p>
--	--

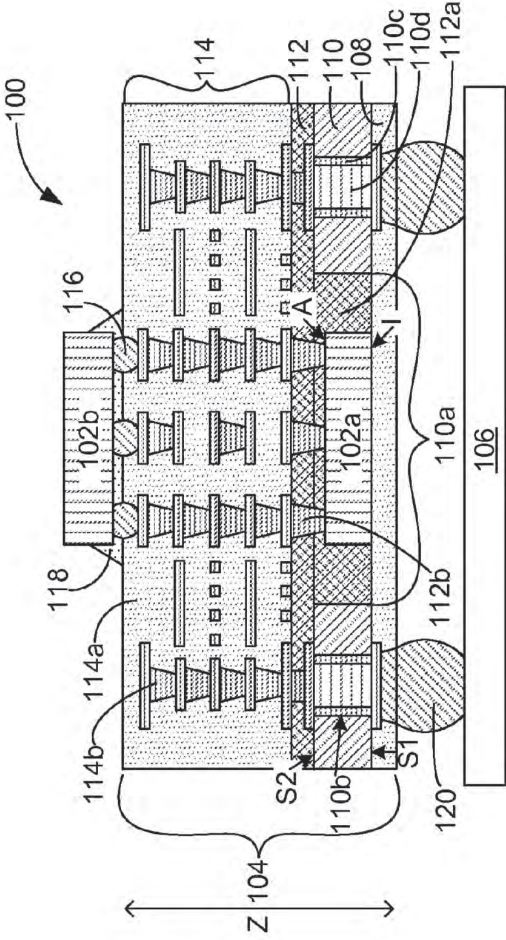
	<p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“The package assembly 100 may further include a circuit board 106 coupled with the package substrate 104 through the package-level interconnects (e.g., solder balls 120). Only a small portion of the circuit board 106 may be depicted for the sake of discussion. The package-level interconnects may be coupled with contacts (e.g., pads) of the circuit board 106 to route electrical signals of the dies 102 a, 102 b between the package substrate 104 and the circuit board 106. The circuit board 106 may be a printed circuit board (PCB) composed of an electrically insulative material such as, for example, an epoxy laminate. For example, the circuit board 106 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Electrical routing structures (not shown) such as traces, trenches, vias, and the like may be formed through the electrically insulating layers to route the electrical signals of the dies 102 a, 102 b through the circuit board 106. The circuit board 106 may be composed of other</p>
--	--

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>suitable materials in other embodiments. In some embodiments, the circuit board 106 is a motherboard (e.g., motherboard 802 of FIG. 8).” Shuto, [6:41-6:64].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>Shuto discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer</p>

	<p>(hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>  <p>Shuto, FIG. 1</p> <p>“In some embodiments, the prepreg material of the laminate layer 112 and die encapsulant material 112 a may include an epoxy resin with glass cloth. The prepreg material may further strengthen and/or reinforce the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114. The material of the laminate layer 112 and die encapsulant material 112 a may include other suitable materials in other embodiments. One or more interconnects may be formed in the laminate layer 112 to</p>
--	---

	<p>electrically couple the die 102 a with conductive features 114 b (e.g., electrical routing features) of the build-up layers 114. For example, in some embodiments, the interconnects may include via structures 112 b that extend through the laminate layer 112 and die encapsulant material 112 a to corresponding contacts such as pads on the die 102 a. The via structures 112 b may be formed using any suitable process including, for example, a laser process to remove material of the laminate layer 112 and die encapsulant material 112 a to provide a laser via joint between the die 102 a and the build-up layers 114. The laser via joint may have a structure consistent with being formed by a laser process. For example, a profile of the laser via joint may taper as can be seen. The interconnects of the laminate layer 112 may include other suitable interconnect structures in other embodiments.” Shuto, [4:63-5:21].</p> <p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers</p>
--	---

	<p>114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments. In other embodiments, additional build-up layers (not shown) may be formed on the die attach layer 108 to provide additional electrical routing for the package substrate 104 and the</p>
--	--

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>package-level interconnects may be coupled with the additional build-up layers.” Shuto, [6:25-6:40].</p> <p>“The package assembly 100 may further include a circuit board 106 coupled with the package substrate 104 through the package-level interconnects (e.g., solder balls 120). Only a small portion of the circuit board 106 may be depicted for the sake of discussion. The package-level interconnects may be coupled with contacts (e.g., pads) of the circuit board 106 to route electrical signals of the dies 102 a, 102 b between the package substrate 104 and the circuit board 106. The circuit board 106 may be a printed circuit board (PCB) composed of an electrically insulative material such as, for example, an epoxy laminate. For example, the circuit board 106 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Electrical routing structures (not shown) such as traces, trenches, vias, and the like may be formed through the electrically insulating layers to route the electrical signals of the dies 102 a, 102 b through the circuit board 106. The circuit board 106 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 106 is a motherboard (e.g., motherboard 802 of FIG. 8).” Shuto, [6:41-6:64].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Shuto discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>

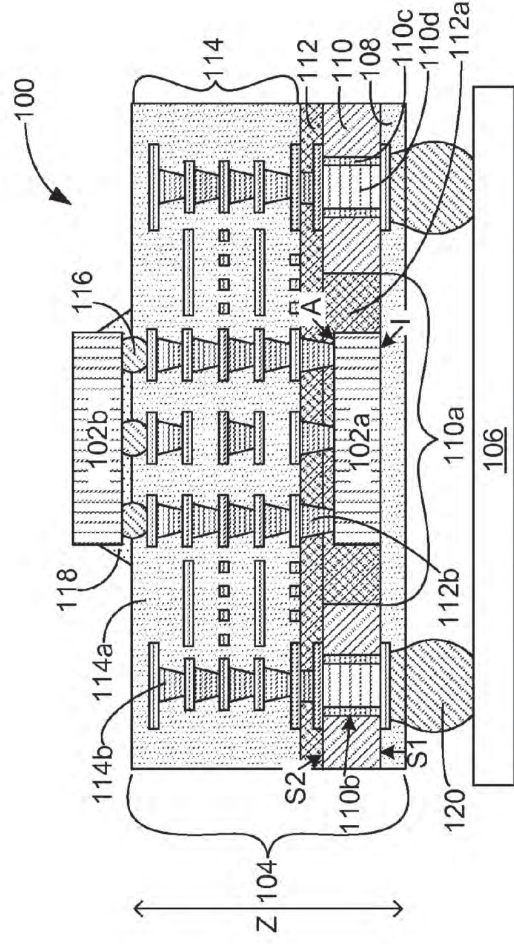


FIG. 1

Shuto, FIG. 1

“The package substrate 104 may include a die attach layer 108, which may be used as a substrate for attachment of the die 102 a. That is, in some embodiments, the die 102 a may be coupled in direct contact with the die attach layer 108. In some embodiments, the die attach layer 108 may be composed of an electrically insulative material such as, for example, an epoxy resin. In some embodiments, the die attach layer 108 may be composed of a same material as an insulator 114 a of the build-up layers 114. The die attach layer 108 may be composed of other suitable materials in other embodiments.” Shuto, [3:26-3:36].

	<p>“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the prepreg material of the laminate layer 112 and die encapsulant material 112 a may include an epoxy resin with glass cloth. The prepreg material may further strengthen and/or reinforce the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114. The material of the laminate layer 112 and die encapsulant material 112 a may include other suitable materials in other embodiments. One or more interconnects may be formed in the laminate layer 112 to electrically couple the die 102 a with conductive features 114 b (e.g., electrical routing features) of the build-up layers 114. For example, in some embodiments, the interconnects may include via structures 112 b that extend through the laminate layer 112 and die encapsulant material 112 a to corresponding contacts such as pads on the die 102 a. The via structures 112 b may be formed using any suitable process including, for example, a laser process to remove material of the laminate layer 112 and die encapsulant material 112 a to</p>
--	--

	<p>provide a laser via joint between the die 102 a and the build-up layers 114. The laser via joint may have a structure consistent with being formed by a laser process. For example, a profile of the laser via joint may taper as can be seen. The interconnects of the laminate layer 112 may include other suitable interconnect structures in other embodiments.” Shuto, [4:63-5:21].</p> <p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments. In other embodiments, additional build-up layers (not shown) may be formed on the die attach layer 108 to provide additional electrical routing for the package substrate 104 and the package-level interconnects may be coupled with the additional build-up layers.” Shuto, [6:25-6:40].</p> <p>“The package assembly 100 may further include a circuit board 106 coupled with the package substrate 104 through the package-level interconnects (e.g., solder balls 120). Only a small portion of the circuit board 106 may be depicted for the sake of discussion. The package-</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>level interconnects may be coupled with contacts (e.g., pads) of the circuit board 106 to route electrical signals of the dies 102 a, 102 b between the package substrate 104 and the circuit board 106. The circuit board 106 may be a printed circuit board (PCB) composed of an electrically insulative material such as, for example, an epoxy laminate. For example, the circuit board 106 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Electrical routing structures (not shown) such as traces, trenches, vias, and the like may be formed through the electrically insulating layers to route the electrical signals of the dies 102 a, 102 b through the circuit board 106. The circuit board 106 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 106 is a motherboard (e.g., motherboard 802 of FIG. 8).” Shuto, [6:41-6:64].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on	Shuto discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 schematically illustrates a cross-section side view of an example integrated circuit (IC) package assembly (hereinafter “package assembly 100”), in accordance with some embodiments. In some embodiments, the package assembly 100 includes a package substrate 104 coupled with one or more dies (e.g., dies 102 a, 102 b) and a circuit board 106, as can be seen. In an embodiment, the package assembly 100 may refer to only the package substrate 104. The package substrate 104 may include a die attach layer 108, a reinforced layer (hereinafter “reinforced plate 110”), a laminate layer 112 and one or more build-up layers (hereinafter “build-up layers 114”), coupled as shown.” Shuto, [3:13-3:25].</p>
---	---

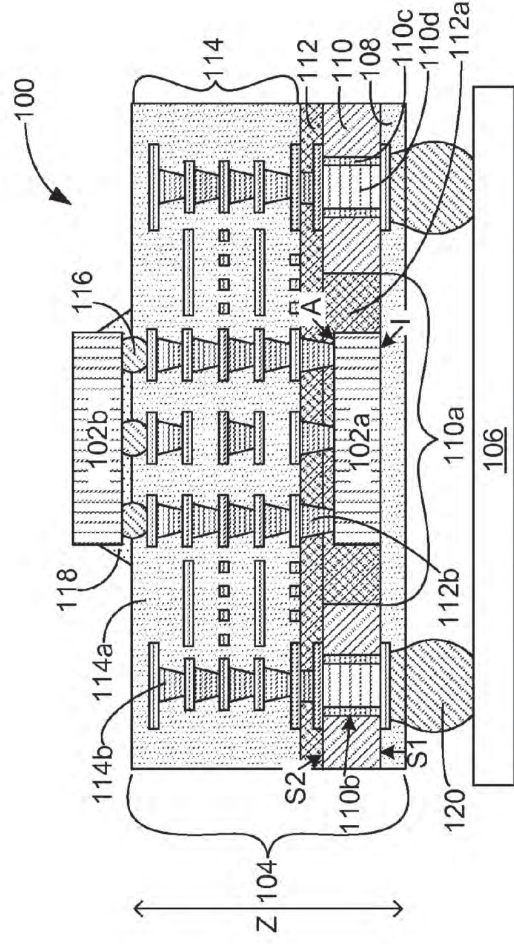


FIG. 1

Shuto, FIG. 1

“In some embodiments, the reinforced plate 110 may be composed of an epoxy resin with glass cloth. In other embodiments, the reinforced plate 110 may be composed of a metal (e.g., as described in connection with FIG. 3). The reinforced plate 110 may be composed of other suitable materials in other embodiments. The reinforced plate 110 may strengthen the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114 using, for example bumpless build-up layer (BBUL) techniques. For example, in some embodiments, the reinforced plate 110 may obviate a need for using a fixture jig, which may be used for handling and/or assembly during fabrication of a flexible package substrate. The reinforced plate 110 may have a first side, S1, and a second side, S2, disposed

	<p>opposite to the first side S1. In some embodiments, the first side S1 may be in direct contact with the die attach layer 108. The reinforced plate 110 may further have a cavity 110 a formed in the reinforced plate 110. In some embodiments, the cavity 110 a may pass through the reinforced plate 110 to provide an opening between the first side S1 and the second side S2, as can be seen.” Shuto, [3:66-4:20].</p> <p>“In some embodiments, the prepreg material of the laminate layer 112 and die encapsulant material 112 a may include an epoxy resin with glass cloth. The prepreg material may further strengthen and/or reinforce the package substrate 104 for handling and/or assembly associated with fabrication of the build-up layers 114. The material of the laminate layer 112 and die encapsulant material 112 a may include other suitable materials in other embodiments. One or more interconnects may be formed in the laminate layer 112 to electrically couple the die 102 a with conductive features 114 b (e.g., electrical routing features) of the build-up layers 114. For example, in some embodiments, the interconnects may include via structures 112 b that extend through the laminate layer 112 and die encapsulant material 112 a to corresponding contacts such as pads on the die 102 a. The via structures 112 b may be formed using any suitable process including, for example, a laser process to remove material of the laminate layer 112 and die encapsulant material 112 a to provide a laser via joint between the die 102 a and the build-up layers 114. The laser via joint may have a structure consistent with being formed by a laser process. For example, a profile of the laser via joint may taper as can be seen. The interconnects of the laminate layer 112 may include other suitable interconnect structures in other embodiments.” Shuto, [4:63-5:21].</p> <p>“The package substrate 104 may further include the build-up layers 114 coupled with the first side of reinforced plate 110. In some embodiments, an individual build-up layer of the build-up layers 114 is in direct contact with the laminate layer 112. The build-up layers 114 may include electrical routing features (e.g., hereinafter “conductive features 114 b”) of individual</p>
--	---

	<p>build-up layers 114 coupled together in an electrically insulative material (hereinafter “insulator 114 a”). The conductive features 114 b may include, for example, trenches, vias, traces or other suitable routing structures composed of an electrically conductive material such as metal (e.g., copper). The insulator 114 a may be composed of an epoxy resin. The conductive features 114 b and the insulator 114 a may be composed of other suitable materials in other embodiments. In some embodiments, the build-up layers 114 may be formed using Ajinomoto Build-up Film (ABF) techniques. Other suitable techniques to fabricate the build-up layers 114 may be used in other embodiments. In some embodiments, another die 102 b may be coupled with the package substrate 104. For example, in the depicted embodiment, the die 102 b is coupled with the build-up layers 114 in a flip-chip configuration using solderable material 116 such as solder bumps to couple corresponding contacts (e.g., pads) on the die 102 b with the conductive features 114 b of the build-up layers 114. In some embodiments, an underfill material 118 may be disposed between an active side of the die 102 b and the package substrate 104. The die 102 b may be coupled with the package substrate 104 using other suitable techniques such as, for example, wirebonding techniques, embedding techniques and the like or other FLI interconnect structures such as pillars to couple the die 102 b with the package substrate 104.” Shuto, [5:37-6:2].</p> <p>“In some embodiments, the conductive features 114 b of the build-up layers 114 may be electrically coupled with the dies 102 a and/or 102 b (e.g., and possibly other dies) and configured to route electrical signals of the dies 102 a and/or 102 b through the package substrate 104. The electrical signals may include, for example, input/output (I/O signals) and/or power/ground signals associated with operation of the dies 102 a, 102 b. In some embodiments, the conductive features 114 b may route electrical signals between the dies 102 a, 102 b. In this regard, the dies 102 a and 102 b may be electrically coupled with one another. In some embodiments, the conductive features 114 b may route electrical signals between one or more of the dies 102 a, 102 b and another electrical component such as, for</p>
--	---

	<p>example, a circuit board 106 by way of interconnects in the laminate layer 112, PTHs 110 b and/or package-level interconnects such as solder balls 120.” Shuto, [6:8-6:24].</p> <p>“In some embodiments, one or more package-level interconnects such as, for example, solder balls 120 may be coupled with the package substrate 104 to further route the electrical signals to another electrical component such as circuit board 106. The solder balls 120 may be arranged in a ball-grid array (BGA) configuration in some embodiments. The package-level interconnects may include other suitable structures such as, for example, land-grid array (LGA) structures. The package-level interconnects (e.g., solder balls 120) may be coupled with the PTHs 110 b through the die attach layer 108, as can be seen, in some embodiments. In other embodiments, additional build-up layers (not shown) may be formed on the die attach layer 108 to provide additional electrical routing for the package substrate 104 and the package-level interconnects may be coupled with the additional build-up layers.” Shuto, [6:25-6:40].</p> <p>“The package assembly 100 may further include a circuit board 106 coupled with the package substrate 104 through the package-level interconnects (e.g., solder balls 120). Only a small portion of the circuit board 106 may be depicted for the sake of discussion. The package-level interconnects may be coupled with contacts (e.g., pads) of the circuit board 106 to route electrical signals of the dies 102 a, 102 b between the package substrate 104 and the circuit board 106. The circuit board 106 may be a printed circuit board (PCB) composed of an electrically insulative material such as, for example, an epoxy laminate. For example, the circuit board 106 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are laminated together using an epoxy resin prepreg material. Electrical routing structures (not shown) such as traces, trenches, vias, and the like may be</p>
--	---

Appendix A-30 - Invalidity of U.S. Patent No. 9859202 in view of Shuto - U.S. Patent No. 9685414

	<p>formed through the electrically insulating layers to route the electrical signals of the dies 102 a, 102 b through the circuit board 106. The circuit board 106 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 106 is a motherboard (e.g., motherboard 802 of FIG. 8).” Shuto, [6:41-6:64].</p> <p>To the extent Plaintiff contends that Shuto fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

U.S. Patent Publication No. 20110147908 (“Sun”) is titled Module for Use in a Multi Package Assembly and a Method of Making the Module and the Multi Package Assembly and lists Peng Sun, Kuen Vincent Leung, and Xun Qing Shi as inventors. Sun anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Sun is a U.S. patent publication that was filed December 17, 2009 and published June 23, 2011. Sun is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Sun, or otherwise rendered obvious by disclosures and teachings of Sun, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Sun does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Sun with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Sun, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Sun “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Sun or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Sun set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Sun discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 2 shows a module 100 for use in a multichip package. In particular a module for use in the lower part of a PoP assembly. It comprises a first substrate 110 which may be a PCB, preferably a BT core substrate. A (bismaleimide triazine) core substrate, is a substrate comprising a BT core layer with a metal layer on either side. BT has the advantage that it is a polyimide with higher thermal stability, better chemical resistance and mechanical properties compared to the epoxy resin used in same other types of PCB. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be</p>

	<p>mounted to an external apparatus, such as a motherboard. A chip 200, which may be a memory chip or a processor, is mounted to the first substrate 100. It may be mounted by any appropriate method, for example die attachment with wire bonding, flip chip etc. Wires 220 connect a bonding pad 210 on top of the chip 200 with a bonding pad 240 on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140. The assembly is overmolded with a molding material 120. The molding material covers the chip 200, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed and are level with or extend above the upper surface of the overmold. The upper ends 311 may make contact with an external module.” Sun, [0047-0048].</p> <p>“FIG. 3 shows another embodiment of the first module, similar to FIG. 2. Like reference numerals are used to describe like parts and will not be described again. This embodiment has two chips 500 (a) and 500 (b) stacked one on top of the other. The first chip 500 (a) is mounted to the first substrate 110 by any suitable means. The second chip 500 (b) is mounted on top of the first chip 500 (a) and spaced apart from the first chip by a spacer 530. Wires 520 connect bonding pads on the chips 500 (a), 500 (b) to bonding pads on the first substrate 110. The molding material 120 covers both the first and second chips.” Sun, [0048-0049].</p>
--	--

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“FIG. 4 is a third embodiment similar to the first two embodiments. It has two chips 810 and 820 mounted side by side on the first substrate 110. The overmolding material covers both the first and second chips 810, 820.” Sun, [0050].</p> <p>“FIG. 12 is a schematic diagram of a PoP assembly 1 comprising a second module 5 mounted on a first module 10. The first module 5 is a module of the type described above, e.g. with reference to FIG. 2. It forms a lower module of the PoP assembly. In this example, it has two chips 200, 200 a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220 a respectively. Both chips are processors. Other embodiments could have a different number or type of chips and different method of connecting the chips to the substrate 110. The upper module 5 comprises a pair of chips 30, 31 mounted to a first (upper) side of a third substrate 20. The third substrate may be a PCB, preferably a BT core substrate. The chips 30, 31 are electrically connected to the third substrate 20 by wires 16 or any other suitable means. Preferably the chips 30 and 31 are memory chips. The second module 5 is overmolded with a molding material 18 which covers the chips 30, 31 and the third substrate 20. The second (lower) side of the third substrate 20 is mounted to the first module 10. Specifically the third substrate is mounted directly to the second connectors 310 of the first module 5. Upper ends of the second connectors 310 connect with a conducting electrical contacts (not shown) of the second (lower) side of the third substrate 20 in order to allow communication of electrical signals between the two modules.” Sun, [0058-0059].</p> <p>“The first module 1 will now be described in more detail. It comprises a first substrate 110 which may be a PCB, preferably a BT core substrate. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A pair of chips 200, 200 a may be memory chips or a processor, are mounted to the first substrate 110. They may be mounted by any appropriate</p>
--	--

	<p>method, for example wire bonding, die attachment etc. Wires 220, 220 a connect a bonding pad on top of the chip 200 with a bonding pad on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chips 200, 200 a. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding 140. The first module 10 is overmolded with a molding material 120. The molding material covers the chips 200, 200 a, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed above the overmold 120. The upper ends 311 make contact with electrical contacts of the second module 5.” Sun, [0060-0061].</p> <p>“FIG. 13 shows the second substrate and surrounding components in more detail. In particular, it illustrates the vias 390 extending through the second substrate 300. First metal connectors 320 are provided on a second (lower) side of the second substrate 300. These are surrounded by the molding compound 120 and mounted to the first substrate 110. Second metal connectors 320 are provided on the first (upper) side of the second substrate. They are surrounded by the molding compound 120 and have exposed upper ends 311. The second metal connectors 310 are aligned with corresponding second metal connectors 310 on the opposite side of the substrate 300. Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320. The vias 390 extend through the second substrate 300. The via has first 391 and second 392 side walls. These side walls 391, 392</p>
--	--

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>may be part of the same (e.g. circular) side wall or may be separate side walls. The via 390 further comprises a core 395 between the side walls and extending between the first and second metal connectors 320, 310. In the illustrated embodiment shown in FIG. 13 the side walls 391, 392 are electrically conductive (e.g. made of metal) and put the first and second metal connectors 320, 310 in electrical contact with each other.” Sun, [0062-0064].</p>
<p>[1.A] a bottom package substrate;</p>	<p>Sun discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 2 shows a module 100 for use in a multichip package. In particular a module for use in the lower part of a PoP assembly. It comprises a first substrate 110 which maybe a PCB, preferably a BT core substrate. A (bismaleimide triazine) core substrate, is a substrate comprising a BT core layer with a metal layer on either side. BT has the advantage that it is a polyimide with higher thermal stability, better chemical resistance and mechanical properties compared to the epoxy resin used in same other types of PCB. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard.” Sun, [0047].</p>

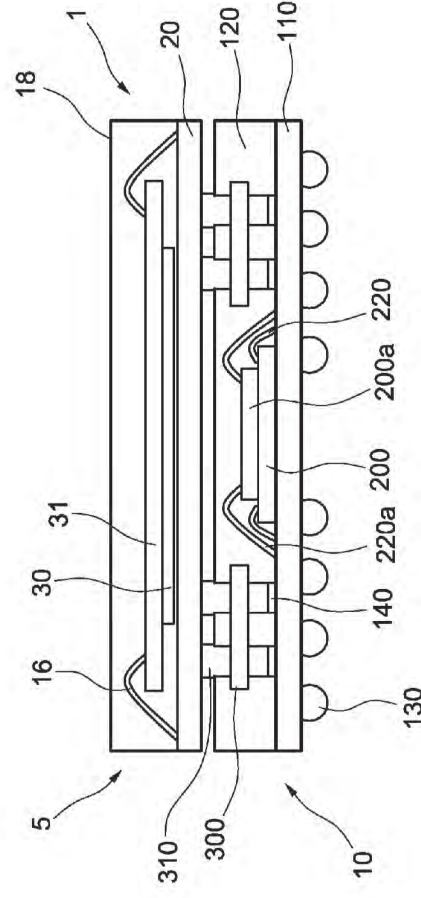


FIG. 12

Sun, FIG. 12

“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140. The assembly is overmolded with a molding material 120. The molding material covers the chip 200, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed and are level with or extend above the upper surface of the overmold. The upper ends 311 may make contact with an external module. For example an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.” Sun, [0048].</p> <p>“FIG. 12 is a schematic diagram of a PoP assembly 1 comprising a second module 5 mounted on a first module 10. The first module 5 is a module of the type described above, e.g. with reference to FIG. 2. It forms a lower module of the PoP assembly. In this example, it has two chips 200, 200 a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220 a respectively.” Sun, [0058].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Sun discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“A typical PoP assembly 1 is shown in FIG. 1. It comprises a first electronic package 5 mounted on top of a second electronic package 10. Typically the top package 5 has a memory device, while the bottom package has a processor. Due to their compact nature, PoP assemblies are used in many electronic devices. For example in a mobile phone the top package may have a memory device and the bottom package a baseband or applications</p>

	<p>processor. In a digital camera the top package may have a memory device and the bottom package an image processor. In a handheld computer or game system, the top package may have a memory device and the bottom package an audio or graphics processor. The top package in FIG. 1 has a substrate 20. Typically the substrate will be a BT core substrate. A pair of chips 30, 31 are mounted to the substrate 20. Wires 16, 18 connect the chips 30, 31 to electrical contacts 11 of the substrate 20. The top package is covered with a molding compound 30 (over molded). This strengthens the assembly and helps to protect the components from damage. The lower package 10 also comprises a substrate 40 and a chip 50 mounted to the substrate. The chip 50 is connected to electrical contacts 41 of the substrate by wires 45. An overmold 60 covers the chip 50 and a surrounding part of the substrate on which the chip is mounted. The top package 5 is mounted to the bottom package 10 by solder balls 70.” Sun, [0003-0007].</p> <p>“A second aspect of the present invention provides a multi-package assembly comprising the module of the first aspect of the present invention as the first module and a second module comprising a chip mounted on a third substrate. The second module may be mounted to the first module; preferably it is mounted directly to the overmold of the first module. The third substrate is preferably mounted to the first module. For example the third substrate may be mounted to the second substrate of the first module via overmold of the second substrate and/or the second electrical connectors. Preferably the at least one second electrical connector is in electrical contact with a conducting contact of the third substrate. Preferably the at least one second connector is in direct physical contact with the third substrate. The chip of the second module is preferably mounted to a first side of the third substrate and a second side of the third substrate is preferably mounted to the first module. E.g. the third substrate may be mounted to the second substrate via the overmold of the second substrate and/or the second electrical connectors.” Sun, [0020-0023].</p>
--	--

	<p>“FIG. 2 shows a module 100 for use in a multichip package. In particular a module for use in the lower part of a PoP assembly. It comprises a first substrate 110 which maybe a PCB, preferably a BT core substrate. A (bismaleimide triazine) core substrate, is a substrate comprising a BT core layer with a metal layer on either side. BT has the advantage that it is a polymide with higher thermal stability, better chemical resistance and mechanical properties compared to the epoxy resin used in same other types of PCB. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A chip 200, which may be a memory chip or a processor, is mounted to the first substrate 100. It may be mounted by any appropriate method, for example die attachment with wire bonding, flip chip etc. Wires 220 connect a bonding pad 210 on top of the chip 200 with a bonding pad 240 on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140. The assembly is overmolded with a molding material 120. The molding material covers the chip 200, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed and are level with or extend above the upper surface of the overmold. The upper ends 311 may make contact with an external module. For example an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.” Sun, [0047-0048].</p>
--	--

	<p>“FIG. 12 is a schematic diagram of a PoP assembly 1 comprising a second module 5 mounted on a first module 10. The first module 5 is a module of the type described above, e.g. with reference to FIG. 2. It forms a lower module of the PoP assembly. In this example, it has two chips 200, 200 a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220 a respectively. Both chips are processors. Other embodiments could have a different number or type of chips and different method of connecting the chips to the substrate 110. The upper module 5 comprises a pair of chips 30, 31 mounted to a first (upper) side of a third substrate 20. The third substrate may be a PCB, preferably a BT core substrate. The chips 30, 31 are electrically connected to the third substrate 20 by wires 16 or any other suitable means. Preferably the chips 30 and 31 are memory chips. The second module 5 is overmolded with a molding material 18 which covers the chips 30, 31 and the third substrate 20. The second (lower) side of the third substrate 20 is mounted to the first module 10.” Sun, [0058-0059].</p>
--	---

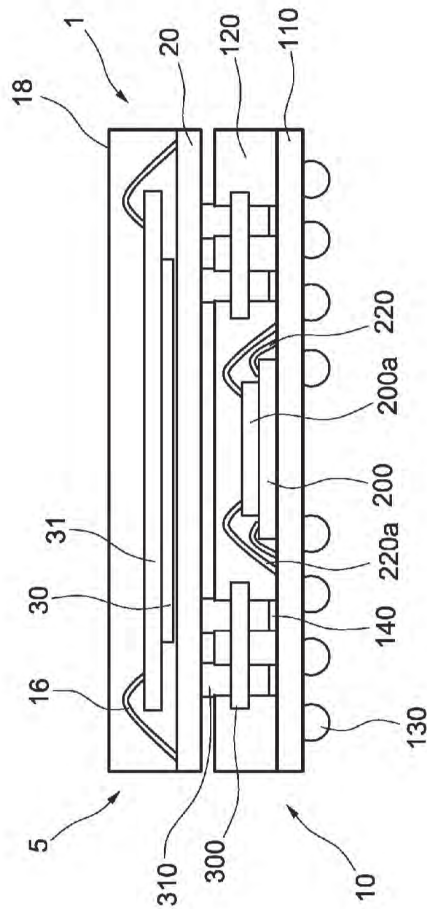


FIG.12

Sun, FIG. 12

“While FIG. 12 shows a gap between the first and second modules, in other embodiments the overmold 120 of the first module may extend flush with the upper ends of the second connectors and the third substrate 20 of the second module 5 may rest on the overmold 120 of the first module. That is the third substrate 20 may be in direct contact with the overmold between the overmold 120 and second connectors 310 and the third substrate 20 of the second module 5.” Sun, [0059].

“The first module 1 will now be described in more detail. It comprises a first substrate 110 which may be a PCB, preferably a BT core substrate. Solder balls 130 are provided on the

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A pair of chips 200, 200 a may be memory chips or a processor, are mounted to the first substrate 110. They may be mounted by any appropriate method, for example wire bonding, die attachment etc. Wires 220, 220 a connect a bonding pad on top of the chip 200 with a bonding pad on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chips 200, 200 a. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding 140. The first module 10 is overmolded with a molding material 120. The molding material covers the chips 200, 200 a, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed above the overmold 120. The upper ends 311 make contact with electrical contacts of the second module 5." Sun, [0060-0061].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Sun discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“The top package 5 is mounted to the bottom package 10 by solder balls 70. The solder balls 70 space the two packages apart allowing room for the chip 50 of the lower package.” Sun, [0007].</p> <p>“Secondly, the space between the upper and lower packages is limited. It would be desirable to increase the vertical separation (stand off height) in order to make room for more and larger chips and enable stacking of chips on the lower substrate.” Sun, [0010].</p> <p>“As the lower module has a second substrate with electrical connectors on either side, the stand off height may be increased. Further, the opening in the second substrate makes room for one or more chips mounted to the first substrate.” Sun, [0014].</p> <p>“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300.” Sun, [0048].</p>
---	--

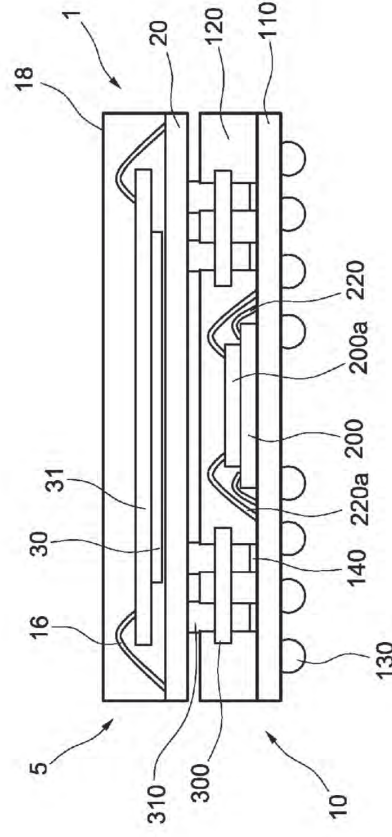


FIG. 12

Sun, FIG. 12

“Upper ends 311 of the second connectors 310 are exposed and are level with or extend above the upper surface of the overmold. The upper ends 311 may make contact with an external module. For example an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.” Sun, [0048].

“The second module 5 is overmolded with a molding material 18 which covers the chips 30, 31 and the third substrate 20. The second (lower) side of the third substrate 20 is mounted to the first module 10. Specifically the third substrate is mounted directly to the second connectors 310 of the first module 5. Upper ends of the second connectors 310 connect with a conducting electrical contacts (not shown) of the second (lower) side of the third substrate

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>20 in order to allow communication of electrical signals between the two modules. While FIG. 12 shows a gap between the first and second modules, in other embodiments the overmold 120 of the first module may extend flush with the upper ends of the second connectors and the third substrate 20 of the second module 5 may rest on the overmold 120 of the first module.” Sun, [0059].</p> <p>“In a second step, shown in FIG. 16 (b), a second substrate 300 having second electrical connectors 310 on a first (upper) side thereof and first electrical connectors 320 on a second (lower) side thereof, is mounted to the first substrate 100. Specifically the first electrical connectors 320 are mounted to the bonding pads 140. The second substrate 300 has one or more openings therein. In a third step, shown in FIG. 16 (c), one or more chips 200, 200 a are mounted to the first substrate via the space provided by the opening in the second substrate.” Sun, [0069-0070].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Sun discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The second substrate may have only a single layer. The single layer is preferably an insulating layer, e.g. made of polymer. Alternatively the second substrate may have plural layers. For example, the second substrate may comprise a core insulator layer and conducting</p>

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>layers on either side of the core layer. There may be insulating layers (e.g. solder resists) outward on either side of the conducting layers.” Sun, [0016].</p> <p>“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars.” Sun, [0048].</p>
--	--

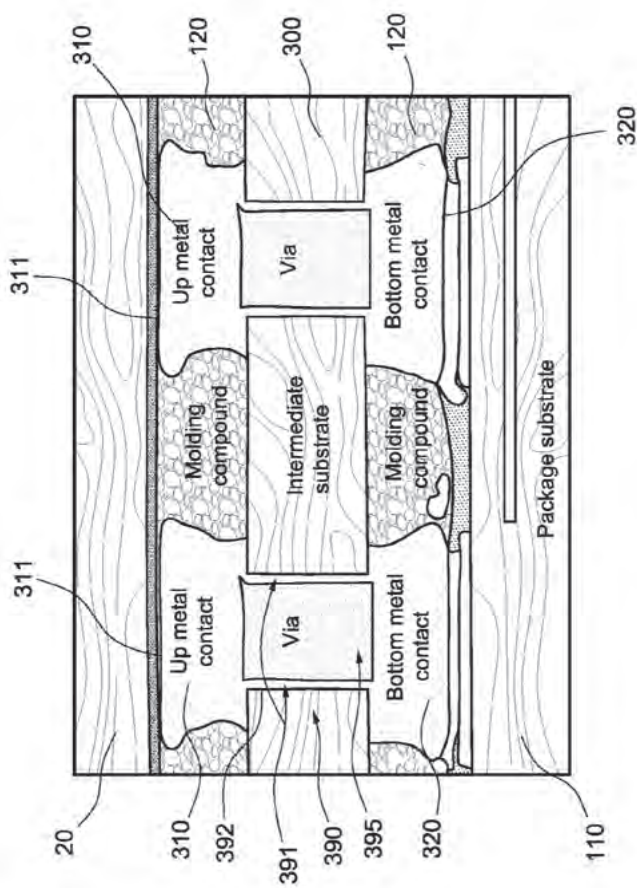
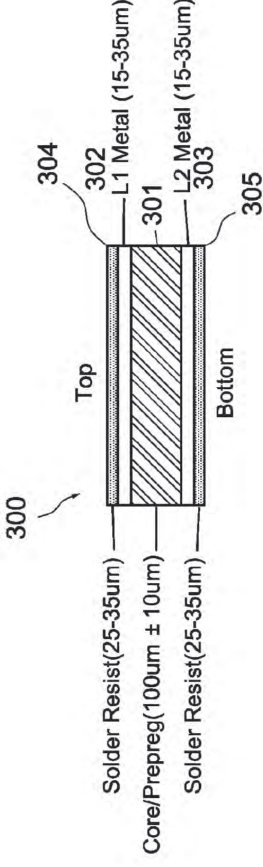


FIG.13

Sun, FIG. 13

	<p>“The second substrate 300 in the FIG. 13 embodiment is a simple insulator, e.g. polymer. However, in other embodiments it may be a PCB or it may comprise a plurality of layers. An example is shown in FIG. 15 where the second substrate 300 comprises a core/prepreg insulating layer 301, a metal layer 302, 303 on either side of the core layer and an insulating solder resist layer 304, 305 on either side of the metal layers.” Sun, [0065].</p>  <p style="text-align: center;">FIG.15</p> <p style="text-align: center;">Sun, FIG. 15</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Sun discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p>

	<p><i>See, e.g.:</i></p> <p>“One or more vias preferably extend through said second substrate. The vias electrically connect the at least one first electrical connector with the at least one second electrical connector. Preferably the via and the first and second electrical connectors which the via connects are three separate pieces.” Sun, [0017].</p> <p>“Each via typically comprises first and second electrically conductive side walls. The first and second side walls are electrically connected to each other by the first electrical connector and said second electrical connector (at either end of the via). The term side walls as used herein includes the situation where the two ‘side walls’ are part of the same wall, e.g. different parts of a circular wall. The via may have an insulating core. Alternatively the via may have metal side walls and a metal core, or an insulating sidewalls and a conducting core.” Sun, [0018].</p> <p>“FIG. 13 shows the second substrate and surrounding components in more detail. In particular, it illustrates the vias 390 extending through the second substrate 300. First metal connectors 320 are provided on a second (lower) side of the second substrate 300. These are surrounded by the molding compound 120 and mounted to the first substrate 110. Second metal connectors 320 are provided on the first (upper) side of the second substrate. They are surrounded by the molding compound 120 and have exposed upper ends 311. The second metal connectors 310 are aligned with corresponding second metal connectors 310 on the opposite side of the substrate 300. Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” Sun, [0062-0063].</p>
--	---

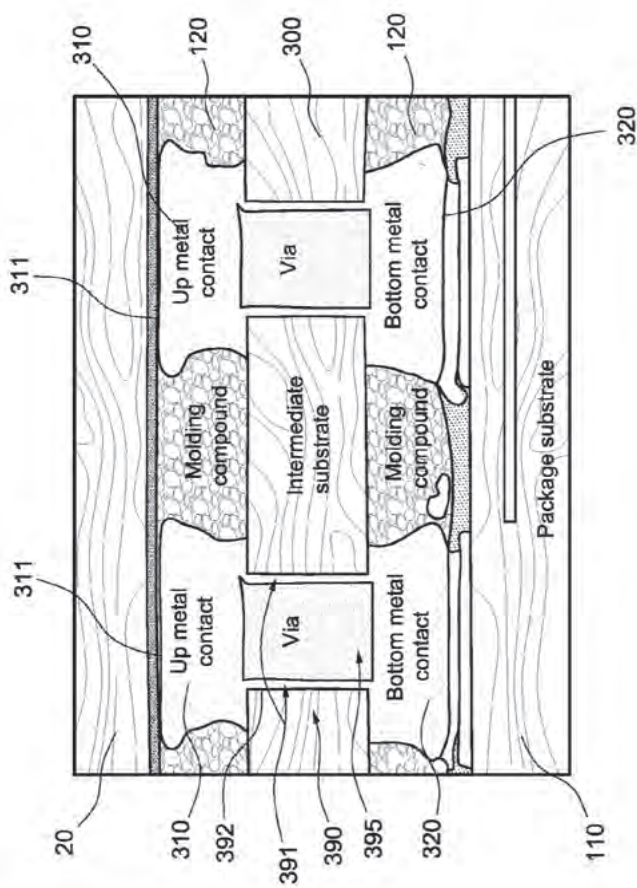


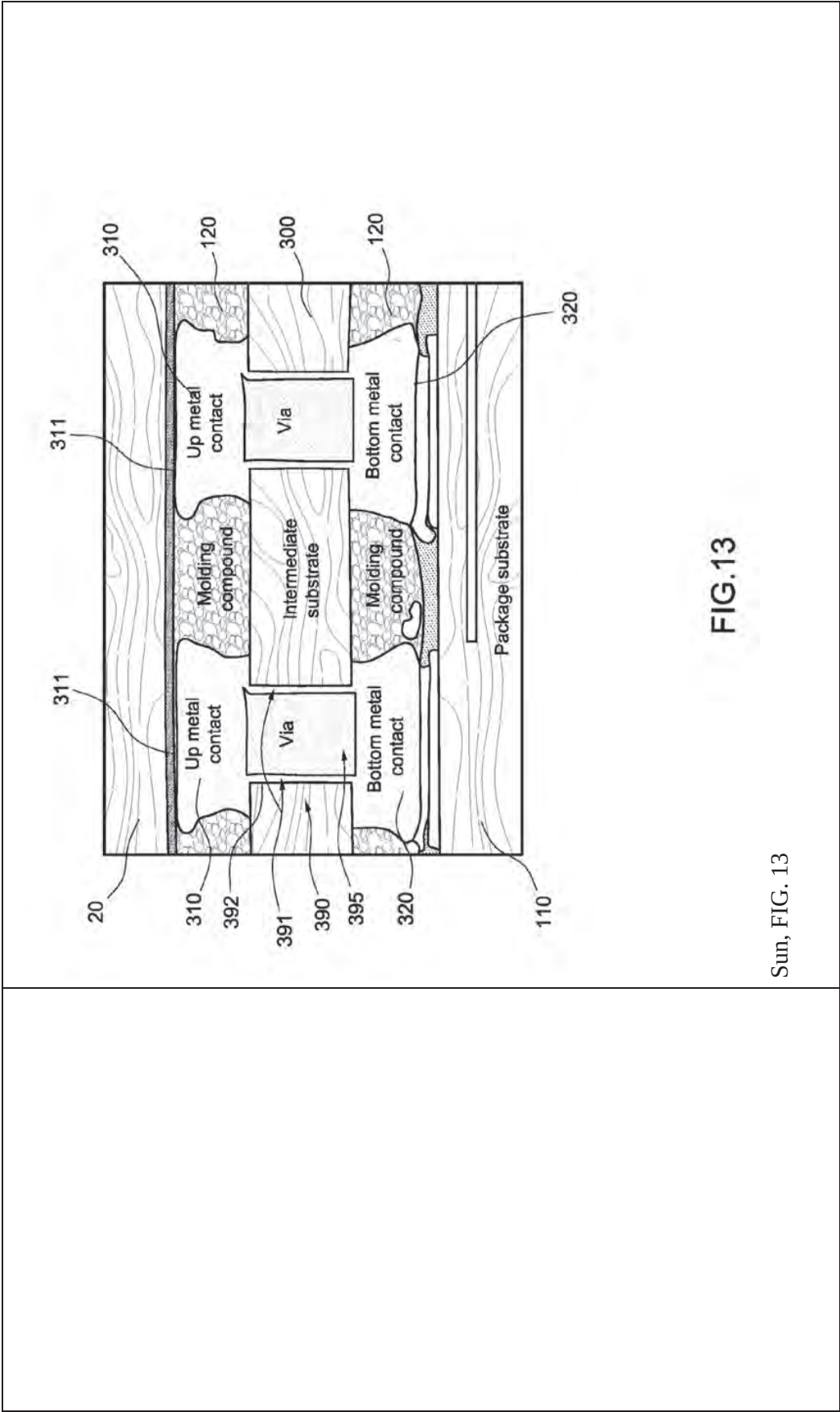
FIG.13

Sun, FIG. 13

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“The vias 390 extend through the second substrate 300. The via has first 391 and second 392 side walls. These side walls 391, 392 may be part of the same (e.g. circular) side wall or may be separate side walls. The via 390 further comprises a core 395 between the side walls and extending between the first and second metal connectors 320, 310.” Sun, [0063].</p> <p>“The core 395 of the via is an insulator. In alternative embodiments the core could instead be made of a conductive material (e.g. metal) or even a void. In still further embodiments the side walls could be an insulator and the core could be made of conductive material (e.g. metal).” Sun, [0064].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Sun discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example</p>

	<p>copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140. The assembly is overmolded with a molding material 120. The molding material covers the chip 200, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed and are level with or extend above the upper surface of the overmold. The upper ends 311 may make contact with an external module. For example an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.” Sun, [0048].</p> <p>“FIG. 13 shows the second substrate and surrounding components in more detail. In particular, it illustrates the vias 390 extending through the second substrate 300. First metal connectors 320 are provided on a second (lower) side of the second substrate 300. These are surrounded by the molding compound 120 and mounted to the first substrate 110. Second metal connectors 320 are provided on the first (upper) side of the second substrate. They are surrounded by the molding compound 120 and have exposed upper ends 311. The second metal connectors 310 are aligned with corresponding second metal connectors 310 on the opposite side of the substrate 300. Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320. The vias 390 extend through the second substrate 300. The via has first 391 and second 392 side walls. These side walls 391, 392 may be part of the same (e.g. circular) side wall or may be separate side walls. The via 390 further comprises a core 395 between the side walls and extending between the first and second metal connectors 320, 310.” Sun, [0062-0063].</p>
--	---



Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“In the illustrated embodiment shown in FIG. 13 the side walls 391, 392 are electrically conductive (e.g. made of metal) and put the first and second metal connectors 320, 310 in electrical contact with each other. The core 395 of the via is an insulator. In alternative embodiments the core could instead by a conductive material (e.g. metal) or even a void. In still further embodiments the side walls could be an insulator and the core could be made of conductive material (e.g. metal).” Sun, [0064].</p> <p>“FIG. 14 (a) illustrates a pair of second connectors 310. They have the same structure as the first connectors 320. They are formed of metal pillars, preferably copper pillars. It can be seen that the pillars have fine pitch and a well defined shape. By way of contrast FIG. 14 (b) shows an arrangement with a pair of solder balls 140 between a substrate 20 and a substrate 300. It can be seen that the solder balls have a less fine pitch and less well defined shape than the metal pillars. Furthermore, at typical processing temperatures (e.g. around 260 degrees Celsius) the solder balls will melt and collapse down, while the metal (e.g. copper) pillars will remain solid and well defined. As a result, for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections. A small amount of solder or bonding pads may used to connect the metal pillars to the respective other substrates.” Sun, [0066].</p>
--	--

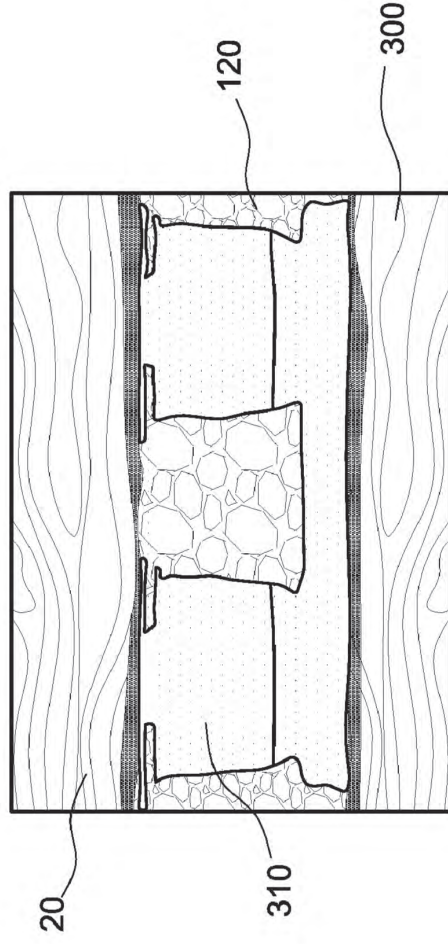


FIG. 14(a)

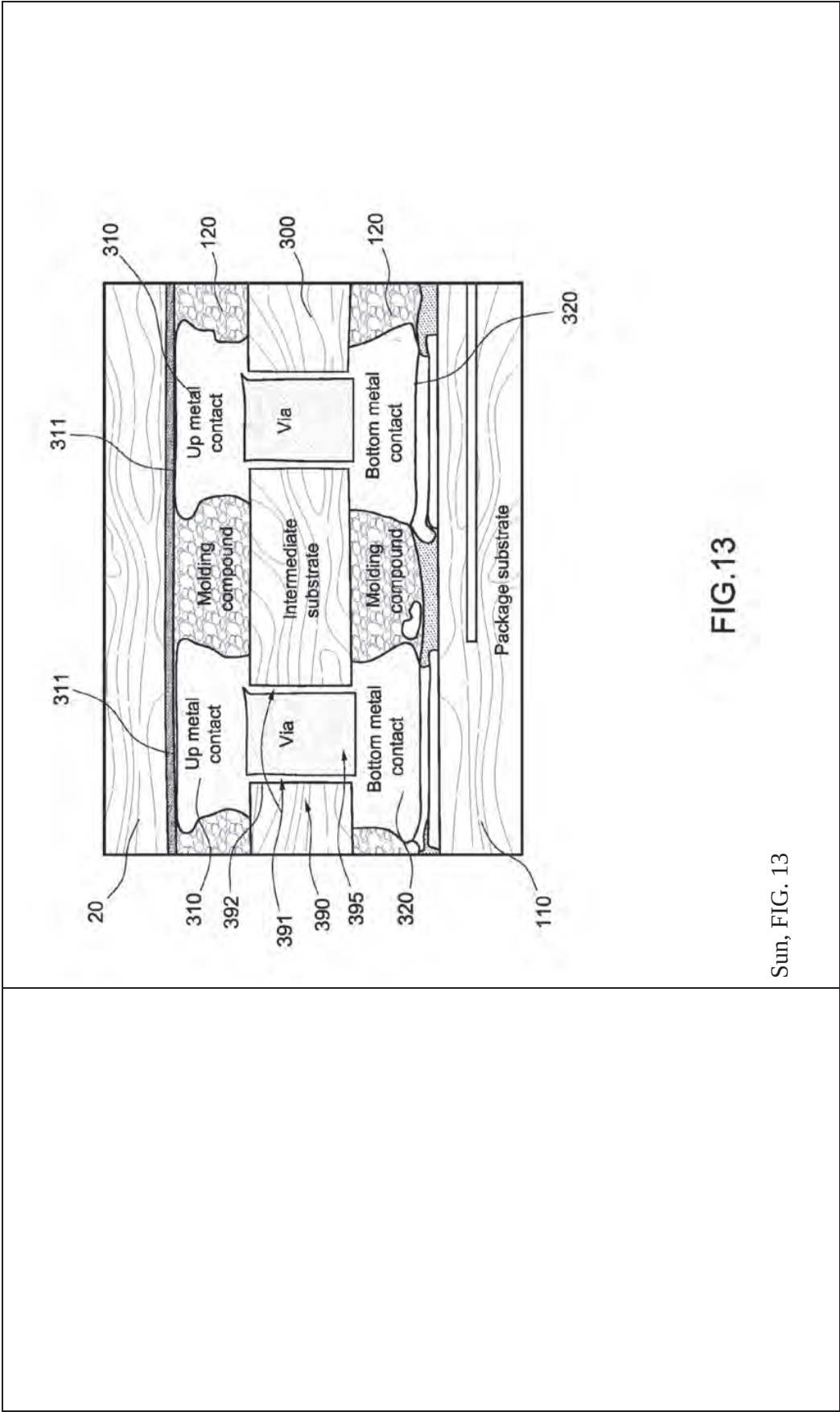
Sun, FIG. 14(a)

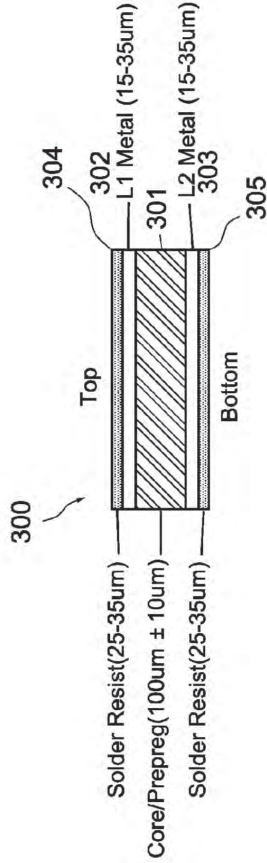
“A second module may then be mounted to the first module shown in FIG. 16 (f) to form a PoP assembly. The second module may be a module 5 as shown in FIG. 12 and described above; it comprises a chip 30 mounted on a third substrate 20. The chip 30 is mounted on the first (upper) side of the third substrate, while electrical contacts (e.g. bonding pads or lands) present on the second (lower) side of the third substrate are placed in contact with the exposed ends of the second electrical connectors 310 of the first module 10.” Sun, [0074].

To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,	<p>Sun discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 13 shows the second substrate and surrounding components in more detail. In particular, it illustrates the vias 390 extending through the second substrate 300. First metal connectors 320 are provided on a second (lower) side of the second substrate 300. These are surrounded by the molding compound 120 and mounted to the first substrate 110. Second metal connectors 320 are provided on the first (upper) side of the second substrate. They are surrounded by the molding compound 120 and have exposed upper ends 311. The second metal connectors 310 are aligned with corresponding second metal connectors 310 on the opposite side of the substrate 300.” Sun, [0062].</p>



	<p>“ias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320. The vias 390 extend through the second substrate 300. The via has first 391 and second 392 side walls. These side walls 391, 392 may be part of the same (e.g. circular) side wall or may be separate side walls. The via 390 further comprises a core 395 between the side walls and extending between the first and second metal connectors 320, 310.” Sun, [0063].</p> <p>“The second substrate 300 in the FIG. 13 embodiment is a simple insulator, e.g. polymer. However, in other embodiments it may be a PCB or it may comprise a plurality of layers. An example is shown in FIG. 15 where the second substrate 300 comprises a core/prepreg insulating layer 301, a metal layer 302, 303 on either side of the core layer and an insulating solder resist layer 304, 305 on either side of the metal layers.” Sun, [0065].</p> <div></div> <p style="text-align: center;">FIG.15</p> <p>Sun, FIG. 15</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	--

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, connector,	<p>Sun discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Preferably there are a plurality of first electrical connectors and a plurality of second electrical connectors. For example, there may be four or more first electrical connectors on the underside of the second substrate and four or more second electrical connectors on the top side of the second substrate. Preferably the first and second electrical connectors are metal pillars, e.g. copper pillars. Preferably the first and second electrical connectors are separate pieces (i.e. not integral parts of the same pillar). Metal pillars allow for fine pitch and maintain their shape at high processing temperatures (e.g. 260° C.), compared to solder joints which melt and break down at such temperatures. However, solder joints may be used to join the metal pillars to a substrate above or below (e.g. to the second substrate and to the first substrate or to a substrate of an external module mounted to the first module).” Sun, [0015].</p> <p>“The vias electrically connect the at least one first electrical connector with the at least one second electrical connector. Preferably the via and the first and second electrical connectors which the via connects are three separate pieces.” Sun, [0017].</p> <p>“The second (lower) side of the third substrate 20 is mounted to the first module 10. Specifically the third substrate is mounted directly to the second connectors 310 of the first module 5. Upper ends of the second connectors 310 connect with a conducting electrical</p>

contacts (not shown) of the second (lower) side of the third substrate 20 in order to allow communication of electrical signals between the two modules.” Sun, [0059].

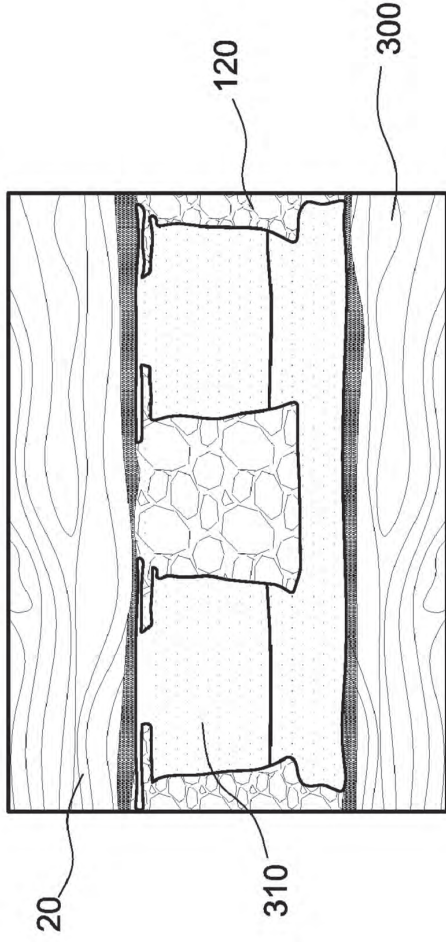


FIG. 14(a)

Sun, FIG. 14(a)

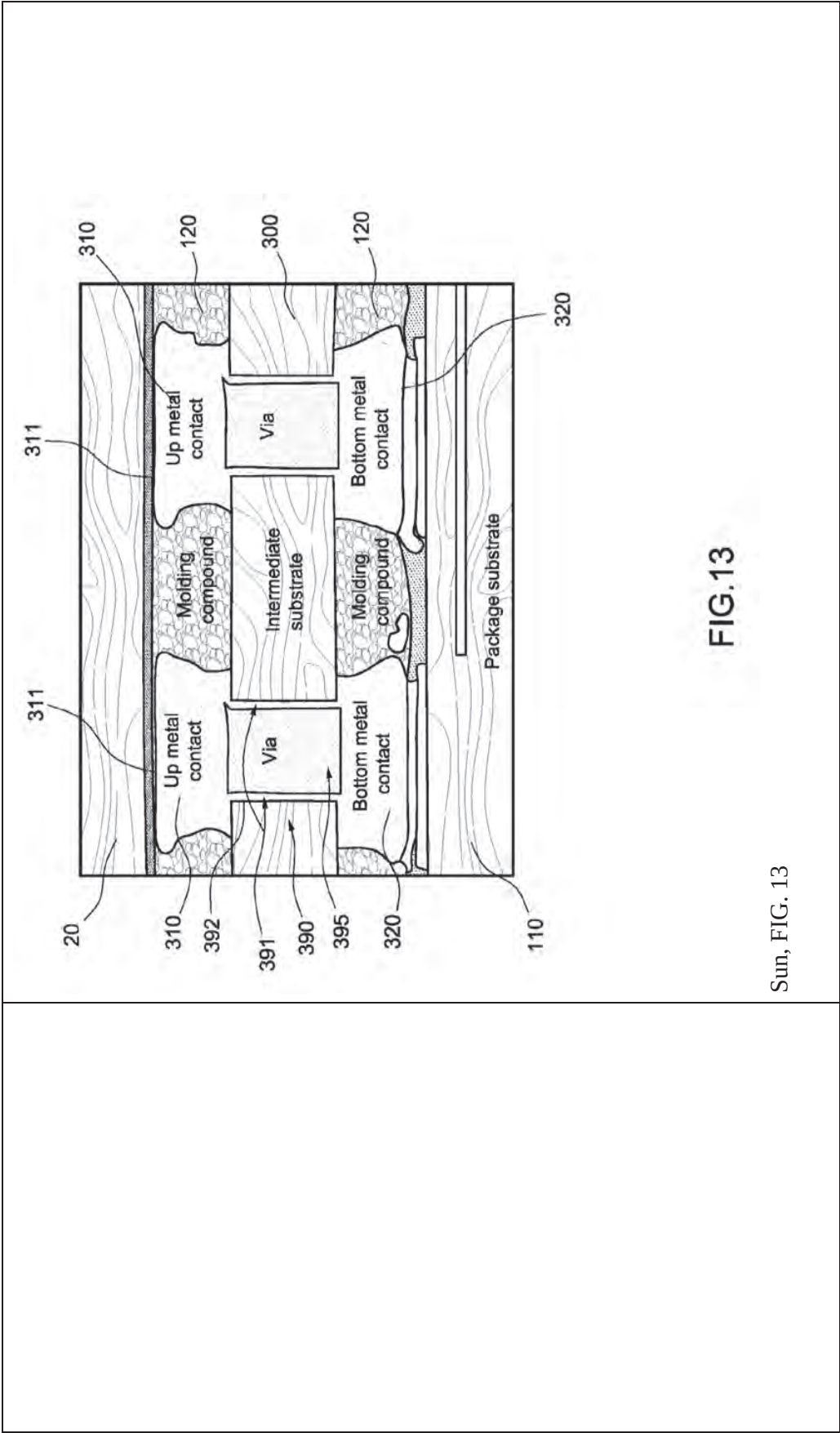
“Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” Sun, [0063].

“The vias 390 extend through the second substrate 300. The via has first 391 and second 392 side walls. These side walls 391, 392 may be part of the same (e.g. circular) side wall or may be separate side walls. The via 390 further comprises a core 395 between the side walls and extending between the first and second metal connectors 320, 310.” Sun, [0063].

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“FIG. 14 (a) illustrates a pair of second connectors 310. They have the same structure as the first connectors 320. They are formed of metal pillars, preferably copper pillars. It can be seen that the pillars have fine pitch and a well defined shape. By way of contrast FIG. 14 (b) shows an arrangement with a pair of solder balls 140 between a substrate 20 and a substrate 300. It can be seen that the solder balls have a less fine pitch and less well defined shape than the metal pillars. Furthermore, at typical processing temperatures (e.g. around 260 degrees Celsius) the solder balls will melt and collapse down, while the metal (e.g. copper) pillars will remain solid and well defined. As a result, for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections. A small amount of solder or bonding pads may be used to connect the metal pillars to the respective other substrates.” Sun, [0066].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Sun discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“Preferably there are a plurality of first electrical connectors and a plurality of second electrical connectors. For example, there may be four or more first electrical connectors on</p>

	<p>the underside of the second substrate and four or more second electrical connectors on the top side of the second substrate. Preferably the first and second electrical connectors are metal pillars, e.g. copper pillars. Preferably the first and second electrical connectors are separate pieces (i.e. not integral parts of the same pillar). Metal pillars allow for fine pitch and maintain their shape at high processing temperatures (e.g. 260° C.), compared to solder joints which melt and break down at such temperatures. However, solder joints may be used to join the metal pillars to a substrate above or below (e.g. to the second substrate and to the first substrate or to a substrate of an external module mounted to the first module).” Sun, [0015].</p> <p>“The vias electrically connect the at least one first electrical connector with the at least one second electrical connector. Preferably the via and the first and second electrical connectors which the via connects are three separate pieces.” Sun, [0017].</p> <p>“The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140.” Sun, [0048].</p>
--	---



Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” Sun, [0063].</p> <p>“The vias 390 extend through the second substrate 300. The via has first 391 and second 392 side walls. These side walls 391, 392 may be part of the same (e.g. circular) side wall or may be separate side walls. The via 390 further comprises a core 395 between the side walls and extending between the first and second metal connectors 320, 310.” Sun, [0063].</p> <p>“FIG. 14 (a) illustrates a pair of second connectors 310. They have the same structure as the first connectors 320. They are formed of metal pillars, preferably copper pillars. It can be seen that the pillars have fine pitch and a well defined shape. By way of contrast FIG. 14 (b) shows an arrangement with a pair of solder balls 140 between a substrate 20 and a substrate 300. It can be seen that the solder balls have a less fine pitch and less well defined shape than the metal pillars. Furthermore, at typical processing temperatures (e.g. around 260 degrees Celsius) the solder balls will melt and collapse down, while the metal (e.g. copper) pillars will remain solid and well defined. As a result, for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections. A small amount of solder or bonding pads may be used to connect the metal pillars to the respective other substrates.” Sun, [0066].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Sun discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“In one aspect of the present invention a (first) module is proposed comprising a first substrate and at least one chip mounted on the first substrate; a second substrate mounted to the first substrate and having an opening in therein; said opening being aligned with said at least one chip on the first substrate; the second substrate being overmolded; the first substrate being electrically connected to the second substrate by at least one first electrical connector; and at least one second electrical connector extending from the second substrate through the overmold and having an exposed end for electrical connection to an external module. Preferably the module is for use in a multi-package assembly. A “multi-package assembly” is an assembly comprising two electronic packages each of which has a chip mounted to a substrate. The module may be used as the lower package in a PoP. A second (upper) module may be mounted to the first module to form the PoP. The second module may make electrical contact with the exposed end(s) of the second electrical connector(s) in order to enable communication between the two modules or packages.” Sun, [0012-0013].</p> <p>“Preferably there are a plurality of first electrical connectors and a plurality of second electrical connectors. For example, there may be four or more first electrical connectors on the underside of the second substrate and four or more second electrical connectors on the top side of the second substrate. Preferably the first and second electrical connectors are metal pillars, e.g. copper pillars. Preferably the first and second electrical connectors are separate pieces (i.e. not integral parts of the same pillar). Metal pillars allow for fine pitch and maintain</p>
--	---

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>their shape at high processing temperatures (e.g. 260° C.), compared to solder joints which melt and break down at such temperatures. However, solder joints may be used to join the metal pillars to a substrate above or below (e.g. to the second substrate and to the first substrate or to a substrate of an external module mounted to the first module).” Sun, [0015].</p> <p>“One or more vias preferably extend through said second substrate. The vias electrically connect the at least one first electrical connector with the at least one second electrical connector. Preferably the via and the first and second electrical connectors which the via connects are three separate pieces.” Sun, [0017].</p> <p>“FIG. 13 shows the second substrate and surrounding components in more detail. In particular, it illustrates the vias 390 extending through the second substrate 300. First metal connectors 320 are provided on a second (lower) side of the second substrate 300. These are surrounded by the molding compound 120 and mounted to the first substrate 110. Second metal connectors 320 are provided on the first (upper) side of the second substrate. They are surrounded by the molding compound 120 and have exposed upper ends 311. The second metal connectors 310 are aligned with corresponding second metal connectors 310 on the opposite side of the substrate 300. Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” Sun, [0062-0063].</p>
--	---

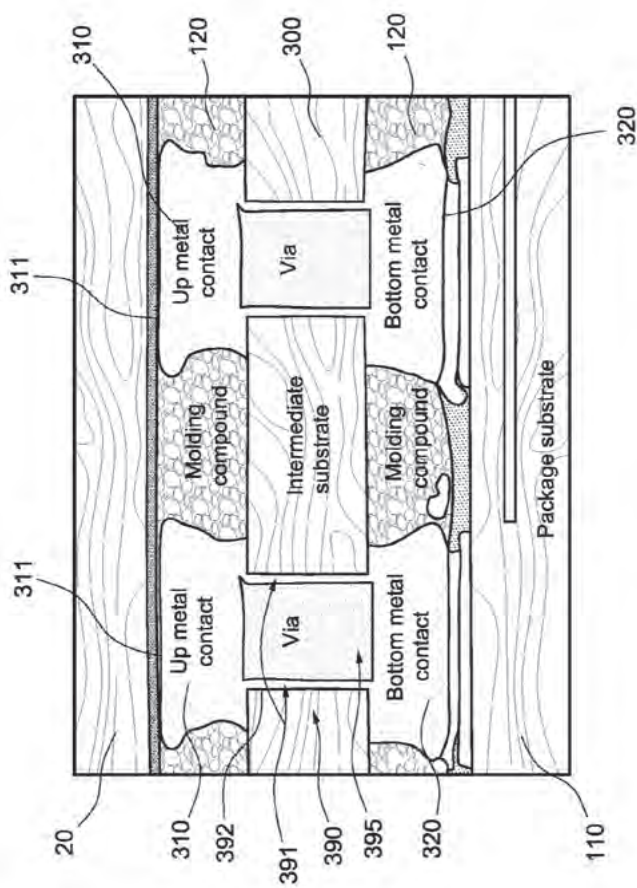


FIG.13

Sun, FIG. 13

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“A second module may then be mounted to the first module shown in FIG. 16 (f) to form a PoP assembly. The second module may be a module 5 as shown in FIG. 12 and described above; it comprises a chip 30 mounted on a third substrate 20. The chip 30 is mounted on the first (upper) side of the third substrate, while electrical contacts (e.g. bonding pads or lands) present on the second (lower) side of the third substrate are placed in contact with the exposed ends of the second electrical connectors 310 of the first module 10.” Sun, [0074].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Sun discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“A chip 200, which may be a memory chip or a processor, is mounted to the first substrate 100. It may be mounted by any appropriate method, for example die attachment with wire bonding, flip chip etc. Wires 220 connect a bonding pad 210 on top of the chip 200 with a bonding pad 240 on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200.” Sun, [0047-0048].</p>

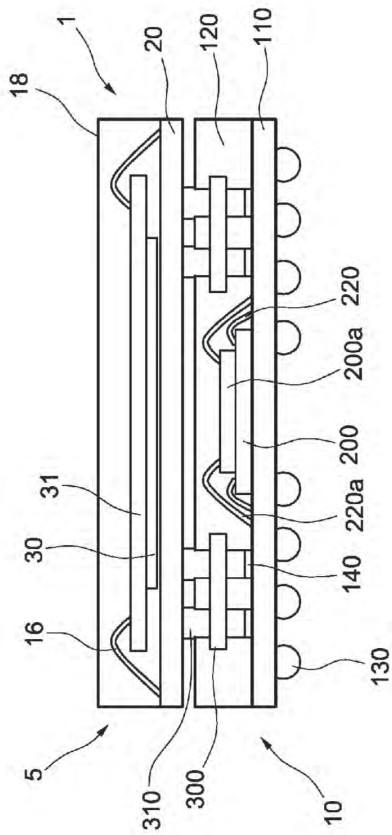


FIG.12

Sun, FIG. 12

“This embodiment has two chips 500 (a) and 500 (b) stacked one on top of the other. The first chip 500 (a) is mounted to the first substrate 110 by any suitable means. The second chip 500 (b) is mounted on top of the first chip 500 (a) and spaced apart from the first chip by a spacer 530. Wires 520 connect bonding pads on the chips 500 (a), 500 (b) to bonding pads on the first substrate 110. The molding material 120 covers both the first and second chips.” Sun, [0049].

“FIG. 4 is a third embodiment similar to the first two embodiments. It has two chips 810 and 820 mounted side by side on the first substrate 110. The overmolding material covers both the first and second chips 810, 820.” Sun, [0050].

	<p>“FIG. 5 shows a fourth embodiment similar to the first embodiment. The chip 800 is mounted on the first substrate 110. A wire 920 connects the chip 800 and the second substrate 300. The molding material covers the chip 800 and the first and second substrates 110, 300.” Sun, [0051].</p> <p>“FIG. 12 is a schematic diagram of a PoP assembly 1 comprising a second module 5 mounted on a first module 10. The first module 5 is a module of the type described above, e.g. with reference to FIG. 2. It forms a lower module of the PoP assembly. In this example, it has two chips 200, 200 a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220 a respectively. Both chips are processors. Other embodiments could have a different number or type of chips and different method of connecting the chips to the substrate 110. The upper module 5 comprises a pair of chips 30, 31 mounted to a first (upper) side of a third substrate 20. The third substrate may be a PCB, preferably a BT core substrate. The chips 30, 31 are electrically connected to the third substrate 20 by wires 16 or any other suitable means. Preferably the chips 30 and 31 are memory chips. The second module 5 is overmolded with a molding material 18 which covers the chips 30, 31 and the third substrate 20. The second (lower) side of the third substrate 20 is mounted to the first module 10. Specifically the third substrate is mounted directly to the second connectors 310 of the first module 5.” Sun, [0058-0059].</p> <p>“The first module 1 will now be described in more detail. It comprises a first substrate 110 which may be a PCB, preferably a BT core substrate. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A pair of chips 200, 200 a may be memory chips or a processor, are mounted to the first substrate 110. They may be mounted by any appropriate method, for example wire bonding, die attachment etc. Wires 220, 220 a connect a bonding</p>
--	--

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>pad on top of the chip 200 with a bonding pad on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chips 200, 200 a.” Sun, [0060-0061].</p> <p>“The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding 140. The first module 10 is overmolded with a molding material 120. The molding material covers the chips 200, 200 a, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed above the overmold 120. The upper ends 311 make contact with electrical contacts of the second module 5.” Sun, [0061].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Sun discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

“A chip 200, which may be a memory chip or a processor, is mounted to the first substrate 100. It may be mounted by any appropriate method, for example die attachment with wire bonding, flip chip etc. Wires 220 connect a bonding pad 210 on top of the chip 200 with a bonding pad 240 on the upper side of the first substrate 110.” Sun, [0047].

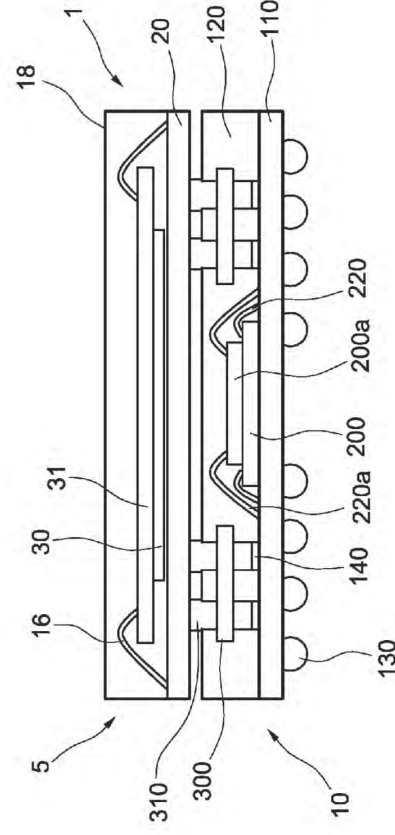


FIG. 12

Sun, FIG. 12

“FIG. 3 shows another embodiment of the first module, similar to FIG. 2. Like reference numerals are used to describe like parts and will not be described again. This embodiment has two chips 500 (a) and 500 (b) stacked one on top of the other. The first chip 500 (a) is mounted to the first substrate 110 by any suitable means.” Sun, [0048-0049].

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“FIG. 4 is a third embodiment similar to the first two embodiments. It has two chips 810 and 820 mounted side by side on the first substrate 110.” Sun, [0050].</p> <p>“FIG. 5 shows a fourth embodiment similar to the first embodiment. The chip 800 is mounted on the first substrate 110.” Sun, [0051].</p> <p>“FIG. 12 is a schematic diagram of a PoP assembly 1 comprising a second module 5 mounted on a first module 10. The first module 5 is a module of the type described above, e.g. with reference to FIG. 2. It forms a lower module of the PoP assembly. In this example, it has two chips 200, 200 a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220 a respectively.” Sun, [0058].</p> <p>“The first module 1 will now be described in more detail. It comprises a first substrate 110 which may be a PCB, preferably a BT core substrate. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A pair of chips 200, 200 a may be memory chips or a processor, are mounted to the first substrate 110. They may be mounted by any appropriate method, for example wire bonding, die attachment etc. Wires 220, 220 a connect a bonding pad on top of the chip 200 with a bonding pad on the upper side of the first substrate 110.” Sun, [0060].</p> <p>“In a third step, shown in FIG. 16 (c), one or more chips 200, 200 a are mounted to the first substrate via the space provided by the opening in the second substrate.” Sun, [0070].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	---

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.	<p>Sun discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“As the lower module has a second substrate with electrical connectors on either side, the stand off height may be increased. Further, the opening in the second substrate makes room for one or more chips mounted to the first substrate. Overmolded means that molding material covers the second substrate. As the ‘intermediate’ second substrate and the second connectors are overmolded, the assembly is less prone to warpage. Preferably the at least one chip is overmolded. Preferably the first substrate is overmolded. Preferably the overmold extends over the first substrate at least as far as the second substrate; more preferably the whole of the first substrate is overmolded. The assembly is also relatively cheap to manufacture compared to other arrangements which require laser drilling or other complex machinery.”</p> <p>Sun, [0014].</p> <p>“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chips 200, 200 a. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding 140. The first module 10 is overmolded</p>

	<p>with a molding material 120. The molding material covers the chips 200, 200 a, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed above the overmold 120. The upper ends 311 make contact with electrical contacts of the second module 5.” Sun, [0048].</p> <p>“FIG. 9 shows yet another arrangement in which the second substrate 300 is rectangular and has a rectangular opening 340 in the middle. Second connectors 310 are provided in a line on each side and corresponding first connectors (not shown) are provided on the opposite face of the substrate. Each side has a gap 350. The gaps 350 are of different shapes and join the central opening 340.” Sun, [0055].</p> <p>“FIG. 12 is a schematic diagram of a PoP assembly 1 comprising a second module 5 mounted on a first module 10. The first module 5 is a module of the type described above, e.g. with reference to FIG. 2. It forms a lower module of the PoP assembly. In this example, it has two chips 200, 200 a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220 a respectively. Both chips are processors. Other embodiments could have a different number or type of chips and different method of connecting the chips to the substrate 110.” Sun, [0058].</p>
--	---

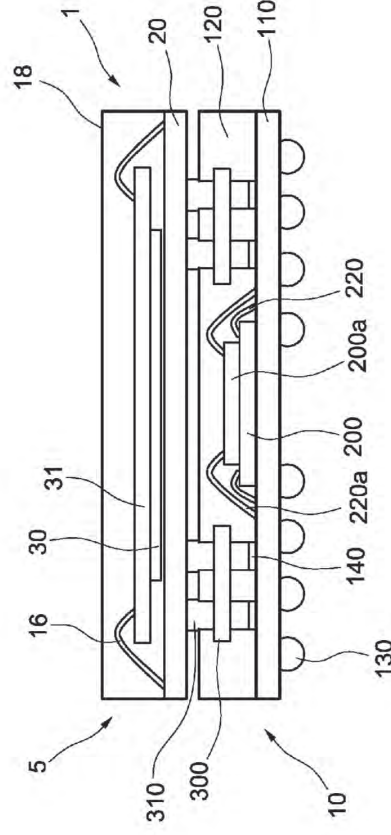


FIG. 12

Sun, FIG. 12

“The upper module 5 comprises a pair of chips 30, 31 mounted to a first (upper) side of a third substrate 20. The third substrate may be a PCB, preferably a BT core substrate. The chips 30, 31 are electrically connected to the third substrate 20 by wires 16 or any other suitable means. Preferably the chips 30 and 31 are memory chips. The second module 5 is overmolded with a molding material 18 which covers the chips 30, 31 and the third substrate 20. The second (lower) side of the third substrate 20 is mounted to the first module 10. Specifically the third substrate is mounted directly to the second connectors 310 of the first module 5. Upper ends of the second connectors 310 connect with a conducting electrical contacts (not shown) of the second (lower) side of the third substrate 20 in order to allow communication of electrical signals between the two modules. While FIG. 12 shows a gap

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>between the first and second modules, in other embodiments the overmold 120 of the first module may extend flush with the upper ends of the second connectors and the third substrate 20 of the second module 5 may rest on the overmold 120 of the first module. That is the third substrate 20 may be in direct contact with the overmold 120. In this embodiment there are no intervening PCBs or other electric circuits or insulators between the overmold 120 and second connectors 310 and the third substrate 20 of the second module 5. In this embodiment the two chips 31, 30 are memory chips, but in other embodiments they may be different types of chips (e.g. processors).” Sun, [0059].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Sun discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Secondly, the space between the upper and lower packages is limited. It would be desirable to increase the vertical separation (stand off height) in order to make room for more and larger chips and enable stacking of chips on the lower substrate.” Sun, [0010].</p>

	<p>“As the lower module has a second substrate with electrical connectors on either side, the stand off height may be increased. Further, the opening in the second substrate makes room for one or more chips mounted to the first substrate. Overmolded means that molding material covers the second substrate. As the ‘intermediate’ second substrate and the second connectors are overmolded, the assembly is less prone to warpage. Preferably the at least one chip is overmolded. Preferably the first substrate is overmolded. Preferably the overmold extends over the first substrate at least as far as the second substrate; more preferably the whole of the first substrate is overmolded. The assembly is also relatively cheap to manufacture compared to other arrangements which require laser drilling or other complex machinery.” Sun, [0014].</p> <p>“A chip 200, which may be a memory chip or a processor, is mounted to the first substrate 100. It may be mounted by any appropriate method, for example die attachment with wire bonding, flip chip etc. Wires 220 connect a bonding pad 210 on top of the chip 200 with a bonding pad 240 on the upper side of the first substrate 110.” Sun, [0047].</p> <p>“FIG. 12 is a schematic diagram of a PoP assembly 1 comprising a second module 5 mounted on a first module 10. The first module 5 is a module of the type described above, e.g. with reference to FIG. 2. It forms a lower module of the PoP assembly. In this example, it has two chips 200, 200 a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220 a respectively. Both chips are processors. Other embodiments could have a different number or type of chips and different method of connecting the chips to the substrate 110.” Sun, [0058].</p>
--	---

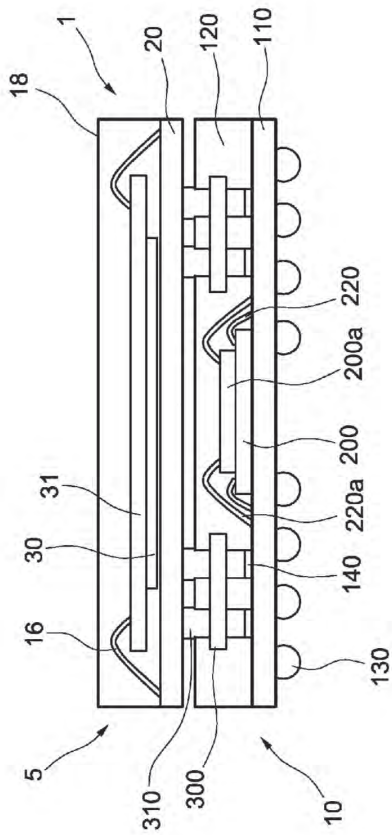


FIG.12

Sun, FIG. 12

“The first module 1 will now be described in more detail. It comprises a first substrate 110 which may be a PCB, preferably a BT core substrate. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A pair of chips 200, 200 a may be memory chips or a processor, are mounted to the first substrate 110. They may be mounted by any appropriate method, for example wire bonding, die attachment etc. Wires 220, 220 a connect a bonding pad on top of the chip 200 with a bonding pad on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chips 200, 200 a. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding 140. The first module 10 is overmolded with a molding material 120. The molding material covers the chips 200, 200 a, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed above the overmold 120. The upper ends 311 make contact with electrical contacts of the second module 5.” Sun, [0060-0061].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	Sun discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

<p>bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p><i>See, e.g.:</i></p> <p>“The top package in FIG. 1 has a substrate 20. Typically the substrate will be a BT core substrate. A pair of chips 30, 31 are mounted to the substrate 20. Wires 16, 18 connect the chips 30, 31 to electrical contacts 11 of the substrate 20. The top package is covered with a molding compound 30 (over molded). This strengthens the assembly and helps to protect the components from damage. The lower package 10 also comprises a substrate 40 and a chip 50 mounted to the substrate. The chip 50 is connected to electrical contacts 41 of the substrate by wires 45. An overmold 60 covers the chip 50 and a surrounding part of the substrate on which the chip is mounted. The top package 5 is mounted to the bottom package 10 by solder balls 70. The solder balls 70 space the two packages apart allowing room for the chip 50 of the lower package. The solder balls 70 connect with electrical contacts on the lower side of the substrate 20 and electrical contacts on the upper surface of the substrate 40. This allows electrical signals to be passed between the upper and lower packages.” Sun, [0005-0007].</p> <p>“FIG. 2 shows a module 100 for use in a multichip package. In particular a module for use in the lower part of a PoP assembly. It comprises a first substrate 110 which maybe a PCB, preferably a BT core substrate. A (bismaleimide triazine) core substrate, is a substrate comprising a BT core layer with a metal layer on either side. BT has the advantage that it is a polyimide with higher thermal stability, better chemical resistance and mechanical properties compared to the epoxy resin used in same other types of PCB. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A chip 200, which may be a memory chip or a processor, is mounted to the first substrate 100. It may be mounted by any appropriate method, for example die attachment with wire bonding, flip chip etc. Wires 220 connect a bonding pad 210 on top of the chip 200 with a bonding pad 240 on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The</p>
---	--

	<p>second substrate has an opening therein for accommodating the chip 200. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140. The assembly is overmolded with a molding material 120. The molding material covers the chip 200, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed and are level with or extend above the upper surface of the overmold. The upper ends 311 may make contact with an external module. For example an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.” Sun, [0047-0048].</p> <p>“FIG. 4 is a third embodiment similar to the first two embodiments. It has two chips 810 and 820 mounted side by side on the first substrate 110. The overmolding material covers both the first and second chips 810, 820.” Sun, [0050].</p> <p>“FIG. 8 is a plan view of another arrangement. A double row of second connectors 310 is provided on each side of the rectangular second substrate 300, surrounding the opening 330. First connectors are provided at corresponding locations on the other side. Further, there is an electronic device 340 mounted on top of the second substrate on the same side as the second connectors. The electronic device 340 could be, for example, a capacitor, resistor or active component.” Sun, [0054].</p>
--	--

	<p>“The first module 5 is a module of the type described above, e.g. with reference to FIG. 2. It forms a lower module of the PoP assembly. In this example, it has two chips 200, 200 a stacked one on top of the other and connected to a first substrate 110 by wires 220 and 220 a respectively. Both chips are processors. Other embodiments could have a different number or type of chips and different method of connecting the chips to the substrate 110. The upper module 5 comprises a pair of chips 30, 31 mounted to a first (upper) side of a third substrate 20. The third substrate may be a PCB, preferably a BT core substrate. The chips 30, 31 are electrically connected to the third substrate 20 by wires 16 or any other suitable means. Preferably the chips 30 and 31 are memory chips. The second module 5 is overmolded with a molding material 18 which covers the chips 30, 31 and the third substrate 20. The second (lower) side of the third substrate 20 is mounted to the first module 10. Specifically the third substrate is mounted directly to the second connectors 310 of the first module 5.” Sun, [0058-0059].</p>
--	--

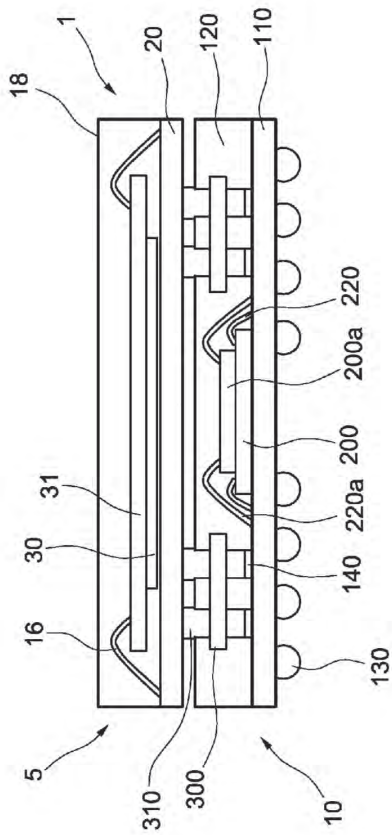


FIG.12

Sun, FIG. 12

“In this embodiment there are no intervening PCBs or other electric circuits or insulators between the overmold 120 and second connectors 310 and the third substrate 20 of the second module 5. In this embodiment the two chips 31, 30 are memory chips, but in other embodiments they may be different types of chips (e.g. processors). The first module 1 will now be described in more detail. It comprises a first substrate 110 which may be a PCB, preferably a BT core substrate. Solder balls 130 are provided on the lower side of the first substrate 110 to enable the module 100 to be mounted to an external apparatus, such as a motherboard. A pair of chips 200, 200 a may be memory chips or a processor, are mounted to the first substrate 110. They may be mounted by any appropriate method, for example wire bonding, die attachment etc. Wires 220, 220 a connect a bonding pad on top of the chip 200

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>with a bonding pad on the upper side of the first substrate 110. A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chips 200, 200 a. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding 140. The first module 10 is overmolded with a molding material 120. The molding material covers the chips 200, 200 a, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed above the overmold 120. The upper ends 311 make contact with electrical contacts of the second module 5.” Sun, [0059-0061].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of	Sun discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.	<p>among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The vias electrically connect the at least one first electrical connector with the at least one second electrical connector. Preferably the via and the first and second electrical connectors which the via connects are three separate pieces.” Sun, [0017].</p> <p>“The second metal connectors 310 are aligned with corresponding second metal connectors 310 on the opposite side of the substrate 300. Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” Sun, [0062-0063].</p>
--	---

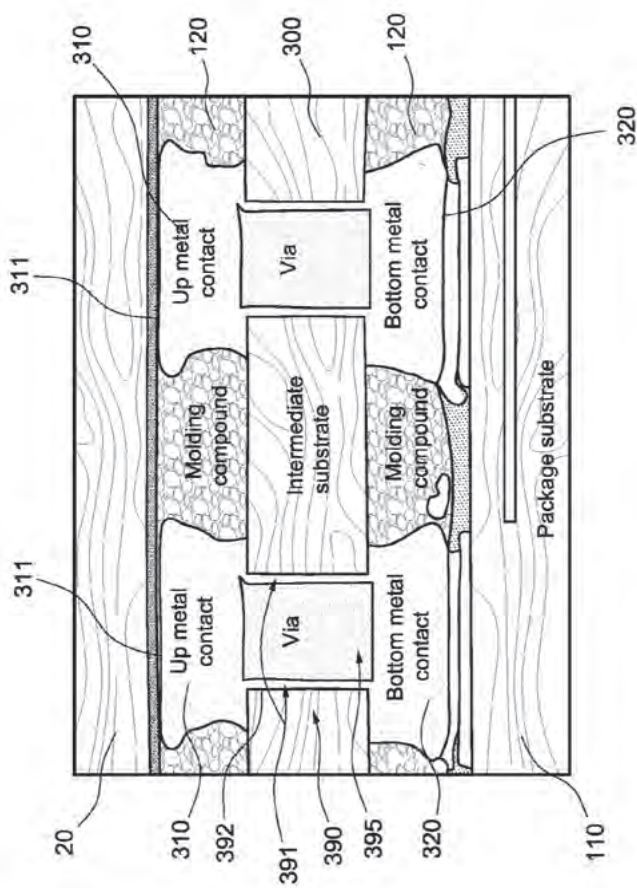


FIG.13

Sun, FIG. 13

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“FIG. 13 shows the second substrate and surrounding components in more detail. In particular, it illustrates the vias 390 extending through the second substrate 300. First metal connectors 320 are provided on a second (lower) side of the second substrate 300. These are surrounded by the molding compound 120 and mounted to the first substrate 110. Second metal connectors 320 are provided on the first (upper) side of the second substrate. They are surrounded by the molding compound 120 and have exposed upper ends 311.” Sun, [0062].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Sun discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

<p>pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>“FIG. 13 shows the second substrate and surrounding components in more detail. In particular, it illustrates the vias 390 extending through the second substrate 300. First metal connectors 320 are provided on a second (lower) side of the second substrate 300. These are surrounded by the molding compound 120 and mounted to the first substrate 110. Second metal connectors 320 are provided on the first (upper) side of the second substrate. They are surrounded by the molding compound 120 and have exposed upper ends 311. The second metal connectors 310 are aligned with corresponding second metal connectors 310 on the opposite side of the substrate 300. Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320. The vias 390 extend through the second substrate 300. The via has first 391 and second 392 side walls. These side walls 391, 392 may be part of the same (e.g. circular) side wall or may be separate side walls. The via 390 further comprises a core 395 between the side walls and extending between the first and second metal connectors 320, 310. In the illustrated embodiment shown in FIG. 13 the side walls 391, 392 are electrically conductive (e.g. made of metal) and put the first and second metal connectors 320, 310 in electrical contact with each other.” Sun, [0062-0064].</p>
---	---

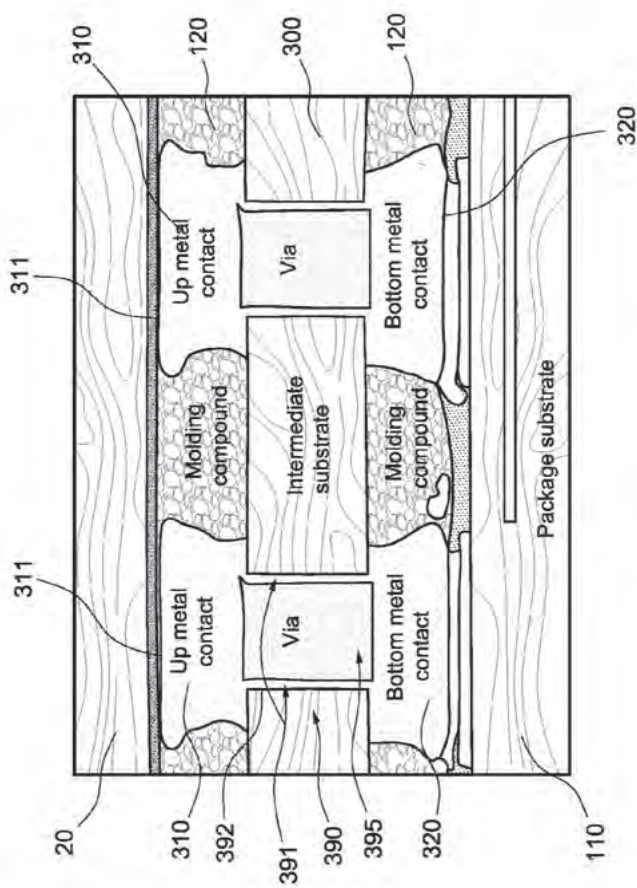


FIG.13

Sun, FIG. 13

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>“The core 395 of the via is an insulator. In alternative embodiments the core could instead by a conductive material (e.g. metal) or even a void. In still further embodiments the side walls could be an insulator and the core could be made of conductive material (e.g. metal).” Sun, [0064].</p> <p>“The metal pillars allow finer pitch and thus denser electrical connections. A small amount of solder or bonding pads may used to connect the metal pillars to the respective other substrates.” Sun, [0066].</p> <p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom end of a corresponding metal pillar among the plurality of metal pillars, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	Sun discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

<p>ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p><i>See, e.g.:</i></p> <p>“A second substrate 300 is mounted to the first substrate 110. The second substrate has an opening therein for accommodating the chip 200. The second substrate 300 has a plurality of first connectors 320 for connecting the substrate electrically with the first substrate 110. The first connectors are provided on a first (underside) of the second substrate. A plurality of second connectors 310 are provided on the second (upper surface) of the second substrate 300. The first and second connectors preferably take the form of metal pillars, for example copper pillars. The first connectors may be electrically connected to the electrical contacts of the first substrate 110 by solder bonding or intermetallic bonding) 140. The assembly is overmolded with a molding material 120. The molding material covers the chip 200, the upper surface of the first substrate 110 and the second substrate 300. This overmolding helps to provide solidity and stability to the assembly and minimizes the occurrence of warping. Upper ends 311 of the second connectors 310 are exposed and are level with or extend above the upper surface of the overmold. The upper ends 311 may make contact with an external module. For example an upper PoP module may be mounted on top of the first module 110 and make electrical contact via the second connectors 311.” Sun, [0048].</p> <p>“FIG. 13 shows the second substrate and surrounding components in more detail. In particular, it illustrates the vias 390 extending through the second substrate 300. First metal connectors 320 are provided on a second (lower) side of the second substrate 300. These are surrounded by the molding compound 120 and mounted to the first substrate 110. Second metal connectors 320 are provided on the first (upper) side of the second substrate. They are surrounded by the molding compound 120 and have exposed upper ends 311. The second metal connectors 310 are aligned with corresponding second metal connectors 310 on the</p>
--	---

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	opposite side of the substrate 300. Vias 390 electrically connect each second metal connector 310 with a corresponding first metal connector 320.” Sun, [0062-0063].
--	--

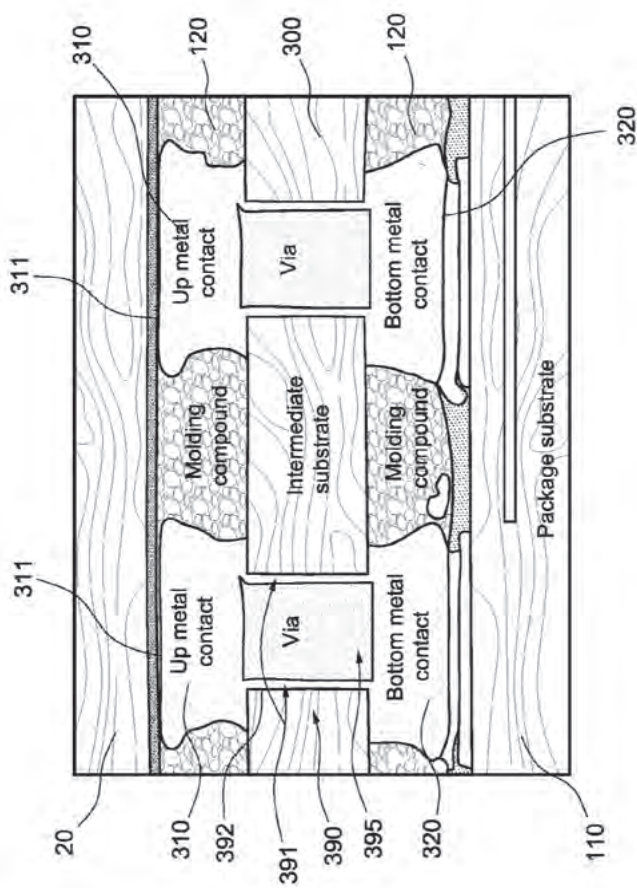


FIG.13

Sun, FIG. 13

	<p>“In the illustrated embodiment shown in FIG. 13 the side walls 391, 392 are electrically conductive (e.g. made of metal) and put the first and second metal connectors 320, 310 in electrical contact with each other. The core 395 of the via is an insulator. In alternative embodiments the core could instead by a conductive material (e.g. metal) or even a void. In still further embodiments the side walls could be an insulator and the core could be made of conductive material (e.g. metal).” Sun, [0064].</p> <p>“FIG. 14 (a) illustrates a pair of second connectors 310. They have the same structure as the first connectors 320. They are formed of metal pillars, preferably copper pillars. It can be seen that the pillars have fine pitch and a well defined shape. By way of contrast FIG. 14 (b) shows an arrangement with a pair of solder balls 140 between a substrate 20 and a substrate 300. It can be seen that the solder balls have a less fine pitch and less well defined shape than the metal pillars. Furthermore, at typical processing temperatures (e.g. around 260 degrees Celsius) the solder balls will melt and collapse down, while the metal (e.g. copper) pillars will remain solid and well defined. As a result, for a given stand off height, metal pillars provide a superior solution to solder balls for connecting the upper and lower surfaces of the second substrate to respective other substrates. The metal pillars allow finer pitch and thus denser electrical connections. A small amount of solder or bonding pads may be used to connect the metal pillars to the respective other substrates.” Sun, [0066].</p> <p>“A second module may then be mounted to the first module shown in FIG. 16 (f) to form a PoP assembly. The second module may be a module 5 as shown in FIG. 12 and described above; it comprises a chip 30 mounted on a third substrate 20. The chip 30 is mounted on the first (upper) side of the third substrate, while electrical contacts (e.g. bonding pads or lands) present on the second (lower) side of the third substrate are placed in contact with the exposed ends of the second electrical connectors 310 of the first module 10.” Sun, [0074].</p>
--	---

Appendix A-31 - Invalidity of U.S. Patent No. 9859202 in view of Sun - U.S. Patent Publication No. 20110147908

	<p>To the extent Plaintiff contends that Sun fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

U.S. Patent Publication No. 20120139010 (“Takeda”) is titled Interposer and Semiconductor Device and lists Tsutomu Takeda as inventor. Takeda anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Takeda is a U.S. patent publication that was filed December 5, 2011 and published June 7, 2012. Takeda claims priority to JP 2010-270079 filed on December 3, 2010. Takeda is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Takeda, or otherwise rendered obvious by disclosures and teachings of Takeda, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Takeda does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Takeda with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Takeda, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

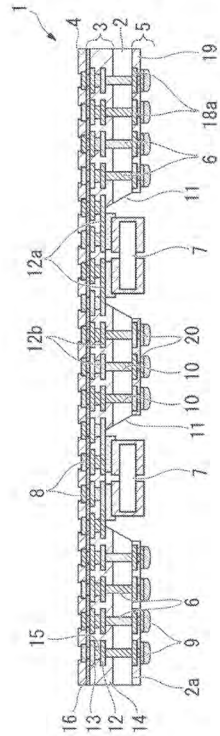
Where the chart below states that Takeda “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Takeda or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Takeda set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Takeda discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“The interposer 1 indicated in FIG. 1 includes a silicon substrate 2, a multilayer wiring portion 3, and an encapsulant resin 4 formed on one side surface of the silicon substrate 2, a bump forming portion 5 provided on another side surface of the silicon substrate 2, penetrating electrodes 6 that penetrate the silicon substrate 2 in the thickness direction, and capacitors (electronic parts for mounting) 7 provided in a cavity 11 of the silicon substrate 2.” Takeda, [0035].</p>

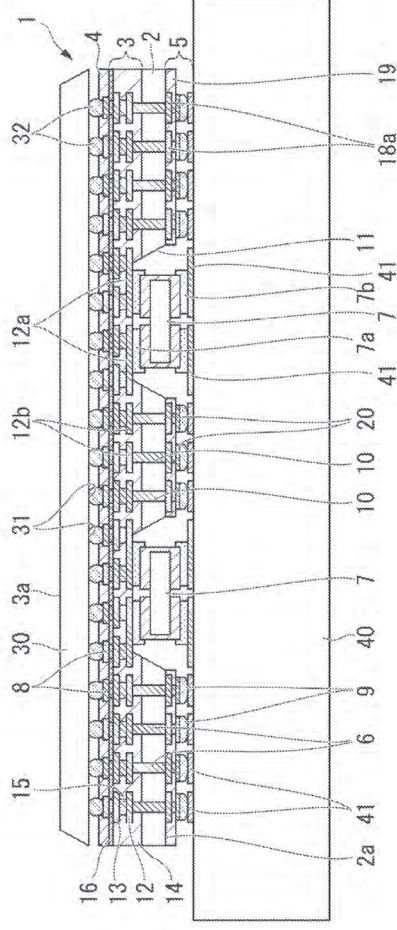
FIG. 1



Takeda, FIG. 1

“As shown in FIG. 2, with respect to the interposer 1, each first UBM structure 8 is formed on the multilayer wiring portion 3 to which each connection portion 31 of the electronic part (mounting electronic part) 30 is electrically connected via a bump 32. In this way, the electronic part 30 is mounted on the interposer 1.” Takeda, [0035].

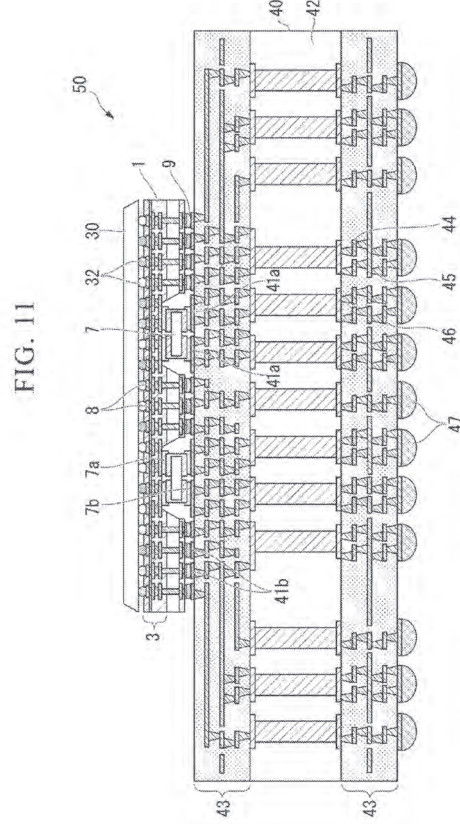
FIG. 2



Takeda, FIG 2.

“The first wiring layer 12 is formed with a predetermined pattern on the silicon substrate 2. The second wiring layer 13 is formed on the first wiring layer 12 with a predetermined pattern. In the present invention, the first wiring layer 12 includes pad-ports 12 a formed on areas which correspond to the cavity portions 11, in which the pad portions 12 a are electrically connected to the capacitors 7. The pad portions 12 a are electrically connected to the first UBM structures 8 via the first wiring layer 12, the via electrodes 15, and the second wiring layer 13, where the first UBM structures 8 respectively correspond to pins (power supply connections) and ground pins (ground connections) of the electronic part 30. Therefore, with reference to the interposer 1, the capacitors 7 are connected to the pad portions 12 a with the electronic part 30 being mounted on the interposer 1. The capacitors 7 are electrically connected to the power supply pins and ground pins via each of the above

	<p>parts. In descriptions below, other pads excluding the pad portions 12 a of the first wiring layer 12 will be referred to as wiring 12.” Takeda, [0040].</p> <p>“The bump 9 is a conductive terminal with a round shape, and formed of a low melting point metal such as solder. The bump 9 is provided on each of the second UBM structures 20 (e.g., on the conductive portion 20 d). The interposer 1 is mounted on the wiring substrate 40 by connecting each bump 9 with each pad portion 41 b of the wiring substrate 40.” Takeda, [0065].</p> <p>“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].</p>
--	--



Takeda, FIG. 11

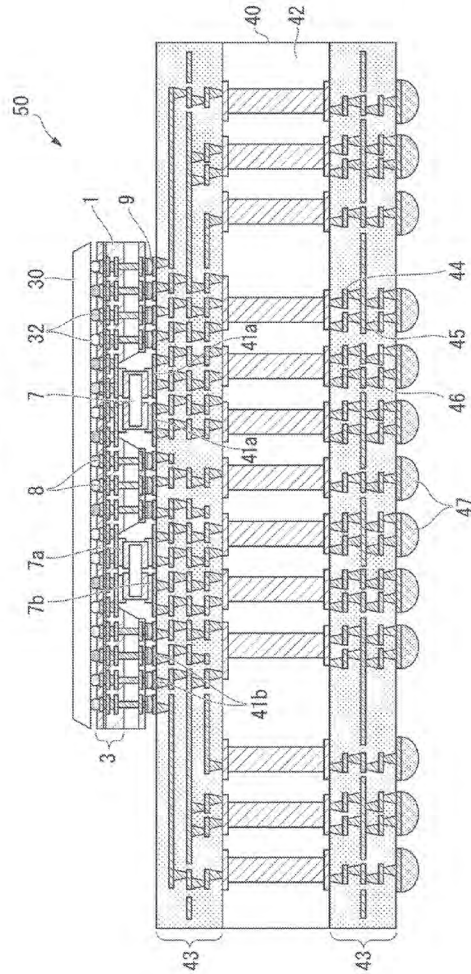
“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41 a and 41 b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].

“The bumps 9 of the interposer 1 are respectively connected to the pad portions 41 b, and the connecting terminals 7 b are respectively connected to pad portions 41 a of the wiring

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

	<p>substrate 40. In this way, the interposer 1 is mounted on the wiring substrate 40.” Takeda, [0153].</p> <p>“As the connection terminals 7 b of the capacitors 7 are electrically connected to the pad portions 41 a of the wiring substrate 40, each of the wiring layers of the wiring substrate 40 can be used as power supply paths, so that sufficient power supply can be achieved. Thereby, the semiconductor device in accordance with the present embodiment can perform stable operation.” Takeda, [0155].</p>
<p>[1.A] a bottom package substrate;</p>	<p>Takeda discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].</p>

FIG. 11

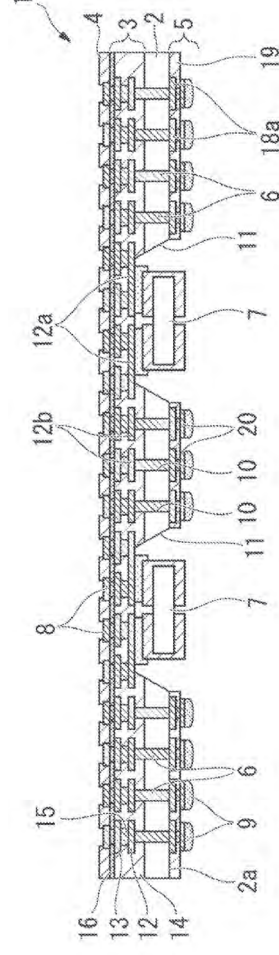


Takeda, FIG. 11

“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41a and 41b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

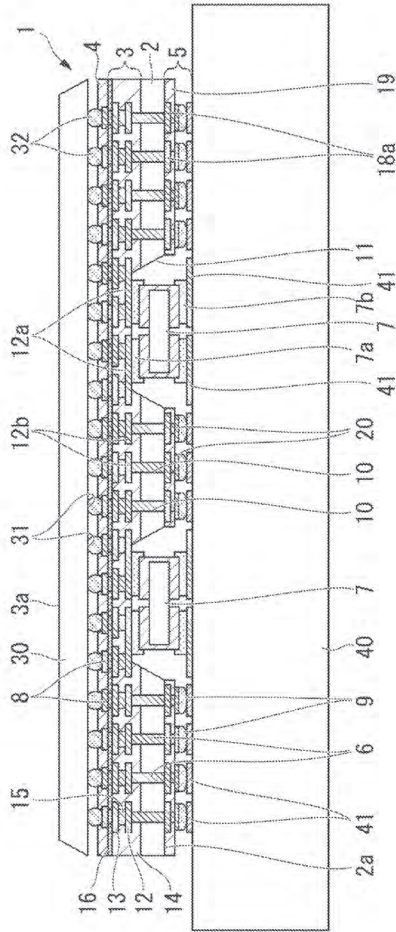
	<p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Takeda discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer 1 indicated in FIG. 1 includes a silicon substrate 2, a multilayer wiring portion 3, and an encapsulant resin 4 formed on one side surface of the silicon substrate 2, a bump forming portion 5 provided on another side surface of the silicon substrate 2, penetrating electrodes 6 that penetrate the silicon substrate 2 in the thickness direction, and capacitors (electronic parts for mounting) 7 provided in a cavity 11 of the silicon substrate 2.” Takeda, [0035].</p>



Takeda, FIG. 1

“As shown in FIG. 2, with respect to the interposer 1, each first UBM structure 8 is formed on the multilayer wiring portion 3 to which each connection portion 31 of the electronic part (mounting electronic part) 30 is electrically connected via a bump 32. In this way, the electronic part 30 is mounted on the interposer 1.” Takeda, [0035].

FIG. 2



Takeda, FIG 2.

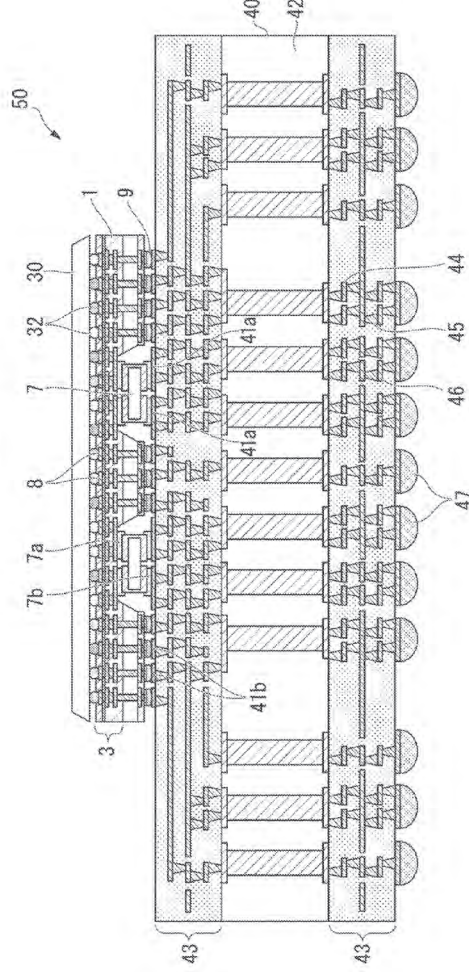
“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].

	<p style="text-align: center;">FIG. 11</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom</p>	<p>Takeda, FIG. 11</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Takeda discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p>

<p>package substrate and the top package substrate, wherein</p>	<p>See, e.g.:</p> <p>“The interposer 1 indicated in FIG. 1 includes a silicon substrate 2, a multilayer wiring portion 3, and an encapsulant resin 4 formed on one side surface of the silicon substrate 2, a bump forming portion 5 provided on another side surface of the silicon substrate 2, penetrating electrodes 6 that penetrate the silicon substrate 2 in the thickness direction, and capacitors (electronic parts for mounting) 7 provided in a cavity 11 of the silicon substrate 2.” Takeda, [0035].</p> <p style="text-align: center;">FIG. 1</p> <p style="text-align: center;">Takeda, FIG. 1</p> <p>“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor</p>
---	--

device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].

FIG. 11



Takeda, FIG. 11

To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

[1.D] the spacer connector comprises a core substrate;

Takeda discloses, either expressly or inherently, the spacer connector comprises a core substrate.

See, e.g.:

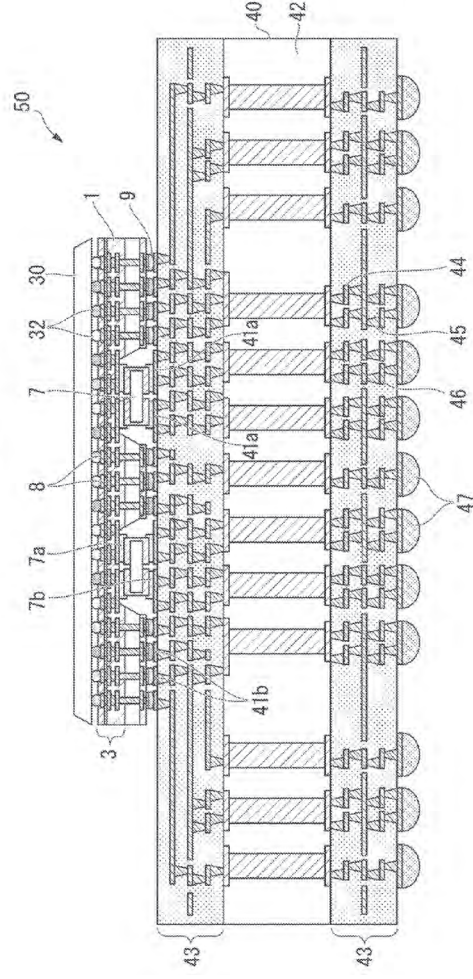
“The interposer 1 indicated in FIG. 1 includes a silicon substrate 2, a multilayer wiring portion 3, and an encapsulant resin 4 formed on one side surface of the silicon substrate 2, a bump forming portion 5 provided on another side surface of the silicon substrate 2, penetrating electrodes 6 that penetrate the silicon substrate 2 in the thickness direction, and capacitors (electronic parts for mounting) 7 provided in a cavity 11 of the silicon substrate 2.” Takeda, [0035].

FIG. 1

Takeda, FIG. 1

“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].

FIG. 11

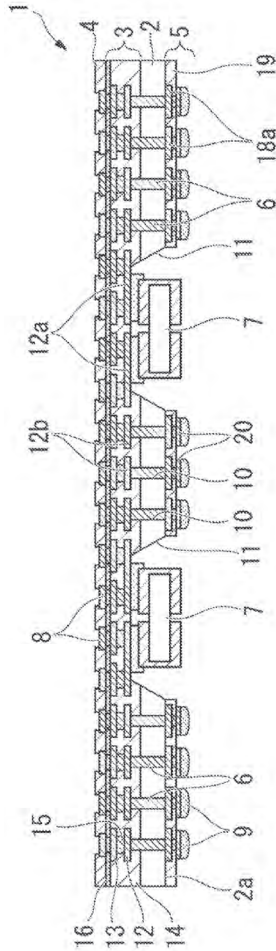


Takeda, FIG. 11

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

	<p>“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41 a and 41 b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Takeda discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The interposer 1 indicated in FIG. 1 includes a silicon substrate 2, a multilayer wiring portion 3, and an encapsulant resin 4 formed on one side surface of the silicon substrate 2, a bump forming portion 5 provided on another side surface of the silicon substrate 2, penetrating electrodes 6 that penetrate the silicon substrate 2 in the thickness direction, and capacitors (electronic parts for mounting) 7 provided in a cavity 11 of the silicon substrate 2.” Takeda, [0035].</p>

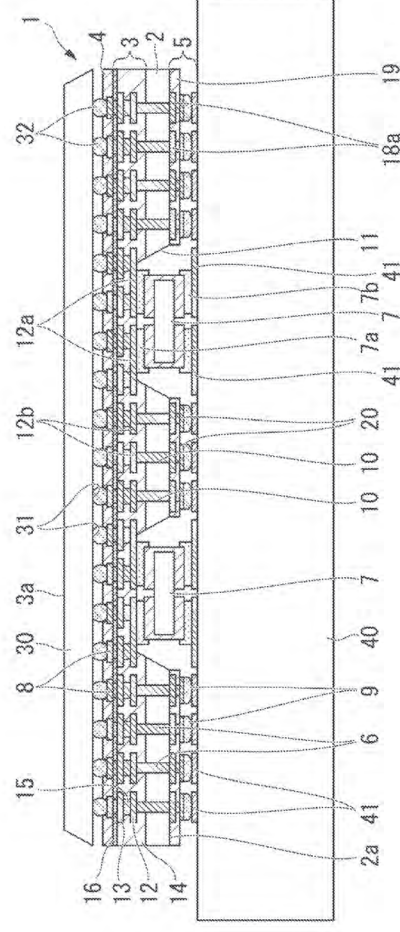
FIG. 1



Takeda, FIG. 1

“As shown in FIG. 2, with respect to the interposer 1, each first UBM structure 8 is formed on the multilayer wiring portion 3 to which each connection portion 31 of the electronic part (mounting electronic part) 30 is electrically connected via a bump 32. In this way, the electronic part 30 is mounted on the interposer 1.” Takeda, [0035].

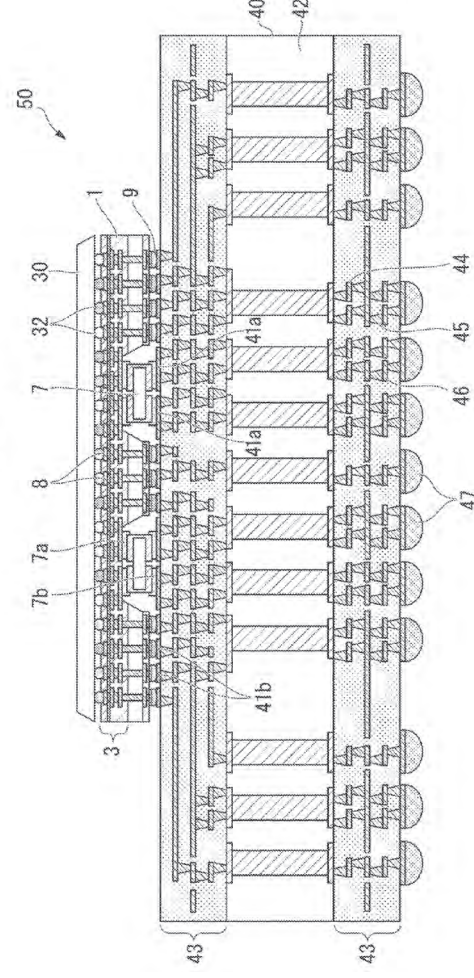
FIG. 2



Takeda, FIG. 2

“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].

FIG. 11



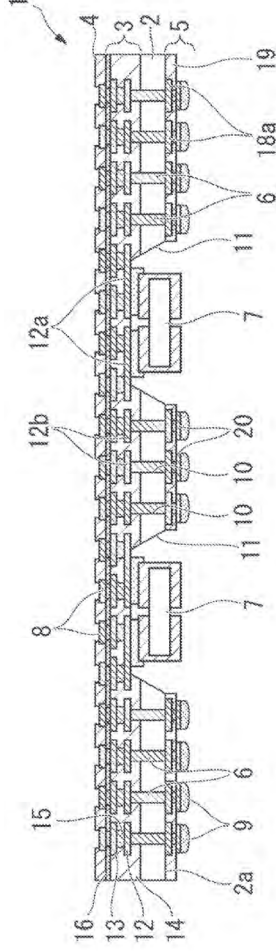
Takeda, FIG. 11

“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41 a and 41 b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

	<p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Takeda discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“The interposer 1 indicated in FIG. 1 includes a silicon substrate 2, a multilayer wiring portion 3, and an encapsulant resin 4 formed on one side surface of the silicon substrate 2, a bump forming portion 5 provided on another side surface of the silicon substrate 2, penetrating electrodes 6 that penetrate the silicon substrate 2 in the thickness direction, and capacitors (electronic parts for mounting) 7 provided in a cavity 11 of the silicon substrate 2.” Takeda, [0035].</p>

FIG. 1

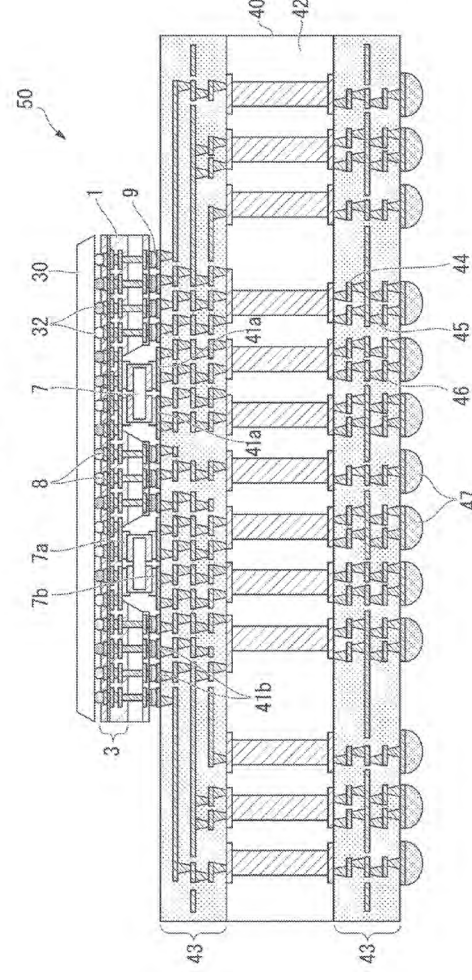


Takeda, FIG. 1

“The first wiring layer 12 is formed with a predetermined pattern on the silicon substrate 2. The second wiring layer 13 is formed on the first wiring layer 12 with a predetermined pattern. In the present invention, the first wiring layer 12 includes pad portions 12a formed on areas which correspond to the cavity portions 11, in which the pad portions 12a are electrically connected to the capacitors 7. The pad portions 12a are electrically connected to the first UBM structures 8 via the first wiring layer 12, the via electrodes 15, and the second wiring layer 13, where the first UBM structures 8 respectively correspond to pins (power supply connections) and ground pins (ground connections) of the electronic part 30. Therefore, with reference to the interposer 1, the capacitors 7 are connected to the pad portions 12a with the electronic part 30 being mounted on the interposer 1. The capacitors 7 are electrically connected to the power supply pins and ground pins via each of the above

	<p>parts. In descriptions below, other pads excluding the pad portions 12 a of the first wiring layer 12 will be referred to as wiring 12.” Takeda, [0040].</p> <p>“In this case, each of the penetrating holes 10 and each of the cavity portions 11, which are formed in the silicon substrate 2, are continuously formed through the interlayer insulating layer 14 that is positioned between the silicon substrate 2 and the first wiring layer 12. The top end of each penetrating hole 10 exposes the bottom surface of the wiring portion 12 b of the first wiring layer 12. The top end of each cavity portion 11 exposes the bottom of each pad portion 12 a of the first wiring layer 12. Each capacitor 7 mounted in the cavity portion 11 is electrically connected to each of the pad portions 12 a exposed at the top of the cavity portions 11.” Takeda, [0043].</p> <p>“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].</p>
--	---

FIG. 11



Takeda, FIG. 11

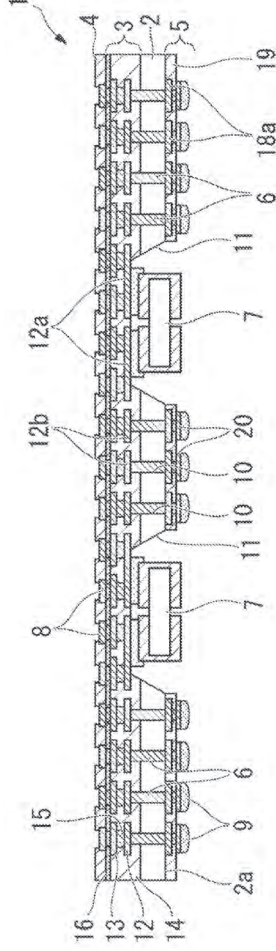
To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Takeda discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.

See, e.g.:

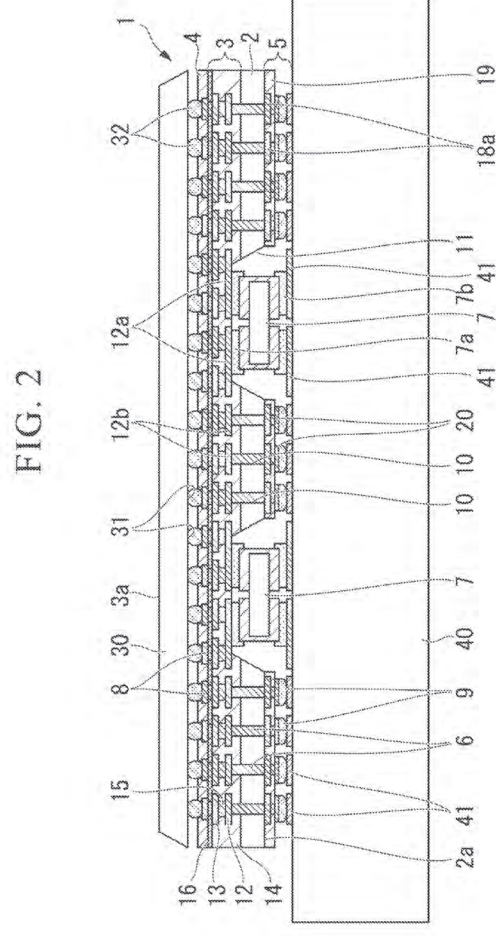
“The interposer 1 indicated in FIG. 1 includes a silicon substrate 2, a multilayer wiring portion 3, and an encapsulant resin 4 formed on one side surface of the silicon substrate 2, a bump forming portion 5 provided on another side surface of the silicon substrate 2, penetrating electrodes 6 that penetrate the silicon substrate 2 in the thickness direction, and capacitors (electronic parts for mounting) 7 provided in a cavity 11 of the silicon substrate 2.” Takeda, [0035].

FIG. 1



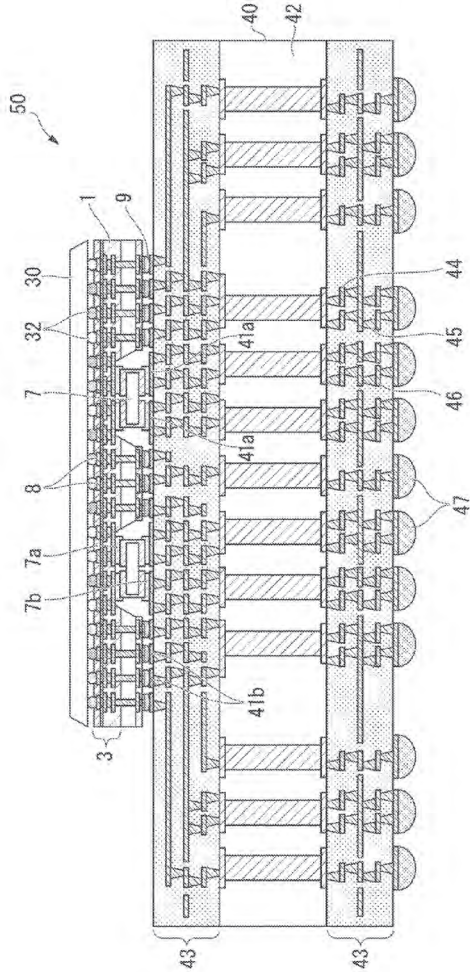
Takeda, FIG. 1

“As shown in FIG. 2, with respect to the interposer 1, each first UBM structure 8 is formed on the multilayer wiring portion 3 to which each connection portion 31 of the electronic part (mounting electronic part) 30 is electrically connected via a bump 32. In this way, the electronic part 30 is mounted on the interposer 1.” Takeda, [0035].



Takeda, FIG. 2

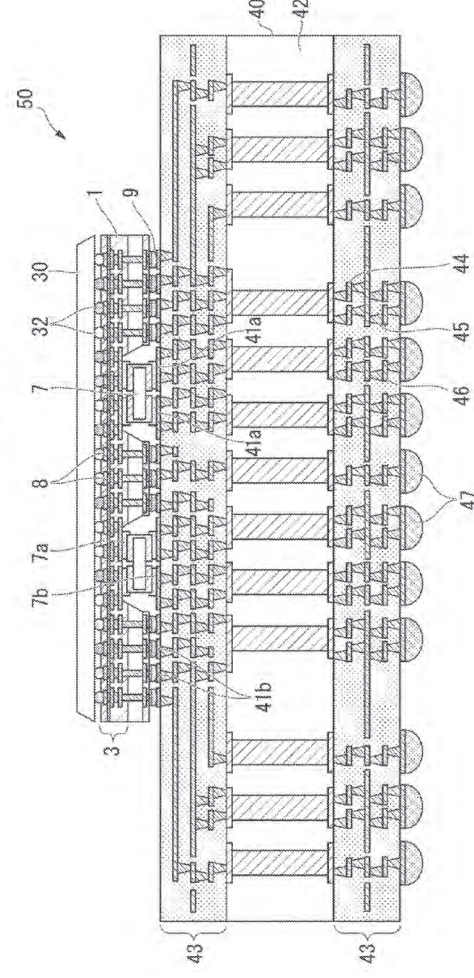
“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].

	<p>FIG. 11</p>  <p>Takeda, FIG. 11</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the</p>	<p>Takeda discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

plurality of metal pillars of the spacer connector,	<p><i>See, e.g.:</i></p> <p>“The first UBM structures 8 are respectively connected to the connecting portions 31 of the electronic part 30 via solder bumps 32, in which the electronic part 30 is mounted on the interposer 1.” Takeda, [0051].</p> <p>“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].</p>
---	---

FIG. 11



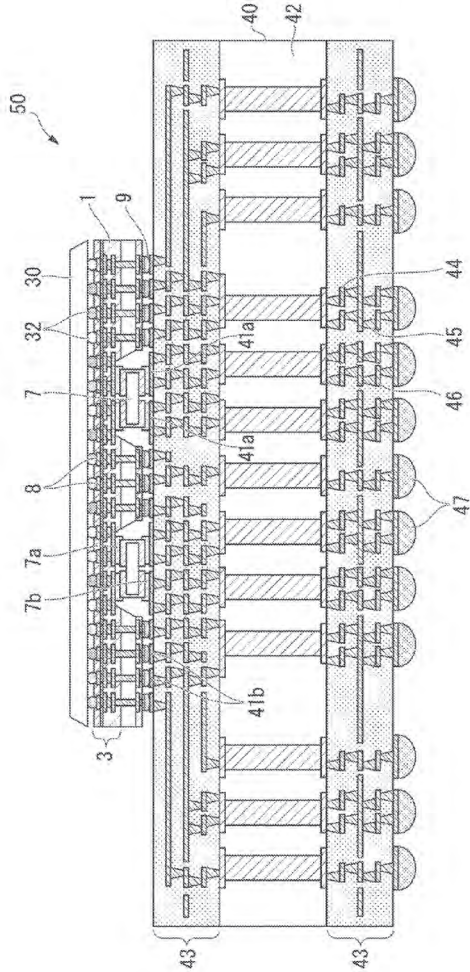
Takeda, FIG. 11

“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41 a and 41 b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

	<p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Takeda discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].</p>

FIG. 11



Takeda, FIG. 11

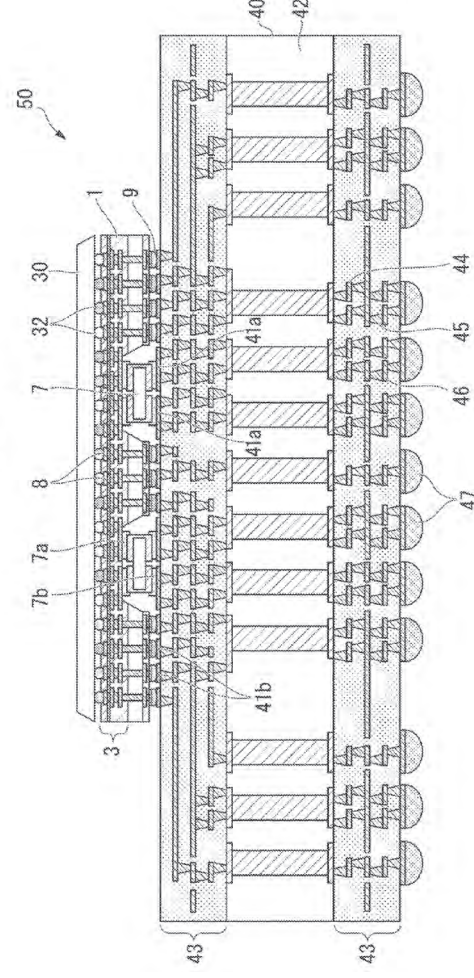
“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41a and 41b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

	<p>“The bumps 9 of the interposer 1 are respectively connected to the pad portions 41 b, and the connecting terminals 7 b are respectively connected to pad portions 41 a of the wiring substrate 40. In this way, the interposer 1 is mounted on the wiring substrate 40.” Takeda, [0153].</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Takeda discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The first wiring layer 12 is formed with a predetermined pattern on the silicon substrate 2. The second wiring layer 13 is formed on the first wiring layer 12 with a predetermined pattern. In the present invention, the first wiring layer 12 includes pad-portions 12 a formed on areas which correspond to the cavity portions 11, in which the pad portions 12 a are electrically connected to the capacitors 7. The pad portions 12 a are electrically connected to the first UBM structures 8 via the first wiring layer 12, the via electrodes 15, and the second wiring layer 13, where the first UBM structures 8 respectively correspond to pins (power supply connections) and ground pins (ground connections) of the electronic part 30. Therefore, with reference to the interposer 1, the capacitors 7 are connected to the pad portions 12 a with the electronic part 30 being mounted on the interposer 1. The capacitors 7</p>

	<p>are electrically connected to the power supply pins and ground pins via each of the above parts. In descriptions below, other pads excluding the pad portions 12 a of the first wiring layer 12 will be referred to as wiring 12.” Takeda, [0040].</p> <p>“The bump 9 is a conductive terminal with a round shape, and formed of a low melting point metal such as solder. The bump 9 is provided on each of the second UBM structures 20 (e.g., on the conductive portion 20 d). The interposer 1 is mounted on the wiring substrate 40 by connecting each bump 9 with each pad portion 41 b of the wiring substrate 40.” Takeda, [0065].</p> <p>“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].</p>
--	--

FIG. 11



Takeda, FIG. 11

“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41 a and 41 b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

	<p>“The bumps 9 of the interposer 1 are respectively connected to the pad portions 41 b, and the connecting terminals 7 b are respectively connected to pad portions 41 a of the wiring substrate 40. In this way, the interposer 1 is mounted on the wiring substrate 40.” Takeda, [0153].</p> <p>“As the connection terminals 7 b of the capacitors 7 are electrically connected to the pad portions 41 a of the wiring substrate 40, each of the wiring layers of the wiring substrate 40 can be used as power supply paths, so that sufficient power supply can be achieved. Thereby, the semiconductor device in accordance with the present embodiment can perform stable operation.” Takeda, [0155].</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein	<p>Takeda discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>

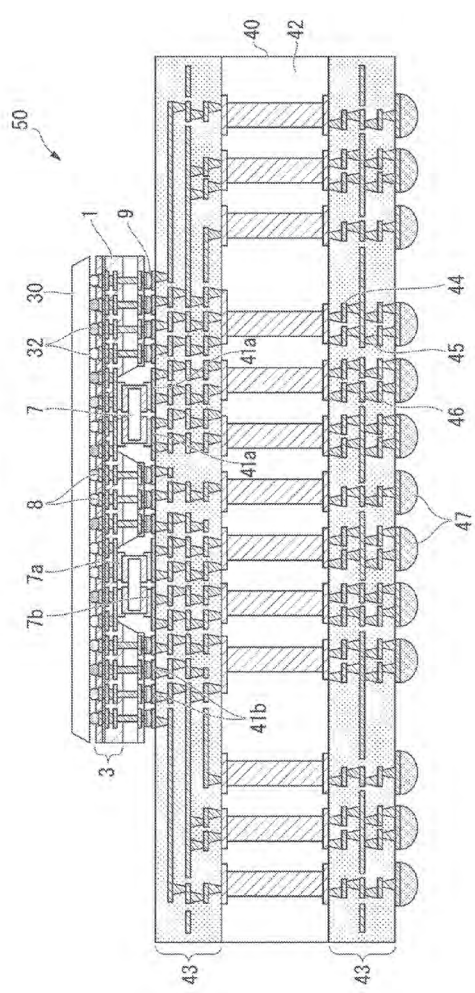
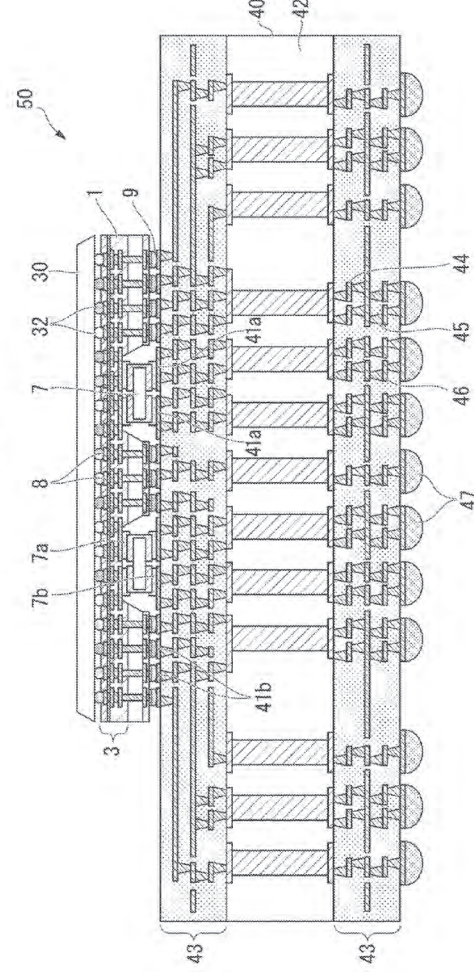
	<p style="text-align: center;">FIG. 11</p>  <p style="text-align: center;">Takeda, FIG. 11</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Takeda discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p>

FIG. 11



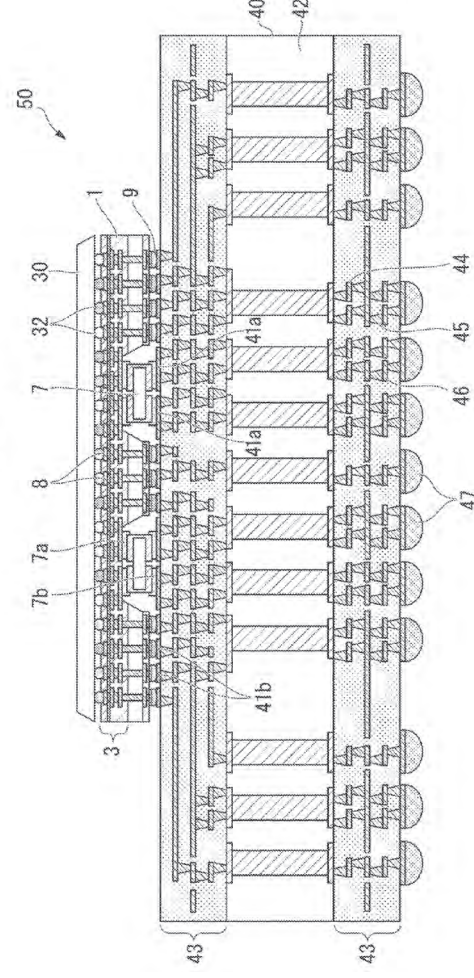
Takeda, FIG. 11

To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Takeda discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.

See, e.g.:

FIG. 11



Takeda, FIG. 11

To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 2, U.S. Patent No. 9859202

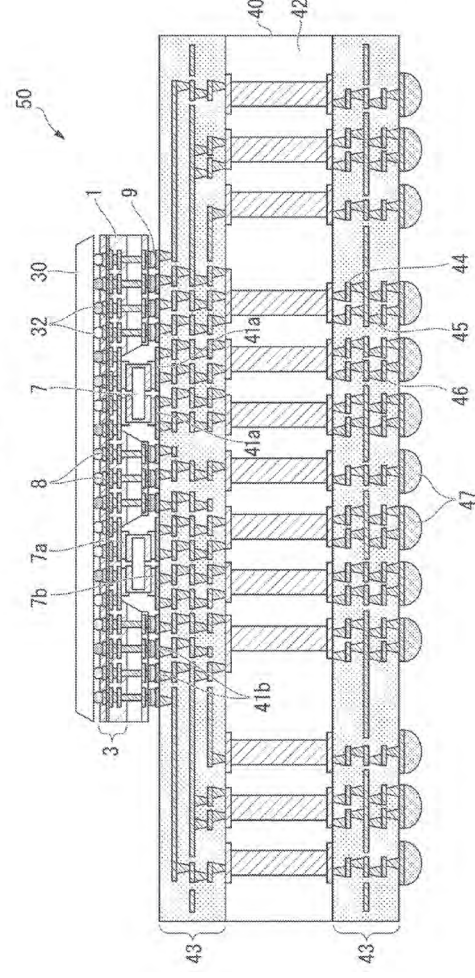
Claim Limitation	Disclosure
------------------	------------

[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

Takeda discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

See, e.g.:

FIG. 11



Takeda, FIG. 11

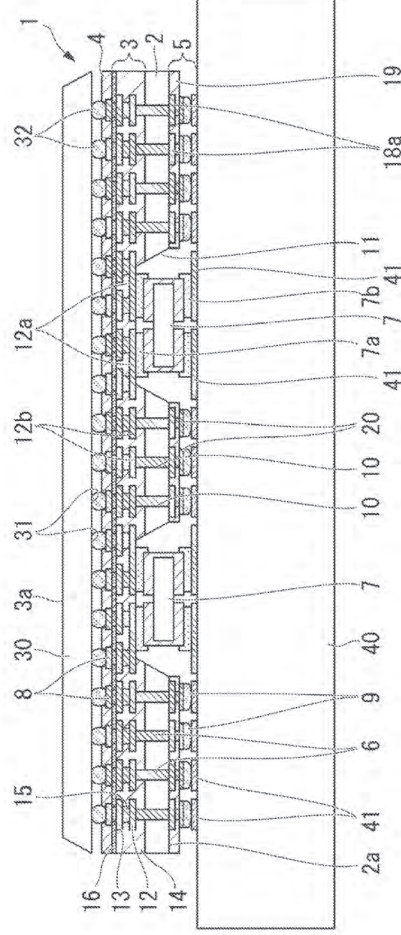
To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	<p>Takeda discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, e.g.:</p> <p>“FIG. 2 is a schematic diagram that illustrates a longitudinal cross-section of the interposer 1, in which an electronic part 30 is mounted on an interposer 1 and the interposer 1 is mounted on a wiring substrate 3.” Takeda, [0019].</p>

FIG. 2



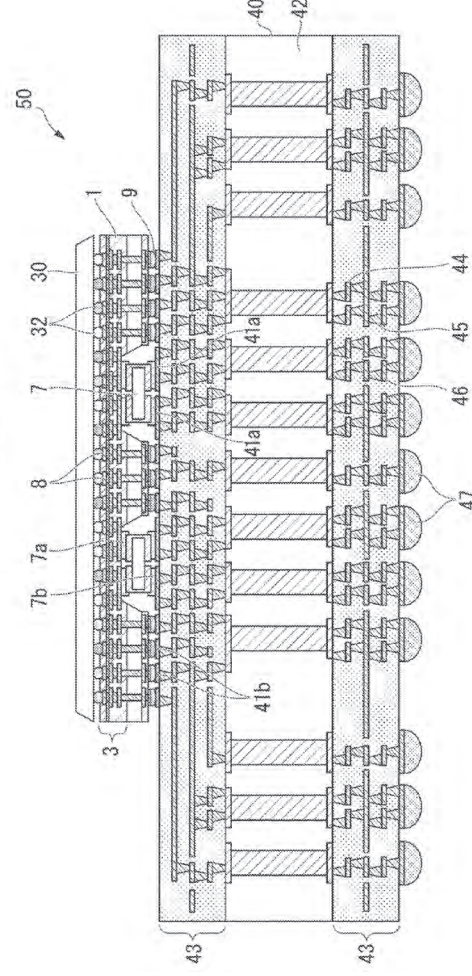
Takeda, FIG. 2

“As shown in FIG. 2, with respect to the interposer 1, each first UBM structure 8 is formed on the multilayer wiring portion 3 to which each connection portion 31 of the electronic part (mounting electronic part) 30 is electrically connected via a bump 32. In this way, the electronic part 30 is mounted on the interposer 1. Furthermore, each bump 9 of the bump forming portion 5 is electrically connected to a respective pad portion 41 b of the wiring substrate 40, so that the interposer 1 is mounted to the wiring substrate 40.” Takeda, [0035-0036].

“Furthermore, with respect to the interposer 1 in accordance with the present invention, capacitors 7 are respectively provided in each of the cavity portions 11 of the silicon substrate 2. The connecting terminal 7 a of the capacitor 7 is electrically connected to the pad portion 12 a that is exposed in the cavity portion 11.” Takeda, [0066].

“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].

FIG. 11



Takeda, FIG. 11

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

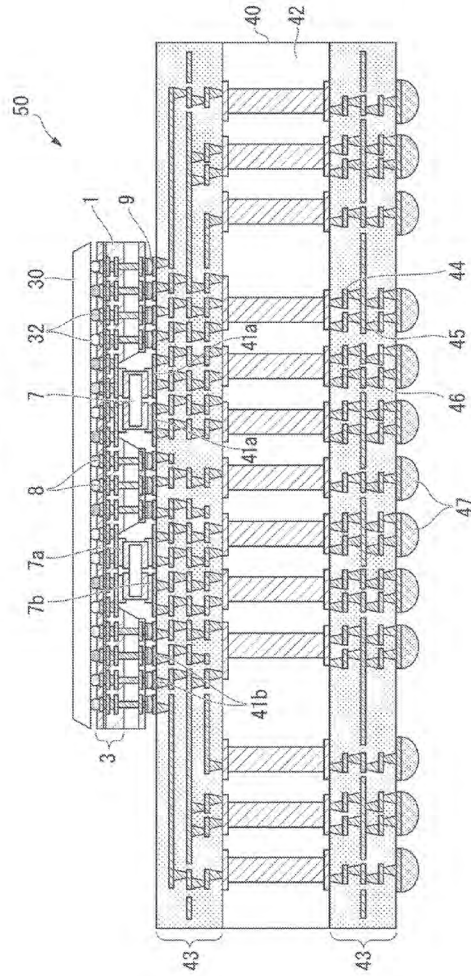
	<p>“The electronic part 30 includes multiple connection portions 31 at the back surface of the electronic part 30, and the multiple connection portions 31 are connected to each of the first UBM structures 8, so that the electronic part 30 is mounted on the interposer 1. For the interposer 1 mounted by the electronic part 30, the capacitors 7 are disposed in the cavity portion 10 and electrically connected to the ground pins and the power supply pins of the electronic part 30 via each of portions of the multilayer wiring portion 3.” Takeda, [0150-0151].</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>Takeda discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The first wiring layer 12 is formed with a predetermined pattern on the silicon substrate 2. The second wiring layer 13 is formed on the first wiring layer 12 with a predetermined</p>

	<p>pattern. In the present invention, the first wiring layer 12 includes pad-portions 12 a formed on areas which correspond to the cavity portions 11, in which the pad portions 12 a are electrically connected to the capacitors 7. The pad portions 12 a are electrically connected to the first UBM structures 8 via the first wiring layer 12, the via electrodes 15, and the second wiring layer 13, where the first UBM structures 8 respectively correspond to pins (power supply connections) and ground pins (ground connections) of the electronic part 30. Therefore, with reference to the interposer 1, the capacitors 7 are connected to the pad portions 12 a with the electronic part 30 being mounted on the interposer 1. The capacitors 7 are electrically connected to the power supply pins and ground pins via each of the above parts. In descriptions below, other pads excluding the pad portions 12 a of the first wiring layer 12 will be referred to as wiring 12.” Takeda, [0040].</p> <p>“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].</p>
--	---

FIG. 11



Takeda, FIG. 11

“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41a and 41b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].

Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

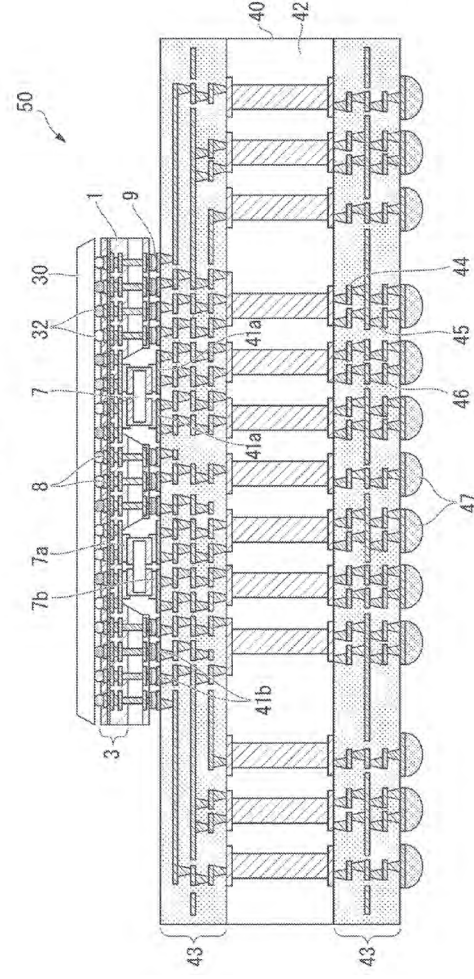
	<p>“The bumps 9 of the interposer 1 are respectively connected to the pad portions 41 b, and the connecting terminals 7 b are respectively connected to pad portions 41 a of the wiring substrate 40. In this way, the interposer 1 is mounted on the wiring substrate 40.” Takeda, [0153].</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Takeda discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

spacer connector via the corresponding top metal pads of the spacer connector.

FIG. 11



Takeda, FIG. 11

To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

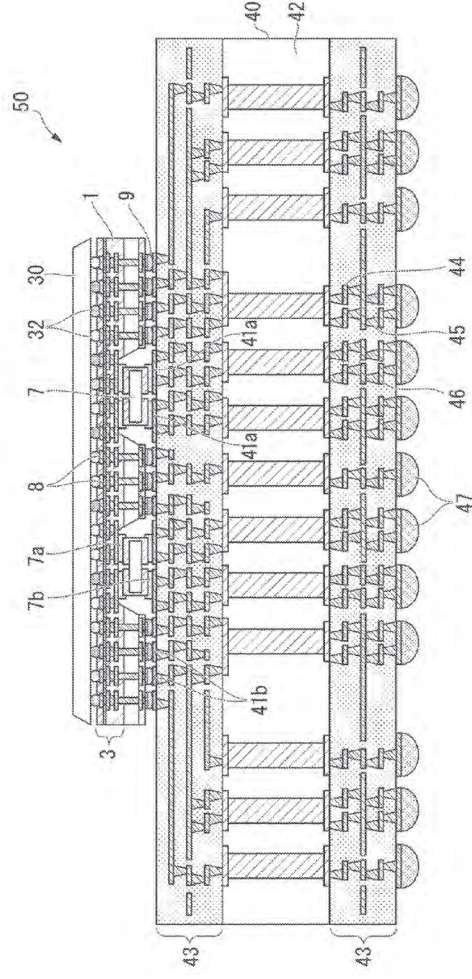
Appendix A-32 - Invalidity of U.S. Patent No. 9859202 in view of Takeda - U.S. Patent Publication No. 20120139010

<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Takeda discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The first wiring layer 12 is formed with a predetermined pattern on the silicon substrate 2. The second wiring layer 13 is formed on the first wiring layer 12 with a predetermined pattern. In the present invention, the first wiring layer 12 includes pad-portions 12 a formed on areas which correspond to the cavity portions 11, in which the pad portions 12 a are electrically connected to the capacitors 7. The pad portions 12 a are electrically connected to the first UBM structures 8 via the first wiring layer 12, the via electrodes 15, and the second wiring layer 13, where the first UBM structures 8 respectively correspond to pins (power supply connections) and ground pins (ground connections) of the electronic part 30. Therefore, with reference to the interposer 1, the capacitors 7 are connected to the pad portions 12 a with the electronic part 30 being mounted on the interposer 1. The capacitors 7 are electrically connected to the power supply pins and ground pins via each of the above parts. In descriptions below, other pads excluding the pad portions 12 a of the first wiring layer 12 will be referred to as wiring 12.” Takeda, [0040].</p> <p>“The bump 9 is a conductive terminal with a round shape, and formed of a low melting point metal such as solder. The bump 9 is provided on each of the second UBM structures 20 (e.g., on the conductive portion 20 d). The interposer 1 is mounted on the wiring substrate 40 by</p>
--	---

connecting each bump 9 with each pad portion 41 b of the wiring substrate 40.” Takeda, [0065].

“Next, a description will be given of a semiconductor device (a semiconductor device of the present invention) that utilizes the interposer in accordance with the present invention. FIG. 11 is a schematic diagram that illustrates a longitudinal cross-section of a semiconductor device 50 in accordance with an embodiment of the present invention. The semiconductor device 50 of FIG. 11 includes an interposer 1, an electronic part (mounting electronic part) 30 mounted on the interposer 1, and a buildup substrate (wiring substrate) 40 on which the interposer 1 is mounted.” Takeda, [0146-0148].

FIG. 11



	<p>Takeda, FIG. 11</p> <p>“The wiring substrate 40 includes a substrate 42 and multilayer wiring portions 43 disposed on both sides of the substrate 42. Each of the multilayer wiring portions 43 includes three wiring layers 44, 45, and 46. One side of the multilayer wiring portions 43 includes multiple pad portions 41 a and 41 b, which are electrically connected to the wiring layers 44, 45, and 46, respectively. Furthermore, the other side of the multilayer wiring portions 43 includes multiple bumps 47, which are electrically connected to the wiring layers 44, 45 and 46, respectively.” Takeda, [0152].</p> <p>“The bumps 9 of the interposer 1 are respectively connected to the pad portions 41 b, and the connecting terminals 7 b are respectively connected to pad portions 41 a of the wiring substrate 40. In this way, the interposer 1 is mounted on the wiring substrate 40.” Takeda, [0153].</p> <p>“As the connection terminals 7 b of the capacitors 7 are electrically connected to the pad portions 41 a of the wiring substrate 40, each of the wiring layers of the wiring substrate 40 can be used as power supply paths, so that sufficient power supply can be achieved. Thereby, the semiconductor device in accordance with the present embodiment can perform stable operation.” Takeda, [0155].</p> <p>To the extent Plaintiff contends that Takeda fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

U.S. Patent No.8379403 (“Waite”) is titled Spacer-Connector and Circuit Board Assembly and lists David W. Waite, James L. Blair, Ashish Lohiya, Arvid G. Sammulu, Jeffery T. Smith, and Saritha Narra as inventors. Waite is assigned to Qualcomm, Incorporated. Waite anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Waite is a U.S. patent that was filed March 30, 2010 and published October 7, 2010. Waite claims priority to a provisional application filed on April 2, 2009. Waite is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Waite, or otherwise rendered obvious by disclosures and teachings of Waite, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Waite does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Waite with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Waite, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Waite “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Waite or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Waite set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Waite discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 2A illustrates a motherboard 200 on which a daughter board 202 is mounted. Daughter board 202 is supported on the motherboard 200 by first and second spacer-connectors 204 which connectors 204 include conductive pathways discussed hereinafter. A first conductive elastomer 206 provides an electrical connection between the daughter board 202 and the spacer-connectors 204, and a second conductive elastomer 208 provides an electrical connection between the motherboard 200 and the spacer-connector assembly 204.” Waite, [4:3-4:11].</p>

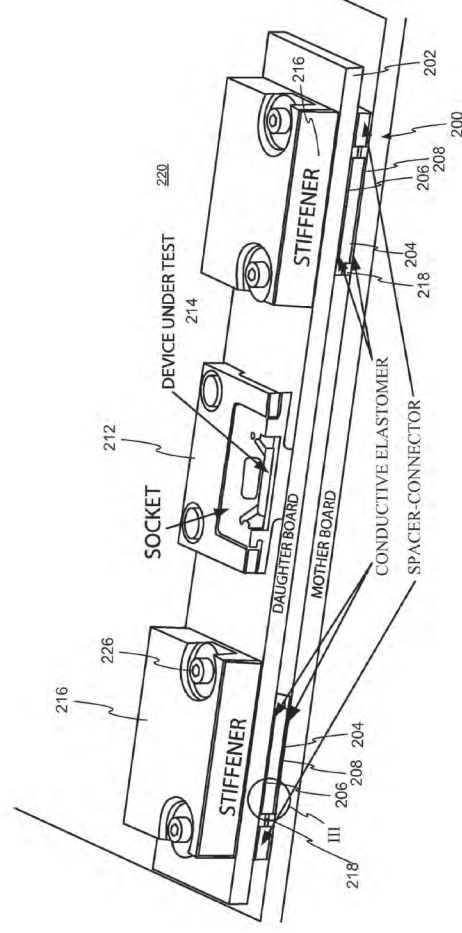


FIG. 2A

Waite, FIG. 2A

“FIG. 2B illustrates a plan view of the spacer-connector 204. A portion illustrated in FIG. 2A is enclosed within the dashed area. As can be seen from the plan view, the spacer-connector has two pad arrays 250 (or connectors) with frame elements 218 (including frame 318 and frame well 316 in FIG. 3) disposed around the pad array 250. An open area or cavity 260 may provide for access to the underside of the DUT as illustrated in FIG. 2A. The cavity 260 can be located between the pad arrays 250 and may be enclosed by a thin web of material 265.” Waite, [6:31-6:39].

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface. The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper. The cavity 260 between a pair of connectors/pad arrays of spacer-connector 204 can be produced by milling out a single piece of circuit board. The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.” Waite, [6:59-7:6].</p> <p>“FIG. 4B illustrates an alternative configuration where spacer-connector 204 is located on only one side of the DUT 214 and socket 212 assembly and may contain a single pad array portion as illustrated in FIG. 2C, for example. To maintain mechanical stability of the daughter board 202 a separate mechanical spacer 480 may be provided. Additionally, spacer-connector 204 and mechanical spacer 480 will cause an area 482 to be formed under the daughter board 202, which can also be used for mounting components 406.” Waite, [7:26-7:34].</p> <p>“In order to connect RF signals to/from DUT 214 and tuning elements 406 on the daughter board 202 with RF components and pathways located on motherboard 200, a wide band RF pathway between the DUT 214 and the motherboard 200 is provided through connector of spacer-connector 204. The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:39-7:46].</p>
--	---

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“FIG. 8 also illustrates a sectional view of a multilayered PCB having a plurality of ground planes 422 separated by layers of dielectric material 424. Further, additional conductive planes/traces may be included internally (e.g., 432, 433) separated by dielectric layers for routing signals internally. Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [9:67-10:5].</p>
[1.A] a bottom package substrate;	<p>Waite discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:19-4:26].</p> <p>“With reference to FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface. The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper. The cavity 260 between a pair of connectors/pad arrays of spacer-connector 204 can be produced by milling out a single piece of circuit board. The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.” Waite, [6:59-7:6].</p>

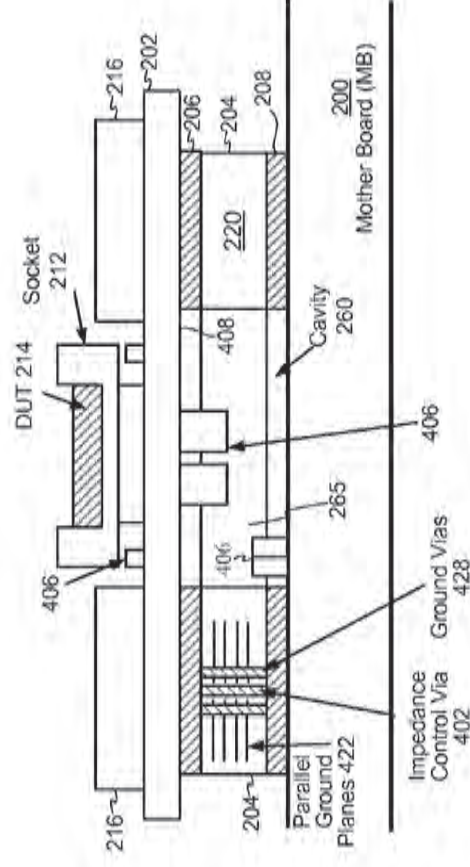


FIG. 4A

Waite, FIG. 4A

“In order to connect RF signals to/from DUT 214 and tuning elements 406 on the daughter board 202 with RF components and pathways located on motherboard 200, a wide band RF pathway between the DUT 214 and the motherboard 200 is provided through connector of spacer-connector 204.” Waite, [7:39-7:43].

To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Waite discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Other embodiments may include more than two connectors of spacer-connector 204 arranged around socket 212 to provide a larger area for connections between the DUT 214 and the motherboard 200. The assembly of the motherboard 200, the first and second conductive elastomers 206, 208 and the connectors of spacer-connector 204 are compressed to from the conductive elements in the first and second conductive elastomers 206, 208 into conductive pathways. Stiffener blocks 216 may be provided to keep an even amount of pressure over the spacer-connectors 204 and to maintain good electrical connections between the first and second conductive elastomers 206, 208 and the connectors of spacer-connector 204.” Waite, [5:21-5:34].</p> <p>“With reference to FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface. The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper. The cavity 260 between a pair of connectors/pad arrays of spacer-connector 204 can be produced by milling out a single piece of circuit board. The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.” Waite, [6:59-7:6].</p>
---	---

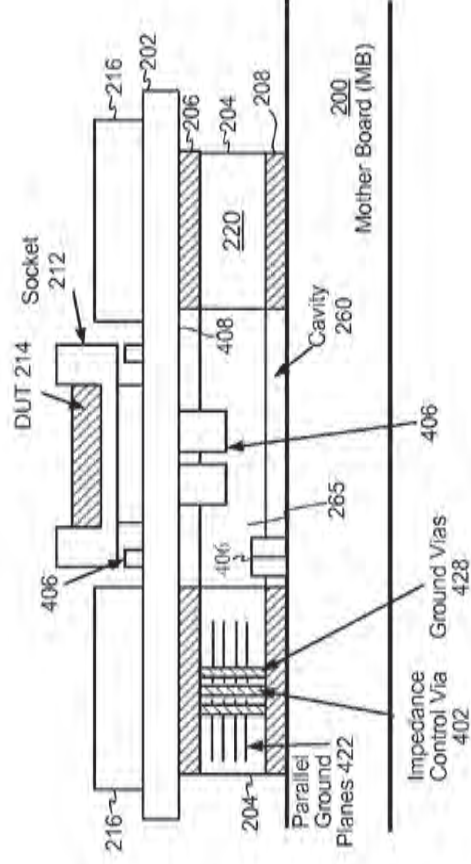


FIG. 4A

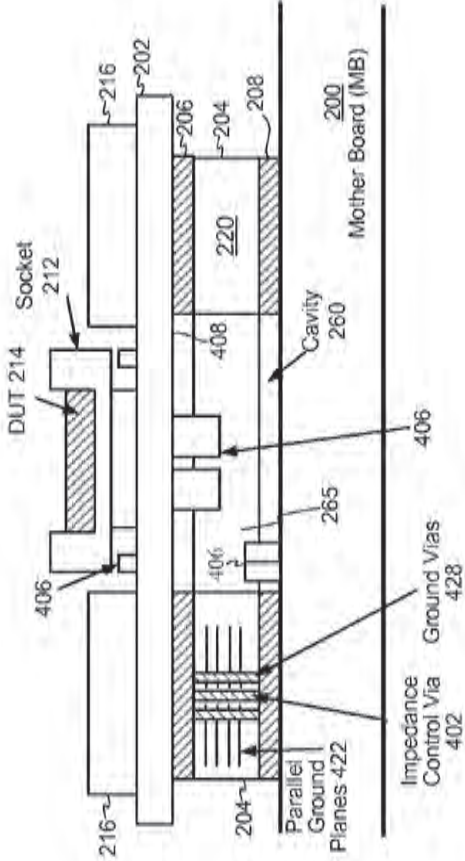
Waite, FIG. 4A

“FIG. 4B illustrates an alternative configuration where spacer-connector 204 is located on only one side of the DUT 214 and socket 212 assembly and may contain a single pad array portion as illustrated in FIG. 2C, for example. To maintain mechanical stability of the daughter board 202 a separate mechanical spacer 480 may be provided. Additionally, spacer-connector 204 and mechanical spacer 480 will cause an area 482 to be formed under the daughter board 202, which can also be used for mounting components 406.” Waite, [7:26-7:34].

To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Waite discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“When the device under test 214 includes RF components, it may be desirable to place RF tuning circuitry and RF-related components close to the device under test to reduce the effects of the pathway between the DUT 214 and such circuitry. For example, if RF traces are routed at appreciable length on a PCB the signal integrity (fidelity) of these electrical pathways will suffer due to insertion and return loss effects attributable in part to loss of impedance control due to the presence of parasitic (stray) inductance and/or capacitance or conductor skin effect losses. It would therefore be desirable to keep RF components at a controllable, small distance from the DUT 214. One way of providing more usable real estate near the DUT 214 is to elevate the DUT 214 and daughter board 202 above the motherboard using spacer-connector 204 as described above.” Waite, [6:14-6:28].</p> <p>“FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface. The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper. The cavity 260 between a pair of connectors/pad arrays of spacer-connector 204 can be produced by milling out a single piece of circuit board. The cavity 260 provides room for RF tuning components 406 and/or other components to be</p>
---	--

	<p>located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.” Waite, [6:59-7:6].</p> <div></div> <p>Waite, FIG. 4A</p> <p>“FIG. 4B illustrates an alternative configuration where spacer-connector 204 is located on only one side of the DUT 214 and socket 212 assembly and may contain a single pad array portion as illustrated in FIG. 2C, for example. To maintain mechanical stability of the daughter board 202 a separate mechanical spacer 480 may be provided. Additionally, spacer-connector 204 and mechanical spacer 480 will cause an area 482 to be formed under the</p>
--	---

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>daughter board 202, which can also be used for mounting components 406.” Waite, [7:26-7:34].</p> <p>“A variety of RF connections can be made when using one or more connectors of spacer-connector 204 to elevate a daughter board 202 above a motherboard 200. As illustrated in FIG. 7, coaxial cables 702 may be used to connect elements (RF, analog, high speed digital) on the top side of the daughter board 202 to ATE test channels, test hardware or data acquisition systems (not illustrated) while allowing the tuning components 406 to be located near the DUT 214 on the underside of the daughter board 202 and/or on the motherboard 200 in the region between the daughter board 202 and the motherboard 200. When a large number of RF connections with a DUT 214 are required, it may also be possible to route additional coaxial leads 704 in cavity 260 to the underside of the daughter board 202 and through openings 706 in the motherboard 200 so that fewer coaxial cables need to be routed from the top side of the daughter board 202.” Waite, [9:24-9:39].</p> <p>“As illustrated in FIG. 7, coaxial cables 702 may be used to connect elements (RF, analog, high speed digital) on the top side of the daughter board 202 to ATE test channels, test hardware or data acquisition systems (not illustrated) while allowing the tuning components 406 to be located near the DUT 214 on the underside of the daughter board 202 and/or on the motherboard 200 in the region between the daughter board 202 and the motherboard 200.” Waite, [9:26-9:34].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Waite discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Accordingly, an embodiment can include a circuit board assembly comprising: a spacer-connector assembly positioned between a first circuit board and a second circuit board, wherein the spacer-connector assembly comprises: a spacer-connector formed of a multilayer printed circuit board (PCB) having a configurable pad array that is configured to pass signals between the first circuit board and the second circuit board, wherein the pad array is formed from the surface conductive layer of the PCB; and elastomeric conductive interface positioned between the pad array of each of the spacer-connector the first circuit board and second circuit board.” Waite, [2:10-2:20].</p> <p>“Another embodiment can include a spacer-connector formed of a multilayer printed circuit board (PCB) comprising contact means for passing signals from a first surface of the PCB to a second surface of the PCB, wherein the contact means is formed from a surface conductive layer of the PCB on respective first and second surfaces; and a conductive means for conducting signals formed through the PCB, wherein the PCB includes multiple parallel ground planes.” Waite, [2:25-2:32].</p> <p>“spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface. The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper.” Waite, [6:59-6:66].</p>
--	--

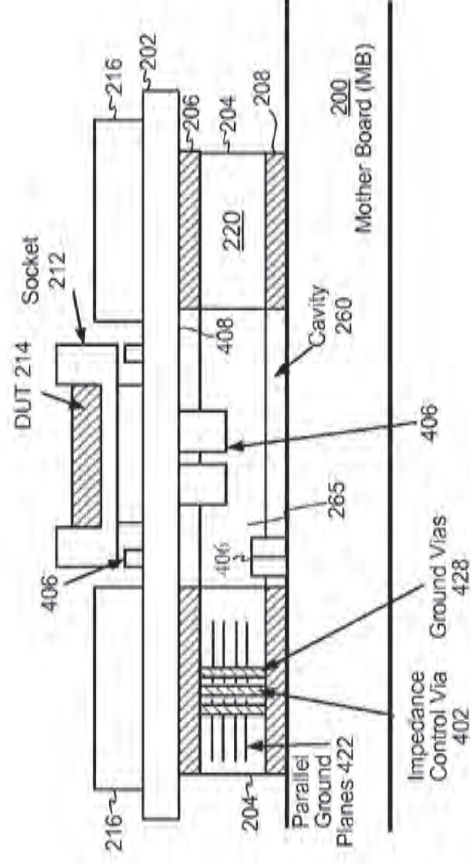


FIG. 4A

Waite, FIG. 4A

“The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper. The cavity 260 between a pair of connectors/pad arrays of spacer-connector 204 can be produced by milling out a single piece of circuit board.” Waite, [6:62-7:1].

“The first and second connectors of spacer-connector 204 may be connected to one another by a thin web of material 265 illustrated in FIGS. 2B and 4. This web 265 is provided primarily to maintain a desired separation and registration between the first and second connectors of spacer-connector 204.” Waite, [7:16-7:21].

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“FIG. 8 also illustrates a sectional view of a multilayered PCB having a plurality of ground planes 422 separated by layers of dielectric material 424. Further, additional conductive planes/traces may be included internally (e.g., 432, 433) separated by dielectric layers for routing signals internally.” Waite, [9:67-10:1].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Waite discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface. The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper.” Waite, [6:59-6:66].</p>

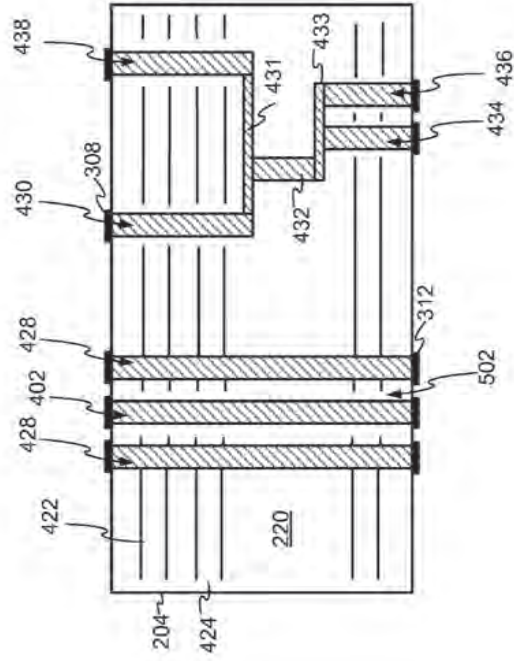


FIG. 8

Waite, FIG. 8

“The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.”
Waite, [7:43-7:46].

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“The impedance of vias 402 are also affected by the spacing of the ground planes in the body of material 220 (not shown), by via diameter relative to antipad 502 clearance on each ground plane and by the number and physical placement of the surrounding ground vias 428.” Waite, [8:12-8:16].</p> <p>“FIG. 8 also illustrates a sectional view of a multilayered PCB having a plurality of ground planes 422 separated by layers of dielectric material 424. Further, additional conductive planes/traces may be included internally (e.g., 432, 433) separated by dielectric layers for routing signals internally. Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422.” Waite, [9:67-10:3].</p> <p>“Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [10:2-10:5].</p> <p>“Further it will be appreciated that in various embodiments a first contact pad may be coupled to a conductive via that may extend only partially through the PCB (e.g., 432, 434, and 436) to an internal connection point (e.g., 431, 433) and may be routed from there to one or more conductive vias (e.g., 434, 436) that couple to one or more pads that may be physically offset from the first contact pad (430).” Waite, [10:9-10:16].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Waite discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:19-4:26].</p> <p>“The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:43-7:46].</p> <p>“The pads of the pad arrays 250 illustrated in FIGS. 5A-5C may be formed of gold-plated nickel plate on a copper pad. The overall height may be approximately 2.8 mils (0.0028 inches) as that molds more easily into the elastomer and accommodates small variations in co-planarity.” Waite, [7:58-7:62].</p> <p>“Conductive ground vias 428 and signal vias 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [10:2-10:5].</p>
--	---

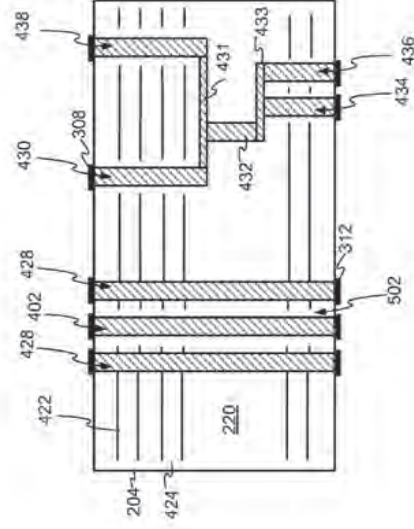


FIG. 8

Waite, FIG. 8

“Each via is connected to contact pads (308, 312) affixed to it at each PCB surface. The ground vias 428 can be coupled to the ground planes, whereas the signal vias 402, 432 may have antipads 502 formed in each ground plane.” Waite, [10:3-10:7].

To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Waite discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Similarly, upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:23-4:26].</p>
--	---

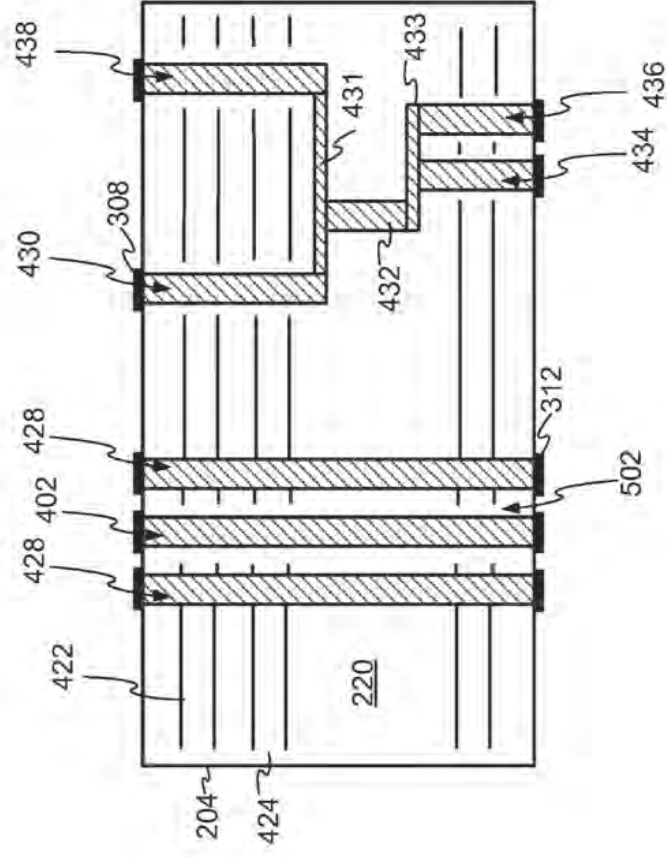
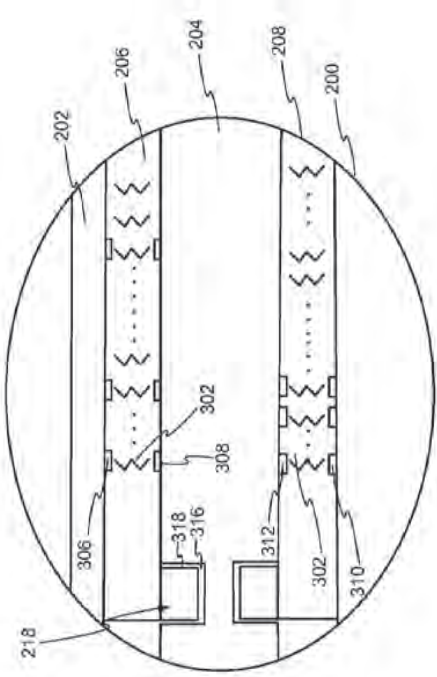


FIG. 8

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>Waite, FIG. 8</p> <p>“Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [10:2-10:5].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Waite discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Another embodiment can include a spacer-connector formed of a multilayer printed circuit board (PCB) comprising: a configurable pad array that is configured to pass signals between a first surface of the PCB and a second surface of the PCB, wherein the pad array is formed from a surface conductive layer of the PCB on respective first and second surfaces; and a plurality of conductive vias formed through the PCB, wherein the PCB includes multiple parallel ground planes.” Waite, [2:33-2:42].</p> <p>“Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the motherboard 200 are</p>

	<p>coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:19-4:26].</p> <div></div> <p>FIG. 3</p> <p>Waite, FIG. 3</p> <p>“The daughter board 202 includes a plurality of electrical connections between various electrical contacts (not illustrated) of the socket 212 and daughter board lower contact pads (shown in FIG. 3).” Waite, [5:7-5:10].</p>
--	--

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“With reference to FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface.” Waite, [6:59-6:62].</p> <p>“In order to connect RF signals to/from DUT 214 and tuning elements 406 on the daughter board 202 with RF components and pathways located on motherboard 200, a wide band RF pathway between the DUT 214 and the motherboard 200 is provided through connector of spacer-connector 204. The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:39-7:46].</p> <p>“FIG. 8 also illustrates a sectional view of a multilayered PCB having a plurality of ground planes 422 separated by layers of dielectric material 424. Further, additional conductive planes/traces may be included internally (e.g., 432, 433) separated by dielectric layers for routing signals internally. Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [9:67-10:5].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the	<p>Waite discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>plurality of metal pillars of the spacer connector, and</p>	<p>See, e.g.:</p> <p>“Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206.” Waite, [4:19-4:22].</p> <p>“Similarly, upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:23-4:26].</p> <div></div> <p>FIG. 3</p> <p>Waite, FIG. 3</p>
--	---

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“Referring again to FIG. 2A, the daughter board 202 includes a socket 212 into which a DUT 214 may be inserted to electrically couple the DUT 214 electrical pin-contacts to the daughter board 202. The daughter board 202 includes a plurality of electrical connections between various electrical contacts (not illustrated) of the socket 212 and daughter board lower contact pads (shown in FIG. 3).” Waite, [5:4-5:10].</p> <p>“In order to connect RF signals to/from DUT 214 and tuning elements 406 on the daughter board 202 with RF components and pathways located on motherboard 200, a wide band RF pathway between the DUT 214 and the motherboard 200 is provided through connector of spacer-connector 204. The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:39-7:46].</p> <p>“The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:43-7:46].</p> <p>“Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [10:2-10:5].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Waite discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:19-4:26].</p>
--	---

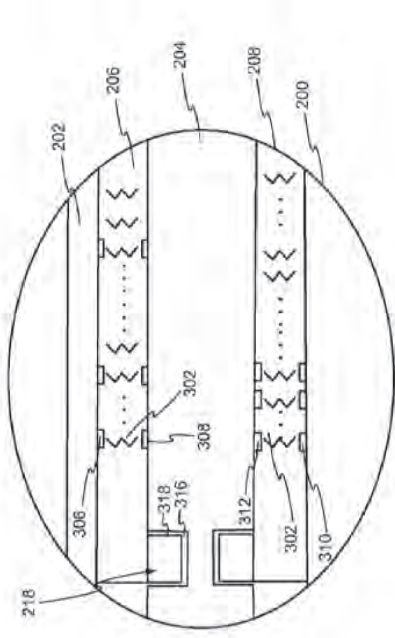


FIG. 3

Waite, FIG. 3

“The daughter board 202 includes a plurality of electrical connections between various electrical contacts (not illustrated) of the socket 212 and daughter board lower contact pads (shown in FIG. 3).” Waite, [5:7-5:10].

“With reference to FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface.” Waite, [6:59-6:62].

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“In order to connect RF signals to/from DUT 214 and tuning elements 406 on the daughter board 202 with RF components and pathways located on motherboard 200, a wide band RF pathway between the DUT 214 and the motherboard 200 is provided through connector of spacer-connector 204.” Waite, [7:39-7:43].</p> <p>“The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:43-7:46].</p> <p>“Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [10:2-10:5].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Waite discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“When the device under test 214 includes RF components, it may be desirable to place RF tuning circuitry and RF-related components close to the device under test to reduce the effects of the pathway between the DUT 214 and such circuitry.” Waite, [6:14-6:17].</p>

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

“The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.” Waite, [7:1-7:6].

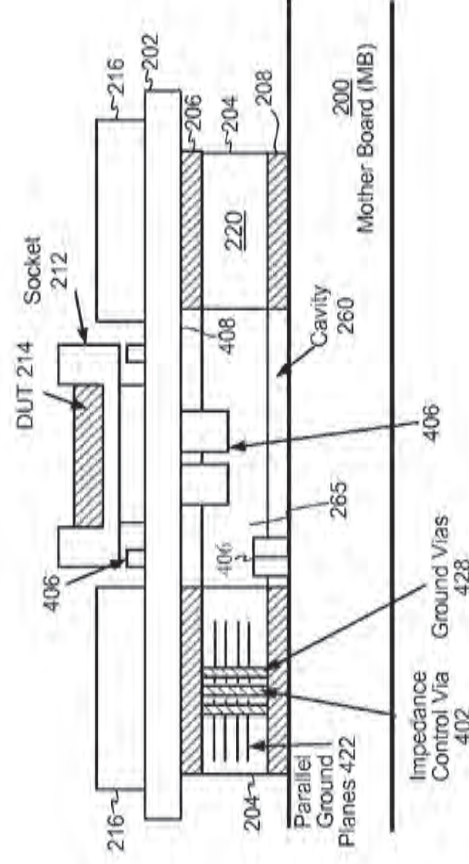


FIG. 4A

Waite, FIG. 4A

To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Waite discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“A device under test (DUT) 115 having a certain ball grid array (BGA) spacing (e.g., 0.5 mm BGA) is mounted in the socket 110.” Waite, [1:48-1:50].</p> <p>“FIG. 2A illustrates a motherboard 200 on which a daughter board 202 is mounted.” Waite, [4:3-4:4].</p> <p>“Referring again to FIG. 2A, the daughter board 202 includes a socket 212 into which a DUT 214 may be inserted to electrically couple the DUT 214 electrical pin-contacts to the daughter board 202.” Waite, [5:4-5:7].</p> <p>“The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.” Waite, [7:1-7:6].</p>
---	---

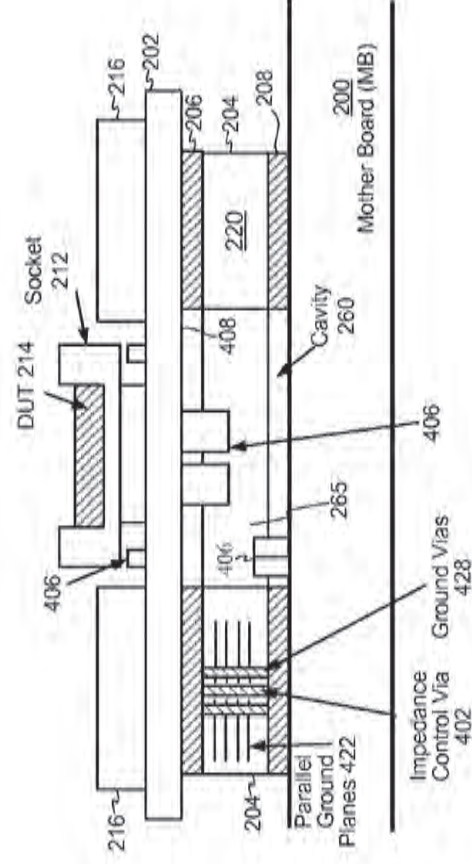
	<div><p>FIG. 4A</p></div> <p>Waite, FIG. 4A</p> <p>“In order to connect RF signals to/from DUT 214 and tuning elements 406 on the daughter board 202 with RF components and pathways located on motherboard 200, a wide band RF pathway between the DUT 214 and the motherboard 200 is provided through connector of spacer-connector 204.” Waite, [7:39-7:43].</p> <p>“As illustrated in FIG. 7, coaxial cables 702 may be used to connect elements (RF, analog, high speed digital) on the top side of the daughter board 202 to ATE test channels, test hardware or data acquisition systems (not illustrated) while allowing the tuning components 406 to be located near the DUT 214 on the underside of the daughter board 202 and/or on the</p>
--	---

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>motherboard 200 in the region between the daughter board 202 and the motherboard 200.” Waite, [9:26-9:34].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Waite discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 2A illustrates a motherboard 200 on which a daughter board 202 is mounted. Daughter board 202 is supported on the motherboard 200 by first and second spacer-connectors 204 which connectors 204 include conductive pathways discussed hereinafter.” Waite, [4:3-4:7].</p> <p>“FIG. 2B illustrates a plan view of the spacer-connector 204. A portion illustrated in FIG. 2A is enclosed within the dashed area. As can be seen from the plan view, the spacer-connector has two pad arrays 250 (or connectors) with frame elements 218 (including frame 318 and frame well 316 in FIG. 3) disposed around the pad array 250. An open area or cavity 260 may provide for access to the underside of the DUT as illustrated in FIG. 2A. The cavity 260 can be located between the pad arrays 250 and may be enclosed by a thin web of material 265.” Waite, [6:31-6:39].</p> <p>“FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled</p>

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

to pad arrays on the surface. The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper. The cavity 260 between a pair of connectors/pad arrays of spacer-connector 204 can be produced by milling out a single piece of circuit board. The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214.” Waite, [6:59-7:6].



Waite, FIG. 4A

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“The first and second connectors of spacer-connector 204 may be connected to one another by a thin web of material 265 illustrated in FIGS. 2B and 4. This web 265 is provided primarily to maintain a desired separation and registration between the first and second connectors of spacer-connector 204. Additionally, the web material 265 can provide mechanical support to inhibit the center of the daughter board 202 from excessive deflection or “spring boarding.” Additionally, the web material 265 can form a barrier to prevent contamination from getting into the spacer cavity 260.” Waite, [7:16-7:25].</p> <p>“FIG. 4B illustrates an alternative configuration where spacer-connector 204 is located on only one side of the DUT 214 and socket 212 assembly and may contain a single pad array portion as illustrated in FIG. 2C, for example. To maintain mechanical stability of the daughter board 202 a separate mechanical spacer 480 may be provided. Additionally, spacer-connector 204 and mechanical spacer 480 will cause an area 482 to be formed under the daughter board 202, which can also be used for mounting components 406.” Waite, [7:26-7:34].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
-------------------------	-------------------

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Waite discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“With reference to FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface. The body of material 220 may be formed from multiple layers of high performance printed circuit board material, FR4, for example, separated by conductive layers of, for example, copper. The cavity 260 between a pair of connectors/pad arrays of spacer-connector 204 can be produced by milling out a single piece of circuit board. The cavity 260 provides room for RF tuning components 406 and/or other components to be located immediately below the DUT 214, either on the bottom side 408 of daughter board 202 or on the top side of the motherboard 200 allowing for relatively short connections between the tuning elements 406 and the DUT 214. Pressure components 216 (e.g., stiffener blocks) may be provided as discussed above to fasten the assembly and provide a substantially homogeneous pressure across the conductive elastomers 206, 208 and connectors (pad arrays) of spacer-connector 204. It will be appreciated that the thickness of the conductive elastomers 206, 208 is greatly exaggerated and that in most embodiments, there would be no perceptible spacing between the spacer-connector 204 and the daughter board 202 and mother board 200.” Waite, [6:59-7:15].</p>
---	--

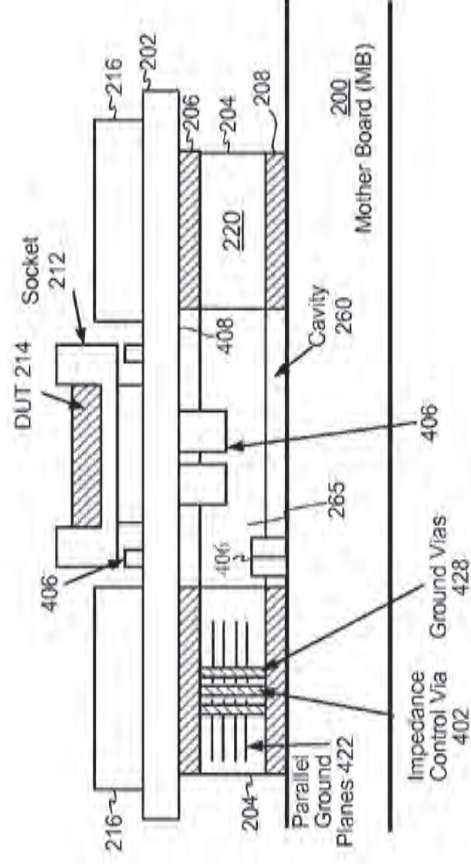


FIG. 4A

Waite, FIG. 4A

To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

Waite discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

See, e.g.:

FIG. 4A

Waite, FIG. 4A

To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Waite discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Further, the high density conductive grid of the conductive elastomers 206, 208 can accommodate misalignment of opposing mating surface pads. The density of the conductive elastomer conductive elements is chosen to ensure that a requisite number of elements make contact to a sustentative portion of each of the related pads.” Waite, [1:39-1:44].</p> <p>“Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:19-4:26].</p>

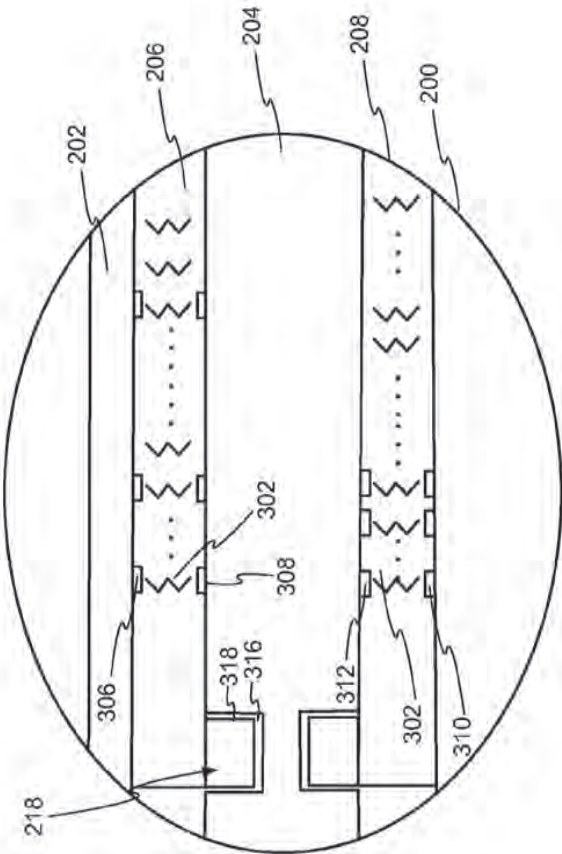


FIG. 3

Waite, FIG. 3

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:43-7:46].</p> <p>“As illustrated in FIGS. 5A and 5B, the impedance controlled/signal vias 402 surrounded by a plurality of ground vias 428 to form an RF via arrangement 508. Controlling the number and placement of the ground vias 428 around the signal via 402 maintains tight control of the pathway characteristics such as impedance, return loss, bandwidth, etc. This allows a signal to pass through the connector of spacer-connector 204 in a transparent way.” Waite, [7:46-7:54].</p> <p>“Further, it will also be appreciated that the ground and/or power pad/vias may be further arranged to provide additional isolation to a critical high frequency signals (e.g., 504). FIG. 5D illustrates another pad/via arrangement for spacer-connector 204. This configuration is similar to that of FIG. 5B, but also includes impedance controlled conductive vias 402 configured as a fully differential via set 514.” Waite, [8:35-8:41].</p> <p>“FIG. 8 also illustrates a sectional view of a multilayered PCB having a plurality of ground planes 422 separated by layers of dielectric material 424. Further, additional conductive planes/traces may be included internally (e.g., 432, 433) separated by dielectric layers for routing signals internally. Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [9:67-10:5].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	--

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

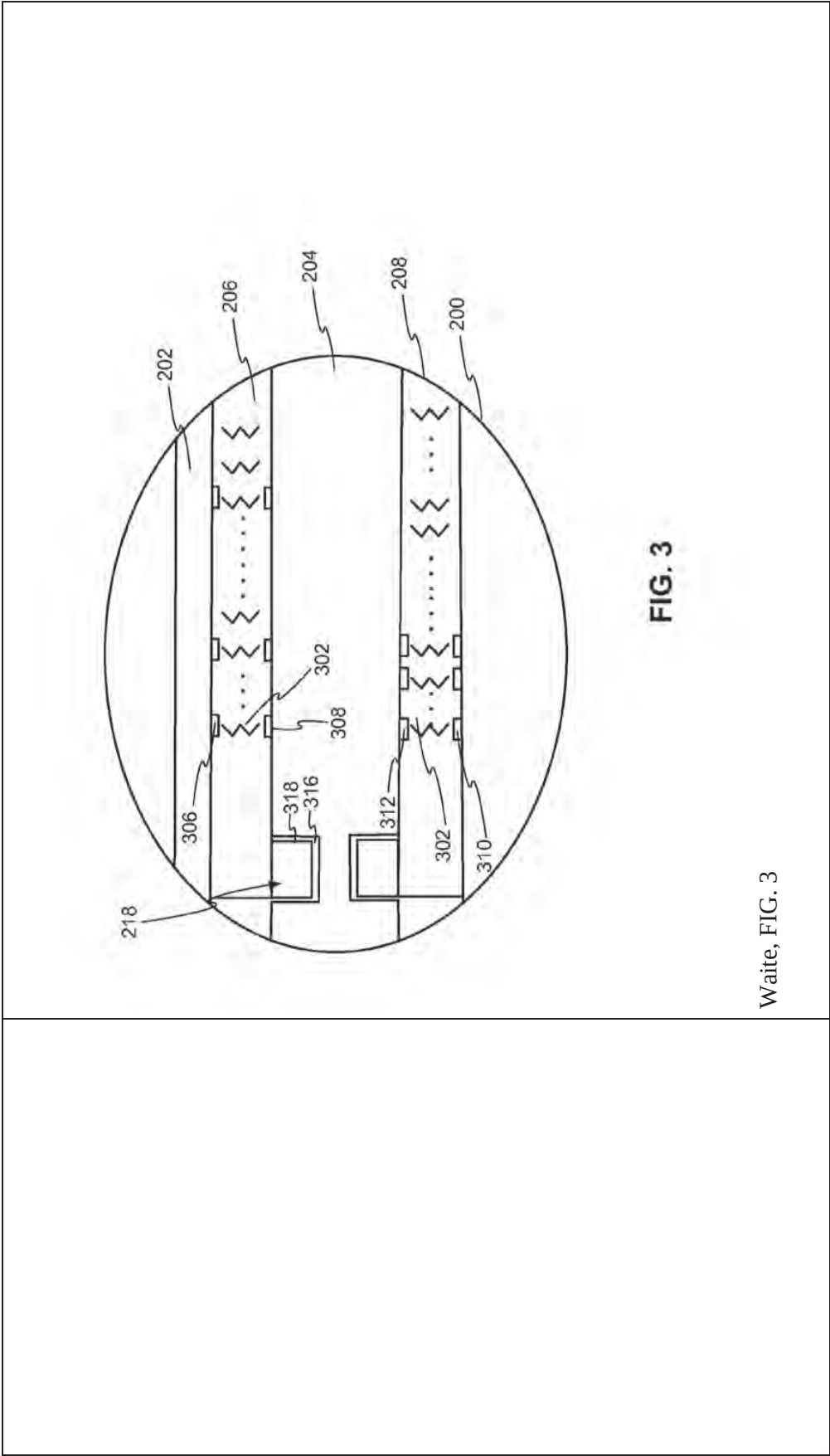
	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Waite discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Another embodiment can include a spacer-connector formed of a multilayer printed circuit board (PCB) comprising: a configurable pad array that is configured to pass signals between a first surface of the PCB and a second surface of the PCB, wherein the pad array is formed from a surface conductive layer of the PCB on respective first and second surfaces; and a plurality of conductive vias formed through the PCB, wherein the PCB includes multiple parallel ground planes.” Waite, [2:33-2:42].</p> <p>“As illustrated in FIG. 3, the first and second conductive elastomers 206, 208 each include vertically coupled conductive elements 302 in a high density grid that provide high quality coupling (e.g., low parasitic (e.g., resistance, capacitance, inductance), low noise and cross-</p>

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>talk, wide band) path. As used herein, the conductive elements 302 may include wires, balls, spheres, cubes, segments, particles, and the like, that can be utilized as a conductive path. Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:12-4:25].</p>
--	---



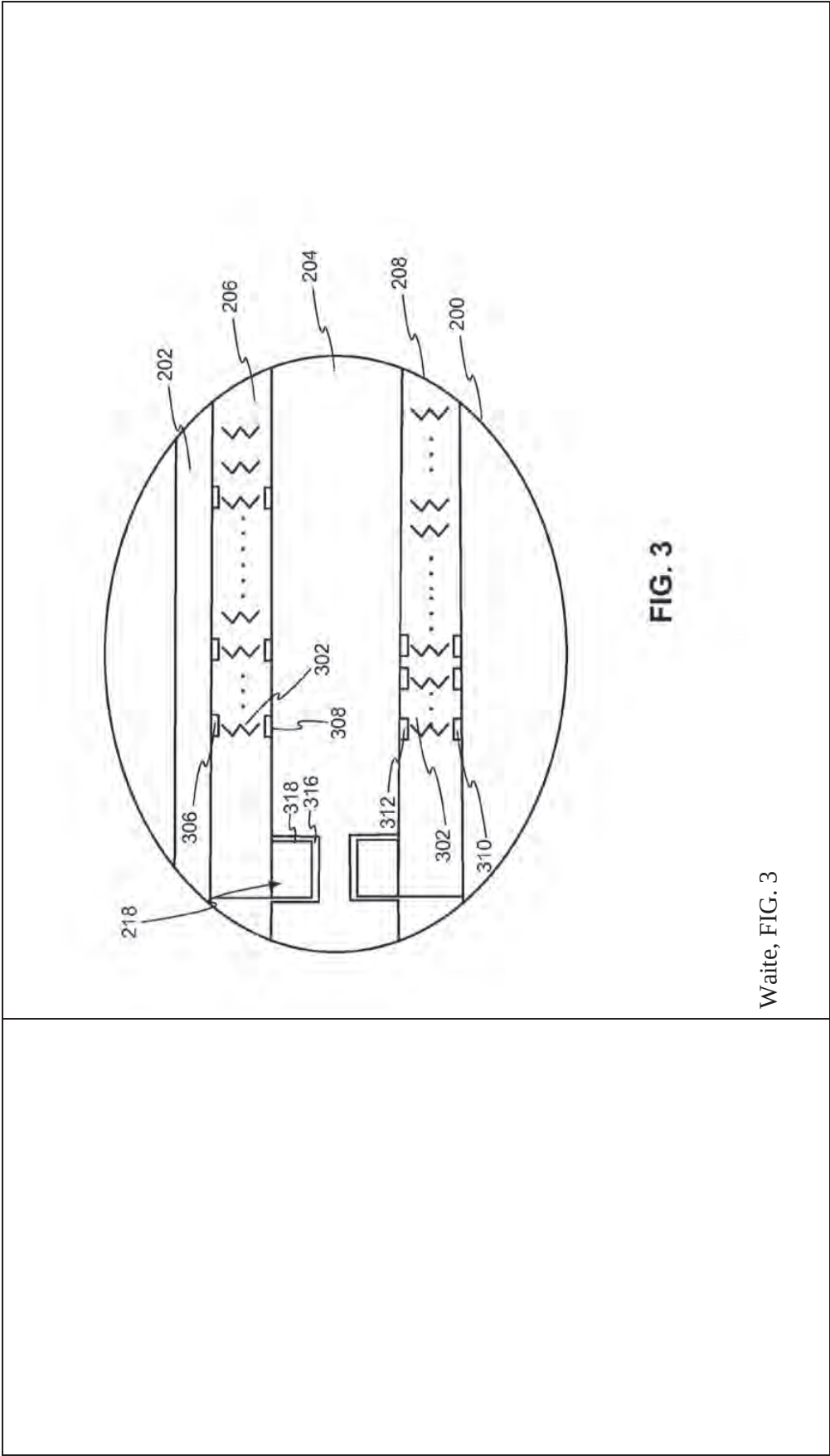
Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“With reference to FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface.” Waite, [6:59-6:62].</p> <p>“In order to connect RF signals to/from DUT 214 and tuning elements 406 on the daughter board 202 with RF components and pathways located on motherboard 200, a wide band RF pathway between the DUT 214 and the motherboard 200 is provided through connector of spacer-connector 204. The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:39-7:46].</p> <p>“The pads of the pad arrays 250 illustrated in FIGS. 5A-5C may be formed of gold-plated nickel plate on a copper pad. The overall height may be approximately 2.8 mils (0.0028 inches) as that molds more easily into the elastomer and accommodates small variations in co-planarity.” Waite, [7:58-7:62].</p> <p>“FIG. 8 also illustrates a sectional view of a multilayered PCB having a plurality of ground planes 422 separated by layers of dielectric material 424. Further, additional conductive planes/traces may be included internally (e.g., 432, 433) separated by dielectric layers for routing signals internally. Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [9:67-10:5].</p> <p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top metal pads of the plurality of metal pillars of the top package substrate via the corresponding top metal pads of the plurality of metal pillars of the spacer connector, and bottom ends of the plurality of bottom metal pillars are connected to corresponding top metal pads of the plurality of metal pillars of the top package substrate via the corresponding top metal pads of the plurality of metal pillars of the spacer connector.</p>	<p>Waite discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“As illustrated in FIG. 3, the first and second conductive elastomers 206, 208 each include vertically coupled conductive elements 302 in a high density grid that provide high quality coupling (e.g., low parasitic (e.g., resistance, capacitance, inductance), low noise and cross-talk, wide band) path. As used herein, the conductive elements 302 may include wires, balls, spheres, cubes, segments, particles, and the like, that can be utilized as a conductive path. Lower contact pads 306 of the daughter board 202 are coupled to upper contact pads 308 of the first spacer-connector 204, through the multiple conductive elements 302 of the first conductive elastomer 206. Similarly, upper contact pads 310 of the motherboard 200 are coupled to lower spacer contact pads 312 of the first connector 204 through the conductive elements 302 of the second conductive elastomer 208.” Waite, [4:12-4:25].</p>



Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>“With reference to FIG. 4A, spacer-connector 204 includes a body of material (PCB) 220 having a plurality of signal vias 402 and ground vias 428 and parallel ground planes 422 formed therein coupled to pad arrays on the surface.” Waite, [6:59-6:62].</p> <p>“The pathway through connector of spacer-connector 204 includes impedance controlled vias 402 connected to conductive pads on the surfaces of the connector of spacer-connector 204.” Waite, [7:43-7:46].</p> <p>“The impedance of vias 402 are also affected by the spacing of the ground planes in the body of material 220 (not shown), by via diameter relative to antipad 502 clearance on each ground plane and by the number and physical placement of the surrounding ground vias 428.” Waite, [8:12-8:16].</p> <p>“FIG. 8 also illustrates a sectional view of a multilayered PCB having a plurality of ground planes 422 separated by layers of dielectric material 424. Further, additional conductive planes/traces may be included internally (e.g., 432, 433) separated by dielectric layers for routing signals internally. Conductive ground vias 428 and signal vias 402, 432 can run substantially perpendicular to the ground planes 422. Each via is connected to contact pads (308, 312) affixed to it at each PCB surface.” Waite, [9:67-10:5].</p> <p>“Further it will be appreciated that in various embodiments a first contact pad may be coupled to a conductive via that may extend only partially through the PCB (e.g., 432, 434, and 436) to an internal connection point (e.g., 431, 433) and may be routed from there to one or more conductive vias (e.g., 434, 436) that couple to one or more pads that may be physically offset from the first contact pad (430).” Waite, [10:9-10:16].</p>
--	--

Appendix A-33 - Invalidity of U.S. Patent No. 9859202 in view of Waite - U.S. Patent No. 8379403

	<p>To the extent Plaintiff contends that Waite fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

U.S. Patent No.10319607 (“Wu”) is titled Package-on-Package Structure with Organic Interposer and lists Jiun Yi Wu, Yu-Min Liang, Mirmg-Ji Lii, Chien-Hsun Lee, Tsung-Ding Wang, and Jung Wei Cheng as inventors. Wu is assigned to Taiwan Semiconductor Manufacturing Company, Ltd. Wu anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Wu is a U.S. patent that was filed August 22, 2014 and published February 25, 2016. Wu is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(2).

The chart below provides representative examples of where each element of each Asserted Claim is found within Wu, or otherwise rendered obvious by disclosures and teachings of Wu, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Wu does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Wu with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Wu, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

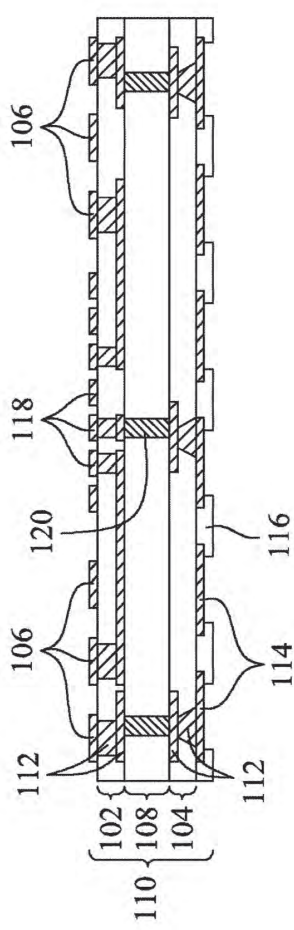
such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Wu “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

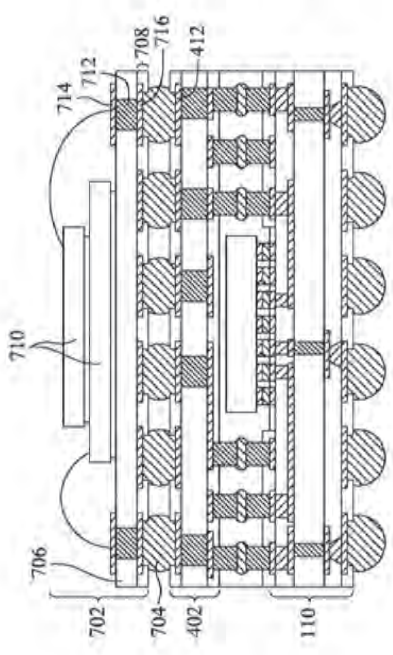
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Wu or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Wu set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Wu discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly. 3D integrated circuits are formed by stacking multiple chips. Electrical connectivity for signals and power connections from external devices are provided to various levels of the package by vertical interconnections. Described herein is a structure having reduced interconnection pitch between levels.” Wu, [2:19-2:28].</p>

	<p>“FIG. 1 is a cross-sectional view illustrating a substrate 110 according to some embodiments. The substrate 110 has a first redistribution layer (RDL) 102 and a second RDL 104 disposed on opposite sides of a substrate layer 108. The substrate layer 108 has one or more vias 120 extending from the top surface of the substrate layer 108 to the bottom surface of the substrate layer 108. The vias 120 connect conductive features 112 in the top RDL 102 to conductive features 112 in the bottom RDL 104.” Wu, [2:37-2:45].</p>  <p style="text-align: center;">Fig. 1</p> <p>Wu, FIG. 1</p> <p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the</p>
--	---

	<p>interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404.” Wu, [4:58-4:67].</p> <p>Fig. 4</p> <p>Wu, FIG. 4</p> <p>“FIG. 7 is a cross-sectional view illustrating mounting a package 702 on the interposer 402 according to some embodiments. Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702. In some embodiments, the package 702 has one or more dies 710 electrically connected to conductive features 714 that are in</p>
--	---

	<p>turn electrically connected to the lands 716 by way of vias 712 disposed in a package substrate 706.” Wu, [6:36-6:47].</p>  <p>Wu, FIG. 7</p> <p>“According to an embodiment, a device comprises a substrate having a die mounted on the first side of the substrate and a moldable underfill (MUF) disposed on the first side of the substrate and around the die. An interposer is mounted on the first side of the substrate, with the interposer having lands disposed on a first side of the interposer. The interposer mounted to the substrate by connectors bonded to a second side of the interposer, the connectors providing electrical connectivity between the interposer and the substrate. A package is mounted on the first side of the interposer and is electrically connected to the lands. At least</p>
--	--

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>one of the lands is aligned directly over the die and wherein a pitch of the connectors is different than a pitch of the lands.” Wu, [9:1-9:12].</p> <p>“According to another embodiment, a device comprises a substrate having a die disposed on a first side of the substrate and first pillars disposed on the first side of the substrate. The first pillars have a first pitch. A moldable underfill (MUF) is disposed on the first side of the substrate, with the MUF surrounding the die and each of the first pillars. An interposer is mounted over the first side of the substrate and has lands disposed on a first side of the interposer. The lands have a second pitch greater than the first pitch, and at least one of the lands is aligned directly over the die. Second pillars are disposed on a second side of the interposer, and the second pillars are bonded to the first pillars and provide electrical connectivity between the interposer and the substrate.” Wu, [9:1-9:13].</p>
[1.A] a bottom package substrate;	<p>Wu discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1 is a cross-sectional view illustrating a substrate 110 according to some embodiments. The substrate 110 has a first redistribution layer (RDL) 102 and a second RDL 104 disposed on opposite sides of a substrate layer 108. The substrate layer 108 has one or more vias 120 extending from the top surface of the substrate layer 108 to the bottom surface of the substrate layer 108. The vias 120 connect conductive features 112 in the top RDL 102 to conductive features 112 in the bottom RDL 104. The bottom RDL 104 and top RDL 102 each have one or more insulating layers with the conductive features 112 disposed therein. The top RDL 102 has one or more lands 106 disposed on the top surfaces. Die lands 118 are disposed on the top surface of the top RDL 102.” Wu, [2:38-2:51].</p>

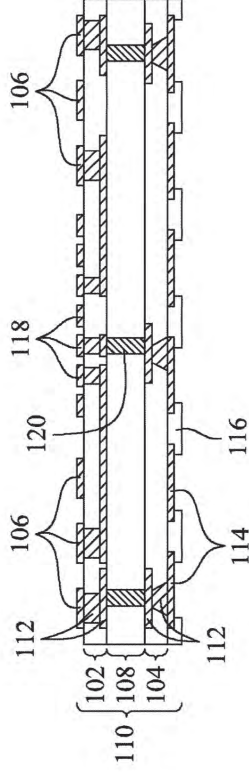


Fig. 1

Wu, FIG. 1

“The bottom RDL 104 also has lands 114 disposed on a bottom surface. In some embodiments, a protective layer 116 is disposed over the lands 114 on the bottom surface of the bottom RDL 104 and has openings exposing surfaces of the lands 114.” Wu, [2:54-2:58].

“In an embodiment, substrate 110 is formed by forming the bottom RDL 104 first, with the substrate layer 108 formed over the bottom RDL 104 and the top RDL 102 subsequently formed over the substrate layer 108. The RDLs 102 and 104 are formed by metal layer deposition and patterning by, for example, deposition of a seed layer, masking and deposition of metal over the patterned mask. The mask and exposed portions of the seed layer are removed, and a dielectric layer such as PBO, polyimide, or the like is formed around the patterned metal elements.” Wu, [2:59-3:1].

“The vias 120 are formed by plating or otherwise depositing metal in the via openings formed in the substrate layer 108. In other embodiments, the substrate layer 108 is formed first, with

the top RDL 102 and bottom RDL 104 formed on respective surfaces of the substrate layer 108. In such an embodiment, the substrate layer 108 is formed on a carrier or other support surface with bottom RDL layers (such as metal traces or copper foil) on opposite sides of the substrate layer 108.” Wu, [3:24-3:33].

“FIG. 3 is a cross-sectional view illustrating mounting a die 302 on the substrate 110 according to some embodiments. In some embodiments, the die 302 has one or more active or passive devices such as transistors, inductors, capacitors, resistors or the like disposed therein. The die 302 is attached to the die lands 118 by, for example, a flip-chip bonding technique.” Wu, [4:44-4:50].

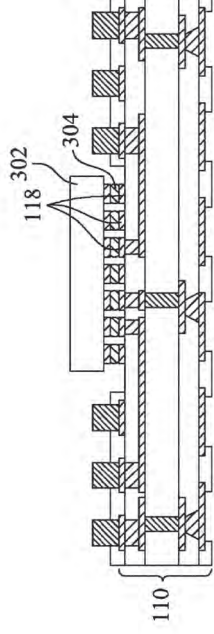
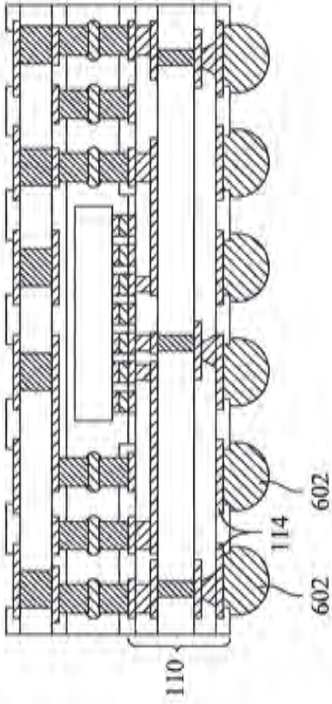
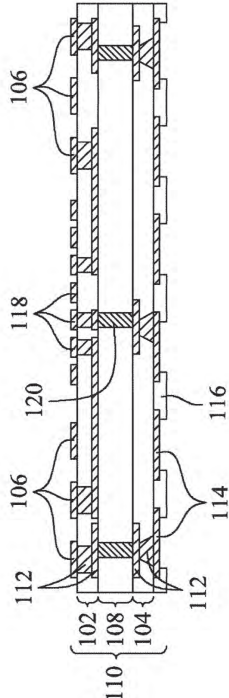


Fig. 3

Wu, FIG. 3

“FIG. 6 is a cross-sectional view illustrating mounting connectors 602 on the substrate 110 according to some embodiments. Connectors 602, such as, for example, solder balls, are mounted on the lands 114. In other embodiments, the connectors 602 are conductive bumps, pillars, studs or another conductive structure.” Wu, [6:30-6:35].

	 <p style="text-align: center;">Fig. 6</p> <p>Wu, FIG. 6</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Wu discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p> <p>“FIG. 1 is a cross-sectional view illustrating a substrate 110 according to some embodiments. The substrate 110 has a first redistribution layer (RDL) 102 and a second RDL 104 disposed</p>

	<p>on opposite sides of a substrate layer 108. The substrate layer 108 has one or more vias 120 extending from the top surface of the substrate layer 108 to the bottom surface of the substrate layer 108. The vias 120 connect conductive features 112 in the top RDL 102 to conductive features 112 in the bottom RDL 104. The bottom RDL 104 and top RDL 102 each have one or more insulating layers with the conductive features 112 disposed therein. The top RDL 102 has one or more lands 106 disposed on the top surfaces. Die lands 118 are disposed on the top surface of the top RDL 102.” Wu, [2:37-2:50].</p>  <p>The diagram is a cross-sectional view of a multi-layered substrate assembly. It shows a central substrate layer 108 with two conductive layers, a top RDL 102 and a bottom RDL 104, disposed on its opposite surfaces. The RDLs are separated by an insulating layer 110. Conductive features 112 are formed in the RDLs and extend through the insulating layer 110, connecting the top and bottom surfaces. Vias 120 are formed in the substrate layer 108, extending from the top surface to the bottom surface. Die lands 118 are formed on the top surface of the top RDL 102. The assembly is further protected by a top insulating layer 106 and a bottom insulating layer 114. A bottom RDL 104 is also shown at the bottom of the assembly.</p> <p style="text-align: center;">Fig. 1</p> <p>Wu, FIG. 1</p> <p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404.” Wu, [4:58-4:67].</p>
--	--

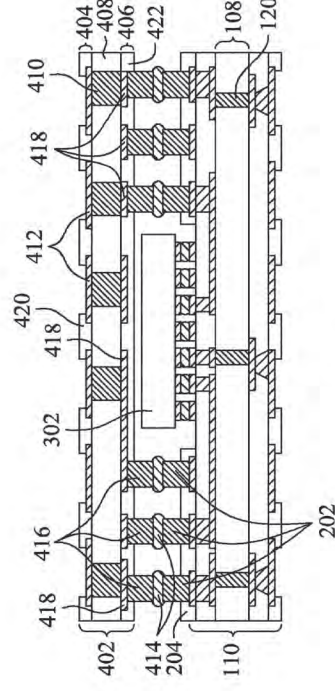


Fig. 4

Wu, FIG. 4

“FIG. 7 is a cross-sectional view illustrating mounting a package 702 on the interposer 402 according to some embodiments. Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702. In some embodiments, the package 702 has one or more dies 710 electrically connected to conductive features 714 that are in turn electrically connected to the lands 716 by way of vias 712 disposed in a package substrate 706.” Wu, [6:36-6:47].

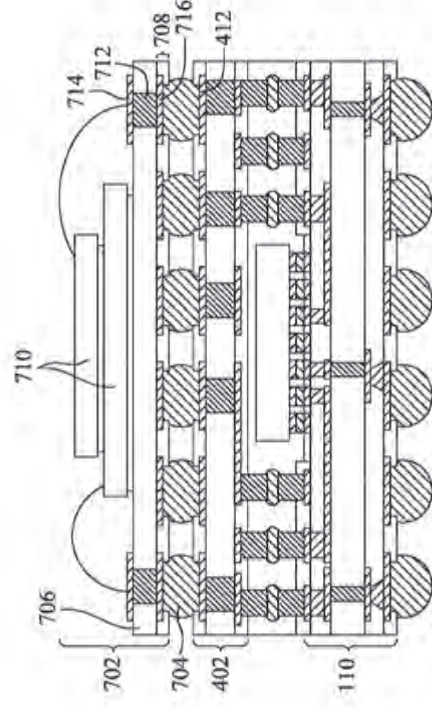


Fig. 7

Wu, FIG. 7

“FIG. 10 is a cross-sectional view illustrating mounting of the package 702 on the interposer 402 in an interposer last process according to some embodiments. The package 702 is mounted to the interposer by connectors 704, as described above.” Wu, [7:24-7:28].

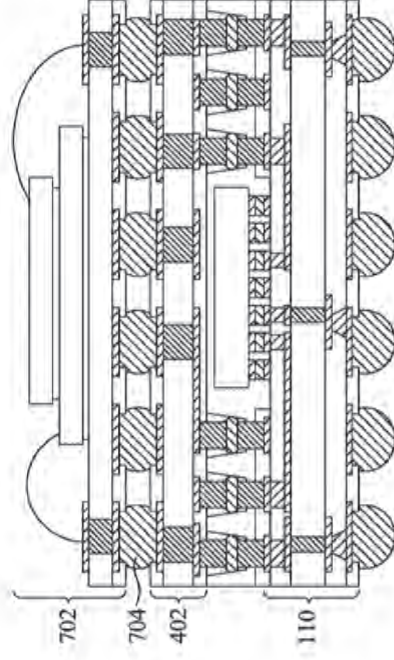


Fig. 10

Wu, FIG. 10

“According to an embodiment, a device comprises a substrate having a die mounted on the first side of the substrate and a moldable underfill (MUF) disposed on the first side of the substrate and around the die. An interposer is mounted on the first side of the substrate, with the interposer having lands disposed on a first side of the interposer. The interposer mounted to the substrate by connectors bonded to a second side of the interposer, the connectors providing electrical connectivity between the interposer and the substrate. A package is mounted on the first side of the interposer and is electrically connected to the lands.” Wu, [8:55-8:65].

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>“A method of forming a device according to an embodiment comprises mounting a die on a first side of a substrate and forming first pillars on the first side of the substrate. A moldable underfill (MUF) is applied on the first side of the substrate and surrounds the die and each of the first pillars. An interposer is mounted on the first side of the substrate by bonding second pillars on a second side of the interposer to the first pillars. The interposer has lands disposed on a first side of the interposer and at least one of the lands is aligned directly over the die. After the mounting the interposer, the first pillars and second pillars provide electrical connectivity between the interposer and the substrate. A package is mounted on the lands and the die is disposed between the first pillars.” Wu, [9:15-9:28].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Wu discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p> <p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL</p>

406 to the top RDL 404. The interposer substrate 408 is formed, in some embodiments, from an organic material such as an epoxy impregnated glass-fiber laminate, polymer impregnated glass-fiber laminate, preimpregnated composite fiber, Ajinomoto build-up film (ABF), molding compound, epoxy, PBO, polyimide or another organic material.” Wu, [4:57-5:5].

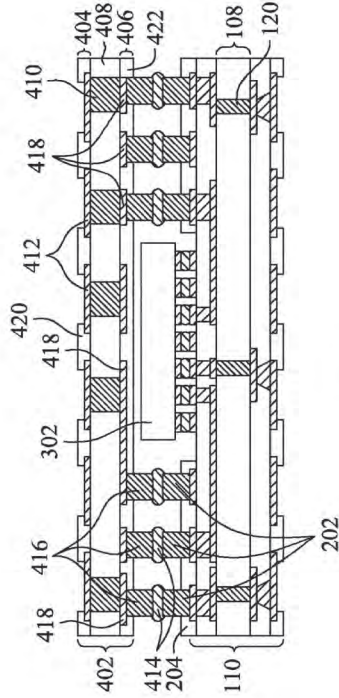


Fig. 4

Wu, FIG. 4

“FIG. 5 is a cross-sectional view illustrating application of a moldable underfill (MUF) 502 according to some embodiments. In the interposer first process, the interposer 402 is mounted to the substrate 110 and the MUF 502 is formed between the joined interposer 402 and substrate 110. In some embodiments, the MUF 502 is a molding compound, epoxy, PBO, polyimide or another moldable insulating material. The MUF 502 is injected between the interposer 402 and the substrate 110 and retained in place by way of a mold or the like during application and curing. In such an embodiment, the MUF 502 contacts the sidewalls of the pillars 202 and 416 and surrounds the pillars 202, connecting members 414 and pillars 416.

Additionally, the MUF 502 contacts and extends from the top surface of the substrate 110 to contact the bottom surface of the interposer 402. In some embodiments, the top surface of the die 302 is spaced apart from the bottom surface of the interposer 402, and a portion of the MUF 502 is disposed in the space between the die 302 and the interposer 402.” Wu, [6:10-6:28].

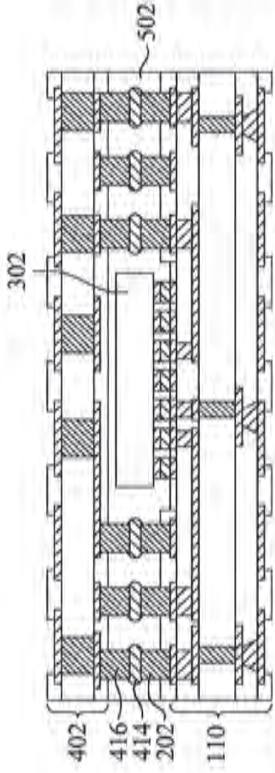


Fig. 5

Wu, FIG. 5

“FIG. 7 is a cross-sectional view illustrating mounting a package 702 on the interposer 402 according to some embodiments. Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702.” Wu, [6:36-6:43].

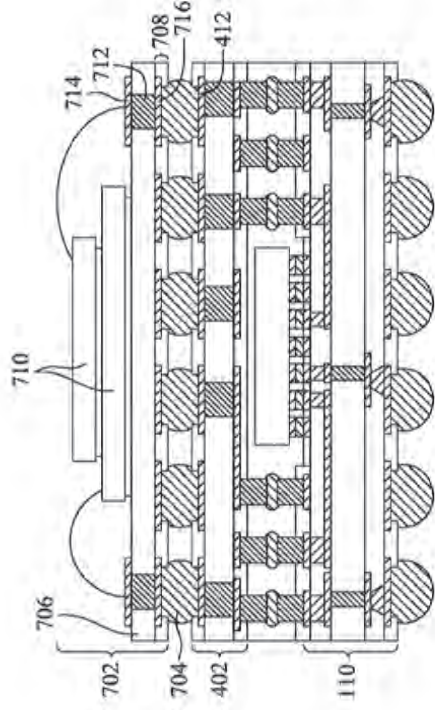


Fig. 7

Wu, FIG. 7

“FIG. 9 is a cross-sectional view illustrating mounting of the interposer 402 on the substrate 110 after formation of the MUF 802 according to some embodiments. In such embodiments, pillars 416 extend into the openings 804, with the connecting members 414 disposed in the openings 804. The sidewalls of the openings 804 are, in some embodiments, spaced apart from the sidewalls of the pillars 202 and 416.” Wu, [7:17-7:23].

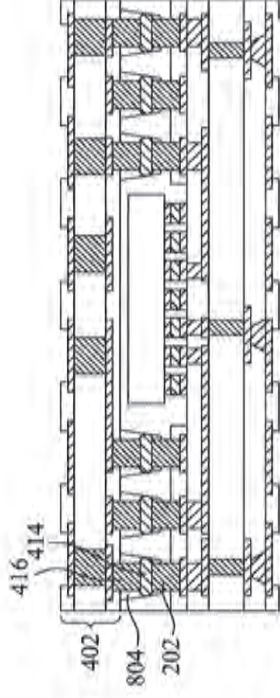


Fig. 9

Wu, FIG. 9

“FIG. 11A is a cross sectional enlarged view illustrating a MUF 802 over the die 302 and spaced apart from the interposer 402 according to some embodiments. In such embodiments, the MUF 802 is formed by the interposer last process, with the MUF 802 molded to cover the die 302. The MUF 802 is spaced apart from the bottom surface of the interposer 402 by an air gap 1104 having a distance less than the separation between the top surface of the die 302 and the bottom surface of the interposer 402. In some embodiments, the air gap 1104 helps the pillars 202 and 416 successfully bond to each other without being influenced by the height and surface uniformity of MUF 802 in the interposer last process.” Wu, [7:34-7:46].

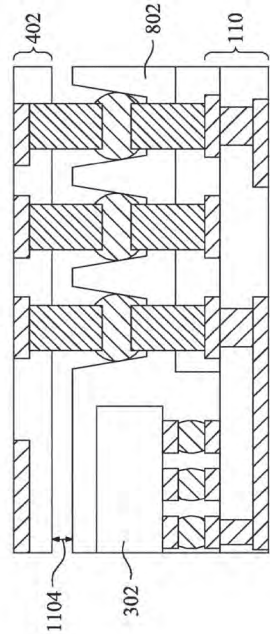


Fig. 11A

Wu, FIG. 11A

“FIG. 11B is a cross-sectional enlarged view illustrating the die 302 extending above the MUF 802 according to some embodiments. In such embodiments, the MUF is formed by the interposer last process, with the MUF 802 molded around the die 302. The die 302 has a top surface that is exposed through the top surface of the MUF 802. The MUF 802 is spaced apart from the bottom surface of the interposer 402 by an air gap 1104 having a distance equal to, or greater than, the separation between the top surface of the die 302 and the bottom surface of the interposer 402.” Wu, [7:47-7:56].

	<div> </div> <div> <p>Fig. 11B</p> </div> <div> <p>Wu, FIG. 11B</p> </div> <div> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> </div>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Wu discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, <i>e.g.</i>:</p> <p>“It has been discovered that an interposer with an organic interposer substrate 408 provides a structure with a coefficient of thermal expansion (CTE) that more closely matches the CTE of a substrate 110 than an inorganic interposer substrate 408.” Wu, [5:6-5:10].</p>

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>“However, the interposer substrate 408 is not limited to such material, as in other embodiments, the interposer substrate 408 is formed from an oxide, oxynitride, nitride, or another insulating material.” Wu, [5:13-5:16].</p> <p>“The interposer substrate 408 and vias 410 are formed, in some embodiments as described above with respect to the substrate layer 108 and vias 120. In some embodiments, the interposer substrate 408 is formed first, with the top RDL 404 and bottom RDL 406 subsequently formed, respectively, on the top surface and bottom surface of the interposer substrate 408. In other embodiments, the interposer 402 is formed by forming the top RDL 404 or bottom RDL 406 on a carrier or the like, with the interposer substrate 408 formed on the first formed RDL 404 / 406 and the remaining RDL 404 / 406 formed over the interposer substrate 408.” Wu, [5:16-5:27].</p> <p>“While the top RDL 404 and bottom RDL 406 of the interposer 402 are illustrated as each having a single layer of conductive features, the RDLs 404 and 406 are not limited to such structures, as the RDLs 404 and 406, in some embodiments, have multiple conductive features and dielectric layers.” Wu, [5:29-5:34].</p> <p>“Pillars 416 are disposed on the lands 418 and extend through the openings in the protection layer 422. In some embodiments, the pillars 416 are formed as described above with respect to the pillars 202, with the pillars 416 formed over the protection layer 422 instead of over the solder resist 204. In some embodiments, the pillars 416 on the interposer 402 are formed to have about the same size and pitch as the pillars 202 on the substrate 110, and with a complementary arrangement so that pillars 416 align with pillars 202 when the interposer 402 is mounted on the substrate 110.” Wu, [5:55-5:64].</p>
--	--

“The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404. The interposer substrate 408 is formed, in some embodiments, from an organic material such as an epoxy impregnated glass-fiber laminate, polymer impregnated glass-fiber laminate, preimpregnated composite fiber, Ajinomoto build-up film (ABF), molding compound, epoxy, PBO, polyimide or another organic material.” Wu, [7:56-7:64].

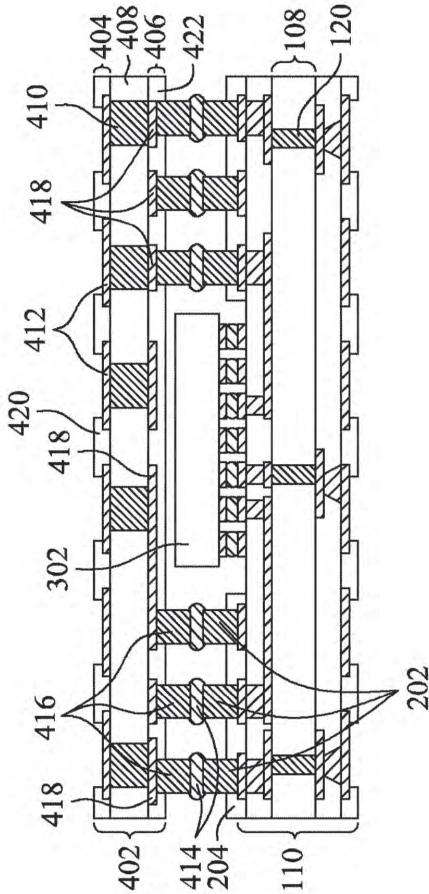


Fig. 4

Wu, FIG. 4

To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

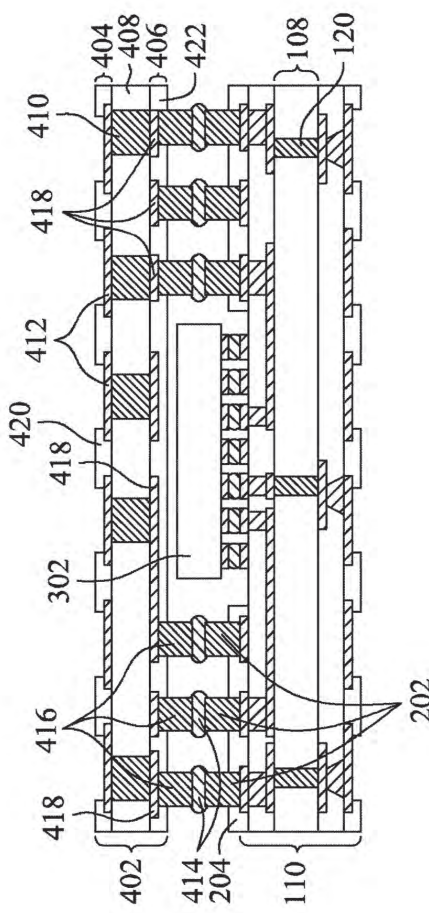
	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Wu discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The substrate layer 108 has one or more vias 120 extending from the top surface of the substrate layer 108 to the bottom surface of the substrate layer 108. The vias 120 connect conductive features 112 in the top RDL 102 to conductive features 112 in the bottom RDL 104.” Wu, [2:40-2:45].</p> <p>“The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404.” Wu, [2:41-2:46].</p> <p>“The substrate layer 108 is formed over the bottom RDL 104 and is an electrically insulating layer such as an oxide, a nitride, a molding compound, polybenzoxazole (PBO), epoxy, polyimide, polymer or the like with conductive vias 120 in the insulating layer.” Wu, [3:5-3:9].</p> <p>“In such an embodiment, the substrate layer 108 is formed with openings for the vias 120 in place, such as with a molding chase, or the substrate layer 108 is formed and via openings are formed after forming the substrate layer 108 using a process such as laser drilling, etching or the like. The vias 120 are formed by plating or otherwise depositing metal in the via openings formed in the substrate layer 108.” Wu, [3:19-3:26].</p>

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>“In some embodiments, the package 702 has one or more dies 710 electrically connected to conductive features 714 that are in turn electrically connected to the lands 716 by way of vias 712 disposed in a package substrate 706.” Wu, [6:43-6:47].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Wu discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“The substrate 110 has a first redistribution layer (RDL) 102 and a second RDL 104 disposed on opposite sides of a substrate layer 108. The substrate layer 108 has one or more vias 120 extending from the top surface of the substrate layer 108 to the bottom surface of the substrate layer 108. The vias 120 connect conductive features 112 in the top RDL 102 to conductive features 112 in the bottom RDL 104.” Wu, [2:38-2:45].</p> <p>“The bottom RDL 104 also has lands 114 disposed on a bottom surface. In some embodiments, a protective layer 116 is disposed over the lands 114 on the bottom surface of the bottom RDL 104 and has openings exposing surfaces of the lands 114.” Wu, [2:54-2:58].</p> <p>“In an embodiment, substrate 110 is formed by forming the bottom RDL 104 first, with the substrate layer 108 formed over the bottom RDL 104 and the top RDL 102 subsequently</p>

	<p>formed over the substrate layer 108. The RDLs 102 and 104 are formed by metal layer deposition and patterning by, for example, deposition of a seed layer, masking and deposition of metal over the patterned mask. The mask and exposed portions of the seed layer are removed, and a dielectric layer such as PBO, polyimide, or the like is formed around the patterned metal elements. The process is repeated to form additional layers, with the metal features in each layer aligning with metal elements in adjacent metal features to form conductive elements 112.” Wu, [2:59-3:4].</p> <p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404.” Wu, [4:58-4:67].</p> <p>“While the top RDL 404 and bottom RDL 406 of the interposer 402 are illustrated as each having a single layer of conductive features, the RDLs 404 and 406 are not limited to such structures, as the RDLs 404 and 406, in some embodiments, have multiple conductive features and dielectric layers. The conductive features in the bottom RDL 406 comprise lands 418 that are exposed at the bottom side of the interposer 402 by openings in an overlying protection layer 422. The protection layer 420 on the top RDL 404 has openings exposing lands 412 for subsequent mounting of an external device such as a die, package, board, device or the like.” Wu, [5:29-5:40].</p> <p>“Pillars 416 are disposed on the lands 418 and extend through the openings in the protection layer 422. In some embodiments, the pillars 416 are formed as described above with respect</p>
--	--

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>the pillars 202, with the pillars 416 formed over the protection layer 422 instead of over the solder resist 204.” Wu, [5:55-5:59].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Wu discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, e.g.:</p>  <p>Fig. 4</p>
	<p>Wu, FIG. 4</p>

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Wu discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404.” Wu, [4:58-4:67].</p>

702 has one or more dies 710 electrically connected to conductive features 714 that in turn electrically connected to the lands 716 by way of vias 712 disposed in a package substrate 706.” Wu, [6:36-6:47].

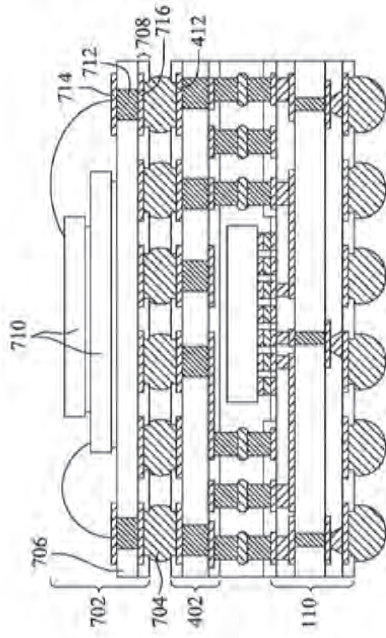


Fig. 7

Wu, FIG. 7

“In other embodiments, the package 702 is a die or chip mounted directly on the connectors 704, multiple dies or packages on the connectors 704 or another arrangement.” Wu, [6:51-6:53].

“FIG. 10 is a cross-sectional view illustrating mounting of the package 702 on the interposer 402 in an interposer last process according to some embodiments. The package 702 is mounted to the interposer by connectors 704, as described above.” Wu, [7:24-7:28].

	<div> </div> <div> <p>Fig. 10</p> </div> <div> <p>Wu, FIG. 10</p> </div> <div> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> </div>
<p>[1.1] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the</p>	<p>Wu discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

plurality of metal pillars of the spacer connector, and	<p>“FIG. 2 is a cross-sectional view illustrating formation of pillars 202 on the substrate 110 according to some embodiments. In some embodiments, the pillars 202 are formed by initially depositing a seed layer over the lands 106. The seed layer is formed from copper (Cu), titanium (Ti), aluminum (Al), an alloy of the same, or another conductive material. The seed layer is formed by, for example, electroless copper deposition, atomic layer deposition, physical vapor deposition (PVD) by sputtering Ti, Cu, or another deposition process. A mask layer is formed over the seed layer from a material such as a photoresist or the like. The mask layer is patterned to form openings exposing the lands 106 by, for example, exposing and developing a photoresist mask layer. A metal layer is formed over the patterned mask layer by, for example physical vapor deposition, electroless plating, seed layer deposition by ALD and electroplating, or by another metal formation process. In some embodiments, the deposited metal layer is planarized by, for example, a chemical-mechanical polish (CMP), grinding, etching, or the like. The planarization step removes excess deposited metal from over the patterned mask layer, leaving pillars 202. The mask layer is then removed by, for example, chemical stripping or ashing with a plasma oxygen treatment. The seed layer outside of the pillars 202 subsequently removed by etching or the like. In some embodiments, a tin (Sn) plating layer is applied over the pillars 202, with the tin reflowed after etching or otherwise removing the excess seed layer material. In some embodiments, the pillars 202 are formed with a pitch between adjacent pillars that is between about 200 μm and about 400 μm.” Wu, [3:45-4:8].</p>
---	--

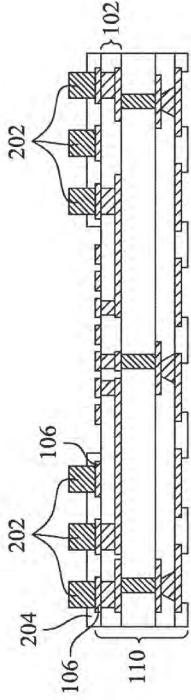


Fig. 2

Wu, FIG. 2

“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404. The interposer substrate 408 is formed, in some embodiments, from an organic material such as an epoxy impregnated glass-fiber laminate, polymer impregnated glass-fiber laminate, preimpregnated composite fiber, Ajinomoto build-up film (ABF), molding compound, epoxy, PBO, polyimide or another organic material. It has been discovered that an interposer with an organic interposer substrate 408 provides a structure with a coefficient of thermal expansion (CTE) that more closely matches the CTE of a substrate 110 than an inorganic interposer substrate 408. It should be understood that the matching of the CTEs for the interposer 402 will depend on the materials used for the substrate 110. However, the interposer substrate 408 is not limited to such material, as in

	<p>other embodiments, the interposer substrate 408 is formed from an oxide, oxynitride, nitride, or another insulating material. The interposer substrate 408 and vias 410 are formed, in some embodiments as described above with respect to the substrate layer 108 and vias 120.” Wu, [4:57-5:18].</p> <p>“In some embodiments, the interposer substrate 408 is formed first, with the top RDL 404 and bottom RDL 406 subsequently formed, respectively, on the top surface and bottom surface of the interposer substrate 408. In other embodiments, the interposer 402 is formed by forming the top RDL 404 or bottom RDL 406 on a carrier or the like, with the interposer substrate 408 formed on the first formed RDL 404 / 406 and the remaining RDL 404 / 406 formed over the interposer substrate 408. The RDLs 404 and 406 are formed as described above with respect to RDLs 102 and 104. While the top RDL 404 and bottom RDL 406 of the interposer 402 are illustrated as each having a single layer of conductive features, the RDLs 404 and 406 are not limited to such structures, as the RDLs 404 and 406, in some embodiments, have multiple conductive features and dielectric layers. The conductive features in the bottom RDL 406 comprise lands 418 that are exposed at the bottom side of the interposer 402 by openings in an overlying protection layer 422. The protection layer 420 on the top RDL 404 has openings exposing lands 412 for subsequent mounting of an external device such as a die, package, board, device or the like. It has been discovered that the interposer 402 having lands 412 on the top surface that are disposed over the die 302 permits connectors for subsequently formed devices to have a pitch that is different than the pitch of the pillars 416. In particular, a larger pitch for the lands 412 permits greater spacing of the connectors on the lands 412, preventing solder bridging between adjacent connectors, and permitting larger connectors. Additionally, the lands 412 being disposed over the die 302 allows for a greater number of lands 412 and associated connectors than the number of pillars 416. In some embodiments, the lands 412 have exposed regions with a diameter between about 200 μm and about 400 μm and a pitch between about 350 μm and about 650 μm. Pillars</p>
--	---

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>416 are disposed on the lands 418 and extend through the openings in the protection layer 422. In some embodiments, the pillars 416 are formed as described above with respect to pillars 202, with the pillars 416 formed over the protection layer 422 instead of over the solder resist 204. In some embodiments, the pillars 416 on the interposer 402 are formed to have about the same size and pitch as the pillars 202 on the substrate 110, and with a complementary arrangement so that pillars 416 align with pillars 202 when the interposer 402 is mounted on the substrate 110. The interposer 402 is mounted to the substrate 110 by aligning the pillars 416 over the pillars 202 and bonding the aligned pairs of pillars 202 and 416 to each other. In some embodiments, a connecting member 414, such as a solder cap, tin layer, or other conductive material is used to joining the aligned ends of the pillars 202 and 416.” Wu, [5:19-6:3].</p> <p>“FIG. 9 is a cross-sectional view illustrating mounting of the interposer 402 on the substrate 110 after formation of the MUF 802 according to some embodiments. In such embodiments, pillars 416 extend into the openings 804, with the connecting members 414 disposed in the openings 804. The sidewalls of the openings 804 are, in some embodiments, spaced apart from the sidewalls of the pillars 202 and 416.” Wu, [7:17-7:23].</p>
--	--

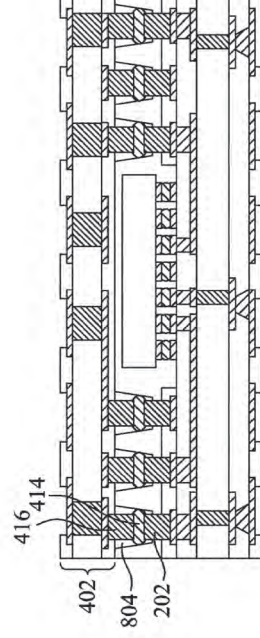
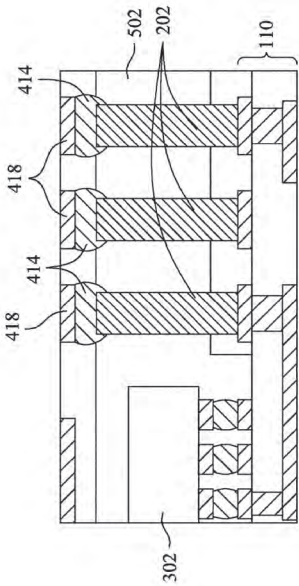
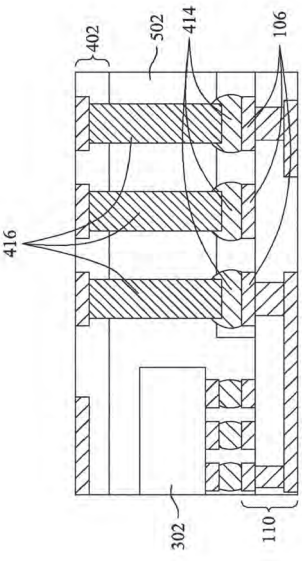


Fig. 9

Wu, FIG. 9

“FIG. 12A is a cross-sectional enlarged view illustrating an alternative pillar 202 arrangement according to some embodiments. The pillars 202 are formed on the substrate 110 and extend above the top surface of the die 302. The connecting members 414 bond the pillars 202 to the lands 418 on the bottom surface of the interposer 402.” Wu, [8:26-8:32]

	<div>A cross-sectional diagram of a semiconductor device. It shows a substrate 110 at the bottom. Above it is a layer 106. On top of layer 106 are several pillars 416. Between the pillars are connecting members 414. Above the pillars is a layer 502. A die 302 is shown on the left, with its top surface below the pillars. Labels 418 point to the pillars 416. Labels 202 point to the connecting members 414.</div> <div><p>Fig. 12A</p></div> <div><p>Wu, FIG. 12A</p></div> <div><p>“FIG. 12B is a cross-sectional enlarged view illustrating an alternative pillar 416 arrangement according to some embodiments. The pillars 416 are formed on the interposer 402 and extend below the top surface of the die 302. The connecting members 414 directly bond the pillars 416 to the lands 106 on the top surface of the substrate 110.” Wu, [8:33-8:38].</p></div>
--	---

	 <p>Fig. 12B</p> <p>Wu, FIG. 12B</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Wu discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p> <p>“The substrate 110 has a first redistribution layer (RDL) 102 and a second RDL 104 disposed on opposite sides of a substrate layer 108. The substrate layer 108 has one or more vias 120 extending from the top surface of the substrate layer 108 to the bottom surface of the substrate</p>

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>layer 108. The vias 120 connect conductive features 112 in the top RDL 102 to conductive features 112 in the bottom RDL 104.” Wu, [2:38-2:45].</p> <p>“In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404.” Wu, [4:60-4:67].</p> <p>“In some embodiments, the pillars 416 on the interposer 402 are formed to have about the same size and pitch as the pillars 202 on the substrate 110, and with a complementary arrangement so that pillars 416 align with pillars 202 when the interposer 402 is mounted on the substrate 110. The interposer 402 is mounted to the substrate 110 by aligning the pillars 416 over the pillars 202 and bonding the aligned pairs of pillars 202 and 416 to each other. In some embodiments, a connecting member 414, such as a solder cap, tin layer, or other conductive material is used to joining the aligned ends of the pillars 202 and 416.” Wu, [5:60-6:3].</p> <p>“Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702. In some embodiments, the package 702 has one or more dies 710 electrically connected to conductive features 714 that are in turn electrically connected to the lands 716 by way of vias 712 disposed in a package substrate 706.” Wu, [6:38-6:47].</p>
--	---

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>“The pillars 202 are formed on the substrate 110 and extend above the top surface of the die 302. The connecting members 414 bond the pillars 202 to the lands 418 on the bottom surface of the interposer 402.” Wu, [8:28-8:32].</p> <p>“The pillars 416 are formed on the interposer 402 and extend below the top surface of the die 302. The connecting members 414 directly bond the pillars 416 to the lands 106 on the top surface of the substrate 110.” Wu, [8:35-8:38].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Wu discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404. The interposer substrate 408 is formed, in some embodiments, from an organic material such as an epoxy impregnated glass-fiber laminate, polymer impregnated glass-fiber laminate, preimpregnated composite fiber, Ajinomoto build-up film (ABF),</p>

	<p>molding compound, epoxy, PBO, polyimide or another organic material. It has been discovered that an interposer with an organic interposer substrate 408 provides a structure with a coefficient of thermal expansion (CTE) that more closely matches the CTE of a substrate 110 than an inorganic interposer substrate 408. It should be understood that the matching of the CTEs for the interposer 402 will depend on the materials used for the substrate 110. However, the interposer substrate 408 is not limited to such material, as in other embodiments, the interposer substrate 408 is formed from an oxide, oxynitride, nitride, or another insulating material. The interposer substrate 408 and vias 410 are formed, in some embodiments as described above with respect to the substrate layer 108 and vias 120. In some embodiments, the interposer substrate 408 is formed first, with the top RDL 404 and bottom RDL 406 subsequently formed, respectively, on the top surface and bottom surface of the interposer substrate 408. In other embodiments, the interposer 402 is formed by forming the top RDL 404 or bottom RDL 406 on a carrier or the like, with the interposer substrate 408 formed on the first formed RDL 404 / 406 and the remaining RDL 404 / 406 formed over the interposer substrate 408. The RDLs 404 and 406 are formed as described above with respect to RDLs 102 and 104. While the top RDL 404 and bottom RDL 406 of the interposer 402 are illustrated as each having a single layer of conductive features, the RDLs 404 and 406 are not limited to such structures, as the RDLs 404 and 406, in some embodiments, have multiple conductive features and dielectric layers. The conductive features in the bottom RDL 406 comprise lands 418 that are exposed at the bottom side of the interposer 402 by openings in an overlying protection layer 422. The protection layer 420 on the top RDL 404 has openings exposing lands 412 for subsequent mounting of an external device such as a die, package, board, device or the like. It has been discovered that the interposer 402 having lands 412 on the top surface that are disposed over the die 302 permits connectors for subsequently formed devices to have a pitch that is different than the pitch of the pillars 416. In particular, a larger pitch for the lands 412 permits greater spacing of the connectors on the lands 412, preventing solder bridging between adjacent connectors, and permitting larger connectors. Additionally,</p>
--	--

	<p>the lands 412 being disposed over the die 302 allows for a greater number of lands 412 and associated connectors than the number of pillars 416.” Wu, [4:58-5:51].</p> <div><p>The diagram is a cross-sectional view of a semiconductor assembly. At the bottom is a substrate 110. On top of the substrate are several pillars 202. A die 302 is mounted on top of the pillars. The die has lands 412 on its top surface. A moldable underfill (MUF) 502 is applied between the die and the substrate. The MUF 502 is shown as a hatched region. It is disposed over the lands 412 and around the pillars 202. The MUF 502 is shown to be in contact with the top surface of the substrate 110 and the bottom surface of the die 302. Other labels include 418, 416, 414, 204, 402, 404, 406, 408, 420, 418, 412, 410, 108, and 120.</p></div> <p>Fig. 4</p> <p>Wu, FIG. 4</p> <p>“FIG. 5 is a cross-sectional view illustrating application of a moldable underfill (MUF) 502 according to some embodiments. In the interposer first process, the interposer 402 is mounted to the substrate 110 and the MUF 502 is formed between the joined interposer 402 and substrate 110. In some embodiments, the MUF 502 is a molding compound, epoxy, PBO, polyimide or another moldable insulating material. The MUF 502 is injected between the interposer 402 and the substrate 110 and retained in place by way of a mold or the like during application and curing. In such an embodiment, the MUF 502 contacts the sidewalls of the pillars 202 and 416 and surrounds the pillars 202, connecting members 414 and pillars 416. Additionally, the MUF 502 contacts and extends from the top surface of the substrate 110 to contact the bottom surface of the interposer 402. In some embodiments, the top surface of the die 302 is spaced apart from the bottom surface of the interposer 402, and a portion of the</p>
--	---

MUF 502 is disposed in the space between the die 302 and the interposer 402.” Wu, [6:10-6:28].

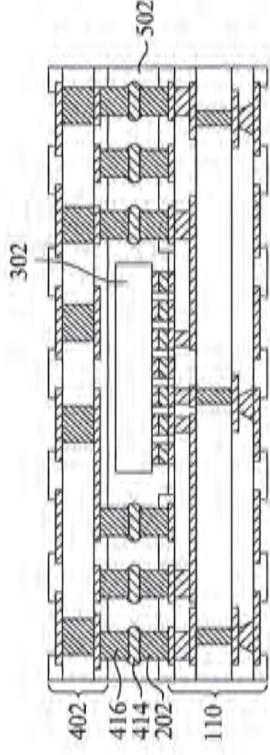


Fig. 5

Wu, FIG. 5

“FIG. 7 is a cross-sectional view illustrating mounting a package 702 on the interposer 402 according to some embodiments. Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702. In some embodiments, the package 702 has one or more dies 710 electrically connected to conductive features 714 that are in turn electrically connected to the lands 716 by way of vias 712 disposed in a package substrate 706. While the package 702 is illustrated herein as having a substrate 706 with dies 710 disposed thereon, the structure is not limited to having such a package 702 with such an arrangement. In other embodiments, the package 702 is a die or chip mounted directly on the

connectors 704, multiple dies or packages on the connectors 704 or another arrangement.”
Wu, [6:36-6:53].

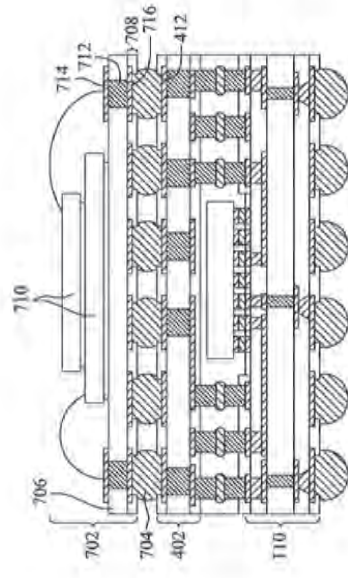
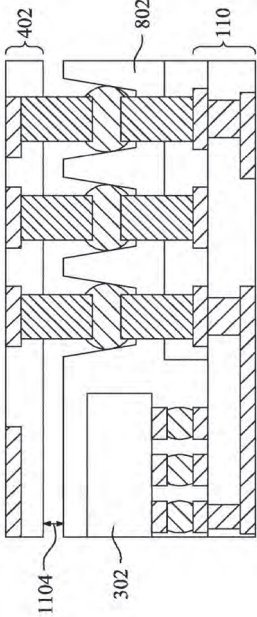


Fig. 7

Wu, FIG. 7

“FIG. 11A is a cross sectional enlarged view illustrating a MUF 802 over the die 302 and spaced apart from the interposer 402 according to some embodiments. In such embodiments, the MUF 802 is formed by the interposer last process, with the MUF 802 molded to cover the die 302. The MUF 802 is spaced apart from the bottom surface of the interposer 402 by an air gap 1104 having a distance less than the separation between the top surface of the die 302 and the bottom surface of the interposer 402.” Wu, [7:34-7:43].

	<div><p>The diagram is a cross-sectional view of a mold assembly. It shows a die 302 (hatched) positioned within a mold cavity. Above the die is a MUF 802 (hatched). The MUF 802 is spaced apart from the bottom surface of the interposer 402 by an air gap 1104. The interposer 402 is shown as a series of vertical pillars. The top surface of the interposer 402 is labeled 402, and the bottom surface is labeled 110. The die 302 is labeled 302.</p></div> <div><p>Fig. 11A</p></div> <div><p>Wu, FIG. 11A</p></div> <div><p>“FIG. 11B is a cross-sectional enlarged view illustrating the die 302 extending above the MUF 802 according to some embodiments. In such embodiments, the MUF is formed by the interposer last process, with the MUF 802 molded around the die 302. The die 302 has a top surface that is exposed through the top surface of the MUF 802. The MUF 802 is spaced apart from the bottom surface of the interposer 402 by an air gap 1104 having a distance equal to, or greater than, the separation between the top surface of the die 302 and the bottom surface of the interposer 402.” Wu, [7:47-7:56].</p></div>
--	---

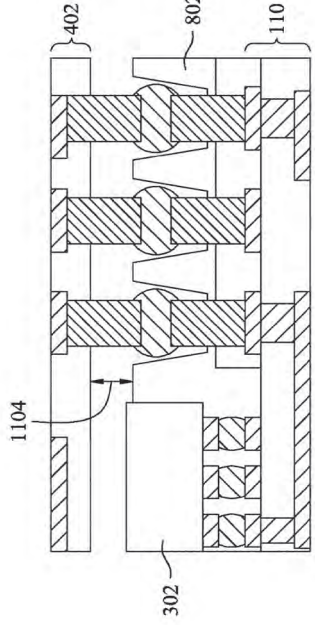
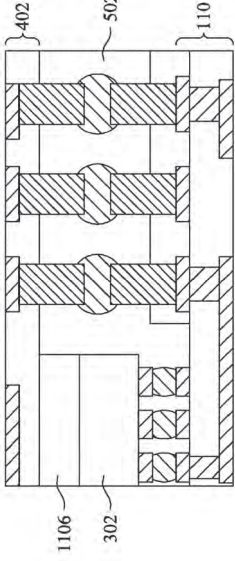


Fig. 11B

Wu, FIG. 11B

“FIG. 11C is a cross-sectional enlarged view illustrating a die attachment film (DAF) 1106 disposed on the top surface of the die 302 according to some embodiments. In some embodiments, the die 302 is attached to the interposer prior to the die 302 being mounted to the substrate 110. In such embodiments, the die 302 is mounted to the substrate 110 when the interposer 402 is mounted to the substrate 110. In other embodiments, the DAF 1106 is applied to the die 302 or to the interposer after the die 302 is mounted to the substrate 110 and prior to the interposer 402 being mounted to the substrate 110. The die 302 is bonded to the interposer 402 by the DAF 1106 when the interposer 402 is mounted to the substrate 110.” Wu, [7:57-8:2].

	 <p style="text-align: center;">Fig. 11C</p> <p>Wu, FIG. 11C</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Wu discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 3 is a cross-sectional view illustrating mounting a die 302 on the substrate 110 according to some embodiments. In some embodiments, the die 302 has one or more active or passive devices such as transistors, inductors, capacitors, resistors or the like disposed therein. The die 302 is attached to the die lands 118 by, for example, a flip-chip bonding technique. In some embodiments, connectors 304 are disposed between contact pads on the</p>

die 302 and the die lands 118. The connectors 304 bond the die 302 to the die lands 118 while providing electrical connections between the die 302 and the die lands 118.” Wu, [4:43-4:53].

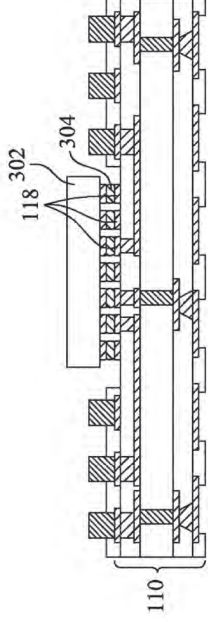
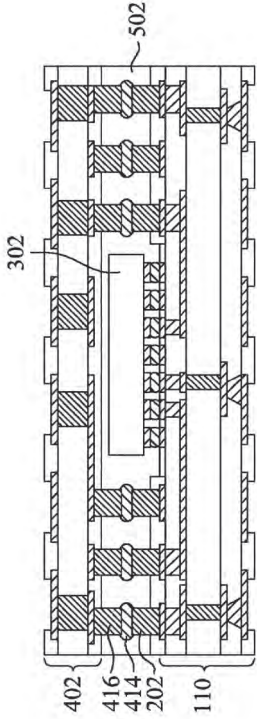


Fig. 3

Wu, FIG. 3

“FIG. 5 is a cross-sectional view illustrating application of a moldable underfill (MUF) 502 according to some embodiments. In the interposer first process, the interposer 402 is mounted to the substrate 110 and the MUF 502 is formed between the joined interposer 402 and substrate 110. In some embodiments, the MUF 502 is a molding compound, epoxy, PBO, polyimide or another moldable insulating material. The MUF 502 is injected between the interposer 402 and the substrate 110 and retained in place by way of a mold or the like during application and curing. In such an embodiment, the MUF 502 contacts the sidewalls of the pillars 202 and 416 and surrounds the pillars 202, connecting members 414 and pillars 416. Additionally, the MUF 502 contacts and extends from the top surface of the substrate 110 to contact the bottom surface of the interposer 402. In some embodiments, the top surface of the die 302 is spaced apart from the bottom surface of the interposer 402, and a portion of the MUF 502 is disposed in the space between the die 302 and the interposer 402. In some

	<p>embodiments, a portion of the MUF 502 extends between the die 302 and the substrate 110.” Wu, [6:10-6:29].</p>  <p>Fig. 5</p> <p>Wu, FIG. 5</p> <p>“FIG. 8 is a cross-sectional view illustrating formation of an MUF 802 prior to mounting the interposer 402 according to some embodiments. The MUF 802 is formed after the die 302 is mounted to the substrate 110 as shown in FIGS. 1 and 3, and in some embodiments, the MUF 802 is also formed after formation of the pillars 202 as shown in FIG.” Wu, [6:60-6:66].</p>
--	---

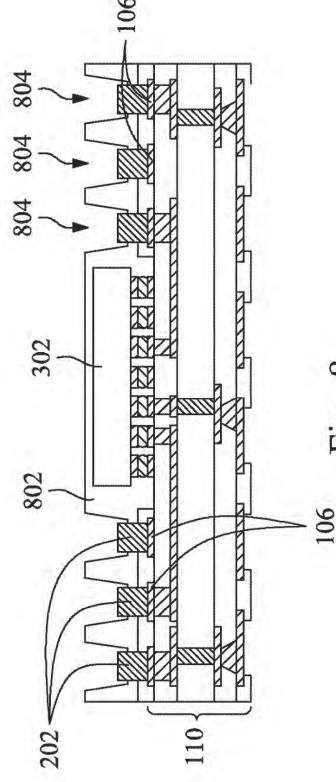
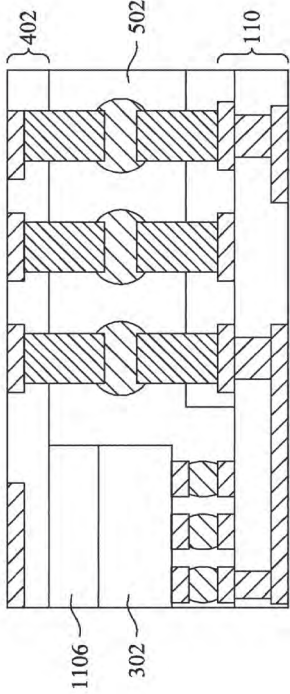
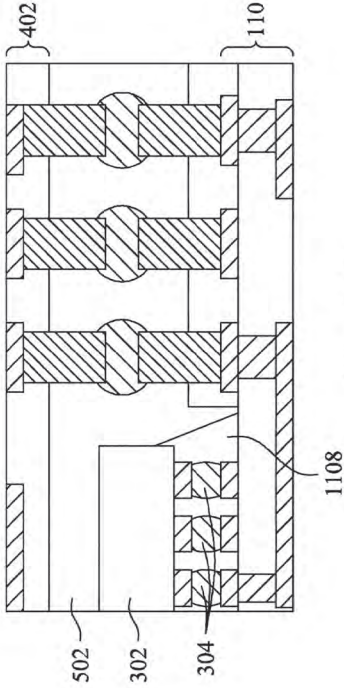


Fig. 8

Wu, FIG. 8

“FIG. 11C is a cross-sectional enlarged view illustrating a die attachment film (DAF) 110C disposed on the top surface of the die 302 according to some embodiments. In some embodiments, the die 302 is attached to the interposer prior to the die 302 being mounted to the substrate 110. In such embodiments, the die 302 is mounted to the substrate 110 when the interposer 402 is mounted to the substrate 110. In other embodiments, the DAF 110C is applied to the die 302 or to the interposer after the die 302 is mounted to the substrate 110 and prior to the interposer 402 being mounted to the substrate 110.” Wu, [7:57-7:67].

	<div><p>The diagram is a cross-sectional view of a substrate assembly. It shows a top layer 1106, a middle layer 302, and a bottom layer 110. There are three vertical vias or pillars, each labeled 502, extending from the middle layer 302 through the bottom layer 110. The vias are filled with a material, and the space between them is also filled. A bracket 402 is shown at the top of the vias, indicating a specific region or layer.</p></div> <div><p>Fig. 11C</p></div> <div><p>Wu, FIG. 11C</p></div> <div><p>“FIG. 11D is a cross-sectional enlarged view illustrating an underfill (UF) 1108 disposed between the die 302 and the substrate 110. The UF 1108 is a molding compound, epoxy, PBO, polyimide or another moldable insulating material, and in some embodiments, the UF 1108 is a different material than the MUF 502. In some embodiments the UF 1108 is dispensed along the bottom edge of the die 302, so that the UF 1108 will flow and fill the space in between the bottom of die 302 and the substrate 110 through capillary effect.” Wu, [8:6-8:15].</p></div>
--	---

	 <p>Fig. 11D</p> <p>Wu, FIG. 11D</p> <p>“A method of forming a device according to an embodiment comprises mounting a die on a first side of a substrate and forming first pillars on the first side of the substrate.” Wu, [9:15-9:17].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Wu discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>

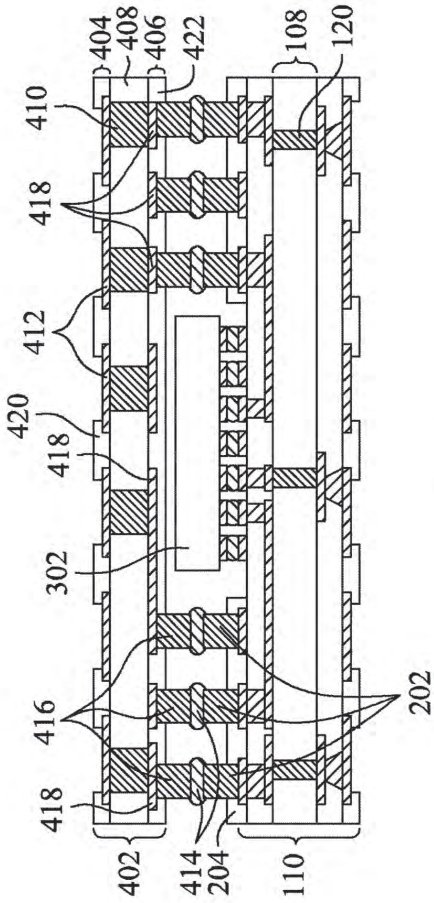


Fig. 4

Wu, FIG. 4

To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Wu discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In some embodiments, the top surface of the die 302 is spaced apart from the bottom surface of the interposer 402, and a portion of the MUF 502 is disposed in the space between the die 302 and the interposer 402.” Wu, [6:24-6:28].</p> <p>“In such embodiments, the MUF 802 is formed by the interposer last process, with the MUF 802 molded to cover the die 302. The MUF 802 is spaced apart from the bottom surface of the interposer 402 by an air gap 1104 having a distance less than the separation between the top surface of the die 302 and the bottom surface of the interposer 402.” Wu, [7:37-7:43].</p> <p>“In such embodiments, the MUF is formed by the interposer last process, with the MUF 802 molded around the die 302. The die 302 has a top surface that is exposed through the top surface of the MUF 802. The MUF 802 is spaced apart from the bottom surface of the interposer 402 by an air gap 1104 having a distance equal to, or greater than, the separation between the top surface of the die 302 and the bottom surface of the interposer 402.” Wu, [7:49-7:56].</p> <p>“The die 302 has a top surface that is exposed through the top surface of the MUF 802. The MUF 802 is spaced apart from the bottom surface of the interposer 402 by an air gap 1104</p>

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>having a distance equal to, or greater than, the separation between the top surface of the die 302 and the bottom surface of the interposer 402.” Wu, [7:51-7:56].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Wu discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“In some embodiments, the die 302 has one or more active or passive devices such as transistors, inductors, capacitors, resistors or the like disposed therein. The die 302 is attached to the die lands 118 by, for example, a flip-chip bonding technique. In some embodiments, connectors 304 are disposed between contact pads on the die 302 and the die lands 118. The connectors 304 bond the die 302 to the die lands 118 while providing electrical connections between the die 302 and the die lands 118. In some embodiments, the connectors 304 are</p>

	<p>solder balls, controlled collapse chip connections (C 4), a land grid array, microbumps, pillars, studs, or the like.” Wu, [4:45-4:57].</p> <p>“It has been discovered that the interposer 402 having lands 412 on the top surface that are disposed over the die 302 permits connectors for subsequently formed devices to have a pitch that is different than the pitch of the pillars 416. In particular, a larger pitch for the lands 412 permits greater spacing of the connectors on the lands 412, preventing solder bridging between adjacent connectors, and permitting larger connectors. Additionally, the lands 412 being disposed over the die 302 allows for a greater number of lands 412 and associated connectors than the number of pillars 416.” Wu, [5:41-5:51].</p> <p>“In some embodiments, the top surface of the die 302 is spaced apart from the bottom surface of the interposer 402, and a portion of the MUF 502 is disposed in the space between the die 302 and the interposer 402.” Wu, [6:24-6:28].</p> <p>“FIG. 7 is a cross-sectional view illustrating mounting a package 702 on the interposer 402 according to some embodiments. Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702. In some embodiments, the package 702 has one or more dies 710 electrically connected to conductive features 714 that are in turn electrically connected to the lands 716 by way of vias 712 disposed in a package substrate 706. While the package 702 is illustrated herein as having a substrate 706 with dies 710 disposed thereon, the structure is not limited to having such a package 702 with such an arrangement.” Wu, [6:36-6:51].</p>
--	---

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>“While the package 702 is illustrated herein as having a substrate 706 with dies 710 disposed thereon, the structure is not limited to having such a package 702 with such an arrangement. In other embodiments, the package 702 is a die or chip mounted directly on the connectors 704, multiple dies or packages on the connectors 704 or another arrangement.” Wu, [6:48-6:53].</p> <p>“FIG. 10 is a cross-sectional view illustrating mounting of the package 702 on the interposer 402 in an interposer last process according to some embodiments. The package 702 is mounted to the interposer by connectors 704, as described above.” Wu, [7:24-7:28].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>Wu discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

plurality of top metal pillars of the bottom package substrate.	<p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110.” Wu, [4:58-4:63].</p> <p>“In some embodiments, the pillars 416 on the interposer 402 are formed to have about the same size and pitch as the pillars 202 on the substrate 110, and with a complementary arrangement so that pillars 416 align with pillars 202 when the interposer 402 is mounted on the substrate 110. The interposer 402 is mounted to the substrate 110 by aligning the pillars 416 over the pillars 202 and bonding the aligned pairs of pillars 202 and 416 to each other.” Wu, [5:60-5:67].</p> <p>“In some embodiments, the pillars 416 on the interposer 402 are formed to have about the same size and pitch as the pillars 202 on the substrate 110, and with a complementary arrangement so that pillars 416 align with pillars 202 when the interposer 402 is mounted on the substrate 110. The interposer 402 is mounted to the substrate 110 by aligning the pillars 416 over the pillars 202 and bonding the aligned pairs of pillars 202 and 416 to each other. In some embodiments, a connecting member 414, such as a solder cap, tin layer, or other conductive material is used to joining the aligned ends of the pillars 202 and 416.” Wu, [5:60-6:3].</p> <p>“The pillars 202 and 416 are then brought together, and the connecting member 414 is subjected to heat and/or pressure to reflow the material of the connecting member 414 or otherwise bond the aligned pairs of pillars 202 and 416.” Wu, [6:5-6:9].</p> <p>“Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically</p>
---	---

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702.” Wu, [6:38-6:43].</p> <p>“FIG. 9 is a cross-sectional view illustrating mounting of the interposer 402 on the substrate 110 after formation of the MUF 802 according to some embodiments. In such embodiments, pillars 416 extend into the openings 804, with the connecting members 414 disposed in the openings 804.” Wu, [7:17-7:21].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Wu discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

<p>pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404. The interposer substrate 408 is formed, in some embodiments, from an organic material such as an epoxy impregnated glass-fiber laminate, polymer impregnated glass-fiber laminate, preimpregnated composite fiber, Ajinomoto build-up film (ABF), molding compound, epoxy, PBO, polyimide or another organic material. It has been discovered that an interposer with an organic interposer substrate 408 provides a structure with a coefficient of thermal expansion (CTE) that more closely matches the CTE of a substrate 110 than an inorganic interposer substrate 408. It should be understood that the matching of the CTEs for the interposer 402 will depend on the materials used for the substrate 110. However, the interposer substrate 408 is not limited to such material, as in other embodiments, the interposer substrate 408 is formed from an oxide, oxynitride, nitride, or another insulating material. The interposer substrate 408 and vias 410 are formed, in some embodiments as described above with respect to the substrate layer 108 and vias 120. In some embodiments, the interposer substrate 408 is formed first, with the top RDL 404 and bottom RDL 406 subsequently formed, respectively, on the top surface and bottom surface of the interposer substrate 408. In other embodiments, the interposer 402 is formed by forming the top RDL 404 or bottom RDL 406 on a carrier or the like, with the interposer substrate 408 formed on the first formed RDL 404 / 406 and the remaining RDL 404 / 406 formed over the interposer substrate 408.” Wu, [4:58-5:27].</p>
---	---

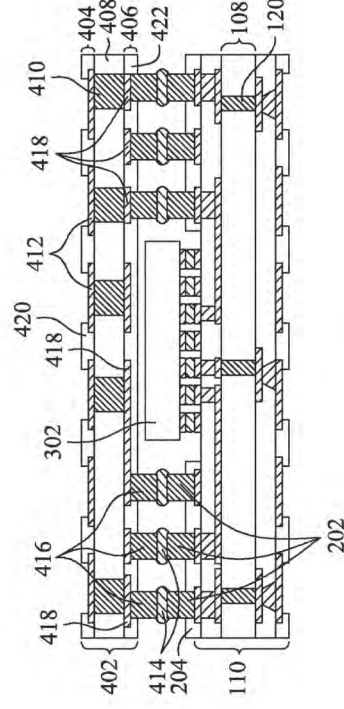


Fig. 4

Wu, FIG. 4

“In some embodiments, the pillars 416 on the interposer 402 are formed to have about the same size and pitch as the pillars 202 on the substrate 110, and with a complementary arrangement so that pillars 416 align with pillars 202 when the interposer 402 is mounted on the substrate 110. The interposer 402 is mounted to the substrate 110 by aligning the pillars 416 over the pillars 202 and bonding the aligned pairs of pillars 202 and 416 to each other.

In some embodiments, a connecting member 414, such as a solder cap, tin layer, or other conductive material is used to joining the aligned ends of the pillars 202 and 416. The connecting member is, for example, formed on one set of pillars 202 or 416 prior to the pillars 202 and 416 being connected. The pillars 202 and 416 are then brought together, and the connecting member 414 is subjected to heat and/or pressure to reflow the material of the connecting member 414 or otherwise bond the aligned pairs of pillars 202 and 416.” Wu, [5:60-6:9].

“FIG. 7 is a cross-sectional view illustrating mounting a package 702 on the interposer 402 according to some embodiments. Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702.” Wu, [6:36-6:43].

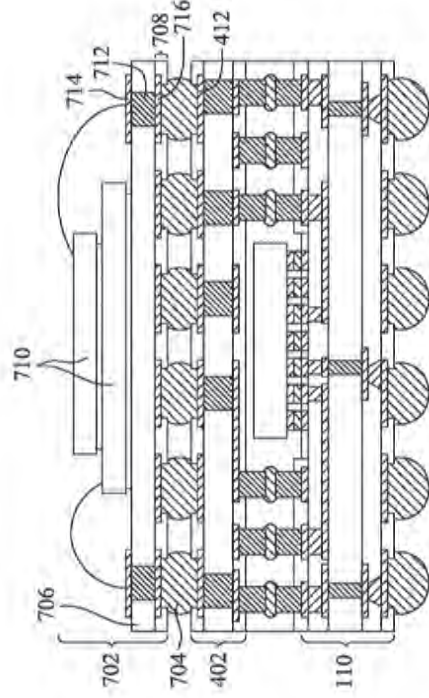


Fig. 7

Wu, FIG. 7

“FIG. 9 is a cross-sectional view illustrating mounting of the interposer 402 on the substrate 110 after formation of the MUF 802 according to some embodiments. In such embodiments, pillars 416 extend into the openings 804, with the connecting members 414 disposed in the

openings 804. The sidewalls of the openings 804 are, in some embodiments, spaced apart from the sidewalls of the pillars 202 and 416.” Wu, [7:17-7:23].

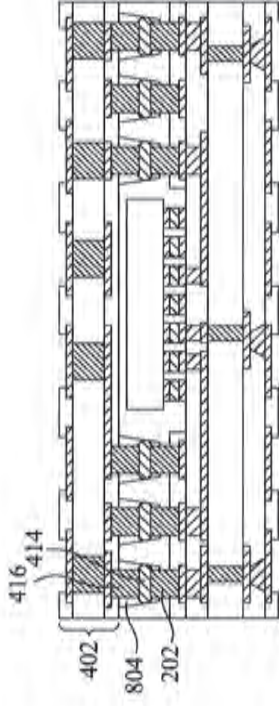


Fig. 9

Wu, FIG. 9

“FIG. 12A is a cross-sectional enlarged view illustrating an alternative pillar 202 arrangement according to some embodiments. The pillars 202 are formed on the substrate 110 and extend above the top surface of the die 302. The connecting members 414 bond the pillars 202 to the lands 418 on the bottom surface of the interposer 402.” Wu, [8:26-8:32].

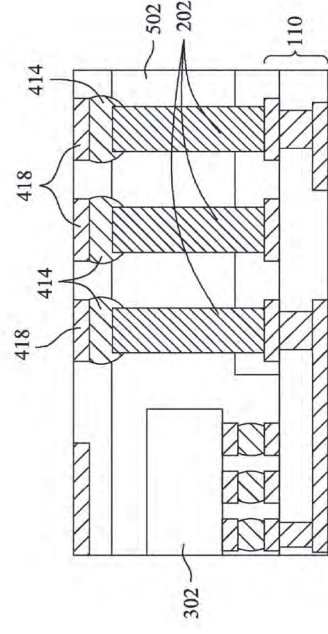
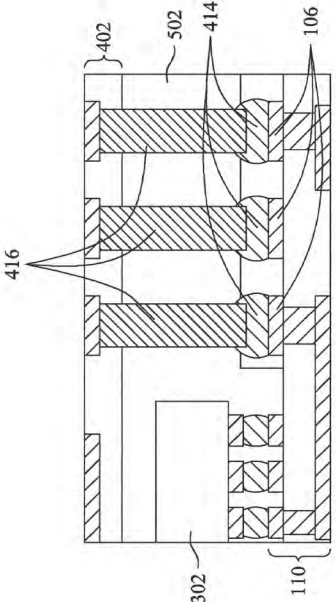


Fig. 12A

Wu, FIG. 12A

“FIG. 12B is a cross-sectional enlarged view illustrating an alternative pillar 416 arrangement according to some embodiments. The pillars 416 are formed on the interposer 402 and extend below the top surface of the die 302. The connecting members 414 directly bond the pillars 416 to the lands 106 on the top surface of the substrate 110.” Wu, [8:33-8:38].

	 <p>Fig. 12B</p> <p>Wu, FIG. 12B</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the bottom end of a corresponding metal	Wu discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

<p>pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 4 is a cross-sectional view illustrating mounting an interposer 402 on the substrate 110 according to some embodiments. In an interposer first process, an interposer 402 is initially provided and mounted over the substrate 110 by attaching pillars 416 on the interposer 402 to the pillars 202 on the substrate 110. The interposer 402 has an interposer substrate 408 with a top RDL 404 and bottom RDL 406 disposed on the top and bottom surfaces of the interposer substrate 408. Vias 410 in the interposer substrate 408 connect the bottom RDL 406 to the top RDL 404. The interposer substrate 408 is formed, in some embodiments, from an organic material such as an epoxy impregnated glass-fiber laminate, polymer impregnated glass-fiber laminate, preimpregnated composite fiber, Ajinomoto build-up film (ABF), molding compound, epoxy, PBO, polyimide or another organic material. It has been discovered that an interposer with an organic interposer substrate 408 provides a structure with a coefficient of thermal expansion (CTE) that more closely matches the CTE of a substrate 110 than an inorganic interposer substrate 408. It should be understood that the matching of the CTEs for the interposer 402 will depend on the materials used for the substrate 110. However, the interposer substrate 408 is not limited to such material, as in other embodiments, the interposer substrate 408 is formed from an oxide, oxynitride, nitride, or another insulating material. The interposer substrate 408 and vias 410 are formed, in some embodiments as described above with respect to the substrate layer 108 and vias 120. In some embodiments, the interposer substrate 408 is formed first, with the top RDL 404 and bottom RDL 406 subsequently formed, respectively, on the top surface and bottom surface of the interposer substrate 408. In other embodiments, the interposer 402 is formed by forming the</p>
--	---

	<p>top RDL 404 or bottom RDL 406 on a carrier or the like, with the interposer substrate 408 formed on the first formed RDL 404 / 406 and the remaining RDL 404 / 406 formed over the interposer substrate 408. The RDLs 404 and 406 are formed as described above with respect to RDLs 102 and 104. While the top RDL 404 and bottom RDL 406 of the interposer 402 are illustrated as each having a single layer of conductive features, the RDLs 404 and 406 are not limited to such structures, as the RDLs 404 and 406, in some embodiments, have multiple conductive features and dielectric layers. The conductive features in the bottom RDL 406 comprise lands 418 that are exposed at the bottom side of the interposer 402 by openings in an overlying protection layer 422. The protection layer 420 on the top RDL 404 has openings exposing lands 412 for subsequent mounting of an external device such as a die, package, board, device or the like. It has been discovered that the interposer 402 having lands 412 on the top surface that are disposed over the die 302 permits connectors for subsequently formed devices to have a pitch that is different than the pitch of the pillars 416. In particular, a larger pitch for the lands 412 permits greater spacing of the connectors on the lands 412, preventing solder bridging between adjacent connectors, and permitting larger connectors. Additionally, the lands 412 being disposed over the die 302 allows for a greater number of lands 412 and associated connectors than the number of pillars 416. In some embodiments, the lands 412 have exposed regions with a diameter between about 200 μm and about 400 μm and a pitch between about 350 μm and about 650 μm. Pillars 416 are disposed on the lands 418 and extend through the openings in the protection layer 422. In some embodiments, the pillars 416 are formed as described above with respect to the pillars 202, with the pillars 416 formed over the protection layer 422 instead of over the solder resist 204. In some embodiments, the pillars 416 on the interposer 402 are formed to have about the same size and pitch as the pillars 202 on the substrate 110, and with a complementary arrangement so that pillars 416 align with pillars 202 when the interposer 402 is mounted on the substrate 110. The interposer 402 is mounted to the substrate 110 by aligning the pillars 416 over the pillars 202 and bonding the aligned pairs of pillars 202 and 416 to each other. In some embodiments, a</p>
--	--

connecting member 414, such as a solder cap, tin layer, or other conductive material is used to joining the aligned ends of the pillars 202 and 416. The connecting member is, for example, formed on one set of pillars 202 or 416 prior to the pillars 202 and 416 being connected. The pillars 202 and 416 are then brought together, and the connecting member 414 is subjected to heat and/or pressure to reflow the material of the connecting member 414 or otherwise bond the aligned pairs of pillars 202 and 416.” Wu, [4:58-6:9].

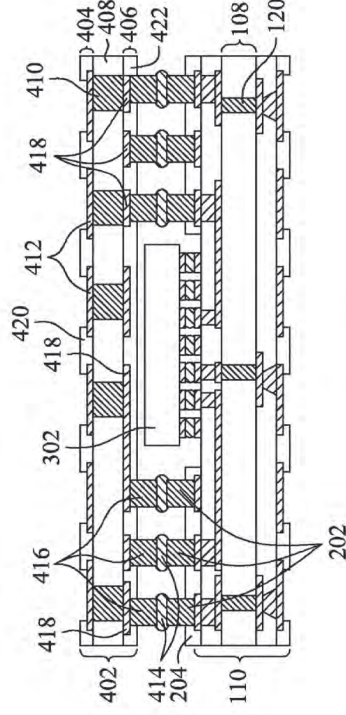


Fig. 4

Wu, FIG. 4

“FIG. 7 is a cross-sectional view illustrating mounting a package 702 on the interposer 402 according to some embodiments. Package connectors 704 such as, for example, solder balls, pillars, studs, conductive bumps, or the like bond the package 702 to the interposer 402. The connectors 704 electrically connect the lands 412 on the top surface of the interposer 402 to the lands 716 on the bottom surface of the package 702. In some embodiments, the package 702 has one or more dies 710 electrically connected to conductive features 714 that are in

	<p>turn electrically connected to the lands 716 by way of vias 712 disposed in a package substrate 706. While the package 702 is illustrated herein as having a substrate 706 with dies 710 disposed thereon, the structure is not limited to having such a package 702 with such an arrangement. In other embodiments, the package 702 is a die or chip mounted directly on the connectors 704, multiple dies or packages on the connectors 704 or another arrangement. While FIGS. 1 through 7 describe a process for forming the described structure using an interposer first process, in other embodiments, an interposer last process is employed to form the structure. In such embodiments, the MUF 502 is formed prior to mounting the interposer 402 to the substrate 110, as shown in FIGS. 8 through 10. FIG. 8 is a cross-sectional view illustrating formation of an MUF 802 prior to mounting the interposer 402 according to some embodiments. The MUF 802 is formed after the die 302 is mounted to the substrate 110 as shown in FIGS. 1 and 3, and in some embodiments, the MUF 802 is also formed after formation of the pillars 202 as shown in FIG. 2. In such embodiments, the MUF 802 is formed with openings 804 exposing the pillars 202.” Wu, [6:36-7:1].</p> <p>“FIG. 12A is a cross-sectional enlarged view illustrating an alternative pillar 202 arrangement according to some embodiments. The pillars 202 are formed on the substrate 110 and extend above the top surface of the die 302. The connecting members 414 bond the pillars 202 to the lands 418 on the bottom surface of the interposer 402. FIG. 12B is a cross-sectional enlarged view illustrating an alternative pillar 416 arrangement according to some embodiments. The pillars 416 are formed on the interposer 402 and extend below the top surface of the die 302. The connecting members 414 directly bond the pillars 416 to the lands 106 on the top surface of the substrate 110.” Wu, [8:26-8:38].</p>
--	--

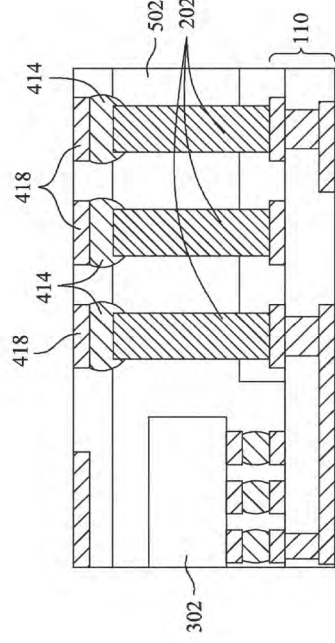


Fig. 12A

Wu, FIG. 12A

“According to an embodiment, a device comprises a substrate having a die mounted on the first side of the substrate and a moldable underfill (MUF) disposed on the first side of the substrate and around the die. An interposer is mounted on the first side of the substrate, with the interposer having lands disposed on a first side of the interposer. The interposer mounted to the substrate by connectors bonded to a second side of the interposer, the connectors providing electrical connectivity between the interposer and the substrate. A package is mounted on the first side of the interposer and is electrically connected to the lands. At least one of the lands is aligned directly over the die and wherein a pitch of the connectors is different than a pitch of the lands.” Wu, [8:55-8:67].

“According to another embodiment, a device comprises a substrate having a die disposed on a first side of the substrate and first pillars disposed on the first side of the substrate. The first pillars have a first pitch. A moldable underfill (MUF) is disposed on the first side of the

Appendix A-34 - Invalidity of U.S. Patent No. 9859202 in view of Wu - U.S. Patent No. 10319607

	<p>substrate, with the MUF surrounding the die and each of the first pillars. An interposer is mounted over the first side of the substrate and has lands disposed on a first side of the interposer. The lands have a second pitch greater than the first pitch, and at least one of the lands is aligned directly over the die. Second pillars are disposed on a second side of the interposer, and the second pillars are bonded to the first pillars and provide electrical connectivity between the interposer and the substrate.” Wu, [9:1-9:13].</p> <p>“A method of forming a device according to an embodiment comprises mounting a die on a first side of a substrate and forming first pillars on the first side of the substrate. A moldable underfill (MUF) is applied on the first side of the substrate and surrounds the die and each of the first pillars. An interposer is mounted on the first side of the substrate by bonding second pillars on a second side of the interposer to the first pillars. The interposer has lands disposed on a first side of the interposer and at least one of the lands is aligned directly over the die. After the mounting the interposer, the first pillars and second pillars provide electrical connectivity between the interposer and the substrate. A package is mounted on the lands and the die is disposed between the first pillars.” Wu, [9:15-9:28].</p> <p>To the extent Plaintiff contends that Wu fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

U.S. Patent Publication No. 20120119370 (“Yoo”) is titled Semiconductor Package and Semiconductor System Including the Same and lists Jae-Wook Yoo as inventor. Yoo anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ‘202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Yoo is a U.S. patent publication that was filed September 16, 2011 and published May 17, 2012. Yoo claims priority to KR 10-2010-0112273 filed on November 11, 2010. Yoo is therefore prior art to the ‘202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Yoo, or otherwise rendered obvious by disclosures and teachings of Yoo, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Yoo does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Yoo with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Yoo, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Yoo “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

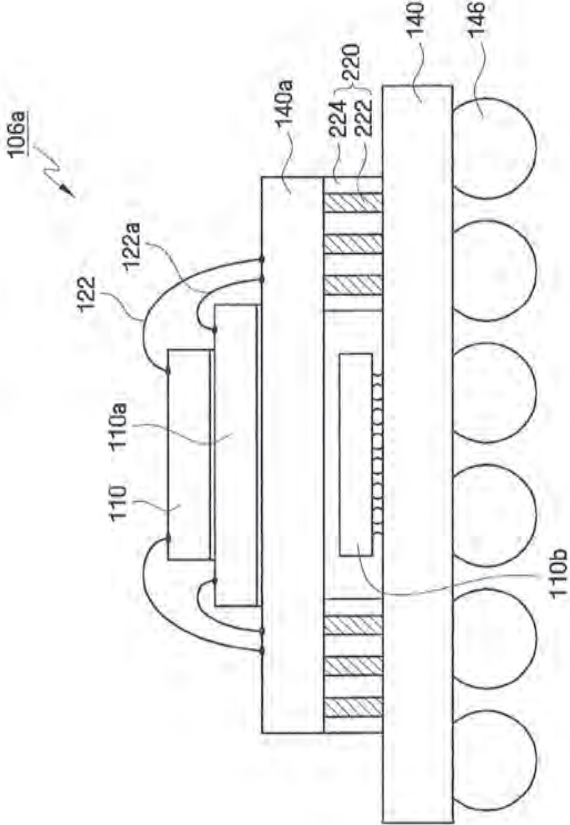
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Yoo or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Yoo set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Yoo discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“External terminals 146 such as, for example, solder balls are bonded to a portion of the other surface of the package substrate 140. The semiconductor device 110 is electrically connected to the package substrate through bumps 117.” Yoo, [0065].</p> <p>“As a set on which a semiconductor package is mounted decreases in thickness, a semiconductor package needs to also have a reduced thickness. Decreasing the thickness of a semiconductor substrate is a commonly used method to reduce the thickness of a</p>

	<p>semiconductor package. However, this method may cause warping at a middle portion of the package substrate 140. Thus, since the interconnect structure 210 suffers less deformation than the solder balls, warping of the package substrate 140 can be prevented by disposing the interconnect structure 210 on the middle portion of the package substrate 140.” Yoo, [0067-0068].</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	---

Fig. 12



Yoo, FIG. 12

“Referring to FIG. 13, in the semiconductor package 106 according to the present embodiment, an interconnect structure 50 is disposed between a first semiconductor package 144 and an interconnect structure 220. A space is created between the package substrates 140

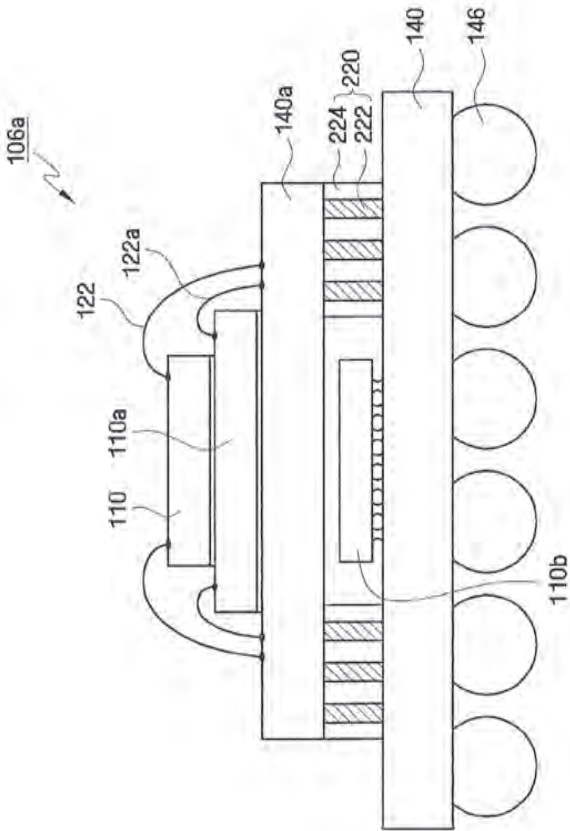
	<p>and 140 a, by the interconnect structures 50 and 220, and a second semiconductor package 110 b is disposed within the space.” Yoo, [0074].</p> <p>“FIG. 14 is a cross-sectional view of a semiconductor package 107 according to another embodiment of the present inventive concept. Referring to FIG. 14, the semiconductor package according to the present embodiment includes the semiconductor package 101 described with reference to FIG. 7 and a semiconductor package 1101 having a mirror image of the semiconductor package 101 with respect to a package substrate 140. For example, according to an embodiment, the semiconductor package 101 is disposed on a top surface of the package substrate 140 and the semiconductor package 1101 is disposed on a bottom surface thereof.” Yoo, [0075].</p> <p>“The semiconductor package 101 has the same construction as that described with reference to FIG. 7. In the semiconductor package 1101, an interconnect structure 440, acting as an interposer, is disposed between a semiconductor device 1110 and the package substrate 140. The interconnect structure 440 includes anodized insulation regions 414 and interconnects 412 defined by the anodized insulation regions 414. The interconnect structure 40 acting as an interposer is connected to the semiconductor device 110 via the bumps 112, but is not limited thereto.” Yoo, [0076].</p> <p>“The memory device 1730 may include a volatile memory such as dynamic random access memory (DRAM) and a nonvolatile memory such as a flash memory. For example, an information processing system such as a mobile device or desk top computer may be equipped with a flash memory. The flash memory may be used to construct a semiconductor disk device (SSD). In an embodiment, the electronic system 1700 stably stores a large amount of data in the flash memory.” Yoo, [0083].</p>
--	--

<p>[1.A] a bottom package substrate;</p>	<p>Yoo discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“External terminals 146 such as, for example, solder balls are bonded to a portion of the other surface of the package substrate 140. The semiconductor device 110 is electrically connected to the package substrate through bumps 117.” Yoo, [0065].</p> <p>“As a set on which a semiconductor package is mounted decreases in thickness, a semiconductor package needs to also have a reduced thickness. Decreasing the thickness of a semiconductor substrate is a commonly used method to reduce the thickness of a semiconductor package. However, this method may cause warping at a middle portion of the package substrate 140. Thus, since the interconnect structure 210 suffers less deformation than the solder balls, warping of the package substrate 140 can be prevented by disposing the interconnect structure 210 on the middle portion of the package substrate 140.” Yoo, [0067-0068].</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are</p>
--	---

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



Yoo, FIG. 12

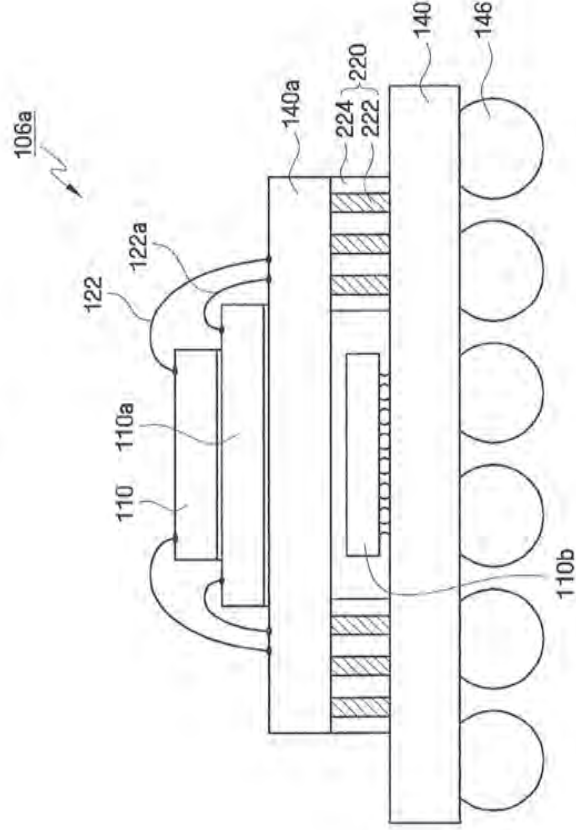
“Referring to FIG. 13, in the semiconductor package 106 according to the present embodiment, an interconnect structure 50 is disposed between a first semiconductor package 144 and an interconnect structure 220. A space is created between the package substrates 140

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>and 140 a, by the interconnect structures 50 and 220, and a second semiconductor package 110 b is disposed within the space.” Yoo, [0074].</p> <p>“FIG. 14 is a cross-sectional view of a semiconductor package 107 according to another embodiment of the present inventive concept. Referring to FIG. 14, the semiconductor package according to the present embodiment includes the semiconductor package 101 described with reference to FIG. 7 and a semiconductor package 1101 having a mirror image of the semiconductor package 101 with respect to a package substrate 140. For example, according to an embodiment, the semiconductor package 101 is disposed on a top surface of the package substrate 140 and the semiconductor package 1101 is disposed on a bottom surface thereof.” Yoo, [0075].</p> <p>“The semiconductor package 101 has the same construction as that described with reference to FIG. 7. In the semiconductor package 1101, an interconnect structure 440, acting as an interposer, is disposed between a semiconductor device 1110 and the package substrate 140. The interconnect structure 440 includes anodized insulation regions 414 and interconnects 412 defined by the anodized insulation regions 414. The interconnect structure 40 acting as an interposer is connected to the semiconductor device 110 via the bumps 112, but is not limited thereto.” Yoo, [0076].</p> <p>To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Yoo discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p>

	<p><i>See, e.g.:</i></p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	---

Fig. 12



Yoo, FIG. 12

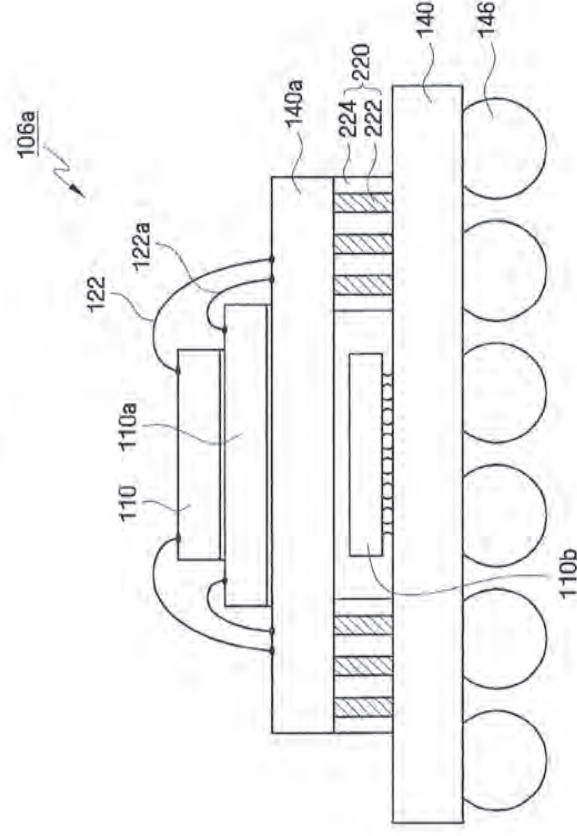
“Referring to FIG. 13, in the semiconductor package 106 according to the present embodiment, an interconnect structure 50 is disposed between a first semiconductor package 144 and an interconnect structure 220. A space is created between the package substrates 140

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>and 140 a, by the interconnect structures 50 and 220, and a second semiconductor package 110 b is disposed within the space.” Yoo, [0074].</p> <p>To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Yoo discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144</p>

exchanges signals with the outside through the interconnect structure 220 and the package substrate 140." Yoo, [0069-0072].

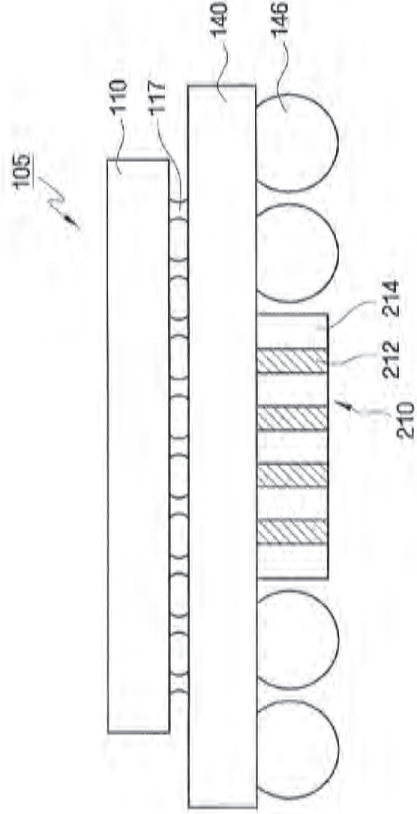
Fig. 12



Yoo, FIG. 12

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

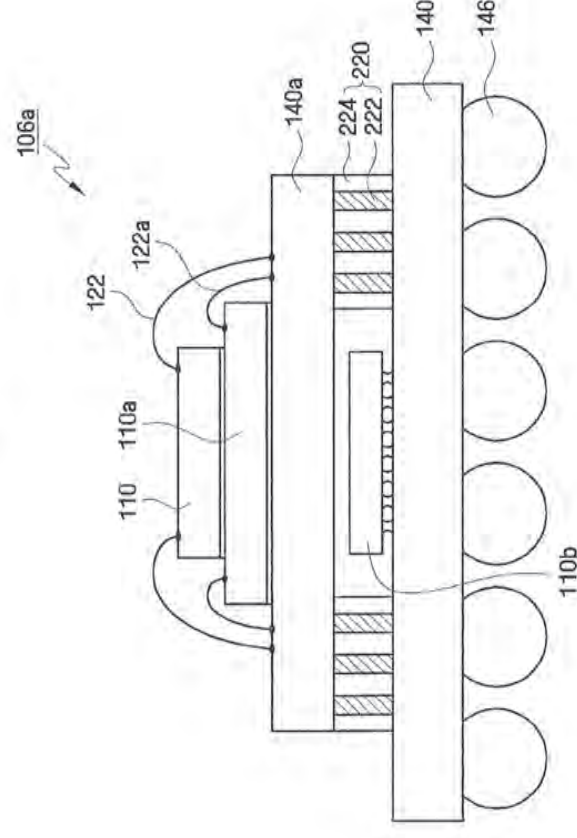
	<p>“Referring to FIG. 13, in the semiconductor package 106 according to the present embodiment, an interconnect structure 50 is disposed between a first semiconductor package 144 and an interconnect structure 220. A space is created between the package substrates 140 and 140 a, by the interconnect structures 50 and 220, and a second semiconductor package 110 b is disposed within the space.” Yoo, [0074].</p> <p>To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Yoo discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 11 is a cross-sectional view of a semiconductor package 105 according to another embodiment of the present inventive concept. Referring to FIG. 11, in the semiconductor package 105 according to the present embodiment, a semiconductor device 110 is mounted on one surface of the package substrate 140, while an interconnect structure 210 is disposed on another surface of the package substrate 140. External terminals 146 such as, for example, solder balls are bonded to a portion of the other surface of the package substrate 140. The semiconductor device 110 is electrically connected to the package substrate through bumps 117. The interconnect structure 210 acts as an external terminal of the semiconductor package 105, like solder balls. The interconnect structure 210 includes anodized insulation regions 214 and interconnects 212 defined by the anodized insulation regions 214. As a set on which a semiconductor package is mounted decreases in thickness, a semiconductor package needs to also have a reduced thickness. Decreasing the thickness of a semiconductor substrate is a</p>

	<p>commonly used method to reduce the thickness of a semiconductor package. However, this method may cause warping at a middle portion of the package substrate 140.” Yoo, [0065-0068].</p> <p style="text-align: center;">Fig. 11</p>  <p>Yoo, FIG. 11</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first</p>
--	---

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



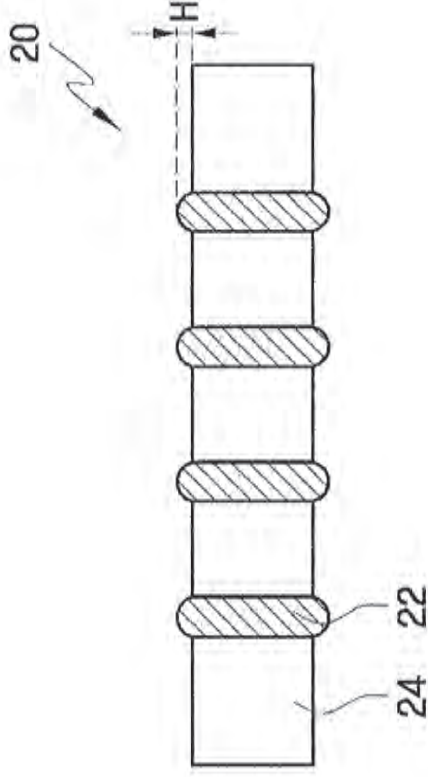
Yoo, FIG. 12

To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Yoo discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2, the interconnects 22 of the interconnect structure 20 are thicker than the anodized insulation regions 24. According to an embodiment, the interconnects 22 protrude upward above and/or downward below the anodized insulation regions 24 by a predetermined height H in order to facilitate coupling of the interconnects 22 with other semiconductor devices, which is described in more detail with reference to FIG. 8.” Yoo, [0043].</p>

Fig. 2



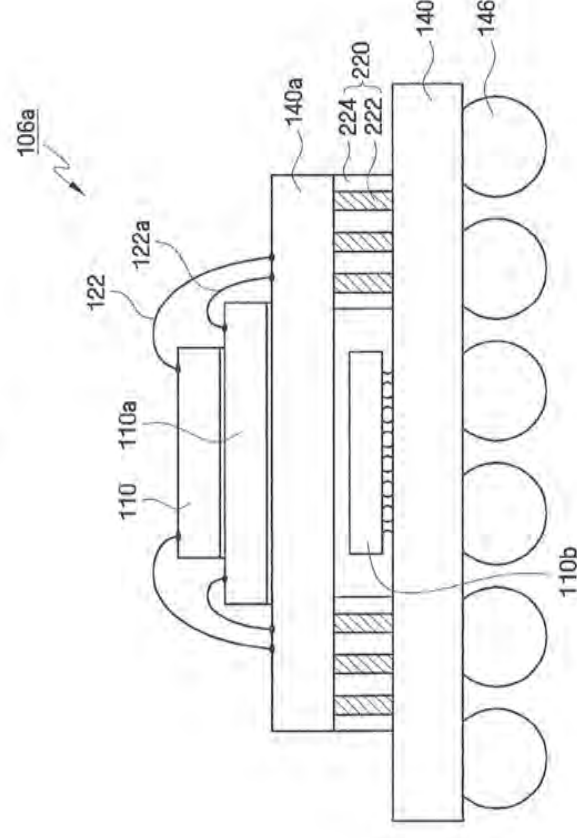
Yoo, FIG. 2

“After forming the anodized insulation regions 24 using the anodizing process, etching is performed to remove a portion of a surface of the anodized insulation regions 24. That is, etching is performed to cause the interconnects 22 to protrude higher than the anodized insulation regions 24.” Yoo, [0044].

“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging

	<p>technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	---

Fig. 12



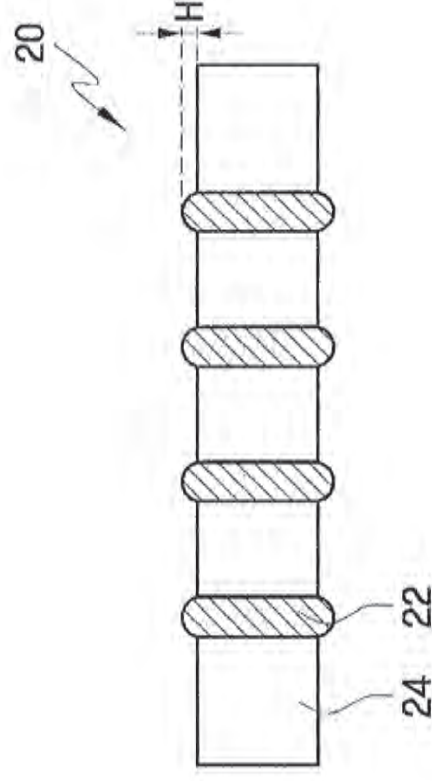
Yoo, FIG. 12

To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;	<p>Yoo discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2, the interconnects 22 of the interconnect structure 20 are thicker than the anodized insulation regions 24. According to an embodiment, the interconnects 22 protrude upward above and/or downward below the anodized insulation regions 24 by a predetermined height H in order to facilitate coupling of the interconnects 22 with other semiconductor devices, which is described in more detail with reference to FIG. 8. After forming the anodized insulation regions 24 using the anodizing process, etching is performed to remove a portion of a surface of the anodized insulation regions 24. That is, etching is performed to cause the interconnects 22 to protrude higher than the anodized insulation regions 24.” Yoo, [0043-0044].</p>

Fig. 2



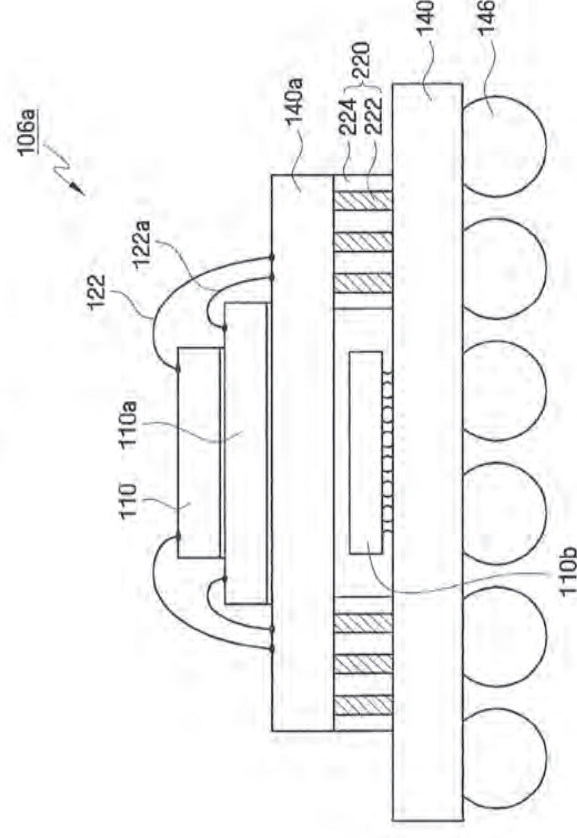
Y00, FIG. 2

“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip-form

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



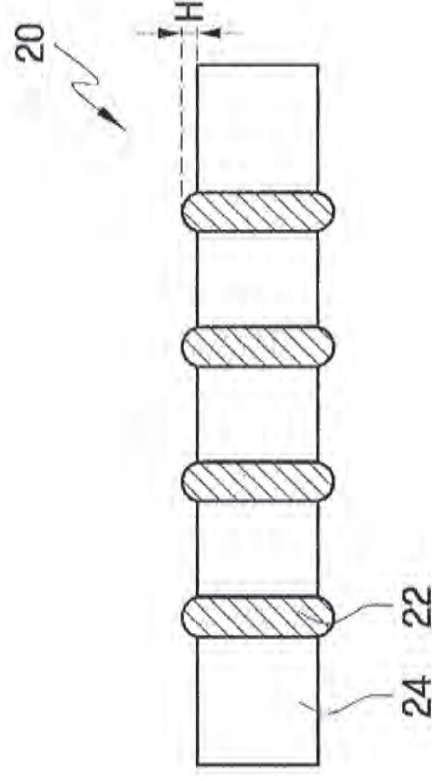
Yoo, FIG. 12

To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,	<p>Yoo discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2, the interconnects 22 of the interconnect structure 20 are thicker than the anodized insulation regions 24. According to an embodiment, the interconnects 22 protrude upward above and/or downward below the anodized insulation regions 24 by a predetermined height H in order to facilitate coupling of the interconnects 22 with other semiconductor devices, which is described in more detail with reference to FIG. 8. After forming the anodized insulation regions 24 using the anodizing process, etching is performed to remove a portion of a surface of the anodized insulation regions 24. That is, etching is performed to cause the interconnects 22 to protrude higher than the anodized insulation regions 24.” Yoo, [0043-0044].</p>

Fig. 2



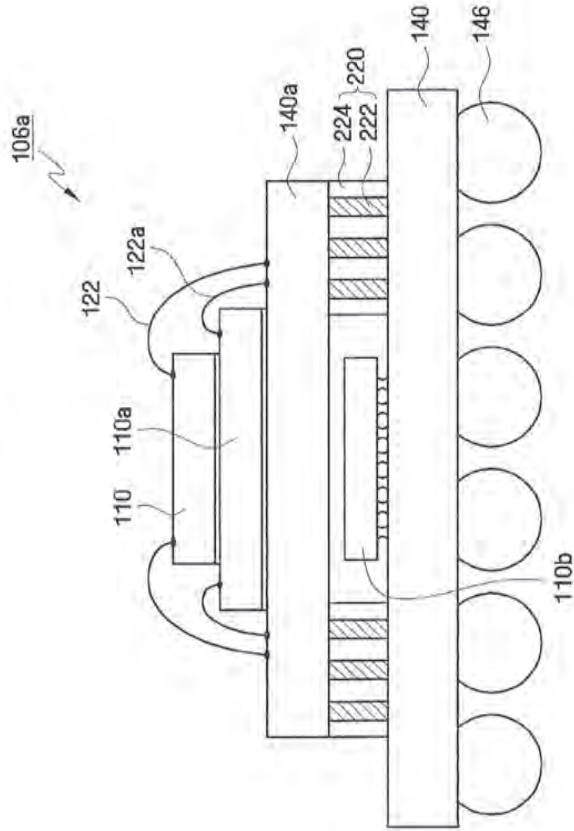
Y00, FIG. 2

“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip-form

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



Yoo, FIG. 12

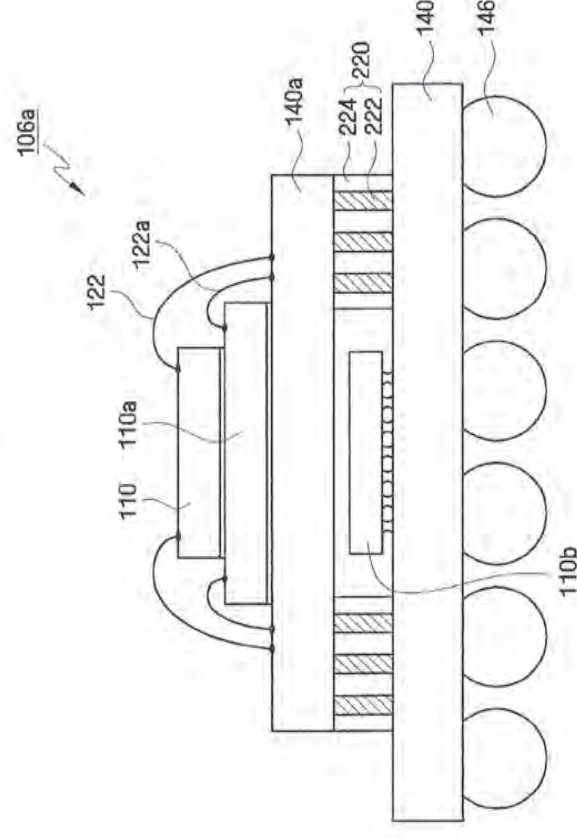
To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,	<p>Yoo discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“For example, the semiconductor device 110 may be connected to the interconnect structure 40 using a solder paste (150 in FIG. 8) instead of the bumps 112. The interconnect structure 40 may also be connected to the package substrate 140 through bumps, a solder paste, or other various materials.” Yoo, [0054].</p> <p>“Although not shown in FIG. 7, the semiconductor package 101 may further include a molding layer for molding the semiconductor device 110 on the package substrate 140 and external terminals such as solder balls attached to a bottom of the package substrate 140. FIG. 8 is a cross-sectional view of a semiconductor package according to another embodiment of the present inventive concept. Referring to FIG. 8, a semiconductor device 110 connects to an interconnect structure 40 through a solder paste 150 and the interconnect structure 40 connects to a package substrate 140 through a solder paste 160.” Yoo, [0055-0056].</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor</p>

	<p>package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



Yoo, FIG. 12

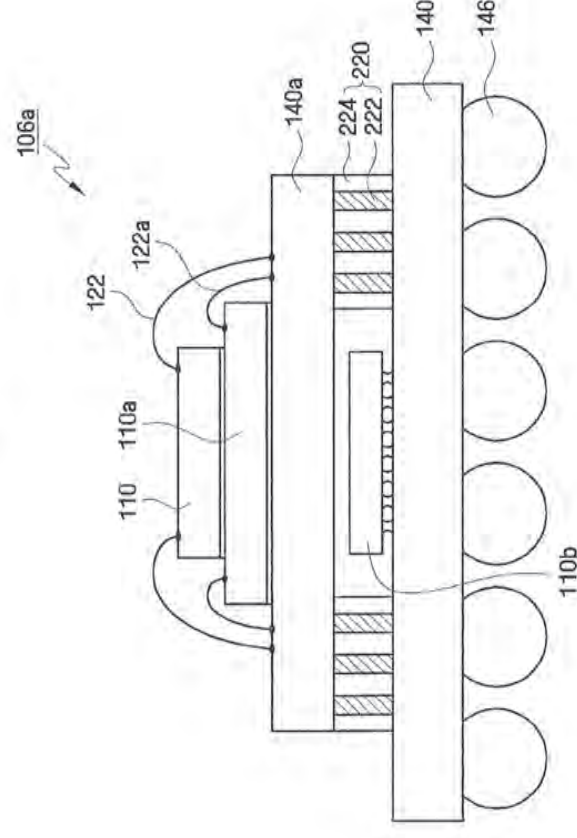
To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and	<p>Yoo discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 8 is a cross-sectional view of a semiconductor package according to another embodiment of the present inventive concept. Referring to FIG. 8, a semiconductor device 110 connects to an interconnect structure 40 through a solder paste 150 and the interconnect structure 40 connects to a package substrate 140 through a solder paste 160. Referring to FIG. 8, a chip pad 114 is mounted on a surface of the chip-form semiconductor device 110, and a protective layer 118 is also formed on the surface of the chip-form semiconductor device 110, and includes an open portion exposing at least a portion of the chip pad 114. An under barrier metal (UBM) 116 is formed on a portion of the protective layer 118 and in the open portion of the protective layer on the exposed portion of the chip pad 114. The solder paste 150 is interposed between the UBM 116 and a first region 42 b of an interconnect 42. A package pad 144 is disposed on a surface of the package substrate 140, and a protective layer 148 is formed on the surface of the package substrate, and includes an open portion exposing at least a portion of the package pad 144. The solder paste 160 is disposed between the exposed portion of the package pad 144 and a second region 42 a of the interconnect 42 in the interconnect structure 40.” Yoo, [0056-0058].</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according</p>

	<p>to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



Yoo, FIG. 12

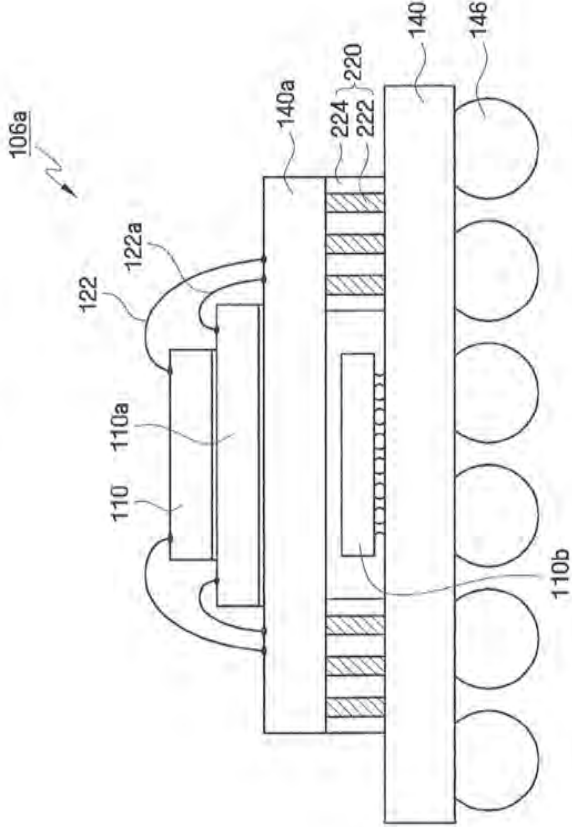
To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and	<p>Yoo discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“For example, the semiconductor device 110 may be connected to the interconnect structure 40 using a solder paste (150 in FIG. 8) instead of the bumps 112. The interconnect structure 40 may also be connected to the package substrate 140 through bumps, a solder paste, or other various materials. Although not shown in FIG. 7, the semiconductor package 101 may further include a molding layer for molding the semiconductor device 110 on the package substrate 140 and external terminals such as solder balls attached to a bottom of the package substrate 140. FIG. 8 is a cross-sectional view of a semiconductor package according to another embodiment of the present inventive concept. Referring to FIG. 8, a semiconductor device 110 connects to an interconnect structure 40 through a solder paste 150 and the interconnect structure 40 connects to a package substrate 140 through a solder paste 160. Referring to FIG. 8, a chip pad 114 is mounted on a surface of the chip-form semiconductor device 110, and a protective layer 118 is also formed on the surface of the chip-form semiconductor device 110, and includes an open portion exposing at least a portion of the chip pad 114. An under barrier metal (UBM) 116 is formed on a portion of the protective layer 118 and in the open portion of the protective layer on the exposed portion of the chip pad 114. The solder paste 150 is interposed between the UBM 116 and a first region 42 b of an interconnect 42. A package pad 144 is disposed on a surface of the package substrate 140,</p>

	<p>and a protective layer 148 is formed on the surface of the package substrate, and includes an open portion exposing at least a portion of the package pad 144. The solder paste 160 is disposed between the exposed portion of the package pad 144 and a second region 42 a of the interconnect 42 in the interconnect structure 40.” Yoo, [0054-0058].</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	---

Fig. 12



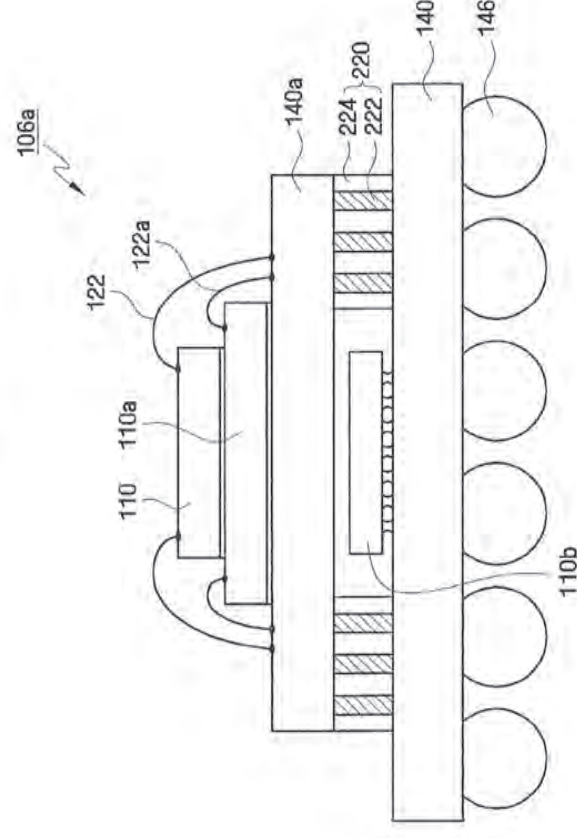
Yoo, FIG. 12

To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein the top package substrate, wherein	<p>Yoo discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>

Fig. 12



Yoo, FIG. 12

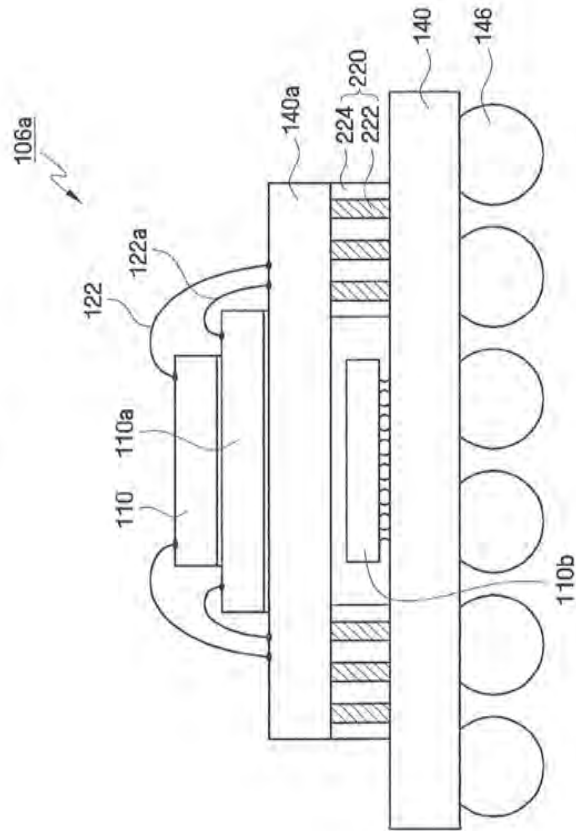
“Referring to FIG. 13, in the semiconductor package 106 according to the present embodiment, an interconnect structure 50 is disposed between a first semiconductor package 144 and an interconnect structure 220. A space is created between the package substrates 140

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>and 140 a, by the interconnect structures 50 and 220, and a second semiconductor package 110 b is disposed within the space.” Yoo, [0074].</p> <p>“The semiconductor package 101 has the same construction as that described with reference to FIG. 7. In the semiconductor package 1101, an interconnect structure 440, acting as an interposer, is disposed between a semiconductor device 1110 and the package substrate 140. The interconnect structure 440 includes anodized insulation regions 414 and interconnects 412 defined by the anodized insulation regions 414. The interconnect structure 40 acting as an interposer is connected to the semiconductor device 110 via the bumps 112, but is not limited thereto.” Yoo, [0076].</p> <p>“The memory device 1730 may include a volatile memory such as dynamic random access memory (DRAM) and a nonvolatile memory such as a flash memory. For example, an information processing system such as a mobile device or desk top computer may be equipped with a flash memory. The flash memory may be used to construct a semiconductor disk device (SSD). In an embodiment, the electronic system 1700 stably stores a large amount of data in the flash memory.” Yoo, [0083].</p> <p>To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Yoo discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



Yoo, FIG. 12

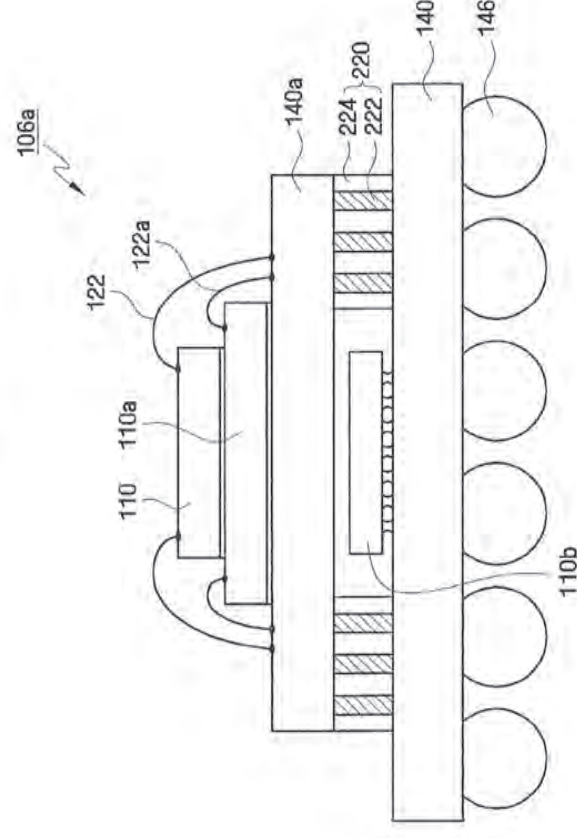
“Referring to FIG. 13, in the semiconductor package 106 according to the present embodiment, an interconnect structure 50 is disposed between a first semiconductor package 144 and an interconnect structure 220. A space is created between the package substrates 140

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>and 140 a, by the interconnect structures 50 and 220, and a second semiconductor package 110 b is disposed within the space.” Yoo, [0074].</p> <p>“The semiconductor package 101 has the same construction as that described with reference to FIG. 7. In the semiconductor package 1101, an interconnect structure 440, acting as an interposer, is disposed between a semiconductor device 1110 and the package substrate 140. The interconnect structure 440 includes anodized insulation regions 414 and interconnects 412 defined by the anodized insulation regions 414. The interconnect structure 40 acting as an interposer is connected to the semiconductor device 110 via the bumps 112, but is not limited thereto.” Yoo, [0076].</p> <p>“The memory device 1730 may include a volatile memory such as dynamic random access memory (DRAM) and a nonvolatile memory such as a flash memory. For example, an information processing system such as a mobile device or desk top computer may be equipped with a flash memory. The flash memory may be used to construct a semiconductor disk device (SSD). In an embodiment, the electronic system 1700 stably stores a large amount of data in the flash memory.” Yoo, [0083].</p> <p>To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Yoo discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>

	<p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



Yoo, FIG. 12

To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

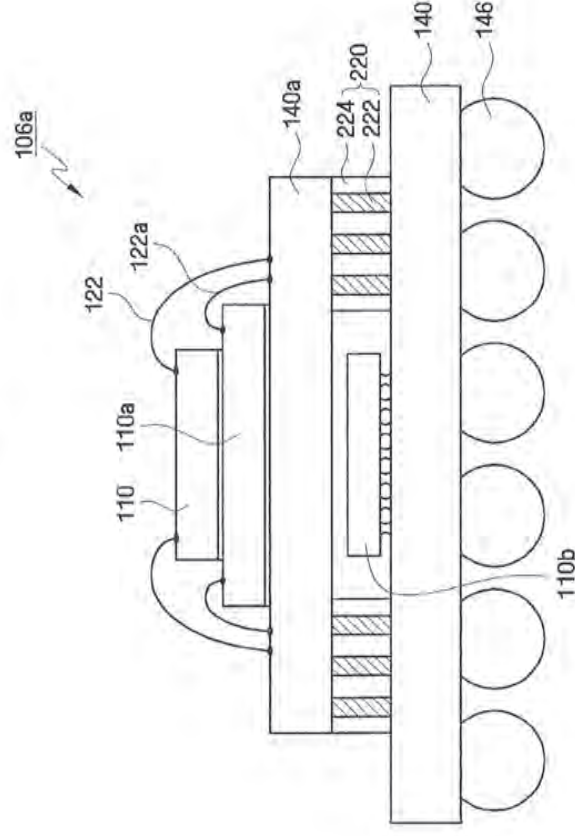
	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Yoo discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144</p>

exchanges signals with the outside through the interconnect structure 220 and the package substrate 140." Yoo, [0069-0072].

Fig. 12



Yoo, FIG. 12

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>“Referring to FIG. 13, in the semiconductor package 106 according to the present embodiment, an interconnect structure 50 is disposed between a first semiconductor package 144 and an interconnect structure 220. A space is created between the package substrates 140 and 140 a, by the interconnect structures 50 and 220, and a second semiconductor package 110 b is disposed within the space.” Yoo, [0074].</p> <p>“The semiconductor package 101 has the same construction as that described with reference to FIG. 7. In the semiconductor package 1101, an interconnect structure 440, acting as an interposer, is disposed between a semiconductor device 1110 and the package substrate 140. The interconnect structure 440 includes anodized insulation regions 414 and interconnects 412 defined by the anodized insulation regions 414. The interconnect structure 40 acting as an interposer is connected to the semiconductor device 110 via the bumps 112, but is not limited thereto.” Yoo, [0076].</p> <p>“The memory device 1730 may include a volatile memory such as dynamic random access memory (DRAM) and a nonvolatile memory such as a flash memory. For example, an information processing system such as a mobile device or desk top computer may be equipped with a flash memory. The flash memory may be used to construct a semiconductor disk device (SSD). In an embodiment, the electronic system 1700 stably stores a large amount of data in the flash memory.” Yoo, [0083].</p> <p>To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

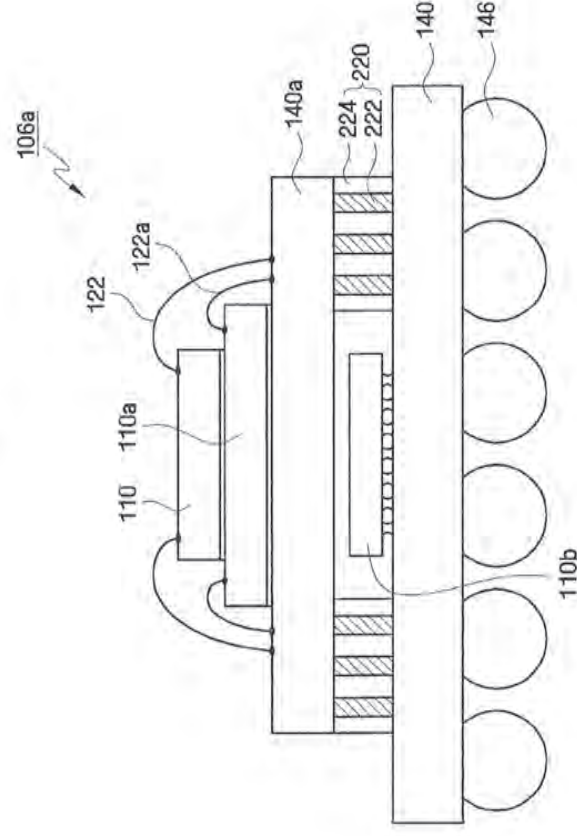
Claim 3, U.S. Patent No. 9859202

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Yoo discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“External terminals 146 such as, for example, solder balls are bonded to a portion of the other surface of the package substrate 140. The semiconductor device 110 is electrically connected to the package substrate through bumps 117.” Yoo, [0065].</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144</p>

exchanges signals with the outside through the interconnect structure 220 and the package substrate 140." Yoo, [0069-0072].

Fig. 12



Yoo, FIG. 12

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>“The memory device 1730 may include a volatile memory such as dynamic random access memory (DRAM) and a nonvolatile memory such as a flash memory. For example, an information processing system such as a mobile device or desk top computer may be equipped with a flash memory. The flash memory may be used to construct a semiconductor disk device (SSD). In an embodiment, the electronic system 1700 stably stores a large amount of data in the flash memory.” Yoo, [0083].</p> <p>To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

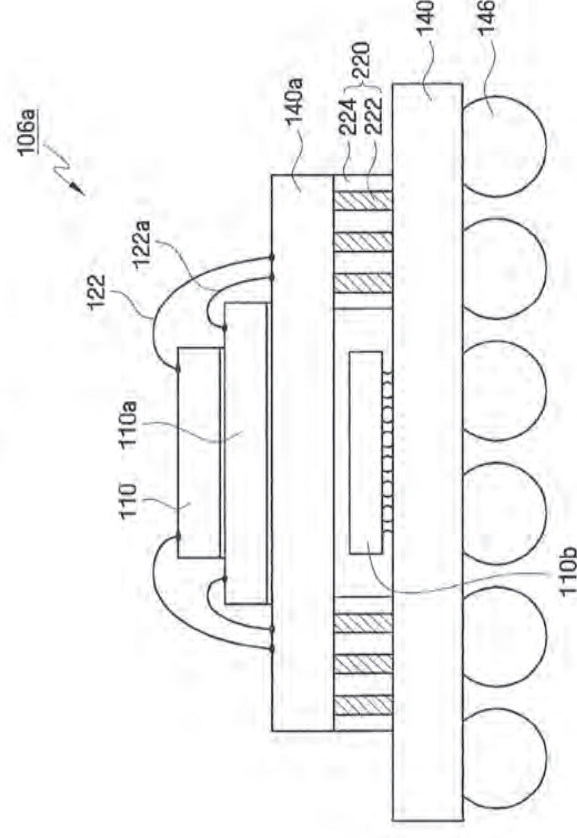
Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>Yoo discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“For example, the semiconductor device 110 may be connected to the interconnect structure 40 using a solder paste (150 in FIG. 8) instead of the bumps 112. The interconnect structure 40 may also be connected to the package substrate 140 through bumps, a solder paste, or</p>

	<p>other various materials. Although not shown in FIG. 7, the semiconductor package 101 may further include a molding layer for molding the semiconductor device 110 on the package substrate 140 and external terminals such as solder balls attached to a bottom of the package substrate 140. FIG. 8 is a cross-sectional view of a semiconductor package according to another embodiment of the present inventive concept. Referring to FIG. 8, a semiconductor device 110 connects to an interconnect structure 40 through a solder paste 150 and the interconnect structure 40 connects to a package substrate 140 through a solder paste 160. Referring to FIG. 8, a chip pad 114 is mounted on a surface of the chip-form semiconductor device 110, and a protective layer 118 is also formed on the surface of the chip-form semiconductor device 110, and includes an open portion exposing at least a portion of the chip pad 114. An under barrier metal (UBM) 116 is formed on a portion of the protective layer 118 and in the open portion of the protective layer on the exposed portion of the chip pad 114. The solder paste 150 is interposed between the UBM 116 and a first region 42 b of an interconnect 42. A package pad 144 is disposed on a surface of the package substrate 140, and a protective layer 148 is formed on the surface of the package substrate, and includes an open portion exposing at least a portion of the package pad 144. The solder paste 160 is disposed between the exposed portion of the package pad 144 and a second region 42 a of the interconnect 42 in the interconnect structure 40.” Yoo, [0054-0058].</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form</p>
--	---

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



Yoo, FIG. 12

To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

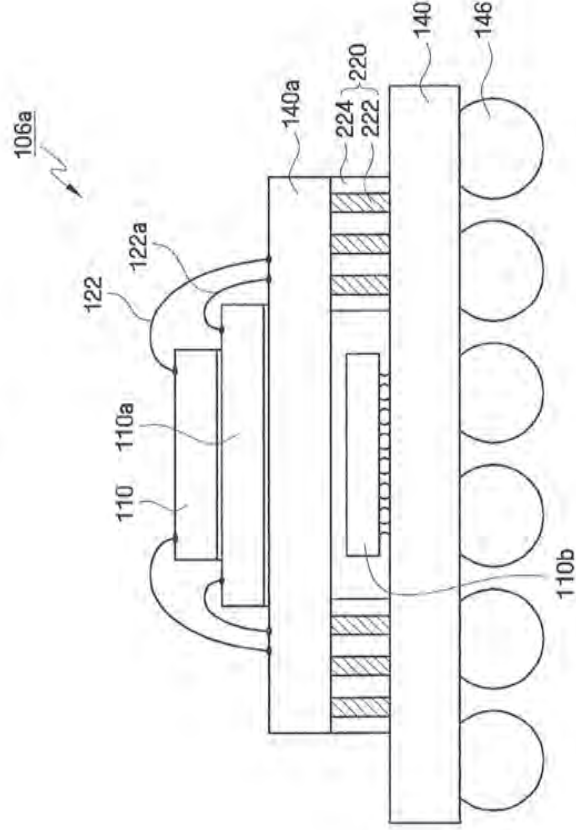
Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“For example, the semiconductor device 110 may be connected to the interconnect structure 40 using a solder paste (150 in FIG. 8) instead of the bumps 112. The interconnect structure 40 may also be connected to the package substrate 140 through bumps, a solder paste, or other various materials. Although not shown in FIG. 7, the semiconductor package 101 may further include a molding layer for molding the semiconductor device 110 on the package substrate 140 and external terminals such as solder balls attached to a bottom of the package substrate 140. FIG. 8 is a cross-sectional view of a semiconductor package according to another embodiment of the present inventive concept. Referring to FIG. 8, a semiconductor device 110 connects to an interconnect structure 40 through a solder paste 150 and the interconnect structure 40 connects to a package substrate 140 through a solder paste 160.</p>	<p>Yoo discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“For example, the semiconductor device 110 may be connected to the interconnect structure 40 using a solder paste (150 in FIG. 8) instead of the bumps 112. The interconnect structure 40 may also be connected to the package substrate 140 through bumps, a solder paste, or other various materials. Although not shown in FIG. 7, the semiconductor package 101 may further include a molding layer for molding the semiconductor device 110 on the package substrate 140 and external terminals such as solder balls attached to a bottom of the package substrate 140. FIG. 8 is a cross-sectional view of a semiconductor package according to another embodiment of the present inventive concept. Referring to FIG. 8, a semiconductor device 110 connects to an interconnect structure 40 through a solder paste 150 and the interconnect structure 40 connects to a package substrate 140 through a solder paste 160.</p>

	<p>Referring to FIG. 8, a chip pad 114 is mounted on a surface of the chip-form semiconductor device 110, and a protective layer 118 is also formed on the surface of the chip-form semiconductor device 110, and includes an open portion exposing at least a portion of the chip pad 114. An under barrier metal (UBM) 116 is formed on a portion of the protective layer 118 and in the open portion of the protective layer on the exposed portion of the chip pad 114. The solder paste 150 is interposed between the UBM 116 and a first region 42 b of an interconnect 42. A package pad 144 is disposed on a surface of the package substrate 140, and a protective layer 148 is formed on the surface of the package substrate, and includes an open portion exposing at least a portion of the package pad 144. The solder paste 160 is disposed between the exposed portion of the package pad 144 and a second region 42 a of the interconnect 42 in the interconnect structure 40.” Yoo, [0054-0058].</p> <p>“As a set on which a semiconductor package is mounted decreases in thickness, a semiconductor package needs to also have a reduced thickness. Decreasing the thickness of a semiconductor substrate is a commonly used method to reduce the thickness of a semiconductor package. However, this method may cause warping at a middle portion of the package substrate 140. Thus, since the interconnect structure 210 suffers less deformation than the solder balls, warping of the package substrate 140 can be prevented by disposing the interconnect structure 210 on the middle portion of the package substrate 140.” Yoo, [0067-0068].</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first</p>
--	---

	<p>semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	--

Fig. 12



Yoo, FIG. 12

“The semiconductor package 101 has the same construction as that described with reference to FIG. 7. In the semiconductor package 1101, an interconnect structure 440, acting as an interposer, is disposed between a semiconductor device 1110 and the package substrate 140.

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	<p>The interconnect structure 440 includes anodized insulation regions 414 and interconnects 412 defined by the anodized insulation regions 414. The interconnect structure 40 acting as an interposer is connected to the semiconductor device 110 via the bumps 112, but is not limited thereto.” Yoo, [0076].</p> <p>To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

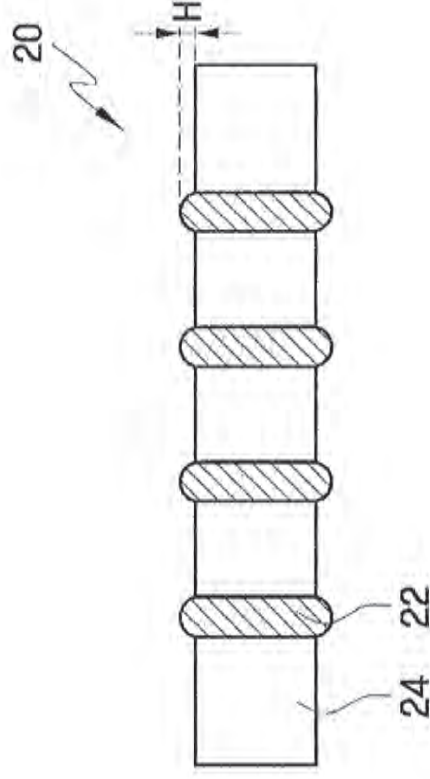
Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the plurality of metal pillars among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Yoo discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 2 is a cross-sectional view showing another example of an interconnect structure 20 for use in a semiconductor package according to embodiments of the present inventive</p>

package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

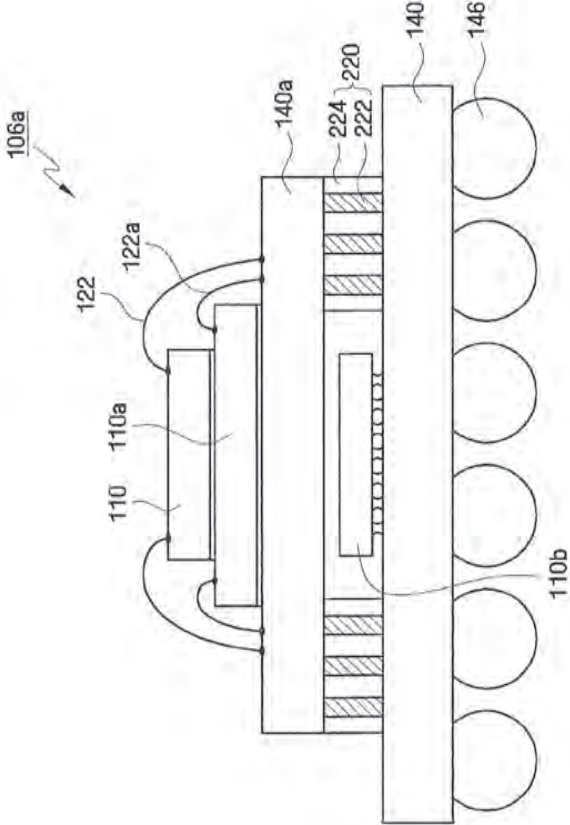
concept. Referring to FIG. 2, the interconnects 22 of the interconnect structure 20 are thicker than the anodized insulation regions 24. According to an embodiment, the interconnects 22 protrude upward above and/or downward below the anodized insulation regions 24 by a predetermined height H in order to facilitate coupling of the interconnects 22 with other semiconductor devices, which is described in more detail with reference to FIG. 8. After forming the anodized insulation regions 24 using the anodizing process, etching is performed to remove a portion of a surface of the anodized insulation regions 24. That is, etching is performed to cause the interconnects 22 to protrude higher than the anodized insulation regions 24.” Yoo, [0042-0044].

Fig. 2



	<p>Yoo, FIG. 2</p> <p>“FIG. 12 is a cross-sectional view of a semiconductor package 106 a according to another embodiment of the present inventive concept. The semiconductor package 106 a according to the present embodiment is formed using a Package-On-Package (POP) packaging technique, but is not limited thereto. In the semiconductor package 106 a according to the present embodiment, an interconnect structure 220 is disposed between a first semiconductor package 144 and a package substrate 140 so as to create a space between the first semiconductor package 144 and the package substrate 140 in which a second semiconductor package 110 b is mounted. The first semiconductor package 144 includes chip- form semiconductor devices 110 and 110 a sequentially stacked on a package substrate 140 a. According to an embodiment, the chip- form semiconductor devices 110 and 110 a are connected to a package substrate 140 a by wire bonding 122, 122 a, but are not limited thereto. The interconnect structure 220 may serve as an interconnect in a POP semiconductor package as well. According to an embodiment, the first semiconductor package 144 exchanges signals with the outside through the interconnect structure 220 and the package substrate 140.” Yoo, [0069-0072].</p>
--	---

Fig. 12



Yoo, FIG. 12

To the extent Plaintiff contends that Yoo fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general

Appendix A-35 - Invalidity of U.S. Patent No. 9859202 in view of Yoo - U.S. Patent Publication No. 20120119370

	knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

U.S. Patent No. 10026671 (“Yu '671”) is titled Substrate Design for Semiconductor Packages and Method of Forming Same and lists Chen-Hua Yu, Mirng-Ji Lii, Chien-Hsun Lee, Tsung-Ding Wang, Jung Wei Cheng, Ming-Che Liu, Hao-Cheng Hou, and Hung-Jen Lin as inventors. Yu '671 is assigned to Taiwan Semiconductor Manufacturing Company, Ltd. Yu '671 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the '202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Yu '671 is a U.S. patent that was filed August 29, 2014 and published August 20, 2015. Yu '671 claims priority to US 14/181,305 filed on February 14, 2014. Yu '671 is therefore prior art to the '202 patent under at least 35 U.S.C. § 102(a)(2).

The chart below provides representative examples of where each element of each Asserted Claim is found within Yu '671, or otherwise rendered obvious by disclosures and teachings of Yu '671, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Yu '671 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Yu '671 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the '202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Yu '671, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

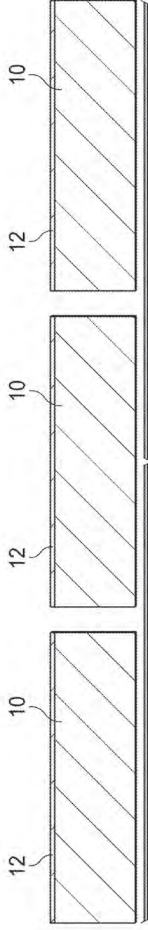
To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

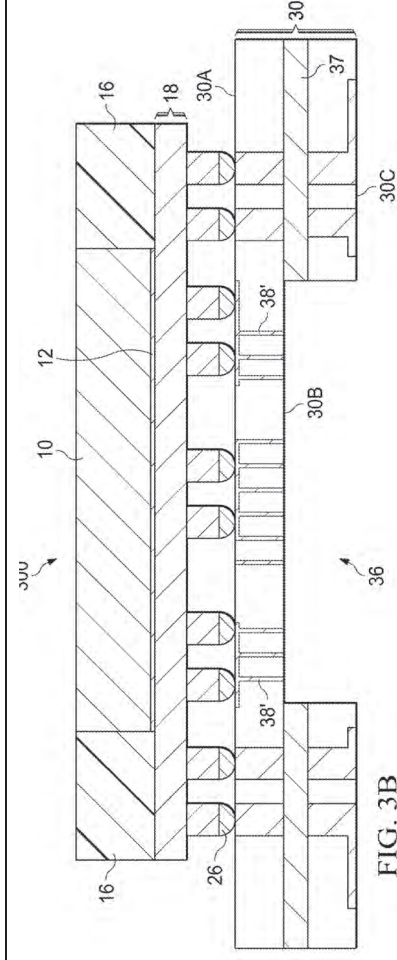
Where the chart below states that Yu '671 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Yu '671 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Yu '671 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

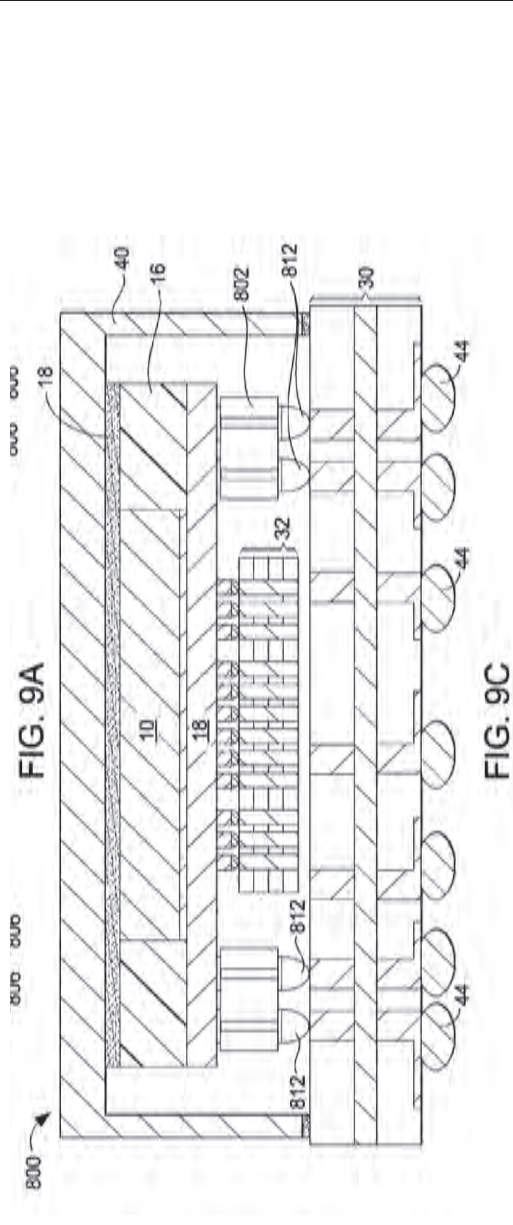
Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Yu '671 discloses, either expressly or inherently, a structure.</p> <p>See, <i>e.g.</i>:</p> <p>“FIGS. 1A through 1N illustrate cross-sectional views of various intermediary stages of manufacturing an integrated circuit (IC) package 100 (see FIG. 1N) in accordance with various embodiments. FIG. 1A illustrates a plurality of dies 10. Dies 10 may include a substrate, active devices, and interconnect layers (not shown). The substrate may be a bulk silicon substrate although other semiconductor materials including group III, group IV, and group V elements may also be used. Alternatively, the substrate may be a silicon-on-insulator</p>

	<p>(SOI) substrate. Active devices such as transistors may be formed on the top surface of the substrate. Interconnect layers may be formed over the active devices and the substrate.” Yu '671, [2:63-3:8].</p> <div></div> <p>FIG. 1A</p> <p>Yu '671, FIG. 1A.</p> <p>“FIG. 3B illustrates the singulation of dies 10 (e.g., along scribe lines using a suitable pick and place tool) and the attachment of dies 10 to package substrate 30 through connectors 26. Notably, die 10 may be bonded to package substrate 30 prior to the attachment of dies 32 to package 300. The configuration of package substrate 30 in package 300 may be altered from the configuration in package 100. For example, cavity 36 may be disposed on an opposing side (rather than a same side) of package substrate 30. In package 300, die 10 may be bonded to a surface 30 A of package substrate 30. Surface 30 A may be substantially level. Package substrate 30 may further include surface 30 B (e.g., in cavity 36) and surface 30 C opposing die 10. Due to the inclusion of cavity 36, surfaces 30 B and 30 C may not be substantially level.” Yu '671, [8:27-8:42].</p>
--	---



Yu '671, FIG. 3B.

“However, as illustrated by the cross-sectional view of FIG. 9C, in package 800, connectors 26 may be replaced by an interposer 802, which is used to bond a bottom surface of RDLs 18 to a top surface of package substrate 30. Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough.” Yu ’671 [13:9-13:15].



Yu '671, FIG. 9C.

“Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30. FIG. 11C further illustrates the completed package 900 after the formation of additional features, such as, heat dissipation feature 40 and connectors 44. FIG. 12 illustrates a process flow 1000 of a method for forming a semiconductor device package in accordance with some embodiments. In step 1002, one or more RDLs (e.g., RDLs 18) are formed on a surface of a first die (e.g., die 10). The one or more RDLs may extend laterally past edges of the first die (e.g., over a molding compound), and thus such RDLs may also be referred to as fan-out RDLs.” Yu '671, [14:20-14:31].

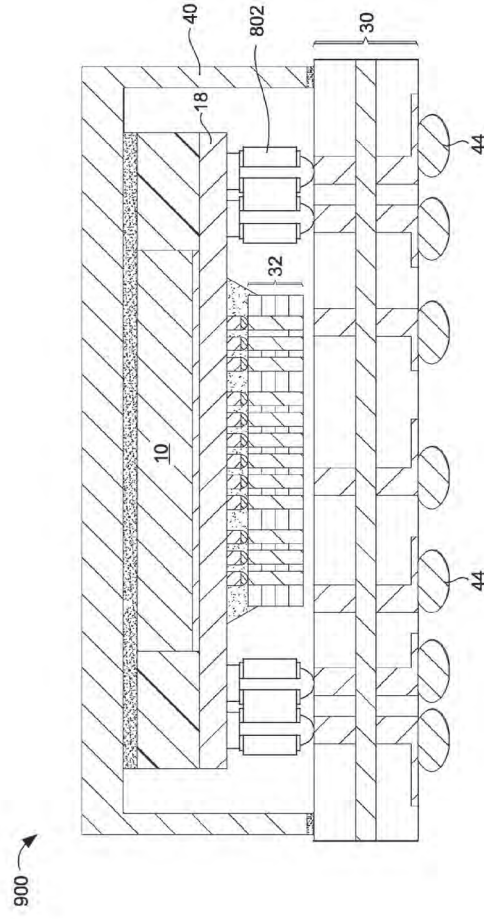


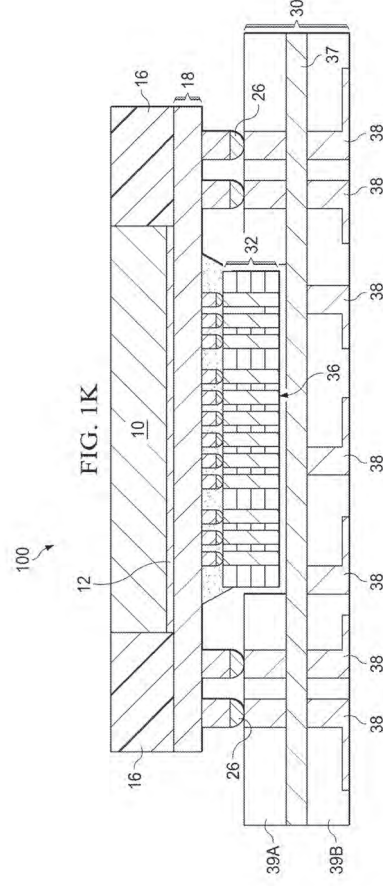
FIG. 11C

Yu '671, FIG. 11C.

“In step 1008, a package substrate (e.g., package substrate 30) is bonded to the surface of the one or more RDLs using the connector element. In some embodiments, the package substrate and the one or more second dies are bonded to a same surface of the one or more RDLs, and the one or more second dies may be disposed between the package substrate and the one or more RDLs. In order to accommodate this configuration, in such embodiments, the connector element may have a greater vertical dimension than the one or more second dies.” Yu ’671, [14:47-14:56].

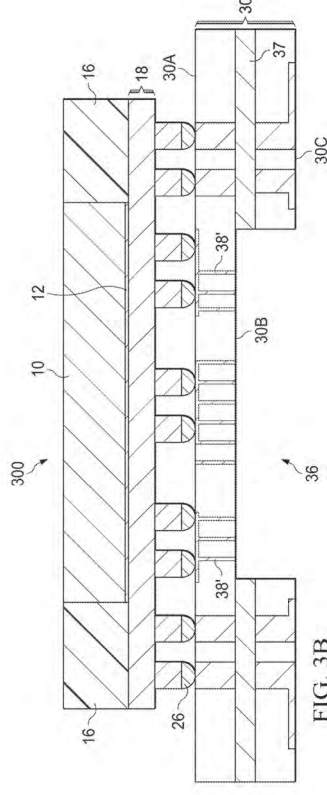
Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu ‘671 - U.S. Patent No. 10026671

	<p>“Thus, as described above, a package substrate may include a cavity. A first die may be bonded to the package substrate. Where the cavity may be on the same side of the package substrate as the first die or on an opposing side of the package substrate as the first die. One or more second dies may be bonded to the package substrate and the first die, and the second dies may be disposed in the cavity.” Yu ‘671, [14:57-14:63].</p>
[1.A] a bottom package substrate;	<p>Yu ‘671 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Next, as illustrated by FIG. 1K, each die stack 10 / 32 may be bonded to a package substrate 30 through connectors 26. A reflow may be performed on connectors 26 to bond die stack 10 / 32 to package substrate 30. Subsequently, as illustrated by FIG. 1L, an underfill 46 may be dispensed between die stack 10 / 32 and package substrate 30 around connectors 26. Underfill 46 may be substantially similar to underfill 34. Package substrate 30 may be an interposer, a printed circuit board (PCB), and the like. For example, package substrate 30 may include a core 37 and one or more build-up layers 39 (labeled 39 A and 39 B) disposed on either side of core 37.” Yu ‘671, [5:13-5:24].</p>



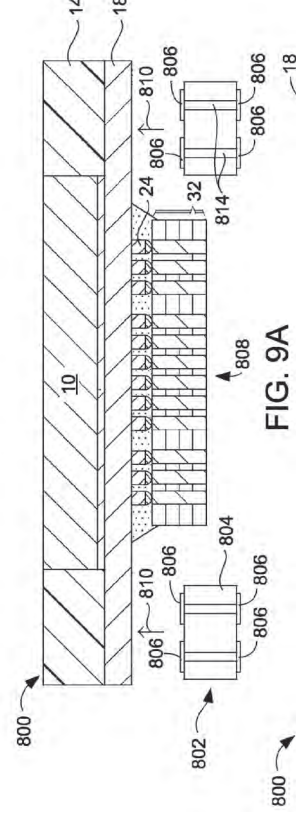
Yu '671, FIG. 1K.

“FIG. 3B illustrates the singulation of dies 10 (e.g., along scribe lines using a suitable pick and place tool) and the attachment of dies 10 to package substrate 30 through connectors 26. Notably, die 10 may be bonded to package substrate 30 prior to the attachment of dies 32 to package 300. The configuration of package substrate 30 in package 300 may be altered from the configuration in package 100. For example, cavity 36 may be disposed on an opposing side (rather than a same side) of package substrate 30. In package 300, die 10 may be bonded to a surface 30 A of package substrate 30. Surface 30 A may be substantially level. Package substrate 30 may further include surface 30 B (e.g., in cavity 36) and surface 30 C opposing die 10. Due to the inclusion of cavity 36, surfaces 30 B and 30 C may not be substantially level.” Yu ’671, [8:27-8:42].



Yu '671, FIG. 3B.

“However, as illustrated by the cross-sectional view of FIG. 9C, in package 800, connectors 26 may be replaced by an interposer 802, which is used to bond a bottom surface of RDLs 18 to a top surface of package substrate 30. Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough.” Yu ’671 [13:9-13:15].



Yu '671, FIG. 9A.

“Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30. FIG. 11C further illustrates the completed package 900 after the formation of additional features, such as, heat dissipation feature 40 and connectors 44. FIG. 12 illustrates a process flow 1000 of a method for forming a semiconductor device package in accordance with some embodiments. In step 1002, one or more RDLs (e.g., RDLs 18) are formed on a surface of a first die (e.g., die 10). The one or more RDLs may extend laterally past edges of the first die (e.g., over a molding compound), and thus such RDLs may also be referred to as fan-out RDLs.” Yu '671, [14:20-14:31].

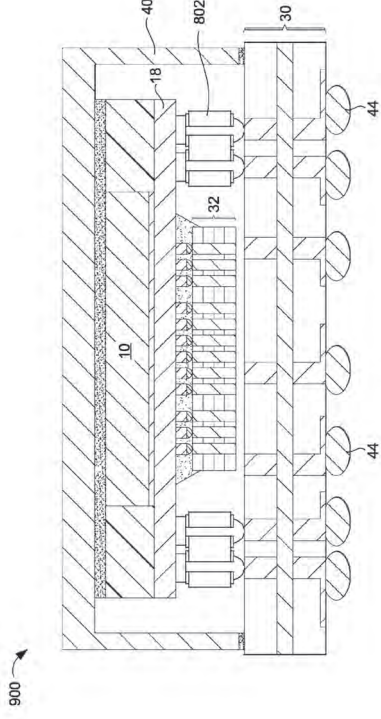


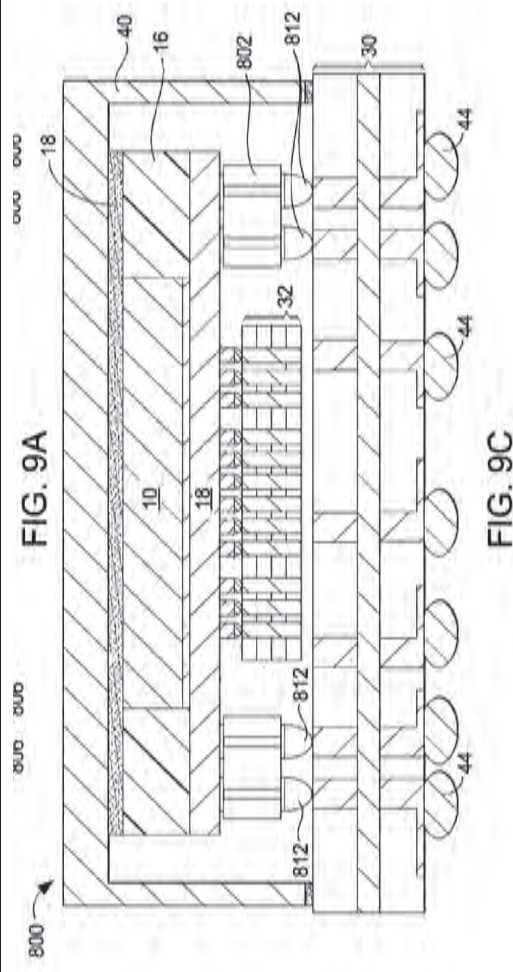
FIG. 11C

Yu '671, FIG. 11C.

“In step 1008, a package substrate (e.g., package substrate 30) is bonded to the surface of the one or more RDLs using the connector element. In some embodiments, the package

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>substrate and the one or more second dies are bonded to a same surface of the one or more RDLs, and the one or more second dies may be disposed between the package substrate and the one or more RDLs. In order to accommodate this configuration, in such embodiments, the connector element may have a greater vertical dimension than the one or more second dies.” Yu ’671, [14:47-14:56].</p> <p>“Thus, as described above, a package substrate may include a cavity. A first die may be bonded to the package substrate. Where the cavity may be on the same side of the package substrate as the first die or on an opposing side of the package substrate as the first die. One or more second dies may be bonded to the package substrate and the first die, and the second dies may be disposed in the cavity.” Yu ’671, [14:57-14:63].</p> <p>To the extent Plaintiff contends that Yu ’671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Yu ’671 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	 <p>FIG. 9A and FIG. 9C are cross-sectional views of a semiconductor device assembly. FIG. 9A shows a top package substrate 10 with a bottom surface 16 and a top surface 40. A spacer connector 18 is positioned between the bottom package substrate 10 and the top package substrate 30. The spacer connector 18 includes a central core 32 and side walls 812. The top package substrate 30 has a bottom surface 30 and a top surface 44. FIG. 9C shows a similar assembly with a spacer connector 18 between the bottom package substrate 10 and the top package substrate 30. The spacer connector 18 includes a central core 32 and side walls 812. The top package substrate 30 has a bottom surface 30 and a top surface 44.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Yu '671, FIG. 9C.</p> <p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Yu '671 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>“Subsequently, die stacks 10 / 34 may be singulated for packaging in an IC package. The singulation of die stacks 10 / 34 may include the use of a suitable pick-and-place tool. Next, as illustrated by FIG. 1K, each die stack 10 / 32 may be bonded to a package substrate 30 through connectors 26. A reflow may be performed on connectors 26 to bond die stack 10 / 32 to package substrate 30. Subsequently, as illustrated by FIG. 1L, an underfill 46 may be dispensed between die stack 10 / 32 and package substrate 30 around connectors 26. Underfill 46 may be substantially similar to underfill 34. Package substrate 30 may be an interposer, a printed circuit board (PCB), and the like. For example, package substrate 30 may include a core 37 and one or more build-up layers 39 (labeled 39 A and 39 B) disposed on either side of core 37. Interconnect structures 38 (e.g., conductive lines, vias, and/or through vias) may be included in package substrate 30 to provide functional electrical purposes such as power, ground, and/or signal layers. Other configurations of package substrate 30 may also be used. Furthermore, package substrate 30 may include a cavity 36. Cavity 36 may not extend through package substrate 30. Rather, a portion or all of build-up layers 39 A (e.g., build-up layers 39 disposed on a same side of core 37 as die stack 10 / 32) may be patterned to form cavity 36.” Yu '671, [5:9-5:33].</p> <p>“In packages 600 and 650, dies 32 and package substrate 30 may be bonded to a same surface of RDLs 18, which electrically connects dies 32, package substrate 30, and die 10. In such embodiments, dies 32 may be disposed between RDLs 18 and package substrate 30. Connectors 26 (e.g., bonding RDLs 18 to package substrate 30) maybe elongated to provide a sufficient standoff height to accommodate the vertical dimension of dies 32. For example, connectors 26 may have a vertical dimension that is greater than the combined vertical dimensions of dies 32 and connectors 24 (used to bond dies 32 to RDLs 18).” Yu '671, [10:12-10:22].</p>
--	---

	<p>“Each connector 26 may comprise one or more conductive pillars 27 comprising copper, nickel, gold, aluminum, combinations thereof, and the like, for example. In some embodiments (e.g., as illustrated by FIG. 6A), each connector 26 may include a single conductive pillar 27 extending from a bottom surface of RDLs 18. A solder region 26 ” (e.g., a solder ball) may be disposed on conductive pillar 27, and solder region 26 ” may contact and electrically connect to a contact pad on package substrate 30. In other embodiments (e.g., as illustrated by FIG. 6B), each connector 26 may include a first conductive pillar 27 ’ and a second conductive pillar 27 ”. The first conductive pillar 27 ’ extends from a bottom surface of RDLs 18. The second conductive pillar 27 ” extends from a top surface of package substrate 30. In such embodiments, solder ball 26 ” may be disposed between and contact the two conductive pillars 27 ’ and 27 ”. In packages 600 and 650, conductive pillars 27, 27 ’, and 27 ” may be elongated and relatively large compared to solder region 26 ”.” Yu ’671, [10:23-10:41].</p> <p>“FIG. 7 illustrates a cross-sectional view of semiconductor device package 700. Package 700 may be substantially similar to package 600 or 650 where like reference numerals represent like elements. However, connectors 26 have an alternative configuration in package 700. For example, connectors 26 in package 700 may comprise solder regions 702 and 704, and such connectors 26 are used to bond a bottom surface of RDLs 18 to a top surface of package substrate 30. RDLs 18 may provide electrical connection between die 10 (e.g., a logic die), dies 32, and package substrate 30. Similarly to packages 600 and 650, connectors 26 may have a vertical dimension that is sufficiently large to accommodate dies 32 between RDLs 18 and package substrate 30.” Yu ’671, [10:58-11:3].</p>
--	---

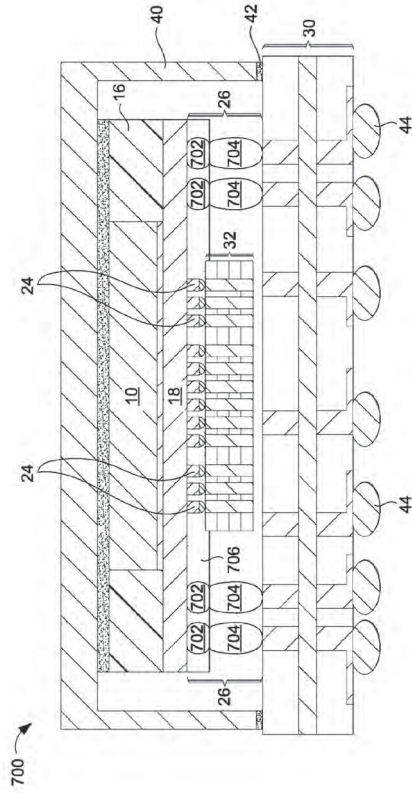
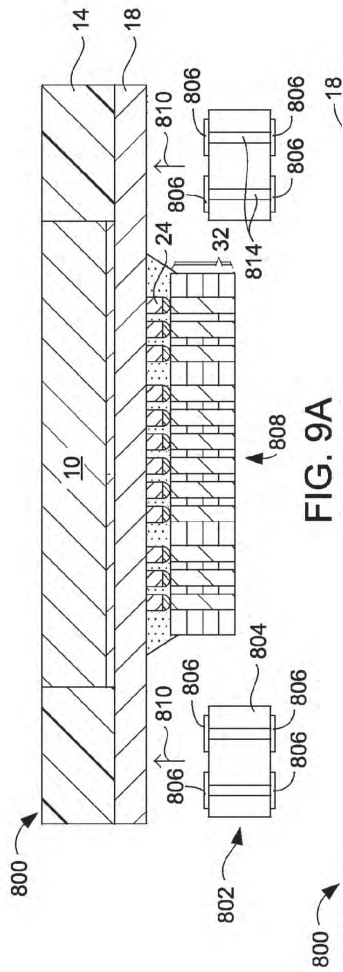


FIG. 7

Yu '671, FIG. 7.

“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814. In the illustrated embodiment, interposer 802 may be laminated to a bottom surface of RDLs 18 (as indicated by arrows 810), and contact pads 806 may be electrically connected to conductive features (not separately illustrated) in RDLs 18. Such conductive features may further provide electrical connection between interposer 802 and dies 10 / 32. Interposer 802

may have a suitable configuration and vertical dimension to accommodate dies 32 between RDLs 18 and package substrate 30.” Yu ’671, [13:14-13:33].



Yu ’671, FIG. 9A.

“In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26 ” extending through substrate 804. Interposer 802 may be attached to solder regions 26 ” using a reflow process, for example. In some embodiments, solder regions 26 ” may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26. Connectors 26 bonds interposer 802 to RDLs 18, and dies 32 may be disposed in a through hole 808 of interposer 802. Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30.” Yu ’671, [14:11-14:22].

To the extent Plaintiff contends that Yu ’671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.D] the spacer connector comprises a core substrate;	<p>Yu '671 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Package substrate 30 may be an interposer, a printed circuit board (PCB), and the like. For example, package substrate 30 may include a core 37 and one or more build-up layers 39 (labeled 39 A and 39 B) disposed on either side of core 37. Interconnect structures 38 (e.g., conductive lines, vias, and/or through vias) may be included in package substrate 30 to provide functional electrical purposes such as power, ground, and/or signal layers.” Yu '671, [5:20-5:27].</p> <p>“In FIG. 4A, core 37 is provided. Core 37 may be a metal-clad insulated base material such as a copper-clad epoxy-impregnated glass-cloth laminate, a copper-clad polyimide-impregnated glass-cloth laminate, or the like. As illustrated by FIG. 4B, cavity 36 and/or through holes 52 may be formed in core 37, for example, using a mechanical drilling or milling process.” Yu '671, [5:47-5:53].</p>

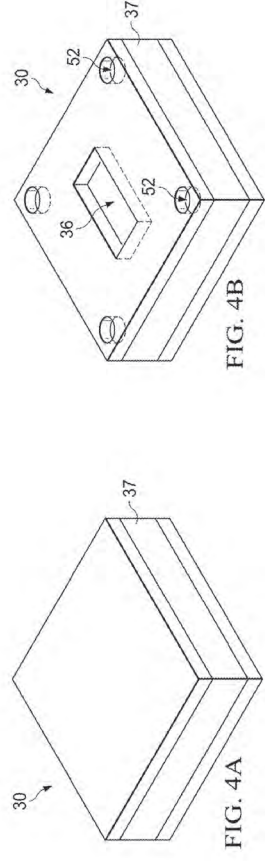


FIG. 4B

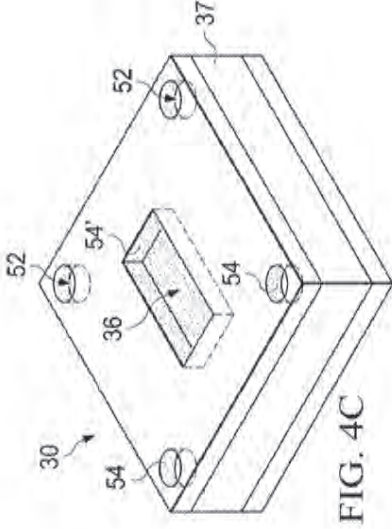
FIG. 4A

Yu '671, FIG. 4A & 4B.

“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814.” Yu '671, [13:14-13:24].

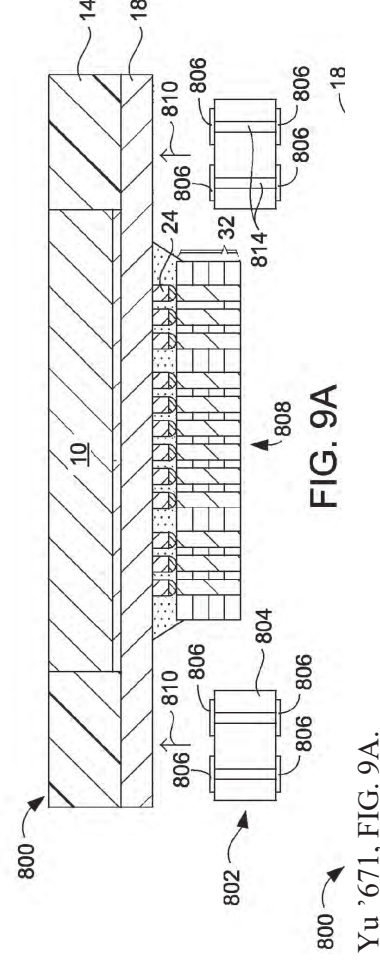
“FIG. 11A, an interposer 802 is provided having through holes 902 extending through substrate 804. Also provided are connectors 26 disposed on a bottom surface of RDLs 18. Connectors 26 may include UBM's 26' and solder regions 26". In some embodiments, solder regions 26" may have a sufficient vertical dimension to extend through openings 902 in interposer 802. In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26" extending through substrate 804. Interposer 802 may be attached to solder regions 26" using a reflow process, for example.” Yu '671, [14:5-14:15].

	<div></div> <div><p>FIG. 11A</p></div> <div><p>Yu '671, FIG. 11A.</p></div> <div><p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<div><p>Yu '671 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p></div> <div><p>See, <i>e.g.</i>:</p></div>

	<p>“Package substrate 30 may be an interposer, a printed circuit board (PCB), and the like. For example, package substrate 30 may include a core 37 and one or more build-up layers 39 (labeled 39 A and 39 B) disposed on either side of core 37. Interconnect structures 38 (e.g., conductive lines, vias, and/or through vias) may be included in package substrate 30 to provide functional electrical purposes such as power, ground, and/or signal layers.” Yu '671, [5:20-5:27].</p> <p>“Next, in FIG. 4C, surfaces of through hole 52 and cavity 36 may be plated with metallic material 54, for example, using an electrochemical plating process. In some embodiments, metallic material 54 may comprise copper. The plating of through holes 52 may form through vias for providing electrical connections from one side of core 37 to another.” Yu '671, [5:57-5:63].</p> <div></div> <p>FIG. 4C</p> <p>Yu '671, FIG. 4C.</p>
--	--

	<p>“In FIG. 4H, a build-up layer 39' may be laminated over conductive lines 38' (shown in ghost). The lamination of build-up layer 39' may include a curing process (e.g., a heat treatment or pressing process). Openings 62 may be patterned in build-up layer 39' (e.g., through laser drilling), and openings 62 may be aligned with conductive lines 38'. As illustrated by FIG. 4I, additional conductive lines 38'' may be formed over build-up layer 39' using a substantially similar process as illustrated by FIGS. 4E through 4H for forming conductive lines 38' (e.g., conductive layer plating and patterning). The conductive layer plating process used for forming conductive lines 38'' may also plate openings 62 (not illustrated in FIG. 4H), thus forming conductive vias (not illustrated) for interconnecting conductive lines 38' and 38'' through build-up layer 39'.” Yu '671, [6:17-6:31].</p> <div> <p>FIG. 4H</p> </div> <p>Yu '671, FIG. 4H.</p> <p>“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further</p>
--	---

comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804.” Yu ’671, [13:14-13:22].



To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Yu '671 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.

See, e.g.:

	<p>“In some embodiments, the ILD and IMDs comprise silicon oxide, SiCOH, and the like. A contact layer 12 including one or more contact pads is formed over the interconnect structure and may be electrically coupled to the active devices through various metallic lines and vias in the interconnect layers. Contact pads in contact layer 12 may be made of a metallic material such as aluminum, although other metallic materials may also be used.” Yu '671, [3:13-3:21].</p> <p>“FIG. 4J a solder resist 64 may be formed over build-up layers 39 (e.g., on both sides of core 37). Next, as illustrated by FIG. 4K, cavity 36 may be patterned in package substrate 30. The formation of cavity 36 may include patterning solder resist 63 (e.g., using an exposure technique) and a laser etching build-up layers 39 using material 54 ' as a laser stop layer. Thus, cavity 36 may not extend through package substrate 30. Furthermore, the patterning of solder resist 64 may pattern openings (not shown) around cavity 36 to expose interconnect structures 38 in build-up layers 39. These openings may be plated with a suitable material (e.g., nickel, aluminum, or the like) to form contact pads 66 on package substrate 30. Contact pads 66 may be electrically connected to interconnect structures 38 in build-up layers 39.” Yu '671, [6:41-6:55].</p> <div> <p>FIG. 4J</p> </div> <p>Yu, FIG. 4J.</p>
--	---

“In FIG. 8B, connectors 24 (e.g., used to subsequently bond RDLs 18 to dies 32, not illustrated in FIG. 8B) are at least partially formed in openings 712. For example, connectors 24 may be microbumps formed in openings 712 using an electrochemical plating process. Connectors 24 may comprise multiple conductive layers. For example, in FIG. 8B, connectors 24 include a copper portion 24 A and a nickel portion 24 B over the copper portion.” Yu '671, [11:45-11:52].

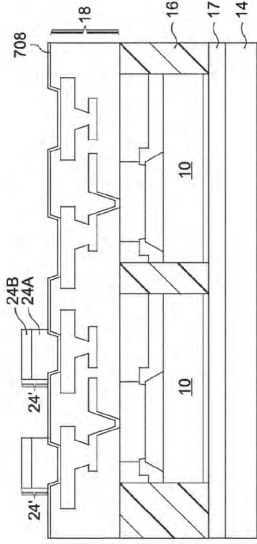
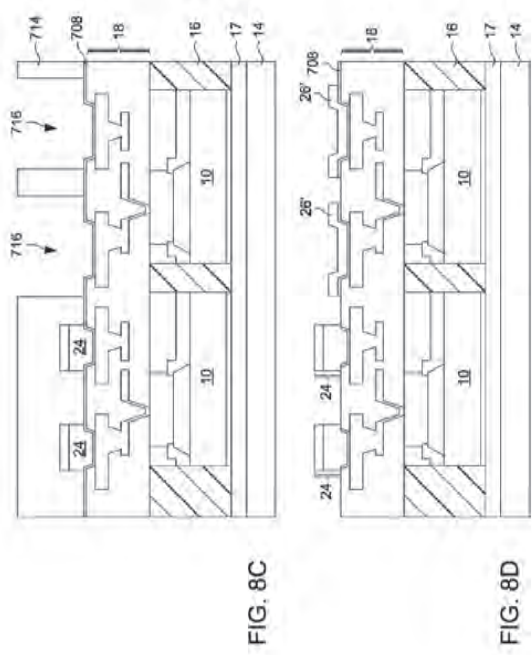


FIG. 8B

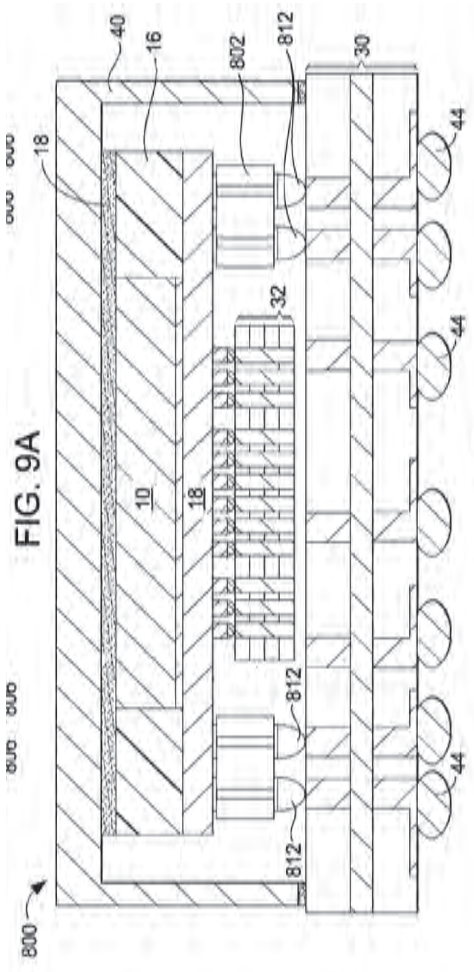
Yu '671, FIG. 8B.

“FIGS. 8C and 8D illustrate the formation of UBMs 26 ' for connectors 26. In FIG. 8C, a second photoresist 714 is formed over seed layer 708 and connectors 24. Photoresist 714 may mask over connectors 24, and photoresist 714 is patterned to include openings 716, which reveals portions of seed layer 708 previously masked by photoresist 710 (see FIG. 8A). Next, as illustrated by FIG. 8D, UBMs 26 ' are formed in openings 716 using an electrochemical plating process, for example.” Yu '671, [11:64-12:5].

	<div><p>FIG. 8C</p><p>FIG. 8D</p></div> <p>Yu '671, FIG. 8C & 8D.</p> <p>“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814.” Yu '671, [13:14-13:24].</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>“In some embodiments, solder regions 26 " may have a sufficient vertical dimension to extend through openings 902 in interposer 802. In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26 " extending through substrate 804. Interposer 802 may be attached to solder regions 26 " using a reflow process, for example. In some embodiments, solder regions 26 " may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26.” Yu '671, [14:9-14:18].</p> <div> </div> <p>Yu '671, FIG. 11B.</p> <p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Yu '671 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, e.g.:</p>

	 <p>FIG. 9A is a cross-sectional view of a semiconductor device 800. It shows a substrate 10 with a top layer 16 and a bottom layer 40. A central region 18 contains a series of vertical pillars 32. The pillars 32 are connected to a top contact layer 802 and a bottom contact layer 812. The bottom contact layer 812 is connected to a series of circular pads 44. FIG. 9C is a cross-sectional view of a semiconductor device 30. It shows a substrate 30 with a top layer 44 and a bottom layer 44. A central region 32 contains a series of vertical pillars 44. The pillars 44 are connected to a top contact layer 802 and a bottom contact layer 812. The bottom contact layer 812 is connected to a series of circular pads 44.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Yu '671, FIG. 9C.</p> <p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Yu '671 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p>

“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814. In the illustrated embodiment, interposer 802 may be laminated to a bottom surface of RDLs 18 (as indicated by arrows 810), and contact pads 806 may be electrically connected to conductive features (not separately illustrated) in RDLs 18.” Yu ’671, [13:14-13:28].

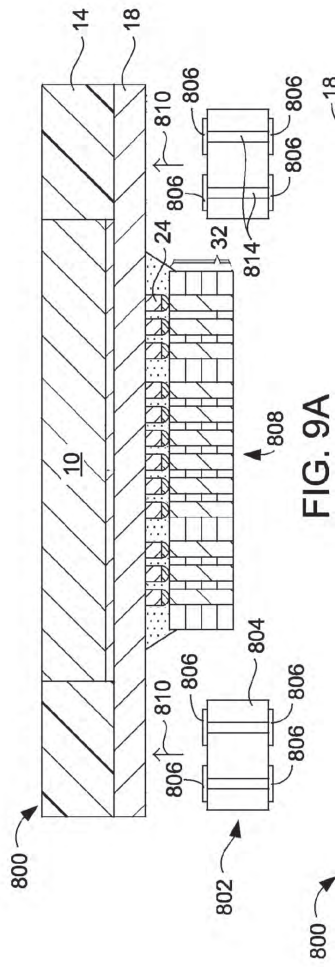


FIG. 9A

Yu '671, FIG. 9A.

“Subsequently, package substrate 30 may be bonded to a bottom surface of interposer 802 using connectors 812 (e.g., solder balls), which may be aligned with conductive vias 814. Interposer 802 and RDLs 18 may provide electrical connection between die 10 (e.g., a logic die), dies 32, and package substrate 30.” Yu ’671, [13:38-13:43].

	<p>“In package 850, interposer 802 may be bonded to RDLs 18 by connectors 26 rather than laminated on RDLs 18. In some embodiments (e.g., as illustrated by FIG. 10A), interposer 802 may be bonded to RDLs 18 prior to the attachment of package substrate 30. In alternative embodiments (e.g., as illustrated by FIG. 10B), interposer 802 may be first bonded to package substrate 30 (e.g., using connectors 812 and/or a lamination process), and die 10 /RDLs 18 are subsequently attached.” Yu ’671, [13:50-13:58].</p> <p>“Rather, at least a portion of connectors 26 may extend through openings 902 in interposer 802 to bond RDLs 18 to package substrate 30. For example, referring to FIG. 11A, an interposer 802 is provided having through holes 902 extending through substrate 804. Also provided are connectors 26 disposed on a bottom surface of RDLs 18. Connectors 26 may include UBMs 26 ’ and solder regions 26 ”.” Yu ’671, [14:2-14:9].</p> <p>“In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26 ” extending through substrate 804. Interposer 802 may be attached to solder regions 26 ” using a reflow process, for example. In some embodiments, solder regions 26 ” may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26. Connectors 26 bonds interposer 802 to RDLs 18, and dies 32 may be disposed in a through hole 808 of interposer 802. Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30.” Yu ’671, [14:11-14:22].</p>
--	---

	<p>FIG. 11B</p>
	<p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
	<p>Yu '671 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>
	<p>See, e.g.: “Interconnect structures 20 (e.g., conductive lines and/or vias) may be formed in polymer layers 22 and electrically connected to contact layer 12 of dies 10. The formation of interconnect structures 20 may include patterning polymer layers 22 (e.g., using a combination of photolithography and etching processes) and forming interconnect structures 20 (e.g., depositing a seed layer and using a mask layer to define the shape of interconnect structures 20) in the patterned polymer layers 22. Interconnect structures 20 may be formed</p>
[1.I]	<p>the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>of copper or a copper alloy although other metals such as aluminum, gold, and the like may also be used. Interconnect structures 20 may be electrically connected to contact pads in contact layer 12 (and as a result, active devices) in dies 10.” Yu ’671, [4:5-4:17].</p> <p>“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804.” Yu ’671, [13:14-13:22].</p> <p>“Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814. In the illustrated embodiment, interposer 802 may be laminated to a bottom surface of RDLs 18 (as indicated by arrows 810), and contact pads 806 may be electrically connected to conductive features (not separately illustrated) in RDLs 18. Such conductive features may further provide electrical connection between interposer 802 and dies 10 / 32. Interposer 802 may have a suitable configuration and vertical dimension to accommodate dies 32 between RDLs 18 and package substrate 30.” Yu ’671, [13:22-13:33].</p> <p>“Subsequently, package substrate 30 may be bonded to a bottom surface of interposer 802 using connectors 812 (e.g., solder balls), which may be aligned with conductive vias 814.” Yu ’671, [13:38-13:41].</p> <p>“In alternative embodiments (e.g., as illustrated by FIG. 10B), interposer 802 may be first bonded to package substrate 30 (e.g., using connectors 812 and/or a lamination process), and die 10 /RDLs 18 are subsequently attached.” Yu ’671, [13:54-13:58].</p>
--	---

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>“In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26 ” extending through substrate 804. Interposer 802 may be attached to solder regions 26 ” using a reflow process, for example. In some embodiments, solder regions 26 ” may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26. Connectors 26 bonds interposer 802 to RDLs 18, and dies 32 may be disposed in a through hole 808 of interposer 802. Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30.” Yu ’671, [14:11-14:22].</p> <p>To the extent Plaintiff contends that Yu ’671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Yu ’671 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface</p>

	<p>to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814. In the illustrated embodiment, interposer 802 may be laminated to a bottom surface of RDLs 18 (as indicated by arrows 810), and contact pads 806 may be electrically connected to conductive features (not separately illustrated) in RDLs 18. Such conductive features may further provide electrical connection between interposer 802 and dies 10 / 32. Interposer 802 may have a suitable configuration and vertical dimension to accommodate dies 32 between RDLs 18 and package substrate 30. For example, interposer 802 may include a through-hole extending therethrough as illustrated by the top down view of interposer 802 provided by FIG. 9B. When interposer 802 is bonded to RDLs 18, dies 32 may be (at least partially) disposed in through-hole 808. Subsequently, package substrate 30 may be bonded to a bottom surface of interposer 802 using connectors 812 (e.g., solder balls), which may be aligned with conductive vias 814. Interposer 802 and RDLs 18 may provide electrical connection between die 10 (e.g., a logic die), dies 32, and package substrate 30.” Yu ’671, [13:14-13:42].</p> <p>“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814.” Yu ’671, [13:14-13:24].</p> <p>“In package 850, interposer 802 may be bonded to RDLs 18 by connectors 26 rather than laminated on RDLs 18. In some embodiments (e.g., as illustrated by FIG. 10A), interposer 802 may be bonded to RDLs 18 prior to the attachment of package substrate 30. In alternative</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>embodiments (e.g., as illustrated by FIG. 10B), interposer 802 may be first bonded to package substrate 30 (e.g., using connectors 812 and/or a lamination process), and die 10 /RDLs 18 are subsequently attached. FIG. 10C illustrates the bonded package 850 having die 10, RDLs 18, interposer 802, dies 32 disposed in through hole 808 of interposer 802, and package substrate 30.” Yu ’671, [13:50-13:61].</p> <p>“In package 900, interposer 802 may not include conductive vias 814 (see FIG. 9A). Rather, at least a portion of connectors 26 may extend through openings 902 in interposer 802 to bond RDLs 18 to package substrate 30. For example, referring to FIG. 11A, an interposer 802 is provided having through holes 902 extending through substrate 804. Also provided are connectors 26 disposed on a bottom surface of RDLs 18. Connectors 26 may include UBMs 26 ’ and solder regions 26 ”. In some embodiments, solder regions 26 ” may have a sufficient vertical dimension to extend through openings 902 in interposer 802. In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26 ” extending through substrate 804. Interposer 802 may be attached to solder regions 26 ” using a reflow process, for example. In some embodiments, solder regions 26 ” may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26. Connectors 26 bonds interposer 802 to RDLs 18, and dies 32 may be disposed in a through hole 808 of interposer 802. Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30.” Yu ’671, [14:1-14:22].</p> <p>To the extent Plaintiff contends that Yu ’671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

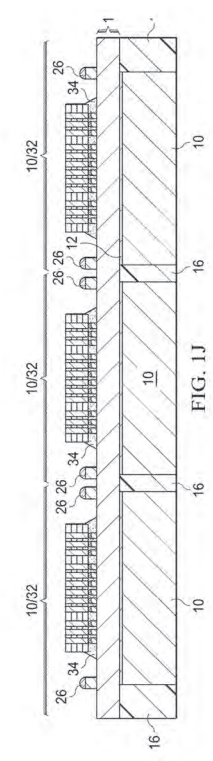
Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

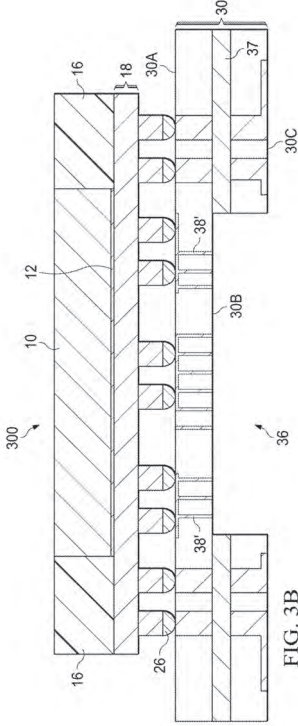
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Yu '671 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In packages 600 and 650, dies 32 and package substrate 30 may be bonded to a same surface of RDLs 18, which electrically connects dies 32, package substrate 30, and die 10. In such embodiments, dies 32 may be disposed between RDLs 18 and package substrate 30. Connectors 26 (e.g., bonding RDLs 18 to package substrate 30) maybe elongated to provide a sufficient standoff height to accommodate the vertical dimension of dies 32. For example, connectors 26 may have a vertical dimension that is greater than the combined vertical dimensions of dies 32 and connectors 24 (used to bond dies 32 to RDLs 18).” Yu '671, [10:12-10:22].</p> <p>“FIG. 7 illustrates a cross-sectional view of semiconductor device package 700. Package 700 may be substantially similar to package 600 or 650 where like reference numerals represent like elements. However, connectors 26 have an alternative configuration in package 700. For example, connectors 26 in package 700 may comprise solder regions 702 and 704, and such connectors 26 are used to bond a bottom surface of RDLs 18 to a top surface of package substrate 30. RDLs 18 may provide electrical connection between die 10 (e.g., a logic die), dies 32, and package substrate 30. Similarly to packages 600 and 650, connectors 26 may have a vertical dimension that is sufficiently large to accommodate dies 32 between RDLs 18 and package substrate 30.” Yu '671, [10:58-11:3].</p> <p>“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide,</p>
---	--

	<p>and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814. In the illustrated embodiment, interposer 802 may be laminated to a bottom surface of RDLs 18 (as indicated by arrows 810), and contact pads 806 may be electrically connected to conductive features (not separately illustrated) in RDLs 18. Such conductive features may further provide electrical connection between interposer 802 and dies 10 / 32. Interposer 802 may have a suitable configuration and vertical dimension to accommodate dies 32 between RDLs 18 and package substrate 30. For example, interposer 802 may include a through-hole extending therethrough as illustrated by the top down view of interposer 802 provided by FIG. 9B. When interposer 802 is bonded to RDLs 18, dies 32 may be (at least partially) disposed in through-hole 808.” Yu ’671, [13:14-13:37].</p> <p>“FIG. 10C illustrates the bonded package 850 having die 10, RDLs 18, interposer 802, dies 32 disposed in through hole 808 of interposer 802, and package substrate 30.” Yu ’671, [13:58-13:61].</p> <p>“In package 900, interposer 802 may not include conductive vias 814 (see FIG. 9A). Rather, at least a portion of connectors 26 may extend through openings 902 in interposer 802 to bond RDLs 18 to package substrate 30. For example, referring to FIG. 11A, an interposer 802 is provided having through holes 902 extending through substrate 804. Also provided are connectors 26 disposed on a bottom surface of RDLs 18. Connectors 26 may include UBMs 26 ’ and solder regions 26 ”. In some embodiments, solder regions 26 ” may have a sufficient vertical dimension to extend through openings 902 in interposer 802. In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26 ” extending through substrate 804. Interposer 802 may be attached to solder regions 26 ” using a reflow process,</p>
--	--

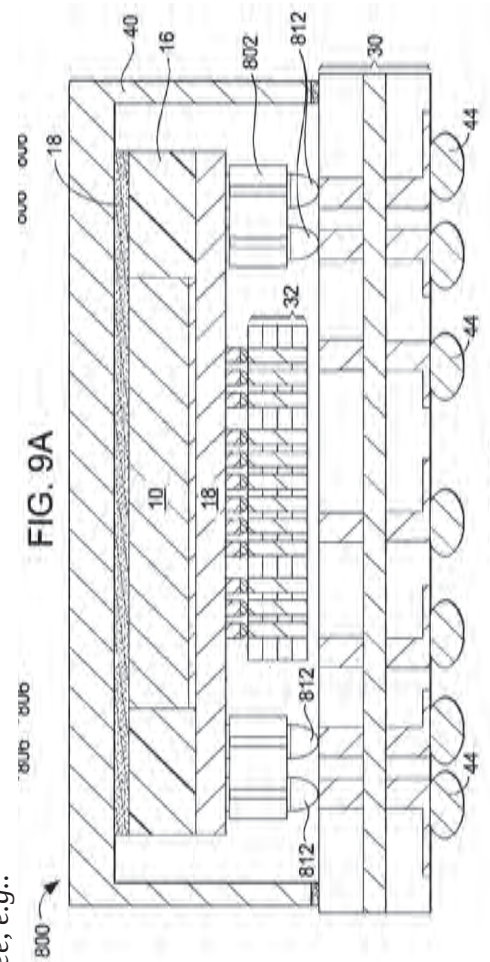
Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>for example. In some embodiments, solder regions 26 " may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26. Connectors 26 bonds interposer 802 to RDLs 18, and dies 32 may be disposed in a through hole 808 of interposer 802." Yu '671, [14:1-14:20].</p> <p>"In step 1008, a package substrate (e.g., package substrate 30) is bonded to the surface of the one or more RDLs using the connector element. In some embodiments, the package substrate and the one or more second dies are bonded to a same surface of the one or more RDLs, and the one or more second dies may be disposed between the package substrate and the one or more RDLs. In order to accommodate this configuration, in such embodiments, the connector element may have a greater vertical dimension than the one or more second dies." Yu '671, [14:47-14:56].</p> <p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Yu '671 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>"FIG. 1J illustrates the removal of carrier 14 from die stack 10 / 32 using any suitable method. For example, in an embodiment in which the adhesive between dies 10 and carrier 14 is formed of UV tape, dies 10 may be removed by exposing the adhesive layer to UV light. Subsequently, die stacks 10 / 34 may be singulated for packaging in an IC package. The</p>

	<p>singulation of die stacks 10 / 34 may include the use of a suitable pick-and-place tool. Next, as illustrated by FIG. 1K, each die stack 10 / 32 may be bonded to a package substrate 30 through connectors 26.” Yu ’671, [5:5-5:14].</p> <div></div> <p>Yu ’671, FIG. 1J.</p> <p>“Subsequently, die stacks 10 / 34 may be singulated for packaging in an IC package. The singulation of die stacks 10 / 34 may include the use of a suitable pick-and-place tool. Next, as illustrated by FIG. 1K, each die stack 10 / 32 may be bonded to a package substrate 30 through connectors 26. A reflow may be performed on connectors 26 to bond die stack 10 / 32 to package substrate 30.” Yu ’671, [5:9-5:16].</p> <p>“FIG. 3B illustrates the singulation of dies 10 (e.g., along scribe lines using a suitable pick and place tool) and the attachment of dies 10 to package substrate 30 through connectors 26. Notably, die 10 may be bonded to package substrate 30 prior to the attachment of dies 32 to package 300. The configuration of package substrate 30 in package 300 may be altered from the configuration in package 100. For example, cavity 36 may be disposed on an opposing side (rather than a same side) of package substrate 30. In package 300, die 10 may be bonded to a surface 30 A of package substrate 30.” Yu ’671, [8:27-8:38].</p>
--	--

	<div><p>FIG. 3B</p></div> <p>Yu '671, FIG. 3B.</p> <p>“Connectors 24 may be electrically connect dies 32 to die 10 through interconnect structures 38 in package substrate 30 (e.g., interconnect structures 38), connectors 26, and RDLs 18. Dies 32 may be disposed in cavity 36 of package substrate. In package 300, dies 32 and die 10 may be disposed on opposing sides of package substrate 30.” Yu '671, [9:10-9:15].</p> <p>“In some embodiments (e.g., as illustrated by FIG. 10A), interposer 802 may be bonded to RDLs 18 prior to the attachment of package substrate 30. In alternative embodiments (e.g., as illustrated by FIG. 10B), interposer 802 may be first bonded to package substrate 30 (e.g., using connectors 812 and/or a lamination process), and die 10 /RDLs 18 are subsequently attached.” Yu '671, [13:52-13:58].</p> <p>“In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26 ” extending through substrate 804. Interposer 802 may be attached to solder regions 26 ” using a reflow process, for example. In some embodiments, solder regions 26 ” may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26. Connectors 26 bonds interposer 802 to RDLs 18, and dies 32</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>may be disposed in a through hole 808 of interposer 802. Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30.” Yu ’671, [14:11-14:22].</p> <p>To the extent Plaintiff contends that Yu ’671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Yu ’671 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>  <p>FIG. 9A</p> <p>FIG. 9C</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>Yu '671, FIG. 9C.</p> <p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

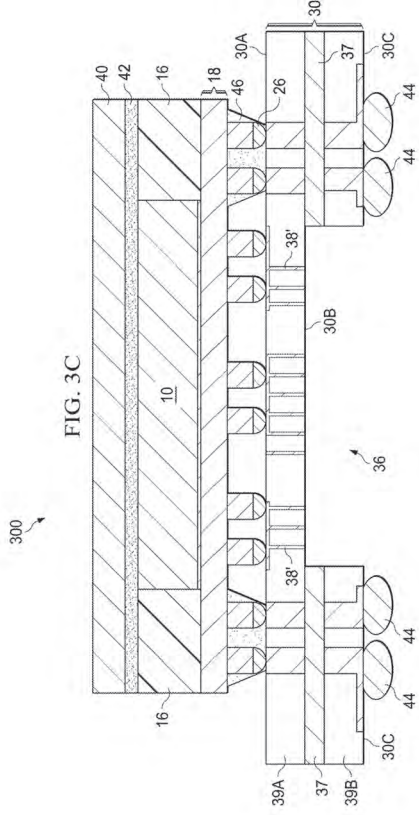
Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Yu '671 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Although a particular configuration of dies 10 and RDLs 18 is illustrated, alternative configurations may be applied (e.g., having a different number of RDLs 18 and/or connectors 24 / 26) in alternative embodiments. In FIG. 1H, a plurality of dies 32 may be bonded to dies 10 through connectors 24 (e.g., by reflowing connectors 24) to form die stacks 10 / 32. Dies 32 may be electrically connected to active devices in dies 10 through RDLs 18. In some embodiments, die stack 10 / 32 may include memory dies 32 (e.g., dynamic random access memory (DRAM) dies) bonded to dies 10, which may be logic dies providing control functionality for memory dies 32. In alternative embodiments, other types of dies may be included in dies stacks 10 / 32. Next, as illustrated in FIG. 1I, underfill 34 may be dispensed between dies 32 and RDLs 18 around connectors 24.” Yu '671, [4:56-5:4].</p>

	<p>“Subsequently, die stacks 10 / 34 may be singulated for packaging in an IC package. The singulation of die stacks 10 / 34 may include the use of a suitable pick-and-place tool. Next, as illustrated by FIG. 1K, each die stack 10 / 32 may be bonded to a package substrate 30 through connectors 26. A reflow may be performed on connectors 26 to bond die stack 10 / 32 to package substrate 30. Subsequently, as illustrated by FIG. 1L, an underfill 46 may be dispensed between die stack 10 / 32 and package substrate 30 around connectors 26. Underfill 46 may be substantially similar to underfill 34. Package substrate 30 may be an interposer, a printed circuit board (PCB), and the like. For example, package substrate 30 may include a core 37 and one or more build-up layers 39 (labeled 39 A and 39 B) disposed on either side of core 37. Interconnect structures 38 (e.g., conductive lines, vias, and/or through vias) may be included in package substrate 30 to provide functional electrical purposes such as power, ground, and/or signal layers. Other configurations of package substrate 30 may also be used. Furthermore, package substrate 30 may include a cavity 36. Cavity 36 may not extend through package substrate 30. Rather, a portion or all of build-up layers 39 A (e.g., build-up layers 39 disposed on a same side of core 37 as die stack 10 / 32) may be patterned to form cavity 36. As illustrated in FIG. 1L, cavity 36 may not affect the configuration of core 37 and/or build-up layers 39 B (e.g., build-up layers 39 disposed on an opposite side of core 37 as die stack 10 / 32).” Yu '671, [5:9-5:36].</p> <p>“In FIG. 4H, a build-up layer 39 ' may be laminated over conductive lines 38 ' (shown in ghost). The lamination of build-up layer 39 ' may include a curing process (e.g., a heat treatment or pressing process). Openings 62 may be patterned in build-up layer 39 ' (e.g., through laser drilling), and openings 62 may be aligned with conductive lines 38 '. As illustrated by FIG. 4I, additional conductive lines 38 " may be formed over build-up layer 39 ' using a substantially similar process as illustrated by FIGS. 4E through 4H for forming conductive lines 38 ' (e.g., conductive layer plating and patterning). The conductive layer</p>
--	---

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>plating process used for forming conductive lines 38 " may also plate openings 62 (not illustrated in FIG. 4H), thus forming conductive vias (not illustrated) for interconnecting conductive lines 38 ' and 38 " through build-up layer 39 '. Conductive lines 38 " may be patterned to align with conductive vias formed in openings 62. The process steps illustrated by FIGS. 4E through 4I may be repeated as desired to form any number of build-up layers (e.g., power, ground, and/or signal layers) in package substrate 30. Furthermore, although FIGS. 4E through 4I only illustrate the formation of interconnect structures 38 /build-up layers 39 on one side of core 37, similar processes may be applied to form of interconnect structures 38 /build-up layers 39 on an opposing side of core 37. FIG. 4J a solder resist 64 may be formed over build-up layers 39 (e.g., on both sides of core 37). Next, as illustrated by FIG. 4K, cavity 36 may be patterned in package substrate 30. The formation of cavity 36 may include patterning solder resist 63 (e.g., using an exposure technique) and a laser etching build-up layers 39 using material 54 ' as a laser stop layer. Thus, cavity 36 may not extend through package substrate 30." Yu '671, [6:17-6:48].</p> <p>"Referring back to FIG. 1L, when die stack 10 / 34 is bonded to package substrate 30, dies 32 may be disposed, at least partially, in cavity 36. In a top down view of package 100 (not shown), cavity 36 may encircle dies 32. Thus, the bonded structure may advantageously have a relatively small form factor and higher bandwidth." Yu '671, [6:58-6:63].</p> <p>"FIG. 3C illustrates the formation of various other features of package 300. For example, a reflow may be performed on connectors 26 and underfill 46 may be dispensed around connectors 26. Connectors 44 may be attached to surface 30 C of package substrate 30 opposite die 10. Furthermore, a heat dissipation feature 40 may be disposed over die 10 /molding compound 16. An interfacing material 42 (e.g., including a TIM and/or adhesive material) may be disposed between heat dissipation feature 40 and die 10 /molding compound 16." Yu '671, [8:50-8:59].</p>
--	--



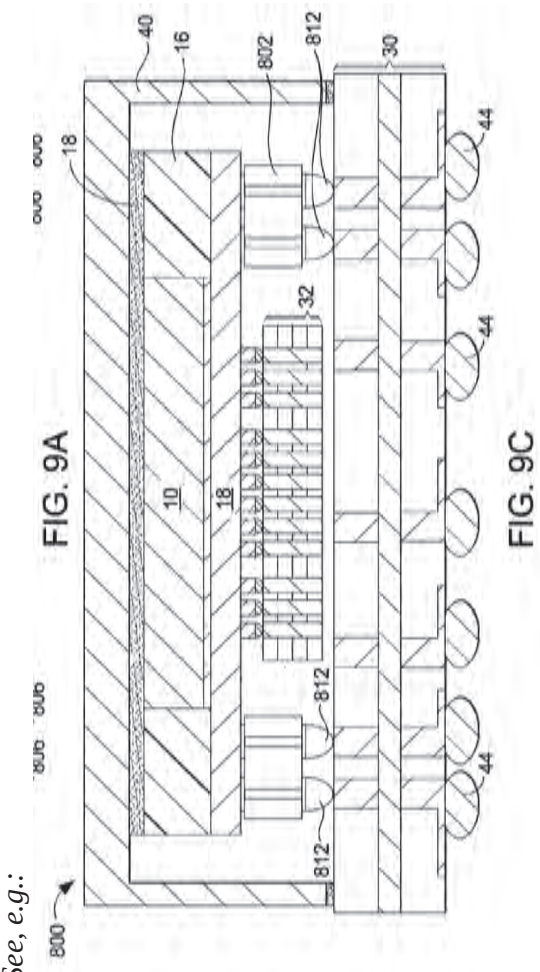
Yu '671, FIG. 3C.

“In some embodiments, die 32 may be disposed in a cavity formed in substrate 30 (as illustrated by FIG. 5A). In other embodiments, die 32 may be disposed in a through-hole 74 in substrate 30 (as illustrated by FIG. 5B). Through hole 74 may be formed in substrate 30, for example, using a laser drilling process.” Yu '671, [9:46-9:51].

To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 3, U.S. Patent No. 9859202

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Yu '671 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, e.g.:</p> <div><p>FIG. 9A is a cross-sectional view of a package assembly 800. It shows a top package substrate 10 with a top chip 18 mounted on its top surface. A bottom package substrate 16 is stacked below the top substrate. A spacer connector 32 is positioned between the two substrates. The top chip 18 overlaps the bottom chip and the spacer connector. Other components labeled include 40, 802, 812, and 30.</p><p>FIG. 9C is a cross-sectional view of the same assembly, showing the top chip 18 overlapping the bottom chip and the spacer connector 32. Other components labeled include 44 and 44.</p></div> <p>Yu '671, FIG. 9C.</p> <p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Yu '671 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In other embodiments (e.g., as illustrated by FIG. 6B), each connector 26 may include a first conductive pillar 27 ' and a second conductive pillar 27 ". The first conductive pillar 27 ' extends from a bottom surface of RDLs 18. The second conductive pillar 27 " extends from a top surface of package substrate 30.” Yu '671, [10:31-10:36].</p> <p>“In such embodiments, solder ball 26 " may be disposed between and contact the two conductive pillars 27 ' and 27 ". In packages 600 and 650, conductive pillars 27, 27 ', and 27 " may be elongated and relatively large compared to solder region 26 ".” Yu '671, [10:36-10:41].</p> <p>“Furthermore, in FIG. 6B, each of the first and second conductive pillars 27 ' and 27 " (of package 650) may account for at least about 20% to about 50% of the vertical dimension of each respective connector 26. In some embodiments, each conductive pillar 27 (in FIG. 6A) and conductive pillars 27 ' and 27 " (in FIG. 6B) may have a vertical dimension of about 100 μm or more.” Yu '671, [10:46-10:52].</p>

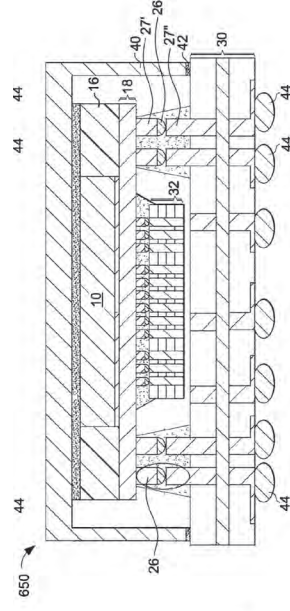


FIG. 6B

Yu '671, FIG. 6B.

“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814. In the illustrated embodiment, interposer 802 may be laminated to a bottom surface of RDLs 18 (as indicated by arrows 810), and contact pads 806 may be electrically connected to conductive features (not separately illustrated) in RDLs 18.” Yu ’671, [13:14-13:28].

“Subsequently, package substrate 30 may be bonded to a bottom surface of interposer 802 using connectors 812 (e.g., solder balls), which may be aligned with conductive vias 814.” Yu ’671, [13:38-13:41].

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Yu '671 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1E illustrates the formation of redistribution layers (RDLs) 18 over dies 10 and molding compound 16. As illustrated by FIG. 1E, RDLs 18 may extend laterally past edges of dies 10 over molding compound 16. RDLs 18 may include interconnect structures 20 formed in one or more polymer layers 22. Polymer layers 22 may be formed of any suitable material (e.g., polyimide (PI), polybenzoxazole (PBO), benzocyclobuten (BCB), epoxy, silicone, acrylates, nano-filled pheno resin, siloxane, a fluorinated polymer, polynorbornene, and the like) using any suitable method, such as, a spin-on coating technique, and the like. Interconnect structures 20 (e.g., conductive lines and/or vias) may be formed in polymer</p>

layers 22 and electrically connected to contact layer 12 of dies 10. The formation of interconnect structures 20 may include patterning polymer layers 22 (e.g., using a combination of photolithography and etching processes) and forming interconnect structures 20 (e.g., depositing a seed layer and using a mask layer to define the shape of interconnect structures 20) in the patterned polymer layers 22. Interconnect structures 20 may be formed of copper or a copper alloy although other metals such as aluminum, gold, and the like may also be used. Interconnect structures 20 may be electrically connected to contact pads in contact layer 12 (and as a result, active devices) in dies 10.” Yu ’671, [3:61-4:17].

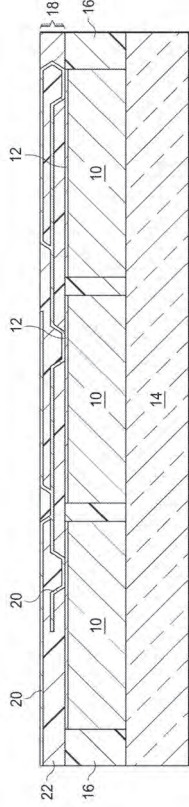
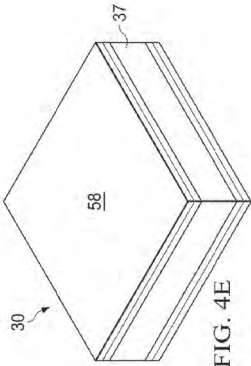


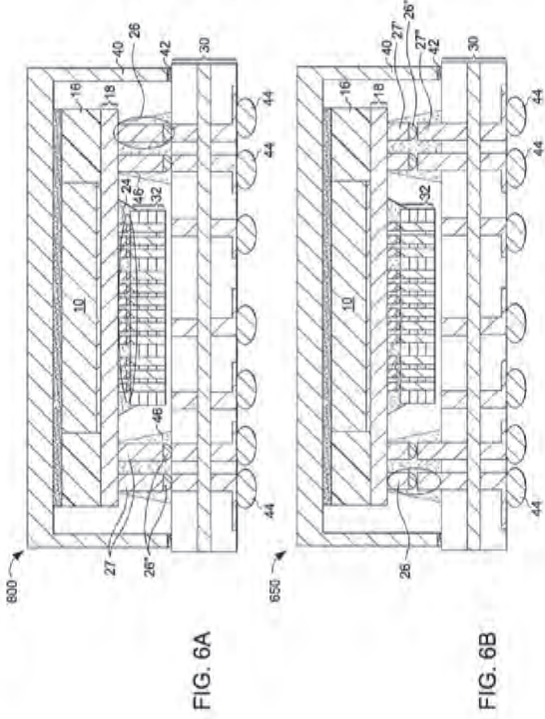
FIG. 1E

Yu ’671, FIG. 1E.

“As illustrated by FIGS. 4E through 4I, one or more build-up layers 39 having interconnect structures 38 may be formed on either side of core 37. The formation of build-up layers 39 may include plating core 37 with a conductive layer 58, for example, comprising copper as illustrated by FIG. 4E. Next, as illustrated by FIGS. 4F and 4G, conductive layer 58 may be patterned to form conductive lines 38’. The patterning of conductive layer 58 may include laminating a dry film 60 (e.g., a photoresist) over conductive layer 58, patterning dry film 60 (e.g., using suitable exposure techniques), and etching conductive layer 58 using the patterned dry film 60 as a mask. Subsequently, dry film 60 may be removed. In FIG. 4H, a build-up layer 39’ may be laminated over conductive lines 38’ (shown in ghost). The

	<p>lamination of build-up layer 39 ' may include a curing process (e.g., a heat treatment or pressing process). Openings 62 may be patterned in build-up layer 39 ' (e.g., through laser drilling), and openings 62 may be aligned with conductive lines 38 '. As illustrated by FIG. 4I, additional conductive lines 38 " may be formed over build-up layer 39 ' using a substantially similar process as illustrated by FIGS. 4E through 4H for forming conductive lines 38 ' (e.g., conductive layer plating and patterning). The conductive layer plating process used for forming conductive lines 38 " may also plate openings 62 (not illustrated in FIG. 4H), thus forming conductive vias (not illustrated) for interconnecting conductive lines 38 ' and 38 " through build-up layer 39 '. Conductive lines 38 " may be patterned to align with conductive vias formed in openings 62." Yu '671, [6:4-6:33].</p> <div></div> <p>FIG. 4E</p> <p>Yu '671, FIG. 4E.</p> <p>“FIGS. 6A and 6B illustrate cross-sectional views of semiconductor device packages 600 and 650, respectively. Packages 600 and 650 may be substantially similar to package 100 where like reference numerals represent like elements. Package substrates 30 in packages 600 and 650 may not include any cavities or through holes disposed therein. Rather, both top and bottom surfaces of package substrate 30 may be substantially level. In packages 600 and 650,</p>
--	---

	<p>dies 32 and package substrate 30 may be bonded to a same surface of RDLs 18, which electrically connects dies 32, package substrate 30, and die 10. In such embodiments, dies 32 may be disposed between RDLs 18 and package substrate 30. Connectors 26 (e.g., bonding RDLs 18 to package substrate 30) maybe elongated to provide a sufficient standoff height to accommodate the vertical dimension of dies 32. For example, connectors 26 may have a vertical dimension that is greater than the combined vertical dimensions of dies 32 and connectors 24 (used to bond dies 32 to RDLs 18). Each connector 26 may comprise one or more conductive pillars 27 comprising copper, nickel, gold, aluminum, combinations thereof, and the like, for example. In some embodiments (e.g., as illustrated by FIG. 6A), each connector 26 may include a single conductive pillar 27 extending from a bottom surface of RDLs 18. A solder region 26 " (e.g., a solder ball) may be disposed on conductive pillar 27, and solder region 26 " may contact and electrically connect to a contact pad on package substrate 30. In other embodiments (e.g., as illustrated by FIG. 6B), each connector 26 may include a first conductive pillar 27 ' and a second conductive pillar 27 ". The first conductive pillar 27 ' extends from a bottom surface of RDLs 18. The second conductive pillar 27 " extends from a top surface of package substrate 30. In such embodiments, solder ball 26 " may be disposed between and contact the two conductive pillars 27 ' and 27 ". Yu '671, [10:4-10:38].</p>
--	--



Yu '671, FIG. 6A & 6B.

“Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814. In the illustrated embodiment, interposer 802 may be laminated to a bottom surface of RDLs 18 (as indicated by arrows 810), and contact pads 806 may be electrically connected to conductive features (not separately illustrated) in RDLs 18. Such conductive features may

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu ‘671 - U.S. Patent No. 10026671

	<p>further provide electrical connection between interposer 802 and dies 10 / 32. Interposer 802 may have a suitable configuration and vertical dimension to accommodate dies 32 between RDLs 18 and package substrate 30. For example, interposer 802 may include a through-hole extending therethrough as illustrated by the top down view of interposer 802 provided by FIG. 9B. When interposer 802 is bonded to RDLs 18, dies 32 may be (at least partially) disposed in through-hole 808. Subsequently, package substrate 30 may be bonded to a bottom surface of interposer 802 using connectors 812 (e.g., solder balls), which may be aligned with conductive vias 814.” Yu ‘671, [13:14-13:41].</p> <p>“FIGS. 10A through 10D illustrate cross-sectional views of forming a semiconductor device package 850 according to alternative embodiments. Package 850 may be substantially similar to package 800 where like reference numerals represent like elements. In package 850, interposer 802 may be bonded to RDLs 18 by connectors 26 rather than laminated on RDLs 18. In some embodiments (e.g., as illustrated by FIG. 10A), interposer 802 may be bonded to RDLs 18 prior to the attachment of package substrate 30. In alternative embodiments (e.g., as illustrated by FIG. 10B), interposer 802 may be first bonded to package substrate 30 (e.g., using connectors 812 and/or a lamination process), and die 10 /RDLs 18 are subsequently attached. FIG. 10C illustrates the bonded package 850 having die 10, RDLs 18, interposer 802, dies 32 disposed in through hole 808 of interposer 802, and package substrate 30.” Yu ‘671, [13:46-13:61].</p>
--	---

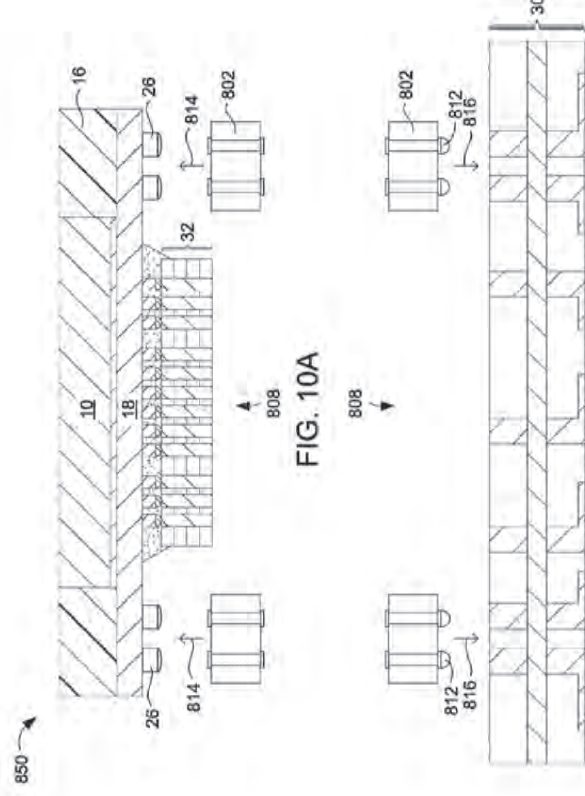
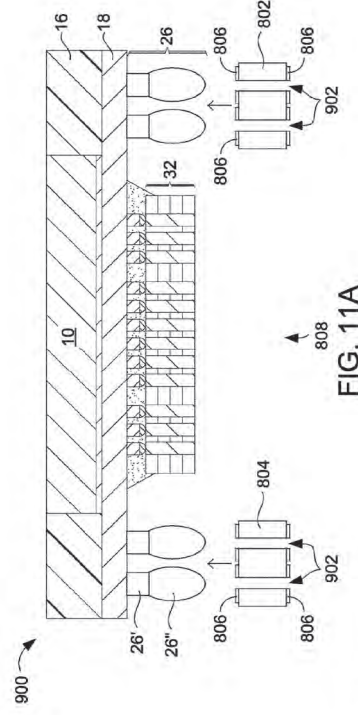


FIG. 10B

Yu '671, FIG. 10A & 10B.

“FIGS. 11A through 11C illustrate cross-sectional views of forming a semiconductor device package 900 according to alternative embodiments. Package 900 may be substantially similar to package 800 where like reference numerals represent like elements. In package 900, interposer 802 may not include conductive vias 814 (see FIG. 9A). Rather, at least a portion of connectors 26 may extend through openings 902 in interposer 802 to bond RDLs 18 to package substrate 30. For example, referring to FIG. 11A, an interposer 802 is provided having through holes 902 extending through substrate 804. Also provided are connectors 26

disposed on a bottom surface of RDLs 18. Connectors 26 may include UBMs 26' and solder regions 26". In some embodiments, solder regions 26" may have a sufficient vertical dimension to extend through openings 902 in interposer 802. In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26" extending through substrate 804. Interposer 802 may be attached to solder regions 26" using a reflow process, for example. In some embodiments, solder regions 26" may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26. Connectors 26 bonds interposer 802 to RDLs 18, and dies 32 may be disposed in a through hole 808 of interposer 802. Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30." Yu '671, [13:64-14:22].



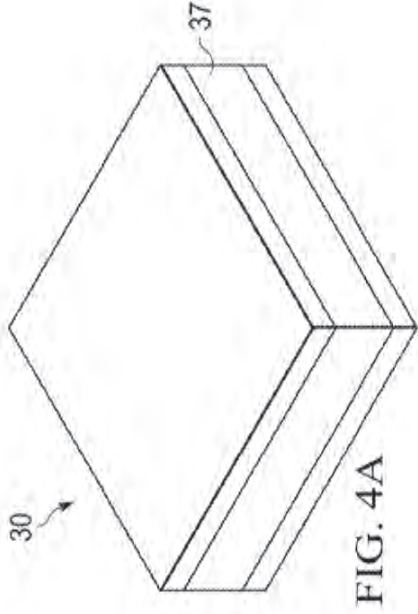
Yu '671, FIG. 11A.

To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the corresponding top metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the corresponding top metal pads of the spacer connector.</p>	<p>Yu '671 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In FIG. 4A, core 37 is provided. Core 37 may be a metal-clad insulated base material such as a copper-clad epoxy-impregnated glass-cloth laminate, a copper-clad polyimide-impregnated glass-cloth laminate, or the like. As illustrated by FIG. 4B, cavity 36 and/or through holes 52 may be formed in core 37, for example, using a mechanical drilling or milling process. The mechanical drilling/milling process may extend through holes 52 through core 37. However, the mechanical drilling/milling process may not extend cavity 36 through core 37. Next, in FIG. 4C, surfaces of through hole 52 and cavity 36 may be plated with metallic material 54, for example, using an electrochemical plating process. In some embodiments, metallic material 54 may comprise copper. The plating of through holes 52 may form through vias for providing electrical connections from one side of core 37 to another.” Yu '671, [5:47-5:63].</p>

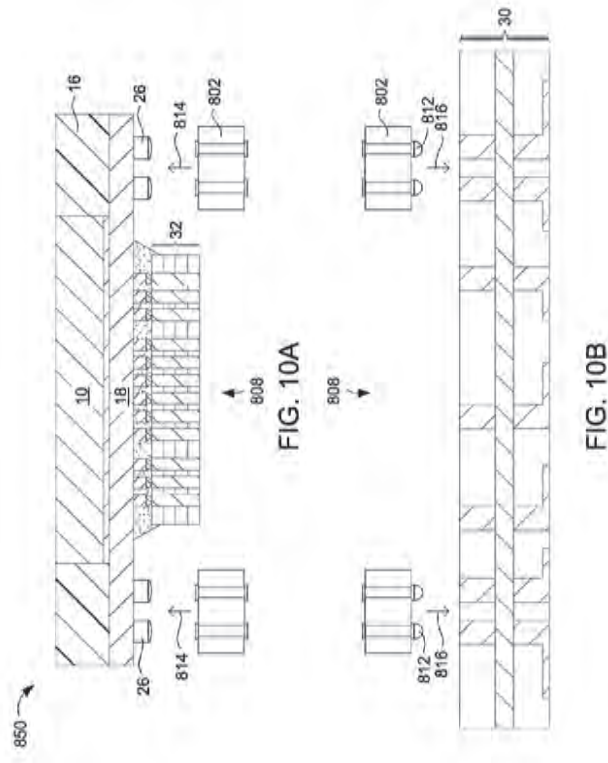


Yu '671, FIG. 4A.

“Next, as illustrated by FIGS. 4F and 4G, conductive layer 58 may be patterned to form conductive lines 38'. The patterning of conductive layer 58 may include laminating a dry film 60 (e.g., a photoresist) over conductive layer 58, patterning dry film 60 (e.g., using suitable exposure techniques), and etching conductive layer 58 using the patterned dry film 60 as a mask. Subsequently, dry film 60 may be removed. In FIG. 4H, a build-up layer 39' may be laminated over conductive lines 38' (shown in ghost). The lamination of build-up layer 39' may include a curing process (e.g., a heat treatment or pressing process). Openings 62 may be patterned in build-up layer 39' (e.g., through laser drilling), and openings 62 may be aligned with conductive lines 38'. As illustrated by FIG. 4I, additional conductive lines 38'' may be formed over build-up layer 39' using a substantially similar process as illustrated by FIGS. 4E through 4H for forming conductive lines 38' (e.g., conductive layer plating and

	<p>patterning). The conductive layer plating process used for forming conductive lines 38 " may also plate openings 62 (not illustrated in FIG. 4H), thus forming conductive vias (not illustrated) for interconnecting conductive lines 38 ' and 38 " through build-up layer 39 '. Conductive lines 38 " may be patterned to align with conductive vias formed in openings 62. The process steps illustrated by FIGS. 4E through 4I may be repeated as desired to form any number of build-up layers (e.g., power, ground, and/or signal layers) in package substrate 30. Furthermore, although FIGS. 4E through 4I only illustrate the formation of interconnect structures 38 /build-up layers 39 on one side of core 37, similar processes may be applied to form of interconnect structures 38 /build-up layers 39 on an opposing side of core 37." Yu '671, [6:9-6:40].</p> <p>"Referring to FIG. 9A, interposer 802 includes a substrate 804 having conductive vias 814 extending therethrough. Substrate 804 may comprise silicon and may or may not further comprise filler materials (e.g., e.g., silica filler, glass filler, aluminum oxide, silicon oxide, and the like). Conductive vias 814 may comprise copper, nickel, gold, aluminum combinations thereof, and the like, and conductive vias 814 may extend from a top surface to a bottom surface of substrate 804. Contact pads 806 (e.g., comprising a conductive material) may be formed on top and bottom surfaces of substrate 804 on conductive vias 814. In the illustrated embodiment, interposer 802 may be laminated to a bottom surface of RDLs 18 (as indicated by arrows 810), and contact pads 806 may be electrically connected to conductive features (not separately illustrated) in RDLs 18. Such conductive features may further provide electrical connection between interposer 802 and dies 10 / 32. Interposer 802 may have a suitable configuration and vertical dimension to accommodate dies 32 between RDLs 18 and package substrate 30. For example, interposer 802 may include a through-hole extending therethrough as illustrated by the top down view of interposer 802 provided by FIG. 9B. When interposer 802 is bonded to RDLs 18, dies 32 may be (at least partially) disposed in through-hole 808. Subsequently, package substrate 30 may be bonded to a bottom</p>
--	--

	<p>surface of interposer 802 using connectors 812 (e.g., solder balls), which may be aligned with conductive vias 814.” Yu ‘671, [13:14-13:41].</p> <p>“FIGS. 10A through 10D illustrate cross-sectional views of forming a semiconductor device package 850 according to alternative embodiments. Package 850 may be substantially similar to package 800 where like reference numerals represent like elements. In package 850, interposer 802 may be bonded to RDLs 18 by connectors 26 rather than laminated on RDLs 18. In some embodiments (e.g., as illustrated by FIG. 10A), interposer 802 may be bonded to RDLs 18 prior to the attachment of package substrate 30. In alternative embodiments (e.g., as illustrated by FIG. 10B), interposer 802 may be first bonded to package substrate 30 (e.g., using connectors 812 and/or a lamination process), and die 10 /RDLs 18 are subsequently attached. FIG. 10C illustrates the bonded package 850 having die 10, RDLs 18, interposer 802, dies 32 disposed in through hole 808 of interposer 802, and package substrate 30.” Yu ‘671, [13:46-13:61].</p>
--	---

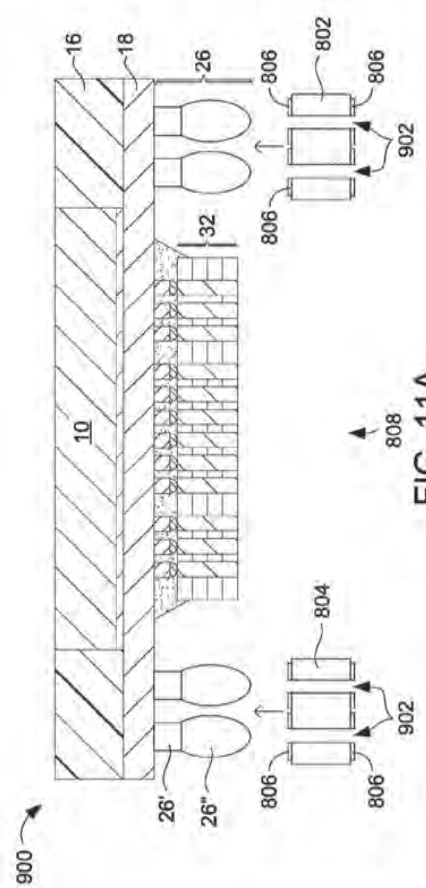
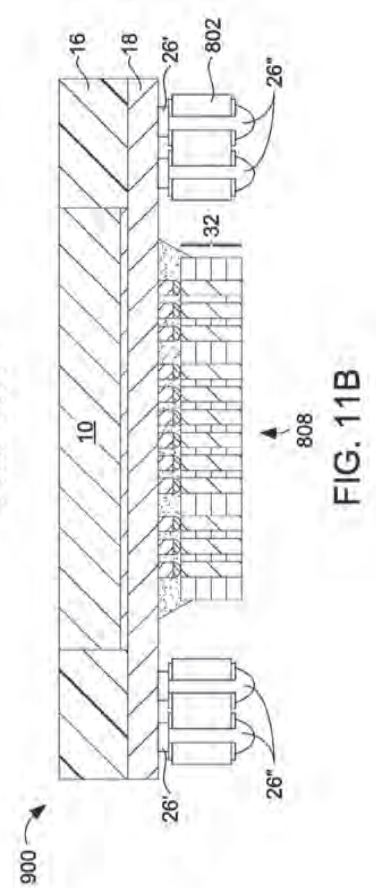


Yu '671, FIG. 10A & 10B.

“FIGS. 11A through 11C illustrate cross-sectional views of forming a semiconductor device package 900 according to alternative embodiments. Package 900 may be substantially similar to package 800 where like reference numerals represent like elements. In package 900, interposer 802 may not include conductive vias 814 (see FIG. 9A). Rather, at least a portion of connectors 26 may extend through openings 902 in interposer 802 to bond RDLs 18 to package substrate 30. For example, referring to FIG. 11A, an interposer 802 is provided having through holes 902 extending through substrate 804. Also provided are connectors 26 disposed on a bottom surface of RDLs 18. Connectors 26 may include UBMs 26 ' and solder regions 26 ". In some embodiments, solder regions 26 " may have a sufficient vertical

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu '671 - U.S. Patent No. 10026671

	<p>dimension to extend through openings 902 in interposer 802. In FIG. 11B, interposer 802 is bonded to connectors 26 with solder regions 26 " extending through substrate 804. Interposer 802 may be attached to solder regions 26 " using a reflow process, for example. In some embodiments, solder regions 26 " may further extend past a bottom surface of interposer 802. Furthermore, contact pads 806 may be electrically connected to connectors 26. Connectors 26 bonds interposer 802 to RDLs 18, and dies 32 may be disposed in a through hole 808 of interposer 802. Subsequently, as illustrated by FIG. 11C, connectors 26 are used to bond RDLs 18 to a package substrate 30." Yu '671, [13:64-14:22].</p>
--	--

	<div><p>FIG. 11A</p></div> <div><p>FIG. 11B</p></div>
	<p>Yu '671, FIG. 11A & 11B.</p> <p>To the extent Plaintiff contends that Yu '671 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9859202 in view of Yu ‘671 - U.S. Patent No. 10026671

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

E.D. Tex. Case No. 2:25-CV-118

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

U.S. Patent No.11107798 (“Yu ’798”) is titled Semiconductor Packages and Methods of Forming the Same and lists Chen-Hua Yu, Jing-Cheng Lin, and Po-Hao Tsai as inventors. Yu ’798 is assigned to Taiwan Semiconductor Manufacturing Company, Ltd. Yu ’798 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Yu ’798 is a U.S. patent that was filed May 18, 2020 and published September 3, 2020. Yu ’798 claims priority to US 9,543,170 filed on August 22, 2014. Yu ’798 is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(2).

The chart below provides representative examples of where each element of each Asserted Claim is found within Yu ’798, or otherwise rendered obvious by disclosures and teachings of Yu ’798, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Yu ’798 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Yu ’798 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Yu ’798, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Yu '798 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Yu '798 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Yu '798 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Yu '798 discloses, either expressly or inherently, a structure.</p> <p>See, e.g.:</p> <p>“FIG. 2C illustrates the semiconductor packages 300 being singulated. The semiconductor packages 300 may be removed from the frame 138 and placed over a structure 232, such as a dicing tape. The semiconductor packages 300 may be singulated by a cutting tool 234, such as a die saw, a laser, the like, or a combination thereof. The numbers of the first packages 100 and the second packages 200 in FIGS. 1A through 1J and FIGS. 2A through 2C are only for illustrative purposes and are not limiting.” Yu '798, [9:48-9:56].</p>

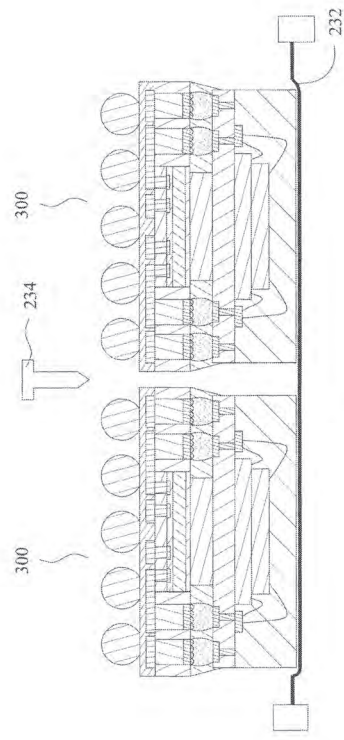
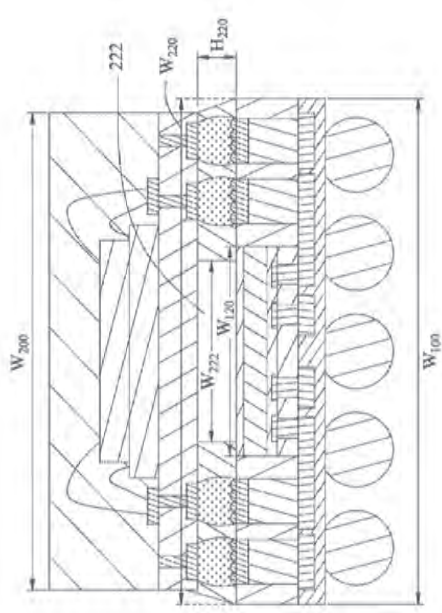


FIG. 2C

Yu '798, FIG. 2C.

“FIGS. 3A through 3C illustrate cross-sectional views of semiconductor packages 300 in accordance with some embodiments.” Yu '798, [9:59-9:61].

	<div></div> <div><p>FIG. 3A</p></div> <div><p>Yu '798, FIG. 3A.</p></div> <div><p>“FIG. 8 illustrates a cross-sectional view of a semiconductor package 400 in accordance with some embodiments. The semiconductor package 400 includes the semiconductor package 300 being mounted to a package substrate 402.” Yu '798, [12:27-12:30].</p></div>
--	---

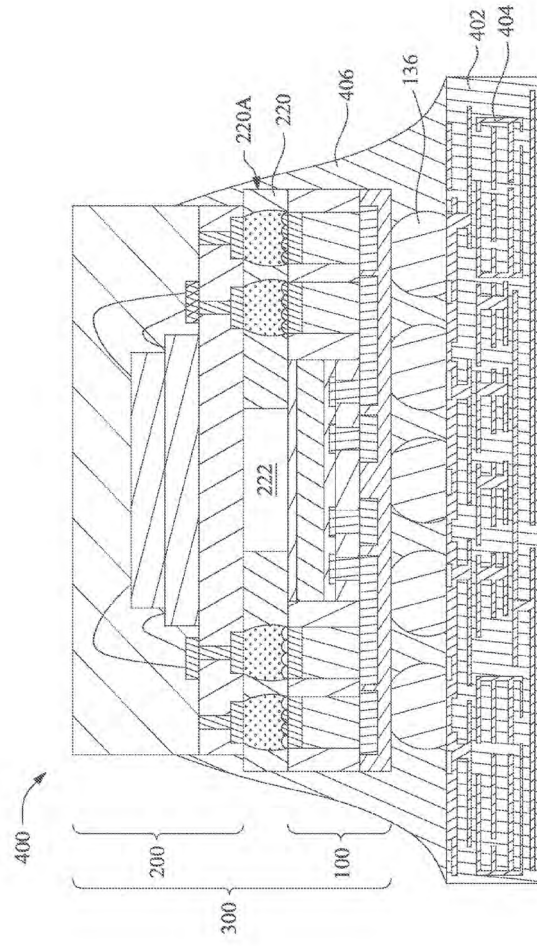


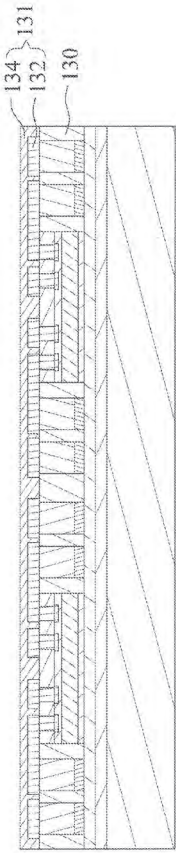
FIG. 8

Yu '798, FIG. 8.

“An embodiment is a method including forming a first package. The forming the first package including forming a first dielectric layer over a carrier substrate, forming a first electrical connector over the first dielectric layer, attaching a first die adjacent the first electrical connector and over the first dielectric layer, forming a redistribution layer over the first die and the first electrical connector, forming a second electrical connector over the redistribution layer, the second electrical connector being coupled to at least one of the first die and the first electrical connector, removing the carrier substrate to expose the first

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>dielectric layer, and removing the first dielectric layer to expose portions of the first die and the first electrical connector.” Yu ’798, [13:34-13:46].</p> <p>“A further embodiment is a semiconductor package including a first package. The first package including a first die, an encapsulant surrounding the first die, and a through package via extending through the encapsulant. The semiconductor package further including a second package comprising a second die, the second package being bonded to the first package by a set of connectors, and an underfill between the first package and the second package and surrounding the set of connectors, the underfill having sidewalls that are substantially perpendicular to a backside surface of the first die.” Yu ’798, [13:61-14:3].</p> <p>“A further embodiment is a package including a first package. The first package includes a first die, an encapsulant extending along sidewalls of the first die, and a plurality of conductive columns extending through the encapsulant. The package further includes a second package bonded to the first package.” Yu ’798, [14:4-14:9].</p>
[1.A] a bottom package substrate;	<p>Yu ’798 discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1F illustrates forming a redistribution layer 131 over the dies 120, the TTVs 110, and the molding material 130. The redistribution layer 131 may include one or more metal layers, sometimes referred to as M 1 and/or M N, wherein the metal layer M 1 is the metal layer immediately adjacent the dies 120, and metal layer M N (sometimes referred to as the top metal layer M N) is the metal layer furthest from the dies 120. Throughout the description, the term “metal layer” refers to the collection of metal lines 132 in the same layer. The redistribution layer 131 may include one or more passivation layers 134, wherein the one or</p>

	<p>more metal layers (M 1 through M N) are disposed in the one or more passivation layers 134. The passivation layers 134 can be silicon nitride, silicon carbide, silicon oxide, low-k dielectrics such as carbon doped oxides, extremely low-k dielectrics such as porous carbon doped silicon dioxide, a polymer, such as an epoxy, polyimide, BCB, PBO, solder resist (SR), the like, or a combination thereof, although other relatively soft, often organic, dielectric materials can also be used, and deposited by CVD, PVD, ALD, a spin-on-dielectric process, a lamination process, the like, or a combination thereof. The passivation layers 134 may undergo a curing step to cure the passivation layers 134, wherein the curing may be a thermal curing, a UV curing, the like, or a combination thereof.” Yu ’798, [5:16-5:41].</p> <div><p>The diagram shows a cross-section of a semiconductor device. It features a substrate 202 at the bottom, which is a semiconductor material like silicon or germanium. Above the substrate is a series of alternating layers: a conductive layer 130, a dielectric layer 131, another conductive layer 132, and a final dielectric layer 134. The passivation layers 134 are shown as thicker regions that encapsulate the underlying conductive and dielectric layers. The layers are labeled with reference numerals 130, 131, 132, and 134.</p></div> <p style="text-align: center;">FIG. 1F</p> <p>Yu ’798, FIG. 1F.</p> <p>“The substrate 202 may be made of a semiconductor material such as silicon, germanium, diamond, or the like. Alternatively, compound materials such as silicon germanium, silicon</p>
--	--

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>carbide, gallium arsenic, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, combinations of these, and the like, may also be used. Additionally, the substrate 202 may be a silicon-on-insulator (SOI) substrate. Generally, an SOI substrate includes a layer of a semiconductor material such as epitaxial silicon, germanium, silicon germanium, SOI, silicon germanium on insulator (SGOI), or combinations thereof. The substrate 202 is, in one alternative embodiment, based on an insulating core such as a fiberglass reinforced resin core. One example core material is fiberglass resin such as FR4. Alternatives for the core material include bismaleimide-triazine (BT) resin, or alternatively, other printed circuit board (PCB) materials or films. Build up films such as Ajinomoto build-up film (ABF) or other laminates may be used for substrate 202. The substrate 202 may be referred to as a package substrate 202.” Yu ’798, [7:38-7:57].</p> <p>“The substrate 202 may have bond pads 204 on a first side the substrate 202 to couple to the stacked dies 212, and bond pads 206 on a second side of the substrate 202, the second side being opposite the first side of the substrate 202, to couple to the conductive connectors 210.” Yu ’798, [8:10-8:14].</p> <p>“FIG. 8 illustrates a cross-sectional view of a semiconductor package 400 in accordance with some embodiments. The semiconductor package 400 includes the semiconductor package 300 being mounted to a package substrate 402. The semiconductor package 300 may be any of the embodiments of the semiconductor package 300 described above. The semiconductor package 300 is mounted to the package substrate 402 using the conductive connectors 136.” Yu ’798, [12:27-12:34].</p>
--	---

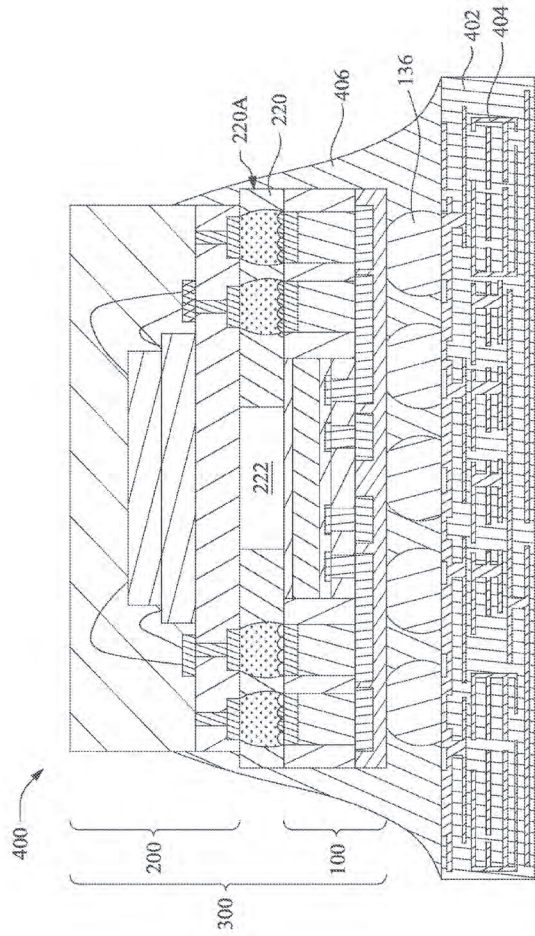


FIG. 8

Yu '798, FIG. 8.

“The package substrate 402 may be made of a semiconductor material such as silicon, germanium, diamond, or the like. Alternatively, compound materials such as silicon germanium, silicon carbide, gallium arsenic, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, combinations of these, and the like, may also be used. Additionally, the package substrate 402 may be a SOI substrate. Generally, an SOI substrate includes a layer of a semiconductor material such as epitaxial silicon, germanium, silicon germanium, SOI, SGOI, or combinations thereof. The

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>package substrate 402 is, in one alternative embodiment, based on an insulating core such as a fiberglass reinforced resin core. One example core material is fiberglass resin such as FR4. Alternatives for the core material include bismaleimide-triazine BT resin, or alternatively, other PCB materials or films. Build up films such as ABF or other laminates may be used for package substrate 402.” Yu '798, [12:35-12:52].</p> <p>“The package substrate 402 may also include metallization layers and vias 404. The metallization layers 404 may be formed over the active and passive devices and are designed to connect the various devices to form functional circuitry. The metallization layers 404 may be formed of alternating layers of dielectric (e.g., low-k dielectric material) and conductive material (e.g., copper) with vias interconnecting the layers of conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, or the like).” Yu '798, [12:60-13:2].</p> <p>To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Yu '798 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Referring to FIG. 2A, second packages 200 are bonded to the first package 100 with a set of conductive connectors 210 forming semiconductor packages 300. The second packages 200 each include a substrate 202 and one or more stacked dies 212 (212 A and 212 B)</p>

coupled to the substrate 202. The substrate 202 may be made of a semiconductor material such as silicon, germanium, diamond, or the like. Alternatively, compound materials such as silicon germanium, silicon carbide, gallium arsenic, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, combinations of these, and the like, may also be used. Additionally, the substrate 202 may be a silicon-on-insulator (SOI) substrate.” Yu ’798, [7:32-7:45].

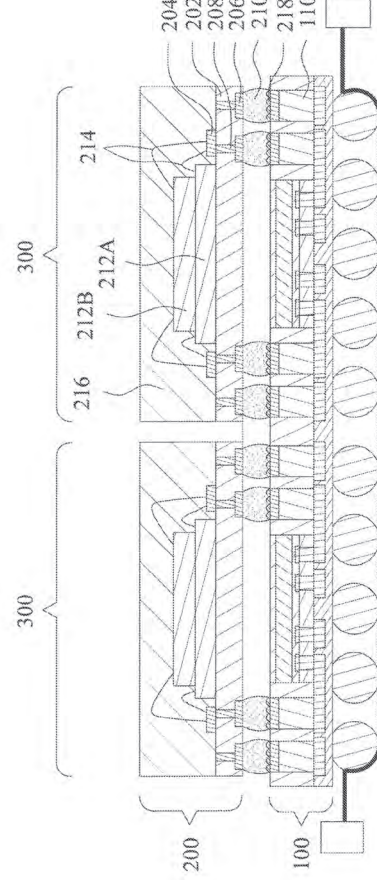
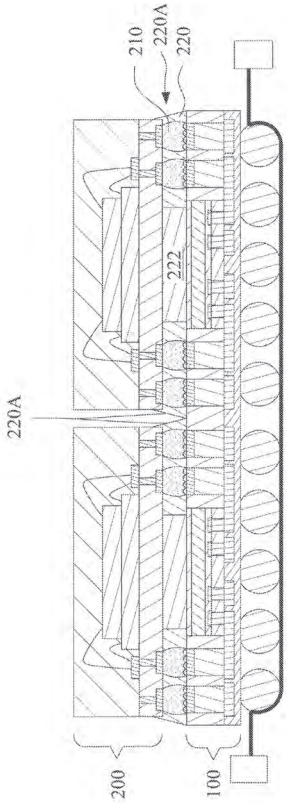


FIG. 2A

Yu '798, FIG. 2A.

“After the second packages 200 are formed, the packages 200 are bonded to the first packages 100 by way of conductive connectors 210, the bond pads 206, and the TIVs 110. In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110.” Yu ’798, [9:4-9:10].</p> <p>“FIG. 2B illustrates forming an underfill 220 between the first package 100 and the second package 200 and between the conductive connectors 210. The underfill 220 may be formed of a liquid epoxy, a deformable gel, a silicon rubber, a non-conductive film, a polymer, PBO, polyimide, solder resist, or a combination thereof. The underfill 220 provides structural support for the conductive connectors 210, and may be dispensed using capillary force after the conductive connectors 210 are bonded between the first package 100 and the second package 200.” Yu ’798, [9:34-9:43].</p>  <p style="text-align: center;">FIG. 2B</p> <p>Yu ’798, FIG. 2B.</p>
--	--

“FIG. 4B illustrates attaching second packages 200 to the first package 100 of FIG. 4A. This is similar to the process described above in FIG. 2A, except that the underfill 220 is present during the bonding process. Details regarding this embodiment that are similar to those for the previously described embodiment will not be repeated herein. The packages 200 and 100 will then be singulated as described above in FIG. 2C.” Yu '798, [11:24-11:31].

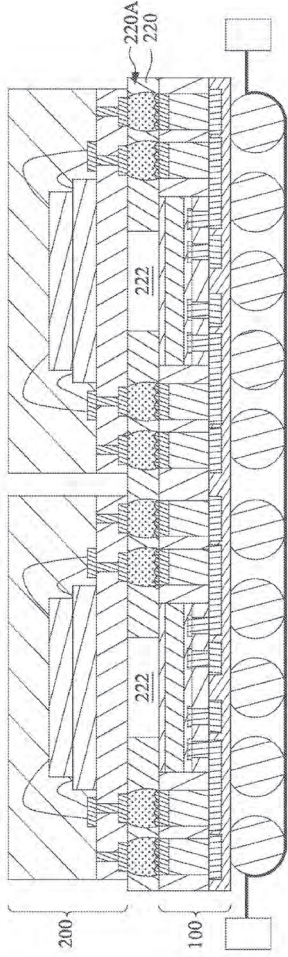


FIG. 4B

Yu '798, FIG. 4B.

“FIG. 8 illustrates a cross-sectional view of a semiconductor package 400 in accordance with some embodiments. The semiconductor package 400 includes the semiconductor package 300 being mounted to a package substrate 402. The semiconductor package 300 may be any of the embodiments of the semiconductor package 300 described above. The semiconductor package 300 is mounted to the package substrate 402 using the conductive connectors 136. The package substrate 402 may be made of a semiconductor material such as silicon,

germanium, diamond, or the like. Alternatively, compound materials such as silicon germanium, silicon carbide, gallium arsenic, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, combinations of these, and the like, may also be used. Additionally, the package substrate 402 may be a SOI substrate.” Yu '798, [12:27-12:42].

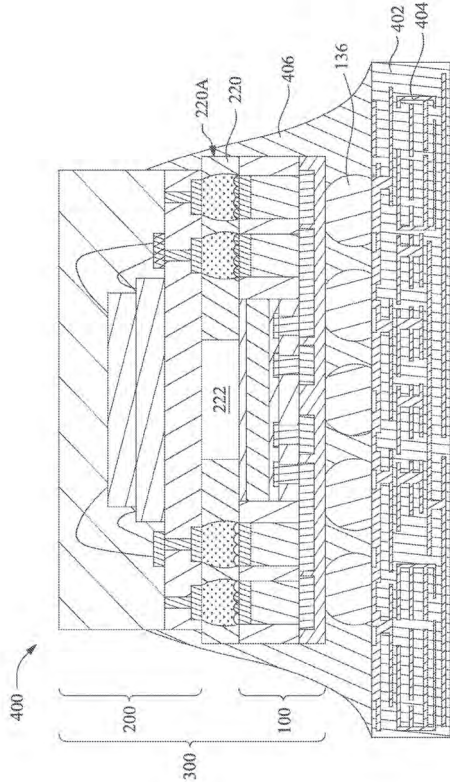


FIG. 8

Yu '798, FIG. 8.

“Another embodiment is a method including forming a first die package, the first die package including a first die, a first electrical connector, and a first redistribution layer, the first redistribution layer being coupled to the first die and the first electrical connector, forming an underfill over the first die package, patterning the underfill to have an opening to expose a portion of the first electrical connector, and bonding a second die package to the first die

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>package with a bonding structure, the bonding structure being coupled to the first electrical connector in the opening of the underfill.” Yu ’798, [13:51-13:60].</p> <p>To the extent Plaintiff contends that Yu ’798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Yu ’798 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“After the second packages 200 are formed, the packages 200 are bonded to the first packages 100 by way of conductive connectors 210, the bond pads 206, and the TIVs 110. In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110. The conductive connectors 210 may be similar to the conductive connectors 136 described above and the description is not repeated herein, although the conductive connectors 210 and 136 need not be the same. In some embodiments, before bonding the conductive connectors 210, the conductive connectors 210 are coated with a flux (not shown), such as a no-clean flux. The conductive connectors 210 may be dipped in the flux or the flux may be jetted onto the conductive connectors 210. In another embodiment, the flux may be applied to the surfaces of the TIVs 110. The bonding between the second package 200 and the first package 100 may be a solder bonding or a direct metal-to-metal (such as a copper-to-copper or tin-to-tin) bonding. In an embodiment, the second package 200 is bonded to the</p>

	<p>first package 100 by a reflow process. During this reflow process, the conductive connectors 210 are in contact with the bond pads 206 and the TIV's 110 to physically and electrically couple the second package 200 to the first package 100.” Yu '798, [9:4-9:28].</p> <p>“FIG. 2B illustrates forming an underfill 220 between the first package 100 and the second package 200 and between the conductive connectors 210. The underfill 220 may be formed of a liquid epoxy, a deformable gel, a silicon rubber, a non-conductive film, a polymer, PBO, polyimide, solder resist, or a combination thereof. The underfill 220 provides structural support for the conductive connectors 210, and may be dispensed using capillary force after the conductive connectors 210 are bonded between the first package 100 and the second package 200. In these embodiments, the underfill 220 includes a fillet where a sidewalls 220 A that are diagonal to backside surfaces 120 B of the dies 120. In some embodiments, the underfill 220 is formed to leave openings 222 over the dies 120.” Yu '798, [9:34-9:47].</p> <p>“The underfill 220 has a height H 220 between the first and second packages 100 and 200 (sometimes referred to as a standoff height). In an embodiment, the height H 220 is from about 1 μm to about 200 μm.” Yu '798, [10:6-10:9].</p> <p>“The underfill 220 may be formed to have the height H 220 from about 1 μm to about 200 μm. In this embodiment, the underfill 220 has sidewalls 220 A that are substantially perpendicular to backside surfaces 120 B of the dies 120.” Yu '798, [11:17-11:21].</p> <p>“FIG. 4B illustrates attaching second packages 200 to the first package 100 of FIG. 4A. This is similar to the process described above in FIG. 2A, except that the underfill 220 is present during the bonding process.” Yu '798, [11:24-11:27].</p>
--	--

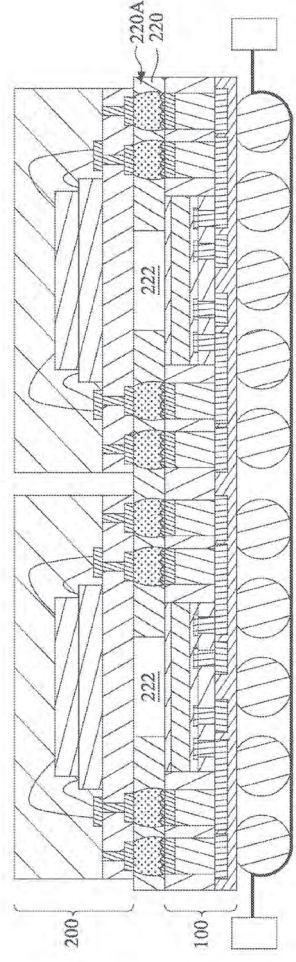


FIG. 4B

Yu '798, FIG. 4B.

“The semiconductor package 400 includes an underfill 406 between the semiconductor package 300 and the substrate 402 and between the conductive connectors 136. The underfill 406 may be formed of a liquid epoxy, a deformable gel, a silicon rubber, a non-conductive film, a polymer, PBO, polyimide, solder resist, or a combination thereof. The underfill 406 provides structural support for the conductive connectors 136, and may be dispensed using capillary force after the conductive connectors 136 are bonded between the semiconductor package 300 and the substrate 402.” Yu ’798, [13:5-13:14].

To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Yu '798 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The substrate 202 may be made of a semiconductor material such as silicon, germanium, diamond, or the like. Alternatively, compound materials such as silicon germanium, silicon carbide, gallium arsenic, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, combinations of these, and the like, may also be used. Additionally, the substrate 202 may be a silicon-on-insulator (SOI) substrate. Generally, an SOI substrate includes a layer of a semiconductor material such as epitaxial silicon, germanium, silicon germanium, SOI, silicon germanium on insulator (SGOI), or combinations thereof.” Yu '798, [7:38-7:49].</p> <p>“The substrate 202 is, in one alternative embodiment, based on an insulating core such as a fiberglass reinforced resin core. One example core material is fiberglass resin such as FR4. Alternatives for the core material include bismaleimide-triazine (BT) resin, or alternatively, other printed circuit board (PCB) materials or films. Build up films such as Ajinomoto build-up film (ABF) or other laminates may be used for substrate 202.” Yu '798, [7:49-7:56].</p> <p>“The package substrate 402 may be made of a semiconductor material such as silicon, germanium, diamond, or the like. Alternatively, compound materials such as silicon germanium, silicon carbide, gallium arsenic, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, combinations of these, and the like, may also be used. Additionally, the package substrate 402 may be a SOI substrate. Generally, an SOI substrate includes a layer of a semiconductor material such as epitaxial silicon, germanium, silicon germanium, SOI, SGOI, or combinations thereof.” Yu '798, [12:35-12:45].</p>
--	--

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>“The package substrate 402 is, in one alternative embodiment, based on an insulating core such as a fiberglass reinforced resin core. One example core material is fiberglass resin such as FR4. Alternatives for the core material include bismaleimide-triazine BT resin, or alternatively, other PCB materials or films. Build up films such as ABF or other laminates may be used for package substrate 402.” Yu ’798, [12:45-12:52].</p> <p>To the extent Plaintiff contends that Yu ’798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Yu ’798 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The devices may be formed using any suitable methods. The substrate 202 may also include metallization layers (not shown) and through vias 208. The metallization layers may be formed over the active and passive devices and are designed to connect the various devices to form functional circuitry. The metallization layers may be formed of alternating layers of dielectric (e.g., low-k dielectric material) and conductive material (e.g., copper) with vias interconnecting the layers of conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, or the like).” Yu ’798, [7:63-8:7].</p> <p>“The package substrate 402 may also include metallization layers and vias 404. The metallization layers 404 may be formed over the active and passive devices and are designed</p>

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

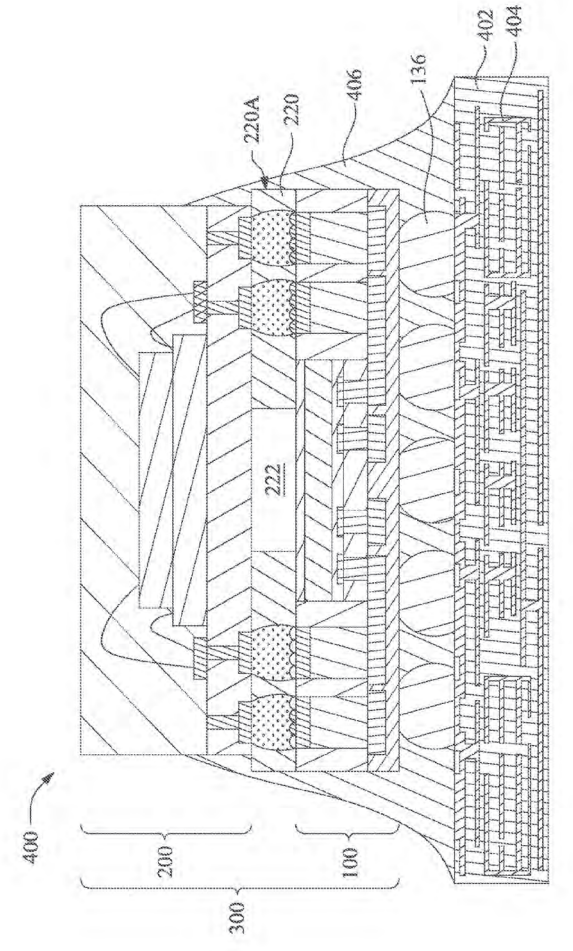
	<p>to connect the various devices to form functional circuitry. The metallization layers 404 may be formed of alternating layers of dielectric (e.g., low-k dielectric material) and conductive material (e.g., copper) with vias interconnecting the layers of conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, or the like).” Yu ’798, [12:60-13:2].</p> <p>“The metallization layers may be formed over the active and passive devices and are designed to connect the various devices to form functional circuitry. The metallization layers may be formed of alternating layers of dielectric (e.g., low-k dielectric material) and conductive material (e.g., copper) with vias interconnecting the layers of conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, or the like).” Yu ’798, [12:61-13:2].</p> <p>“In some embodiments, the through vias 208 extend through the substrate 202 and couple at least one bond pad 204 to at least one bond pad 206.” Yu ’798, [13:2-13:6].</p> <p>To the extent Plaintiff contends that Yu ’798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Yu ’798 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>“In some embodiments, the bond pads 124 include a thin seed layer (not shown) made of copper, titanium, nickel, gold, tin, the like, or a combination thereof. The conductive material of the bond pads 124 may be deposited over the thin seed layer.” Yu ’798, [4:22-4:26].</p> <p>“In an embodiment, the contact areas 124 are underbump metallizations (UBMs) that include three layers of conductive materials, such as a layer of titanium, a layer of copper, and a layer of nickel. However, one of ordinary skill in the art will recognize that there are many suitable arrangements of materials and layers, such as an arrangement of chrome/chrome-copper alloy/copper/gold, an arrangement of titanium/titanium tungsten/copper, or an arrangement of copper/nickel/gold, that are suitable for the formation of the UBMs 124.” Yu ’798, [4:32-4:41].</p> <p>“In another embodiment, the conductive connectors 136 are metal pillars (such as a copper pillar) formed by a sputtering, printing, electro plating, electroless plating, CVD, or the like. The metal pillars may be solder free and have substantially vertical sidewalls. In some embodiments, a metal cap layer (not shown) is formed on the top of the metal pillar connectors 136. The metal cap layer may include nickel, tin, tin-lead, gold, silver, palladium, indium, nickel-palladium-gold, nickel-gold, the like, or a combination thereof and may be formed by a plating process.” Yu ’798, [6:9-6:21].</p> <p>“Although not shown, there may be UBMs coupled to the redistribution layer 131 with the conductive connectors 136 coupled to the UBMs (not shown). The UBMs may be formed by first forming a set of openings (not shown) may be formed through the topmost passivation layer 134 to expose surfaces of the metal lines 132 in the metal layer M N. The UBMs may extend through these openings in the passivation layer 134 and also extend along a surface of passivation layer 134. The UBMs may include three layers of conductive materials, such as a layer of titanium, a layer of copper, and a layer of nickel.” Yu ’798, [6:38-6:48].</p>
--	---

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>“In some embodiments, the bond pads 204 and 206 include a thin seed layer (not shown) made of copper, titanium, nickel, gold, palladium, the like, or a combination thereof. The conductive material of the bond pads 204 and 206 may be deposited over the thin seed layer.” Yu '798, [8:21-8:26].</p> <p>“In an embodiment, the bond pads 204 and 206 are UBMs that include three layers of conductive materials, such as a layer of titanium, a layer of copper, and a layer of nickel. However, one of ordinary skill in the art will recognize that there are many suitable arrangements of materials and layers, such as an arrangement of chrome/chrome-copper alloy/copper/gold, an arrangement of titanium/titanium tungsten/copper, or an arrangement of copper/nickel/gold, that are suitable for the formation of the UBMs 204 and 206.” Yu '798, [8:32-8:40].</p> <p>To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Yu '798 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, e.g.:</p>

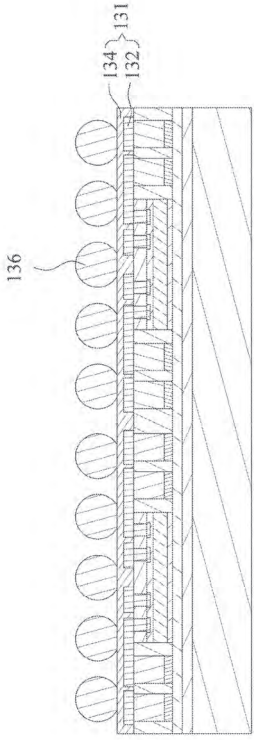
	 <p>FIG. 8</p> <p>Yu '798, FIG. 8.</p> <p>To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a</p>	<p>Yu '798 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

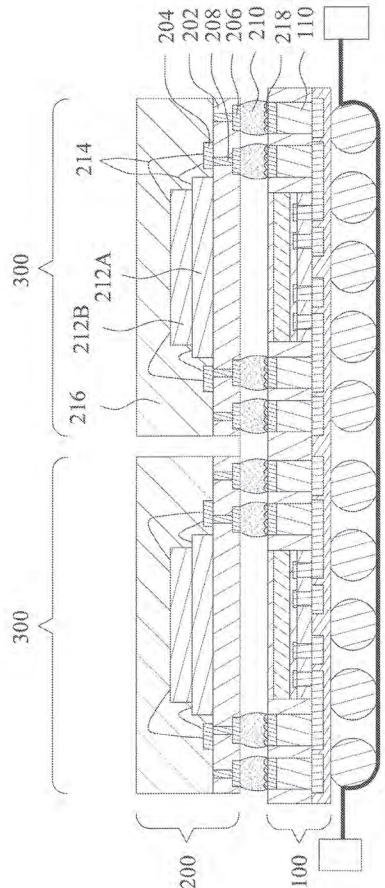
<p>corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p><i>See, e.g.:</i></p> <p>“After the second packages 200 are formed, the packages 200 are bonded to the first packages 100 by way of conductive connectors 210, the bond pads 206, and the TIVs 110. In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110. The conductive connectors 210 may be similar to the conductive connectors 136 described above and the description is not repeated herein, although the conductive connectors 210 and 136 need not be the same. In some embodiments, before bonding the conductive connectors 210, the conductive connectors 210 are coated with a flux (not shown), such as a no-clean flux. The conductive connectors 210 may be dipped in the flux or the flux may be jetted onto the conductive connectors 210. In another embodiment, the flux may be applied to the surfaces of the TIVs 110. The bonding between the second package 200 and the first package 100 may be a solder bonding or a direct metal-to-metal (such as a copper-to-copper or tin-to-tin) bonding. In an embodiment, the second package 200 is bonded to the first package 100 by a reflow process. During this reflow process, the conductive connectors 210 are in contact with the bond pads 206 and the TIVs 110 to physically and electrically couple the second package 200 to the first package 100. After the bonding process, an intermetallic compound (IMC) 218 may form at the interface of the TIVs 110 and the conductive connectors 210 and also at the interface between the conductive connectors 210 and the bond pads 206 (not shown).” Yu ’798, [9:4-9:32].</p> <p>To the extent Plaintiff contends that Yu ’798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
---	--

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Yu '798 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1G illustrates the formation of a set of conductive connectors 136 over and electrically coupled to the redistribution layer 131. The conductive connectors 136 may be solder balls, metal pillars, controlled collapse chip connection (C4) bumps, micro bumps, electroless nickel-electroless palladium-immersion gold technique (ENEPIG) formed bumps, or the like. The conductive connectors 136 may include a conductive material such as solder, copper, aluminum, gold, nickel, silver, palladium, tin, the like, or a combination thereof. In an embodiment in which the conductive connectors 136 are solder bumps, the conductive connectors 136 are formed by initially forming a layer of solder through such commonly used methods such as evaporation, electroplating, printing, solder transfer, ball placement, or the like. Once a layer of solder has been formed on the structure, a reflow may be performed in order to shape the material into the desired bump shapes. In another embodiment, the conductive connectors 136 are metal pillars (such as a copper pillar) formed by a sputtering, printing, electro plating, electroless plating, CVD, or the like.” Yu '798, [6:11-6:30].</p>
---	--

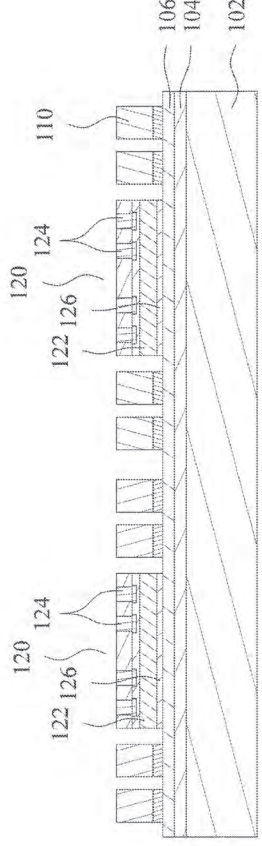
	 <p style="text-align: center;">FIG. 1G</p> <p>Yu '798, FIG. 1G.</p> <p>To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Yu '798 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<p>“The electrical connectors 110 may be formed over the seed layer 108 and extend from the seed layer 108 in a direction that is substantially perpendicular to a surface of the dielectric layer 106. In some embodiments, the electrical connectors 110 are formed through electrical plating. In these embodiments, the electrical connectors 110 are made of copper, aluminum, nickel, gold, silver, palladium, tin, the like, or a combination thereof, and may have a composite structure including a plurality of layers.” Yu ’798, [3:18-3:26].</p> <p>“The redistribution layer 131 may include one or more metal layers, sometimes referred to as M 1 and/or M N, wherein the metal layer M 1 is the metal layer immediately adjacent the dies 120, and metal layer M N (sometimes referred to as the top metal layer M N) is the metal layer furthest from the dies 120. Throughout the description, the term “metal layer” refers to the collection of metal lines 132 in the same layer. The redistribution layer 131 may include one or more passivation layers 134, wherein the one or more metal layers (M 1 through M N) are disposed in the one or more passivation layers 134.” Yu ’798, [5:18-5:28].</p> <p>“The substrate 202 may be referred to as a package substrate 202. The substrate 202 may include active and passive devices (not shown in FIG. 2A). As one of ordinary skill in the art will recognize, a wide variety of devices such as transistors, capacitors, resistors, combinations of these, and the like may be used to generate the structural and functional requirements of the design for the semiconductor package 300. The devices may be formed using any suitable methods. The substrate 202 may also include metallization layers (not shown) and through vias 208. The metallization layers may be formed over the active and passive devices and are designed to connect the various devices to form functional circuitry.” Yu ’798, [7:56-8:2].</p>
--	---

	<div></div> <div><p>FIG. 2A</p></div> <div><p>Yu '798, FIG. 2A.</p></div> <div><p>“The metallization layers may be formed of alternating layers of dielectric (e.g., low-k dielectric material) and conductive material (e.g., copper) with vias interconnecting the layers of conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, or the like). In some embodiments, the substrate 202 is substantially free of active and passive devices. The substrate 202 may have bond pads 204 on a first side the substrate 202 to couple to the stacked dies 212, and bond pads 206 on a second side of the substrate 202, the second side being opposite the first side of the substrate 202, to couple to the conductive connectors 210.” Yu '798, [8:2-8:14].</p></div>
--	---

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>“After the second packages 200 are formed, the packages 200 are bonded to the first packages 100 by way of conductive connectors 210, the bond pads 206, and the TIVs 110.” Yu ’798, [9:4-9:7].</p> <p>“In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110.” Yu ’798, [9:7-9:10].</p> <p>To the extent Plaintiff contends that Yu ’798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Yu ’798 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1D illustrates attaching dies 120 to the dielectric layer 106. First sides of the dies 120 may be attached to the dielectric layer 106 with an adhesive layer 126. The adhesive layer 126 may be any suitable adhesive, such as a die attach film or the like. The dies 120 may be a single die or may be more than two dies. The dies 120 may include a logic die, such as a central processing unit (CPU), a graphics processing unit (GPU), the like, or a combination thereof. In some embodiments, the dies 120 include a die stack (not shown) which may include both logic dies and memory dies. The dies 120 may include an input/output (I/O) die, such as a wide I/O die that provides a connection between the first package 10 and the</p>

	<p>subsequently attached second package 200 (see FIG. 2A). The dies 120 include contact areas 124 on a second side of the dies 120.” Yu ’798, [3:63-4:11].</p>  <p>FIG. 1D</p> <p>Yu ’798, FIG. 1D.</p> <p>“Referring to FIG. 2A, second packages 200 are bonded to the first package 100 with a set of conductive connectors 210 forming semiconductor packages 300. The second packages 200 each include a substrate 202 and one or more stacked dies 212 (212 A and 212 B) coupled to the substrate 202. The substrate 202 may be made of a semiconductor material such as silicon, germanium, diamond, or the like. Alternatively, compound materials such as silicon germanium, silicon carbide, gallium arsenic, indium arsenide, indium phosphide, silicon germanium carbide, gallium arsenic phosphide, gallium indium phosphide, combinations of these, and the like, may also be used. Additionally, the substrate 202 may</p>
--	--

	<p>be a silicon-on-insulator (SOI) substrate. Generally, an SOI substrate includes a layer of a semiconductor material such as epitaxial silicon, germanium, silicon germanium, SOI, silicon germanium on insulator (SGOI), or combinations thereof. The substrate 202 is, in one alternative embodiment, based on an insulating core such as a fiberglass reinforced resin core. One example core material is fiberglass resin such as FR4. Alternatives for the core material include bismaleimide-triazine (BT) resin, or alternatively, other printed circuit board (PCB) materials or films. Build up films such as Ajinomoto build-up film (ABF) or other laminates may be used for substrate 202. The substrate 202 may be referred to as a package substrate 202. The substrate 202 may include active and passive devices (not shown in FIG. 2A). As one of ordinary skill in the art will recognize, a wide variety of devices such as transistors, capacitors, resistors, combinations of these, and the like may be used to generate the structural and functional requirements of the design for the semiconductor package 300. The devices may be formed using any suitable methods. The substrate 202 may also include metallization layers (not shown) and through vias 208. The metallization layers may be formed over the active and passive devices and are designed to connect the various devices to form functional circuitry. The metallization layers may be formed of alternating layers of dielectric (e.g., low-k dielectric material) and conductive material (e.g., copper) with vias interconnecting the layers of conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, or the like). In some embodiments, the substrate 202 is substantially free of active and passive devices. The substrate 202 may have bond pads 204 on a first side the substrate 202 to couple to the stacked dies 212, and bond pads 206 on a second side of the substrate 202, the second side being opposite the first side of the substrate 202, to couple to the conductive connectors 210. In some embodiments, the bond pads 204 and 206 are formed by forming recesses (not shown) into dielectric layers (not shown) on the first and second sides of the substrate 202. The recesses may be formed to allow the bond pads 204 and 206 to be embedded into the dielectric layers. In other embodiments, the recesses are omitted as the bond pads 204 and 206 may be formed on the</p>
--	---

	<p>dielectric layer. In some embodiments, the bond pads 204 and 206 include a thin seed layer (not shown) made of copper, titanium, nickel, gold, palladium, the like, or a combination thereof. The conductive material of the bond pads 204 and 206 may be deposited over the thin seed layer. The conductive material may be formed by an electro-chemical plating process, an electroless plating process, CVD, ALD, PVD, the like, or a combination thereof. In an embodiment, the conductive material of the bond pads 204 and 206 is copper, tungsten, aluminum, silver, gold, the like, or a combination thereof. In an embodiment, the bond pads 204 and 206 are UBMs that include three layers of conductive materials, such as a layer of titanium, a layer of copper, and a layer of nickel. However, one of ordinary skill in the art will recognize that there are many suitable arrangements of materials and layers, such as an arrangement of chrome/chrome-copper alloy/copper/gold, an arrangement of titanium/titanium tungsten/copper, or an arrangement of copper/nickel/gold, that are suitable for the formation of the UBMs 204 and 206. Any suitable materials or layers of material that may be used for the UBMs 204 and 206 are fully intended to be included within the scope of the current application. In some embodiments, the through vias 208 extend through the substrate 202 and couple at least one bond pad 204 to at least one bond pad 206. In the illustrated embodiment, the stacked dies 212 are coupled to the substrate 202 by wire bonds 214, although other connections may be used, such as conductive bumps. In an embodiment, the stacked dies 212 are stacked memory dies. For example, the stacked memory dies 212 may include low-power (LP) double data rate (DDR) memory modules, such as LPDDR1, LPDDR2, LPDDR3, or the like memory modules. In some embodiments, the stacked dies 212 and the wire bonds 214 may be encapsulated by a molding material 216. The molding material 216 may be molded on the stacked dies 212 and the wire bonds 214, for example, using compression molding. In some embodiments, the molding material 216 is a molding compound, a polymer, an epoxy, silicon oxide filler material, the like, or a combination thereof. A curing step may be performed to cure the molding material 216, wherein the curing may be a thermal curing, a UV curing, the like, or a combination thereof. In some</p>
--	--

embodiments, the stacked dies 212 and the wire bonds 214 are buried in the molding material 216, and after the curing of the molding material 216, a planarization step, such as a grinding, is performed to remove excess portions of the molding material 216 and provide a substantially planar surface for the second packages 200. After the second packages 200 are formed, the packages 200 are bonded to the first packages 100 by way of conductive connectors 210, the bond pads 206, and the TIVs 110. In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110.” Yu ’798, [7:32-9:9].

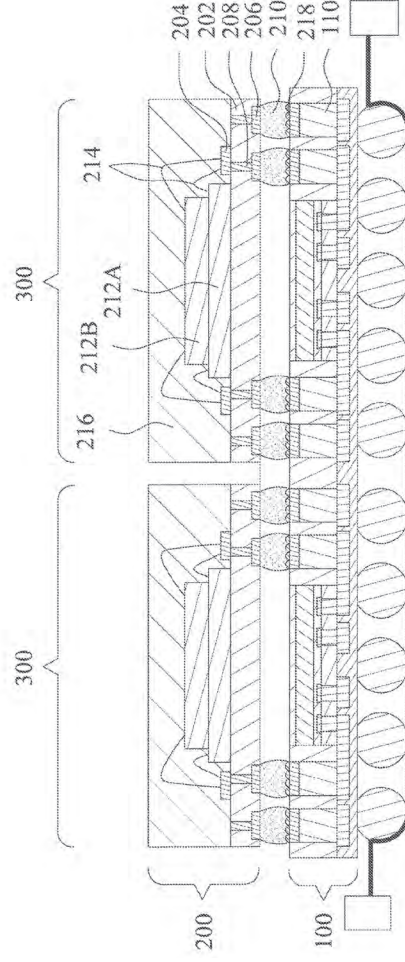


FIG. 2A

	<p>Yu '798, FIG. 2A.</p> <p>“FIG. 2B illustrates forming an underfill 220 between the first package 100 and the second package 200 and between the conductive connectors 210. The underfill 220 may be formed of a liquid epoxy, a deformable gel, a silicon rubber, a non-conductive film, a polymer, PBO, polyimide, solder resist, or a combination thereof. The underfill 220 provides structural support for the conductive connectors 210, and may be dispensed using capillary force after the conductive connectors 210 are bonded between the first package 100 and the second package 200. In these embodiments, the underfill 220 includes a fillet where a sidewalls 220 A that are diagonal to backside surfaces 120 B of the dies 120. In some embodiments, the underfill 220 is formed to leave openings 222 over the dies 120.” Yu '798, [9:34-9:47].</p> <p>“FIG. 3A, this embodiment has the underfill 220 including fillets. The first package 100 has a width W 100, the second package has a width W 200, and the underfill 220 has an outer width W 220 between the first and second packages 100 and 200. The opening 222 in the underfill 220 has a width W 222 and the die 120 has a width W 120. In an embodiment, the width W 220 is less than or equal to the width W 100, the width W 200 is less than or equal to the width W 220, and the width W 222 is less than or equal to the width W 120. In another embodiment, the width W 220 is less than the width W 100, the width W 200 is less than the width W 220, and the width W 222 is less than the width W 120. The underfill 220 has a height H 220 between the first and second packages 100 and 200 (sometimes referred to as a standoff height). In an embodiment, the height H 220 is from about 1 μm to about 200 μm. FIG. 3B illustrates another embodiment of the semiconductor package 300.” Yu '798, [9:61-10:11].</p>
--	--

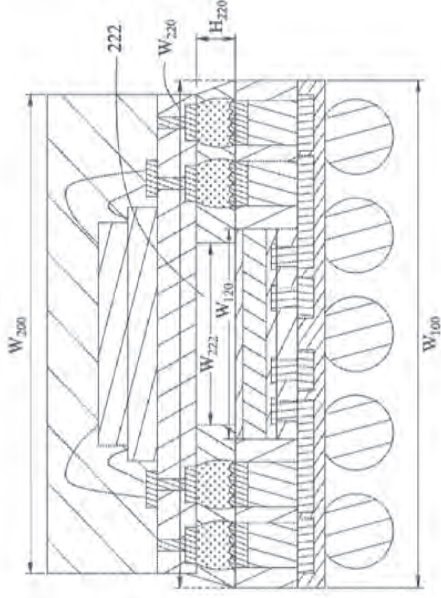


FIG. 3A

Yu '798, FIG. 3A.

“FIG. 8 illustrates a cross-sectional view of a semiconductor package 400 in accordance with some embodiments. The semiconductor package 400 includes the semiconductor package 300 being mounted to a package substrate 402. The semiconductor package 300 may be any of the embodiments of the semiconductor package 300 described above. The semiconductor package 300 is mounted to the package substrate 402 using the conductive connectors 136.”
Yu '798, [12:27-12:34].

“A further embodiment is a package including a first package, a second package bonded to the first package, and a first underfill between the first package and the first substrate. The first package includes a first die having an active surface and a backside surface opposite the

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>active surface, a molding material surrounding the first die, and a redistribution layer coupled to the first die. The backside surface of the first die has a first width. A first surface of the molding material is level with the active surface of the first die. A second surface of the molding material is level with the backside surface of the first die. The active surface of the first die is closer to the redistribution layer than the backside surface of the first die. The second package includes a second die attached to a first substrate. A sidewall of the first underfill is coplanar with a sidewall of the molding material. The first underfill has a first opening exposing a portion of a first surface of the first substrate. The first surface of the first substrate faces the backside surface of the first die. The first opening has a second width less than the first width.” Yu ’798, [15:6-15:24].</p> <p>To the extent Plaintiff contends that Yu ’798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Yu ’798 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1D illustrates attaching dies 120 to the dielectric layer 106. First sides of the dies 120 may be attached to the dielectric layer 106 with an adhesive layer 126. The adhesive layer 126 may be any suitable adhesive, such as a die attach film or the like.” Yu ’798, [3:64-3:68].</p>

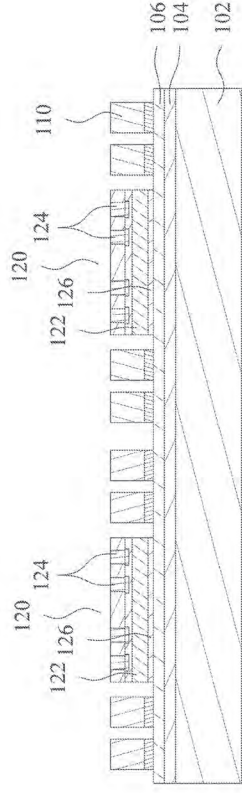
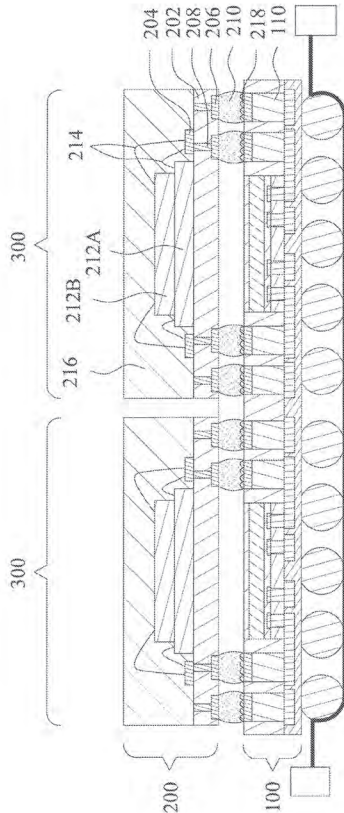


FIG. 1D

Yu '798, FIG. 1D.

“FIG. 2A, second packages 200 are bonded to the first package 100 with a set of conductive connectors 210 forming semiconductor packages 300. The second packages 200 each include a substrate 202 and one or more stacked dies 212 (212 A and 212 B) coupled to the substrate 202.” Yu '798, [7:32-7:38].

	<div></div> <div><p>FIG. 2A</p></div> <div><p>Yu '798, FIG. 2A.</p></div> <div><p>“In the illustrated embodiment, the stacked dies 212 are coupled to the substrate 202 by wire bonds 214, although other connections may be used, such as conductive bumps.” Yu '798, [8:47-8:49].</p></div> <div><p>“In some embodiments, the stacked dies 212 and the wire bonds 214 may be encapsulated by a molding material 216. The molding material 216 may be molded on the stacked dies 212 and the wire bonds 214, for example, using compression molding.” Yu '798, [8:55-8:59].</p></div> <div><p>“After the second packages 200 are formed, the packages 200 are bonded to the first packages 100 by way of conductive connectors 210, the bond pads 206, and the TIVs 110. In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire</p></div>
--	---

bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110.” Yu '798, [9:4-9:10].

“FIG. 8 illustrates a cross-sectional view of a semiconductor package 400 in accordance with some embodiments. The semiconductor package 400 includes the semiconductor package 300 being mounted to a package substrate 402. The semiconductor package 300 may be any of the embodiments of the semiconductor package 300 described above. The semiconductor package 300 is mounted to the package substrate 402 using the conductive connectors 136.” Yu '798, [12:27-12:34].

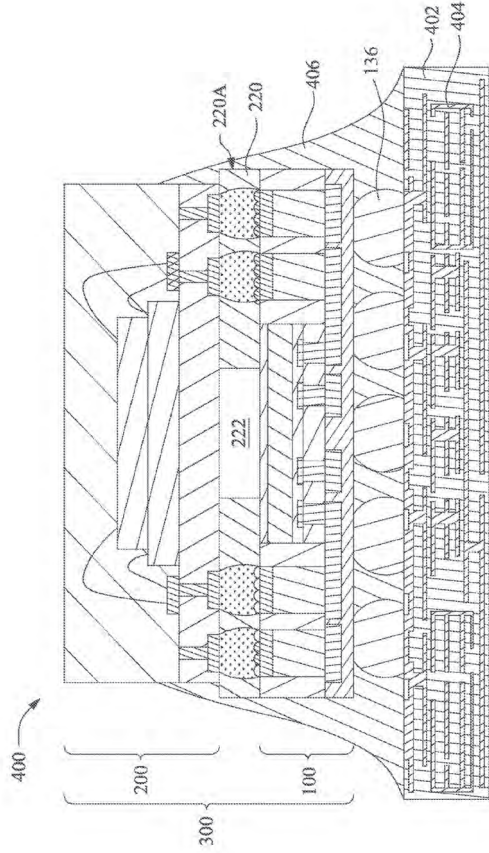
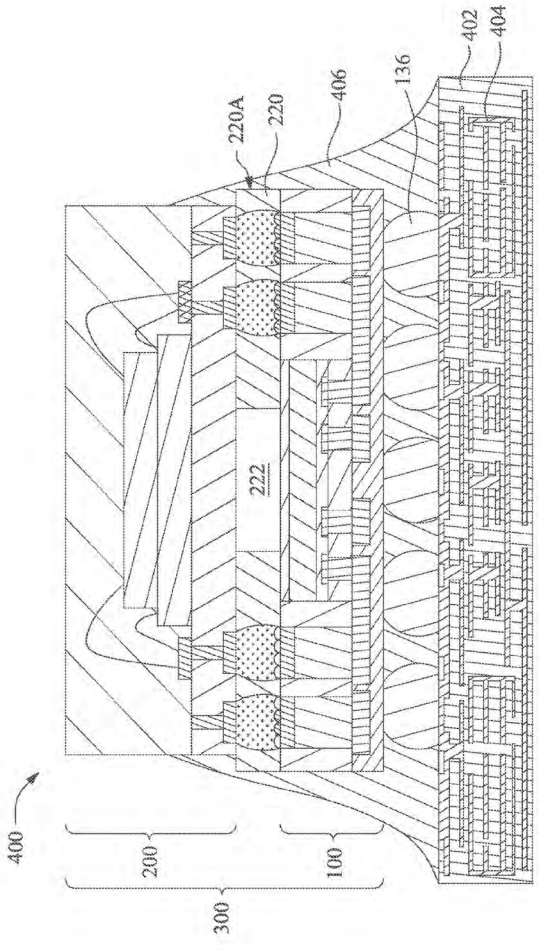


FIG. 8

Yu '798, FIG. 8.

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Yu '798 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>  <p>FIG. 8</p> <p>Yu '798, FIG. 8.</p>

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Yu '798 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In some embodiments, the underfill 220 is formed to leave openings 222 over the dies 120.” Yu '798, [9:45-9:47].</p> <p>“The underfill 220 has a height H 220 between the first and second packages 100 and 200 (sometimes referred to as a standoff height). In an embodiment, the height H 220 is from about 1 μm to about 200 μm.” Yu '798, [10:6-10:9].</p> <p>“FIG. 3B illustrates another embodiment of the semiconductor package 300. This embodiment is similar to the previous embodiment of FIG. 3A except that that there is no opening (see 222 in FIG. 3A) in the underfill 220.” Yu '798, [10:10-10:13].</p>

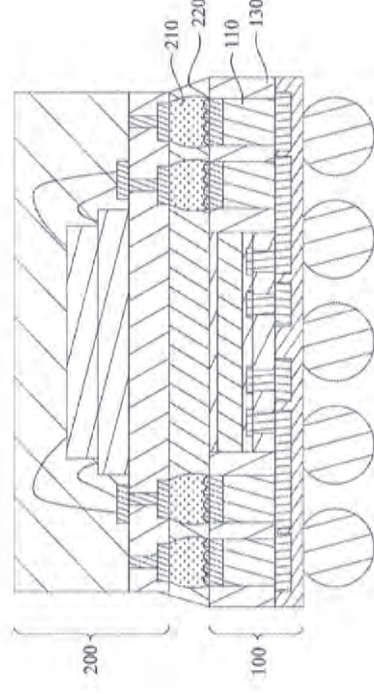


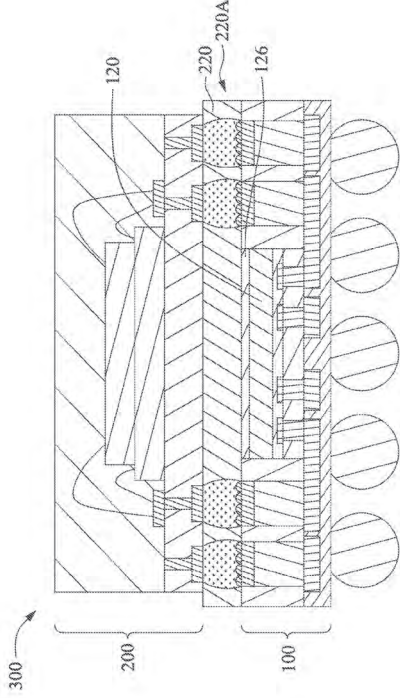
FIG. 3B

Yu '798, FIG. 3B.

“In some embodiments, the underfill 220 is patterned to form openings 222 over the dies 120 (and adhesive layer 126 if present).” Yu ’798, [11:3-11:5].

“Referring to FIG. 5A, the underfill 220 has the opening 222 over the die 120.” Yu ’798, [11:43-11:44].

	<div> </div> <div> <p>FIG. 5A</p> </div> <div> <p>Yu '798, FIG. 5A.</p> </div> <div> <p>“FIG. 5B illustrates the underfill 220 having no opening over the die 120.” Yu '798, [11:44-11:45].</p> </div>
--	--

	<div></div> <div><p>FIG. 5B</p></div> <div><p>Yu '798, FIG. 5B.</p></div> <div><p>To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Yu '798 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“FIG. 1G illustrates the formation of a set of conductive connectors 136 over and electrically coupled to the redistribution layer 131. The conductive connectors 136 may be solder balls, metal pillars, controlled collapse chip connection (C4) bumps, micro bumps, electroless nickel-electroless palladium-immersion gold technique (ENEPIG) formed bumps, or the like. The conductive connectors 136 may include a conductive material such as solder, copper, aluminum, gold, nickel, silver, palladium, tin, the like, or a combination thereof.” Yu '798, [6:11-6:20].</p>
---	---

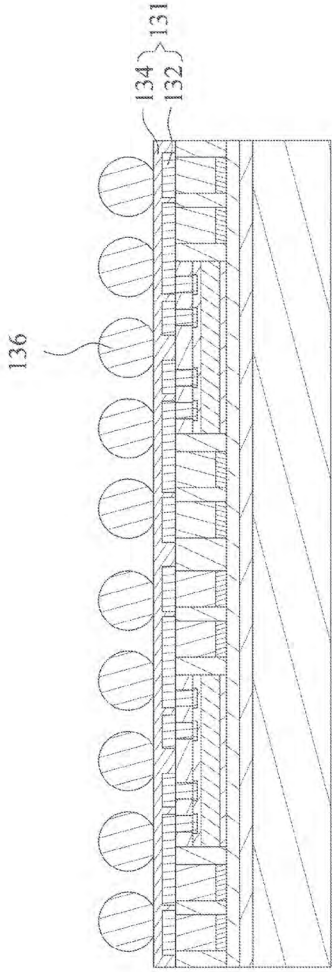


FIG. 1G

Yu '798, FIG. 1G.

“Referring to FIG. 2A, second packages 200 are bonded to the first package 100 with a set of conductive connectors 210 forming semiconductor packages 300. The second packages 200 each include a substrate 202 and one or more stacked dies 212 (212 A and 212 B) coupled to the substrate 202.” Yu '798, [7:32-7:38].

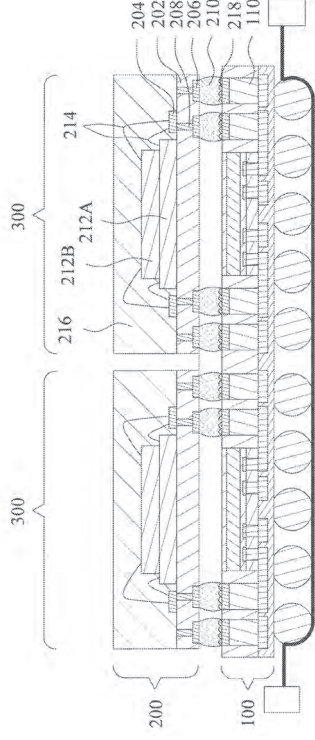


FIG. 2A

Yu '798, FIG. 2A.

“In the illustrated embodiment, the stacked dies 212 are coupled to the substrate 202 by wire bonds 214, although other connections may be used, such as conductive bumps. In an embodiment, the stacked dies 212 are stacked memory dies. For example, the stacked memory dies 212 may include low-power (LP) double data rate (DDR) memory modules, such as LPDDR1, LPDDR2, LPDDR3, or the like memory modules. In some embodiments, the stacked dies 212 and the wire bonds 214 may be encapsulated by a molding material 216. The molding material 216 may be molded on the stacked dies 212 and the wire bonds 214, for example, using compression molding. In some embodiments, the molding material 216 is a molding compound, a polymer, an epoxy, silicon oxide filler material, the like, or a combination thereof. A curing step may be performed to cure the molding material 216, wherein the curing may be a thermal curing, a UV curing, the like, or a combination thereof. In some embodiments, the stacked dies 212 and the wire bonds 214 are buried in the molding

	<p>material 216, and after the curing of the molding material 216, a planarization step, such as a grinding, is performed to remove excess portions of the molding material 216 and provide a substantially planar surface for the second packages 200. After the second packages 200 are formed, the packages 200 are bonded to the first packages 100 by way of conductive connectors 210, the bond pads 206, and the TIVs 110. In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110.” Yu ’798, [8:47-9:10].</p> <p>“FIG. 2B illustrates forming an underfill 220 between the first package 100 and the second package 200 and between the conductive connectors 210. The underfill 220 may be formed of a liquid epoxy, a deformable gel, a silicon rubber, a non-conductive film, a polymer, PBO, polyimide, solder resist, or a combination thereof. The underfill 220 provides structural support for the conductive connectors 210, and may be dispensed using capillary force after the conductive connectors 210 are bonded between the first package 100 and the second package 200. In these embodiments, the underfill 220 includes a fillet where a sidewalls 220 A that are diagonal to backside surfaces 120 B of the dies 120. In some embodiments, the underfill 220 is formed to leave openings 222 over the dies 120.” Yu ’798, [9:34-9:47].</p>
--	---

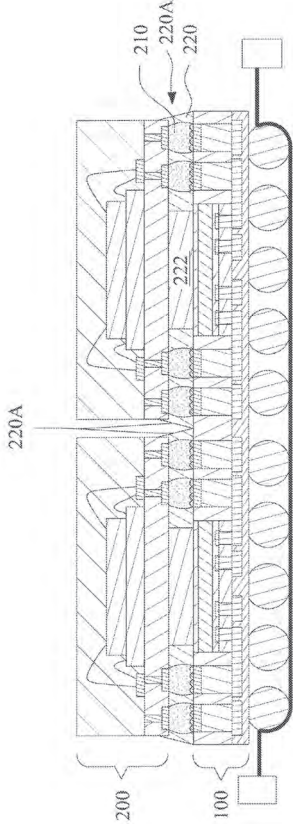


FIG. 2B

Yu '798, FIG. 2B.

“Referring the FIG. 3A, this embodiment has the underfill 220 including fillets. The first package 100 has a width W_{100} , the second package has a width W_{200} , and the underfill 220 has an outer width W_{220} between the first and second packages 100 and 200. The opening 222 in the underfill 220 has a width W_{222} and the die 120 has a width W_{120} . In an embodiment, the width W_{220} is less than or equal to the width W_{100} , the width W_{200} is less than or equal to the width W_{220} , and the width W_{222} is less than or equal to the width W_{120} . In another embodiment, the width W_{220} is less than the width W_{100} , the width W_{200} is less than the width W_{220} , and the width W_{222} is less than the width W_{120} .” Yu '798, [9:61-10:5].

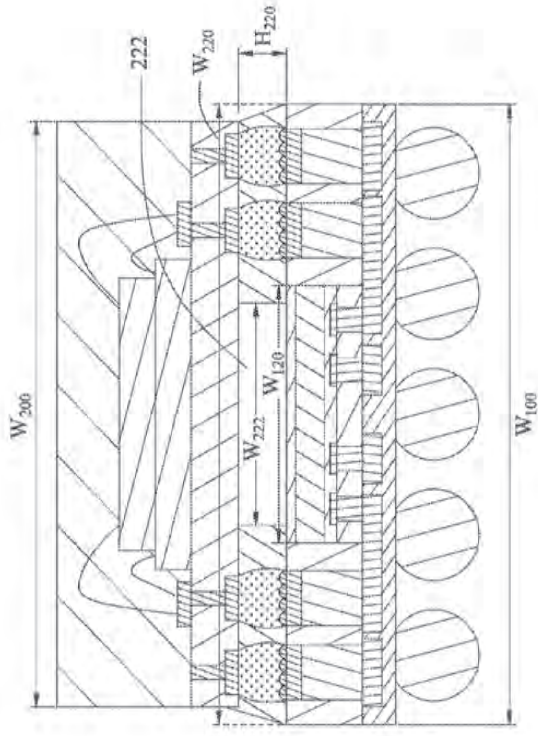
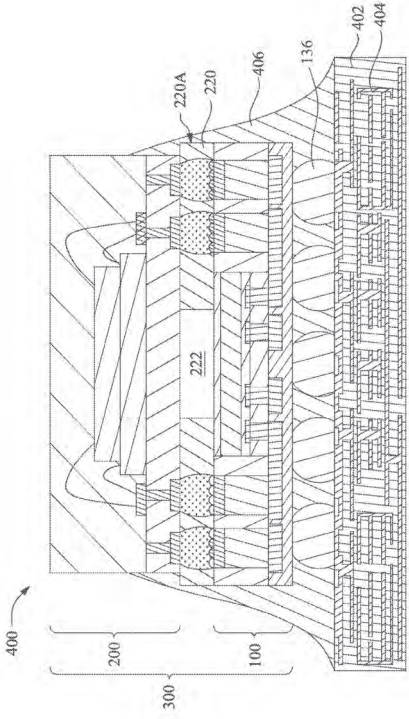


FIG. 3A

Yu '798, FIG. 3A.

“FIG. 8 illustrates a cross-sectional view of a semiconductor package 400 in accordance with some embodiments. The semiconductor package 400 includes the semiconductor package 300 being mounted to a package substrate 402. The semiconductor package 300 may be any of the embodiments of the semiconductor package 300 described above. The semiconductor package 300 is mounted to the package substrate 402 using the conductive connectors 136.”
Yu '798, [12:27-12:34].

	 <p style="text-align: center;">FIG. 8</p> <p>Yu '798, FIG. 8.</p> <p>To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of metal pillars of the top package substrate is aligned with a corresponding metal	Yu '798 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

<p>bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The substrate 202 may have bond pads 204 on a first side the substrate 202 to couple to the stacked dies 212, and bond pads 206 on a second side of the substrate 202, the second side being opposite the first side of the substrate 202, to couple to the conductive connectors 210.” Yu ’798, [8:10-8:14].</p> <p>“In some embodiments, the through vias 208 extend through the substrate 202 and couple at least one bond pad 204 to at least one bond pad 206.” Yu ’798, [8:43-8:46].</p> <p>“After the second packages 200 are formed, the packages 200 are bonded to the first packages 100 by way of conductive connectors 210, the bond pads 206, and the TIVs 110. In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110.” Yu ’798, [9:4-9:10].</p> <p>“In some embodiments, the stacked memory dies 212 may be coupled to the dies 120 through the wire bonds 214, the bond pads 204 and 206, through vias 208, the conductive connectors 210, and the TIVs 110.” Yu ’798, [9:7-9:10].</p> <p>“In another embodiment, the flux may be applied to the surfaces of the TIVs 110. The bonding between the second package 200 and the first package 100 may be a solder bonding or a direct metal-to-metal (such as a copper-to-copper or tin-to-tin) bonding. In an embodiment, the second package 200 is bonded to the first package 100 by a reflow process.</p>
---	--

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>During this reflow process, the conductive connectors 210 are in contact with the bond pads 206 and the TIVs 110 to physically and electrically couple the second package 200 to the first package 100.” Yu ’798, [9:19-9:29].</p> <p>“The metallization layers may be formed of alternating layers of dielectric (e.g., low-k dielectric material) and conductive material (e.g., copper) with vias interconnecting the layers of conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, or the like).” Yu ’798, [12:64-13:2].</p> <p>To the extent Plaintiff contends that Yu ’798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Yu ’798 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

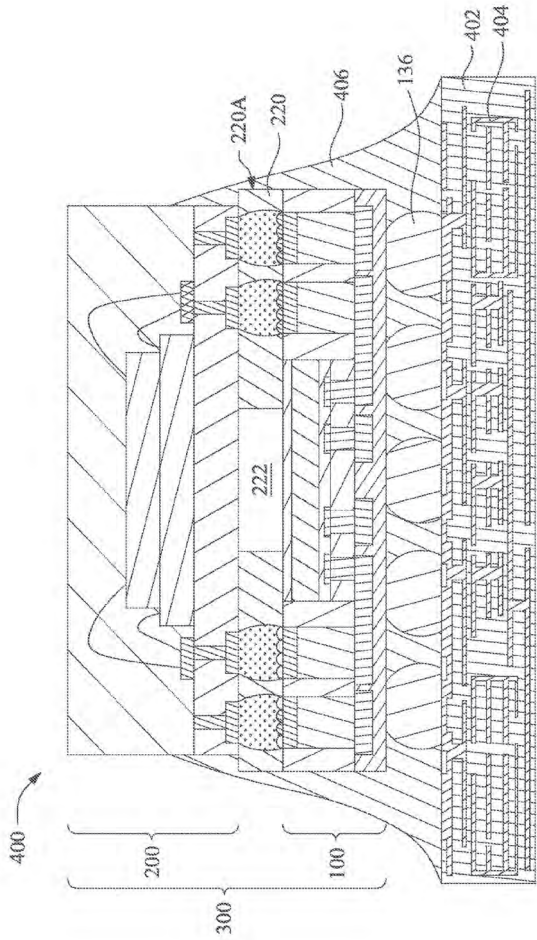


FIG. 8

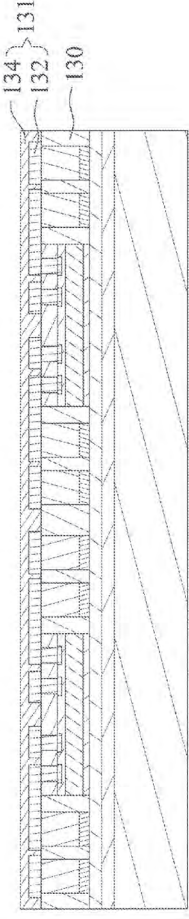
Yu '798, FIG. 8.

To the extent Plaintiff contends that Yu '798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Claim 9, U.S. Patent No. 9859202

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the top package substrate via the plurality of bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Yu '798 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The conductive connectors 136 may be solder balls, metal pillars, controlled collapse chip connection (C4) bumps, micro bumps, electroless nickel-electroless palladium-immersion gold technique (ENEPIG) formed bumps, or the like. The conductive connectors 136 may include a conductive material such as solder, copper, aluminum, gold, nickel, silver, palladium, tin, the like, or a combination thereof. In an embodiment in which the conductive connectors 136 are solder bumps, the conductive connectors 136 are formed by initially forming a layer of solder through such commonly used methods such as evaporation, electroplating, printing, solder transfer, ball placement, or the like. Once a layer of solder has been formed on the structure, a reflow may be performed in order to shape the material into the desired bump shapes. In another embodiment, the conductive connectors 136 are metal pillars (such as a copper pillar) formed by a sputtering, printing, electro plating, electroless plating, CVD, or the like. The metal pillars may be solder free and have substantially vertical sidewalls. In some embodiments, a metal cap layer (not shown) is formed on the top of the metal pillar connectors 136.” Yu '798, [6:13-6:34].</p>

	<p>“Although not shown, there may be UBMs coupled to the redistribution layer 131 with the conductive connectors 136 coupled to the UBMs (not shown). The UBMs may be formed by first forming a set of openings (not shown) may be formed through the topmost passivation layer 134 to expose surfaces of the metal lines 132 in the metal layer M N. The UBMs may extend through these openings in the passivation layer 134 and also extend along a surface of passivation layer 134. The UBMs may include three layers of conductive materials, such as a layer of titanium, a layer of copper, and a layer of nickel.” Yu ’798, [6:38-6:48].</p>  <p>FIG. 1F</p> <p>Yu ’798, FIG. 1F.</p> <p>“In some embodiments, the bond pads 204 and 206 are formed by forming recesses (not shown) into dielectric layers (not shown) on the first and second sides of the substrate 202. The recesses may be formed to allow the bond pads 204 and 206 to be embedded into the dielectric layers. In other embodiments, the recesses are omitted as the bond pads 204 and 206 may be formed on the dielectric layer. In some embodiments, the bond pads 204 and 206</p>
--	---

Appendix A-37 - Invalidity of U.S. Patent No. 9859202 in view of Yu '798 - U.S. Patent No. 11107798

	<p>include a thin seed layer (not shown) made of copper, titanium, nickel, gold, palladium, the like, or a combination thereof. The conductive material of the bond pads 204 and 206 may be deposited over the thin seed layer.” Yu ’798, [8:14-8:26].</p> <p>“In some embodiments, the through vias 208 extend through the substrate 202 and couple at least one bond pad 204 to at least one bond pad 206.” Yu ’798, [8:43-8:46].</p> <p>“The conductive connectors 210 may be similar to the conductive connectors 136 described above and the description is not repeated herein, although the conductive connectors 210 and 136 need not be the same. In some embodiments, before bonding the conductive connectors 210, the conductive connectors 210 are coated with a flux (not shown), such as a no-clean flux. The conductive connectors 210 may be dipped in the flux or the flux may be jetted onto the conductive connectors 210. In another embodiment, the flux may be applied to the surfaces of the TIVs 110. The bonding between the second package 200 and the first package 100 may be a solder bonding or a direct metal-to-metal (such as a copper-to-copper or tin-to-tin) bonding.” Yu ’798, [9:11-9:23].</p> <p>“After the bonding process, an intermetallic compound (IMC) 218 may form at the interface of the TIVs 110 and the conductive connectors 210 and also at the interface between the conductive connectors 210 and the bond pads 206 (not shown).” Yu ’798, [9:29-9:33].</p> <p>To the extent Plaintiff contends that Yu ’798 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

**Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication**

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications - Non-Patent Publication

Polymer Adhesives and Encapsulants for Microelectronic Applications was published by Richard C. Benson, Dawnielle Farrar, and Joseph A. Miragliotta. Polymer Adhesives and Encapsulants for Microelectronic Applications anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ‘202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Polymer Adhesives and Encapsulants for Microelectronic Applications is an academic article that was published January 1, 2008. Polymer Adhesives and Encapsulants for Microelectronic Applications is therefore prior art to the ‘202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Polymer Adhesives and Encapsulants for Microelectronic Applications, or otherwise rendered obvious by disclosures and teachings of Polymer Adhesives and Encapsulants for Microelectronic Applications, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Polymer Adhesives and Encapsulants for Microelectronic Applications does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Polymer Adhesives and Encapsulants for Microelectronic Applications with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Polymer Adhesives and Encapsulants for Microelectronic Applications, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Polymer Adhesives and Encapsulants for Microelectronic Applications “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Polymer Adhesives and Encapsulants for Microelectronic Applications or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Polymer Adhesives and Encapsulants for Microelectronic Applications set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>"In flip-chip devices, polymers are being used for electrical interconnects instead of metallurgical joints. Polymer encapsulants are widely used to package microelectronic and optoelectronic devices when hermetic-" Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p>
[1.A] a bottom package substrate;	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>"Polymer adhesives can be dispensed from tubes, screen- printed, or placed on substrates in a tape format (generally that is pressure-sensitive)." Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>"When thermal or electrical conductivity is not required, insulating polymer adhesives are used for bonding surface-mounted components to printed circuit boards, semiconductor die to substrates, substrates to packages, and lids to packages (where hermeticity is not required)." Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>"Polymers filled with thermally conducting particles are used as thermal interface materials (TIMs) in applications where moderate, but not maximum, heat transport is required." Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>"LSI VCSEL array PD array Interposer Microlens array -Solder bumps LSI PD array Polymer waveguide VCSEL array protocols have been developed to assess the effects of stress factors on the electrical performance of the device and evaluate the reliability. 27 These</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>tests include burn-in or high-" Polymer Adhesives and Encapsulants for Microelectronic Applications, [68].</p> <p>"For encapsulated devices, test protocols were developed by the Joint Electron Device Engineering Council (JEDEC) and employ severe conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it." Polymer Adhesives and Encapsulants for Microelectronic Applications, [68].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>"In flip-chip devices, polymers are being used for electrical interconnects instead of metallurgical joints. Polymer encapsulants are widely used to package microelectronic and optoelectronic devices when hermetic-" Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>“Polymer adhesives can be dispensed from tubes, screen- printed, or placed on substrates in a tape format (generally that is pressure-sensitive). Thermoset materials (e.g., epoxies, polyimides, and cyanate esters) require exposure to elevated temperatures to cure or induce cross-linking chemical reactions between the monomers.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“Polymers filled with thermally conducting particles are used as thermal interface materials (TIMs) in applications where moderate, but not maximum, heat transport is required. Thermal conduction and the role of phonon transport at solid/solid interfaces are not well under-” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“When thermal or electrical conductivity is not required, insulating polymer adhesives are used for bonding surface-mounted components to printed circuit boards, semiconductor die to substrates, substrates to packages, and lids to packages (where hermeticity is” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Various approaches have been investigated to improve the thermal conductivity of polymeric TIMs. Recent investigations have been made by using electro- spun fibers that were embedded with different thermally conductive particles, but the resultant TIMs did not have a significantly higher thermal conductivity than” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“LSI VCSEL array PD array Interposer Microlens array -Solder bumps LSI PD array Polymer waveguide VCSEL array protocols have been developed to assess the effects of stress factors on the electrical performance of the device and evaluate the reliability. 27 These</p>
--	---

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>tests include burn-in or high-" Polymer Adhesives and Encapsulants for Microelectronic Applications, [68].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>"Miragliotta his article provides an overview of the use of polymer adhesives in microelectronic packaging, with key applications including die attachment," Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p> <p>"In flip-chip devices, polymers are being used for electrical interconnects instead of metallurgical joints." Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>“Polymer adhesives can be dispensed from tubes, screen- printed, or placed on substrates in a tape format (generally that is pressure-sensitive).” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“Underfill materials are primarily used to improve the reliability of the flip-chip solder interconnects. These materials fill the gap between the chip and substrate and surround the solder joints, thereby reducing any thermal stress that may be induced on the solder joint as, for example, a result of thermal cycling.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [63].</p> <p>“A flip- chip device is defined as a die/chip mounted on a substrate by using various interconnection materials such as solder bumps, wire/stud bump interconnects, and ICAs/ACAs.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [63].</p> <p>“The gap height typically ranges from 30 μm to 200 μm, and the underfill material flows via capillary forces (i.e., it is wicked) through the gap and around the solder bumps.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [63].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p><i>See, e.g.:</i></p> <p>“Another emerging application area is the use of polymer adhesives in optoelectronic devices. Over the past decade, the introduction of miniaturized optical components and interconnects within microelectronic devices has led to the development of new processes for polymer-based packaging (see Fig. 11). Although most development efforts have focused on the fabrication of polymer-based optical components, packaging issues associated with interconnect alignment and encapsulation also are critical to device performance. 35 For the latter, conventional electronics packaging technologies (e.g., automatic pick-and-place and transfer molding) are being used in the mass production of optoelectronic devices that include optical transceivers.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [68].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>“Polymers filled with thermally conducting particles are used as thermal interface materials (TIMs) in applications where moderate, but not maximum, heat transport is required. Thermal conduction and the role of phonon transport at solid/solid interfaces are not well understood for TIMs. Comprehensive measurements, along with modeling, recently have been made on electrically insulating TIMs to determine the effect of the bulk thermal conductivity of filler particles, bondline thickness, and the various interfaces (substrate/polymer matrix, polymer matrix/particle, and particle/particle) on the overall thermal conductivity of the TIM.² As the bulk” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“When thermal or electrical conductivity is not required, insulating polymer adhesives are used for bonding surface-mounted components to printed circuit boards, semiconductor die to substrates, substrates to packages, and lids to packages (where hermeticity is not required). The materials used are typically unfilled epoxies, although other polymers are used occasionally. A major application involves the use of adhesives as underfills for flip-chip devices to provide some stress relief of the solder joints during temperature cycling (see Underfill Materials for Flip-Chip Devices below). Another application of polymer adhesives, in particular benzocyclobutenes (BCB) and polyimides, is to serve as the dielectric layer/adhesive for redistributing the metal interconnection geometry on die (this application is not discussed in this article).” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Various factors affect the overall conductivity of filled adhesives: polymer chemistry, the volume fraction of filler, and the filler properties (material type, coatings, particle morphology, and size distribution). The actual formulation chemistry of commercial adhesives is proprietary, and various additives are present at low concentrations to improve</p>
--	--

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>the performance of the adhesive. The electrical conductivity of the cured adhesive is generally described by percolation theory, with tunneling processes possibly occurring during the early stages of the cure. The particle fraction at which conductance first occurs is the percolation threshold, and it depends on the morphology and size of the metallic fillers.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [61].</p> <p>“In addition to traditional semiconductor devices, chip-level packaging of MEMS occasionally involves the use of encapsulants to minimize the impact of environmental factors on the micrometer-scaled movable elements. In most applications, polymer encapsulation of MEMS devices protects movable fragile parts during wafer handling, wafer dicing, or plastic molding. Encapsulation provides a more robust device for transportation and handling without altering the performance of the devices. Several MEMS packaging techniques have been reported involving wafer-to-wafer bonding and thin-film sacrificial-based sealing methods. 33,34 As shown in Fig. 10, Insulator (a) Unity- (b) Polymer overcoat (c) (d) Metal Figure 10. MEMS packaging sequence that produces an encapsulated and released micrometer-scaled movable device. (Reproduced with permission from Ref. 34 © 2006, Institute of Physics.)” Polymer Adhesives and Encapsulants for Microelectronic Applications, [67-68].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Filler materials include metal particles (typically silver), ferromagnetic metal particles (silver-coated nickel), and metal-coated polymeric spheres.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“ACAs have a lower filler content than ICAs to minimize any conduction in the XY direction. A limitation of conductive adhesives is that they are not self-aligning (as is the case with solder), so accurate alignment of components is required. Filler materials include metal particles (typically silver), ferromagnetic metal particles (silver-coated nickel), and metal-coated polymeric spheres. The ferromagnetic particles are aligned in the z direction by applying an (a) (b) (c) Pad Anisotropic conductive film Substrate Conductive particle Chip Bump Pad Substrate Pressure and heat Chip Bump Pad Substrate Figure 1. Schematic illustrating the die attachment process using” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Various approaches have been investigated to improve the thermal conductivity of polymeric TIMs. Recent investigations have been made by using electrospun fibers that were embedded with different thermally conductive particles, but the resultant TIMs did not have a significantly higher thermal conductivity than conventional materials. 4 A new approach that appears promising involves low-temperature sintering adhesives in which a variety of</p>
--	---

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>low-melting-point and high-melt-” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“See Fig. 3 for a schematic of the packing of large and small particles, and see Fig. 4 for scanning electron micrographs of the surface morphology. Jeong et al. 10 investigated an epoxy formulation that contained a mixture of 5-nm and 3-μm silver particles, with a total silver content of 92 mass %. They found that the optimum content of nanoparticles was 2 mass %.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [61].</p> <p>“As an alternative to using ACAs for z-axis interconnections, gold ball bonds are made on the substrate or die pads, truncated, and then coined (flattened), 17 as shown in Fig. 5. The advantages of this ball-bumping process are that no expensive masks or chemical processing equipment are required, the assembly is straightforward, and, in contrast to using ACAs, the interconnects can carry higher current. The yields and reliability are high because the ball-bonding process is the same as the initial step in producing wire bonds. These gold BUMPED AND COINED WAFER HTUSE Figure 5. Image of gold ball bonds that are coined to form stud” Polymer Adhesives and Encapsulants for Microelectronic Applications, [62].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Electrically conductive adhesives typically have metallic fillers in the polymer matrix and generally are in two categories: isotropic and anisotropic. Isotropic conductive adhesives (ICAs) exhibit electrical conduction in all directions, whereas anisotropic conductive” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Another application of polymer adhesives, in particular benzocyclobutenes (BCB) and polyimides, is to serve as the dielectric layer/adhesive for redistributing the metal interconnection geometry on die (this application is not discussed in this article).” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“ACA films are widely used in flat-panel-display applications. The ultimate pitch (spacing) of the interconnect array using ACAs is limited by the size of the metal particle filler. In most cases, the polymer matrix is electrically insulating, but recent investigations have been performed on polymers that are intrinsically conductive, such as polythiophenes and polyanilines.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [61].</p> <p>“As an alternative to using ACAs for z-axis interconnections, gold ball bonds are made on the substrate or die pads, truncated, and then coined (flattened), 17 as shown in Fig. 5. The advantages of this ball-bumping process are that no expensive masks or chemical processing equipment are required, the assembly is straightforward, and, in contrast to using ACAs, the</p>
--	--

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>interconnects can carry higher current. The yields and reliability are high because the ball-bonding process is the same as the initial step in producing wire bonds. These gold BUMPED AND COINED WAFER HTUSE Figure 5. Image of gold ball bonds that are coined to form stud” Polymer Adhesives and Encapsulants for Microelectronic Applications, [62].</p> <p>“JOHNS HOPKINS APL TECHNICAL DIGEST, VOLUME 28, NUMBER 1 (2008) stud bumps then are used with an insulating adhesive to bond the die and substrate under heat and pressure. The interconnect density (or pitch) is limited to that in which wire-bonding equipment can effectively bond gold wire to the metal pads.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [62-63].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>“Die attachment Wire bonding Plastic ball and grid array Wafer sorting Optical Wafer mounting Wafer sawing Die attachment Wire bonding” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“Polymer adhesives can be dispensed from tubes, screen-printed, or placed on substrates in a tape format (generally that is pressure-sensitive). Thermoset materials (e.g., epoxies, polyimides, and cyanate esters) require exposure to elevated temperatures to cure or induce cross-linking chemical reactions between the monomers.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“Electrically conductive adhesives typically have metallic fillers in the polymer matrix and generally are in two categories: isotropic and anisotropic. Isotropic conductive adhesives (ICAs) exhibit electrical conduction in all directions, whereas anisotropic conductive adhesives (ACAs) conduct in only one direction (generally referred to as the z axis); see Fig. 1 for a schematic of the cross-sectional bond.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“As an alternative to using ACAs for z-axis interconnections, gold ball bonds are made on the substrate or die pads, truncated, and then coined (flattened), 17 as shown in Fig. 5. The advantages of this ball-bumping process are that no expensive masks or chemical processing equipment are required, the assembly is straightforward, and, in contrast to using ACAs, the interconnects can carry higher current.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [62].</p>
--	---

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>“Pad Anisotropic conductive film Substrate Conductive particle Chip Bump Pad Substrate Pressure and heat Chip Bump Pad Substrate” Polymer Adhesives and Encapsulants for Microelectronic Applications, [64].</p> <p>“LSI VCSEL array PD array Interposer Microlens array -Solder bumps LSI PD array Polymer waveguide VCSEL array” Polymer Adhesives and Encapsulants for Microelectronic Applications, [68].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Polymer adhesives can be dispensed from tubes, screen-printed, or placed on substrates in a tape format (generally that is pressure-sensitive). Thermoset materials (e.g., epoxies, polyimides, and cyanate esters) require exposure to elevated temperatures to cure or induce cross-linking chemical reactions between the monomers.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>“When thermal or electrical conductivity is not required, insulating polymer adhesives are used for bonding surface-mounted components to printed circuit boards, semiconductor die to substrates, substrates to packages, and lids to packages (where hermeticity is not required).” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Various approaches have been investigated to improve the thermal conductivity of polymeric TIMs. Recent investigations have been made by using electrospun fibers that were embedded with different thermally conductive particles, but the resultant TIMs did not have a significantly higher thermal conductivity than conventional materials.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Pad Anisotropic conductive film Substrate Conductive particle Chip Bump Pad Substrate Pressure and heat Chip Bump Pad Substrate Figure 1. Schematic illustrating the die attachment process using an ACA. (a) ACA applied to substrate. (b) Chip placement onto substrate. (c) Cross-section of ACA bond after cure.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“These gold BUMPED AND COINED WAFER HTUSE Figure 5. Image of gold ball bonds that are coined to form stud bumps, which are an alternative to using ACAs for z-axis interconnections. (Reproduced with permission from Ref. 17 © 1997, IEEE.) 62” Polymer Adhesives and Encapsulants for Microelectronic Applications, [62].</p> <p>“LSI VCSEL array PD array Interposer Microlens array -Solder bumps LSI PD array Polymer waveguide VCSEL array” Polymer Adhesives and Encapsulants for Microelectronic Applications, [68].</p>
--	---

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“In flip-chip devices, polymers are being used for electrical interconnects instead of metallurgical joints. Polymer encapsulants are widely used to package microelectronic and optoelectronic devices when hermetic-” Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In flip-chip devices, polymers are being used for electrical interconnects instead of metallurgical joints. Polymer encapsulants are widely used to package microelectronic and optoelectronic devices when hermeticity is not required.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p> <p>“Polymer adhesives can be dispensed from tubes, screen-printed, or placed on substrates in a tape format (generally that is pressure-sensitive).” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“When used in hermetic packages, the materials are subjected to a bakeout (typically done in an inert environment such as flowing dry nitrogen or sometimes under vacuum) to outgas volatile components, and then the packages are sealed in dry nitrogen.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“Various approaches have been investigated to improve the thermal conductivity of polymeric TIMs. Recent investigations have been made by using electro-spun fibers that were embedded with different thermally conductive particles, but the resultant TIMs did not have a significantly higher thermal conductivity than conventional materials.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p>
--	--

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>“When thermal or electrical conductivity is not required, insulating polymer adhesives are used for bonding surface-mounted components to printed circuit boards, semiconductor die to substrates, substrates to packages, and lids to packages (where hermeticity is not required).” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Underfill materials are primarily used to improve the reliability of the flip-chip solder interconnects. These materials fill the gap between the chip and substrate and surround the solder joints, thereby reducing any ther”- Polymer Adhesives and Encapsulants for Microelectronic Applications, [63].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Polymer adhesives can be dispensed from tubes, screen- printed, or placed on substrates in a tape format (generally that is pressure-sensitive). Thermoset materials (e.g., epoxies, polyimides, and cyanate esters) require exposure to elevated temperatures to cure or induce cross-linking chemical reactions between the monomers.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>“To ensure a good interface between the adhesive and die or substrates, cleaning of the components often is required before assembly, and, in most cases, some chemical additives are present in the polymer formulation to improve the interface adhesion.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“During the attachment procedure, the temperature is raised above T_g; therefore, rather high T_s are required in order for the adhesive joint to survive high-temperature exposure during subsequent processing.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“When thermal or electrical conductivity is not required, insulating polymer adhesives are used for bonding surface-mounted components to printed circuit boards, semiconductor die to substrates, substrates to packages, and lids to packages (where hermeticity is not required).” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Various approaches have been investigated to improve the thermal conductivity of polymeric TIMs. Recent investigations have been made by using electro-spun fibers that were embedded with different thermally conductive particles, but the resultant TIMs did not have a significantly higher thermal conductivity than conventional materials.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p> <p>“Polymers filled with thermally conducting particles are used as thermal interface materials (TIMs) in applications where moderate, but not maximum, heat transport is required.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [60].</p>
--	---

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“In flip-chip devices, polymers are being used for electrical interconnects instead of metallurgical joints. Polymer encapsulants are widely used to package microelectronic and optoelectronic devices when hermetic-” Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>

Claim 2, U.S. Patent No. 9859202

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Underfill materials are primarily used to improve the reliability of the flip-chip solder interconnects. These materials fill the gap between the chip and substrate and surround the solder joints, thereby reducing any ther-” Polymer Adhesives and Encapsulants for Microelectronic Applications, [63].</p> <p>“The gap height typically ranges from 30 μm to 200 μm, and the underfill material flows via capillary forces (i.e., it is wicked) through the gap and around the solder bumps.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [63].</p> <p>“A flip- chip device is defined as a die/chip mounted on a substrate by using various interconnection materials such as solder bumps, wire/stud bump interconnects, and ICAs/ACAs. Underfill materials are primarily used to improve the reliability of the flip-chip solder interconnects. These materials fill the gap between the chip and substrate and” Polymer Adhesives and Encapsulants for Microelectronic Applications, [63].</p> <p>“To overcome these limitations, no-flow underfill materials have been developed that have been regarded as a next-generation flip-chip technology because of its advantages. These advantages include the ability to assemble chips having fine-pitch, high-density arrays onto</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>substrates with a narrow gap between the chip and substrate; the assembly steps are” Polymer Adhesives and Encapsulants for Microelectronic Applications, [64].</p> <p>“Conformal coatings encapsulate circuit boards and their electronic components in order to minimize the permeation of moisture and prevent the ingress of fungus, particles (dust), and other environmental contaminants.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [67].</p> <p>“Optical-input/output chip packaging concept. 35 LSI, Large-scale integration (chip); PD, photodiode; VCSEL, vertical cavity surface-emitting laser. (Reproduced with permission from Ref. 35 © 2001, IEEE.) a sacrificial polymer placeholder is first patterned on top of the MEMS component of interest, followed by over- coating with a low-dielectric-constant polymer overcoat. The sacrificial polymer decomposes at elevated temperatures, and the volatile products from the sacrificial material permeate through the overcoat polymer, leaving an embedded air cavity around the MEMS structure.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [68].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Polymer adhesives can be dispensed from tubes, screen- printed, or placed on substrates in a tape format (generally that is pressure-sensitive). Thermoset materials (e.g., epoxies, polyimides, and cyanate esters) require exposure to elevated temperatures to cure or induce cross-linking chemical reactions between the monomers. Depending on the adhesive chemistry, varying time periods are required to cure the polymeric system; cure schedules for epoxy formulations range from “snap cures” that require only a few minutes at 150–175°C to the more standard cure schedule of 0.5-2 h at 150-175°C; higher temperatures (e.g., 275°C) are required to cure polyimides. When used in hermetic packages, the materials are subjected to a bakeout (typically done in an inert environment such as flowing dry nitrogen or sometimes under vacuum) to outgas volatile components, and then the packages” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“Table 1. General assembly steps for various package types associated with semiconductor die devices. Plastic lead frame Wafer sorting Optical General steps Inspection Wafer preparation Wafer mounting Wafer sawing Interconnection Die attachment Wire bonding Plastic ball and grid array Wafer sorting Optical Wafer mounting Wafer sawing Die attachment Wire bonding Package type Hermetic Wafer sorting Optical Wafer mounting</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>Wafer sawing Die attachment Wire bonding Flip chip Wafer sorting Optical Wafer mounting Wafer sawing Polymer adhesive die attachment Alignment Inspection Packaging Optical Encapsulate (mold compound) Optical Encapsulate (mold compound or glob top) Optical Lid seal Ball attach and reflow Leakage test Acoustic Encapsulate with glob top Wafer bumping Reflow Underfill Acoustic or wafer-bond lid” Polymer Adhesives and Encapsulants for Microelectronic Applications, [59].</p> <p>“A flip- chip device is defined as a die/chip mounted on a substrate by using various interconnection materials such as solder bumps, wire/stud bump interconnects, and ICAs/ACAs. Underfill materials are primarily used to improve the reliability of the flip-chip solder interconnects. These materials fill the gap between the chip and substrate and surround the solder joints, thereby reducing any thermal stress that may be induced on the solder joint as, for example, a result of thermal cycling.” Polymer Adhesives and Encapsulants for Microelectronic Applications, [63].</p> <p>“LSI VCSEL array PD array Interposer Microlens array -Solder bumps LSI PD array Polymer waveguide VCSEL array protocols have been developed to assess the effects of stress factors on the electrical performance of the” Polymer Adhesives and Encapsulants for Microelectronic Applications, [67-68].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“In flip-chip devices, polymers are being used for electrical interconnects instead of metallurgical joints. Polymer encapsulants are widely used to package microelectronic and optoelectronic devices when hermetic-” Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In flip-chip devices, polymers are being used for electrical interconnects instead of metallurgical joints. Polymer encapsulants are widely used to package microelectronic and optoelectronic devices when hermetic-” Polymer Adhesives and Encapsulants for Microelectronic Applications, [58].</p> <p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>

Claim 9, U.S. Patent No. 9859202

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Polymer Adhesives and Encapsulants for Microelectronic Applications discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p>See, e.g.:</p> <p>“In addition to the anisotropic adhesive approach for achieving only z-axis interconnections, gold stud bumps are used with an electrically insulating adhesive (which will be discussed later).” Polymer Adhesives and Encapsulants for Microelectronic Applications, [61].</p> <p>“As an alternative to using ACAs for z-axis interconnections, gold ball bonds are made on the substrate or die pads, truncated, and then coined (flattened), 17 as shown in Fig. 5. The advantages of this ball-bumping process are that no expensive masks or chemical processing equipment are required, the assembly is straightforward, and, in contrast to using ACAs, the interconnects can carry higher current. The yields and reliability are high because the ball-bonding process is the same as the initial step in producing wire bonds. These gold BUMPED AND COINED WAFER HTUSE Figure 5. Image of gold ball bonds that are coined to form stud bumps, which are an alternative to using ACAs for z-axis interconnections. (Reproduced</p>

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>with permission from Ref. 17 © 1997, IEEE.) 62 JOHNS HOPKINS APL TECHNICAL DIGEST, VOLUME 28, NUMBER 1 (2008) stud bumps then are used with an insulating adhesive” Polymer Adhesives and Encapsulants for Microelectronic Applications, [62-63].</p> <p>“As shown in Fig. 10, Insulator (a) Unity- (b) Polymer overcoat (c) (d) Metal Figure 10. MEMS packaging sequence that produces an encapsulated and released micrometer-scaled movable device. (Reproduced with permission from Ref. 34 © 2006, Institute of Physics.)” Polymer Adhesives and Encapsulants for Microelectronic Applications, [67-68].</p> <p>“LSI VCSEL array PD array Interposer Microlens array -Solder bumps LSI PD array Polymer waveguide VCSEL array protocols have been developed to assess the effects of stress factors on the electrical performance of the device and evaluate the reliability. 27 These tests include burn-in or high- temperature soak (typically 500 h at 125°C), thermal cycling (typically -65°C to +125°C), 85/85 testing (85°C/85% relative humidity), and the highly accelerated stress test (HAST) (typically 145°C/85% relative humidity at a pressure of two atmospheres). In many cases, these tests are conducted with the devices under bias (applied voltage). It should be noted that predicted lifetimes based on accelerated tests should be used with caution because there is the possibility that new failure mechanisms may occur with harsher test conditions. In addition to materials properties and process parameters, there are a variety of environmental factors that may affect the performance and reliability of a packaged device. These include moisture, heat, thermal cycling, chemical contaminants, and mechanical stress. Typical reliability issues are listed below. 25,37,38 Figure 11. Optical-input/output chip packaging concept. 35 LSI, Large-scale integration (chip); PD, photodiode; VCSEL, vertical cavity surface-emitting laser. (Reproduced with permission from Ref. 35 © 2001, IEEE.)” Polymer Adhesives and Encapsulants for Microelectronic Applications, [68].</p>
--	--

Appendix A-38 - Invalidity of U.S. Patent No. 9859202 in view of Polymer Adhesives and Encapsulants for Microelectronic Applications
- Non-Patent Publication

	<p>To the extent Plaintiff contends that Polymer Adhesives and Encapsulants for Microelectronic Applications fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration and was published by Rabindra N. Das, et al. in the 25th International Symposium on Microelectronics. Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration is an academic article that was published September 13, 2012. Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, or otherwise rendered obvious by disclosures and teachings of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration does not disclose any claim

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions asserted herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

elements of the Asserted Claims, it would have been obvious to combine the teachings of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration set forth in this chart.

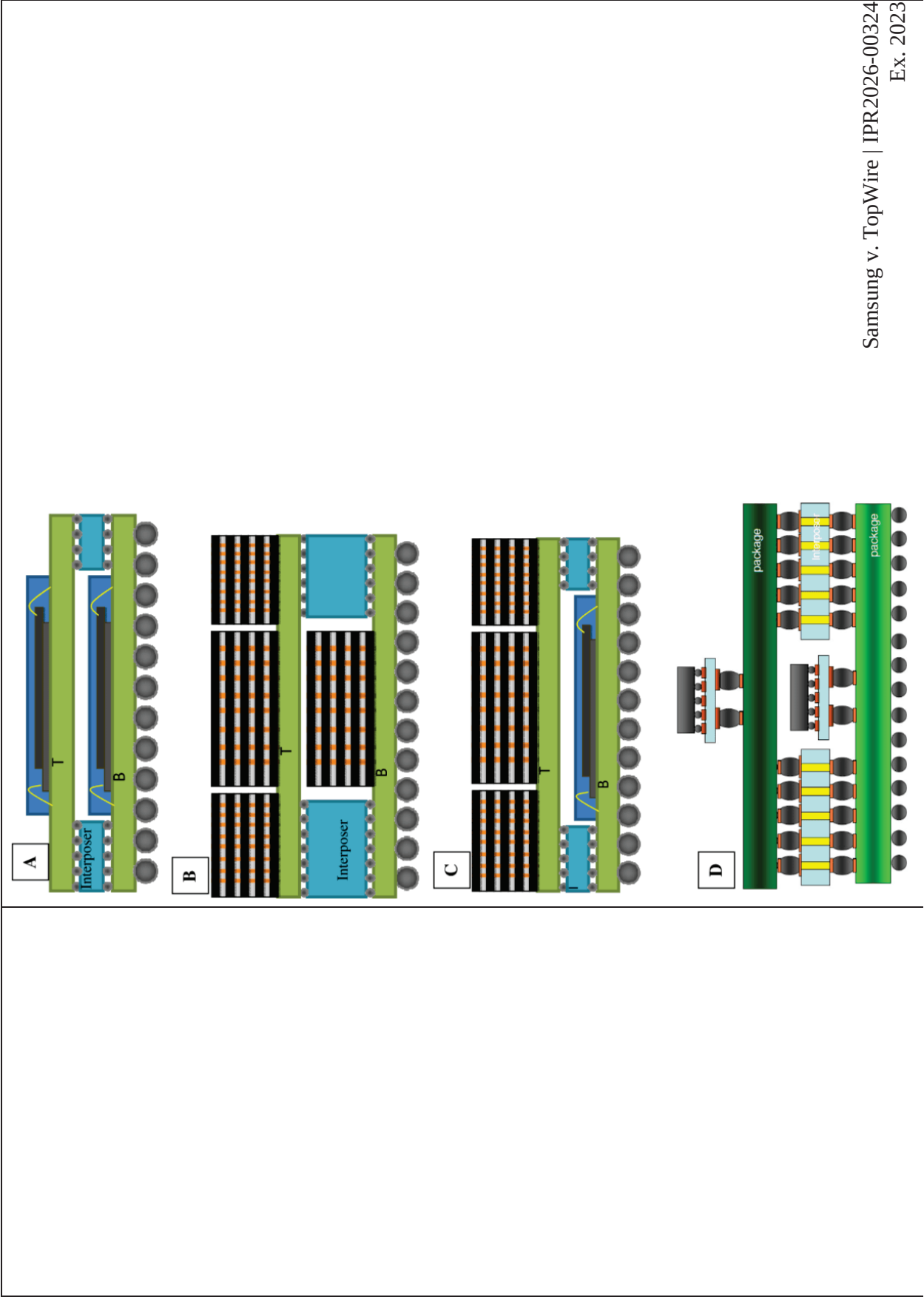
Claim 1, U.S. Patent No. 9,859,202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, a structure.

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p><i>See, e.g.:</i></p> <p>“Figure 2: Package-Interposer-Package (PIP) construction with a single interposer. (A) Top and bottom packages have wire bonded stacked die, (B) Top and bottom packages have TSV processed stacked die, (C) Top package has TSV processed stacked die, and the bottom package has wired bonded stacked die, (D) 3D-PIP construction with a single interposer.”</p> <p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [2].</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication



Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

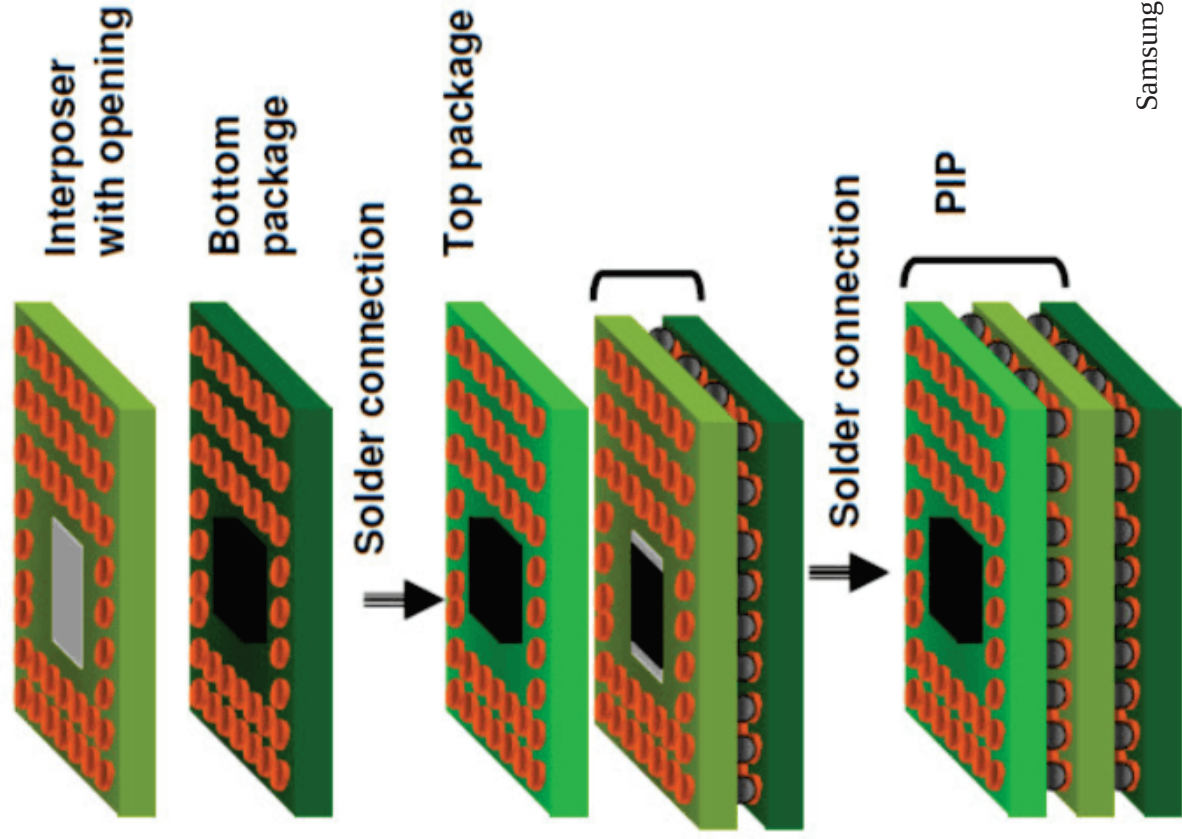
	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 2.</p> <p>“A PIP was constructed using an interposer consisting of multiple metal inner planes. A top view of the contacting pads for this interposer is shown schematically in Figure 5.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“As part of an on-going effort to develop new electrical interconnection between the interposer and the package on either side of the interposer, connections can be made by a Figure 5. Top view of interposer A PIP was constructed using an interposer consisting of multiple metal inner planes. A top view of the contacting” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“Figure 6. Process flow for a PIP construction. The interposer has an opening. The top side of the bottom package is connected with the bottom side of the interposer in such a way that die on the bottom package resides within the opening of the interposer. The bottom side of the top package is connected with the top side of the interposer in a subsequent step to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“As stated above, ECA-filled interposers can also be used to produce a PIP structure. High temperature/pressure lamination is used to cure the adhesive in the PIP and provide electrical interconnection among the packages. A variety of interposer structures such as OS/1P, OS/2P, 2S/1P, 2S/2P can be used. Figure 8 shows optical photographs and SEM micrographs of a joining core having ECA-filled holes with diameters ranging from 55 μm to 65 μm, as a</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>typical representative example of an interposer that can be used for PIP. The ECA protrudes above the surface of the dielectric by about 5-10 μm, (Figure 8B).” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Figure 7. magnification (top), and higher magnification (bottom). 000564 A” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4-5].</p>
[1.A] a bottom package substrate;	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Traditional Package on Package (POP) approaches use direct solder connections between the substrates and are limited to use of single (or minimum) die on the bottom substrate, to reduce warpage and improve stability.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“Figure 6. Process flow for a PIP construction. The interposer has an opening. The top side of the bottom package is connected with the bottom side of the interposer in such a way that</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>die on the bottom package resides within the opening of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Figure 12 shows highly populated double side assembled substrate having stacked packaged die attached to the substrate.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>“PIP can accommodate modules with stacked die on organic, ceramic, or silicon board substrates, where in some cases defective substrates can be detached and replaced without affecting the rest of the package.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [6].</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p>
--	--



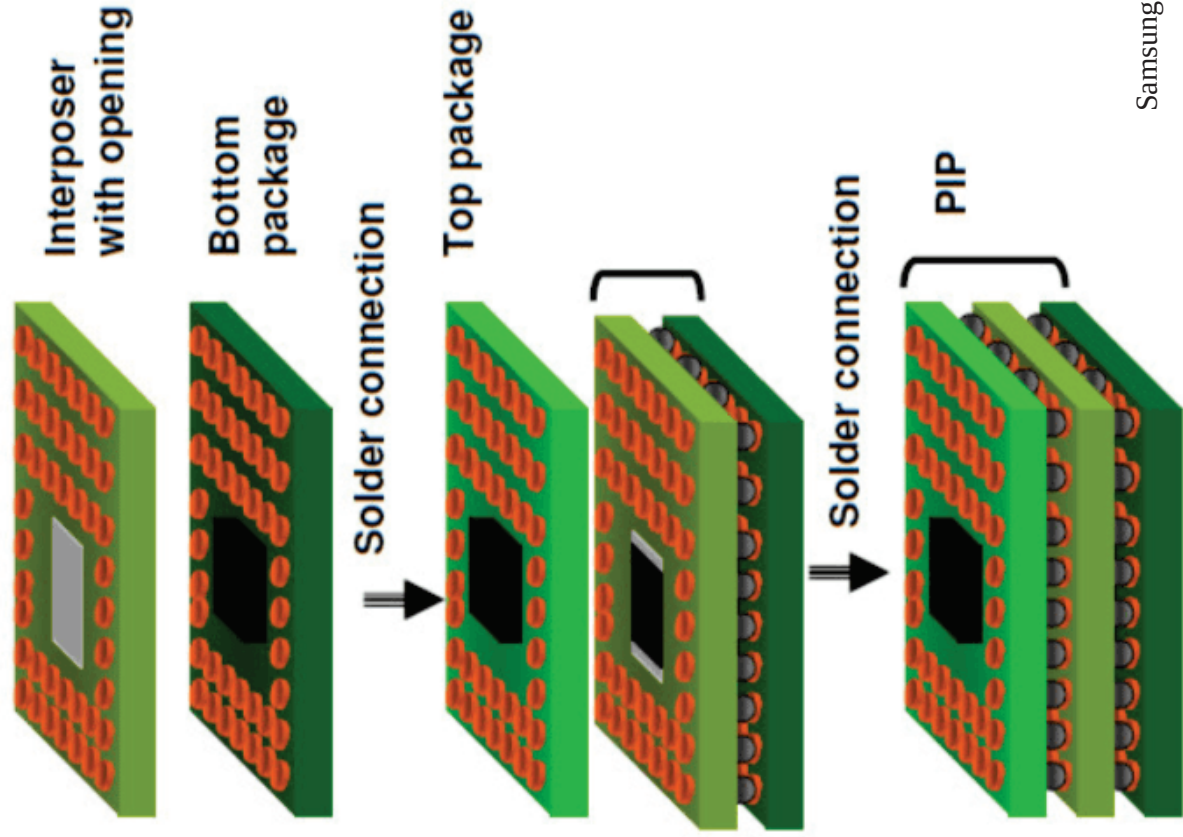
Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 6.</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“Figure 2: Package-Interposer-Package (PIP) construction with a single interposer. (A) Top and bottom packages have wire bonded stacked die, (B) Top and bottom packages have TSV processed stacked die, (C) Top package has TSV processed stacked die, and the bottom package has wired bonded stacked” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [2].</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication



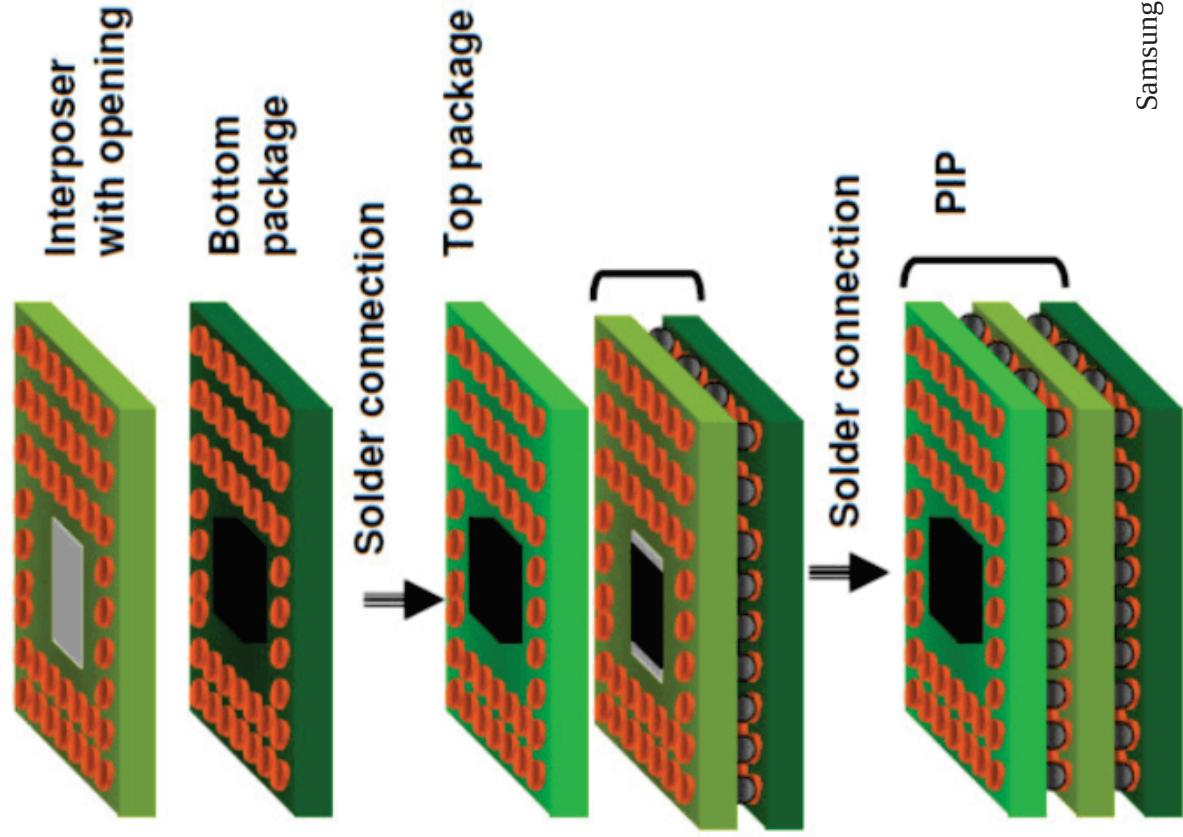
Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 6.</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Figure 10 shows PIP structures for connecting 4 packages with three interposers. An optical photo of a cross section of the PIP structure built with 4 packages with three interposers is shown in Figure 11.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>“Traditional PoP approaches use direct solder connections between the substrates and are limited to use of single (or minimum) die on the bottom substrate, in order to reduce warpage and improve stability.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [6].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.C] at least one spacer connector interposed between the bottom package	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, at least one spacer connector interposed between</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

<p>substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In the PIP structure, multiple packages will be attached with an interposer instead of direct soldering between packages, and maintain finer ball pitch for thicker stacked or wire bond die component assemblies. The interposer will not only reduce the package to package ball pitch but also improves package stability and reliability.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“For PIP, use of an interposer between the two packages provides for the use of low volume interconnect metallurgy between the interposer and the packages, enabling finer pitch connections from package to package.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [2].</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p>
--	---

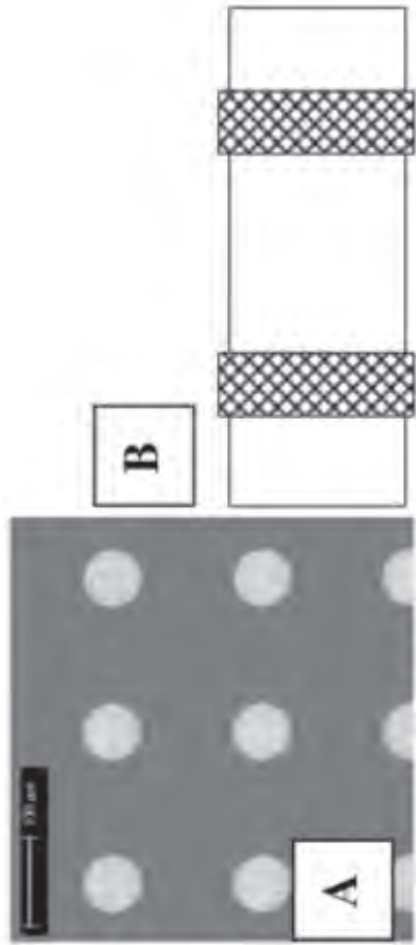
Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication



Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 6.</p> <p>“PIP can accommodate a larger range in attached component thickness because of the flexibility in selection of interposer thickness.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [6].</p> <p>“Smaller pitch is attainable owing to the need for smaller solder volumes (most of the space between packages is occupied by the interposer), or a landless joining core technology, where the pitch is limited solely by the size of the via one can fill with ECA.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [6].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Figure 4. Various means can be employed for interposer- package joining. Illustrated here is (A) an optical photo, top view, of an interposer formed using an ECA-filled joining core,</p>

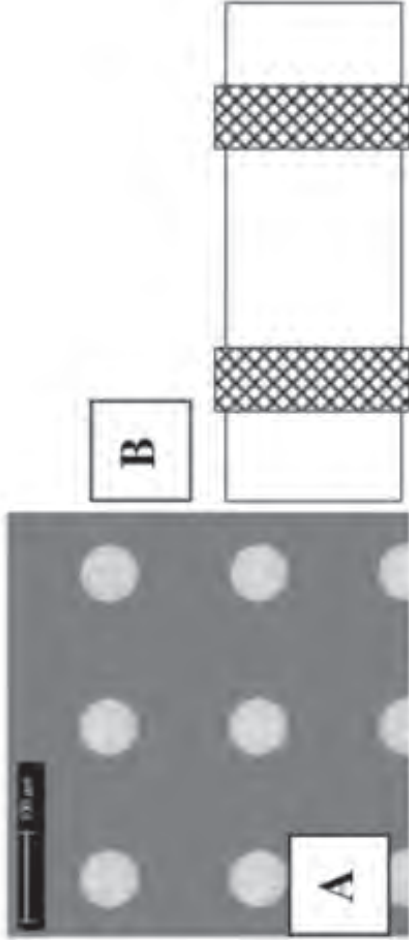
Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>and (B) a schematic representation, in cross section of one possible interposer configuration using this joining core structure, where the crosshatched area is ECA.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p>  <p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 4.</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>“High temperature/pressure lamination is used to cure the adhesive in the PIP and provide electrical interconnection among the packages. A variety of interposer structures such as OS/1P, OS/2P, 2S/1P, 2S/2P can be used. Figure 8 shows optical photographs and SEM micrographs of a joining core having ECA-filled holes with diameters ranging from 55 μm to 65 μm, as a typical representative example of an interposer that can be used for PIP.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“The second building block in this case study was a chip carrier. By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Figure 8. Optical and SEM micrographs of adhesive-filled joining cores; (A) array with ECA-filled vias having a diameter of 55 microns, and (B) corresponding SEM micrograph showing ECA “nubs” extending above the surface of the dielectric in the joining core.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p>See, e.g.:</p> <p>“Figure 4. Various means can be employed for interposer- package joining. Illustrated here is (A) an optical photo, top view, of an interposer formed using an ECA-filled joining core, and (B) a schematic representation, in cross section of one possible interposer configuration using this joining core structure, where the crosshatched area is ECA.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> 
--	---

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

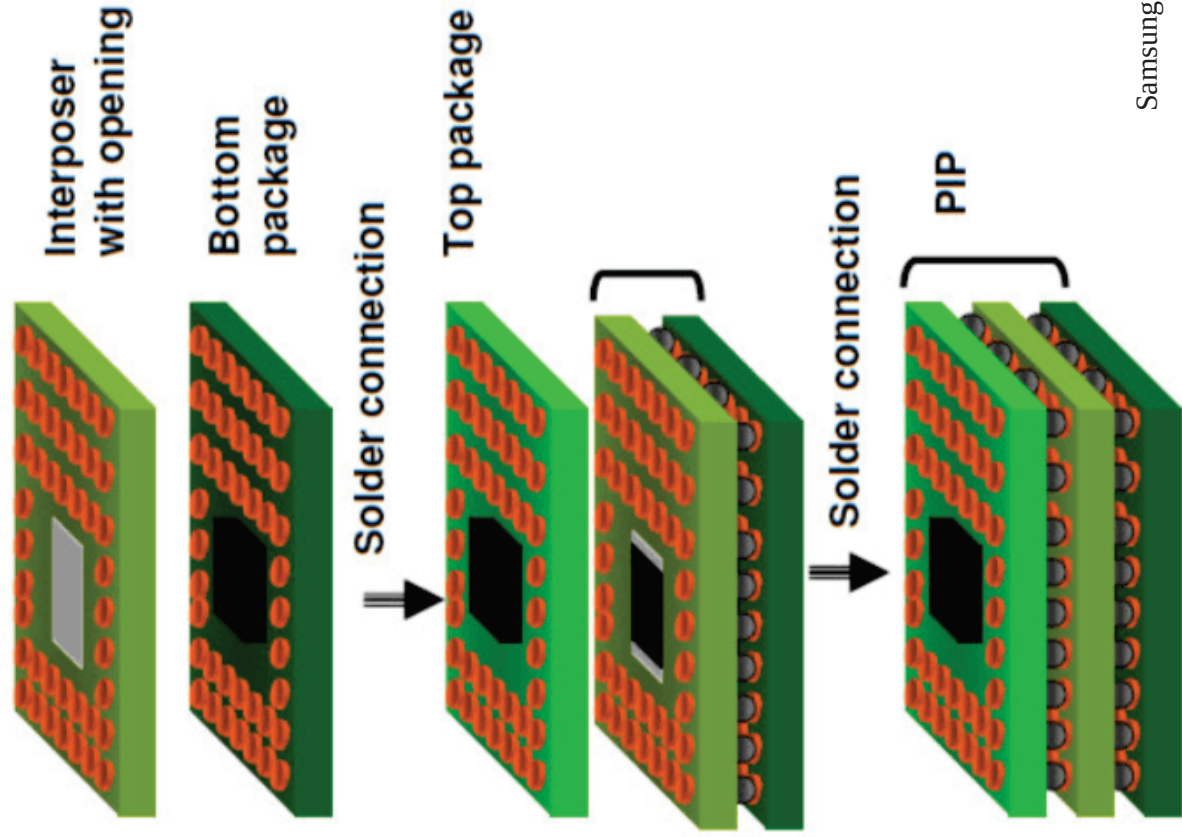
	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 4.</p> <p>“As part of an on-going effort to develop new electrical interconnection between the interposer and the package on either side of the interposer, connections can be made by a Figure 5. Top view of interposer A PIP was constructed using an interposer consisting of multiple metal inner planes. A top view of the contacting” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“High temperature/pressure lamination is used to cure the adhesive in the PIP and provide electrical interconnection among the packages. A variety of interposer structures such as OS/1P, OS/2P, 2S/1P, 2S/2P can be used. Figure 8 shows optical photographs and SEM micrographs of a joining core having ECA-filled holes with diameters ranging from 55 μm to 65 μm, as a typical representative example of an interposer that can be used for PIP. The ECA protrudes above the surface of the dielectric by about 5-10 μm, (Figure 8B). Hole pitch is on the order of 180 μm..” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Similarly, 150-300 μm hole diameter and 500-1000 μm pitch is used for boards. Chip to chip connections require interconnects with diameters ranging from 5 μm to 65 μm, depending on the application.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Figure 8. Optical and SEM micrographs of adhesive-filled joining cores; (A) array with ECA-filled vias having a diameter of 55 microns, and (B) corresponding SEM micrograph showing ECA “nubs” extending above the surface of the dielectric in the joining core.”</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Plated through holes in the interposers, formed by laser or mechanical drilling and having diameters ranging from 50 um to 250 um, were filled with an electrically conductive adhesive and cured. The adhesive-filled and cured interposers were reflowed with circuitized substrates to produce a PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“A top view of the contacting pads for this interposer is shown schematically in Figure 5.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

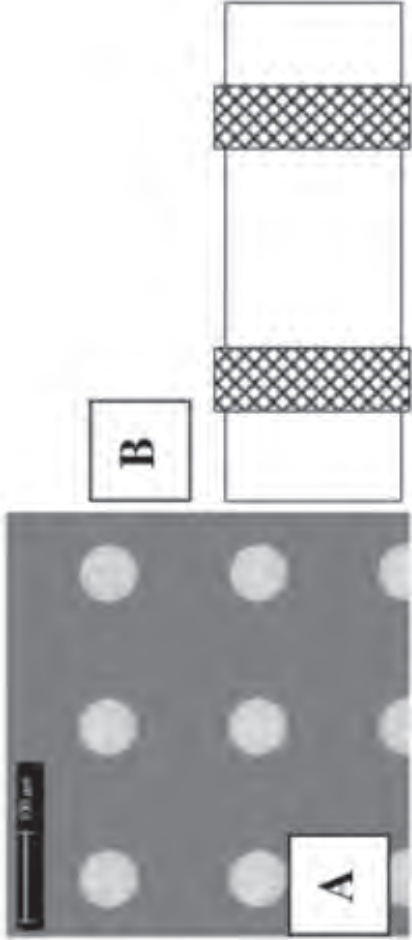
	<p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“Figure 6. Process flow for a PIP construction. The interposer has an opening. The top side of the bottom package is connected with the bottom side of the interposer in such a way that die on the bottom package resides within the opening of the interposer. The bottom side of the top package is connected with the top side of the interposer in a subsequent step to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“By alternating packages and interposer in the lay-up prior to reflow, the solder paste electrically connects copper pads on the package that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [564].</p>
--	---

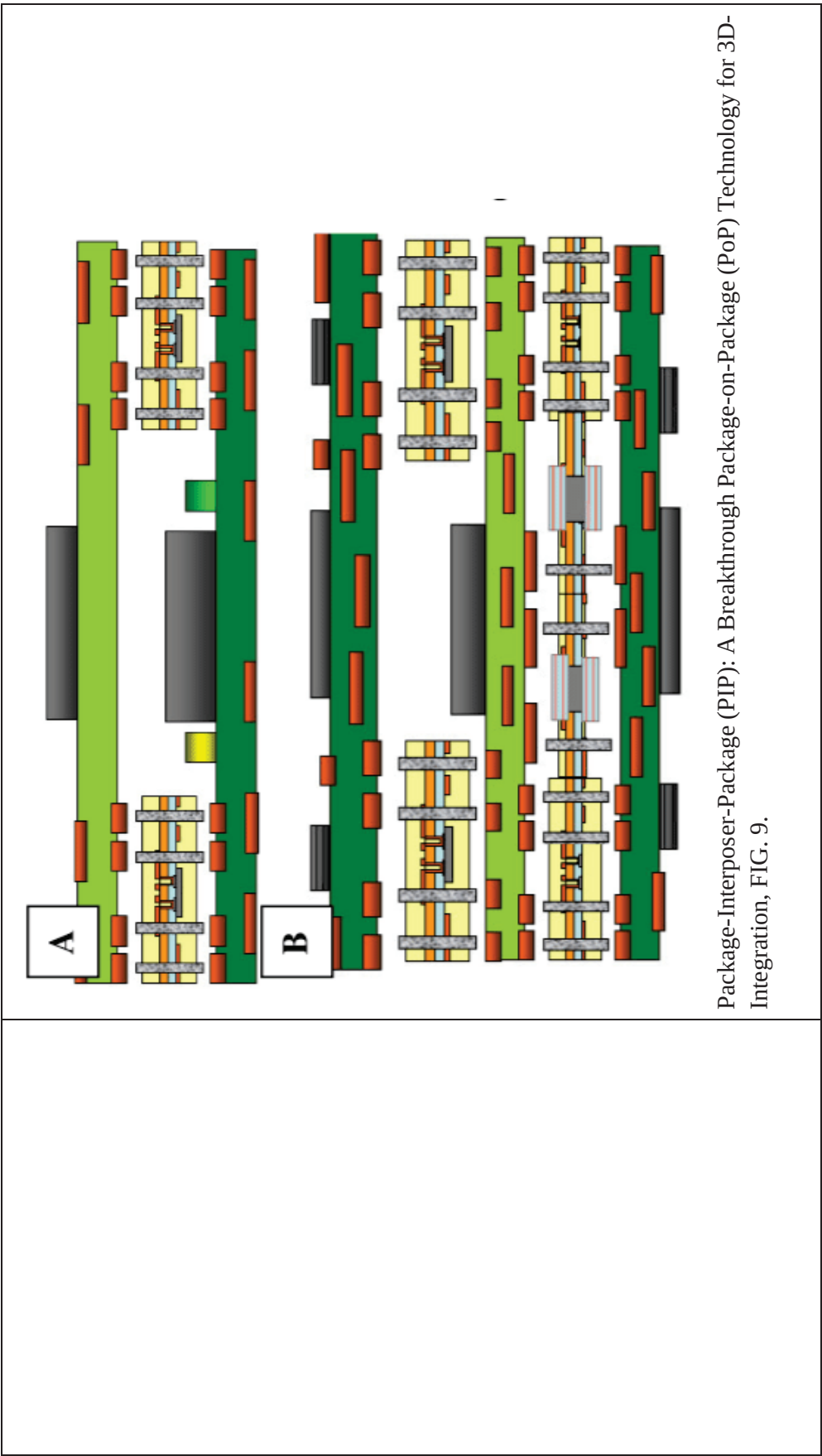


Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 6.</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Various means can be employed for interposer-package joining. Illustrated here is (A) an optical photo, top view, of an interposer formed using an ECA-filled joining core, and (B) a schematic representation, in cross section of one possible interposer configuration using this joining core structure, where the crosshatched area is ECA.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	 <p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 4.</p> <p>“(A) Package-Interposer-Package construction using a single interposer. Here the interposer is a functional/active part of a package, for example an interposer with embedded actives. (B) A stack may contain multiple interposers (n) and packages (n + 1).” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p>
--	---



Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 9.

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Plated through holes in the interposers, formed by laser or mechanical drilling and having diameters ranging from 50 um to 250 um, were filled with an electrically conductive adhesive and cured. The adhesive-filled and cured interposers were reflowed with circuitized substrates to produce a PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“Figure 4 shows an interconnection made using an electrically conductive adhesive (ECA), as is used for joining cores in z-interconnect technology [2]. Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly. This is accomplished by heating the solder to a temperature</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>greater than its melting point (MP).” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer. It can be a single step or multiple step process. Figure 6 shows the processing sequence for this PIP. The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“The second building block in this case study was a chip carrier. By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“A variety of interposer structures such as OS/1P, OS/2P, 2S/1P, 2S/2P can be used. Figure 8 shows optical photographs and SEM micrographs of a joining core having ECA-filled holes with diameters ranging from 55 μm to 65 μm, as a typical representative example of an interposer that can be used for PIP. The ECA protrudes above the surface of the dielectric by about 5-10 μm, (Figure 8B).” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“By alternating packages and interposer in the lay-up prior to reflow, the solder paste electrically connects copper pads on the package that reside on either side of the interposer.”</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“As part of an on-going effort to develop new electrical interconnection between the interposer and the package on either side of the interposer, connections can be made by a Figure 5. Top view of interposer A PIP was constructed using an interposer consisting of</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>multiple metal inner planes. A top view of the contacting” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“A top view of the contacting pads for this interposer is shown schematically in Figure 5.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer. It can be a single step or multiple step process.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer. It can be a single step or multiple step process. Figure 6 shows the processing sequence for this PIP. The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [564].</p>
--	---

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Interconnection among substrates (packages) in the stack was achieved using interposers. Plated through holes in the interposers, formed by laser or mechanical drilling and having diameters ranging from 50 um to 250 um, were filled with an electrically conductive adhesive and cured.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

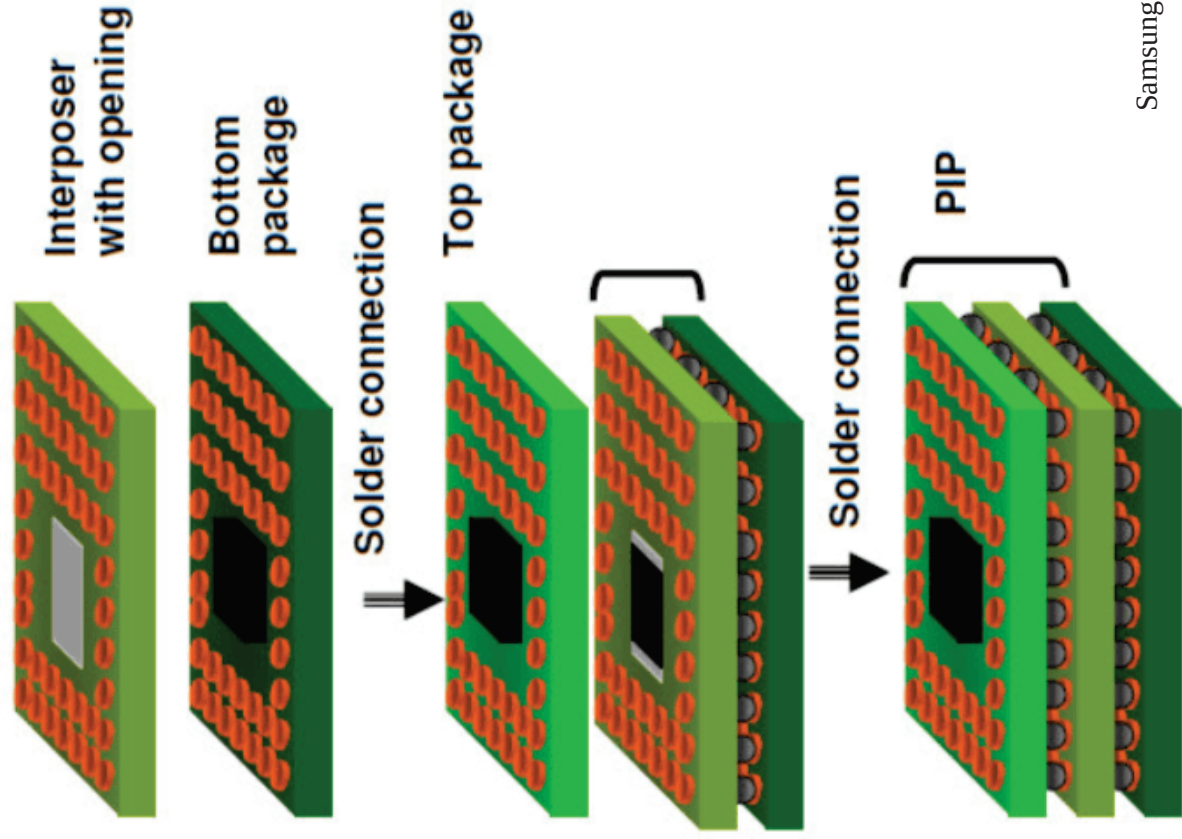
	<p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“High temperature/pressure lamination is used to cure the adhesive in the PIP and provide electrical interconnection among the packages.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“By alternating packages and interposer in the lay-up prior to reflow, the solder paste electrically connects copper pads on the package that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“PIP can accommodate modules with stacked die on organic, ceramic, or silicon board substrates, where each can be detached and replaced without affecting the rest of the package.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“Traditional Package on Package (POP) approaches use direct solder connections between the substrates and are limited to use of single (or minimum) die on the bottom substrate, to reduce warpage and improve stability. For PIP, the stability imparted by the interposer” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“In a similar fashion, the thickness of the PIP interposer(s) would be thicker than the thickest component on the packages which the interposer(s) is connecting.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p>
--	---

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>“The interposer has an opening. The top side of the bottom package is connected with the bottom side of the interposer in such a way that die on the bottom package resides within the opening of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [564].</p>
--	--

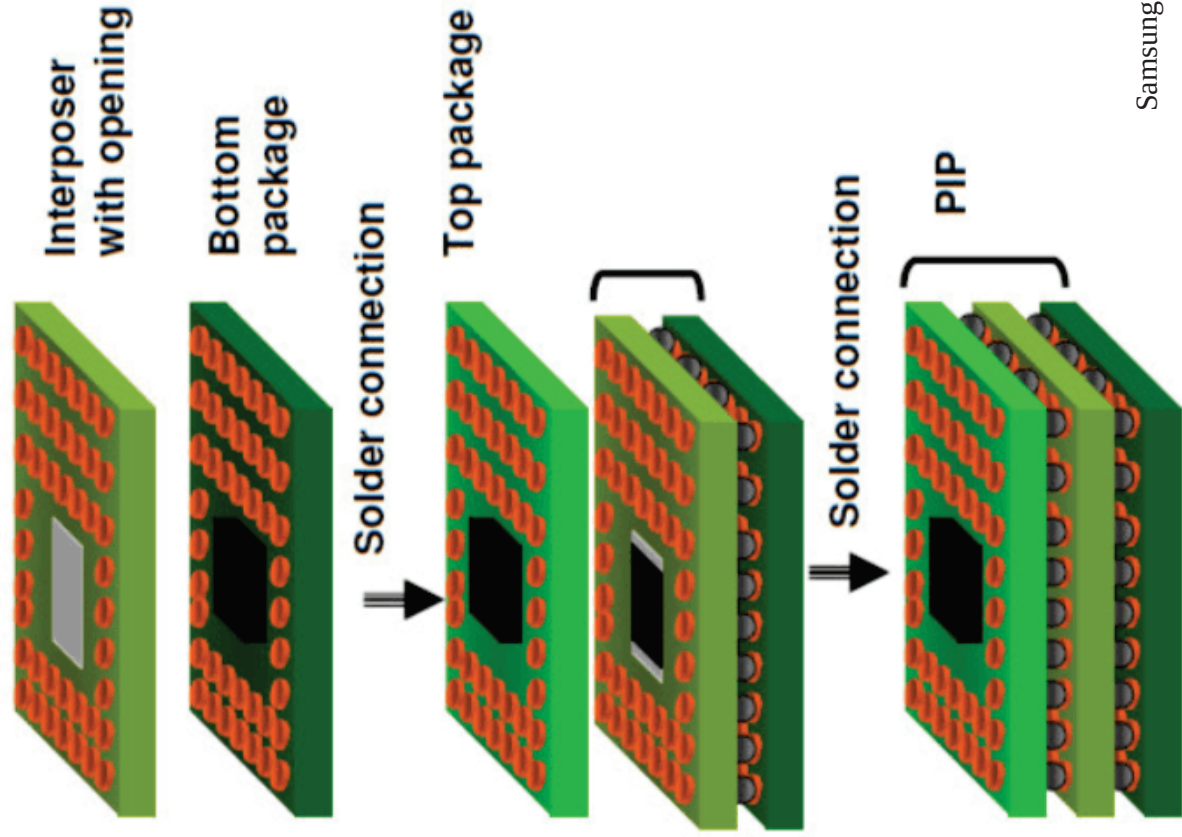


Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 6.</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Traditional Package on Package (POP) approaches use direct solder connections between the substrates and are limited to use of single (or minimum) die on the bottom substrate, to reduce warpage and improve stability.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p>
--	--



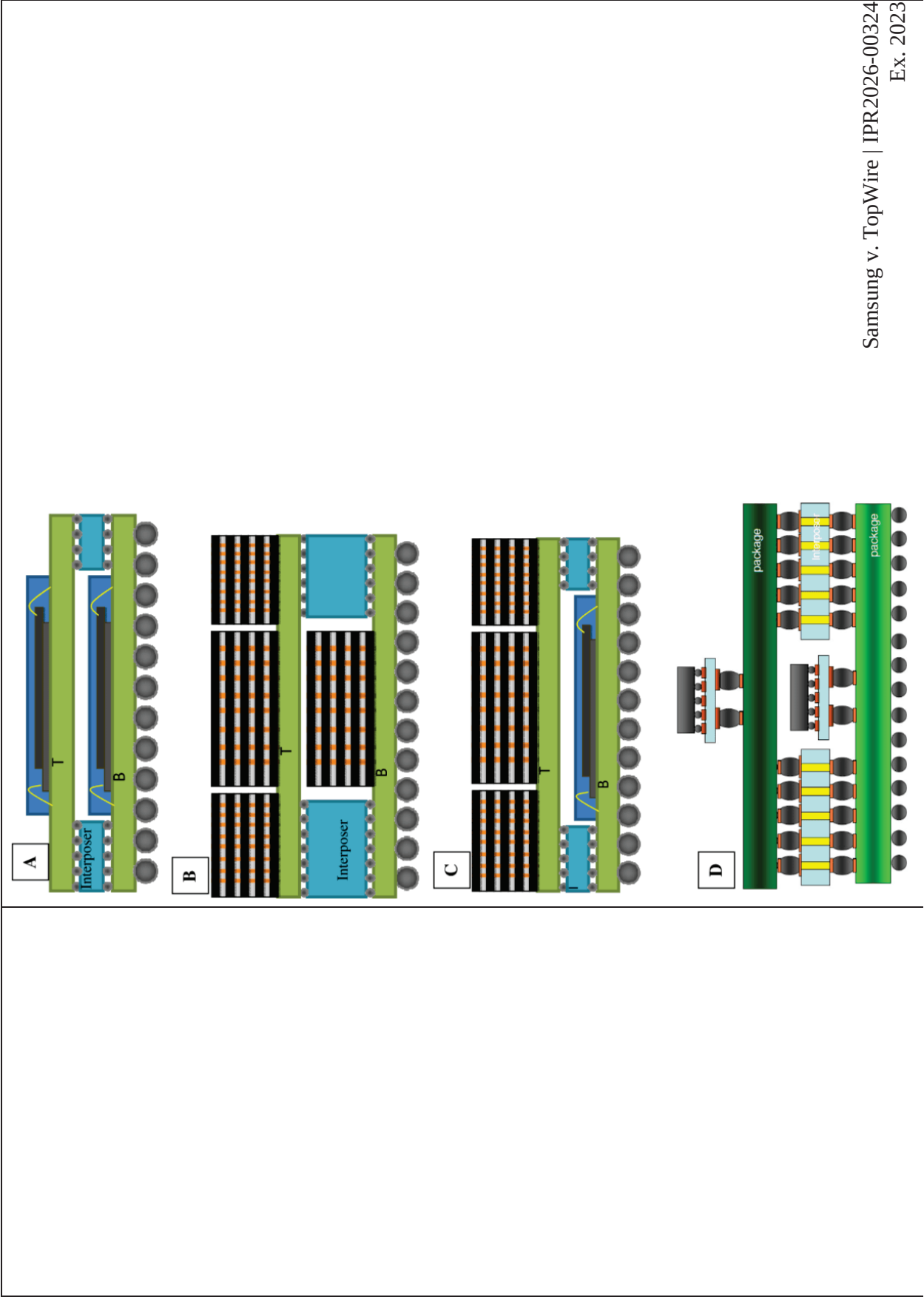
Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 6.</p> <p>“The interposer has an opening. The top side of the bottom package is connected with the bottom side of the interposer in such a way that die on the bottom package resides within the opening of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Figure 6. Process flow for a PIP construction. The interposer has an opening. The top side of the bottom package is connected with the bottom side of the interposer in such a way that die on the bottom package resides within the opening of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“PIP can accommodate modules with stacked die on organic, ceramic, or silicon board substrates, where in some cases defective substrates can be detached and replaced without affecting the rest of the package.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [6].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

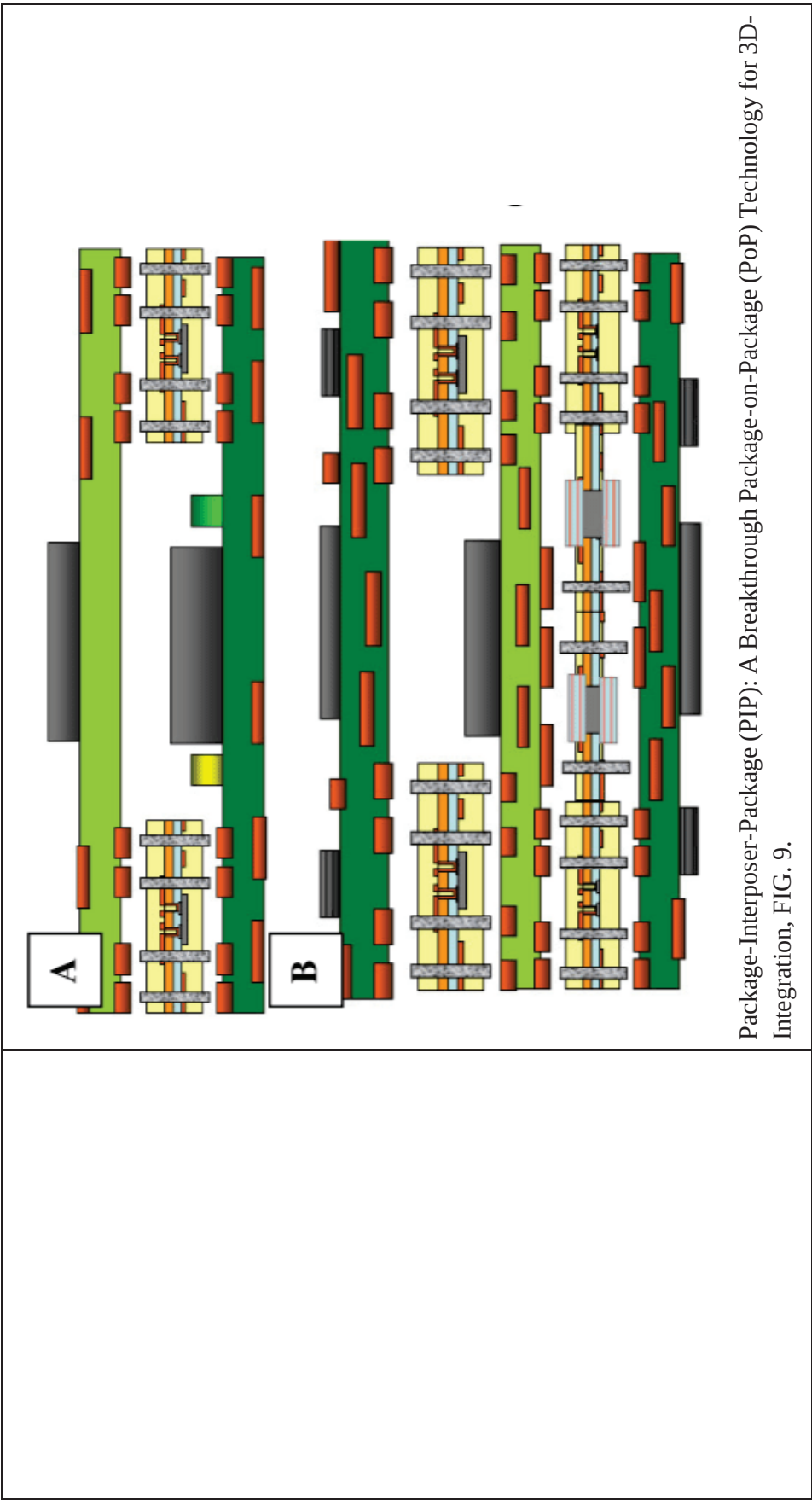
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“Package-Interposer-Package (PIP) construction with a single interposer. (A) Top and bottom packages have wire bonded stacked die, (B) Top and bottom packages have TSV processed stacked die, (C) Top package has TSV processed stacked die, and the bottom package has wired bonded stacked die, (D) 3D-PIP construction with a single interposer”</p> <p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [2].</p>
--	--

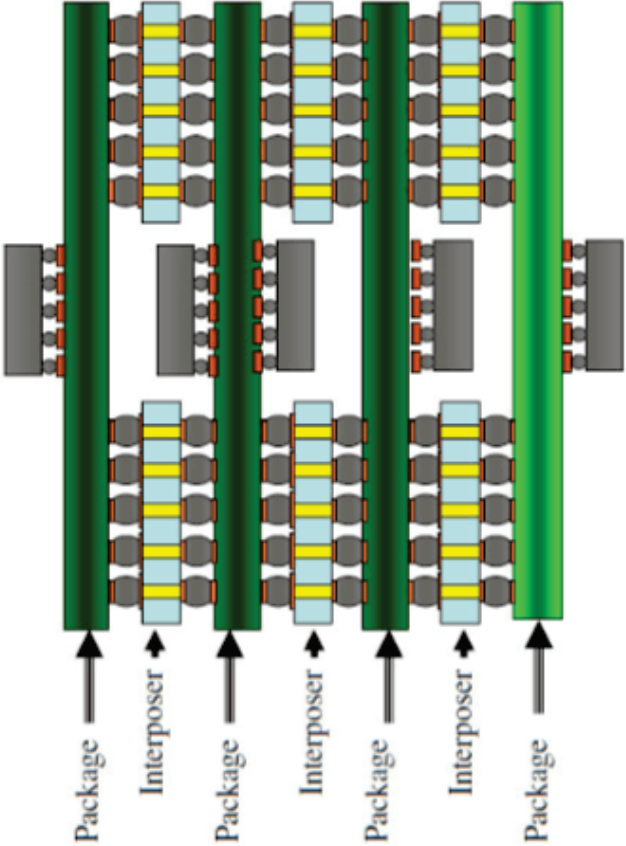
Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication



Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 2.</p> <p>“(A) Package-Interposer-Package construction using a single interposer. Here the interposer is a functional/active part of a package, for example an interposer with embedded actives. (B) A stack may contain multiple interposers (n) and packages (n +1)” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p>
--	---



	<p>“Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p>  <p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 10.</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

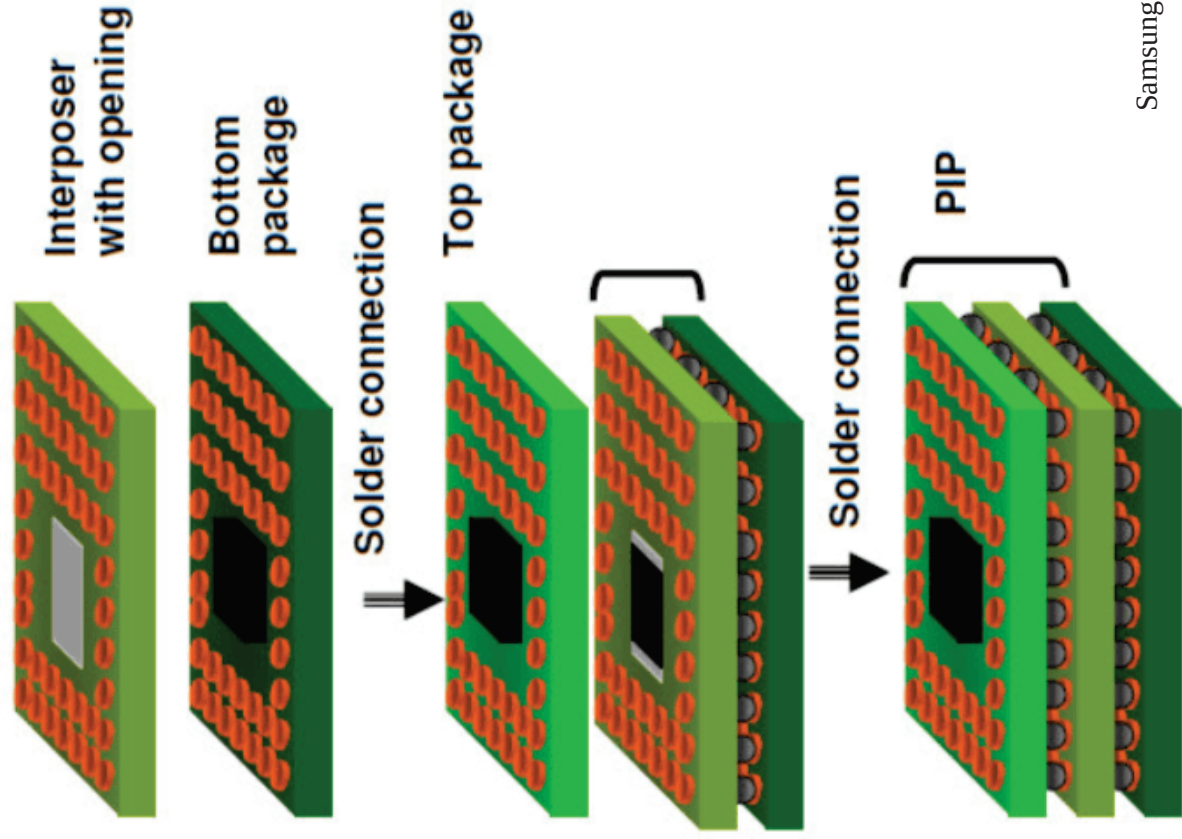
	obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	--

Claim 2, U.S. Patent No. 9,859,202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p> <p>“For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“Traditional Package on Package (POP) approaches use direct solder connections between the substrates and are limited to use of single (or minimum) die on the bottom substrate, to reduce warpage and improve stability. For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>“The total thickness of the stiffeners shown in Figure 3B is always greater than the thickest components on the surface of the package. In a similar fashion, the thickness of the PIP interposer(s) would be thicker than the thickest component on the packages which the interposer(s) is connecting.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“The interposer can have the same opening size as the stiffener to accommodate the area footprint of the component. The same is true for every level of substrate/interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p>
--	---



Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 6.</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that die on the bottom package resides within the opening of the interposer. The bottom side of the top package is connected with the top side of the interposer in a subsequent step to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

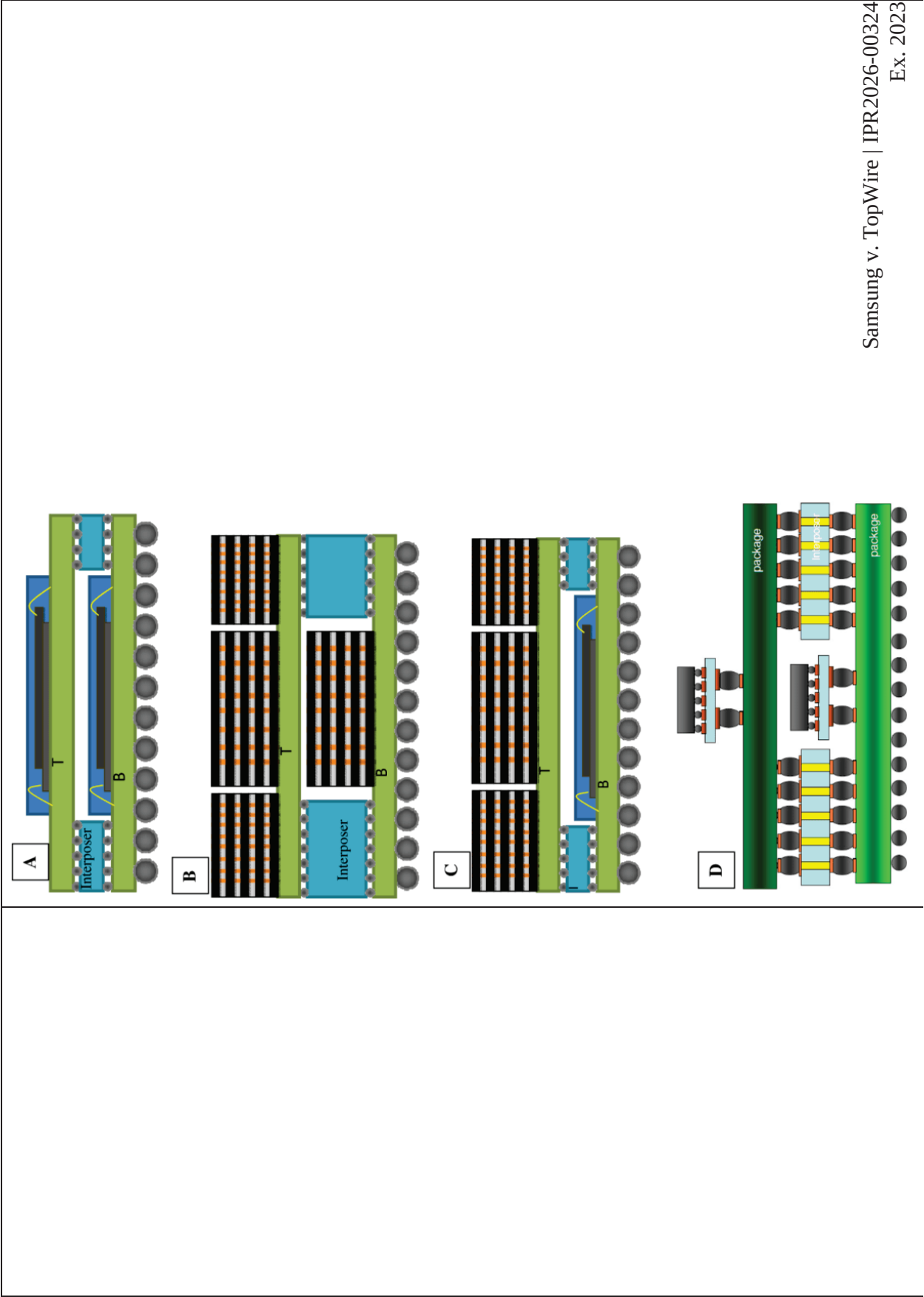
Claim 3, U.S. Patent No. 9,859,202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

overlaps the bottom chip and each of the two spacer connectors.	<p>See, e.g.:</p> <p>“For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“Figure 2: Package-Interposer-Package (PIP) construction with a single interposer. (A) Top and bottom packages have wire bonded stacked die, (B) Top and bottom packages have TSV processed stacked die, (C) Top package has TSV processed stacked die, and the bottom package has wired bonded stacked” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [2].</p>
---	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication



Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, FIG. 2.</p> <p>“Figure 6. Process flow for a PIP construction. The interposer has an opening. The top side of the bottom package is connected with the bottom side of the interposer in such a way that die on the bottom package resides within the opening of the interposer. The bottom side of the top package is connected with the top side of the interposer in a subsequent step to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“PIP can accommodate modules with stacked die on organic, ceramic, or silicon board substrates, where in some cases defective substrates can be detached and replaced without affecting the rest of the package.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [6].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

Claim 4, U.S. Patent No. 9,859,202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“For PIP, use of an interposer between the two packages provides for the use of low volume interconnect metallurgy between the interposer and the packages, enabling finer pitch connections from package to package.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [2].</p> <p>“A PIP was constructed using an interposer consisting of multiple metal inner planes. A top view of the contacting pads for this interposer is shown schematically in Figure 5.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.” Package-</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“By alternating packages and interposer in the lay-up prior to reflow, the solder paste electrically connects copper pads on the package that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9,859,202

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to</p>

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“The ECA protrudes above the surface of the dielectric by about 5-10 μm, (Figure 8B).” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Figure 8. Optical and SEM micrographs of adhesive-filled joining cores; (A) array with ECA-filled vias having a diameter of 55 microns, and (B) corresponding SEM micrograph showing ECA “nubs” extending above the surface of the dielectric in the joining core.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9,859,202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a	Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration discloses, either expressly or inherently, wherein the spacer connector further comprises

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

<p>plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Electrical connections were formed during reflow using a tin- lead eutectic solder paste. Interconnection among substrates (packages) in the stack was achieved using interposers. Plated through holes in the interposers, formed by laser or mechanical drilling and having diameters ranging from 50 um to 250 um, were filled with an electrically conductive adhesive and cured.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [1].</p> <p>“A PIP was constructed using an interposer consisting of multiple metal inner planes. A top view of the contacting pads for this interposer is shown schematically in Figure 5. 1499 Figure 3B. Module with stiffener and components. 000563 45th International Symposium on Microelectronics September 9-13, 2012 San Diego, California USA The second building block in this case study was a chip carrier. By alternating chip carrier and interposer in the lay-” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3-4].</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the</p>
---	--

	<p>assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“Figure 4 shows an interconnection made using an electrically conductive adhesive (ECA), as is used for joining cores in z-interconnect technology [2]. Connection between interposer and package made using solder between a pad on the interposer and a pad on the” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [3].</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer. It can be a single step or multiple step process. Figure 6 shows the processing sequence for this PIP. The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [4].</p> <p>“Figure 10: Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers. Figure 9. (A) Package-Interposer-Package construction using a single interposer. Here the interposer is a functional/active part of a package, for example an interposer with embedded actives. (B) A stack may contain multiple interposers (n) and packages (n+1). (PIP) As a case study, an example of extreme 3D interconnect technology using a Package-Interposer-Package concept was constructed using three interposers and four</p>
--	--

Appendix A-36 - Invalidity of U.S. Patent No. 9,859,202 in view of Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration - Non-Patent Publication

	<p>assembled packages consisting of multiple metal inner planes. By alternating packages and interposer in the lay-up prior to reflow, the solder paste electrically connects copper pads on the package that reside on either side of the interposer.” Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration, [5].</p> <p>To the extent Plaintiff contends that Package-Interposer-Package (PIP): A Breakthrough Package-on-Package (PoP) Technology for 3D-Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

Copper Pillar Bumping Technology was published by Christopher Henderson. Copper Pillar Bumping Technology anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Copper Pillar Bumping Technology is an academic article that was published June 27, 2012. Copper Pillar Bumping Technology is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Copper Pillar Bumping Technology, or otherwise rendered obvious by disclosures and teachings of Copper Pillar Bumping Technology, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Copper Pillar Bumping Technology does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Copper Pillar Bumping Technology with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Copper Pillar Bumping Technology, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Copper Pillar Bumping Technology “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Copper Pillar Bumping Technology or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Copper Pillar Bumping Technology set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Copper Pillar Bumping Technology discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Figure 3. Optical image of a cross-section through an FCOL package with copper pillar bumps.” Copper Pillar Bumping Technology, [3].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For small dice, copper pillars can be used with no underfill in injection-molded components like QFN and Thin Small Outline Packages, or TSOPs. The connections can be made using solder materials with no-clean fluxes. For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow-able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“Copper pillar bumps are now commonly used on QFN packages. They provide benefits for high-speed circuits, including improved co-planarity and heat dissipation.” Copper Pillar Bumping Technology, [3].</p>
[1.A] a bottom package substrate;	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“In this example, the silicon interposer is attached to the package substrate using copper pillar” Copper Pillar Bumping Technology, [1].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>“Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow-able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“Most manufacturers are experimenting with no-flow underfills, no-clean fluxes, and pre-plated leadframes (typically nickel-palladium-gold) to provide both manufacturability and reliability improvements.” Copper Pillar Bumping Technology, [4].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

define a space between the bottom package substrate and the top package substrate, wherein	<p>See, e.g.:</p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Copper pillars can be held to the substrate more securely through the use of an underfill. The underfill is applied as a non-conductive paste in the open areas between the pillars. The chip is then placed onto the substrate and the underfill is snap-cured.” Copper Pillar Bumping Technology, [2].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p>
--	--

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.D] the spacer connector comprises a core substrate;	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Copper pillars can be held to the substrate more securely through the use of an underfill. The underfill is applied as a non-conductive paste in the open areas between the pillars. The chip is then placed onto the substrate and the underfill is snap-cured.” Copper Pillar Bumping Technology, [2].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow-able tin solder.” Copper Pillar Bumping Technology, [3].</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Copper pillars can be held to the substrate more securely through the use of an underfill. The underfill is applied as a non-conductive paste in the open areas between the pillars. The chip is then placed onto the substrate and the underfill is snap-cured.” Copper Pillar Bumping Technology, [2].</p> <p>“Copper pillar bumping is intended as a replacement to traditional solder bumping” Copper Pillar Bumping Technology, [2].</p> <p>“Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow. The solder is consumed, as well as a portion of the copper pillars, forming an intermetallic compound that provides the mechanical and electrical connection. Silicon” Copper Pillar Bumping Technology, [3].</p> <p>“The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow-able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone</p>
--	--

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“In this example, the silicon interposer is attached to the package substrate using copper pillar bumps.” Copper Pillar Bumping Technology, [1].</p> <p>“Figure 2 shows the deformed tin-silver cap on the copper pillar that results from this process.” Copper Pillar Bumping Technology, [2].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow. The solder is consumed, as well as a portion of the copper pillars, forming an intermetallic compound that provides the mechanical and electrical connection.” Copper Pillar Bumping Technology, [3].</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Copper pillar bumps are now commonly used on QFN packages. They provide benefits for high-speed circuits, including improved co-planarity and heat dissipation.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Copper pillars can be held to the substrate more securely through the use of an underfill. The underfill is applied as a non-conductive paste in the open areas between the pillars. The</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>chip is then placed onto the substrate and the underfill is snap-cured.” Copper Pillar Bumping Technology, [2].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

corresponding metal pillar among the plurality of metal pillars of the spacer connector,	<p>See, e.g.:</p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“An example of a circuit that employs copper pillar bumping. Copper pillar bumping is intended as a replacement to traditional solder bumping. While solder bumping is a lower cost process than copper pillar bumping, it doesn’t allow for the density and current” Copper Pillar Bumping Technology, [2].</p> <p>“Copper pillar bumping is intended as a replacement to traditional solder bumping” Copper Pillar Bumping Technology, [2].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow. The solder is consumed, as well as a portion of the copper pillars, forming an intermetallic compound that provides the mechanical and electrical connection.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate. The underfills can use capillary action and can be reworkable or” Copper Pillar Bumping Technology, [3].</p>
--	--

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“Copper pillar bumps are now commonly used on QFN packages. They provide benefits for high-speed circuits, including improved co-planarity and heat dissipation.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Copper pillar bumping is intended as a replacement to traditional solder bumping” Copper Pillar Bumping Technology, [2].</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow. The solder is consumed, as well as a portion of the copper pillars, forming an intermetallic compound that provides the mechanical and electrical connection.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow-able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow-able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Copper pillar technology can be used on small dice in small packages like quad flat no-lead, or QFN, packages, on medium dice with the pillars providing connection to a laminate substrate, and on large dice 2 Issue 36 June 2012” Copper Pillar Bumping Technology, [2].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“Copper pillar bumps are now commonly used on QFN packages. They provide benefits for high-speed circuits, including improved co-planarity and heat dissipation.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p>
--	---

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Copper pillars can be held to the substrate more securely through the use of an underfill. The underfill is applied as a non-conductive paste in the open areas between the pillars. The chip is then placed onto the substrate and the underfill is snap-cured.” Copper Pillar Bumping Technology, [2].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>“For large dice, Intel, Amkor and Texas Instruments have all released products that use fine pitch copper pillar bumps. These devices have utilized more than 200 I/O connections.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p>See, e.g.:</p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using</p>

	<p>copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“An example of a circuit that employs copper pillar bumping. Copper pillar bumping is intended as a replacement to traditional solder bumping. While solder bumping is a lower cost process than copper pillar bumping, it doesn’t allow for the density and current” Copper Pillar Bumping Technology, [2].</p> <p>“Copper pillars can be held to the substrate more securely through the use of an underfill. The underfill is applied as a non-conductive paste in the open areas between the pillars. The chip is then placed onto the substrate and the underfill is snap-cured.” Copper Pillar Bumping Technology, [2].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“For small dice, copper pillars can be used with no underfill in injection-molded components like QFN and Thin Small Outline Packages, or TSOPs. The connections can be made using solder materials with no- clean fluxes. For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p>
--	---

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Copper pillar technology can be used on small dice in small packages like quad flat no-lead, or QFN, packages, on medium dice with the pillars providing connection to a laminate substrate, and on large dice 2 Issue 36 June 2012” Copper Pillar Bumping Technology, [2].</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow- able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

plurality of top metal pillars of the bottom package substrate.	<p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow. The solder is consumed, as well as a portion of the copper pillars, forming an intermetallic compound that provides the mechanical and electrical connection.” Copper Pillar Bumping Technology, [3].</p> <p>“Copper pillar bumps are now commonly used on QFN packages. They provide benefits for high-speed circuits, including improved coplanarity and heat dissipation.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow-able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
---	--

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Copper Pillar Bumping Technology discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Figure 1 shows an example where copper pillar bumping enables 3-D integration and packaging. In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Figure 2 shows the deformed tin-silver cap on the copper pillar that results from this process.” Copper Pillar Bumping Technology, [2].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow. The solder is consumed, as well as a portion</p>

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>of the copper pillars, forming an intermetallic compound that provides the mechanical and electrical connection.” Copper Pillar Bumping Technology, [3].</p> <p>“For small dice, copper pillars can be used with no underfill in injection-molded components like QFN and Thin Small Outline Packages, or TSOPs. The connections can be made using solder materials with no-clean fluxes.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflowable tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and the bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the	Copper Pillar Bumping Technology discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

<p>pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“In this example, the silicon interposer is attached to the package substrate using copper pillar bumps. TSVs through the silicon interposer bring signals to the active dice on top.” Copper Pillar Bumping Technology, [1].</p> <p>“Figure 2 shows the deformed tin-silver cap on the copper pillar that results from this process.” Copper Pillar Bumping Technology, [2].</p> <p>“Figure 4 helps to illustrate the micro-bumping process. This is a process that facilitates die-to-die bonding. Copper pillars are attached to both dice, with tin solder applied to one of the die. In this example, we show it applied to the flipped die. The dice are brought in contact with one another and then subjected to reflow. The solder is consumed, as well as a portion of the copper pillars, forming an intermetallic compound that provides the mechanical and electrical connection.” Copper Pillar Bumping Technology, [3].</p> <p>“Here is an example of a small die in a flip chip on lead, or FCOL, package. The copper pillar is mounted to the bond pad, and the die is flipped upside down and mounted to the copper leadframe with a reflow-able tin solder.” Copper Pillar Bumping Technology, [3].</p> <p>“For medium and large-sized dice, underfills with flux are required to stabilize the stresses between the die and the substrate.” Copper Pillar Bumping Technology, [3].</p>
---	--

Appendix A-40 - Invalidity of U.S. Patent No. 9859202 in view of Copper Pillar Bumping Technology - Non-Patent Publication

	<p>“Most manufacturers are experimenting with no-flow underfills, no-clean fluxes, and pre-plated leadframes (typically nickel-palladium-gold) to provide both manufacturability and reliability improvements.” Copper Pillar Bumping Technology, [4].</p> <p>To the extent Plaintiff contends that Copper Pillar Bumping Technology fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

**Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication**

E.D. Tex. Case No. 2:25-CV-1183

**INVALIDITY CLAIM CHART
Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration - Non-Patent
Publication**

Embedded Glass Interposer for Heterogeneous Multi-Chip Integration was published by Dyi-Chung Hu. Embedded Glass Interposer for Heterogeneous Multi-Chip Integration anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Embedded Glass Interposer for Heterogeneous Multi-Chip Integration is an academic article that was published May 29, 2015. Embedded Glass Interposer for Heterogeneous Multi-Chip Integration is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, or otherwise rendered obvious by disclosures and teachings of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations;

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

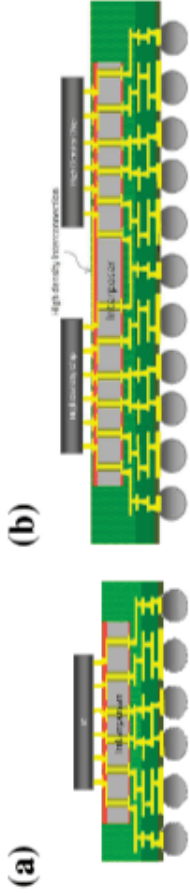
Where the chart below states that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Embedded Glass Interposer for Heterogeneous Multi-Chip Integration or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Embedded Glass Interposer for Heterogeneous Multi-Chip Integration set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, a structure.</p> <p>See, e.g.:</p> <p>“In this study, an EIC substrate with embedded glass interposer for flip chip assembly is demonstrated. Glass interposers with size of 21x14 mm² and 100 μm thickness, through glass</p>

vias (TGV) of 30 μm diameter, and line/space of 3 $\mu\text{m}/3 \mu\text{m}$ were produced. Subsequently, the glass interposer was embedded in built-up dielectric materials to form the EIC substrate. Multi-layers dielectrics were built up with filled blind vias and RDL patterns to fan-out the circuits from the embedded glass interposer.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].



Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, FIG. 2.

“Figure 2. FC-EIC structure for (a) single chip integration and (b) multi-chip integration” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].

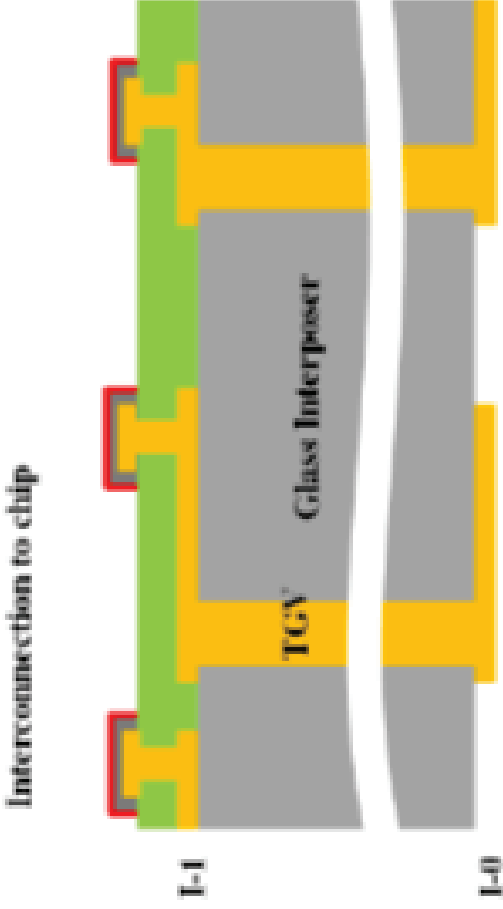
“Table 1 showed the general specifications of the interposers used in this study.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].

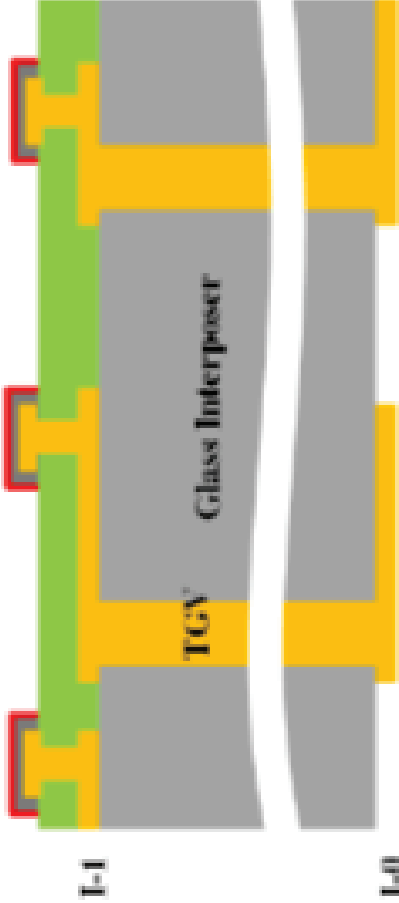
“The general specifications of EIC- Glass substrate were listed in Table 2.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].

“Table 3. General specifications of the chips to be integrated in EIC-Glass substrate” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

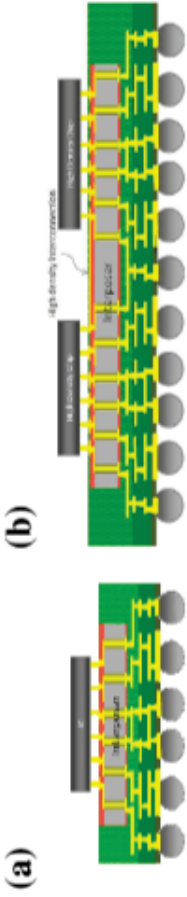
	<p>“Figure 6. Accomplishments of EIC-Glass substrate (25mm x 25mm)” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p>
<p>[1.A] a bottom package substrate;</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Reliability and electrical performance can be improved due to the direct interconnection of the interposer to carrier by means of Cu plating rather than solder joining.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“Table 1. General specifications of the glass interposer” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p>

	 <p>Interconnection to chip</p> <p>Interconnection to carrier</p> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, e.g.:</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	

	<p>Interconnection to chip</p>  <p>Interconnection to carrier</p> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p>
[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom	

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

package substrate and the top package substrate, wherein	<p><i>See, e.g.:</i></p> <p>“Interposer technology has been developed for providing a fine line/space and high density interconnections that cannot be matched by current laminate substrate technology.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“In this study, an EIC substrate with embedded glass interposer for flip chip assembly is demonstrated. Glass interposers with size of 21x14 mm² and 100 μm thickness, through glass vias (TGV) of 30 μm diameter, and line/space of 3 μm/3 μm were produced. Subsequently, the glass interposer was embedded in built-up dielectric materials to form the EIC substrate.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“Fine pitch interconnection is needed to achieve high performance requirement of future electronic devices. 2.5D package structure which contains an interposer with fine pitch interconnections together with vertical through silicon via (TSV) to connect devices can reduce laminate layers and enhancing the performance of the package.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“FC-EIC structure for (a) single chip integration and (b) multi-chip integration” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p>
--	---

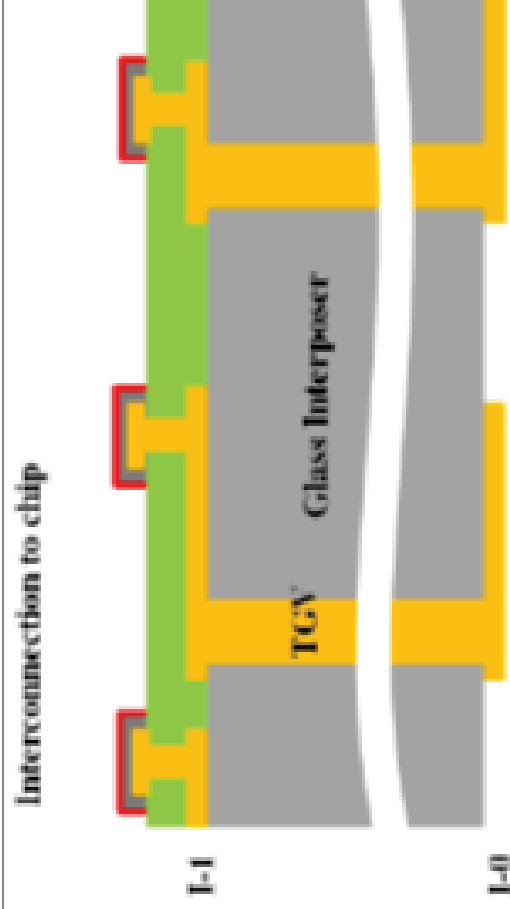
	<div>  </div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, FIG. 2.</p> <p>“After the 12” glass interposer wafers fabricating process, the interposer wafer was singularized into individual interposer chips. Subsequently the interposer chips were attached to a temporary carrier with alignment accuracy $\leq 10 \mu\text{m}$. Later the bonded glass interposers were embedded into a 2-layers laminate substrate using ABF typed materials.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“In the built-up process of EIC-Glass, the glass interposer was attached to an organic core panel. The built-up approaches were in panel level (508 mm x 508 mm).” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p>

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	<p><i>See, e.g.:</i></p> <p>“We have been developing EIC (Embedded Interposer Carrier) technology which eliminates the interconnection between the interposer and the underneath organic substrate [1, 2].” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“Subsequently, the glass interposer was embedded in built-up dielectric materials to form the EIC substrate.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“In this study, EIC substrate using glass interposers for multi-chip module was fabricated.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“After the 12” glass interposer wafers fabricating process, the interposer wafer was singularized into individual interposer chips. Subsequently the interposer chips were attached to a temporary carrier with alignment accuracy $\leq 10 \mu\text{m}$. Later the bonded glass interposers were embedded into a 2-layers laminate substrate using ABF typed materials.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“In the built-up process of EIC-Glass, the glass interposer was attached to an organic core panel.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>“Figure 7 showed the cross-sectional view of the accomplished EIC-Glass substrate. The interposers were 316 successfully embedded into the carrier.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316-317].</p>
--	---

**Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication**

	<p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“In this study, an EIC substrate with embedded glass interposer for flip chip assembly is demonstrated. Glass interposers with size of 21x14 mm² and 100 μm thickness, through glass vias (TGV) of 30 μm diameter, and line/space of 3 μm/3 μm were produced.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“TGV holes were provided by Corning glass. Detail processes of glass interposer were described in previous study [4]. Interconnections on top of the interposer chip are Cu pillar for integrating with silicon chips. The minimum line/space design in this test vehicle is 3μm/3μm on the glass interposer. And two chips were designed for glass interposer integration to form an EIC module.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p>

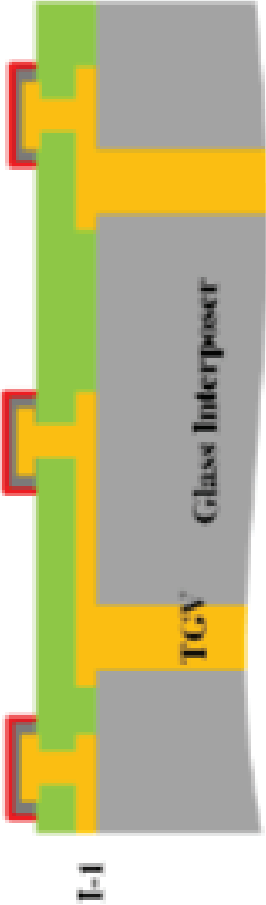


Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.

“Table 2. General specifications of the EIC-Glass substrate EIC-Glass Size Layer 25 mm x 25 mm 2 layers C1 Schematic C2 H D1 D2 SM I-1 Schematic Size Design Glass Interposer Interconnection to chip TGV Glass Interposer I-0 Integration to carrier 21 mm x 14 mm 21000.0 Line/space Pad Via ϕ Cu thickness Solder mask 30 μm / 30 μm C1: 100 μm C2: 200 μm 60 μm for built up layer 110 μm opening for probing 16 μm for each layer 50 μm Table 3. General specifications of the chips to be integrated in EIC-Glass substrate AP area Wide I/O area Size Dummy AP chip on EIC-Glass 9 mm x 9 mm Dummy wide I/O chip on EIC-Glass 10 mm x 10 mm Pillar : 20 μm Pillar pitch: 80 μm ” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].

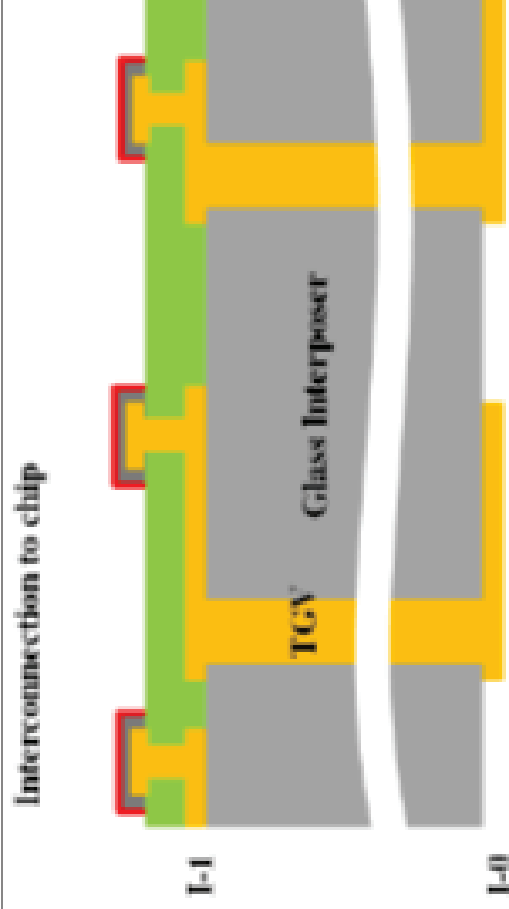
Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	<p>“Figure 7 showed the cross-sectional view of the accomplished EIC-Glass substrate. The interposers were 316 successfully embedded into the carrier. It is also noted that the bumping structure for integrating conventional interposers to carrier was eliminated and replaced by blind via forming and Cu plating.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316-317].</p> <p>“For the glass interposer shown in Figure 3, there are 5,380 TGVs in one glass interposer.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>“For evaluating the reliability of the EIC substrate, daisy chain connections were design in the fabricated test vehicle. Figure 8 showed the daisy chains designed for evaluating the reliability of the EIC-Glass substrate. Each daisy chain contains 50 TGVs.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [317].</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

	<p>“Interconnections on top of the interposer chip are Cu pillar for integrating with silicon chips.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <div> <div> <p>Interconnection to chip</p>  <p>I-1</p> </div> <div> <p>Integration to carrier</p>  <p>I-0</p> </div> </div> <p>Class Interposer</p> <p>TGV</p> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p> <p>“Table 3. General specifications of the chips to be integrated in EIC-Glass substrate AP area Wide I/O area Size Dummy AP chip on EIC-Glass 9 mm x 9 mm Dummy wide I/O chip on EIC-Glass 10 mm x 10 mm” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“I-O metal Line/space: 3 μm / 3 μm μm Pad o: 40 μm, Cu thickness: 3” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p>
--	--

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	<p>“1-1 metal TSV/TGV I-O metal Line/space: 3 μm / 3 μm μη Pad o: 40 μm, Cu thickness: 3” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“After a series of built-up processes, the built-up EIC substrate was released from the organic panel. Surface cleaning was used to remove the residue on the released EIC substrate and a layer of PdAu was applied on the Cu pillars.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Table 1. General specifications of the glass interposer” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p>



Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.

“Subsequently the interposer chips were attached to a temporary carrier with alignment accuracy $\leq 10\text{ }\mu\text{m}$. Later the bonded glass interposers were embedded into a 2-layers laminate substrate using ABF typed materials.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].

“After the 12” glass interposer wafers fabricating process, the interposer wafer was singularized into individual interposer chips. Subsequently the interposer chips were attached to a temporary carrier with alignment accuracy $\leq 10\text{ }\mu\text{m}$. Later the bonded glass interposers were embedded into a 2-layers laminate substrate using ABF typed materials. In 315 Layout

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	<p>Min. line/space 6 um/ 6 um 5 um line Line width RDL image I/O pin count Bump size o Space 2904” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“Interconnections on top of the interposer chip are Cu pillar for integrating with silicon chips.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“Figure 7 showed the cross-sectional view of the accomplished EIC-Glass substrate. The interposers were 316 successfully embedded into the carrier. It is also noted that the bumping structure for integrating conventional interposers to carrier was eliminated and replaced by blind via forming and” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316-317].</p> <p>“After a series of built-up processes, the built-up EIC substrate was released from the organic panel. Surface cleaning was used to remove the residue on the released EIC substrate and a layer of PdAu was applied on the Cu pillars.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

<p>plurality of metal pillars of the spacer connector,</p>	<p>See, e.g.:</p> <div> <p>The diagram consists of two cross-sectional views of a glass interposer. The top view, labeled 'I-1' and titled 'Interconnection to chip', shows a grey substrate with a yellow 'TCV' (Through-Circuit Via) and a green 'Glass Interposer' layer. A red outline indicates a connection to a chip. The bottom view, labeled 'I-0' and titled 'Integration to carrier', shows the same grey substrate with the yellow TCV and green glass interposer layer, but without the chip connection. The text 'Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.' is located below the diagrams.</p> </div> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.1] the bottom package substrate has, on a top surface thereof, a plurality of top</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars</p>

metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and	<p>each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“FC-EIC structure for (a) single chip integration and (b) multi-chip integration” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <div> </div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, FIG. 2.</p> <p>“After the 12” glass interposer wafers fabricating process, the interposer wafer was singularized into individual interposer chips. Subsequently the interposer chips were attached to a temporary carrier with alignment accuracy $\leq 10\text{ }\mu\text{m}$. Later the bonded glass interposers were embedded into a 2-layers laminate substrate using ABF typed materials.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“Interconnections on top of the interposer chip are Cu pillar for integrating with silicon chips. The minimum line/space design in this test vehicle is $3\mu\text{m}/3\mu\text{m}$ on the glass interposer.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p>
--	---

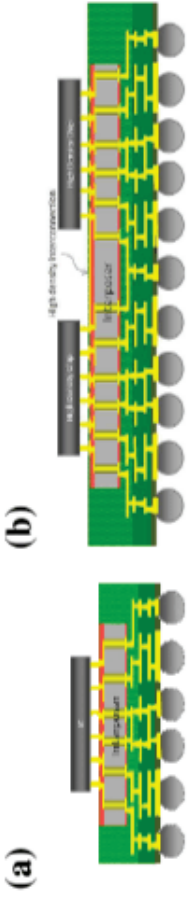
Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	<p>“In the built-up process of EIC-Glass, the glass interposer was attached to an organic core panel. The built-up approaches were in panel level (508 mm x 508 mm). The RDL patterns on EIC-Glass were defined by LDI (laser direct imaging). With well-developed seed layer forming and Cu plating processes, the RDLs on the built-up layers can be successfully formed.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>“After a series of built-up processes, the built-up EIC substrate was released from the organic panel. Surface cleaning was used to remove the residue on the released EIC substrate and a layer of PdAu was applied on the Cu pillars.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>“Figure 7 showed the cross-sectional view of the accomplished EIC-Glass substrate. The interposers were 316 successfully embedded into the carrier. It is also noted that the bumping structure for integrating conventional interposers to carrier was eliminated and replaced by blind via forming and” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316-317].</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p>

<p>substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<div> <p>See, e.g.:</p> </div> <div> <p>The diagram consists of two cross-sectional views of a glass interposer. The top view, labeled 'I-1' and titled 'Interconnection to chip', shows a grey substrate with a yellow 'TCV' (Through-Circuit Via) structure extending upwards. A green layer is on top of the TCV, and a red-outlined yellow structure is on top of the green layer. The bottom view, labeled 'I-0' and titled 'Integration to carrier', shows a grey substrate with a yellow TCV structure extending downwards. The text 'Glass Interposer' is written across the middle of both views.</p> </div> <div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p> </div> <div> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation..</p> </div>
---	--

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“In this study, an EIC substrate with embedded glass interposer for flip chip assembly is demonstrated. Glass interposers with size of 21x14 mm² and 100 μm thickness, through glass vias (TGV) of 30 μm diameter, and line/space of 3 μm/3 μm were produced. Subsequently, the glass interposer was embedded in built-up dielectric materials to form the EIC substrate. Multi-layers dielectrics were built up with filled blind vias and RDL patterns to fan-out the circuits from the embedded glass interposer.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“Silicon chips to mimic the AP (application processor, 2904 I/O in 9x9 mm²) and wide I/O chips (1.200 I/Os in 10x10 mm²) were flip-chip bonded to the EIC substrate via joints of 40 μm pitch Cu pillars and micro solder bump to form an integrated module.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“FC-EIC structure for (a) single chip integration and (b) multi-chip integration” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p>
---	---

	<div>  <p>(a) (b)</p> </div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, FIG. 2.</p> <p>“After the 12” glass interposer wafers fabricating process, the interposer wafer was singularized into individual interposer chips. Subsequently the interposer chips were attached to a temporary carrier with alignment accuracy $\leq 10\ \mu\text{m}$. Later the bonded glass interposers were embedded into a 2-layers laminate substrate using ABF typed materials.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“Figure 7 showed the cross-sectional view of the accomplished EIC-Glass substrate. The interposers were 316 successfully embedded into the carrier.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316-317].</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p>

	<p>See, e.g.:</p> <p>“FC-EIC structure for (a) single chip integration and (b) multi-chip integration” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <div> <p>The figure consists of two cross-sectional diagrams, (a) and (b), illustrating different multi-chip integration architectures. Diagram (a) shows a single chip (labeled 'Chip') mounted on a glass interposer (labeled 'Glass Interposer'). The chip is connected to the interposer via a 'High Density Interconnection' (HDI) layer. Diagram (b) shows multiple chips (labeled 'Chip') mounted on a glass interposer (labeled 'Glass Interposer'). The chips are connected to the interposer via a 'High Density Interconnection' (HDI) layer. The interposer is shown with a 'Glass Interposer' layer and a 'High Density Interconnection' layer. The chips are connected to the interposer via a 'High Density Interconnection' layer.</p> </div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, FIG. 2.</p> <p>“In order to verify the capability of the flip-chip assembly for the EIC substrate, special designed Si chips with daisy chain connected to the interconnections on the interposers were prepared. The specifications as well as the general (a) design were shown in Table 3. The EIC substrate is designed for high pin count applications. The specifications of test chips miming the real applications. Minimum line/space of 3 μm/3 μm was achieved while the device to be integrated is from single chip to multi- chips. Moreover, integrating glass interposer into EIC structure is one of the key feature of this study. The 100 μm thick 12” glass interposer wafer was successfully produced according to the specifications in Table 1. Subsequent chip singulation and attaching techniques on organic panel was also evaluated and included.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315-316].</p>
--	---

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	<p>“After finishing the build-up process, the laminated substrate with EIC structure was released from the temporary carrier and singulated into EIC substrates with size of 25 mm x 25 mm.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p> <p>“Figure 4 for forming high density interconnections between the AP test chip and the wide I/O” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>“After a series of built-up processes, the built-up EIC substrate was released from the organic panel. Surface cleaning was used to remove the residue on the released EIC substrate and a layer of PdAu was applied on the Cu pillars. Figure 6 showed the accomplished EIC-Glass substrate which was ready for further integration.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> <p>“Flip-chip bonding of the silicon chips to the EIC-Glass substrates was conducted by TCB (thermal compression bonding) with NCF (non-conductive adhesive film). The NCF is a pre-applied underfill which was laminated on the silicon wafer containing the chips to be bonded to the EIC substrate.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [317].</p> <p>“Figure 9 showed the assembled EIC-Glass module. The flip chip bonding was accomplished on EIC sheets with plurality of substrates on it by using flip chip bonder.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [317].</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the</p>
--	---

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“Later, special designed Si chips to mimic the AP (application processor, 2,904 I/O in 9x9 mm²) and wide I/O chips (1,200 I/Os in 10x10 mm²) were flip-” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“In this study, an EIC substrate with embedded glass interposer for flip chip assembly is demonstrated. Glass interposers with size of 21x14 mm² and 100 μm thickness, through glass vias (TGV) of 30 μm diameter, and line/space of 3 μm/3 μm were produced.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [314].</p> <p>“FC-EIC structure for (a) single chip integration and (b) multi-chip integration” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315].</p>
--	---

	<div> </div> <div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, FIG. 2.</p> </div> <div> <p>“In order to verify the capability of the flip-chip assembly for the EIC substrate, special designed Si chips with daisy chain connected to the interconnections on the interposers were prepared.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [315-316].</p> </div> <div> <p>“Figure 3 showed the fabricated interposers and chips to be integrated into the EIC-Glass multi-chip module. For the glass interposer shown in Figure 3, there are 5,380 TGVs in one glass interposer. A 3μm/3μm pattern on the glass interposer were shown in Figure 4 for forming high density interconnections between the AP test chip and the wide I/O test chip.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [316].</p> </div> <div> <p>“Two test chips mimic AP and Memory were built. The glass interposer was successfully integrated to the laminated substrate in a 508mm x 508mm panel format.” Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, [317].</p> </div> <div> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> </div>
--	---

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p>See, e.g.:</p> <div> </div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p>

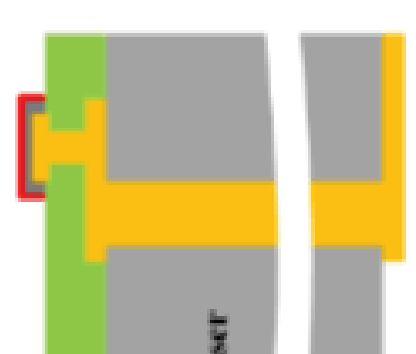
Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors. <i>See, e.g.:</i>

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration

	<div> <div> <p>Interconnection to chip</p>  <p>I-1</p> </div> <div> <p>Integration to carrier</p>  <p>I-0</p> </div> </div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p> <hr/> <div> </div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p> <p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the</p>
--	---

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of top metal pillars of the bottom package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration

<div> <p>I-1</p> <p>I-0</p> </div> <div> <p>Interconnection to chip</p> <p>Interconnection to carrier</p> </div> <div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p> </div>	<p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the plurality of metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p>See, <i>e.g.</i>:</p> <div> <p>The diagram consists of two cross-sectional views, labeled I-I and I-II. View I-I shows a central 'Glass Interposer' (grey) with a 'TCV' (Through-Circuit Via, yellow) running through it. On the left side, there are two red rectangular structures representing metal pillars. The top of the glass interposer is connected to a green layer, which is further connected to a red layer. View I-II shows the bottom of the glass interposer, which is connected to a yellow layer, which is further connected to a grey layer. The label 'Interconnection to chip' is positioned above view I-I, and 'Integration to carrier' is positioned below view I-II.</p> </div> <p>Embedded Glass Interposer for Heterogeneous Multi-Chip Integration, Table 1.</p>
--	--

Appendix A-41 - Invalidity of U.S. Patent No. 9859202 in view of Embedded Glass Interposer for Heterogeneous Multi-Chip Integration
Non-Patent Publication

	<p>To the extent Plaintiff contends that Embedded Glass Interposer for Heterogeneous Multi-Chip Integration fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

The Requirement of Future Substrate - Maker Point of View - and was published by Dyi-Chung Hu. The Requirement of Future Substrate - Maker Point of View - anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² The Requirement of Future Substrate - Maker Point of View - is a conference presentation that was published April 22, 2014. The Requirement of Future Substrate - Maker Point of View - is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within The Requirement of Future Substrate - Maker Point of View -, or otherwise rendered obvious by disclosures and teachings of The Requirement of Future Substrate - Maker Point of View -, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that The Requirement of Future Substrate - Maker Point of View - does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of The Requirement of Future Substrate - Maker Point of View - with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 patent. TopWire has

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by The Requirement of Future Substrate - Maker Point of View -, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

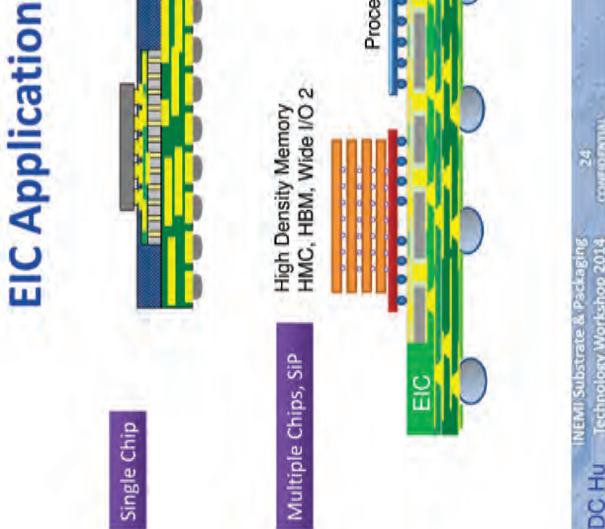
Where the chart below states that The Requirement of Future Substrate - Maker Point of View - “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to The Requirement of Future Substrate - Maker Point of View - or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding The Requirement of Future Substrate - Maker Point of View - set forth in this chart.

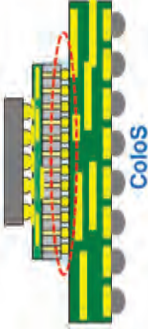
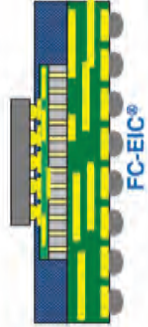
Claim 1, U.S. Patent No. 9859202

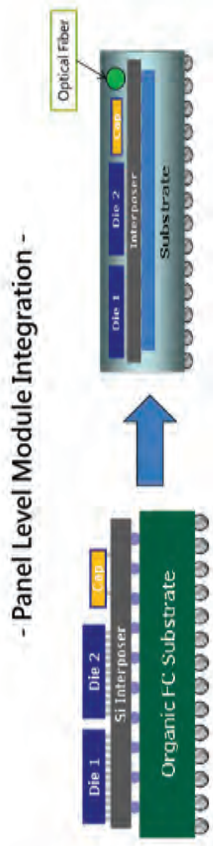
Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, a structure.</p> <p>See, e.g.:</p> <p>“Unimicron’s Solution - EIC Basic Structure” The Requirement of Future Substrate - Maker Point of View -, [22].</p>

	<div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.<p>Benefits:</p><ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.<div><p>Embedded Interposer Carrier (EIC)</p><p>DC Hu, TJ Tseng, YH Chen, WJ Lo ECTC 2013</p><p>Unimicron</p></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p> <p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, a bottom package substrate.</p> <p>See, e.g.:</p>
[1.A] a bottom package substrate;	

	<p>“EIC Application” The Requirement of Future Substrate - Maker Point of View -, [2].</p>  <p>The Requirement of Future Substrate - Maker Point of View -, at 24.</p>
--	---

	<div><div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.<p>Benefits:</p><ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.</div><div><p>Embedded Interposer Carrier (EIC)</p><p>DC-Hu, TJ Tseng, YH Chen, WJ Lo ECTC 2013</p><p>Unimicron</p></div></div> <div><p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p></div>
--	--

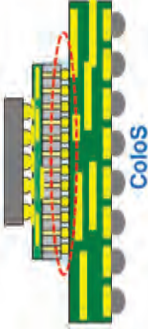
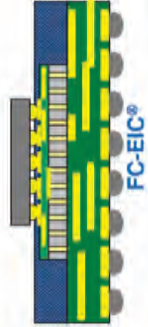
	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, Interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only <i>two</i> testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>25</div><div>CONFIDENTIAL</div><div>Unimicron</div></div></div>
	<p>The Requirement of Future Substrate - Maker Point of View -, at 25.</p>

	<div><h3>The Changing Role of Organic Substrate</h3><p>New Role of Substrate in 3D ERA</p><p>- Panel Level Module Integration -</p><p>Now</p><p>Future</p><p>DC-Hu INEMI Substrate & Packaging Technology Workshop 2014 25 CONFIDENTIAL</p><p>Unimicron</p></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 25.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, e.g.:</p> <div><p>Chip on Interposer on Substrate vs. FC-EIC®</p><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, Interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only <i>two</i> testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<p>DC-Hu INEMI Substrate & Packaging Technology Workshop 2014 CONFIDENTIAL Unimicron</p></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p>
--	---

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

	<p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only <i>two</i> testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>CONFIDENTIAL</div><div>25</div><div>Unimicron</div></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, e.g.:</p> <div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.● Benefits:<ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.<div><p>Embedded Interposer Carrier (EIC)</p><p>Silicon Interposer</p><p>DC Hu, TJ Tseng, YH Chen, WJ Lo ECTC 2013</p><p>INEMI Substrate & Packaging Technology Workshop 2014 22 CONFIDENTIAL</p><p>Unimicron</p></div></div>
---	---

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

	<p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p>

EIC Application

Single Chip

Multiple Chips, SiP

High Density Memory
HMC, HBM, Wide I/O 2

EIC

Processor

Capacitor

DC-Hu

INEMI Substrate & Packaging Technology Workshop 2014

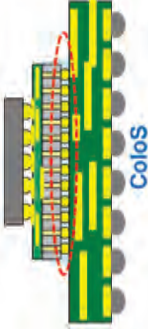
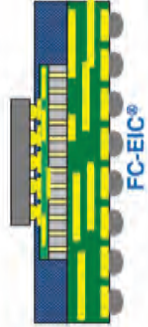
24

CONFIDENTIAL

Unimicron

The Requirement of Future Substrate - Maker Point of View -, at 24.

	<div><div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.<p>Benefits:</p><ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.</div><div><p>Embedded Interposer Carrier (EIC)</p><p>DC-Hu, TJ Tseng, YH Chen, WJ Lo ECTC 2013</p><p>Unimicron</p></div></div> <div><p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p></div>
--	--

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only <i>two</i> testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>CONFIDENTIAL</div><div>25</div><div>Unimicron</div></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>
--	---

	<div><div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.<p>Benefits:</p><ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.</div><div><p>Embedded Interposer Carrier (EIC)</p><p>DC-Hu, TJ-Tseng, YH-Chen, WJ-Lo INEMI Substrate & Packaging Technology Workshop 2014 22 CONFIDENTIAL</p><p>Unimicron</p><p>* DC-Hu, TJ-Tseng, YH-Chen, WJ-Lo ECTC2013</p></div></div> <div><p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p><p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

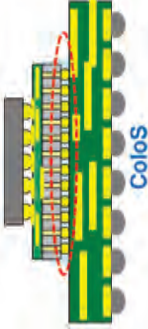
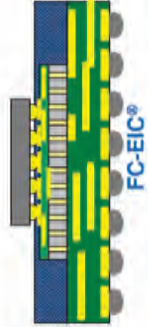
Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>
--	---

	<div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.<p>Benefits:</p><ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.<div><p>Embedded Interposer Carrier (EIC)</p><p>DC Hu, TJ Tseng, YH Chen, WJ Lo INEMI Substrate & Packaging Technology Workshop 2014</p><p>22 CONFIDENTIAL</p><p>Unimicron</p></div><p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p><p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>
--	---

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only two testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>CONFIDENTIAL</div><div>25</div><div>Unimicron</div></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>
---	--

EIC Application

Single Chip

Multiple Chips, SiP

High Density Memory
HMC, HBM, Wide I/O 2

EIC

Processor

Capacitor

DC-Hu

INEMI Substrate & Packaging
Technology Workshop 2014

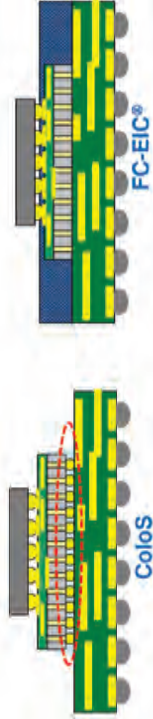
24

CONFIDENTIAL

Unimicron

The Requirement of Future Substrate - Maker Point of View -, at 24.

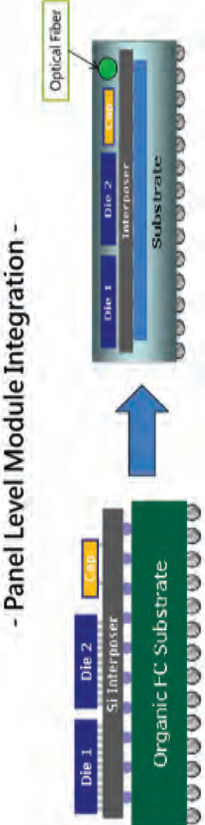
Chip on Interposer on Substrate vs. FC-EIC®



- **Chip on Interposer on Substrate: (ColoS)**
 - Interposer need double side RDL/Bumping and assembly process.
 - Four testing steps are used: Interposer, carrier, Interposer+carrier, chip+interposer +carrier.
- **FC-EIC®: Flip Chip – Embedded Interposer Carrier**
 - Interposer need to be embedded into the substrate.
 - Only *two* testing steps are used: interposer, and interposer+carrier.
 - Risk of thin wafer handling process is reduced.

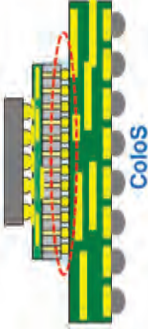
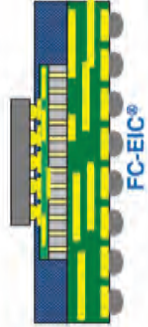
DC-Hu INEMI Substrate & Packaging Technology Workshop 2014 25 CONFIDENTIAL **Unimicron**

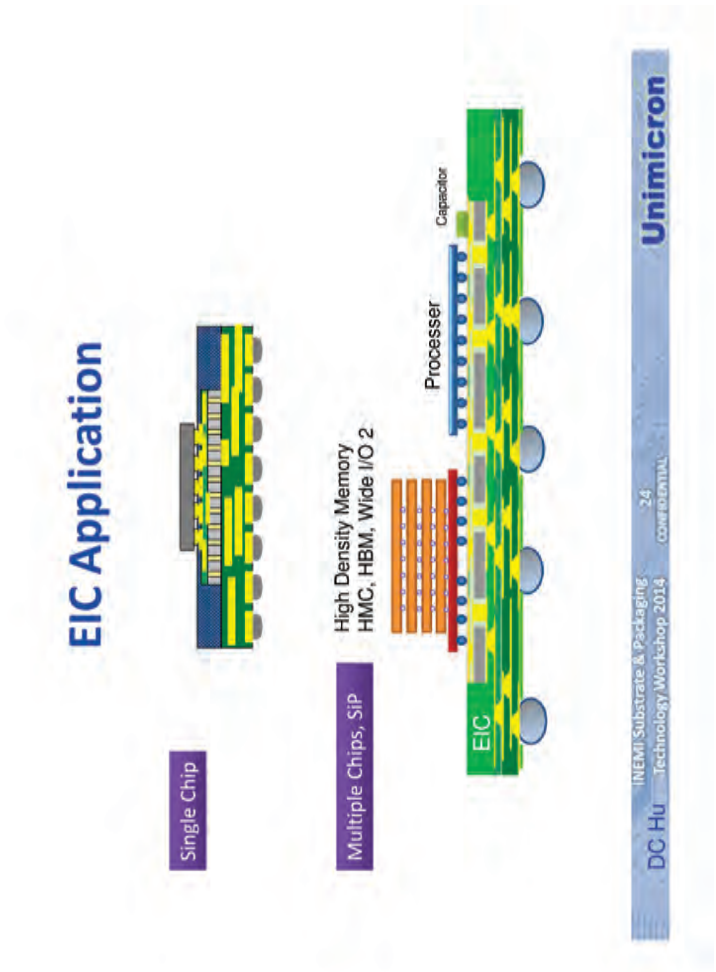
The Requirement of Future Substrate - Maker Point of View -, at 23.

	<div><h3>The Changing Role of Organic Substrate</h3><p>New Role of Substrate in 3D ERA</p><p>- Panel Level Module Integration -</p><p>Now</p><p>Future</p><p>DC-Hu INEMI Substrate & Packaging Technology Workshop 2014 25 CONFIDENTIAL</p><p>Unimicron</p><p>The Requirement of Future Substrate - Maker Point of View -, at 25.</p><p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>
--	--

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only two testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>CONFIDENTIAL</div><div>25</div><div>Unimicron</div></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p>See, e.g.:</p> <div><h3>EIC Application</h3><p>Single Chip</p><p>Multiple Chips, SiP</p><p>High Density Memory HMC, HBM, Wide I/O 2</p><p>Processor</p><p>Capacitor</p><p>EIC</p><p>DC Hu INEMI Substrate & Packaging Technology Workshop 2014 24 CONFIDENTIAL</p><p>Unimicron</p></div>
--	---

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

	<p>The Requirement of Future Substrate - Maker Point of View -, at 24.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

EIC Application

Single Chip

Multiple Chips, SiP

High Density Memory
HMC, HBM, Wide I/O 2

EIC

Processor

Capacitor

DC-Hu

INEMI Substrate & Packaging Technology Workshop 2014

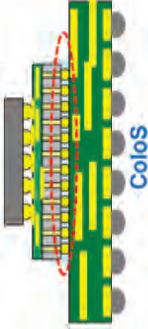
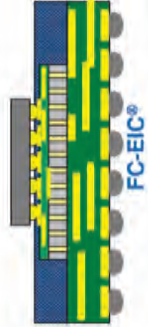
24

CONFIDENTIAL

Unimicron

The Requirement of Future Substrate - Maker Point of View -, at 24.

	<div><div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.<p>Benefits:</p><ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.</div><div><p>Embedded Interposer Carrier (EIC)</p><p>DC-Hu, TJ Tseng, YH Chen, WJ Lo ECTC 2013</p><p>Unimicron</p></div></div> <div><p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p></div>
--	--

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only <i>two</i> testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>25 CONFIDENTIAL</div><div>Unimicron</div></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p>
--	--

	<div><h3>The Changing Role of Organic Substrate</h3></div> <div><p>New Role of Substrate in 3D ERA</p></div> <div><p>- Panel Level Module Integration -</p></div> <div></div> <div><p>Now</p></div> <div><p>Future</p></div> <div><p>DC-Hu INEMI Substrate & Packaging Technology Workshop 2014 25 CONFIDENTIAL Unimicron</p></div> <div><p>The Requirement of Future Substrate - Maker Point of View -, at 25.</p></div> <div><p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>
---	---

EIC Application

Single Chip

Multiple Chips, SiP

High Density Memory
HMC, HBM, Wide I/O 2

EIC

Processor

Capacitor

DC-Hu

INEMI Substrate & Packaging Technology Workshop 2014

24

CONFIDENTIAL

Unimicron

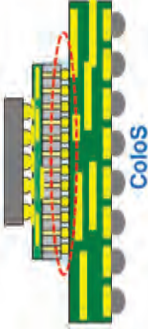
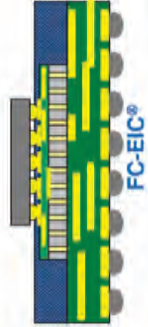
The Requirement of Future Substrate - Maker Point of View -, at 24.

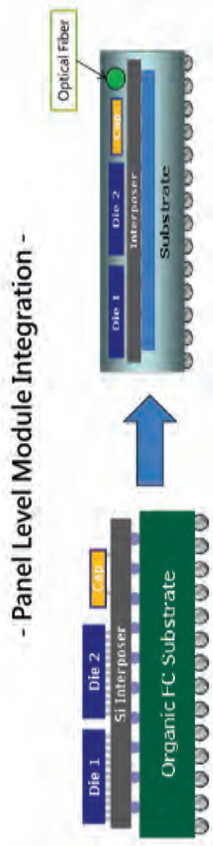
Unimicron's Solution - EIC Basic Structure

- Combine interposer and organic substrate.
- Eliminates the solder joints between interposer and organic substrate.
- Benefits:
 - Layer reduction compare with conventional organic substrate.
 - Alternative solution for high density SiP.
 - Cost reduction by interposer/carrier integration.



The Requirement of Future Substrate - Maker Point of View -, at 22.

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only <i>two</i> testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>25</div><div>CONFIDENTIAL</div><div>Unimicron</div></div></div> <div><p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p></div>
--	---

	<div><h3>The Changing Role of Organic Substrate</h3><p>New Role of Substrate in 3D ERA</p><p>- Panel Level Module Integration -</p><p>Now</p><p>Future</p><p>DC-Hu INEMI Substrate & Packaging Technology Workshop 2014 25 CONFIDENTIAL</p><p>Unimicron</p><p>The Requirement of Future Substrate - Maker Point of View -, at 25.</p><p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>

EIC Application

Single Chip

Multiple Chips, SiP

High Density Memory
HMC, HBM, Wide I/O 2

Processor

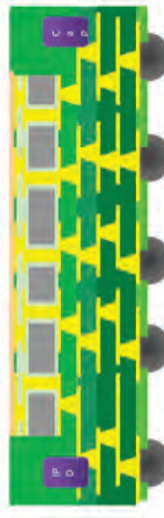
Capacitor

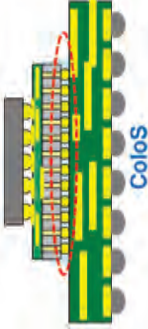
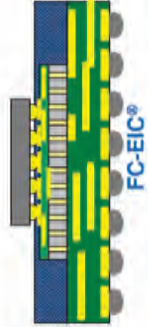
EIC

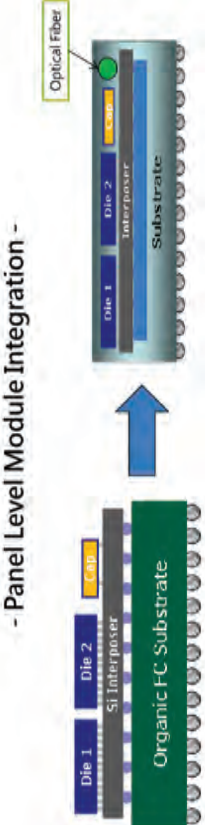
DC-Hu INEMI Substrate & Packaging Technology Workshop 2014 24 CONFIDENTIAL

Unimicron

The Requirement of Future Substrate - Maker Point of View -, at 24.

	<div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.<p>Benefits:</p><ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.<div><p>Embedded Interposer Carrier (EIC)</p><p>DC-Hu, TJ Tseng, YH Chen, WJ Lo ECTC 2013</p><p>Unimicron</p></div></div> <div><p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p></div>
--	--

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div><div><p>ColoS</p></div><div><p>FC-EIC®</p></div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only <i>two</i> testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>25</div><div>CONFIDENTIAL</div><div>Unimicron</div></div></div> <div>The Requirement of Future Substrate - Maker Point of View -, at 23.</div>
--	--

	<div><h3>The Changing Role of Organic Substrate</h3><p>New Role of Substrate in 3D ERA</p><p>- Panel Level Module Integration -</p><p>Now</p><p>Future</p><p>DC-Hu INEMI Substrate & Packaging Technology Workshop 2014 25 CONFIDENTIAL</p><p>Unimicron</p></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 25.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, <i>e.g.</i>:</p>

EIC Application

Single Chip

Multiple Chips, SiP

High Density Memory
HMC, HBM, Wide I/O 2

EIC

Processor

Capacitor

DC-Hu

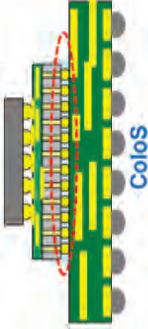
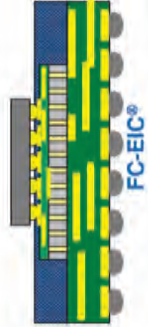
INEMI Substrate & Packaging Technology Workshop 2014

24

CONFIDENTIAL

Unimicron

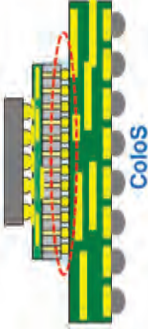
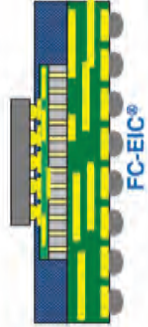
The Requirement of Future Substrate - Maker Point of View -, at 24.

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only <i>two</i> testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>CONFIDENTIAL</div><div>25</div><div>Unimicron</div></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

Claim 4, U.S. Patent No. 9859202

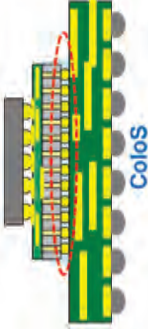
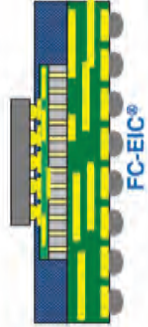
Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<div><div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div><div><p>ColoS</p></div><div><p>FC-EIC®</p></div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only two testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>CONFIDENTIAL</div><div>25</div><div>Unimicron</div></div></div><p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p><p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of top metal pillars of the bottom package substrate are connected to the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

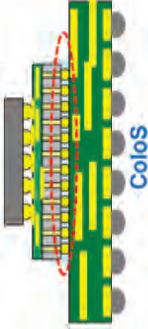
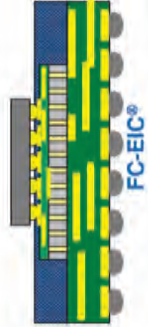
	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only two testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>CONFIDENTIAL</div><div>25</div><div>Unimicron</div></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-42 - Invalidity of U.S. Patent No. 9859202 in view of The Requirement of Future Substrate - Maker Point of View - - Non-Patent Publication

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pads of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>The Requirement of Future Substrate - Maker Point of View - discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

	<div><div><h3>Unimicron's Solution - EIC Basic Structure</h3><ul style="list-style-type: none">● Combine interposer and organic substrate.● Eliminates the solder joints between interposer and organic substrate.<p>Benefits:</p><ul style="list-style-type: none">● Layer reduction compare with conventional organic substrate.● Alternative solution for high density SiP.● Cost reduction by interposer/carrier integration.</div><div><p>Embedded Interposer Carrier (EIC)</p><p>DC-Hu, TJ Tseng, YH Chen, WJ Lo ECTC 2013</p><p>Unimicron</p></div></div> <div><p>The Requirement of Future Substrate - Maker Point of View -, at 22.</p></div>
--	--

	<div><h3>Chip on Interposer on Substrate vs. FC-EIC®</h3><div></div><ul style="list-style-type: none">● Chip on Interposer on Substrate: (ColoS)<ul style="list-style-type: none">● Interposer need double side RDL/Bumping and assembly process.● Four testing steps are used: Interposer, carrier, Interposer+carrier, chip+interposer +carrier.● FC-EIC®: Flip Chip – Embedded Interposer Carrier<ul style="list-style-type: none">● Interposer need to be embedded into the substrate.● Only two testing steps are used: interposer, and interposer+carrier.● Risk of thin wafer handling process is reduced.<div><div>DC-Hu</div><div>INEMI Substrate & Packaging Technology Workshop 2014</div><div>CONFIDENTIAL</div><div>25</div><div>Unimicron</div></div></div> <p>The Requirement of Future Substrate - Maker Point of View -, at 23.</p> <p>To the extent Plaintiff contends that The Requirement of Future Substrate - Maker Point of View - fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

IPC-4761 Design Guide for Protection of Printed Board Via Structures (“IPC-4761”) was published by Associate Connecting Electronics Industries (IPC). IPC-4761 anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ‘202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² IPC-4761 is an industry standard document that was published May 7, 2008. IPC-4761 is therefore prior art to the ‘202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within IPC-4761, or otherwise rendered obvious by disclosures and teachings of IPC-4761, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that IPC-4761 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of IPC-4761 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by IPC-4761, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

Where the chart below states that IPC-4761 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to IPC-4761 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding IPC-4761 set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, IPC-4761 discloses, either expressly or inherently, a structure.</p> <p>See, <i>e.g.</i>:</p> <p>“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p>
[1.A] a bottom package substrate;	IPC-4761 discloses, either expressly or inherently, a bottom package substrate.

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p><i>See, e.g.:</i></p> <p>“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>IPC-4761 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p>

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>IPC-4761 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>

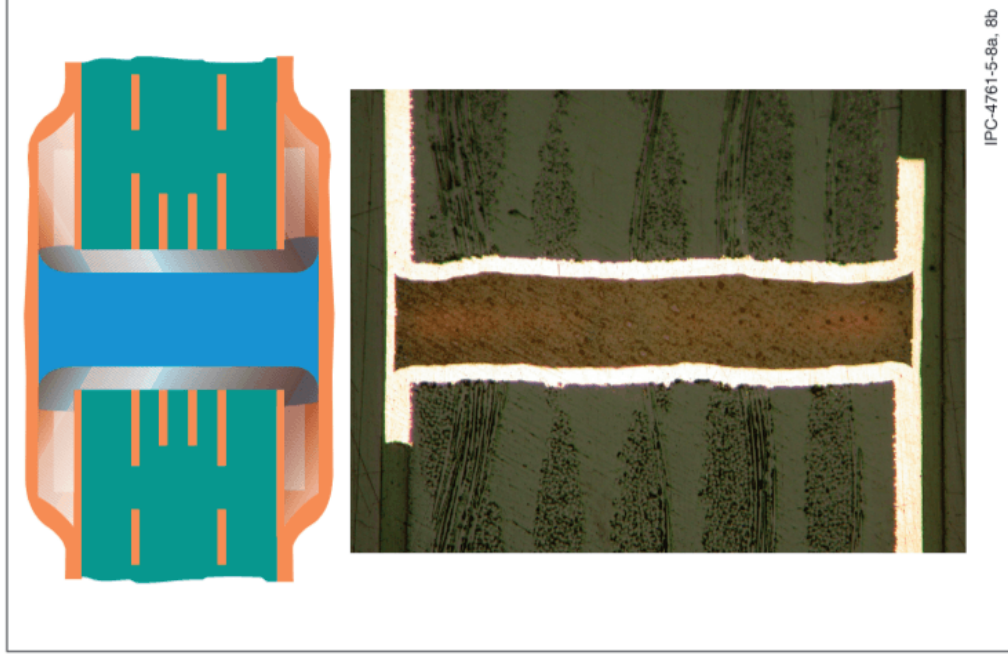


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>IPC-4761 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p>

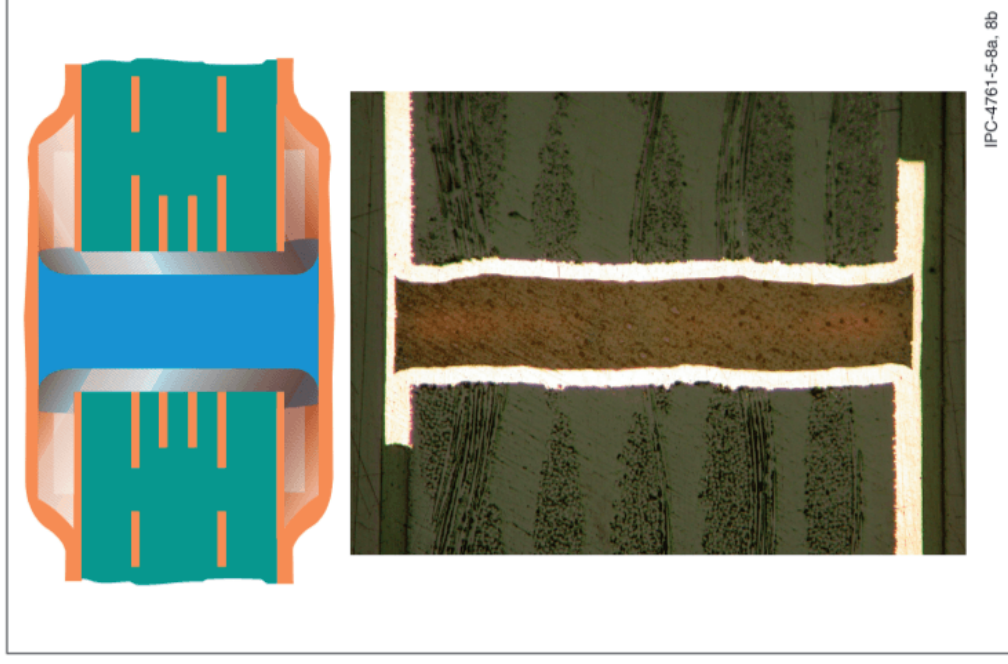


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>IPC-4761 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p> <p>“Conductive hole plugging materials are polymer-based and filled with metal particles, usually silver or copper.” IPC-4761, [11].</p> <p>“Fill or Plug Adhesion When required, materials must not separate from any metallized surface” IPC-4761, [12].</p>

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>“Plating - When required, capable of being plated uniformly • Plating adhesion - Minimize separation from the fill material during subsequent processing when required.” IPC-4761, [12].</p> <p>“A via with material applied into the via targeting a full penetration and encapsulation of the hole (see Figure 5-5).” IPC-4761, [15].</p> <p>“Via Metallization When vias are to be solder coated, before they are coated the plug of material in the hole can become loose as the solder reflows or melts during soldering processes.” IPC-4761, [16].</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>IPC-4761 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“Filled and Capped Via (Type VII Via) A Type V via with a secondary metallized coating covering the via (see Figure 5-8). The metallization is on both sides: Process: Metallized coating over Type V. Applicable where high density features are required. Benefits: Via-In-Pad and Ball-on-Via pad. Via stacking. Applicable where high density features are required. Benefits useful in sequential lamination processes.” IPC-4761, [at 9].</p>

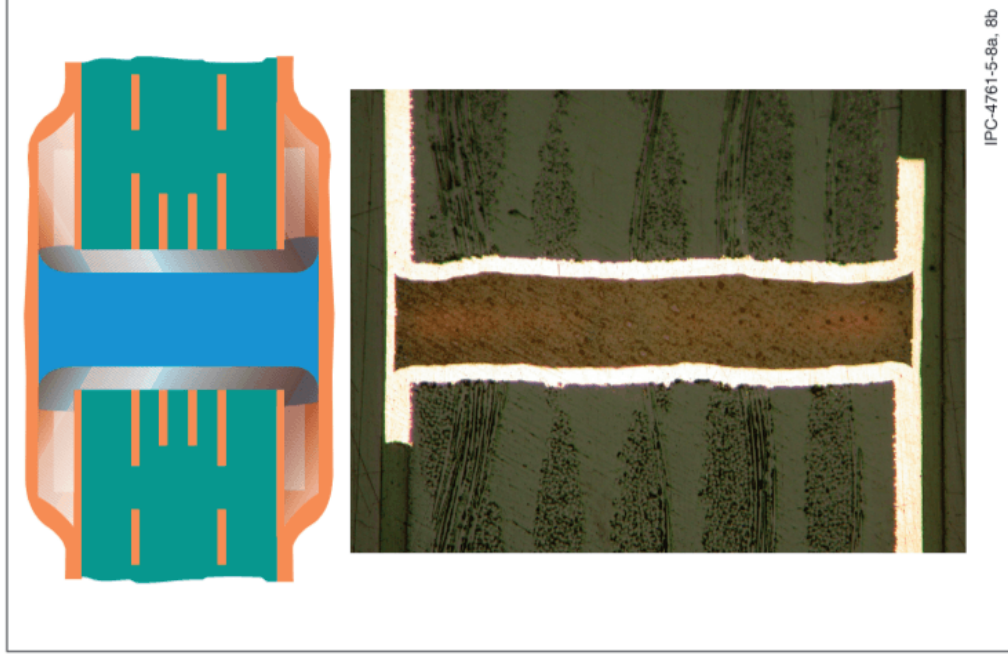


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>“Concerns: Adhesion of the metallized coating to the via fill and copper pad. Copper thickness. The planarity between the fill material and the copper surface. CTE mismatch between the fill material and metallization resulting in air gap (fill material shrinkage). Less than 100% via fill may result in a metallized cap that is too thin or a dimple that can also cause entrapped air resulting in voids in BGA solder joints. Pinholes in the metallized coatings result in non-solderable areas of a land where the capped via is intended for a BGA solder joint. Reduced solder volume is also a concern with dimples.” IPC-4761, [at 10].</p>
--	---

Table 5-1 Application Guidelines for Via Protection Types ¹										
Description (Type)	Applications									
	Before Final Finish	After Non-Melting Metal Final Finish	Prevent air leakage in ICT (Vacuum Seal) ²	Keeping chemistry or solder from passing through the via	Keeping chemistry or solder from being trapped in the via	Dielectric protection of via land	Fill holes in cores prior to lamination	Improves surface planarity	Best For thermal conductivity ³	Prevent migration of solder, adhesives or encapsulants into vias
Tented - Single-Sided (Ia)				NOT RECOMMENDED ⁵						
Tented - Double-Sided (Ib)	X	X	X	X	X	X				X
Tented and Covered - Single-Sided (IIa)				NOT RECOMMENDED ⁵						
Tented and Covered - Double-Sided (Ib)	X	X	X	X	X	X				X
Plugged - Single-Sided (IIa)				NOT RECOMMENDED ⁵						
Plugged - Double-Sided (IIb)	X	X	X	X	X	X		X		X
Plugged and Covered - Single-Sided (IVa)				NOT RECOMMENDED ⁵						
Plugged and Covered Double-sided (IVb)	X	X	X	X	X	X				X
Filled (fully plugged) (V)	X	X	X	X	X		X	X	X	X
Filled and Covered (VI)	X	X	X	X	X	X				X
Filled and Capped (VII) ²	X	X	X	X	X		X	X	X	X

1) Descriptions of specific types of via protection are provided in 5.1 through 5.7.

2) Not recommended over melting metals.

3) It is recommended to use a thermally conductive hole filling ink (e.g. silver ink).

4) When specifying Via-in-Pad, it is recommended that Type VII via protection be used.

5) See 3.4 for concerns associated with single sided via protection.

IPC-4761, Table 5-1.

“this document does recognize manufacturing processes where solder mask flows into the hole during liquid solder mask application, without intending to provide complete coverage or protection, and may result in partial plugging. This is not acceptable with bare copper surface finishes.” IPC-4761, [at 10].

“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,	<p>IPC-4761 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

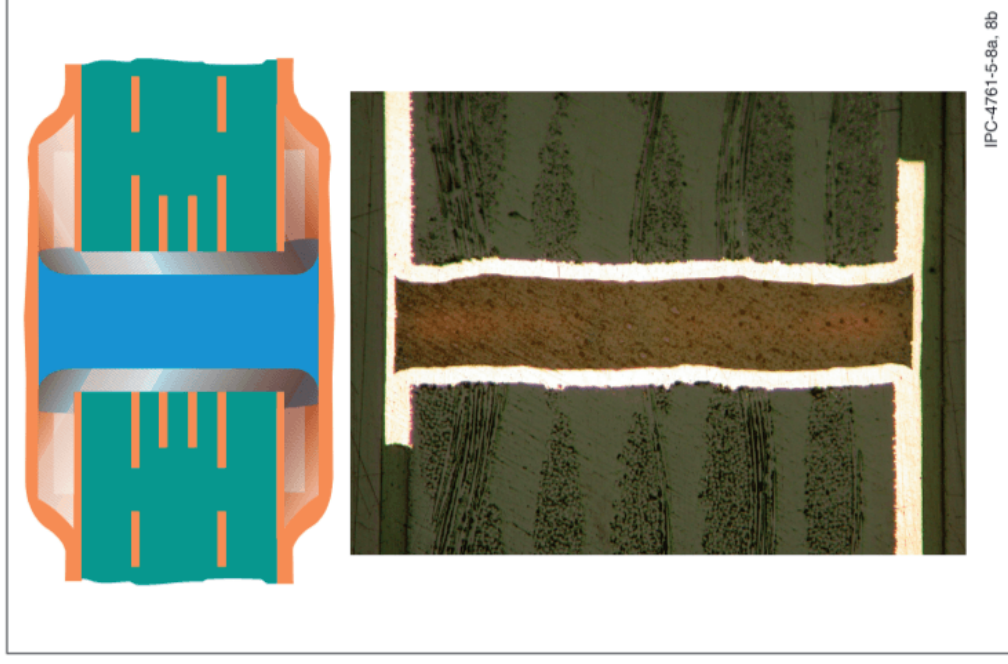


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>IPC-4761 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

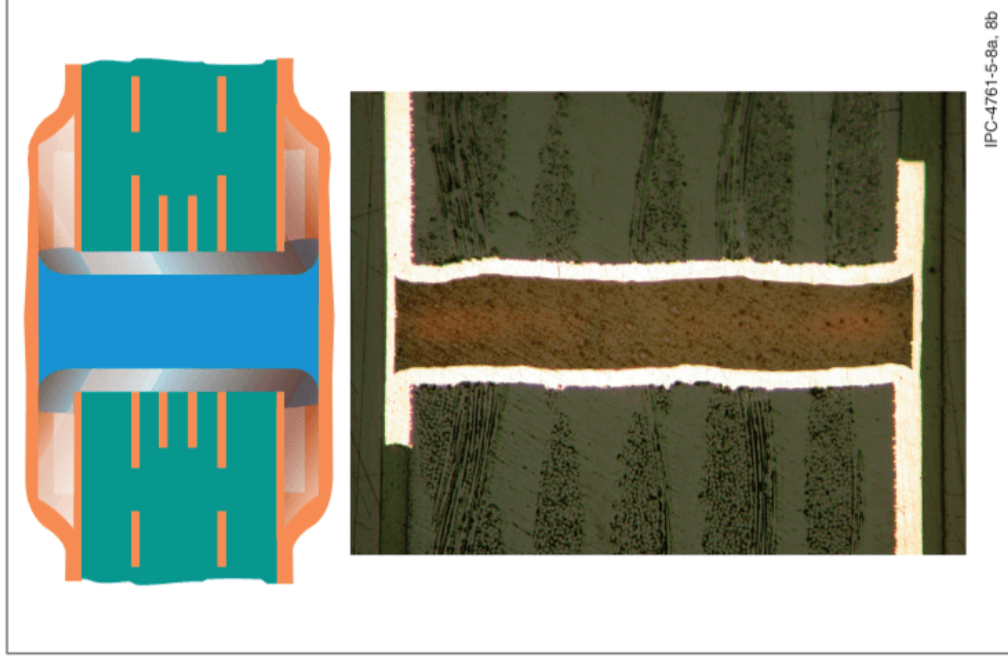


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>IPC-4761 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

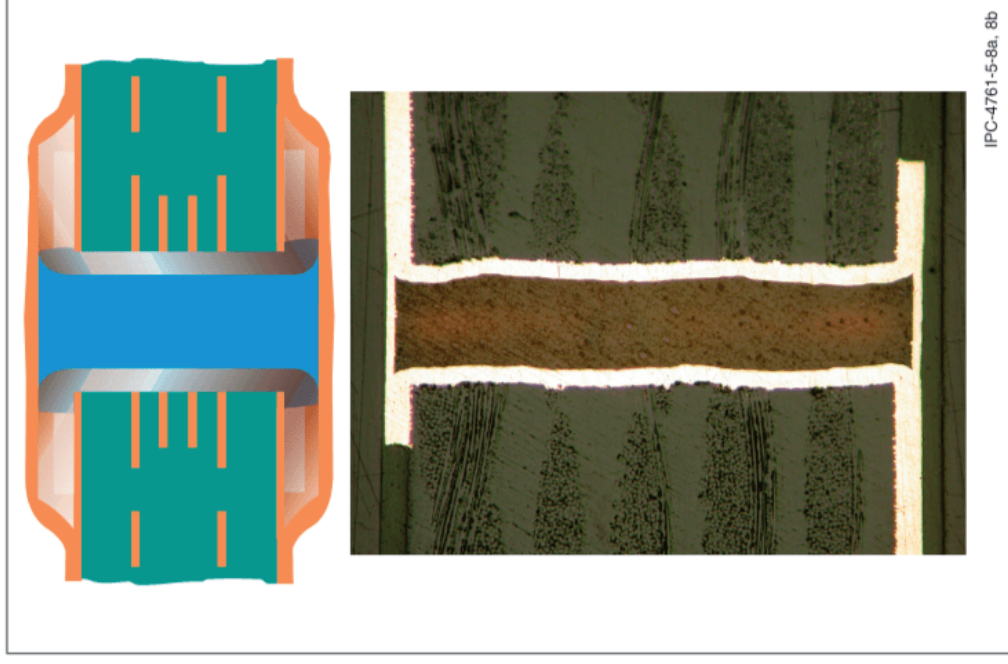


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>IPC-4761 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein

IPC-4761 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.

See, e.g.:

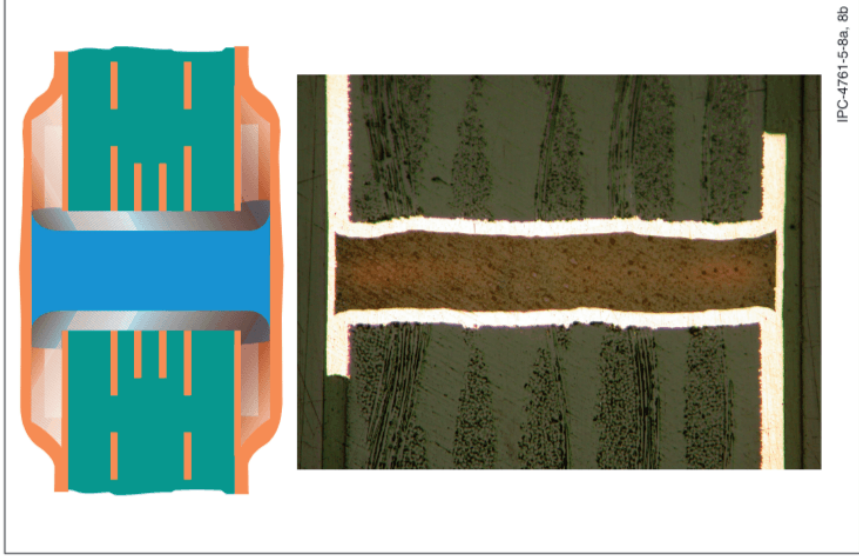


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>IPC-4761 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

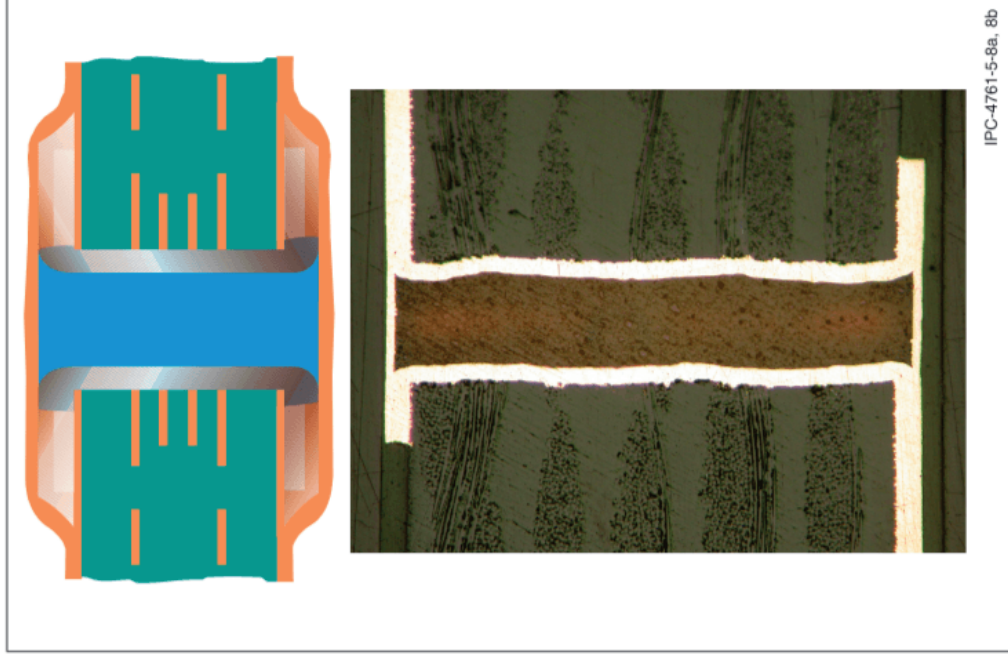


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>IPC-4761 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

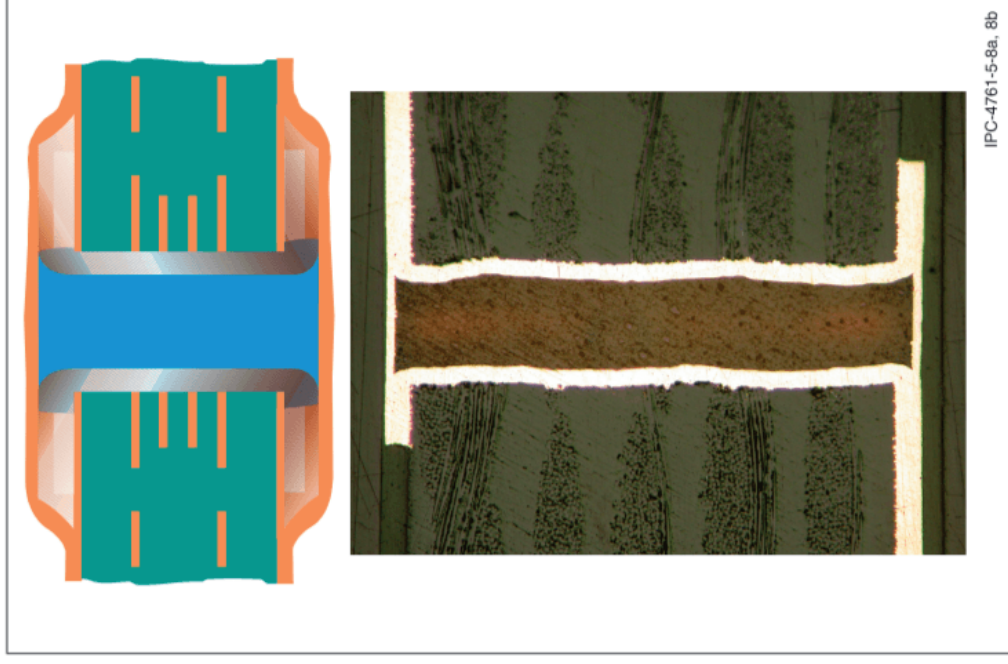


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>IPC-4761 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>

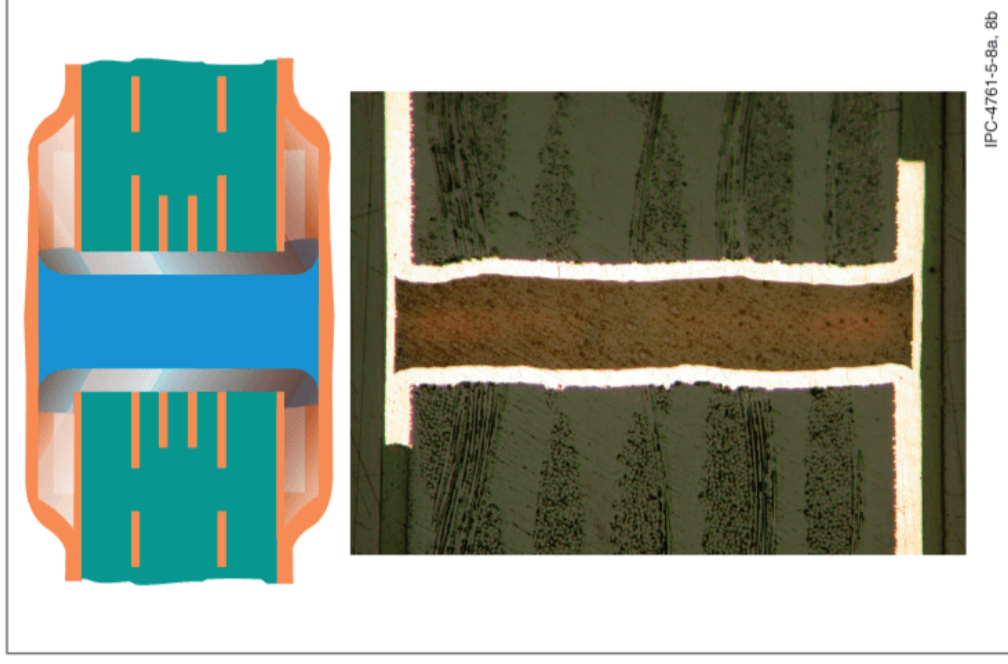


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>IPC-4761 discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p>

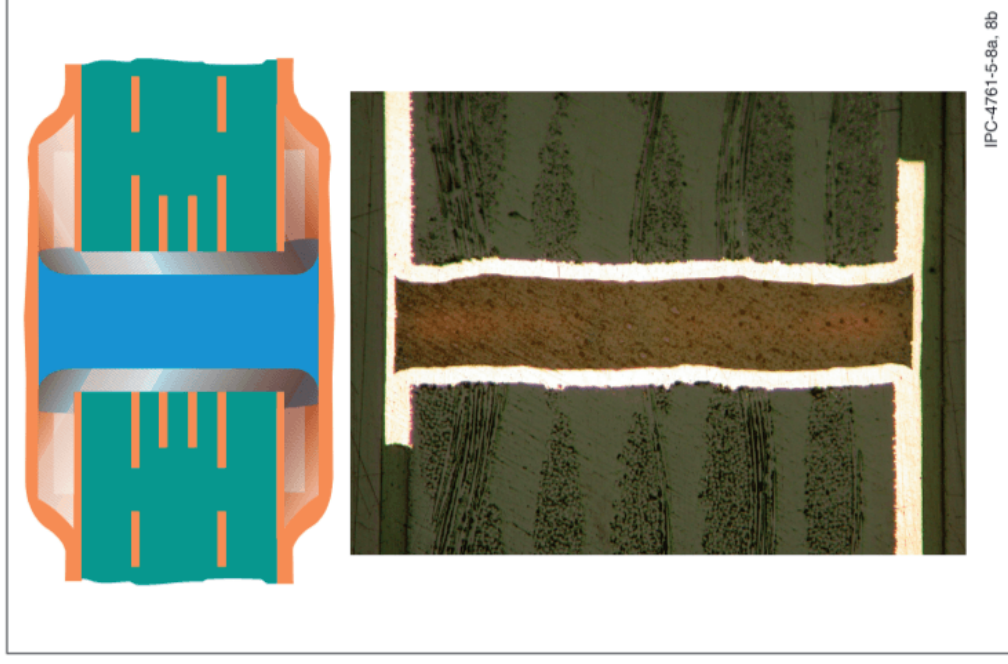


Figure 5-8 Examples of Type VII Filled and Capped Via

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>IPC-4761, FIG. 5-8.</p> <p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p>	<p>IPC-4761 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p>

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>IPC-4761 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p>

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to the bottom ends of the plurality of metal pillars of the bottom package substrate via the plurality of bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>IPC-4761 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.” IPC-4761, [8].</p>

Appendix A-43 - Invalidity of U.S. Patent No. 9859202 in view of IPC-4761 - Non-Patent Publication

	<p>To the extent Plaintiff contends that IPC-4761 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART
Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module was published by Christian Kriedl. Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory². Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module is a dissertation that was published December 31, 2011. Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, or otherwise rendered obvious by disclosures and teachings of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p>

	<p>“By enlarging the silicon size of a DEPFET sensor, while keeping the size of the active area constant, space can be created for directly mounting the steering and readout chips onto the detector silicon and for routing the interconnection and power traces. On a highly integrated and densely populated area of such all-silicon modules, the routing of a huge amount of signal and power connections is a difficult task. The components, located on the detector silicon, must not influence the detector or the electronics operation. Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged 3.2. WAFER THINNING 23 quickly. A high capacitive load on the drain lines is not as limiting as on the control lines, because the DEPFET is operated in drain read-out mode, yielding to a current signal. Control, data and power lines have to be connected directly to the silicon, the module is mounted on a support structure, which is also used for actively cooling the readout chips. By thinning the silicon of the detector and the chips, the material budget of the module can be reduced furthermore. For interconnecting the chips with the detector module, the flip chip technology has been chosen.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32-33].</p> <p>“Figure 3.15 shows a drawing of the two barrels without the steering and readout chips. The ladders of both layers are 15.4mm wide, while the outer layer has much longer ladders. Overlapping ladders cover the inactive part of the support frame carrying the steering chips. The active area will be thinned to 75µm using the technology presented in chapter 3.2 to reduce the multiple scattering effects. The support frame is 400 µm thick and will be 38 88 CHAPTER 3. THE DEPFET AS A VERTEX DETECTOR Figure 3.15: The two layers of Belle II PXD with the longer outer layer. The gray area marks the active region containing the DEPFET pixel cells. [10] Pixel size µm² 50 x 55 and 50 × 60 Layer Radius Number of</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>(mm) ladders 1 14 8 Length (mm) 2×68 Ladder active length(mm) $2 \times 45 \ 2 \ 22 \ 12 \ 2 \times 85 \ 2 \times 62 \ 50 \times 70$ and 50×85 Table 3.3: Belle II DEPFET vertex detector layer configuration. partially thinned. The $75\mu\text{m}$ thin active area is mechanically more robust and allows better position resolution than the $50\mu\text{m}$ option. Charge generated by an incident particle passing through the thicker detector is shared between more pixels. [28] Table 3.3 shows a summary of the ladder dimensions. The width of the modules is 15.4mm with a 2.2mm wide balcony for the steering chips on one side and a $400\mu\text{m}$ wide support frame on the other side of the module. The active area has a width of 12.8mm. 256 pixel columns can be realized with the given pixel width of $50\mu\text{m}$. Both layers will have 1600 pixel rows with two different pixel pitches. Smaller pixels are located close to the beam collision point, while larger pixels are used towards the end of stave. The outer layer is build with $70\mu\text{m}$ and $85 \ \mu\text{m}$ long pixels, whereas $55\mu\text{m}$ and $60\mu\text{m}$ short pixels are used on the inner layer [29] to keep the occupancy low.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [47-49].</p> <p>“Figure 3.17 shows the mounting scheme with the beam pipe in the middle and two half barrels containing both layers. The outer layer is mounted on the support structure with the chips facing outwards and the inner layer facing towards the beam pipe. The support structure itself is mounted on the beam pipe, while one end is fixed and the other end floats on the beam pipe to compensate for thermal expansion. The ladders float on the structure using a slot instead of a hole for screwing the silicon to the structure. The kapton flex cable of 6mm width is affixed on the support structure for stress relief and to keep the electrical connection from the kapton to the silicon module stable. Between the kapton cables are the pipes for the coolant connected to the support structure. After everything is assembled on the two halves, they are mounted on the beam pipe. 40” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [49-50].</p>
--	--

	<p>“The flip-chip bonding process offers advantages over the wire bonding connection, such as a lower area requirement, shorter paths between substrate and chip, lower inductance and a fast parallel bonding process. The pads of substrate and chip are placed face-to- face and brought into contact using a conductive material. Flip-chip bonding needs less area on the substrate, because the landing pads are covered by the chip, whereas wire bonding needs space for wire looping and for the destination pads located around the chip. The path between source and destination pads is only a few tens of micrometers long, whereas bonding wires are in the range of hundreds or thousands of micrometers. Different conductive materials can be used to form the interconnection, e.g. gold-stud bumps, solder bumps, indium bumps or conductive glues and films. Gold-stud bumps can be easily placed with a modified wire bonder, but require high bonding forces in the range of 40-60gr/bump and temperatures up to 320 °C. Indium can be bonded with 60°C and <10gr/bump, but the bumps are deposited by evaporation, which needs additional preprocessing. Solder bumps can be deposited in many ways (see chapter 6.4), including a flexible single ball placement. Solder processing parameters range between those of gold and indium bumps. Glues and foils share the advantage of supporting the mechanical stability of an assembly by their adhesive properties. They require lower temperatures and forces for curing the adhesive, but have a higher resistivity and require larger pads and pitches.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [91].</p> <p>“The first test vehicles used were made of glass substrates with gold coated structures. They included 4 daisy chain connections of 16 bumps each, with probe pads for connectivity tests. Single bump and double bump approaches have been tested. Single bump assemblies use bumps on the chip only, while bumps on the chip and on the substrate are called double bump. The same flip-chip parameters have been used with all assemblies. A pressure of 80gr/bump</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>and 350°C for 120 seconds forms the connection during the thermocompression bonding. Both assembly types showed successful bonds on all bumps, determined by the electrical connection. A resistivity of 13 ± 0.2 has been measured for all snake structures, which includes the trace resistances. The bond quality has been checked by shearing the chip off the substrate. The bond interface broke equally on the chip and on the substrate side of the bump, indicating that thermosonic bumping and thermocompression flip-chip bonding created equally good bonds.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [100].</p> <p>“The gold dummy chips were sufficient for the first test, but the Switcher3 and DCD chips, as well as the DEPFET module are based on silicon substrates with aluminum structures and have a higher pad count. The higher pad count results in a high pressure applied to the chip and substrate, which can possibly cause mechanical defects on the thinned DEPFET modules. A new set of test vehicles has been developed during the thesis, to adopt the bumping and the flip-chip processes to aluminum structured devices. The dummy chips should be mechanically as similar as possible to the real chips, although they were manufactured in a different technology and without active devices. 6” wafers with a single aluminum layer have been used to produce the test dummies. They were structured with a wafer size mask, which allowed to include a full size ILC module design as a mechanical demonstrator together with the DCD and Switcher dummy chips.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [100-101].</p>
[1.A] a bottom package substrate;	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<p>“By enlarging the silicon size of a DEPFET sensor, while keeping the size of the active area constant, space can be created for directly mounting the steering and readout chips onto the detector silicon and for routing the interconnection and power traces. On a highly integrated and densely populated area of such all-silicon modules, the routing of a huge amount of signal and power connections is a difficult task. The components, located on the detector silicon, must not influence the detector or the electronics operation. Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged 3.2. WAFER THINNING 23 quickly. A high capacitive load on the drain lines is not as limiting as on the control lines, because the DEPFET is operated in drain read-out mode, yielding to a current signal. Control, data and power lines have to be connected directly to the silicon, the module is mounted on a support structure, which is also used for actively cooling the readout chips.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32-33].</p> <p>“The DEPFET uses pixel sizes of $25\mu\text{m} \times 25\mu\text{m}$, which allows a binary resolution of $25\mu\text{m}/\sqrt{12} \approx 7\mu\text{m}$. The pixel signal is compared with a threshold value to detect a hit at the binary read-out scheme. Only this hit information is stored. A resolution of $3.5\mu\text{m}$ is achieved with the $50\mu\text{m}$ thin detector by interpolation using the center-of-gravity method and a signal-to-noise ratio of 40 [12]. Figure 3.9 shows the innermost layer. The modules are placed as close as possible to the beam pipe, at a radius of 1.5cm. The steering chips are at the long side of the matrix and the readout chips are at the short end. The modules are overlapping, to</p> <p>28 80 CHAPTER 3. THE DEPFET AS A VERTEX DETECTOR active DEPFET area (~50μm thick) SWITCHER Steering chips CURO Readout chips Figure 3.9: ILC inner layer modules placed around the beam pipe with steering and read- out chips. [12] Layer Radius</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>Number of Ladder length” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [37-38].</p> <p>“The flip-chip bonding process offers advantages over the wire bonding connection, such as a lower area requirement, shorter paths between substrate and chip, lower inductance and a fast parallel bonding process. The pads of substrate and chip are placed face-to- face and brought into contact using a conductive material. Flip-chip bonding needs less area on the substrate, because the landing pads are covered by the chip, whereas wire bonding needs space for wire looping and for the destination pads located around the chip. The path between source and destination pads is only a few tens of micrometers long, whereas bonding wires are in the range of hundreds or thousands of micrometers. Different conductive materials can be used to form the interconnection, e.g. gold-stud bumps, solder bumps, indium bumps or conductive glues and films.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [91].</p> <p>“The substrate pads have to be cleaned of remaining solder prior soldering a new chip. The solder jetting machine has been ordered with an additional desoldering head. It allows a selective removal of solder balls. Its working principle is shown in figure 6.14. The substrate is pre-heated to a temperature below the melting point to assist a selective melting of solder balls. The solder ball’s temperature is increased above the melting point by hot nitrogen gas blown through a heating nozzle (A). The head moves then downwards and vacuum is applied to the tapered capillary. A sideways movement pushes the solder ball to the pads edge and the vacuum removes it (B).” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [99].</p>
--	--

	<p>“The DEPFET matrixes of the PXD5 production for characterization of the ILC type designs were tested in setups with the read-out and steering chips wire bonded to the matrix. The novel all-silicon module approach, with flip-chip bonded chips, has not yet been demonstrated with active components. The first DEPFET matrixes with flip-chip interconnection of the read-out and steering chips were included on the PXD6 wafer run. Different matrix design are used to evaluate the optimal pixel layout for the Belle II vertex detector. Most of the matrixes are still wire bondable for a faster comparison of different matrix types with the same steering and readout chips. They are bonded to PCBs, which can be plugged into the read-out system. Some matrix types have flip-chip footprints on the detector silicon, to build all-silicon modules. Most of the flip-chip matrixes have an active area of 128×16 pixels, which is sufficient for evaluation of the flip-chip module performance. Large matrixes with more than 768×120 pixels are included on the wafer too, to gain information about the production yield and the performance of large matrixes. The wafers will be partially thinned with the technology presented in 3.2. The PXD6 matrixes are the first thinned and bump bondable DEPFET matrixes. Besides the DEPFET design evaluation, work on the mechanical integration of the modules in the Belle II detector is necessary. A support carrier is needed to mount the modules in two concentric layers around the beam pipe. The data signals and power supply lines have to be routed on a cable through the Belle detector to the DEPFET ladders. The cable has to be securely connected to the modules. Power dissipated by chips and DEPFET transistors has to be removed by cooling and the thermal expansion of the material has to be taken into account for the mechanical designs. The signal routing and cable mounting on the module with a constrained size require training. Two” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [115-117].</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>“The PXD6 production provides two poly-silicon layers for the DEPFET gate and clear- gate structures. Two aluminum metal layers with a sheet resistance of 30m/□ are available for routing the power supplies and the data signals. Gold stud bumps have to be used to interconnect the flip-chip devices, as the pad metallization is aluminum and an additional under bump metallization is not available. Since the test structures presented in chapter 6.5.5 couldn’t provide information on the insulator stability and the impact of bumping on pads with traces routed below, this routing option was avoided. The traces are routed in between the bumps with at least 7μm distance to pads, to accommodate the pad deformation during uncentered bump placement. A bump pad is designed with both metal layers, as this design showed a good bondability on the bumping test structures. Poly-silicon is forming a barrier layer below each bump pad and thereby prohibits shorts between the bulk material and the metal layers.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [119].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<p>“The chips can be directly connected to the matrix by wire- or bump-bond techniques or by an intermediate layer of PCB¹, silicon or a kapton based flex board.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [31].</p> <p>“The All-Silicon Model By enlarging the silicon size of a DEPFET sensor, while keeping the size of the active area constant, space can be created for directly mounting the steering and readout chips onto the detector silicon and for routing the interconnection and power traces. On a highly integrated and densely populated area of such all-silicon modules, the routing of a huge amount of signal and power connections is a difficult task. The components, located on the detector silicon, must not influence the detector or the electronics operation. Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32].</p> <p>“The flip-chip bonding process offers advantages over the wire bonding connection, such as a lower area requirement, shorter paths between substrate and chip, lower inductance and a fast parallel bonding process. The pads of substrate and chip are placed face-to- face and brought into contact using a conductive material. Flip-chip bonding needs less area on the substrate, because the landing pads are covered by the chip, whereas wire bonding needs space for wire looping and for the destination pads located around the chip.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [91].</p> <p>“The DCDB adapter (figure 6.27) allows to connect all 128 drains of a matrix. The digital output signals are routed to the DCDB-RO converter chip, which is located close to the DCDB on the same wire bond adapter. It converts the DCDB’s single ended signals to differential pairs, which can be wire bonded to a PCB. Additional sense pads allow measurements of the</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>supply voltages close to the chips, to compensate for voltage drops caused by the sheet resistance of the adapter's aluminum traces. Two adapter types were designed for the Switcher-B. The first type (figure 6.28) can control a DEPFET Matrix of the PXD6 production (see chapter 7.1). It connects all 16 gate and clear signals of the matrix. The second adapter type is required to operate the matrixes from the previous DEPFET production PXD5, which were designed for the Switcher3. Two chips are needed to provide the gate and clear signals, as the bond pads are located on opposite sides of the matrix. While the gate signals can be connected by the first adapter type, the second type has to be used to connect to the clear pads¹.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [106].</p> <p>“Figure 6.31 shows a side view of the assembled adapter, with the DCD-RO on the left and the DCDB on the right. The adapter for the Switcher chips were also flip-chip bonded with double bumps.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [107].</p> <p>“The DEPFET matrixes of the PXD5 production for characterization of the ILC type designs were tested in setups with the read-out and steering chips wire bonded to the matrix. The novel all-silicon module approach, with flip-chip bonded chips, has not yet been demonstrated with active components. The first DEPFET matrixes with flip-chip interconnection of the read-out and steering chips were included on the PXD6 wafer run.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [117].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“By enlarging the silicon size of a DEPFET sensor, while keeping the size of the active area constant, space can be created for directly mounting the steering and readout chips onto the detector silicon and for routing the interconnection and power traces. On a highly integrated and densely populated area of such all-silicon modules, the routing of a huge amount of signal and power connections is a difficult task. The components, located on the detector silicon, must not influence the detector or the electronics operation. Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged 3.2. WAFER THINNING 23 quickly. A high capacitive load on the drain lines is not as limiting as on the control lines, because the DEPFET is operated in drain read-out mode, yielding to a current signal. Control, data and power lines have to be connected directly to the silicon, the module is mounted on a support structure, which is also used for actively cooling the readout chips. By thinning the silicon of the detector and the chips, the material budget of the module can be reduced furthermore. For interconnecting the chips with the detector module, the flip chip technology has been chosen.</p>

	<p>Details on interconnection will be presented in” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32-33].</p> <p>“Figure 3.6: Schematic side view of a thin module with a hole pattern in the support frame and a steering chip attached by bump bonding. 26 CHAPTER 3.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [35-36].</p> <p>“The flip-chip bonding process offers advantages over the wire bonding connection, such as a lower area requirement, shorter paths between substrate and chip, lower inductance and a fast parallel bonding process. The pads of substrate and chip are placed face-to- face and brought into contact using a conductive material. Flip-chip bonding needs less area on the substrate, because the landing pads are covered by the chip, whereas wire bonding needs space for wire looping and for the destination pads located around the chip. The path between source and destination pads is only a few tens of micrometers long, whereas bonding wires are in the range of hundreds or thousands of micrometers. Different conductive materials can be used to form the interconnection, e.g. gold-stud” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [91].</p> <p>“The flip-chip process starts by picking up the chip with a bond tool and placing the substrate on the bond table. Chip and substrate pads are then precisely aligned. The bond tool places the chip onto the substrate, while maintaining the precise alignment. The bonding is performed by applying a defined pressure while cycling through a temperature profile. Fully automatic machines for mass production use camera systems with pattern recognition to pick up and align the devices. The machine used during this thesis is a manual machine for R&D, reworking or low volume productions. Pick up, alignment and chip placing is a manual process, while the temperature profile is automatically cycled. The manual process in the</p>
--	--

	<p>‘Fineplacer Lambda’ is depicted in figure 6.2. The substrate is placed on the table and the bumped chip is fixed on the bond head by vacuum. An optical beam splitter superimposes the two images of the chip and the substrate to visualize the relative position of pads and bumps (A). The substrate is moved horizontally and the chip is rotated by the operator, until the pads and bumps are aligned. The chip is placed on the substrate in a precise 90° movement, maintaining the aligned position (B). The desired force is applied and a temperature cycle is started to form the bonds (C).” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [92-93].</p> <p>“The wire was of a type that had been normally used for ball/wedge bonding. It was made of a softer gold alloy with an elongation of 2-6% and a break load of >7cN and showed a 84 CHAPTER 6. INTERCON. TECHNOLOGY DEVELOPMENTS Figure 6.5: Photograph of bumps with uniform and short tails. Figure 6.6: 48µm free air ball on 17.5µm wire. non-uniform rip-off at gold-stud bumping. Figure 6.4 shows 65µm diameter test bumps with about 60-120µm long wire tails. These tails can cause shorts to neighboring bumps during flip-chip bonding, as they possibly bend sideways and touch neighboring bumps. A uniform bump height with short tails is desired to avoid shorts and to ensure that” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [93-94].</p> <p>“Figure 6.16 shows a side view of a double bump assembly. The rough cutting edge surface is caused by the laser cutting of the wafer. A cross section of single bump assembly is shown in figure 6.17 with a squashed bump diameter of 105µm and a chip distance of 32µm.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [101].</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“A set of adapters has been developed during this thesis, which is required to build test systems with the flip-chip only devices DCDB and Switcher-B. They convert the bump- bond footprint to a wire bondable pad pattern, which is compatible to the existing bond pattern of small DEPFET test matrixes and to the pad pitch available in PCB technologies. Pre-metallized 6” silicon wafers were used and manufactured in an engineering processing chain at the MPI semiconductor lab. The coarser design rules of that processing were sufficient for routing on the wire bond adapters and allowed a faster processing with a reasonable yield. The various adapter designs have been developed and arranged on the wafer area with respect to the dicing ability at an external facility. The DCDB adapter (figure 6.27) allows to connect all 128 drains of a matrix. The digital output signals are routed to the DCDB-RO converter chip, which is located close to the DCDB on the same wire bond adapter. It converts the DCDB’s single ended signals to differential pairs, which can be wire bonded to a PCB. Additional sense pads allow measurements of the supply voltages close to the chips, to compensate for voltage drops caused by the sheet resistance of the adapter’s aluminum</p>

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>traces.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [106].</p> <p>“A ceramic interposer with filled through hole vias is used to connect the detector with the read-out ASIC and provides a fan-out for the ASIC’s power and data signals. The detector is flip-chip bonded to one side of the interposer, while the ASIC is bonded to the other side.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [114].</p> <p>“Figure 6.46: Side view of the optical coupling principle. [58] avalanche photodiodes (APD). The read-out chip supports 16 detector inputs, which are connected to a 4x4 APD detector. A ceramic interposer with filled through hole vias is used to connect the detector with the read-out ASIC and provides a fan-out for the ASIC’s power and data signals. The detector is flip-chip bonded to one side of the interposer, while the ASIC is bonded to the other side.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [114].</p> <p>“The filling material of the interposer’s through hole vias (figure 6.44) was not solderable and caused the detector to fall off. A new interposer based on PCB material was then developed.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [114].</p> <p>“Since the detector is pressure sensitive, it cannot be bonded using gold-stud bumps and has to be soldered. The read- out chip had to be mounted first using gold-stud bumps, to allow a soldering of the detector in a second step (figure 6.43).” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [114].</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The additional routing layer can be seen between the bumps, which connects the bumps and is also used to distribute a supply voltage across the chip.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [96-97].</p> <p>“The solder jetting technology was chosen, because it doesn’t need mask sets and can be flexibly adjusted to different bump patterns. It neither needs toxic chemicals for plating, nor solder pastes. The solder is delivered as a powder with single spheres of a controlled diameter. The machine can support sphere diameters from 60µm up to 760µm. Currently, only the 60 µm diameter balls are in use. Figure 6.8 illustrates the solder jetting process. The solder balls are stored in a reservoir and singularized by a disk with holes and thickness matching the ball diameter. A single ball is fed into the capillary with an exit hole smaller than the ball (A). It clogs the hole and nitrogen pressure is applied to the airtight bond head. An infrared laser pulse melts the ball in the capillary (B) and the pressure blows the melted solder out (C). It is deposited onto the destination pad and solidifies (D). This process requires</p>

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>nitrogen gas to prevent the solder balls from oxidizing during the jetting process and during storage in the reservoir. The process can be adopted to different ball sizes by exchanging the capillary and the singularization disc. An under bump metallization is also required for the solder jetting process. As the devices are delivered with an aluminum pad finish and the standard UBM processes are not available, a flattened gold stud bump is used to place on the solder spheres. The gold bumps are flattened (coined) by pressing a glass plate with a defined force upon the bumps. A force of 40gr/bump creates a flat top with 40µm diameter on the 60µm diameter gold bump (figure 6.9). Afterwards, the chip has been solder bumped with 60µm solder balls, which created bumps with 65µm diameter and 40µm height (figure 6.11).” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [97].</p> <p>“The HyperImage medical imaging project [51] develops a hybrid system of time-of-flight positron emission tomography and magnetic resonance imaging. A multi channel read- out ASIC has been developed, which allows time-stamping in the range of 15 picoseconds [52]. A stack of 3 PCBs contains the silicon photo-multiplier (SiPM) detectors on top, the read- out ASICS in the middle and a controller board at the bottom [53].” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [109].</p> <p>“A ceramic interposer with filled through hole vias is used to connect the detector with the read-out ASIC and provides a fan-out for the ASIC’s power and data signals. The detector is flip-chip bonded to one side of the interposer, while the ASIC is bonded to the other side.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [114].</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>“The filling material of the interposer’s through hole vias (figure 6.44) was not solderable and caused the detector to fall off.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [114].</p> <p>“Figure 6.44: Filled through-hole vias in the ceramic interposer with solder bumps.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [148].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“A current source, controlled by a 2 bit DAC, is included in every input cell. It roughly compensates pedestal fluctuations of the DEPFET matrix and adopts the drain current to the dynamic range of the ADCs. The digitized signals of 32 input cells, with 2 ADCs each, are serialized to a 8 bit parallel link. The link runs at a speed of up to 400MHz, which is defined by the ADC conversion time. Eight slices of 32 inputs are included in one chip (figure 3.20). In total, one chip running at 100ns sampling time generates a data-rate of 2.56GB/s. The DACs for pedestal correction have to be set externally for every conversion cycle. Including</p>

	<p>on-chip memory was not possible due to space limitations. The digital part of the DCDB has been tested and operates at the target speed of 320 MHz correctly, with a noise of 90nA and a ADC resolution of 6 bits. For more detailed information it is referred to [34], [33] and [35]. The analog part, from the input up to the ADCs, is a full custom design, while the processing of the ADC output and multiplexing in the digital domain is an automatically 46 46 ROW_CLK GCK SW_STRB Switcher sequencer 18 PLL CHAPTER 3. THE DEPFET AS A VERTEX DETECTOR DCD_CLK DCD_IN 1 DCD_OUT de-serializer common mode correction off set DAC RD raw data memory memory controller memory x 10-20 PLL pedestal correction pedestal memory zero suppression hit pairing FIFO link layer framing DO serializer Gbit TX TRG Figure 3.22: Block diagram of the DHP data processing chip. [36] placed and routed standard cell design. A JTAG interface is integrated to configure and test the chip. It allows access to the control registers and the boundary scan chain. A 180nm 1.8V technology with 6 metal layers is used for the DCDB, which also provides an additional 7th metal layer with solder bumps (see figures 3.21). The 7th metal layer is used as a redistribution layer, originally meant to add solder bumps to a wire-bond only design and route the signals from the wire bond pads to the bump bond pads.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [55-56].</p> <p>“The octagonal bump pads are located in the center of the die. Additional wire bond pads have been added to be able to test the chip with existing, non flip-chip matrixes. The silicon area covered by the rectangular wire bond pads does not contain any circuits, allowing the pads to be easily removed for the final chip production. The chip size is reduced to 5780µm × 1400µm without these pads. The control signals are located at the bottom of figure 5.1 and the 128 outputs are arranged in a 4 × 32 bump pad array.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [70].</p>
--	---

	<p>“A solder wettable surface like copper or nickel is needed to place solder bumps on.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [95].</p> <p>“Figure 6.7 shows the DCDB solder bumps with 100µm diameter and a horizontal pitch of 200µm. The additional routing layer can be seen between the bumps, which connects the bumps and is also used to distribute a supply voltage across the chip.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [96-97].</p> <p>“The solder balls are of the same material SAC305 as the DCDB bumps, to assure an equal melting point during assembly of a DEPFET module. Figure 6.12 shows the side view of a soldered assembly, where gold stud bumps have been used as an UBM on the chip and the substrate. A soldering cycle starts with a preheat phase of about 120 seconds and slowly heats up all components. The temperature is then increased quickly above the melting point and stays constant for 10-30 seconds in order to form the solder joint. The assembly is then cooled down to ambient temperature.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [98].</p> <p>“The Switcher3 chip has a size of $5790 \times 1540\mu\text{m}^2$ and is forming 6 daisy chains with up to 32 bumps and a total of 164 connections, when bonded to the $9546 \times 1350\mu\text{m}^2$ large substrate.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [101].</p> <p>“The additional metal layer is based on copper and provides by a factor of 6 lower resistivity, but it has not yet been added to a 2-layer DEPFET production. Yield problems on the 2-layered PXD6 wafers’ metal structures can be addressed and evaluated on the MCM design, especially in conjunction with the 3rd metal layer. Two different MCM designs are</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>manufactured: One includes the metal layers of a DEPFET matrix in the active area to measure the parasitic capacitances and to check the yield issue (see figure 7.10). The other layout has test structures in this area, needed to operate and to test the chip performance.</p> <p>7.2.1 Switcher Balcony The Switcher balcony layout of the MCM is comparable to the PXD6 layout. Figure 7.11 shows a single Switcher with routing and decoupling. The first layer is used to route the control and strobe signals, as well as the JTAG slow control from the DHP chips to the Switchers. The digital power supply located left of the bumps is also routed in long buses to all chips. The second layer interconnects the chips with the buses and with the gate and clear lines of the matrix area. Termination resistors for the differential signals are not yet included into the chip and discrete surface mount resistors with a size of 01005 (0.4 × 0.2mm²) had to be added to the MCM layout. Wire bond pads are foreseen to short circuit the serial input and output lines in case of a broken Switcher. The resistor and the wire bond jumper pads are located in the ‘active area’ and are only needed for the MCM design. The final Switcher production will include the termination resistors. The right picture in figure 7.11 shows the 3rd metal layer. It is used to provide the bump landing pads in the solderable copper metallization.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [130].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The first adapters were produced together with the Belle-type dummy chips and didn’t include a passivation layer. They were sensitive to mechanical damages during handling or to machine malfunction during bumping. This caused damaged or shorted metal traces, as displayed in figure 6.29. The next iteration of the adapters included a passivation layer to protect the soft aluminum traces. The adapter close to the wafer edge showed shorts between metal traces caused by dust particle contaminations during lithography or etching (figure 6.30). The adapters were therefore optically inspected and selected prior bumping and flip-chip assembly. The wire bond adapters were first bumped with gold stud bumps to provide an UBM for the solder bumps of the DCDB and to allow double bump flip-chip for the DCD-RO. In the first step, the DCD-RO was bonded with thermocompression, as it is thinner than the DCDB. The bonding force could not be applied, if the thicker DCDB had been soldered first. The DCDB was then placed on the gold studs and soldered. Figure 6.31 shows a side view of the assembled adapter, with the DCD-RO on the left and the DCDB on the right. The adapter for the Switcher chips were also flip-chip bonded with double bumps. Positioning errors in the gold stud bumping process caused higher assembly failures. The bump bonder is a flexible machine designed for low volume production or research and development applications with medium pad pitches. It’s placement accuracy is limited 98” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [107-108].</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“A sideways movement pushes the solder ball to the pads edge and the vacuum removes it (B). 6.5 Test Structures Test substrates and test chips were used for evaluation of the flipping process, which create daisy chain connection of bumps after flipping. The substrate includes multiple pads for probing the connectivity of the daisy chained bump connections. Flip-chip process parameters like pressure, time and temperature were evaluated with gold stud” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [99-100].</p> <p>“The first test vehicles used were made of glass substrates with gold coated structures. They included 4 daisy chain connections of 16 bumps each, with probe pads for connectivity tests. Single bump and double bump approaches have been tested. Single bump assemblies use bumps on the chip only, while bumps on the chip and on the substrate are called double bump. The same flip-chip parameters have been used with all assemblies. A pressure of 80gr/bump</p>

	<p>and 350°C for 120 seconds forms the connection during the thermocompression bonding. Both assembly types showed successful bonds on all bumps, determined by the electrical connection.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [100].</p> <p>“The gold dummy chips were sufficient for the first test, but the Switcher3 and DCD chips, as well as the DEPFET module are based on silicon substrates with aluminum structures and have a higher pad count. The higher pad count results in a high pressure applied to the chip and substrate, which can possibly cause mechanical defects on the thinned DEPFET modules. A new set of test vehicles has been developed during the thesis, to adopt the bumping and the flip-chip processes to aluminum structured devices. The dummy chips should be mechanically as similar as possible to the real chips, although they were manufactured in a different technology and without active devices.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [101].</p> <p>“The digital output signals are routed to the DCD-RO converter chip, which is located close to the DCDB on the same wire bond adapter. It converts the DCDB’s single ended signals to differential pairs, which can be wire bonded to a PCB. Additional sense pads allow measurements of the supply voltages close to the chips, to compensate for voltage drops caused by the sheet resistance of the adapter’s aluminum traces. Two adapter types were designed for the Switcher-B. The first type (figure 6.28) can control a DEPFET Matrix of the PXD6 production (see chapter 7.1). It connects all 16 gate and clear signals of the matrix. The second adapter type is required to operate the matrixes from the previous DEPFET production PXD5, which were designed for the Switcher3. Two chips are needed to provide the gate and clear signals, as the bond pads are located on opposite sides of the matrix. While the gate signals can be connected by the first adapter type, the second type has to be used to</p>
--	---

	<p>connect to the clear pads¹. 1The matrix rows would be read out and cleared in opposite directions, if the first type also used to provide the clear signals. The Switcher-B is rotated by 180° on the second adapter type. 6.6. WIRE BONDING ADAPTERS 97 Figure 6.29: Damaged aluminum caused by a touching gold wire due to a bumping machine malfunction. Figure 6.30: Short circuit on a wire bond adapter caused by incomplete etching. Figure 6.31: Photograph of an assembled wire bond adapter with a DCD-RO (left) and a DCDB (right). The different chip thicknesses are well visible. The first adapters were produced together with the Belle-type dummy chips and didn't include a passivation layer. They were sensitive to mechanical damages during handling or to machine malfunction during bumping. This caused damaged or shorted metal traces, as displayed in figure 6.29. The next iteration of the adapters included a passivation layer to protect the soft aluminum traces. The adapter close to the wafer edge showed shorts between metal traces caused by dust particle contaminations during lithography or etching (figure 6.30). The adapters were therefore optically inspected and selected prior bumping and flip-chip assembly. The wire bond adapters were first bumped with gold stud bumps to provide an UBM for" Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [106-107].</p> <p>"The wire bond adapters were first bumped with gold stud bumps to provide an UBM for the solder bumps of the DCDB and to allow double bump flip-chip for the DCD-RO. In the first step, the DCD-RO was bonded with thermocompression, as it is thinner than the DCDB. The bonding force could not be applied, if the thicker DCDB had been soldered first. The DCDB was then placed on the gold studs and soldered. Figure 6.31 shows a side view of the assembled adapter, with the DCD-RO on the left and the DCDB on the right." Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [107].</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>“A flip-chip assembly of dies to PCBs is only possible for low pin count devices with a large pad pitch, as the possible pad pitches of the chips are much smaller than the pitches available on PCBs.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [109].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Figure 6.12 shows the side view of a soldered assembly, where gold stud bumps have been used as an UBM on the chip and the substrate. A soldering cycle starts with a preheat phase of about 120 seconds and slowly heats up all components. The temperature is then increased quickly above the melting point and stays constant for 10-30 seconds in order to form the solder joint. The assembly is then cooled down to ambient temperature.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [98].</p>

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>“The same devices have been used for evaluation of the solder jetting process as for the gold-only flipping. The solder bumped chip has been aligned and slightly placed onto the gold studs of the substrate to deform the small gold tails and ensure a contact between gold and solder. The temperature cycle was started after shutting off the vacuum holding the chip. It is observed that the chip slightly moves downwards, when the melting temperature of the solder was reached. The assemblies were measured and showed only one failure in 150 connections.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [98].</p> <p>“The first test vehicles used were made of glass substrates with gold coated structures. They included 4 daisy chain connections of 16 bumps each, with probe pads for connectivity tests. Single bump and double bump approaches have been tested. Single bump assemblies use bumps on the chip only, while bumps on the chip and on the substrate are called double bump. The same flip-chip parameters have been used with all assemblies. A pressure of 80gr/bump and 350°C for 120 seconds forms the connection during the thermocompression bonding. Both assembly types showed successful bonds on all bumps, determined by the electrical connection. A resistivity of 13 ± 0.2 has been measured for all snake structures, which includes the trace resistances. The bond quality has been checked by shearing the chip off the substrate. The bond interface broke equally on the chip and on the substrate side of the bump, indicating that thermosonic bumping and thermocompression flip-chip bonding created equally good bonds.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [100].</p> <p>“Flipping the silicon dummies with aluminum pads using single bumps worked well with the same setting as with the glass substrates. It was necessary to reduce the force in regard to damages of the thinned module, as 80gr/bump results in 17.9kg per DCD chip. An aggressive</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>step down to 20gr/bump resulted in $\approx$ 60% unconnected daisy chain structures and weak mechanical stability. 60gr/bump showed equally good results as 80gr/bump. The double bump approach was tested with the aim to reduce the force even more. Only one of 158 tests (0.6%) failed with a force 22gr/bump and a reduced temperature of 200°C.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [101].</p> <p>“The ILC dummy module is a mechanical sample demonstrating the ability to flip-chip bond with a low chip distance, but it doesn’t allow electrical tests. A low pitch device for connectivity testing was necessary. An uncut dummy chip wafer was cut with a different pattern. The substrates were cut in groups of three, while the chips were singularized. Three chips could then be bonded to the substrate sequentially. The large pickup tool 6.5.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [102-103].</p> <p>“Figure 6.21: Resistances per bump for different flip-chip assembly methods. covers all three chips and thus, the bonding force had to be increased for each flipping to ensure a force of 22gr/bump for all bumps. Double bumps were used, as they showed better results at the single chip substrate tests.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [103].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“By enlarging the silicon size of a DEPFET sensor, while keeping the size of the active area constant, space can be created for directly mounting the steering and readout chips onto the detector silicon and for routing the interconnection and power traces. On a highly integrated and densely populated area of such all-silicon modules, the routing of a huge amount of signal and power connections is a difficult task. The components, located on the detector silicon, must not influence the detector or the electronics operation. Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged 3.2. WAFER THINNING 23 quickly. A high capacitive load on the drain lines is not as limiting as on the control lines, because the DEPFET is operated in drain read-out mode, yielding to a current signal. Control, data and power lines have to be connected directly to the silicon, the module is mounted on a support structure, which is also used for actively cooling the readout chips.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32-33].</p> <p>“The DEPFET uses pixel sizes of $25\mu\text{m} \times 25\mu\text{m}$, which allows a binary resolution of $25\mu\text{m}/\sqrt{12} \approx 7\mu\text{m}$. The pixel signal is compared with a threshold value to detect a hit at the binary read-out scheme. Only this hit information is stored. A resolution of $3.5\mu\text{m}$ is achieved</p>
---	---

	<p>with the 50µm thin detector by interpolation using the center-of- gravity method and a signal-to-noise ratio of 40 [12]. Figure 3.9 shows the innermost layer. The modules are placed as close as possible to the beam pipe, at a radius of 1.5cm. The steering chips are at the long side of the matrix and the readout chips are at the short end. The modules are overlapping, to</p> <p>28 80 CHAPTER 3. THE DEPFET AS A VERTEX DETECTOR active DEPFET area (~50µm thick)” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [37-38].</p> <p>“The readout chips are located at the end of the module, which is in direct contact to the support structure. Channels for evaporative CO2 cooling are integrated within the support structure. They remove heat from the end of the modules directly and cool the chips through the module’s silicon and the bump bond connections.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [53].</p> <p>“The wire bond adapters were first bumped with gold stud bumps to provide an UBM for the solder bumps of the DCDB and to allow double bump flip-chip for the DCD-RO. In the first step, the DCD-RO was bonded with thermocompression, as it is thinner than the DCDB. The bonding force could not be applied, if the thicker DCDB had been soldered first. The DCDB was then placed on the gold studs and soldered. Figure 6.31 shows a side view of the assembled adapter, with the DCD-RO on the left and the DCDB on the right. The adapter for the Switcher chips were also flip-chip bonded with double bumps.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [107].</p> <p>“The adapters were therefore optically inspected and selected prior bumping and flip-chip assembly. The wire bond adapters were first bumped with gold stud bumps to provide an UBM for the solder bumps of the DCDB and to allow double bump flip-chip for the DCD-</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>RO. In the first step, the DCD-RO was bonded with thermocompression, as it is thinner than the DCDB. The bonding force could not be applied, if the thicker DCDB had been soldered first. The DCDB was then placed on the gold studs and soldered. Figure 6.31 shows a side view of the assembled adapter, with the DCD-RO on the left and the DCDB on the right. The adapter for the Switcher chips were also flip-chip bonded with double bumps. Positioning errors in the gold stud bumping process caused higher assembly failures. The” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [107].</p> <p>“Figure 7.12 display a close-up of the left DCDB, showing the drain fan-out connections on the bottom and the Switcher traces passing by the chip on the left. The DCDB’s bump pattern has been optimized for power supply routing on the module. Five bump rows allow the horizontal placement of power buses across all four chips. The drain input bumps are located below these power rails, while the digital I/O and control signals are above. The right sub-figure shows the copper layer with the five rails in the upper half of the DCDB. The routing of the drain lines in the chip’s lower half can be seen in the left sub-figure. Blue traces connect the DCDB to the DHP above.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [133].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“The DEPFET uses a pn-junction with a fully depleted bulk for signal generation and sidewards depletion to modulate the electrical field. A p-MOS signal amplification transistor is integrated in the front-side of the high resistivity n-type detector material. The highly p-doped back side implantation and the p-implantation of the transistor are used for sidewards depletion. The n⁺-contact needed for depletion is not shown in figure 2.8 and is located outside the sensitive area. The potential minimum for electrons is shifted towards the front side, to $\approx 1\mu\text{m}$ below the surface. A structured n⁺-implant is located beneath the transistor channel and creates the potential minimum, which collects the signal electrons.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [24].</p> <p>“By enlarging the silicon size of a DEPFET sensor, while keeping the size of the active area constant, space can be created for directly mounting the steering and readout chips onto the detector silicon and for routing the interconnection and power traces. On a highly integrated and densely populated area of such all-silicon modules, the routing of a huge amount of signal and power connections is a difficult task. The components, located on the detector silicon, must not influence the detector or the electronics operation. Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged 3.2. WAFER THINNING 23 quickly. A high capacitive load on the drain lines is not as limiting as on the control lines, because the</p>
---	--

	<p>DEPFET is operated in drain read-out mode, yielding to a current signal. Control, data and power lines have to be connected directly to the silicon, the module is mounted on a support structure, which is also used for actively cooling the readout chips. By thinning the silicon of the detector and the chips, the material budget of the module can be reduced furthermore. For interconnecting the chips with the detector module,” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32-33].</p> <p>“A benefit of the DEPFET is its low power consumption. A pixel consumes $ID \times VDS$ $100\mu A \times 5V \approx 500\mu W$ during read out. The power consumption of a switched off pixel is almost zero, although it is still sensitive and collects signal electrons. A half module has 2 rows of 512 DEPFET pixels activated during read out with the readout scheme described above. Therefore, an inner layer module consumes 1W. Adding the Switcher steering chips’ 0.85W and the DCD readout chips’ 2048 channels, with 5mW per channel, this sums up to $\approx 12W$.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [40].</p> <p>“The flip-chip bonding process offers advantages over the wire bonding connection, such as a lower area requirement, shorter paths between substrate and chip, lower inductance and a fast parallel bonding process. The pads of substrate and chip are placed face-to- face and brought into contact using a conductive material. Flip-chip bonding needs less area on the substrate, because the landing pads are covered by the chip, whereas wire bonding needs space for wire looping and for the destination pads located around the chip. The path between source and destination pads is only a few tens of micrometers long, whereas bonding wires are in the range of hundreds or thousands of micrometers.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [91].</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>“The manual process in the ‘Fineplacer Lambda’ is depicted in figure 6.2. The substrate is placed on the table and the bumped chip is fixed on the bond head by vacuum. An optical beam splitter superimposes the two images of the chip and the substrate to visualize the relative position of pads and bumps (A). The substrate is moved horizontally and the chip is rotated by the operator, until the pads and bumps are aligned. The chip is placed on the substrate in a precise 90° movement, maintaining the aligned position (B). The desired force is applied and a temperature cycle is started to form the bonds (C). Temperatures 6.3. GOLD-STUD FLIP-CHIP BONDING” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [92-93].</p> <p>“The DEPFET matrixes of the PXD5 production for characterization of the ILC type designs were tested in setups with the read-out and steering chips wire bonded to the matrix. The novel all-silicon module approach, with flip-chip bonded chips, has not yet been demonstrated with active components. The first DEPFET matrixes with flip-chip interconnection of the read-out and steering chips were included on the PXD6 wafer run. Different matrix design are used to evaluate the optimal pixel layout for the Belle II vertex detector.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [117].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

<p>[1.1.] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“The thickness of the PCB material and its components is enlarging the radius, increasing multiple scattering and deteriorating the physics performance of the detectors. A thin and small solution is needed. The All-Silicon Model By enlarging the silicon size of a DEPFET sensor, while keeping the size of the active area constant, space can be created for directly mounting the steering and readout chips onto the detector silicon and for routing the interconnection and power traces. On a highly integrated and densely populated area of such all-silicon modules, the routing of a huge amount of signal and power connections is a difficult task. The components, located on the detector silicon, must not influence the detector or the electronics operation. Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged 3.2. WAFER THINNING 23 quickly. A high capacitive load on the drain lines is not as limiting as on the control lines, because the DEPFET is operated in drain read-out mode, yielding to a current signal. Control, data and power lines have to be connected directly to the silicon, the module is mounted on a support structure, which is also used for actively cooling the readout chips. By thinning the silicon of the detector and the chips, the material budget of the module can be reduced furthermore. For interconnecting the chips with the detector module, the flip chip technology has been chosen. Details on interconnection will be presented in chapter 6. Cooling The integrated circuits, the leakage current of the detector and the currents flowing in signal and power traces are heat sources, that often need to be</p>
--	---

	<p>actively cooled.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32-33].</p> <p>“The flip-chip bonding process offers advantages over the wire bonding connection, such as a lower area requirement, shorter paths between substrate and chip, lower inductance and a fast parallel bonding process. The pads of substrate and chip are placed face-to- face and brought into contact using a conductive material. Flip-chip bonding needs less area on the substrate, because the landing pads are covered by the chip, whereas wire bonding needs space for wire looping and for the destination pads located around the chip.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [91].</p> <p>“The interconnection material can also assist in chip cooling, as it transfers heat from the chips to the cooled module. The flip-chip process starts by picking up the chip with a bond tool and placing the substrate on the bond table. Chip and substrate pads are then precisely aligned. The bond tool places the chip onto the substrate, while maintaining the precise alignment.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [92].</p> <p>“Figure 7.3 showed a 128×16 pixel matrix with bump bond pads. The Switcher is shown at the bottom with the fan-out connecting the steering signals to the active area above. The wire bond pads of the control and power signals are located left of the chip. The 128 drain lines of the matrix are connected to one DCDB.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [126].</p> <p>“The read-out chips DCDB and DHP, the kapton connection and a hole for a screw are located at the end of stave. Many components and traces have to be placed within the</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>constrained space. The signal path has to be routed from the matrix drains through the chips towards the kapton cable.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [133].</p> <p>“The first all-silicon layouts have been designed and were manufactured with the PXD6 DEPFET test production. The module sizes and technological options differ from the final properties for the Belle II detectors, but the modules might reveal problems which can be addressed in the upcoming chip and detector developments.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [142].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p> <p>“The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged 3.2. WAFER THINNING 23 quickly. A high capacitive load on the drain lines is not as limiting as on the control lines, because the DEPFET is operated</p>

	<p>in drain read-out mode, yielding to a current signal.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32-33].</p> <p>“Figure 3.2 shows a sketch of the module concept. The steering chips are located on the long side of the detector, while the readout chips are mounted on the short end. This setup results in short and low capacitance matrix steering signals, which can be charged 3.2.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [32-33].</p> <p>“Figure 3.9 shows the innermost layer. The modules are placed as close as possible to the beam pipe, at a radius of 1.5cm. The steering chips are at the long side of the matrix and the readout chips are at the short end. The modules are overlapping, to 28 80 CHAPTER 3. THE DEPFET AS A VERTEX DETECTOR active DEPFET area (~50µm thick)” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [37-38].</p> <p>“The steering chips are located on a balcony on the long side of the matrix. Contrarily to the IL/C balcony, only one column of steering chips is used for the Belle detector. The chips for Belle, called Switcher-B (see chapter 5.2), include the clear and gate driver within one chip. The readout chain contains two chips on the module: The DCDB (see chapter 3.5.2) does a basic offset subtraction and digitizes the drain current values. It’s digital output is processed by the DHP (see chapter 3.5.3), which does hit detection to reduce the amount of data. The DHP controls the DCDB and the Switcher-B chips and provides the timing of the readout cycles.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [52].</p> <p>“The Switcher is shown at the bottom with the fan-out connecting the steering signals to the active area above. The wire bond pads of the control and power signals are located left of the</p>
--	---

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>chip. The 128 drain lines of the matrix are connected to one DCDB.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [126].</p> <p>“The Switcher balcony layout of the MCM is comparable to the PXD6 layout. Figure 7.11 shows a single Switcher with routing and decoupling.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [130].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>“A cross section of single bump assembly is shown in figure 6.17 with a squashed bump diameter of 105µm and a chip distance of 32µm.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [101].</p> <p>“Figure 6.16 shows a side view of a double bump assembly. The rough cutting edge surface is caused by the laser cutting of the wafer. A cross section of single bump assembly is shown in figure 6.17 with a squashed bump diameter of 105µm and a chip distance of 32µm.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [101].</p> <p>“The measured chip sizes have to be taken into account for further module designs, which may differ from the ordered size, especially on multi-project chip productions. Measurements on the DCD2 showed a increased chip size of 26 - 62µm per edge.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [102].</p> <p>“Figure 6.18 displays a side view of the flipping process. A chip is mounted on the bond head and being placed to the substrate. The non-uniform cutting can be seen on its right side.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [102].</p> <p>“Flipping the 52 chips with a distance of 50µm to neighboring chips was doable with the available equipment.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [102].</p> <p>“Figure 6.31 shows a side view of the assembled adapter, with the DCD-RO on the left and the DCDB on the right. The adapter for the Switcher chips were also flip-chip bonded with</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>double bumps.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [107].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Figure 3.18 shows a half module of the second layer, illustrating the 4-fold row readout. One pair of gate and clear steering signals connects to 4 pixel rows and because the pixel column can’t share a common drain line, the number of drains lines has to be increased by a</p>

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>factor of 4, too.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [50-51].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Figure 6.12 shows the side view of a soldered assembly, where gold stud bumps have been used as an UBM on the chip and the substrate. A soldering cycle starts with a preheat phase of about 120 seconds and slowly heats up all components. The temperature is then increased quickly above the melting point and stays constant for 10-30 seconds in order to form the</p>

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>solder joint.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [98].</p> <p>“The same devices have been used for evaluation of the solder jetting process as for the gold-only flipping. The solder bumped chip has been aligned and slightly placed onto the gold studs of the substrate to deform the small gold tails and ensure a contact between gold and solder. The temperature cycle was started after shutting off the vacuum holding the chip. It is observed that the chip slightly moves downwards, when the melting temperature of the solder was reached.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [98].</p> <p>“The substrate is pre-heated to a temperature below the melting point to assist a selective melting of solder balls. The solder ball’s temperature is increased above the melting point by hot nitrogen gas blown through a heating nozzle (A). The head moves then downwards and vacuum is applied to the tapered capillary. A sideways movement pushes the solder ball to the pads edge and the vacuum removes it (B).” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [99].</p> <p>“Figure 6.16 shows a side view of a double bump assembly. The rough cutting edge surface is caused by the laser cutting of the wafer. A cross section of single bump assembly is shown in figure 6.17 with a squashed bump diameter of 105µm and a chip distance of 32µm.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [101].</p> <p>“A flip-chip assembly of dies to PCBs is only possible for low pin count devices with a large pad pitch, as the possible pad pitches of the chips are much smaller than the pitches available</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>on PCBs.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [109].</p> <p>“The DCDB data outputs and steering signals are connected to the closely located DCD-RO converter chips. The 270 differential signals of the DCD-RO are routed to the wire bond pads at the end of the module. The DCDBS power supply bump layout is optimized for routing on the module. Five horizontal bump rows provide five supply voltages to the chip. Horizontal power buses can be routed across all DCDBs, connecting the chips in parallel.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [125].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an	Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

<p>end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The flip-chip process starts by picking up the chip with a bond tool and placing the substrate on the bond table. Chip and substrate pads are then precisely aligned. The bond tool places the chip onto the substrate, while maintaining the precise alignment. The bonding is performed by applying a defined pressure while cycling through a temperature profile.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [92].</p> <p>“Gold spheres are used in gold-stud flip-chip bonding as interconnection material between chip and substrate. These sphere are called gold-studs and are produced using a modified wire bonding process. A gold ball is bonded to the pad like in the ball/wedge wire bonding, but instead of forming a loop the wire is ripped off as close as possible to the ball.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [93].</p> <p>“Figure 6.12 shows the side view of a soldered assembly, where gold stud bumps have been used as an UBM on the chip and the substrate. A soldering cycle starts with a preheat phase of about 120 seconds and slowly heats up all components. The temperature is then increased quickly above the melting point and stays constant for 10-30 seconds in order to form the solder joint. The assembly is then cooled down to ambient temperature. The same devices have been used for evaluation of the solder jetting process as for the gold-only flipping. The solder bumped chip has been aligned and slightly placed onto the gold studs of the substrate to deform the small gold tails and ensure a contact between gold and solder. The temperature</p>
--	--

	<p>cycle was started after shutting off the vacuum holding the chip. It is observed that the chip slightly moves downwards, when the melting temperature of the solder was reached.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [98].</p> <p>“The solder bumped chip has been aligned and slightly placed onto the gold studs of the substrate to deform the small gold tails and ensure a contact between gold and solder. The temperature cycle was started after shutting off the vacuum holding the chip. It is observed that the chip slightly moves downwards, when the melting temperature of the solder was reached. The assemblies were measured and showed only one failure in 150 connections.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [98].</p> <p>“Figure 6.16 shows a side view of a double bump assembly. The rough cutting edge surface is caused by the laser cutting of the wafer. A cross section of single bump assembly is shown in figure 6.17 with a squashed bump diameter of 105μm and a chip distance of 32μm.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [101].</p> <p>“Figure 6.32 shows a X-ray image of the DCD-RO with an alignment error of corresponding gold stud bumps of up to 40μm. Solder balls were added to the chip, which compensated the alignment error. The chip has been solder bumped using the jetting technique after coining the gold bumps to provide a flat surface. DCD-RO and DCDB have been placed on the wire bond adapter and a reflow cycle has been started to solder both chips at once.” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [108].</p>
--	--

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

	<p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“A bump pad with $\approx 70\mu\text{m}$ diameter is thus blocking much layout area. The circuit has to be designed around the pad, which is increasing the pad pitch or limiting the design complexity.</p> <p>Test structures have been included on a UMC 180nm chip submission by the chip designer</p> <p>6.5. TEST STRUCTURES 1 A Figure 6.24: Layout of the test structures in UMC 180nm</p>	<p>Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“A bump pad with $\approx 70\mu\text{m}$ diameter is thus blocking much layout area. The circuit has to be designed around the pad, which is increasing the pad pitch or limiting the design complexity.</p> <p>Test structures have been included on a UMC 180nm chip submission by the chip designer</p> <p>6.5. TEST STRUCTURES 1 A Figure 6.24: Layout of the test structures in UMC 180nm</p>

Appendix A-44 - Invalidity of U.S. Patent No. 9859202 in view of Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module - Non-Patent Publication

<p>the corresponding top metal pads of the spacer connector.</p>	<p>technology. ✓ Gate = -1.2Vorig VGate -1.2V bump -1.2Vflipped VGate Gate VGate = -1.8Vorig VGate -1.8V flipped 120 100 80 VGate=1.2Vorig VGate 1.2V bump 1.2Vflipped VGatate = 1.8Vorig VGate 1.8V bump VGate 1.8Vflipped 60 40 60 Idrain [mA] 20 0 -20 40 -40 20 -60 0 0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6 1.8 Idrain [mA] 95 95 -1.8 -1.6 -1.4-1.2 -1 -0.8 -0.6 -0.4 -0.2 0 Vdrain[V] Figure 6.25: NMOS transistor output for different gate voltages before and after bumping and flipping. Vdrain[V] Figure 6.26: PMOS transistor output for different gate voltages before and after bumping and flipping. to investigate the influence of bonding onto pads above transistors and metal traces. Each chip includes 6 transistors and 4 metal trace tests. Two structures have parallel traces to test for shorts between the layers and two have narrow and long traces to check the connectivity. The three upper metal layers build the bump pad and the three lower, together with the poly-silicon layer, were used for testing. Figure 6.24 shows a part of” Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module, [104-105].</p> <p>To the extent Plaintiff contends that Steering Electronics, Module Design and Construction of an All Silicon DEPFET Module fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART
Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

All-Copper Chip-To-Substrate Interconnects For High Performance Integrated Circuit Devices was published by Tyler N. Osborn. All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ‘202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory². All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices is a dissertation that was published April 2, 2009. All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices is therefore prior art to the ‘202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, or otherwise rendered obvious by disclosures and teachings of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices with: (1) the

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>“In this work, all-copper connections between silicon microchips and substrates are developed. The semiconductor industry advances the transistor density on a microchip based on the roadmap set by Moore’s Law. Communicating with a microprocessor which has nearly one billion transistors is a daunting challenge. Interconnects from the chip to the system (i.e. memory, graphics, drives, power supply) are rapidly growing in number and becoming a serious concern. Specifically, the solder ball connections that are formed between the chip itself and the package are challenging to make and still have acceptable electrical and mechanical performance.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [16].</p> <p>“The fabrication process flow diagram is shown in Figure 3.1. A seed layer consisting of Cr/Cu/Ti (50nm/500nm/10nm) was DC sputtered onto a bare <100> 4” Si wafer. Then, a Unaxis PECVD system was used to deposit 1.5 μm of silicon dioxide at 250°C on top of the Ti layer. Microposit SC1813 photoresist (Shipley Corporation) was spun on the silicon dioxide surface. After photo-patterning the photoresist layer, buffered oxide etch (BOE) was used to etch the SiO₂ and Ti layers in the exposed areas down to the underlying Cu seed layer. Remaining photoresist was removed by acetone rinsing. Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface. The spin speed for the polymer was 500 RPM for 60 seconds. After spin-coating, a 100°C soft-bake was performed on a hotplate for 40 minutes. The Avatrel layer was then photo-patterned using 250 mJ/cm² dose at 365nm wavelength. Following exposure a post-exposure bake was applied in an oven at 100°C for 20 minutes. Then, the layer was developed in BioAct EC-7R Defluxer for 30 seconds immersed in an ultra-sonic bath. The polymer pattern generated high aspect ratio hollow core molds for copper pillar electroplating. 33 Si Cu and SiO₂ Deposition</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>SiO2 Patterning Polymer Coating SiO2 Cu” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [50-51].</p> <p>“After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held together with a low temperature melting wax. The aligned samples were then placed into a copper electroless plating bath.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin- coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10mm x 10mm test samples for bonding to fabricated silicon test chips.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>“The effects of increased modulus of the polymer collar were experimentally verified. Copper pillars were fabricated with three different photodefinable polymer collars, each with a different elastic modulus. The samples were bonded via the electroless copper plating and annealing process, as described previously, and then shear tested to investigate the mechanical strength.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [55].</p>
--	--

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>“Copper pillars were pre-fabricated on silicon substrates and flip-chip assembled, as previously discussed³. The test samples were electrolessly copper plated and joined using copper baths with different PEG concentrations. The samples were then potted in epoxy and cross-sectioned prior to any annealing to analyze the joint between the deposited metal.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [107].</p>
[1.A] a bottom package substrate;	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Chip-to-substrate interconnects provide power, electrical contacts, and a mechanical link between the chip and the substrate. The two most common chip assembly schemes today, wire bonding and flip chip bonding are illustrated in Figure 1 (a) and (b), respectively. [1-4] The area-array flip-chip configuration provides for a higher number of I/O and the electrical environment is superior to wire bonding because it has lower inductance and capacitance. An area array of flip-chip solder balls has more I/O than peripheral wire bonds. Flip-chip connections also provide an additional thermal path for chip cooling through the I/O. Flip chip assembly uses metal connections; often solder spheres, to connect the chip to the substrate and/or the substrate to the board as shown in Figure 1 (b). Chips can also be connected directly to the board in a chip-on-board (COB) configuration, Figure 1 (c). COB is a less costly and lower profile (total height) technology; however, the substrate helps in electrical fan-out and allows for a higher number of I/O. The substrate also assists in assembly of a heat-sink which is needed on high power chips.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [19-20].</p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>“Packaging with cost-effective organic printed circuit boards requires that elevated temperature excursions be as low as possible, but definitely below 250 C.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [23].</p> <p>“To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin- coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10mm x 10mm test samples for bonding to fabricated silicon test chips.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>“Samples were made using the flip-chip alignment, electroless plating, and low temperature annealing process described above. An anneal temperature of 180°C for one hour was used. Bonding between silicon and the organic materials is unique versus the silicon-to-silicon bonding tests in that the materials no longer have the same coefficient of thermal expansion (CTE). The CTE of Si is 3 ppm/°C versus 14 ppm/°C for FR-4 and 15 ppm/°C for BT. During the annealing process, the copper interconnects will be under shear stress conditions. Brongersma et al have shown that copper films under stress during recrystallization can exhibit unusually large grain growth termed super secondary grain growth. [56] Shear loading conditions could potentially be helpful to the bonding process and encourage grain growth in the bonded 53 53 region. After annealing, the samples were shear tested and compared to silicon-to-silicon bonded samples annealed at the same temperature. The</p>
--	--

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>silicon-to-board bonded samples exhibit different failure characteristics versus silicon-to-silicon bonding. Since the Avatrel is no longer a single polymer collar surrounding the copper pillar on the organic substrate, but instead a continuous polymer film, it can no longer detach from the surface easily during shear force testing. Therefore, the stress failure takes place in two steps. First, the copper pillar is broken from the copper laminate surface (pillar-to-surface adhesion). Then, the pillar is pulled out from the polymer film and remains attached to the pillar on the silicon sample surface. An example of successful bonding chip-to-substrate that survived the destructive shear force testing is shown in cross-section in Figure 4.7. It exhibits very uniform cross-section and no interfaces between the bonded pillar structures. All of the samples tested showed no visible degradation of the organic board materials.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [71-72].</p> <p>“Since increasing the temperature alone leads to transport limitations and porosity, an additive based strategy was employed. If the temperature could be increased, but the deposition rate suppressed by adsorption of an inhibitor, the kinetically controlled conditions could be maintained. PEG was chosen as an inhibiting additive since its interactions with copper surfaces and electroless plating chemistries have been studied.[73-79] In order to characterize the effects of PEG on our electroless plating rate, various concentrations of PEG were used and the plating rate was measured. Clean copper 87 surfaces were used for this experiment to reduce the transport limitations as much as” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [105-106].</p> <p>“Since the industry is moving towards on-chip interconnect networks that require the use of brittle inter-metal dielectric materials to meet low-k requirements, stress on these networks in the package is a serious concern.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [112].</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Chip-to-substrate interconnects provide power, electrical contacts, and a mechanical link between the chip and the substrate. The two most common chip assembly schemes today, wire bonding and flip chip bonding are illustrated in Figure 1 (a) and (b), respectively. [1-4] The area-array flip-chip configuration provides for a higher number of I/O and the electrical environment is superior to wire bonding because it has lower inductance and capacitance. An area array of flip-chip solder balls has more I/O than peripheral wire bonds. Flip-chip connections also provide an additional thermal path for chip cooling through the I/O. Flip chip assembly uses metal connections; often solder spheres, to connect the chip to the substrate and/or the substrate to the board as shown in Figure 1 (b). Chips can also be connected directly to the board in a chip-on-board (COB) configuration, Figure 1 (c). COB is a less costly and lower profile (total height) technology; however, the substrate helps in electrical fan-out and allows for a higher number of I/O. The substrate also assists in assembly</p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>of a heat-sink which is needed on high power chips.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [19-20].</p> <p>“The need for small chip footprint, especially in portable electronics, and higher I/O density has created the need for new packaging technologies. Chip-scale packages were created to address a rapidly growing segment of the market. These chip-scale packages enabled a high silicon packing density, however, CTE mismatch between the silicon and the board needed to be addressed.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [24].</p> <p>“A small amount of compliance between the chip and substrate was achieved by Fujitsu in the SuperCSP package.[7] Short copper posts were fabricated on the chip in wafer form. A polymer was then used to encapsulate the posts. The structure has a degree of compliance because the post can elastically deform and the polymer encapsulation can help distribute the stress. Most of the compliance was provided by conventional solder 8 bumps attached to ends of the posts. The Fujitsu SuperCSP used copper-posts 350 μm diameter and 100 μm tall.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [26-27].</p> <p>“After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO_4, 52 g/L H_2SO_4, 40ppm Cl, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm^2 for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held</p>
--	--

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>together with a low temperature melting wax.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“Samples were made using the flip-chip alignment, electroless plating, and low temperature annealing process described above. An anneal temperature of 180°C for one hour was used. Bonding between silicon and the organic materials is unique versus the silicon-to-silicon bonding tests in that the materials no longer have the same coefficient of thermal expansion (CTE). The CTE of Si is 3 ppm/°C versus 14 ppm/°C for FR-4 and 15 ppm/°C for BT. During the annealing process, the copper interconnects will be under shear stress conditions.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [71].</p> <p>“The objective of the modeling work was to examine approaches to lowering the stress exerted by the copper pillar on the die. This is intended to minimize the risk of failure in the on-chip low-k copper interconnect network. The metric chosen as an acceptable level of stress was that of the yield stress for currently used solder alloys in flip-chip packaging, such as SnAg3.5Cu0.7.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [80].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“The all-copper process entails electroless copper deposition between two copper pillars, followed by low temperature annealing to ‘knit’ together the seam left between xvi the two pillars and mechanically strengthen the joint.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [16-17].</p> <p>“After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held together with a low temperature melting wax.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“To evaluate the effect of height mismatch, polystyrene micro-spheres (Polysciences Megabeads) with a diameter of 125 μm ± 2.3 μm were dispersed from a DI water solution with 1 wt% solids onto the sample surface. These micro-spheres served to set a known standard off distance between the sample surfaces illustrated in Figure 3.2. To create different</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>separation distances between the pillar top surfaces, different height pillars were electroplated onto the samples of 30, 40, and 50 μm, leading to separation distances between the pillar surfaces of approximately 65, 45, and 25 μm respectively.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [53].</p> <p>“The solder reflow process has unique capabilities to overcome the non-planarity of organic substrates and either elongate or flatten as necessary to bond the chip to the package. Assessing the z-axis height mismatch the all-copper process can overcome is important in characterizing its dexterity versus traditional solder processing. Figure 4.5 shows SEM images of the results of testing separation distances of approximately 25, 45, 51 and 65 μm.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [69-70].</p> <p>“Figure 4.5: SEM images showing the effects of increasing separation distance between pillar surfaces at distances of: (left) 25 μm (middle) 45 μm (right) 65 μm” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [70].</p> <p>“Figure 5.2: Illustration and finite element model of the single copper pillar system used in this study” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [80].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The structure has been simplified to eliminate one of the half-turn structures, shown in Fig. 2.4.[17] The electrical properties of the compliant I/O are an essential element of the design. Of particular interest for helix structures is the self-inductance, which ranged from 0.03 to 0.15 nH for the designs studied.[17] 11 A bimetallic beam structure has been designed and studied. [18] The bimetallic internal stress gradient in the beam creates an upward bending of the beam upon release from the surface. Solder attachment metal on the released end of the beam provides for attachment to the next layer of packaging.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [29-30].</p> <p>“Finally, more complex beam shapes have been investigated. Liao et al. have studied released beams on the chip.[19] The beams are anchored on both ends (on the chip) and released in the middle. The released portion of the beam can take a variety of forms, including ‘S’ shaped elements. A solder attachment bump can be placed in the middle of the release beam. This provides extensive design freedom.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [30].</p> <p>“By applying a metal conductor to the 13 exterior of a polymer pillar, the compliance of the interconnect structure could be improved. Aggarwal et al. showed that by using a compliant polyimide core material with a copper shell the compliance increased versus the use of a solid copper pillar of the same diameter (as shown in Figure 2.6).[24] Due to the skin effect at high operating frequency, the copper shell does not have to be very thick since the signal does not</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>penetrate deep into the metal. For example, copper has a skin depth of approximately $1.2\text{ }\mu\text{m}$ at 3 GHz operating frequency. This portion of metal is primarily involved in the transmission of the electrical signal. As operating frequency increases the skin depth continues to decrease which works in favor of these structures since the exterior copper thickness limits the mechanical compliance.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [31-32].</p> <p>“Thus, one can consider geometries other than cylindrical in order to distribute a given force (dictated by the CTE mismatch between Si and FR-4) over a wider area (lower effective stress at the critical point in the chip-pillar interface). Expanding the effective surface area of the pillar in the direction of the thermal expansion was achieved by considering an elliptical pillar. Using the ellipse requires careful consideration of the orientation of the I/O so that the broader face of the elliptical pillar is facing the direction of thermal expansion. Three different elliptical shapes were chosen based on their eccentricity. For simplicity, the ratio of the two diameters that define the ellipse, A and B, will be used to define the shape, as shown in Figure 5.7. While holding the cross-sectional area approximately constant, three different A/B ratios were chosen and compared to the $50\text{ }\mu\text{m}$ diameter circular pillar. Cross-sectional plots of the stress at the chip surface for a cylinder with $A/B = 1$ and an ellipse with $A/B = 3$ are” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [86].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“The materials available to create capped solid metal pillar connections are highly variable and most likely depend on cost and application requirements” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [31].</p> <p>“Huffman et al. have shown that pure tin placed between two copper bumps can be used to create a solid pillar interconnect (as shown in Figure2.7).[25] It was shown that 2 μm thick tin layers would form homogeneous Cu3Sn intermetallics in the bonded region, but were very sensitive to non-planarity between chip and substrate. Small variations in the vertical separation between bumps could prevent forming of a solid bond. Thicker tin layers, 3.7 – 6 μm, were used to alleviate the sensitivity to non-planarity and lower bonding pressures were used to prevent squeeze out of the tin. Unfortunately, this resulted in bond intermetallics layers consisting of a tri-layer structure of Cu3Sn/Cu6Sn5/Cu3Sn. Higher pressures could still achieve the homogeneous Cu3Sn intermetallic but led to significant squeeze out of tin. The results also showed that, based on die shear testing, the homogeneous bonded Cu3Sn intermetallic led to higher shear strength” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [33].</p> <p>“By using an undercut photoresist pattern as the electroplating mold cone shaped gold bumps can be created. Due to the extremely small cross-section of the tip of the cone, the material can be made to yield and flatten during the thermo-compressive bonding cycle. Figure 2.11</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>shows an image of the cone shaped Au bumps and the process steps for bonding the cone shaped gold bumps to the plated gold pads.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [44].</p> <p>“Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface. The spin speed for the polymer was 500 RPM for 60 seconds. After spin-coating, a 100°C soft-bake was performed on a hotplate for 40 minutes. The Avatrel layer was then photo-patterned using 250 mJ/cm² dose at 365nm wavelength. Following exposure a post-exposure bake was applied in an oven at 100°C for 20 minutes. Then, the layer was developed in BioAct EC-7R Defluxer for 30 seconds immersed in an ultra-sonic bath. The polymer pattern generated high aspect ratio hollow core molds for copper pillar electroplating. 33 Si Cu and SiO₂ Deposition SiO₂ Patterning Polymer Coating SiO₂ Cu” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [51-52].</p> <p>“After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin- coated to 50 μm thickness. This layer was</p>
--	--

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>“Copper pillars were fabricated with three different photodefinable polymer collars, each with a different elastic modulus. The samples were bonded via the electroless copper plating and annealing process, as described previously, and then shear tested to investigate the mechanical strength. The fabrication process for all-copper was previously described. Fabrication parameters for the three materials: Avatrel 2195P (Promerus LLC, Brecksville, OH), Avatrel 8000P (Promerus LLC, Brecksville, OH), and SU-8 2025 (MicroChem Corp., Newton, MA) are summarized in Table 3.1. Each polymer was used to create high aspect ratio polymer collar plating molds with different mechanical properties. SEM images of copper pillars fabricated with each of the three systems are shown in Figure 3.4.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [55].</p> <p>“Copper Line Capacitor Fabrication and Testing Copper lines were fabricated on glass substrates to electrically study the deposition process. Utilizing standard microfabrication techniques copper lines were fabricated in a comb capacitor type structure as shown in Figure 3.6. Once the samples were fabricated, insulated copper wiring was attached to the probe pads for electrical contact.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [59].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p> <p>“The solder joint on the copper post provides an inexpensive way to compensate for any z-axis (height) mismatched between the chip and substrate. The solder ball can be slightly compressed or elongated during reflow to make up for non-planarity in the parts.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [27].</p> <p>“Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface. The spin speed for the polymer was 500 RPM for 60 seconds. After spin-coating, a 100°C soft-bake was performed on a hotplate for 40 minutes. The Avatrel layer was then photo-patterned using 250 mJ/cm² dose at 365nm wavelength. Following exposure a post-exposure bake was applied in an oven at 100°C for 20 minutes. Then, the layer was developed in BioAct EC-7R Defluxer for 30 seconds immersed in an ultra-sonic bath. The polymer pattern generated high aspect ratio hollow core molds for copper pillar electroplating.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [51].</p> <p>“After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl, 0.5vol%</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held together with a low temperature melting wax. The aligned samples were then placed into a copper electroless plating bath.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“Figure 4.1 is a cross-section of the two joined pillars after the plating process but before annealing. In Figure 4.1 the two pillars are labeled as Cu and each silicon test surface is also labeled as Si. There is a distinct interface between the two electroless plated regions.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [63].</p> <p>“Cross-sections were made after annealing for a shortened period of time at lower temperature (150 ° C) to analyze the change from the distinct unannealed interface to the continuous smooth copper observed in the fully annealed structures. In Figure 4.2a, the interface is still present after 30 minutes at 150°C. After an additional 30 minutes at 180°C (Figure 4.2b) the interface has been removed entirely and the copper bonding process has completed.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [64-65].</p> <p>“After coating copper pillars with a thin layer of palladium, samples were flip-chip aligned and immersed in the electroless gold bath. Once gold deposition was completed the samples were annealed at 180 C for 1 hr. After annealing they were broken apart and analyzed for</p>
--	--

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>bonded pillar pairs. Figure 6.3 shows an SEM image of the gold-gold bonding region between two pillars.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [99].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface. The spin speed for the polymer was 500 RPM for 60 seconds. After spin-coating, a 100°C soft-bake was performed on a hotplate for 40 minutes. The Avatrel layer was then photo-patterned using 250 mJ/cm² dose at 365nm wavelength. Following exposure a post-exposure bake was applied in an oven at 100°C for 20 minutes. Then, the layer was developed in BioAct EC-7R Defluxer for 30 seconds immersed in an ultra-sonic bath. The polymer pattern generated high aspect ratio hollow core molds for copper pillar electroplating.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [51].</p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

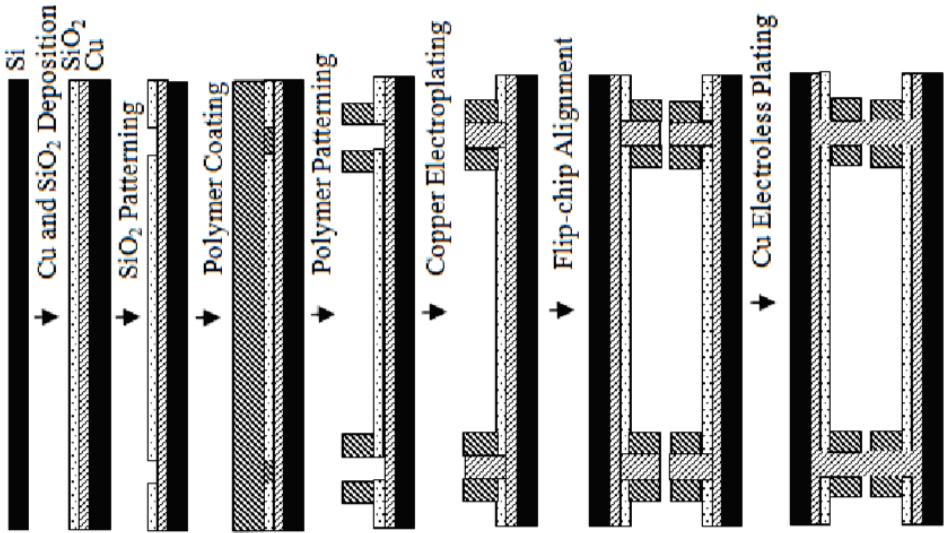
	<p>“After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“Figure 3.1: Fabrication flow for fabrication of all-copper interconnects structures After the patterning steps copper pillars are electroplated to fill the polymer molds.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52].</p> <p>“To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin- coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general</p>
--	--

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The fabrication process flow diagram is shown in Figure 3.1. A seed layer consisting of Cr/Cu/Ti (50nm/500nm/10nm) was DC sputtered onto a bare <100> 4” Si wafer. Then, a Unaxis PECVD system was used to deposit 1.5 μm of silicon dioxide at 250°C on top of the Ti layer. Microposit SC1813 photoresist (Shipley Corporation) was spun on the silicon dioxide surface. After photo-patterning the photoresist layer, buffered oxide etch (BOE) was used to etch the SiO₂ and Ti layers in the exposed areas down to the underlying Cu seed layer. Remaining photoresist was removed by acetone rinsing. Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface. The spin speed for the polymer was 500 RPM for 60 seconds. After spin-coating, a 100°C soft-bake was performed on a hotplate for 40 minutes. The Avatrel layer was then photo-patterned using 250 mJ/cm² dose at 365nm wavelength. Following exposure a post-exposure bake was applied in an oven at 100°C for 20 minutes. Then, the layer was developed in BioAct EC-7R Defluxer for 30 seconds immersed in an ultra-sonic bath. The polymer pattern generated high aspect ratio hollow core molds for copper pillar electroplating.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [50-51].</p>
--	--

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>“After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held together with a low temperature melting wax. The aligned samples were then placed into a copper electroless plating bath. The bath used was Circuposit 3350 from Shipley Corporation. In this bath the reducing agent is formaldehyde (2 g/L), complexing agent is EDTA (ethylenediaminetetraacetic acid) (35 g/L), and also contains sodium hydroxide reaching a pH of 12.5. The electroless plating process proceeded at room temperature for 18 hours with stirring and nitrogen purging. After electroless plating the samples were annealed in a nitrogen environment” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“The aligned samples were then placed into a copper electroless plating bath. The bath used was Circuposit 3350 from Shipley Corporation. In this bath the reducing agent is formaldehyde (2 g/L), complexing agent is EDTA (ethylenediaminetetraacetic acid) (35 g/L), and also contains sodium hydroxide reaching a pH of 12.5. The electroless plating process proceeded at room temperature for 18 hours with stirring and nitrogen purging. After electroless plating the samples were annealed in a nitrogen environment for one hour at various temperatures. In addition some samples were annealed after electroplating but prior to the flip-chip alignment, electroless plating, and post-bonding anneal steps.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [53].</p>
--	---



Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>“To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin-coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10mm x 10mm test samples for bonding to fabricated silicon test chips.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>“The fabrication process for all-copper was previously described. Fabrication parameters for the three materials: Avatrel 2195P (Promerus LLC, Brecksville, OH), Avatrel 8000P (Promerus LLC, Brecksville, OH), and SU-8 2025 (MicroChem Corp., Newton, MA) are summarized in Table 3.1. Each polymer was used to create high aspect ratio polymer collar plating molds with different mechanical properties. SEM images of copper pillars fabricated with each of the three systems are shown in Figure 3.4. Based on reported values for the elastic properties of these three materials, a range of modulus values between 0.5 and 4.0 GPa was expected. All of the samples tested were annealed at 180°C for 1 hour in a nitrogen environment.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [55-56].</p> <p>“Cross-sections were made after annealing for a shortened period of time at lower temperature (150 ° C) to analyze the change from the distinct unannealed interface to the continuous smooth copper observed in the fully annealed structures. In Figure 4.2a, the</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

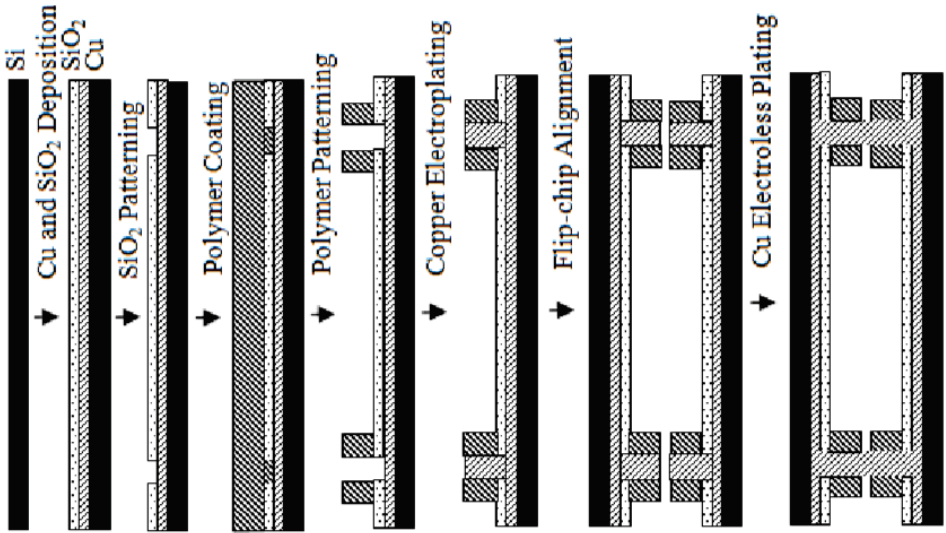
	<p>interface is still present after 30 minutes at 150°C. After an additional 30 minutes at 180°C (Figure 4.2b) the interface has been removed entirely and the copper bonding process has completed.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [64-65].</p> <p>“Figure 4.4 shows two pillars that were successfully bonded despite misalignment greater than the diameter of the pillars themselves, which exceeds the capabilities of solder. The bonded set survived destructive shear testing, showing that the pillar-to-pillar bond was still stronger than the pill-to-surface adhesion despite its significantly reduced cross-sectional area, and non- uniform geometry.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [68-69].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, <i>e.g.</i>:</p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>“The fabrication process flow diagram is shown in Figure 3.1. A seed layer consisting of Cr/Cu/Ti (50nm/500nm/10nm) was DC sputtered onto a bare <100> 4” Si wafer. Then, a Unaxis PECVD system was used to deposit 1.5 μm of silicon dioxide at 250°C on top of the Ti layer. Microposit SC1813 photoresist (Shipley Corporation) was spun on the silicon dioxide surface. After photo-patterning the photoresist layer, buffered oxide etch (BOE) was used to etch the SiO₂ and Ti layers in the exposed areas down to the underlying Cu seed layer. Remaining photoresist was removed by acetone rinsing. Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [51].</p> <p>“After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held together with a low temperature melting wax. The aligned samples were then placed into a copper electroless plating bath.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“The aligned samples were then placed into a copper electroless plating bath. The bath used was Circuposit 3350 from Shipley Corporation. In this bath the reducing agent is formaldehyde (2 g/L), complexing agent is EDTA (ethylenediaminetetraacetic acid) (35 g/L), and also contains sodium hydroxide reaching a pH of 12.5. The electroless plating process</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>proceeded at room temperature for 18 hours with stirring and nitrogen purging. After electroless plating the samples were annealed in a nitrogen environment for one hour at various temperatures. In addition some samples were annealed after electroplating but prior to the flip-chip alignment, electroless plating, and post-bonding anneal steps.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [53].</p>
--	--



Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>“To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin-coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10mm x 10mm test samples for bonding to fabricated silicon test” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>“Successful bonding between silicon test chips and organic printed circuit board materials was also performed showing no observable degradation of the organic board material.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [61].</p> <p>“Figure 4.7: SEM cross-section of pillars bonded between Si and FR-4 54” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [72-73].</p> <p>“With this process bonding between silicon test chips and organic substrates has been performed 56 99 and demonstrated continuous copper connections without any observable degradation of” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [74-75].</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“The all-copper process entails electroless copper deposition between two copper pillars, followed by low temperature annealing to ‘knit’ together the seam left between xvi the two pillars and mechanically strengthen the joint. It was found that using a commercially available electroless copper bath for the plating, followed by annealing at 180 C for 1 hour, the shear strength of the copper-copper bond was approximately 165 MPa. Cross-section analysis showed that during the deposition process plating occurs until a fine seam remains between the two plated surfaces. Then, upon annealing the seam begins to diminish and finally disappear after annealing at 180 C. This is significant since 180 C is compatible with cost-effective organic substrate materials such as FR-4, which are commonly used for typical flip-chip packaging.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [16-17].</p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>“Chip-to-substrate interconnects provide power, electrical contacts, and a mechanical link between the chip and the substrate. The two most common chip assembly schemes today, wire bonding and flip chip bonding are illustrated in Figure 1 (a) and (b), respectively. [1-4] The area-array flip-chip configuration provides for a higher number of I/O and the electrical environment is superior to wire bonding because it has lower inductance and capacitance. An area array of flip-chip solder balls has more I/O than peripheral wire bonds. Flip-chip connections also provide an additional thermal path for chip cooling through the I/O.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [19].</p> <p>“The fabrication process flow diagram is shown in Figure 3.1. A seed layer consisting of Cr/Cu/Ti (50nm/500nm/10nm) was DC sputtered onto a bare <100> 4” Si wafer. Then, a Unaxis PECVD system was used to deposit 1.5 μm of silicon dioxide at 250°C on top of the Ti layer. Microposit SC1813 photoresist (Shipley Corporation) was spun on the silicon dioxide surface. After photo-patterning the photoresist layer, buffered oxide etch (BOE) was used to etch the SiO₂ and Ti layers in the exposed areas down to the underlying Cu seed layer. Remaining photoresist was removed by acetone rinsing. Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [51].</p> <p>“After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held together with a low temperature melting wax. The aligned samples were then placed into a copper electroless plating bath.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [52-53].</p> <p>“The aligned samples were then placed into a copper electroless plating bath. The bath used was Circuposit 3350 from Shipley Corporation. In this bath the reducing agent is formaldehyde (2 g/L), complexing agent is EDTA (ethylenediaminetetraacetic acid) (35 g/L), and also contains sodium hydroxide reaching a pH of 12.5. The electroless plating process proceeded at room temperature for 18 hours with stirring and nitrogen purging. After electroless plating the samples were annealed in a nitrogen environment for one hour at various temperatures. In addition some samples were annealed after electroplating but prior to the flip-chip alignment, electroless plating, and post-bonding anneal steps.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [53].</p>
--	--

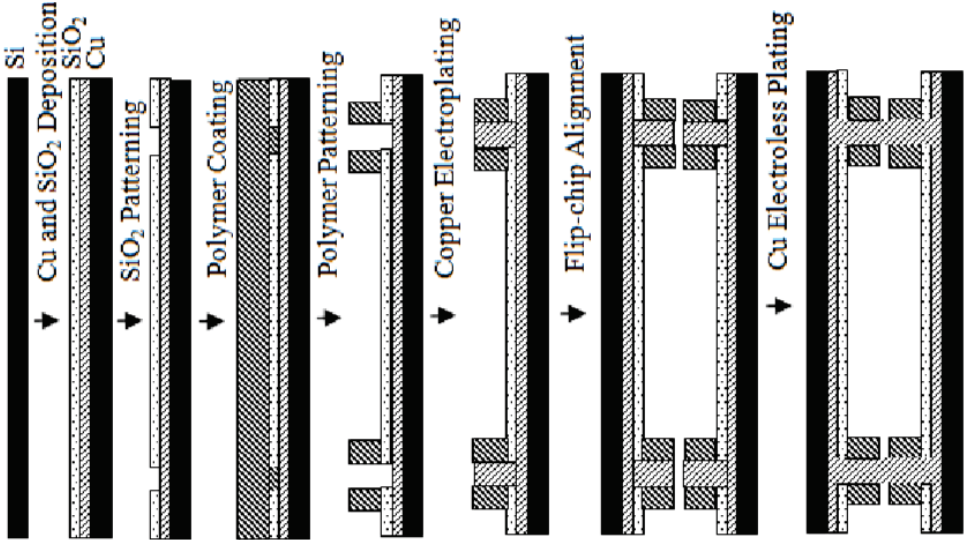


Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>“To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin-coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10mm x 10mm test samples for bonding to fabricated silicon test chips.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>“Bonding of copper pillars between Si and FR-4 was demonstrated and showed that the recrystallization and bonding process for the copper joining is maintained even under the CTE mismatch stress of the package.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [112].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<i>See, e.g.:</i>
--	-------------------



Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

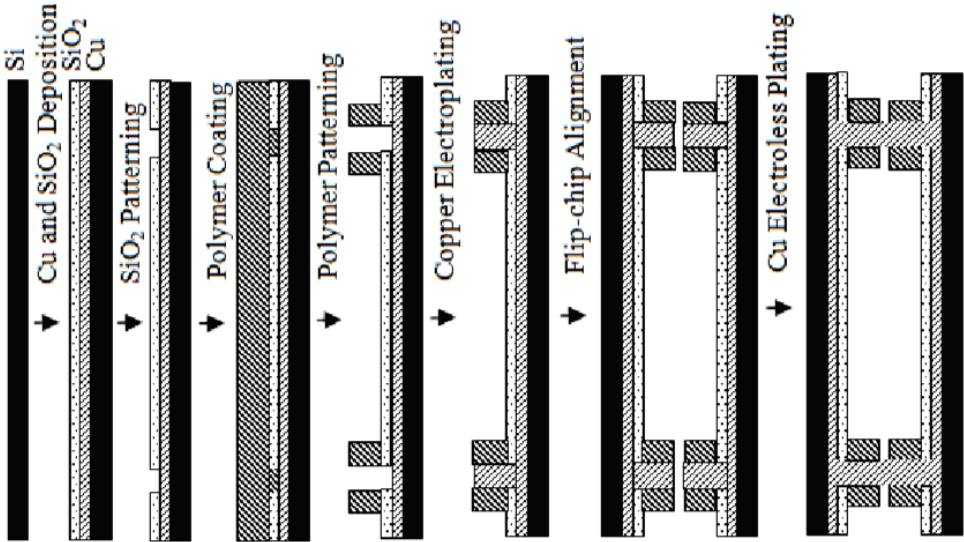
	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Figure 1.1: Illustration of (a) chip-to-substrate wire bonding, (b) chip-to-substrate flip-chip interconnection, and (c) chip on board flip chip connection 2” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [9].</p> <p>“To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin-coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10mm x</p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>10mm test samples for bonding to fabricated silicon test chips.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>“Samples were made using the flip-chip alignment, electroless plating, and low temperature annealing process described above. An anneal temperature of 180°C for one hour was used. Bonding between silicon and the organic materials is unique versus the silicon-to-silicon bonding tests in that the materials no longer have the same coefficient of thermal expansion (CTE). The CTE of Si is 3 ppm/°C versus 14 ppm/°C for FR-4 and 15 ppm/°C for BT. During the annealing process, the copper interconnects will be under shear stress conditions.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [71].</p> <p>“After annealing, the samples were shear tested and compared to silicon-to-silicon bonded samples annealed at the same temperature. The silicon-to-board bonded samples exhibit different failure characteristics versus silicon-to-silicon bonding. Since the Avarel is no longer a single polymer collar surrounding the copper pillar on the organic substrate, but instead a continuous polymer film, it can no longer detach from the surface easily during shear force testing.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [72].</p> <p>“An example of successful bonding chip-to-substrate that survived the destructive shear force testing is shown in cross-section in Figure 4.7. It exhibits very uniform cross-section and no interfaces between the bonded pillar structures. All of the samples tested showed no visible degradation of the organic board materials.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [72].</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>“Bonding of copper pillars between Si and FR-4 was demonstrated and showed that the recrystallization and bonding process for the copper joining is maintained even under the CTE mismatch stress of the package.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [112].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>



Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>



Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p>

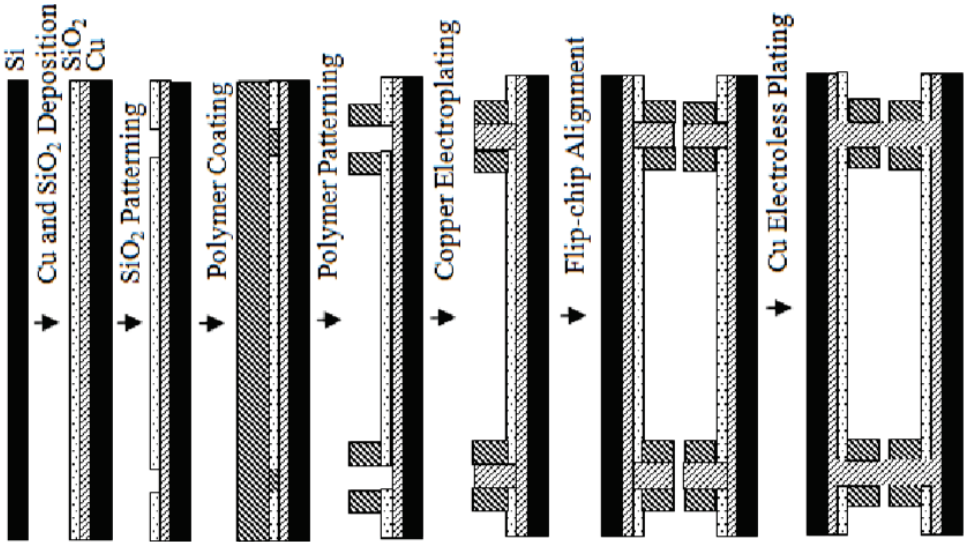


Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>



Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

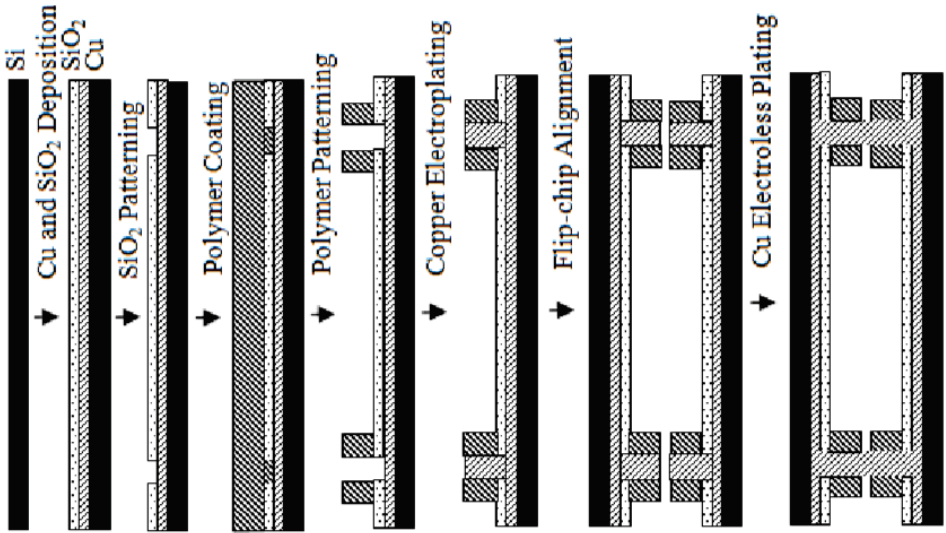
	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“The aligned samples were then placed into a copper electroless plating bath. The bath used was Circuposit 3350 from Shipley Corporation. In this bath the reducing agent is</p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

spacer connector via the corresponding top metal pads of the spacer connector.	formaldehyde (2 g/L), complexing agent is EDTA (ethylenediaminetetraacetic acid) (35 g/L), and also contains sodium hydroxide reaching a pH of 12.5. The electroless plating process proceeded at room temperature for 18 hours with stirring and nitrogen purging. After electroless plating the samples were annealed in a nitrogen environment for one hour at various temperatures. In addition some samples were annealed after electroplating but prior to the flip-chip alignment, electroless plating, and post-bonding anneal steps.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [53].
--	--



Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, FIG. 3.1</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

<p>package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>“The fabrication process flow diagram is shown in Figure 3.1. A seed layer consisting of Cr/Cu/Ti (50nm/500nm/10nm) was DC sputtered onto a bare <100> 4” Si wafer. Then, a Unaxis PECVD system was used to deposit 1.5 μm of silicon dioxide at 250°C on top of the Ti layer. Microposit SC1813 photoresist (Shipley Corporation) was spun on the silicon dioxide surface. After photo-patterning the photoresist layer, buffered oxide etch (BOE) was used to etch the SiO₂ and Ti layers in the exposed areas down to the underlying Cu seed layer. Remaining photoresist was removed by acetone rinsing. Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface. The spin speed for the polymer was 500 RPM for 60 seconds. After spin-coating, a 100°C soft-bake was performed on a hotplate for 40 minutes. The Avatrel layer was then photo-patterned using 250 mJ/cm² dose at 365nm wavelength. Following exposure a post-exposure bake was applied in an oven at 100°C for 20 minutes. Then, the layer was developed in BioAct EC-7R Defluxer for 30 seconds immersed in an ultra-sonic bath. The polymer pattern generated high aspect ratio hollow core molds for copper pillar electroplating. 33 Si Cu and SiO₂ Deposition SiO₂ Patterning Polymer Coating SiO₂ Cu Polymer Patterning Copper Electroplating Flip-chip Alignment Cu Electroless Plating Figure 3.1: Fabrication flow for fabrication of all-copper interconnects structures After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M- 34 10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held together with a low temperature melting wax. The aligned samples were then placed into a copper electroless plating bath. The bath used was Circuposit 3350 from Shipley Corporation. In this bath the reducing agent is formaldehyde (2 g/L),</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>complexing agent is EDTA (ethylenediaminetetraacetic acid) (35 g/L), and also contains sodium hydroxide reaching a pH of 12.5.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [50-53].</p> <p>“After electroless plating the samples were annealed in a nitrogen environment for one hour at various temperatures. In addition some samples were annealed after electroplating but prior to the flip-chip alignment, electroless plating, and post-bonding anneal steps.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [53].</p> <p>“To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin- coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10mm x 10mm test samples for bonding to fabricated silicon test chips. Sputter Ti & Spin Coat Polymer Photo-define Openings for Pillars Copper Electroplating Alignment & Electroless Plating Figure 3.3: Substrate side fabrication flow diagram” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [54].</p> <p>“Figure 4.1 is a cross-section of the two joined pillars after the plating process but before annealing. In Figure 4.1 the two pillars are labeled as Cu and each silicon test surface is also labeled as Si. There is a distinct interface between the two electroless plated regions. The interface between the pillars is evident as a dark crevice between the two copper regions.”</p>
--	---

Appendix A-45 - Invalidity of U.S. Patent No. 9859202 in view of All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices - Non-Patent Publication

	<p>All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [63].</p> <p>“Cross-sections were made after annealing for a shortened period of time at lower temperature (150 ° C) to analyze the change from the distinct unannealed interface to the continuous smooth copper observed in the fully annealed structures. In Figure 4.2a, the interface is still present after 30 minutes at 150°C. After an additional 30 minutes at 180°C (Figure 4.2b) the interface has been removed entirely and the copper bonding process has completed.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [64-65].</p> <p>“Electroless deposition for gold requires is more difficult than copper, since the gold-cyanide complex is very strong, a stronger reducing agent is required, hydrazine. In addition, the reactions will not take place on poor catalyst surfaces at any appreciable rate. This means that using previously fabricated copper pillars is not possible without depositing a suitable catalyst layer prior to the electroless gold process. Palladium is an excellent catalyst for the hydrazine oxidation reaction and therefore was chosen to catalytically activate the copper pillar surfaces before gold deposition.” All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices, [98].</p> <p>To the extent Plaintiff contends that All-Copper Chip-to-Substrate Interconnects for High Performance Integrated Circuit Devices fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

E.D. Tex. Case No. 2:25-CV-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects was published by Aibin Yu, et al. Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects anticipates and/or renders obvious all Asserted Claims¹ of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.² Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects is an academic article that was published July 18, 2011. Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects is therefore prior art to the ’202 patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, or otherwise rendered obvious by disclosures and teachings of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative,

¹ As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

² To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ‘202 patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

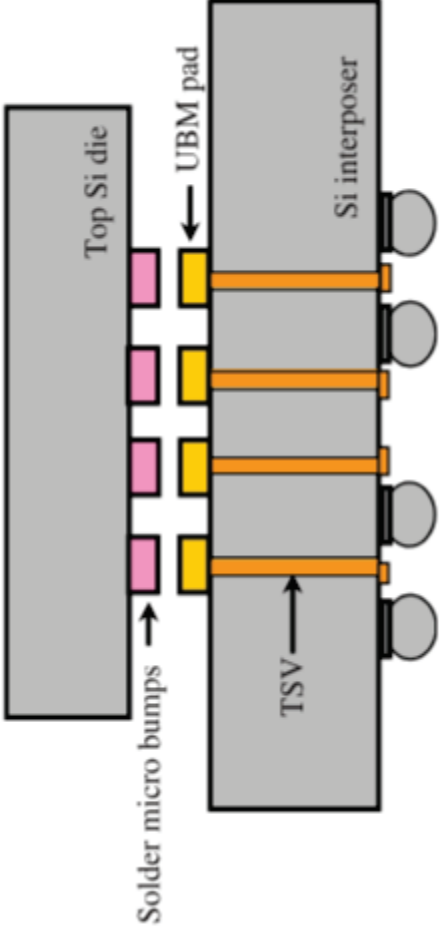
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects set forth in this chart.

Claim 1, U.S. Patent No. 9859202

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	 <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm. Above the TSV is UBM pad. In this paper, ENIG is used as the UBM layer.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>
--	--

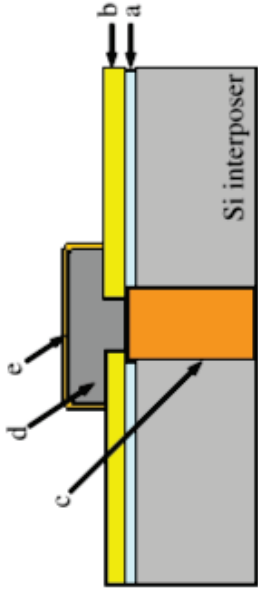
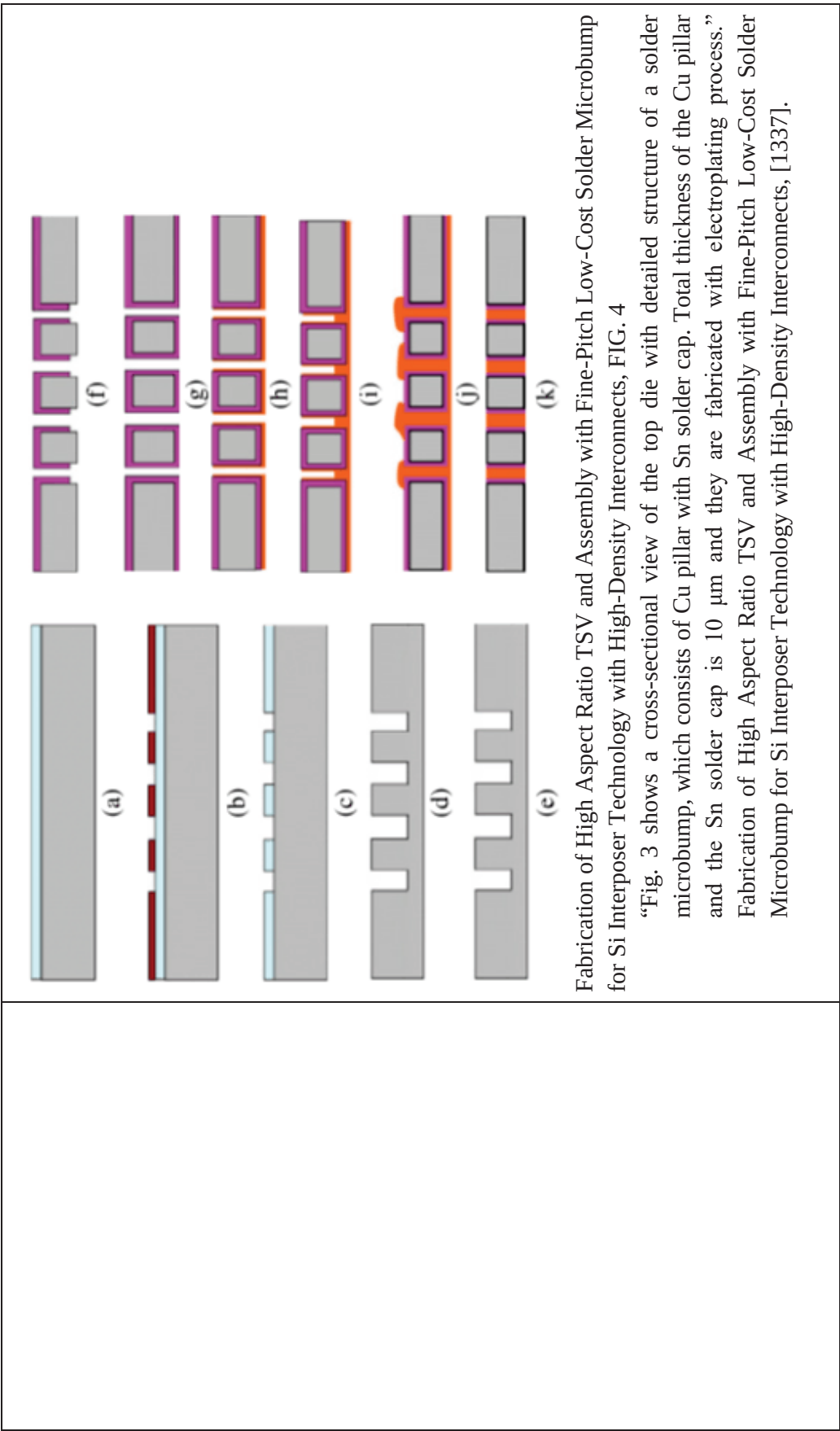
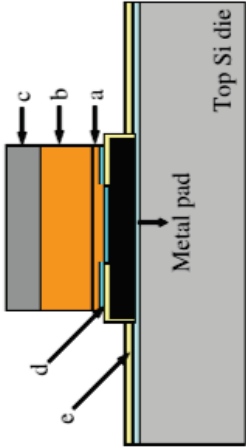


Fig. 2. Schematic cross-sectional view of UBM pad (ENIG) on the Si interposer (not in scale). (a) Passivation layer 1. (b) Passivation layer 2. (c) TSV filled with Cu. (d) Electroless plated Ni. (e) Immersion Au.

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 2

“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].



	<div></div> <div><p>Fig. 3. Schematic cross-sectional view of the Cu pillar and Sn cap on the top die (not in scale). (a) Cu seed layer. (b) Plated Cu. (c) Plated Sn. (d) Ti adhesion layer. (e) Passivation layer.</p></div> <div><p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 3</p></div> <div><p>“Solder micro bumps Fig. 1. TSV Top Si die UBM pad-c ← b a 1337 Metal pad Top Si die Si interposer Fig. 3. Schematic cross-sectional view of the Cu pillar and Sn cap on the top die (not in scale). (a) Cu seed layer. (b) Plated Cu. (c) Plated Sn. (d) Ti adhesion layer. (e) Passivation layer. Schematic drawing of packaging structure (not in scale).” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p></div>
--	--

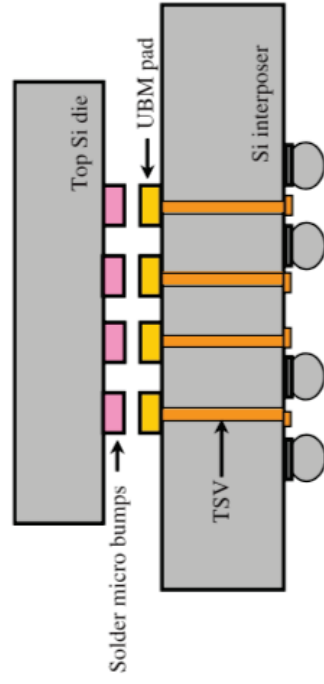
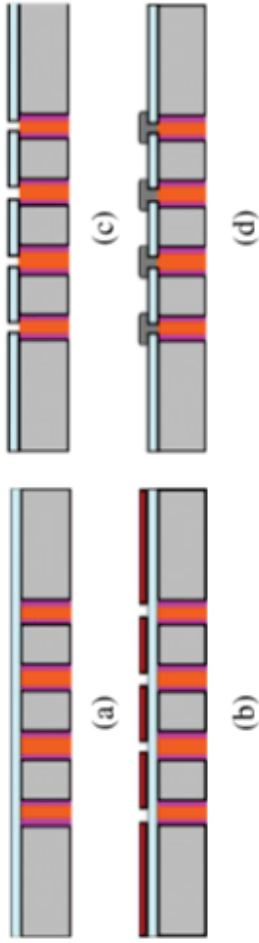


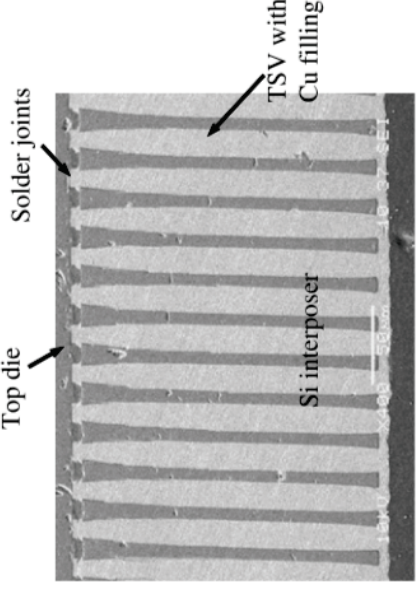
Fig. 1. Schematic drawing of packaging structure (not in scale).

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1

“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.”
Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].



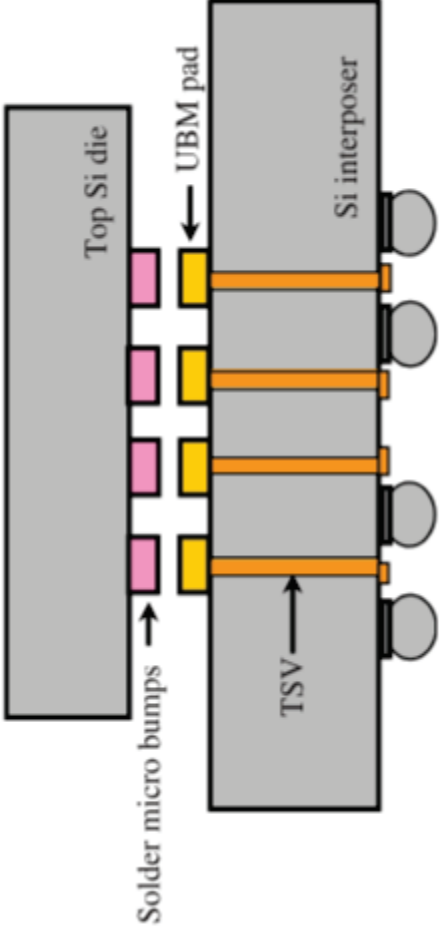
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5</p> <p>“Fig. 18 shows the cross section of the top die and the Si interposer joined together at selected bonding conditions. It can be seen that successful joining is achieved.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].</p>  <p>Fig. 18. Cross section of the top die and the Si interposer joined together.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 18</p> <p>“After fabrication of the CuSn solder microbumps on the top die and the ENIG UBM pads on top of the TSVs on the Si interposer, the top die and the interposer are joined together using a FC150 flip chip bonder.” Fabrication of High Aspect Ratio TSV and Assembly with</p>
--	---

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].</p>
<p>[1.A] a bottom package substrate;</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	 <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>
--	---

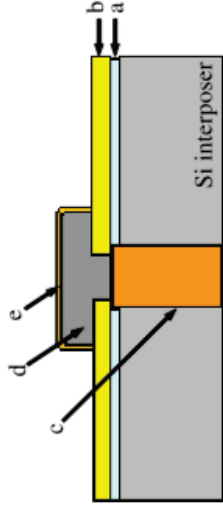


Fig. 2. Schematic cross-sectional view of UBM pad (ENIG) on the Si interposer (not in scale). (a) Passivation layer 1. (b) Passivation layer 2. (c) TSV filled with Cu. (d) Electroless plated Ni. (e) Immersion Au.

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 2

“A. Design of TSV and UBM Pads on Si Interposer Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm . Above the TSV is UBM pad.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].

“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm . Above the TSV is UBM pad. In this paper, ENIG is used as the UBM layer.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].

“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p>
--	--

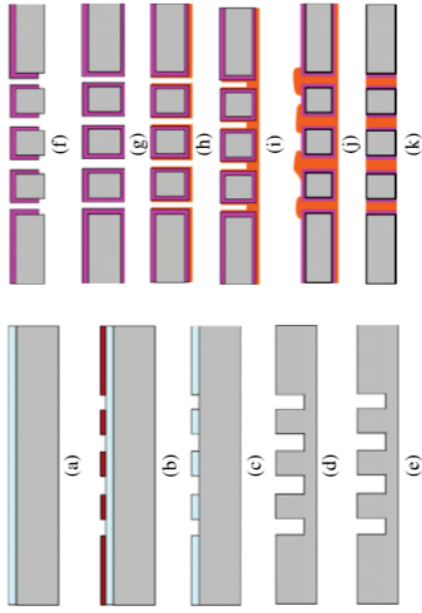
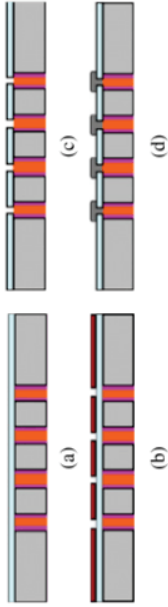
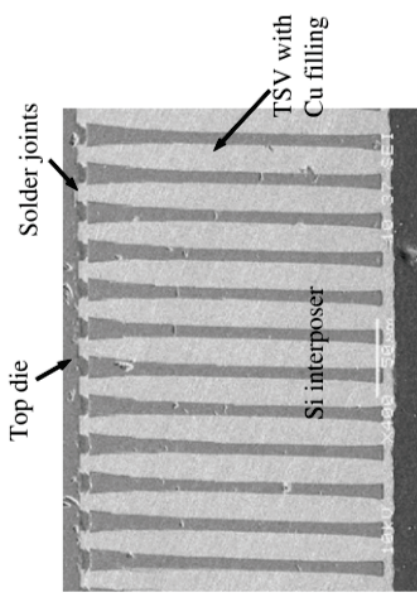


Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm .

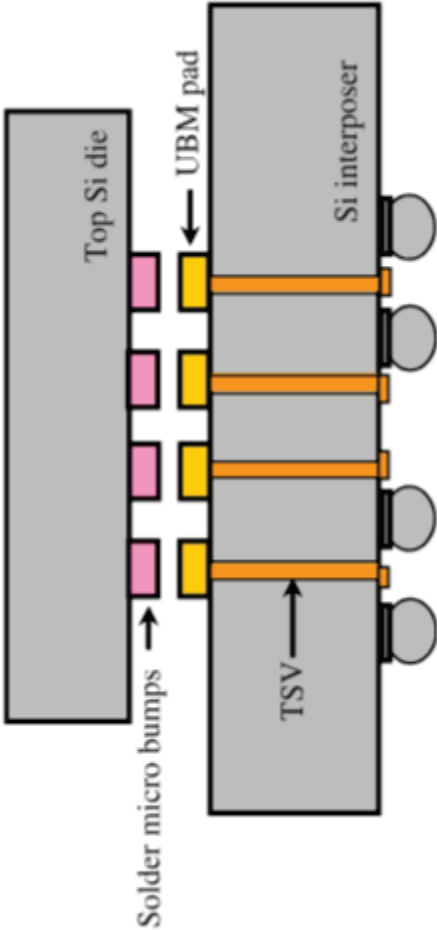
Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 4

“B. Fabrication of ENIG UBM Pads on Si Carrier The ENIG UBM pads are fabricated on top of the TSVs. Fig. 5 shows the process flow. First, a layer of dielectric is deposited on the top of the wafer Fig. 5(a).” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].

	<p>“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.”</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p>  <p>Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5</p> <p>“Fig. 18 shows the cross section of the top die and the Si interposer joined together at selected bonding conditions. It can be seen that successful joining is achieved.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].</p>
--	---

	<div><p>Top die</p><p>Solder joints</p><p>TSV with Cu filling</p><p>Si interposer</p></div> <div><p>Fig. 18. Cross section of the top die and the Si interposer joined together.</p></div> <div><p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 18</p></div> <div><p>“After fabrication of the CuSn solder microbumps on the top die and the ENIG UBM pads on top of the TSVs on the Si interposer, the top die and the interposer are joined together using a FC150 flip chip bonder.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].</p></div> <div><p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, e.g.:</p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>The diagram illustrates a cross-sectional view of a packaging structure. At the top is a grey rectangular block labeled 'Top Si die'. Below it, a row of pink rectangular blocks is labeled 'Solder micro bumps' with an arrow pointing to them. Underneath the bumps is a row of yellow rectangular blocks labeled 'UBM pad' with an arrow pointing to them. Below the UBM pads is a row of orange vertical bars labeled 'TSV' with an arrow pointing to them. At the bottom is a grey rectangular block labeled 'Si interposer' with an arrow pointing to it. The TSVs connect the UBM pads to the Si interposer.</p>
---	---

	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“A. Design of TSV and UBM Pads on Si Interposer Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p> <p>“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm. Above the TSV is UBM pad. In this paper, ENIG is used as the UBM layer.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p> <div></div> <p>Fig. 2. Schematic cross-sectional view of UBM pad (ENIG) on the Si interposer (not in scale). (a) Passivation layer 1. (b) Passivation layer 2. (c) TSV filled with Cu. (d) Electroless plated Ni. (e) Immersion Au.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 2</p> <p>“B. Design of Solder Microbump on the Si Top Die Fig. 3 shows a cross-sectional view of the top die with detailed structure of a solder microbump, which consists of Cu pillar with Sn</p>
--	---

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>solder cap.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p> <p>“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p>
--	---

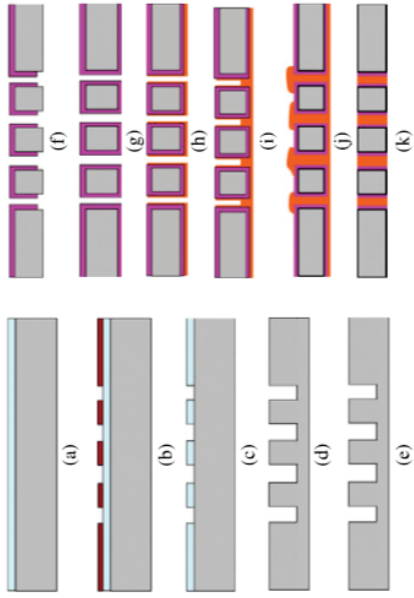


Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 4

“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.”
Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].

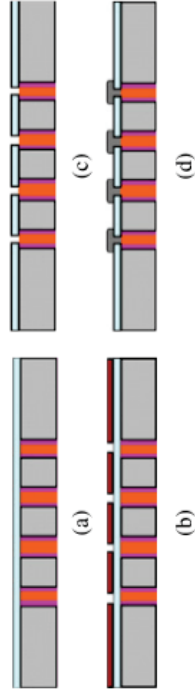


Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5

“After fabrication of the CuSn solder microbumps on the top die and the ENIG UBM pads on top of the TSVs on the Si interposer, the top die and the interposer are joined together using a FC150 flip chip bonder.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].

“Fig. 18 shows the cross section of the top die and the Si interposer joined together at selected bonding conditions.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].

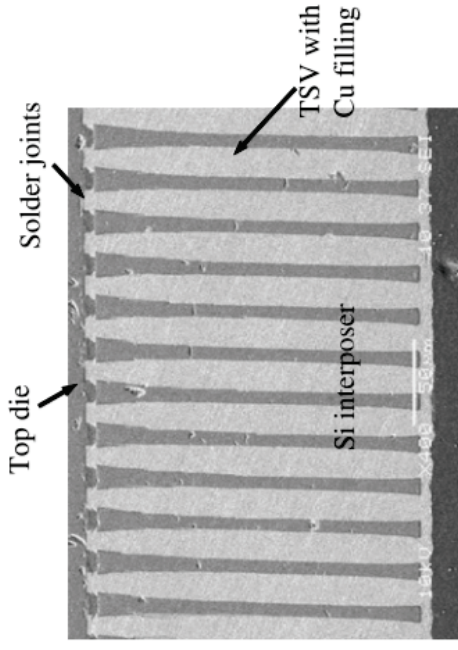


Fig. 18. Cross section of the top die and the Si interposer joined together.

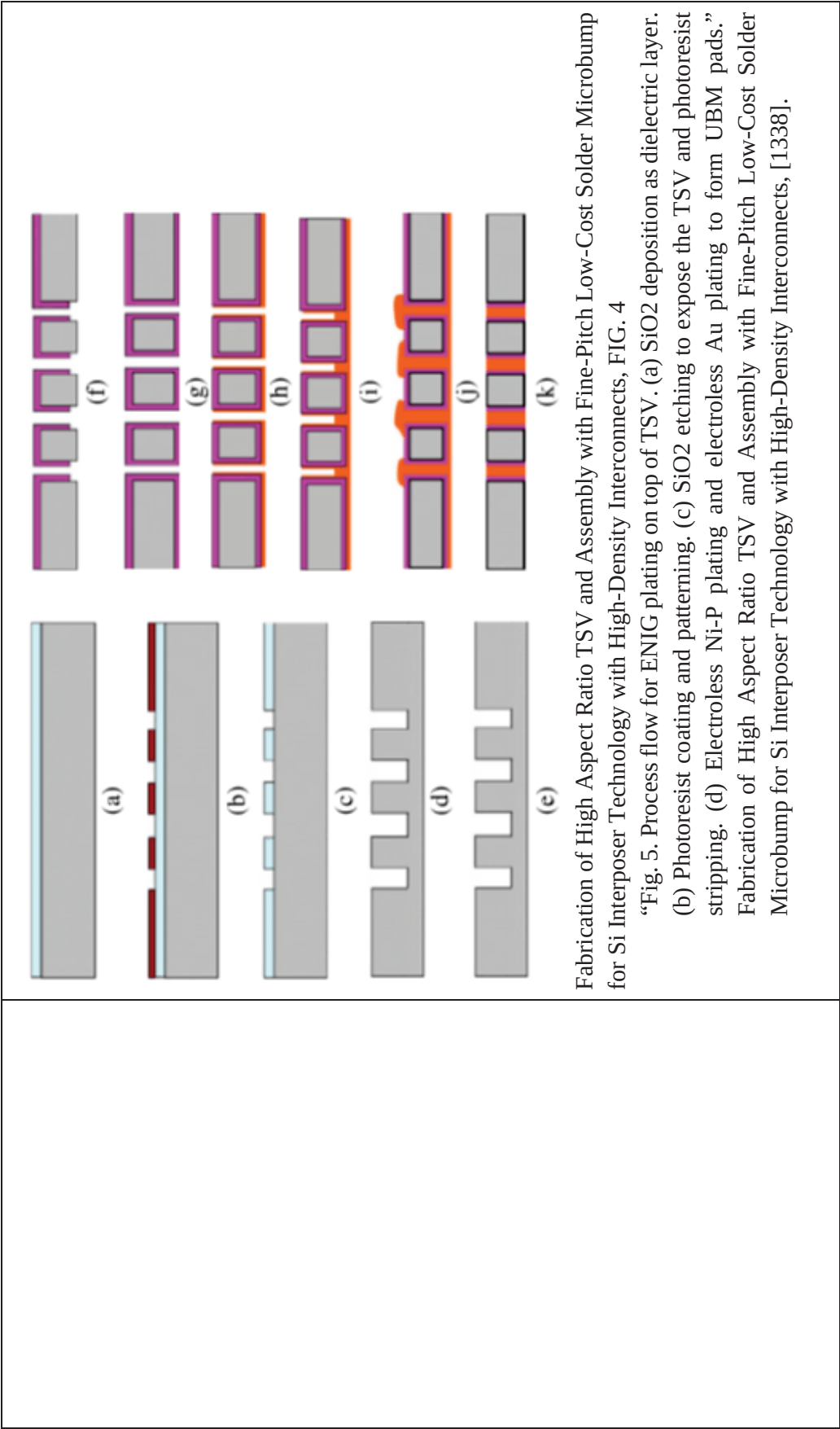
Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 18

“Mechanical modeling shows that with underfill between the top Si die and the Si interposer, the normal stress at the solder micro-joints is greatly reduced and the substrate core thickness has little effect on the stress at the solder micro-joints [17].” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1342].

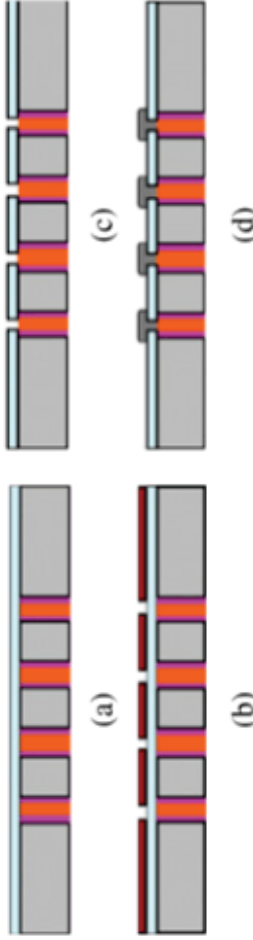
To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based

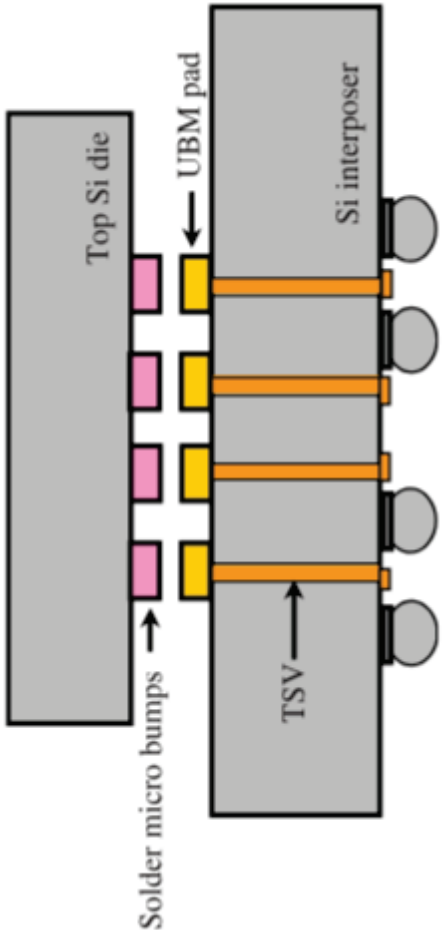
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p> <p>“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p>
---	--

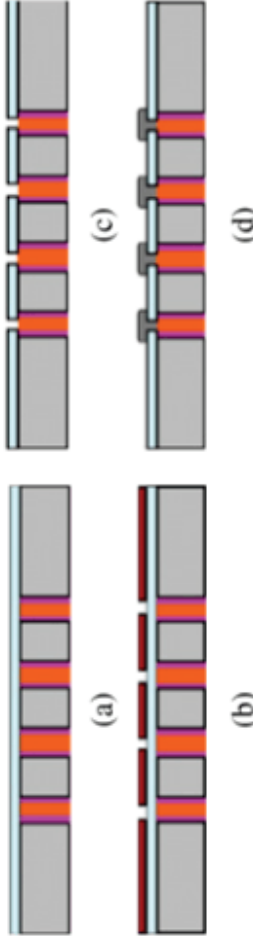


Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	 <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring.” Fabrication of High Aspect Ratio TSV</p>

	<p>and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.”</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p>
--	--

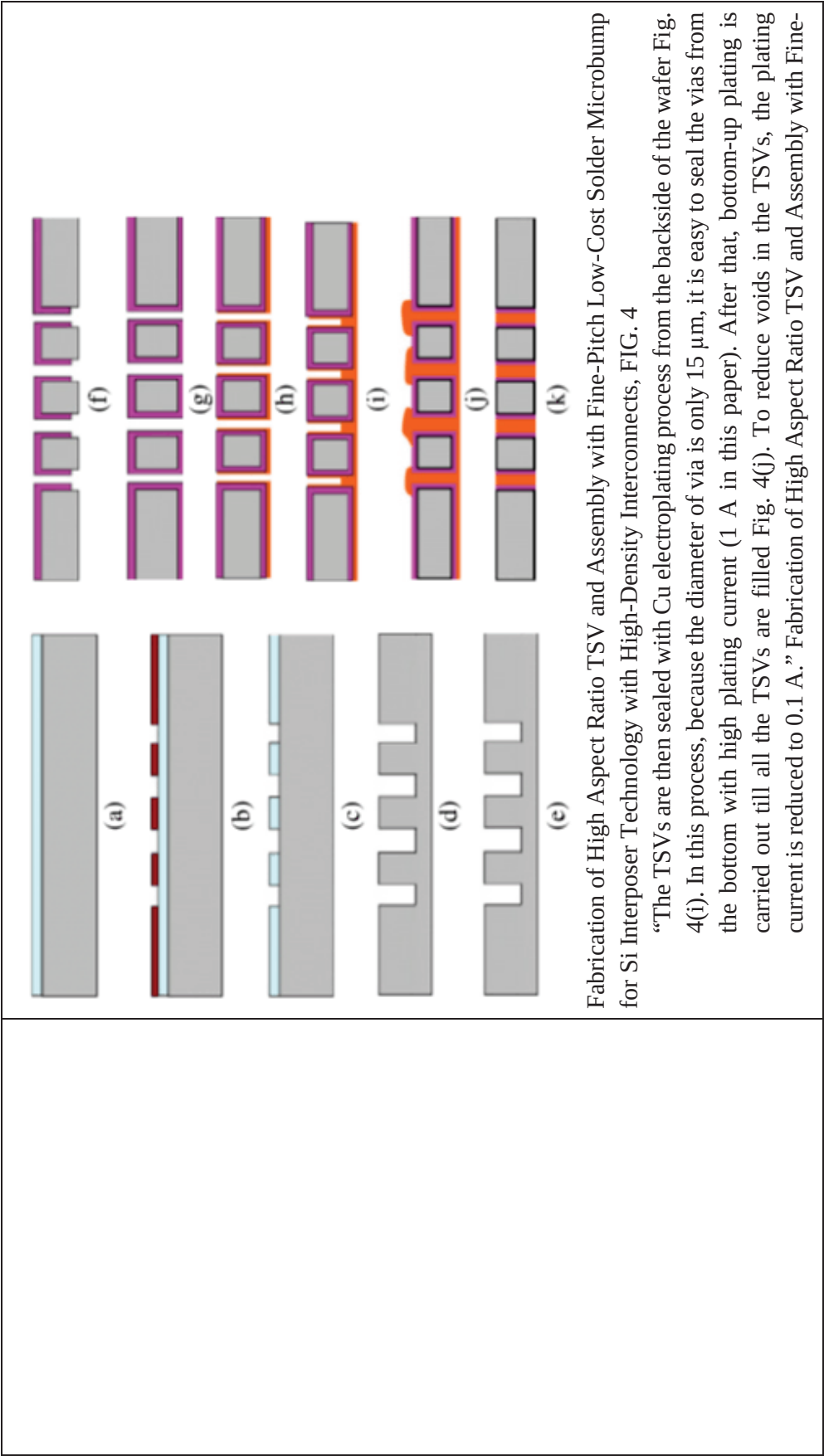
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

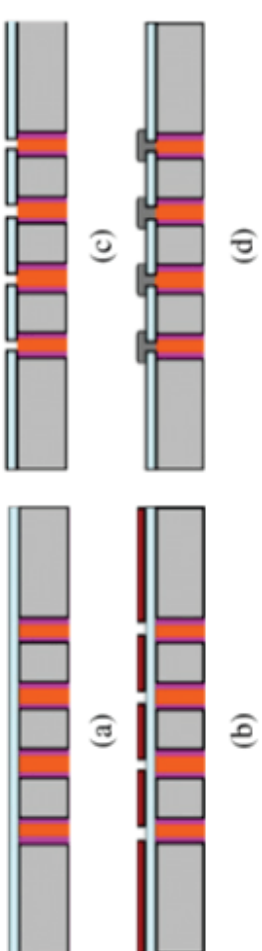
	 <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring.” Fabrication of High Aspect Ratio TSV</p>

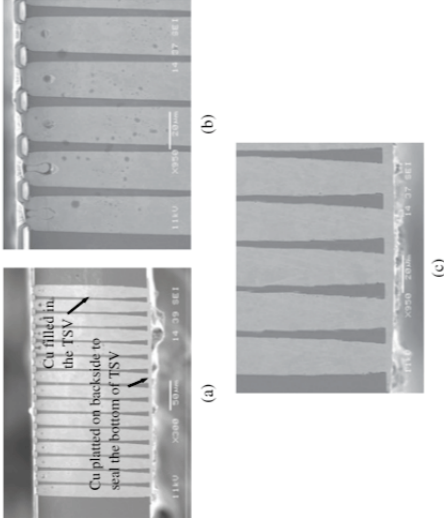
	<div> <p>and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p> </div> <div> </div> <div> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> </div> <div> <p>“In this paper, fine pitch solder microbumps and high aspect ratio TSVs filled with Cu are fabricated and integrated together to form high-density interconnects between a Si chip and a Si interposer. The technology is mainly used for Si interposer technology with high-density interconnect.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p> </div> <div> <p>“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO2 deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO2 etch and photoresist stripping. (d) TSV</p> </div>
--	---

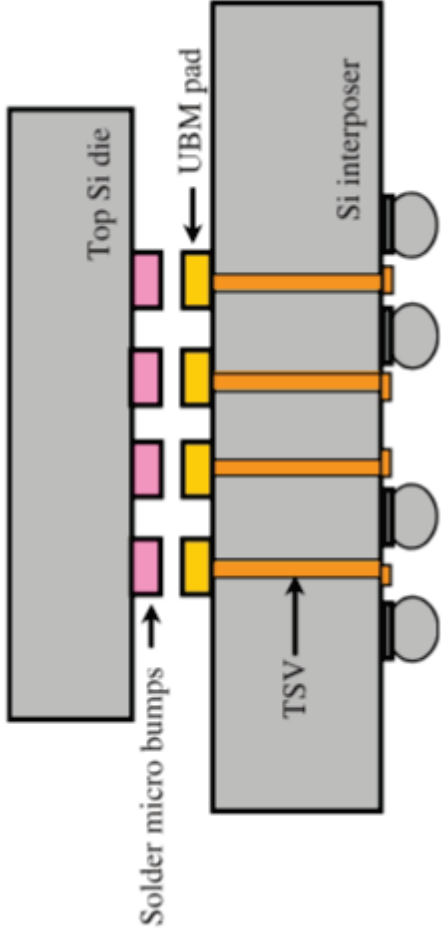
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p>
--	--



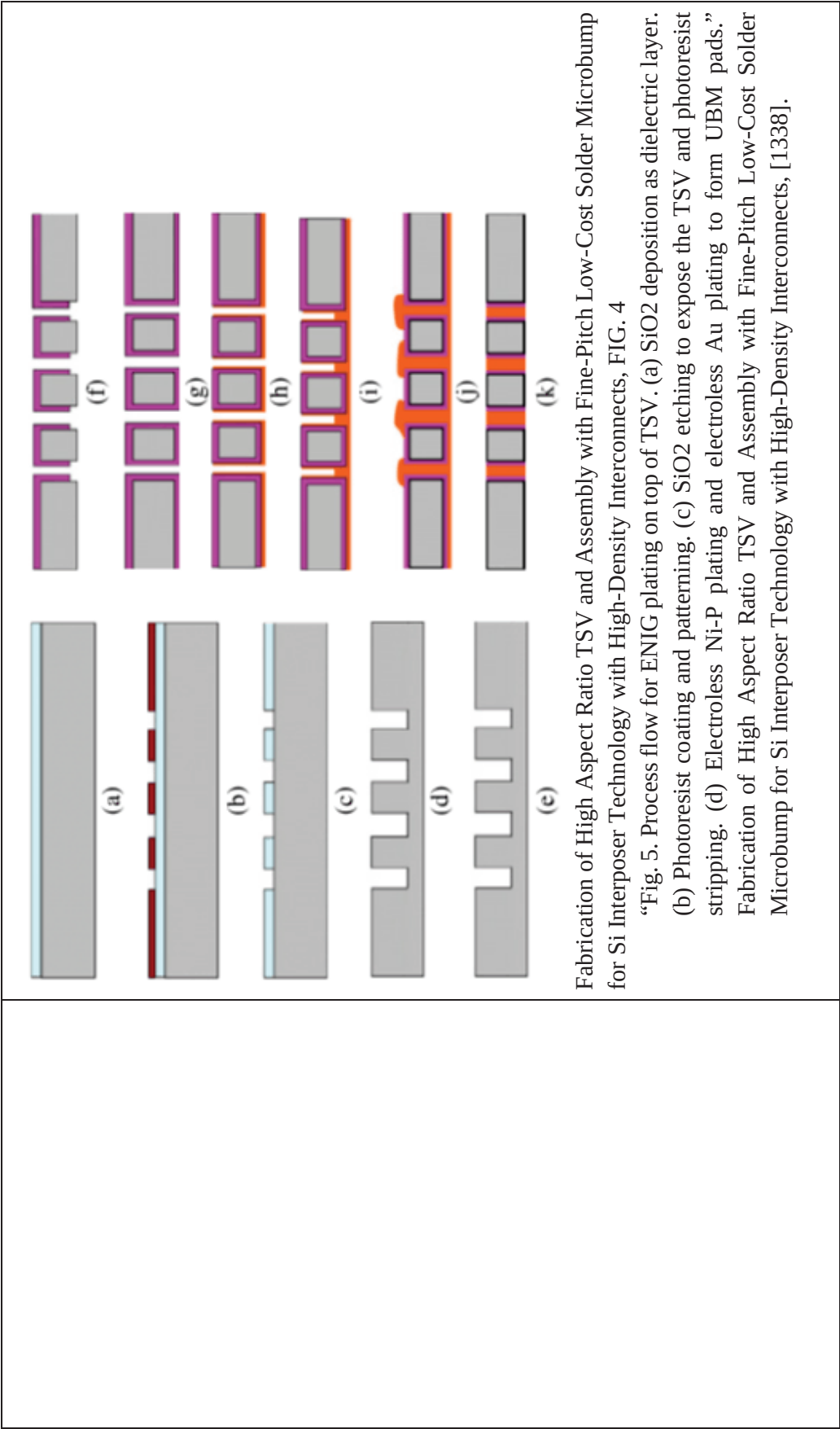
	<p>Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p> <p>“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p>  <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5</p> <p>“Fig. 14(a) and (b) shows that all the TSVs are filled with Cu whereas some tiny voids still exist at the top side of the TSV. On further thinning down the wafer, those tiny voids can be fully removed.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1340].</p>
--	--

	 <p>Fig. 14. Cross section of TSVs after Cu plating and thinning down to 170 μm shows some tiny voids at the top of TSVs (a) overview, (b) zoomed view of TSV upside (with some smears on the cross-sectional surface because of polishing and cleaning process), and (c) zoomed view of TSV bottom side.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 14</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or</p>

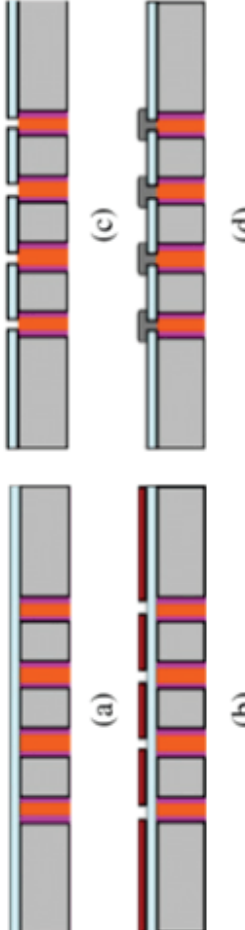
	<p>inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p>See, e.g.:</p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>The diagram is a cross-sectional schematic of a packaging structure. At the top is a grey rectangular block labeled 'Top Si die'. Below it, a row of pink rectangular blocks is labeled 'Solder micro bumps' with an arrow pointing to them. Below the bumps is a row of yellow rectangular blocks labeled 'UBM pad' with an arrow pointing to them. Below the pads is a row of orange vertical bars labeled 'TSV' with an arrow pointing to them. At the bottom is a grey rectangular block labeled 'Si interposer'. On the right side of the Si interposer, there are four circular solder bumps. The TSVs connect the UBM pads to the Si interposer.</p>
--	--

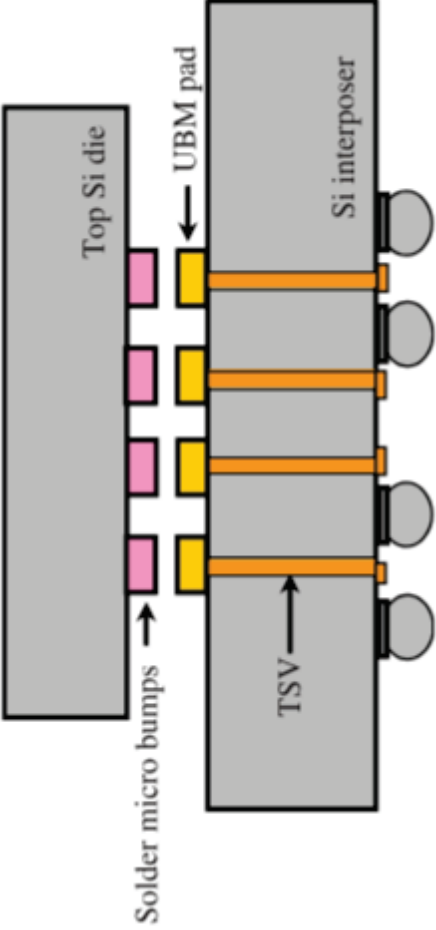
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PTEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p>
--	--



Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

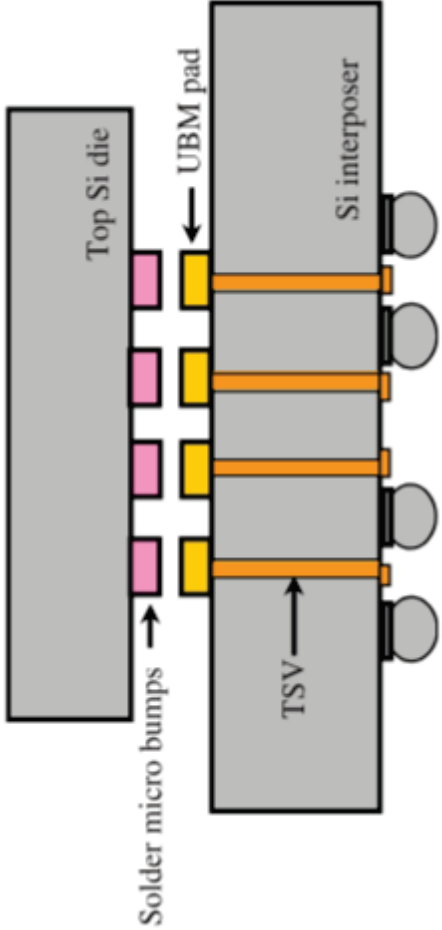
	 <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5</p> <p>“The ENIG UBM pads are fabricated on top of the TSVs. Fig. 5 shows the process flow. First, a layer of dielectric is deposited on the top of the wafer Fig. 5(a). Then a thin layer of photoresist is spin coated and patterned Fig. 5(b). After that, the dielectric layer is etched to expose the TSVs and the photoresist is stripped Fig. 5(c). Finally, electroless Ni-P plating with immersion of Au is done to form the UBM pads Fig. 5(d).” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars</p>	<p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or</p>

<p>protrudes downwardly from a bottom surface of the core substrate,</p>	<p>inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, e.g.:</p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>The diagram is a cross-sectional schematic of a packaging structure. At the top is a grey rectangular block labeled 'Top Si die'. Below it, a row of pink rectangular blocks is labeled 'Solder micro bumps' with an arrow pointing to them. Underneath the bumps is a row of yellow rectangular blocks labeled 'UBM pad' with an arrow pointing to them. Below the UBM pads is a grey rectangular block labeled 'Si interposer'. Inside the Si interposer, there are several vertical orange lines representing TSVs, with one labeled 'TSV' and an arrow pointing to it. At the bottom of the Si interposer, there are four circular solder bumps.</p>
--	---

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“The TSVs are then sealed with Cu electroplating process from the backside of the wafer Fig. 4(i). In this process, because the diameter of via is only 15 μm, it is easy to seal the vias from the bottom with high plating current (1 A in this paper). After that, bottom-up plating is carried out till all the TSVs are filled Fig. 4(j). To reduce voids in the TSVs, the plating current is reduced to 0.1 A.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO</p>

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“After fabrication of the CuSn solder microbumps on the top die and the ENIG UBM pads on top of the TSVs on the Si interposer, the top die and the interposer are joined together using a FC150 flip chip bonder.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].</p>
--	--

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

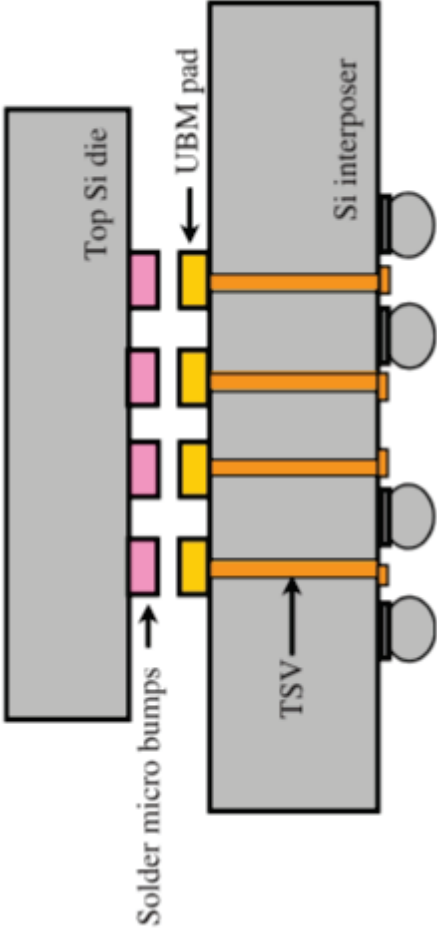
	<p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>

	<div></div> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm. Above the TSV is UBM pad. In this paper, ENIG is used as the UBM layer.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p> <p>“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PATEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the</p>
--	--

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p> <p>“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p>

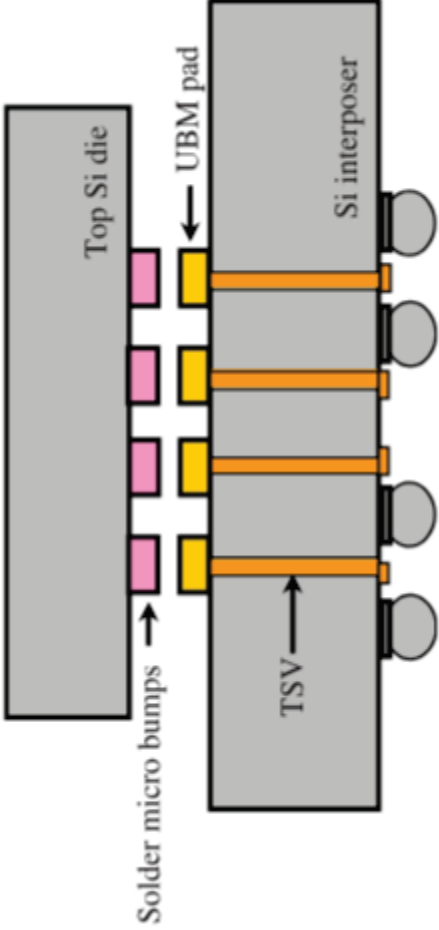
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>The diagram illustrates a cross-sectional view of a packaging structure. At the top is a grey rectangular block labeled 'Top Si die'. Below it, a row of pink rectangular blocks is labeled 'Solder micro bumps' with an arrow pointing to them. These bumps are connected to a row of yellow rectangular blocks labeled 'UBM pad' with an arrow pointing to them. Below the UBM pads are several vertical orange bars labeled 'TSV' with an arrow pointing to one of them. These TSVs are embedded in a grey block labeled 'Si interposer'. At the bottom of the Si interposer, there are four circular solder microbumps.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the Si interposer, there are TSVs that are filled with Cu and on top of the TSV, electroless nickel and immersion gold (ENIG) under bump metallurgy (UBM) pads are plated. The top Si die and the Si interposer are stacked together by joining the solder microbumps and the ENIG pads.”</p>
--	--

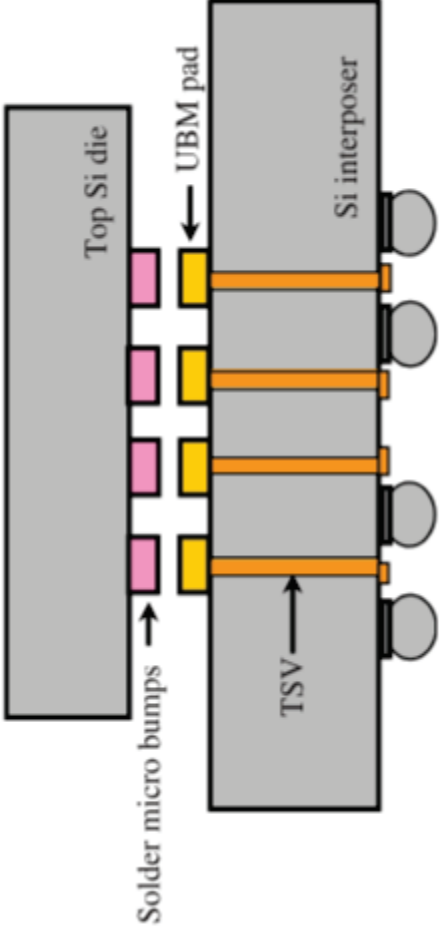
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p> <p>“After fabrication of the CuSn solder microbumps on the top die and the ENIG UBM pads on top of the TSVs on the Si interposer, the top die and the interposer are joined together using a FC150 flip chip bonder.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein.</p> <p><i>See, e.g.:</i></p>

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	 <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	 <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>

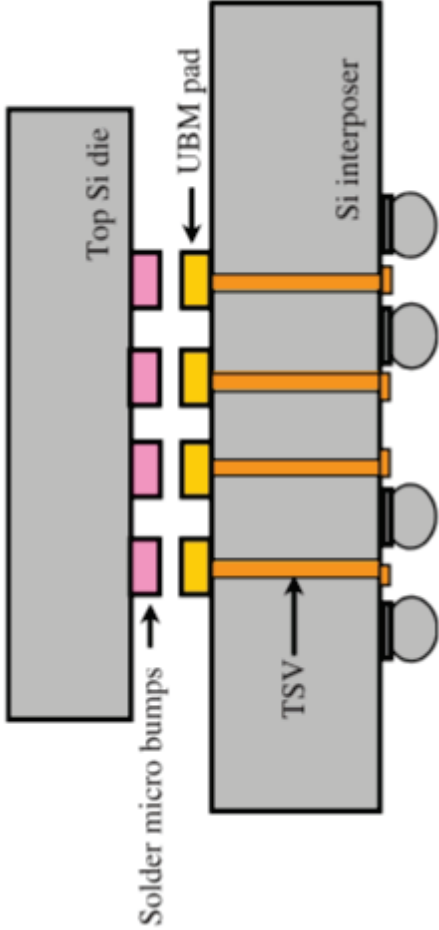
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<div> <p>The diagram is a cross-sectional view of a semiconductor assembly. At the top is a grey rectangular block labeled 'Top Si die'. Below it, a row of pink rectangular blocks is labeled 'Solder micro bumps' with an arrow pointing to them. These bumps are connected to a row of yellow rectangular blocks labeled 'UBM pad' with an arrow pointing to them. Below the UBM pads are four vertical orange bars labeled 'TSV' with an arrow pointing to one of them. These TSVs are connected to a grey rectangular block at the bottom labeled 'Si interposer'. The Si interposer has four circular solder bumps on its bottom surface.</p> </div> <div> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> </div>
--	--

Claim 2, U.S. Patent No. 9859202

Claim Limitation	Disclosure
-------------------------	-------------------

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p>See, e.g.:</p>  <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

Claim 3, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>

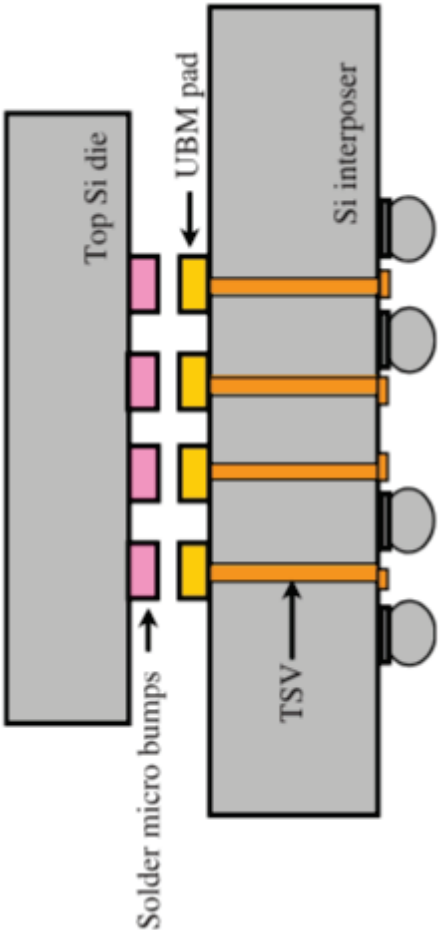
	<div></div> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm. Above the TSV is UBM pad. In this paper, ENIG is used as the UBM layer.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p> <p>“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the</p>
--	--

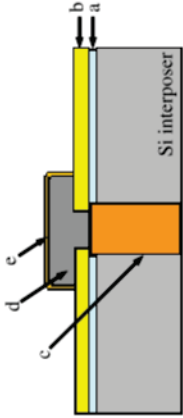
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

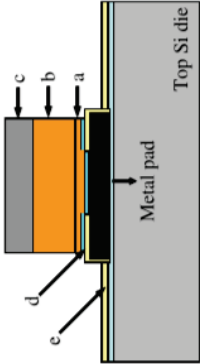
	<p>TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p> <p>“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO2 deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO2 etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

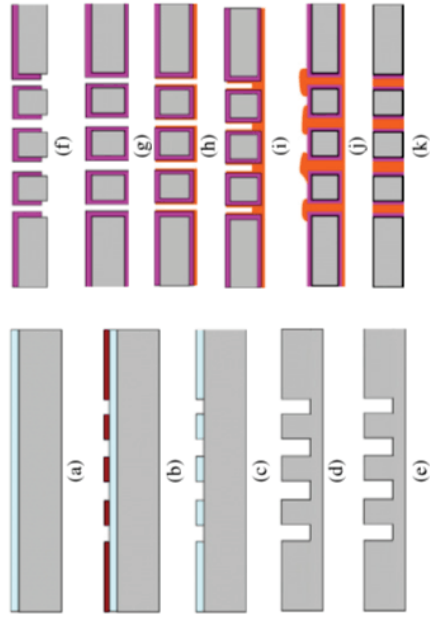
Claim 4, U.S. Patent No. 9859202

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding	Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of

<p>metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>The diagram illustrates a cross-sectional view of a packaging structure. At the top is a grey rectangular block labeled 'Top Si die'. Below it, a row of pink rectangular blocks is labeled 'Solder micro bumps' with an arrow pointing to them. These bumps sit on a yellow rectangular block labeled 'UBM pad'. Below the UBM pad is a grey rectangular block labeled 'Si interposer'. Inside the Si interposer, there are vertical orange lines labeled 'TSV' with an arrow pointing to one of them. At the bottom of the Si interposer, there are four circular solder bumps.</p>
---	--

	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm. Above the TSV is UBM pad.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>Fig. 2. Schematic cross-sectional view of UBM pad (ENIG) on the Si interposer (not in scale). (a) Passivation layer 1. (b) Passivation layer 2. (c) TSV filled with Cu. (d) Electroless plated Ni. (e) Immersion Au.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 2</p> <p>“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm. Above the TSV is UBM pad. In this paper, ENIG is used as the UBM layer.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p> <p>“Fig. 3 shows a cross-sectional view of the top die with detailed structure of a solder microbump, which consists of Cu pillar with Sn solder cap.” Fabrication of High Aspect</p>
--	--

	<p>Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p> <div></div> <p>Fig. 3. Schematic cross-sectional view of the Cu pillar and Sn cap on the top die (not in scale). (a) Cu seed layer. (b) Plated Cu. (c) Plated Sn. (d) Ti adhesion layer. (e) Passivation layer.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 3</p> <p>“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p>
--	--

	<div></div> <div><p>Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Bottom-up plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.</p></div> <div><p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 4</p></div> <div><p>“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p></div>
--	--

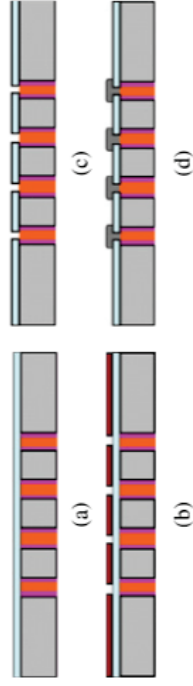


Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5

“Fig. 18 shows the cross section of the top die and the Si interposer joined together at selected bonding conditions. It can be seen that successful joining is achieved.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

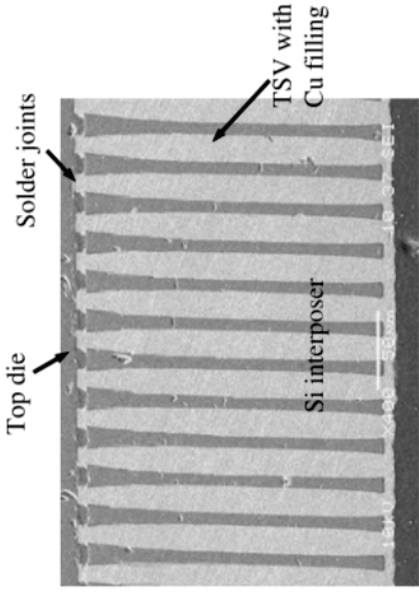


Fig. 18. Cross section of the top die and the Si interposer joined together.

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 18

“After fabrication of the CuSn solder microbumps on the top die and the ENIG UBM pads on top of the TSVs on the Si interposer, the top die and the interposer are joined together using a FC150 flip chip bonder.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].

“After joining, underfills with fine filler size, such as underfills of T693/R3434iHx-2 from Nagase Chemtex Corp. or U8443-14 from Namics, are used to fill the gap between the two Si chips [8].” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].

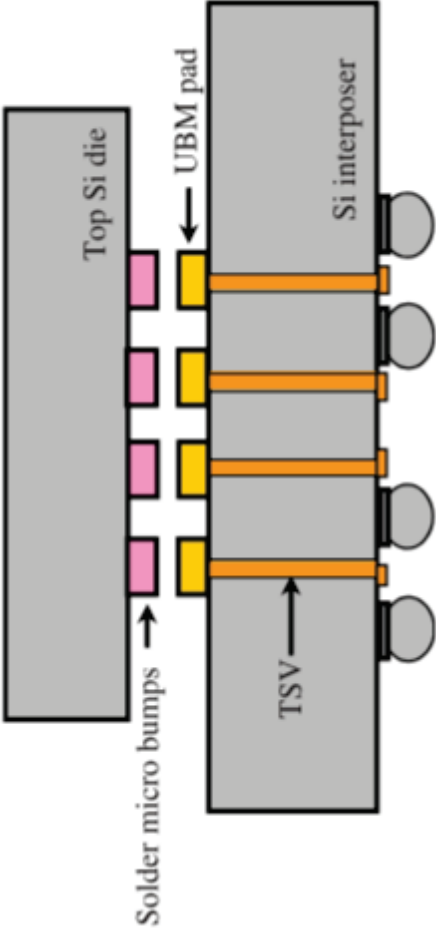
Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

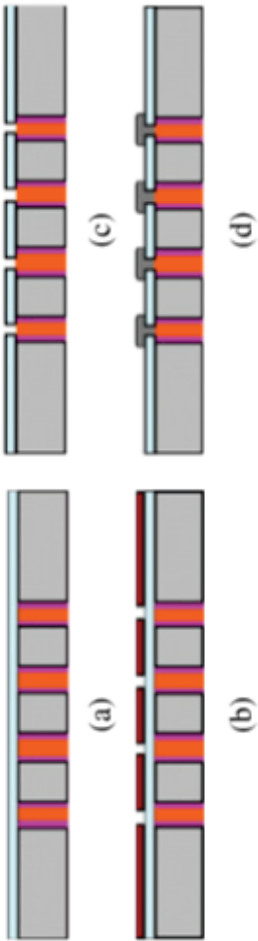
	<p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6, U.S. Patent No. 9859202

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are</p>

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>  <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1</p> <p>“On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the Si interposer, there are TSVs that are filled with Cu and on top of the TSV, electroless nickel and immersion gold (ENIG) under bump metallurgy (UBM) pads are plated. The top Si die and the Si interposer are stacked together by joining the solder microbumps and the ENIG pads.”</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>
--	--

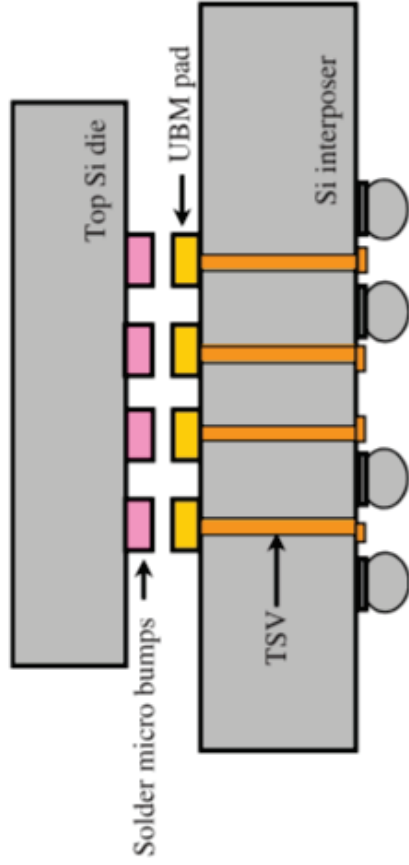
	<p>“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.”</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p>  <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5</p> <p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 9, U.S. Patent No. 9859202

Claim Limitation	Disclosure
------------------	------------

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p>See, e.g.:</p> <p>“Fig. 1 shows a schematic drawing of the packaging structure with a top Si die and a Si interposer. On the top Si die, there are Cu pillars/Sn caps fabricated on it whereas on the TO MEET the miniaturization trend and to reduce power Si interposer, there are TSVs that are filled with Cu and on chip integration with Si interposer technology is studied extensively as it has the potential to provide ultrafine pitch wiring,” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].</p>
--	---



Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 1

“Fig. 2 shows a cross-sectional view of the Si interposer with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm . Above the TSV is UBM pad. In this paper, ENIG is used as the UBM layer.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1336].

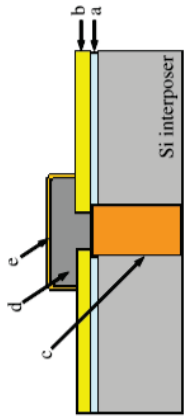


Fig. 2. Schematic cross-sectional view of UBM pad (ENIG) on the Si interposer (not in scale). (a) Passivation layer 1. (b) Passivation layer 2. (c) TSV filled with Cu. (d) Electroless plated Ni. (e) Immersion Au.

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 2

“Fig. 3 shows a cross-sectional view of the top die with detailed structure of a solder microbump, which consists of Cu pillar with Sn solder cap. Total thickness of the Cu pillar and the Sn solder cap is 10 μm and they are fabricated with electroplating process.”
Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].

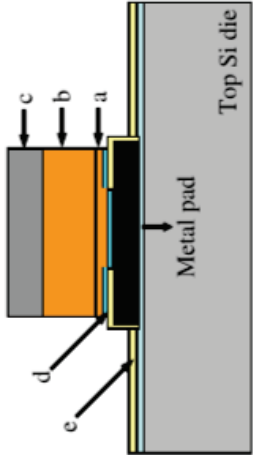
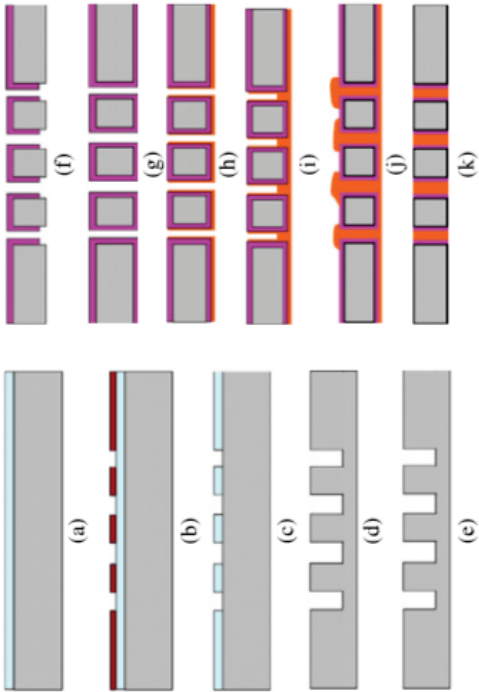


Fig. 3. Schematic cross-sectional view of the Cu pillar and Sn cap on the top die (not in scale). (a) Cu seed layer. (b) Plated Cu. (c) Plated Sn. (d) Ti adhesion layer. (e) Passivation layer.

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 3</p> <p>“After that, a layer of plasma-enhanced tetraethylorthosilicate (PETEOS) is deposited on the front side of the wafer for sidewall passivation Fig. 4(e). Sidewall passivation can also be achieved by thermal oxidation, which can give better uniformity and smoothness of the sidewall. Then the wafer is thinned down to expose the backside of the TSV Fig. 4(f). In order to fully passivate the sidewall of the TSV, another layer of SiO₂ is deposited on the backside of the wafer in a Plasma-” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p>
--	--

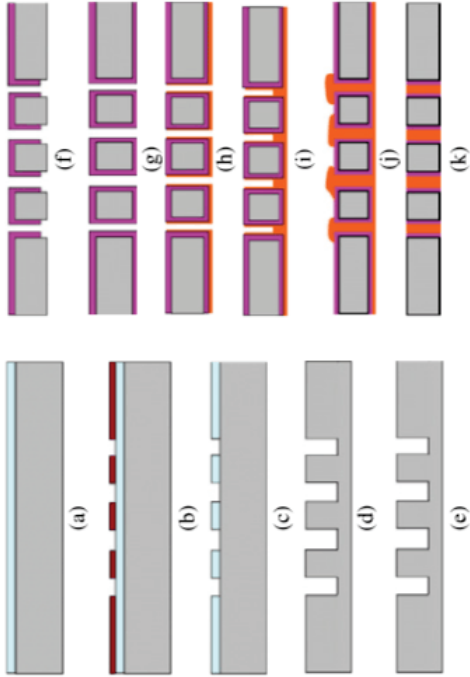
	<div><p>Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.</p></div>
--	--

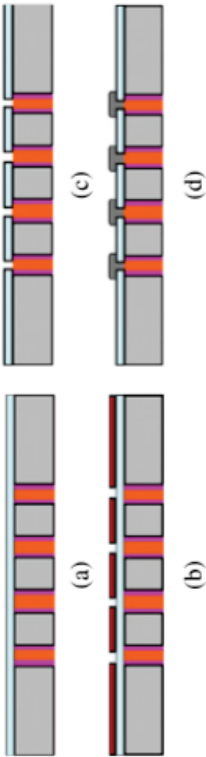
Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 4

“Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<p>the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1337].</p>
--	--

	<div><p>Fig. 4. Process flow for TSV fabrication and Cu filling. (a) SiO₂ deposition as hard mask. (b) Photoresist coating and patterning. (c) SiO₂ etch and photoresist stripping. (d) TSV etching and SiO₂ hard mask removing. (e) PETEOS deposition for sidewall passivation. (f) Wafer thinning to expose the backside of the TSV. (g) SiO₂ deposition on the backside of the wafer. (h) Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. (i) Wafer level plating to seal the TSV from the backside of the wafer. (j) Bottom-up plating till all the TSV is filled. (k) Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm.</p></div>	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 4</p> <p>“Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.”</p>
--	---	--

	<p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1338].</p>  <p>Fig. 5. Process flow for ENIG plating on top of TSV. (a) SiO₂ deposition as dielectric layer. (b) Photoresist coating and patterning. (c) SiO₂ etching to expose the TSV and photoresist stripping. (d) Electroless Ni-P plating and electroless Au plating to form UBM pads.</p> <p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 5</p> <p>“Fig. 15(a) shows the top view of ENIG pads on top of the TSVs. After plating, the diameter of the ENIG pads is about 4 μm larger than the diameter of TSV because of radial Ni growth on the passivation layer [16]. Fig. 15(b) shows the cross section of ENIG pads on top of TSV and Fig. 14(c) illustrates the zoomed view.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].</p>
--	--

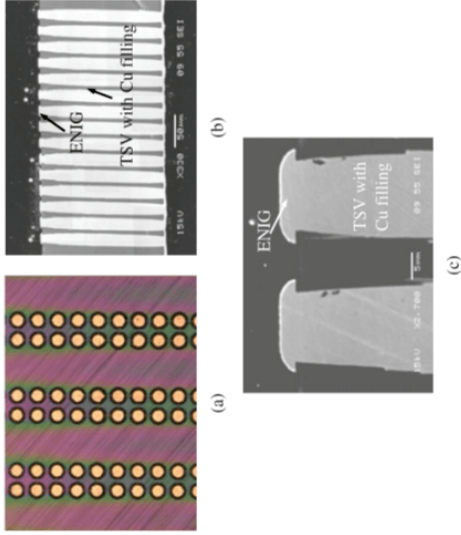
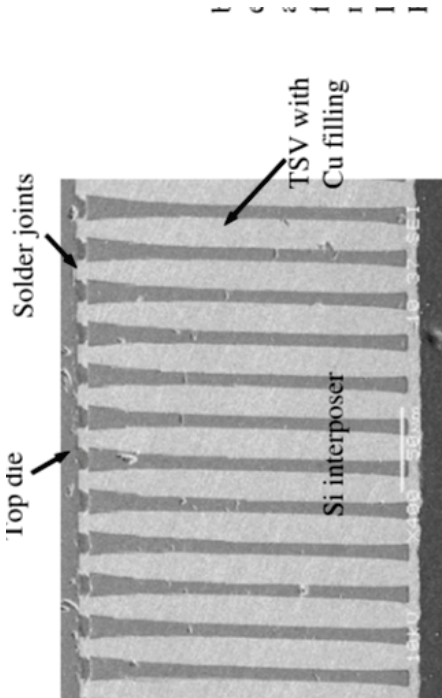


Fig. 15. SEM pictures of UBM layer of ENIG on top of TSV. (a) Top view. (b) Cross section. (c) Zoomed view.

Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 15

“Fig. 18 shows the cross section of the top die and the Si interposer joined together at selected bonding conditions. It can be seen that successful joining is achieved.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

	<div></div> <div><p>Fig. 18. Cross section of the top die and the Si interposer joined together.</p></div> <div><p>Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, FIG. 18</p></div> <div><p>“After fabrication of the CuSn solder microbumps on the top die and the ENIG UBM pads on top of the TSVs on the Si interposer, the top die and the interposer are joined together using a FC150 flip chip bonder.” Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects, [1341].</p></div> <div><p>To the extent Plaintiff contends that Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Appendix A-46 - Invalidity of U.S. Patent No. 9859202 in view of Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects - Non-Patent Publication

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

E.D. Tex. Case No. 2:25-cv-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

The Teensy series, including but not limited to Teensy 2.0, Teensy 3.0, and Teensy 3.1, stacked with various adaptors, including but not limited to Audio Adaptor, SD Adaptor, Wiz820+SD Adaptor, OctoWS2811 Adaptor, Wiz812 Adaptor, and XBee Adaptor (hereinafter “Teensy Board”) was in public use, on sale (including sold to customers and potential customers), and/or otherwise available to the public by PJRC, LLC at least by Dec. 21, 2014.¹ Teensy Board anticipates and/or renders obvious all Asserted Claims² of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.³ Teensy Board, or the written materials describing it, excerpted below, is prior art to the ’202 Patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Teensy Board, or otherwise rendered obvious by disclosures and teachings of Teensy Board, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Teensy Board does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Teensy Board with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 Patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Teensy Board, either alone or in combination with other prior art cited by Samsung and/or with

¹ See, e.g., <https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html>

² As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

³ To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserves the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

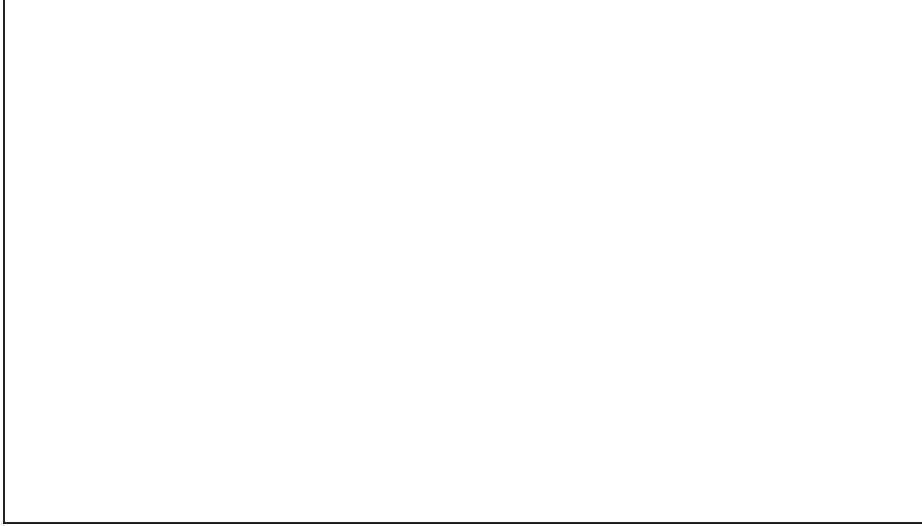
Where the chart below states that Teensy Board “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Teensy Board or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Teensy Board set forth in this chart.

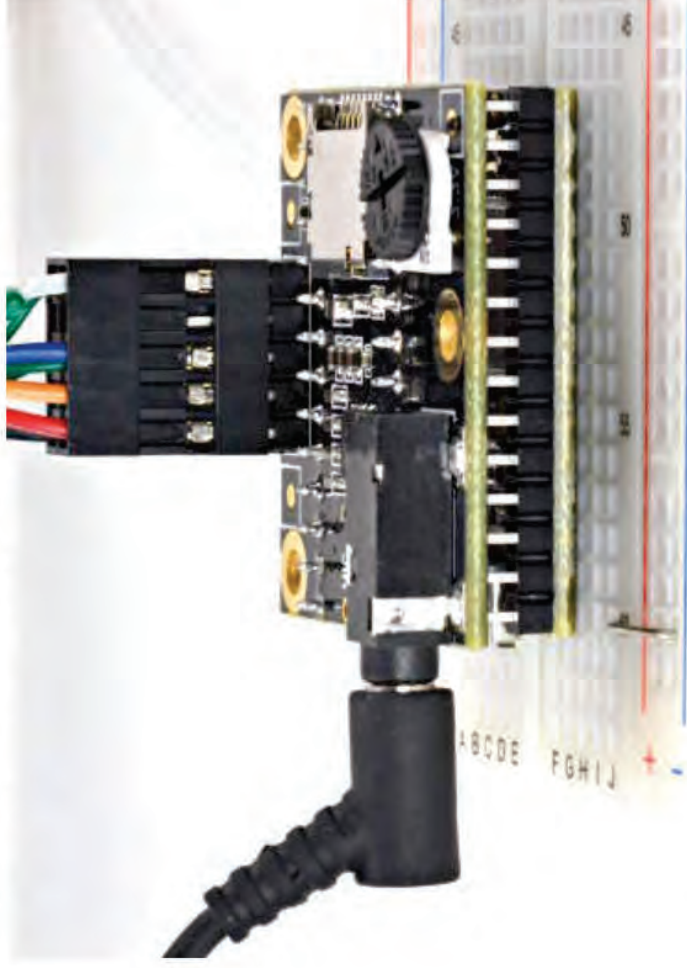
Claim 1

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, Teensy Board discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>

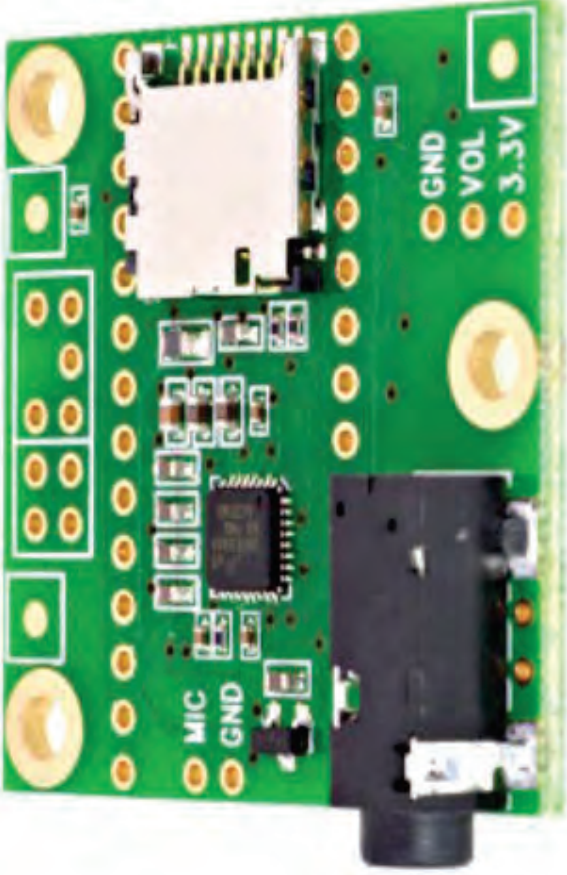
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



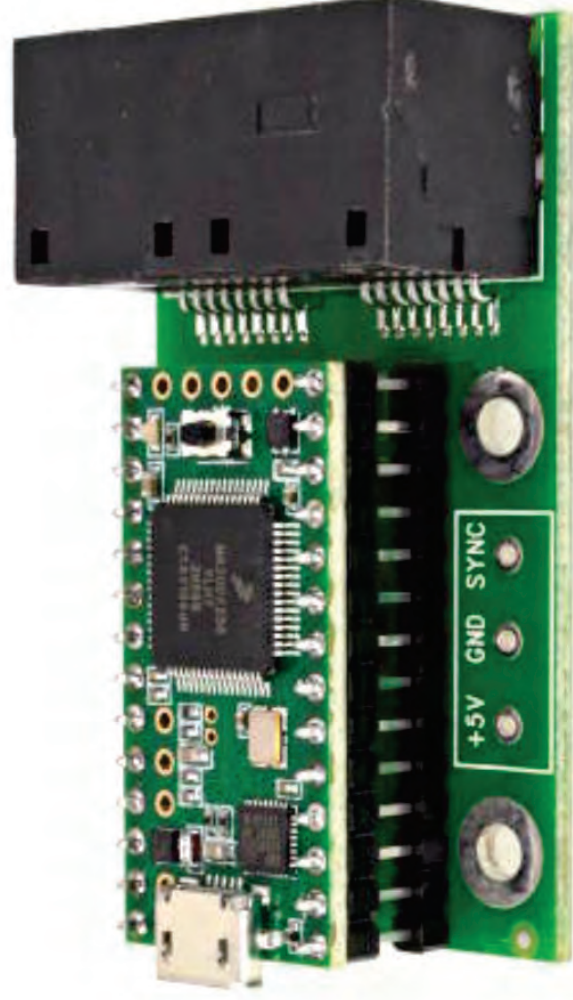
The optional volume knob and line in/out header are also added.

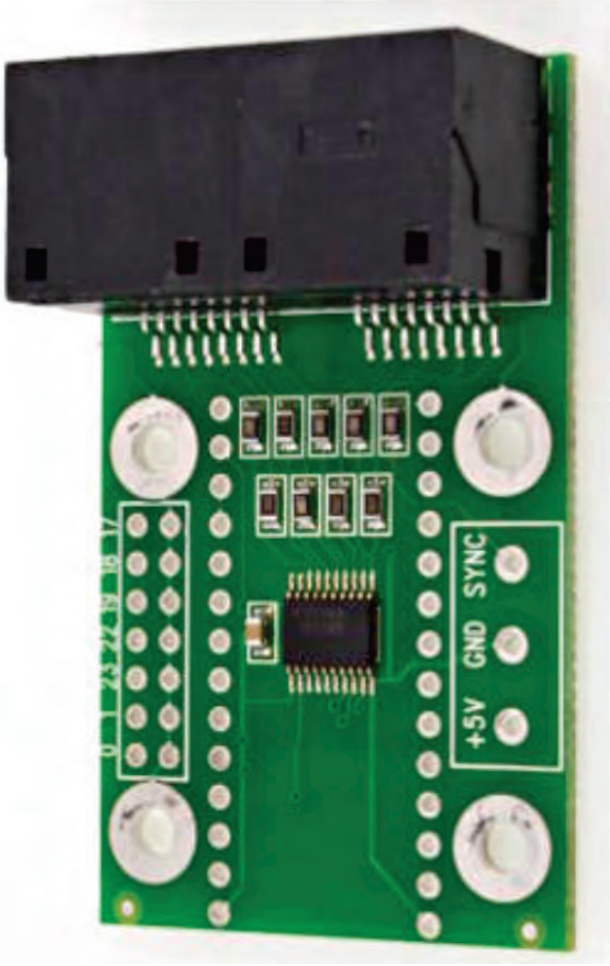
	 <p>“This audio adaptor lets you easily add high quality 16 bit, 44.1 kHz sample rate (CD quality) audio to your projects with Teensy 3.0 or 3.1. It supports stereo headphone and stereo line-level output, and also stereo line-level input or mono microphone input.</p> <p>The Teensy Audio Library lets you use the input and output simultaneously together with a toolkit of audio processing objects, to easily create all types of sophisticated audio applications. You can play multiple sound files, create synthesized waveforms, apply effects, mix multiple streams and output high quality audio to the headphones or line out pins.</p>
--	--

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

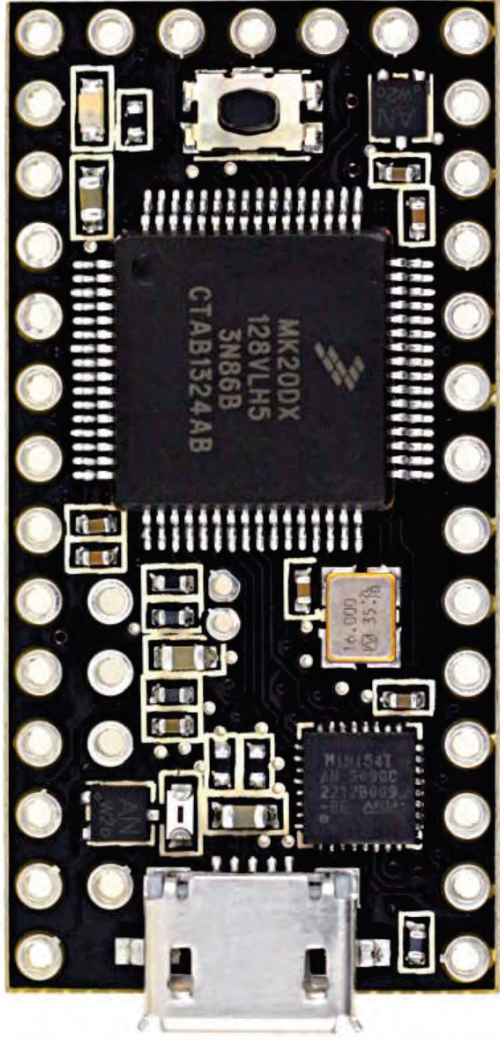
Teensy 3.0 & 3.1 have the Cortex-M4 DSP instructions which provide plenty of computational power for real-time FFT (spectrum analysis), opening up the possibility of creating advanced sound-reactive projects.”

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html

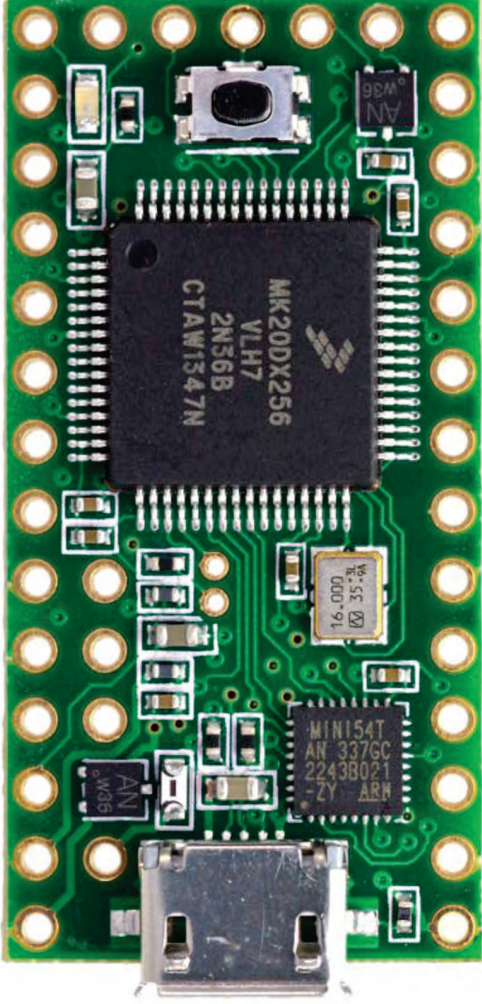


	<div></div> <p>“This adaptor board connects Teensy 3.1 to thousands of LEDs using the OctoWS2811 Library.</p> <p>The adaptor features a 74HCT245 buffer chip and 100 ohm impedance matching resistors. CAT6 Ethernet cable is used from this board to the LED strips. CAT6 cable is designed for very high bandwidth, minimal cross-talk between twisted pairs, and 100 ohm impedance, for a very high quality signal. The RJ-45 network jacks allow your LED array to be easily disconnected from the electronics.</p> <p>...</p> <p>Teensy 3.1 is added on top of the adaptor using stacking header pins, or a header and socket pair if you wish to be able to remove the Teensy 3.1 board.”</p>
--	--

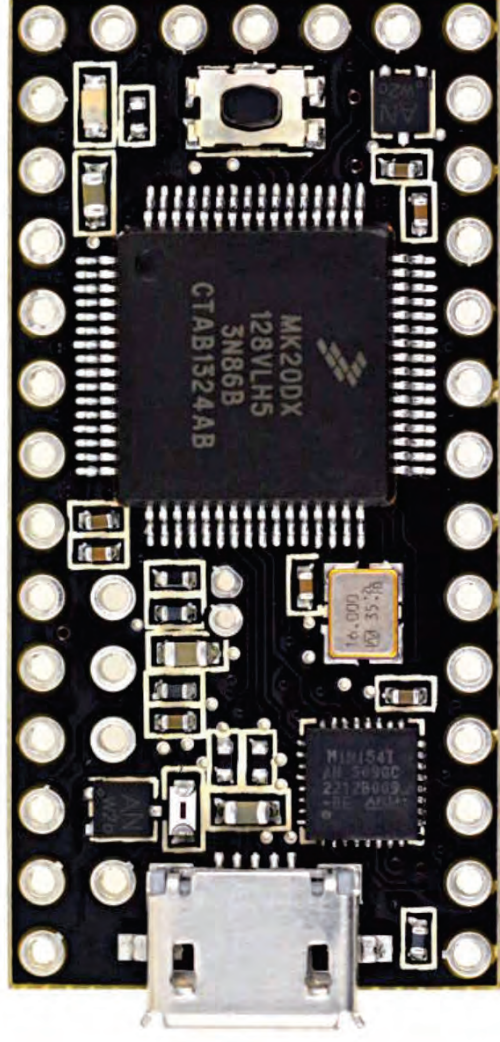
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>https://web.archive.org/web/20141221070129/http://www.pjrc.com/store/octo28_adaptor.html</p>  <p>The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.0 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”</p> <p>https://web.archive.org/web/20141221111436/http://www.pjrc.com/store/teensy3.html</p>
--	--

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	 <p>“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.1 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”</p> <p>https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.A] a bottom package substrate;</p>	<p>Teensy Board discloses, either expressly or inherently, a bottom package substrate.</p> <p>See, e.g.:</p>

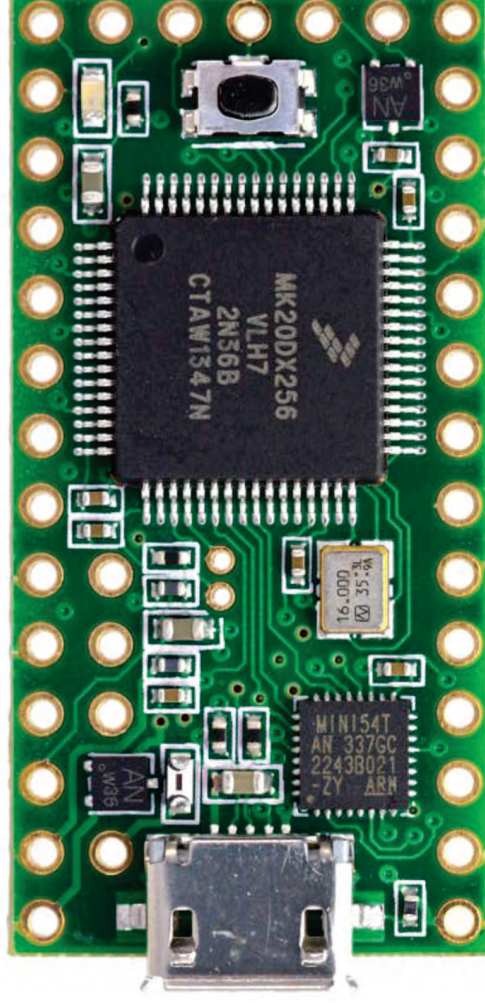
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.0 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221111436/http://www.pjrc.com/store/teensy3.html>

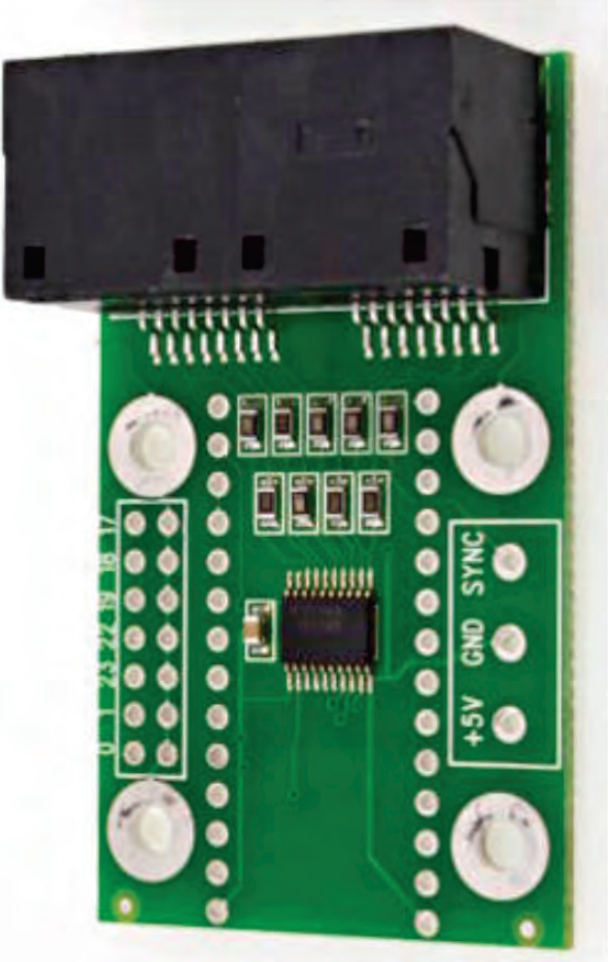
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.1 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	 <p>“Teensy 3.1 is added on top of the adaptor using stacking header pins, or a header and socket pair if you wish to be able to remove the Teensy 3.1 board.”</p> <p>https://web.archive.org/web/20141221070129/http://www.pjrc.com/store/octo28_adaptor.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

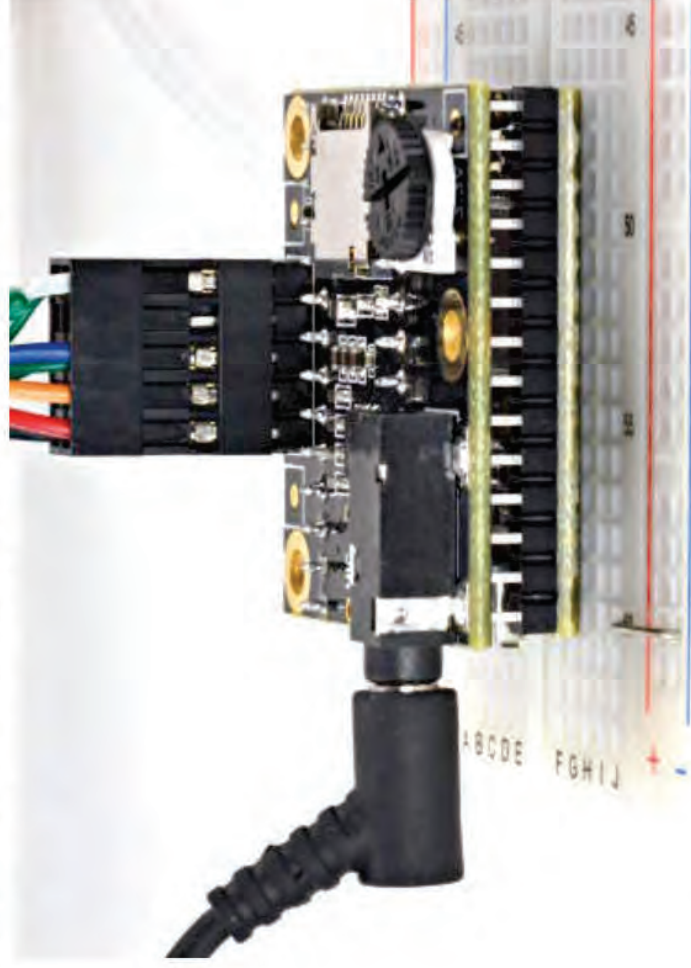
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

[1.B] a top package substrate stacked on top of the bottom package substrate;

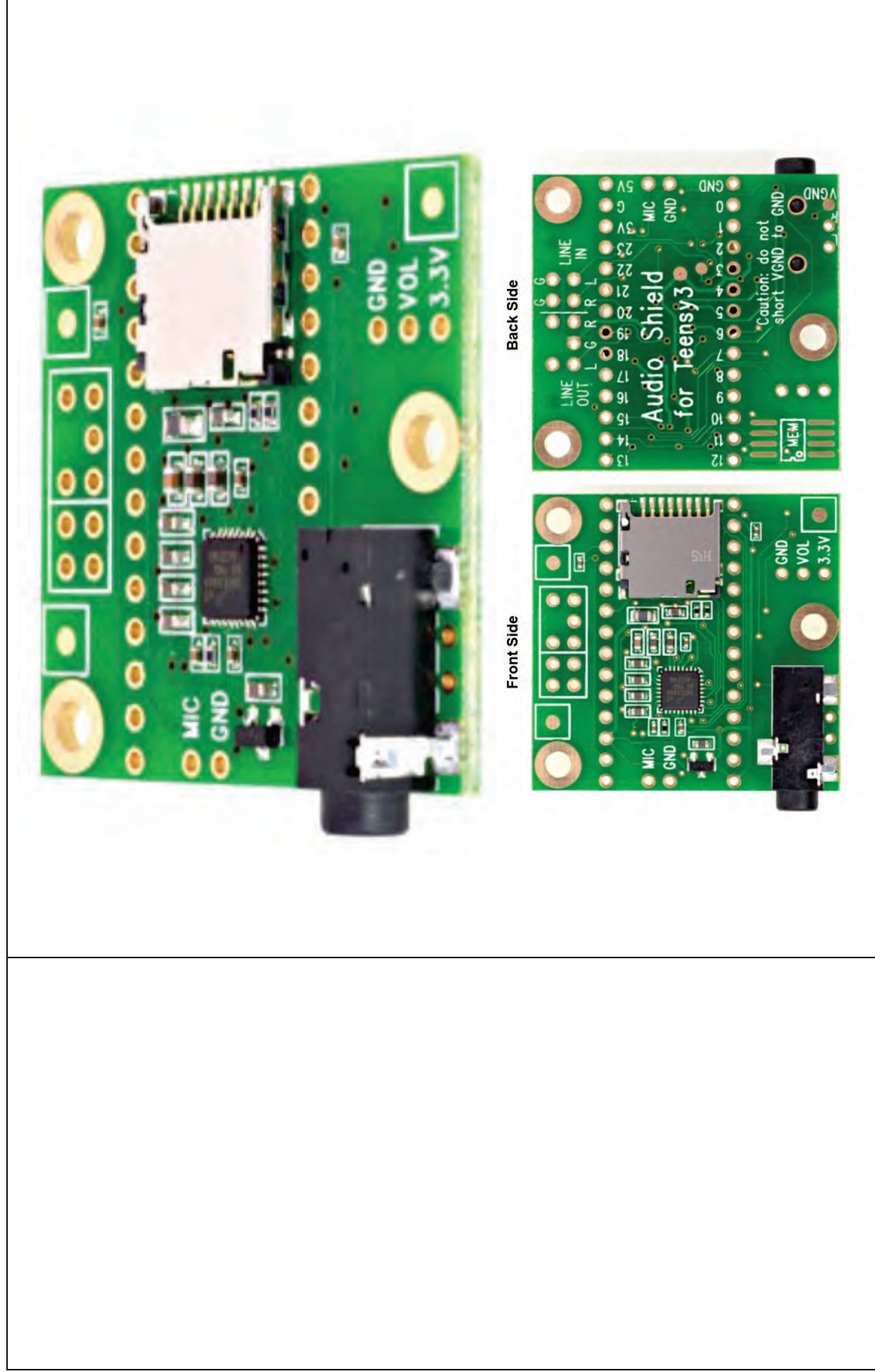
Teensy Board discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.

See, e.g.:

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



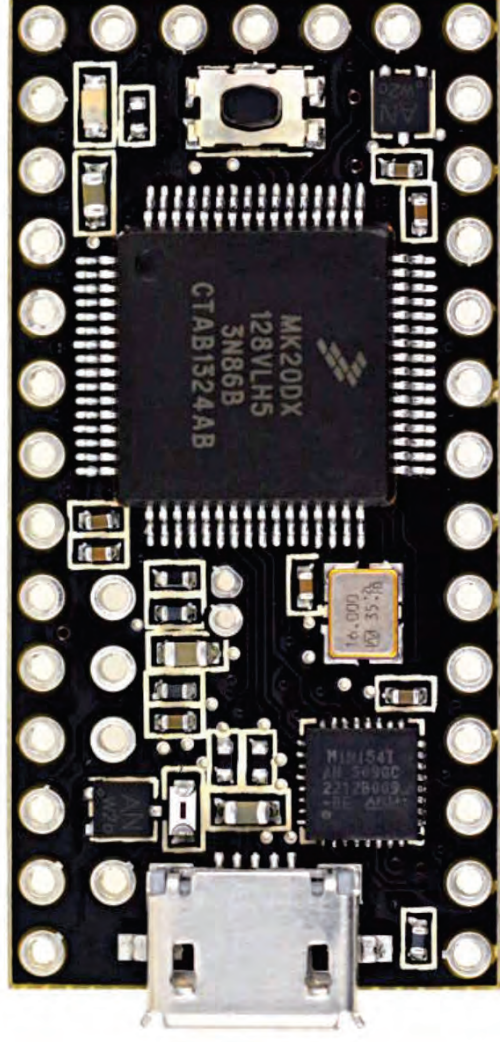
The optional volume knob and line in/out header are also added.



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“This audio adaptor lets you easily add high quality 16 bit, 44.1 kHz sample rate (CD quality) audio to your projects with Teensy 3.0 or 3.1. It supports stereo headphone and stereo line-level output, and also stereo line-level input or mono microphone input.</p> <p>The Teensy Audio Library lets you use the input and output simultaneously together with a toolkit of audio processing objects, to easily create all types of sophisticated audio applications. You can play multiple sound files, create synthesized waveforms, apply effects, mix multiple streams and output high quality audio to the headphones or line out pins.</p> <p>Teensy 3.0 & 3.1 have the Cortex-M4 DSP instructions which provide plenty of computational power for real-time FFT (spectrum analysis), opening up the possibility of creating advanced sound-reactive projects.”</p> <p>https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html</p>
--	---

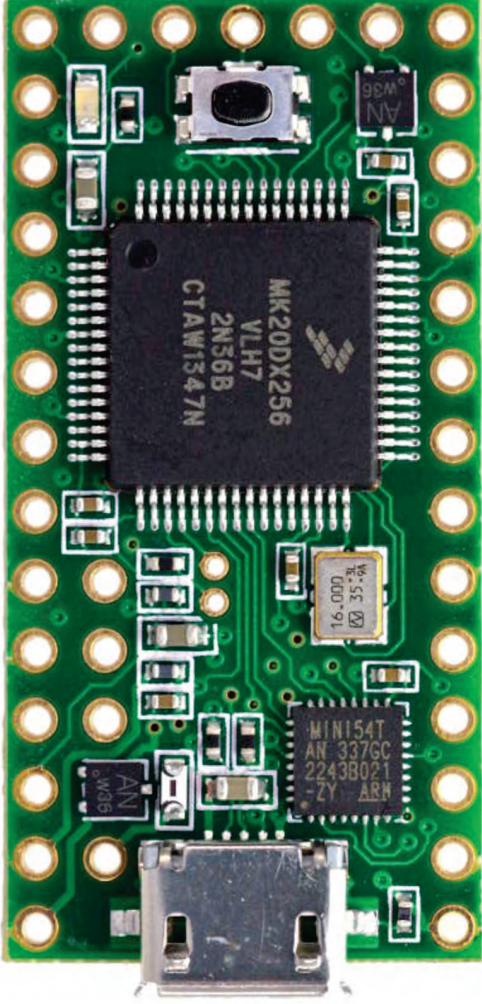
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.0 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221111436/http://www.pjrc.com/store/teensy3.html>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

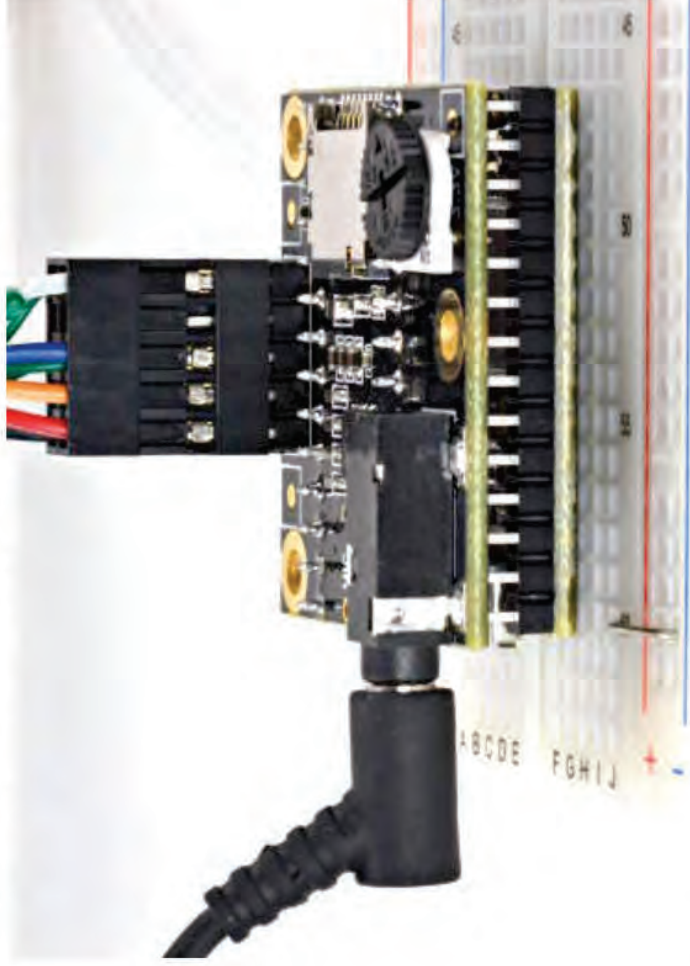
	 <p>“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.1 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”</p> <p>https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate</p>	<p>Teensy Board discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.</p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

to define a space between the bottom package substrate and the top package substrate, wherein

See, e.g.:

This photo shows a Teensy 3.1 soldered under the audio adaptor using two 14x1 pins.



The optional volume knob and line in/out header are also added.

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html

	<div><div><div><div><div><div></div><div>Add To Order</div></div></div><div><div><div>HEADER_14x1</div><div>Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing</div><div>\$1.00</div></div></div></div></div><div><div><div><div>Inventory Status:</div><div>In Stock</div></div><div><div>Last physical count:</div><div>Dec 8, 2014</div></div></div></div><div></div><div>https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html</div></div>
--	---

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

Inventory Status: **In Stock**

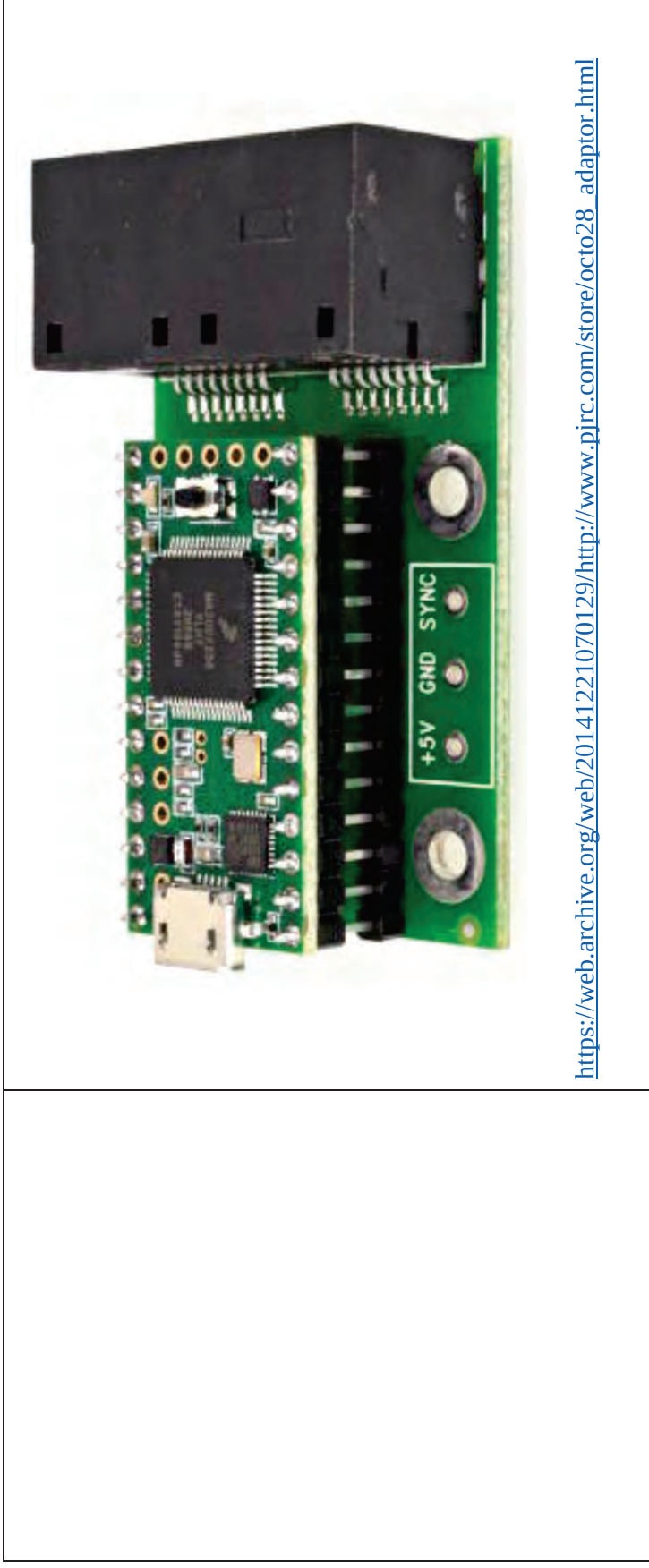
Last physical count: Dec 8, 2014



“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”

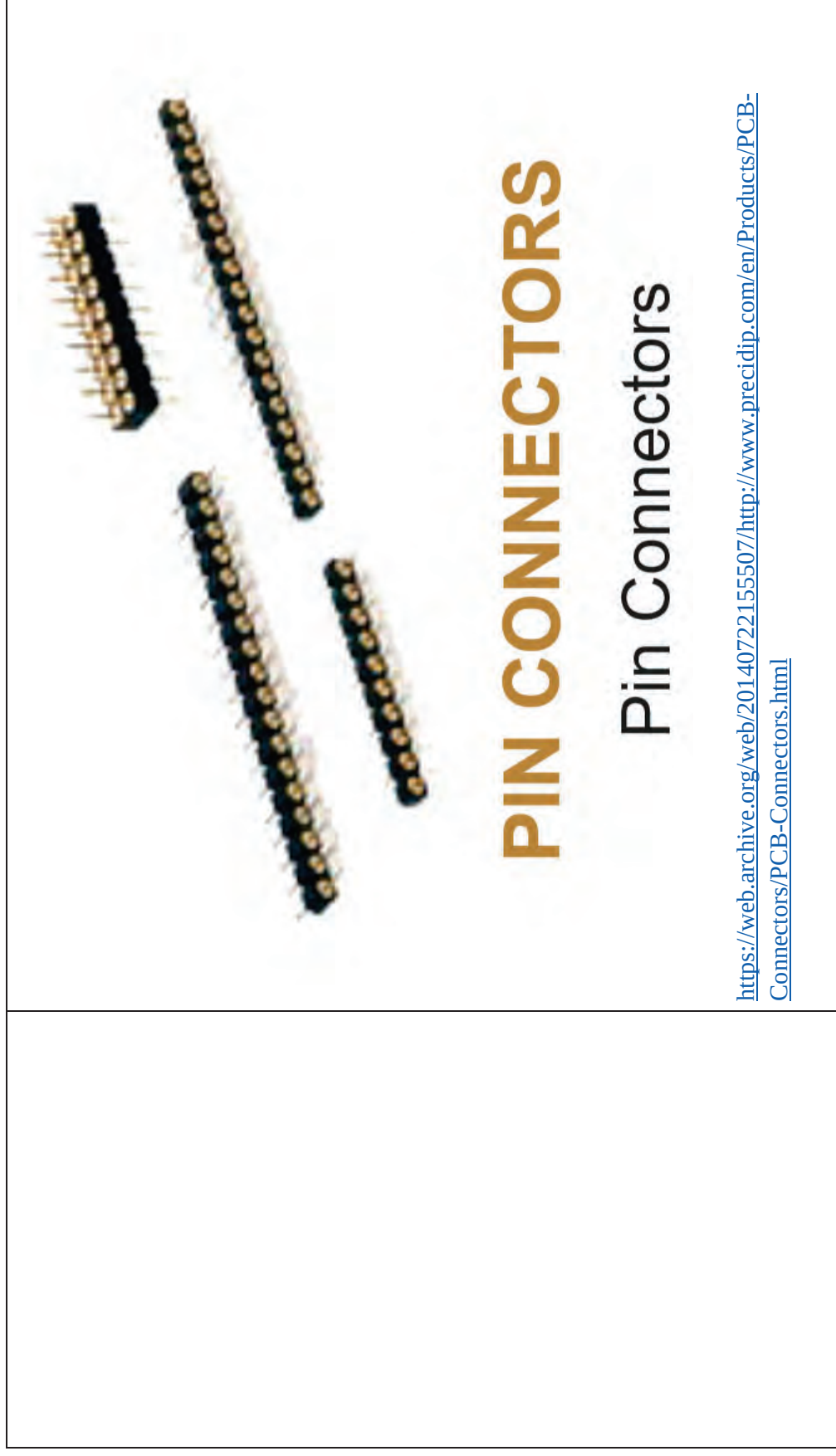
https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

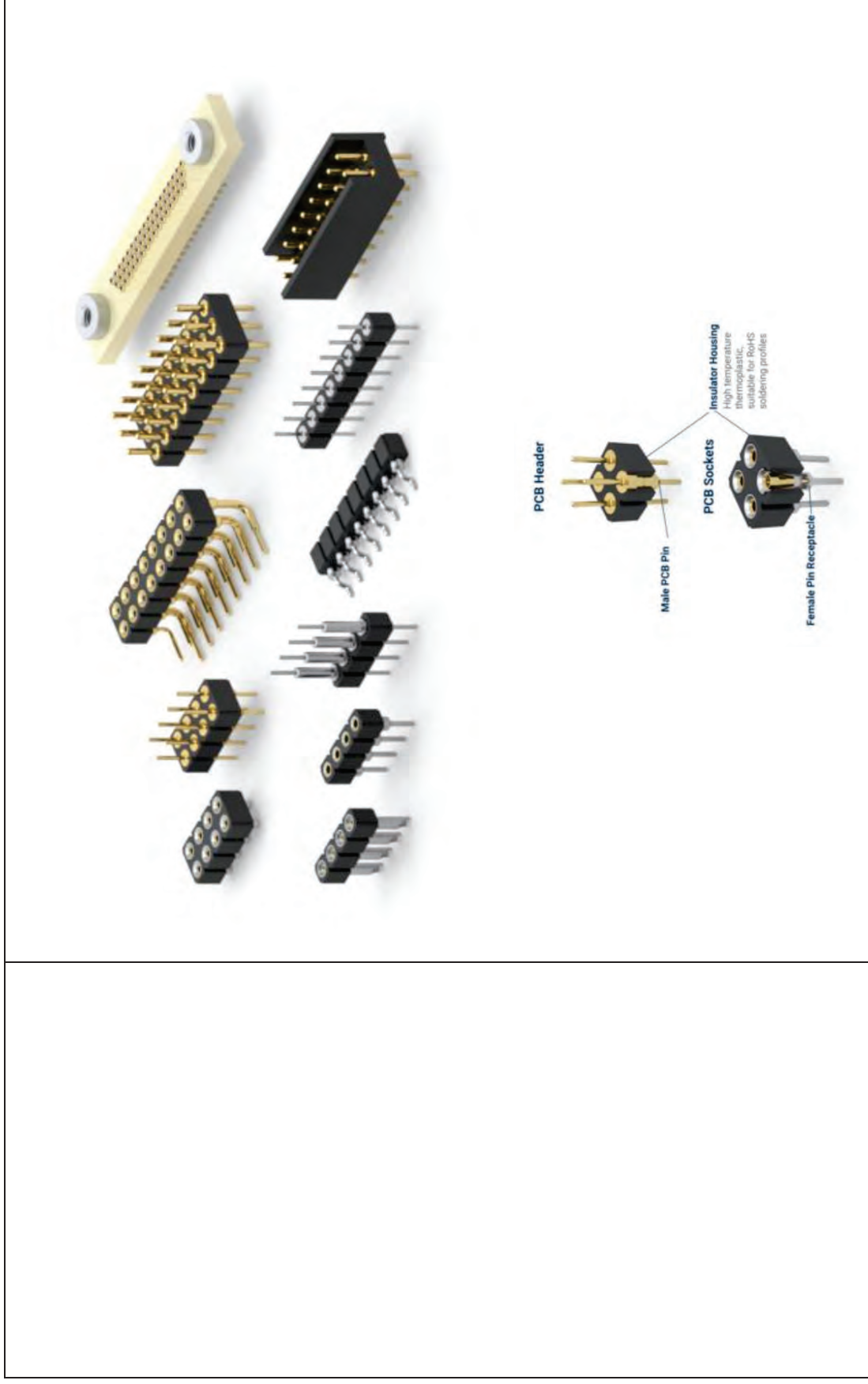
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <div>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</div> <div><p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p><p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p></div>
--	---





Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Teensy Board discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p>

Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing

Add To Order	HEADER_14x1	Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing	\$1.00
------------------------------	-------------	--	--------

Inventory Status: **In Stock**
Last physical count: Dec 8 2014

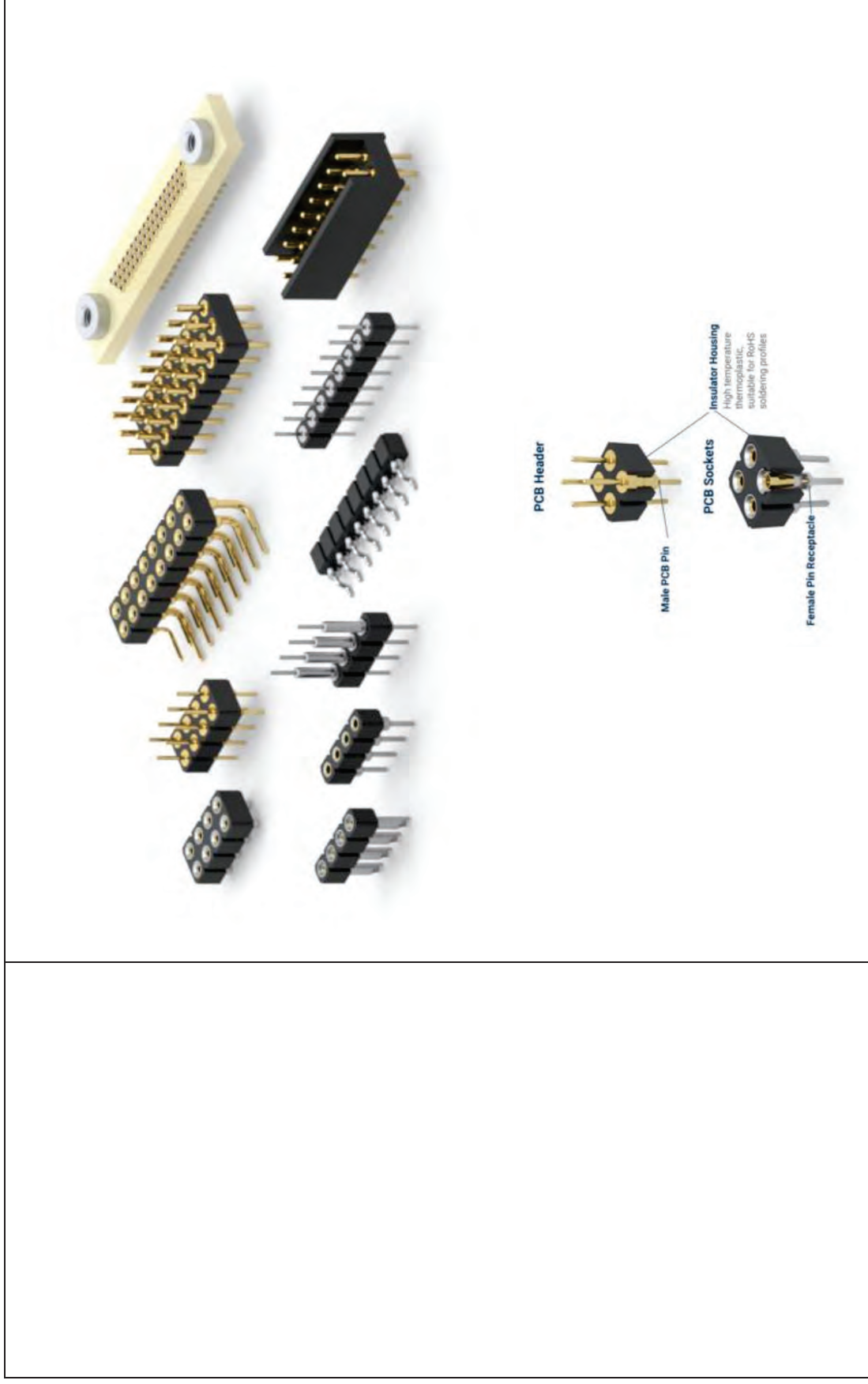


https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <p>“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”</p> <p>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>
--	--

	 <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>Teensy Board discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p>

Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing

Add To Order	HEADER_14x1	Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing	\$1.00
------------------------------	-------------	--	--------

Inventory Status: **In Stock**
Last physical count: Dec 8 2014

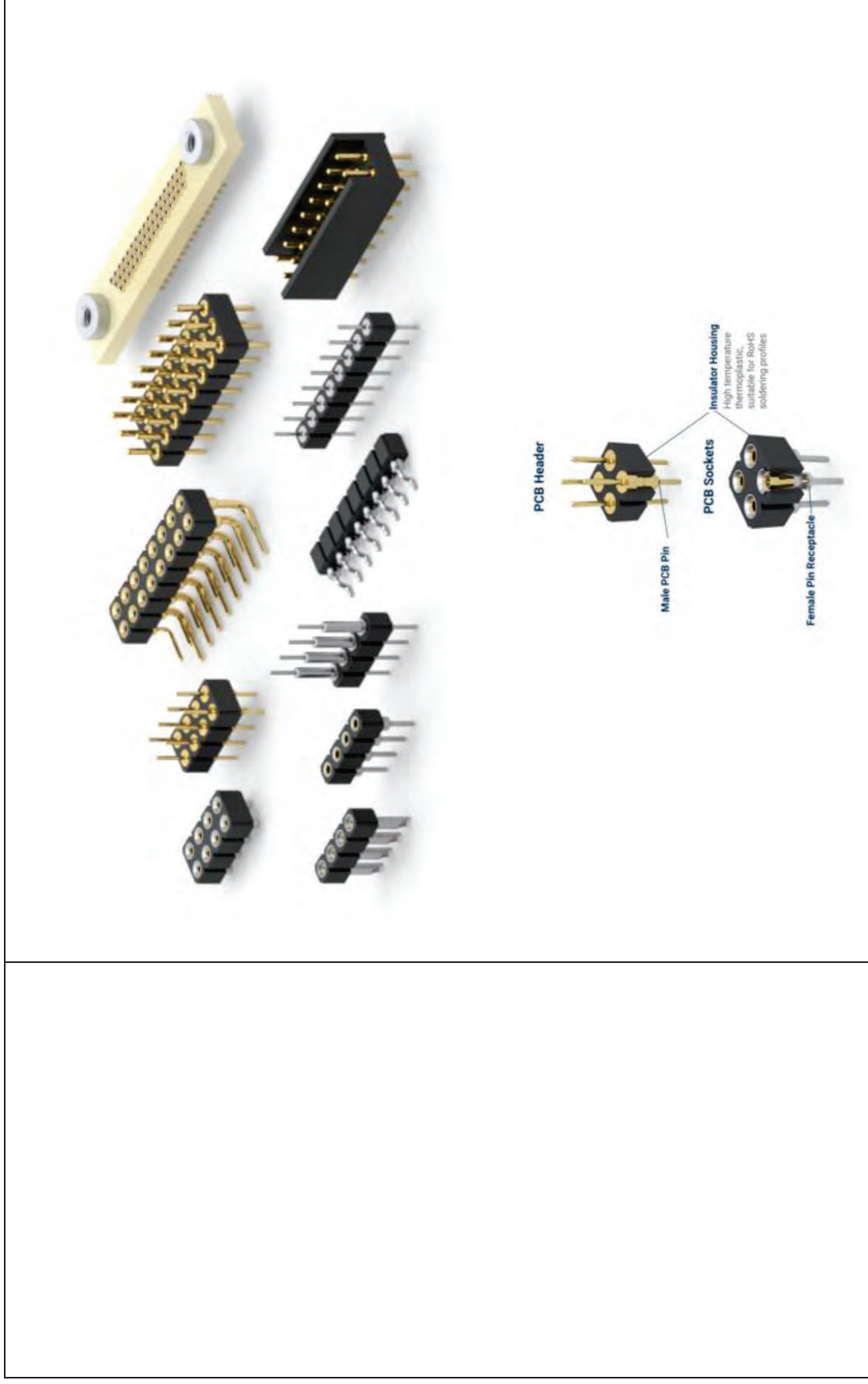


https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <p>“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”</p> <p>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>
--	--





Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Teensy Board discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing

Add To Order	HEADER_14x1	Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing	\$1.00
------------------------------	-------------	--	--------

Inventory Status: **In Stock**
Last physical count: Dec 8 2014

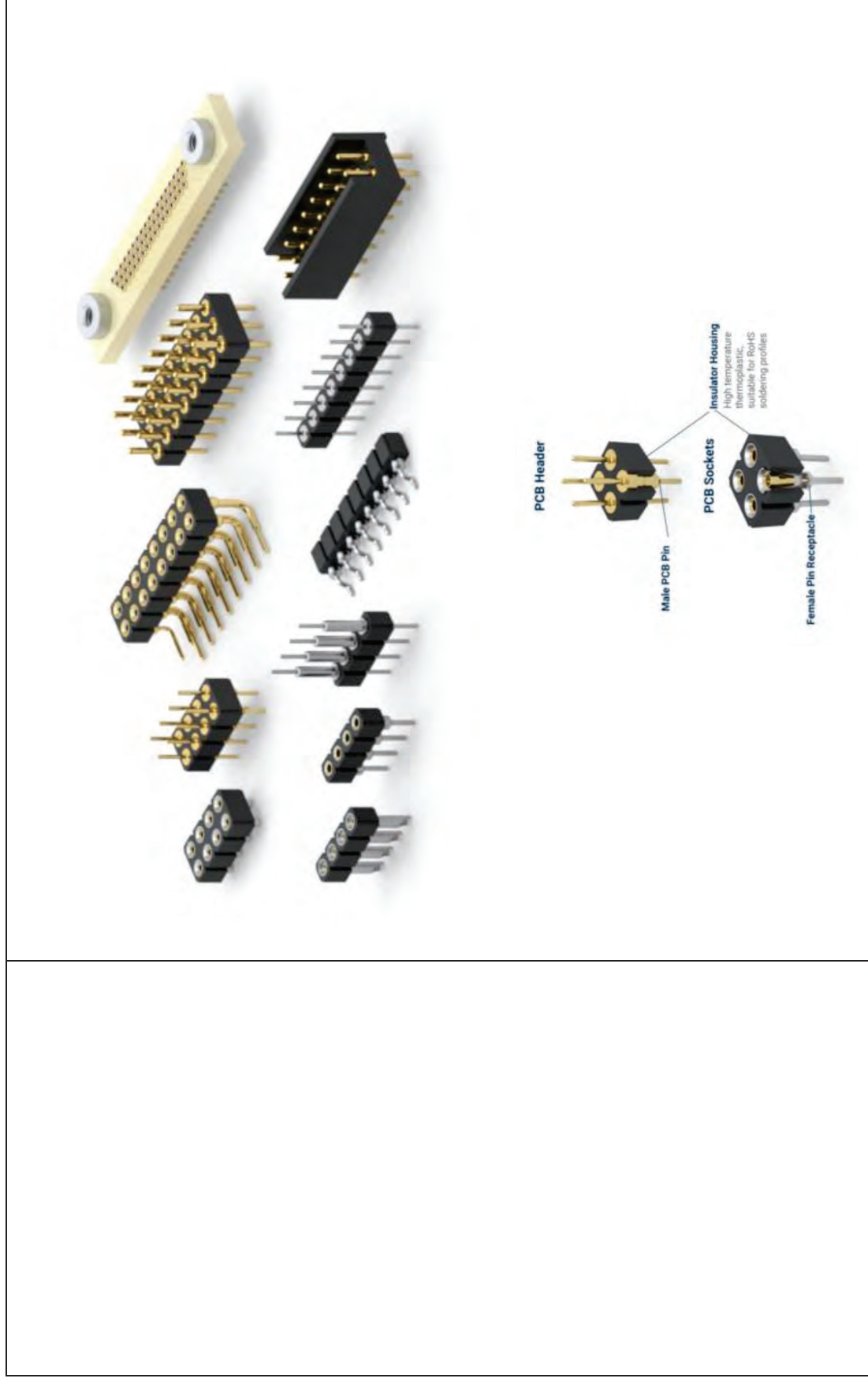


https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <p>“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”</p> <p>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>
--	--

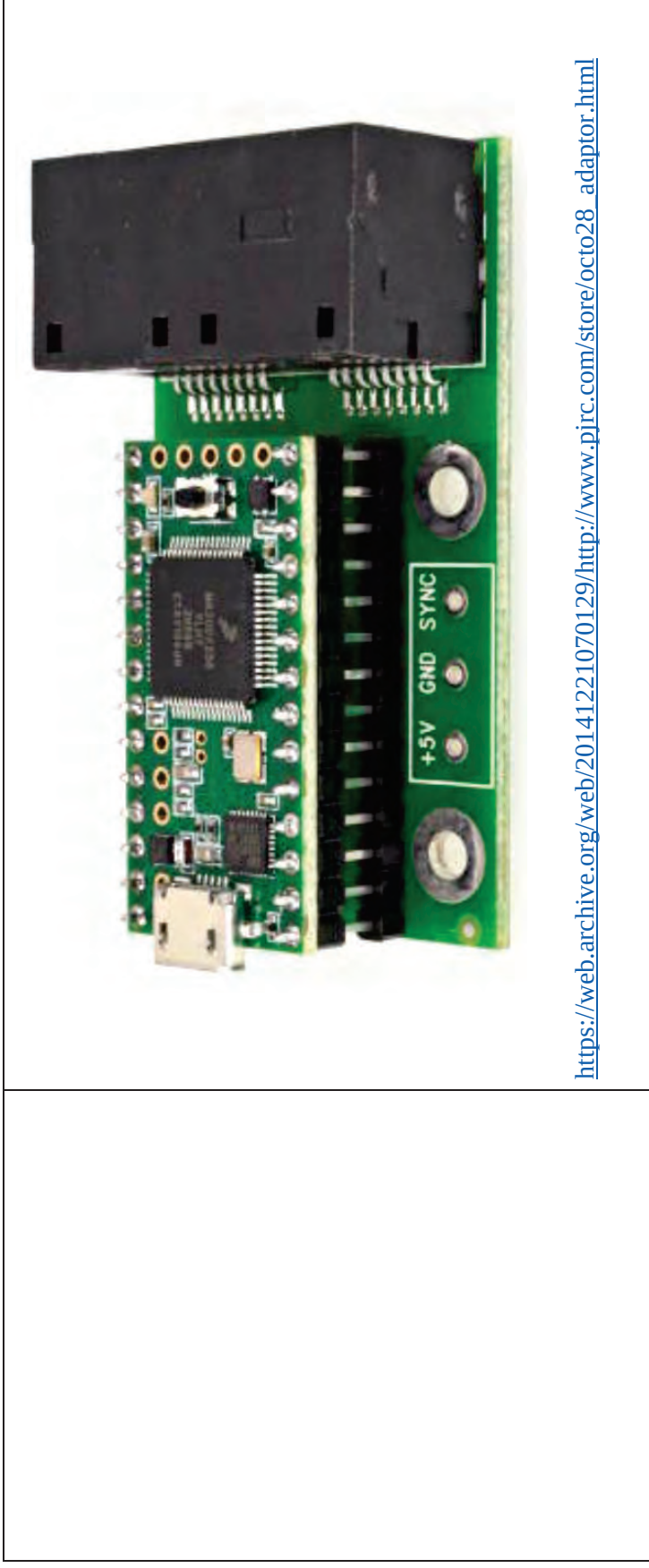
	 <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	--



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Teensy Board discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

Inventory Status: **In Stock**

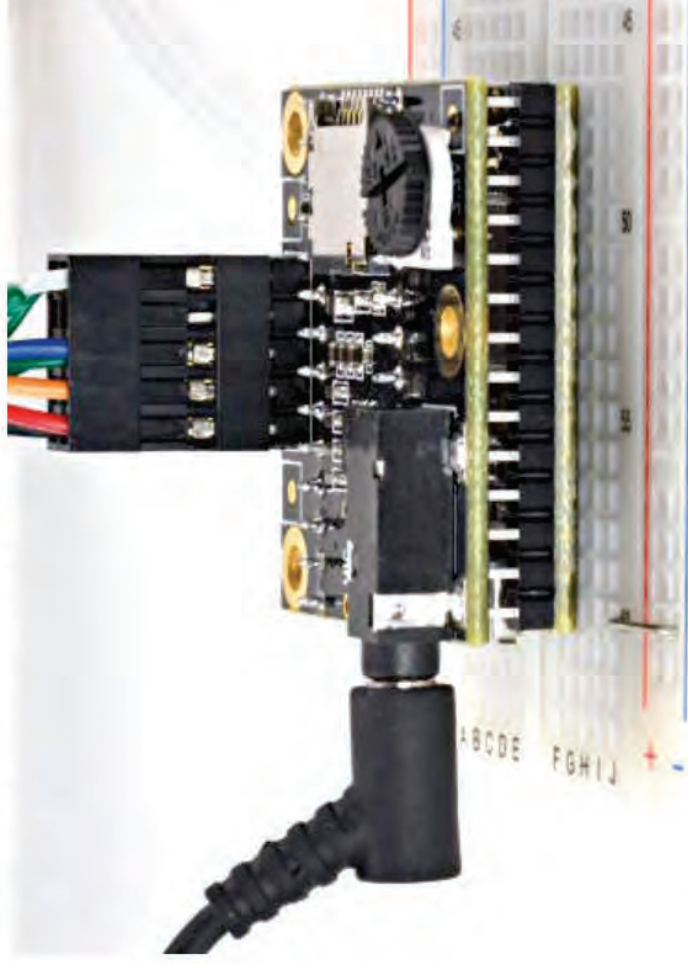
Last physical count: Dec 8, 2014



https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



The optional volume knob and line in/out header are also added.

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html

Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing

Add To Order	HEADER_14x1	Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing	\$1.00
------------------------------	-------------	--	--------

Inventory Status: **In Stock**
Last physical count: Dec 8 2014

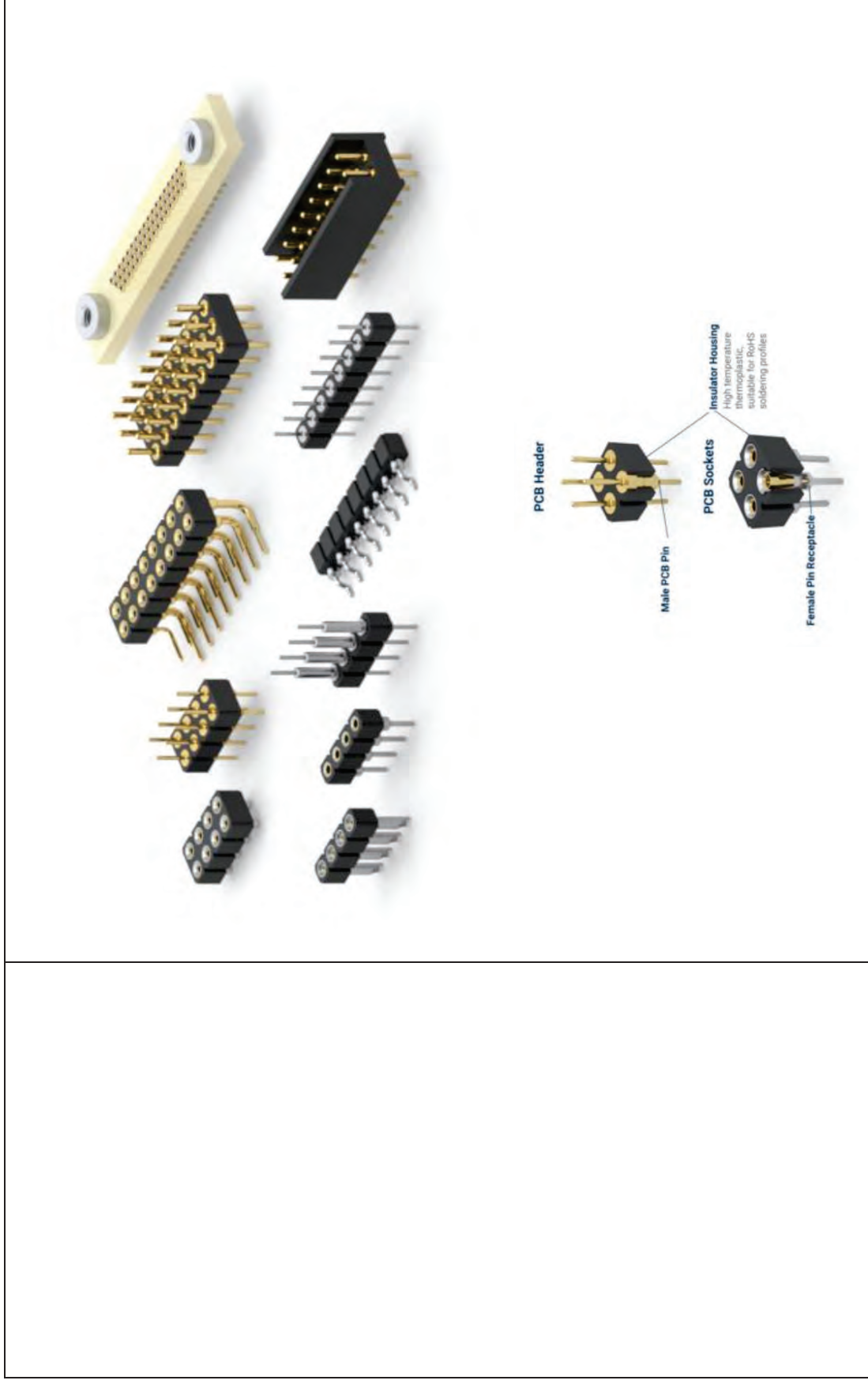


https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <p>“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”</p> <p>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>
--	--



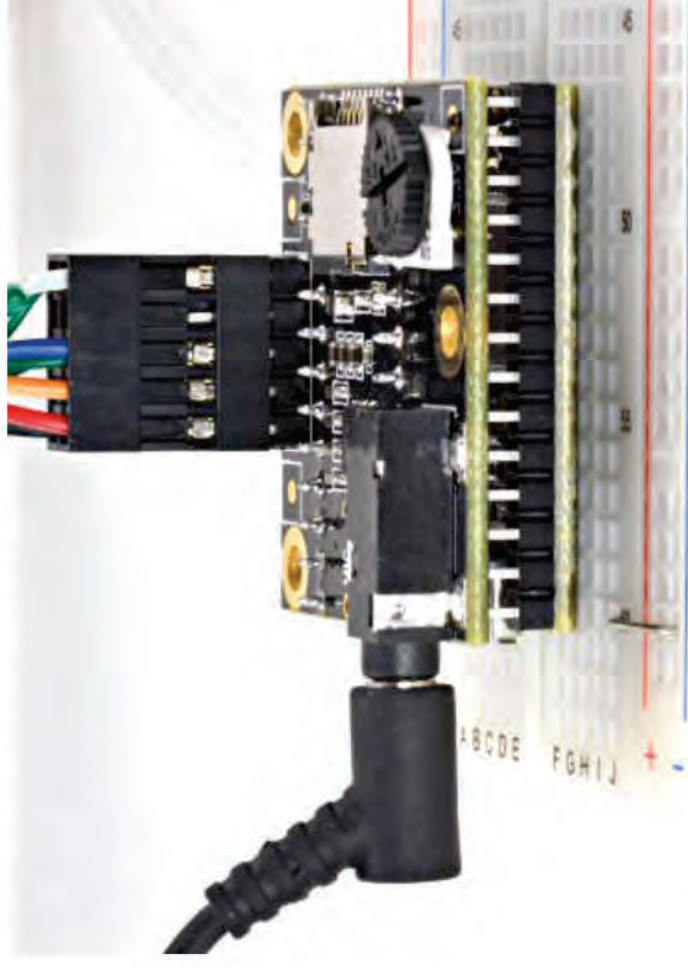


Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Teensy Board discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



The optional volume knob and line in/out header are also added.

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html

Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing

Add To Order	HEADER_14x1	Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing	\$1.00
------------------------------	-------------	--	--------

Inventory Status: **In Stock**
Last physical count: Dec 8 2014



https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

Inventory Status: **In Stock**

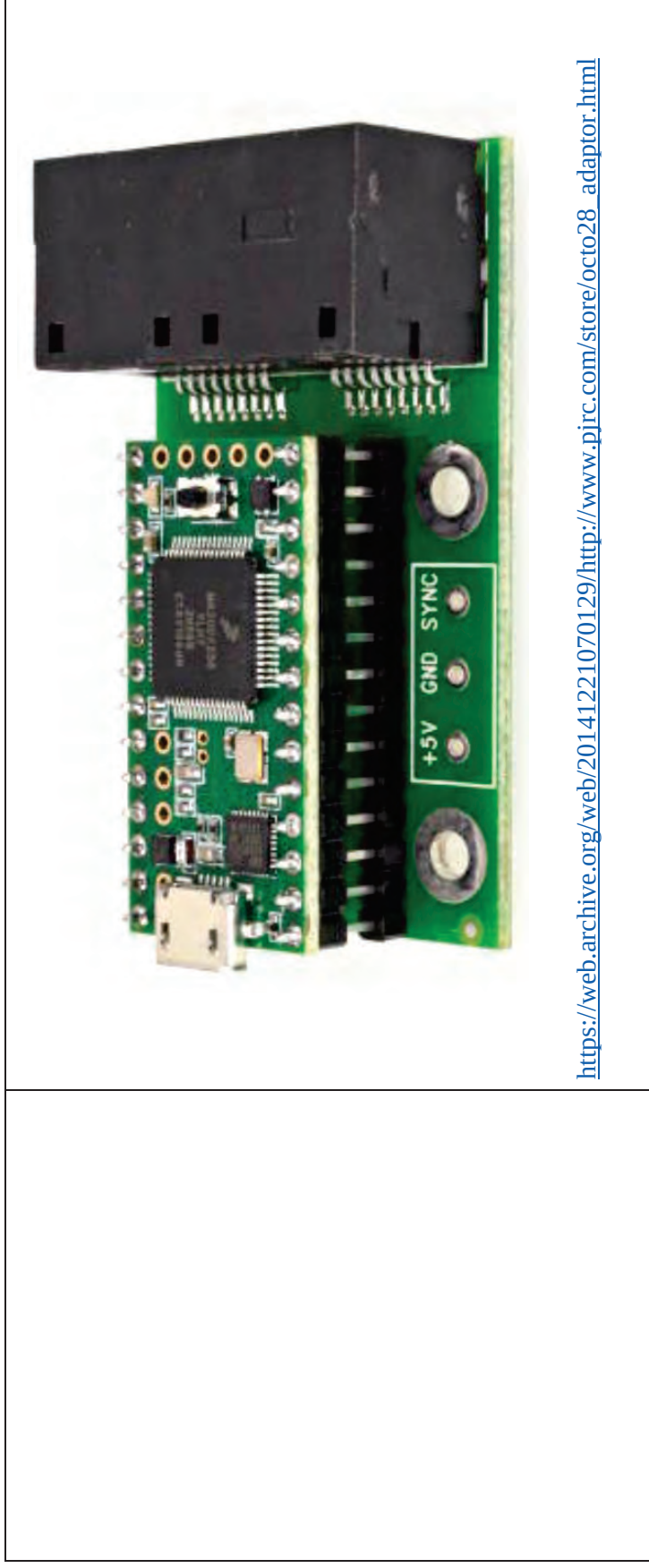
Last physical count: Dec 8, 2014



“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”

https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

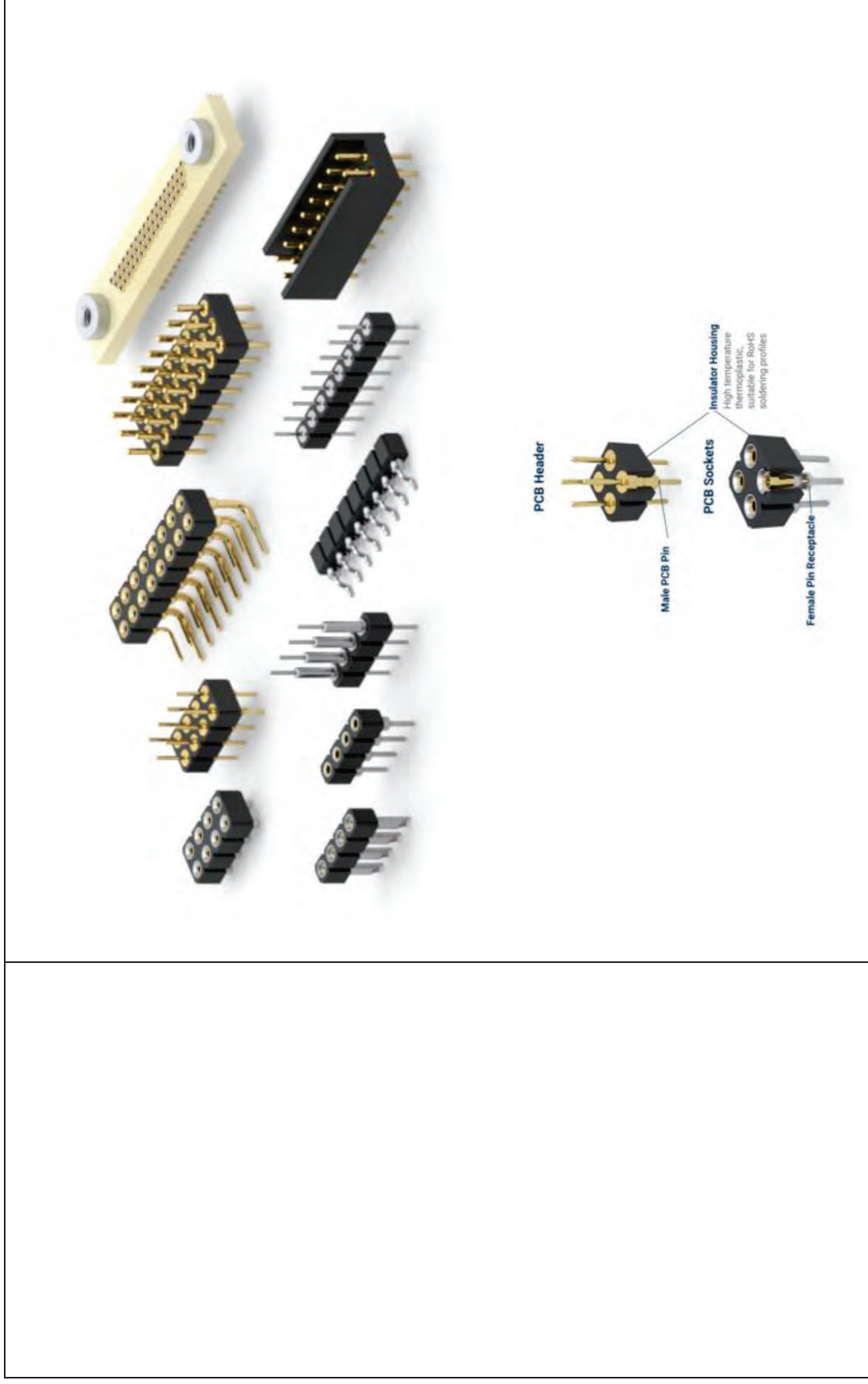
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <div>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</div> <div><p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p><p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p></div>
--	---

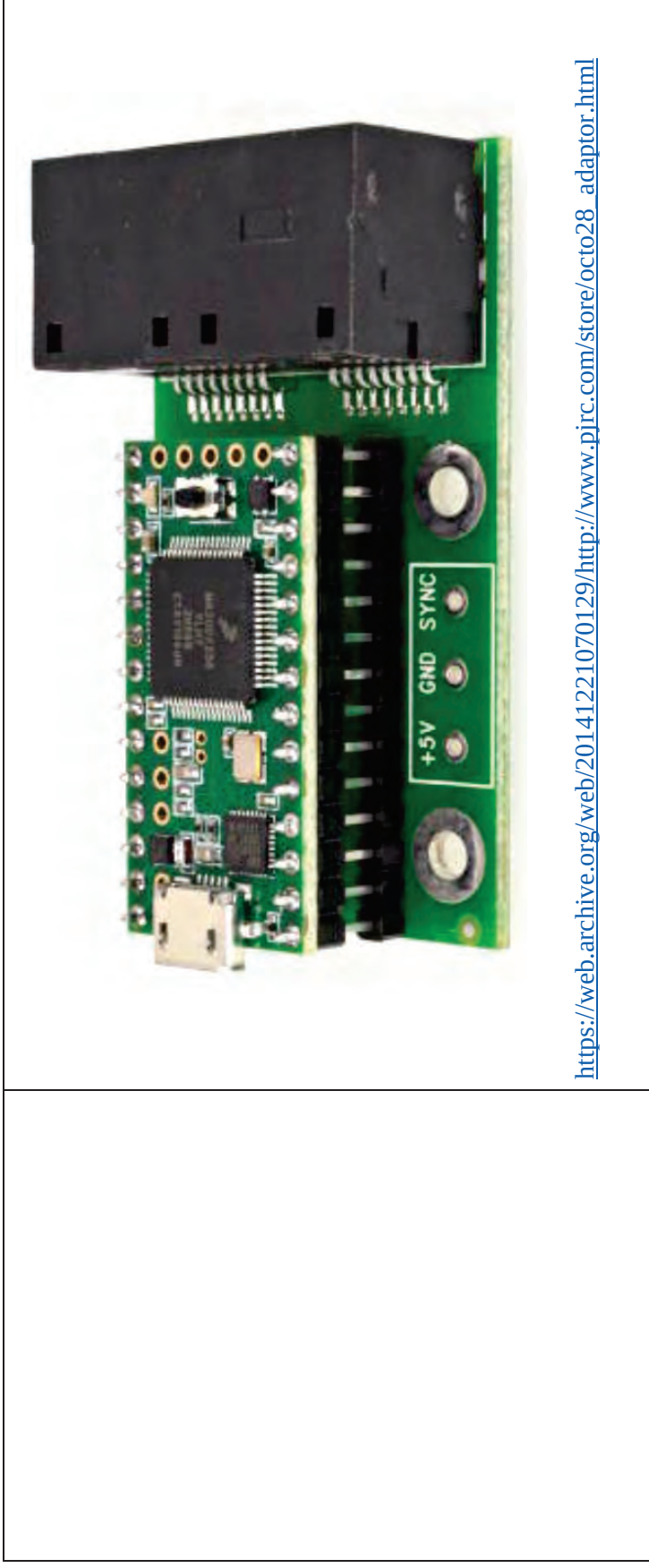




Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Teensy Board discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

Inventory Status: **In Stock**

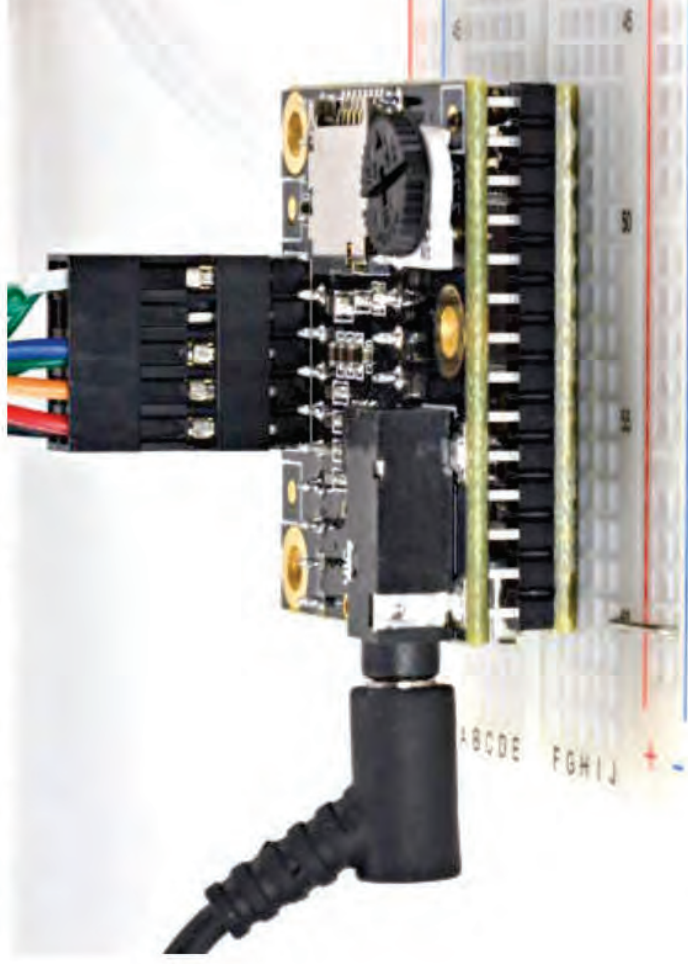
Last physical count: Dec 8, 2014



https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



The optional volume knob and line in/out header are also added.

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html

Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing

Add To Order	HEADER_14x1	Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing	\$1.00
------------------------------	-------------	--	--------

Inventory Status: **In Stock**
Last physical count: Dec 8 2014

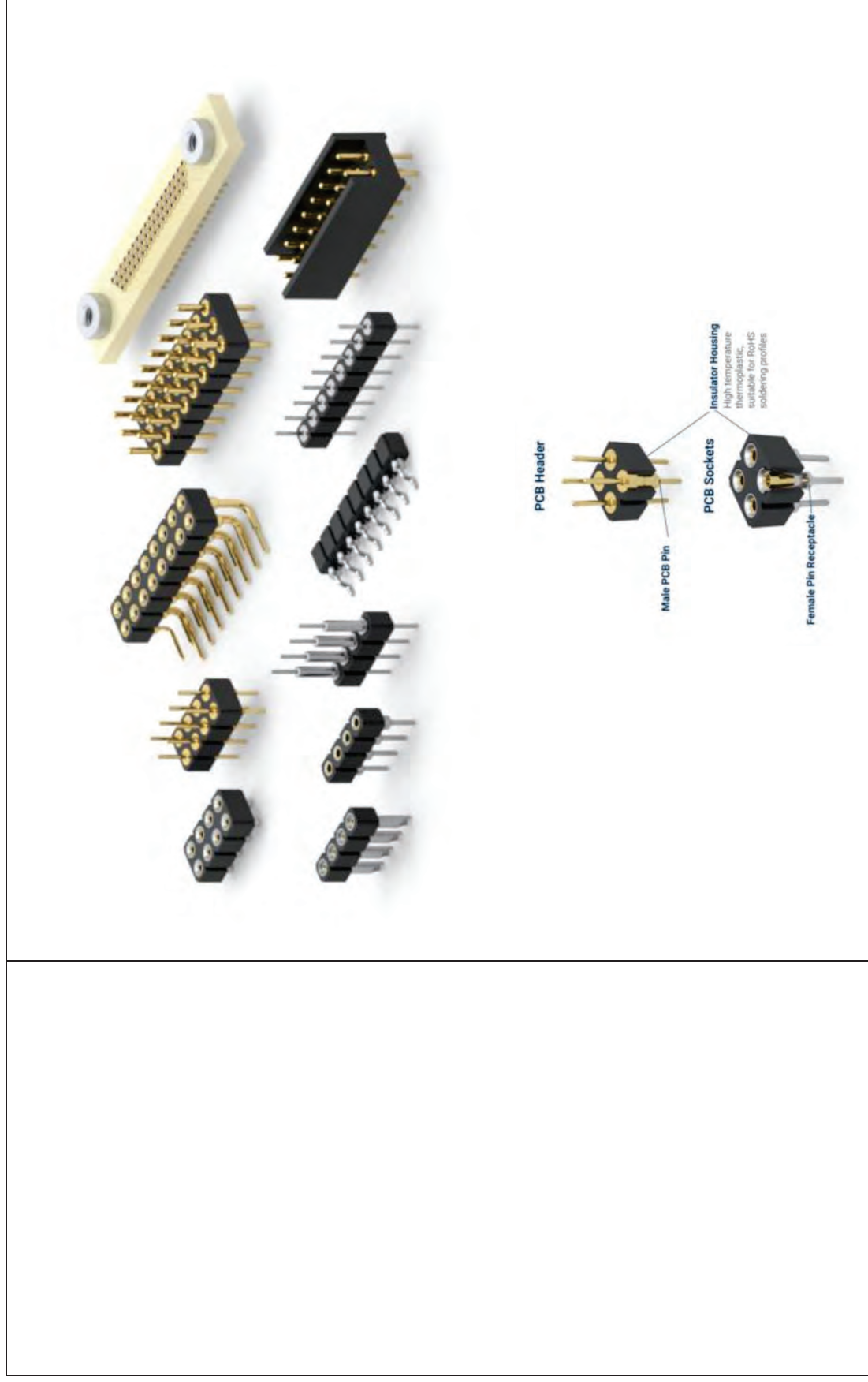


https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <p>“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”</p> <p>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>
--	--

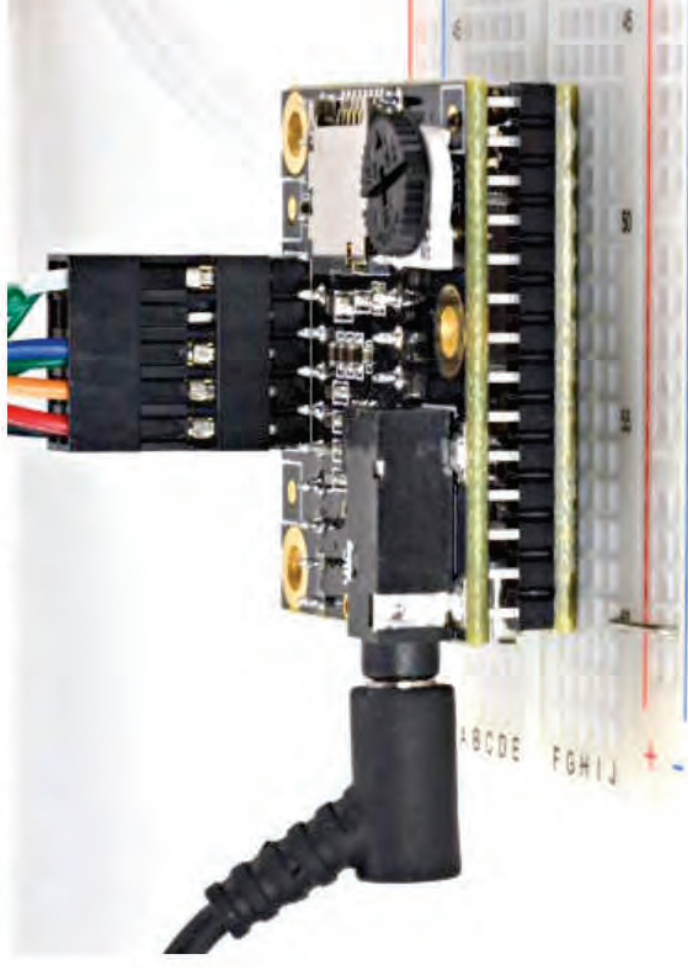




Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Teensy Board discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



The optional volume knob and line in/out header are also added.

“This audio adaptor lets you easily add high quality 16 bit, 44.1 kHz sample rate (CD quality) audio to your projects with Teensy 3.0 or 3.1. It supports stereo headphone and stereo line-level output, and also stereo line-level input or mono microphone input.

	<div><p>The Teensy Audio Library lets you use the input and output simultaneously together with a toolkit of audio processing objects, to easily create all types of sophisticated audio applications. You can play multiple sound files, create synthesized waveforms, apply effects, mix multiple streams and output high quality audio to the headphones or line out pins.</p><p>Teensy 3.0 & 3.1 have the Cortex-M4 DSP instructions which provide plenty of computational power for real-time FFT (spectrum analysis), opening up the possibility of creating advanced sound-reactive projects.”</p><p>https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html</p><div><h2>Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing</h2><div><div>Add To Order</div><div>HEADER_14x1</div><div>Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing</div><div>\$1.00</div></div><div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div></div></div>
	<p>https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html</p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

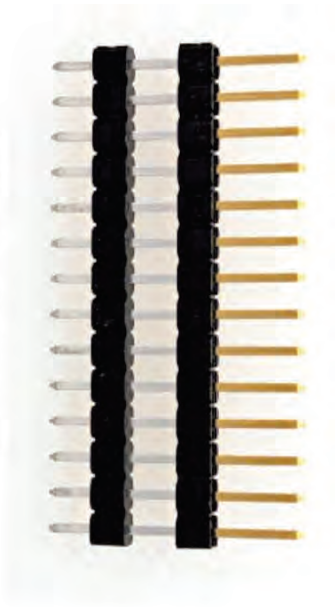
HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

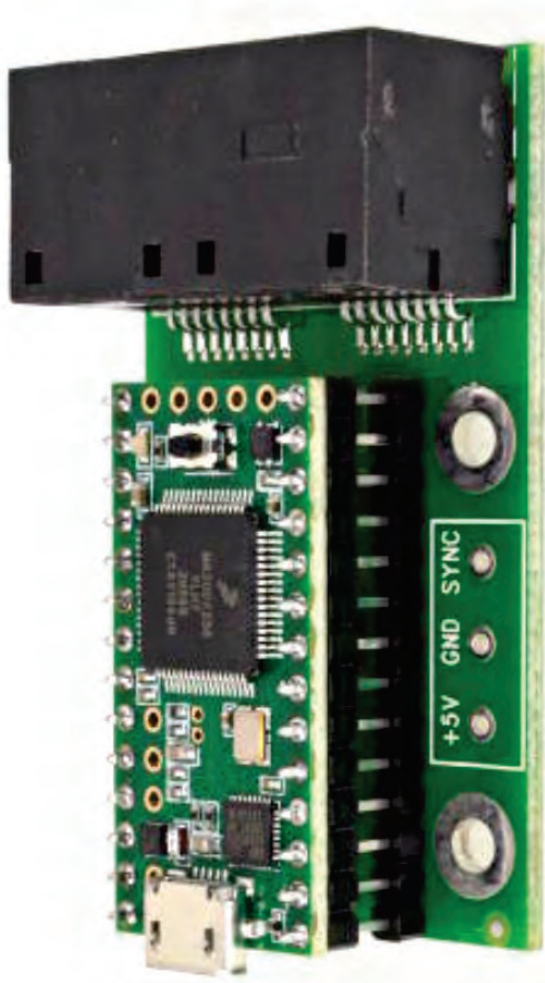
Inventory Status: **In Stock**

Last physical count: Dec 8, 2014



“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”

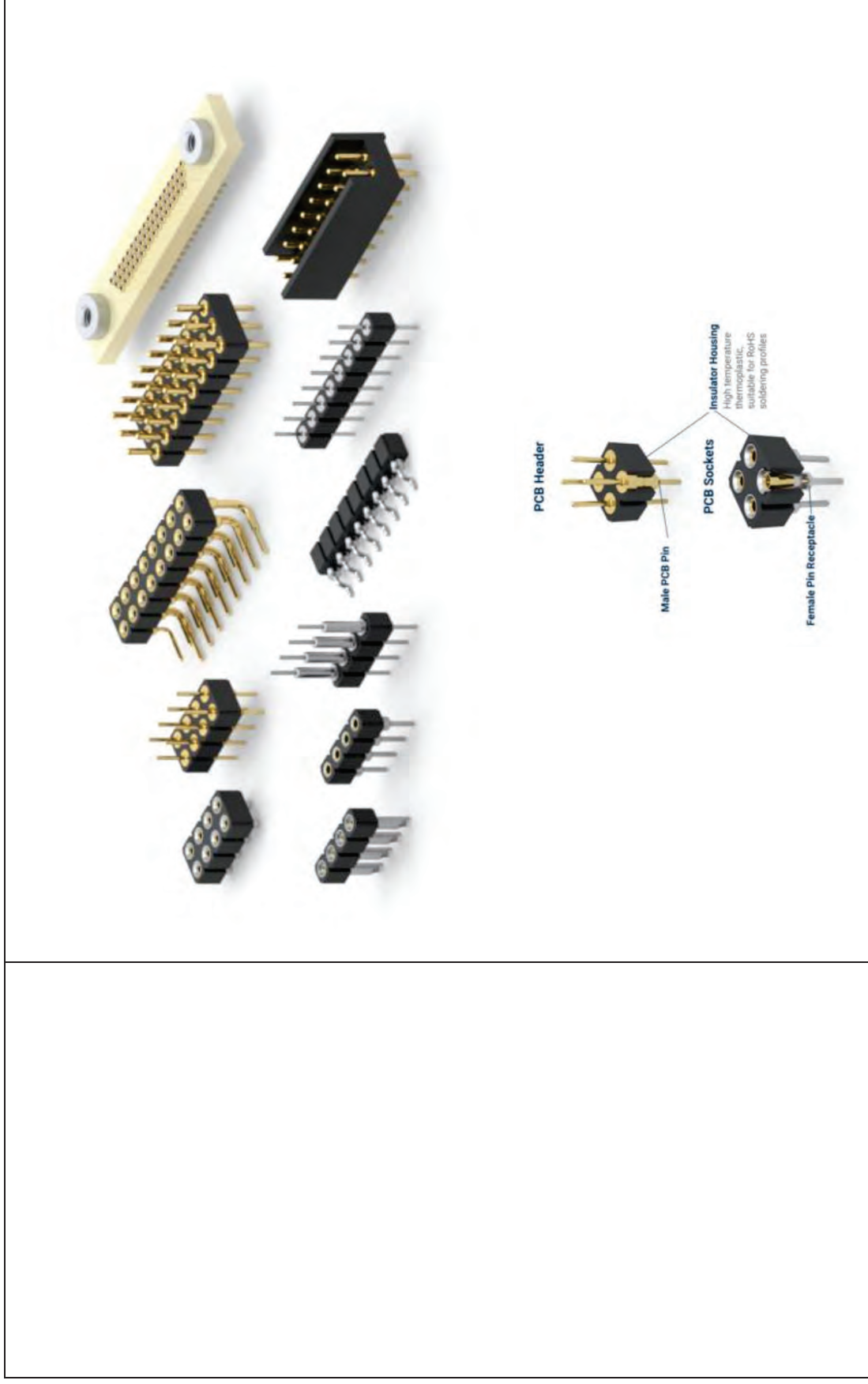
https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

	<div></div> <p>“This adaptor board connects Teensy 3.1 to thousands of LEDs using the OctoWS2811 Library.</p> <p>The adaptor features a 74HCT245 buffer chip and 100 ohm impedance matching resistors. CAT6 Ethernet cable is used from this board to the LED strips. CAT6 cable is designed for very high bandwidth, minimal cross-talk between twisted pairs, and 100 ohm impedance, for a very high quality signal. The RJ-45 network jacks allow your LED array to be easily disconnected from the electronics.</p> <p>...</p> <p>Teensy 3.1 is added on top of the adaptor using stacking header pins, or a header and socket pair if you wish to be able to remove the Teensy 3.1 board.”</p>
--	--

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>https://web.archive.org/web/20141221070129/http://www.pjrc.com/store/octo28_adaptor.html</p> <div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status:</div><div>In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <p>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>
--	--

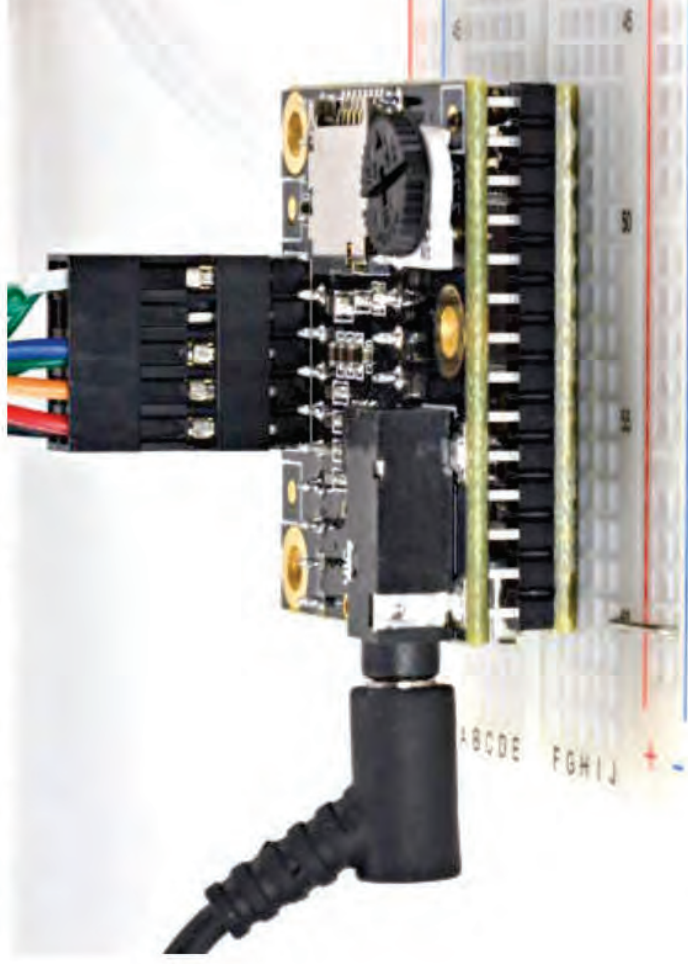




Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Teensy Board discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate.</p> <p><i>See, e.g.:</i></p>

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).

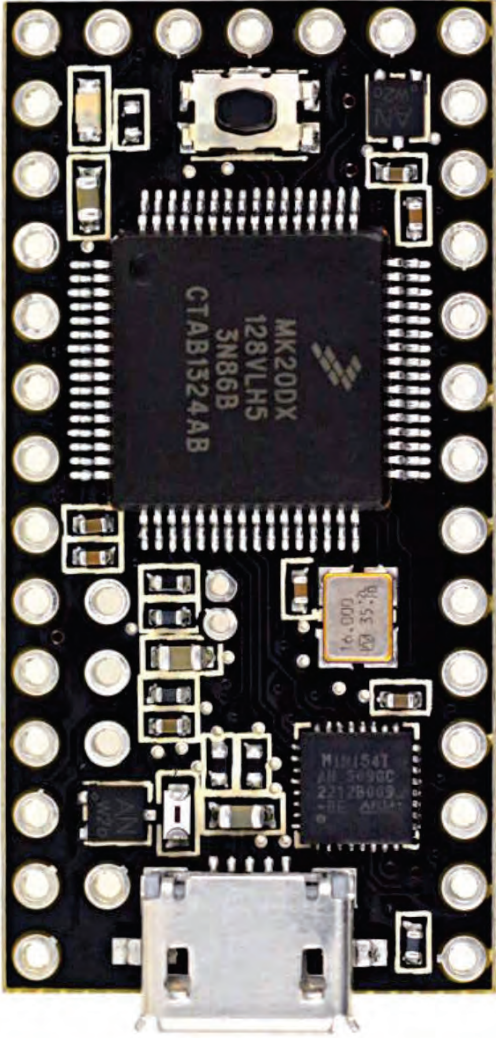


The optional volume knob and line in/out header are also added.

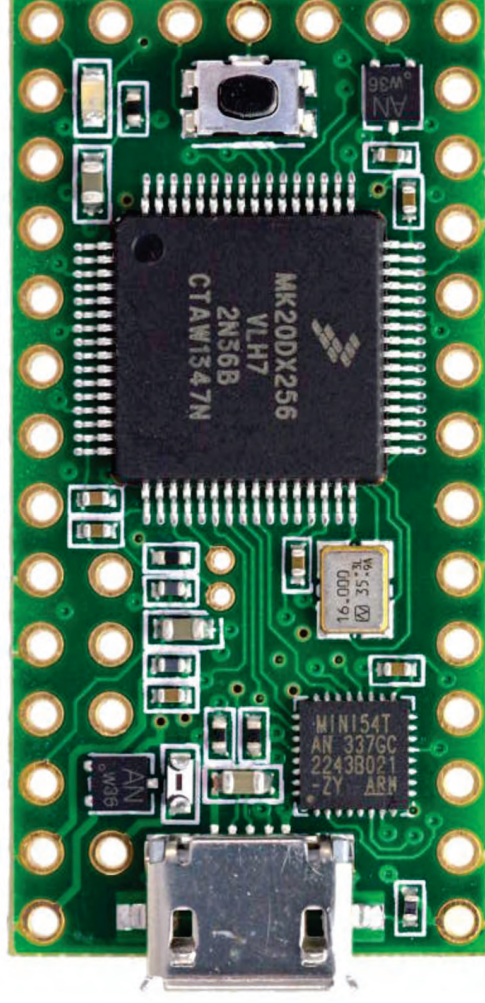
“This audio adaptor lets you easily add high quality 16 bit, 44.1 kHz sample rate (CD quality) audio to your projects with Teensy 3.0 or 3.1. It supports stereo headphone and stereo line-level output, and also stereo line-level input or mono microphone input.

The Teensy Audio Library lets you use the input and output simultaneously together with a toolkit of audio processing objects, to easily create all types of sophisticated audio applications. You can

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>play multiple sound files, create synthesized waveforms, apply effects, mix multiple streams and output high quality audio to the headphones or line out pins.</p> <p>Teensy 3.0 & 3.1 have the Cortex-M4 DSP instructions which provide plenty of computational power for real-time FFT (spectrum analysis), opening up the possibility of creating advanced sound-reactive projects.”</p> <p>https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html</p>  <p>“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.0 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”</p> <p>https://web.archive.org/web/20141221111436/http://www.pjrc.com/store/teensy3.html</p>
--	---

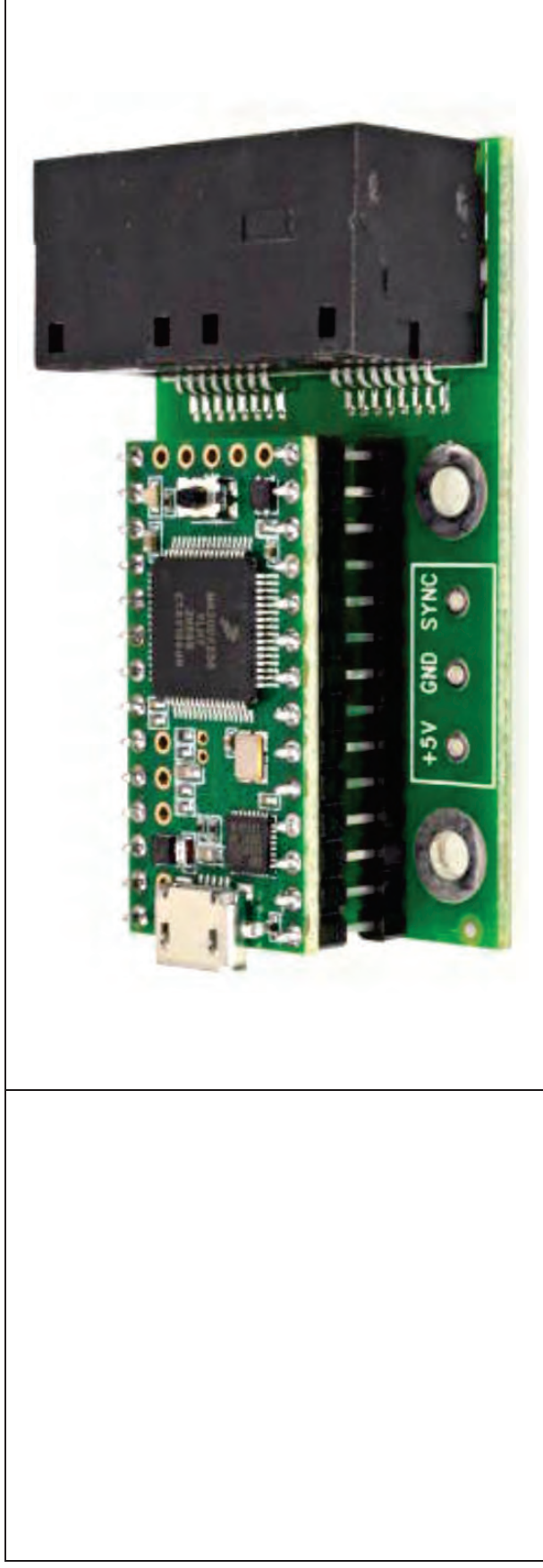
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

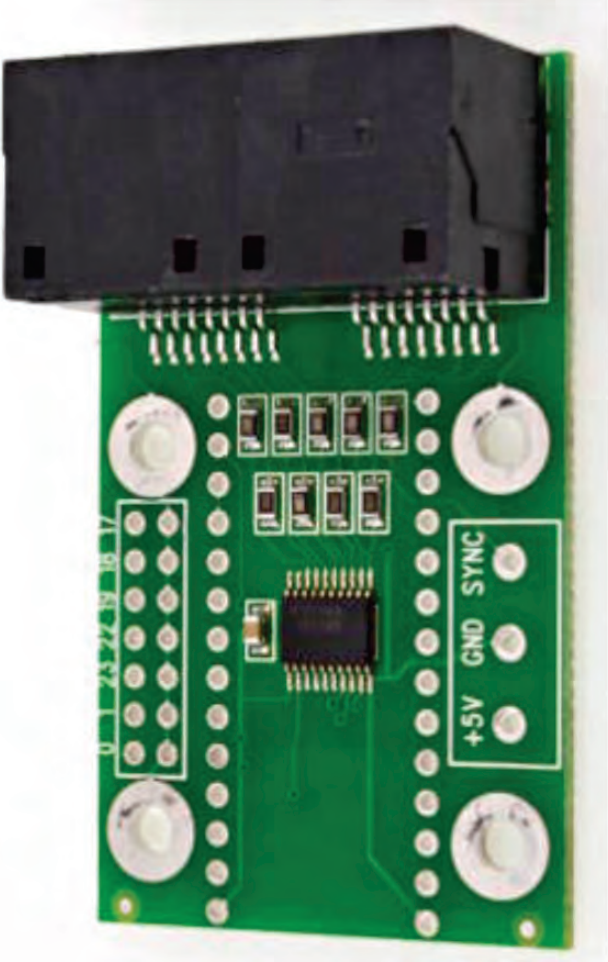


“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.1 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

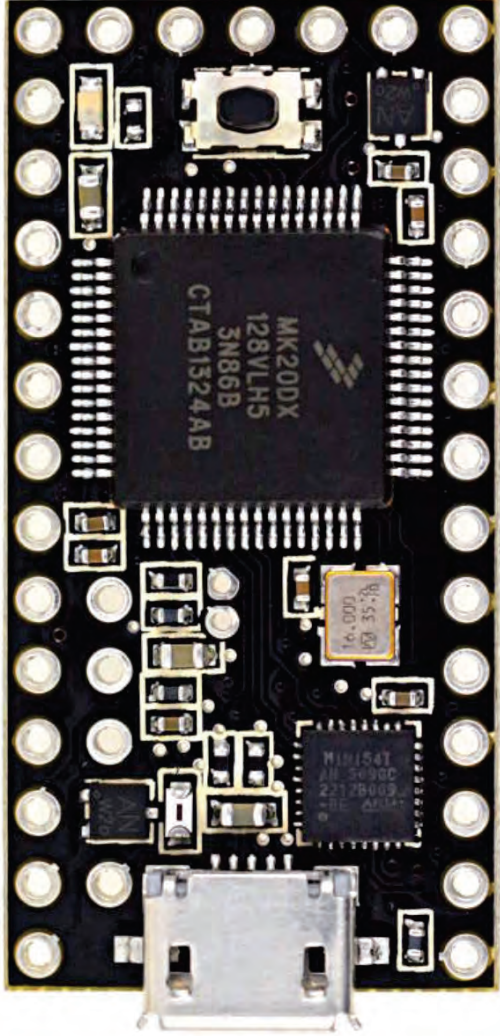
<https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



	<div></div> <p>“This adaptor board connects Teensy 3.1 to thousands of LEDs using the OctoWS2811 Library.</p> <p>The adaptor features a 74HCT245 buffer chip and 100 ohm impedance matching resistors. CAT6 Ethernet cable is used from this board to the LED strips. CAT6 cable is designed for very high bandwidth, minimal cross-talk between twisted pairs, and 100 ohm impedance, for a very high quality signal. The RJ-45 network jacks allow your LED array to be easily disconnected from the electronics.</p> <p>...</p> <p>Teensy 3.1 is added on top of the adaptor using stacking header pins, or a header and socket pair if you wish to be able to remove the Teensy 3.1 board.”</p>
--	--

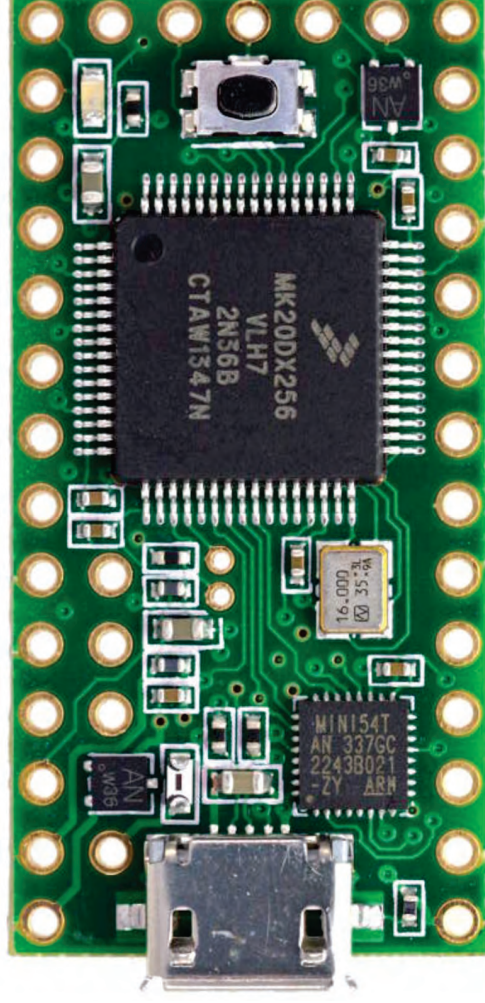
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>https://web.archive.org/web/20141221070129/http://www.pjrc.com/store/octo28_adaptor.html</p> <p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Teensy Board discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p>See, e.g.:</p> 

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

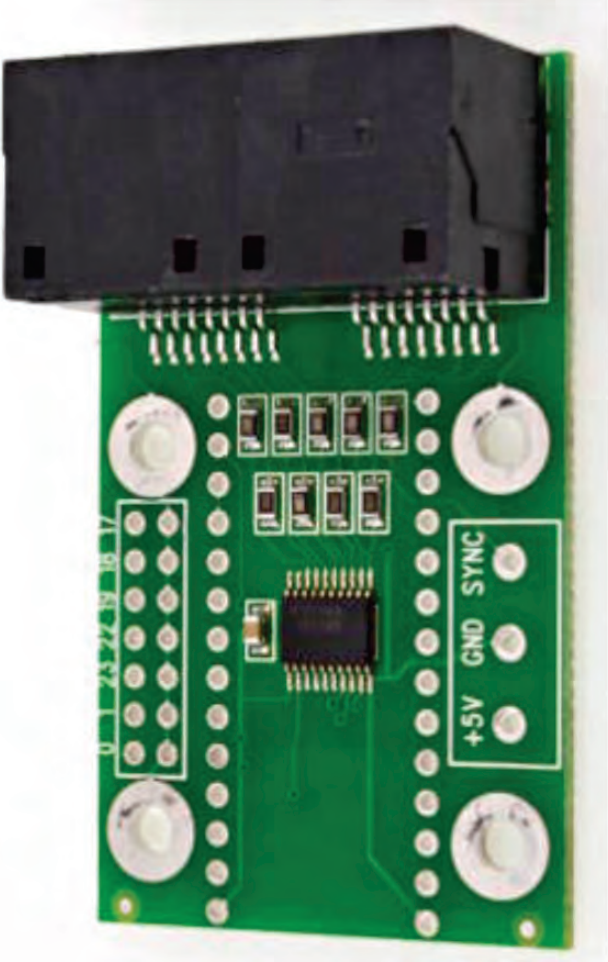
“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.0 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221111436/http://www.pjrc.com/store/teensy3.html>



“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.1 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

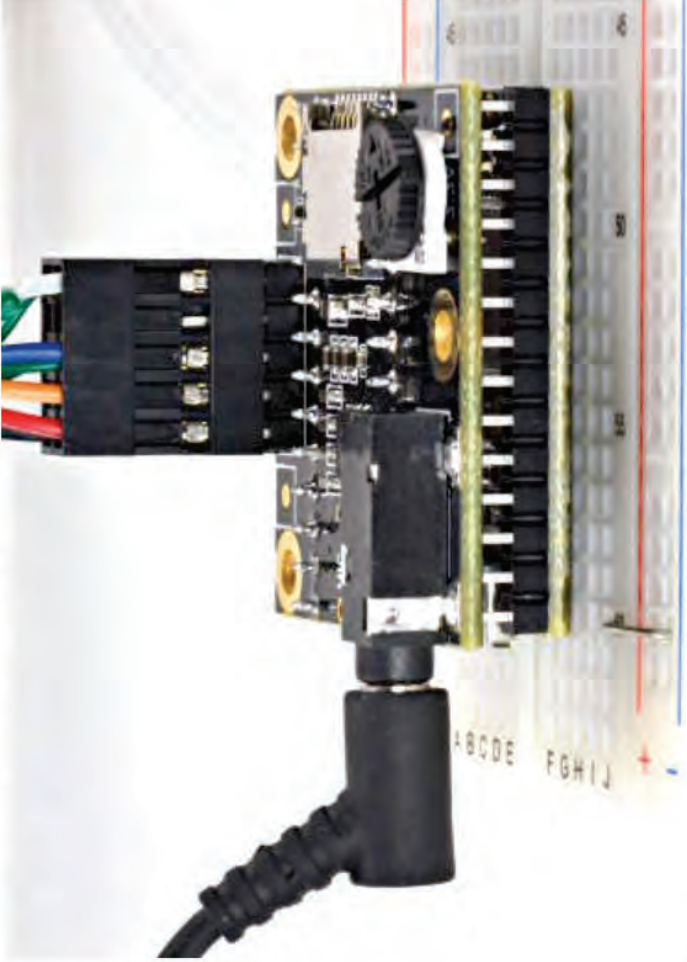
<https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html>

	 <p>“This adaptor board connects Teensy 3.1 to thousands of LEDs using the OctoWS2811 Library.</p> <p>The adaptor features a 74HCT245 buffer chip and 100 ohm impedance matching resistors. CAT6 Ethernet cable is used from this board to the LED strips. CAT6 cable is designed for very high bandwidth, minimal cross-talk between twisted pairs, and 100 ohm impedance, for a very high quality signal. The RJ-45 network jacks allow your LED array to be easily disconnected from the electronics.”</p> <p>https://web.archive.org/web/20141221070129/http://www.pjrc.com/store/octo28_adaptor.html</p>
--	--

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Teensy Board discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>This photo shows a Teensy 3.1 soldered under the audio adaptor using two 14x1 pins.</p>  <p>The optional volume knob and line in/out header are also added.</p> <p>https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html</p>
--	---

	<div><div><div><div><div><div></div><div>Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing</div></div></div><div><div><div>Add To Order</div><div>HEADER_14x1</div><div>Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing</div><div>\$1.00</div></div></div></div><div><div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div></div><div></div><div>https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html</div></div></div>
--	---

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

Inventory Status: **In Stock**

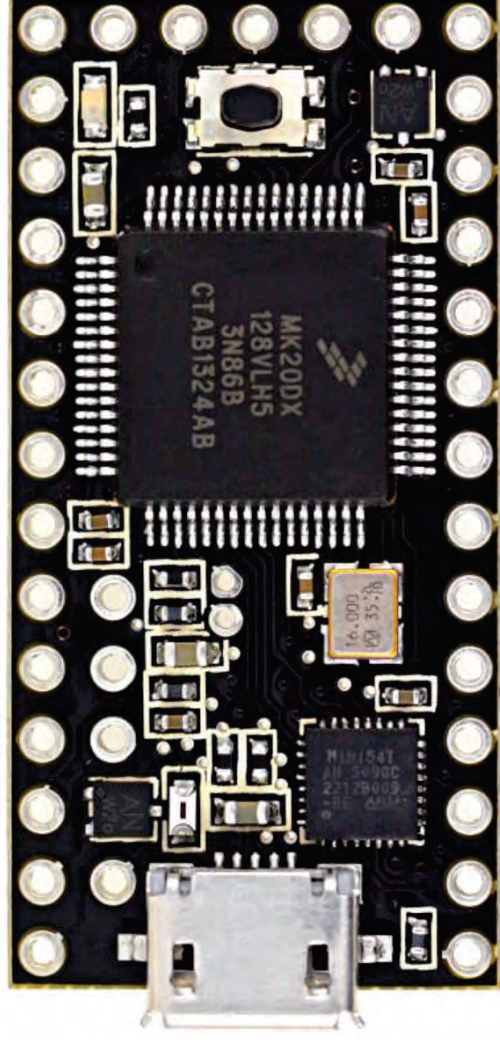
Last physical count: Dec 8, 2014



“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”

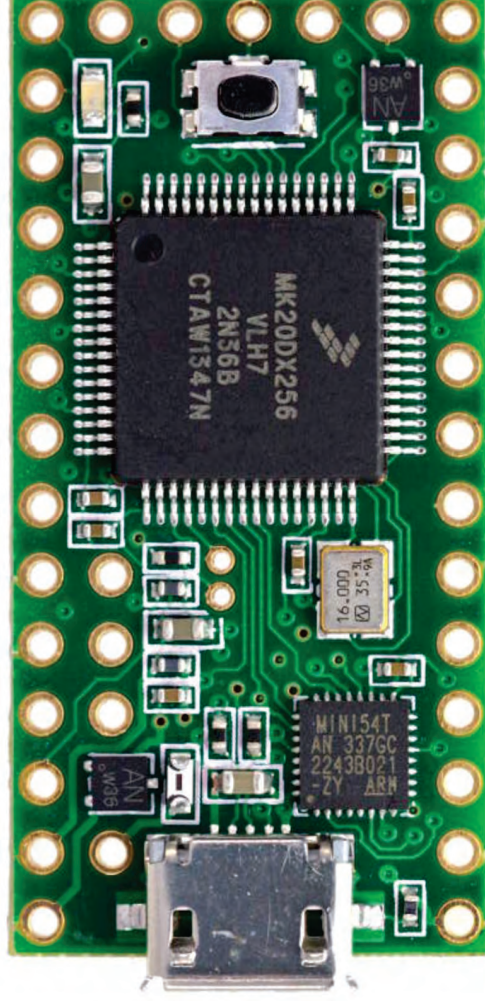
https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.0 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

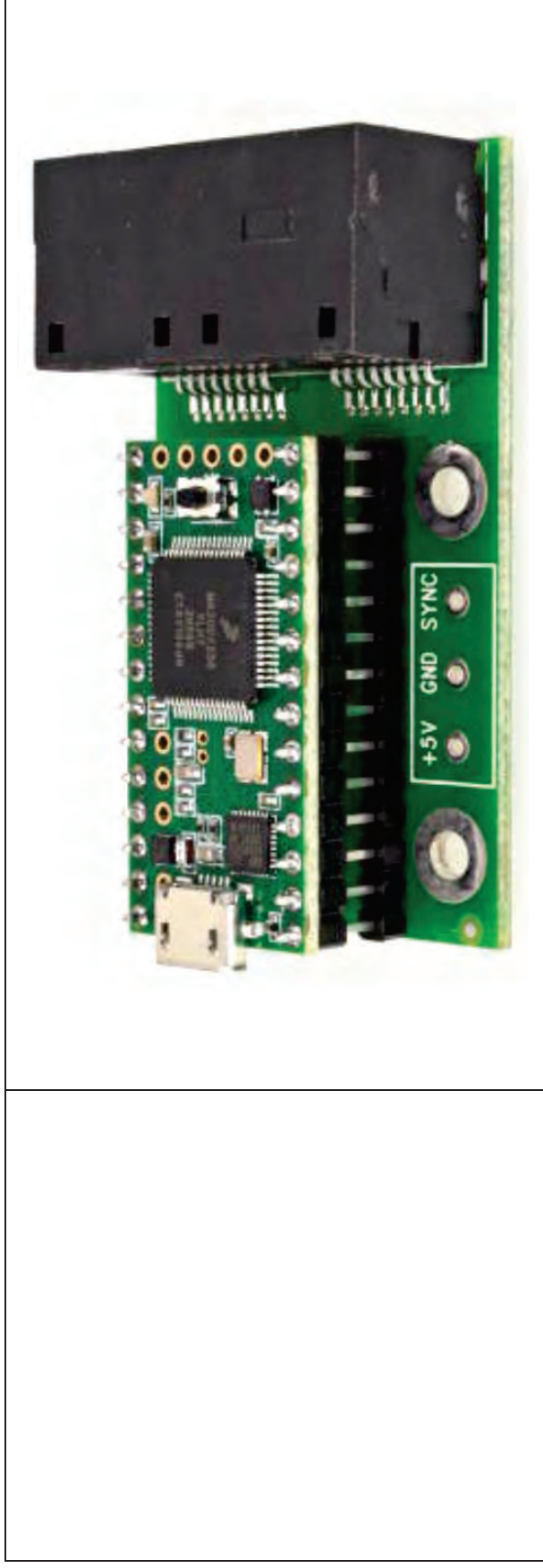
<https://web.archive.org/web/20141221111436/http://www.pjrc.com/store/teensy3.html>



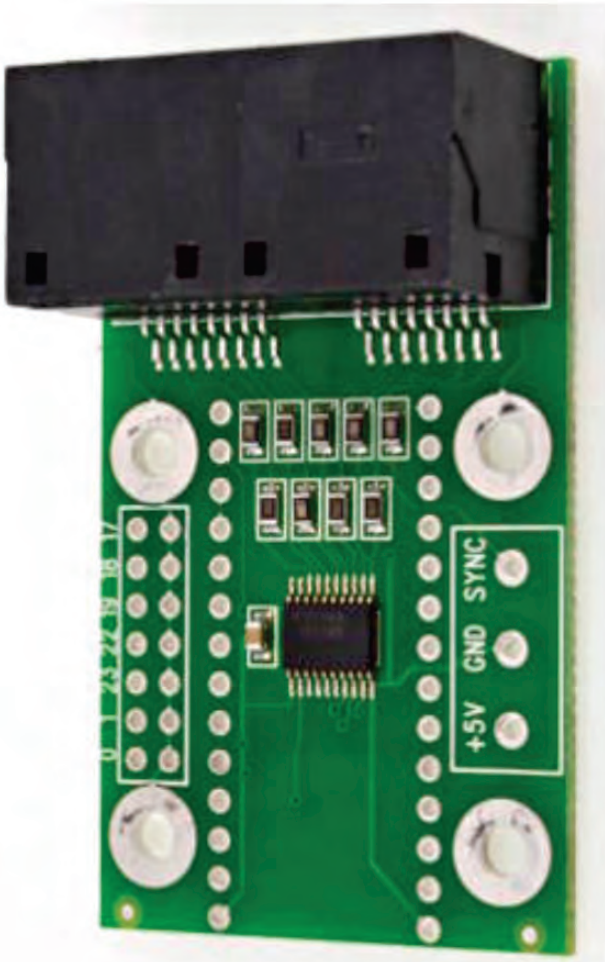
“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.1 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



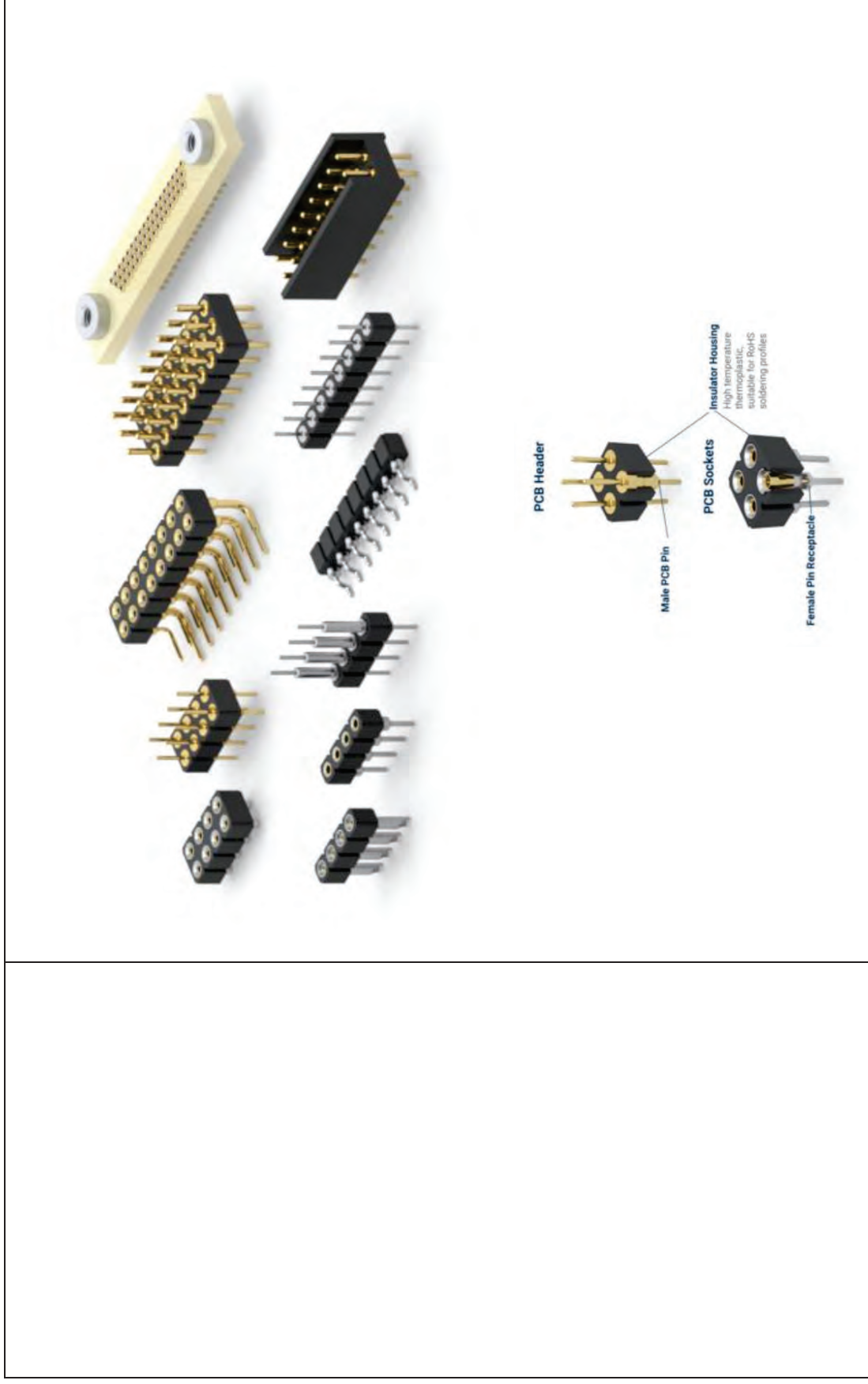
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	 <p>https://web.archive.org/web/20141221070129/http://www.pjrc.com/store/octo28_adaptor.html</p>
--	---

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator \$0.85</div></div> <div><div>Inventory Status: In Stock Last physical count: Dec 8, 2014</div><div></div></div> <div>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html<p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p><p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p></div>
--	--





Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

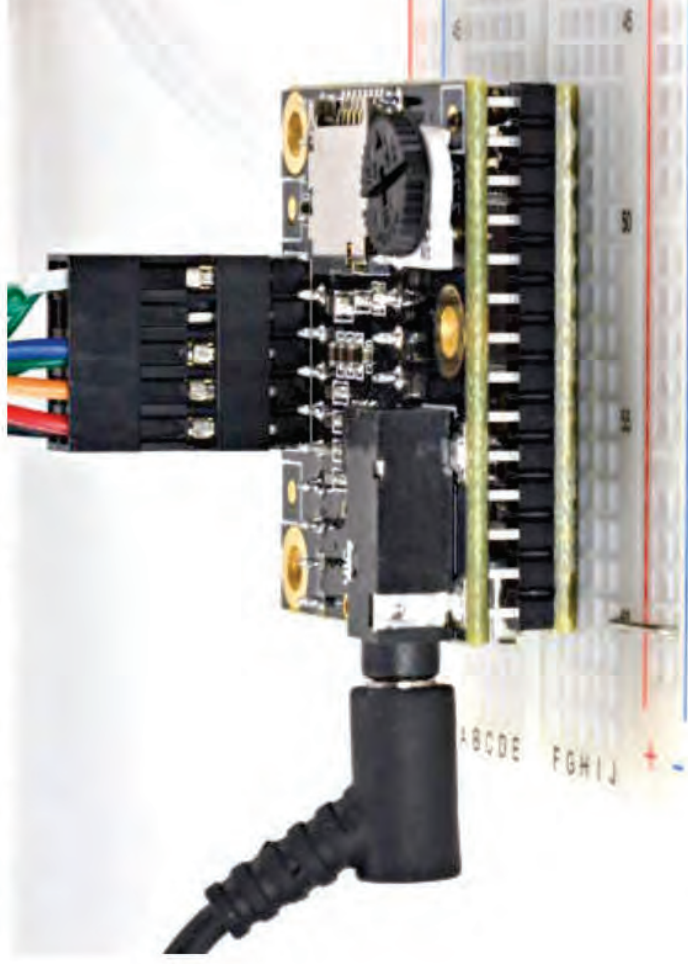
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	---

Claim 2

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Teensy Board discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

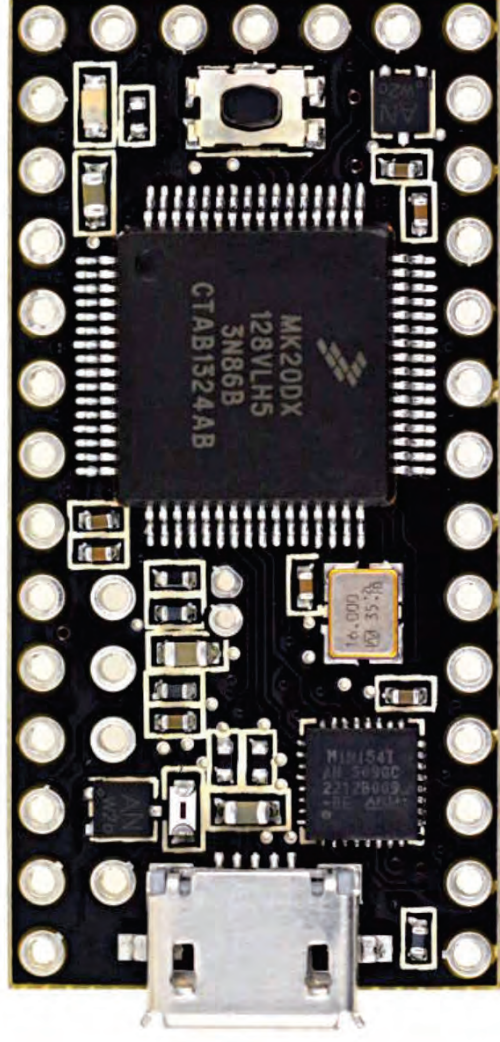
This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



The optional volume knob and line in/out header are also added.

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html

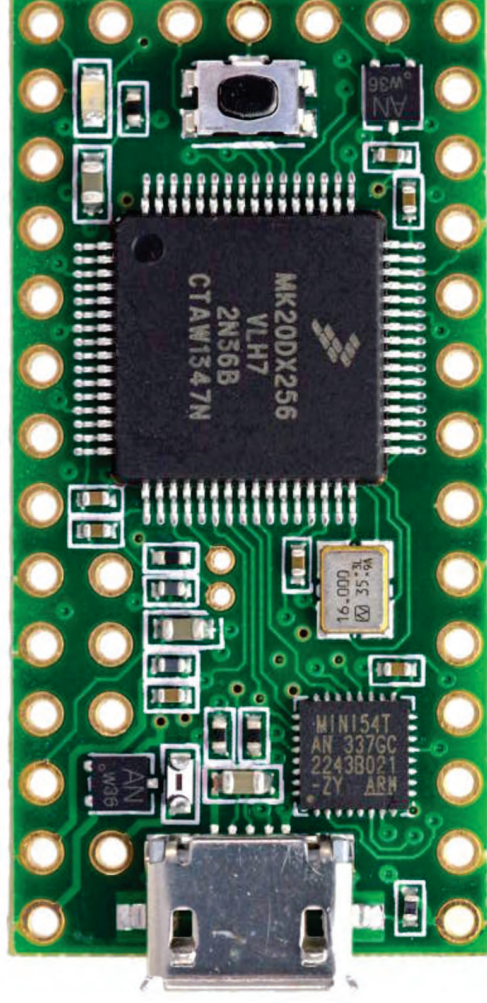
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.0 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221111436/http://www.pjrc.com/store/teensy3.html>

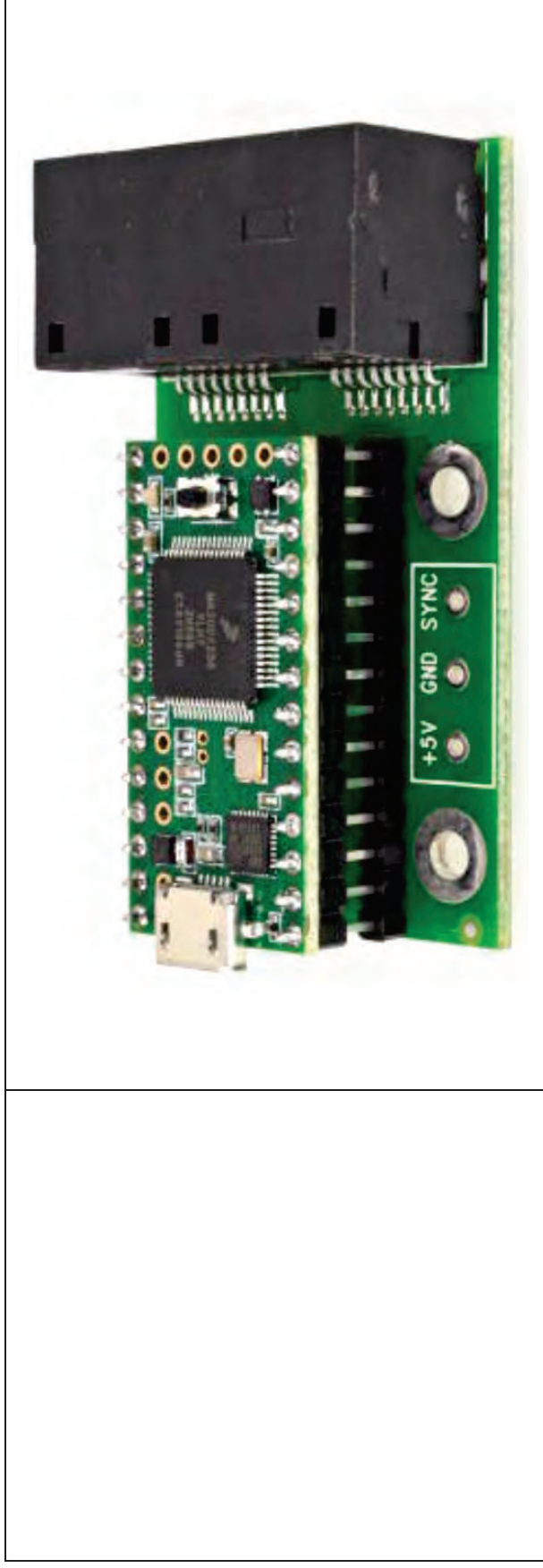
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

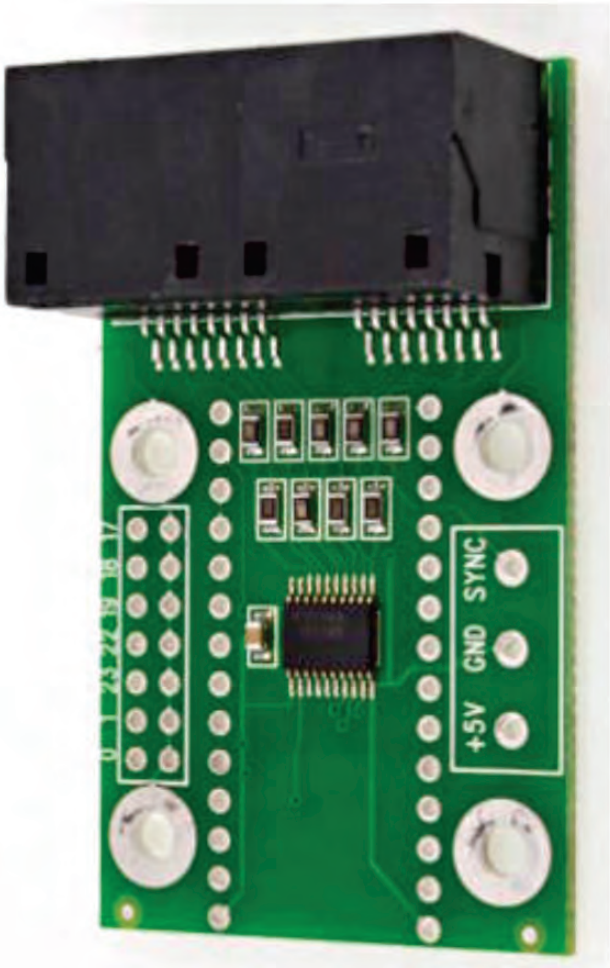


“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.1 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



	<div></div> <div><p>https://web.archive.org/web/20141221070129/http://www.pjrc.com/store/octo28_adaptor.html</p></div> <div><p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	---

Claim 3

Claim Limitation	Disclosure
------------------	------------

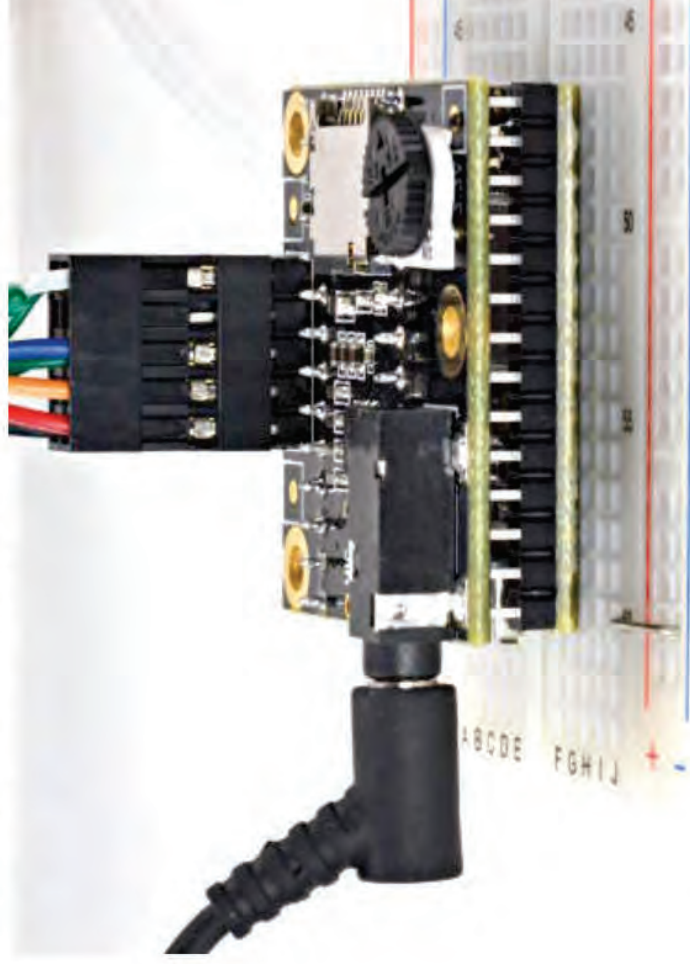
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

Teensy Board discloses, either expressly or inherently, a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

See, e.g.:

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



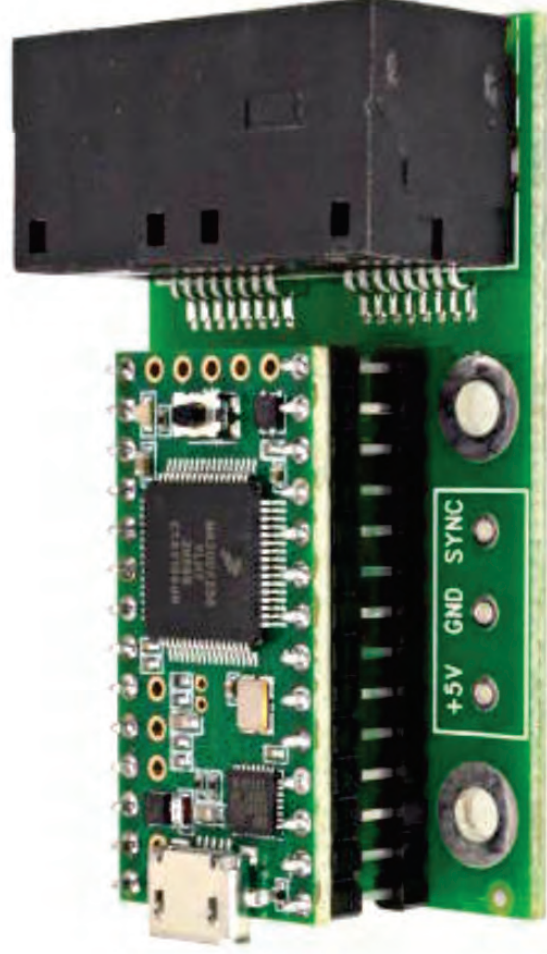
The optional volume knob and line in/out header are also added.

	 <p>“This audio adaptor lets you easily add high quality 16 bit, 44.1 kHz sample rate (CD quality) audio to your projects with Teensy 3.0 or 3.1. It supports stereo headphone and stereo line-level output, and also stereo line-level input or mono microphone input.</p> <p>The Teensy Audio Library lets you use the input and output simultaneously together with a toolkit of audio processing objects, to easily create all types of sophisticated audio applications. You can play multiple sound files, create synthesized waveforms, apply effects, mix multiple streams and output high quality audio to the headphones or line out pins.</p>
--	--

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

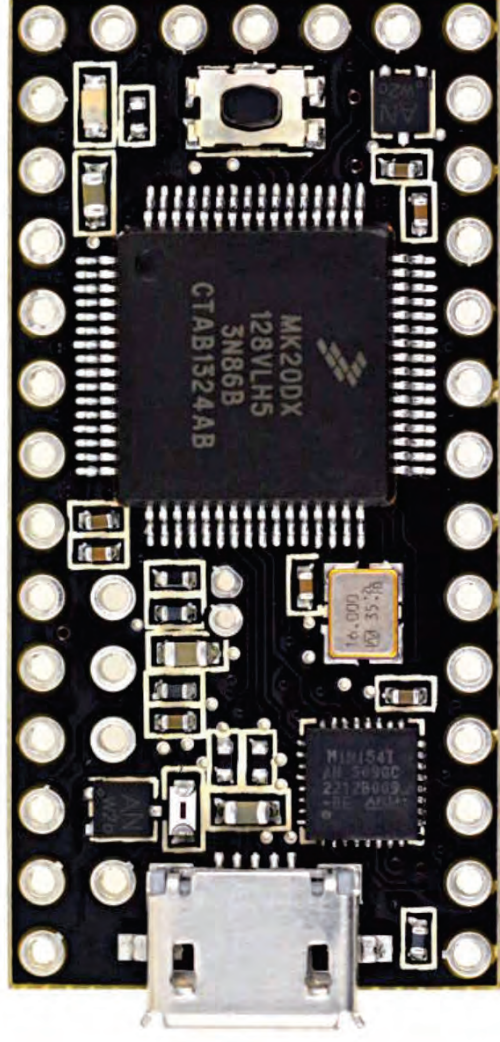
Teensy 3.0 & 3.1 have the Cortex-M4 DSP instructions which provide plenty of computational power for real-time FFT (spectrum analysis), opening up the possibility of creating advanced sound-reactive projects.”

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html



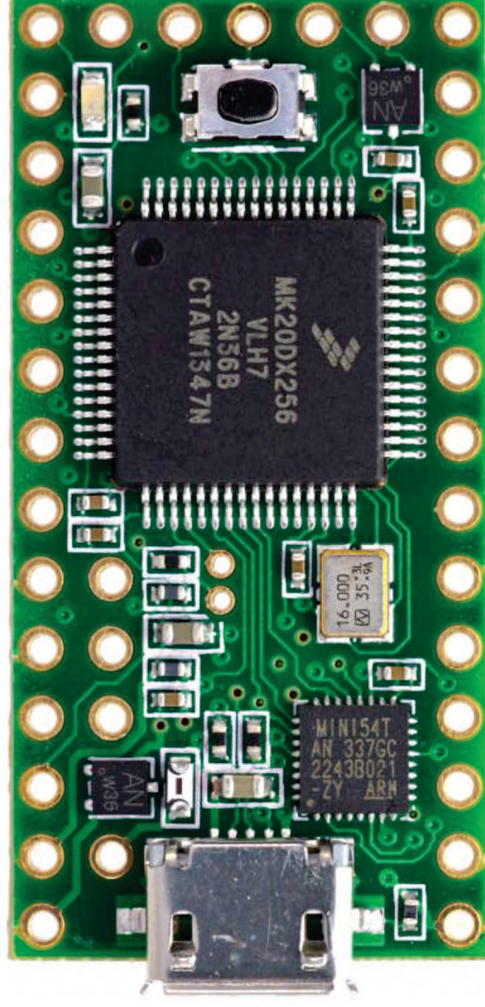
https://web.archive.org/web/20141221070129/http://www.pjrc.com/store/octo28_adaptor.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.0 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221111436/http://www.pjrc.com/store/teensy3.html>



“The Teensy USB Development Board is a complete USB-based microcontroller development system. Version 3.1 features a 32 bit ARM processor. All Teensy boards are shipped assembled and fully tested.”

<https://web.archive.org/web/20141221071236/http://www.pjrc.com/store/teensy31.html>

To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

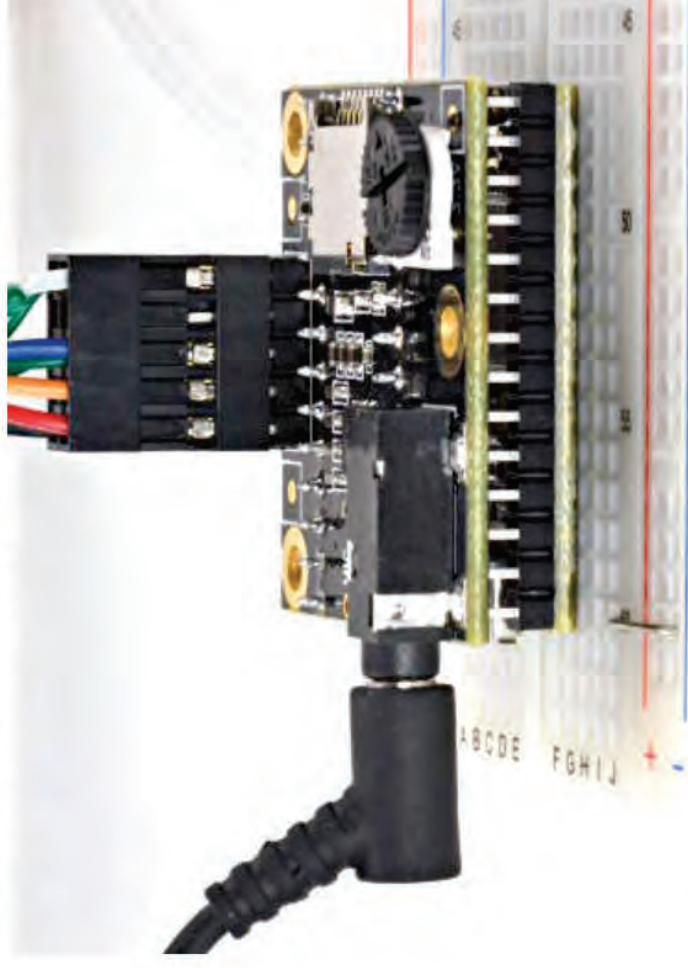
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Claim 4

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>Teensy Board discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



The optional volume knob and line in/out header are also added.

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html

	<div><div><div><div><div><div></div><div>Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing</div></div></div><div><div><div>Add To Order</div><div>HEADER_14x1</div></div><div><div>Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing</div><div>\$1.00</div></div></div></div><div><div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div></div><div></div><div>https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html</div></div></div>
--	--

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

Inventory Status: **In Stock**

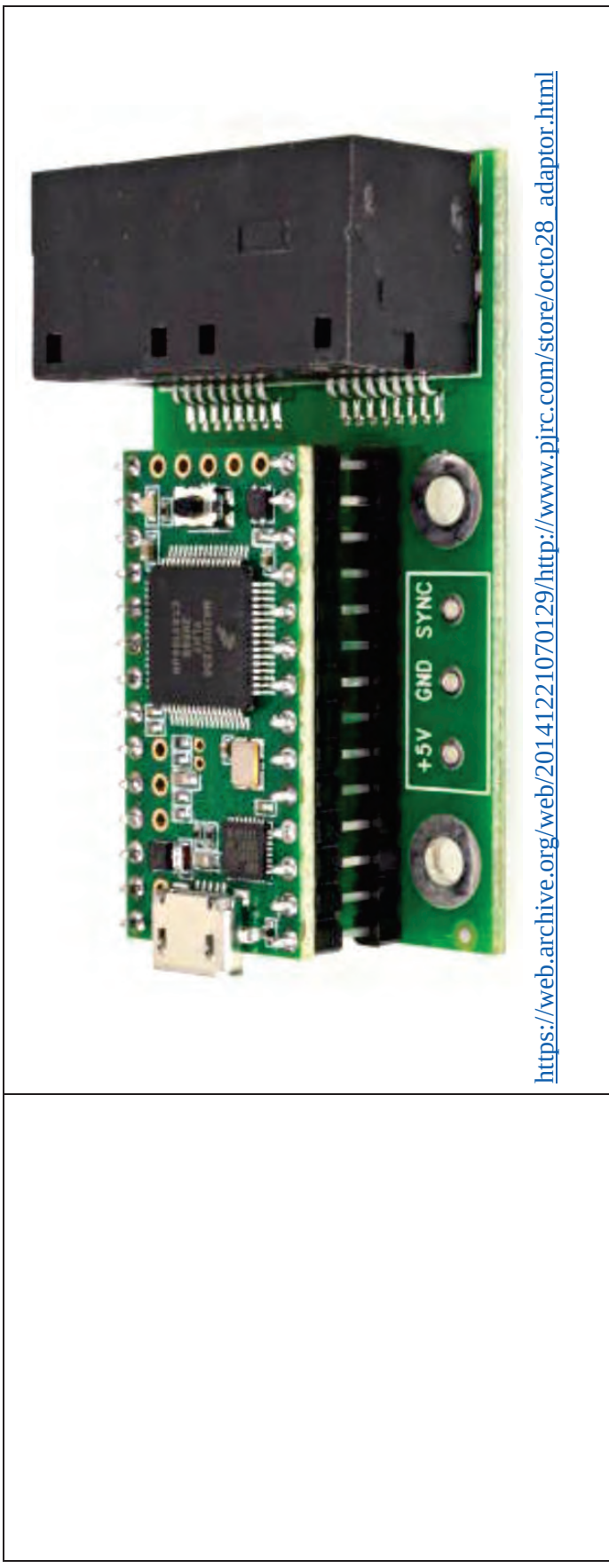
Last physical count: Dec 8, 2014



“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”

https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

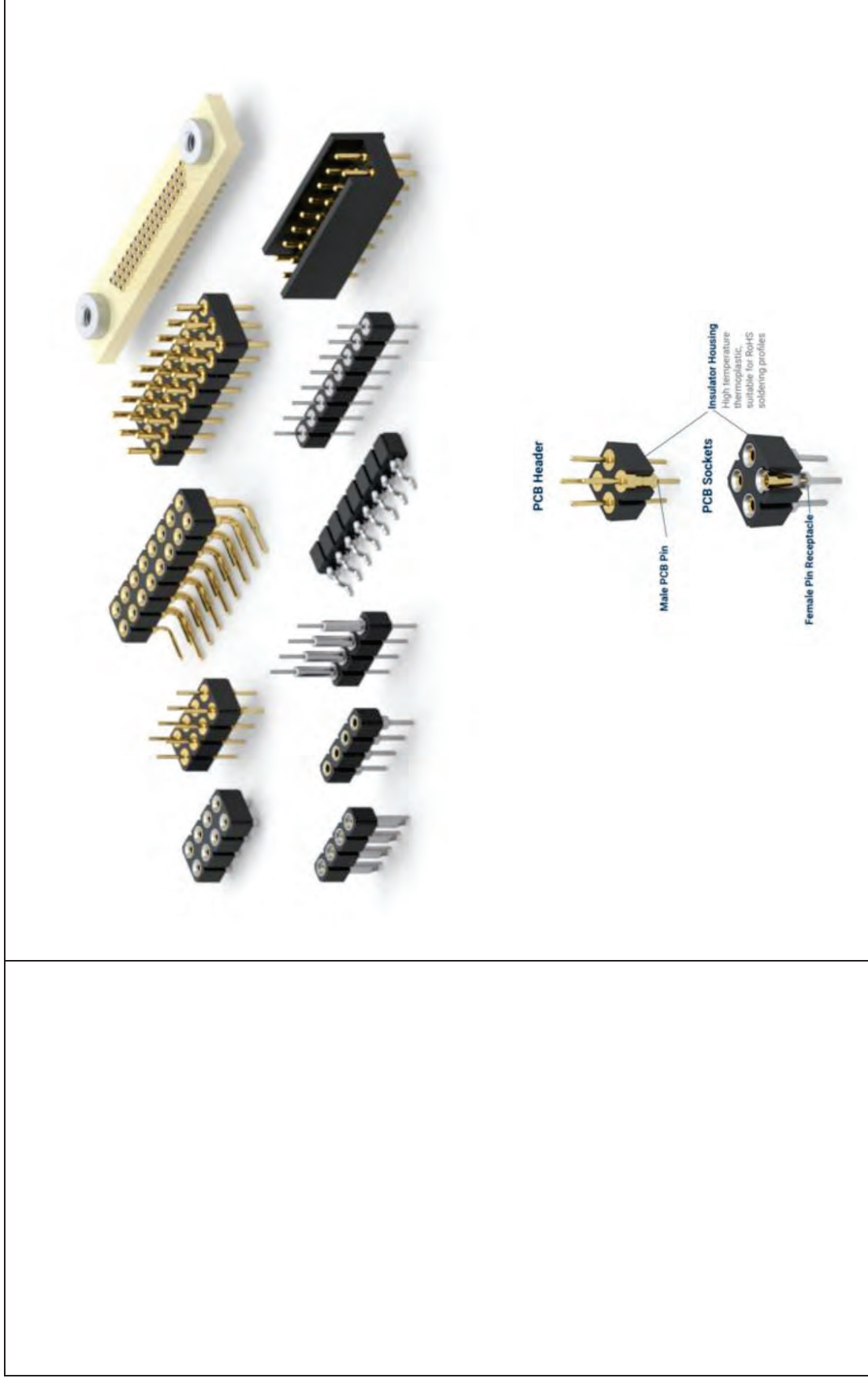
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator \$0.85</div></div> <div><div>Inventory Status: In Stock Last physical count: Dec 8, 2014</div><div></div></div> <div>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html<p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p><p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p></div>
--	--





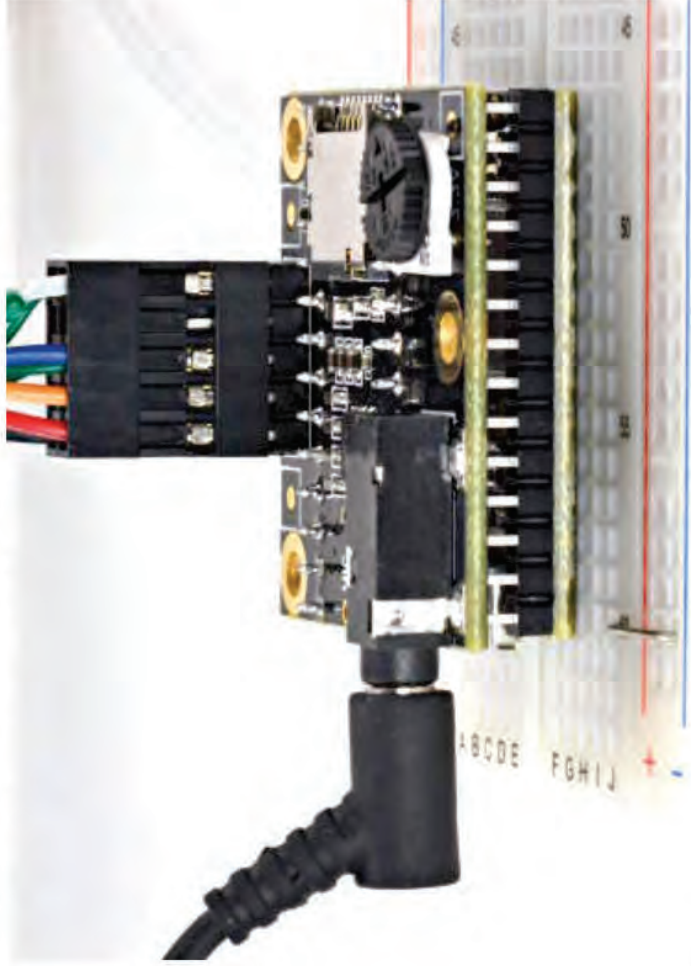
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Claim 6

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>	<p>Teensy Board discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

<p>corresponding top metal pads of the spacer connector.</p>	<p>This photo shows a Teensy 3.1 soldered under the audio adaptor using two 14x1 pins.</p>  <p>The optional volume knob and line in/out header are also added.</p> <p>https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html</p>
--	--

Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing

Add To Order

HEADER 14x1

Pins (header), 14 pins, 0.1 inch (2.54 mm) spacing

\$1.00

Inventory Status:	In Stock

Inventory Status: **In Stock**
Last physical count: Dec 8 2014



https://web.archive.org/web/20141221190227/http://www.pjrc.com/store/header_14x1.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

Inventory Status: **In Stock**

Last physical count: Dec 8, 2014



“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”

https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

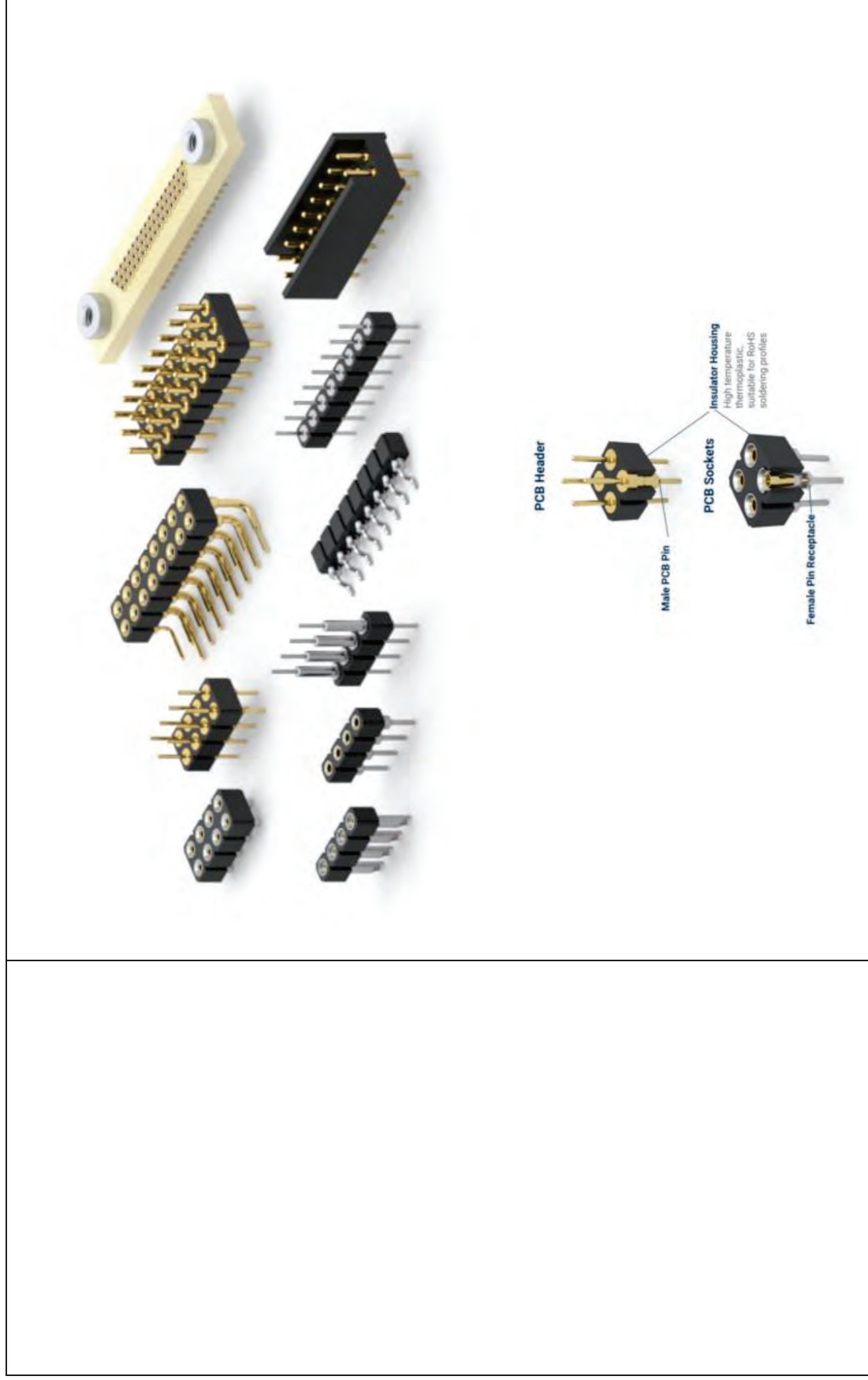
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator \$0.85</div></div> <div><div>Inventory Status: In Stock Last physical count: Dec 8, 2014</div><div></div></div> <div>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html<p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p><p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p></div>
--	--





Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

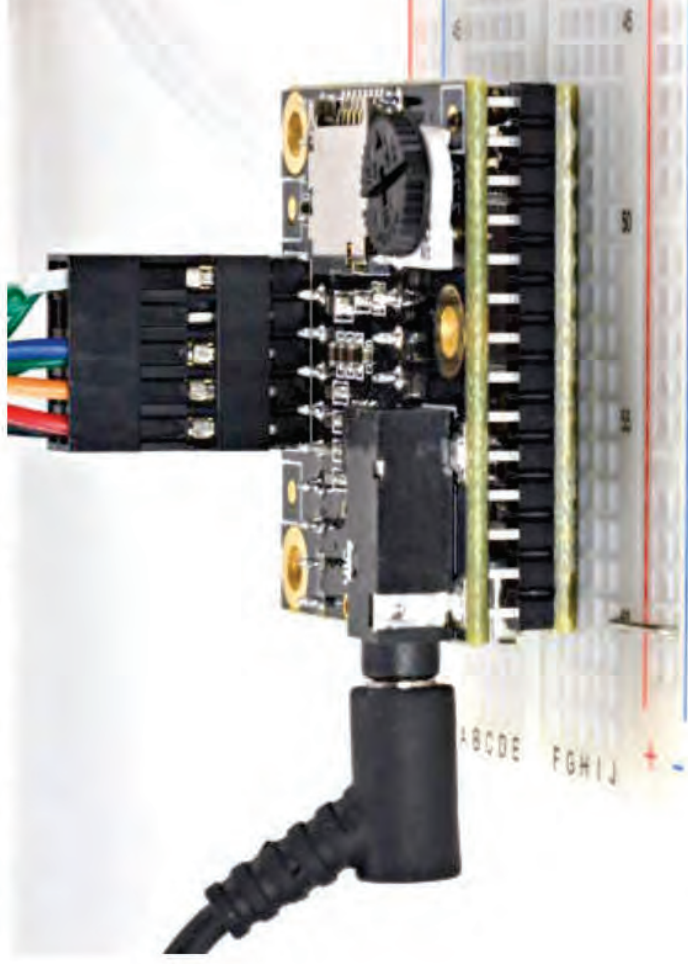
Claim 9

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the</p>	<p>Teensy Board discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the bottom package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

This photo shows a Teensy 3.1 soldered under the audio adaptor using two [14x1 pins](#).



The optional volume knob and line in/out header are also added.

https://web.archive.org/web/20141221060821/http://www.pjrc.com/store/teensy3_audio.html

Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

Add To Order

HEADER_14x1_D

Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator

\$0.85

Inventory Status: **In Stock**

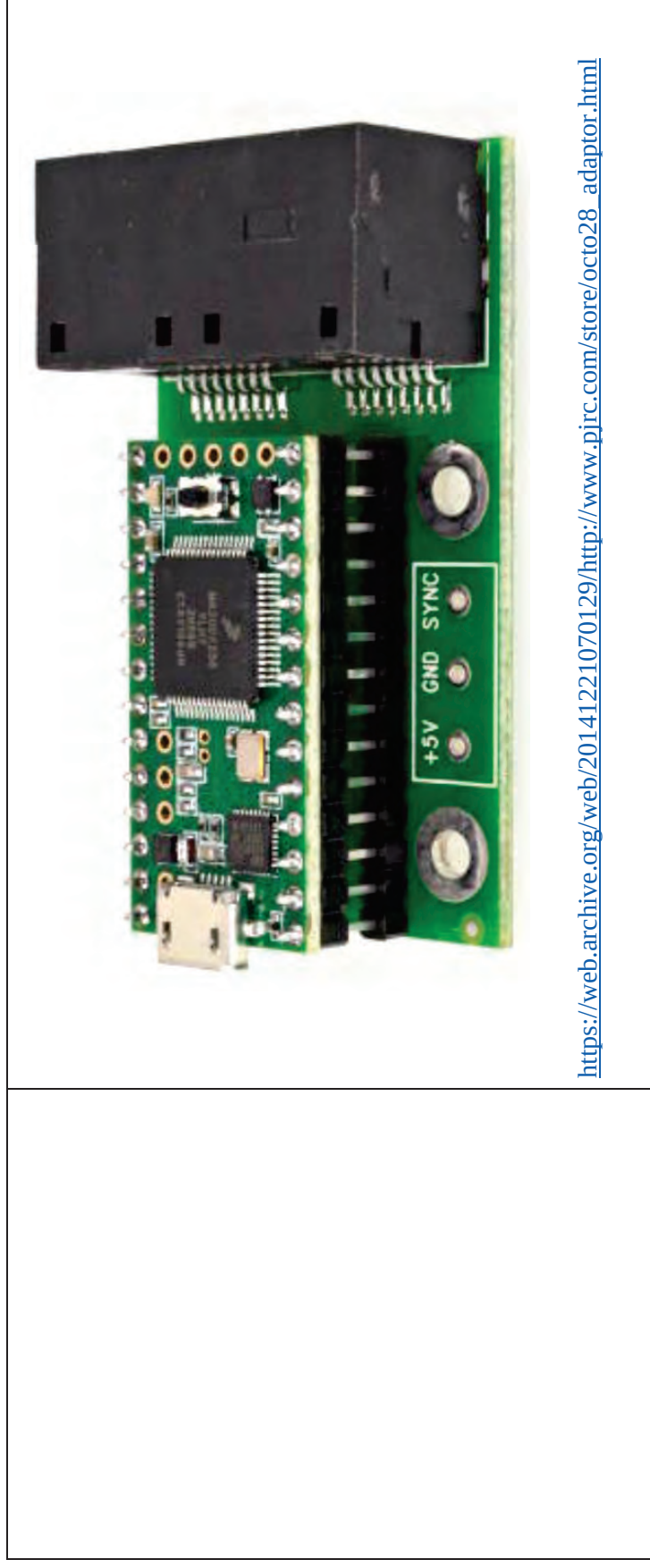
Last physical count: Dec 8, 2014



“This special 14 pin header has two insulators, which makes it very easy to solder the Audio Adaptor to a Teensy 3.0 or 3.1 board. Two headers are needed.”

https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html

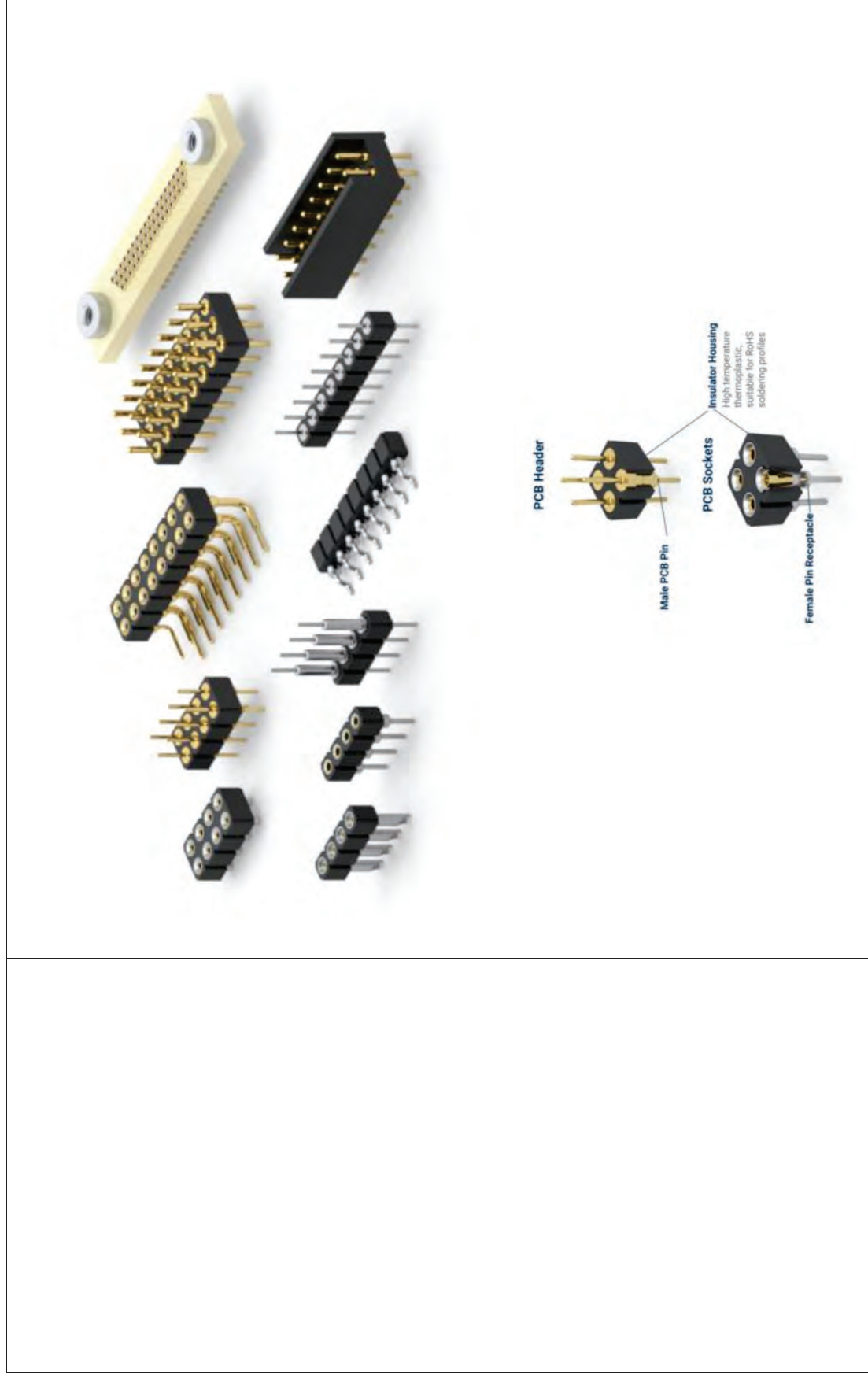
Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board



Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<div><div>Add To Order</div><div>HEADER_14x1_D</div><div>Pins (header), 5 pins, 0.1 inch (2.54 mm) spacing, Double Insulator</div><div>\$0.85</div></div> <div><div>Inventory Status: In Stock</div><div>Last physical count: Dec 8, 2014</div></div> <div></div> <div>https://web.archive.org/web/20141221062227/http://pjrc.com/store/header_14x1_d.html</div> <div><p>To the extent Plaintiff contends that Teensy Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p><p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p></div>
--	---





Appendix A-47 - Invalidity of U.S. Patent No. 9,859,202 in view of Teensy Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

E.D. Tex. Case No. 2:25-cv-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

The Sseed stackable logic boards, including but not limited to Bugduino, Clio Main Board, MilCandy, Rainbowduino LED driver platform-Atmega 328, Sseeduino ADK Main Board, Sseeduino Ethernet, Sseeduino Lite, Arduino YUN, Sseeduino Mega, Sseeduino Stalker, Sseeduino v3.0, Freeduino USB complete Kit, Orbshield v1.0 Kit, Protoshield Kit for Arduino, and Sseeduino Mega Protoshield Kit (hereinafter “Sseed Board”) was in public use, on sale (including sold to customers and potential customers), and/or otherwise available to the public by Sseed Technology Limited at least by Dec. 14, 2014.¹ Sseed Board anticipates and/or renders obvious all Asserted Claims² of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.³ Sseed Board, or the written materials describing it, excerpted below, is prior art to the ’202 Patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Sseed Board, or otherwise rendered obvious by disclosures and teachings of Sseed Board, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Sseed Board does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Sseed Board with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 Patent. TopWire has yet to identify any limitation of the Asserted Claims that it

¹ See, e.g., https://web.archive.org/web/20141214084852/http://www.sseedstudio.com/wiki/index.php?title=Main_Page#Arduino

² As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

³ To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

contends is not fully disclosed by Sseed Board, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

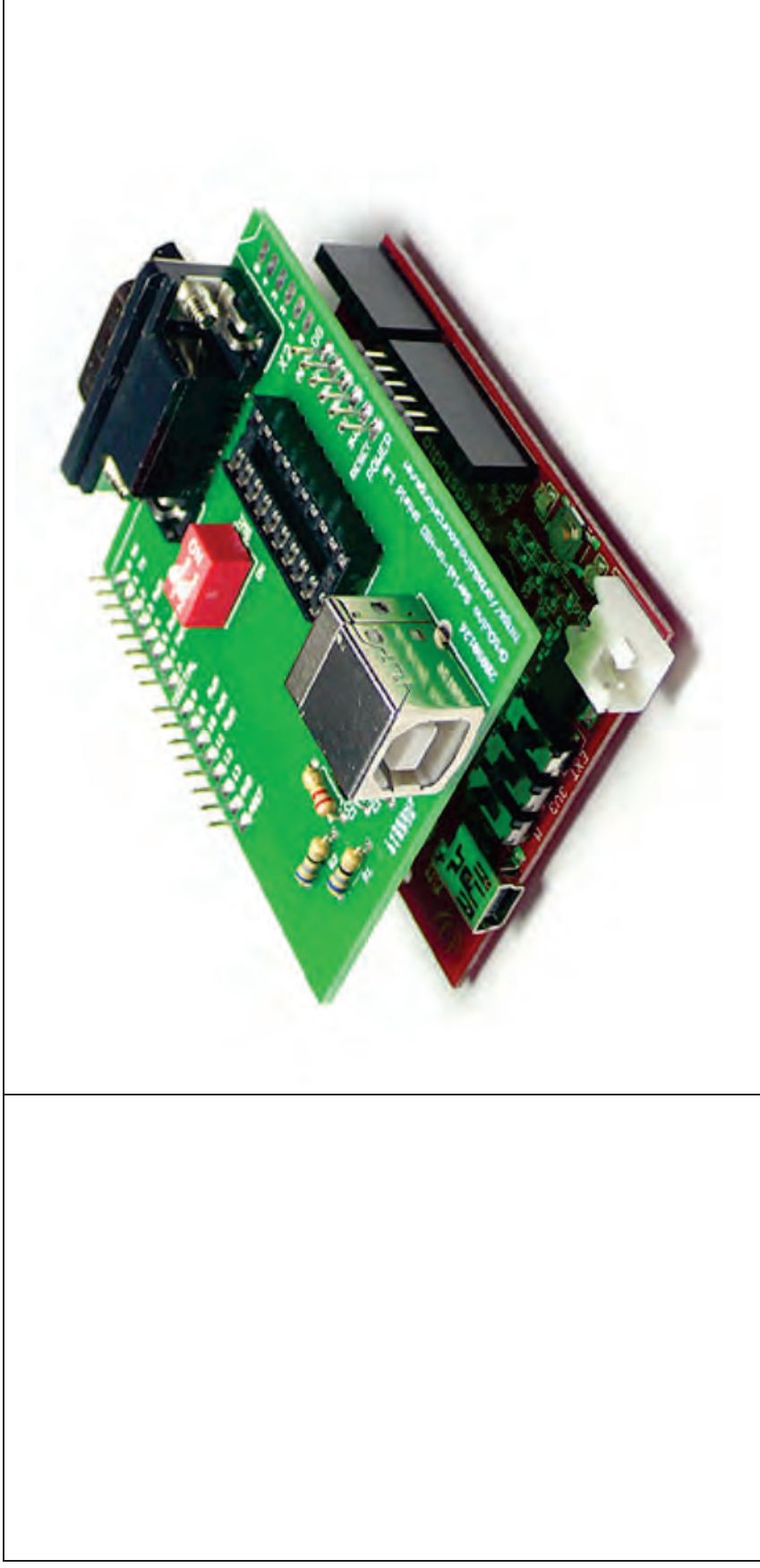
Where the chart below states that Sseed Board “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Sseed Board or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Sseed Board set forth in this chart.

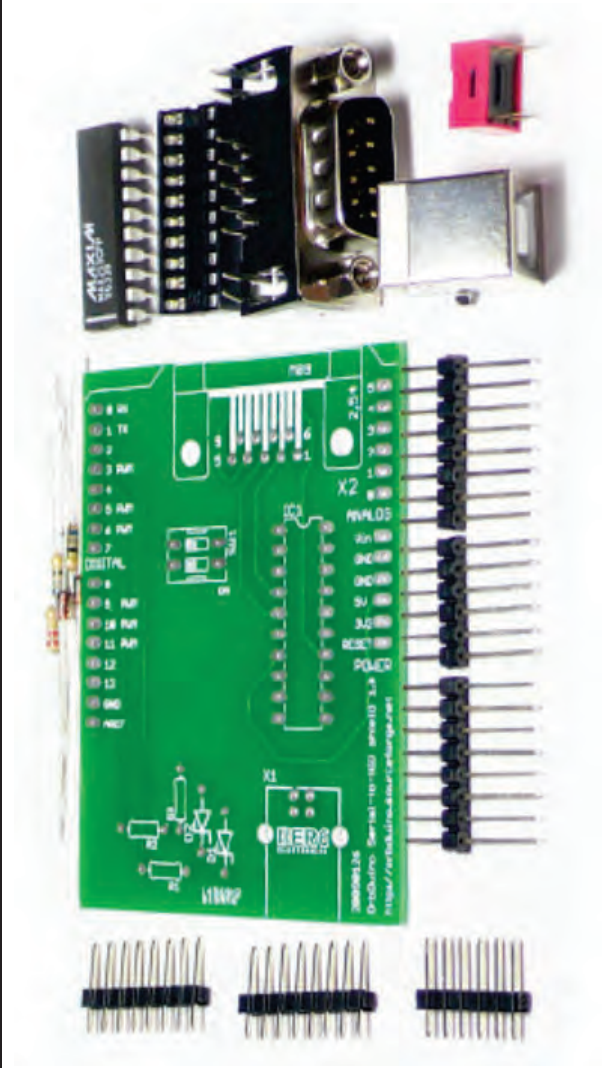
Claim 1

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, Sseed Board discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>

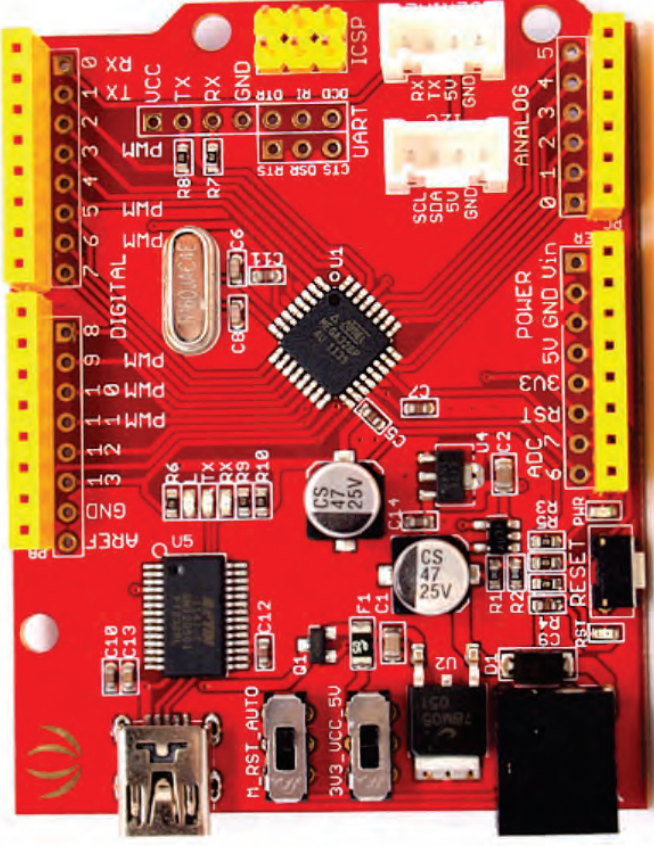
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

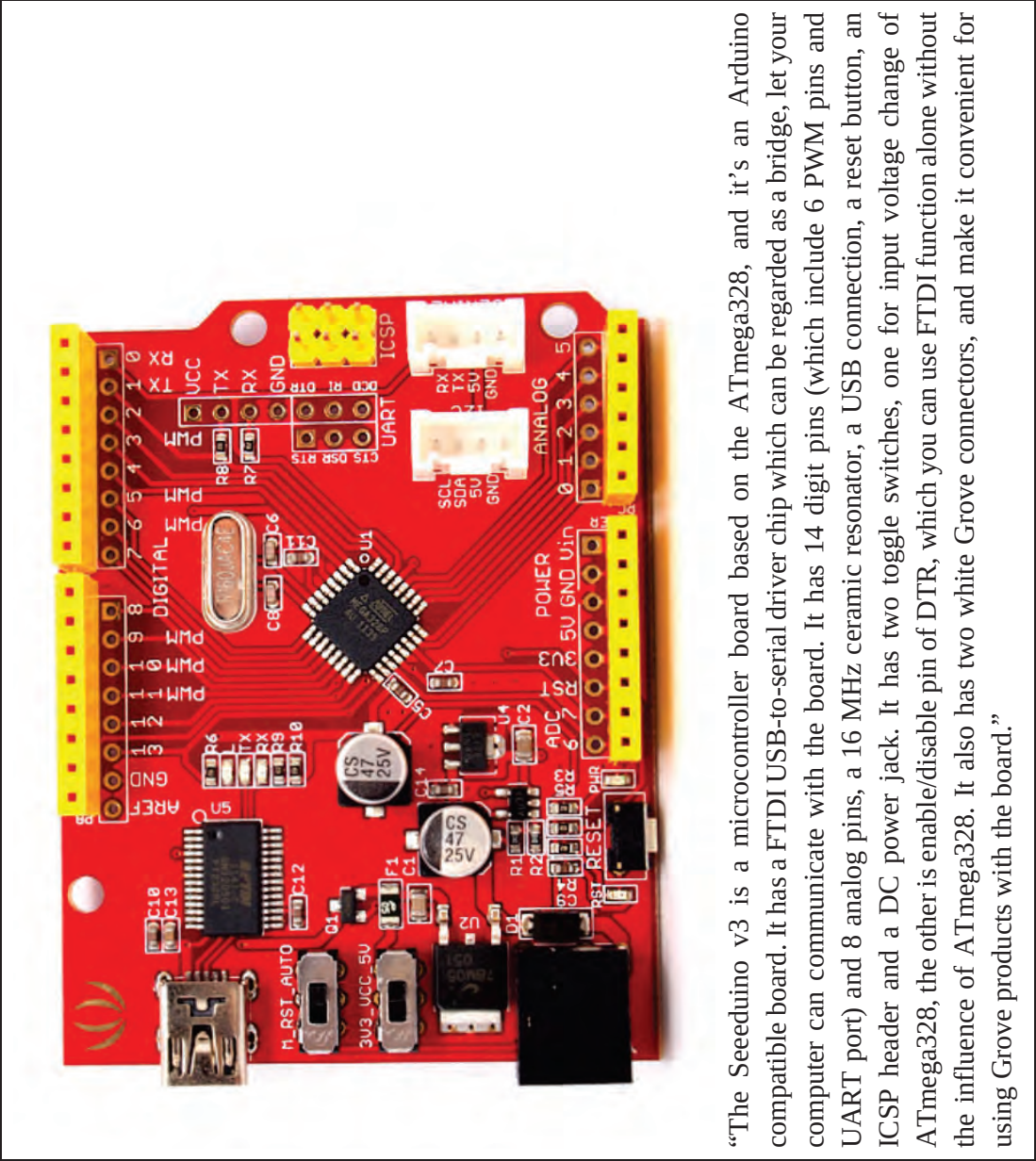
	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“The Seeeduino v3 is a microcontroller board based on the ATmega328, and it’s an Arduino compatible board. It has a FTDI USB-to-serial driver chip which can be regarded as a bridge, let your computer can communicate with the board. It has 14 digit pins (which include 6 PWM pins and UART port) and 8 analog pins, a 16 MHz ceramic resonator, a USB connection, a reset button, an ICSP header and a DC power jack. It has two toggle switches, one for input voltage change of ATmega328, the other is enable/disable pin of DTR, which you can use FTDI function alone without the influence of ATmega328. It also has two white Grove connectors, and make it convenient for using Grove products with the board.”</p>
--	--

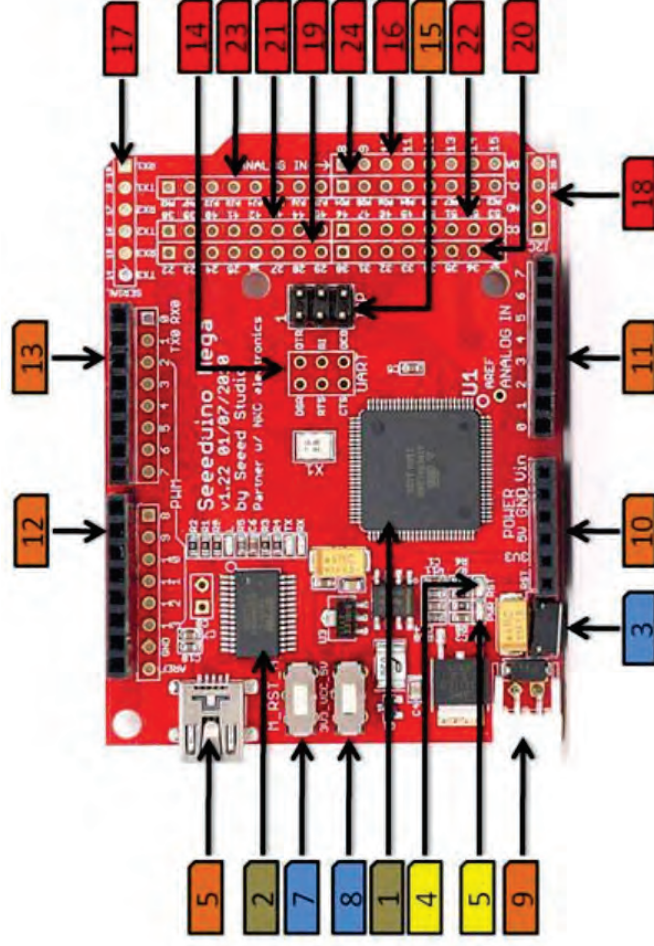
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	<p>https://web.archive.org/web/20141214140820/http://www.sseedstudio.com/wiki/Sseeduino_v3.0</p> <p>To the extent Plaintiff contends that Sseed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.A] a bottom package substrate;</p>	<p>Sseed Board discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p>



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeeduino Board

https://web.archive.org/web/20141214140820/http://www.seeedstudio.com/wiki/Seeeduino_v3.0



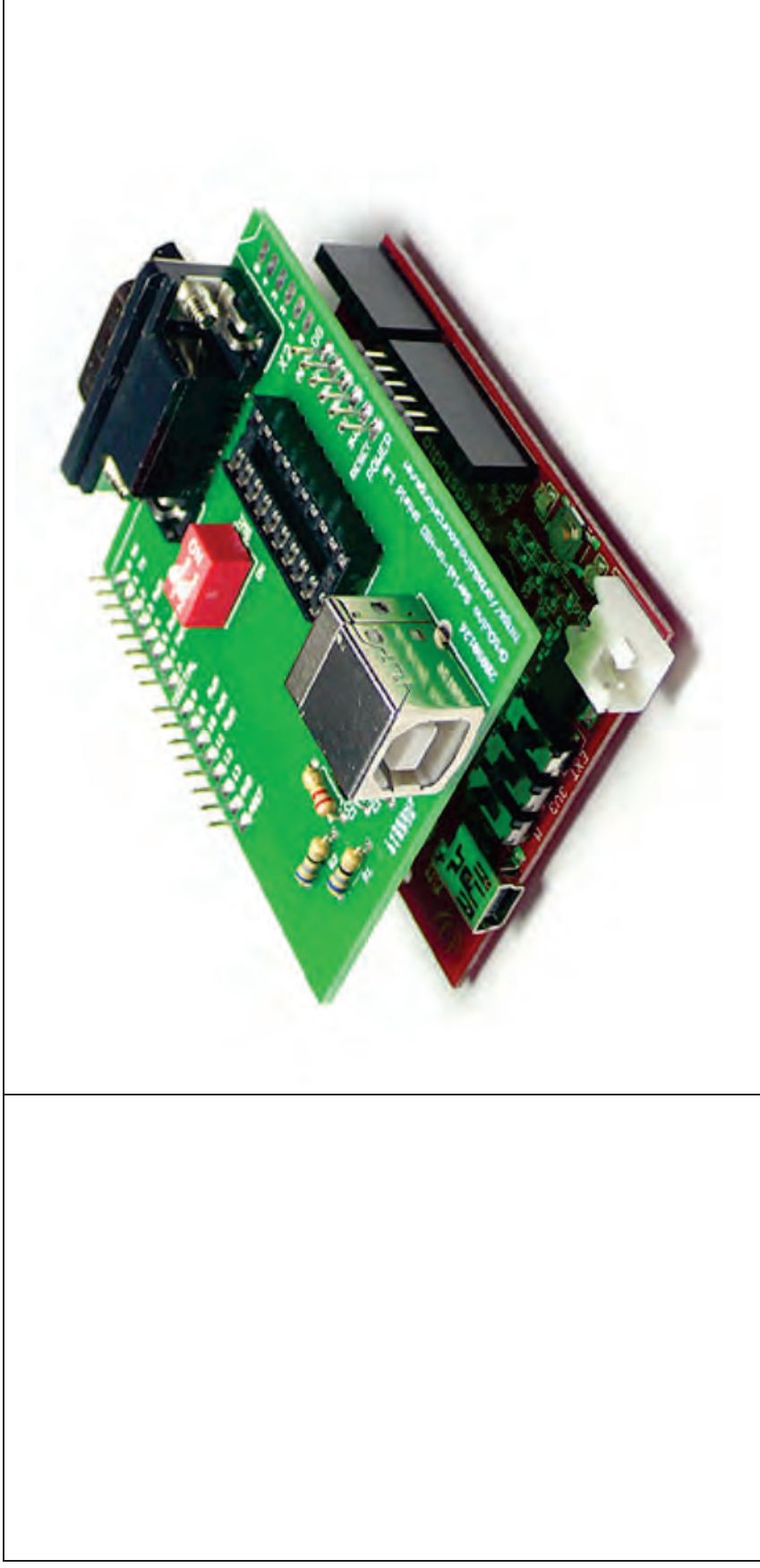
https://web.archive.org/web/20140729011717/http://www.seeedstudio.com/wiki/Seeeduino_Mega



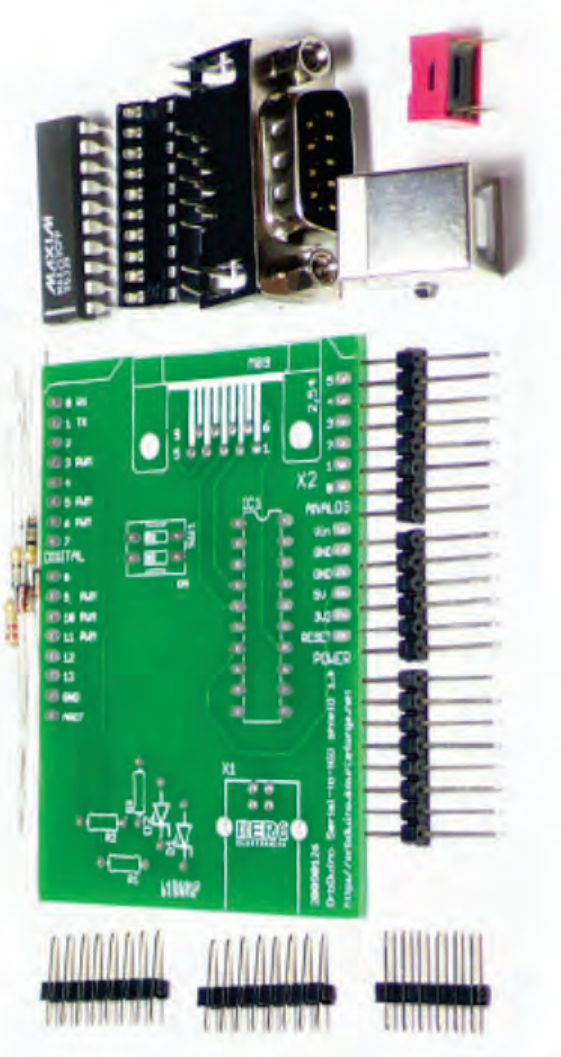
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	<p>https://web.archive.org/web/20141214031550/http://www.sseedstudio.com/wiki/Sseeduino_Stalker</p> <p>To the extent Plaintiff contends that Sseed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Sseed Board discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

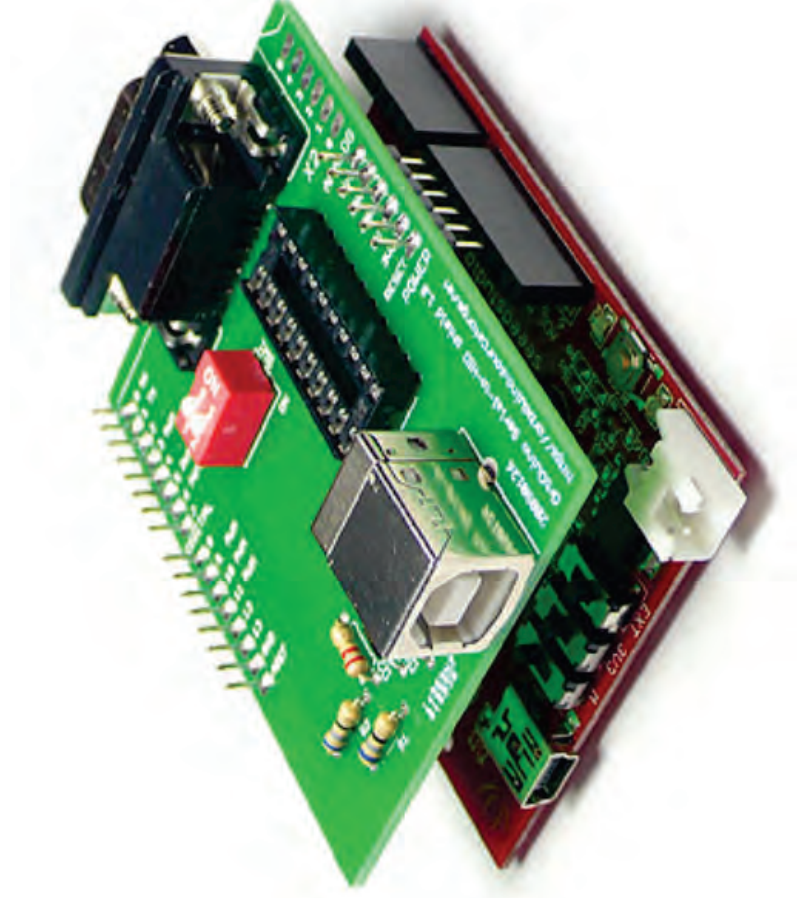
	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

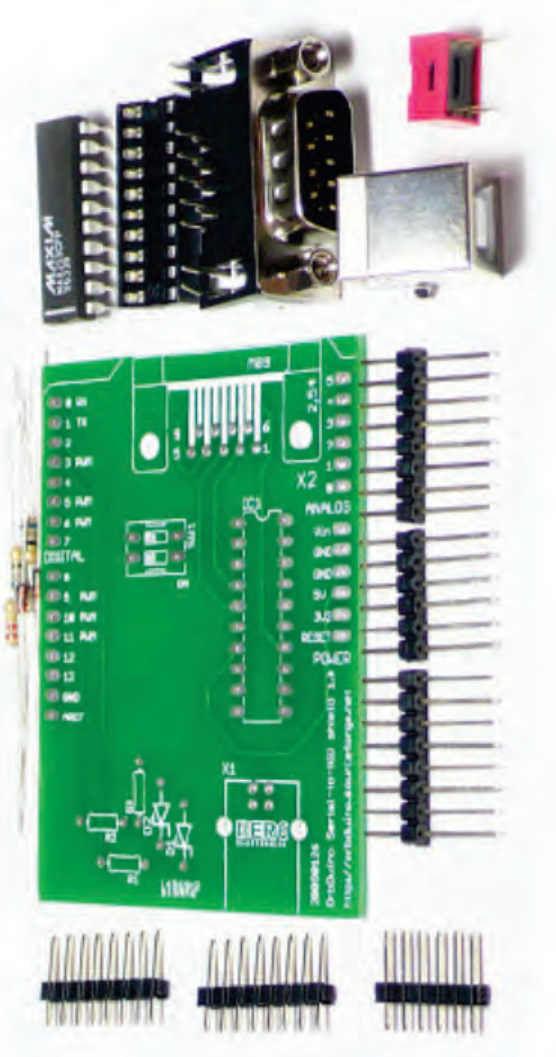
[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein

Sreed Board discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.

See, e.g.:



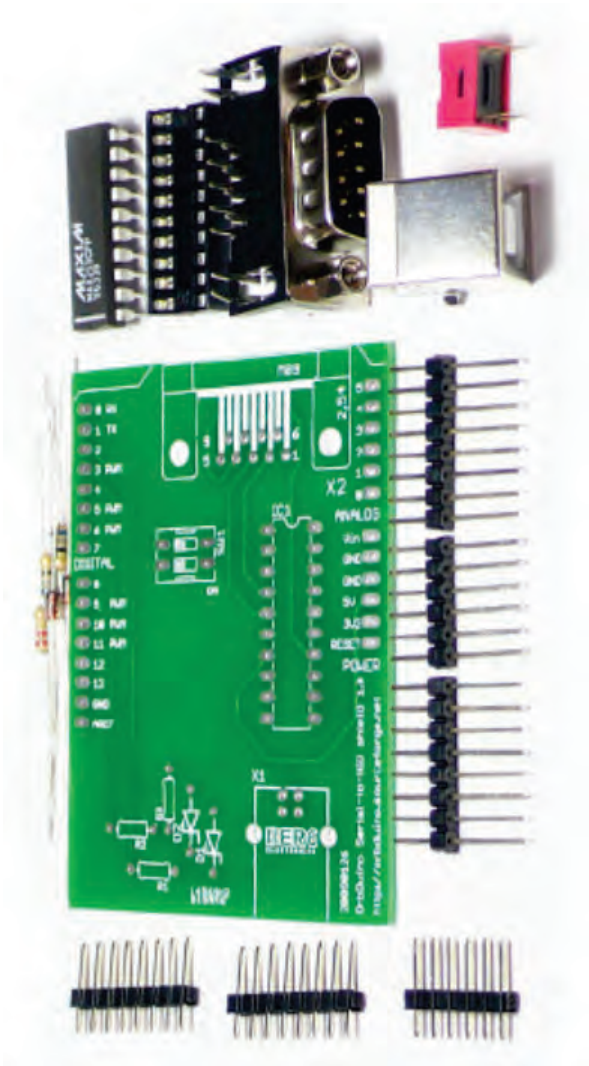
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Seeed Board discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, e.g.:</p>  <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p>
---	---

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

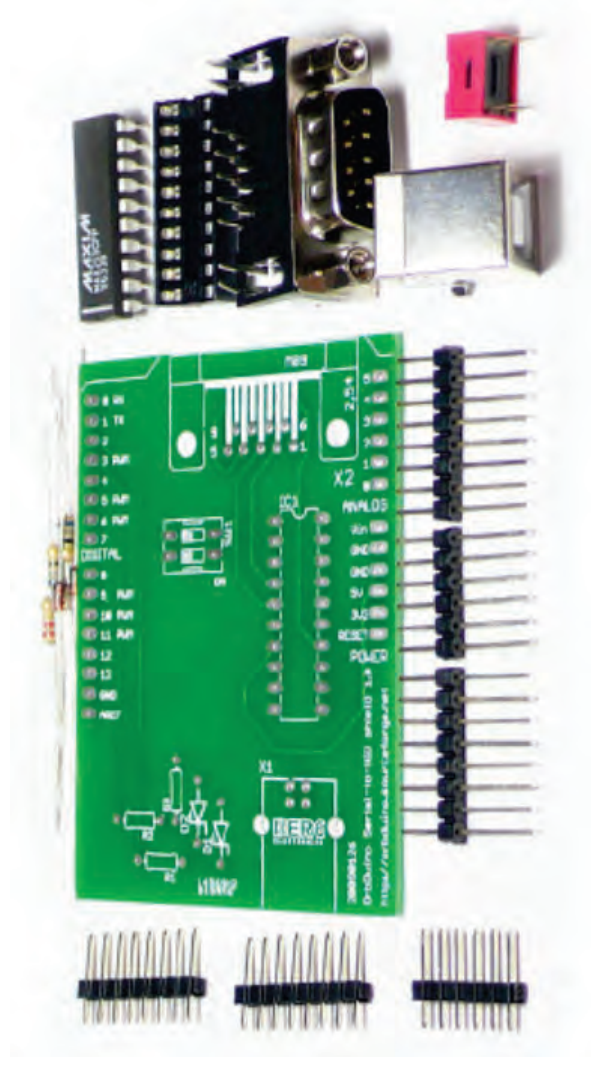
	<p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>  <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

	<p>general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	<div><h1>SOCKET CONNECTORS</h1><h2>Socket Connectors</h2><div>View Range</div><p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p></div>
[1.E] a plurality of metal pillars, each passing through the core substrate; and	Sreed Board discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

See, e.g.:



“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”

https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p>
--	--

For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.

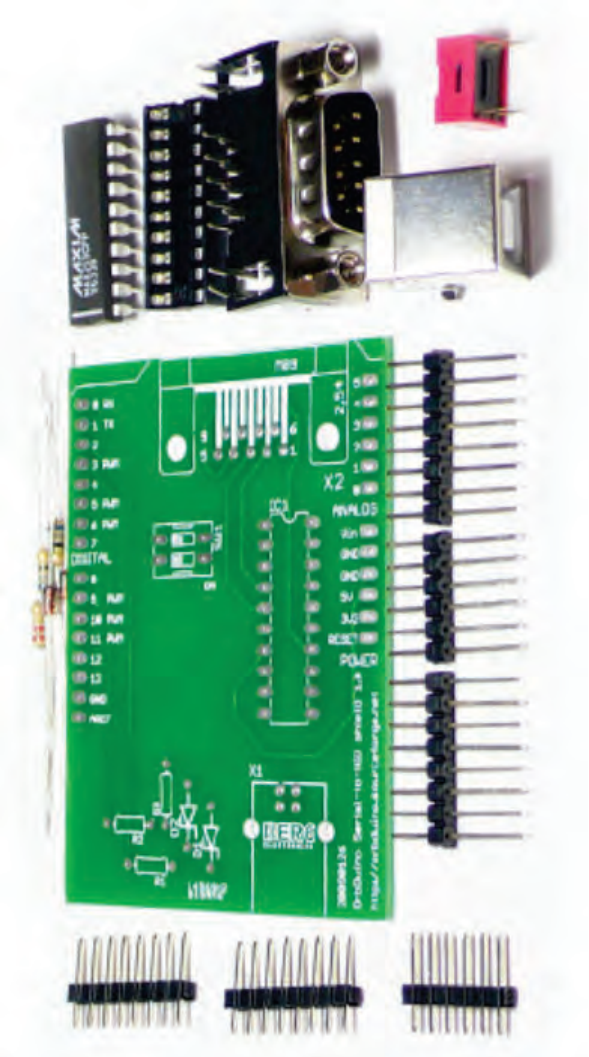


PIN CONNECTORS

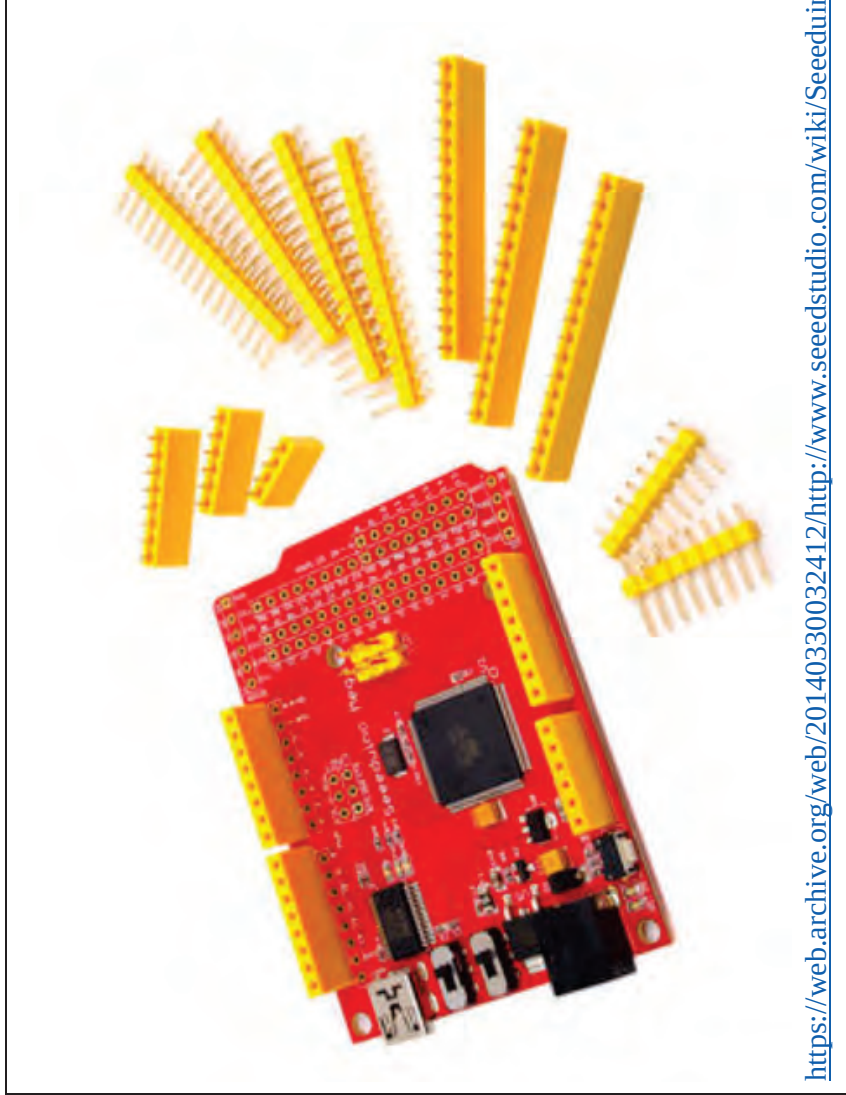
Pin Connectors

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal</p>	<p>Sseed Board discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

<p>pillar among the plurality of metal pillars;</p>	<p>See, e.g.:</p>  <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
---	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p>
--	--

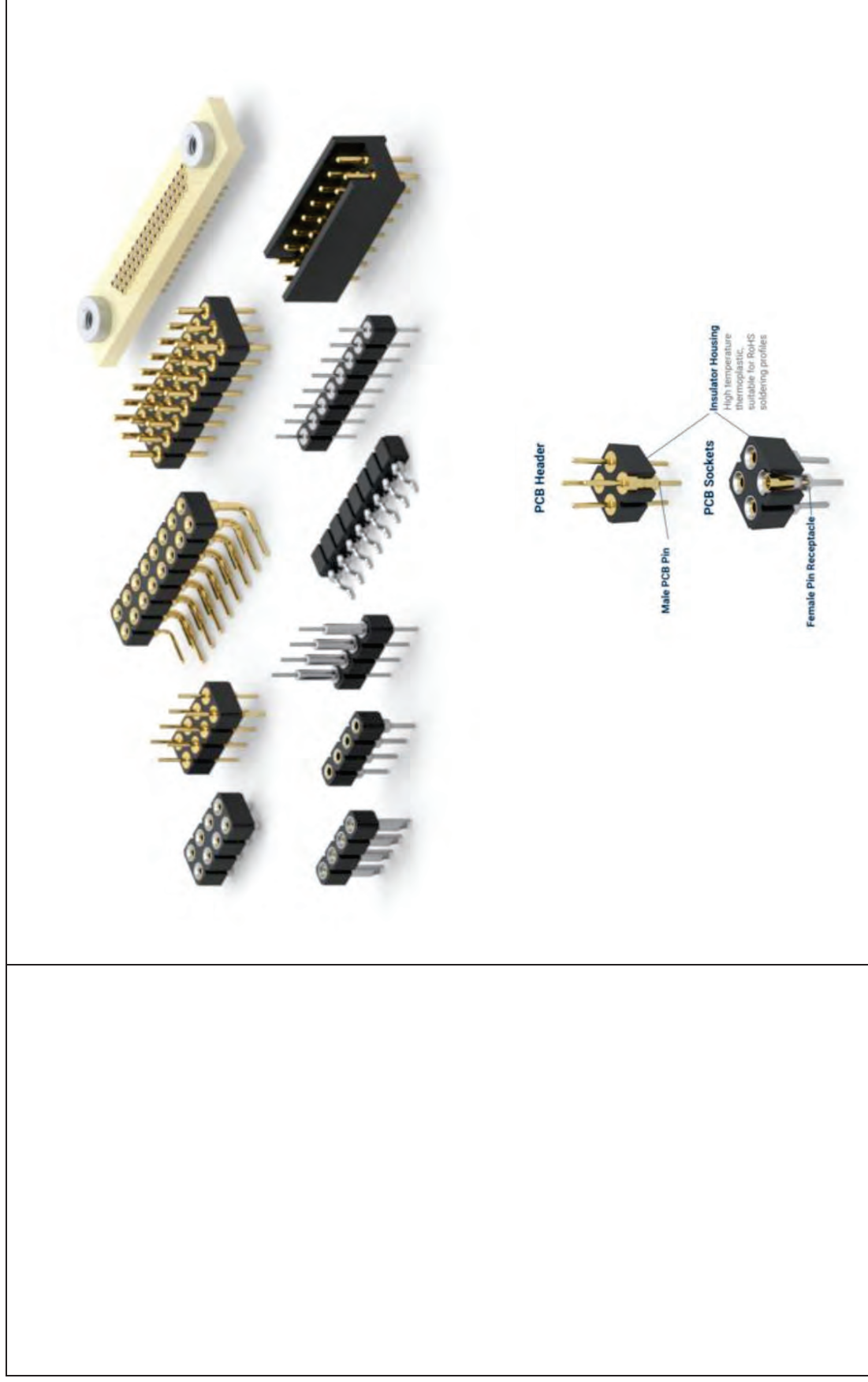
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Saeed Board

	<p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <p>PIN CONNECTORS</p> <p>Pin Connectors</p>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

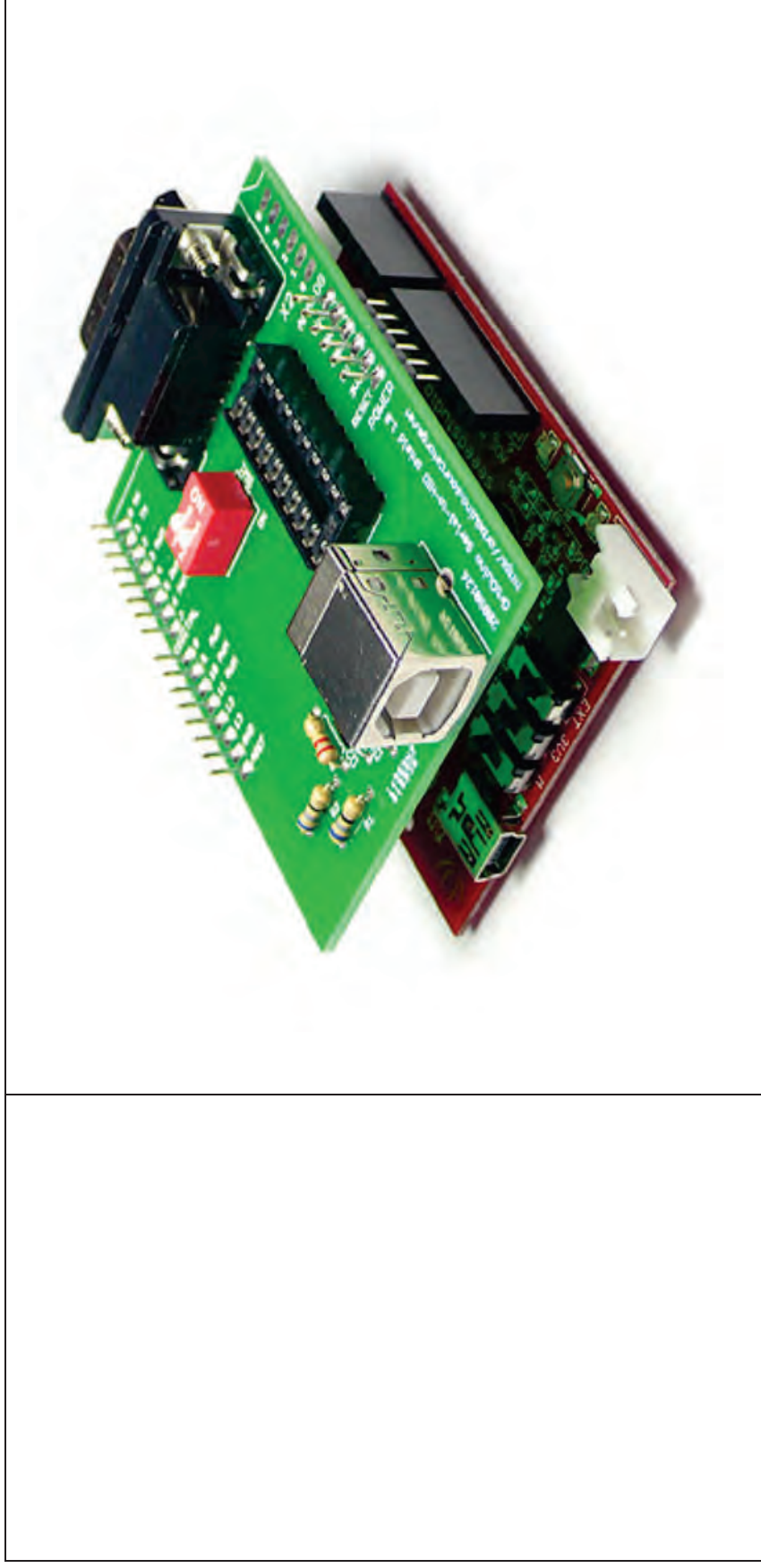
	<p>PCB CONNECTORS</p>  <p>https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html</p>
--	---



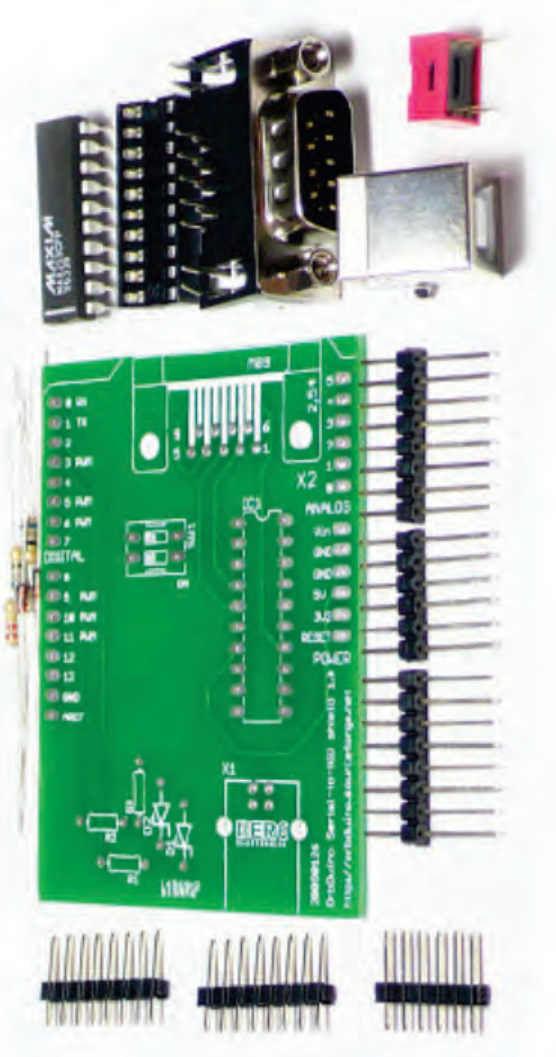
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Sseed Board discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Saeed Board

For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.

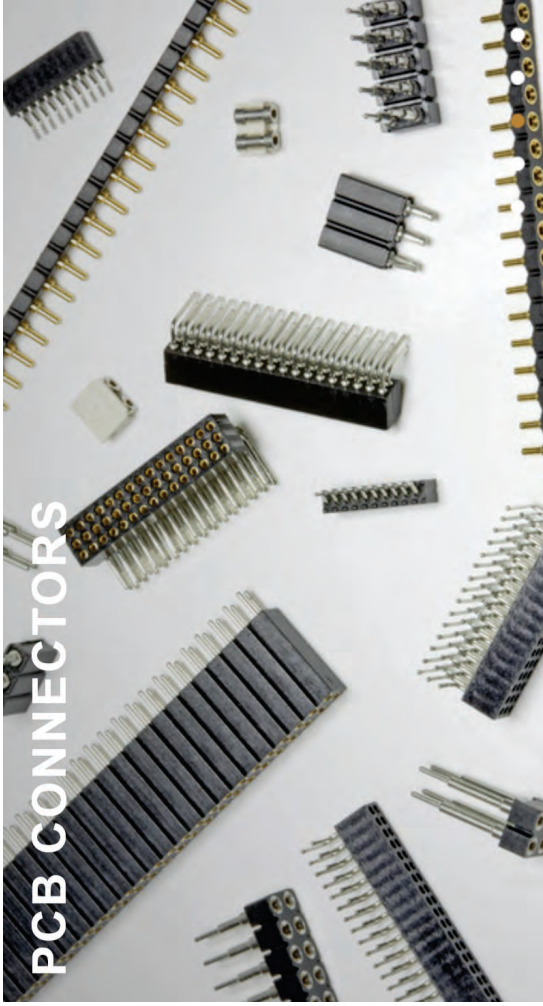


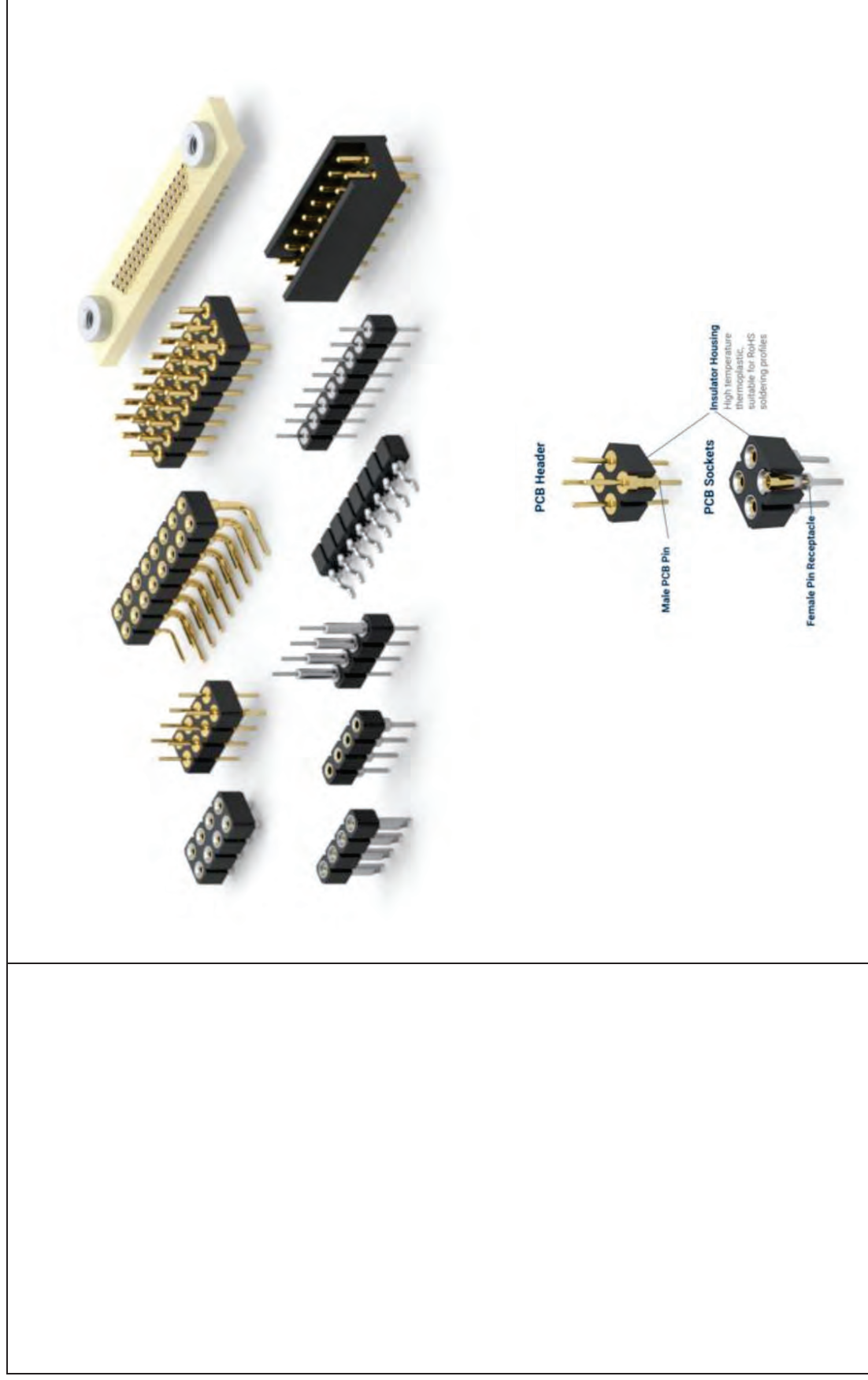
PIN CONNECTORS

Pin Connectors

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

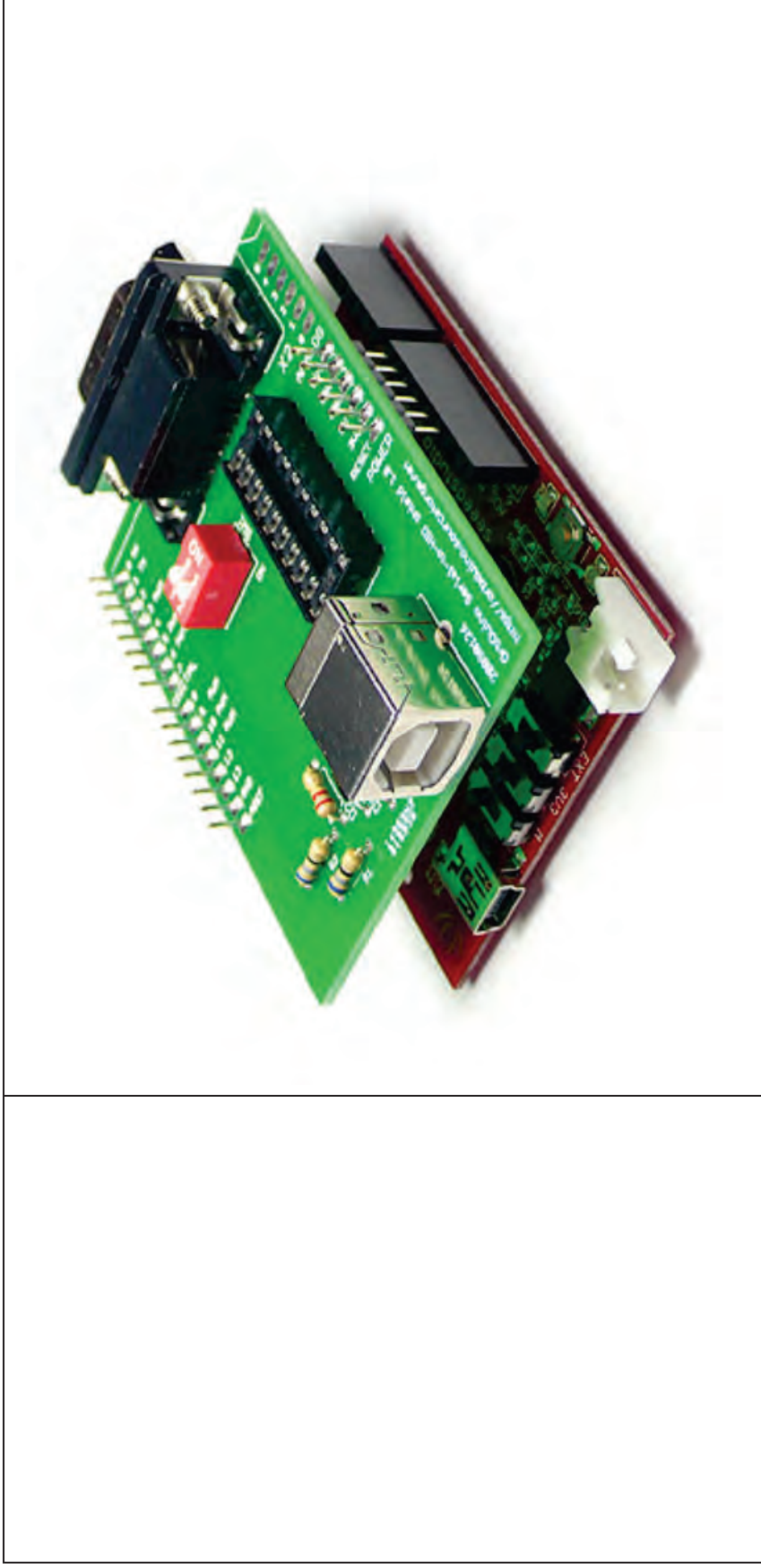
	<p>PCB CONNECTORS</p>  <p>https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html</p>
--	--



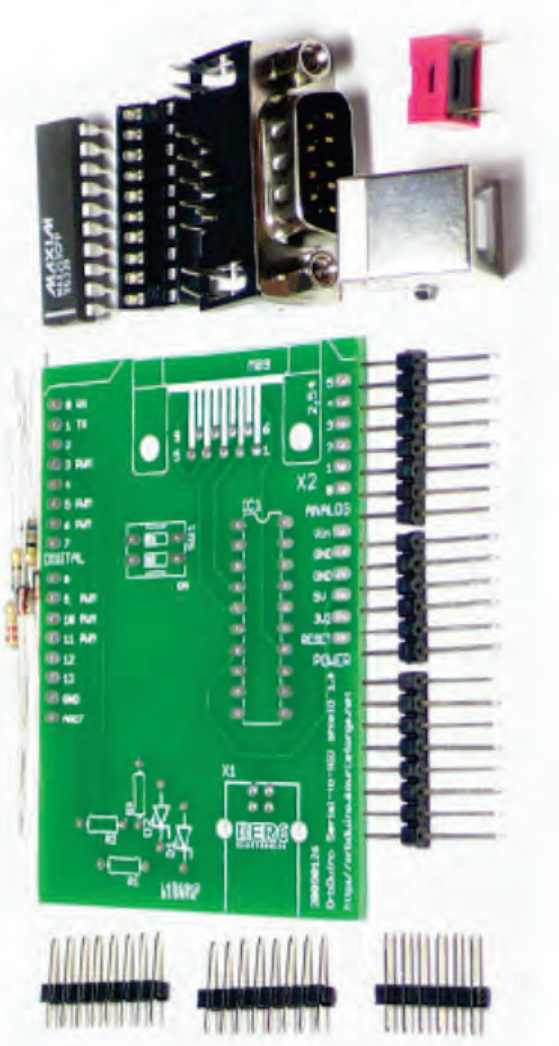
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Sreed Board discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	--

general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.

For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.

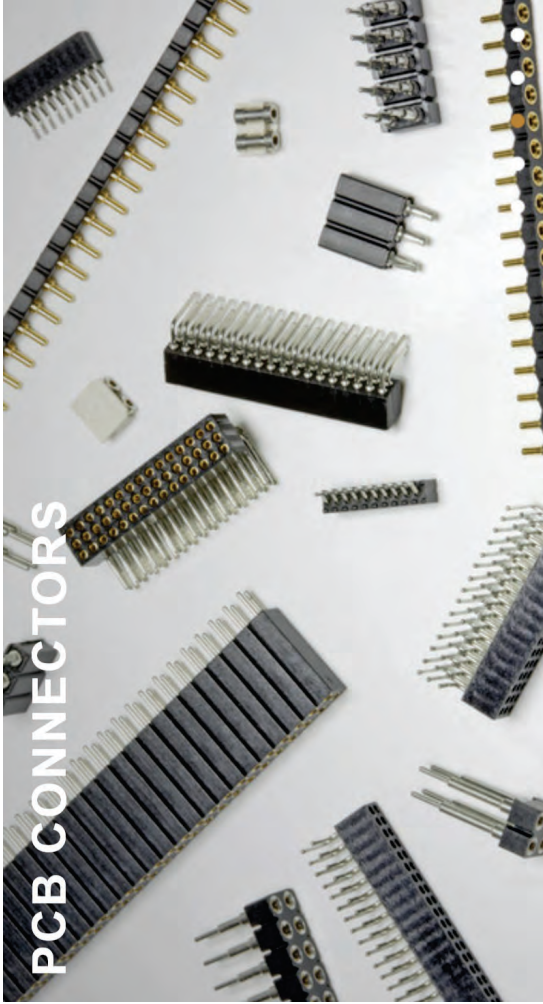


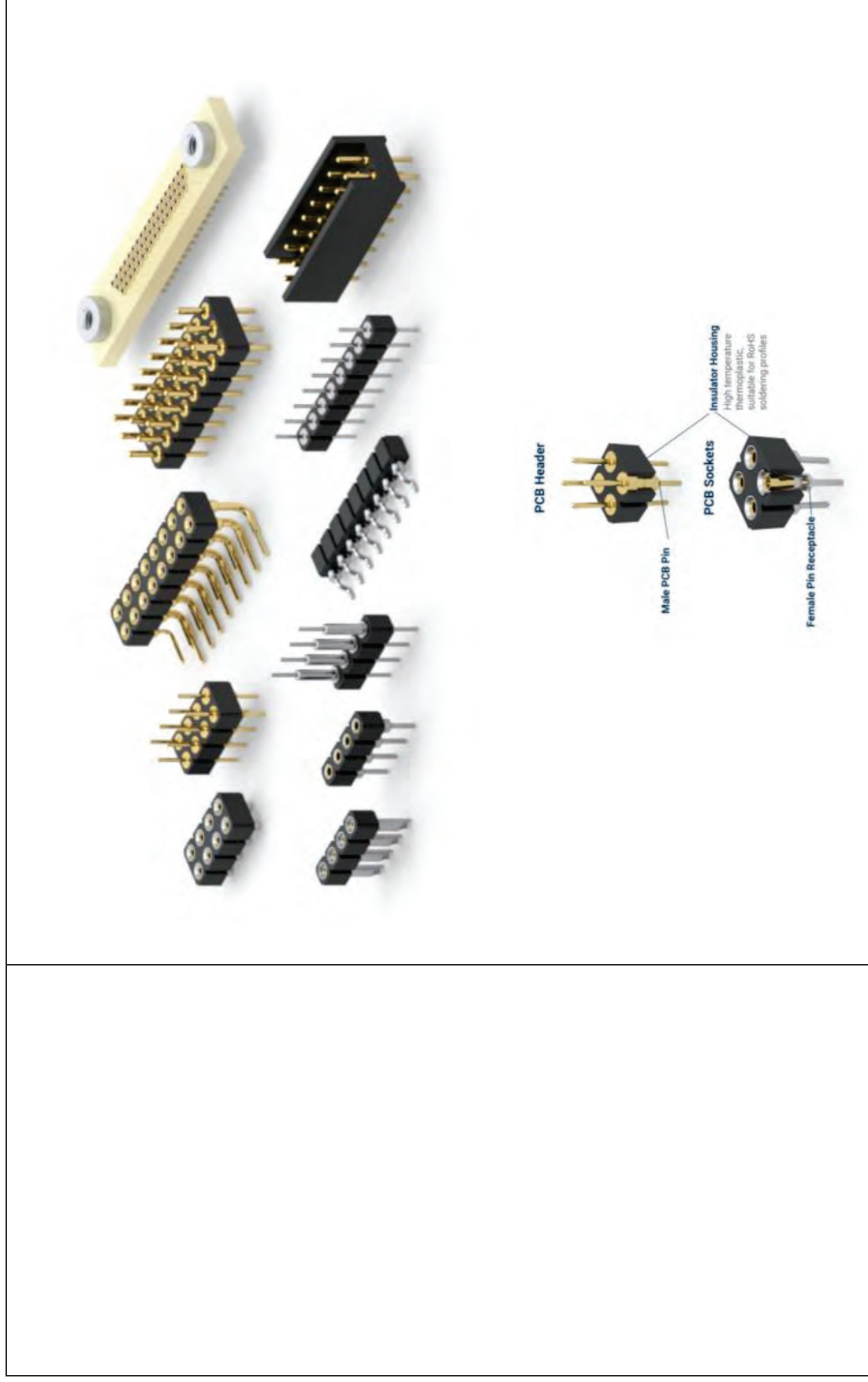
PIN CONNECTORS

Pin Connectors

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

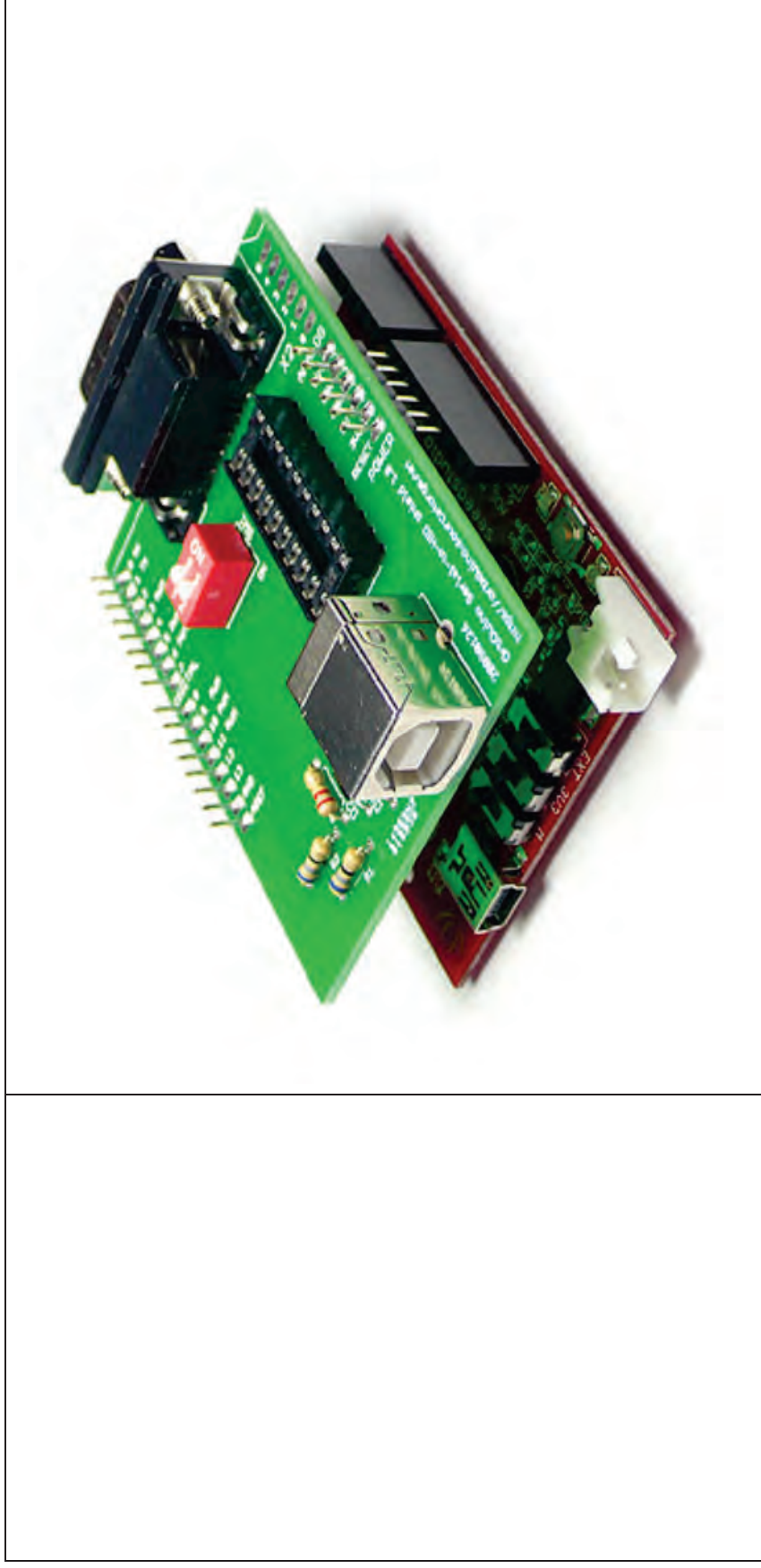
	<p>PCB CONNECTORS</p>  <p>https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html</p>
--	--



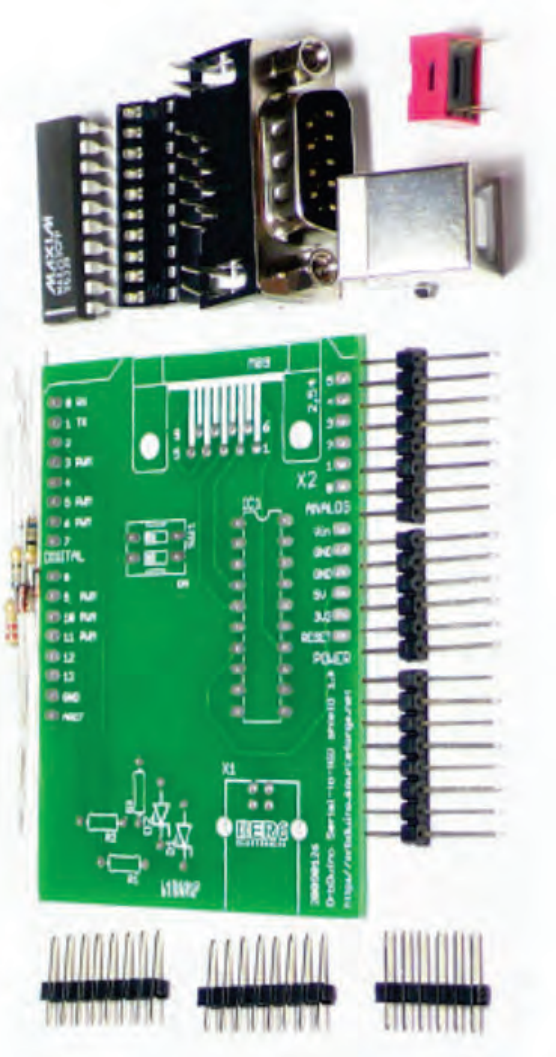
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Sreed Board discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Saeed Board

For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.

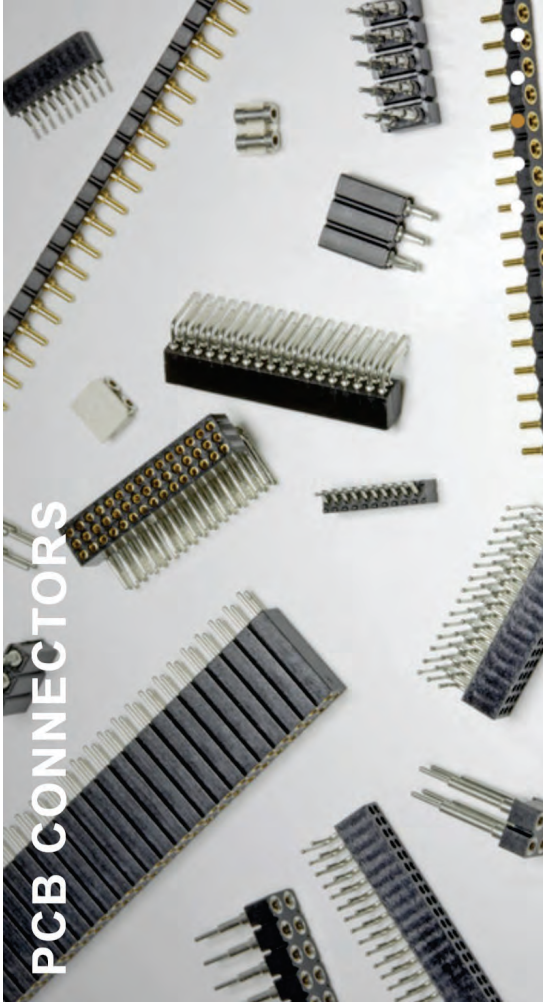


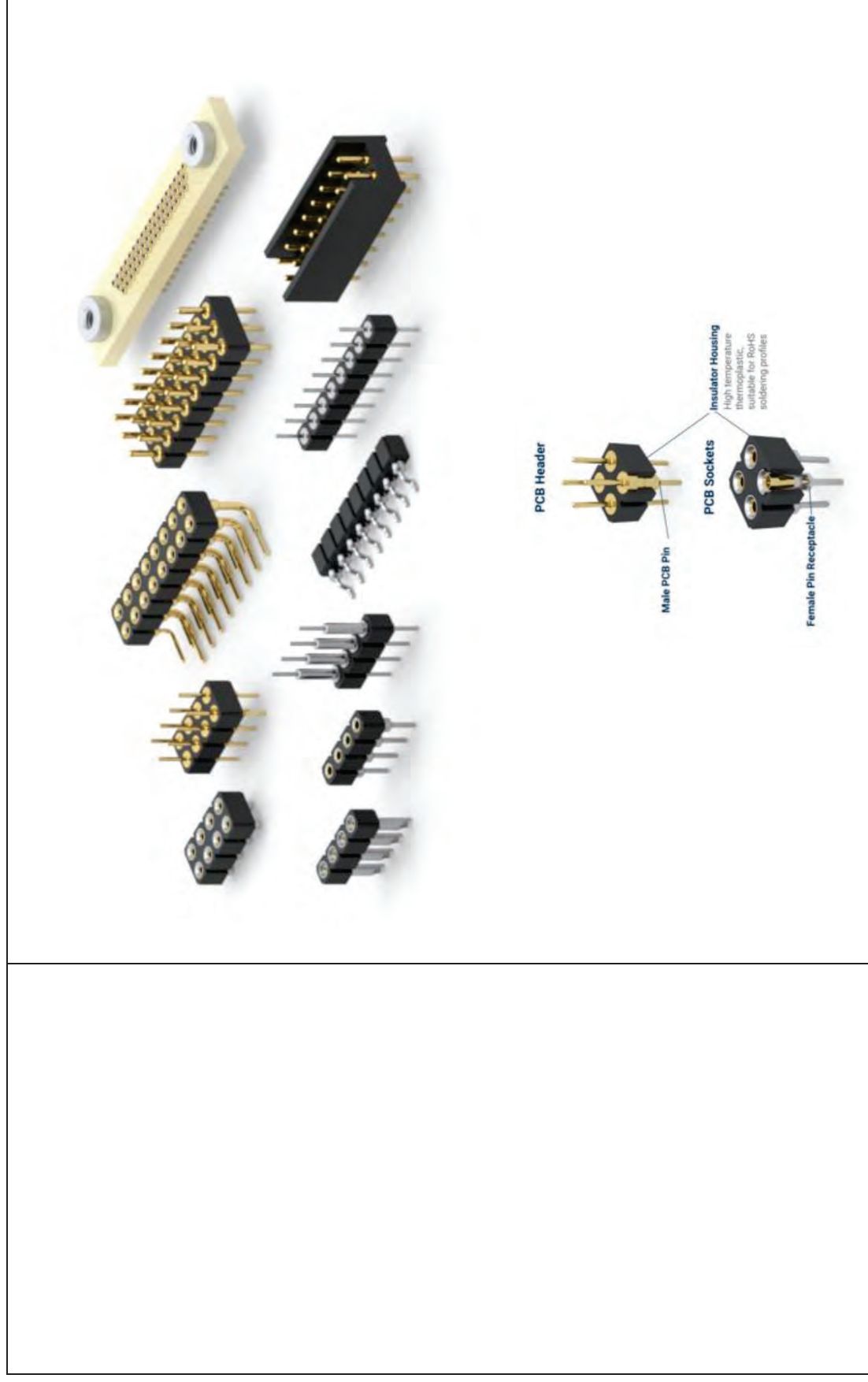
PIN CONNECTORS

Pin Connectors

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

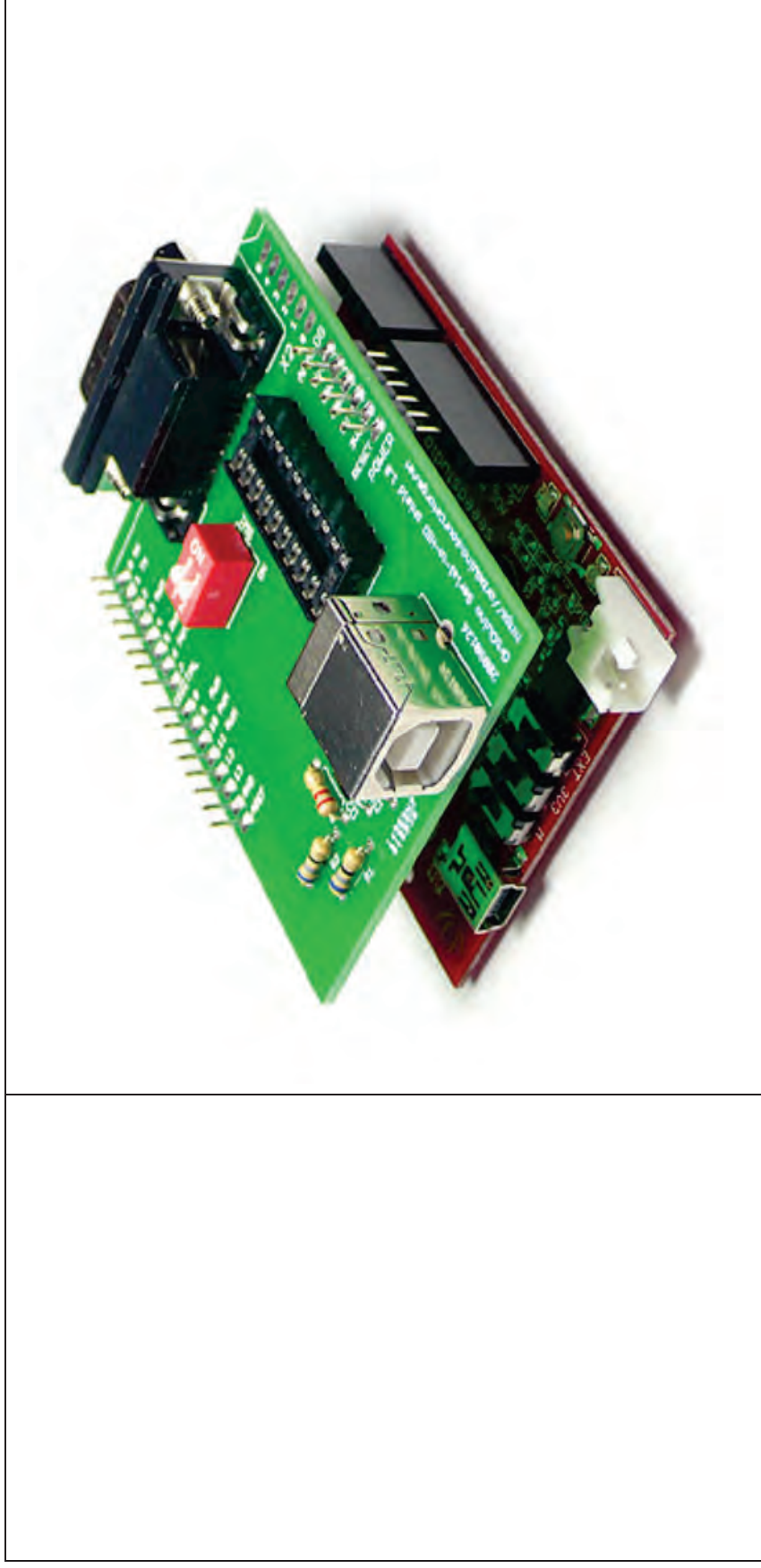
	<p>PCB CONNECTORS</p>  <p>https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html</p>
--	--



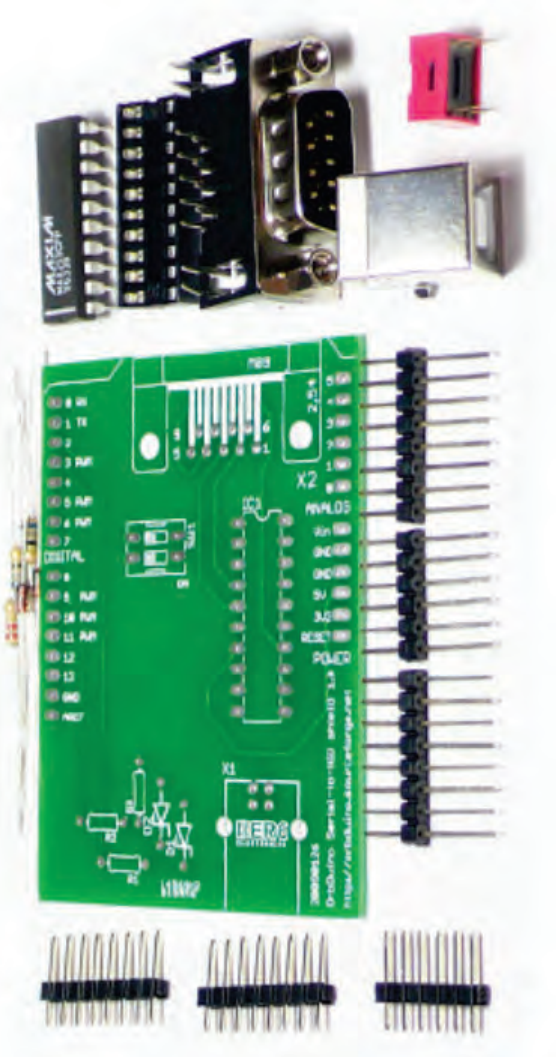
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Sseed Board discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

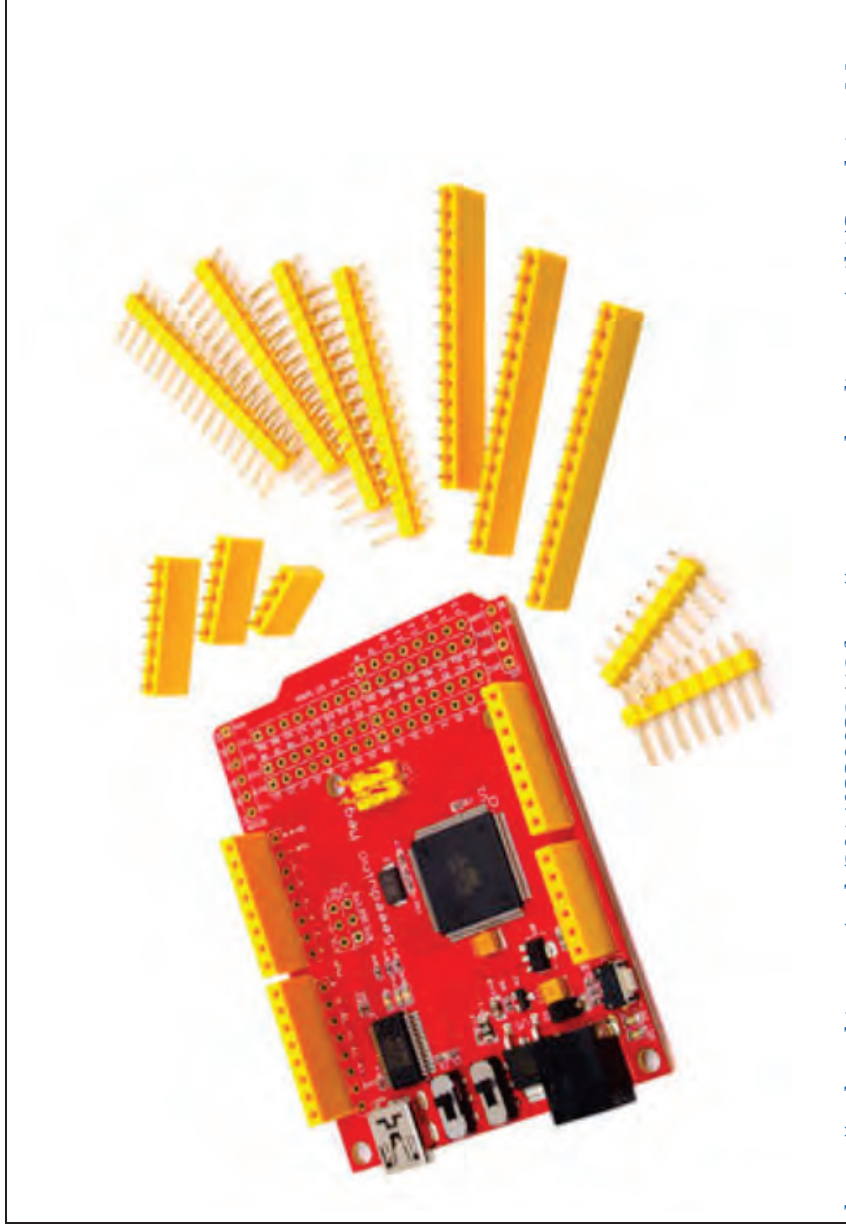
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

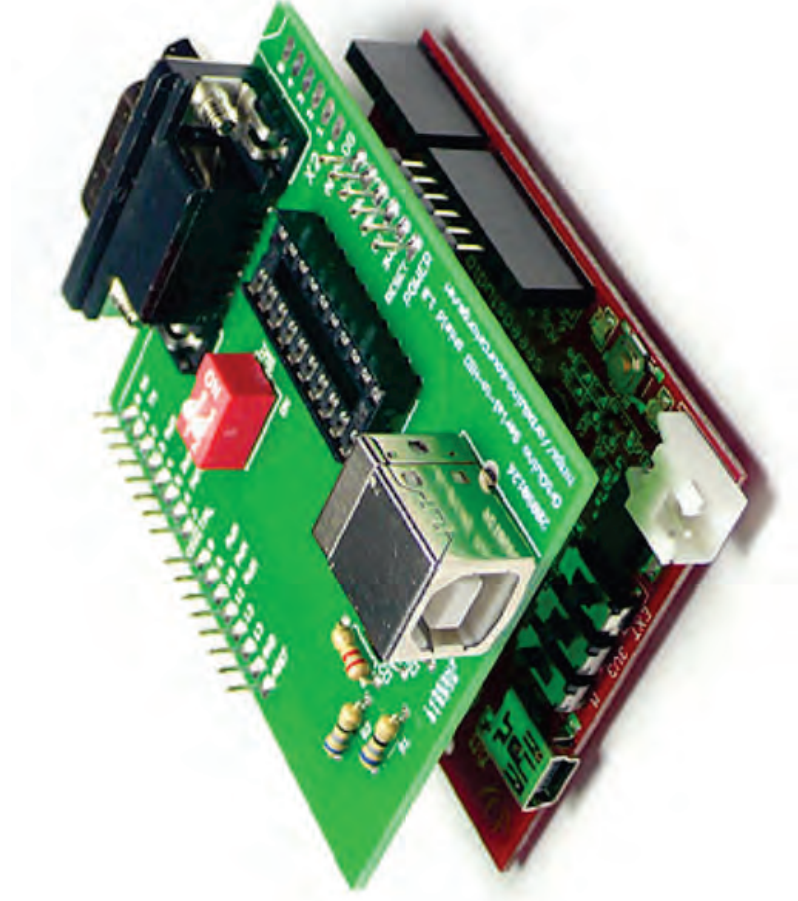
	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein

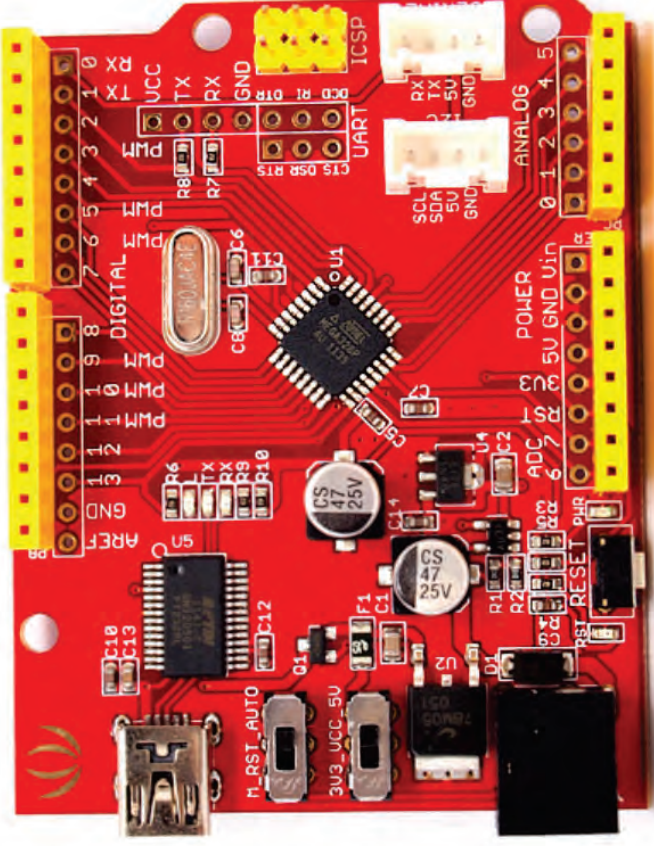
Sreed Board discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate.

See, e.g.:



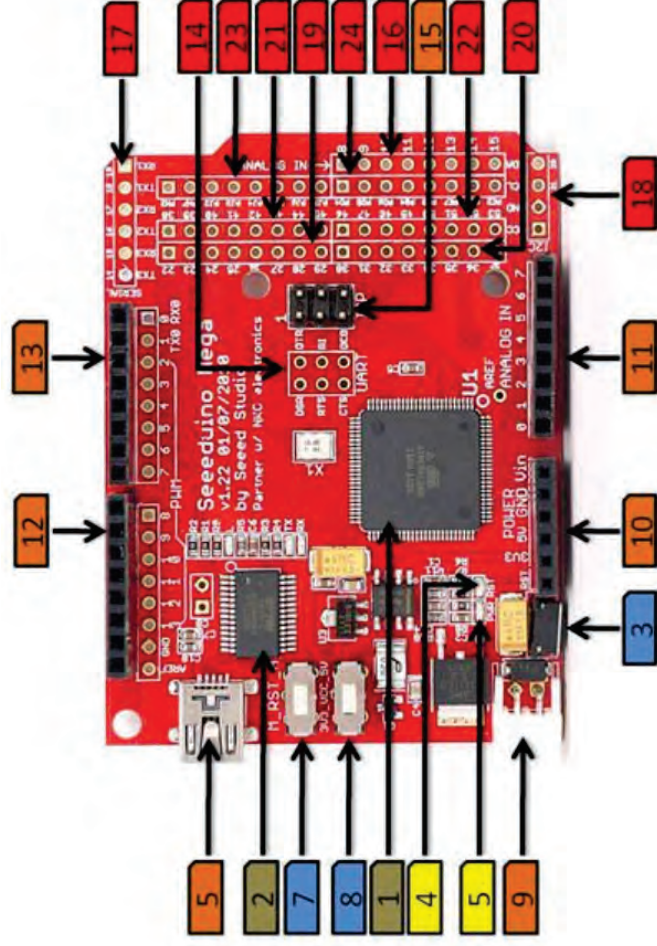
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	<p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	---

	 <p>“The Seeeduino v3 is a microcontroller board based on the ATmega328, and it’s an Arduino compatible board. It has a FTDI USB-to-serial driver chip which can be regarded as a bridge, let your computer can communicate with the board. It has 14 digit pins (which include 6 PWM pins and UART port) and 8 analog pins, a 16 MHz ceramic resonator, a USB connection, a reset button, an ICSP header and a DC power jack. It has two toggle switches, one for input voltage change of ATmega328, the other is enable/disable pin of DTR, which you can use FTDI function alone without the influence of ATmega328. It also has two white Grove connectors, and make it convenient for using Grove products with the board.”</p>
--	--

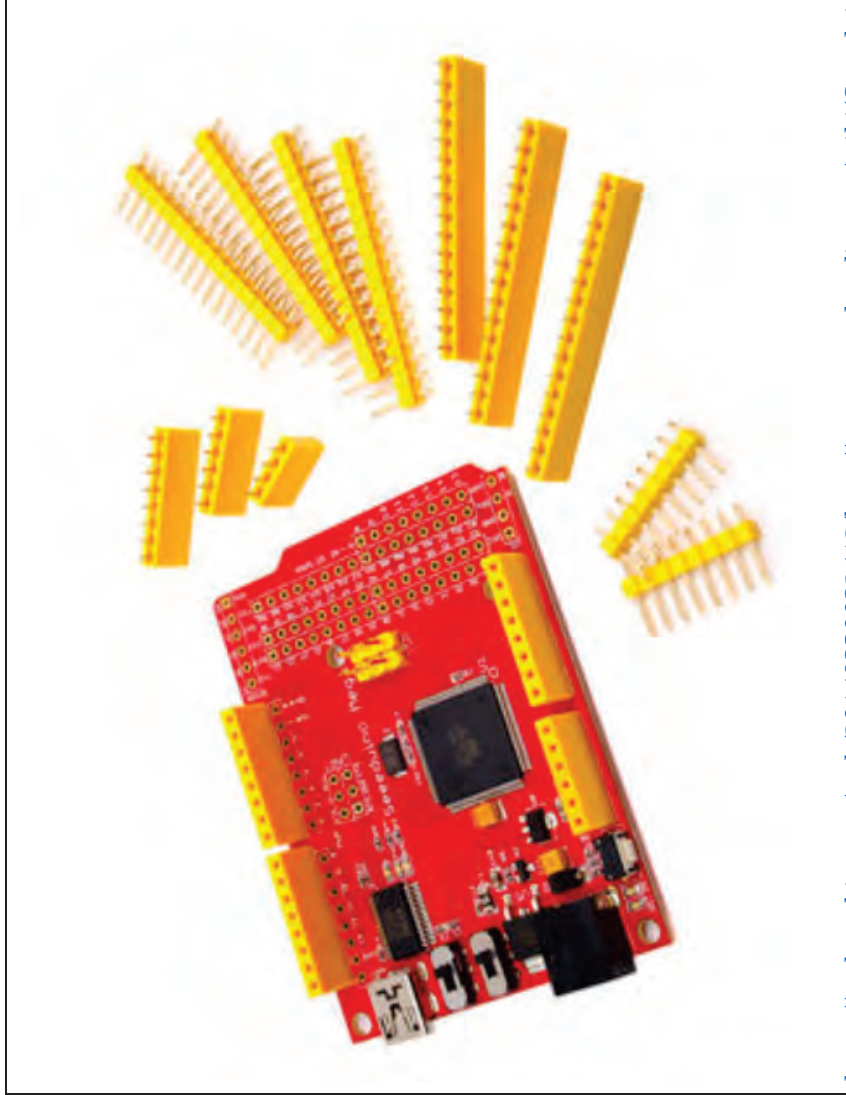
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeeduino Board

https://web.archive.org/web/20141214140820/http://www.seeedstudio.com/wiki/Seeeduino_v3.0

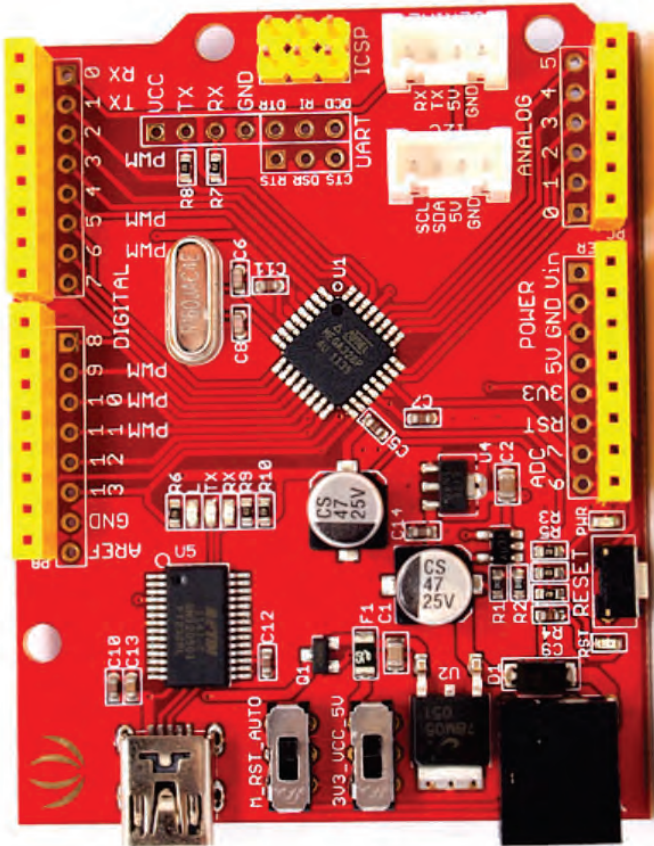


https://web.archive.org/web/20140729011717/http://www.seeedstudio.com/wiki/Seeeduino_Mega

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

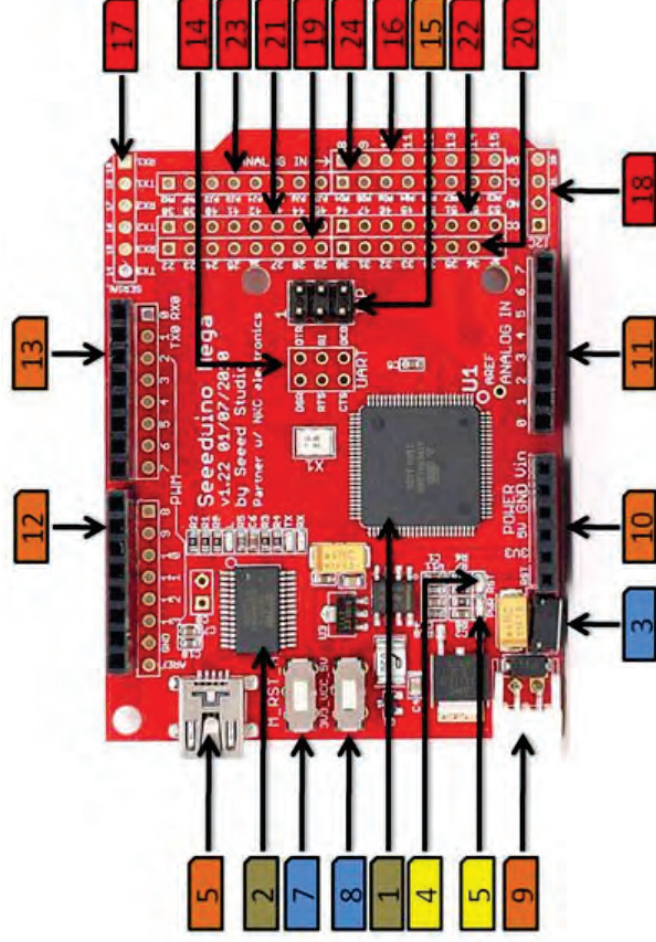
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Seeed Board discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p>See, e.g.:</p>  <p>“The Seeeduino v3 is a microcontroller board based on the ATmega328, and it’s an Arduino compatible board. It has a FTDI USB-to-serial driver chip which can be regarded as a bridge, let your</p>
---	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

computer can communicate with the board. It has 14 digit pins (which include 6 PWM pins and UART port) and 8 analog pins, a 16 MHz ceramic resonator, a USB connection, a reset button, an ICSP header and a DC power jack. It has two toggle switches, one for input voltage change of ATmega328, the other is enable/disable pin of DTR, which you can use FTDI function alone without the influence of ATmega328. It also has two white Grove connectors, and make it convenient for using Grove products with the board.”

https://web.archive.org/web/20141214140820/http://www.seeedstudio.com/wiki/Seeeduino_v3.0



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

https://web.archive.org/web/20140729011717/http://www.seeedstudio.com/wiki/Seeeduino_Mega



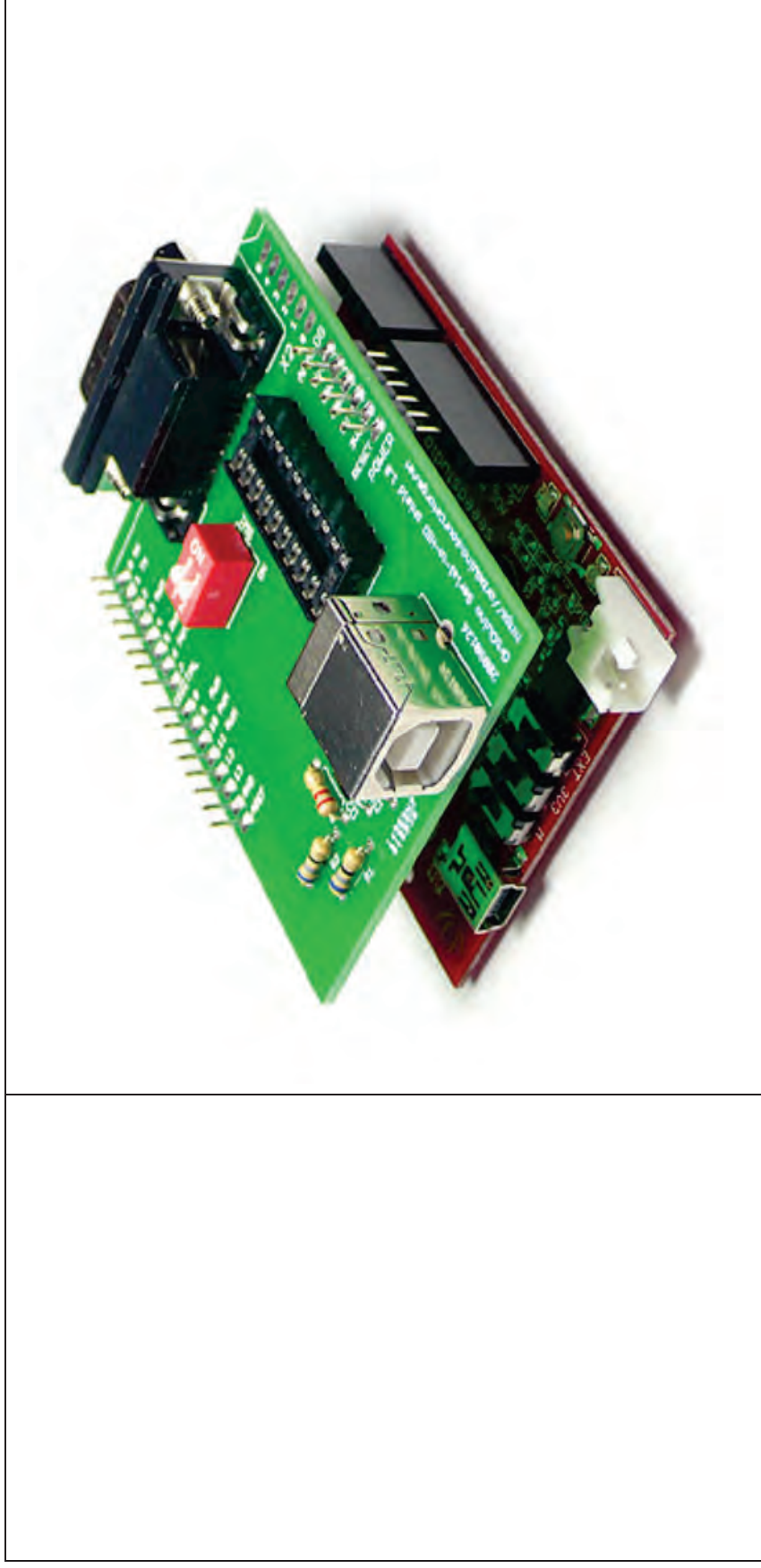
https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega

To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the

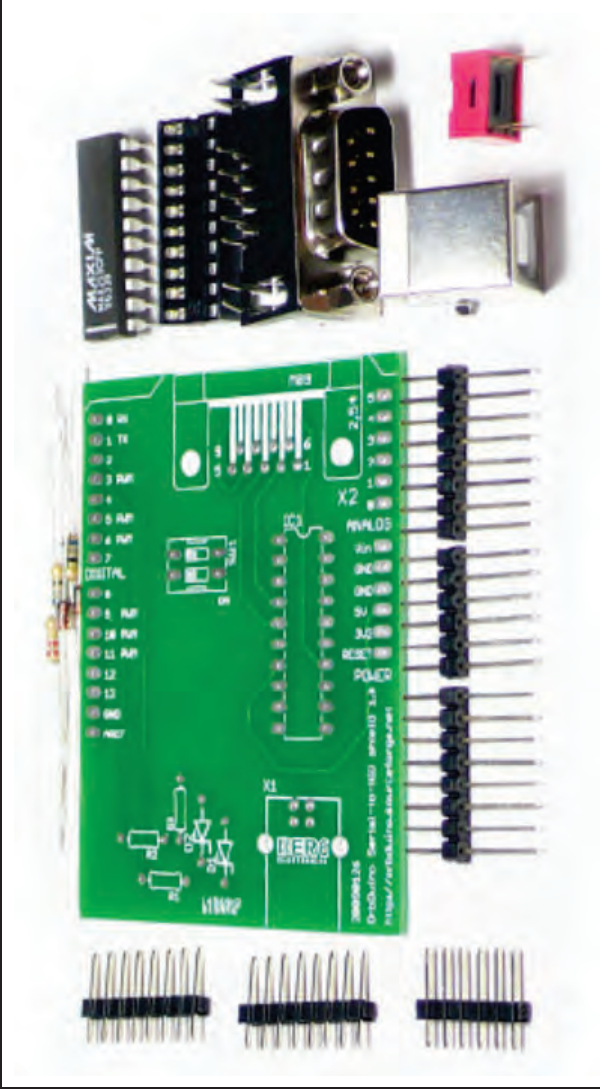
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.	Sreed Board discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip. <i>See, e.g.:</i>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.

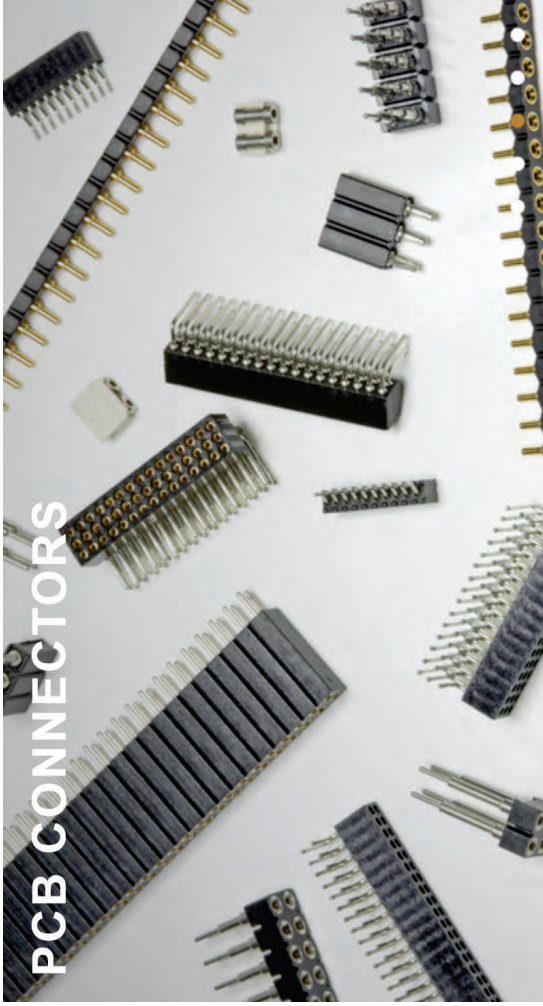


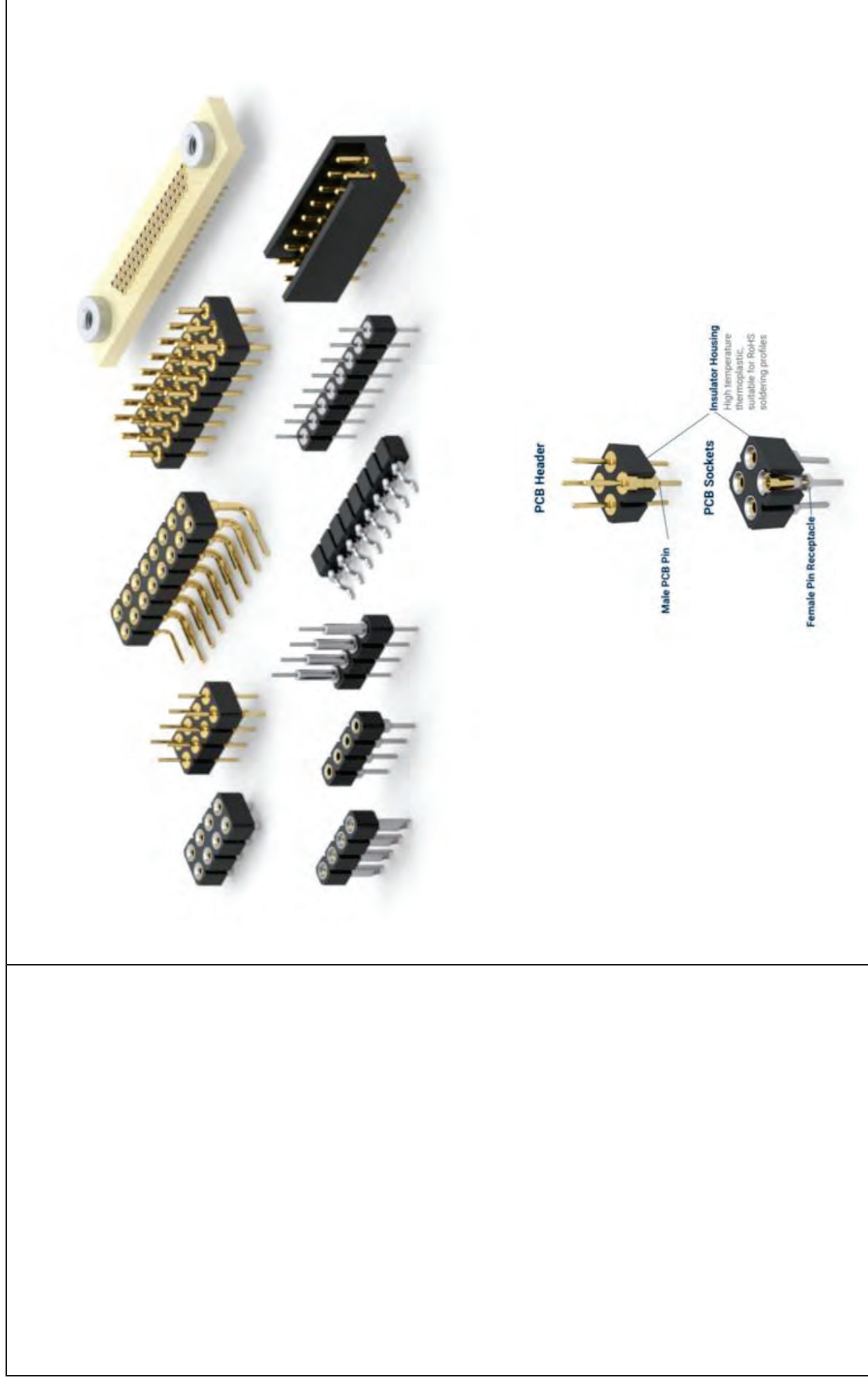
PIN CONNECTORS

Pin Connectors

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	<p>PCB CONNECTORS</p>  <p>https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html</p>
--	--

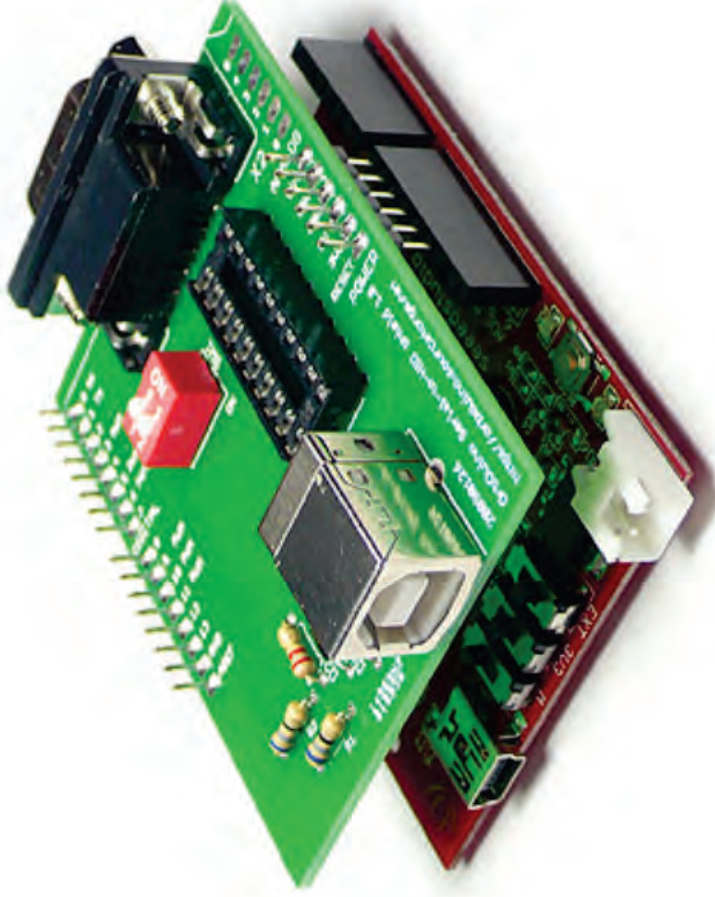


Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

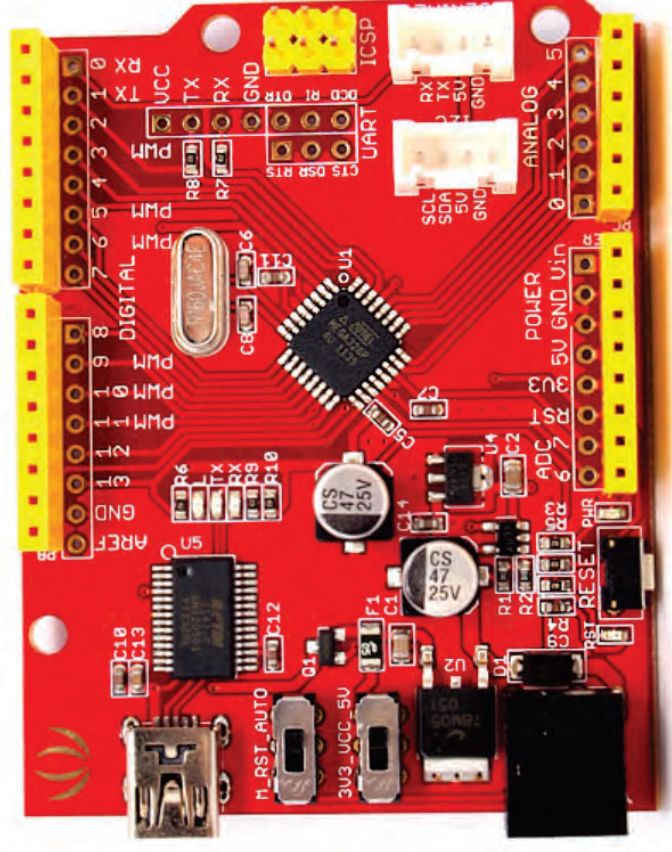
Claim 2

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>Sseed Board discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134



“The Seeeduino v3 is a microcontroller board based on the ATmega328, and it’s an Arduino compatible board. It has a FTDI USB-to-serial driver chip which can be regarded as a bridge, let your computer can communicate with the board. It has 14 digit pins (which include 6 PWM pins and UART port) and 8 analog pins, a 16 MHz ceramic resonator, a USB connection, a reset button, an

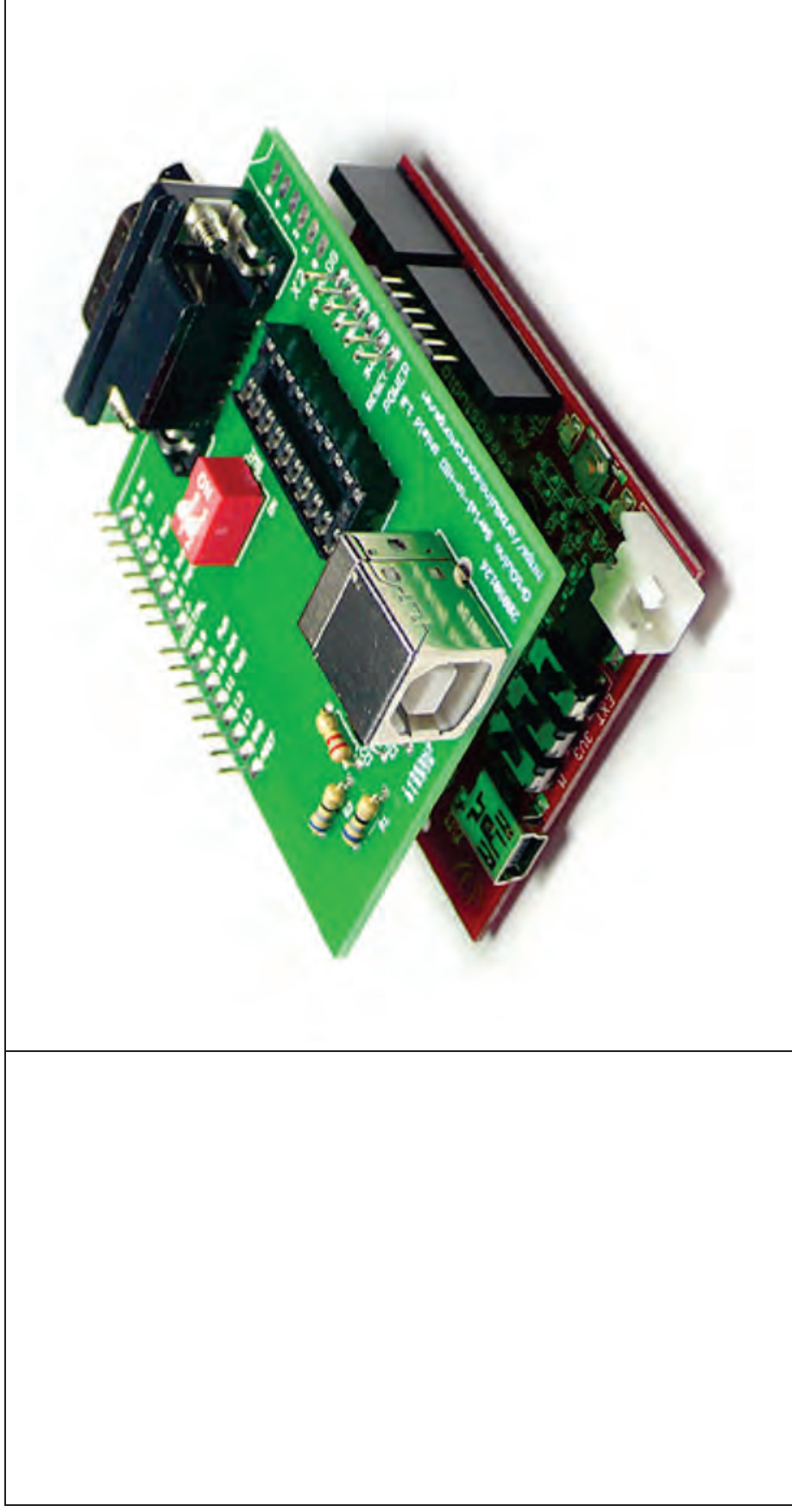
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	<p>ICSP header and a DC power jack. It has two toggle switches, one for input voltage change of ATmega328, the other is enable/disable pin of DTR, which you can use FTDI function alone without the influence of ATmega328. It also has two white Grove connectors, and make it convenient for using Grove products with the board.”</p> <p>https://web.archive.org/web/20141214140820/http://www.seeedstudio.com/wiki/Seeeduino_v3.0</p> <p>To the extent Plaintiff contends that Sseed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

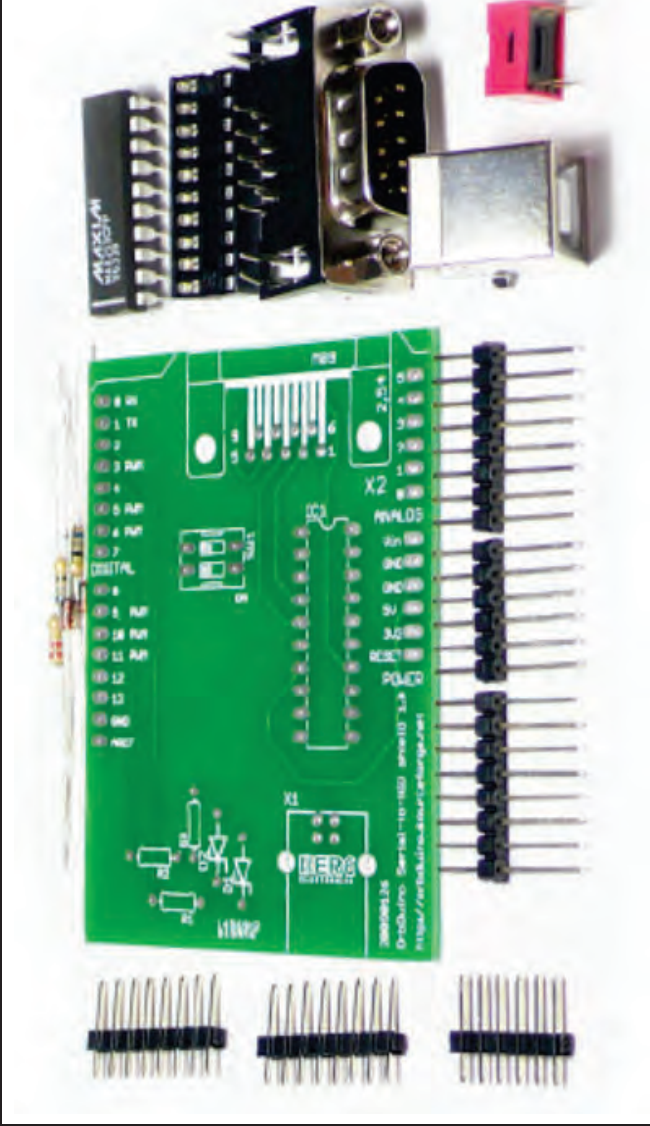
Claim 3

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>Sseed Board discloses, either expressly or inherently, a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p> <p>To the extent Plaintiff contends that Sseed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	--

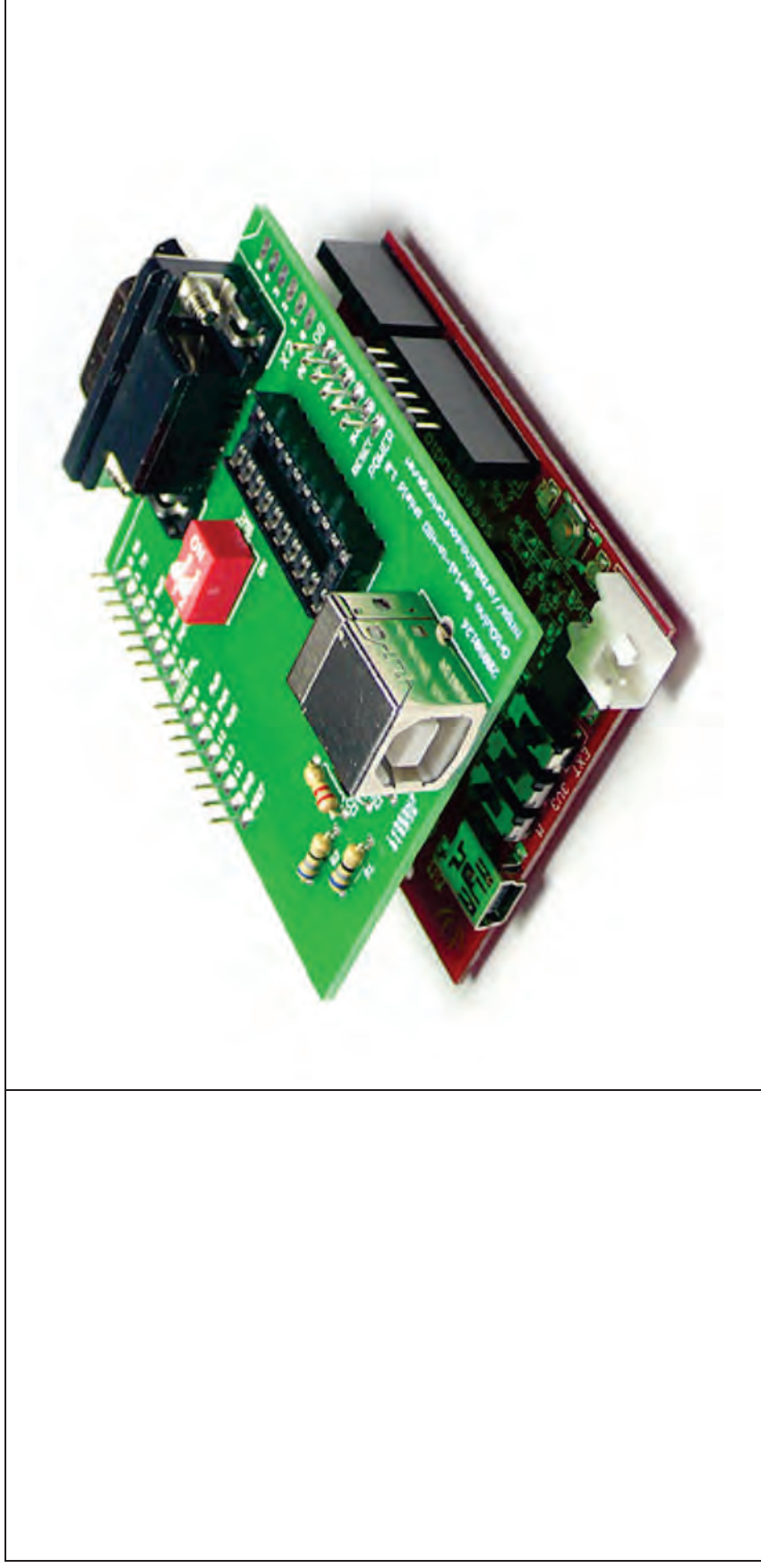
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seseed Board

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

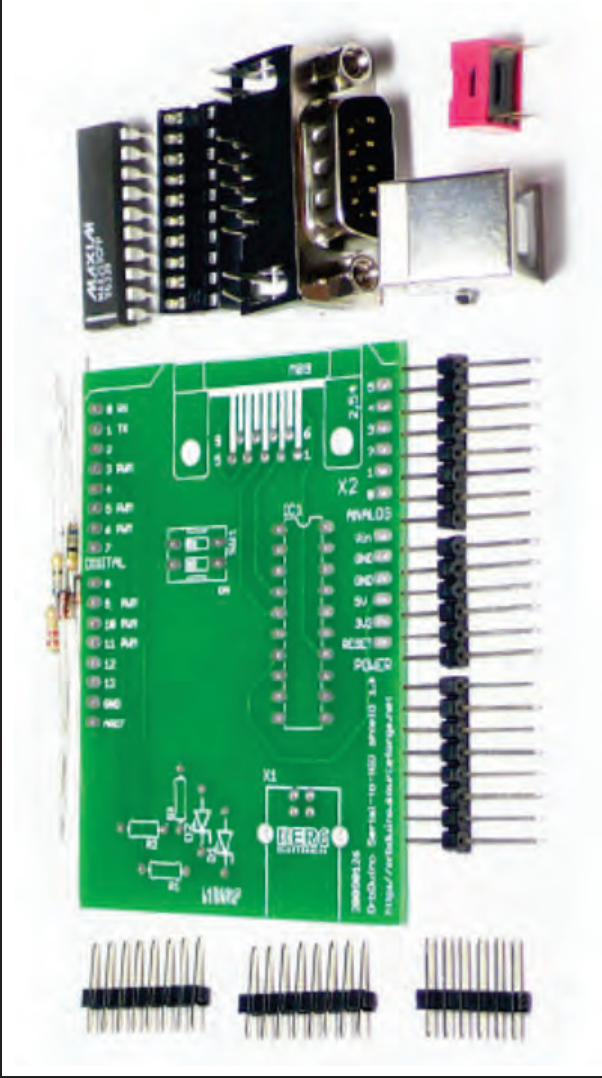
Claim 4

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	Seeed Board discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate. <i>See, e.g.:</i>

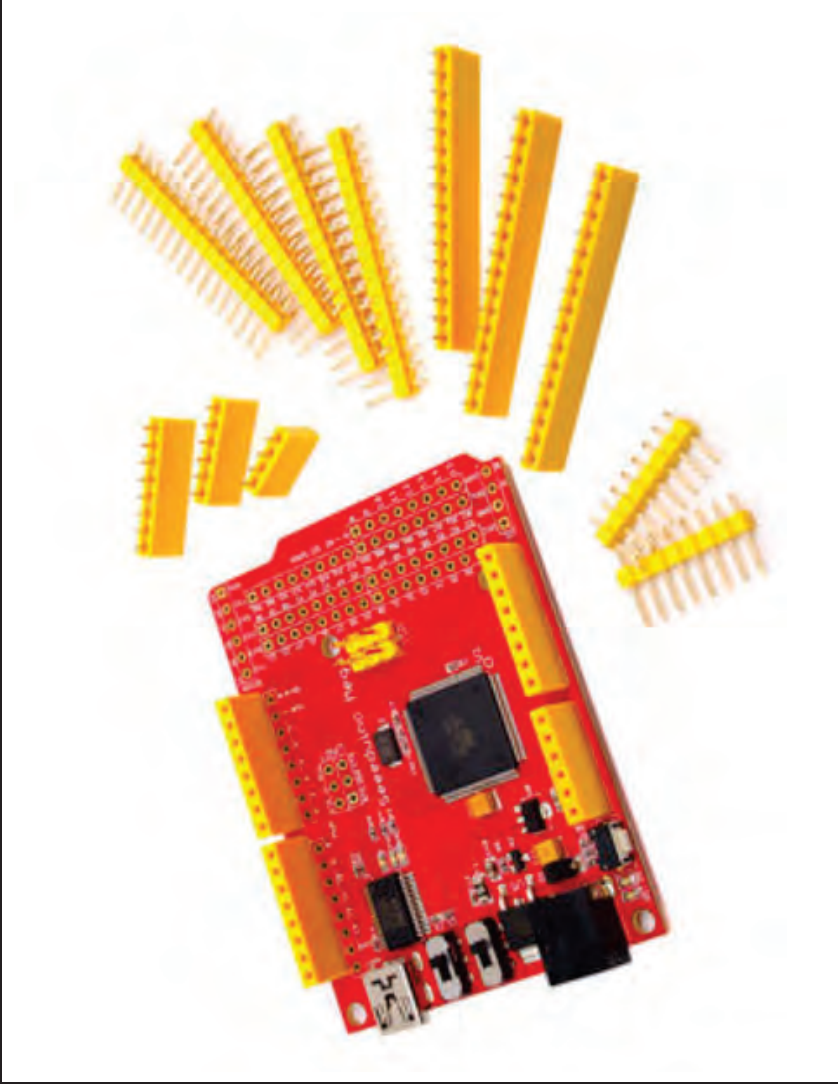
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

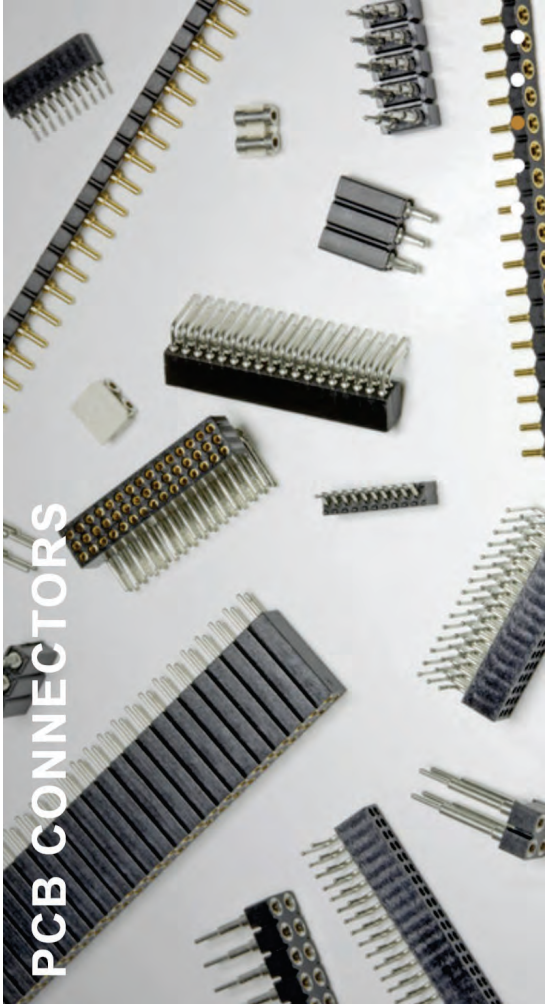
	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p>
--	--

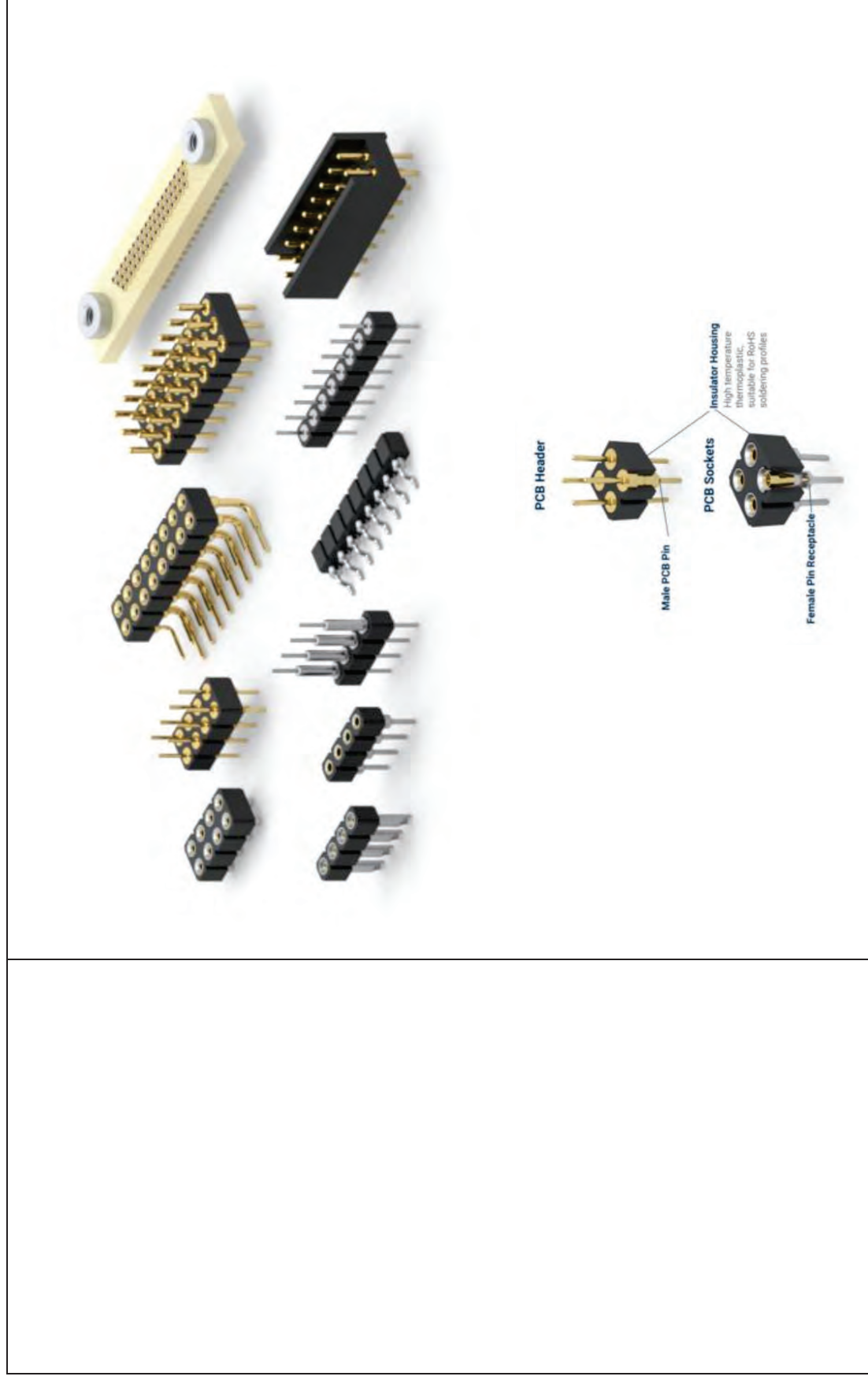
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Saeed Board

	<p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <p>PIN CONNECTORS</p> <p>Pin Connectors</p>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p> <p>View Range</p>
--	---

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

	<p>PCB CONNECTORS</p>  <p>https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html</p>
--	---



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

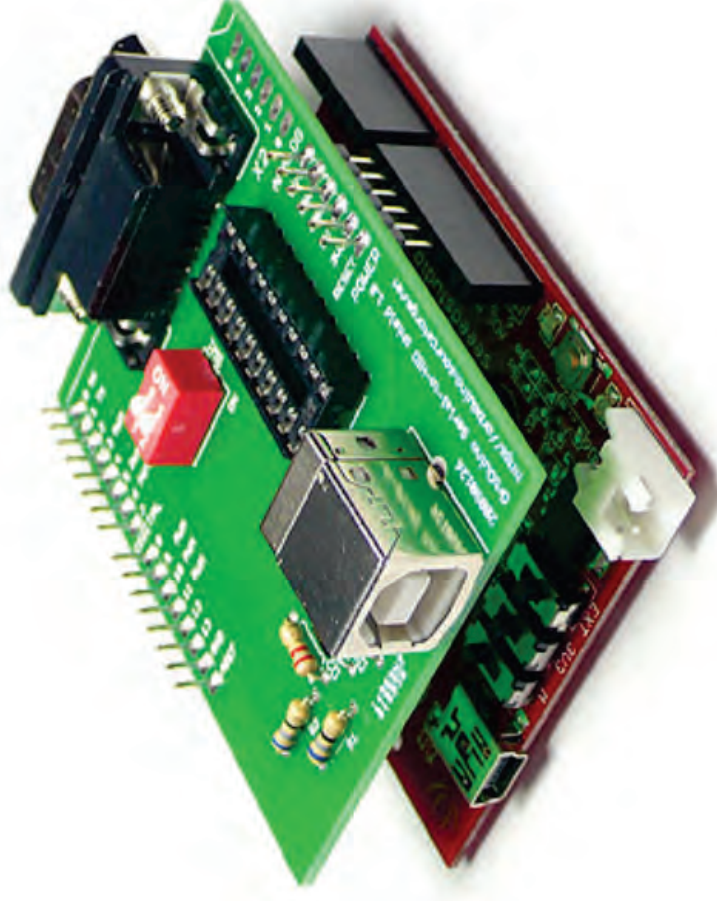
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Claim 6

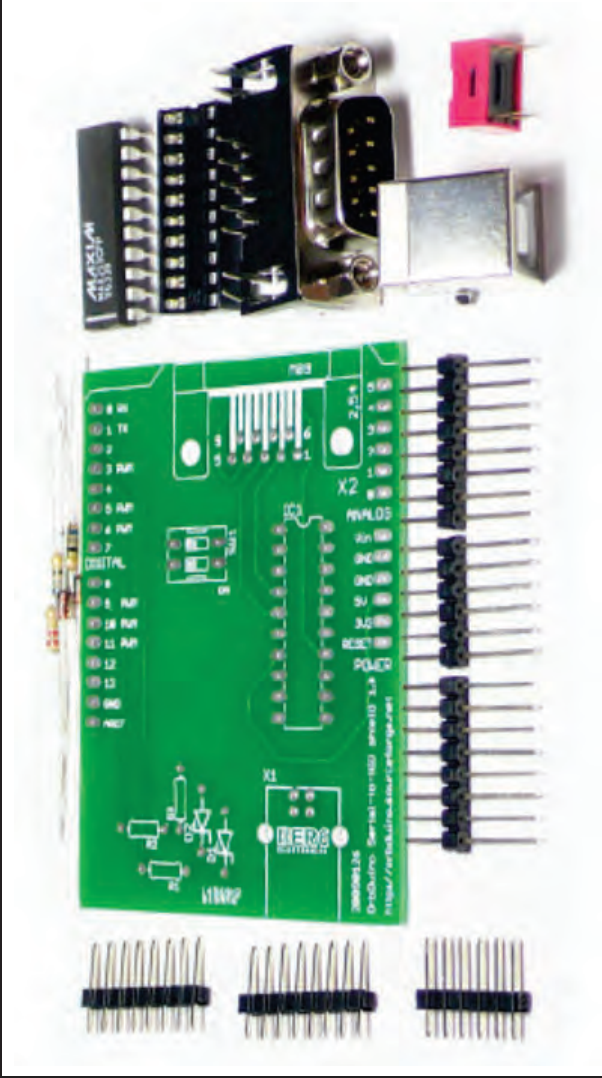
Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of top metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>	<p>Sseed Board discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

corresponding top metal pads of the spacer connector.



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

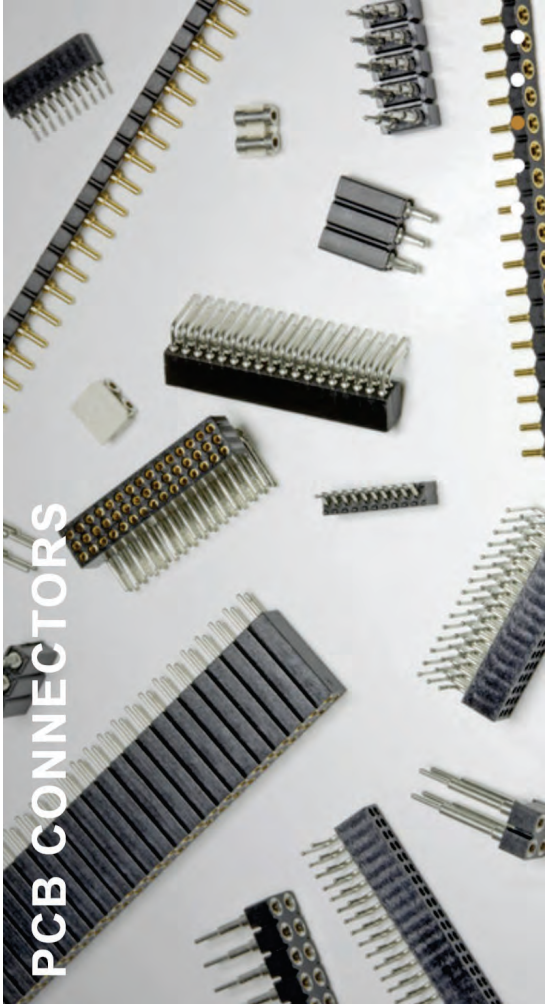
	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p>
--	--

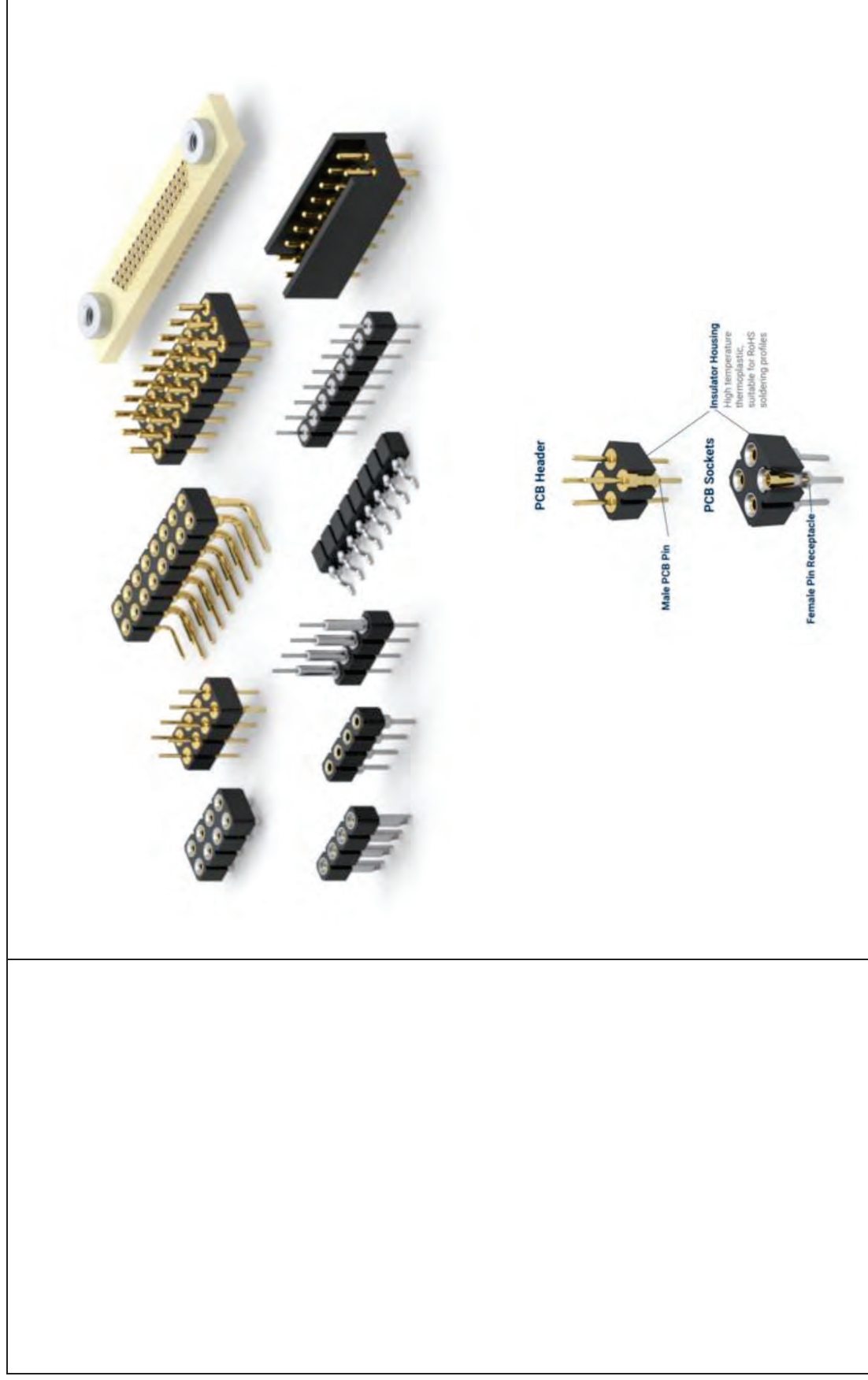
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Saeed Board

	<p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <p>PIN CONNECTORS</p> <p>Pin Connectors</p>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <p>View Range</p> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

	<p>PCB CONNECTORS</p>  <p>https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html</p>
--	---



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

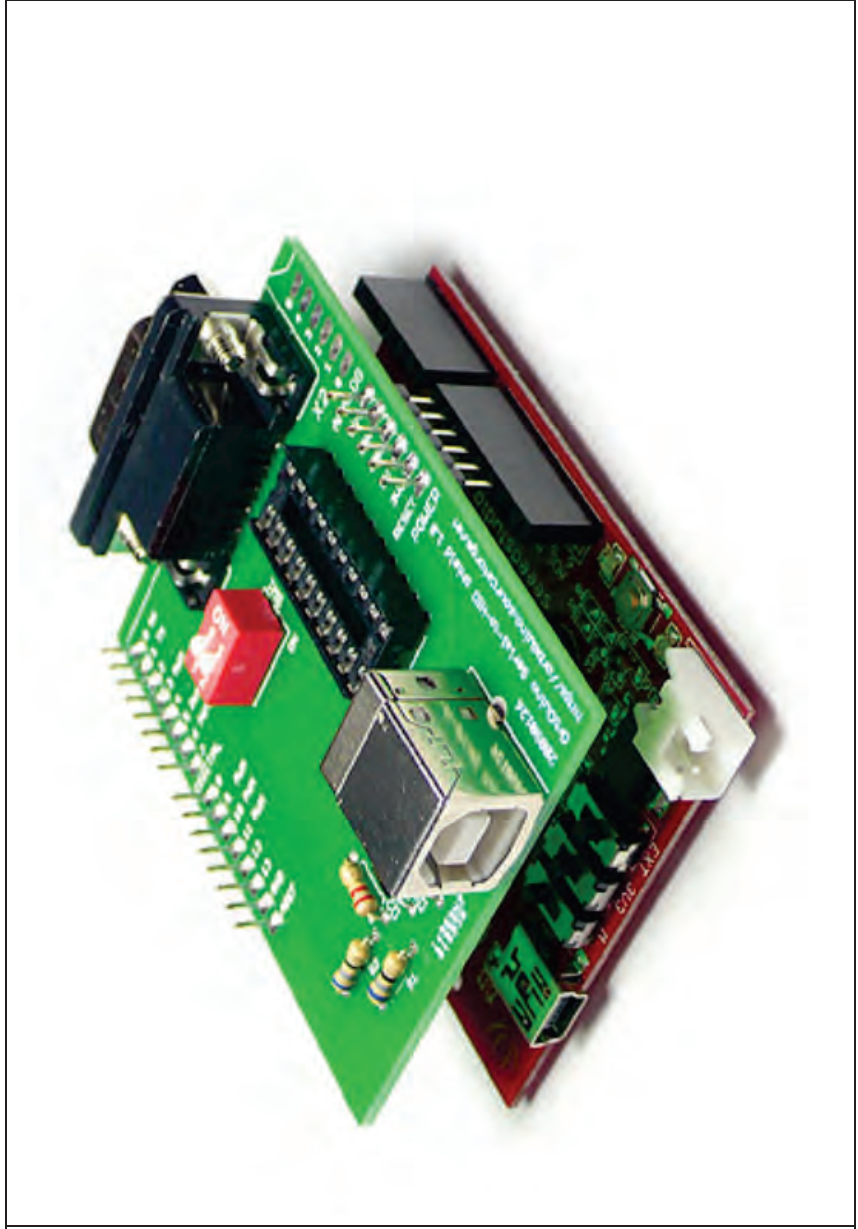
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Claim 9

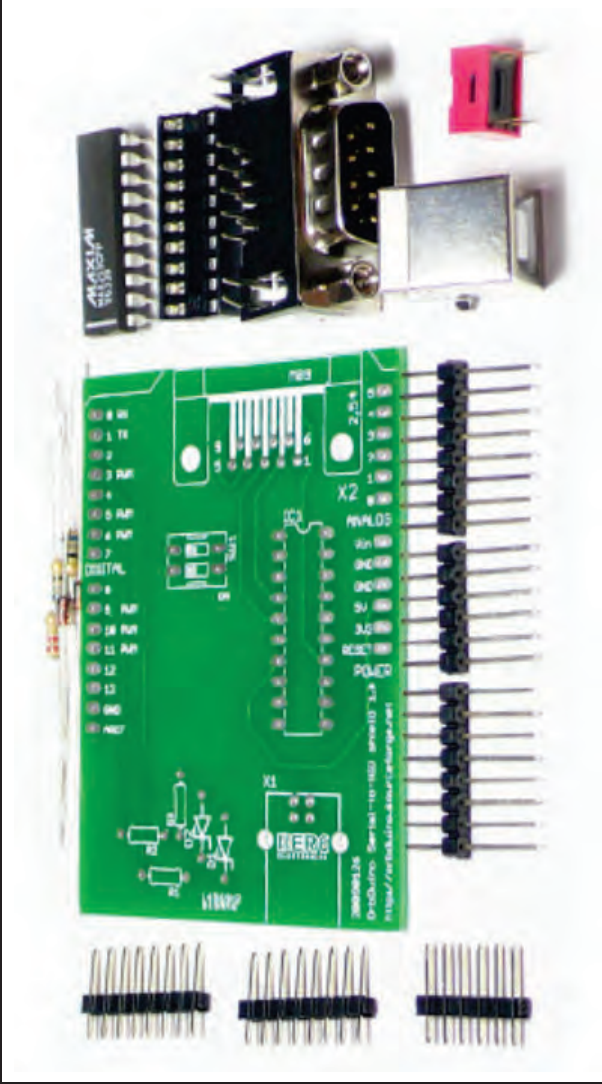
Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>	<p>Seed Board discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sseed Board

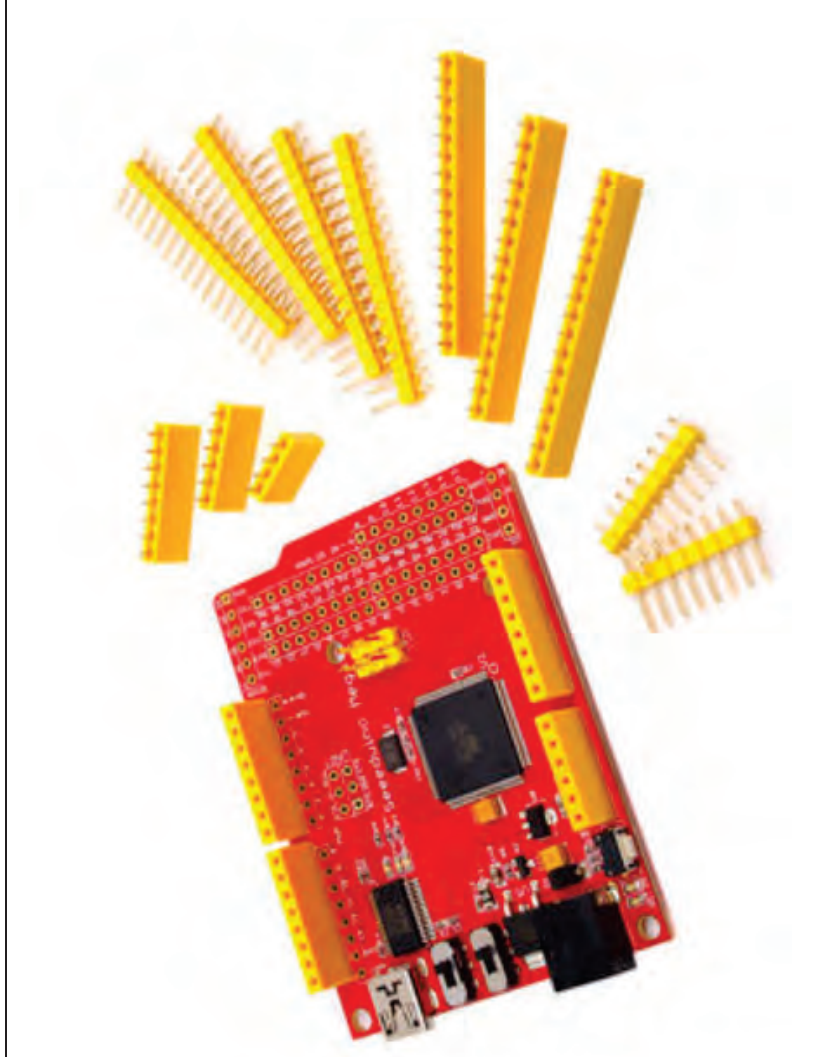
top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

	 <p>“This is the OrbShield, a small circuit board which interfaces with the Arduino microcontroller to convert serial gaming devices to USB HID plug-and-play controllers. It was designed for the SpaceTec SpaceOrb 360, a 6-degree-of-freedom controller for 3d games, and currently supports the SpaceOrb 360 and the Spaceball 2000, 3000, and 4000 series of 3-d CAD controllers.”</p> <p>https://web.archive.org/web/20120920134614/http://www.seeedstudio.com/depot/orbshield-v10-kit-p-671.html?cPath=132_134</p>
--	--

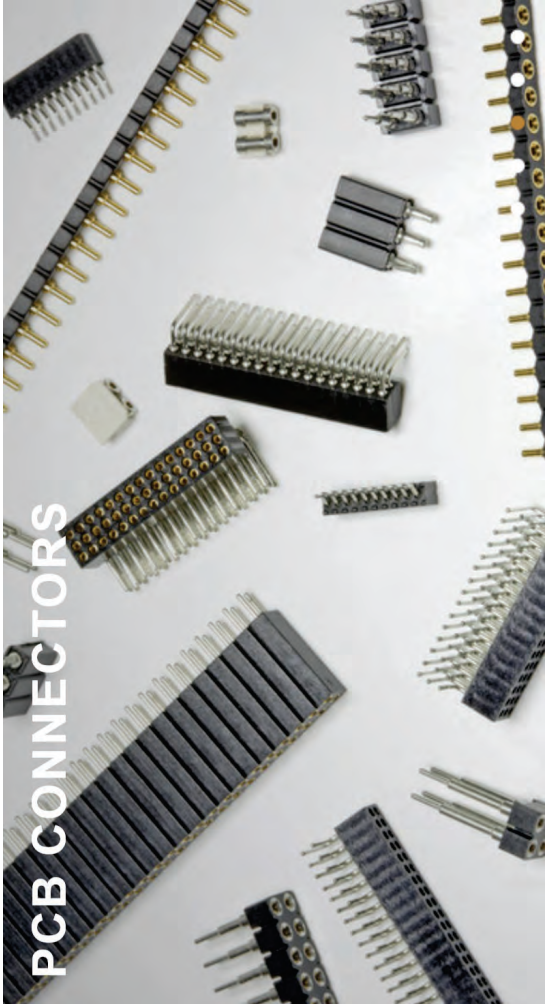
Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Seeed Board

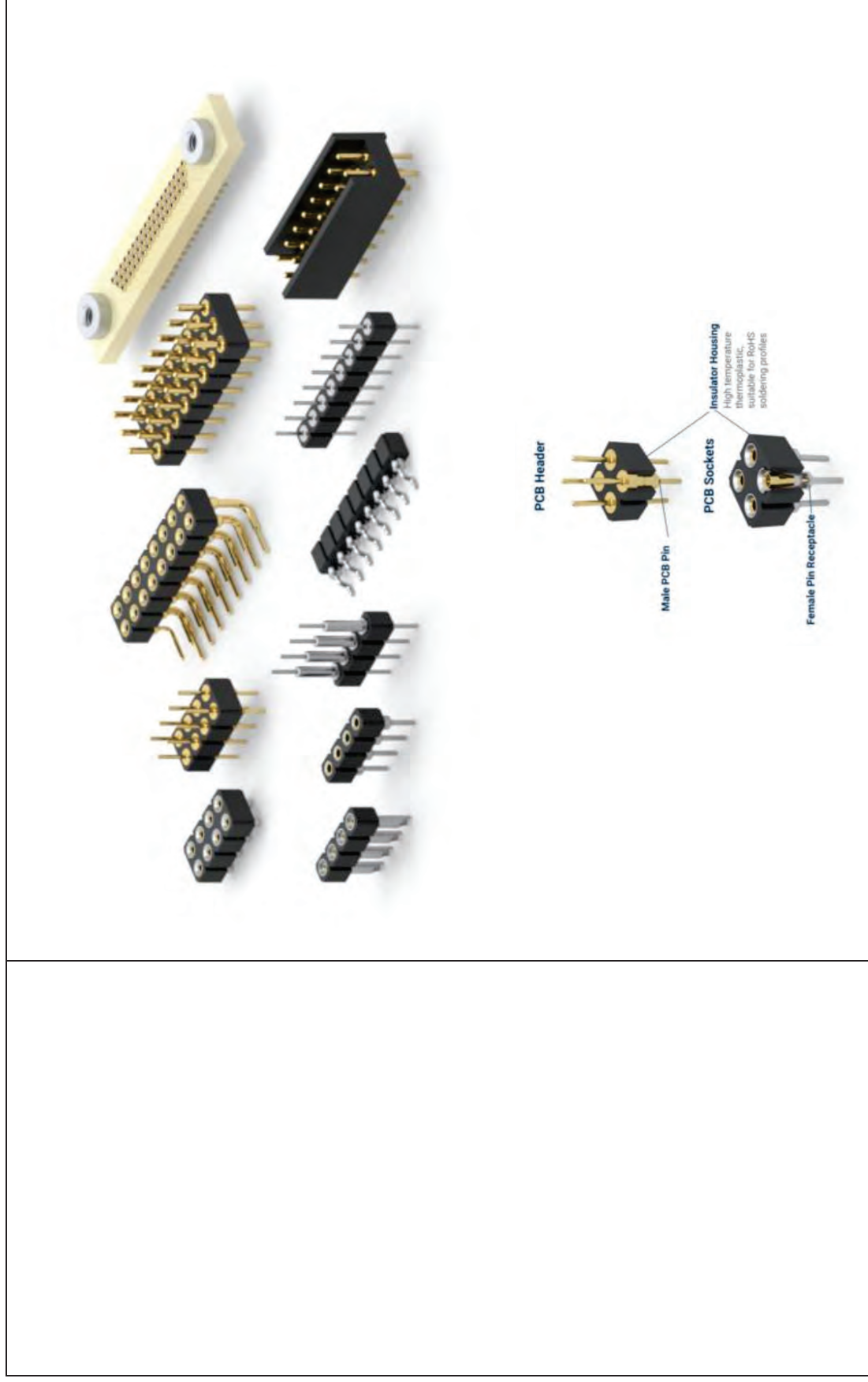
	 <p>https://web.archive.org/web/20140330032412/http://www.seeedstudio.com/wiki/Seeeduino_Mega</p> <p>To the extent Plaintiff contends that Seeed Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p>
--	--

Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Saeed Board

	<p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	--

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	--

	<p>PCB CONNECTORS</p>  <p>https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html</p>
--	--



Appendix A-48 - Invalidity of U.S. Patent No. 9,859,202 in view of Sreed Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

E.D. Tex. Case No. 2:25-cv-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

The SainSmart controller boards, including but not limited to SainSmart UNO and SainSmart Mega stacked with wireless shields, including but not limited to Ethernet Shield W5100 (hereinafter “SainSmart Board”) was in public use, on sale (including sold to customers and potential customers), and/or otherwise available to the public by SainSmart at least by Feb. 9, 2014.¹ SainSmart Board anticipates and/or renders obvious all Asserted Claims² of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.³ SainSmart Board, or the written materials describing it, excerpted below, is prior art to the ’202 Patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within SainSmart Board, or otherwise rendered obvious by disclosures and teachings of SainSmart Board, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that SainSmart Board does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of SainSmart Board with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 Patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by SainSmart Board, either alone or in combination with other prior art cited by Samsung and/or with

¹ See, e.g., <https://web.archive.org/web/20140209015215/http://www.sainsmart.com/arduino/control-boards.html>

² As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

³ To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

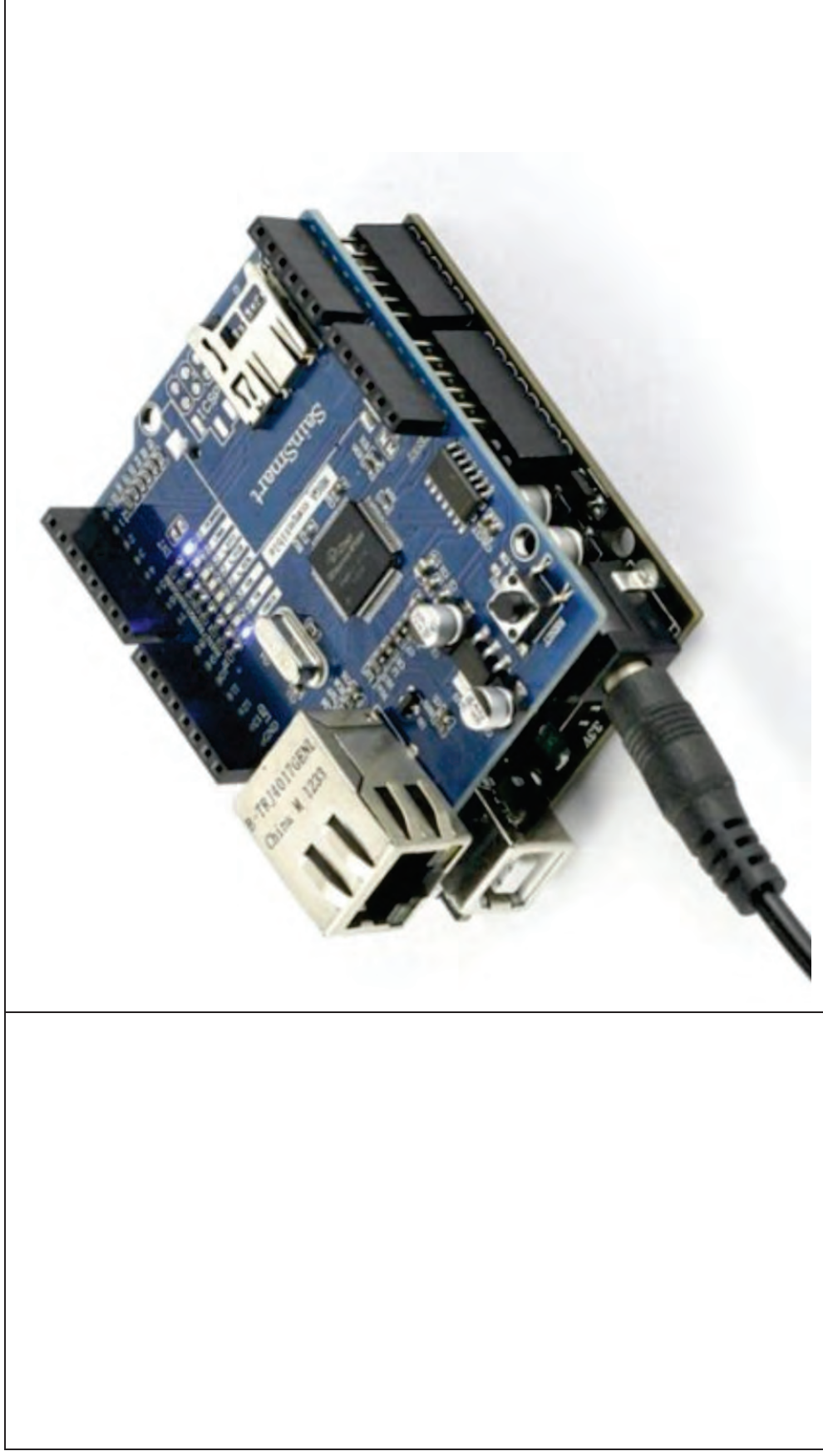
the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that SainSmart Board “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to SainSmart Board or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding SainSmart Board set forth in this chart.

Claim 1

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, SainSmart Board discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>



Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<div> </div> <p>“This is SainSmart UNO R3 Improved Version Starter Kit contains one SainSmart UNO R3 Improved Version and one Ethernet Shield, which is widely used for Arduino Fans and Starters.”</p> <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p> <p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.A] a bottom package substrate;</p>	<p>SainSmart Board discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>“SainSmart UNO R3 Improved Version: ... This is the new SainSmart Uno R3. In addition to all the features of the previous board, the Uno R3 now uses an ATmega16U2 instead of the ATmega8U2 chip. This allows for faster transfer rates, no drivers needed for Linux or Mac (inf file for Windows is needed), and the ability to have the Uno show up as a keyboard, mouse, joystick, etc. ...”</p> <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	---

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

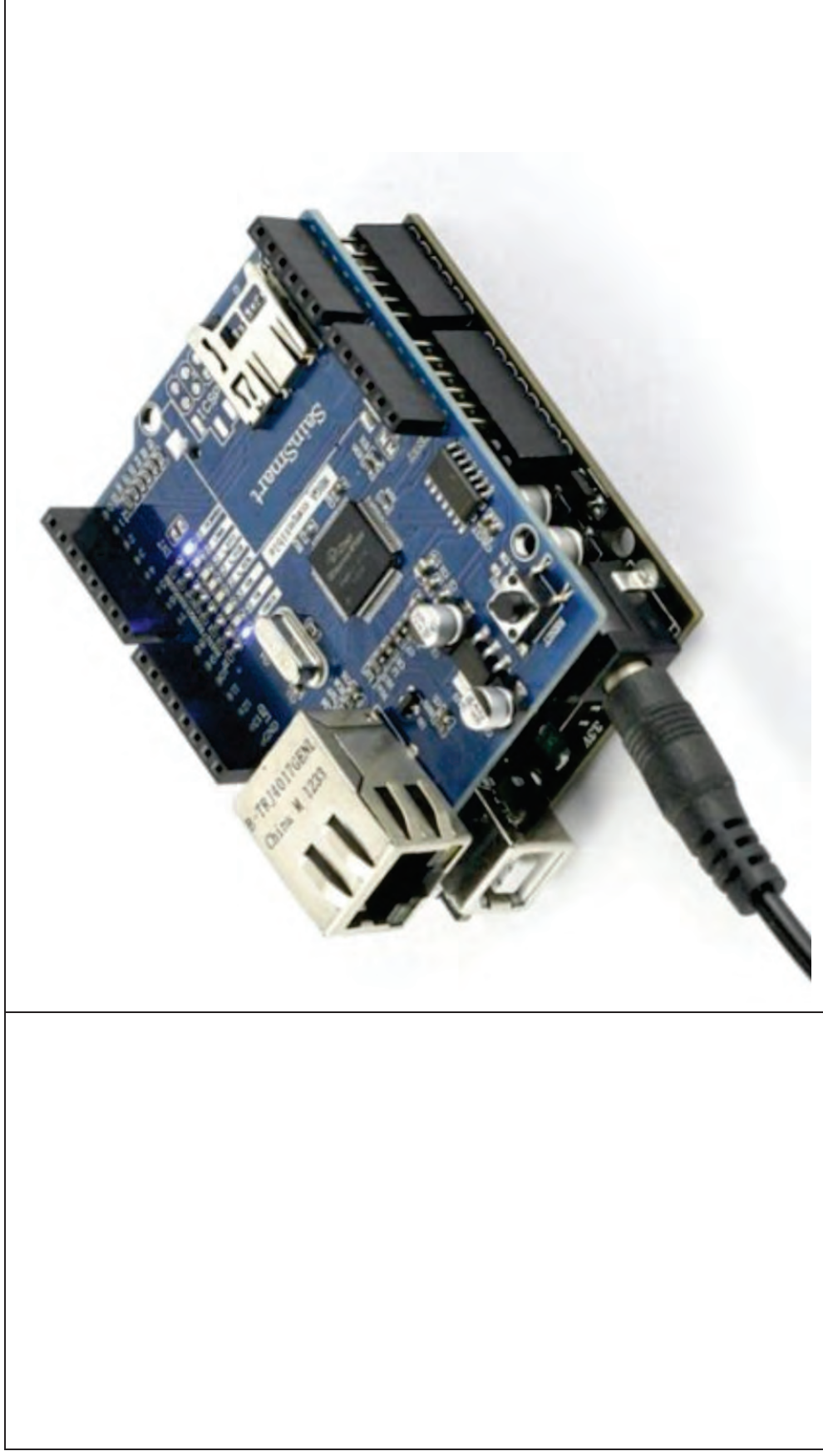
	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>SainSmart Board discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>“Ethernet Shield: For all version of arduino Main board, 2009, UNO, mega 1280, mega 2560 With this Ethernet Shield, your Arduino board can be used to connect to internet controller: w5100 works as server or client ...”</p> <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>SainSmart Board discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.</p> <p><i>See, e.g.:</i></p>



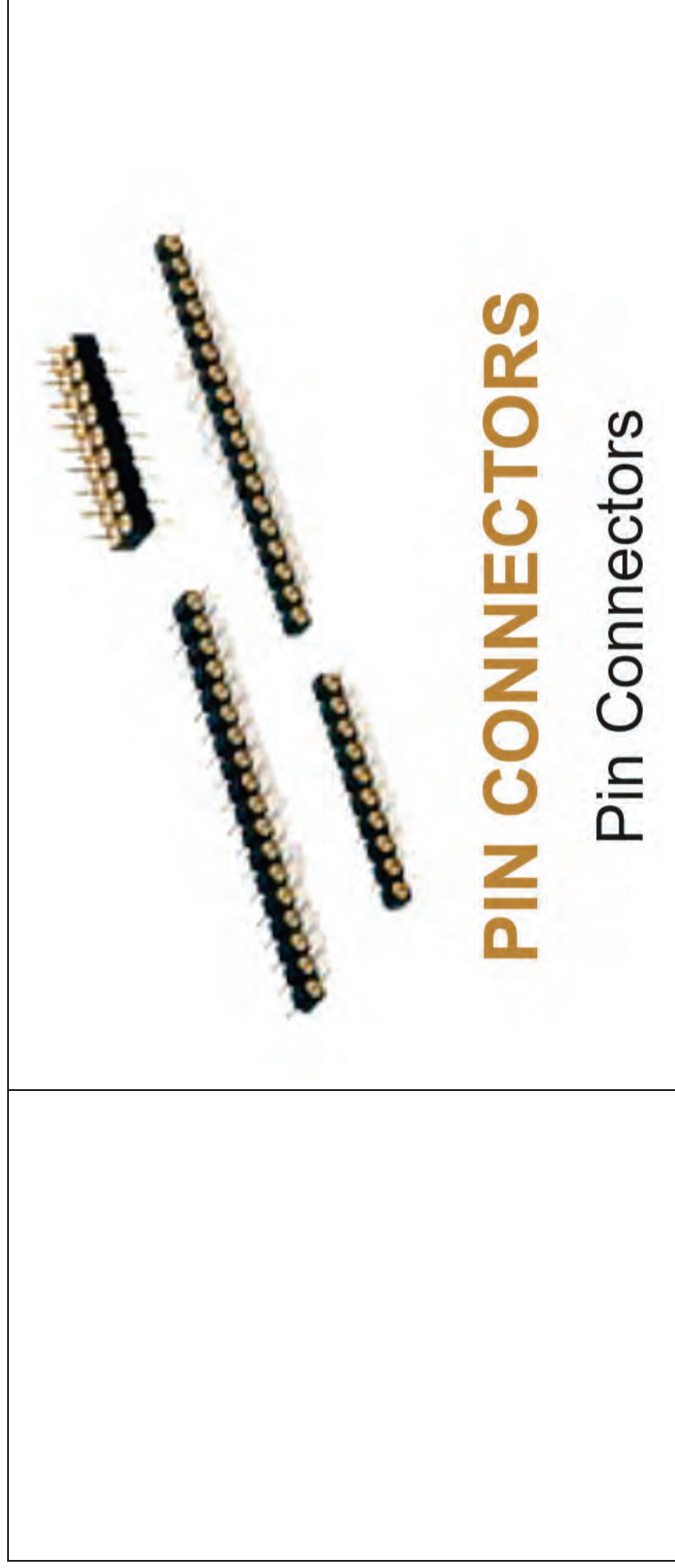
Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board



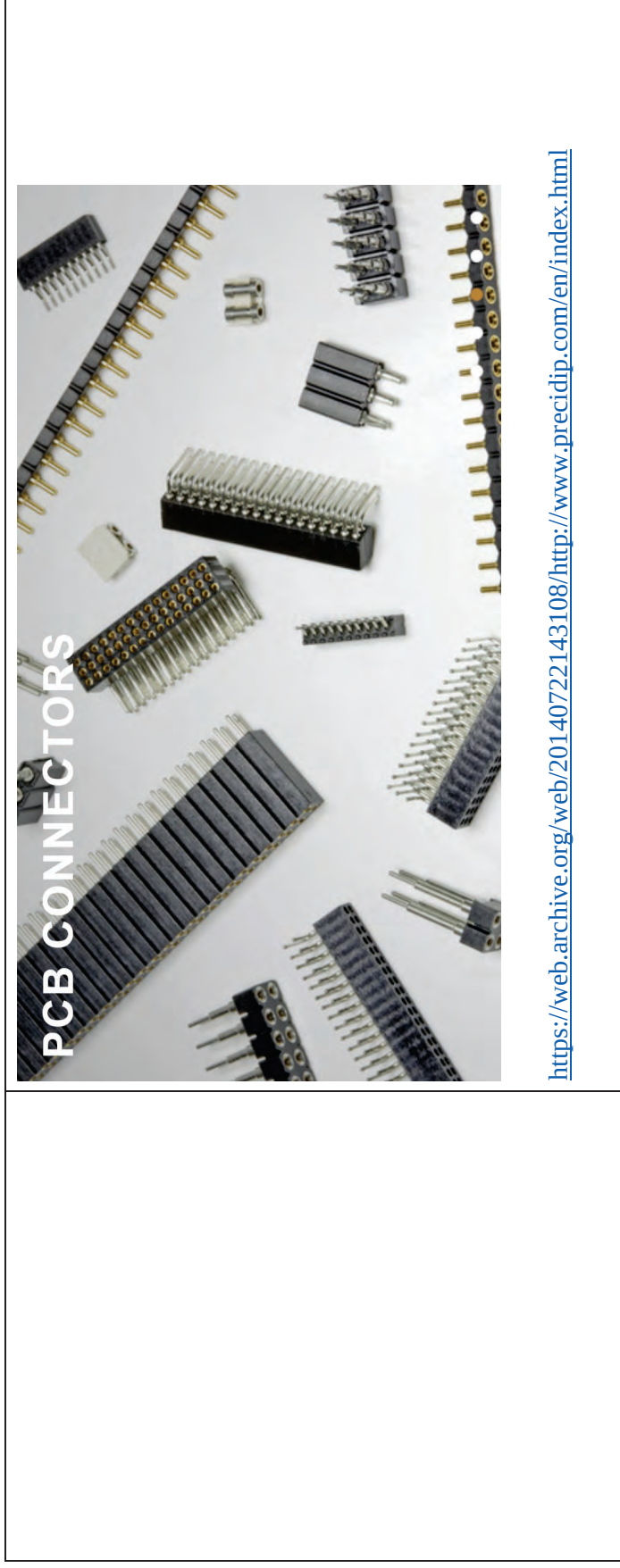
<https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html>

To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.

For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.



	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

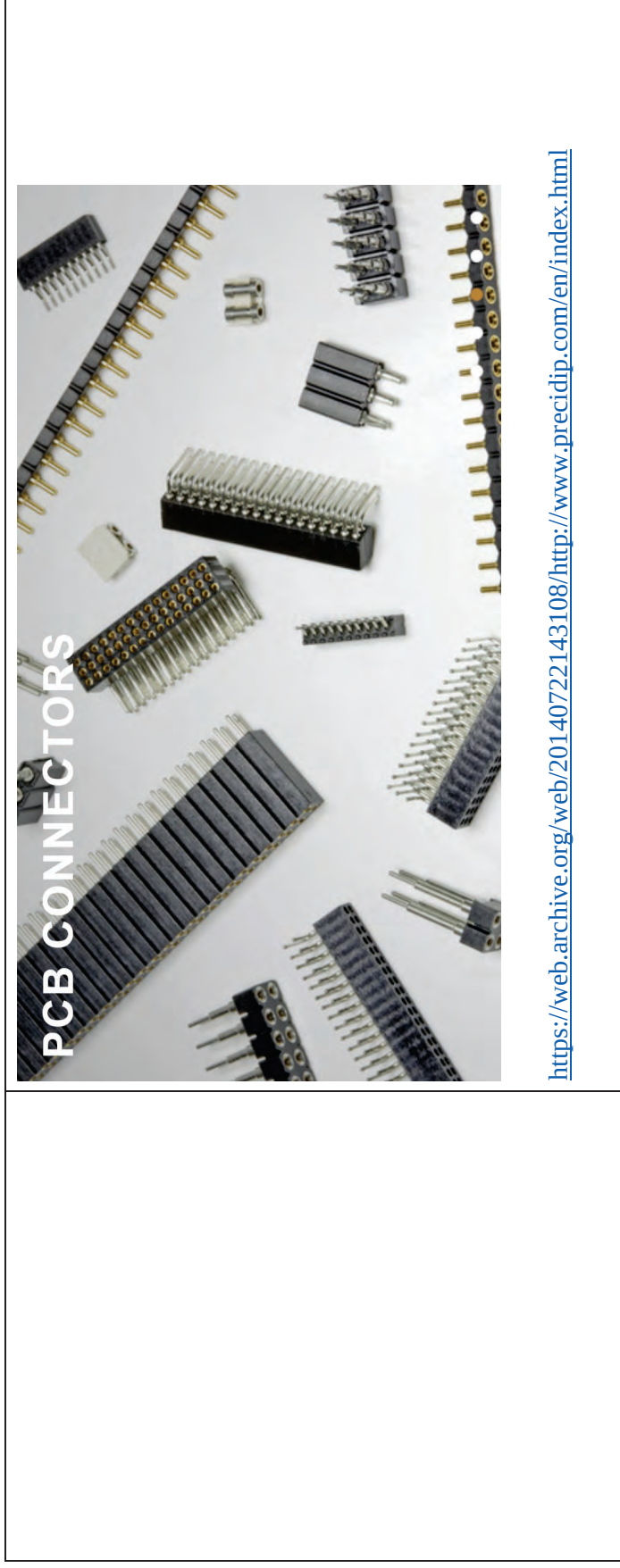
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>SainSmart Board discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

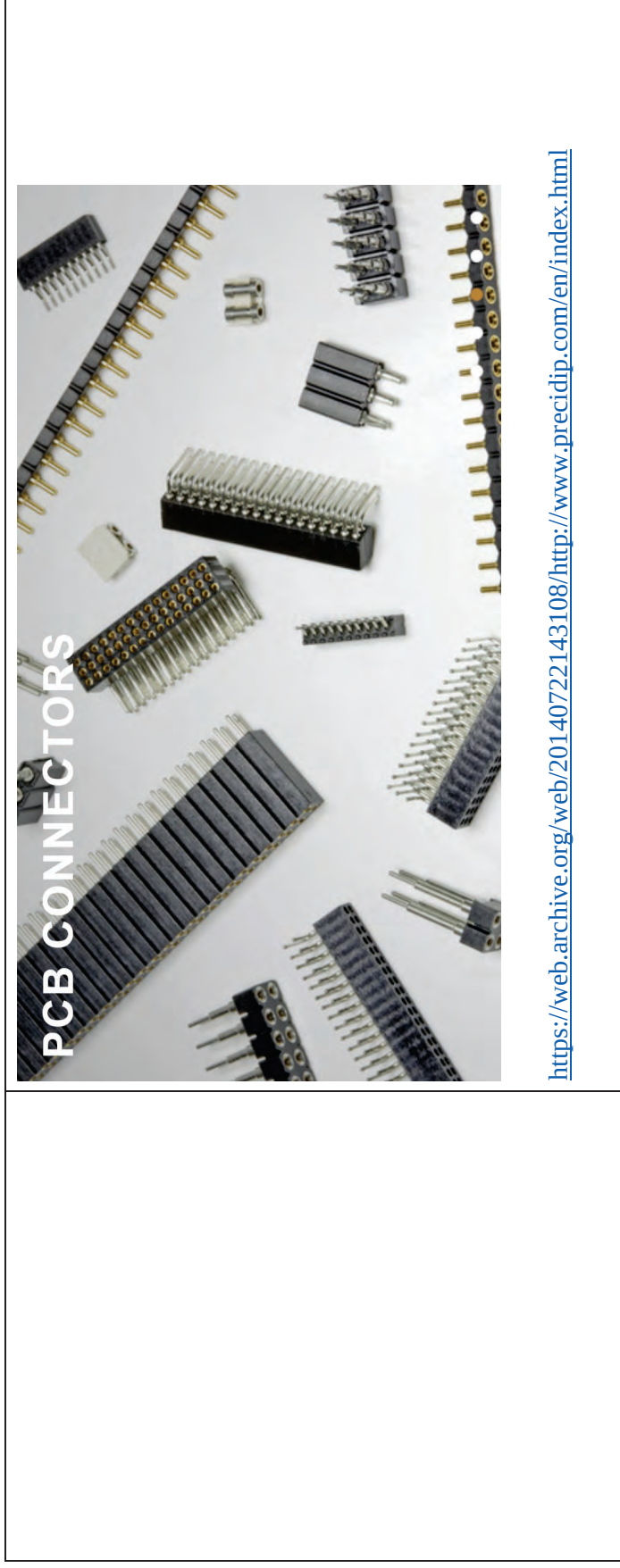
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>SainSmart Board discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board



	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	--





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

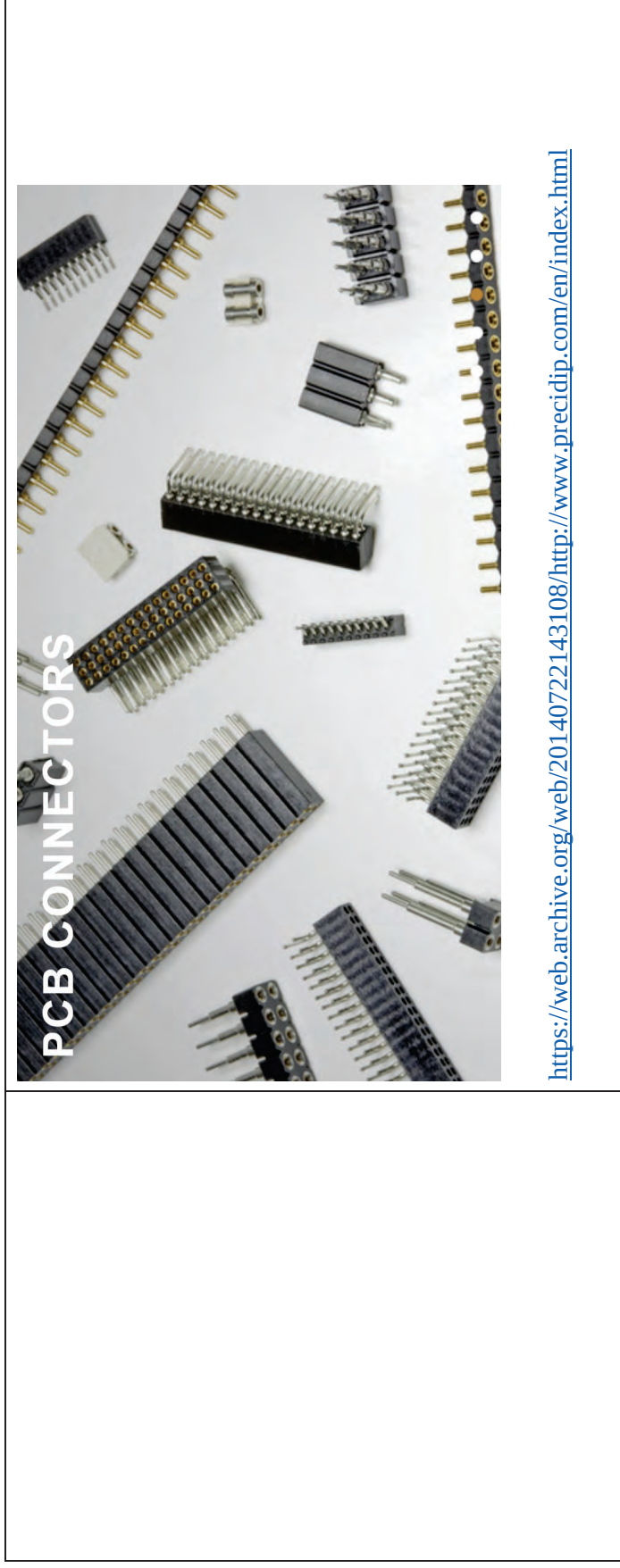
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>SainSmart Board discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

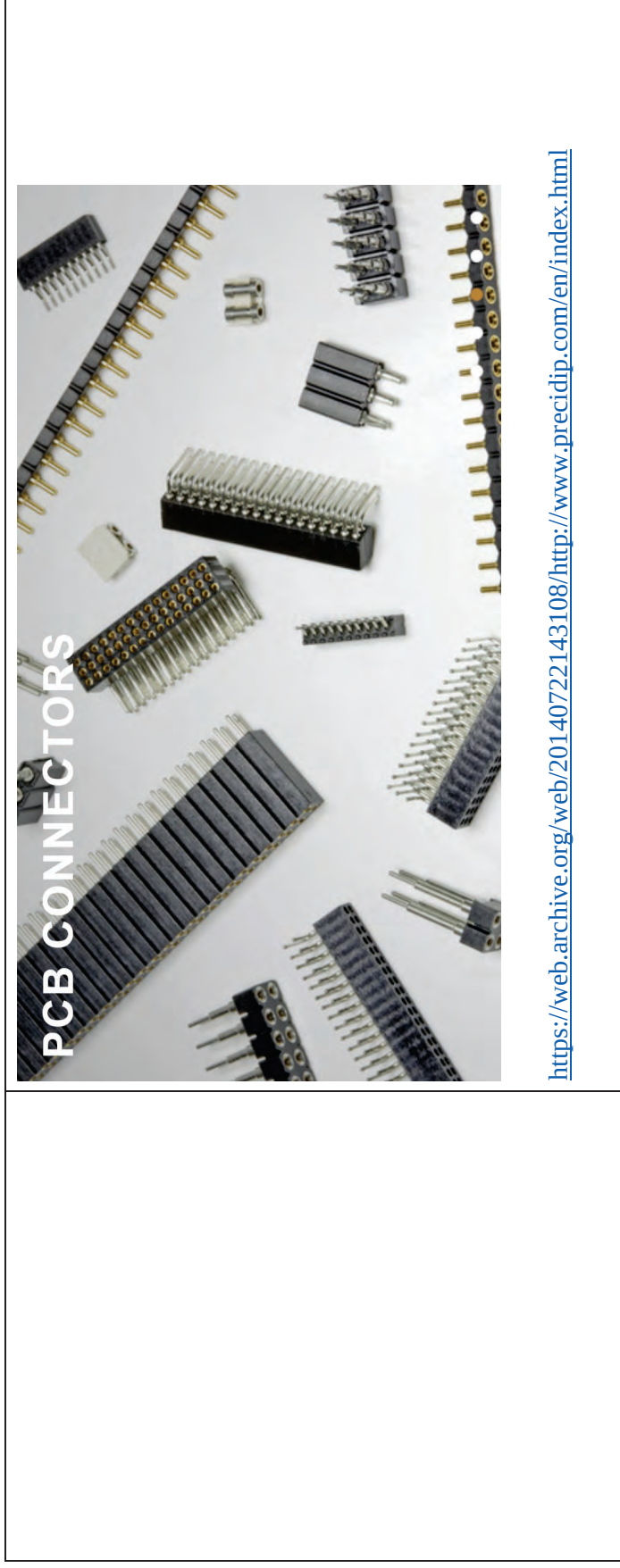
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>SainSmart Board discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

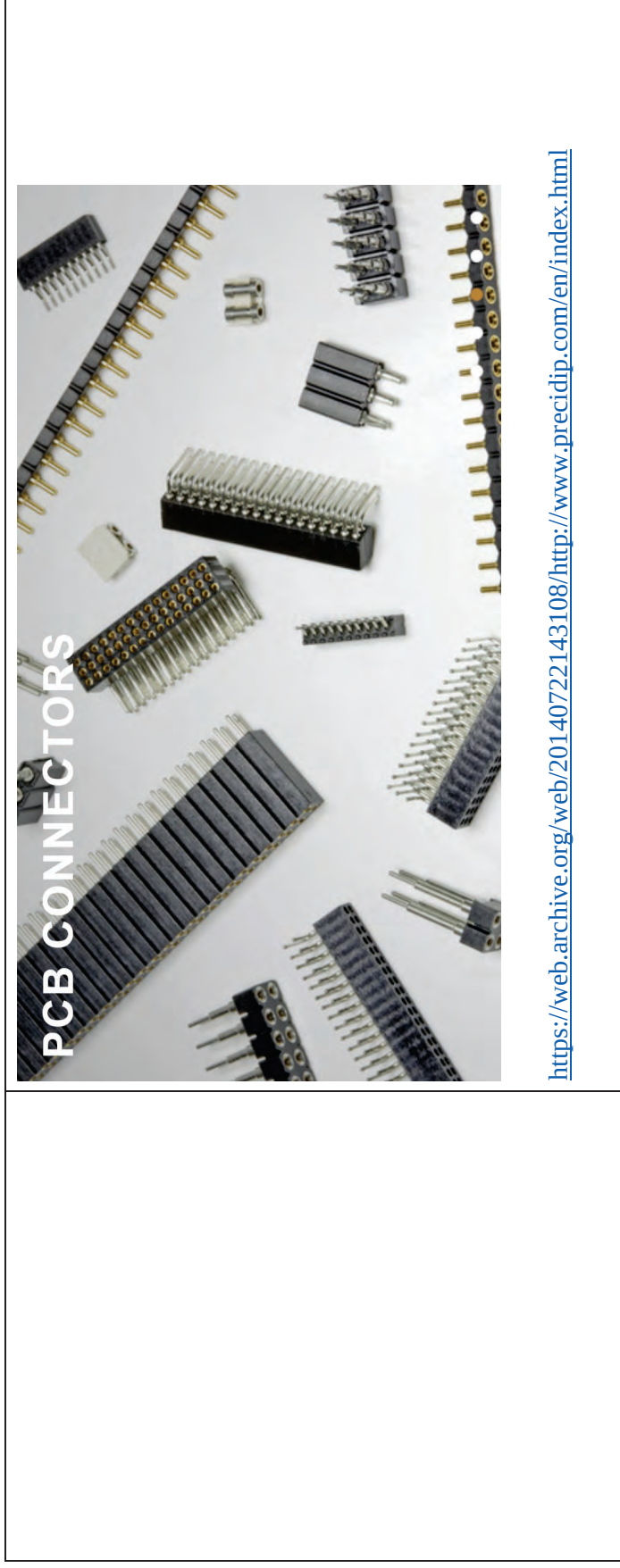
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>SainSmart Board discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

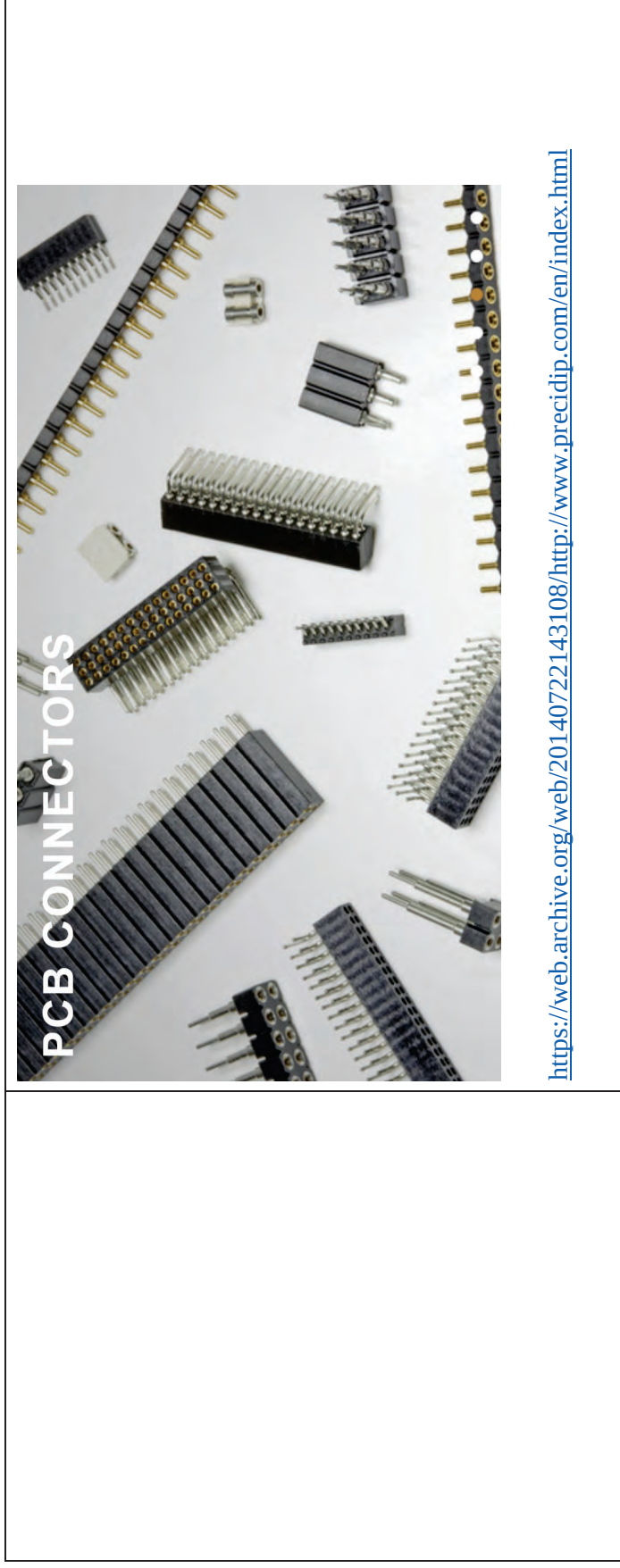
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>SainSmart Board discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





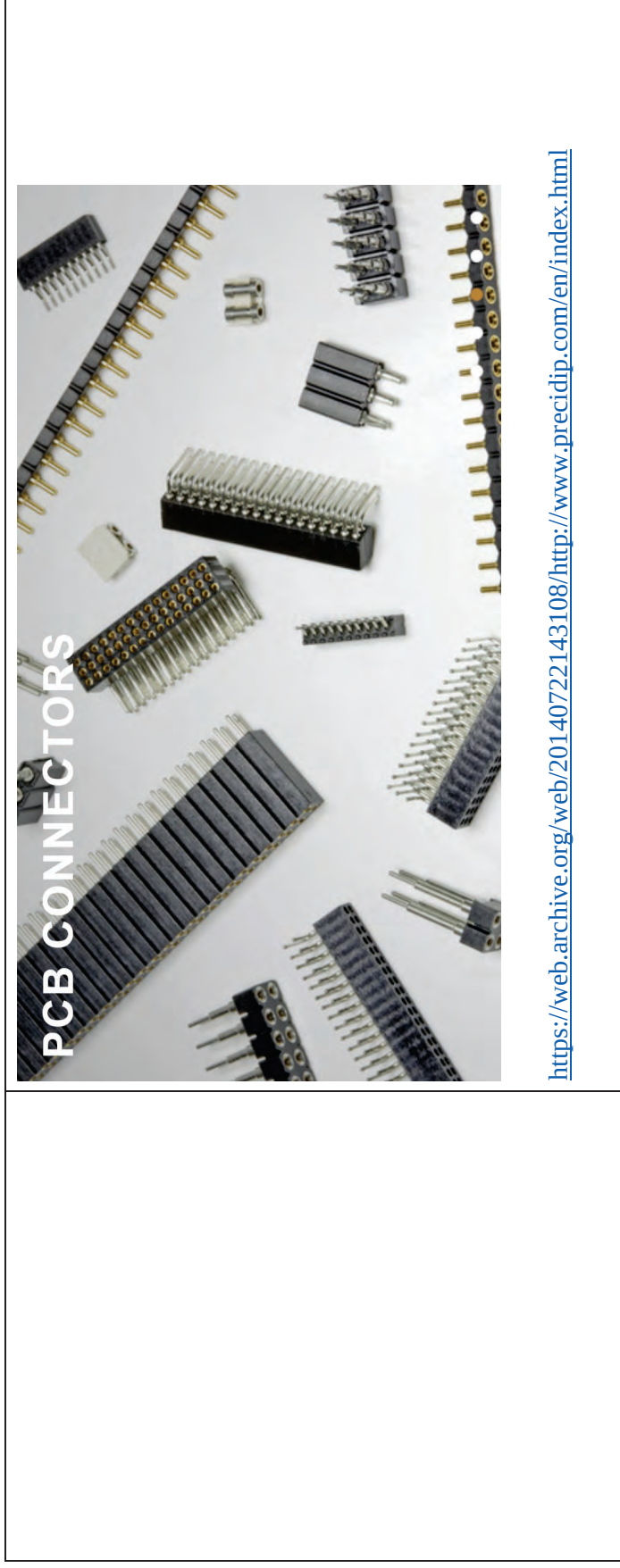
Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>SainSmart Board discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>



	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>SainSmart Board discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate.</p> <p><i>See, e.g.:</i></p>



	<div></div> <div><p>“SainSmart UNO R3 Improved Version: ... This is the new SainSmart Uno R3. In addition to all the features of the previous board, the Uno R3 now uses an ATmega16U2 instead of the ATmega8U2 chip. This allows for faster transfer rates, no drivers needed for Linux or Mac (inf file for Windows is needed), and the ability to have the Uno show up as a keyboard, mouse, joystick, etc. ...”</p></div>
--	--

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p> <p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>SainSmart Board discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	 <p>“SainSmart UNO R3 Improved Version: ... This is the new SainSmart Uno R3. In addition to all the features of the previous board, the Uno R3 now uses an ATmega16U2 instead of the ATmega8U2 chip. This allows for faster transfer rates, no drivers needed for Linux or Mac (inf file for Windows is needed), and the ability to have the Uno show up as a keyboard, mouse, joystick, etc. ...”</p> <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	---

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>SainSmart Board discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

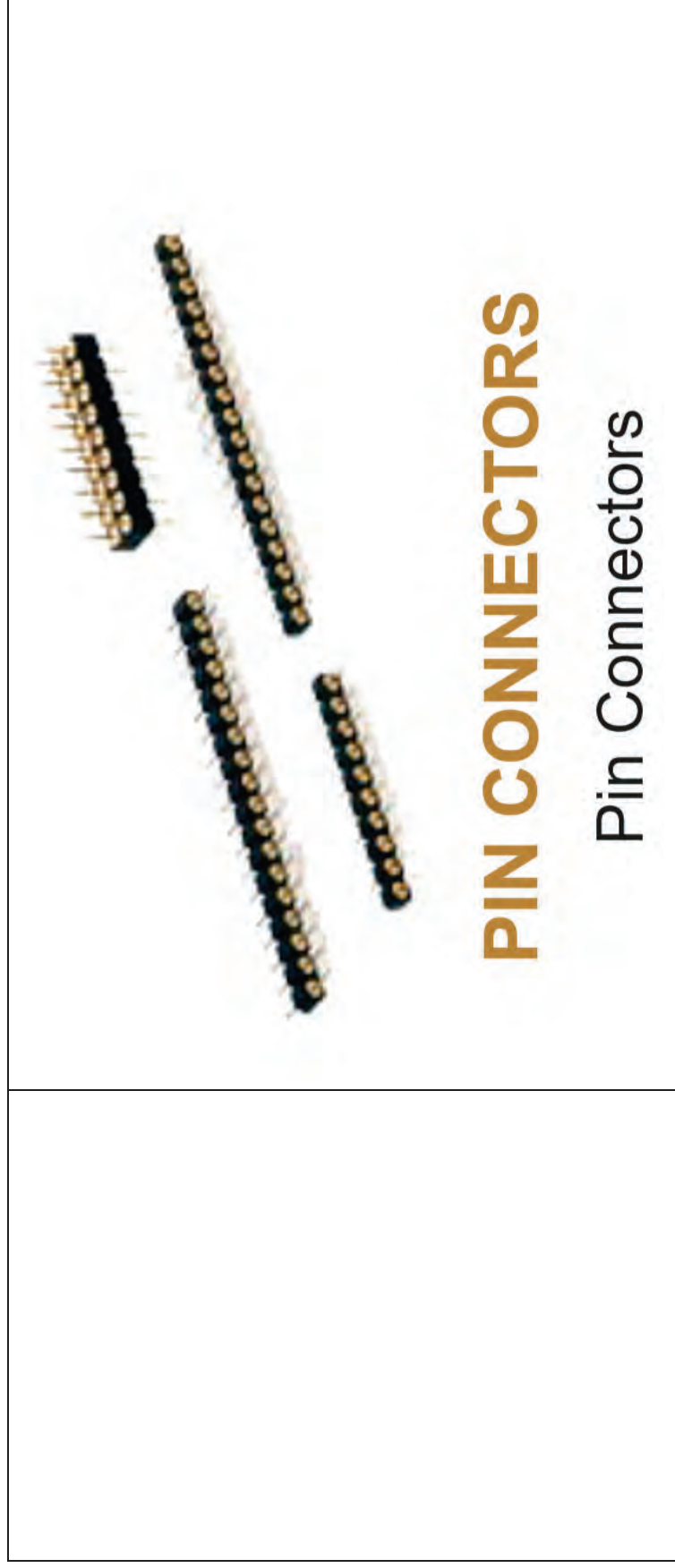




“SainSmart UNO R3 Improved Version: ... This is the new SainSmart Uno R3. In addition to all the features of the previous board, the Uno R3 now uses an ATmega16U2 instead of the ATmega8U2 chip. This allows for faster transfer rates, no drivers needed for Linux or Mac (inf file for Windows is needed), and the ability to have the Uno show up as a keyboard, mouse, joystick, etc. ...”

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p> <p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>
--	--



	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Claim 2

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>SainSmart Board discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>





“SainSmart UNO R3 Improved Version: ... This is the new SainSmart Uno R3. In addition to all the features of the previous board, the Uno R3 now uses an ATmega16U2 instead of the ATmega8U2 chip. This allows for faster transfer rates, no drivers needed for Linux or Mac (inf file for Windows is needed), and the ability to have the Uno show up as a keyboard, mouse, joystick, etc. ...”

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p> <p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>SainSmart Board discloses, either expressly or inherently, a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board



Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>“Ethernet Shield: For all version of arduino Main board, 2009, UNO, mega 1280, mega 2560 With this Ethernet Shield, your Arduino board can be used to connect to internet controller: w5100 works as server or client ...”</p> <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	--

Claim 4

Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.	SainSmart Board discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate. <i>See, e.g.:</i>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	 <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.

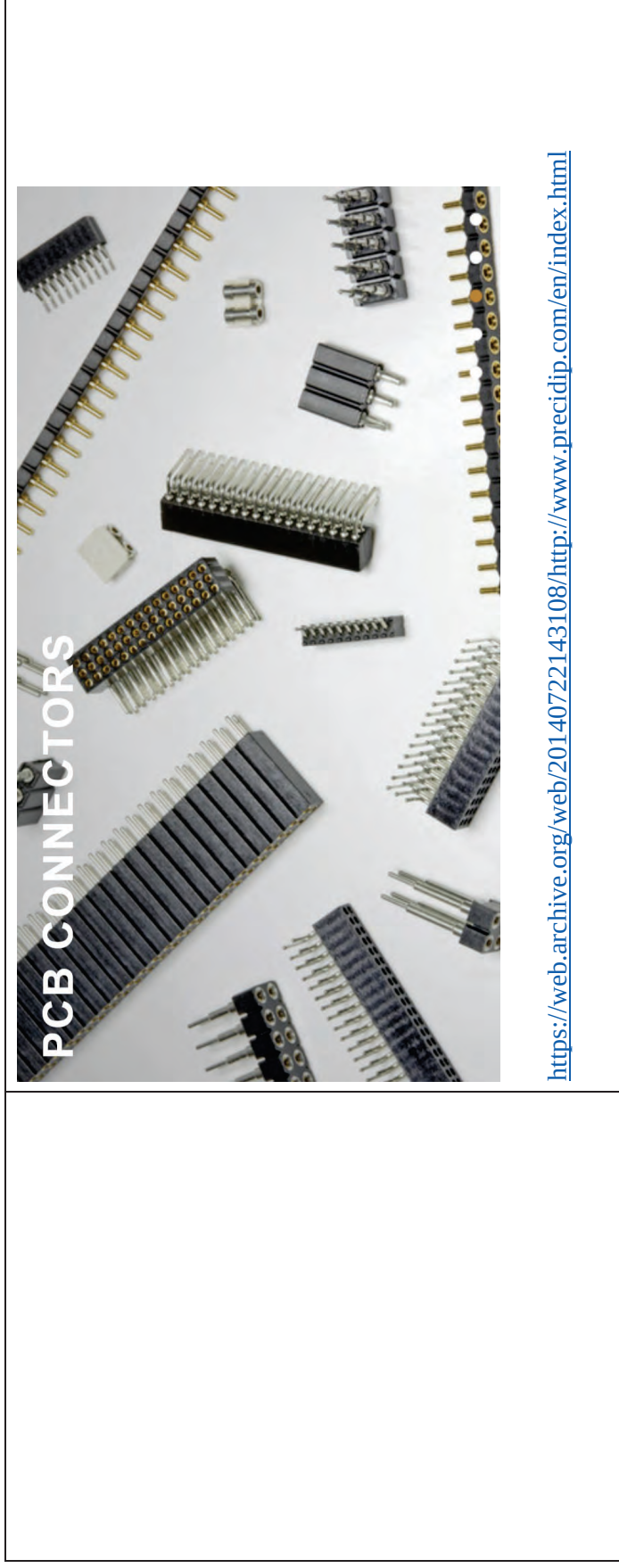
For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.



PIN CONNECTORS

Pin Connectors

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Claim 6

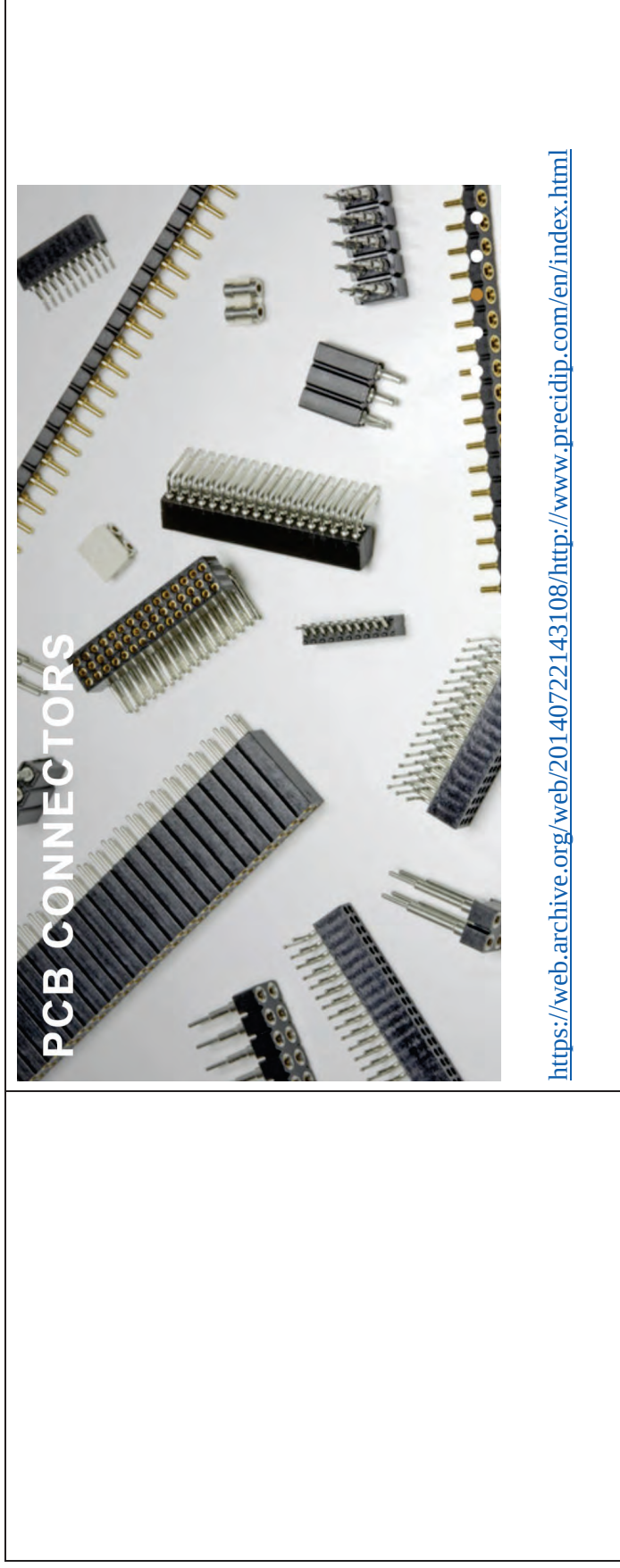
Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of top metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>	<p>SainSmart Board discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of top metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

<p>corresponding top metal pads of the spacer connector.</p>	 <p>https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html</p>
--	--

	<p>To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.</p> <p>For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.</p>  <h1>PIN CONNECTORS</h1> <h2>Pin Connectors</h2>
--	---

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---





Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Claim 9

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the</p>	<p>SainSmart Board discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.



<https://web.archive.org/web/20131215172620/http://www.sainsmart.com/sainsmart-uno-r3-improved-version-ethernet-shield-w5100-for-arduino.html>

To the extent Plaintiff contends that SainSmart Board fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art, (ii) the teachings of any of the charted references with respect to this limitation, and/or (iii) other prior art identified herein.

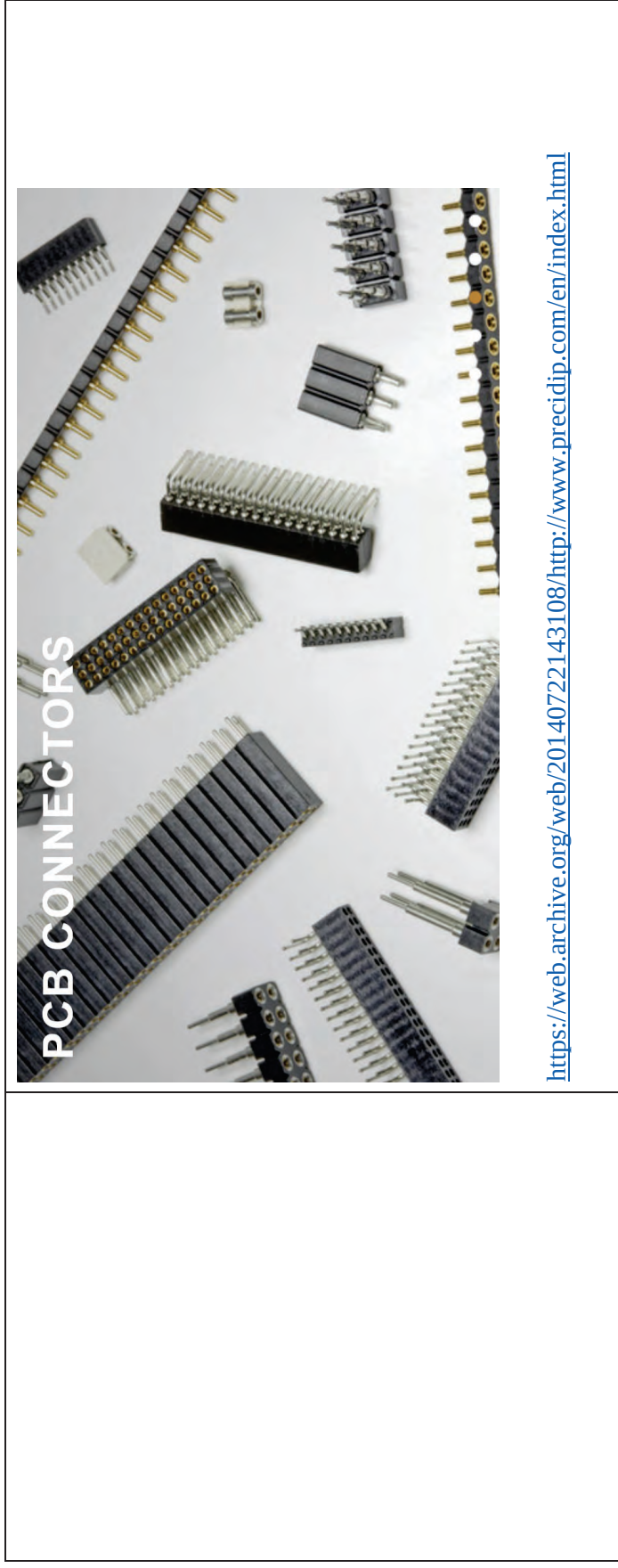
For example, a POSITA would have found it obvious to use other well-known PCB headers, including those shown below, to implement this product feature.



PIN CONNECTORS

Pin Connectors

	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <div>View Range</div> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p>
--	---



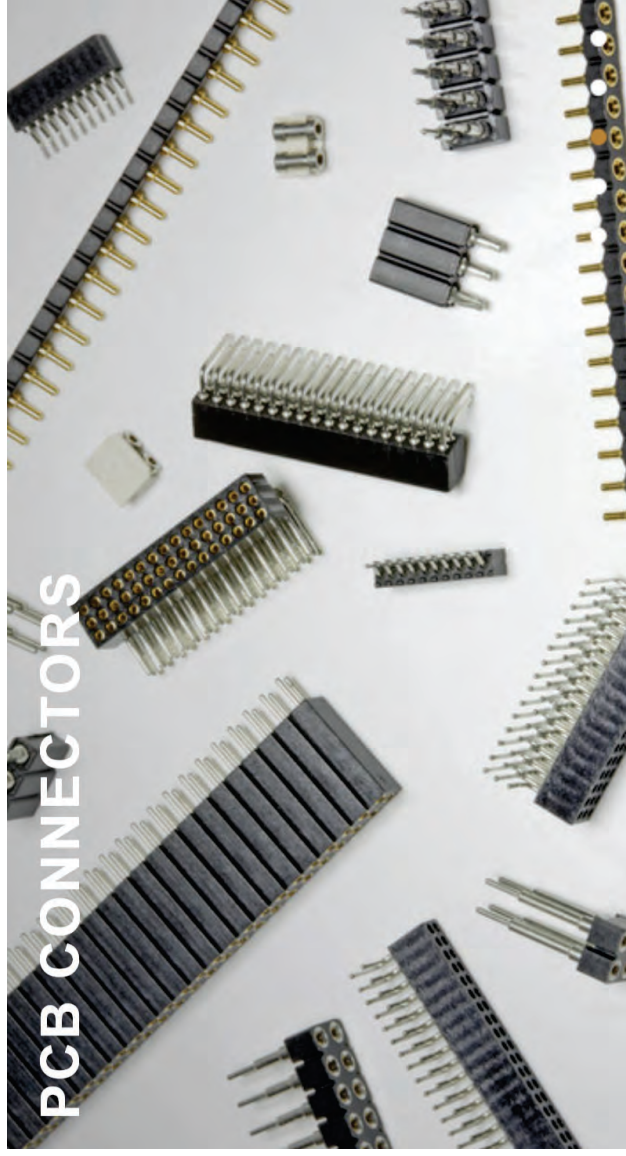


Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

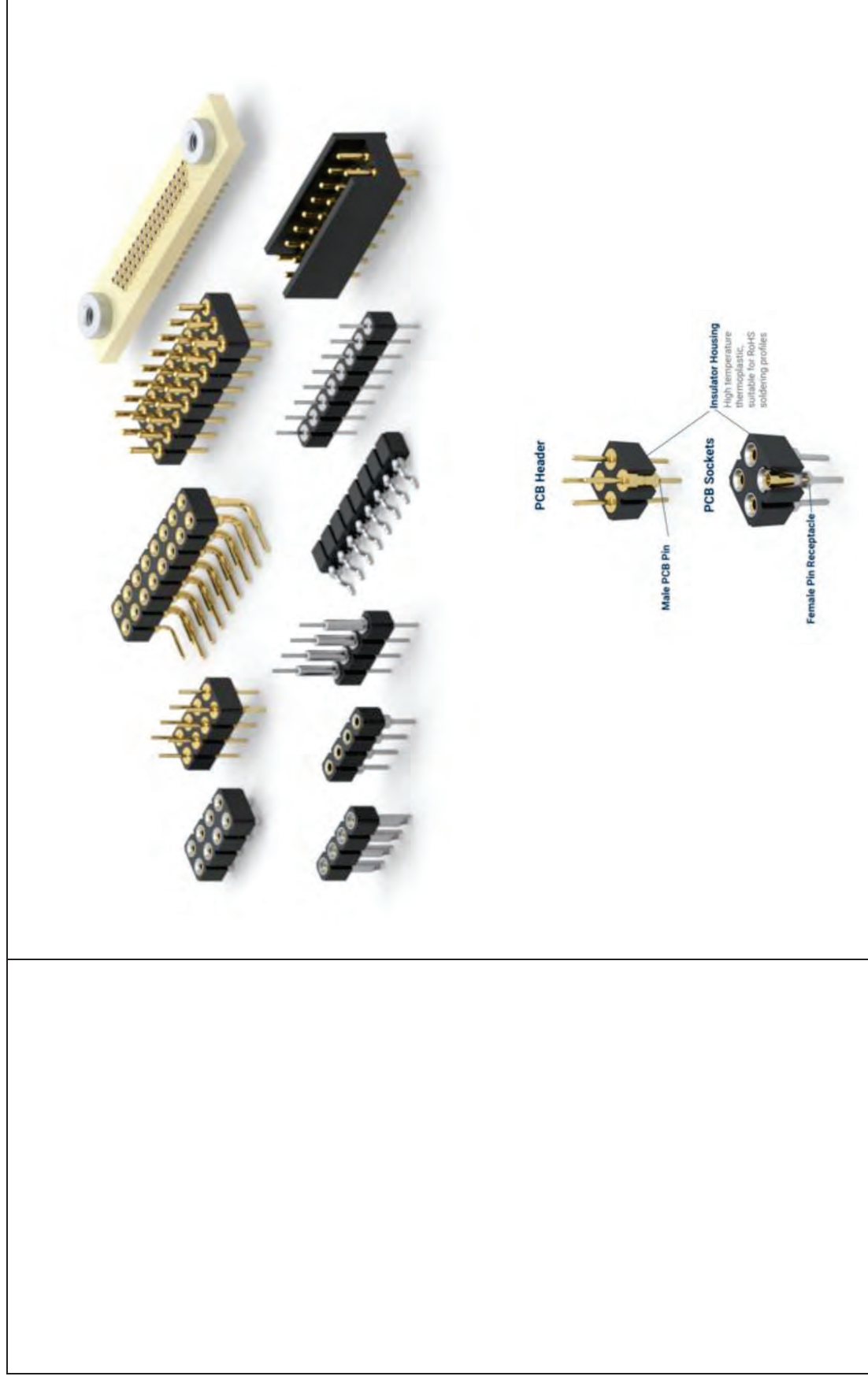
	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--



	 <h1>SOCKET CONNECTORS</h1> <h2>Socket Connectors</h2> <p>https://web.archive.org/web/20140722155507/http://www.precidip.com/en/Products/PCB-Connectors/PCB-Connectors.html</p> <p>View Range</p>
--	---



<https://web.archive.org/web/20140722143108/http://www.precidip.com/en/index.html>



Appendix A-49 - Invalidity of U.S. Patent No. 9,859,202 in view of SainSmart Board

	<p>“PCB connectors and interconnects are often referred to as sockets, headers, or rectangular connectors and are usually offered in many different styles and configurations. Machined Pin PCB connectors offer a highly reliable, precision-made interconnect solution ideal for a number of demanding application requirements in the world of board to board, cable to board, or component to board interconnects.”</p> <p>https://www.mill-max.com/engineering-notebooks/machined-pin-pcb-connectors-interconnects; https://web.archive.org/web/20130827161228/http://www.mill-max.com/</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

E.D. Tex. Case No. 2:25-cv-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

The first generation of Apple iPhone (hereinafter “Apple iPhone 1”) was in public use, on sale (including sold to customers and potential customers), and/or otherwise available to the public by Apple Inc. at least by 2007.¹ Apple iPhone 1 anticipates and/or renders obvious all Asserted Claims² of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.³ Apple iPhone 1, or the written materials describing it, excerpted below, is prior art to the ’202 Patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Apple iPhone 1, or otherwise rendered obvious by disclosures and teachings of Apple iPhone 1, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Apple iPhone 1 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Apple iPhone 1 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 Patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by Apple iPhone 1, either alone or in combination with other prior art cited by Samsung and/or with

¹ See, e.g., [https://en.wikipedia.org/wiki/IPhone_\(1st_generation\)](https://en.wikipedia.org/wiki/IPhone_(1st_generation))

² As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

³ To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Apple iPhone 1 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Apple iPhone 1 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Apple iPhone 1 set forth in this chart.

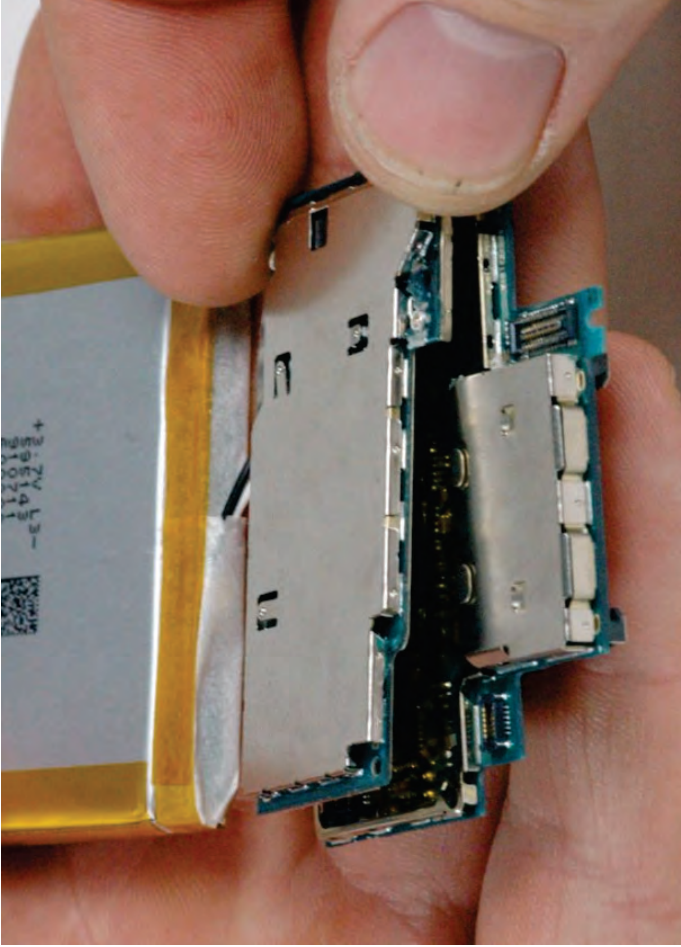
Claim 1

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, Apple iPhone 1 discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

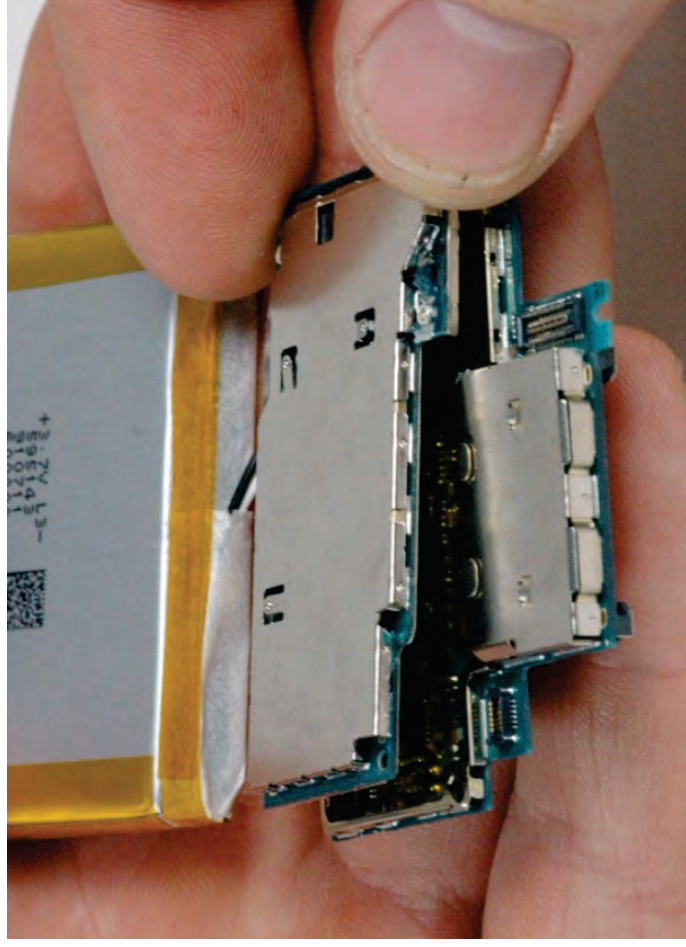


Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

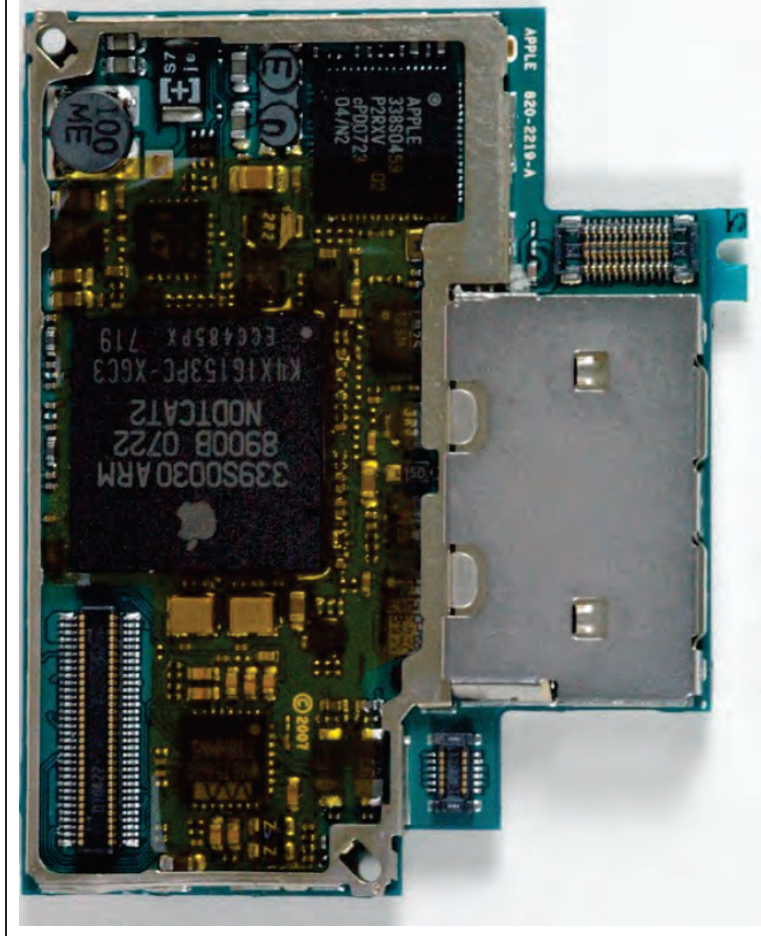
	 <p>“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”</p> <p>https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com</p>
[1.A] a bottom package substrate;	Apple iPhone 1 discloses, either expressly or inherently, a bottom package substrate.

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

See, e.g.:



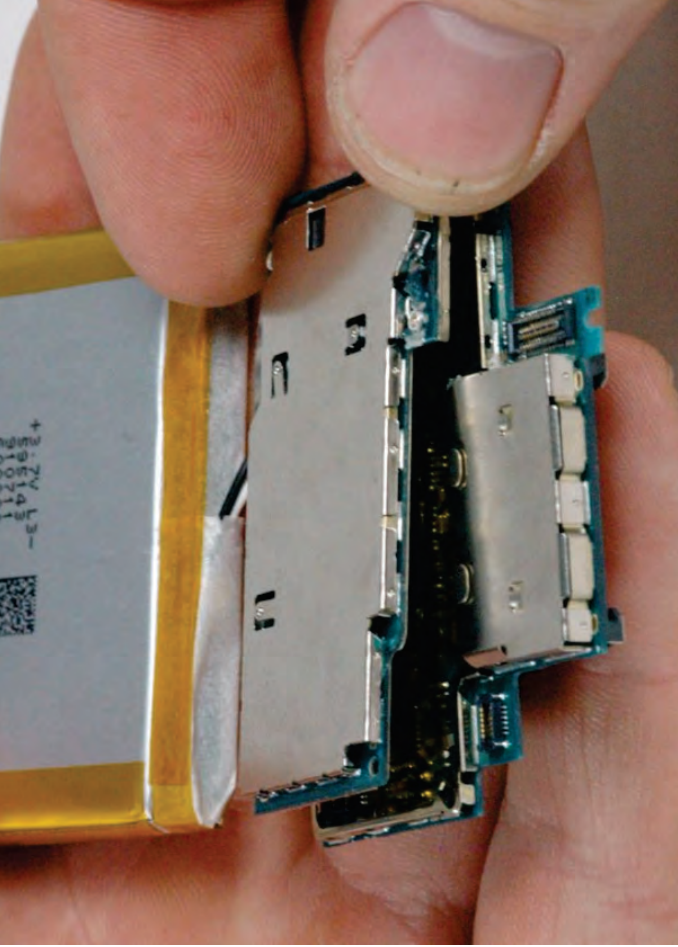
Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	<p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>Apple iPhone 1 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, e.g.:</p> 

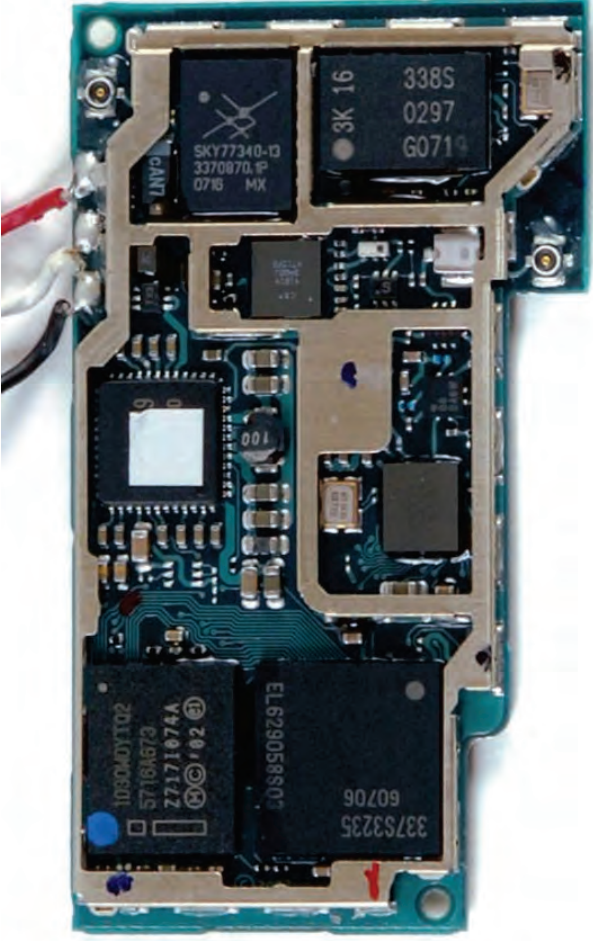
Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com



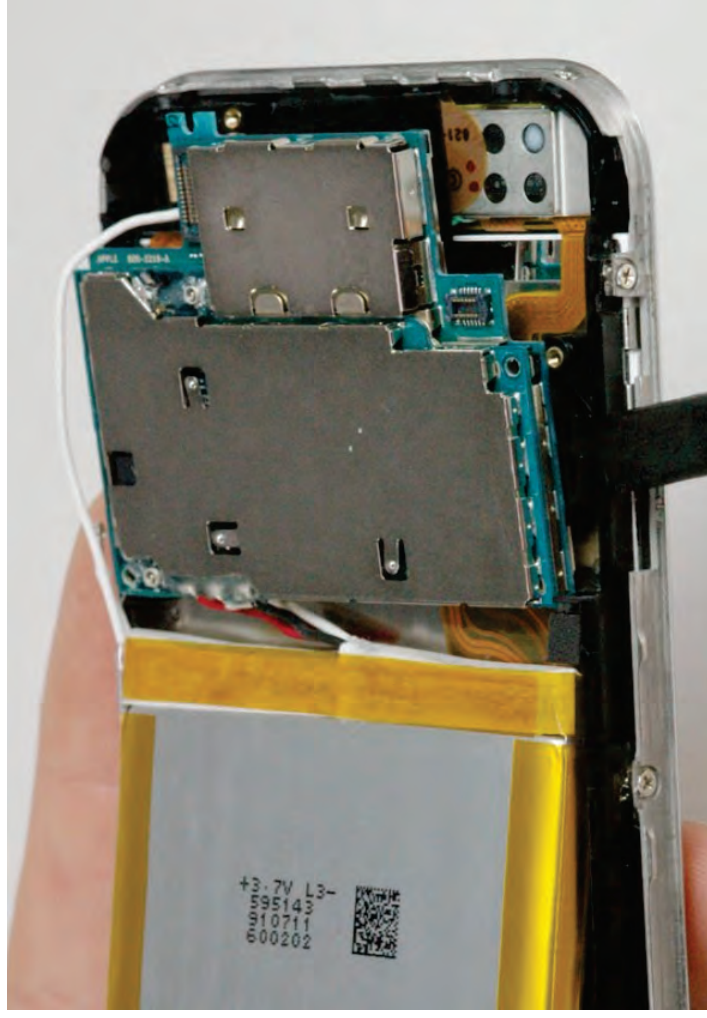
Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	 <p>https://www.ifixit.com/Teardown/iPhone+1st+Generation+Teardown/599</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom</p>	<p>Apple iPhone 1 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.</p>

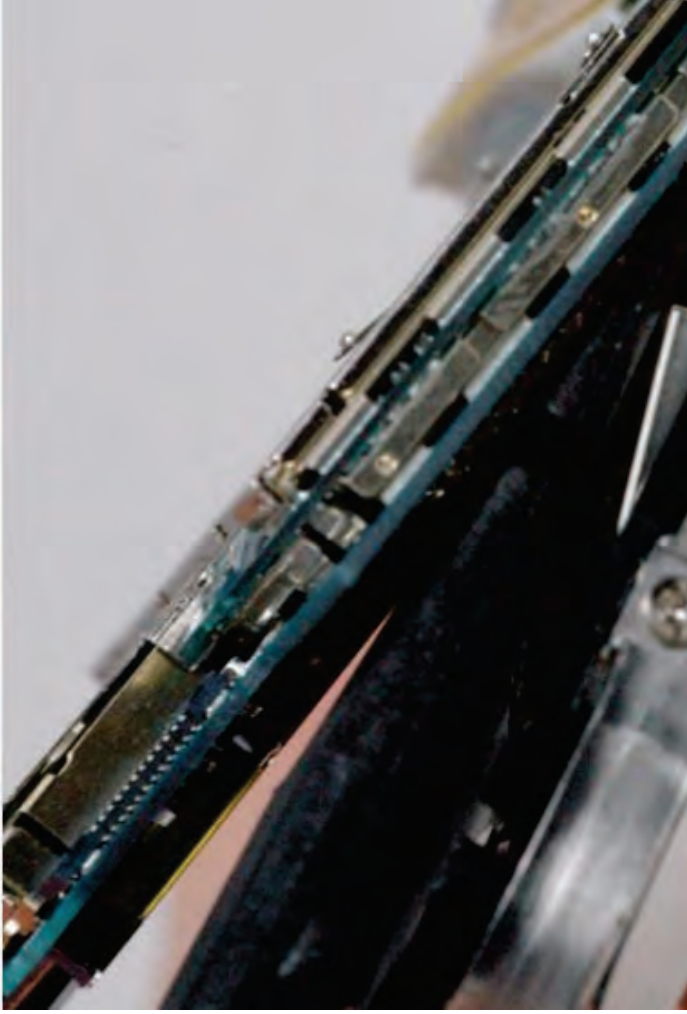
Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

package substrate and the top package substrate, wherein

See, e.g.:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

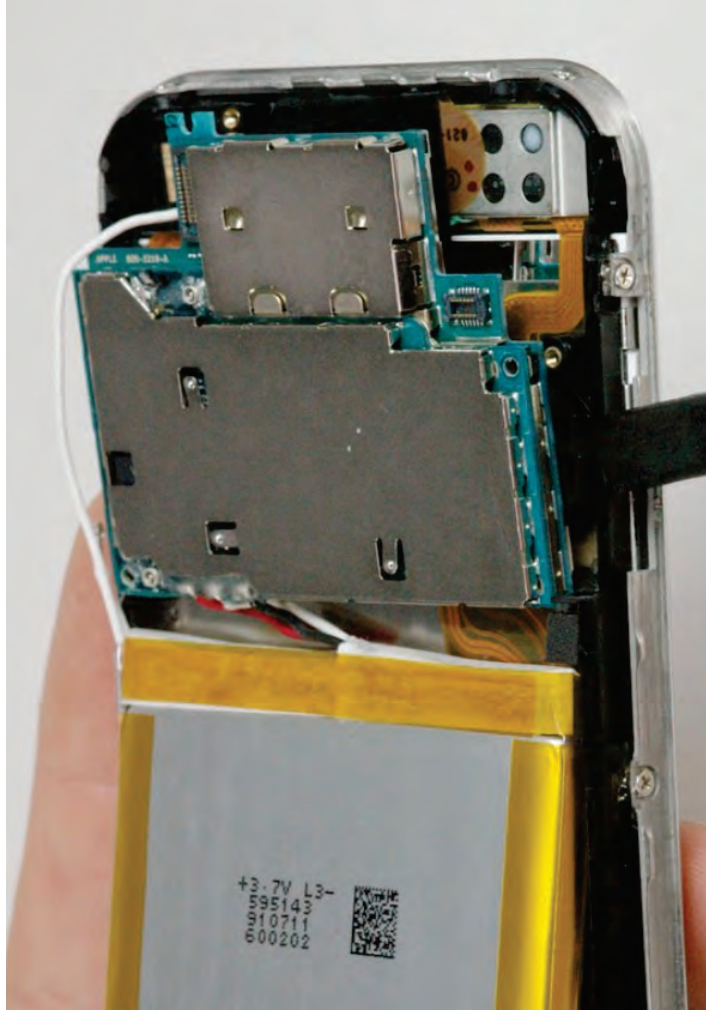
	 <p>https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

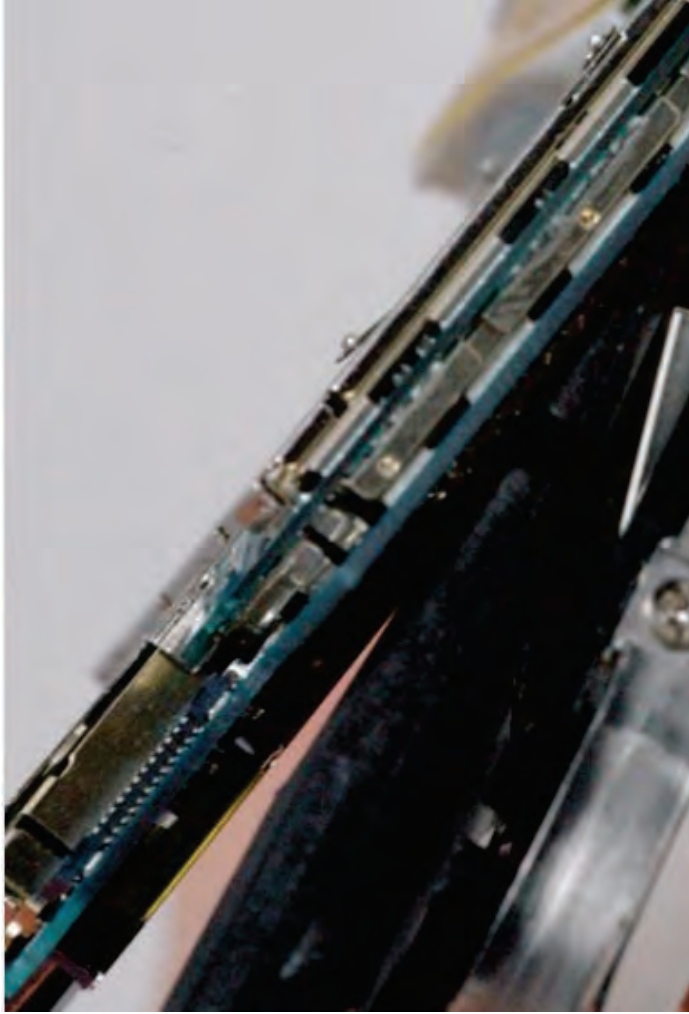
[1.D] the spacer connector comprises a core substrate;

Apple iPhone 1 discloses, either expressly or inherently, the spacer connector comprises a core substrate.

See, e.g.:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

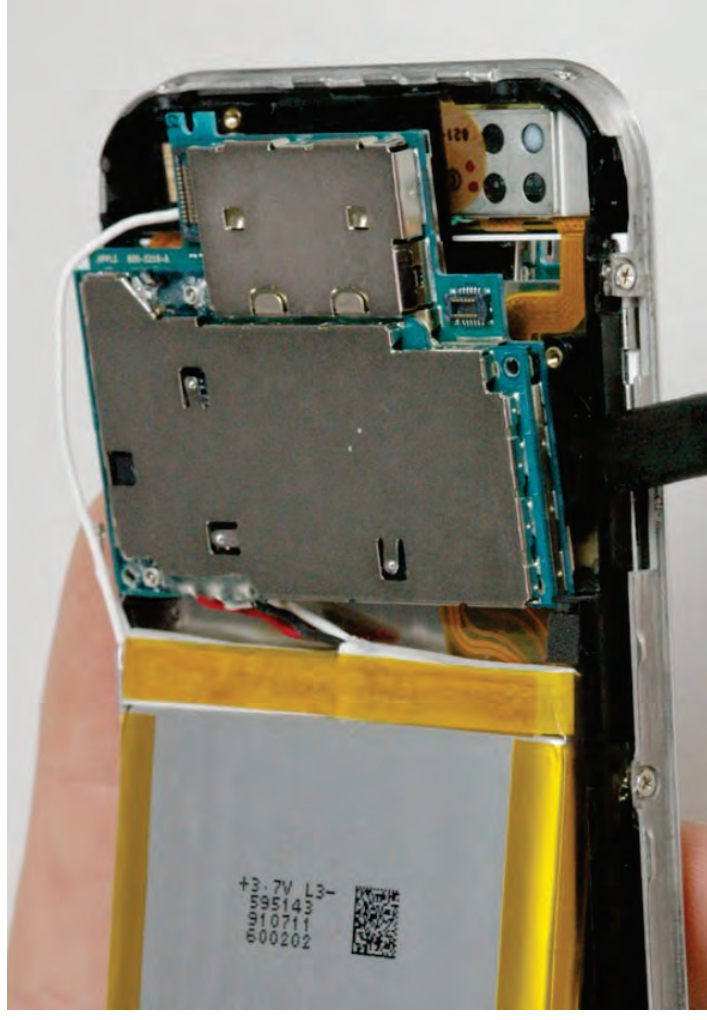
	 <p>https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

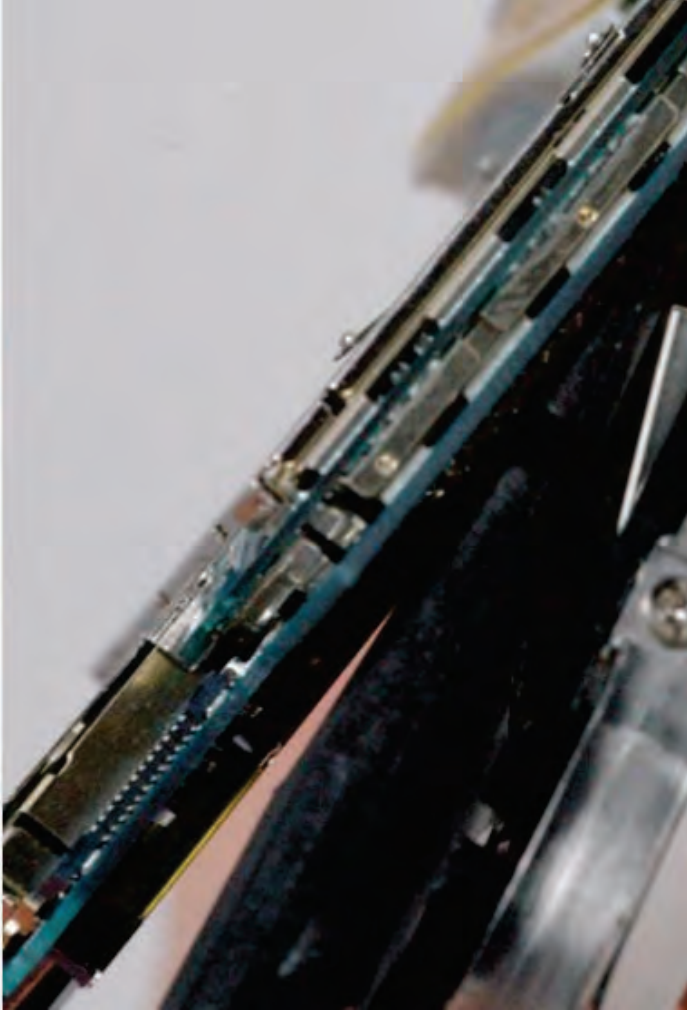
[1.E] a plurality of metal pillars, each passing through the core substrate; and

Apple iPhone 1 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.

See, e.g.:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

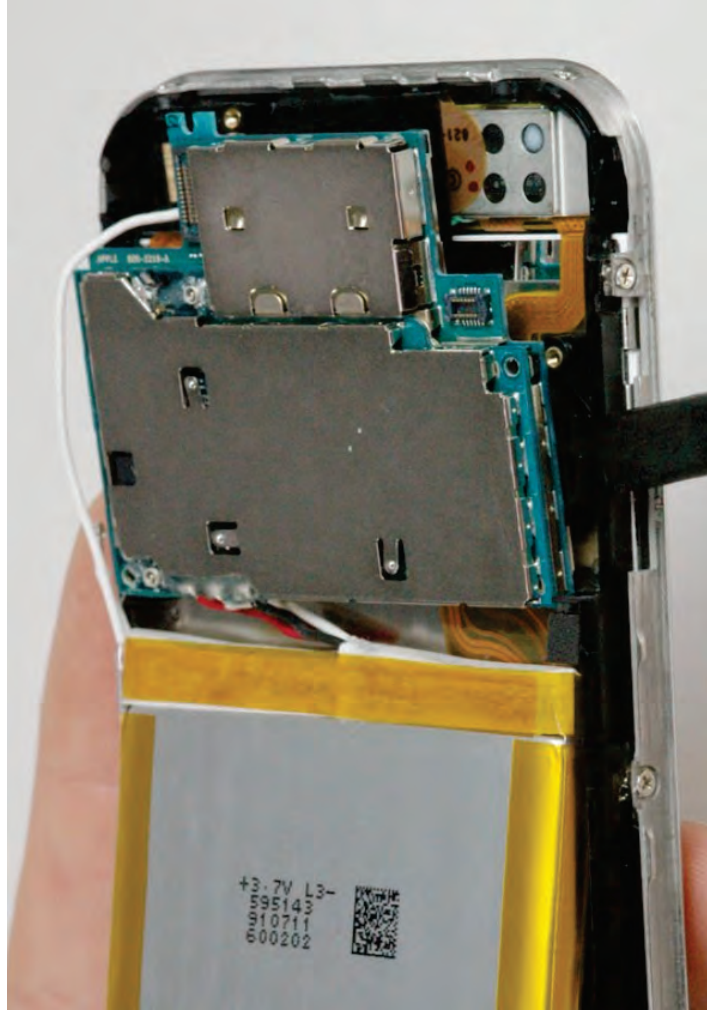
	 <p>https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

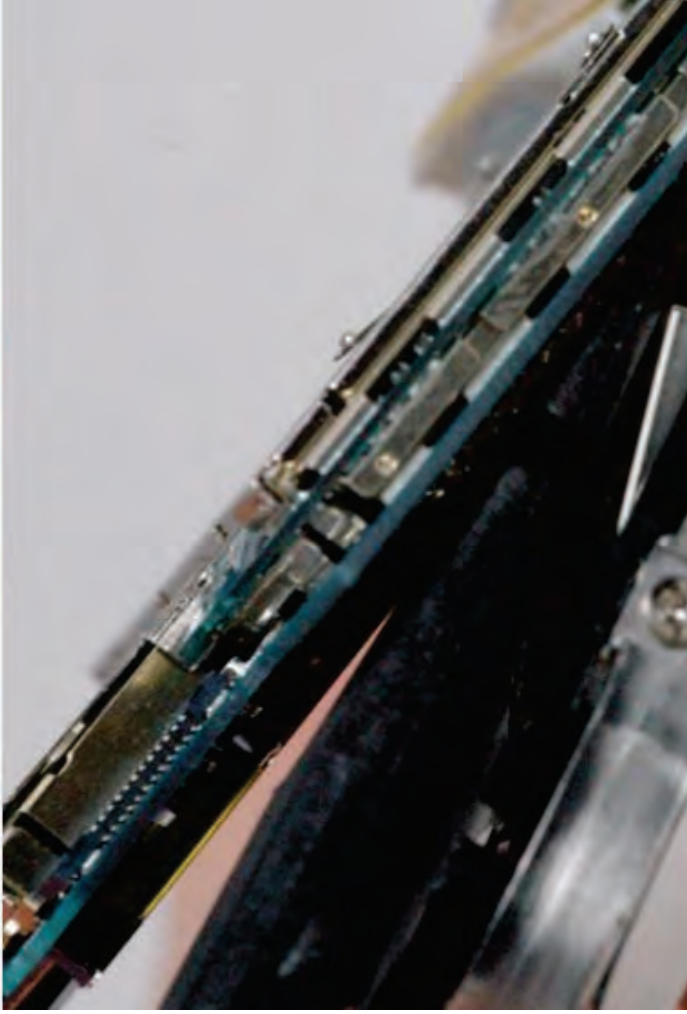
[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;

Apple iPhone 1 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.

See, e.g.:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

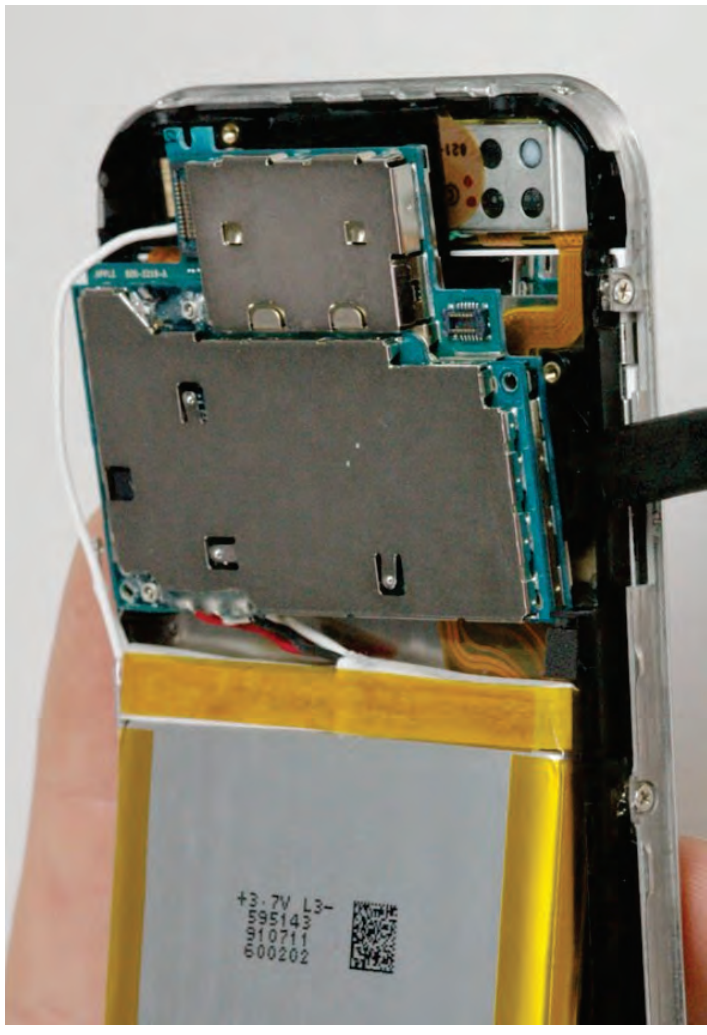
	 <p>https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

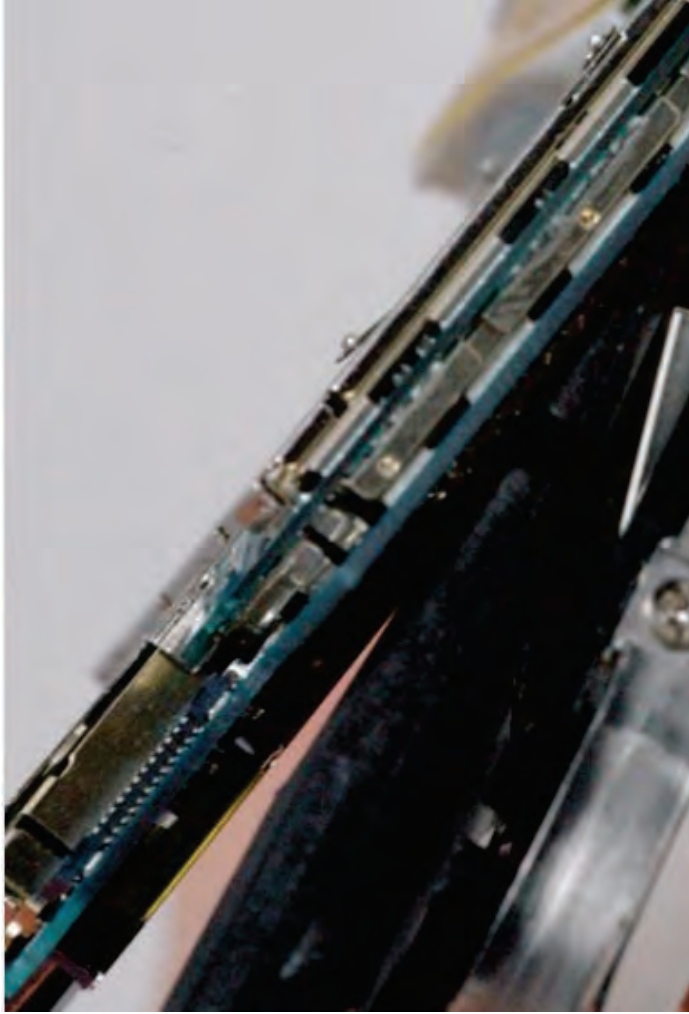
[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,

Apple iPhone 1 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.

See, e.g.:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

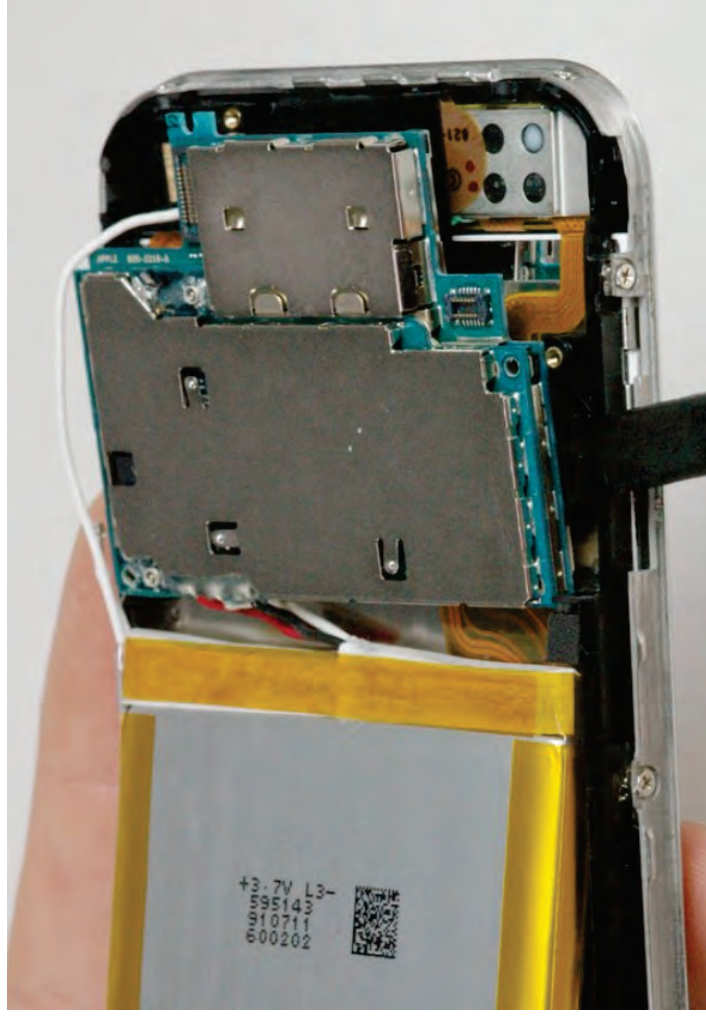
	 <p>https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

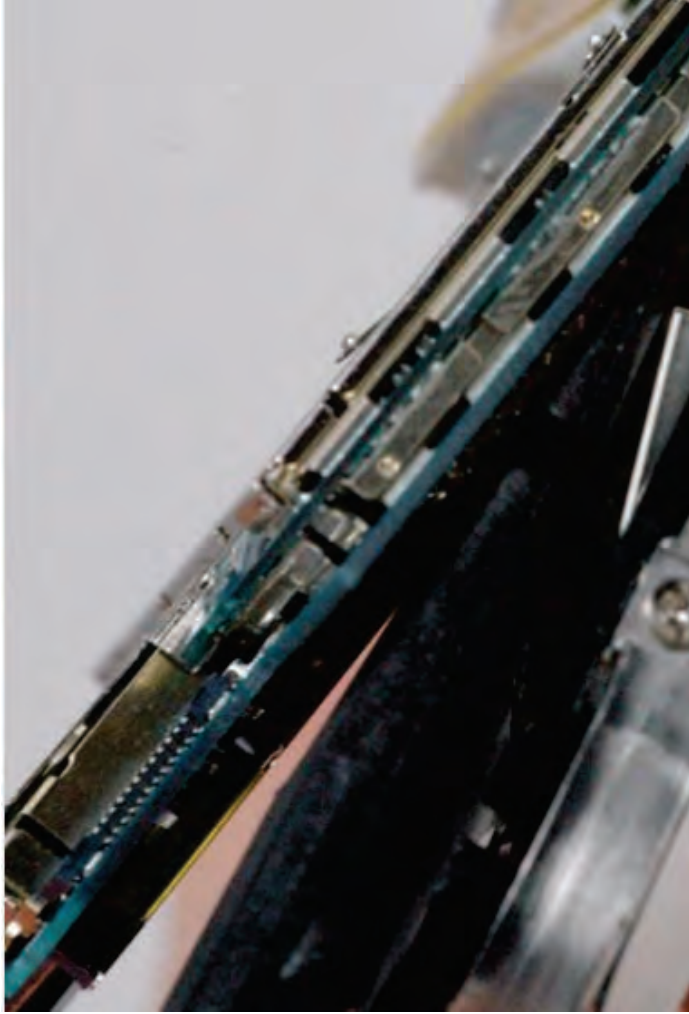
[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,

Apple iPhone 1 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.

See, e.g.:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

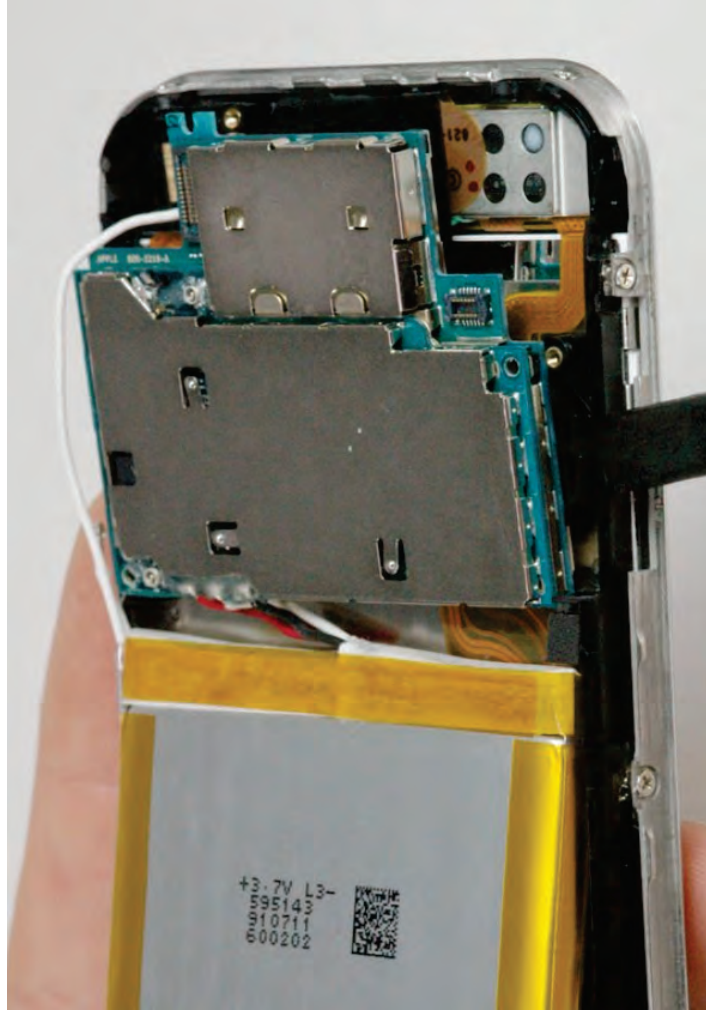
	 <p>https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

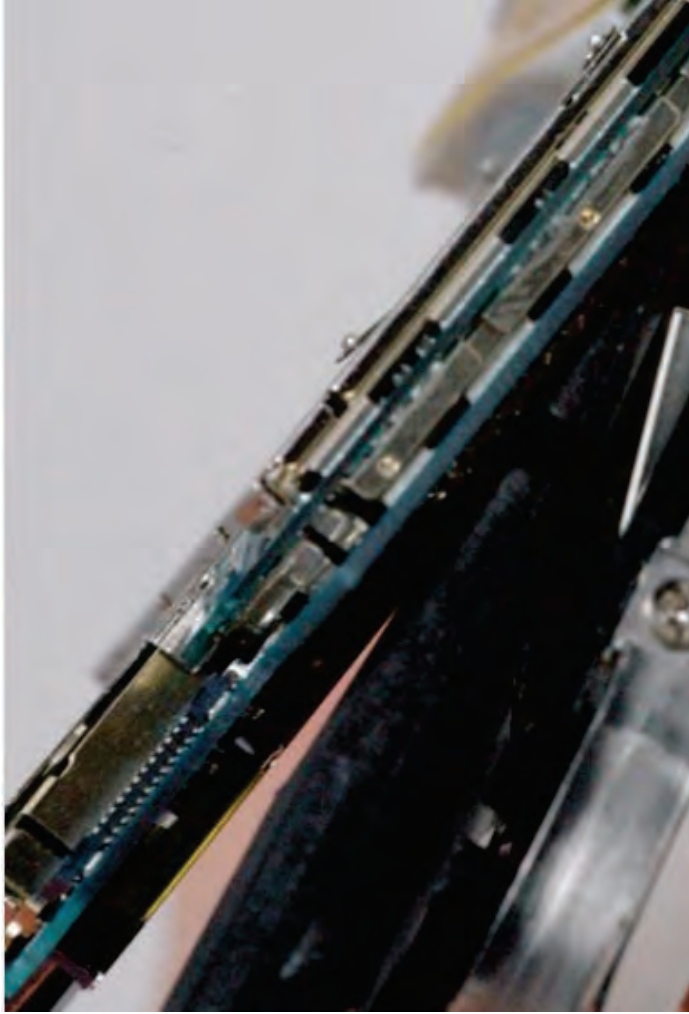
[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and

Apple iPhone 1 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.

See, e.g.:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

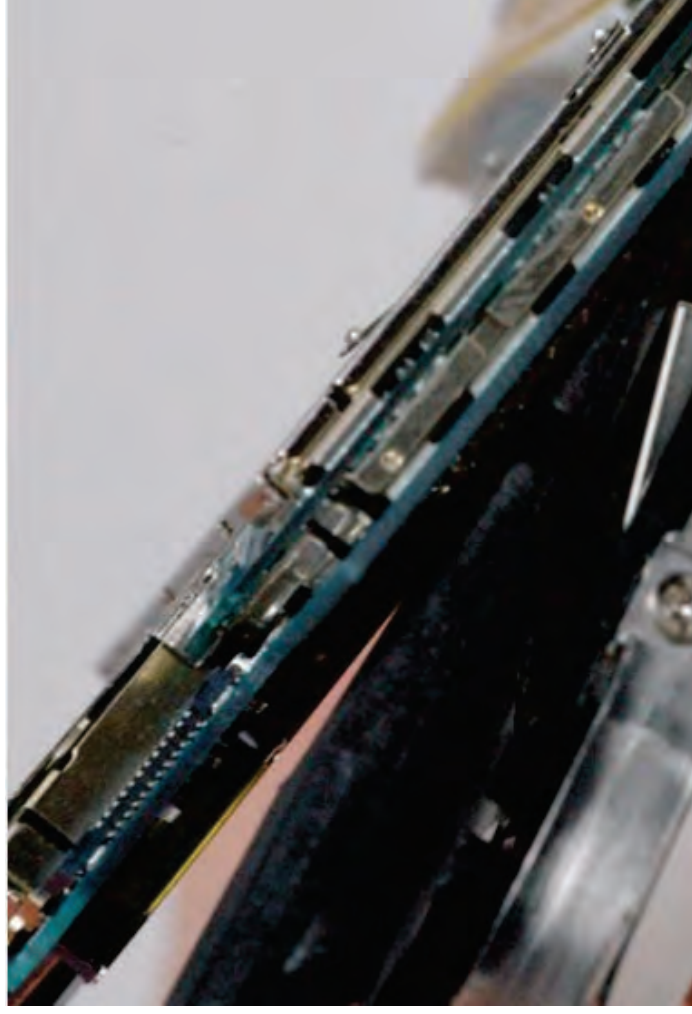
	 <p>https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

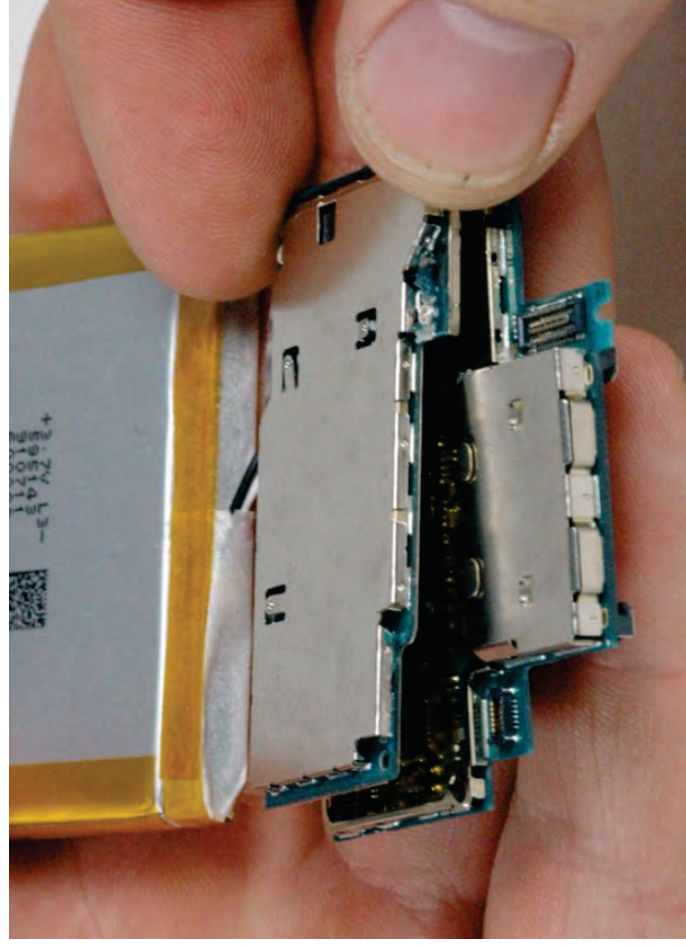
[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and

Apple iPhone 1 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.

See, *e.g.*:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

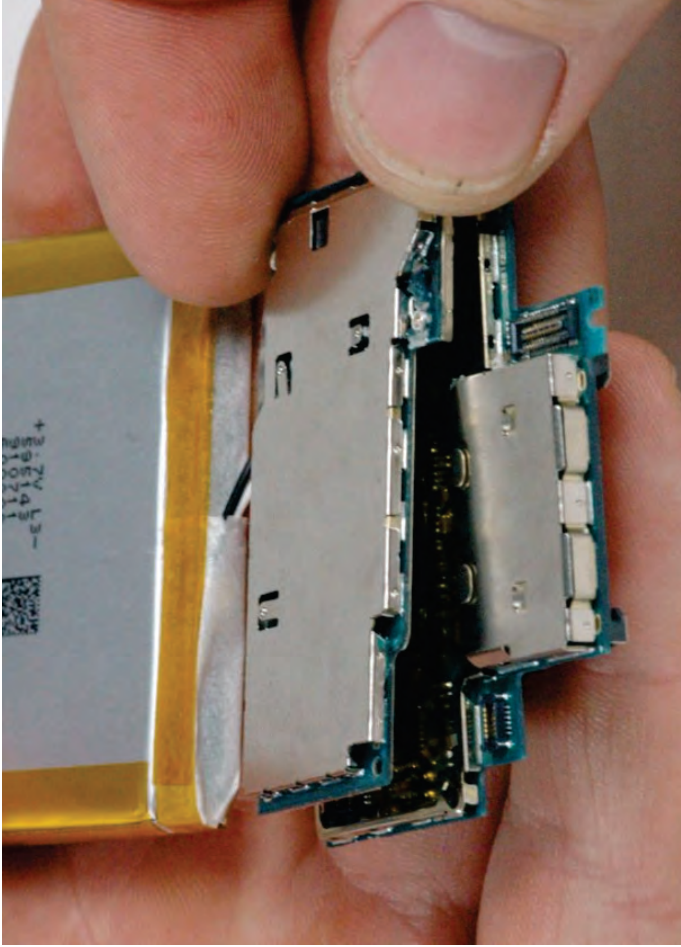


“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

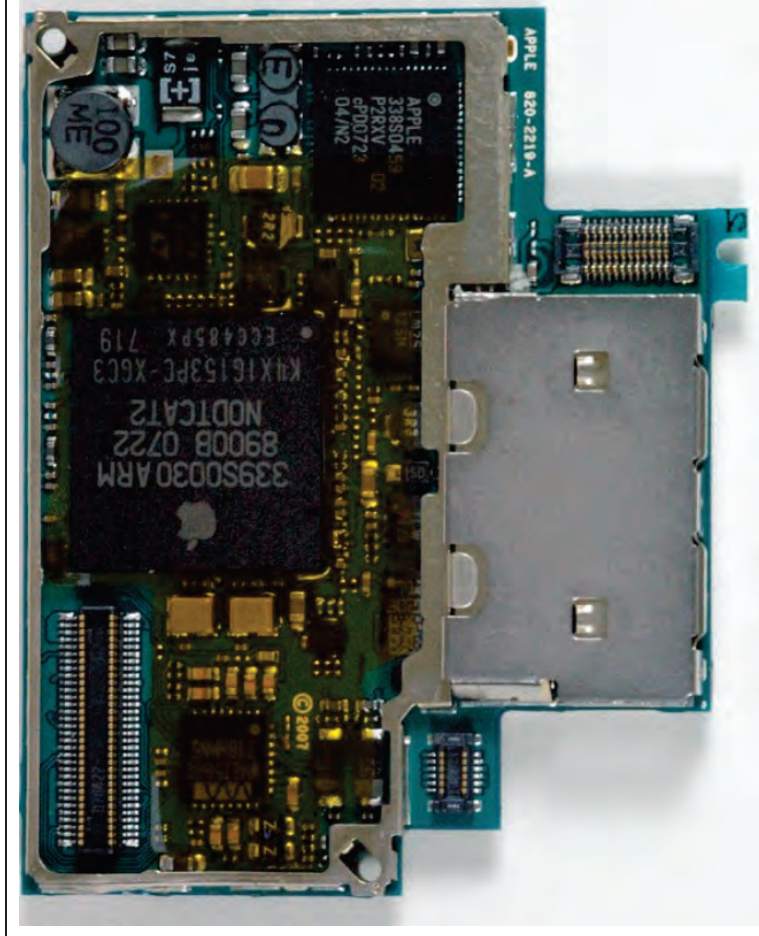
https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com

To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	<p>(i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Apple iPhone 1 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate.</p> <p>See, e.g.:</p> 

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



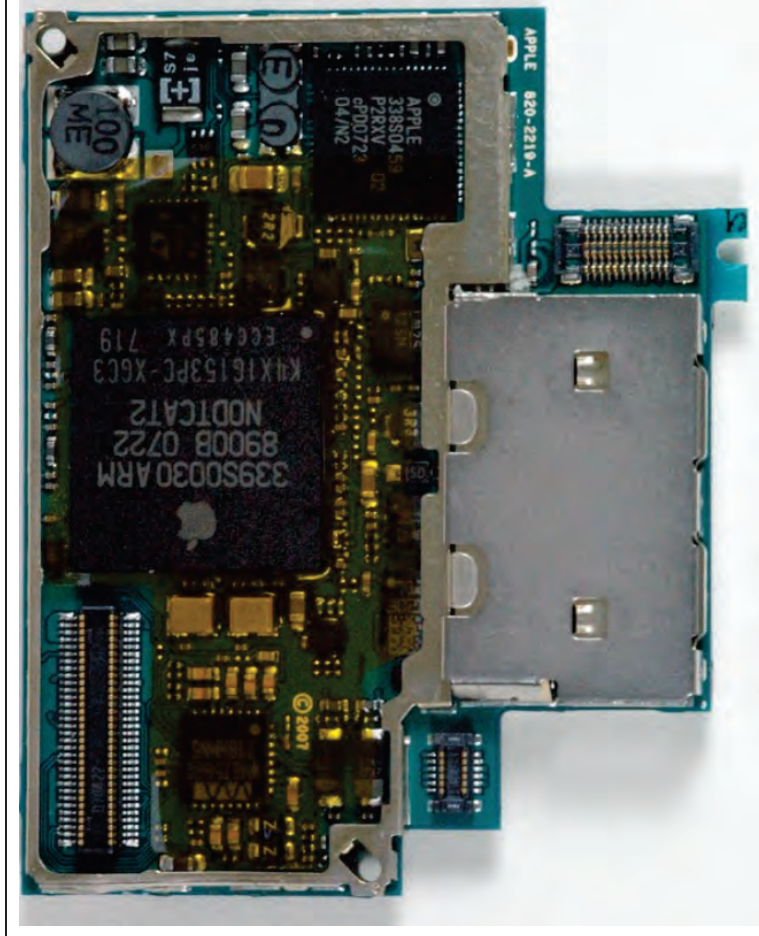
“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

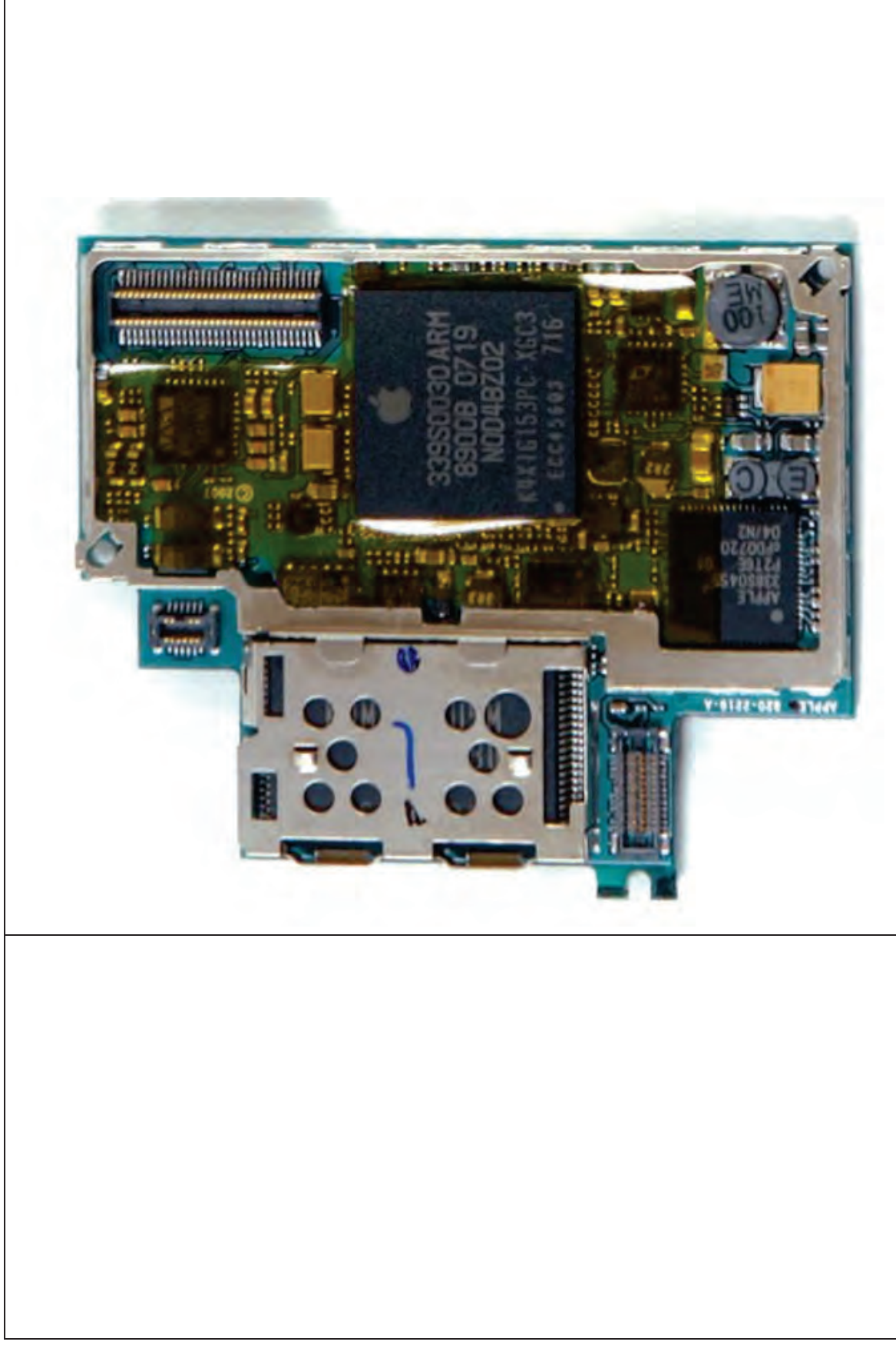
	<p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Apple iPhone 1 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

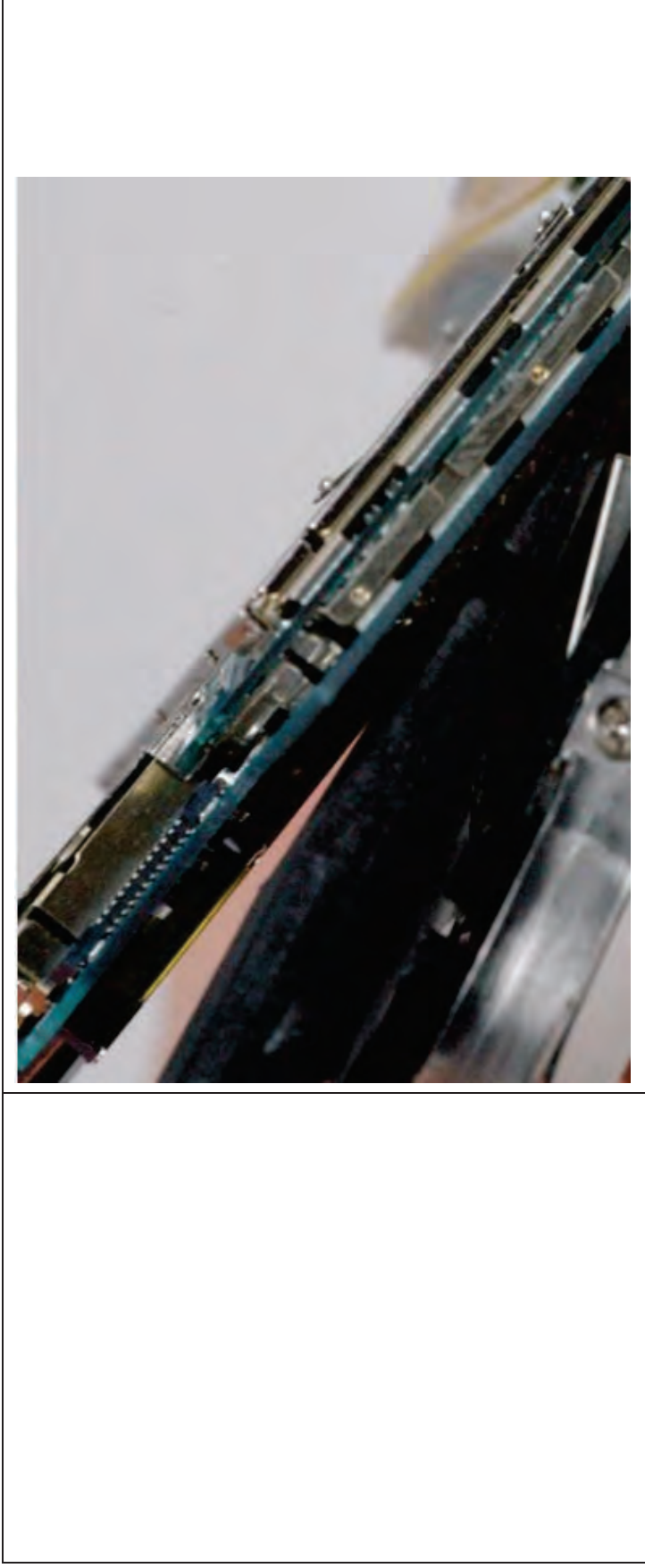
https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com



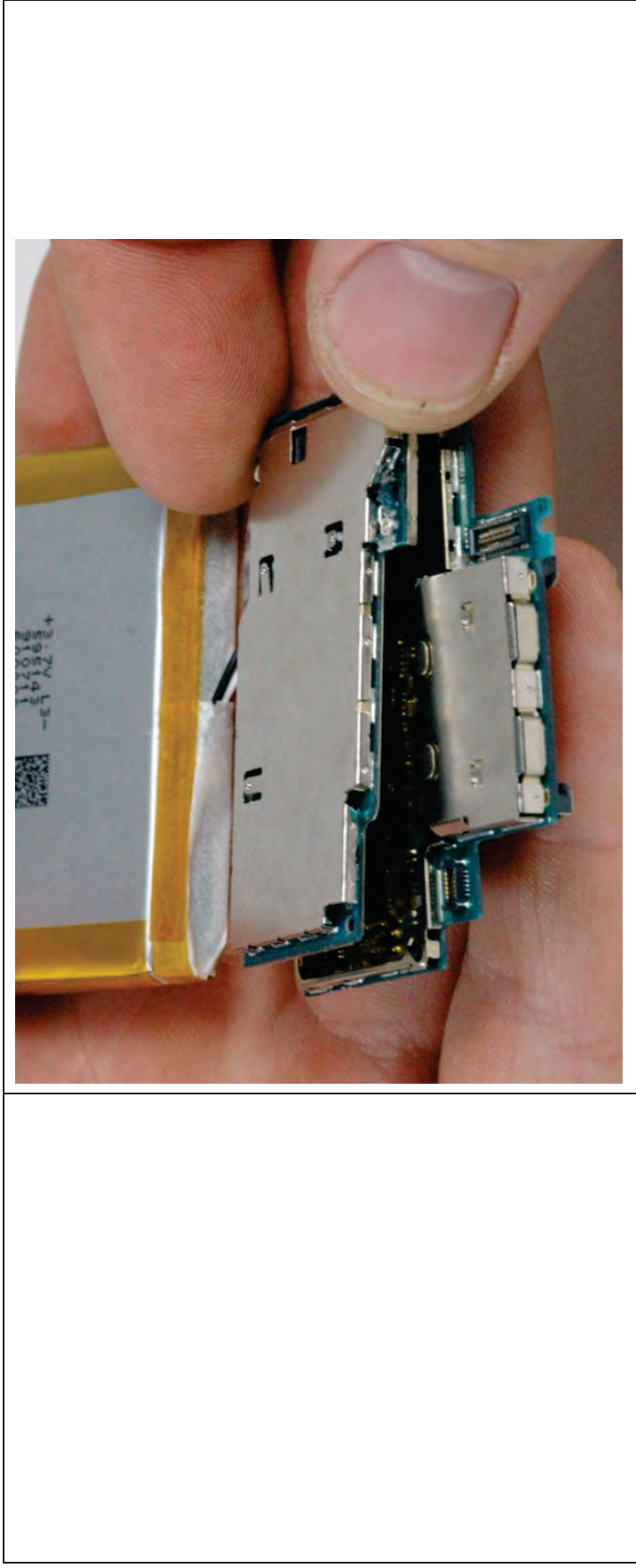
Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	<p>“Samsung chip underneath the metal shield on the left side of the board on the left. Ours reads K9MCGD8U5M. The 4 GB model that Think Secret took apart had K9HBG08U1M on it, which is a 4 GB chip</p> <p>Samsung memory stacked with a 620 MHz ARM architecture processor, ARM1176JZF. Could be a Samsung S3C6400. Numbers: 339S0030ARM, 8900B 0719, NOD4BZ02, K4X1G153PC-XGC3, ECC457Q3 716. The processor is likely stacked on the SDRAM, which could be two 512 Megabit chips. The processor could have H.264 and MP3 hardware decoding built in.</p> <p>The chip above the ARM is a Wolfson audio chip. Part numbers WM8758BG and 73AFMN5.</p> <p>The chip underneath the ARM is a Linear Technology 4066 USB Power Li-Ion Battery Charger, which Apple uses in the iPods as well.”</p> <p>https://www.ifixit.com/Teardown/iPhone+1st+Generation+Teardown/599</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.	<p>Apple iPhone 1 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p>

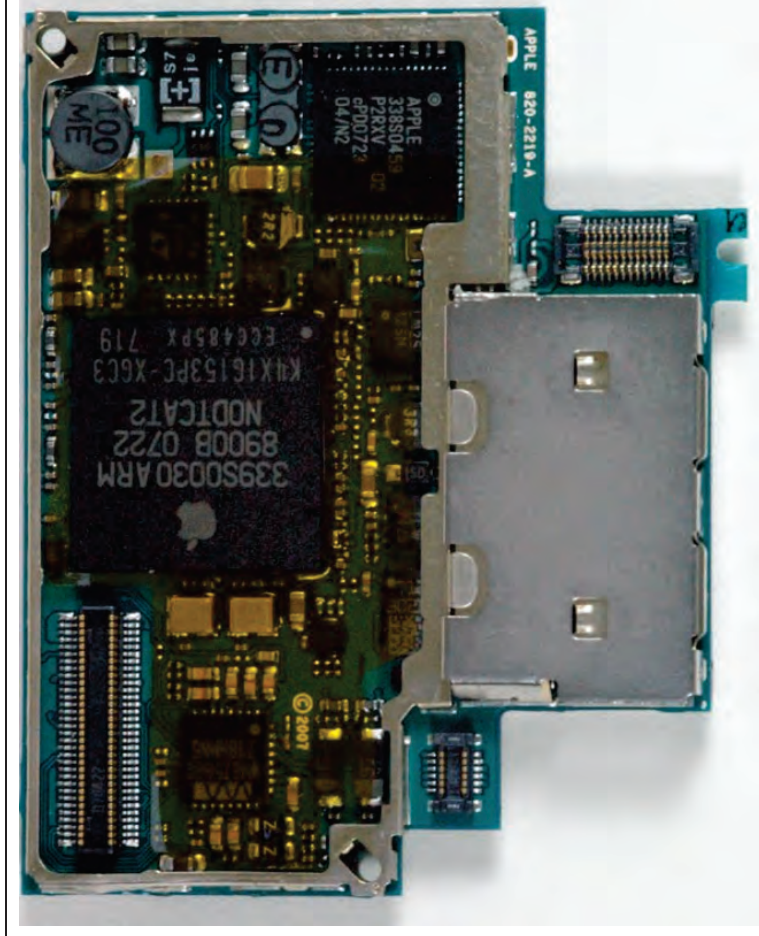
Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

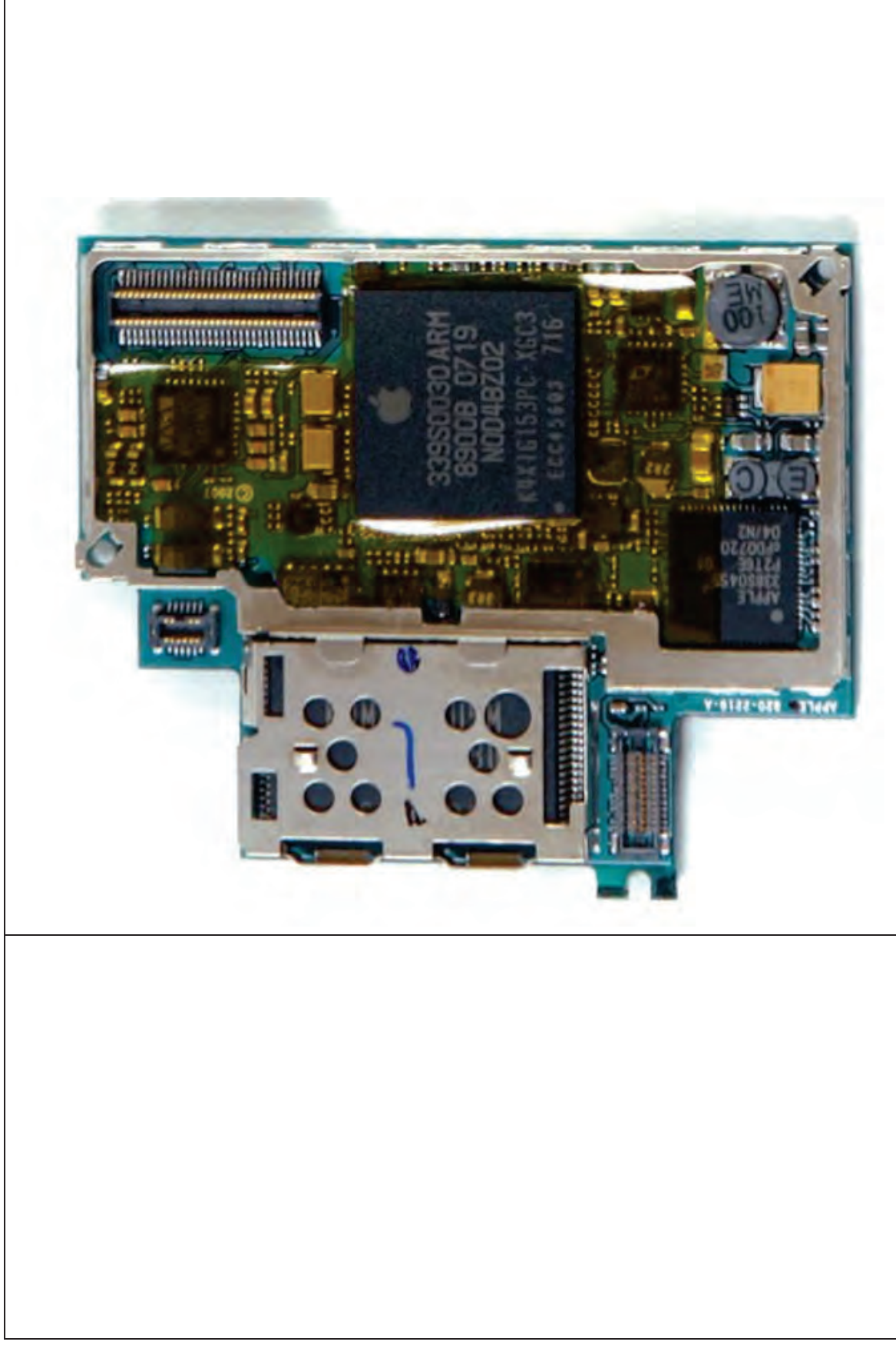


Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	<p>“Samsung chip underneath the metal shield on the left side of the board on the left. Ours reads K9MCGD8U5M. The 4 GB model that Think Secret took apart had K9HGBG08U1M on it, which is a 4 GB chip</p> <p>Samsung memory stacked with a 620 MHz ARM architecture processor, ARM1176JZF. Could be a Samsung S3C6400. Numbers: 339S0030ARM, 8900B 0719, NOD4BZ02, K4X1G153PC-XGC3, ECC457Q3 716. The processor is likely stacked on the SDRAM, which could be two 512 Megabit chips. The processor could have H.264 and MP3 hardware decoding built in.</p> <p>The chip above the ARM is a Wolfson audio chip. Part numbers WM8758BG and 73AFMN5.</p> <p>The chip underneath the ARM is a Linear Technology 4066 USB Power Li-Ion Battery Charger, which Apple uses in the iPods as well.”</p> <p>https://www.ifixit.com/Teardown/iPhone+1st+Generation+Teardown/599</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

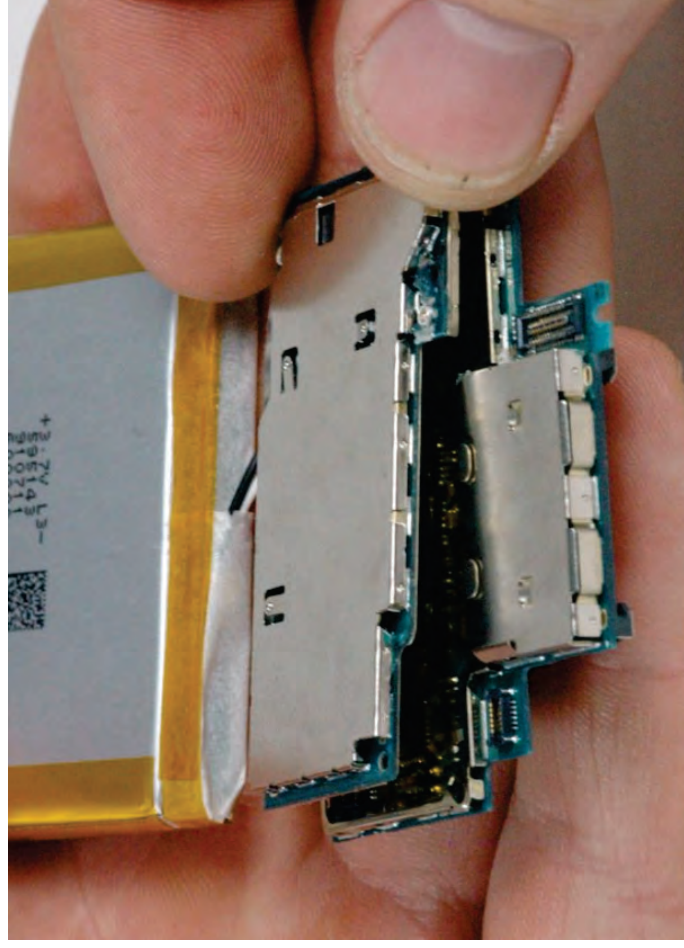
Claim 2

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced	Apple iPhone 1 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.

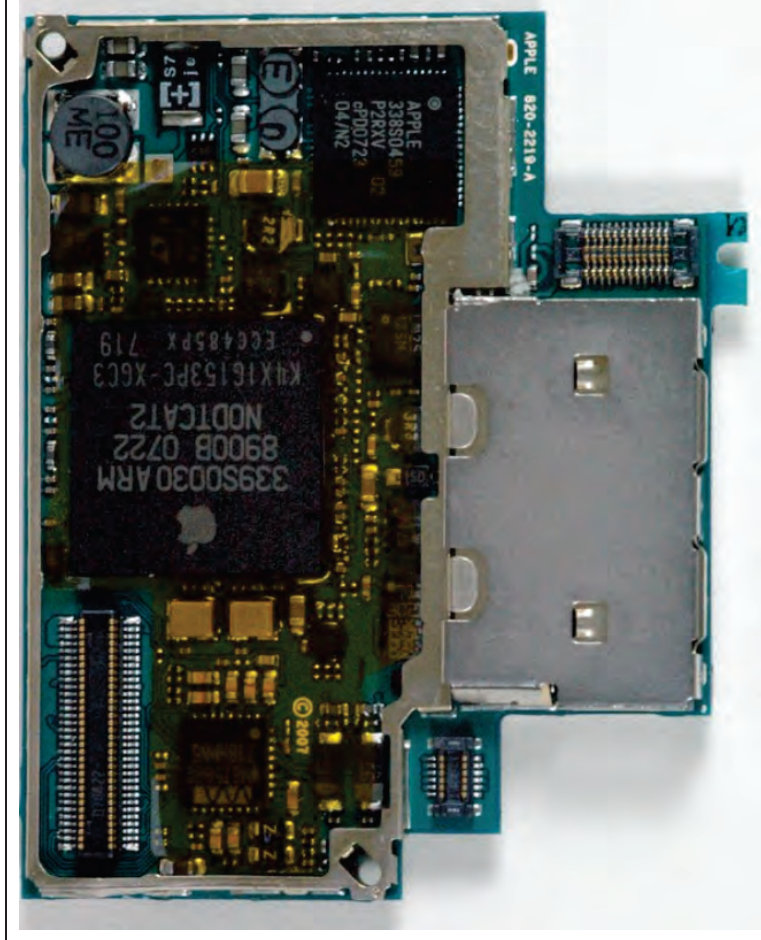
Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

downwardly from the bottom surface of
the top package substrate.

See, e.g.:

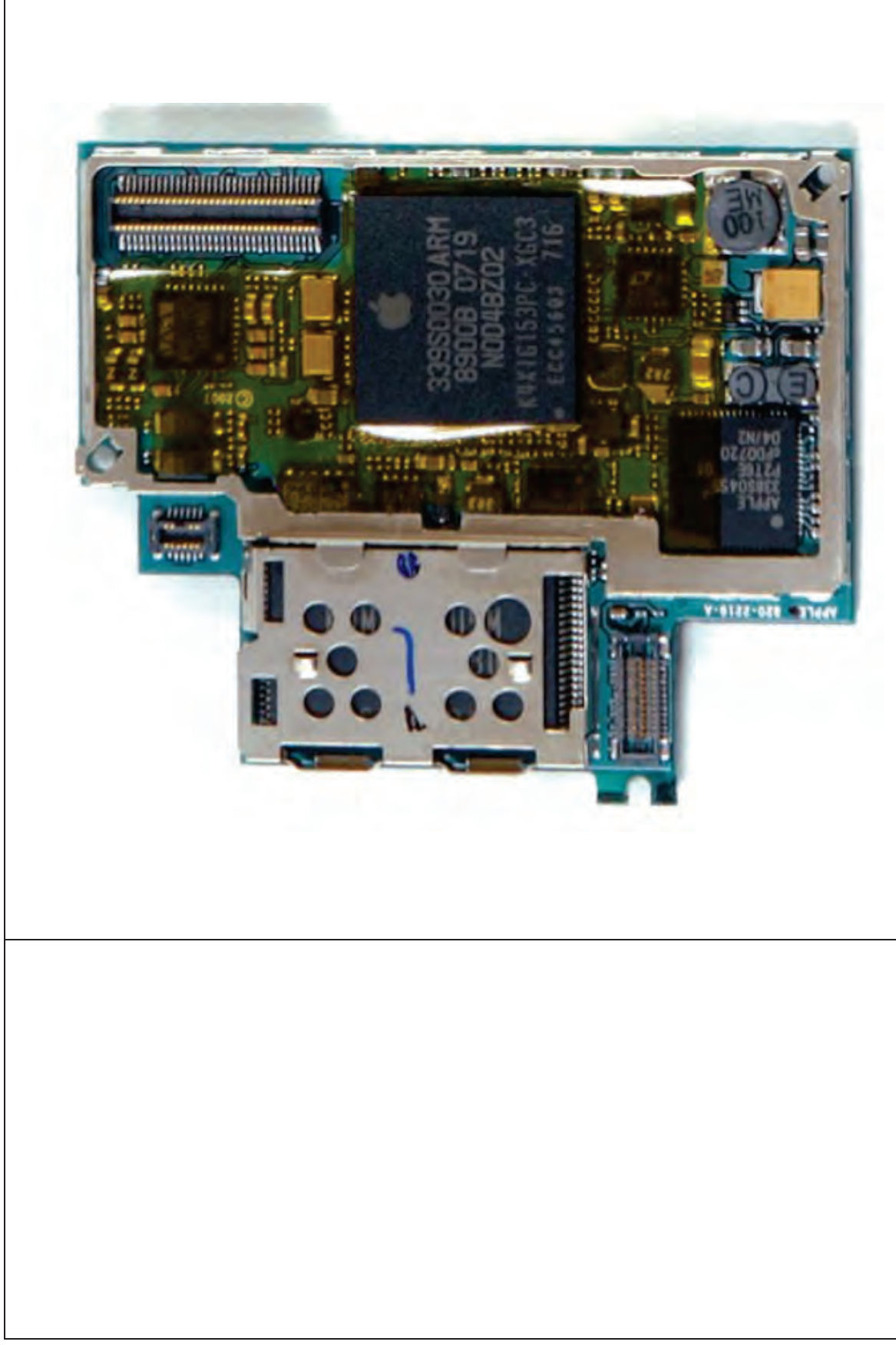


Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com



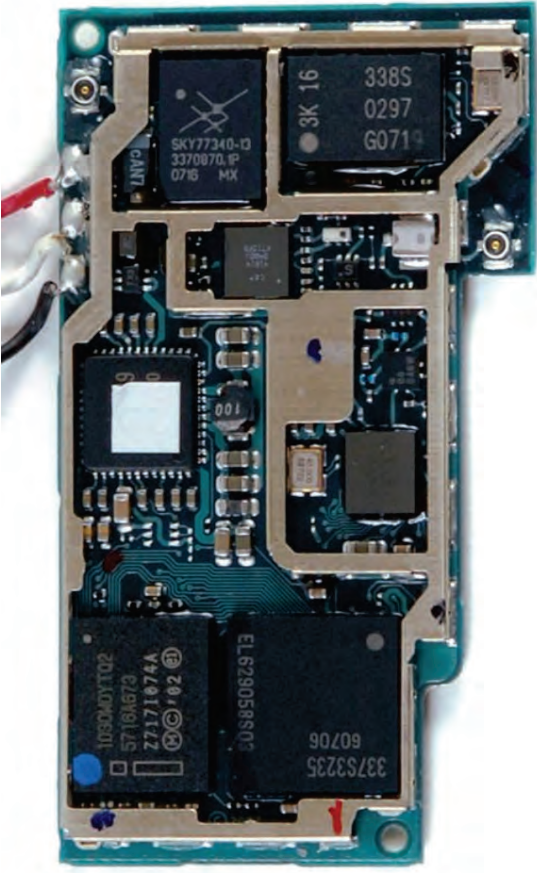
Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	<p>“Samsung chip underneath the metal shield on the left side of the board on the left. Ours reads K9MCGD8U5M. The 4 GB model that Think Secret took apart had K9HGBG08U1M on it, which is a 4 GB chip</p> <p>Samsung memory stacked with a 620 MHz ARM architecture processor, ARM1176JZF. Could be a Samsung S3C6400. Numbers: 339S0030ARM, 8900B 0719, NOD4BZ02, K4X1G153PC-XGCG3, ECC457Q3 716. The processor is likely stacked on the SDRAM, which could be two 512 Megabit chips. The processor could have H.264 and MP3 hardware decoding built in.</p> <p>The chip above the ARM is a Wolfson audio chip. Part numbers WM8758BG and 73AFMN5.</p> <p>The chip underneath the ARM is a Linear Technology 4066 USB Power Li-Ion Battery Charger, which Apple uses in the iPods as well.”</p> <p>https://www.ifixit.com/Teardown/iPhone+1st+Generation+Teardown/599</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the	Apple iPhone 1 discloses, either expressly or inherently, a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

<p>top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, e.g.:</p>  <p>“The chip on the bottom center that looks blank in our image actually has this text: MARVELL, W8686B13, 702AUUP. This is Marvell's 802.11b/g 18.4mm2 chip.</p> <p>The chip in the upper right is a Skyworks GSM/Edge Power amplifier (SKY77340).</p> <p>The silver chip to the left of the Skyworks chip reads CSR 41814 3A06U K715FB. This is a CSR BlueCore4-ROM WLCSP single chip radio and baseband IC for Bluetooth 2+EDR.</p>
--	--

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	<p>The chip covered by the white sticker in the photo has the part numbers 338S0289 and 8G60710 on it. EETimes claims this is an Infineon M1817A11.</p> <p>The chip with the blue dot on it is rumored to be an Intel Wireless Flash stacked 32 Mb NOR + 16 Mb SRAM chip. Part numbers 1030W0YTQ2, 5716A673, and Z717074A. EE Times adds the part #PF38F1030W0YTQ2.</p> <p>The chip in the lower right reads 338S 0297 G0719. Some claim this is an Apple-branded chip, but it's purpose is currently unknown.</p> <p>The chip in the lower left is an Infineon PMB8876 S-Gold 2 multimedia engine. Part numbers: 337S3235, 60708, and EL629058S03.”</p> <p>https://www.ifixit.com/Teardown/iPhone+1st+Generation+Teardown/599</p> <p>To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4

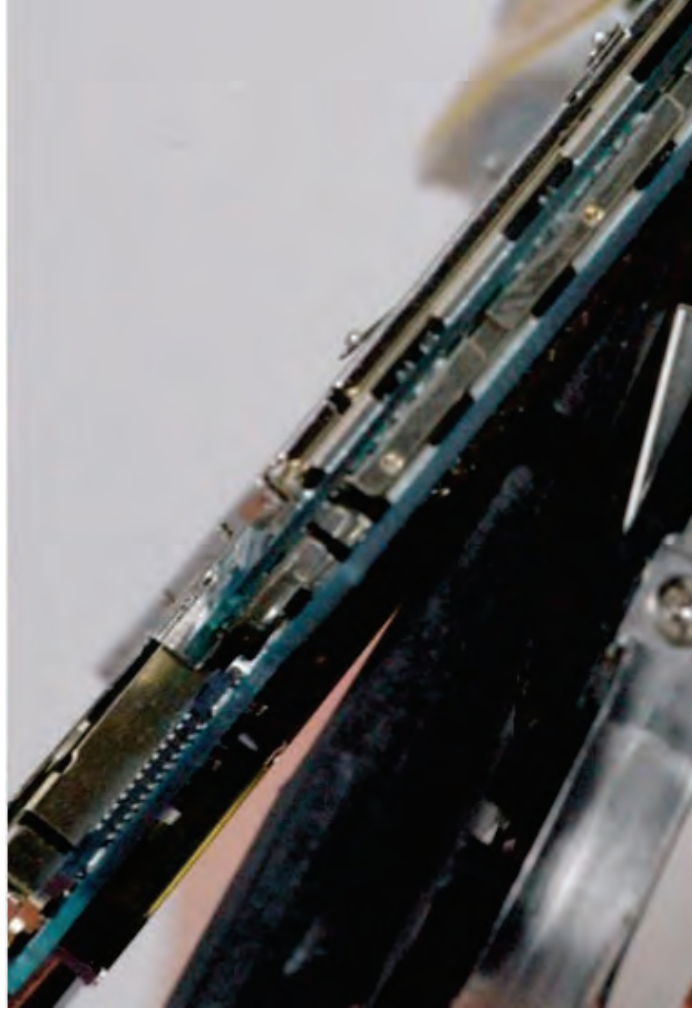
Claim Limitation	Disclosure
[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the	Apple iPhone 1 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

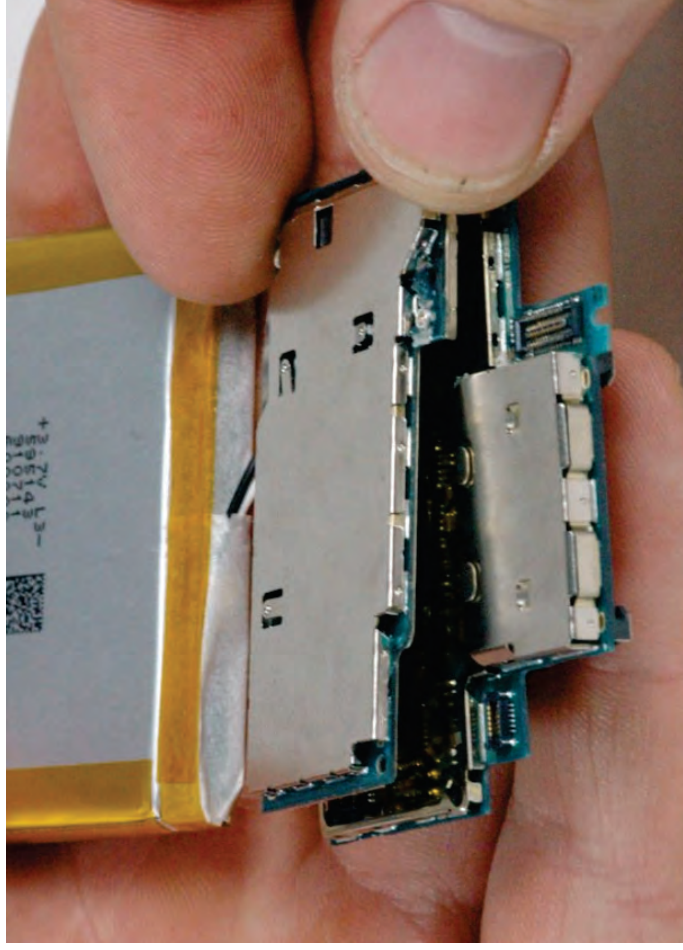
metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

See, e.g.:



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

--	--



“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com

To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	(i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

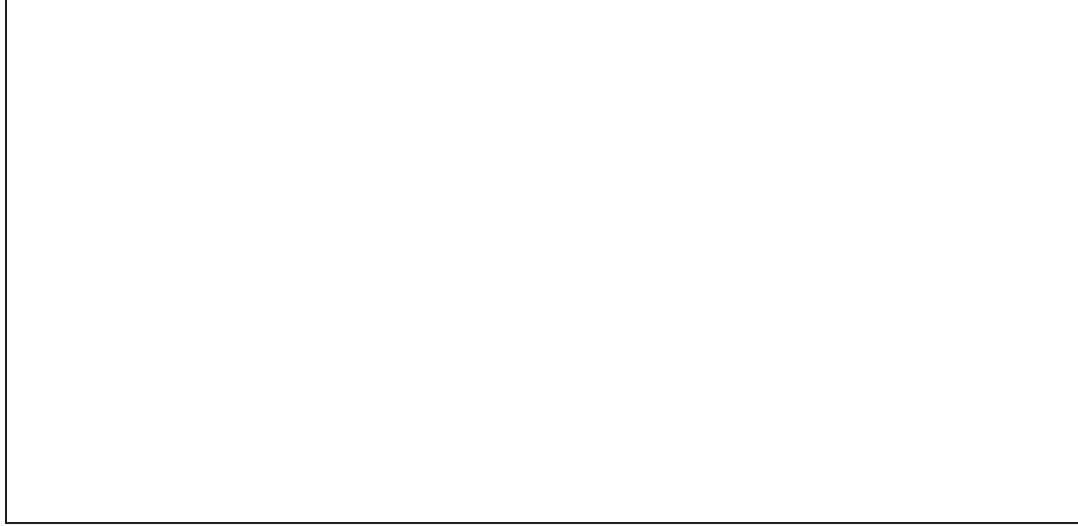
Claim 6

Claim Limitation	Disclosure
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector. <i>See, e.g.:</i>	Apple iPhone 1 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector. <i>See, e.g.:</i>

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com

To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	(i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

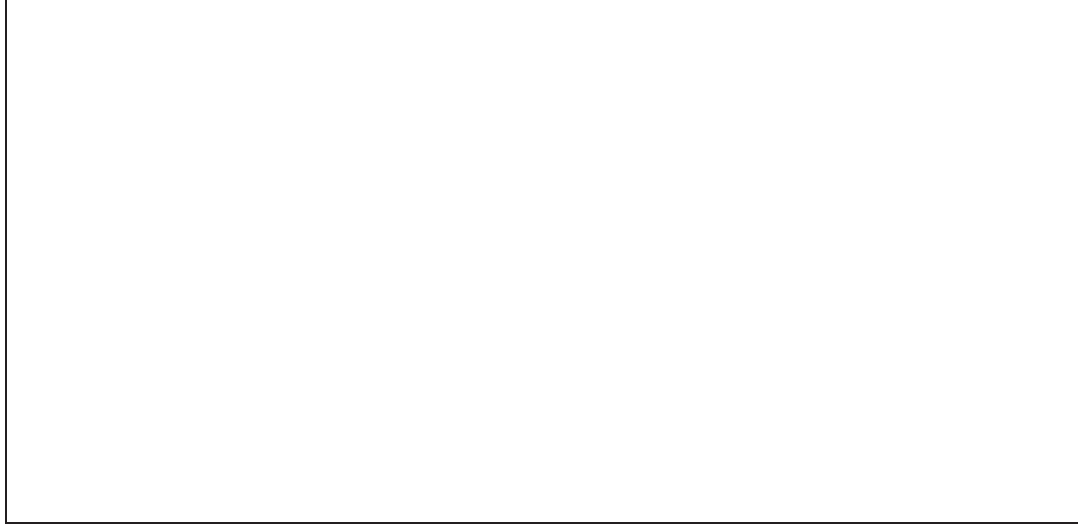
Claim 9

Claim Limitation	Disclosure
[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.	Apple iPhone 1 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector. <i>See, e.g.:</i>

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1



“There are two stacked circuit boards on the iPhone. The communications board is on the top, and the logic board is located on the bottom.”

https://www.ifixit.com/Guide/iPhone+1st+Generation+Logic+Board+Replacement/447?utm_source=chatgpt.com

To the extent Plaintiff contends that Apple iPhone 1 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with

Appendix A-50 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 1

	(i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

E.D. Tex. Case No. 2:25-cv-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

The Through Mold Via Package-on-Package (hereinafter “TMV PoP”) was in public use, on sale (including sold to customers and potential customers), and/or otherwise available to the public by Amkor Technology, Inc. at least by 2011.¹ TMV PoP anticipates and/or renders obvious all Asserted Claims² of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.³ TMV PoP, or the written materials describing it, excerpted below, is prior art to the ’202 Patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within TMV PoP, or otherwise rendered obvious by disclosures and teachings of TMV PoP, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that TMV PoP does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of TMV PoP with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 Patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends

¹ See, e.g., <https://ir.amkor.com/news-releases/news-release-details/sales-amkor-technologies-next-generation-through-mold-package>; <https://web.archive.org/web/20110911192846/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

² As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

³ To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

is not fully disclosed by TMV PoP, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that TMV PoP “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to TMV PoP or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding TMV PoP set forth in this chart.

Claim 1

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, TMV PoP discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>

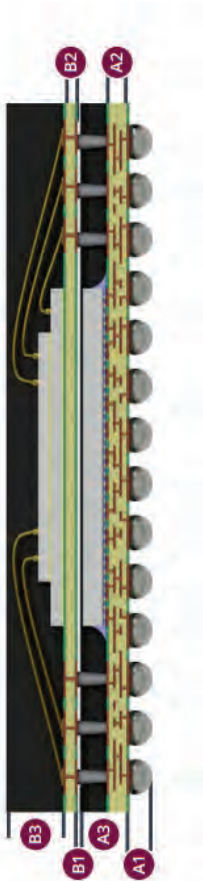
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

TMV® PoP Overall Stack Up Table

Symbol	Unit	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150
A2 (4L laminate)	mm	0.220	0.300	0.260
A3 (Mold cap)	mm	0.230	0.280	0.250
B1 (Stacked gap)	mm	0.020	0.080	0.050
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Package Height	mm	1.140	1.340	1.240

<https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

Cross Section TMV® PoP



The diagram shows a cross-section of a multi-layered structure. From bottom to top, the layers are labeled A1, A2, A3, B1, B2, and B3. A1 is the base layer, followed by A2, A3, B1, B2, and B3. The layers are shown with various patterns and colors, indicating different materials or structures. A1 is a solid dark layer, A2 is a patterned layer, A3 is a thin layer, B1 is a patterned layer, B2 is a thin layer, and B3 is a thin layer. The layers are stacked on top of each other, with A1 at the bottom and B3 at the top.

TMV® Overall Stack Up Table (mm)

Symbol	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150
A2 (4L Laminates)	0.220	0.300	0.260
A3 (Mold Cap)	0.230	0.280	0.250
B1 (Stacked Gap)	0.020	0.080	0.050
B2 (2L Laminates)	0.100	0.160	0.130
B3 (Mold Cap)	0.370	0.430	0.400
Overall Package Height	1.140	1.340	1.240

https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>																																								
<p>[1.A] a bottom package substrate;</p>	<p>TMV PoP discloses, either expressly or inherently, a bottom package substrate.</p> <p>See, e.g.:</p> <div><p>TMV® PoP Overall Stack Up Table</p><table><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div> <p>https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename</p>	Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340	1.240
Symbol	Unit	Min	Max	Nom																																					
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																					
A2 (4L laminate)	mm	0.220	0.300	0.260																																					
A3 (Mold cap)	mm	0.230	0.280	0.250																																					
B1 (Stacked gap)	mm	0.020	0.080	0.050																																					
B2 (2L laminate)	mm	0.100	0.160	0.130																																					
B3 (Mold cap)	mm	0.370	0.430	0.400																																					
Overall Package Height	mm	1.140	1.340	1.240																																					

Cross Section TMV® PoP

A detailed cross-sectional diagram of a TMV PoP assembly. The diagram shows a stack of materials with various layers and components. Labels A1, A2, A3, B1, B2, and B3 are placed at the top of the diagram, corresponding to specific layers. A1 is the bottom-most layer, followed by A2, A3, B1, B2, and B3 at the top. The diagram illustrates the internal structure, including a central core, a mold cap, and a stacked gap. Dimensions are indicated by arrows and numbers, showing the thickness of each layer and the overall package height.

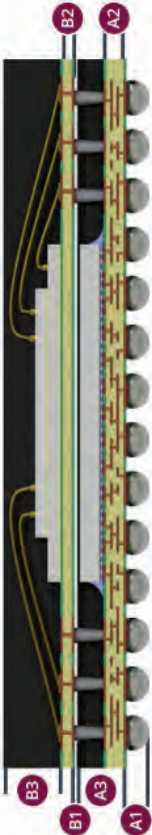
TMV® Overall Stack Up Table (mm)

Symbol	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150
A2 (4L Laminate)	0.220	0.300	0.260
A3 (Mold Cap)	0.230	0.280	0.250
B1 (Stacked Gap)	0.020	0.080	0.050
B2 (2L Laminate)	0.100	0.160	0.130
B3 (Mold Cap)	0.370	0.430	0.400
Overall Package Height	1.140	1.340	1.240

https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>																																								
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>TMV PoP discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, e.g.:</p> <div><p style="text-align: center;">TMV® PoP Overall Stack Up Table</p><table><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div> <p>https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename</p>	Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340	1.240
Symbol	Unit	Min	Max	Nom																																					
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																					
A2 (4L laminate)	mm	0.220	0.300	0.260																																					
A3 (Mold cap)	mm	0.230	0.280	0.250																																					
B1 (Stacked gap)	mm	0.020	0.080	0.050																																					
B2 (2L laminate)	mm	0.100	0.160	0.130																																					
B3 (Mold cap)	mm	0.370	0.430	0.400																																					
Overall Package Height	mm	1.140	1.340	1.240																																					

<div><div>Cross Section TMV® PoP</div><div></div></div>		<div><div>TMV® Overall Stack Up Table (mm)</div><table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminate)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminate)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminate)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminate)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminate)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminate)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>TMV PoP discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

			
		TMV® PoP Overall Stack Up Table	
Symbol	Unit	Min	Max
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200
A2 (4L laminate)	mm	0.220	0.300
A3 (Mold cap)	mm	0.230	0.280
B1 (Stacked gap)	mm	0.020	0.080
B2 (2L laminate)	mm	0.100	0.160
B3 (Mold cap)	mm	0.370	0.430
Overall Package Height	mm	1.140	1.340
			Nom
			0.150
			0.260
			0.250
			0.050
			0.130
			0.400
			1.240

<https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

Cross Section TMV® PoP

The diagram shows a cross-section of a multi-layered structure. From bottom to top, the layers are labeled A1, A2, A3, B1, B2, and B3. Layer A1 is the base, followed by A2, A3, B1, B2, and B3. The layers are shown with different colors and textures to represent different materials. A1 is a dark grey/black layer. A2 is a light grey layer. A3 is a yellow layer. B1 is a dark grey/black layer. B2 is a light grey layer. B3 is a yellow layer. The layers are stacked on top of each other, with some gaps between them. The overall structure is shown in a perspective view, with the layers extending into the distance.

TMV® Overall Stack Up Table (mm)

Symbol	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150
A2 (4L Laminare)	0.220	0.300	0.260
A3 (Mold Cap)	0.230	0.280	0.250
B1 (Stacked Gap)	0.020	0.080	0.050
B2 (2L Laminare)	0.100	0.160	0.130
B3 (Mold Cap)	0.370	0.430	0.400
Overall Package Height	1.140	1.340	1.240

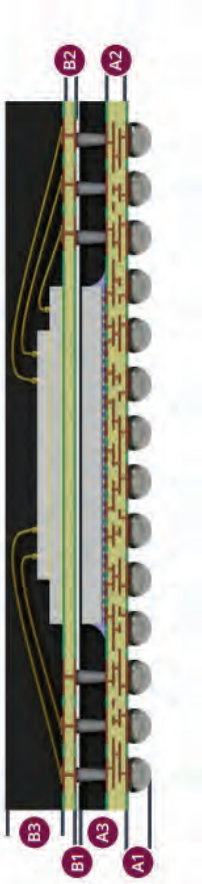
https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>TMV PoP discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, e.g.:</p> <div><p style="text-align: center;">TMV® PoP Overall Stack Up Table</p><table><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>	Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340	1.240
Symbol	Unit	Min	Max	Nom																																					
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																					
A2 (4L laminate)	mm	0.220	0.300	0.260																																					
A3 (Mold cap)	mm	0.230	0.280	0.250																																					
B1 (Stacked gap)	mm	0.020	0.080	0.050																																					
B2 (2L laminate)	mm	0.100	0.160	0.130																																					
B3 (Mold cap)	mm	0.370	0.430	0.400																																					
Overall Package Height	mm	1.140	1.340	1.240																																					
<p>[1.D] the spacer connector comprises a core substrate;</p>																																									

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>“Amkor developed new technologies to create the next generation PoP solution with interconnect vias through the mold cap, naming this technology Through Mold Via (TMV®). TMV technology provides a stable bottom package that enables use of thinner substrates with a larger die to package ratio.”</p> <p>https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename</p>
--	---

<div>Cross Section TMV® PoP</div> <div></div>		<div>TMV® Overall Stack Up Table (mm)</div> <table><thead><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr></thead><tbody><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></tbody></table>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>TMV PoP discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“As can be seen in Figure 18, the TMV™ structure provides mechanical support to the critical bottom interface of the stacked solder joint shown in red through the mold compound of the bottom package shown in gray.”</p>

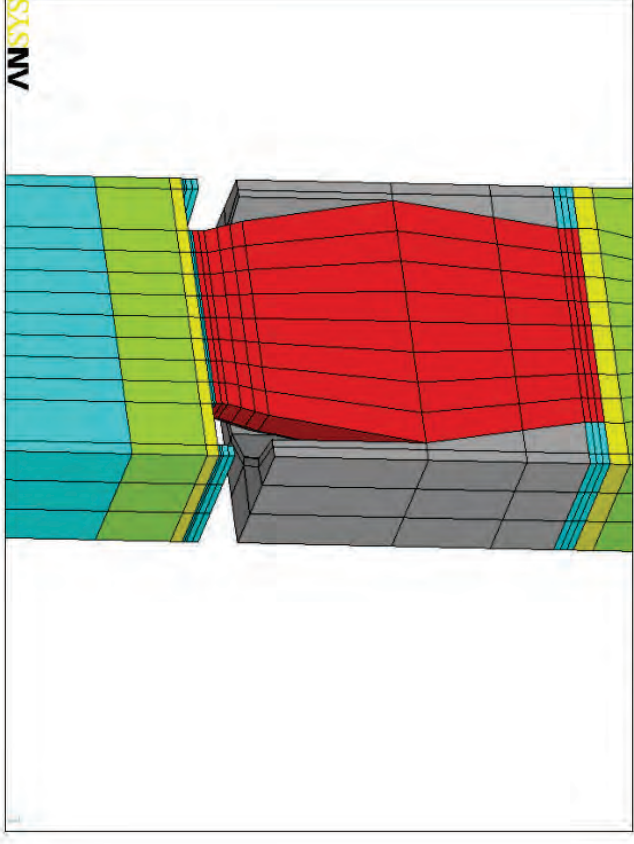


Figure 18. FE Model of top solder joint with TMV™

https://www.circuitnet.com/news/uploads/1/Amkor_SEMC_SMTAI08_TMV_PoP_paper.pdf

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

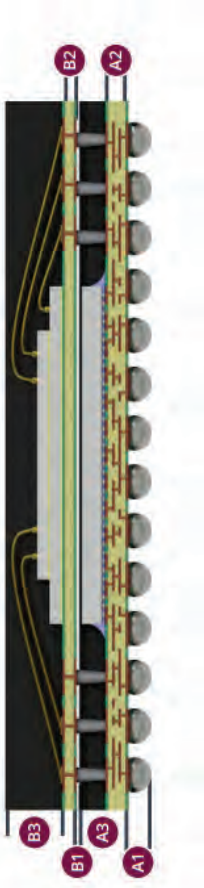
A cross-sectional diagram of a TMV PoP Overall Stack Up. It shows a stack of layers: A1 (bottom, orange), A2 (second, green), A3 (third, orange), B1 (fourth, white), B2 (fifth, green), and B3 (top, orange). Dimensions are indicated by arrows: A1 is 0.150 mm, A2 is 0.260 mm, A3 is 0.250 mm, B1 is 0.050 mm, B2 is 0.130 mm, and B3 is 0.400 mm. The overall package height is 1.240 mm. The diagram also shows a mold cap (A3) and a stacked gap (B1).

TMV[®] PoP Overall Stack Up Table

Symbol	Unit	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150
A2 (4L laminate)	mm	0.220	0.300	0.260
A3 (Mold cap)	mm	0.230	0.280	0.250
B1 (Stacked gap)	mm	0.020	0.080	0.050
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Package Height	mm	1.140	1.340	1.240

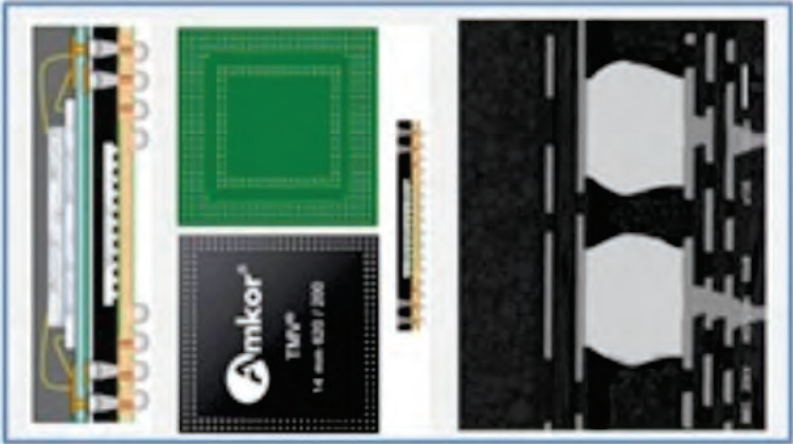
“Amkor developed new technologies to create the next generation PoP solution with interconnect vias through the mold cap, naming this technology Through Mold Via (TMV[®]). TMV technology provides a stable bottom package that enables use of thinner substrates with a larger die to package ratio.”

<https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

<div><div>Cross Section TMV® PoP</div><div></div></div>		<div><div>TMV® Overall Stack Up Table (mm)</div><table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

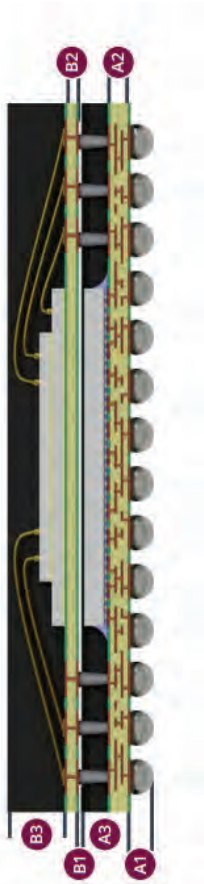
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>TMV PoP discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

	<div><div>TMV</div><div></div><div>0.4-0.5</div><div>300-500</div></div>
--	---

<https://www.uic.com/next-generation-pop-shrinking-the-package-on-package/>

Cross Section TMV® PoP



TMV® Overall Stack Up Table (mm)

Symbol	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150
A2 (4L Laminate)	0.220	0.300	0.260
A3 (Mold Cap)	0.230	0.280	0.250
B1 (Stacked Gap)	0.020	0.080	0.050
B2 (2L Laminate)	0.100	0.160	0.130
B3 (Mold Cap)	0.370	0.430	0.400
Overall Package Height	1.140	1.340	1.240

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>TMV PoP discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p> <p>“As can be seen in Figure 18, the TMV™ structure provides mechanical support to the critical bottom interface of the stacked solder joint shown in red through the mold compound of the bottom package shown in gray.”</p>

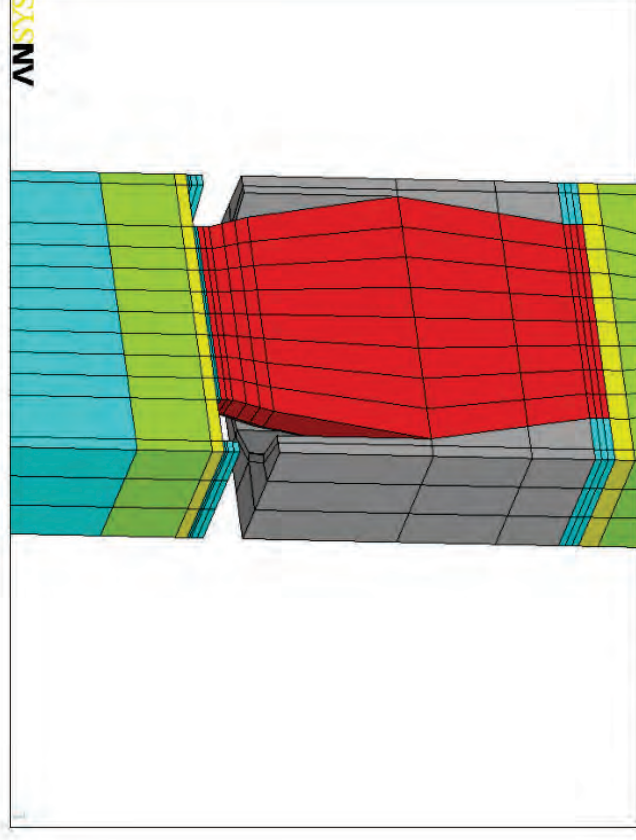
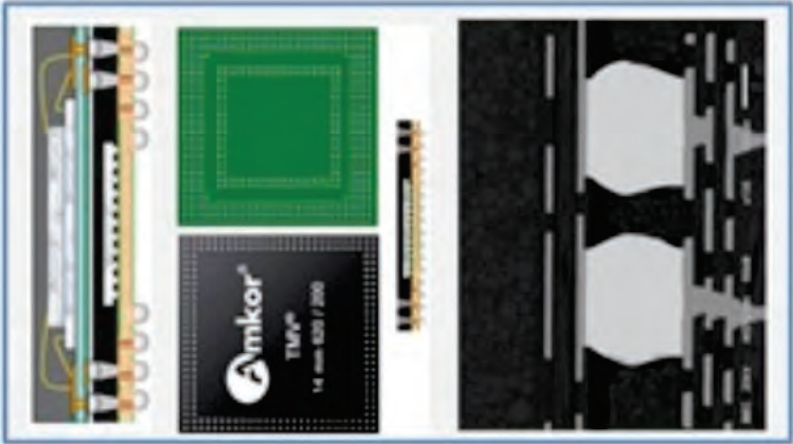


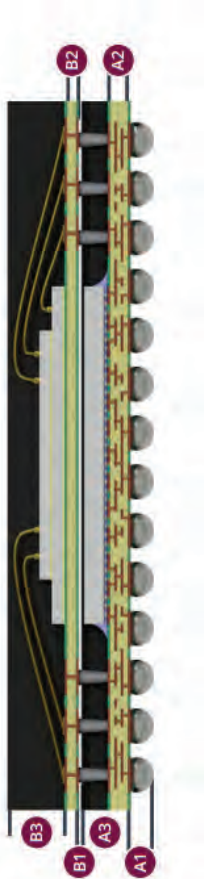
Figure 18. FE Model of top solder joint with TMV™

https://www.circuitnet.com/news/uploads/1/Amkor_SEMC_SMTAI08_TMV_PoP_paper.pdf

	<div><div>TMV</div><div></div><div><div>0.4-0.5</div><div>300-500</div></div></div>
--	--

<https://www.uic.com/next-generation-pop-shrinking-the-package-on-package/>

Cross Section TMV® PoP



TMV® Overall Stack Up Table (mm)

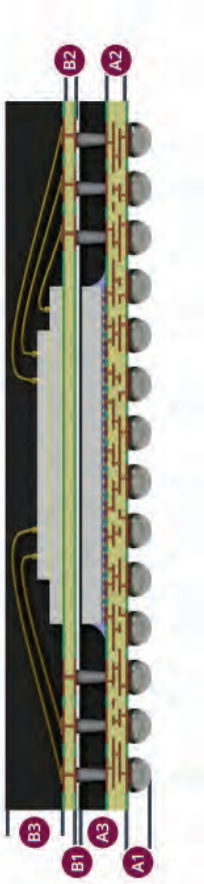
Symbol	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150
A2 (4L Laminate)	0.220	0.300	0.260
A3 (Mold Cap)	0.230	0.280	0.250
B1 (Stacked Gap)	0.020	0.080	0.050
B2 (2L Laminate)	0.100	0.160	0.130
B3 (Mold Cap)	0.370	0.430	0.400
Overall Package Height	1.140	1.340	1.240

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>TMV PoP discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

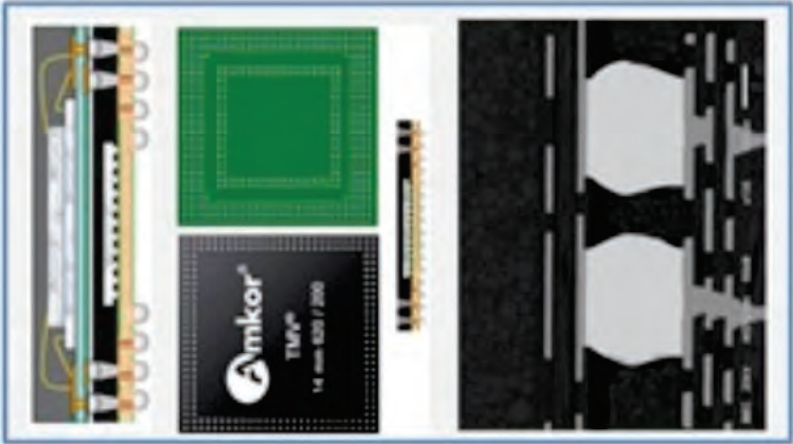
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

																																											
	<p>TMV® PoP Overall Stack Up Table</p> <table><thead><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr></thead><tbody><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></tbody></table>				Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340
Symbol	Unit	Min	Max	Nom																																							
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																							
A2 (4L laminate)	mm	0.220	0.300	0.260																																							
A3 (Mold cap)	mm	0.230	0.280	0.250																																							
B1 (Stacked gap)	mm	0.020	0.080	0.050																																							
B2 (2L laminate)	mm	0.100	0.160	0.130																																							
B3 (Mold cap)	mm	0.370	0.430	0.400																																							
Overall Package Height	mm	1.140	1.340	1.240																																							
<p>https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename</p>																																											

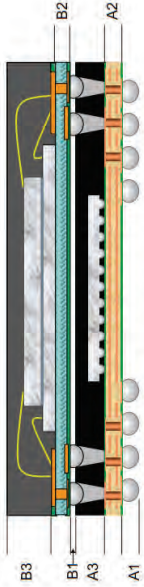
<div><div>Cross Section TMV® PoP</div><div></div></div>		<div><div>TMV® Overall Stack Up Table (mm)</div><table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf
--	---

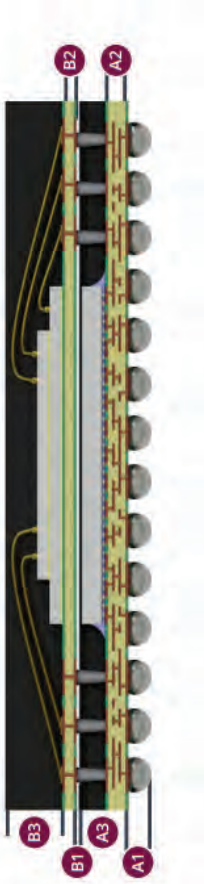
	<div><div>TMV</div><div></div><div><div>0.4-0.5</div><div>300-500</div></div></div>
--	--

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://www.uic.com/next-generation-pop-shrinking-the-package-on-package/</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>																																								
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>TMV PoP discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <div><p>TMV® PoP Overall Stack Up Table</p><table><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>	Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340	1.240
Symbol	Unit	Min	Max	Nom																																					
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																					
A2 (4L laminate)	mm	0.220	0.300	0.260																																					
A3 (Mold cap)	mm	0.230	0.280	0.250																																					
B1 (Stacked gap)	mm	0.020	0.080	0.050																																					
B2 (2L laminate)	mm	0.100	0.160	0.130																																					
B3 (Mold cap)	mm	0.370	0.430	0.400																																					
Overall Package Height	mm	1.140	1.340	1.240																																					

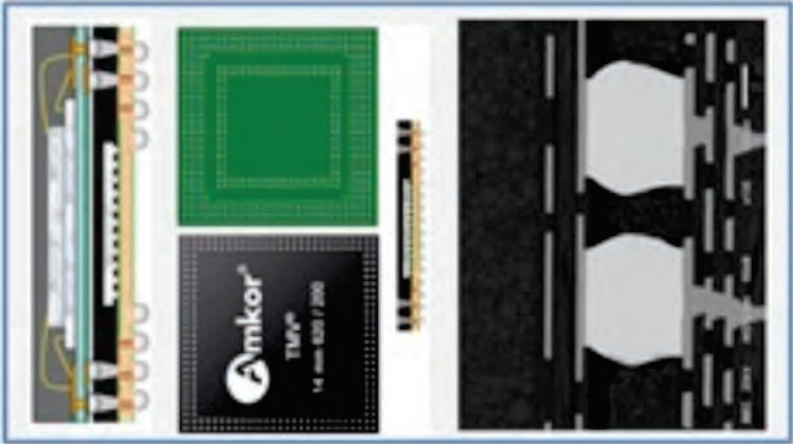
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename
--	---

<div> <div> Cross Section TMV® PoP </div>  </div>		<div> <div>TMV® Overall Stack Up Table (mm)</div> <table> <tr> <th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr> <tr> <td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr> <tr> <td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr> <tr> <td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr> <tr> <td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr> <tr> <td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr> <tr> <td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr> <tr> <td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr> </table> </div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf
--	---

	<div><div>TMV</div><div></div><div><div>0.4-0.5</div><div>300-500</div></div></div>
--	--

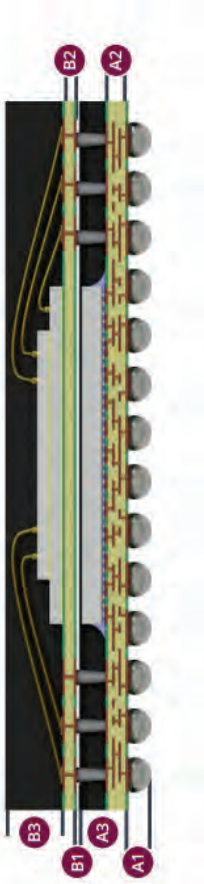
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://www.uic.com/next-generation-pop-shrinking-the-package-on-package/</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate;</p>	<p>TMV PoP discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

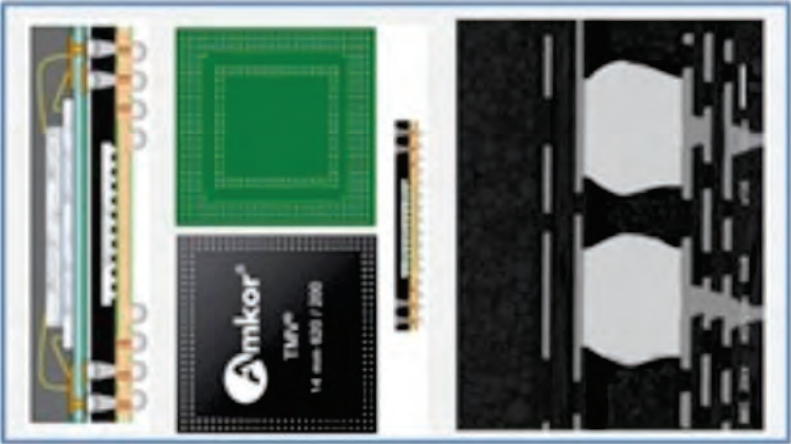
			
		TMV® PoP Overall Stack Up Table	
Symbol	Unit	Min	Max
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200
A2 (4L laminate)	mm	0.220	0.300
A3 (Mold cap)	mm	0.230	0.280
B1 (Stacked gap)	mm	0.020	0.080
B2 (2L laminate)	mm	0.100	0.160
B3 (Mold cap)	mm	0.370	0.430
Overall Package Height	mm	1.140	1.340
			Nom
			0.150
			0.260
			0.250
			0.050
			0.130
			0.400
			1.240

<https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

<div> <div> Cross Section TMV® PoP </div>  </div>		<div> <div>TMV® Overall Stack Up Table (mm)</div> <table> <tr> <th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr> <tr> <td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr> <tr> <td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr> <tr> <td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr> <tr> <td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr> <tr> <td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr> <tr> <td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr> <tr> <td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr> </table> </div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf
--	---

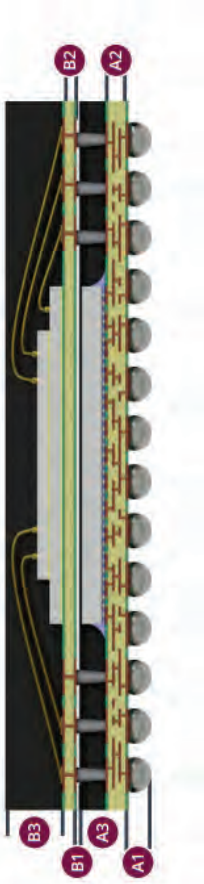
	<div><div>TMV</div><div></div><div><div>0.4-0.5</div><div>300-500</div></div></div>
--	--

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

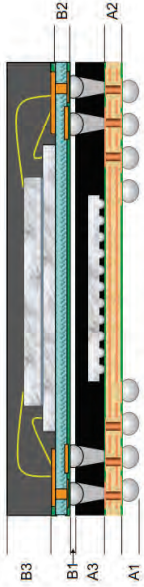
	<p>https://www.uic.com/next-generation-pop-shrinking-the-package-on-package/</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>																																								
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>TMV PoP discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate.</p> <p>See, e.g.:</p> <div><p>TMV® PoP Overall Stack Up Table</p><table><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>	Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340	1.240
Symbol	Unit	Min	Max	Nom																																					
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																					
A2 (4L laminate)	mm	0.220	0.300	0.260																																					
A3 (Mold cap)	mm	0.230	0.280	0.250																																					
B1 (Stacked gap)	mm	0.020	0.080	0.050																																					
B2 (2L laminate)	mm	0.100	0.160	0.130																																					
B3 (Mold cap)	mm	0.370	0.430	0.400																																					
Overall Package Height	mm	1.140	1.340	1.240																																					

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename
--	---

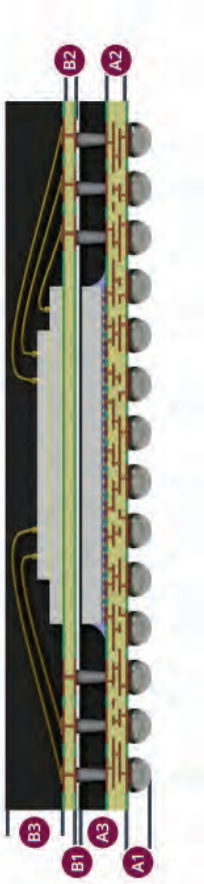
<div>Cross Section TMV® PoP</div> <div></div>		<div>TMV® Overall Stack Up Table (mm)</div> <table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

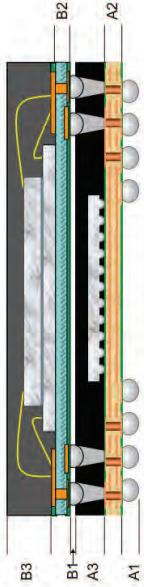
	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>																																								
<p>[1.L.] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>TMV PoP discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p>See, e.g.:</p> <div><p>TMV® PoP Overall Stack Up Table</p><table><thead><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr></thead><tbody><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></tbody></table></div>	Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340	1.240
Symbol	Unit	Min	Max	Nom																																					
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																					
A2 (4L laminate)	mm	0.220	0.300	0.260																																					
A3 (Mold cap)	mm	0.230	0.280	0.250																																					
B1 (Stacked gap)	mm	0.020	0.080	0.050																																					
B2 (2L laminate)	mm	0.100	0.160	0.130																																					
B3 (Mold cap)	mm	0.370	0.430	0.400																																					
Overall Package Height	mm	1.140	1.340	1.240																																					

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename
--	---

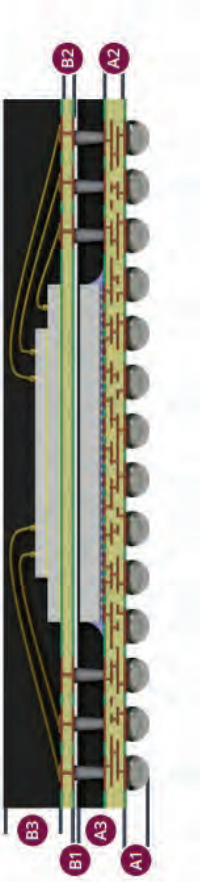
<div><div>Cross Section TMV® PoP</div></div>		<div><div>TMV® Overall Stack Up Table (mm)</div><table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminate)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminate)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminate)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminate)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminate)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminate)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>																																								
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>TMV PoP discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p> <div><p style="text-align: center;">TMV® PoP Overall Stack Up Table</p><table><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>	Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340	1.240
Symbol	Unit	Min	Max	Nom																																					
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																					
A2 (4L laminate)	mm	0.220	0.300	0.260																																					
A3 (Mold cap)	mm	0.230	0.280	0.250																																					
B1 (Stacked gap)	mm	0.020	0.080	0.050																																					
B2 (2L laminate)	mm	0.100	0.160	0.130																																					
B3 (Mold cap)	mm	0.370	0.430	0.400																																					
Overall Package Height	mm	1.140	1.340	1.240																																					

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename
--	---

<div>Cross Section TMV® PoP</div> <div></div>		<div>TMV® Overall Stack Up Table (mm)</div> <table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 2

Claim Limitation	Disclosure
<p>[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p>	<p>TMV PoP discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>

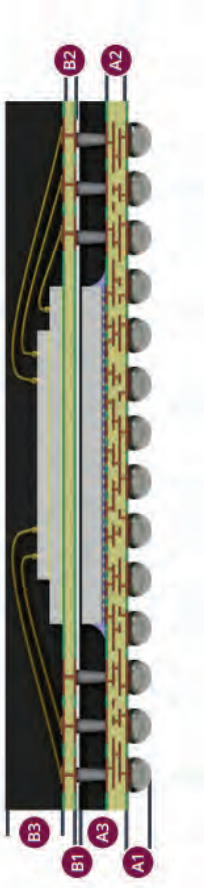
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

A cross-sectional diagram of a TMV PoP Overall Stack Up Table. The diagram shows a stack of layers labeled A1, A2, A3, B1, B2, and B3. Layer A1 is the bottom-most layer, followed by A2, A3, B1, B2, and B3 at the top. The layers are shown in various colors: A1 is orange, A2 is green, A3 is yellow, B1 is white, B2 is blue, and B3 is grey. The diagram also shows the overall package height and the dimensions of each layer.

TMV[®] PoP Overall Stack Up Table

Symbol	Unit	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150
A2 (4L laminate)	mm	0.220	0.300	0.260
A3 (Mold cap)	mm	0.230	0.280	0.250
B1 (Stacked gap)	mm	0.020	0.080	0.050
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Package Height	mm	1.140	1.340	1.240

<https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

<div><div>Cross Section TMV® PoP</div><div></div></div>		<div><div>TMV® Overall Stack Up Table (mm)</div><table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 3

Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p>	<p>TMV PoP discloses, either expressly or inherently, a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p><i>See, e.g.:</i></p>

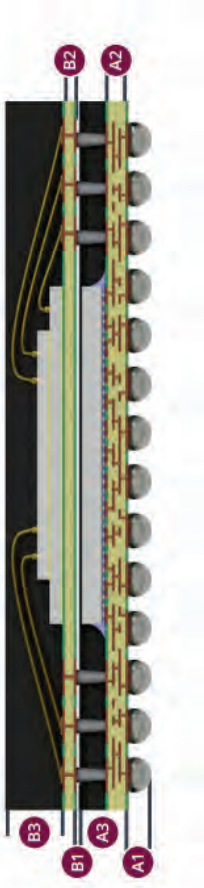
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

A cross-sectional diagram of a TMV PoP Overall Stack Up Table. The diagram shows a stack of layers labeled A1, A2, A3, B1, B2, and B3. Layer A1 is the bottom-most layer, followed by A2, A3, B1, B2, and B3 at the top. The layers are shown in various colors: A1 is orange, A2 is green, A3 is yellow, B1 is white, B2 is blue, and B3 is grey. The diagram also shows the overall package height and the dimensions of each layer.

TMV[®] PoP Overall Stack Up Table

Symbol	Unit	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150
A2 (4L laminate)	mm	0.220	0.300	0.260
A3 (Mold cap)	mm	0.230	0.280	0.250
B1 (Stacked gap)	mm	0.020	0.080	0.050
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Package Height	mm	1.140	1.340	1.240

<https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

<div><div>Cross Section TMV® PoP</div><div></div></div>		<div><div>TMV® Overall Stack Up Table (mm)</div><table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>TMV PoP discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

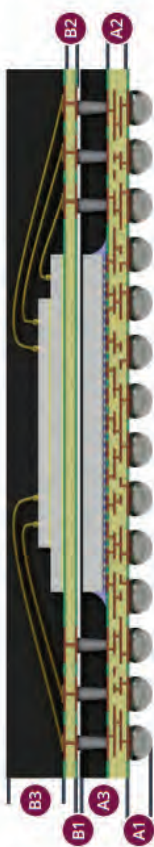
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

TMV® PoP Overall Stack Up Table

Symbol	Unit	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150
A2 (4L laminate)	mm	0.220	0.300	0.260
A3 (Mold cap)	mm	0.230	0.280	0.250
B1 (Stacked gap)	mm	0.020	0.080	0.050
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Package Height	mm	1.140	1.340	1.240

<https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

Cross Section TMV® PoP

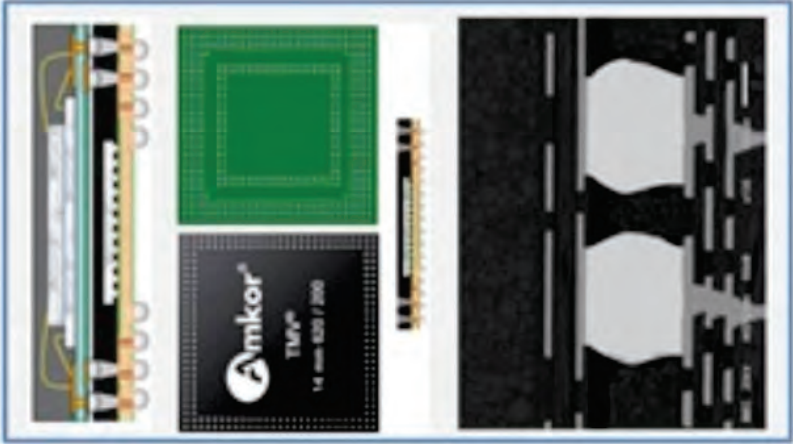


TMV® Overall Stack Up Table (mm)

Symbol	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150
A2 (4L Laminate)	0.220	0.300	0.260
A3 (Mold Cap)	0.230	0.280	0.250
B1 (Stacked Gap)	0.020	0.080	0.050
B2 (2L Laminate)	0.100	0.160	0.130
B3 (Mold Cap)	0.370	0.430	0.400
Overall Package Height	1.140	1.340	1.240

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf
--	---

	<div><div>TMV</div><div></div><div>0.4-0.5</div><div>300-500</div></div>
--	---

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

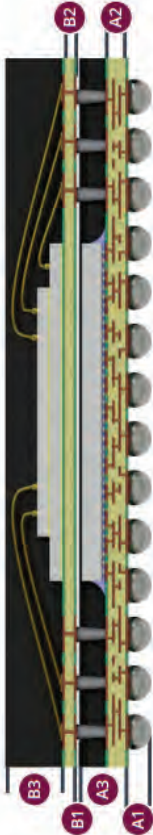
	<p>https://www.uic.com/next-generation-pop-shrinking-the-package-on-package/</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 6

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and the corresponding top ends of the plurality of metal pillars of the top package substrate are connected to the corresponding top metal pads of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>TMV PoP discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

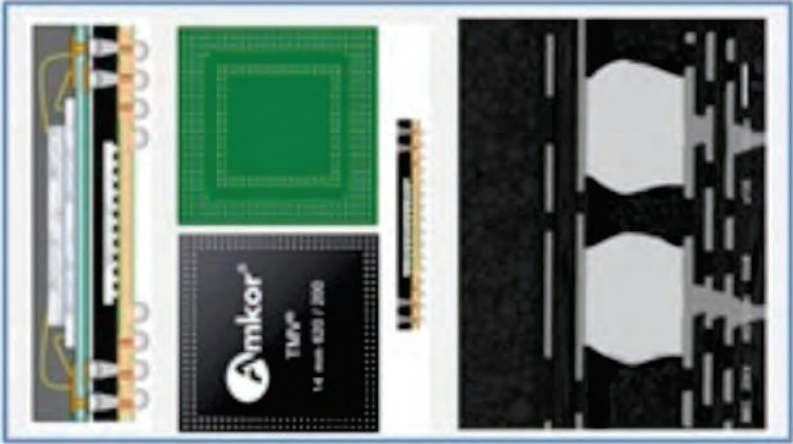
Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

																																											
	<p>TMV® PoP Overall Stack Up Table</p> <table><tr><th>Symbol</th><th>Unit</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>mm</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L laminate)</td><td>mm</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold cap)</td><td>mm</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked gap)</td><td>mm</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L laminate)</td><td>mm</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold cap)</td><td>mm</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>mm</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table>				Symbol	Unit	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150	A2 (4L laminate)	mm	0.220	0.300	0.260	A3 (Mold cap)	mm	0.230	0.280	0.250	B1 (Stacked gap)	mm	0.020	0.080	0.050	B2 (2L laminate)	mm	0.100	0.160	0.130	B3 (Mold cap)	mm	0.370	0.430	0.400	Overall Package Height	mm	1.140	1.340
Symbol	Unit	Min	Max	Nom																																							
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150																																							
A2 (4L laminate)	mm	0.220	0.300	0.260																																							
A3 (Mold cap)	mm	0.230	0.280	0.250																																							
B1 (Stacked gap)	mm	0.020	0.080	0.050																																							
B2 (2L laminate)	mm	0.100	0.160	0.130																																							
B3 (Mold cap)	mm	0.370	0.430	0.400																																							
Overall Package Height	mm	1.140	1.340	1.240																																							
<p>https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename</p>																																											

<div><div>Cross Section TMV® PoP</div><div></div></div>		<div><div>TMV® Overall Stack Up Table (mm)</div><table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table></div>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf
--	---

	<div><div>TMV</div><div></div><div><div>0.4-0.5</div><div>300-500</div></div></div>
--	--

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://www.uic.com/next-generation-pop-shrinking-the-package-on-package/</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>	<p>TMV PoP discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

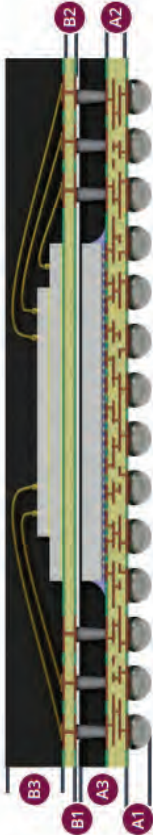
corresponding top metal pads of the spacer connector.



TMV® PoP Overall Stack Up Table

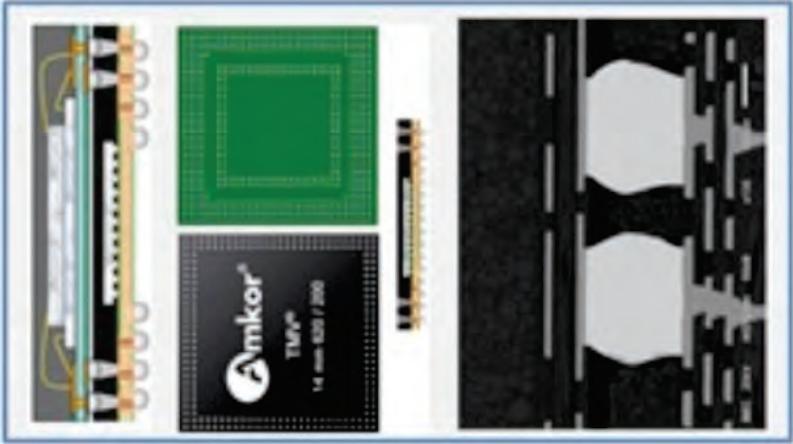
Symbol	Unit	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.100	0.200	0.150
A2 (4L laminate)	mm	0.220	0.300	0.260
A3 (Mold cap)	mm	0.230	0.280	0.250
B1 (Stacked gap)	mm	0.020	0.080	0.050
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Package Height	mm	1.140	1.340	1.240

<https://web.archive.org/web/20130425204531/http://www.amkor.com/download.cfm?downloadfile=062B7525-0B79-3F7F-5BAC6FA59D9C3582&typename=dmFile&fieldname=filename>

<div>Cross Section TMV® PoP</div> <div></div>		<div>TMV® Overall Stack Up Table (mm)</div> <table><tr><th>Symbol</th><th>Min</th><th>Max</th><th>Nom</th></tr><tr><td>A1 (Mounted, 0.4 pitch)</td><td>0.100</td><td>0.200</td><td>0.150</td></tr><tr><td>A2 (4L Laminates)</td><td>0.220</td><td>0.300</td><td>0.260</td></tr><tr><td>A3 (Mold Cap)</td><td>0.230</td><td>0.280</td><td>0.250</td></tr><tr><td>B1 (Stacked Gap)</td><td>0.020</td><td>0.080</td><td>0.050</td></tr><tr><td>B2 (2L Laminates)</td><td>0.100</td><td>0.160</td><td>0.130</td></tr><tr><td>B3 (Mold Cap)</td><td>0.370</td><td>0.430</td><td>0.400</td></tr><tr><td>Overall Package Height</td><td>1.140</td><td>1.340</td><td>1.240</td></tr></table>		Symbol	Min	Max	Nom	A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150	A2 (4L Laminates)	0.220	0.300	0.260	A3 (Mold Cap)	0.230	0.280	0.250	B1 (Stacked Gap)	0.020	0.080	0.050	B2 (2L Laminates)	0.100	0.160	0.130	B3 (Mold Cap)	0.370	0.430	0.400	Overall Package Height	1.140	1.340	1.240
Symbol	Min	Max	Nom																																
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150																																
A2 (4L Laminates)	0.220	0.300	0.260																																
A3 (Mold Cap)	0.230	0.280	0.250																																
B1 (Stacked Gap)	0.020	0.080	0.050																																
B2 (2L Laminates)	0.100	0.160	0.130																																
B3 (Mold Cap)	0.370	0.430	0.400																																
Overall Package Height	1.140	1.340	1.240																																

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	https://amkormarcomexternal.blob.core.windows.net/amkordotcom/wp-content/uploads/2018/02/PoP_DS586.pdf
--	---

	<div><div>TMV</div><div></div><div><div>0.4-0.5</div><div>300-500</div></div></div>
--	--

Appendix A-51 - Invalidity of U.S. Patent No. 9,859,202 in view of TMV PoP

	<p>https://www.uic.com/next-generation-pop-shrinking-the-package-on-package/</p> <p>To the extent Plaintiff contends that TMV PoP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

E.D. Tex. Case No. 2:25-cv-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

The Molded Core embedded Package (hereinafter “MCeP”) was in public use, on sale (including sold to customers and potential customers), and/or otherwise available to the public by Shinko Electric Industries Co., Ltd. at least by 2013.¹ MCeP anticipates and/or renders obvious all Asserted Claims² of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.³ MCeP, or the written materials describing it, excerpted below, is prior art to the ’202 Patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within MCeP, or otherwise rendered obvious by disclosures and teachings of MCeP, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that MCeP does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of MCeP with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 Patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by MCeP, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire

¹ See, e.g., <https://web.archive.org/web/20130215093055/http://www.shinko.co.jp/english/product/sip/mcep.html#link1>

² As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

³ To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that MCeP “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to MCeP or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding MCeP set forth in this chart.

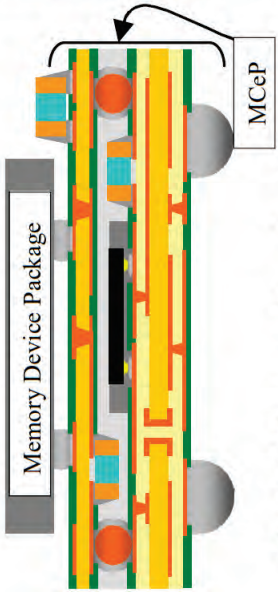
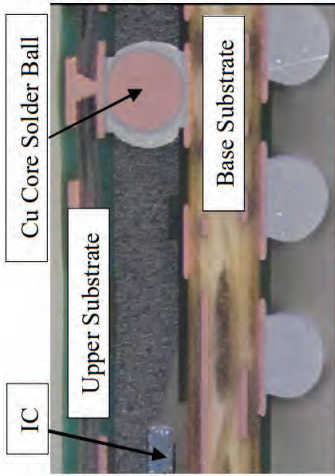
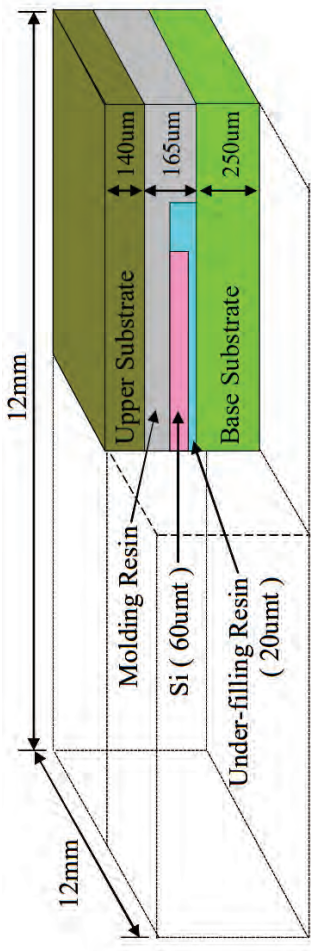
Claim 1

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	<p>To the extent the preamble is a limitation, MCeP discloses, either expressly or inherently, a structure.</p> <p><i>See, e.g.:</i></p> <p>“We offer MCeP®(Molded Core embedded Package) with the package structure achieved by active and passive components built in. The package type is also called ‘embedded substrate’ in the market. We provide the package features compact and thin package size, excellent electric characteristics, and high reliability enabled by our own packaging technology.”</p> <p>https://web.archive.org/web/20130215093055/http://www.shinko.co.jp/english/product/sip/mcep.html#link1</p>

	<div> <p>Structure</p> <p>Standard</p> <p>Mold Resin</p> <p>IC Chip</p> <p>Cu Core Solder Ball</p> <p>Top Substrate</p> <p>Embedded Layer</p> <p>Bottom Substrate</p> <p>Capacitor</p> </div> <div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p> </div> <div> <p>Memory Device Package</p> <p>MCeP</p> </div> <div> <p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p> </div> <div> <p>“We have been also developing embedded device package named MCeP, Molded Core embedded Package. This package consists of base substrate, upper substrate and molding resin. These substrates</p> </div>
--	---

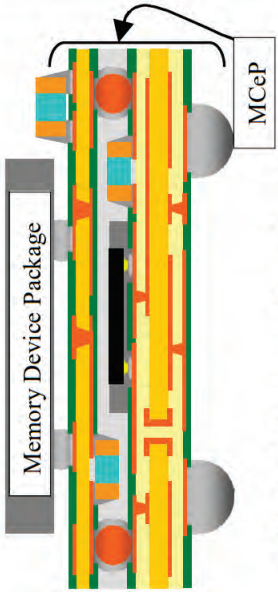
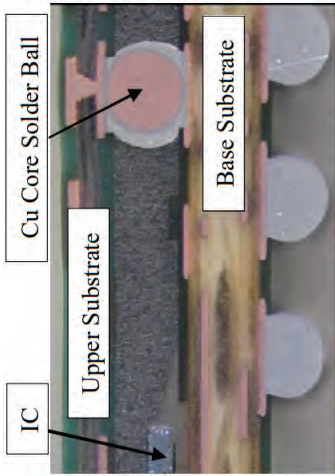
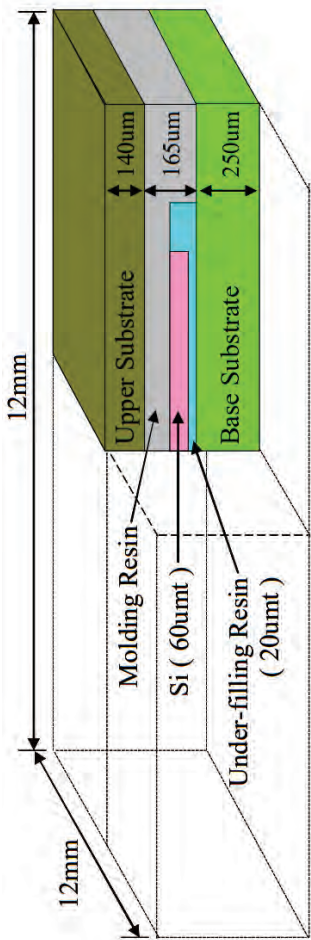
Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>material is conventional organic base. Bare IC devices without re-routing are mounted on inner surface of base substrate. Upper substrate and base substrate are connected electrically by copper core solder balls. The space between upper and base substrate is encapsulated by molding resin.”</p> <p>https://www.google.com/url?sa=t&rct=i&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwIJI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoIYXALBj&opi=89978449</p>
<p>[1.A] a bottom package substrate;</p>	<p>MCeP discloses, either expressly or inherently, a bottom package substrate.</p> <p>See, e.g.:</p> <div> <p>Structure</p> </div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p>

	<div><p>A cross-sectional schematic diagram of a Memory Device Package and MCeP. The package consists of a central black layer (IC) sandwiched between two yellow layers (Upper and Base Substrates). The MCeP is shown as a separate component with a similar structure, including a central black layer and yellow substrate layers. Labels include 'Memory Device Package', 'IC', 'Upper Substrate', 'Base Substrate', and 'MCeP'.</p></div> <div><p>A photograph showing a cross-section of the MCeP. It displays a central black layer (IC) between two yellow layers (Upper and Base Substrates). A red circular feature is labeled 'Cu Core Solder Ball'. Labels include 'IC', 'Upper Substrate', 'Base Substrate', and 'Cu Core Solder Ball'.</p></div> <div><p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p><p>Fig. 1-3 Cross-section photograph of MCeP</p></div> <div><p>A 3D perspective view of a warpage simulation model. The model shows a layered structure with dimensions: 12mm width, 12mm depth, and 140um thickness for the Upper Substrate. The Base Substrate is 250um thick. The total height is 165um. The model includes layers for Molding Resin, Si (60umt), and Under-filling Resin (20umt). Labels include 'Upper Substrate', 'Base Substrate', 'Molding Resin', 'Si (60umt)', and 'Under-filling Resin (20umt)'.</p></div> <div><p>Fig. 7 Warpage simulation model</p></div> <div><p>“Base substrate has 3 conductive layers and thickness is 130um.”</p></div> <div><p>“MCeP consists of a base substrate, an upper substrate and molding resin.”</p></div> <div><p>“Therefore the base substrate was 4 conductive layers substrate with a build up structure and its thickness was 250um.”</p></div>
--	--

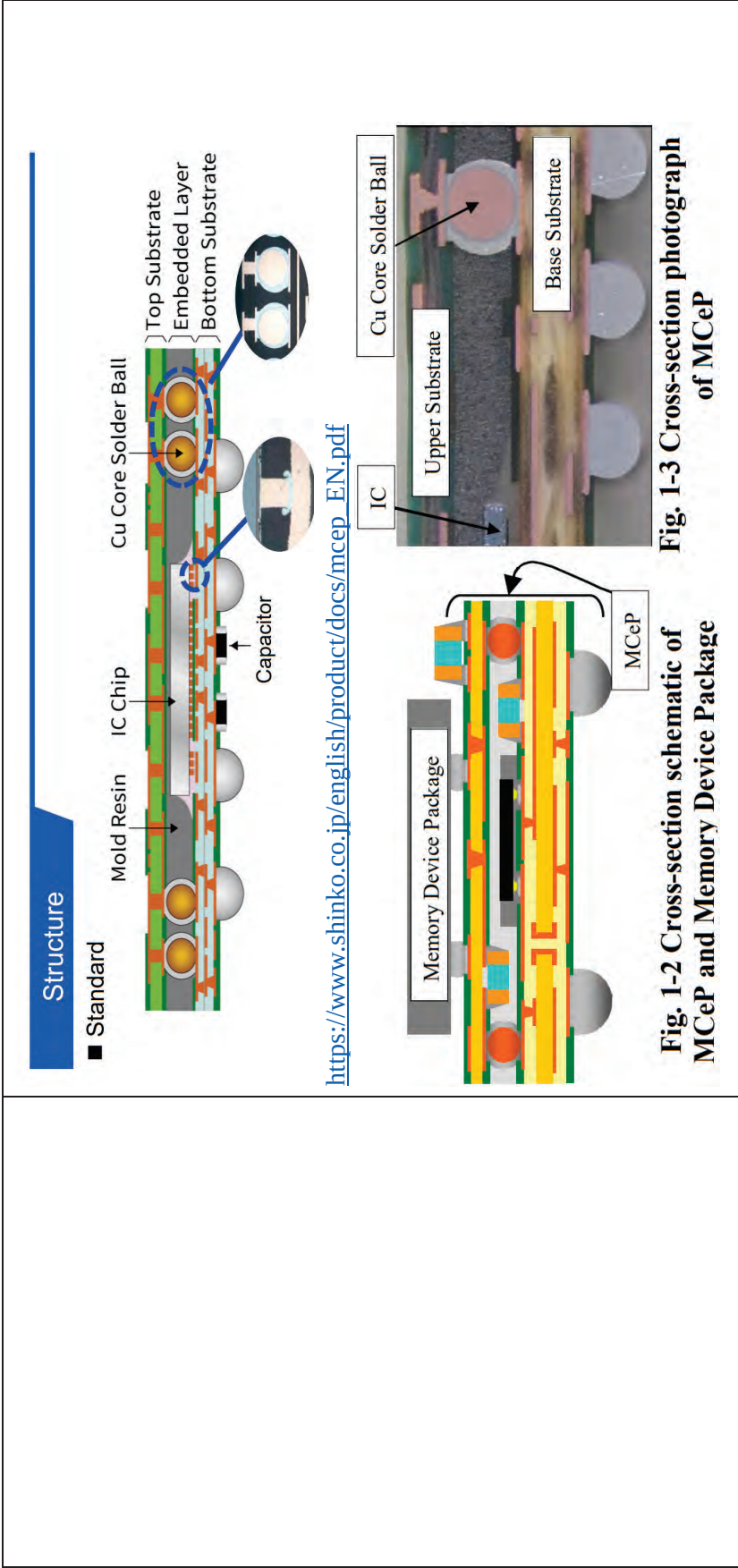
Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>“To be investigated molding process, upper substrate and base substrate with 2 conductive layers were adopted respectively. Upper substrate thickness was 280um and base substrate thickness was 240um.”</p> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbrf6-qo5SUAxWbFjQIHwIJI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usq=AOvVaw0c7ITbFunP15yBoIYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	<p>MCeP discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<div><p>A cross-sectional schematic diagram showing a Memory Device Package (top) and an MCeP (bottom). The package consists of multiple layers in yellow, orange, and green, with a central black layer. The MCeP is a single layer with a central black region. Arrows indicate the relationship between the package and the MCeP.</p></div> <div><p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p></div> <div><p>A photograph of a cross-section of the MCeP. Labels point to the IC (Integrated Circuit) on the left, the Upper Substrate in the middle, and the Base Substrate on the right. A Cu Core Solder Ball is visible on the upper substrate.</p></div> <div><p>Fig. 1-3 Cross-section photograph of MCeP</p></div> <div><p>A 3D simulation model of the MCeP showing warpage. The model is divided into three main sections: Upper Substrate (top, green), Si (middle, pink), and Base Substrate (bottom, green). The Si layer is further divided into Molding Resin (top, 60umt) and Under-filling Resin (bottom, 20umt). Dimensions are indicated: 12mm for the overall width, 140um for the upper substrate thickness, 165um for the Si layer thickness, and 250um for the base substrate thickness.</p></div> <div><p>Fig. 7 Warpage simulation model</p></div> <div><p>“Upper substrate has 2 conductive layers and thickness is 95um.”</p></div> <div><p>“MCeP consists of a base substrate, an upper substrate and molding resin.”</p></div> <div><p>“And the upper substrate was conventional 2 conductive layers substrate of 140um thickness.”</p></div>
--	---

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>“To be investigated molding process, upper substrate and base substrate with 2 conductive layers were adopted respectively. Upper substrate thickness was 280um and base substrate thickness was 240um.”</p> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHWUJ4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>MCeP discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.</p> <p><i>See, e.g.:</i></p>



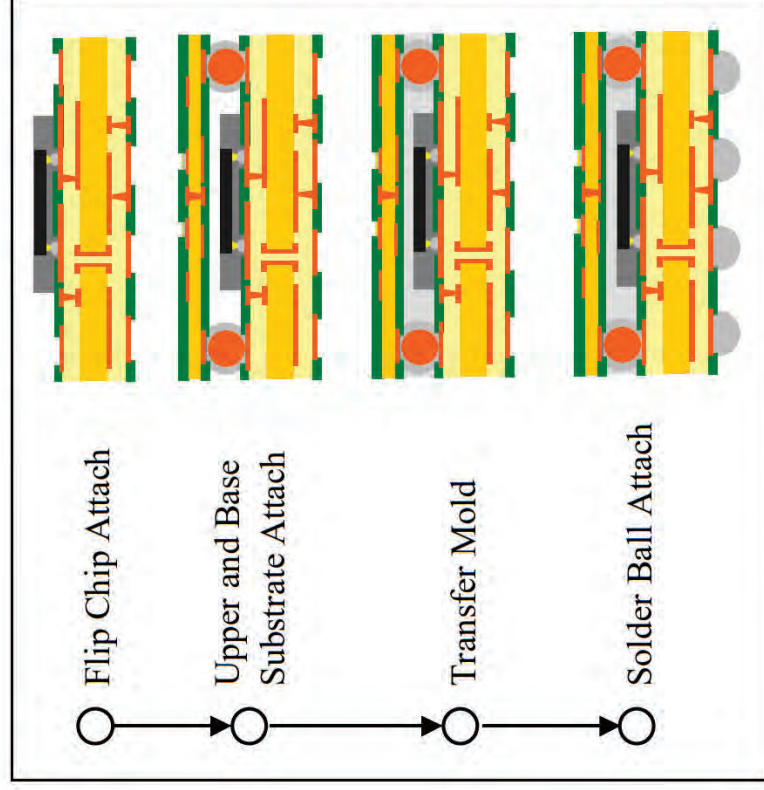
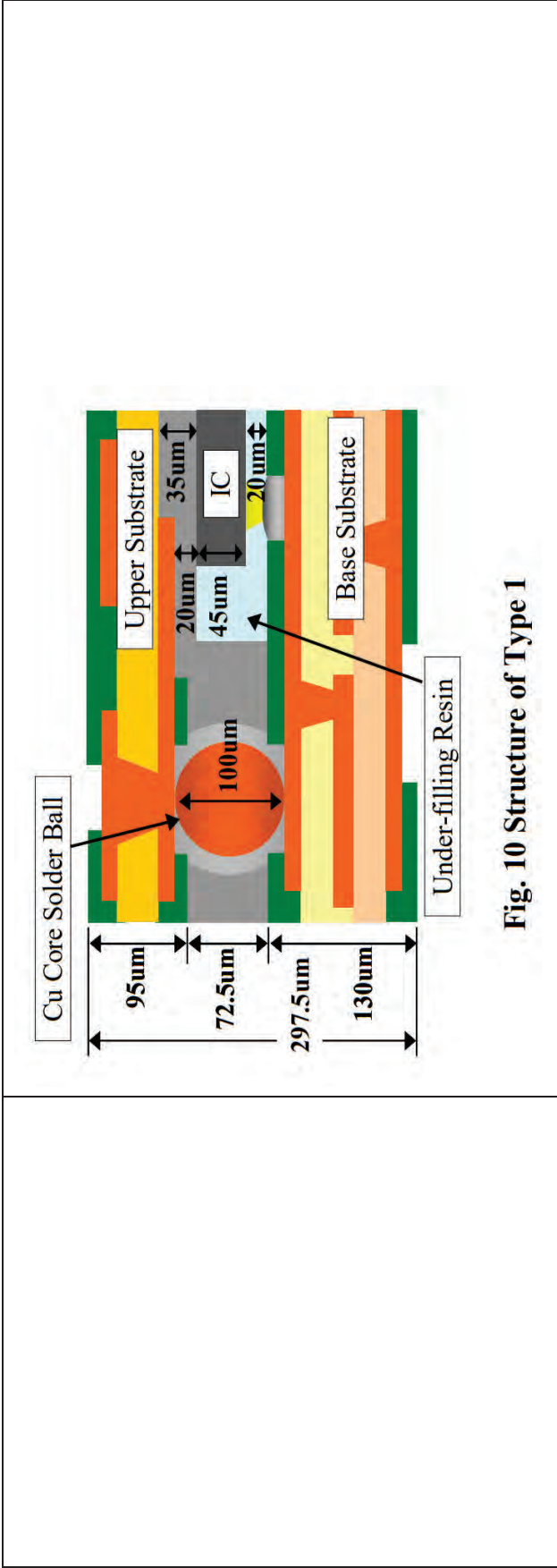


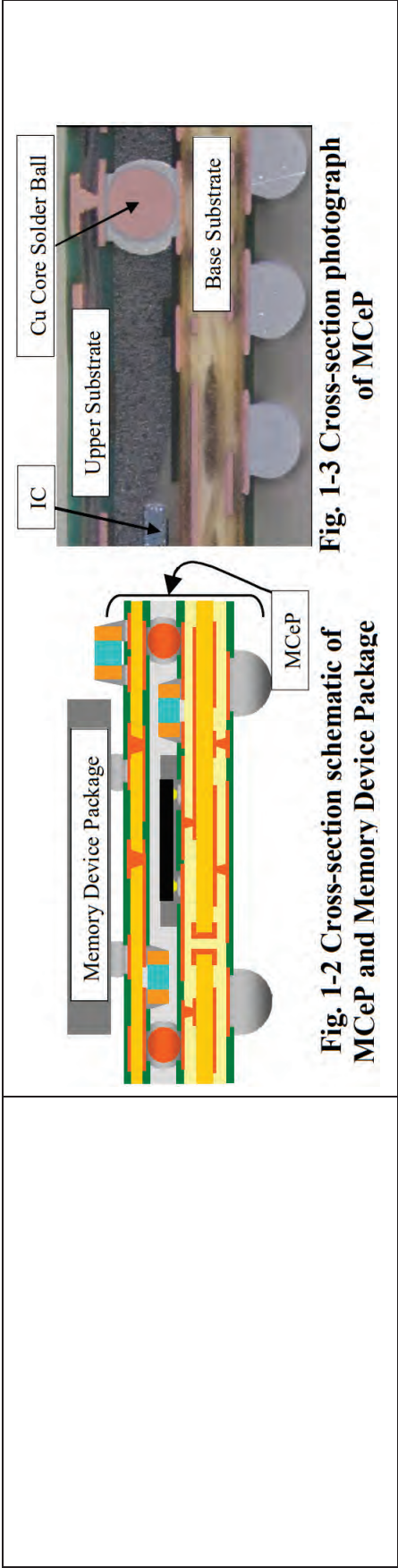
Fig. 2 Process flow of MCeP

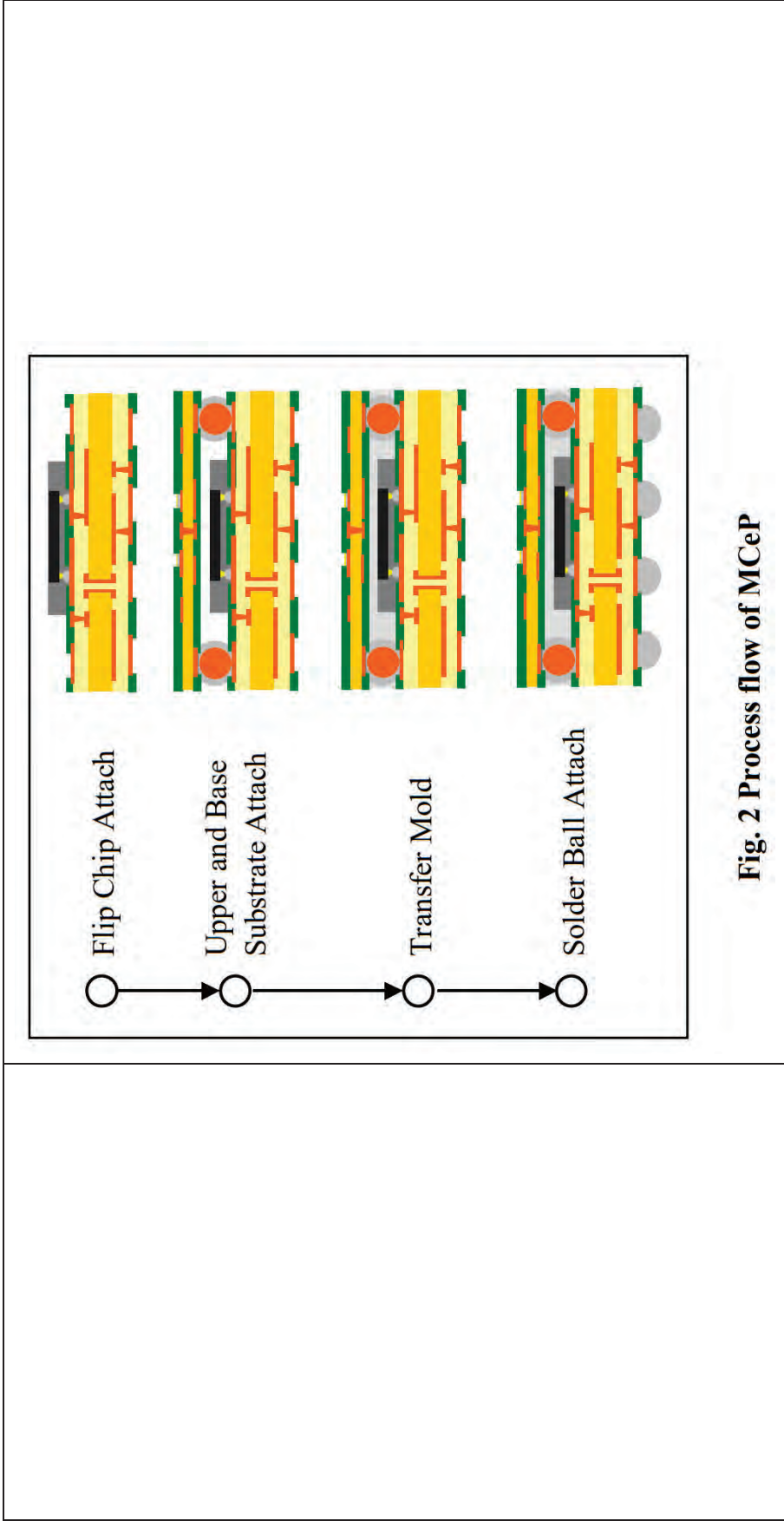


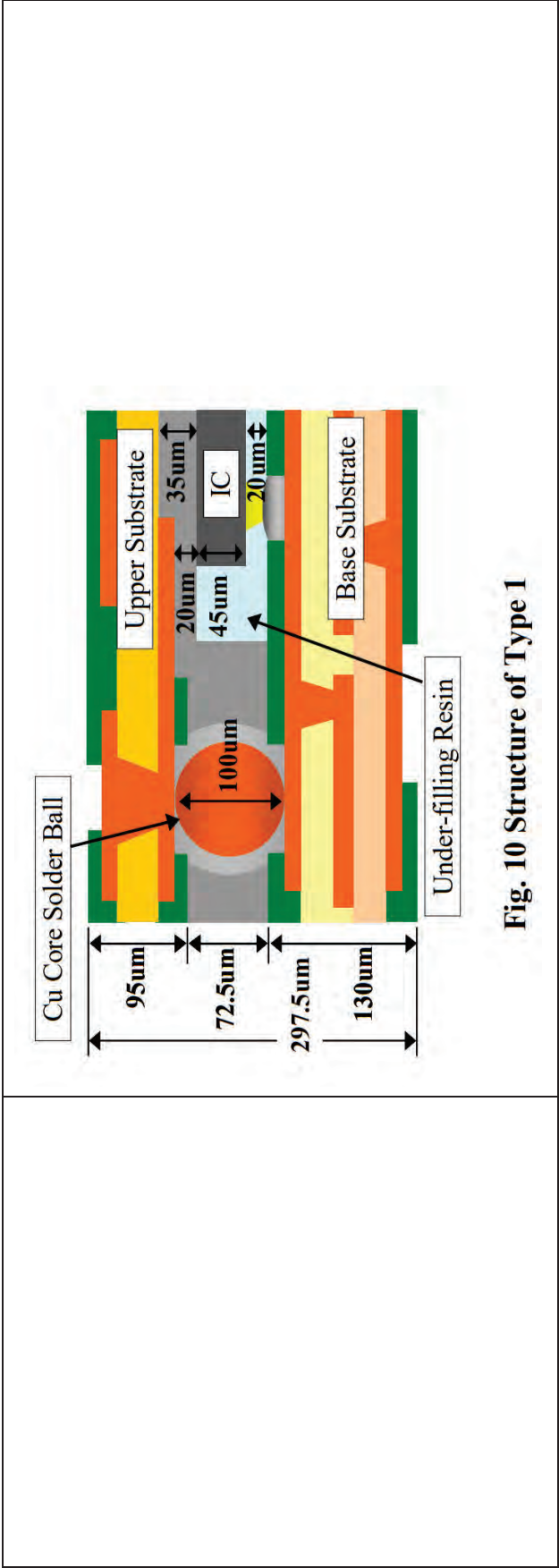
	<div><p>The diagram illustrates the cross-sectional structure of Ultra Thin MCeP Type 2. It shows a central IC (Integrated Circuit) layer with a thickness of 45um, sandwiched between an Upper Substrate (15um) and a Base Substrate (20um). This assembly is mounted on a Cu Core Solder Ball (95um) which is embedded in a Non-Conductive Film (52.5um). The entire structure is encapsulated by Under-filling Resin (277.5um). The total thickness of the assembly is 130um. A dimension of 80um is also indicated for the solder ball diameter.</p></div> <div><p>Fig. 13 Structure of Ultra Thin MCeP Type 2</p></div> <div><p>“The upper substrate and the base substrate are connected electrically by copper core solder balls. To prevent ball collapse and keep specified distance between upper and base substrate, copper core solder balls are adopted. The space between upper and base substrate is encapsulated by molding resin. And finally, solder balls are mounted on bottom layer.”</p></div> <div><p>“Embedded layer thickness of Type 1 is 72.5um by using 100um diameter copper core solder ball.”</p></div> <div><p>“Embedded layer thickness of Type 2 is 52.5um by using 80um diameter copper core solder ball.”</p></div> <div><p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usq=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p></div>
--	--

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>MCeP discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, e.g.:</p> <div> <p>Structure</p> <p>Standard</p> <p>Mold Resin</p> <p>IC Chip</p> <p>Cu Core Solder Ball</p> <p>Top Substrate</p> <p>Embedded Layer</p> <p>Bottom Substrate</p> <p>Capacitor</p> </div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p>







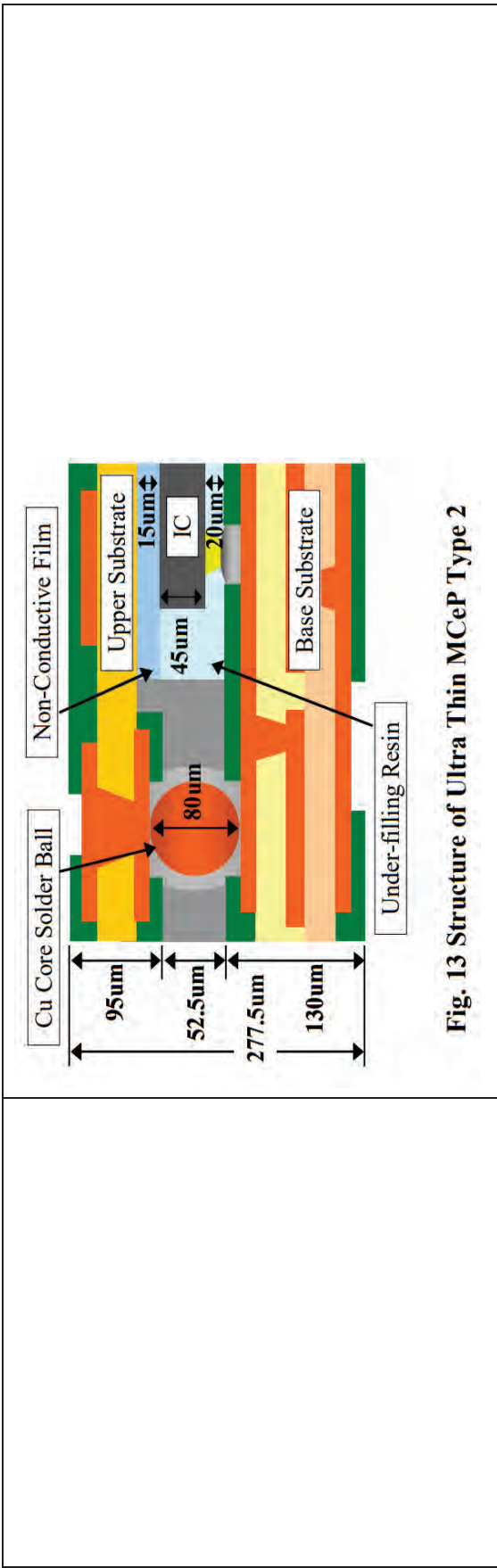


Fig. 13 Structure of Ultra Thin MCeP Type 2

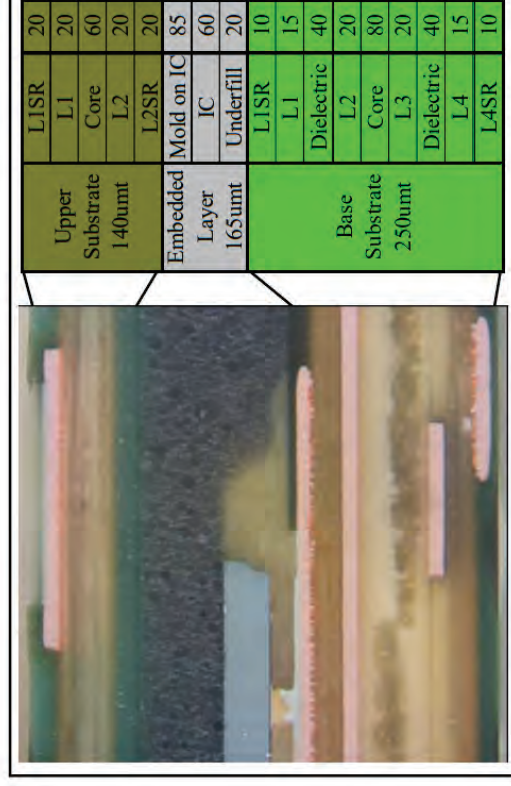


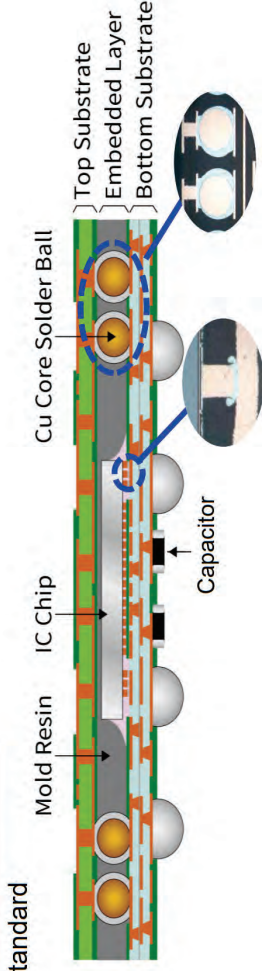
Fig. 4 Cross-section photograph of original MCeP

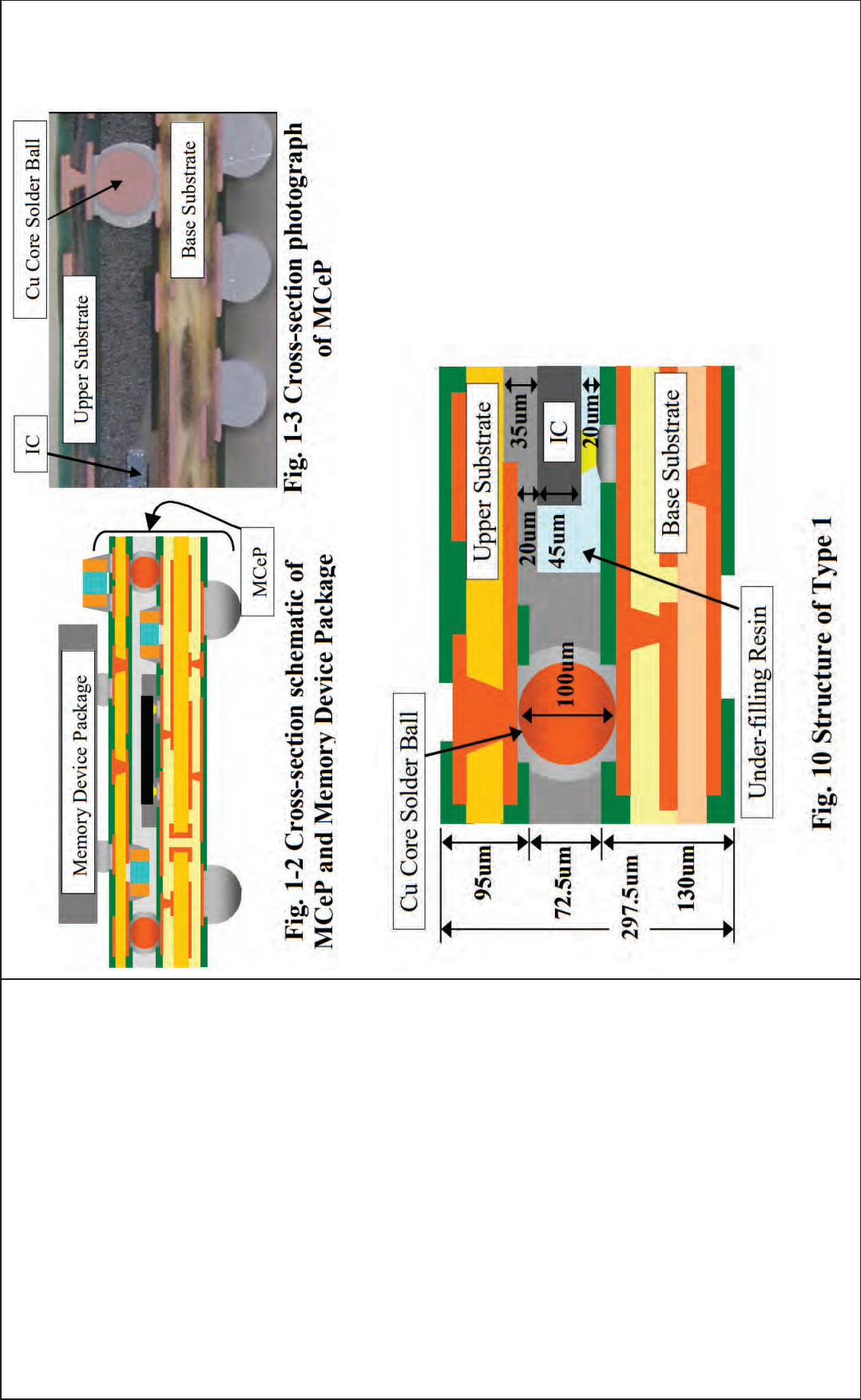
“MCeP consists of a base substrate, an upper substrate and molding resin.”

“The upper substrate and the base substrate are connected electrically by copper core solder balls. To prevent ball collapse and keep specified distance between upper and base substrate, copper core solder balls are adopted. The space between upper and base substrate is encapsulated by molding resin. And finally, solder balls are mounted on bottom layer.”

<https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAXWbFjQIHwJl4sQFn0ECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F>

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.E] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>MCeP discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p>See, e.g.:</p> <div> <p>Structure</p>  <p>Standard</p> <p>Mold Resin</p> <p>IC Chip</p> <p>Capacitor</p> <p>Cu Core Solder Ball</p> <p>Top Substrate</p> <p>Embedded Layer</p> <p>Bottom Substrate</p> </div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p>



	<div><p>The diagram illustrates the cross-sectional structure of Ultra Thin MCeP Type 2. It shows a central IC (Integrated Circuit) layer with a thickness of 45um, sandwiched between an Upper Substrate (15um) and a Base Substrate (20um). This assembly is mounted on a Cu Core Solder Ball (95um) which is embedded in a Non-Conductive Film (52.5um). The entire structure is encapsulated by Under-filling Resin (277.5um). The total thickness of the assembly is 130um. A dimension of 80um is also indicated for the solder ball diameter.</p></div> <div><p>Fig. 13 Structure of Ultra Thin MCeP Type 2</p></div> <div><p>“The upper substrate and the base substrate are connected electrically by copper core solder balls. To prevent ball collapse and keep specified distance between upper and base substrate, copper core solder balls are adopted. The space between upper and base substrate is encapsulated by molding resin. And finally, solder balls are mounted on bottom layer.”</p></div> <div><p>“Embedded layer thickness of Type 1 is 72.5um by using 100um diameter copper core solder ball.”</p></div> <div><p>“Embedded layer thickness of Type 2 is 52.5um by using 80um diameter copper core solder ball.”</p></div> <div><p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usq=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p></div>
--	--

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>MCeP discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p>See, e.g.:</p> <div> <p>Structure</p> <p>Standard</p> <p>Mold Resin</p> <p>IC Chip</p> <p>Cu Core Solder Ball</p> <p>Top Substrate</p> <p>Embedded Layer</p> <p>Bottom Substrate</p> <p>Capacitor</p> </div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p>

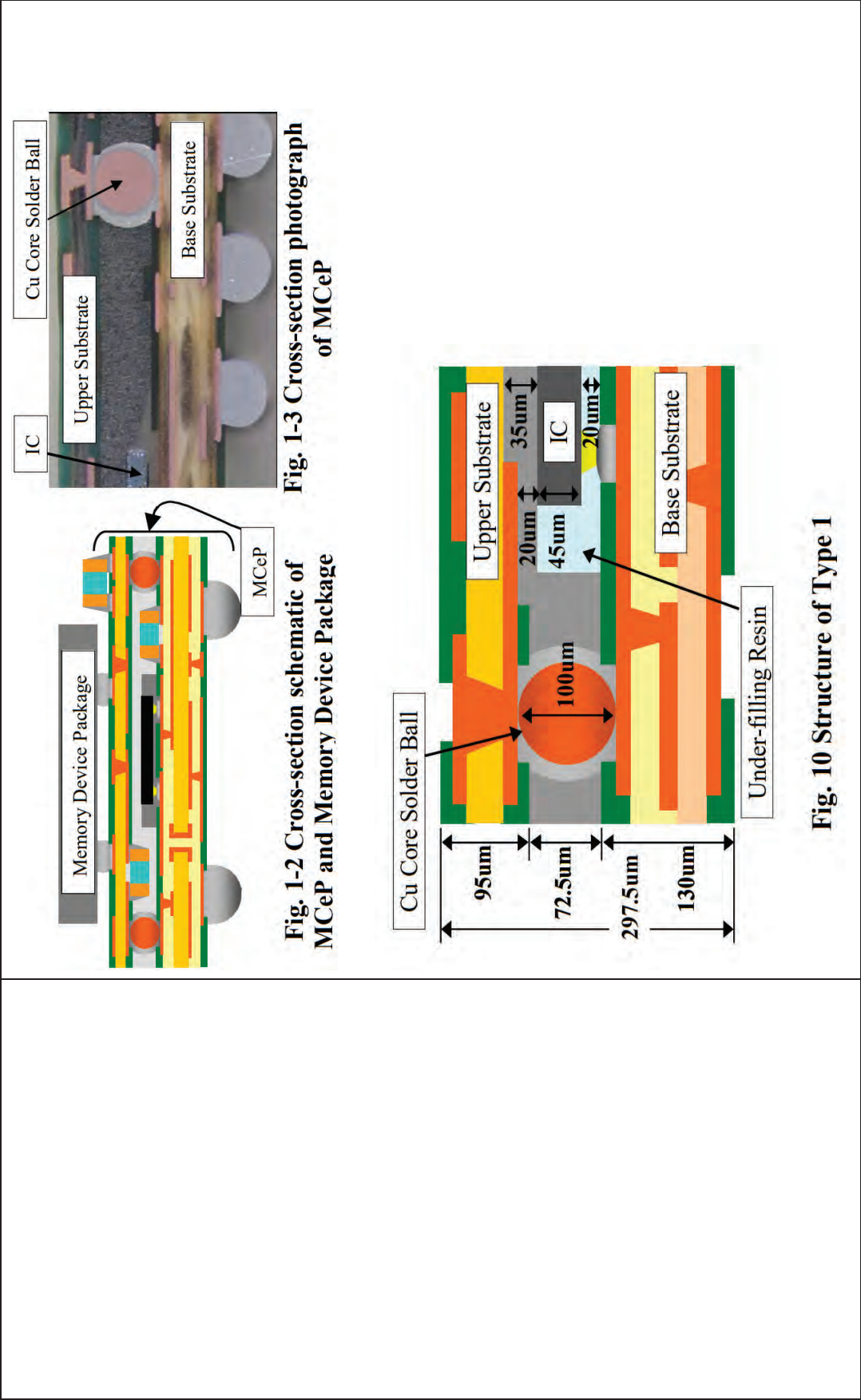
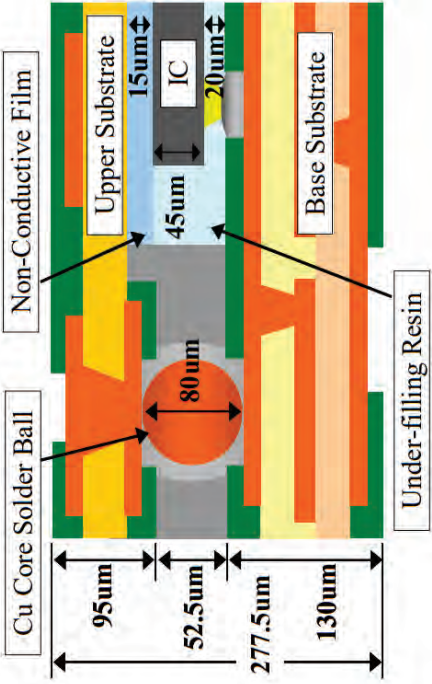


Fig. 10 Structure of Type 1

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	 <p>Fig. 13 Structure of Ultra Thin MCeP Type 2</p> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usq=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal</p>	<p>MCeP discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p>

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

<p>pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<div> <p>See, e.g.:</p> </div> <div> <p>A cross-sectional schematic diagram of a memory device package. It shows a central 'Memory Device Package' (a grey rectangle) mounted on a substrate. The substrate has multiple layers, including a top layer with orange and yellow regions, and a bottom layer with orange and yellow regions. A 'Cu Core Solder Ball' is shown at the bottom, connected to the substrate. An 'IC' (Integrated Circuit) is shown on the left side of the substrate. A 'Base Substrate' is shown at the bottom. An arrow points from the 'Memory Device Package' to the 'Cu Core Solder Ball'.</p> </div> <div> <p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p> </div> <div> <p>A cross-sectional photograph of a memory device package. It shows a central 'Memory Device Package' (a grey rectangle) mounted on a substrate. The substrate has multiple layers, including a top layer with orange and yellow regions, and a bottom layer with orange and yellow regions. A 'Cu Core Solder Ball' is shown at the bottom, connected to the substrate. An 'IC' (Integrated Circuit) is shown on the left side of the substrate. A 'Base Substrate' is shown at the bottom. An arrow points from the 'Memory Device Package' to the 'Cu Core Solder Ball'.</p> </div> <div> <p>Fig. 1-3 Cross-section photograph of MCeP</p> </div>
--	--

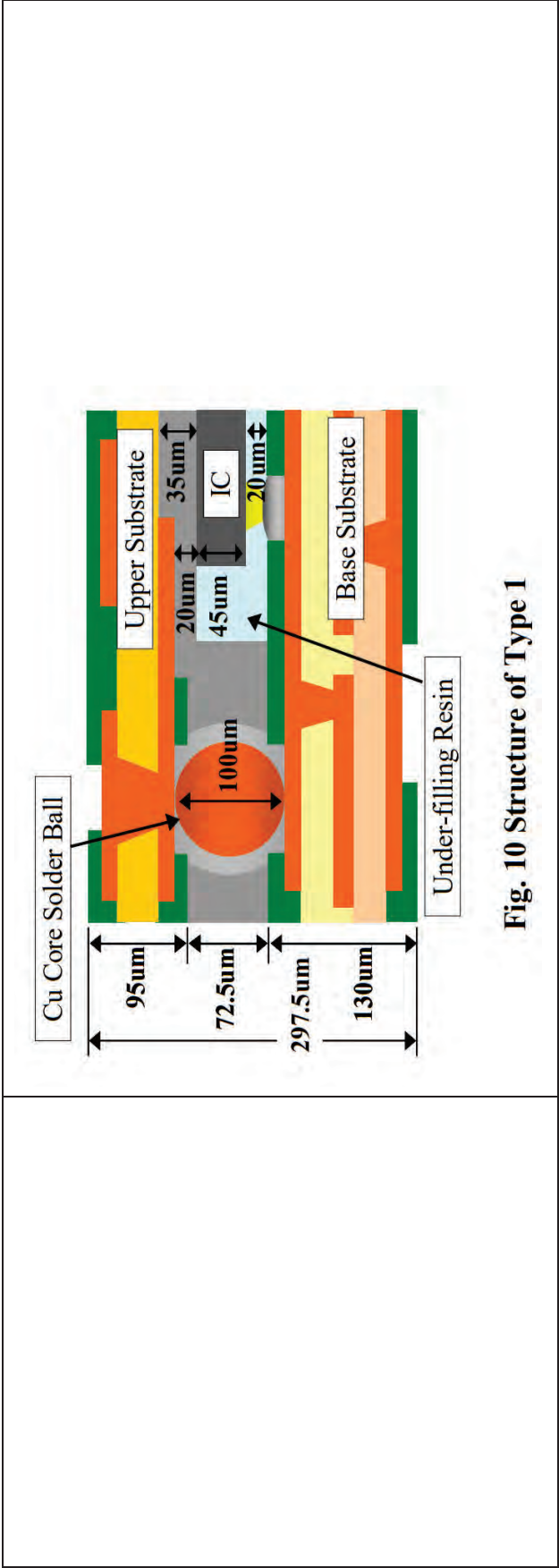
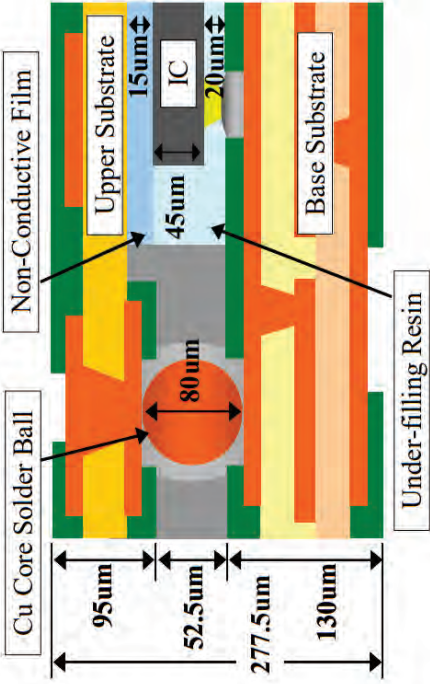


Fig. 10 Structure of Type 1

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	 <p>Fig. 13 Structure of Ultra Thin MCeP Type 2</p> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a</p>	<p>MCeP discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

corresponding metal pillar among the plurality of metal pillars of the spacer connector,

See, e.g.:

Structure

Standard

Mold Resin

IC Chip

Capacitor

Cu Core Solder Ball

Top Substrate

Embedded Layer

Bottom Substrate

Memory Device Package

MCeP

IC

Upper Substrate

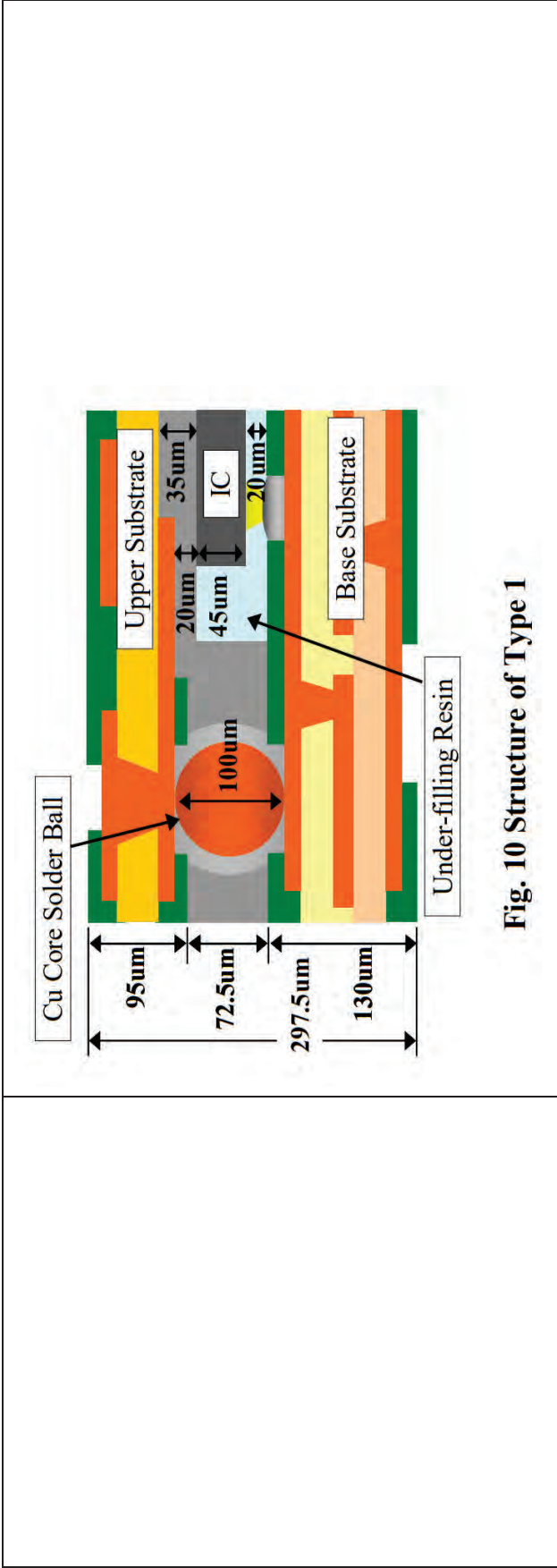
Base Substrate

Cu Core Solder Ball

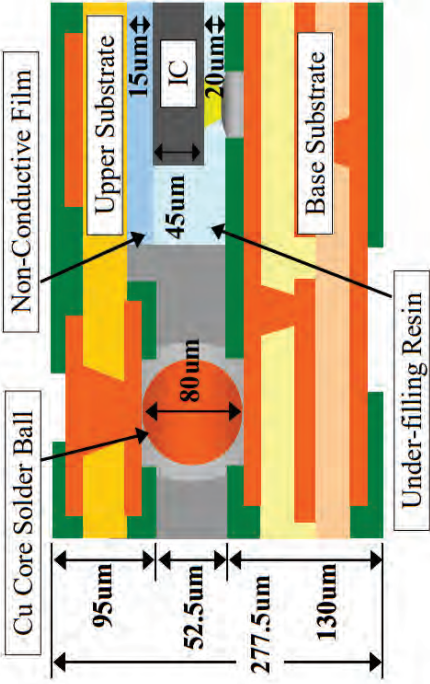
https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf

Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package

Fig. 1-3 Cross-section photograph of MCeP



Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	 <p>Fig. 13 Structure of Ultra Thin MCeP Type 2</p> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwIUI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usq=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a</p>	<p>MCeP discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p>

corresponding metal pillar among the plurality of metal pillars of the spacer connector, and

See, e.g.:

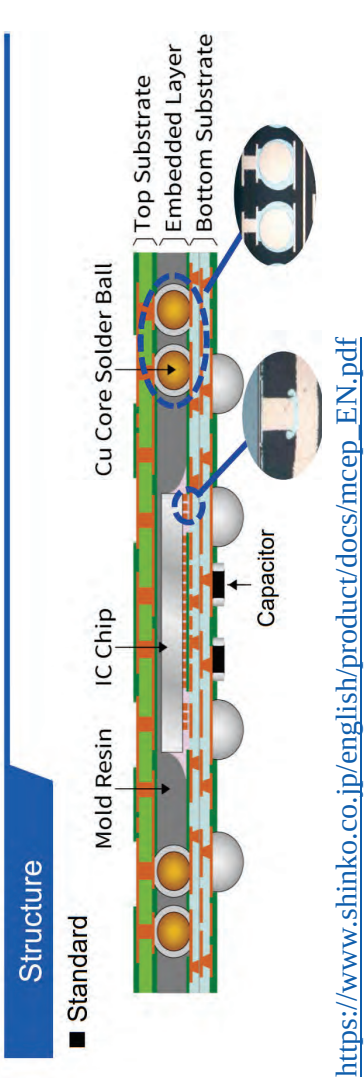
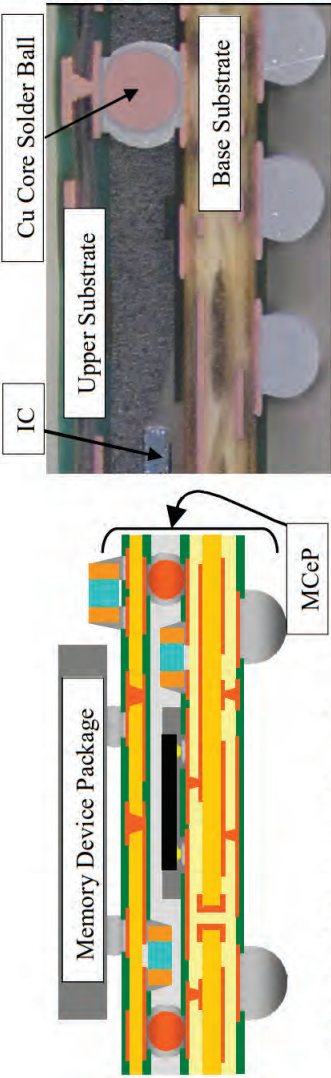
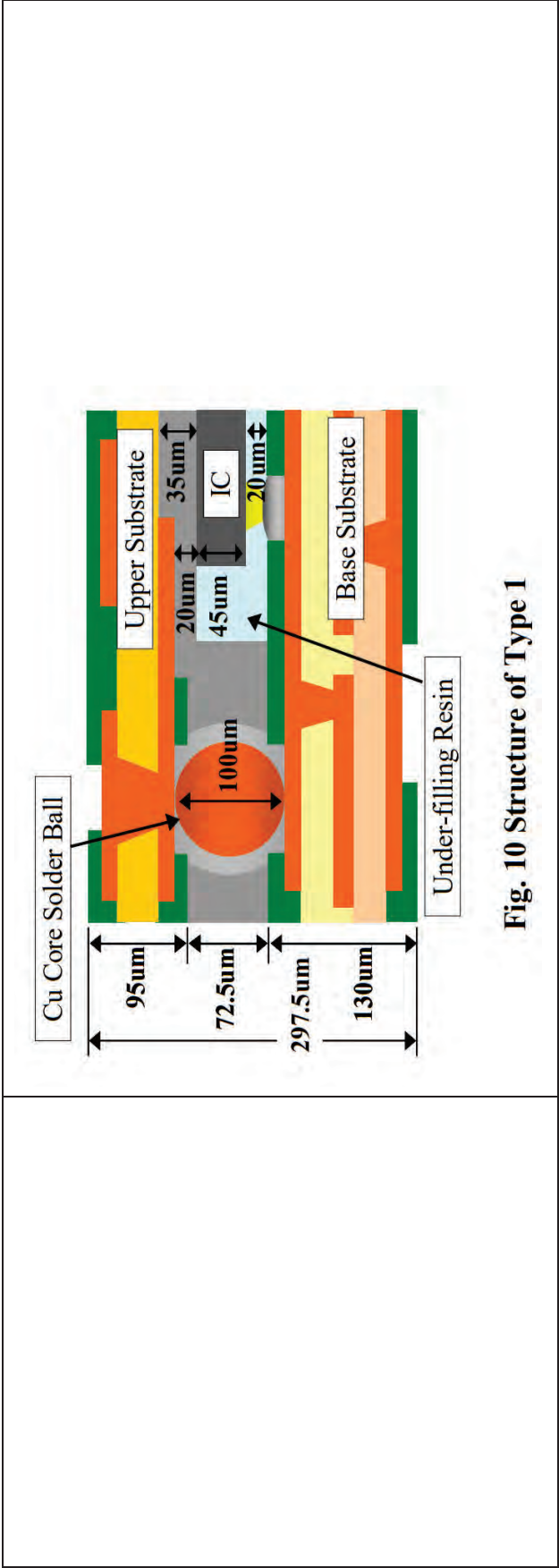
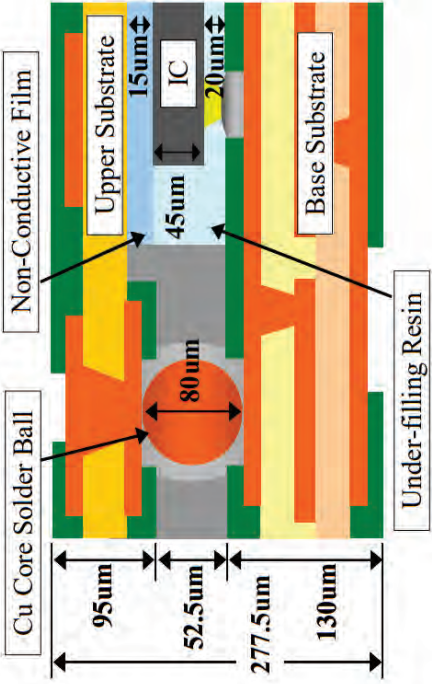


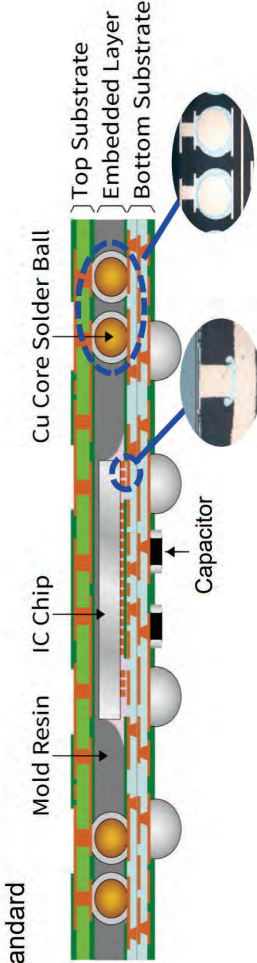
Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package

Fig. 1-3 Cross-section photograph of MCeP



	 <p>Fig. 13 Structure of Ultra Thin MCeP Type 2</p> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwI4sQFn0ECBoQAQ&url=https%3A%2F%2Ffimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usq=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality</p>	<p>MCeP discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package</p>

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

<p>of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, <i>e.g.</i>:</p> <p>“We offer MCeP®(Molded Core embedded Package) with the package structure achieved by active and passive components built in. The package type is also called ‘embedded substrate’ in the market. We provide the package features compact and thin package size, excellent electric characteristics, and high reliability enabled by our own packaging technology.”</p> <p>https://web.archive.org/web/20130215093055/http://www.shinko.co.jp/english/product/sip/mcep.html#link1</p> <div><p>Structure</p><p>■ Standard</p></div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p>
--	---

	<div> </div> <div> </div> <div> <p>Fig. 1-3 Cross-section photograph of MCeP</p> </div> <div> <p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p> </div> <div> <p>“The upper substrate and the base substrate are connected electrically by copper core solder balls.”</p> </div> <div> <p>“The upper substrate had 2 conductive layers and thickness was 95um. The base substrate was a coreless substrate with 3 conductive layers and thickness was 130um.”</p> </div> <div> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> </div> <div> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> </div>
--	--

<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>MCeP discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate.</p> <p>See, <i>e.g.</i>:</p> <div> <p>Structure</p> <p>Standard</p> <p>Mold Resin</p> <p>IC Chip</p> <p>Cu Core Solder Ball</p> <p>Top Substrate</p> <p>Embedded Layer</p> <p>Bottom Substrate</p> <p>Capacitor</p> </div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p> <div> <p>Memory Device Package</p> <p>MCeP</p> <p>IC</p> <p>Upper Substrate</p> <p>Cu Core Solder Ball</p> <p>Base Substrate</p> </div> <p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p> <p>Fig. 1-3 Cross-section photograph of MCeP</p>
--	---

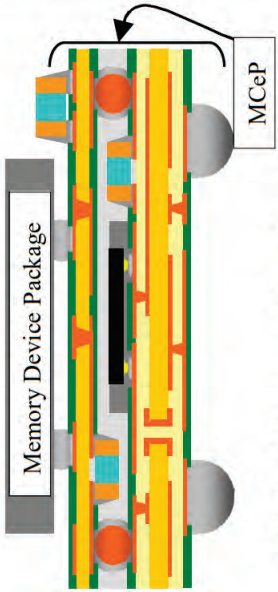
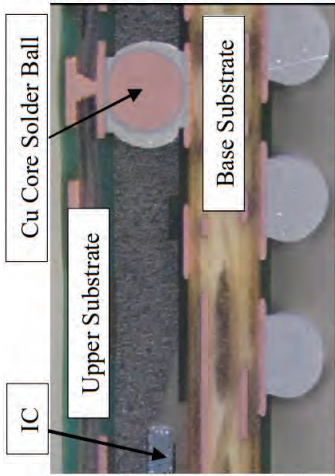
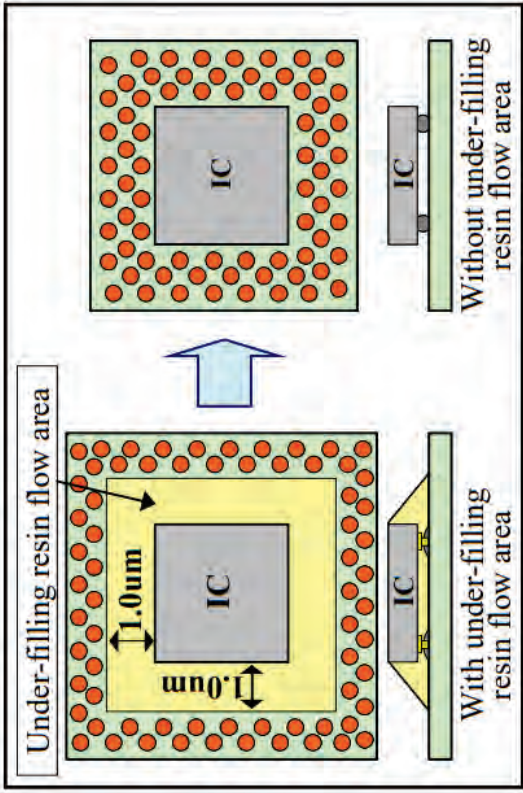
Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHWUJ4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>“MCEP consists of a base substrate, an upper substrate and molding resin. The IC device is sandwiched between upper substrate and base substrate.”</p> <p>“Bare IC devices are mounted on the base substrate using flip chip bonding.”</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>MCeP discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

	<div> <p>Structure</p> <p>Standard</p> <p>Mold Resin</p> <p>IC Chip</p> <p>Cu Core Solder Ball</p> <p>Top Substrate</p> <p>Embedded Layer</p> <p>Bottom Substrate</p> <p>Capacitor</p> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p> </div> <div> <p>IC</p> <p>Upper Substrate</p> <p>Cu Core Solder Ball</p> <p>Base Substrate</p> </div> <div> <p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p> <p>Fig. 1-3 Cross-section photograph of MCeP</p> </div> <div> <p>“MCeP consists of a base substrate, an upper substrate and molding resin. The IC device is sandwiched between upper substrate and base substrate.”</p> <p>“Bare IC devices are mounted on the base substrate using flip chip bonding.”</p> </div>
--	--

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>MCeP discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p>See, e.g.:</p> <div> <p>Structure</p> <p>Standard</p> <p>Mold Resin</p> <p>IC Chip</p> <p>Cu Core Solder Ball</p> <p>Top Substrate</p> <p>Embedded Layer</p> <p>Bottom Substrate</p> <p>Capacitor</p> </div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p>

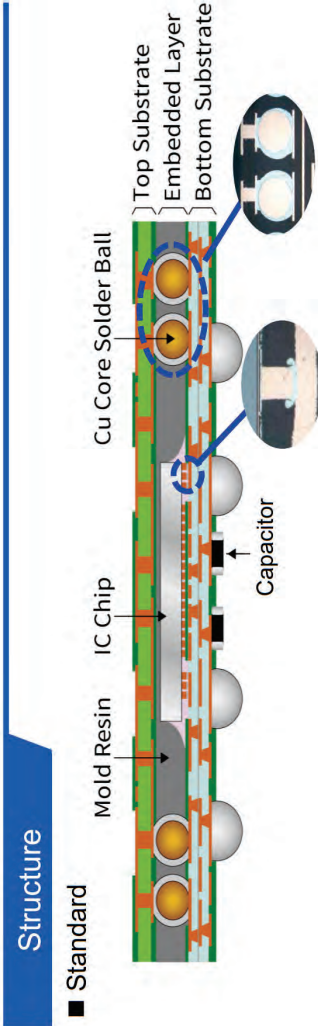
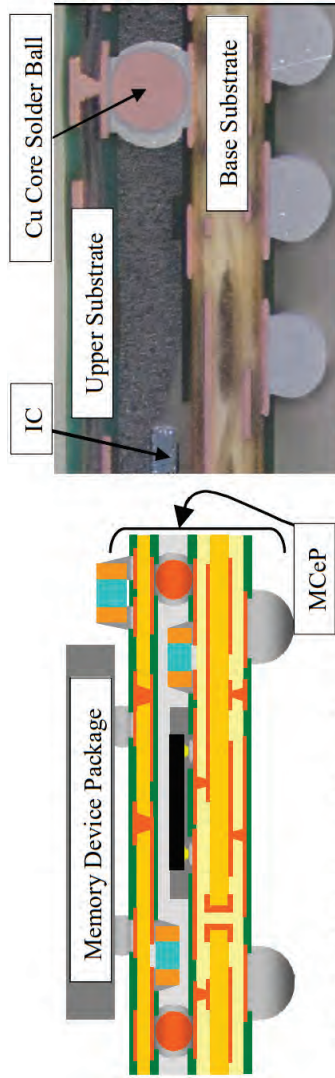
	<div><p>A cross-sectional schematic diagram showing a memory device package assembly. It includes a central IC, an upper substrate, a base substrate, and Cu core solder balls. A label 'MCeP' points to a specific layer or region within the assembly.</p></div> <div><p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p></div> <div><p>A photograph of a cross-section of the MCeP assembly, showing the physical components and their arrangement, corresponding to the schematic in Fig. 1-2.</p></div> <div><p>Fig. 1-3 Cross-section photograph of MCeP</p></div> <div><p>A diagram illustrating the resin flow area under an IC. It shows two scenarios: 'With under-filling resin flow area' and 'Without under-filling resin flow area'. The 'With' scenario shows a resin flow area of 1.0um around the IC, while the 'Without' scenario shows no resin flow area. A label 'Under-filling resin flow area' points to the resin flow area in the 'With' scenario.</p></div> <div><p>Fig. 19 Illustration of under-filling resin flow area</p></div>
--	---

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>“Almost same quantity of copper core solder balls were arranged around IC device, and the package size was shrunk by eliminated of the under-filling flow area.”</p> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwIJJ4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usq=AOvVaw0c7ITbFunP15yBoIYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 2

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>MCeP discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p><i>See, e.g.:</i></p>

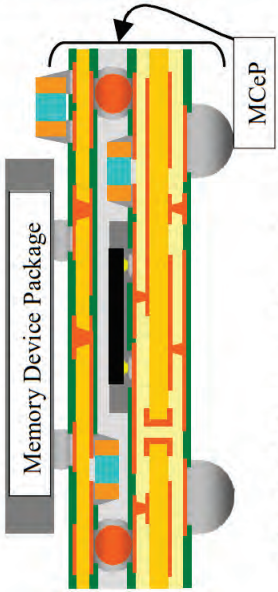
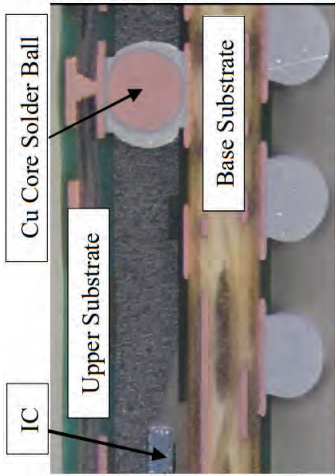
	<div><p>Structure</p></div> <div><p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p></div> <div></div> <div><p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p></div> <div><p>Fig. 1-3 Cross-section photograph of MCeP</p></div> <div><p>“To keep the gap between back side of embedded IC device and upper substrate, IC device was ground down to 45um thickness.”</p></div>
--	--

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

	<p>“To keep the gap between back side of embedded IC device and upper substrate, solder resist and copper pattern of upper substrate which were existing around embedded IC device area were removed.”</p> <p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHWUJl4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

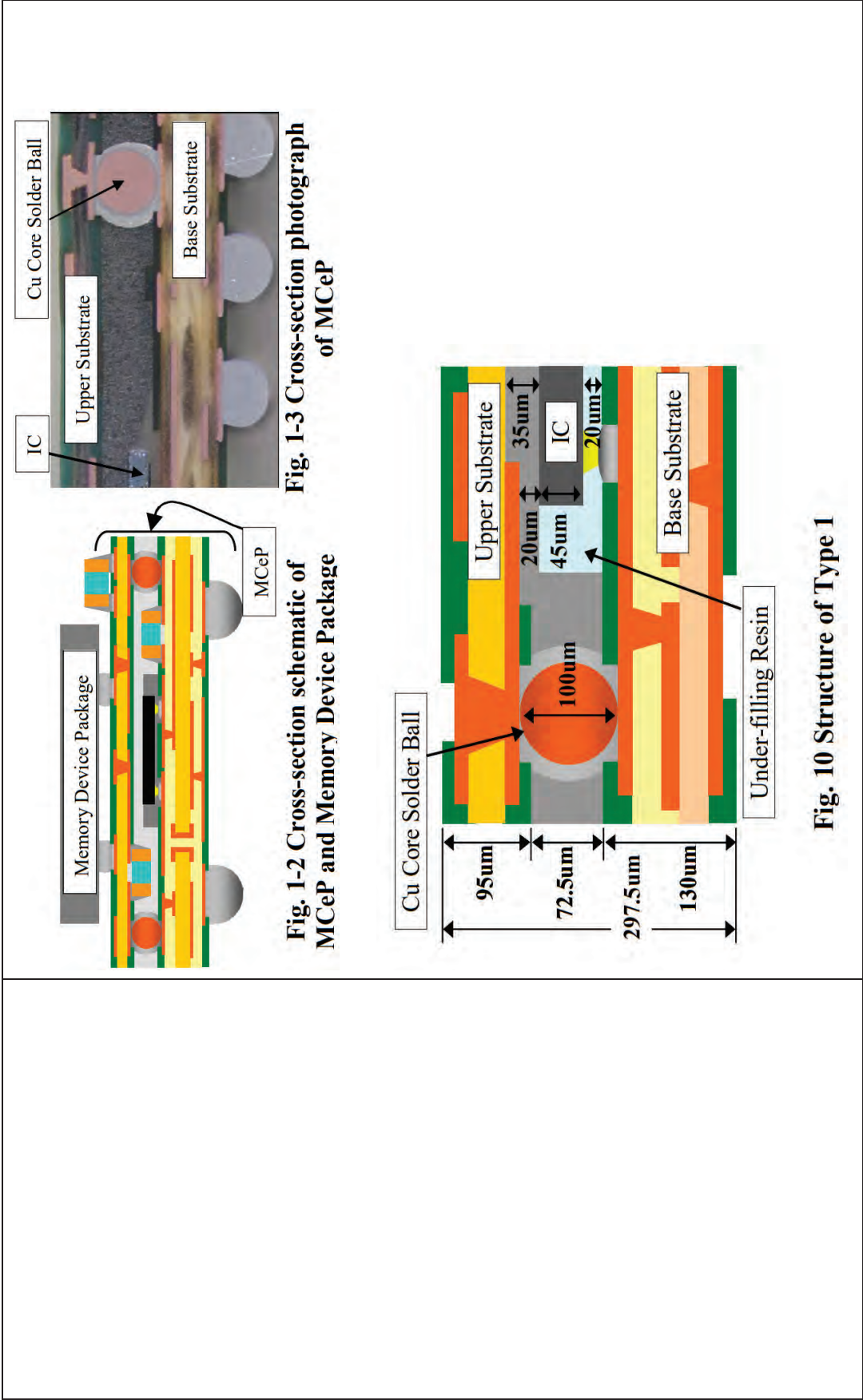
Claim 3

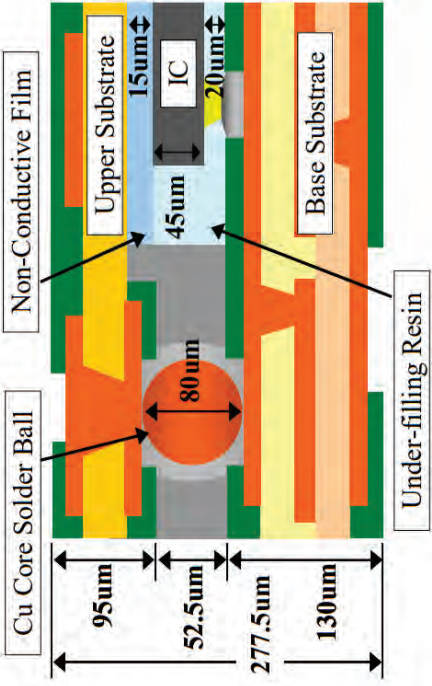
Claim Limitation	Disclosure
<p>[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, <i>e.g.</i>:</p>	<p>MCeP discloses, either expressly or inherently, a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.</p> <p>See, <i>e.g.</i>:</p>

	<div><p>The schematic shows a cross-section of a memory device package (left) and an MCeP package (right). The memory device package has a central black layer with orange and yellow layers above and below it. The MCeP package has a central grey layer with orange and yellow layers above and below it. A label 'MCeP' points to the right package.</p></div> <div><p>Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package</p></div> <div><p>The photograph shows a cross-section of an MCeP package. Labels point to various components: 'IC' points to a small blue component on the left; 'Upper Substrate' points to a yellow layer; 'Cu Core Solder Ball' points to a red circular component; and 'Base Substrate' points to a grey layer at the bottom.</p></div> <div><p>Fig. 1-3 Cross-section photograph of MCeP</p></div> <p>“The bottom package of PoP is usually FC-BGA (Flip Chip Ball Grid Array). The upper package of PoP is usually a memory device package.”</p> <p>“Additionally, MCeP top surface pads are arranged without limitation of IC device layout. Therefore, thinner conventional memory packages can be mounted on MCeP.”</p> <p>https://www.google.com/url?sa=t&rct=i&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAxWbFjQIHwIJI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p> <p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>MCeP discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p> <div> <p>Structure</p> <p>Standard</p> <p>Mold Resin IC Chip Cu Core Solder Ball Top Substrate Embedded Layer Bottom Substrate Capacitor</p> </div> <p>https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf</p>



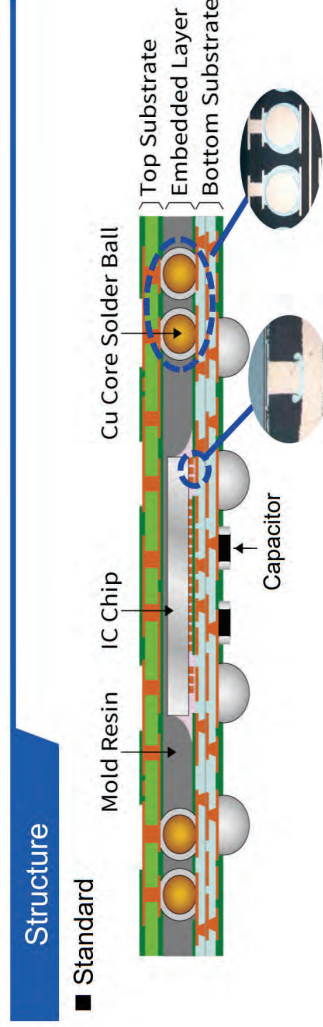
	<div></div> <div><p>Fig. 13 Structure of Ultra Thin MCeP Type 2</p></div> <div><p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-go5SUAxWbFjQIHwIUI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoLYXALBj&opi=89978449</p></div> <div><p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
<p>Claim Limitation</p>	<p>Claim 6</p> <p>Disclosure</p>

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the top package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

MCeP discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

See, e.g.:



https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf

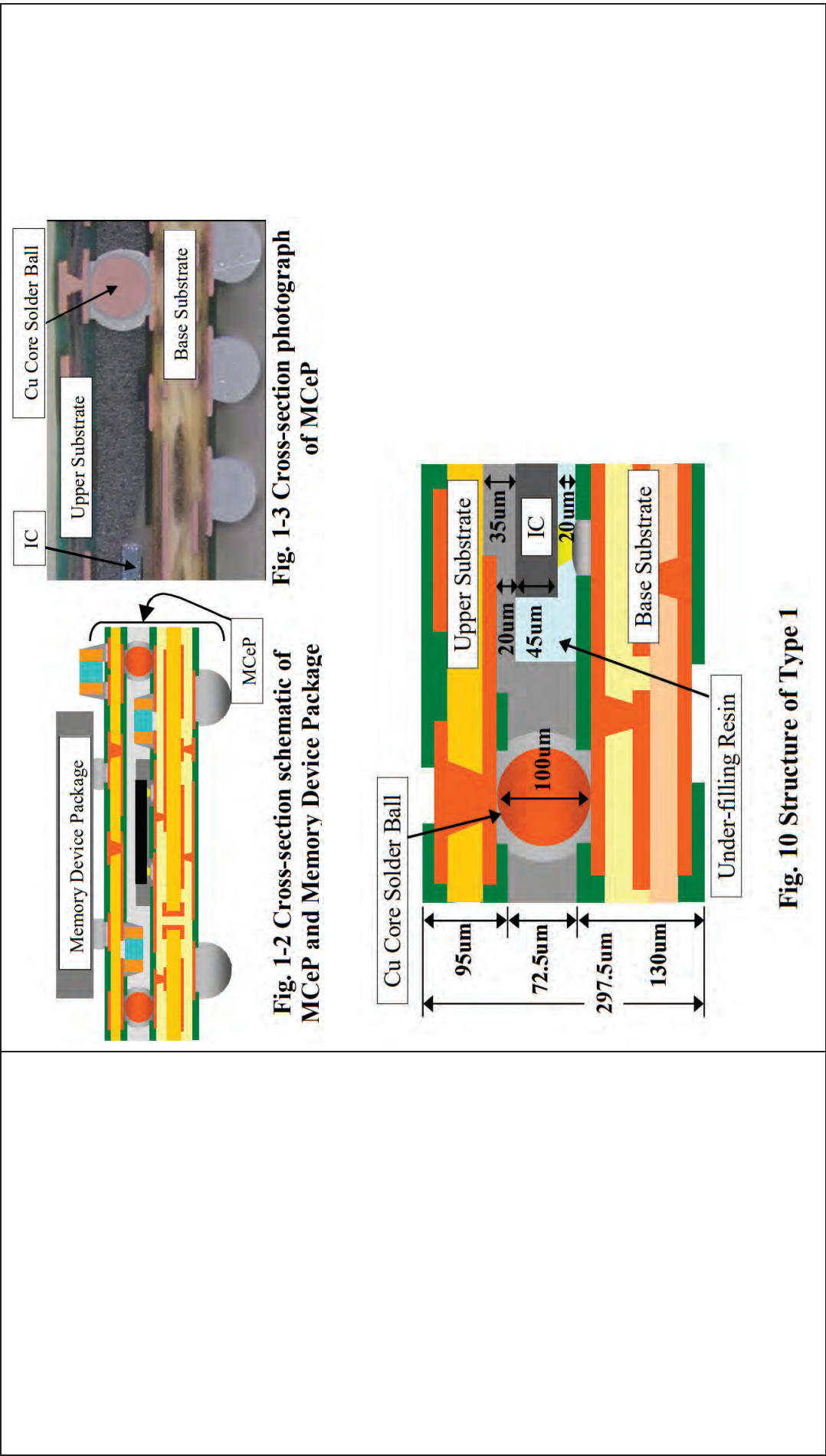


Fig. 10 Structure of Type 1

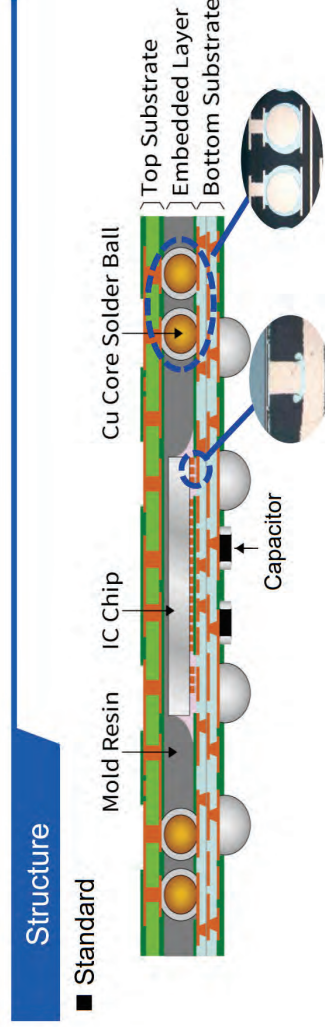
	<div><p>The diagram illustrates the cross-sectional structure of an Ultra Thin MCeP Type 2. It features a central IC (Integrated Circuit) layer, 45um thick, sandwiched between an Upper Substrate (15um) and a Base Substrate (20um). A Cu Core Solder Ball, 95um in diameter, is positioned on the upper substrate. The entire assembly is encapsulated in a Non-Conductive Film. An Under-filling Resin layer, 80um thick, is located beneath the solder ball. The total thickness of the assembly is 277.5um, with a bottom layer of 130um.</p></div> <div><p>Fig. 13 Structure of Ultra Thin MCeP Type 2</p></div> <div><p>https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAXwbfjQIHwIJI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoIXALBj&opi=89978449</p></div> <div><p>To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
<p>Claim Limitation</p>	<p>Disclosure</p>

Appendix A-52 - Invalidity of U.S. Patent No. 9,859,202 in view of MCeP

[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

MCeP discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

See, e.g.:



https://www.shinko.co.jp/english/product/docs/mcep_EN.pdf

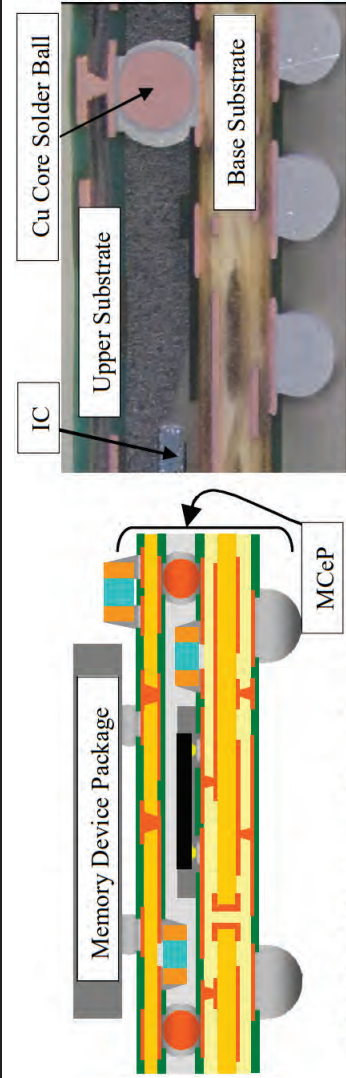


Fig. 1-2 Cross-section schematic of MCeP and Memory Device Package

Fig. 1-3 Cross-section photograph of MCeP

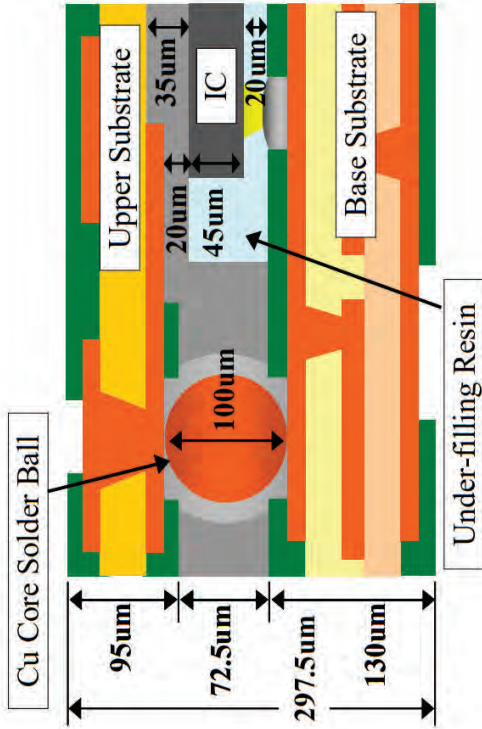


Fig. 10 Structure of Type 1

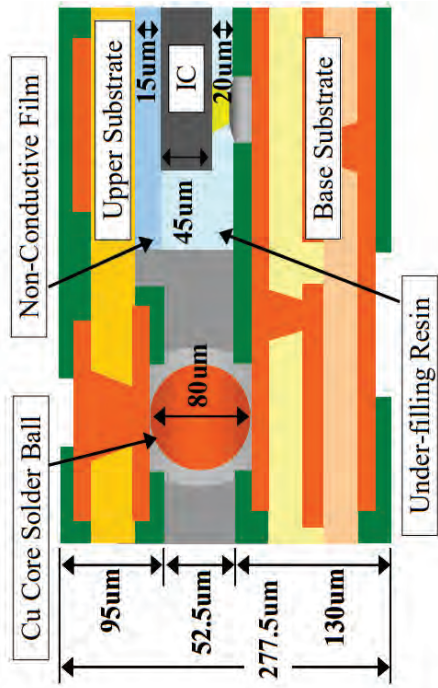


Fig. 13 Structure of Ultra Thin MCeP Type 2

<https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwjbr6-qo5SUAXwbfjQIHwIJI4sQFnoECBoQAQ&url=https%3A%2F%2Fimapsource.org%2Farticle%2F56464-thinner-and-miniaturization-embedded-device-package-mcep-for-pop-and-module-application.pdf&usg=AOvVaw0c7ITbFunP15yBoIXALBj&opi=89978449>

To the extent Plaintiff contends that MCeP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4–6

E.D. Tex. Case No. 2:25-cv-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4–6

The Apple iPhones, including but not limited to iPhone 4, 4S, 5, 5C, 5S, 6, and 6 Plus, which implement Apple application processors, including but not limited to A4, A5, A6, A7, and A8 (hereinafter “Apple iPhone 4–6”) was in public use, on sale (including sold to customers and potential customers), and/or otherwise available to the public by Apple Inc. at least by 2014.¹ Apple iPhone 4–6 anticipates and/or renders obvious all Asserted Claims² of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.³ Apple iPhone 4–6, or the written materials describing it, excerpted below, is prior art to the ’202 Patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within Apple iPhone 4–6, or otherwise rendered obvious by disclosures and teachings of Apple iPhone 4–6, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that Apple iPhone 4–6 does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of Apple iPhone 4–6 with: (1) the knowledge of one of ordinary skill in the art (“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 Patent. TopWire has yet to identify any limitation of the Asserted

¹ See, e.g., <https://en.wikipedia.org/wiki/IPhone#Models>; https://apple.fandom.com/wiki/List_of_Apple_processors; <https://everymac.com/systems/apple/iphone/iphone-faq/iphone-processor-types.html>

² As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

³ To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4–6

Claims that it contends is not fully disclosed by Apple iPhone 4–6, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that Apple iPhone 4–6 “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

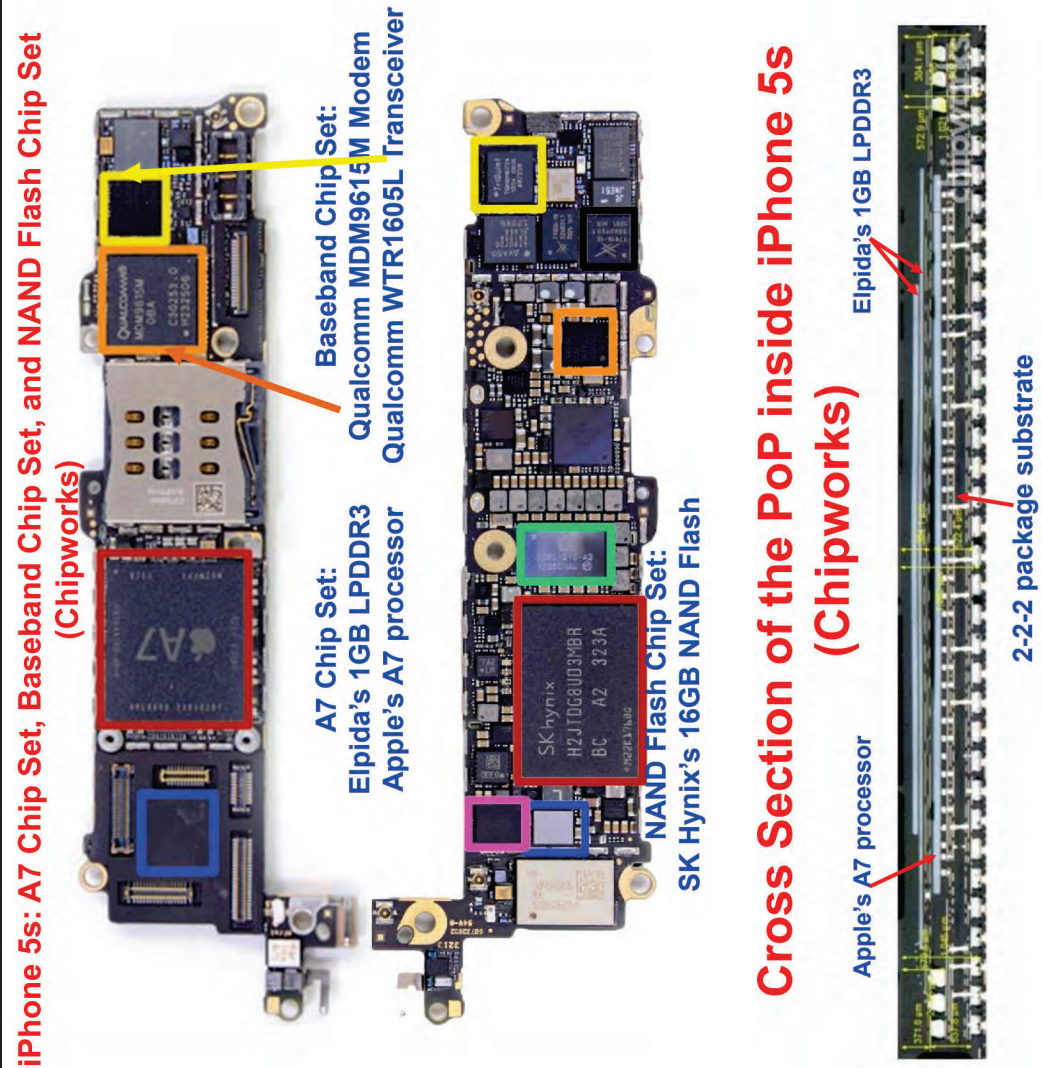
Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to Apple iPhone 4–6 or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding Apple iPhone 4–6 set forth in this chart.

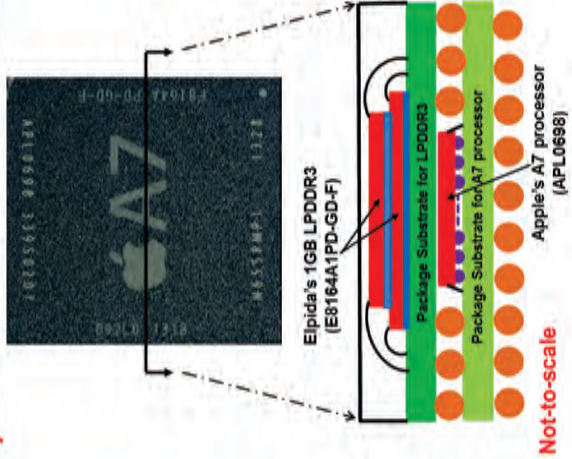
Claim 1

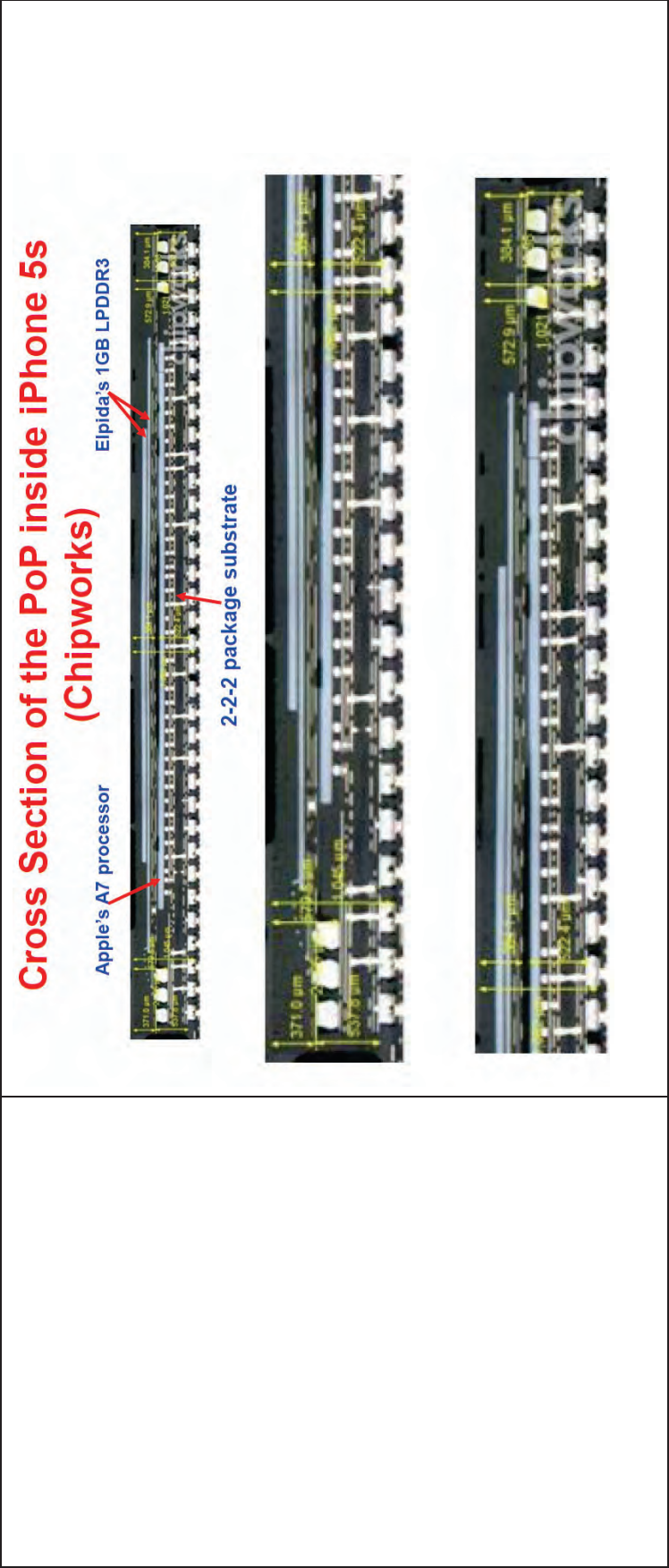
Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, Apple iPhone 4–6 discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>

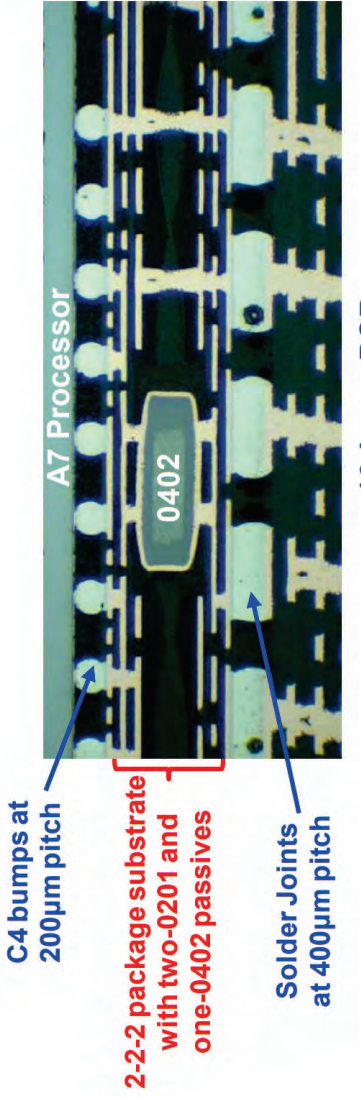
Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4-6

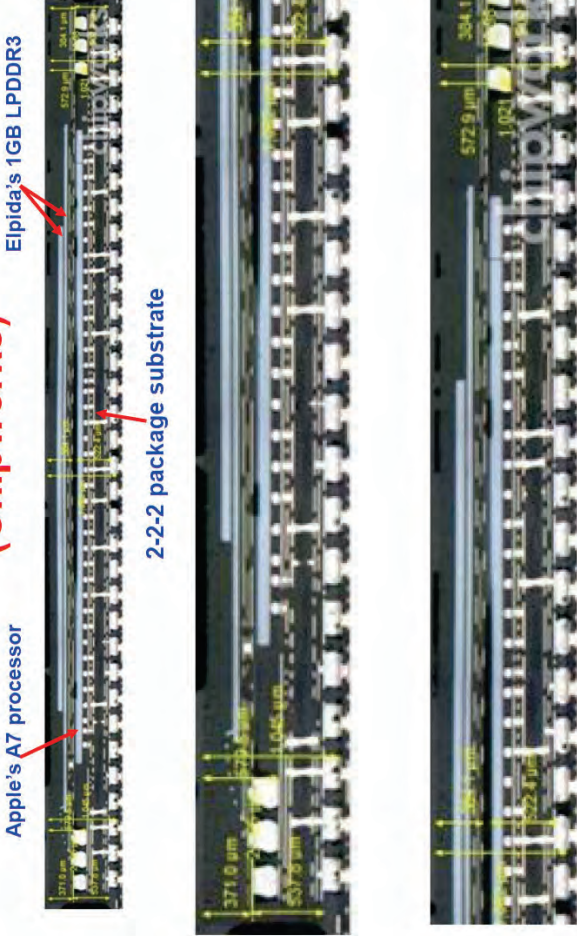


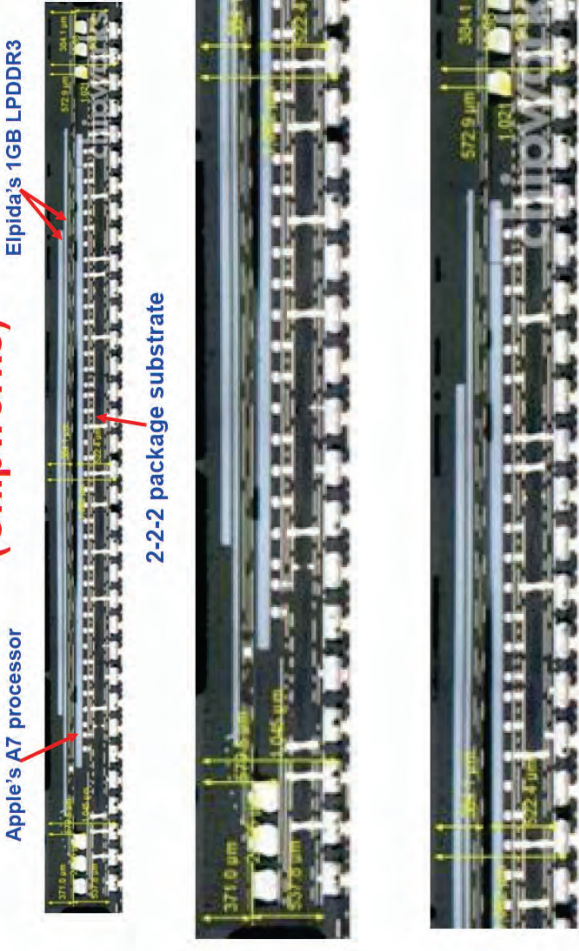


	<p>(Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the PoP</p>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.A] a bottom package substrate;</p>	<p>Apple iPhone 4-6 discloses, either expressly or inherently, a bottom package substrate.</p> <p>See, e.g.:</p>



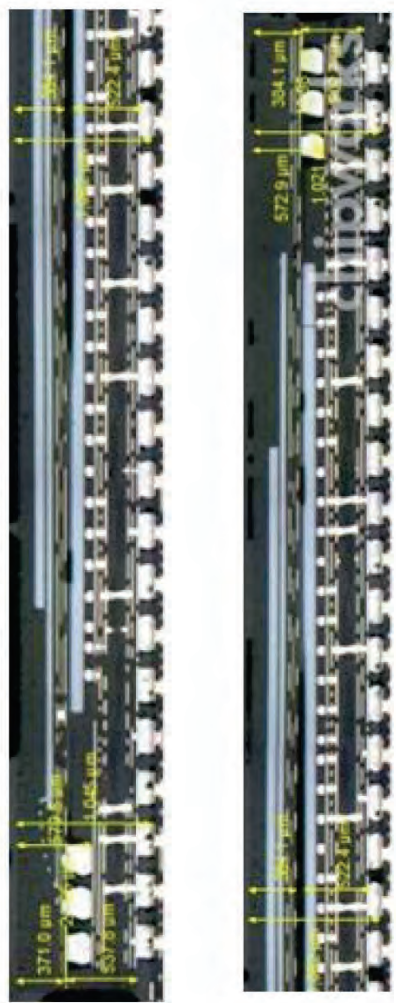
	 <p>10-Layer PCB</p> <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p>
<p>[1.B] a top package substrate stacked on top of the bottom package substrate;</p>	<p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Apple iPhone 4-6 discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.</p> <p>See, e.g.:</p>

	<p>Cross Section of the PoP inside iPhone 5s (Chipworks)</p>  <p>Apple's A7 processor</p> <p>Elpida's 1GB LPDDR3</p> <p>2-2-2 package substrate</p> <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom</p>	<p>Apple iPhone 4-6 discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.</p>

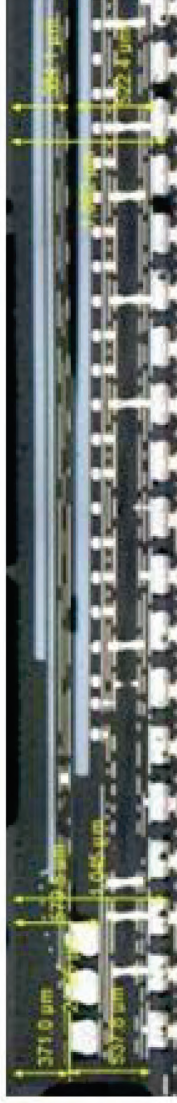
<p>package substrate and the top package substrate, wherein</p>	<p>See, e.g.:</p> <div><p>Cross Section of the PoP inside iPhone 5s (Chipworks)</p><p>Apple's A7 processor</p><p>Elpida's 1GB LPDDR3</p><p>2-2-2 package substrate</p></div> <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
---	--

<p>[1.D] the spacer connector comprises a core substrate;</p>	<p>Apple iPhone 4-6 discloses, either expressly or inherently, the spacer connector comprises a core substrate.</p> <p>See, e.g.:</p> <div><p>Cross Section of the PoP inside iPhone 5s (Chipworks)</p><p>Apple's A7 processor</p><p>Elpida's 1GB LPDDR3</p><p>2-2-2 package substrate</p></div>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with</p>
---	--

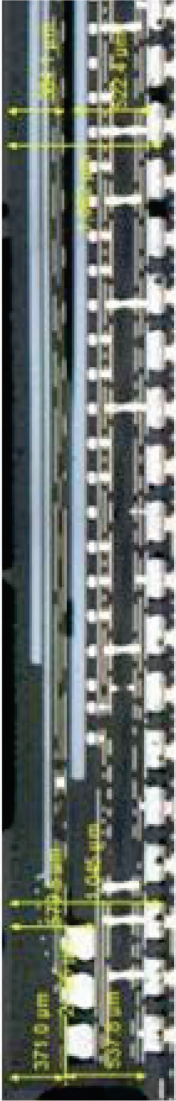
Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4-6

<p>[1.E.] a plurality of metal pillars, each passing through the core substrate; and</p>	<p>(i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p> <p>Apple iPhone 4–6 discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p>See, e.g.:</p> <div> <p>Cross Section of the PoP inside iPhone 5s (Chipworks)</p>  <p>Apple's A7 processor</p> <p>Elpida's 1GB LPDDR3</p> <p>2-2-2 package substrate</p> </div>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p>
--	--

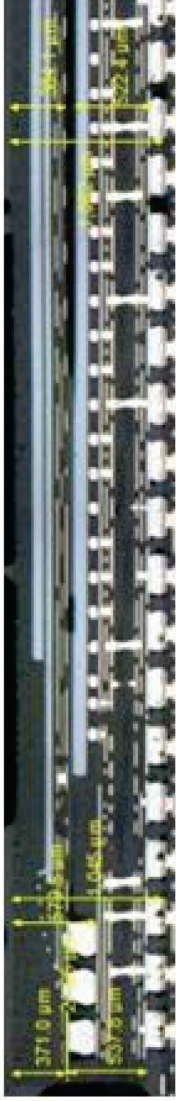
Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4-6

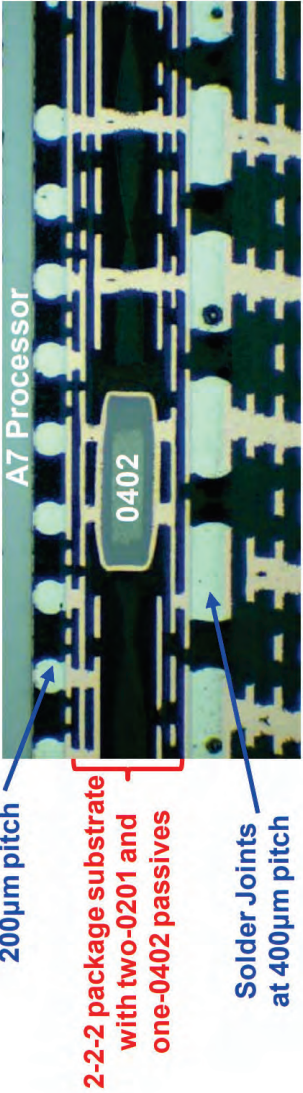
	<p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>Apple iPhone 4-6 discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p>See, e.g.:</p>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>Apple iPhone 4-6 discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p>See, e.g.:</p>

Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4–6

	<p>See, e.g.:</p>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4–6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>Apple iPhone 4–6 discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> <p>See, e.g.:</p> 

Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4–6

	<p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4–6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>Apple iPhone 4–6 discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p>See, e.g.:</p> 

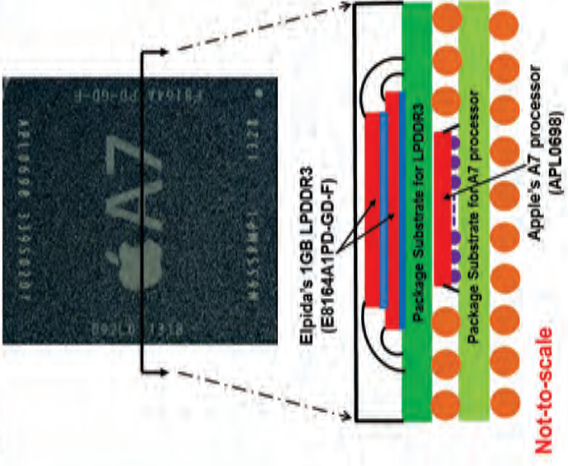
	 <p>A7 Processor</p> <p>10-Layer PCB</p> <p>C4 bumps at 200µm pitch</p> <p>2-2-2 package substrate with two-0201 and one-0402 passives</p> <p>Solder Joints at 400µm pitch</p> <p>0402</p> <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>Apple iPhone 4-6 discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p>See, e.g.:</p>

Cross Section of the PoP inside iPhone 5s (Chipworks)

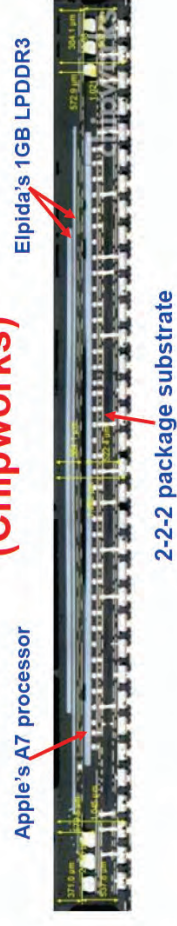


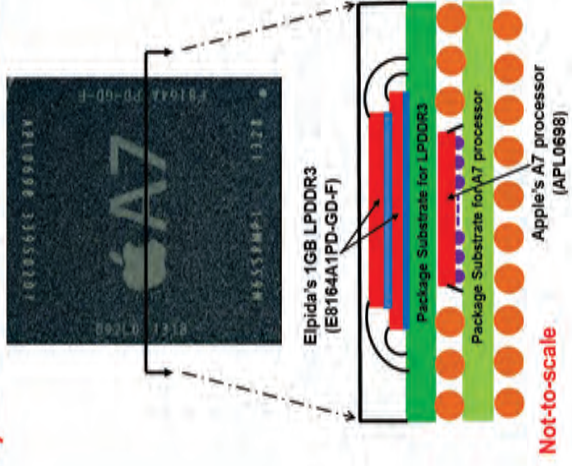
2-2-2 package substrate

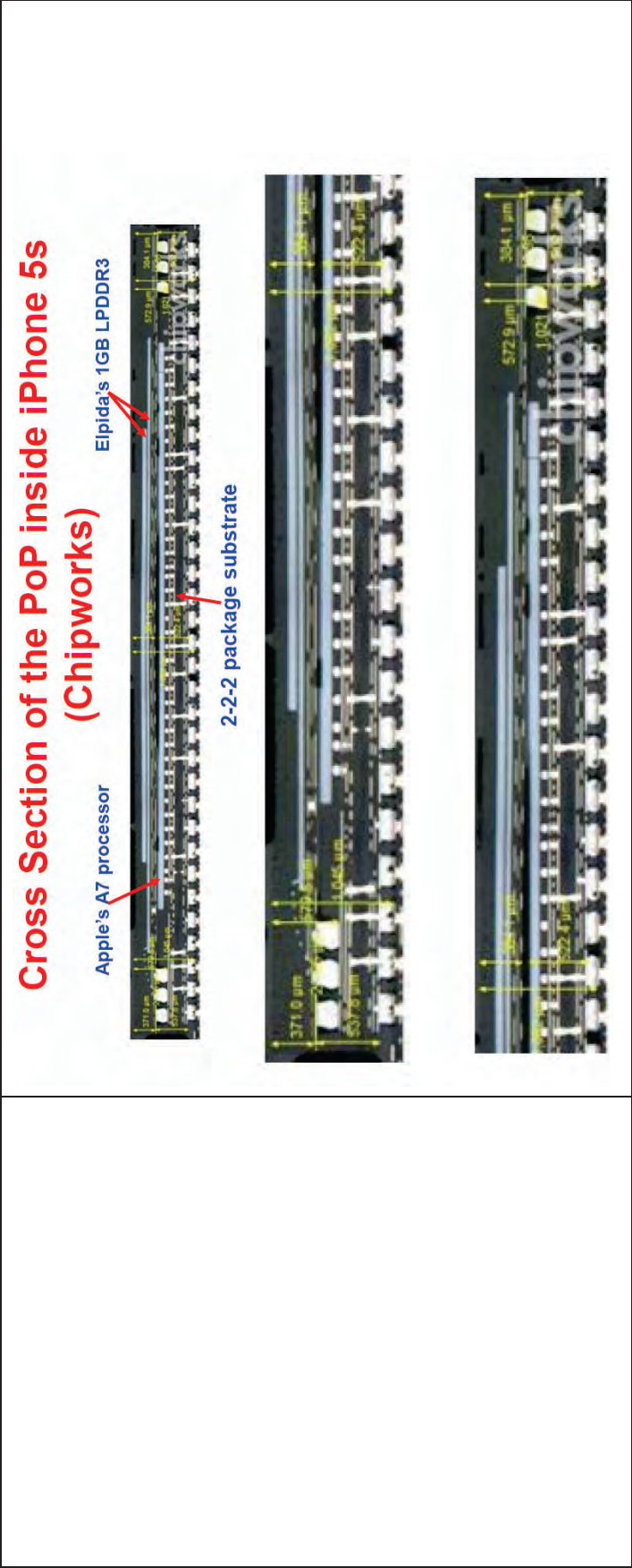


	<p>(Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the PoP</p>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>Apple iPhone 4-6 discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate.</p> <p>See, e.g.:</p>

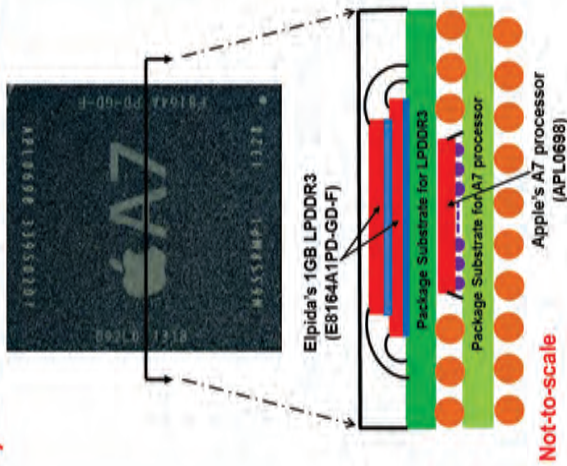
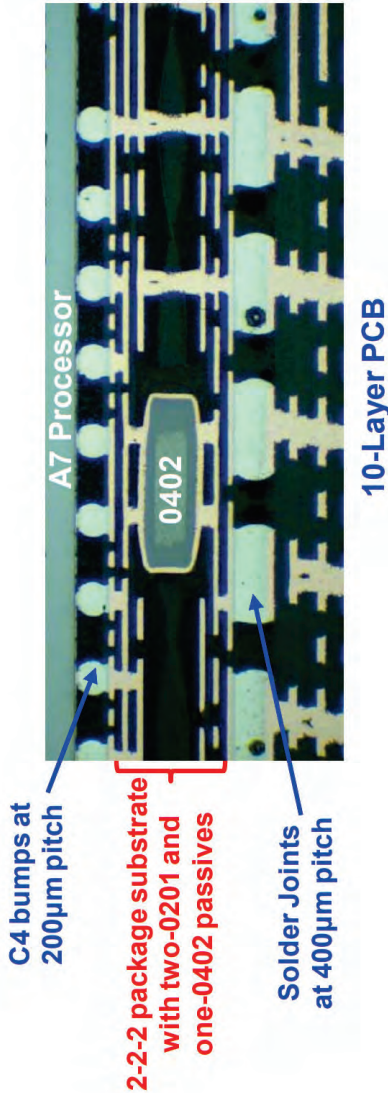
Cross Section of the PoP inside iPhone 5s (Chipworks)



	<p>(Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the PoP</p>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>Apple iPhone 4-6 discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p>See, e.g.:</p>



**(Top) The top view of the A7 processor/memory PoP.
(Bottom) Cross section view of the PoP**



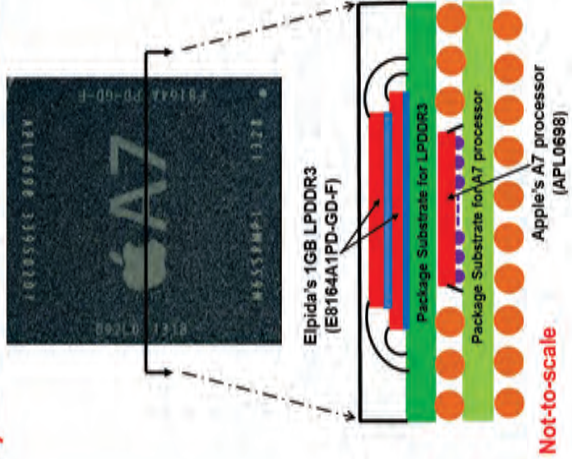
Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4–6

	<p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4–6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>Apple iPhone 4–6 discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

	<div><p>Cross Section of the PoP inside iPhone 5s (Chipworks)</p></div> <div><div>Apple's A7 processor</div><div>Elpida's 1GB LPDDR3</div><div><p>Diagram showing a cross-section of the PoP assembly. The A7 processor is on the left, and the LPDDR3 memory is on the right. Dimensions are provided for various layers and components.</p></div><div>2-2-2 package substrate</div></div> <div><p>Diagram showing a cross-section of the PoP assembly. The A7 processor is on the left, and the LPDDR3 memory is on the right. Dimensions are provided for various layers and components.</p></div> <div><p>Diagram showing a cross-section of the PoP assembly. The A7 processor is on the left, and the LPDDR3 memory is on the right. Dimensions are provided for various layers and components.</p></div> <div><p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p></div> <div><p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p></div>
--	--

Claim 2

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	<p>Apple iPhone 4-6 discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.</p> <p>See, e.g.:</p> <p>Cross Section of the PoP inside iPhone 5s (Chipworks)</p> <p>Apple's A7 processor</p> <p>Elpida's 1GB LPDDR3</p> <p>2-2-2 package substrate</p>

	<p>(Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the PoP</p>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 3

Claim Limitation	Disclosure
------------------	------------

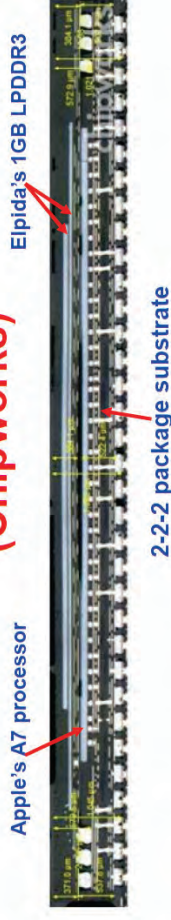
Appendix A-53 - Invalidity of U.S. Patent No. 9,859,202 in view of Apple iPhone 4-6

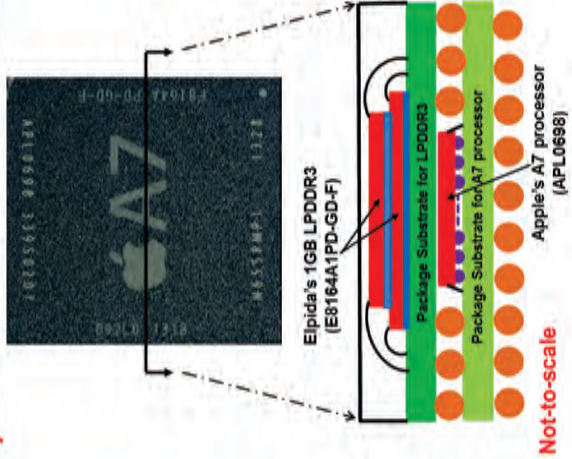
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

Apple iPhone 4–6 discloses, either expressly or inherently, a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.

See, e.g.:

Cross Section of the PoP inside iPhone 5s (Chipworks)



	<p>(Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the PoP</p>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 4

Claim Limitation	Disclosure
------------------	------------

[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

Apple iPhone 4-6 discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.

See, e.g.:

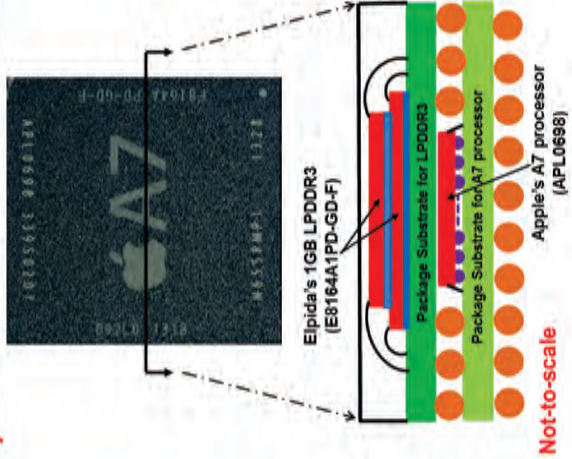
Cross Section of the PoP inside iPhone 5s (Chipworks)

Apple's A7 processor

Elpida's 1GB LPDDR3

2-2-2 package substrate

The diagram shows a cross-section of a 2-2-2 package substrate. It consists of three main layers: a top package substrate, a spacer connector, and a bottom package substrate. Metal pillars are shown extending through these layers, ensuring alignment between the top and bottom package substrates. The top package substrate contains Apple's A7 processor and Elpida's 1GB LPDDR3 memory. Dimensions are provided for various layers and pillars, including 371.0 μm, 577.9 μm, 1.045 μm, 368.1 μm, 572.9 μm, 1.021 μm, 354.1 μm, and 322.4 μm.

	<p>(Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the PoP</p>  <p>Not-to-scale</p> <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 6

Claim Limitation	Disclosure
------------------	------------

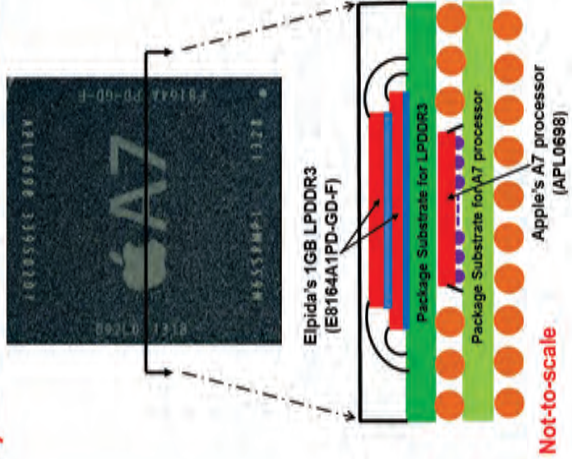
[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Apple iPhone 4-6 discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

See, e.g.:

Cross Section of the PoP inside iPhone 5s (Chipworks)



	<p>(Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the PoP</p>  <p>https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf</p> <p>To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Claim 9

Claim Limitation	Disclosure
------------------	------------

[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

Apple iPhone 4-6 discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.

See, e.g.:

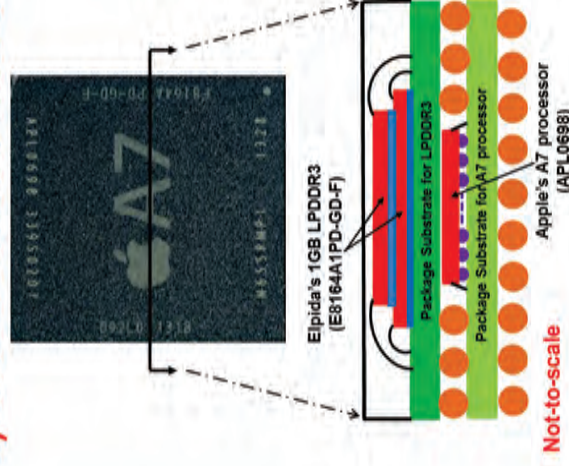
Cross Section of the PoP inside iPhone 5s (Chipworks)

Apple's A7 processor

Elpida's 1GB LPDDR3

2-2-2 package substrate

**(Top) The top view of the A7 processor/memory PoP.
(Bottom) Cross section view of the PoP**



https://www.electronics.org/system/files/technical_resource/E15%26S33_03.pdf

To the extent Plaintiff contends that Apple iPhone 4-6 fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

E.D. Tex. Case No. 2:25-cv-1183

INVALIDITY CLAIM CHART

Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

The Package-Interposer-Package (hereinafter “EIT PIP”) was in public use, on sale (including sold to customers and potential customers), and/or otherwise available to the public by Endicott Interconnect Technologies, Inc at least by 2012. For example, on information and belief, at the 45th International Symposium on Microelectronics held in September 2012 in San Diego, California, an EIT PIP sample was publicly exhibited by Endicott Interconnect Technologies as part of its packaging portfolio at the booth 526 under categories, including “3D IC and Packaging Technologies, TSV” and “Electronic Packages & Packaging” in the official conference directory.¹ EIT PIP anticipates and/or renders obvious all Asserted Claims² of U.S. Patent No. 9,859,202 (“the ’202 Patent”) under 35 U.S.C. §§ 102 and/or 103, including under Plaintiff’s apparent infringement theory.³ EIT PIP, or the written materials describing it, excerpted below, is prior art to the ’202 Patent under at least 35 U.S.C. § 102(a)(1).

The chart below provides representative examples of where each element of each Asserted Claim is found within EIT PIP, or otherwise rendered obvious by disclosures and teachings of EIT PIP, including under TopWire’s apparent interpretation of the Asserted Claims as Samsung understands them from TopWire’s Infringement Contentions served March 12, 2026. The cited evidence is merely illustrative, and Samsung reserves the right to cite alternative or additional evidence. To the extent TopWire contends that EIT PIP does not disclose any claim elements of the Asserted Claims, it would have been obvious to combine the teachings of EIT PIP with: (1) the knowledge of one of ordinary skill in the art

¹ See, e.g., <https://imaps.org/page/PastEvents>;

https://cdn.ymaws.com/imaps.org/resource/resmgr/documents/symposium_programs/imaps2012final.pdf; <https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration>

² As used herein, “Asserted Claims” refers only to those claims charted in TopWire’s March 12, 2026 Infringement Contentions. To the extent TopWire later obtains leave to assert any additional claims for this patent, Samsung will provide its preliminary Invalidity Contentions consistent with the timing requirements set forth in the Court’s order.

³ To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Samsung is not proposing any such constructions as proper constructions of those terms or phrases. Various positions put forth in this document are predicated on TopWire’s apparent interpretation of the Asserted Claims as evidenced by its Infringement Contentions provided to Samsung. Samsung does not agree or acquiesce to any such interpretation by TopWire. The positions presented herein are not intended to and do not necessarily reflect Samsung’s interpretation of the true and proper scope of the Asserted Claims, and Samsung reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

(“POSITA”) to show all the limitations of the claims; (2) the teachings of any of the prior art references set forth in Samsung’s other invalidity charts with respect to the one or more limitations; and/or (3) the teachings of any of the prior art references set forth in the cover document of Samsung’s Invalidity Contentions with respect to the ’202 Patent. TopWire has yet to identify any limitation of the Asserted Claims that it contends is not fully disclosed by EIT PIP, either alone or in combination with other prior art cited by Samsung and/or with the knowledge of a POSITA. To the extent TopWire makes any such contention in the future, Samsung expressly reserves the right to rebut any such contention, including by identifying additional obviousness combinations.

Where the chart below states that EIT PIP “discloses” a limitation, such disclosure may be express or inherent. All emphases are added unless otherwise indicated.

Fact Discovery is ongoing and Samsung’s prior art investigation, including via third party discovery, is therefore not yet complete. Samsung reserves the right to rely upon additional evidence of invalidity obtained in the future as to EIT PIP or any other prior art public use/sales/offers for sale that may anticipate or render obvious one or more claim limitations of the Asserted Claims under 35 U.S.C. §§ 102 and/or 103. Samsung may rely on additional documents and/or things that have not yet been located and/or testimony to support the contentions regarding EIT PIP set forth in this chart.

Claim 1

Claim Limitation	Disclosure
[1.PRE] A structure, comprising:	To the extent the preamble is a limitation, EIT PIP discloses, either expressly or inherently, a structure. <i>See, e.g.:</i>

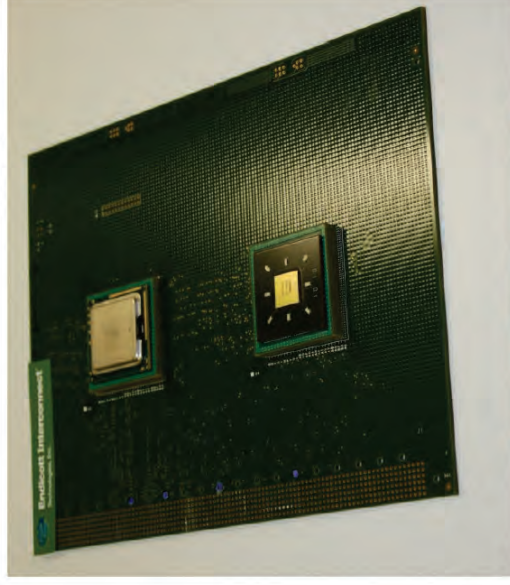
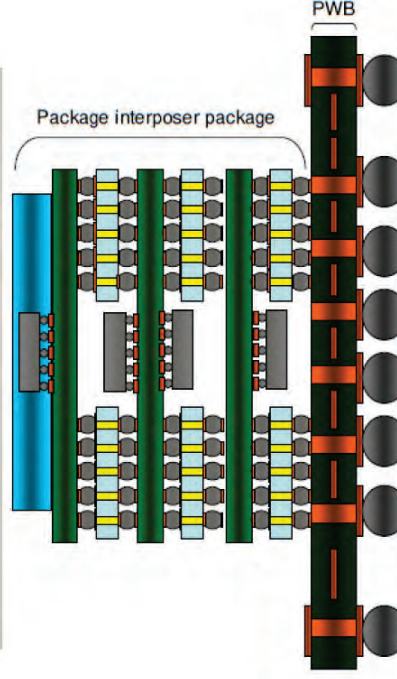


Figure 14: Photograph and schematic representation of PIP attached with low end board.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“A PIP was constructed using an interposer consisting of multiple metal inner planes. A top view of the contacting pads for this interposer is shown schematically in Figure 5.”</p> <p>“As part of an on-going effort to develop new electrical interconnection between the interposer and the package on either side of the interposer, connections can be made by a Figure 5. Top view of interposer A PIP was constructed using an interposer consisting of multiple metal inner planes. A top view of the contacting.”</p> <p>“Figure 6. Process flow for a PIP construction. The interposer has an opening. The top side of the bottom package is connected with the bottom side of the interposer in such a way that die on the bottom package resides within the opening of the interposer. The bottom side of the top package is connected with the top side of the interposer in a subsequent step to complete the PIP structure.”</p> <p>“As stated above, ECA-filled interposers can also be used to produce a PIP structure. High temperature/pressure lamination is used to cure the adhesive in the PIP and provide electrical interconnection among the packages. A variety of interposer structures such as OS/1P, OS/2P, 2S/1P, 2S/2P can be used. Figure 8 shows optical photographs and SEM micrographs of a joining core having ECA-filled holes with diameters ranging from 55 μm to 65 μm, as a typical representative example of an interposer that can be used for PIP. The ECA protrudes above the surface of the dielectric by about 5-10 μm, (Figure 8B).”</p> <p>“Figure 10 shows PIP structures for connecting 4 packages with three interposers. An optical photo of a cross section of the PIP structure built with 4 packages with three interposers is shown in Figure 11.”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p>
--	---

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.A] a bottom package substrate;</p>	<p>EIT PIP discloses, either expressly or inherently, a bottom package substrate.</p> <p><i>See, e.g.:</i></p>

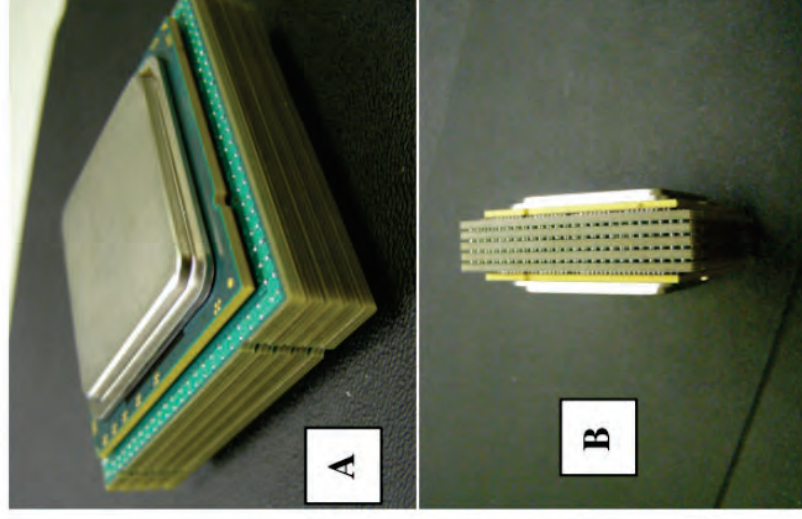


Figure 11: Photograph of package-Interposer-Package (PIP) construction with multiple substrates. (A) top view and (B) cross section view.

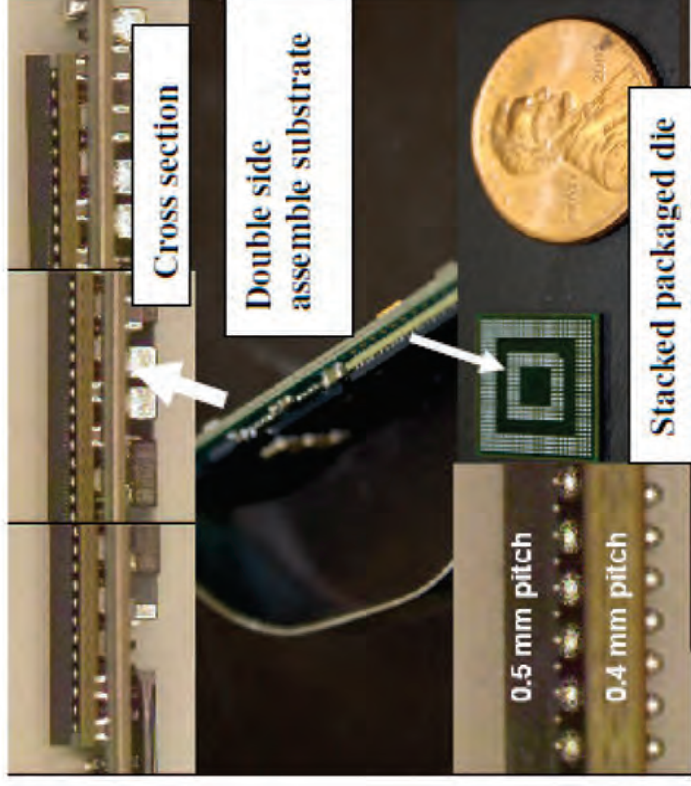


Figure 12: Double side assembled substrate. Top : Assembled substrate cross section. Middle: side view of assembled substrate. Bottom: stacked packaged die (memory attached to the processor) prior to assembly.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“Traditional Package on Package (POP) approaches use direct solder connections between the substrates and are limited to use of single (or minimum) die on the bottom substrate, to reduce warpage and improve stability.”</p> <p>“For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.”</p> <p>“Figure 12 shows highly populated double side assembled substrate having stacked packaged die attached to the substrate.”</p> <p>“PIP can accommodate modules with stacked die on organic, ceramic, or silicon board substrates, where in some cases defective substrates can be detached and replaced without affecting the rest of the package.”</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer.”</p> <p>https://imagesource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.B] a top package substrate stacked on top of the bottom package substrate;	EIT PIP discloses, either expressly or inherently, a top package substrate stacked on top of the bottom package substrate.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<i>See, e.g.:</i>
--	-------------------

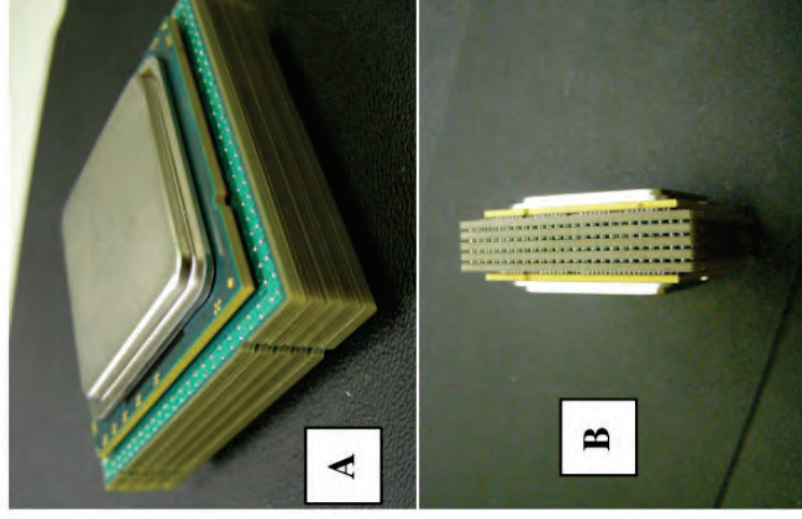


Figure 11: Photograph of package-Interposer-Package (PIP) construction with multiple substrates. (A) top view and (B) cross section view.

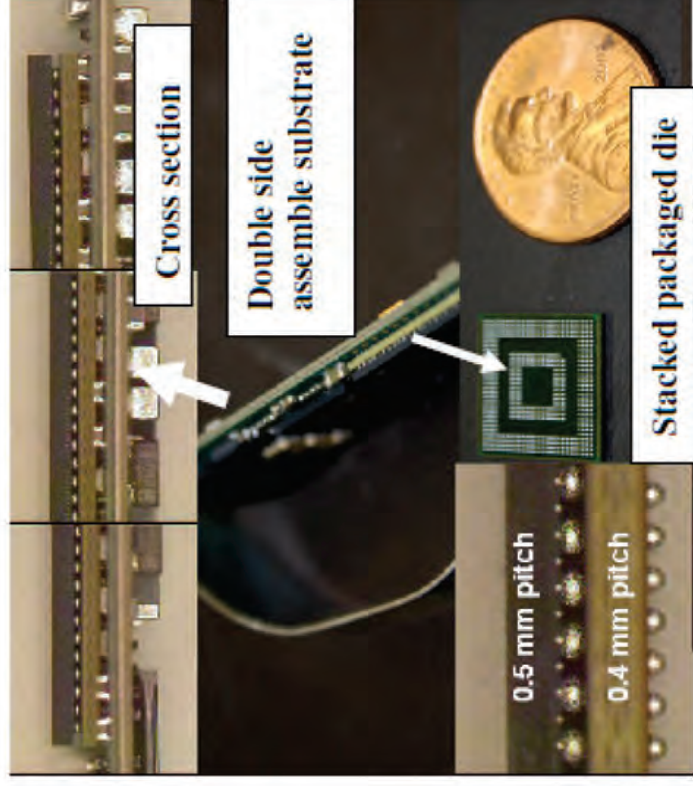


Figure 12: Double side assembled substrate. Top : Assembled substrate cross section. Middle: side view of assembled substrate. Bottom: stacked packaged die (memory attached to the processor) prior to assembly.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“Traditional Package on Package (POP) approaches use direct solder connections between the substrates and are limited to use of single (or minimum) die on the bottom substrate, to reduce warpage and improve stability.”</p> <p>“For PIP, the stability imparted by the interposer reduces warpage, allowing assemblers of the PIP to select the top and bottom components (substrates, die, stacked die, modules) from various suppliers.”</p> <p>“Figure 12 shows highly populated double side assembled substrate having stacked packaged die attached to the substrate.”</p> <p>“PIP can accommodate modules with stacked die on organic, ceramic, or silicon board substrates, where in some cases defective substrates can be detached and replaced without affecting the rest of the package.”</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer.”</p> <p>https://imagesource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

<p>[1.C] at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate, wherein</p>	<p>EIT PIP discloses, either expressly or inherently, at least one spacer connector interposed between the bottom package substrate and the top package substrate to define a space between the bottom package substrate and the top package substrate.</p> <p><i>See, e.g.:</i></p>
---	--

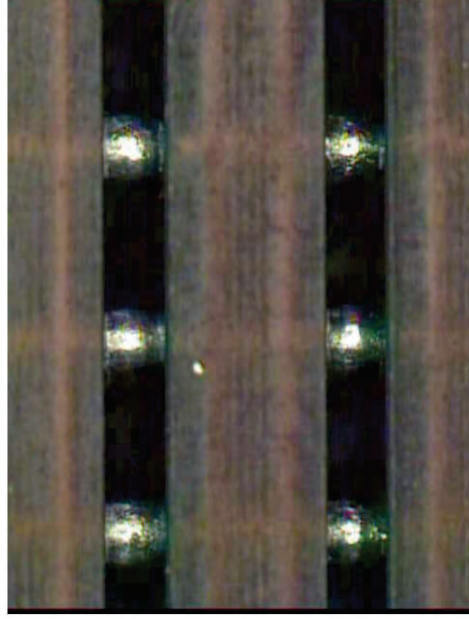


Figure 7. Photographs of cross section of PIP, low magnification (top), and higher magnification (bottom).

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“In the PIP structure, multiple packages will be attached with an interposer instead of direct soldering between packages, and maintain finer ball pitch for thicker stacked or wire bond die component assemblies. The interposer will not only reduce the package to package ball pitch but also improves package stability and reliability.”</p> <p>“For PIP, use of an interposer between the two packages provides for the use of low volume interconnect metallurgy between the interposer and the packages, enabling finer pitch connections from package to package.”</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.”</p> <p>“PIP can accommodate a larger range in attached component thickness because of the flexibility in selection of interposer thickness.”</p> <p>“Smaller pitch is attainable owing to the need for smaller solder volumes (most of the space between packages is occupied by the interposer), or a landless joining core technology, where the pitch is limited solely by the size of the via one can fill with ECA.”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

[1.D] the spacer connector comprises a core substrate;

EIT PIP discloses, either expressly or inherently, the spacer connector comprises a core substrate.

See, e.g.:

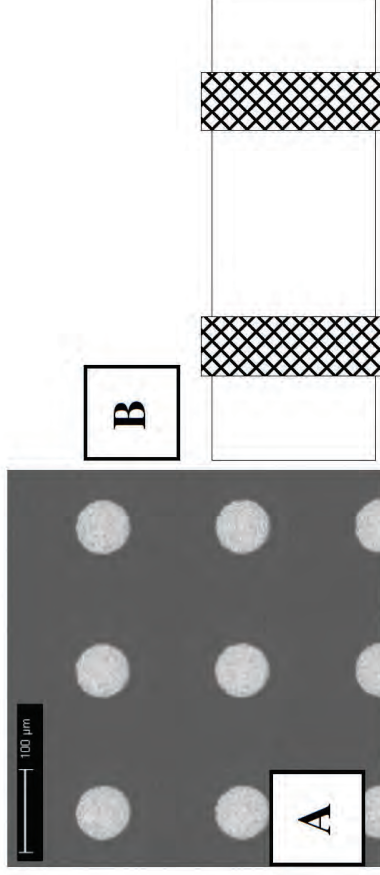


Figure 4. Various means can be employed for interposer-package joining. Illustrated here is (A) an optical photo, top view, of an interposer formed using an ECA-filled joining core, and (B) a schematic representation, in cross section of one possible interposer configuration using this joining core structure, where the crosshatched area is ECA. See also **Figure 8.**

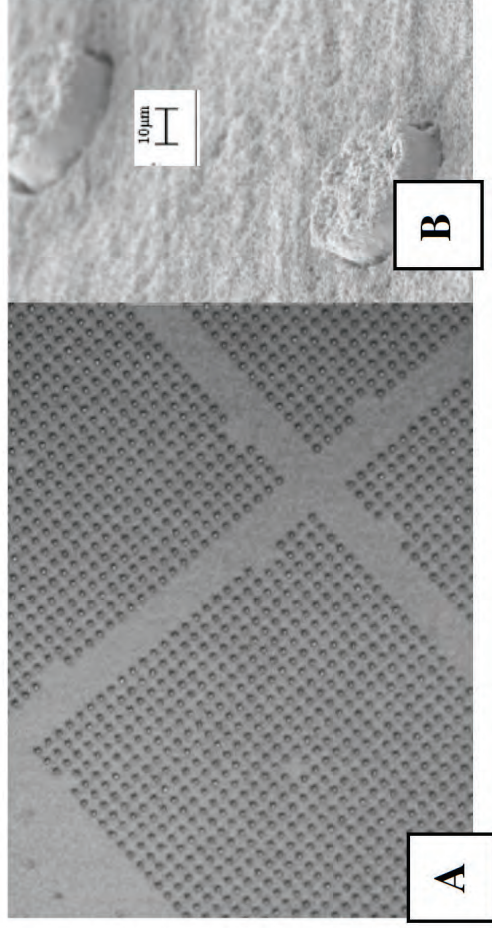


Figure 8. Optical and SEM micrographs of adhesive-filled joining cores; (A) array with ECA-filled vias having a diameter of 55 microns, and (B) corresponding SEM micrograph showing ECA “nubs” extending above the surface of the dielectric in the joining core.

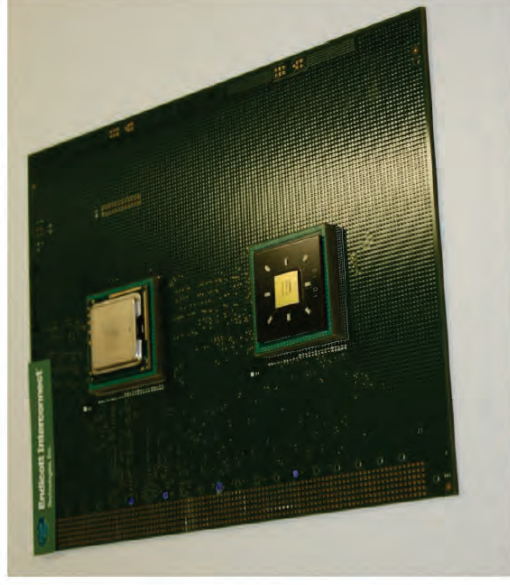
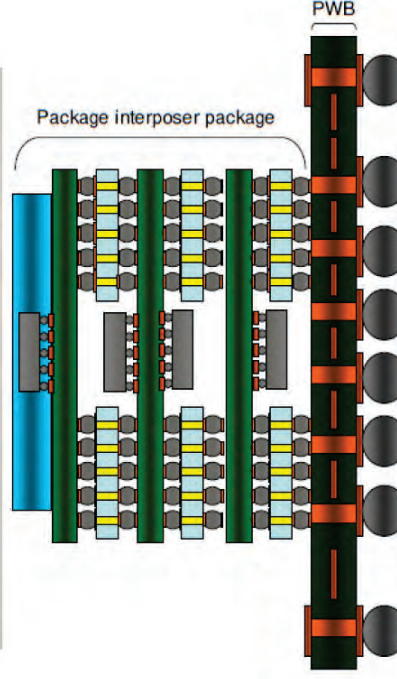


Figure 14: Photograph and schematic representation of PIP attached with low end board.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.”</p> <p>“High temperature/pressure lamination is used to cure the adhesive in the PIP and provide electrical interconnection among the packages. A variety of interposer structures such as OS/1P, OS/2P, 2S/1P, 2S/2P can be used. Figure 8 shows optical photographs and SEM micrographs of a joining core having ECA-filled holes with diameters ranging from 55 μm to 65 μm, as a typical representative example of an interposer that can be used for PIP.”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
[1.E] a plurality of metal pillars, each passing through the core substrate; and	<p>EIT PIP discloses, either expressly or inherently, a plurality of metal pillars, each passing through the core substrate.</p> <p><i>See, e.g.:</i></p>

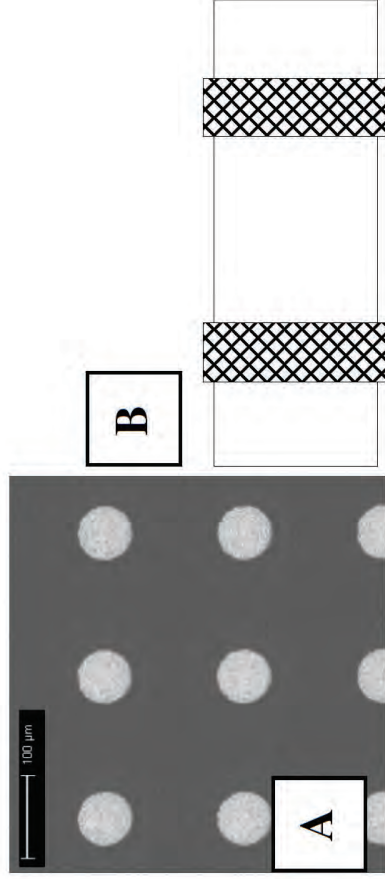


Figure 4. Various means can be employed for interposer-package joining. Illustrated here is (A) an optical photo, top view, of an interposer formed using an ECA-filled joining core, and (B) a schematic representation, in cross section of one possible interposer configuration using this joining core structure, where the crosshatched area is ECA. See also **Figure 8.**

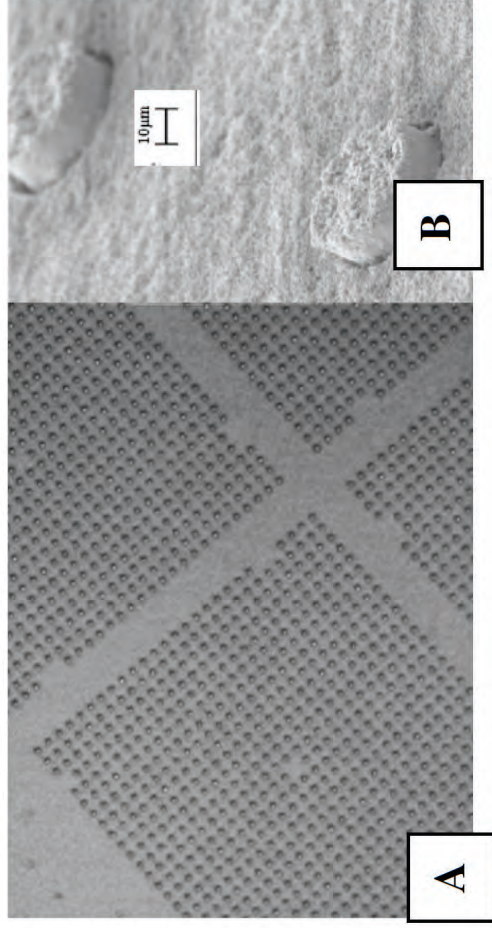


Figure 8. Optical and SEM micrographs of adhesive-filled joining cores; (A) array with ECA-filled vias having a diameter of 55 microns, and (B) corresponding SEM micrograph showing ECA “nubs” extending above the surface of the dielectric in the joining core.

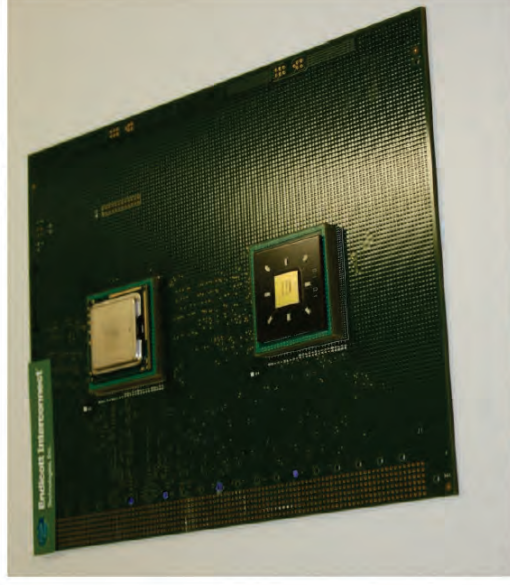
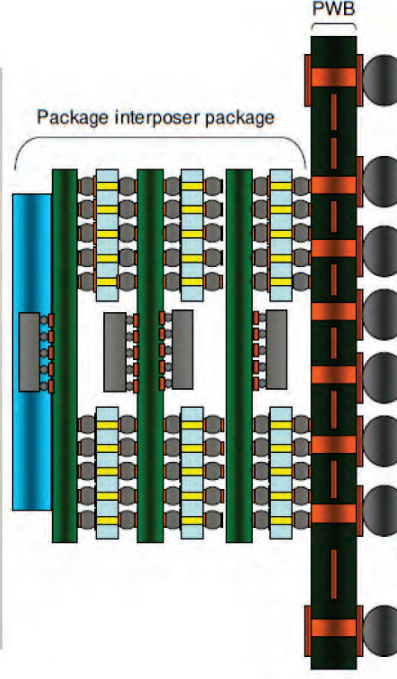


Figure 14: Photograph and schematic representation of PIP attached with low end board.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“Reworkable ECA connections can be achieved if the ECA consists of conducting metal particles and a low MP thermoplastic polymer.”</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.”</p> <p>“High temperature/pressure lamination is used to cure the adhesive in the PIP and provide electrical interconnection among the packages. A variety of interposer structures such as OS/1P, OS/2P, 2S/1P, 2S/2P can be used. Figure 8 shows optical photographs and SEM micrographs of a joining core having ECA-filled holes with diameters ranging from 55 μm to 65 μm, as a typical representative example of an interposer that can be used for PIP.”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.F] a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars;</p>	<p>EIT PIP discloses, either expressly or inherently, a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars.</p> <p><i>See, e.g.:</i></p>

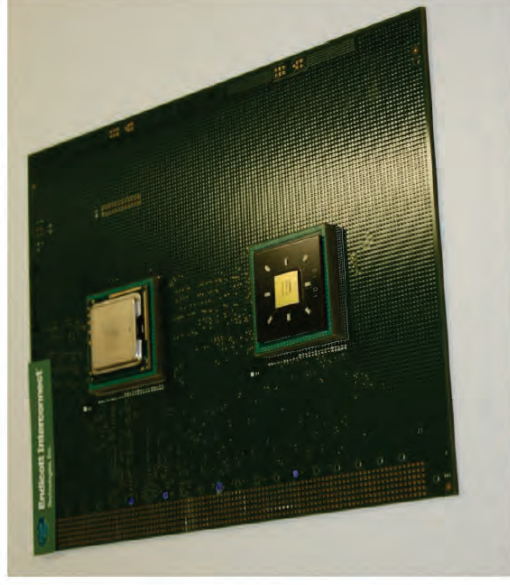
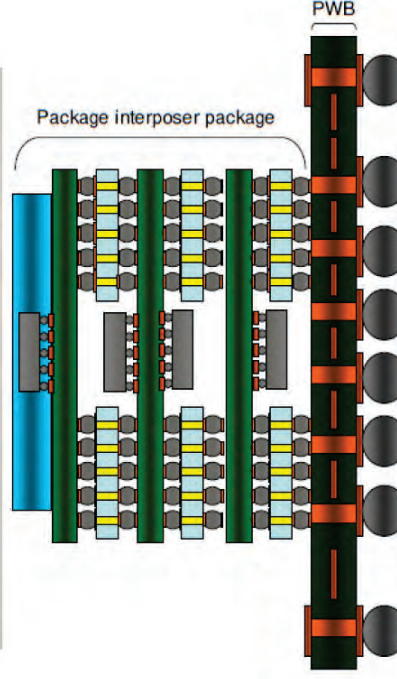


Figure 14: Photograph and schematic representation of PIP attached with low end board.

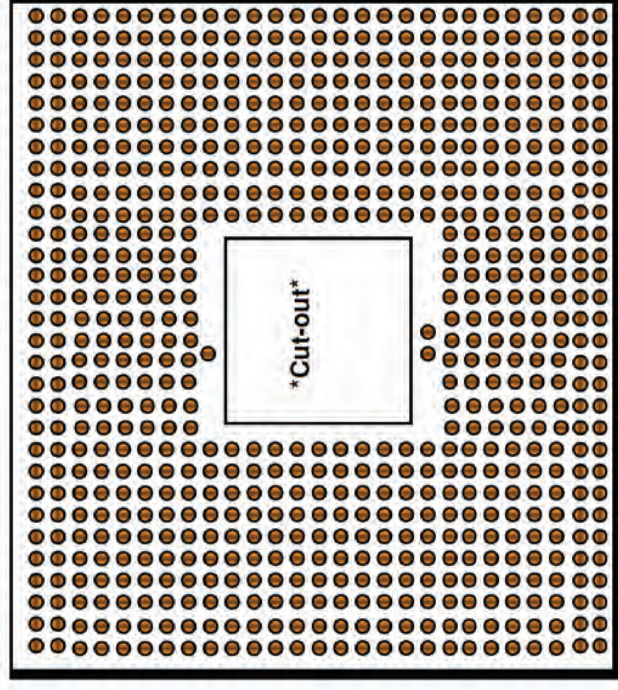


Figure 5. Top view of interposer

“A top view of the contacting pads for this interposer is shown schematically in Figure 5.”

“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.”

<https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration>

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.G] wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate,</p>	<p>EIT PIP discloses, either expressly or inherently, wherein a bottom end of each metal pillar among the plurality of metal pillars protrudes downwardly from a bottom surface of the core substrate.</p> <p><i>See, e.g.:</i></p>

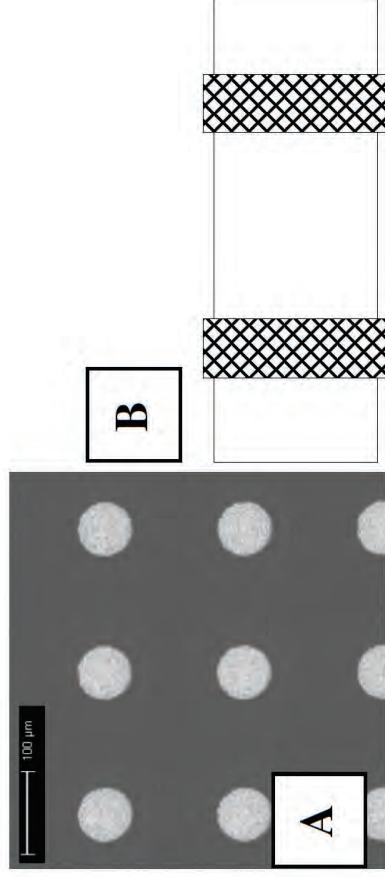


Figure 4. Various means can be employed for interposer-package joining. Illustrated here is (A) an optical photo, top view, of an interposer formed using an ECA-filled joining core, and (B) a schematic representation, in cross section of one possible interposer configuration using this joining core structure, where the crosshatched area is ECA. See also **Figure 8.**

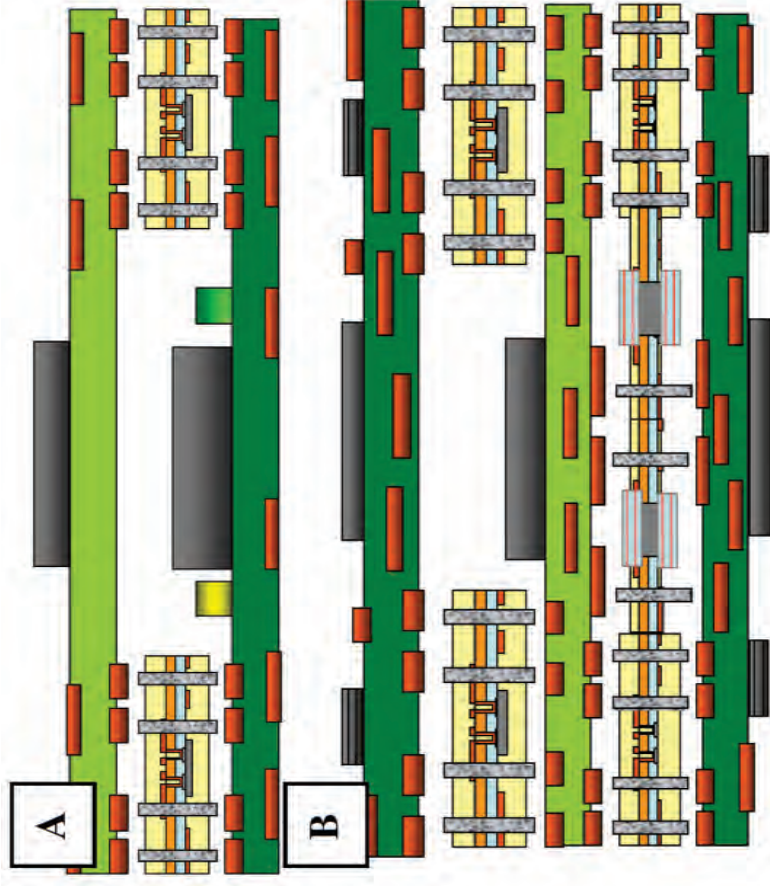


Figure 9. (A) Package-Interposer-Package construction using a single interposer. Here the interposer is a functional/active part of a package, for example an interposer with embedded actives. (B) A stack may contain multiple interposers (n) and packages ($n + 1$).

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“The ECA protrudes above the surface of the dielectric by about 5-10 μm, (Figure 8B).”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.H] the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector,</p>	<p>EIT PIP discloses, either expressly or inherently, the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

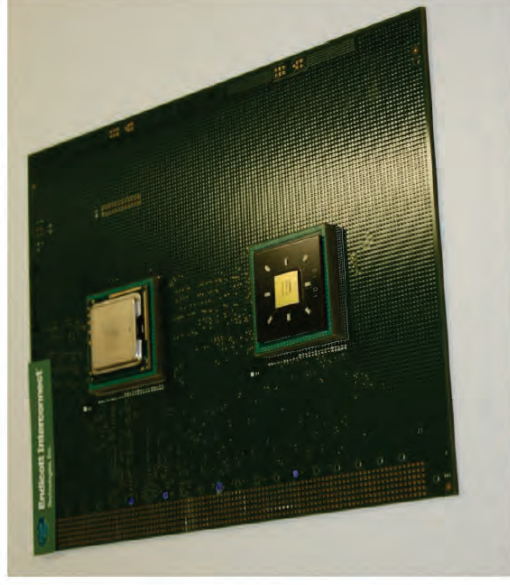
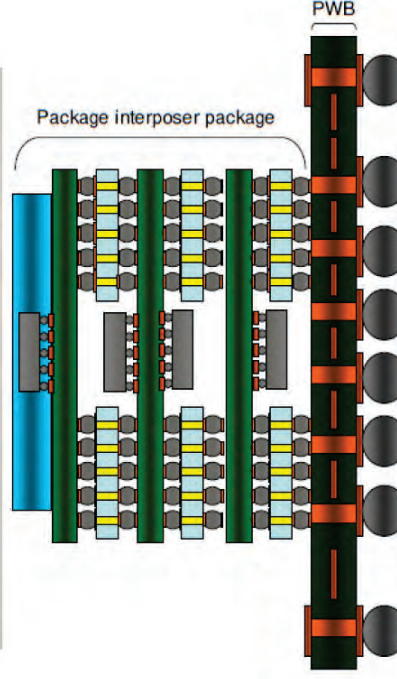
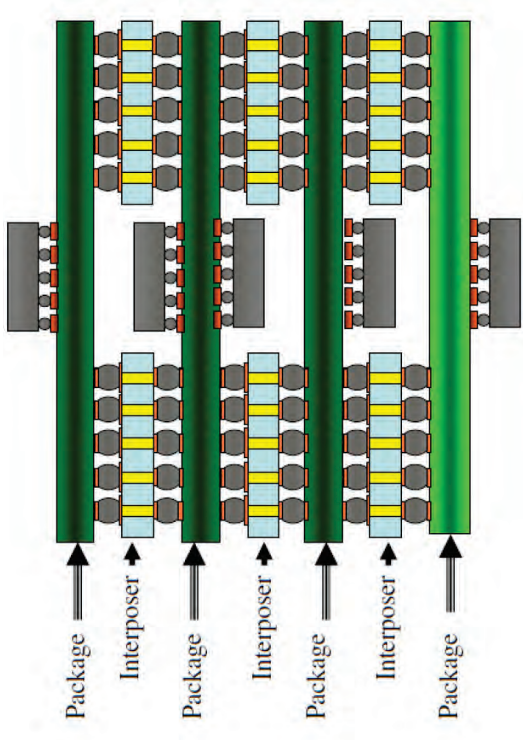


Figure 14: Photograph and schematic representation of PIP attached with low end board.

	 <p>Figure 10: Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers.</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.”</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer. It can be a single step or multiple step process. Figure 6 shows the processing sequence for this PIP. The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.”</p>
--	---

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“By alternating packages and interposer in the lay-up prior to reflow, the solder paste electrically connects copper pads on the package that reside on either side of the interposer.”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.I] the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and</p>	<p>EIT PIP discloses, either expressly or inherently, the bottom package substrate has, on a top surface thereof, a plurality of top metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.</p> <p><i>See, e.g.:</i></p>

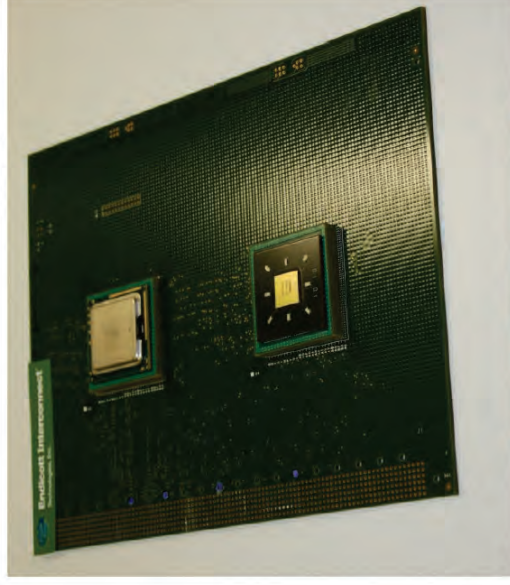
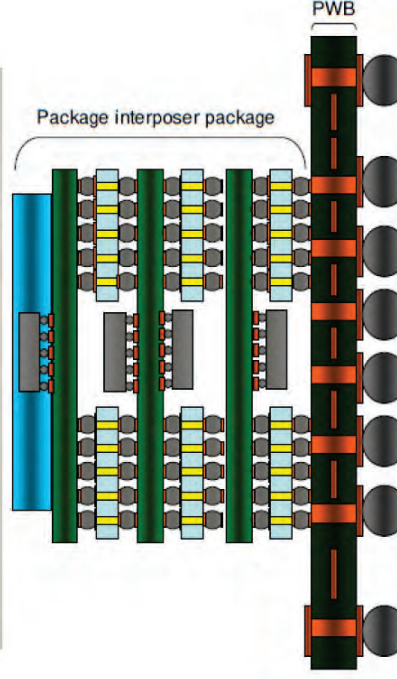
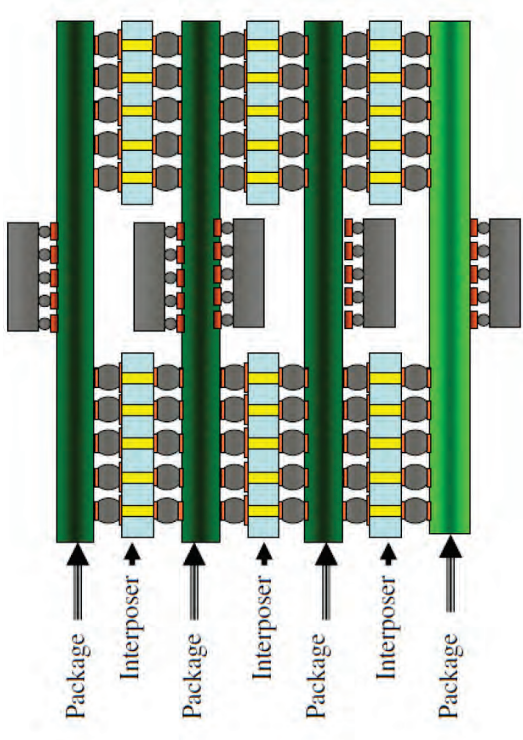


Figure 14: Photograph and schematic representation of PIP attached with low end board.

	 <p>Figure 10: Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers.</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.”</p> <p>“By alternating chip carrier and interposer in the lay- up prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer. It can be a single step or multiple step process. Figure 6 shows the processing sequence for this PIP. The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.”</p>
--	---

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“By alternating packages and interposer in the lay-up prior to reflow, the solder paste electrically connects copper pads on the package that reside on either side of the interposer.”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.J] the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate; and</p>	<p>EIT PIP discloses, either expressly or inherently, the top package substrate is electrically coupled to the bottom package substrate through the plurality of bottom metal pillars of the top package substrate, the plurality of metal pillars of the spacer connector, and the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

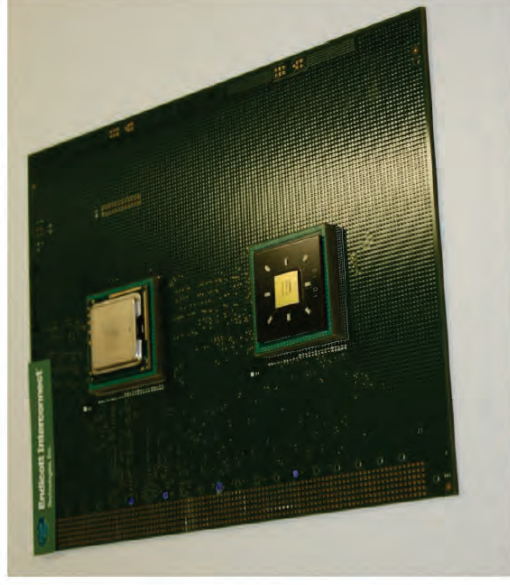
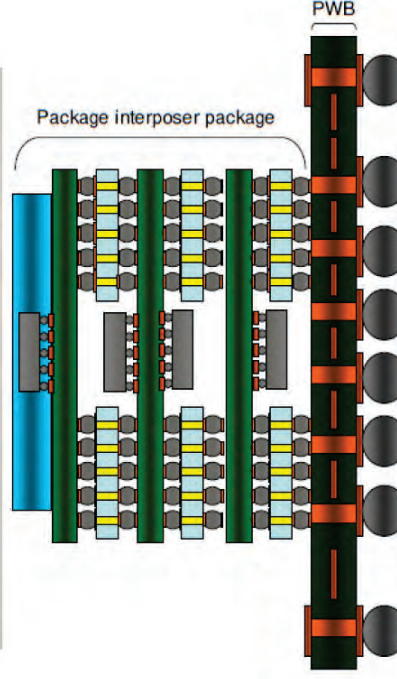
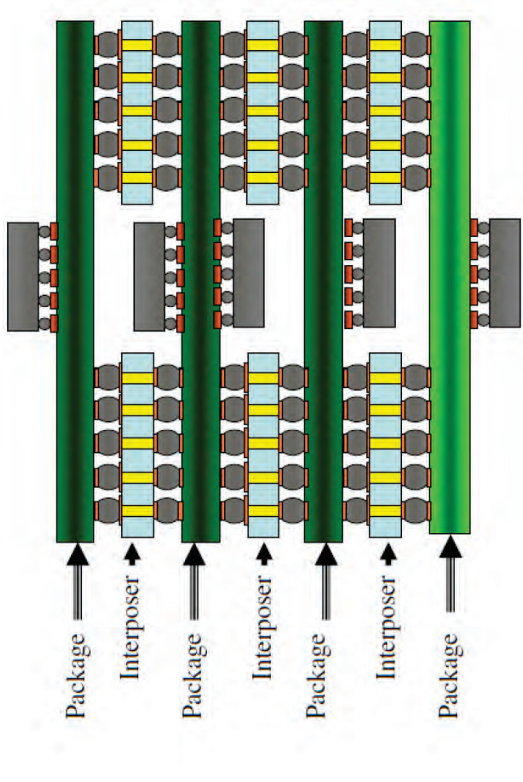


Figure 14: Photograph and schematic representation of PIP attached with low end board.

	 <p>Figure 10: Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers.</p> <p>“Interconnection among substrates (packages) in the stack was achieved using interposers. Plated through holes in the interposers, formed by laser or mechanical drilling and having diameters ranging from 50 μm to 250 μm, were filled with an electrically conductive adhesive and cured.”</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.”</p> <p>“By alternating chip carrier and interposer in the layup prior to reflow, the solder paste electrically connects copper pads on the chip carriers that reside on either side of the interposer.”</p>
--	---

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer. The bottom side of the top package is then connected with the top side of the interposer to complete the PIP structure.”</p> <p>“High temperature/pressure lamination is used to cure the adhesive in the PIP and provide electrical interconnection among the packages.”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.K] a bottom chip arranged in the space between the bottom package substrate and the top package substrate, wherein</p>	<p>EIT PIP discloses, either expressly or inherently, a bottom chip arranged in the space between the bottom package substrate and the top package substrate.</p> <p><i>See, e.g.:</i></p>

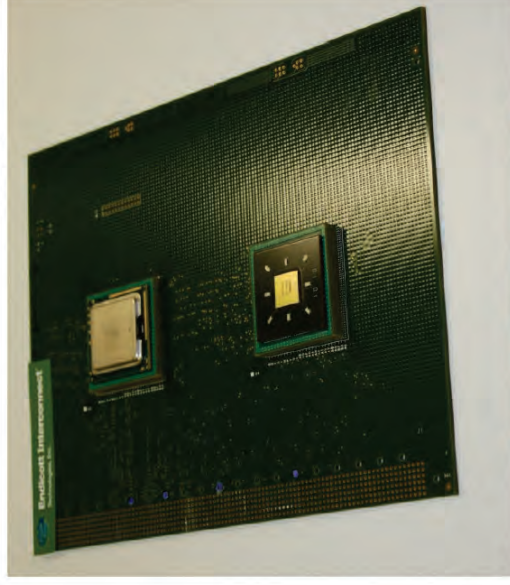
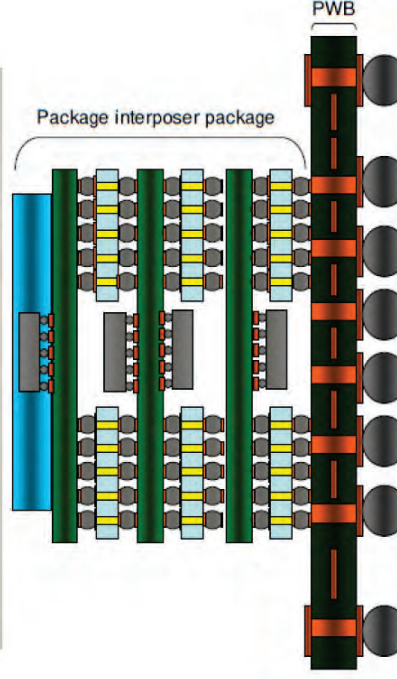
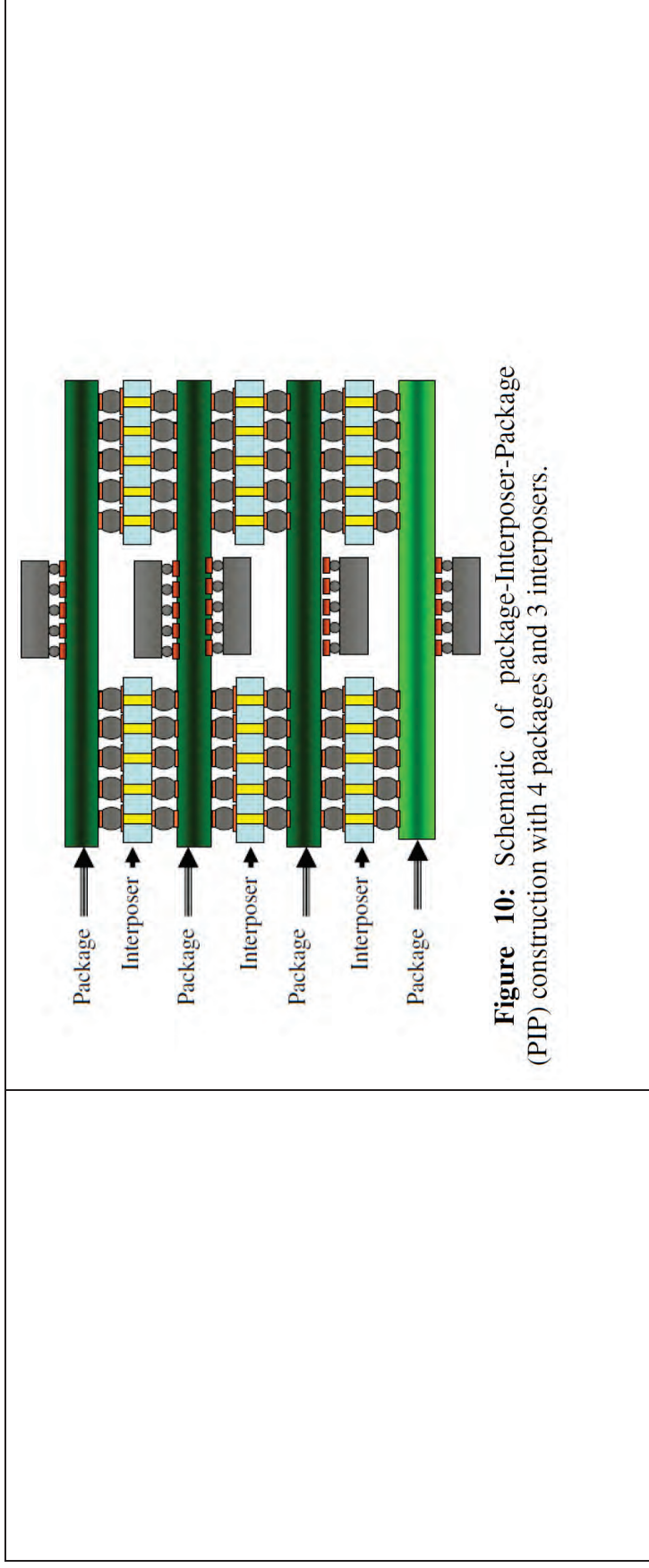


Figure 14: Photograph and schematic representation of PIP attached with low end board.



	<div> <p>The diagram shows a cross-sectional view of a 3D-PIP construction. It consists of a top package (green) and a bottom package (green) separated by a single interposer (light blue). The interposer has a central opening. The top package has a die (black) with wire bonds (orange) connecting it to the interposer. The bottom package has a die (black) with wire bonds (orange) connecting it to the interposer. The interposer has a central opening. The top package has a die (black) with wire bonds (orange) connecting it to the interposer. The bottom package has a die (black) with wire bonds (orange) connecting it to the interposer. The interposer has a central opening.</p> </div> <p>Figure 2: Package-Interposer-Package (PIP) construction with a single interposer. (A) Top and bottom packages have wire bonded stacked die, (B) Top and bottom packages have TSV processed stacked die, and the bottom package has wired bonded stacked die, (D) 3D-PIP construction with a single interposer.</p> <p>“The stacked packages shown in the Figure 2D contains flip chip solder connections to either an organic substrate, a ceramic substrate, or a silicon board.”</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer.”</p>
--	--

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.L] the bottom chip is mounted to the top surface of the bottom package substrate, and</p>	<p>EIT PIP discloses, either expressly or inherently, the bottom chip is mounted to the top surface of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

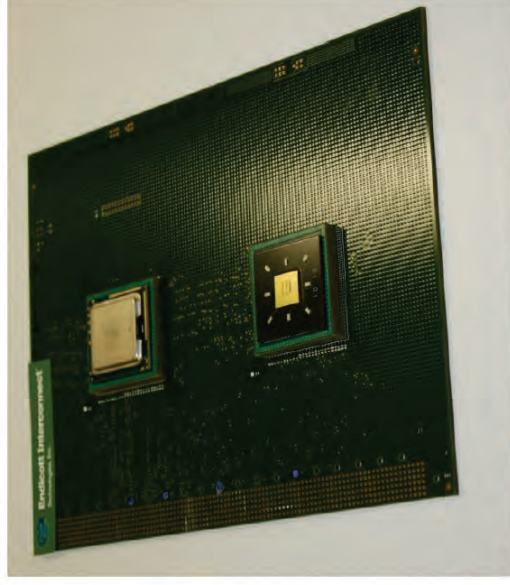
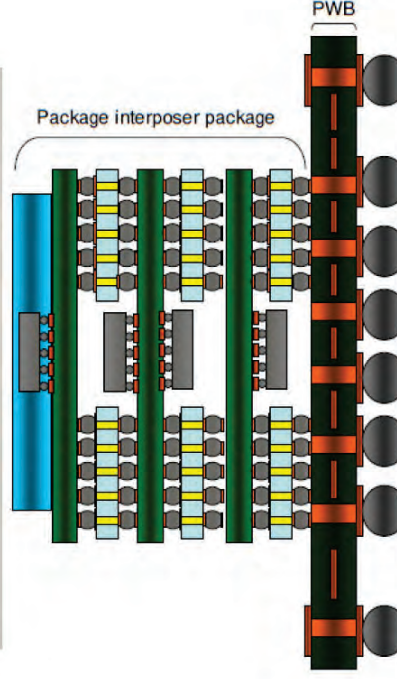
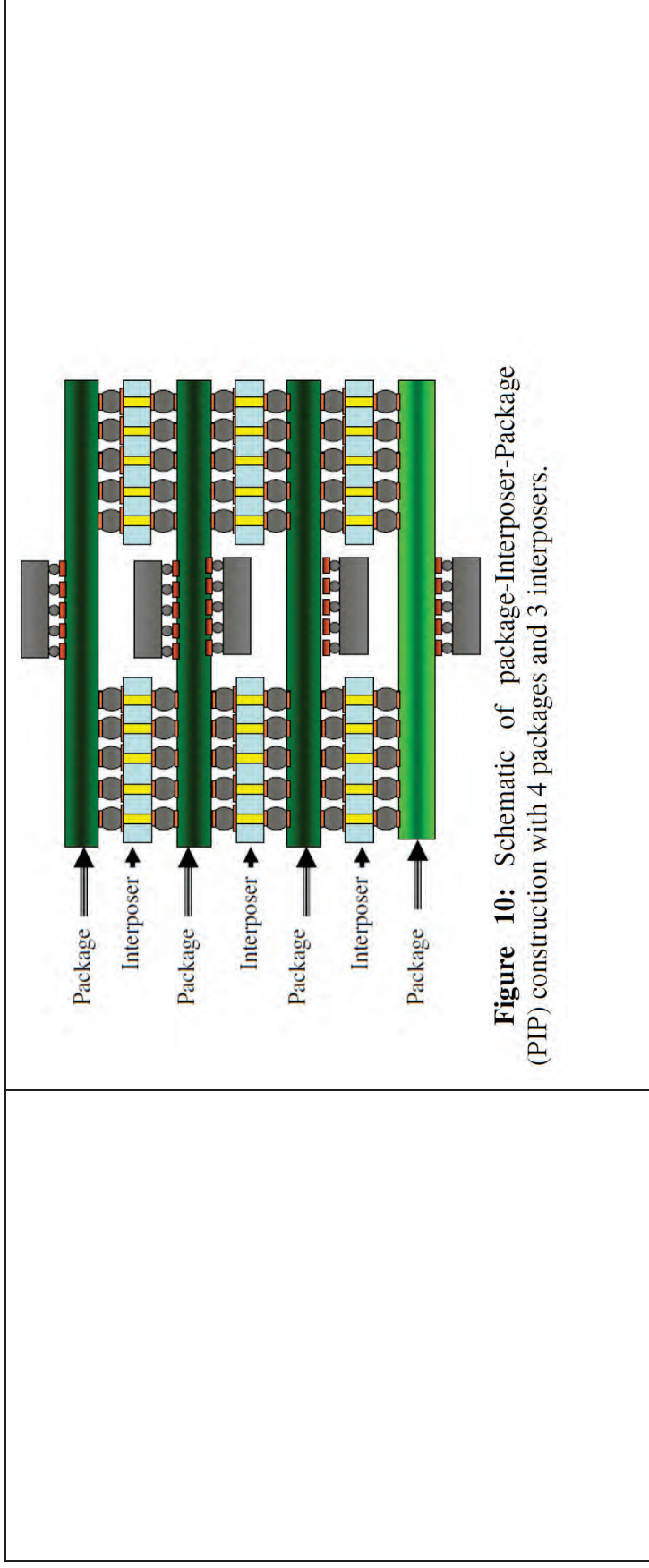
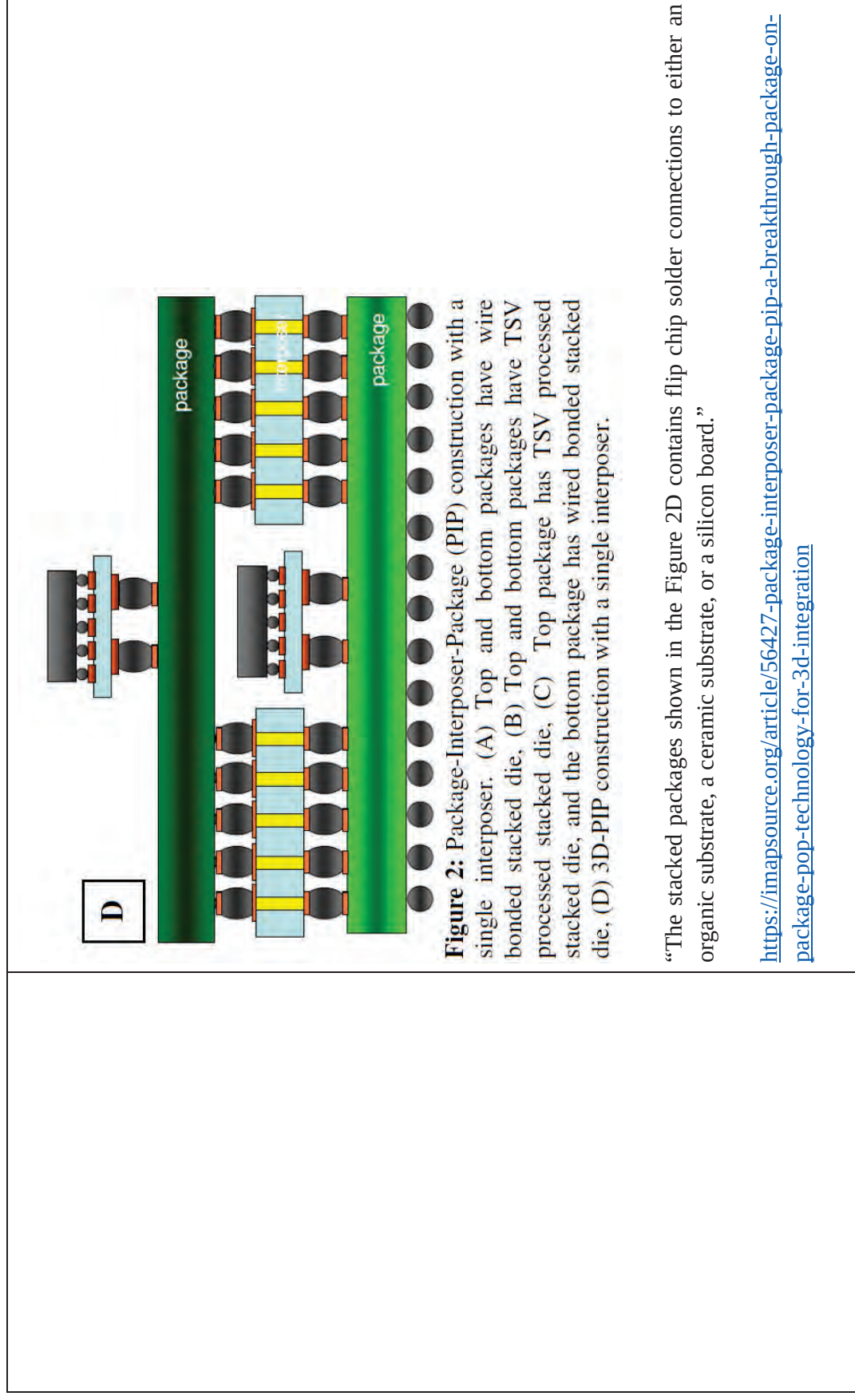


Figure 14: Photograph and schematic representation of PIP attached with low end board.





Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
<p>[1.M] the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p>	<p>EIT PIP discloses, either expressly or inherently, the at least one spacer connector comprises two spacer connectors arranged on opposite sides of the bottom chip.</p> <p><i>See, e.g.:</i></p>

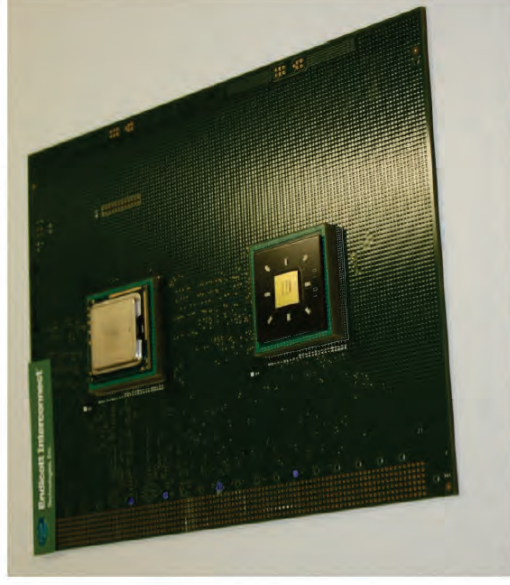
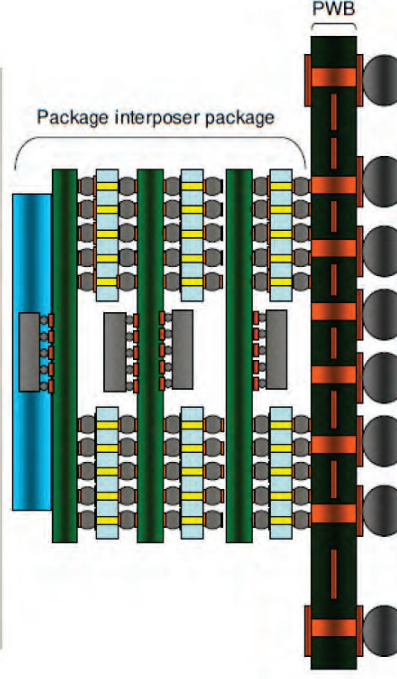
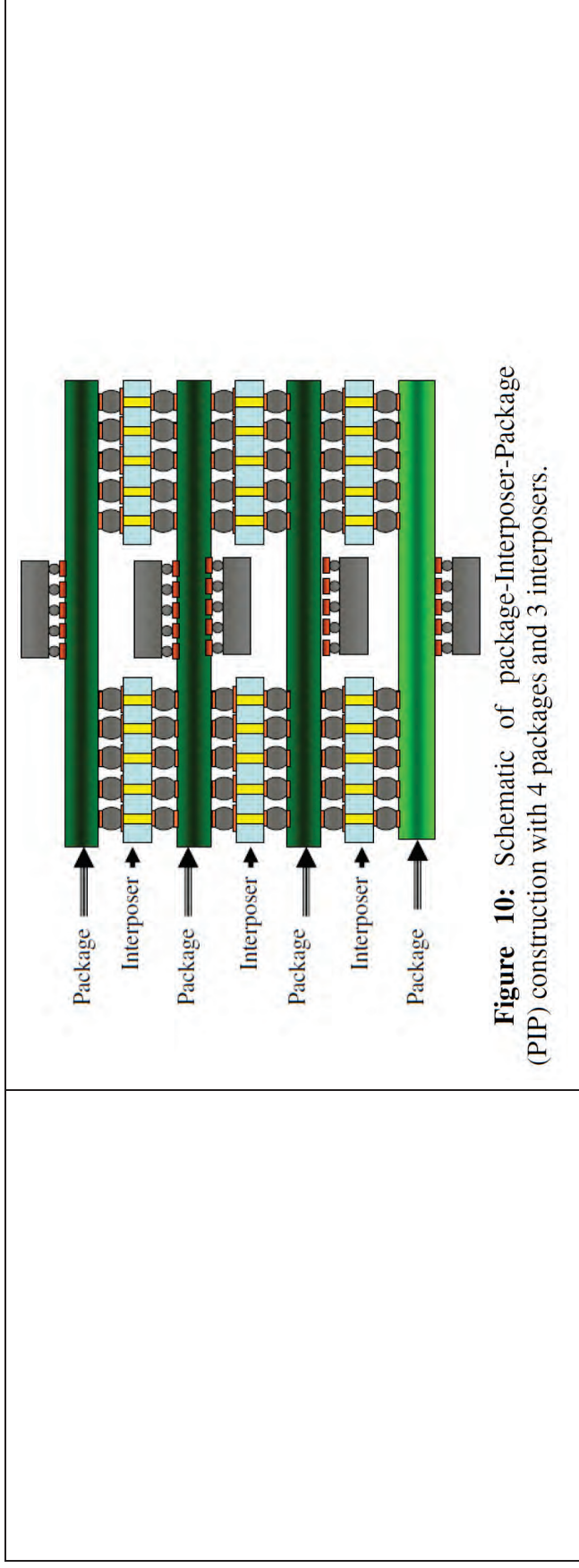


Figure 14: Photograph and schematic representation of PIP attached with low end board.



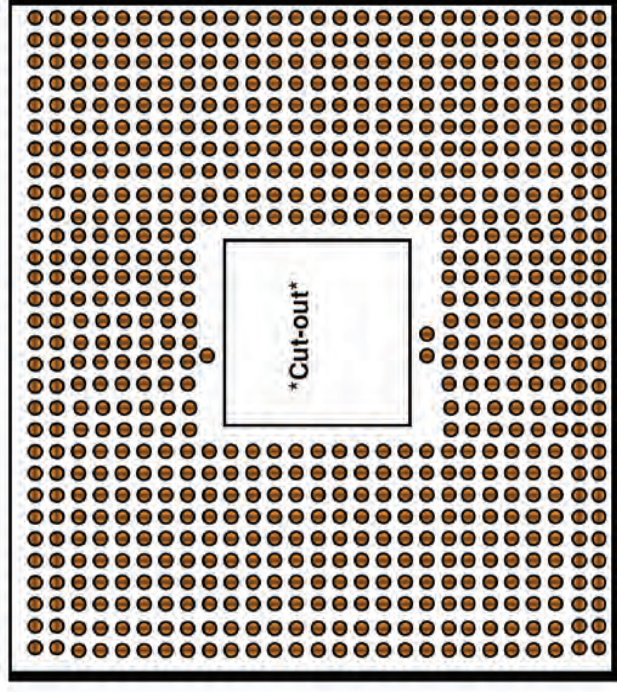


Figure 5. Top view of interposer

“A top view of the contacting pads for this interposer is shown schematically in Figure 5.”

<https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration>

To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

Claim 2

Claim Limitation	Disclosure
[2] The structure of claim 1, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate.	EIT PIP discloses, either expressly or inherently, wherein a top surface of the bottom chip is spaced downwardly from the bottom surface of the top package substrate. <i>See, e.g.:</i>

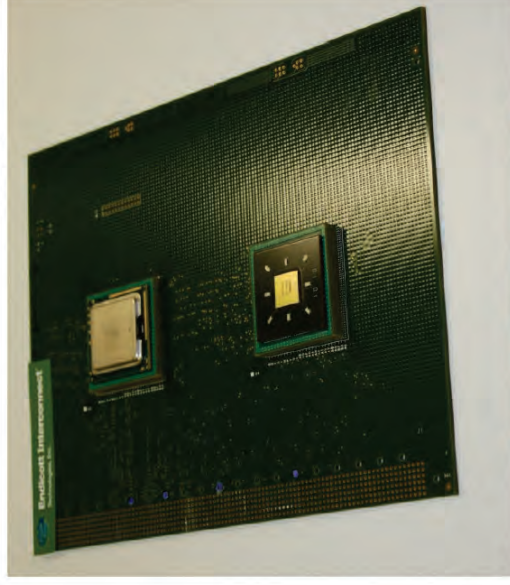
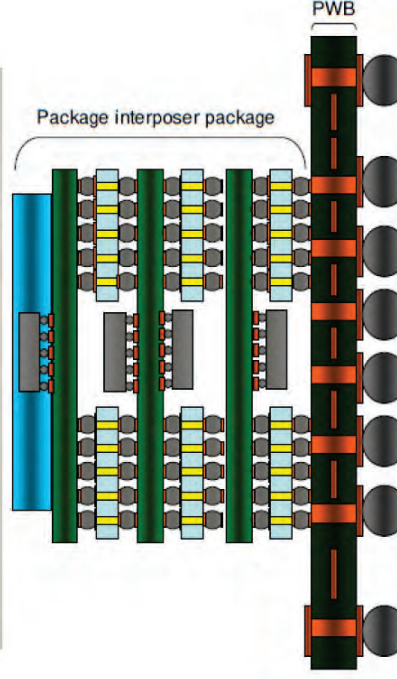
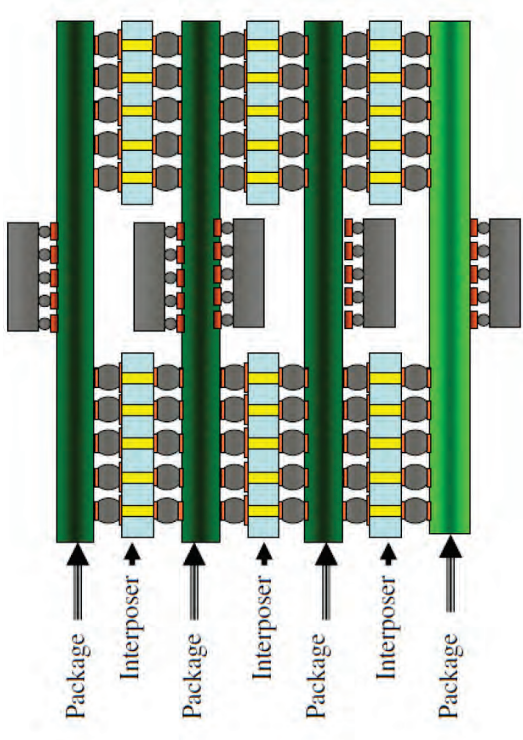


Figure 14: Photograph and schematic representation of PIP attached with low end board.

	 <p>Figure 10: Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers.</p> <p>“The top side of the bottom package is connected with the bottom side of the interposer in such a way that the die on the bottom package resides within the opening of the interposer.”</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

Claim 3

Claim Limitation	Disclosure
[3] The structure of claim 2, further comprising: a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors.	EIT PIP discloses, either expressly or inherently, a top chip mounted to the top surface of the top package substrate, wherein in a direction in which the top package substrate is stacked on top of the bottom package substrate, the top chip overlaps the bottom chip and each of the two spacer connectors. <i>See, e.g.:</i>

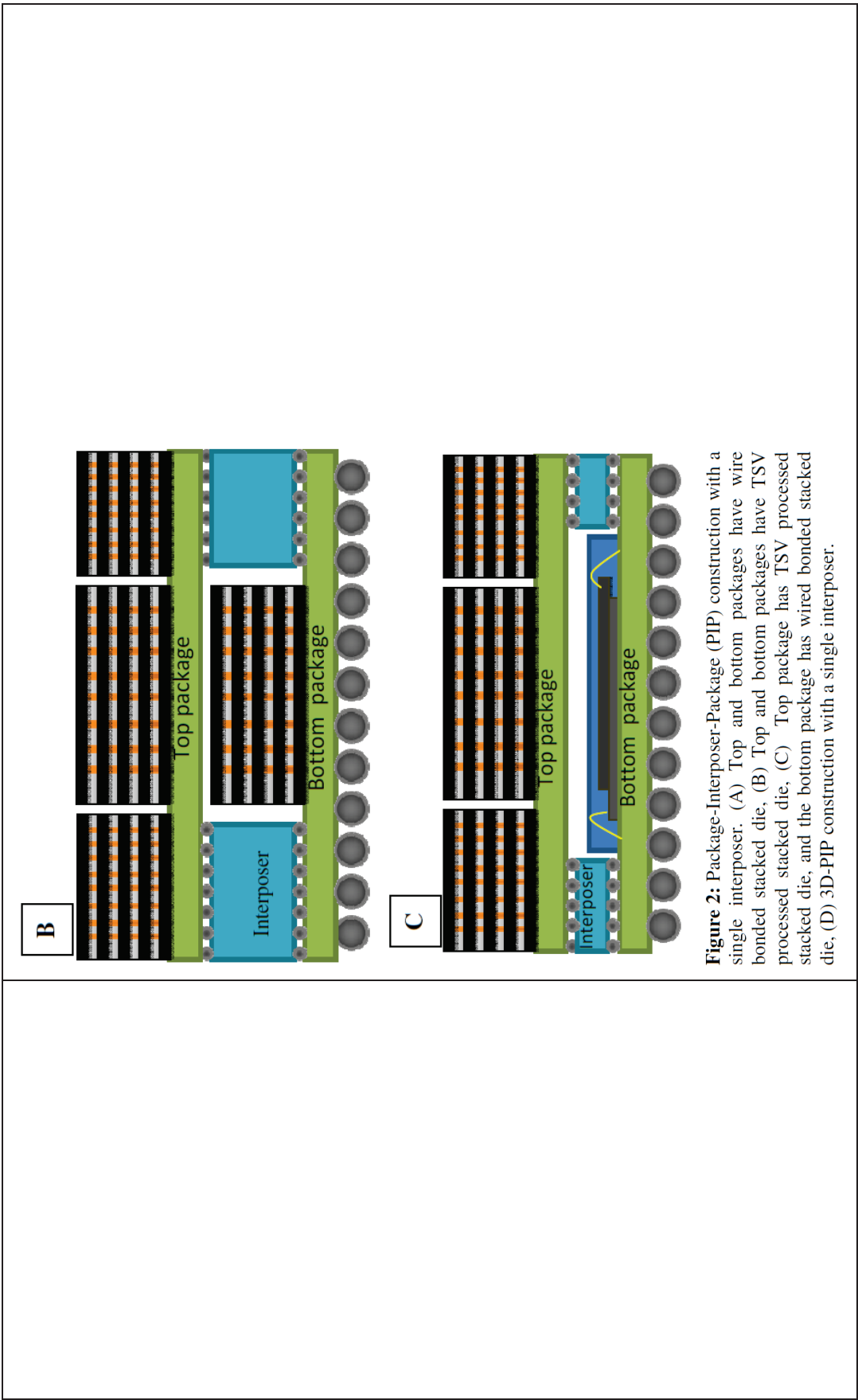


Figure 2: Package-Interposer-Package (PIP) construction with a single interposer. (A) Top and bottom packages have wire bonded stacked die, (B) Top and bottom packages have TSV processed stacked die, (C) Top package has TSV processed stacked die, and the bottom package has wired bonded stacked die, (D) 3D-PIP construction with a single interposer.

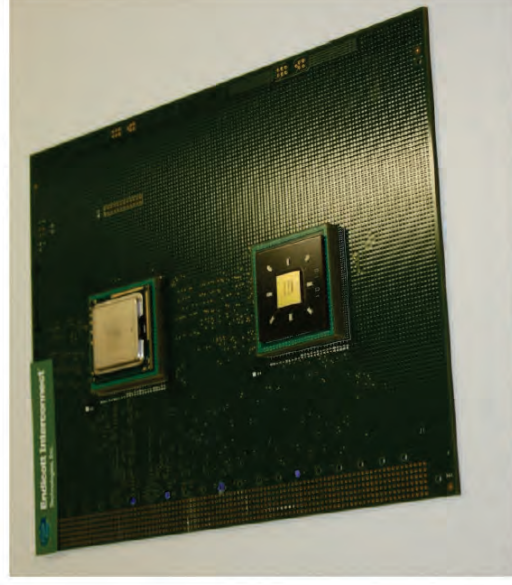
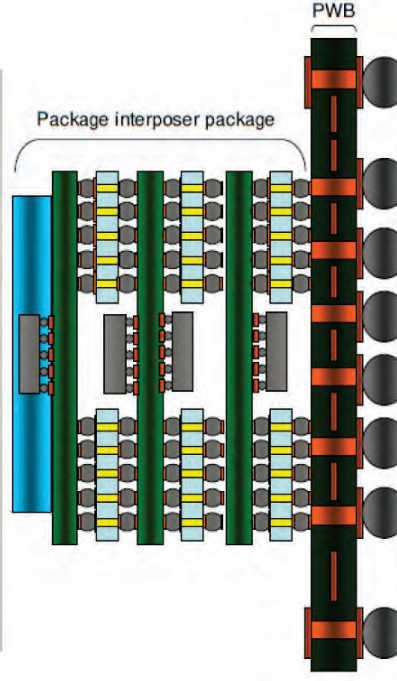


Figure 14: Photograph and schematic representation of PIP attached with low end board.

<https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration>

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	<p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	---

Claim 4

Claim Limitation	Disclosure
<p>[4] The structure of claim 1, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p>	<p>EIT PIP discloses, either expressly or inherently, wherein each bottom metal pillar among the plurality of bottom metal pillars of the top package substrate is aligned with a corresponding metal pillar among the plurality of metal pillars of the spacer connector, and with a corresponding top metal pillar among the plurality of top metal pillars of the bottom package substrate.</p> <p><i>See, e.g.:</i></p>

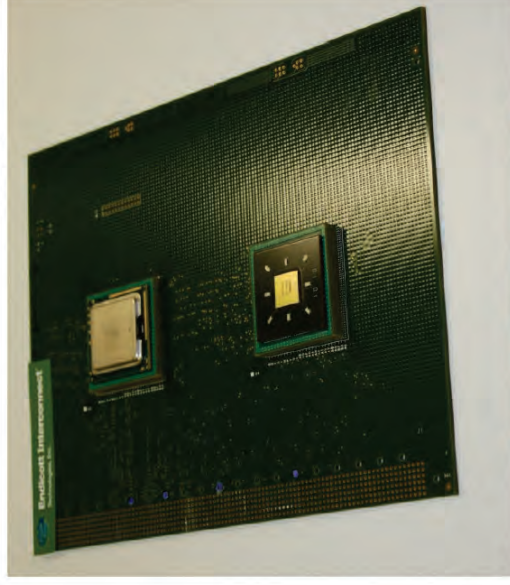
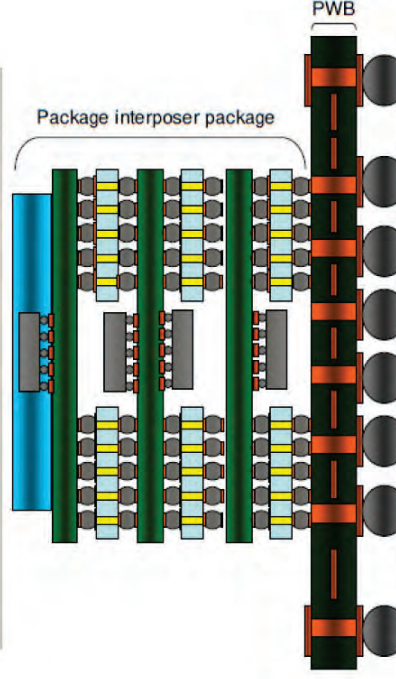
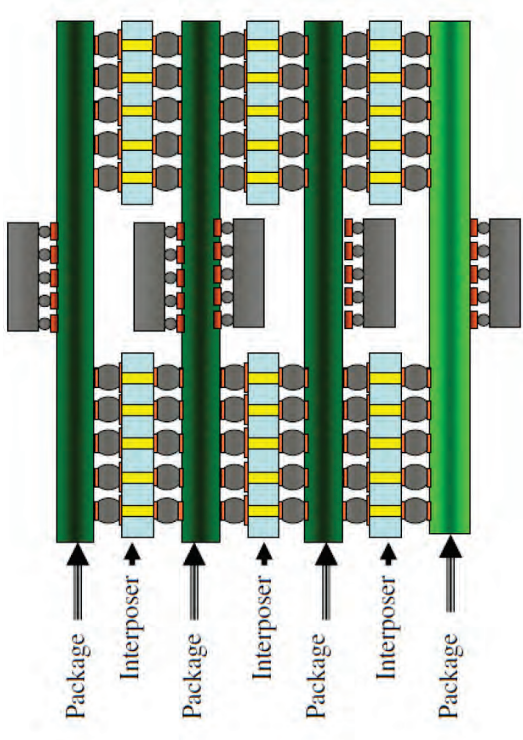


Figure 14: Photograph and schematic representation of PIP attached with low end board.

	 <p>The diagram illustrates a PIP construction with four packages and three interposers. It is shown in a cross-sectional view. From top to bottom, the layers are: a top package (green), an interposer (light blue), a second package (green), another interposer (light blue), a third package (green), a fourth interposer (light blue), and a bottom package (green). Each package is connected to the interposers above and below it via solder bumps (yellow). The interposers are connected to each other via through-silicon vias (TSVs, grey) and solder bumps (yellow). Arrows point to each layer with labels: 'Package' for the green layers and 'Interposer' for the light blue layers. The entire assembly is mounted on a substrate (grey) with solder bumps (yellow) at the bottom.</p> <p>Figure 10: Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers.</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.</p>
--	--

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

Claim 6

Claim Limitation	Disclosure
<p>[6] The structure of claim 4, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>EIT PIP discloses, either expressly or inherently, wherein the bottom ends of the plurality of metal pillars protruding downwardly from the bottom surface of the core substrate of the spacer connector are connected, in an end-to-end manner, to corresponding top ends of the plurality of top metal pillars of the bottom package substrate, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

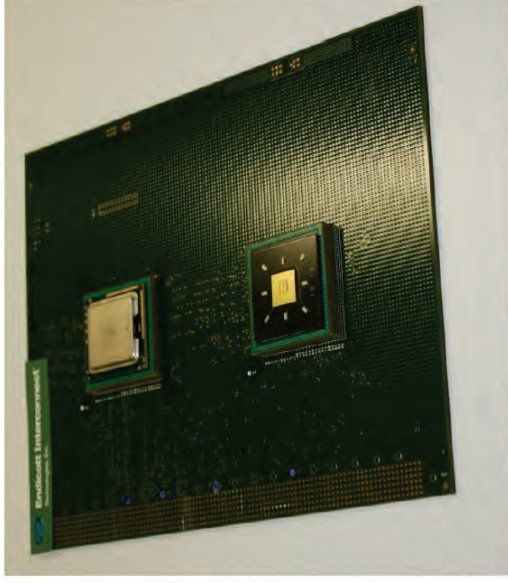
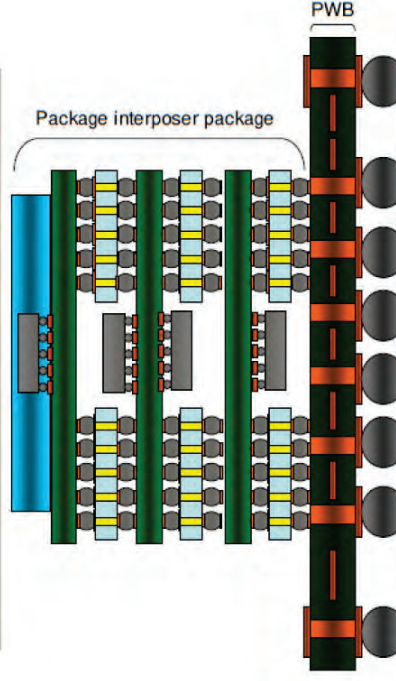


Figure 14: Photograph and schematic representation of PIP attached with low end board.

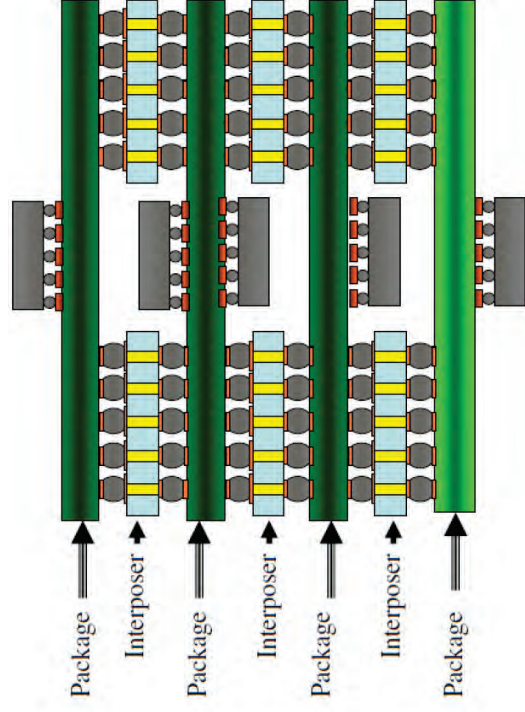


Figure 10: Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers.

<https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration>

To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

Claim 9

Claim Limitation	Disclosure
<p>[9] The structure of claim 4, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p>	<p>EIT PIP discloses, either expressly or inherently, wherein the spacer connector further comprises a plurality of bottom metal pads, each on the bottom end of a corresponding metal pillar among the plurality of metal pillars, the bottom ends of the plurality of metal pillars are connected to corresponding top ends of the plurality of top metal pillars of the bottom package substrate via the corresponding bottom metal pads of the spacer connector, and bottom ends of the plurality of bottom metal pillars of the top package substrate are connected to the corresponding top ends of the plurality of metal pillars of the spacer connector via the corresponding top metal pads of the spacer connector.</p> <p><i>See, e.g.:</i></p>

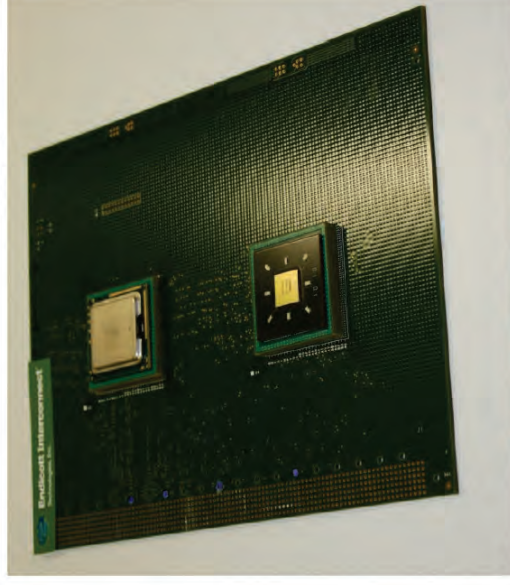
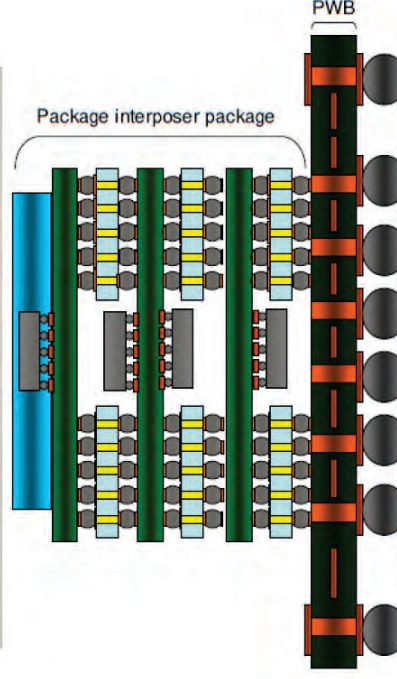
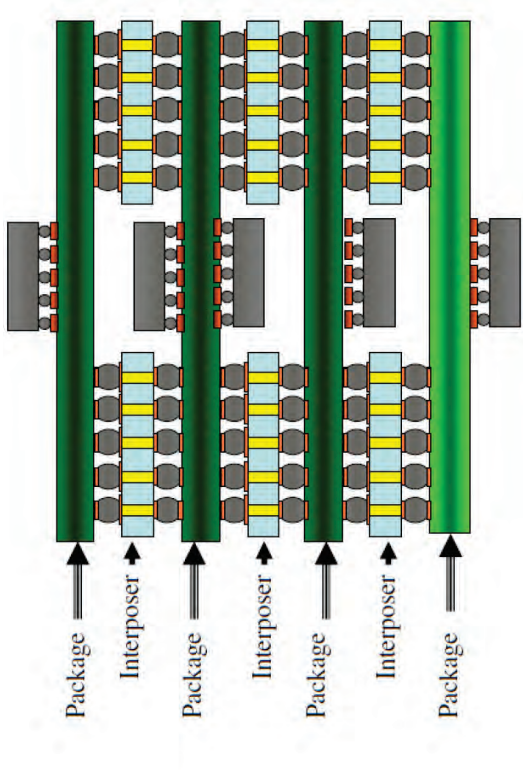


Figure 14: Photograph and schematic representation of PIP attached with low end board.

	 <p>The diagram illustrates a PIP construction with four packages and three interposers. It is shown in a perspective view. Four packages, represented by grey rectangular blocks with multiple pins on their bottom surfaces, are arranged in a row. Between each pair of adjacent packages is an interposer, represented by a light blue rectangular block with pins on its top and bottom surfaces. The interposers are positioned such that their top pins connect to the bottom pins of the package above them, and their bottom pins connect to the bottom pins of the package below them. The entire assembly is supported by a green substrate. Labels with arrows point to the packages and interposers, identifying them as 'Package' and 'Interposer' respectively. The labels are placed below the corresponding components.</p> <p>Figure 10: Schematic of package-Interposer-Package (PIP) construction with 4 packages and 3 interposers.</p> <p>“Connection between interposer and package made using solder between a pad on the interposer and a pad on the package is reworkable, i.e., if initial electrical testing of the assembled structure, Figure 1, indicates that either package and/or interposer are defective, the packages/interposer can be removed without damage to the assembly.”</p> <p>https://imapsource.org/article/56427-package-interposer-package-pip-a-breakthrough-package-on-package-pop-technology-for-3d-integration</p> <p>To the extent Plaintiff contends that EIT PIP fails to disclose this limitation, it would have been obvious to one of ordinary skill in the art based on this reference alone or in combination with (i) the</p>
--	---

Appendix A-54 - Invalidity of U.S. Patent No. 9,859,202 in view of EIT PIP

	general knowledge of one of ordinary skill in the art and/or (ii) the teachings of any of the charted references with respect to this limitation.
--	---