

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.
Petitioners,

v.

TOPWIRE, LLC,
Patent Owner.

Case No. IPR2026-00324
U.S. Patent No. 9,859,202

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	BACKGROUND	3
A.	Background of the Invention.....	3
B.	U.S. Patent Application Publication No. 2013/0182402 ("Chen")	5
C.	U.S. Patent Application Publication No. 2011/0147908 ("Sun").....	7
D.	U.S. Patent No. 5,334,804 ("Love")	8
E.	U.S. Patent Application Publication No. 2013/0249083 ("Hu").....	8
F.	Benson, Polymer Adhesives and Encapsulants for Microelectronic Applications ("Benson").....	9
G.	U.S. Patent No. 8,379,403 ("Waite")	10
H.	IPC-4761	10
III.	LEVEL OF ORDINARY SKILL IN THE ART	11
IV.	CLAIM CONSTRUCTION IS NOT NECESSARY TO DENY INSTITUTION HERE.....	11
V.	THE PETITION'S CHALLENGES ARE NOT REASONABLY LIKELY TO PREVAIL.....	12
A.	The '202 Patent's "Chips" Are More Than Just Bare Dies	13
B.	Grounds 1–4 Fail Because Sun Does Not Teach, Disclose, or Suggest the "bottom Chip" Required By Limitation 1[k] (Claims 1–4 and 6–9).....	14
1.	Sun's "chip 200" does not disclose, teach, or suggest the "bottom chip" because it is a bare die.....	15

2.	Mr. Elenius reinforces Sun’s explanation of “chips.”	17
C.	Grounds 1–2 Fail Because Sun Does Not Disclose, Teach, or Suggest Limitation 1[f] (Claims 1–4 and 6–9)	17
1.	Sun does not disclose, teach, or suggest that the unlabeled portion of Figure 14(a) is a “bonding pad.”	18
2.	It would not have been obvious to apply “top metal pads” to the top of Sun’s vias 390.....	20
D.	Ground 3 Fails Because a POSITA Would Not Be Motivated to Combine Love with Sun (Claims 1–4 and 6– 9).....	22
E.	Ground 4 Fails Because Hu Does Not Cure Sun’s Deficiencies (Claims 1–4 and 6–9)	23
F.	Grounds 5–8 Fail Because Chen Does Not Teach, Disclose, or Suggest the “bottom chip” Required By Limitations 1[k] and 1[l] (Claims 1–9)	23
1.	Chen’s “package component 24” is a bare device die—not the claimed “bottom chip.”	24
2.	Mr. Elenius offers no further analysis of package component 24.	24
3.	Chen’s die is not “mounted to” the “bottom package substrate.”	25
4.	Mr. Elenius does not resolve the deficiencies associated with “packaging component 24.”	27
G.	Grounds 5–8 Fail Because the Petition Does Not Establish the “plurality of top metal pads” Required By Limitation 1[f] (Claims 1–9)	28
1.	Chen’s “RDLs 54” are not the same as its “RDLs 42.”	28
2.	Mr. Elenius offers nothing that cures Chen’s deficiencies.....	29

H.	Grounds 5–6 Fail Because Chen Does Not Disclose, Teach, or Suggest the “plurality of bottom metal pillars” Required By Limitation 1[h] (Claims 1–9).....	30
1.	Chen does not teach, disclose, or suggest anything about the unlabeled features in Figure 9.....	31
2.	The Petition’s “obvious to utilize” fallback is conclusory.	34
I.	Ground 7–8 Fail Because Hu Does Not Cure Sun’s Deficiencies (Claims 1–9).....	35
J.	Ground 9 Fails Because Waite Does Not Disclose the “bottom” or “top metal pillar[s]” Required By Limitations 1[h] and 1[i] (Claims 1–2, 4, 6, and 9).....	36
1.	Waite’s conductive elements are particles held in a stretchy elastomer, not columnar structures.	36
2.	The Petition’s own construction does not contemplate elastomer particles.	38
3.	The Elenius declaration does not cure the gap..	38
VI.	CONCLUSION.....	39

TABLE OF AUTHORITIES

Cases

<i>Arendi S.A.R.L. v. Apple Inc.</i> , 832 F.3d 1355 (Fed. Cir. 2016).....	34
<i>Bell Atl. Network Servs., Inc. v. Covad Commc’ns Grp., Inc.</i> , 262 F.3d 1258 (Fed. Cir. 2001).....	16
<i>In re Kahn</i> , 441 F.3d 977 (Fed. Cir. 2006).....	34
<i>In re Magnum Oil Tools Int’l, Ltd.</i> , 829 F.3d 1364 (Fed. Cir. 2016).....	34
<i>Johnson & Johnson Surgical Vision, Inc. v. Alcon Inc.</i> , IPR2021-01003, 2021 WL 6338373 (P.T.A.B. Nov. 23, 2021).....	11
<i>KSR Int’l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	34
<i>One World Techs., Inc. v. Chevron (HK) Ltd.</i> , PGR2020-00059, 2020 WL 7222691 (P.T.A.B. Dec. 7, 2020).....	39
<i>PlaSmart, Inc. v. Kappos</i> , 482 F. App’x 568 (Fed. Cir. 2012)	32
<i>Realtime Data, LLC v. Iancu</i> , 912 F.3d 1368 (Fed. Cir. 2019).....	12
<i>Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.</i> , 200 F.3d 795 (Fed. Cir. 1999).....	12
<i>Xerox Corp. v. Bytemark, Inc.</i> , IPR2022-00624, Paper 9 (P.T.A.B. Aug. 24, 2022).....	35, 39

Statutes

35 U.S.C. § 314(a) 1

Regulations

37 C.F.R. § 42.65(a)..... 35, 39

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 9,859,202
1003	Declaration of Peter Elenius in support of petition for inter partes review of U.S. Patent No. 9,859,202
1005	U.S. Patent Publication No. 2011/0147908 (“Sun”), published June 23, 2011
1006	U.S. Patent Publication No. 2013/0182402 (“Chen”), published July 18, 2013
1007	U.S. Patent No. 5,334,804 (“Love”), granted Aug. 2, 1994
1008	U.S. Patent Publication No. 2013/0249083 (“Hu”), published Sept. 26, 2013
1009	Benson, et al., Polymer Adhesives and Encapsulants for Microelectronic Applications, Johns Hopkins APL Technical Digest, Volume 28, Number 1 (“Benson”) (2008)
1010	U.S. Patent No. 8,379,403 (“Waite”), granted Feb. 19, 2013
1011	IPC, IPC-4761 Design Guide for Protection of Printed Board Via Structures (“IPC-4761”) (July 2006)
1018	Cohn, et al., Electronic Packaging and Interconnection Handbook, Packaging and Interconnection of Integrated Circuits, Chapter 7, McGraw-Hill (2000)
2039	Rose Anne Acedera, “Overmolding Solutions for 2.5D Semiconductor Packages in Advanced Electronics”, Caplinq Blog, August 26, 2025
2040	“IC Packaging Substrate Technology for Engineers: A Comprehensive Guide”, PCB Master, January 15, 2026

I. INTRODUCTION

Patent Owner TopWire LLC respectfully submits this Preliminary Response and requests that the Board deny institution of inter partes review of U.S. Patent No. 9,859,202 (“the ’202 Patent”) (EX1001). The Petition (Paper 1, “Pet.”) fails to demonstrate a reasonable likelihood of prevailing on any ground, and the Board should decline to institute trial under 35 U.S.C. § 314(a).

The ’202 Patent, titled “Spacer Connector,” claims a package-on-package structure with spacer connectors having metal pillars passing through a core substrate, top metal pads on top ends of the metal pillars, bottom metal pillars on the top package substrate, top metal pillars on the bottom package substrate, and a bottom chip arranged in the space between the two substrates with at least two spacer connectors arranged on opposite sides of the bottom chip. The ’202 Patent addresses the technical challenge of electrically coupling stacked package substrates in a compact, reliable configuration—a chip-level board-on-board structure that was not obvious in view of the prior art.

Petitioners Samsung Electronics Co., Ltd and Samsung Electronics America, Inc. (collectively, “Samsung” or “Petitioner”) challenge claims 1–9 of the ’202 Patent across nine grounds, each predicated on Chen (EX1006), Sun (EX1005), or Waite (EX1010) as the primary reference, combined with Love (EX1007), Hu

(EX1008), Benson (EX1009), or IPC-4761 (EX1011) for certain dependent claims.

But the Petition is fatally flawed for multiple, independent reasons.

First, the Sun-based grounds (Grounds 1–4) fail because Sun never discloses the claimed “bottom chip.” Petitioner maps that limitation to Sun’s “chip 200,” but Sun uses “chip” to mean a bare die—one wire-bonded to a substrate and encased in overmold—not the packaged component the ’202 Patent claims sitting in the open space between substrates. EX1005 at [0047]–[0048]. Sun separately fails to disclose the “top metal pads” of limitation 1[f], and neither Love (Ground 3) nor Hu (Ground 4) cures those defects.

Second, Chen (Grounds 5–8) discloses a fundamentally different, die-level structure and fails three limitations independently. Chen embeds a bare device die inside a molded package rather than mounting a chip between substrates ([1k]/[1l]); it never identifies the rounded Figure 9 features Petitioner calls “bottom metal pillars,” conceding they are “not . . . specifically identified” and supplying the label only by inference (1[h]; Pet. at 66 n.14); and its thin redistribution lines 54—formed on a non-metal dielectric layer—are not the “top metal pads” of limitation 1[f]. EX1006 at [0017].

Third, Ground 9 fails because Waite has no “metal pillars.” Petitioner points to Waite’s “conductive elements 302,” but those are loose conductive particles suspended in a compressible elastomer sheet that conduct only under mechanical

pressure—not the “columnar metal structure, such as a metal post or via” Petitioner’s own construction requires. EX1010 at 4:17–19; Pet. at 5.

For these reasons, and as further detailed below, Patent Owner respectfully requests that the Board deny institution of inter partes review.

II. BACKGROUND

A. Background of the Invention

The ’202 Patent, titled “Spacer Connector,” was filed on June 23, 2016, and claims priority to U.S. Provisional Application No. 62/184,034, filed June 24, 2015. The patent issued on January 2, 2018. EX1001.

The ’202 Patent addresses a challenge in semiconductor packaging: how to electrically couple stacked package substrates in a package-on-package configuration while maintaining a compact and reliable structure.

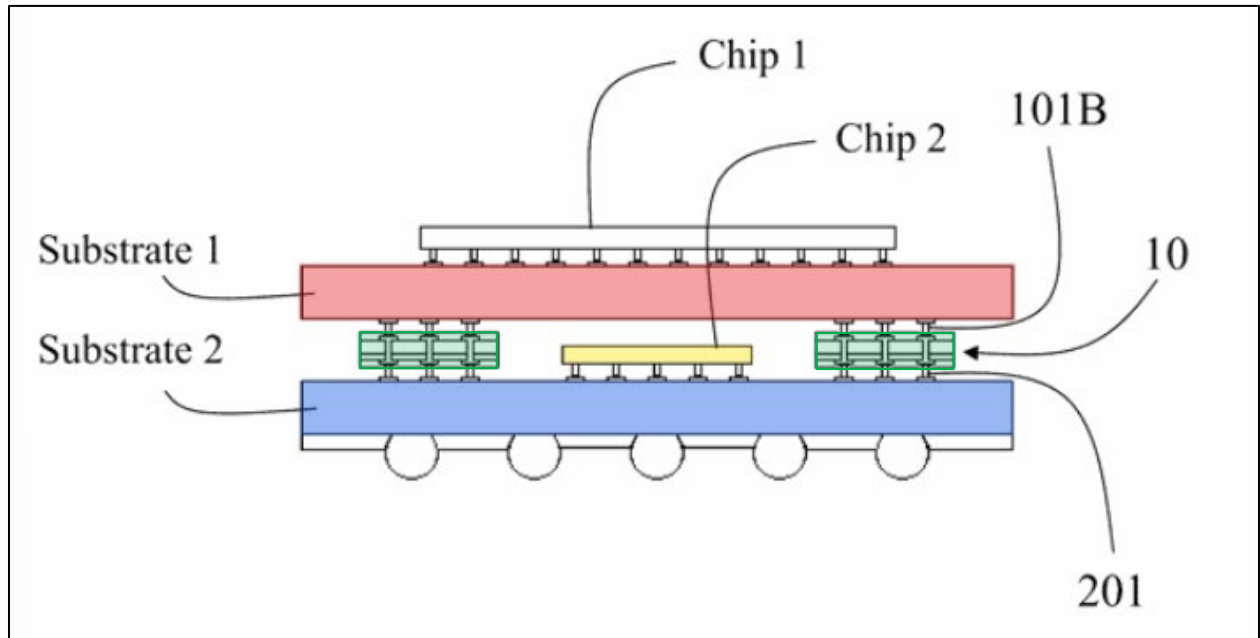
The claimed structure has three principal components: a bottom package substrate (1[a]), a top package substrate stacked above it (1[b]), and at least one spacer connector interposed between them (1[c]). EX1001 at Cl. 1. The spacer connector comprises a core substrate (1[d]), a plurality of metal pillars each passing through the core substrate (1[e]), and a plurality of top metal pads each on the top end of a corresponding metal pillar (1[f]). *Id.* The bottom end of each metal pillar protrudes downwardly from the bottom surface of the core substrate, extending below it. *Id.* (1[h]).

The spacer connector connects to the package substrates above and below through metal pillar interfaces. The top package substrate carries a plurality of bottom metal pillars on its bottom surface, each coupled to a corresponding metal pillar of the spacer connector. *Id.* (1[h]). The bottom package substrate carries a plurality of top metal pillars on its top surface, each coupled to a corresponding metal pillar of the spacer connector. *Id.* (1[i]). This pillar-to-pillar coupling—top package substrate to spacer connector to bottom package substrate—is the electrical backbone of the claimed structure. *Id.* (1[j]).

Critically for this proceeding, claim 1 also requires a bottom chip arranged in the space between the two package substrates and mounted to the top surface of the bottom package substrate (1[k]), with at least two spacer connectors arranged on opposite sides of that chip (1[m]). *Id.* The '202 Patent uses the term “chip”—not “die”—throughout the specification and claims to describe this component. *See, e.g.*, EX1001 at 2:30–35 (“FIG. 8 shows chip 2 is configured on a top center of package substrate 2”), 2:59–65 (“chip 1 is configured on a top center of substrate 1”). The chip sits in the open space the spacer connectors define, mounted directly to the top surface of the bottom package substrate below it. That open-space, direct-mount architecture is illustrated in Figure 8 of the '202 Patent.

The claimed structure is illustrated in Figure 8 of the '202 Patent, which shows two spacer connectors 10 interposed between package substrate 1 (top) and package

substrate 2 (bottom), with chip 2 sitting in the open space between the substrates, mounted to the top center of package substrate 2. EX1001 at 2:28–42.



EX1001 at Figure 8 (annotated).

This configuration—a chip-level board-on-board structure—is distinct from prior art approaches that embedded dies within substrates rather than mounting chips between substrates.

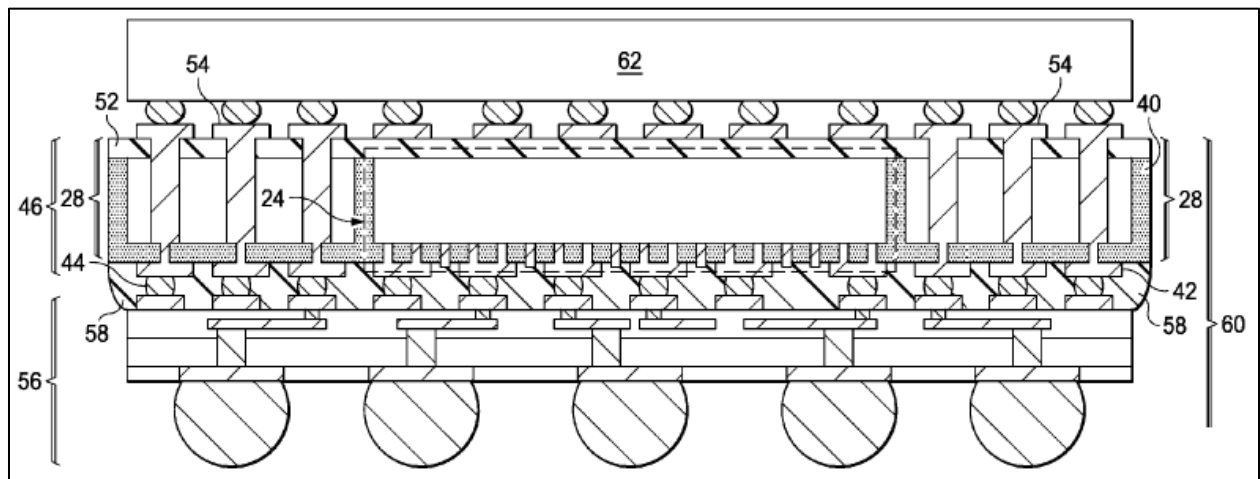
B. U.S. Patent Application Publication No. 2013/0182402 (“Chen”)

Chen is directed to a die-level package-on-package structure using Through-Assembly Via (“TAV”) modules. Importantly, Chen’s structure includes a device die embedded *inside* a substrate—not a chip mounted between package substrates as claimed in the ’202 Patent. *See* EX1006 at [0009], FIG. 9. Chen’s TAV modules serve structurally and functionally different roles from the claimed spacer

connectors: they provide vertical electrical connections through an assembly that encapsulates a die, rather than connectors interposed between two package substrates with a chip arranged in the space between them.

Moreover, key features that Petitioner relies upon in Chen are not actually taught, disclosed, or suggested. For example, Petitioner points to unlabeled, bulb-shaped components in Chen's Figure 9 and asserts—without any support from Chen's specification—that these represent “bottom metal pillars.” Pet. at 66–67. Chen's specification says nothing about the material composition or function of these features.

Chen's Figure 9—the figure the Petition relies upon for both the “bottom chip” and “bottom metal pillar” limitations—is reproduced below. EX1006, FIG. 9.



EX1006 at FIG. 9.

Petitioner also ignores Chen's disclosure for "RDLs 54." That disclosure explains that RDLs 54 are non-metal dielectric layers with redistribution lines—not "top metal pads."

C. U.S. Patent Application Publication No. 2011/0147908 ("Sun")

Sun was published on June 23, 2011. Sun discloses a package-on-package structure in which a first substrate is electrically connected to a third substrate through an intermediate second substrate using metal pillars. *See* EX1005 at [0012], [0066].

Electrical connection between the substrates runs through vias 390 that extend through the second substrate, with first connectors 320 on its lower side and second connectors 310 on its upper side. EX1005 at [0062]–[0063], FIG. 13. Each via 390 has conductive sidewalls 391/392 and a core 395 that "is an insulator" or "a void." EX1005, [0064]. Sun describes the connectors 310/320 as "preferably" taking the form of copper pillars. EX1005 at [0015], [0048].

Critically, Sun's chip is a **bare, wire-bonded die**, not a packaged component. Sun mounts chip 200 directly to the first substrate "by die attachment with wire bonding, flip chip etc.," connecting it with wires 220 to bonding pads on the substrate and then overmolds it. EX1005 at [0047], [0061], [0070]–[0072], FIG. 16. And Sun's vias 390—the features Petitioner maps to the claimed "metal pillars"—terminate in a conductive sidewall and non-solder-wettable core, not in the "top

metal pads” limitation 1[f] requires; Petitioner concedes as much by arguing that pads would have been *obvious to add*. Pet. at 20–21; EX1003, ¶¶ 126–29; EX1005 at [0064]. As discussed in §§V.B–C, these gaps defeat the Sun grounds, and neither Love (Ground 3) nor Hu (Ground 4) supplies what Sun lacks.

D. U.S. Patent No. 5,334,804 (“Love”)

Love issued on August 2, 1994, and is directed to an interconnect structure having a substrate with a plurality of electrically conductive posts. Love teaches forming base pads 20 on conductive posts 14 and adding a fillet 22 to “de-concentrate” mechanical stress and strain at the junction of the post and pad, and further teaches that wide base pads reduce the alignment tolerances required during assembly. EX1007 at 10:5–23, 12:43–60, 13:16–37, FIGs. 5, 6A. The Petition combines Love with Sun in Ground 3, contending that a POSITA would have applied Love’s posts, pads, and fillets to Sun’s connectors to reduce warpage-induced stress and account for alignment errors. Pet. at 41–44. As discussed in Section V, that rationale fails because it rests on a generic, warpage-based benefit untethered to the particular structure being modified and is supported only by an Elenius declaration that repeats the Petition.

E. U.S. Patent Application Publication No. 2013/0249083 (“Hu”)

Hu was published on September 26, 2013, and is directed to a package-on-package assembly in which metal posts are used in combination with a solder

material to overcome the drawbacks of conventional solder balls, including tilted stack structures and poor coplanarity. EX1008 at [0004]–[0005], [0008]. Hu identifies the difficulty of controlling metal-post height uniformity and addresses it by placing conductive bonding layers of offsetting heights on the posts so the resulting posts have the same height. *Id.* at [0008], [0013], [0028]–[0035], FIGs. 2C–2F. The Petition combines Hu with Sun in Ground 4 and with Chen in Ground 7, relying on Hu only for fabrication guidance on implementing the primary reference’s connectors as uniform-height metal pillars. Pet. at 50–56, 85–90. As discussed in Section V, Hu does not cure the primary references’ underlying deficiencies.

F. Benson, Polymer Adhesives and Encapsulants for Microelectronic Applications (“Benson”)

Benson is a 2008 technical article published in the Johns Hopkins APL Technical Digest. It explains that polymer adhesives are commonly used as underfills in microelectronic packaging and that the materials used are typically unfilled epoxies. EX1009 at 1, 3. The Petition invokes Benson only in Ground 8, combining it with Chen and Hu to argue that Chen’s polymer 40 is a dielectric adhesive as required by claim 8. Pet. at 91–93. As discussed in Section V, Benson is a general treatment of underfill materials that does not supply any limitation Chen

and Hu lack, and the Petition's reliance on it rests on the same conclusory reasoning, echoed by the Elenius declaration, that impairs the underlying Chen and Hu grounds.

G. U.S. Patent No. 8,379,403 (“Waite”)

Waite is directed to a “spacer-connector and circuit board assembly” that connects a daughter board holding a device under test to a motherboard in an automated test environment. EX1010 at Abstract, 2:44–56, Fig. 2A. Importantly, Waite does not connect its boards with fixed, columnar conductive structures. Instead, the electrical connections are made through sheets of “conductive elastomer” containing suspended “conductive elements 302” that conduct only when compressed under mechanical pressure. *Id.* at 4:12–19, 4:41–55. Waite emphasizes that these connections “do not require any soldering” and that “precise alignment of the conductive elements 302 is also not required.” *Id.* at 4:26–33.

H. IPC-4761

IPC-4761 is an industry design guide titled “Design Guide for Protection of Printed Board Via Structures,” published in July 2006 by the IPC D-33d Via Protection Task Group. EX1011 at 1. Its subject is via protection—the “methods for the protection of vias on printed boards” through tenting, plugging, filling, covering, capping, or planarizing the via with mask or fill material. *Id.* at 1 (§§1, 1.1), 6–10 (§5). The guide's objectives are to seal vias against contamination, chemistry, and solder migration, to maintain a planar board surface for assembly, and to avoid the

“bulge or bump at the via” that causes soldering defects. *Id.* at 2 (§3.1), 10 (§6.1). IPC-4761 says nothing about semiconductor package-on-package structures, and it does not teach forming a conductive metal pillar that protrudes below the surface of a substrate; to the contrary, its protection types are directed to covering or leveling the via so that the surface remains flat. *See id.* at 1, 6–10.

III. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of denying institution and finding that Petitioner has not met its burden to show a reasonable likelihood of prevailing, TopWire submits that the Board need not determine the level of ordinary skill in the art. *Johnson & Johnson Surgical Vision, Inc. v. Alcon Inc.*, IPR2021-01003, 2021 WL 6338373, at *4 (P.T.A.B. Nov. 23, 2021) (denying institution in part because the Board found that it did “not [need to] determine the level of ordinary skill in the art . . .”).

TopWire reserves the right to address the level of ordinary skill in the event the Board institutes trial.

IV. CLAIM CONSTRUCTION IS NOT NECESSARY TO DENY INSTITUTION HERE

Petitioner proposes constructions for several claim terms: “metal pillar,” “package substrate,” “bottom metal pillars of the top package substrate,” and “top metal pillars of the bottom package substrate.” Pet. at 5–8. For purposes of denying institution because Petitioner has not met its burden to show a reasonable likelihood

of prevailing, TopWire submits the Board need not construe any terms of the challenged claims. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

TopWire reserves the right to assert claim construction positions if trial is ordered.

**V. THE PETITION’S CHALLENGES ARE NOT REASONABLY
LIKELY TO PREVAIL**

The Board should decline to institute trial because the Petition fails to show a reasonable likelihood of prevailing on any ground. Claim 1 is the sole independent claim challenged by Petitioner. The first eight grounds rely on Sun and Chen as the primary references. The final ground relies on Waite as the primary reference. None of the Petition’s challenges are reasonably likely to prevail because Petitioner does not meet its burden to show obviousness based on Sun, Chen, or Waite—whether combined with Love, Hu, Benson, or IPC-4761.

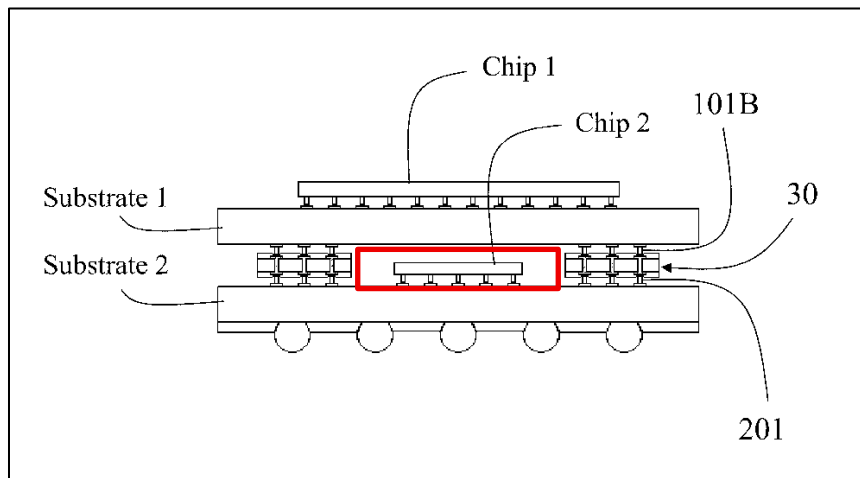
A. The '202 Patent's "Chips" Are More Than Just Bare Dies

As explained below, some of the primary references Petitioner relies on only disclose bare dies. This is also consistent with Petitioner's proposed construction¹ of "package substrate": "A POSITA would have understood 'package substrate' to refer to a substrate that is part of a semiconductor package, that provides mechanical support and electrical interconnection with a *semiconductor die*." Pet. at 6 (emphasis added). But in view of the intrinsic record, a POSITA would know the "chips" in the '202 Patent are not just bare dies.

Petitioner acknowledges bare dies "must be properly packaged to interact and connect to the external circuitry." EX1003 ¶ 46. This "assures environmental protection" for the bare die and "provides for complete testing and high yield assembly to the next level of interconnection." EX1018 at 4. In Sun and Chen, for example, the bare dies are properly packaged between substrates such that there is no air gap between the dies and the substrates. Sun discloses an overmold 120 that fills the air gap between the bare die and the substrates while Chen explains how the die is embedded inside package 46. EX1005 at [0059]; EX1006 at [0014].

¹ Petitioner explains that it "present[s] invalidity positions under . . . Petitioners' construction (Grounds 1–9)." Pet. at 8.

In the claimed structure of the '202 Patent, the “bottom chip”, for example, is not just a bare die because it is exposed in the open air “space” (see below) defined by the “spacer connector” arranged between the top and bottom package substrates. A bare die cannot exist in an open-air space because such exposure would leave the die unprotected.



EX1001 at FIG. 8 (annotated to show the bottom chip within the open air “space”).

B. Grounds 1–4 Fail Because Sun Does Not Teach, Disclose, or Suggest the “bottom Chip” Required By Limitation 1[k] (Claims 1–4 and 6–9)

Grounds 1–4 of the Petition are fatally deficient because Sun does not disclose, teach, or suggest “a bottom chip arranged in the space between the bottom package substrate and the top package substrate.” EX1001 at Cl. 1. The “chip 200” Petitioner identifies as the “bottom chip” is a bare die. But the “bottom chip” is more than just a bare die. Because Grounds 1–4 only rely on Sun for this limitation, these grounds fail to render the '202 Patent invalid.

1. Sun's "chip 200" does not disclose, teach, or suggest the "bottom chip" because it is a bare die.

Petitioner identifies "chip 200" as the "bottom chip." Pet. at 27. Although the '202 Patent and Sun both use the word "chip," they do not refer to the same structure. The '202 Patent uses "chip" according to its plain and ordinary meaning, but Sun departs from this meaning and instead uses "chip" to refer to a bare die. For example, Sun explains that chip 200 is a die bonded to first substrate 110 and encased by overmold 120:

A chip **200**, which may be a memory chip or a processor, is mounted to the first substrate **100**. It may be mounted by any appropriate method, for example *die attachment with wire bonding, flip chip etc.* Wires **220** connect a bonding pad 210 on top of the chip **200** with a bonding pad **240** on the upper side of the first substrate **110**

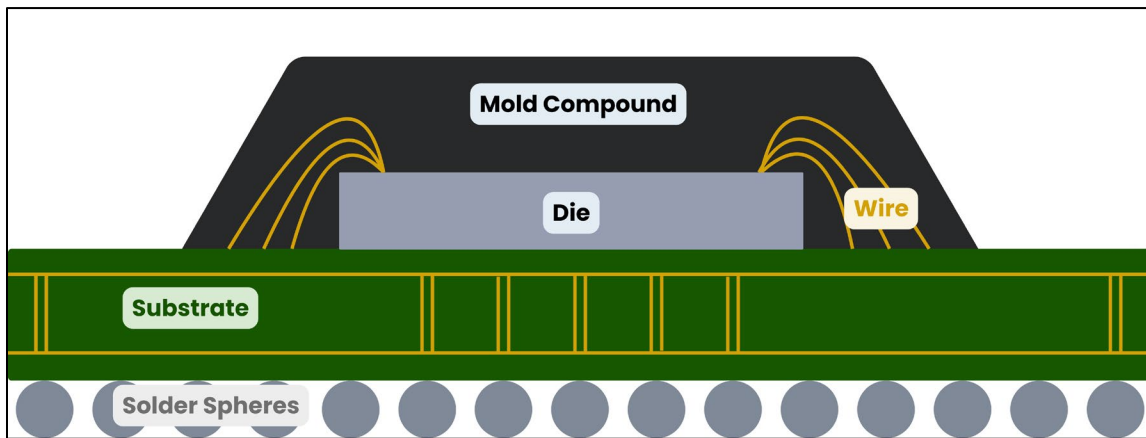
The assembly is overmolded with a molding material **120**. The molding material covers the chip **200**, the upper surface of the first substrate **110** and the second substrate **300**

EX1005 at [0047]–[0048] (emphasis added).

Sun only uses the term "chip" to refer to dies. All embodiments of the "chips" disclosed in the figures and specification illustrate dies wire bonded to substrates and overmold materials covering the "chips." *Id.* at [0047]–[0051], [0058]–[0061], FIGs 2–5, 12. Moreover, Sun's method for manufacturing the modules that contains these "chips" explains how "one or more wires **220**, **220 a** are used to connect the chips to bonding pads on the first (upper) side of the first substrate **100**." *Id.* at

[0071]. Accordingly, Sun defines “chips” as “dies” by implication. *See Bell Atl. Network Servs., Inc. v. Covad Commc’ns Grp., Inc.*, 262 F.3d 1258, 1268 (Fed. Cir. 2001).

Industry literature describing conventional packaging confirms the same distinction. As one technical expert explains, “[f]rom 1965 to 2010, 2D packaging, also called planar integration, was the main way to assemble integrated circuits. In this method, chips sit side-by-side on a substrate or PCB. Manufacturers connect them using wire bonding or flip chip.”² EX2039; *see also* EX2040.



Example of 2D Packaging

² The priority date for Sun is December 17, 2009—a period in which die wire bonding was prevalent.

The 2D packaging illustration shown above is virtually identical to Sun's chip module. Both include dies wire bonded to substrates and an overmold compound covering the dies and wires.

2. Mr. Elenius reinforces Sun's explanation of "chips."

Petitioner's expert, Mr. Elenius, does not disagree that Sun's chips are "dies." He presented his invalidity position for Sun with the understanding that "'package substrate' refers to a substrate used for *semiconductor die-level packaging*." EX1003 ¶¶ 82, 88 (emphasis added). His "analysis" is nothing more than direct quotes from Sun. *Id.* ¶ 114. Accordingly, Mr. Elenius does nothing to cure Sun's deficiencies with respect to the "bottom chip."

Because Grounds 1–4 only rely on Sun to render limitation 1[k] anticipated and/or obvious, and every challenged claim depends from claim 1, this failure of proof is independently fatal to Grounds 1–4.

C. Grounds 1–2 Fail Because Sun Does Not Disclose, Teach, or Suggest Limitation 1[f] (Claims 1–4 and 6–9)

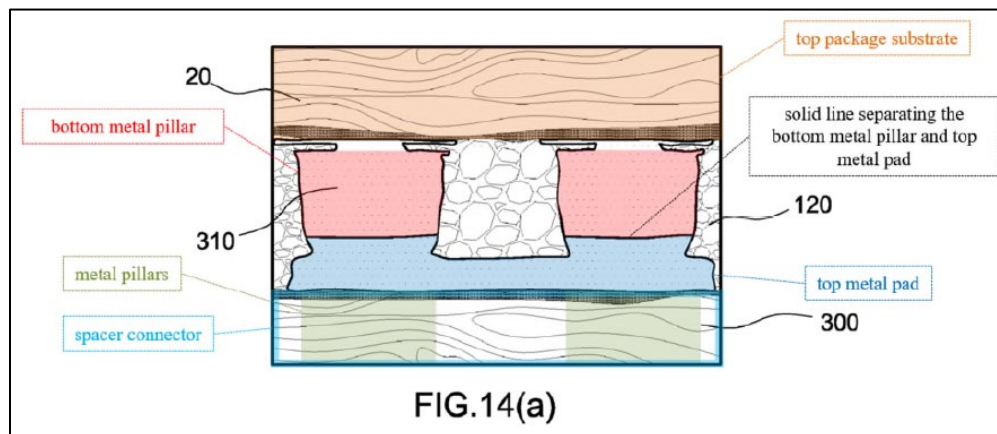
Grounds 1–2 of the Petition are fatally deficient because Sun does not disclose, teach, or suggest "a plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars." EX1001 at Cl. 1. Petitioner based their flawed analysis of limitation 1[f] on unlabeled and undisclosed components in Sun's Figure 14(a). Sun does not expressly disclose limitation 1[f], and Figure 14(a) does not clearly illustrate this limitation. Nor does the evidence

Petitioner offers establish how it would have been obvious for a POSITA to modify Sun with top metal pads to render claim limitation 1[f] obvious. Because Grounds 1–2 only rely on Sun for this limitation, these grounds fail to render the '202 Patent invalid.

1. Sun does not disclose, teach, or suggest that the unlabeled portion of Figure 14(a) is a “bonding pad.”

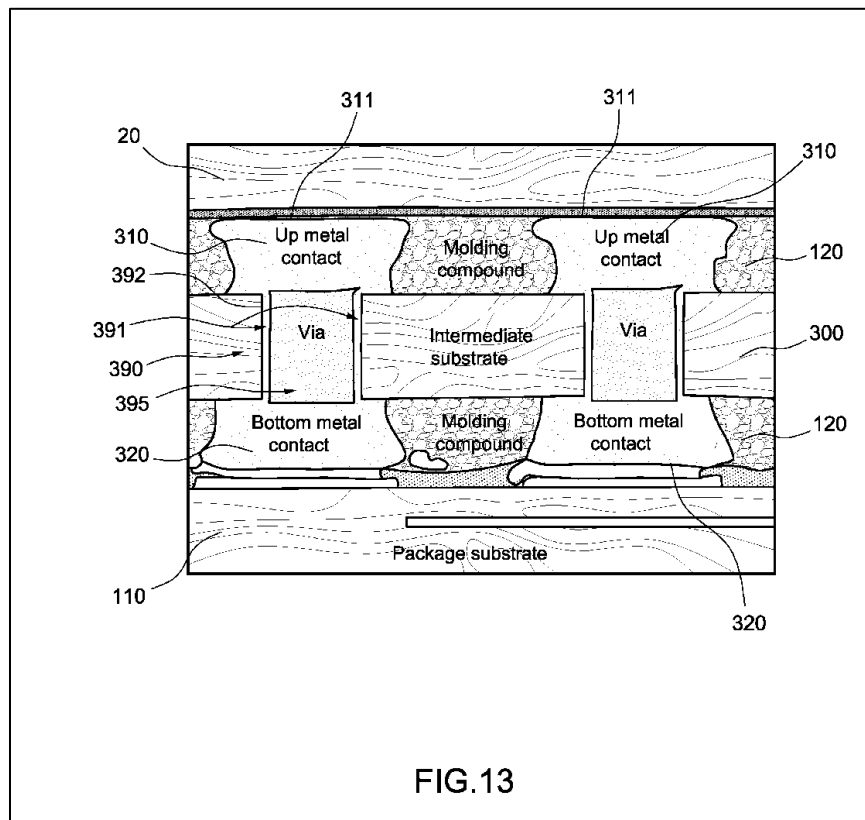
Petitioner claims that Sun discloses “bonding pads” and that these features disclose, teach, or suggest limitation 1[f]. Pet. at 18–19. But all Sun provides is that “[a] small amount of solder or bonding pads may [be] used to connect the metal pillars to the respective other substrates.” EX1005 at [0066]. Sun does not explain *what* this bonding pad is made of, *where* this bonding pad is located, or *how* this bonding pad is configured. In short, the specification offers no meaningful information about these bonding pads.

Nevertheless, Petitioner points to an unlabeled region in Sun’s Figure 14(a) and identifies this region as the “bonding pad.”

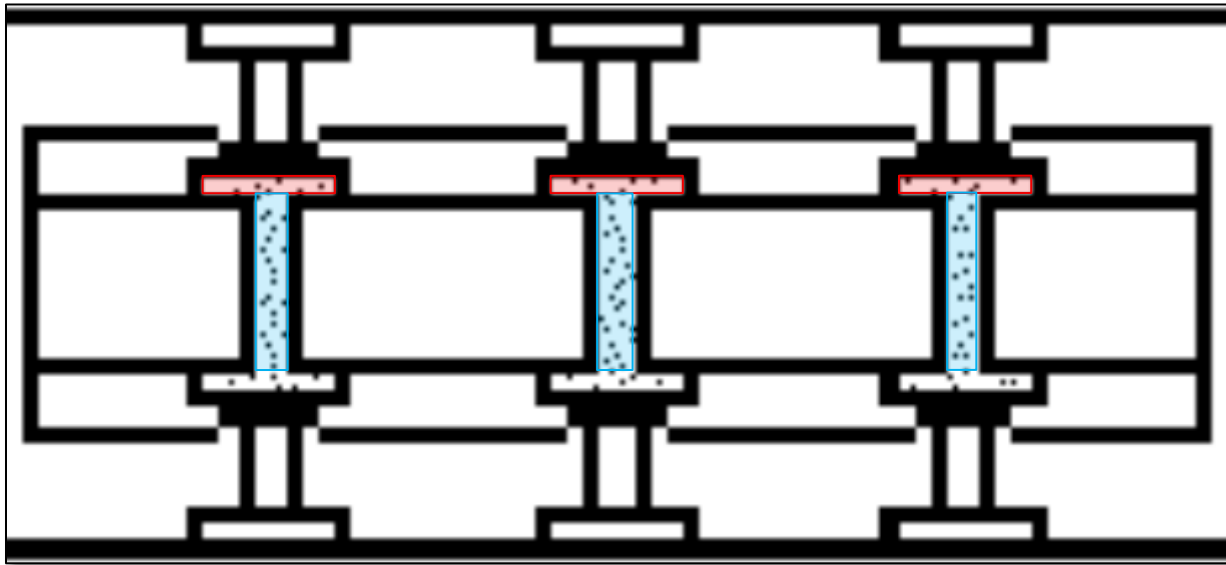


Pet. at 20 (Petitioner annotation of EX1005 at FIG. 14(a)).

There is no evidence that the “line” Petitioner identifies “separat[es] the bottom metal pillar and the top metal pad.” *Id.* In fact, the portions Petitioner identifies as the “bottom metal pillar” and the “top metal pad” are part of one structure: second connectors 310. The second connectors 310 “have the same structure as the first connectors 320.” EX1005 at [0066]. Indeed, “[t]he first and second connectors preferably take the form of metal pillars, for example copper pillars.” *Id.* [0061]. The first connectors 320 (shown below) do not contain any “line” separating different portions of the structure. Accordingly, Figure 14(a) does not disclose, teach, or suggest limitation 1[f].



The '202 Patent further confirms this conclusion. The **top metal pads** are well-defined structures directly corresponding to **metal pillars**. By contrast, Petitioner's alleged "top metal pads" are not defined anywhere in the specification, they are not clearly illustrated in any figures, and they do not bear any clear correspondence to the alleged "metal pillars."



EX1001 at FIG. 8 (cropped and annotated).

2. It would not have been obvious to apply "top metal pads" to the top of Sun's vias 390.

First, Petitioner claims "the structure of vias 390 requires a top metal pad to facilitate electrical connections, and a POSITA would have found it obvious to apply such pads." Pet. at 20; EX1003 ¶ 127. But Sun discloses different via embodiments that obviate the need for "top metal pads." Sun explains that the sidewalls or core of the vias can be electrically conductive. EX1005 at [0018]. The conductive

components in the vias 390 are more than sufficient to establish the electrical connection between Sun's electrical connectors because "the first and second electrical connectors which the via connects are [preferably] three separate pieces." *Id.* at [0017]. Accordingly, Sun has no need for the "top metal pads" on the vias 390.

Second, Petitioner's claim that top metal pads will address Sun's misalignment errors between interconnect structures is unfounded. Pet. at 21; EX1003 ¶ 128. Love, the reference Petitioner relies on for this claim, explains that applying separate photo-resist layers during the semiconductor fabrication process can create positional misalignment between interconnect structures. EX1007 at 13:30–41. But Sun's process for manufacturing the claimed "module" does not involve photolithography, so there is no risk of misalignment errors between interconnect structures. EX1005 at [0066]–[0074]. Accordingly, Sun has no need for "top metal pads."

Third, Petitioner's own mapping undermines its assertion that applying metal pads over Sun's vias would "provide the benefit of preventing solder, solder resist, and other contaminants from flowing into the vias." Pet. at 21; EX1003 ¶ 129. Petitioner claims that the "top metal pad" corresponds to a solder bonding pad shown in Figure 14(a). Pet. at 18–19. Assuming this is true³, Sun connects its vias directly

³ TopWire does not concede that Figure 14(a) illustrates a "top metal pad."

to solder with no intervening metal pad. In other words, Sun itself forgoes the very anti-contamination benefit Petitioner offers as the reason a POSITA would have added pads. This contradicts the motivation on which the Petition relies.

Because Grounds 1–2 only rely on Sun to render limitation 1[f] anticipated and/or obvious, and every challenged claim depends from claim 1, this failure of proof is independently fatal to Grounds 1–2.

D. Ground 3 Fails Because a POSITA Would Not Be Motivated to Combine Love with Sun (Claims 1–4 and 6–9)

Petitioner claims that “[a] POSITA would have been motivated to apply Love’s base pads 20 to Sun’s vias 390 to achieve the benefits of reducing mechanical stress from warping and accommodating alignment errors as taught by Love.” Pet. at 46. As explained above, there is no risk of alignment errors in Sun’s interconnect structures because manufacturing the claimed “module” does not involve photolithography. § V.C.2.

Sun also already addresses the problem of substrate warpage. Sun identifies a prior art package-on-package assembly in FIG. 1 in which solder joints connect upper and lower packages. There, “warpage of one or both substrates **20, 40** can deform the connection and solder joints between the upper and lower packages.” EX1005 at [0011]. To address the problems associated with substrate warpage, the

intermediate second substrate and second connectors Sun disclose are overmolded, making the overall assembly “less prone to warpage.” *Id.* at [0014].

Because there is no risk of alignment errors in Sun’s interconnect structures and the claimed assembly already addresses problems associated with substrate warpage, there is no motivation to combine Love with Sun. Accordingly, the absence of any motivation to combine Love with Sun is independently fatal to Ground 3.

E. Ground 4 Fails Because Hu Does Not Cure Sun’s Deficiencies (Claims 1–4 and 6–9)

Petitioner acknowledges that “the combination of Sun and Hu does not materially alter the final package structure of Sun but merely changes the processing steps.” Pet. at 56. Because Hu does not cure Sun’s deficiencies, Ground 4 fails for the reasons set forth in Section V.B–C.

F. Grounds 5–8 Fail Because Chen Does Not Teach, Disclose, or Suggest the “bottom chip” Required By Limitations 1[k] and 1[l] (Claims 1–9)

Grounds 5–8 of the Petition are fatally deficient because Chen does not teach, disclose, or suggest a “bottom chip arranged in the space between the bottom package substrate and the top package substrate” as required by limitation 1[k], or a bottom chip “mounted to the top surface of the bottom package substrate” as required by limitation 1[l]. EX1001 at Cl. 1. Chen’s failure is twofold: (1) the package component 24 is not a “bottom chip,” and (2) that component is not mounted on the

top surface of package component 56. Because Grounds 5–8 only rely on Chen for these limitations, these grounds fail to render the '202 Patent invalid.

1. Chen’s “package component 24” is a bare device die—not the claimed “bottom chip.”

The Petition maps limitations 1[k] and 1[l] to Chen’s “package component 24.” Chen describes package component 24 as including “one or a plurality of device *dies*” or “a packaging component that includes device *die(s)*.” EX1006 at [0009] (emphasis added); Pet. at 70 (emphasizing “die”). Petitioner only refers to the bare die embodiment of package component 24, and it never explains why this embodiment is a “bottom chip.” The reason is simple: chips and dies are different terms with fundamentally different structures. As explained above, the '202 Patent’s concept of “chips” includes more than just bare dies. § V.A. But package component 24 is nothing more than bare die(s).

2. Mr. Elenius offers no further analysis of package component 24.

Mr. Elenius agrees that the bare die embodiment of packaging component 24 discloses, teaches, and suggests the “bottom chip.” EX1003 ¶ 244. He quotes the same passages from Chen as the Petition, and he offers no explanation for why this embodiment is a “bottom chip.”

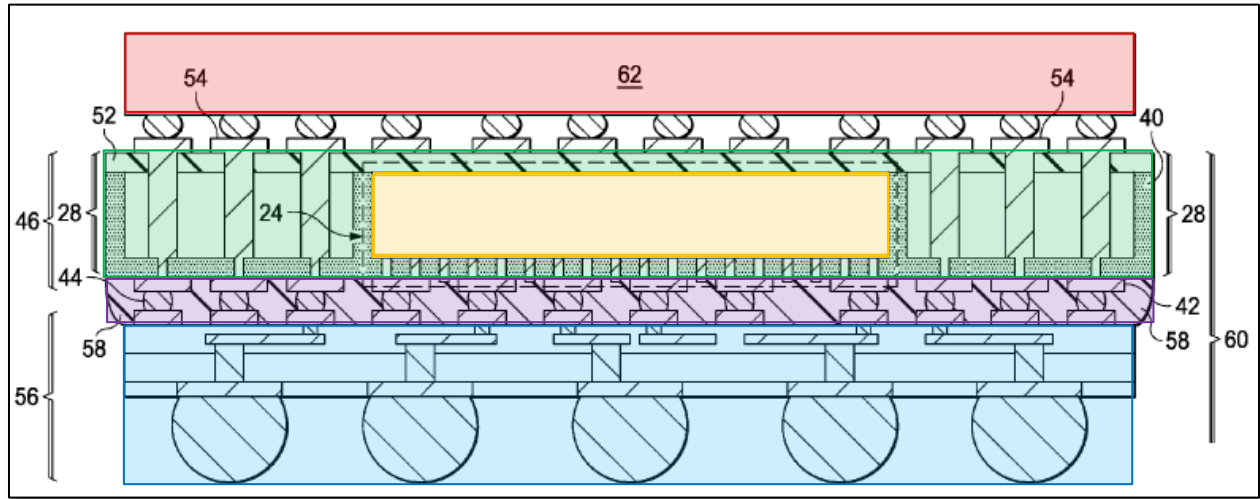
Because Grounds 5–8 only rely on Chen to render limitation 1[k] anticipated and/or obvious, and every challenged claim depends from claim 1, this failure of proof is independently fatal to Grounds 5–8.

3. Chen's die is not "mounted to" the "bottom package substrate."

Even setting aside the die/chip distinction, Chen's structure independently fails limitation 1[I]. Petitioner's analysis for this limitation consists of a single statement: "package component 24 [is] mounted to the top surface of package component 56 *via connectors 44*." Pet. at 71 (emphasis added). Here, Petitioner admits that the package component 24 is not mounted directly on top of the top surface of package component 56 because via connectors 44 separate package component 24 from package component 56. This alone proves fatal for Petitioner's argument. Package component 24 cannot be "mounted to the top surface of package component 56" if there is something separating these two components.

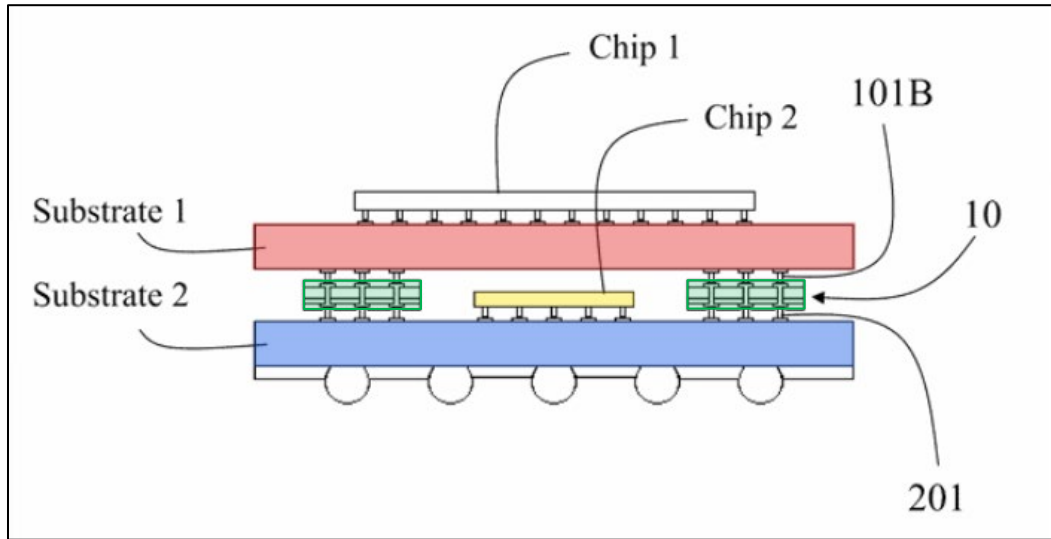
Even worse, Chen discloses more than just via connectors 44 separating package component 24 from package component 56. Package component 24 is embedded inside package 46. EX1006 at [0014] ("Throughout the description, the structure including package component 24, TAV modules 28, and polymer 40 is referred to as package 46."). Within package 46, package component 24 is in direct contact with polymer 40, which is "molded on package component 24 and TAV modules 28" and "fills the gaps between package component 24 and TAV modules 28." *Id.* at [0013]. Package component 24 is therefore "mounted to the top surface" of polymer 40.

More structures and components further separate package 46 from package component 56, including redistribution lines 42, connectors 44, and polymer 58. *Id.* at FIG. 9, [0018] (“Polymer 58 is dispensed between package 46 and package component 56.”).



Id. at FIG. 9 (annotated).

The contrast with the claimed invention further underscores Petitioner’s flawed invalidity theory. The ’202 Patent claims a structure in which a chip sits in the open space defined by the spacer connectors and is mounted directly to the top surface of the bottom package substrate: “FIG. 8 shows chip 2 is configured on a top center of package substrate 2.” EX1001 at 2:33–34.



Id. at FIG. 8 (annotated).

Chen’s architecture—an unpackaged die encapsulated in a molded assembly that is then bonded to a substrate through underfill polymer—is not that structure, and the Petition never confronts the difference.

4. Mr. Elenius does not resolve the deficiencies associated with “packaging component 24.”

Mr. Elenius only raises one new argument in his declaration: the “bottom chip” in the ’202 patent is similar to Chen’s package component 24 because the “bottom chip” is connected to the top surface of bottom package substrate by metal connectors. EX1003 ¶ 246. These “metal connectors”, however, are part of the “bottom chip.” The “bottom chip” is therefore directly connected to the “top surface of the bottom package substrate.” The same is not true for Chen’s package component 24.

Because Grounds 5–8 only rely on Chen to render limitation 1[l] anticipated and/or obvious, and every challenged claim depends from claim 1, this failure of proof is independently fatal to Grounds 5–8.

G. Grounds 5–8 Fail Because the Petition Does Not Establish the “plurality of top metal pads” Required By Limitation 1[f] (Claims 1–9)

Grounds 5–8 are fatally deficient because Chen does not disclose, teach, or suggest a “plurality of top metal pads, each on a top end of a corresponding metal pillar among the plurality of metal pillars” as required by limitation 1[f]. EX1001 at Cl. 1. The Petition improperly conflates RDLs 42 with RDLs 54. While both are redistribution lines, they contain different disclosures. RDLs 54 are non-metal, dielectric layers with redistribution lines—not metal layers. Because Grounds 5–8 only rely on Chen for this limitation, these grounds fail to render the ’202 Patent invalid.

1. Chen’s “RDLs 54” are not the same as its “RDLs 42.”

Petitioner identifies RDLs 54—not RDLs 42—as the “top metal pads.” Pet at 63. But instead of focusing on what RDLs 54 disclose, Petitioner focused on what RDLs 42 discloses. For example, Petitioner seized on the “metal layer” in RDLs 42: “RDLs 42 may be formed by depositing a metal layer, and then patterning the metal layer.” *Id.* at 63 (quoting EX1006 at [0014]); EX1003 ¶ 226. Petitioner then claimed that *RDLs 54* included metal layers because “Chen uses the same term

‘Redistribution Lines (RDLs)’ for both RDLs 54 and RDLs 42, which share the exact same shape/shade in FIG. 9.” EX1003 ¶ 226. This conclusion, however, contradicts the specification.

Petitioner conveniently ignored Chen’s explanation of how RDLs 54 are formed: “dielectric layer **52** is formed on the illustrated top surface of package **46**” and “RDLs **54** are then formed on dielectric layer **52** and connected to RDLs **54**.” EX1006 at [0017]. In other words, RDL 54 is a non-metal dielectric layer with redistribution lines. Accordingly, a non-metal dielectric layer with redistribution lines is not a “top metal pad.”

In view of Chen’s failure to disclose, teach, or suggest the “top metal pad”, Petitioner also fails to establish that it would have been obvious for a POSITA to implement metal pads as well known in the art. Pet. at 64; EX1003 ¶ 227. Petitioner does not identify any specific problems in Chen that top metal pads address. Accordingly, a POSITA would have no motivation to combine metal pads well known in the art with Chen.

2. Mr. Elenius offers nothing that cures Chen’s deficiencies.

Mr. Elenius primarily focuses on one sentence in Chen: “TAV modules 28 may include redistribution layer(s) [RDLs] that include redistribution lines and *metal pads* on the top sides of TAV modules 28.” EX1003 ¶ 226 (quoting EX1006 at [0011]). Chen, however, does not identify these redistribution layers as RDLs

54—the feature Petitioner identified as the “top metal pad.” More importantly, Chen explains that RDL 54 is a non-metal dielectric layer with redistribution lines. EX1006 at [0017]. Instead of engaging with this evidence, Mr. Elenius ignores it. This renders his opinions on this limitation deficient.

Because Grounds 5–8 only rely on Chen to render limitation 1[f] anticipated and/or obvious, and every challenged claim depends from claim 1, this failure of proof is independently fatal to Grounds 5–8.

H. Grounds 5–6 Fail Because Chen Does Not Disclose, Teach, or Suggest the “plurality of bottom metal pillars” Required By Limitation 1[h] (Claims 1–9)

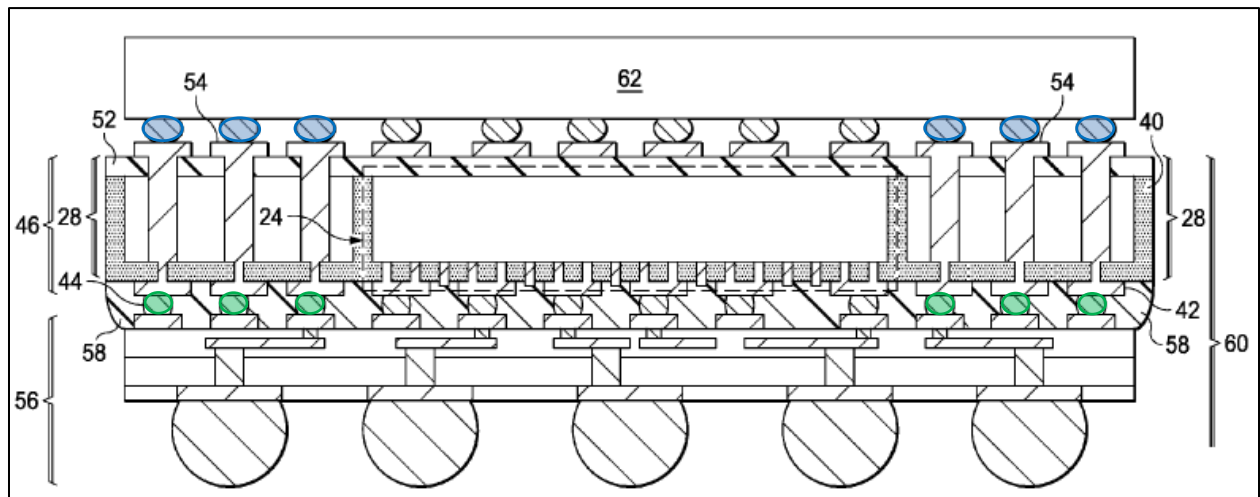
Claim 1 separately requires that “the top package substrate has, on a bottom surface thereof, a plurality of bottom metal pillars each coupled to a corresponding metal pillar among the plurality of metal pillars of the spacer connector.” EX1001 at Cl. 1. For this limitation, Grounds 5–6 rest on the same evidence: unlabeled, rounded features in Chen’s Figure 9. The Petition relies on these [unlabeled connectors](#) colored in Figure 9 of Chen as disclosing the claimed “plurality of bottom metal pillars.” Pet. at 65–66; EX1003 ¶¶ 231–34. That reliance fails three times over: Chen does not teach, disclose, or suggest anything about the unlabeled features; the Petition’s fallback assertion that Chen renders the bottom metal pillars obvious is unsupported attorney argument echoed by a conclusory expert declaration; and Hu does not supply any reason—apart from the ’202 Patent’s own claims—to modify

Chen. Because limitation 1[h] is required by claim 1, and every challenged claim depends from claim 1, this failure of proof is independently fatal to Grounds 5–6.

1. Chen does not teach, disclose, or suggest anything about the unlabeled features in Figure 9.

The Petition’s primary theory is that Chen itself teaches, discloses, or suggests the claimed bottom metal pillars. It does not, and the Petition concedes as much. Chen’s specification never identifies the **features** that Petitioner relies on. Paragraph [0019]—the only passage describing Figure 9—states that “FIG. 9 illustrates the bonding of top package component 62 to bottom package 60” and that “TAV modules 28 are used to electrically couple the circuit devices in package component 62 to package component 56.” EX1006 at [0019]. It assigns these **features** no reference numeral, no name, no structure, and no material composition. The Petition admits the gap: it concedes that “not all of connectors in FIG. 9 are specifically identified as connectors 44,” and it supplies the “connectors 44” label only by inference, asserting that “a POSITA would have understood” the features to be connectors 44 “given the same shading applied to all connectors and the same function served by both sets of connectors.” Pet. at 66 n.14; EX1003 ¶ 232. That Petitioner *asserts* the unlabeled features are the same as a labeled feature does not make them so, and it does not convert Chen’s silence into a disclosure.

The **unlabeled features** the Petition relies upon are shown in Figure 9 of Chen, annotated below. They appear at the top of the TAV modules 28, between the TAV modules and top package component 62, without any reference numeral, name, or material designation in Chen's specification. EX1006 at [0019]. Their rounded, dome shape is also visible—characteristic of a reflowed solder bump, not the straight-sided profile of a metal pillar. *Compare* EX1005 at [0066] (metal pillars have “fine pitch and a well defined shape”) *with id.* (solder balls have “a less well defined shape”).



That admission should end the inquiry. Patent drawings “can be used as prior art, without referring to the surrounding description, *only if the prior art features are clearly disclosed by the drawing.*” *PlaSmart, Inc. v. Kappos*, 482 F. App’x 568, 571 (Fed. Cir. 2012) (emphasis added). An unlabeled, undescribed shape in a cross-

sectional figure does not “clearly disclose” that the depicted feature is metal—much less that it is a metal *pillar*.

The Petition’s attempt to fill the gap by visual inference—that the **features** are nearly the same as **connectors 44**, Pet. at 66-67—defeats itself. The Petition relies on Chen’s paragraph [0014] for the assertion that **[c]onnectors 44** may also “include solder balls . . . metal pillars, or metal pillars and solder caps, which may also be formed through plating.” Pet. at 66 (quoting EX1006 at [0014]). But the Petition omits what precedes that sentence: in Chen’s lead embodiments, connectors 44 are solder. Chen teaches that “the formation of **connectors 44** includes placing solder balls on the exposed portions of RDLs 42, and then reflowing the solder balls,” or alternatively “performing a plating step to form solder regions on RDLs 42, and then reflowing the solder regions”—with metal pillars appearing only in a final “may also include” option. EX1006 at [0014]. And the Petition’s own construction asserts that a “metal pillar . . . cannot be realized by solder balls or other solder structures.” Pet. at 5–6. Taking the Petition’s visual-similarity premise at face value, then, it establishes at most that the **unlabeled features** resemble structures Chen forms from reflowed solder—structures that, by the Petition’s own construction, are not metal pillars. The drawing itself confirms the point: the features are rounded, bulb-shaped domes—the signature of a reflowed solder bump, rather than pillars.

2. The Petition's "obvious to utilize" fallback is conclusory.

Apparently recognizing that Chen discloses no bottom metal pillars, the Petition falls back on obviousness. Its stated rationale—that solder balls have “large” “lateral sizes” while metal pillars’ “pitches and sizes may be very small,” so a POSITA would use pillars for “fine-pitch” PoP (Pet. at 67; EX1006, [0002], [0021])—is hindsight-driven. The Petition offers no reason why a person of ordinary skill building Chen’s structure would have selected pillars for these features when Chen itself depicts them as solder, EX1006, Fig. 9, let alone for different, unlabeled features that Chen never identifies as connectors 44. “To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). There must be “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). And an appeal to what a skilled artisan “would have found obvious . . . according to the . . . knowledge of a POSITA” cannot serve “as a wholesale substitute for reasoned analysis and evidentiary support” where, as here, it is invoked to supply “a limitation missing from the prior art references.” Pet. at 67; *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361–62 (Fed. Cir. 2016).

Mr. Elenius adds nothing. His declaration repeats the Petition’s visual comparison, asserts that the unlabeled features are the same as connectors 44,” quotes the same lone sentence of paragraph [0014], and concludes—again, in a single sentence—that “a POSITA would have found it obvious to implement (upper) connectors 44 as metal pillars to address the drawbacks of solder balls.” EX1003 ¶ 237. Like the Petition, Mr. Elenius never acknowledges that Chen forms connectors 44 from reflowed solder in the embodiments Chen actually describes, and he identifies no facts or data supporting the leap from an unlabeled shape to “metal pillar.” Expert testimony that merely repeats the Petition’s conclusory assertions without disclosing the underlying facts or data on which it is based “is entitled to little or no weight.” 37 C.F.R. § 42.65(a); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (P.T.A.B. Aug. 24, 2022) (precedential).

I. Ground 7–8 Fail Because Hu Does Not Cure Chen’s Deficiencies (Claims 1–9)

Petitioner acknowledges that “the combination of *Chen* and *Hu* does not materially alter the final package structure of *Chen* but merely implement *Chen*’s connectors with *Hu*’s metal pillars and processing steps.” Pet. at 90. Because Hu does not cure Chen’s deficiencies, Grounds 7 and 8 fail for the reasons set forth in Section V.F–H.

J. Ground 9 Fails Because Waite Does Not Disclose the “bottom” or “top metal pillar[s]” Required By Limitations 1[h] and 1[i] (Claims 1–2, 4, 6, and 9)

The Petition’s Ground 9 challenge also fails. Limitations 1[h] and 1[i] require, respectively, that the top package substrate have a “plurality of bottom metal pillars” on its bottom surface and that the bottom package substrate have “a plurality of top metal pillars” on its top surface, each “coupled to a corresponding metal pillar of the spacer connector.” EX1001 at Cl. 1. For both of these “metal pillars,” the Petition points to a structure in Waite called the “conductive elements 302” of Waite’s conductive elastomers. Pet. at 104–107. But these conductive elements are not pillars at all. They are loose conductive particles suspended within a compressible elastomeric sheet, and they fail to satisfy the ordinary meaning of metal pillar, much less the construction that the Petition advances. Because every challenged claim depends from claim 1, which requires “bottom” and “top metal pillars,” this failure is independently dispositive of Ground 9.

1. Waite’s conductive elements are particles held in a stretchy elastomer, not columnar structures.

Waite is directed to systems “for daughter boards connected to printed circuit boards.” EX1010 at 2:8–9. But the daughter board is not coupled to the motherboard by a fixed and conductive column structure, but through two sheets of “conductive elastomer” clamped between boards under mechanical pressure. EX1010 at 4:12–15 (“the first and second conductive elastomers 206, 208 each include vertically

coupled conductive elements 302 in a high density grid that provide high quality coupling”); 4:65–5:1 (“The elastomeric conductive interface may be formed of a material that is conductive under a characteristic pressure [which] may include a range of pressures at which the elastomeric conductive interface 206, 208 is conductive.”). Waite describes the “conductive elements” the Petition relies on as undifferentiated, high-density suspension of particulate matter within those sheets. *Id.* at 4:17-19 (“conductive elements 302 may include wires, balls, spheres, cubes, segments, particles, and the like, that can be utilized as a conductive path.”); 4:12-15 (“the first and second conductive elastomers 206, 208 each include vertically coupled conductive elements 302 in a high density grid.”) Indeed, Waite explicitly teaches that its conductive elements are not discrete, positioned pillars: “precise alignment of the conductive elements 302 is also not required as the high density grid is configured to provide multiple vertical conductive paths between the tops and bottoms of the conductive elastomers.” *Id.* at 4:29-33. A dispersion of particles in a stretchy sheet, which conducts only when compressed and requires no defined arrangement, is far from the “bottom metal pillar” required by the ’202 Patent. That the Petition alternatively lists “spring pins, or formed pin type connectors” (Pet. at 104; EX1010 at 4:56–63) does not help it: each is offered without explanation as an interchangeable form of the same conductive element 302, and a compressible, pressure-actuated contact that is suspended in an elastomer, whether a particle or a

spring pin, is still not the “columnar metal structure, such as a metal post or via” that the Petition’s own construction requires. EX1010 at 4:41–55; Pet. at 5.

2. The Petition’s own construction does not contemplate elastomer particles.

The Petition asks the Board to construe “metal pillar” as “a columnar metal structure, such as a metal post or via,” and represents that this construction reflects the ordinary and customary meaning a POSITA would apply. Pet. at 5. Petitioner supports this construction by explaining that the claims recite metal pillars “passing through the core substrate” and “protrud[ing] downwardly,” which “indicat[es] a columnar structure.” *Id.* at 5–6. Petitioner also argues that the specification illustrates the metal pillars “as columnar metal posts or vias. *Id.* Nothing in that construction contemplates filler suspended in an elastomeric medium. A “metal post” is a discrete support structure; Waite’s conductive elements are loose particles dispersed within a stretchy elastomer, incapable of standing alone and conductive only when compressed. EX1010 at 4:17–19, 4:65–5:1. The Petition cannot simultaneously urge that “metal pillar” means a columnar post or via and map that term onto loose particles in a stretchy elastomer. Its Ground 9 mapping is irreconcilable with the construction it asks the Board to adopt.

3. The Elenius declaration does not cure the gap.

For limitations 1[h] and 1[i], Mr. Elenius does no more than restate the Petition’s mapping of conductive elements 302 to the claimed metal pillars.

Compare Pet. at 104 with EX1003 ¶ 326. He offers no reasoning explaining how particulate matter suspended in a compressible elastomer qualifies as the “columnar metal structure, such as a metal post or via” that his own construction requires. EX1003 ¶ 77. Testimony that “merely parrots the words in the Petition” is entitled to little or no weight and cannot establish a reasonable likelihood of prevailing. *One World Techs., Inc. v. Chevron (HK) Ltd.*, PGR2020-00059, 2020 WL 7222691, at *16 (P.T.A.B. Dec. 7, 2020); 37 C.F.R. § 42.65(a); *Xerox*, Paper 9 at 15.

Because Waite’s conductive elastomer particles are not the “metal pillars” required by limitations 1[h] and 1[i], and every challenged claim depends from claim 1, Ground 9 is not reasonably likely to prevail.

VI. CONCLUSION

For any of these reasons, the Board should deny institution of the Petition.

Respectfully submitted,

Dated: July 2, 2026

/s/ Sean Keller

Sean Keller
Reg. No. 83,409
Attorney for Patent Owner
TopWire, LLC

AHMAD ZAVITSANOS & MENSING PLLC
2001 Ross Avenue, Suite 520
Dallas, TX 75201
Telephone: (214) 800-4501
Facsimile: (713) 655-0062

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITS

Pursuant to §42.24(d) and the Director's Memorandum on Interim Processes for PTAB Workload Management, the undersigned certifies that this paper contains no more than 14,000 words, not including the portions of the paper exempted by §42.24(b). According to the word-processing system used to prepare this paper, the paper contains 8,023 words.

Dated: July 2, 2026

/s/ Sean Keller

Sean Keller
Reg. No. 83,409
Attorney for Patent Owner
TopWire, LLC

AHMAD ZAVITSANOS & MENSING PLLC
2001 Ross Avenue, Suite 520
Dallas, TX 75201
Telephone: (214) 800-4501
Facsimile: (713) 655-0062

CERTIFICATE OF SERVICE

I hereby certify that the foregoing document and Exhibits listed on Patent Owner's Exhibit List were served on July 2, 2026, by electronic mail to the following:

Lead Counsel	Back-up Counsel
Eliot D. Williams, Reg. No. 50,822 Baker Botts L.L.P. 700 K Street, N.W. Washington, D.C. 20001-5692 Phone: 202.639.1334 Fax: 202.639.7890 eliot.williams@bakerbotts.com	Neil Sirota, Reg. No. 38,306 Baker Botts L.L.P. 30 Rockefeller Plaza, Ste 4340 New York, NY 10112-4498 Phone: 212.408.2548 Fax: 212.259.2548 neil.sirota@bakerbotts.com Frank Zhu, Reg. No. 71,214 Baker Botts L.L.P. 30 Rockefeller Plaza, Ste 4340 New York, NY 10112-4498 Phone: 212.408.2639 Fax: 212.259.2439 frank.zhu@bakerbotts.com Coleman Strine, Reg. No. 79,981 Baker Botts L.L.P. 30 Rockefeller Plaza, Ste 4340 New York, NY 10112-4498 Phone: 212.408.2595 coleman.strine@bakerbotts.com Pilseon Yoo (pro hac vice forthcoming) Baker Botts L.L.P. 101 California Street, Ste 3200 San Francisco, CA 94111 Phone: 415.291.6206 pilseon.yoo@bakerbotts.com

Respectfully submitted,

Dated: July 2, 2026

/s/ Sean Keller

Sean Keller
Reg. No. 83,409
Attorney for Patent Owner
TopWire, LLC

AHMAD ZAVITSANOS & MENSING PLLC
2001 Ross Avenue, Suite 520
Dallas, TX 75201
Telephone: (214) 800-4501
Facsimile: (713) 655-0062