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Loctite Eccobond LCM 1000AG-1 for Overmolding of 2.5D Packages



Overmolding Solutions for 2.5D Semiconductor Packages in Advanced Electronics

📅 August 26, 2025 (https://blog.caplinq.com/overmolding-solutions-for-2-5d-semiconductor-packages-in-advanced-electronics_10574/) 👤 Rose Anne Acedera (<https://blog.caplinq.com/author/roseanne/>)

From 1965 to 2010, 2D packaging, also called planar integration, was the main way to assemble integrated circuits. In this method, chips sit side-by-side on a substrate or PCB. Manufacturers connect them using wire bonding or **flip chip** (<https://www.caplinq.com/semiconductors/advanced-packaging/flip-chip-csp/>). During this time, Moore's Law drove device scaling. Intel co-founder Gordon Moore introduced this idea in 1965. In his article *Cramming More Components onto Integrated Circuits*, he observed that from 1958 to 1965, the number of components on a chip doubled every year. He predicted this trend would last for at least another decade. By 1975, the pattern continued, but Moore updated his forecast. He expected **transistor counts to double every two years**.

(<https://www.caplinq.com/semiconductors/transistors/transistor-outline-to/>) This is the version of Moore's Law we know today.

As the number of transistors on chips grew, the feature sizes on those chips steadily decreased. Each generation of process technology is labeled by its technology node, which was historically linked to the smallest feature size that could be reliably made on a chip. In the early decades of 2D packaging, shrinking the technology node brought clear benefits to performance, efficiency, and cost.

Higher Performance

Smaller transistor features, i.e., shorter gate lengths, **reduce the distance electrons needed to travel**. This enables faster transistor switching speeds. For example, at the 250 nm node, CPUs typically ran at about 500 MHz. By the 90 nm node, CPUs could reach over 3 GHz. Faster switching meant higher clock speeds and usually better efficiency.

Lower Power Consumption

Under ideal scaling (pre-2000s), smaller transistors meant each transistor used less power, allowing more transistors to be added without dramatically increasing the total power of the chip. Dynamic power, which is the main power draw during switching, follows the equation:

$$P = \alpha \cdot C \cdot V^2 \cdot f$$

where **α** is the activity factor, **C** is capacitance, **V** is supply voltage, and **f** is switching frequency.

When transistors shrink, capacitance decreases and supply voltage is scaled down. Because power depends on V^2 , even small drops in voltage significantly reduce power use.

Low Cost

Smaller transistors meant more could fit on the same wafer area. Since **wafer processing** (<https://www.caplinq.com/semiconductors/wafers/wafer-backgrinding/>) cost per area was relatively fixed, **cost per transistor dropped sharply**.

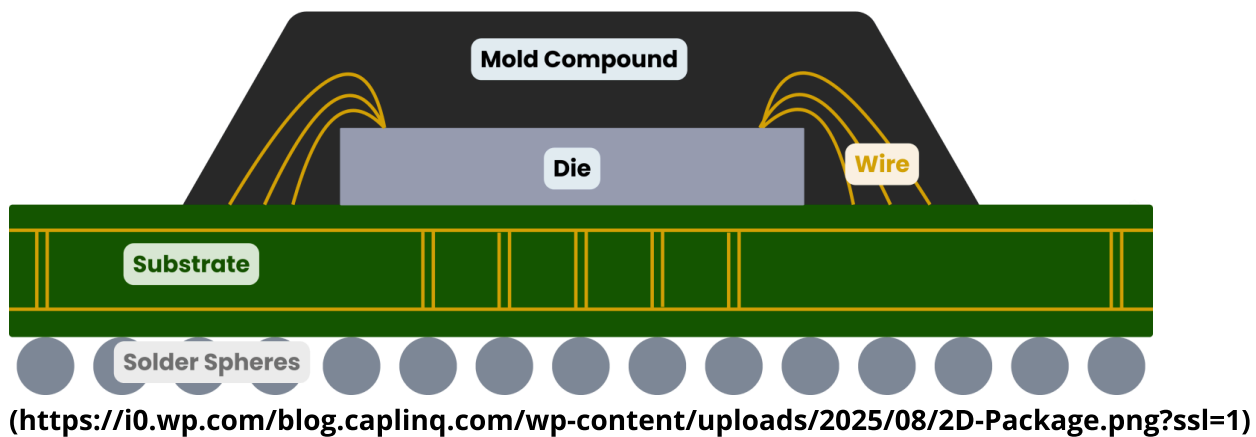
Initially, shrinking the node was a triple win: faster, cheaper, and more power-efficient chips every generation. But, this did not go on forever.

In 2011, the 28 nm node marked a turning point. At this scale, planar transistors began facing short-channel effects. Leakage currents increased as gate lengths shrank, raising static power consumption even at lower supply voltages. Lithography was also hitting its limits. In the past, each shrink made transistors significantly cheaper, but at 28 nm, the cost per transistor still dropped but at a rate far less than before. The benefits of scaling were slowing, and Moore's Law was starting to break down. This slowdown drove the adoption of other packaging technologies.

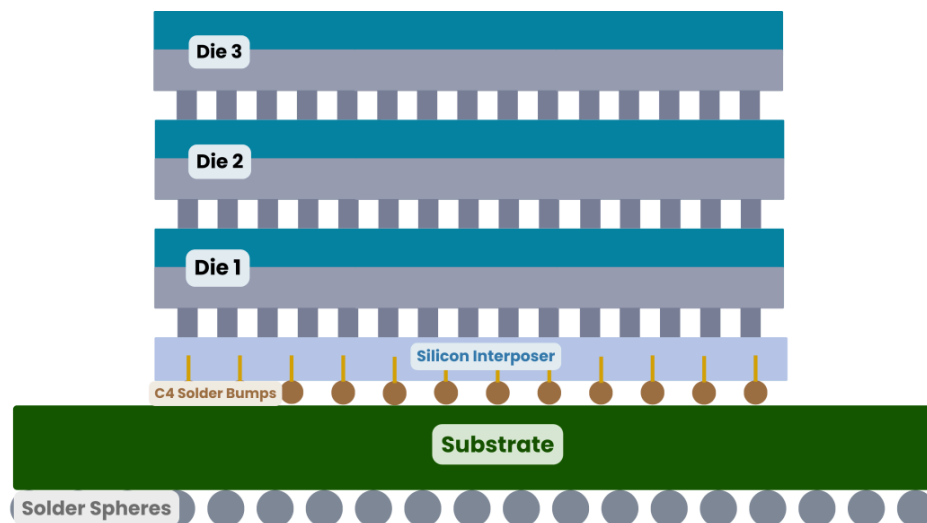
In this blog, we'll take a closer look at **2.5D packaging**, one of the most innovative semiconductor packaging methods driving today's high-performance computing and advanced electronics. We'll explore how 2.5D packaging works, its key advantages and limitations, the common challenges manufacturers face, and the critical materials that make this technology possible.

What is 2.5D Packaging?

In 2D packaging, the chips are connected on a printed circuit board, whereas in true 3D packaging, the chips are stacked vertically using through-silicon vias (TSVs).



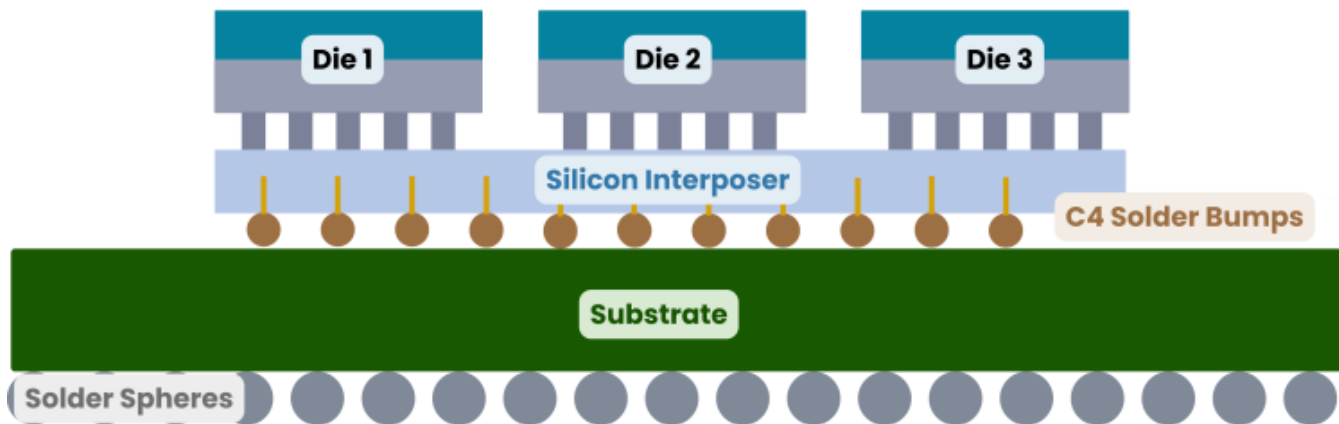
2D Packaging



(<https://i0.wp.com/blog.caplinq.com/wp-content/uploads/2025/08/3D-Package-1.png?ssl=1>)

3D Packaging

2.5D packaging then **serves as an intermediary between the traditional 2D and advanced 3D packaging technologies**. In this semiconductor integration method, multiple chips, such as logic, memory, and analog, are placed side-by-side on a high-density interposer. The dies remain in a single horizontal plane but achieve near-3D performance because of the extremely fine-pitch connections between the chips.



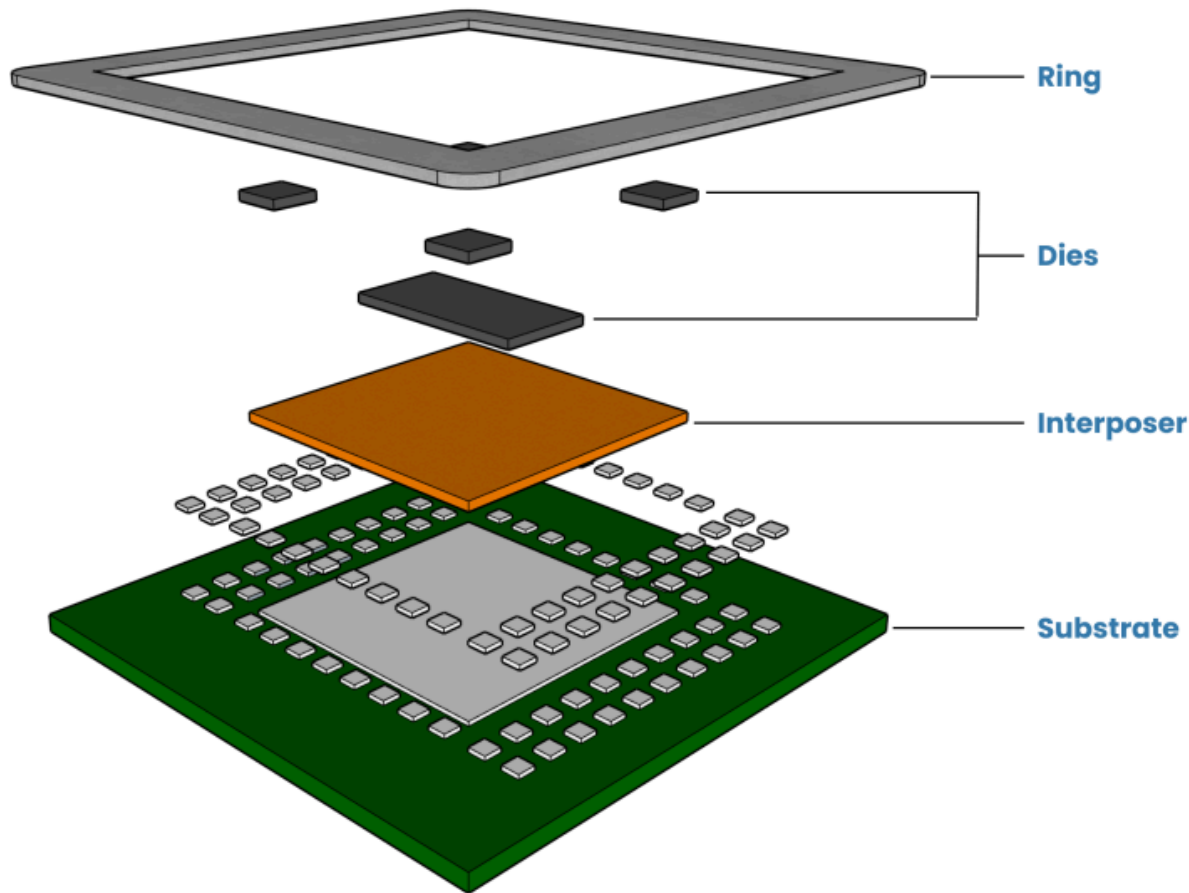
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2.5D Packaging

Feature	2D Packaging	2.5D Packaging	3D Packaging
Interconnect Density	Low (PCB limited)	High (interposer RDL)	Very high (die-to-die TSV)
Thermal Management	Good	Good–Better than 3D	Challenging (stacked dies trap heat)
Latency / Bandwidth	Moderate	High	Very high
Design Flexibility	Moderate	High (mix node sizes, chiplets)	Lower (stacked height and TSV constraints)
Manufacturing Complexity	Low	Moderate	High

Comparative advantages of 2D, 2.5D, and 3D packaging technologies in terms of interconnect density, thermal management, performance, design flexibility, and manufacturing complexity

What is the Structure of 2.5D Packages?



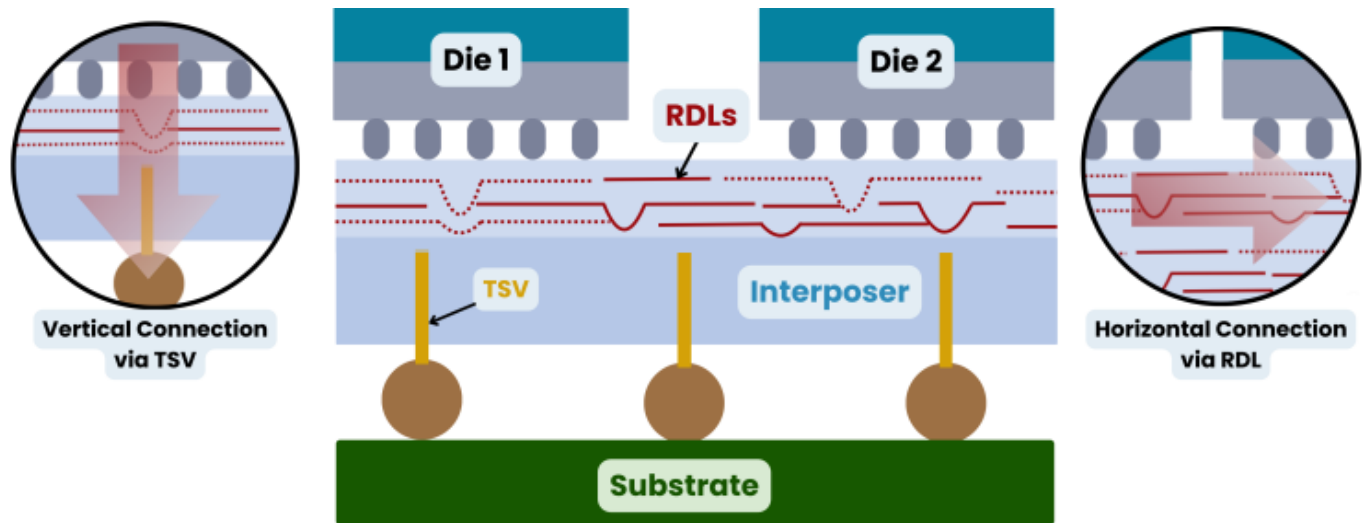
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Components of 2.5D Devices

2.5D devices are built around an **interposer**, a thin substrate made of silicon, glass, or organic materials. It contains horizontal connection elements such as redistribution layers (RDLs), or ultra-fine metal traces that route signals between dies, and microbump pads, which connect each die's input/output (I/O) pads to the RDLs. These elements enable short, high-bandwidth die-to-die communication without passing through the PCB.

The interposer also contains vertical connection elements. In silicon interposers, these are through-silicon vias (TSVs) or metal-filled holes drilled vertically through the substrate that create direct electrical pathways between the top and bottom surfaces. This vertical routing allows signals and power to pass between layers, connecting the dies to the **package substrate** (<https://www.caplinq.com/electronics-assembly/substrates/>) and ultimately to the **printed circuit board (PCB)** (<https://www.caplinq.com/electronics-assembly/substrates/printed-circuit-boards-pcbs/>).

Now, combining the horizontal and vertical connection elements in the interposer creates a dense, three-dimensional routing network. They enable 2.5D devices to achieve high bandwidth, low latency, and efficient integration without the complexity of full 3D stacking.



(<https://i0.wp.com/blog.caplinq.com/wp-content/uploads/2025/08/Horizontal-and-Vertical-Connection-Elements-in-Interposers.png?ssl=1>)

Horizontal and vertical connection elements within a 2.5D interposer, enabling signal routing between dies and the substrate

The dies are connected to the interposer using fine-pitch solder bumps (often <50 µm). The interposer is then connected to the package substrate using C4 solder bumps. An **underfill** (<http://www.caplinq.com/underfills.html>) is applied between the die and interposer to improve mechanical reliability. Finally, the entire assembly is encapsulated or overmolded to protect the 2.5D device from environmental and mechanical stress.

What Are the Benefits and Applications of 2.5D Packaging?

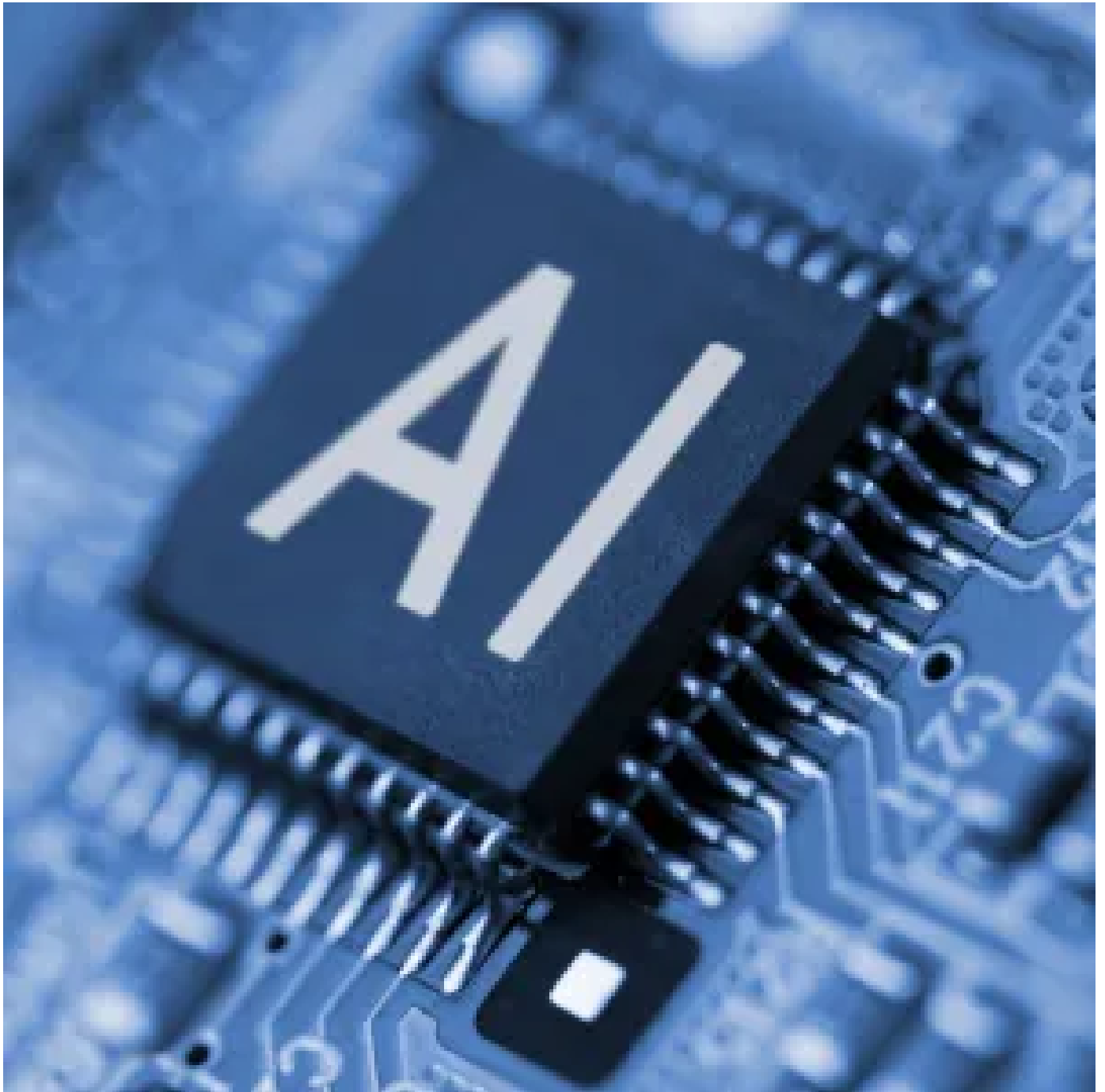
Because of their structure, 2.5D devices offer several advantages over traditional packaging. By placing multiple chips side-by-side on a silicon interposer, they enable higher interconnect density and shorter signal paths. This translates to faster data transfer, lower latency, and better power efficiency. The architecture also allows integration of different chip types into one package, improving performance while reducing overall footprint.

That is why, today, 2.5D packaging is widely used in high-performance computing (HPC), artificial intelligence (AI) accelerators, data center processors, and advanced GPUs where massive bandwidth and fast die-to-die communication are critical. It is also increasingly adopted in networking equipment and 5G infrastructure to handle large data throughput with minimal latency.



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Advanced GPUs

These are exactly the kinds of advanced computing applications Gordon Moore had in mind when he talked about the exponential growth of semiconductor capability. What was once just a projection is now the reality we are living in.

In these applications, every component in the package has an important role in ensuring performance and reliability. Among these, the overmolding process is a critical final step, providing the mechanical protection, moisture barrier, and thermal stability needed to protect the device throughout its operational life.

Why is Overmolding Important for 2.5D Packaging?

Overmolding in 2.5D packaging seals the entire assembly inside a protective molding compound. It protects delicate structures like fine-pitch microbumps, TSVs, and redistribution layers from mechanical stress, moisture, and contamination, while also helping control thermal expansion to maintain package integrity over time, similar to how **epoxy molding compounds**

(<https://www.caplinq.com/semiconductor-epoxy-mold-compounds.html>) protect and encapsulate 2D packages.

The materials used for overmolding 2.5D devices must meet strict requirements:

- Low stress on interconnects
- CTE compatibility with the interposer and substrate
- Excellent flow into narrow gaps
- Moisture resistance, thermal stability, electrical insulation
- Proven reliability under thermal and mechanical cycling.

The challenge is that 2.5D packages have ultrafine or ultras-small gaps between components, especially around dense microbump arrays and TSV structures. Standard molding compounds can have difficulty flowing into these spaces without trapping voids or damaging connections. This creates a **unique requirement for 2.5D overmolding: the use of ultrafine fillers**. These fillers maintain the necessary mechanical and thermal performance while allowing the compound to penetrate tight spaces and fully encapsulate the assembly without defects.

This is why choosing the right overmolding compound is so important. Not many materials can meet the combined demands of low stress, tight CTE control, and ultrafine filler technology needed for reliable 2.5D encapsulation.

Henkel Loctite Eccobond LCM 1000AG-1 for Overmolding 2.5D Devices

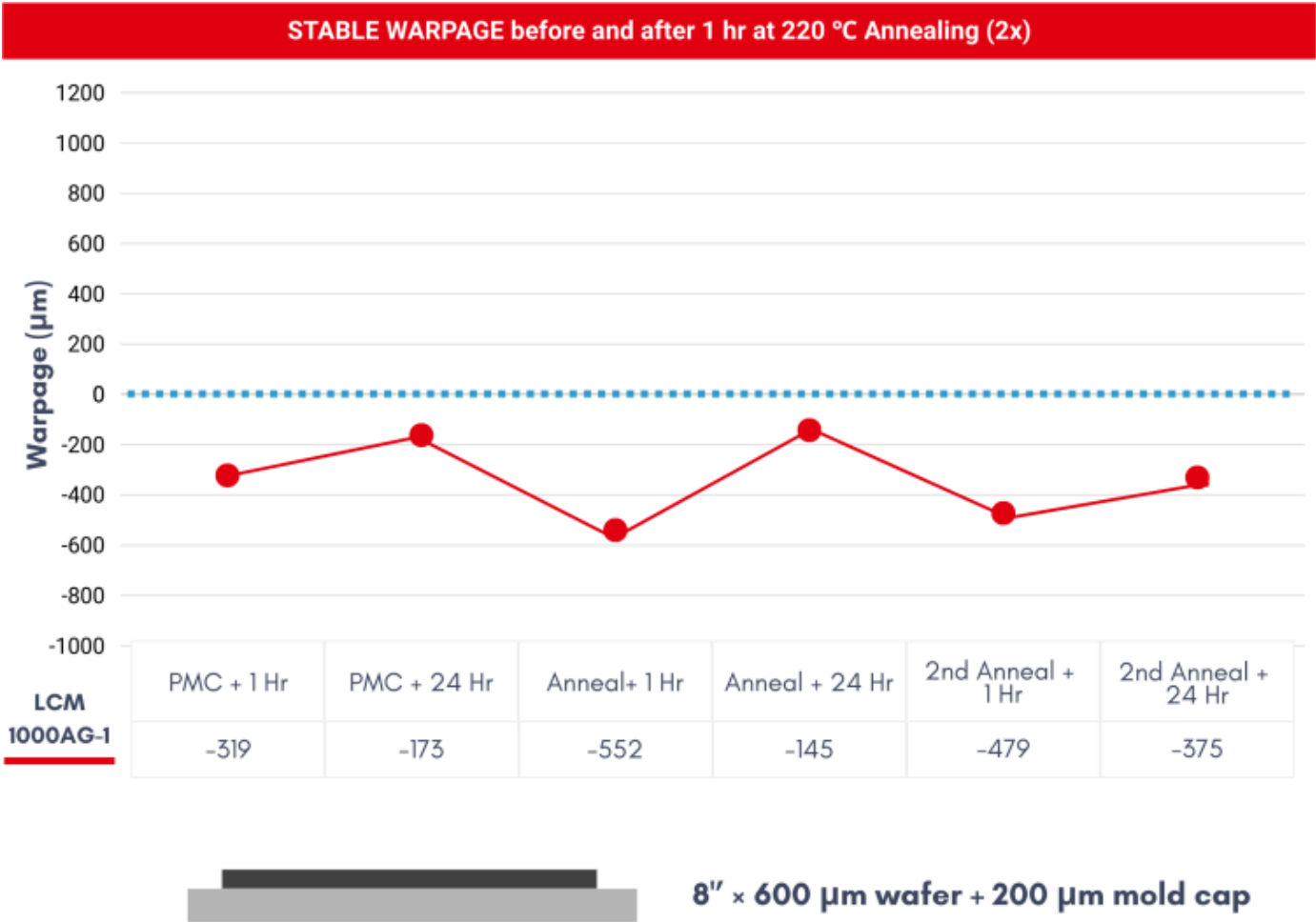
Loctite Eccobond LCM 1000AG-1 (<https://www.caplinq.com/loctite-eccobond-lcm-1000ag-1-wafer-level-encapsulant-for-cow-2.5d-lcm1000ag-1.html>) is an epoxy-amine liquid compression molding compound specifically developed for liquid compression molding of wafer-level packages (WLP) and the overmolding of fan-out WLP (FO-WLP). Three key properties and features give LCM 1000AG1 a distinct edge over other liquid compression molding products.

Ultra-low Warpage – Enabling Better Reliability and Higher Yield

When tested on an 8-inch wafer, LCM 1000AG1 demonstrated exceptional dimensional stability, with an **extremely low wafer warpage of 0.39 mm** after post-mold curing. Remarkably, the wafer maintained its flatness even after undergoing two consecutive annealing cycles at 220 °C, conditions designed to

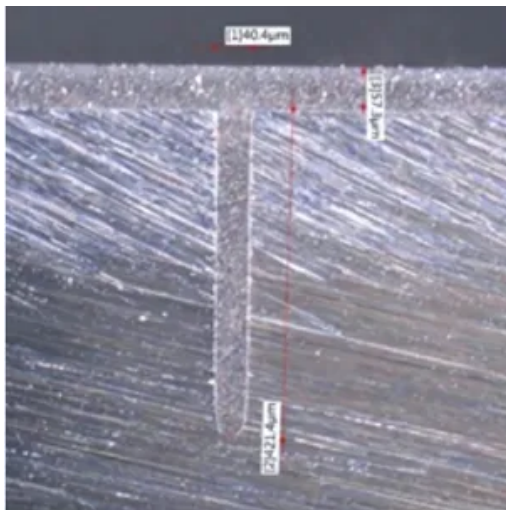
simulate the stress and thermal exposure of the redistribution layer (RDL) process. This performance not only meets but also surpasses that of the leading Japanese POR product.

This is critical because low warpage prevents stress buildup within the package, ensuring that no surface is subjected to excessive compression or tension. As a result, the package stays intact and delivers better long-term reliability. This property makes LCM1000AG-1 an ideal solution for high-density and large-body 2.5D packages.



(<https://i0.wp.com/blog.caplinq.com/wp-content/uploads/2025/08/Low-Warpage.png?ssl=1>)
Low warpage results of a wafer molded with Henkel Loctite ECCOBOND LCM 1000AG-1, demonstrating stability even after two annealing cycles at 220 °C

Ultra-fine Filler – Enabling Void-free Fine Gap Filling



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LCM 1000AG-1 is a solvent-free encapsulant with ultra-fine fillers, ideal for 2.5D devices with ultrasmall gaps between components. The fine filler particles (average 3 µm, upper cut 10 µm) enable fast flow rates and void-free trench filling, ensuring **complete coverage, protection**, and long-term reliability. In a testing, a 40 µm-wide by 400 µm-deep trench was fully filled with no voids using this next-generation LCM material.

Non-Anhydride, SVHC-Free Formulation – Enabling Safer Processing and Regulatory Compliance

In our previous blog, ***SVHC-Free Encapsulants for Semiconductor Applications*** (https://blog.caplinq.com/svhc-free-encapsulants-for-semiconductor-applications_6289/), we discussed that the push towards safer and more sustainable materials has intensified across different industries. One critical area of focus is the use of Substances of Very High Concern (SVHC). According to the European Chemicals Agency (ECHA), SVHC are hazardous to human life and the environment. SVHCs include substances that are carcinogenic, mutagenic, or reprotoxic (CMR) in Category 1A or 1B, as well as those that are persistent, bioaccumulative, and toxic (PBT) or very persistent and very bioaccumulative (vPvB) under REACH criteria. They also cover, on a case-by-case basis, other substances that present an equivalent level of concern, such as endocrine disruptors.

Traditional LCM materials use anhydride as a curing agent, but many aromatic and some alicyclic anhydrides are classified as respiratory and skin sensitizers and are listed as REACH SVHCs. **LCM 1000AG-1 is both anhydride-free and SVHC-free**, simplifying compliance with REACH, RoHS, and customer-specific green procurement standards. Advances in alternative curing systems, such as modified amine in LCM 1000AG-1, now match or even exceed the electrical and thermal performance of anhydride-based systems.

The amine curing agent also enables a significantly faster in-mold cure time: just five minutes compared to the typical ten minutes required by anhydride-based LCM encapsulants. This rapid curing capability allows advanced packaging manufacturers to more than double production throughput and increase units per hour (UPH), delivering higher efficiency in 2.5D and **wafer-level packaging** (<http://www.caplinq.com/wafer-level-packaging.html>) processes.

Molding # of Wafer	Anhydride LCM: Time (min)	Henkel LCM: Time (min)	Time Saving (%)
1	70	65	7%
10	160	110	31%
100	1060	560	47%
1,000	10,060	5,060	50%
	Anhydride LCM	HENKEL LCM	
In-mold-cure (min)	10	5	
Post-mold-cure (min)	60	60	

(<https://i0.wp.com/blog.caplinq.com/wp-content/uploads/2025/08/image.png?ssl=1>)

Comparison of cure times between traditional anhydride-based LCM and Henkel's LOCTITE ECCOBOND LCM 1000AG-1. The amine-based system reduces in-mold cure time from 10 minutes to 5 minutes, resulting in up to 50% total time savings across high wafer volumes and significantly improving throughput.

With its dimensional stability, ultra-fine filler technology, and environmentally safer formulation, Henkel Loctite Eccobond LCM 1000AG-1 sets a new standard for 2.5D overmolding. It delivers the mechanical protection, thermal stability, and regulatory compliance that advanced electronics demand.

Contact us today to discuss your application needs, request technical support, or obtain samples, and take your next-generation designs to higher reliability and yield.

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About Rose Anne Acedera

Rose Anne is a Technical Applications Engineer with a background in electrochemical materials and energy storage technologies. She works with engineers and product teams on materials for batteries, fuel cells, and electrolyzers, with a focus on connecting material properties to real device performance. A strong believer in clarity, she enjoys breaking down complex technical topics so they are easier to understand and apply.

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